contact via 92 to the optoelectronic device 160. The heat may be transferred from a heat sink (not shown) to the at least one first metal contact via 90 and the at least one second metal contact via 92 through metallic interconnect structures embedded in the interconnect-level dielectric material layer 80, then subsequently transferred to the optoelectronic device 160.

Therefore, by reversing the direction of flow of the electrical current, the direction of heat transfer may be reversed. Further, by adjusting the magnitude of the electrical current, the amount of heat transfer may be regulated. Typically, the material of the low-k dielectric material portion 150 has a lower thermal conductivity than the material of the buried insulator layer 20, thereby increasing the thermal isolation of the at least one first metal semiconductor alloy portion 140 and the optoelectronic device 160 from the handle substrate 10.

The first semiconductor device may be operated with a feedback mechanism for performance of the optoelectronic device 160. For example, the performance of the optoelectronic device 160 may be monitored during operation. Based on the monitored performance level of the optoelectronic device, a direction of the electrical current or magnitude of the electrical current may be manipulated to heat or cool the optoelectronic device, thereby reducing deviation in the performance of the optoelectronic device 160 from a target performance level.

Referring to FIG. 17, a third exemplary semiconductor structure according to a third embodiment of the present invention is derived from the second exemplary semiconductor structure by forming a substantially intrinsic lower semiconductor portion 30 and a substantially intrinsic upper semiconductor portion 138 in each temperature control device. A vertically abutting pair of a substantially intrinsic lower semiconductor portion 30 and a substantially intrinsic upper semiconductor portion 138 is herein referred to as a substantially intrinsic semiconductor portion (30, 138). Thus, each of the at least one temperature control device may include the substantially intrinsic semiconductor portion 30.

The substantially intrinsic semiconductor portion (30, 138) is formed between a p-doped semiconductor portion (131, 132) and an n-doped semiconductor portion (133, 134) of the at

SAMSUNG EX. 1002 - 3812/4148

least one temperature control device (90, 142, 131, 132, 140, 30, 138, 133, 134, 144, 92). The substantially intrinsic semiconductor portion (30, 138) may have the same composition as the semiconductor waveguide 136. The substantially intrinsic semiconductor portion (30, 138) vertically abuts the first metal semiconductor alloy region 140 of the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). In one case, the p-doped semiconductor portion (131, 132) and the n-doped semiconductor portion (133, 134) may be not abut each other, and are laterally separated by the substantially intrinsic semiconductor portion (30, 138). In another case, the p-doped semiconductor portion (131, 132) and the n-doped semiconductor portion (133, 134) may abut each other and the substantially intrinsic semiconductor portion (30, 138).

A low-k dielectric material portion 150, an optoelectronic device 160, an interconnect-level dielectric material layer 80, at least one compound semiconductor via 85, at least one first metal contact via 90, and at least one second metal contact via 92 may be formed in the same manner as in the second embodiment. Within the collective volume of the at least one substantially intrinsic semiconductor portion (30, 138) and the at least one first metal semiconductor alloy region 140, the current flows primarily through the at least one first metal semiconductor alloy region 140. Therefore, the addition of the at least one substantially intrinsic semiconductor portion (30, 138) does not change the current path in a substantial manner relative to the current path in the second embodiment. The at least one temperature control device (90, 142, 131, 132, 140, 30, 138, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

Referring to FIG. 18, a fourth exemplary semiconductor structure according to a fourth embodiment of the present invention is shown. The fourth exemplary semiconductor structure is derived from the second exemplary semiconductor structure of FIGS. 13A and 4B by omitting the steps corresponding to FIGS. 14A and 5B in the processing sequence. Specifically, application of a photoresist 147, patterning of the photoresist 147, and transfer of the pattern in the photoresist 147 into an exposed portion of the buried insulator layer 20 are omitted in the third embodiment.

SAMSUNG EX. 1002 - 3813/4148

Instead of patterning the buried insulator layer 20, a lower portion of an interconnect-level dielectric material layer 80 is formed over the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) and the semiconductor waveguide 136. The top surface of the lower portion of the interconnect-level dielectric material layer 80 is planarized by employing a self-planarizing material for the lower portion of the interconnect-level dielectric material layer 80 and/or by performing a planarization processing step such as chemical mechanical planarization or a recess etch. An optoelectronic device 160 is formed over the top surface of the lower portion of the interconnect-level dielectric material layer 80. The optoelectronic device 160 may be the same as in the second embodiment, and may overlie the at least one first metal semiconductor alloy region 140 and a portion of the semiconductor waveguide 136. An upper portion of the interconnect-level dielectric material layer 80 is formed over the optoelectronic device 160. The lower portion and the upper portion of the interconnect-level dielectric material layer 80 may comprise the same material as in the second embodiment. At least one compound semiconductor via 85, at least one first metal contact via 90, and at least one second metal contact via 92 may be formed in the same manner as in the second embodiment. The at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

Referring to FIG. 19, a fifth exemplary semiconductor structure according to a fifth embodiment of the present invention is derived from the second exemplary semiconductor structure by omitting formation of at least one compound semiconductor via 85.

Referring to FIG. 20, a sixth exemplary semiconductor structure according to a sixth embodiment of the present invention is derived from the second exemplary semiconductor structure at a step corresponding to FIGS. 14A and 5B by removing the photoresist 147 and employing a non-conformal deposition process to form a low-k dielectric material portion 150. The material of the low-k dielectric material portion 150 may be the same as in the second embodiment. The non-conformal property of the deposition process employed to form the low-k dielectric material portion 150 deposits a low-k dielectric material over

SAMSUNG EX. 1002 - 3814/4148

narrow portions of the of the semiconductor structures above the top surface of the buried insulator layer 20, i.e., between the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) and the semiconductor waveguide 136. Thus a cavity 152 is formed within the low-k dielectric material portion 150.

Referring to FIG. 21, processing steps corresponding to FIGS. 15A – 7B of the second embodiment are performed on the sixth exemplary semiconductor structure. The cavity 152 may be under vacuum after processing, or may be filled with air or a gas. The cavity 152 has a dielectric constant that is substantially equal to 1.0. The cavity 152 has a lower thermal conductivity than the material of the buried insulator layer 20, thereby increasing the thermal isolation of the at least one first metal semiconductor alloy portion 140 and the optoelectronic device 160 from the handle substrate 10. The at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

Referring to FIG. 22, a seventh exemplary semiconductor structure according to a seventh embodiment of the present invention is shown. FIG. 111 is a top-down view of selected elements including p-doped semiconductor portions (131, 132), n-doped semiconductor portions (133, 134), first metal semiconductor alloy regions 140, second metal semiconductor alloy regions 142, third metal semiconductor alloy regions 144, first metal contact vias 90, second metal contact vias 92, and a semiconductor waveguide 136. The location of the optoelectronic device 160 is shown in a broken line. A vertical cross-sectional view along the plane Z – Z' is the same as FIG. 15A.

Each of the first metal semiconductor alloy regions 140 is located within a first annulus. Each of the p-doped semiconductor portions (131, 132) and n-doped semiconductor portions (133, 134) is located within a second annulus which encloses and abuts the first annulus. Each of the second metal semiconductor alloy regions 142 and the third metal semiconductor alloy regions 144 is located within a third annulus which encloses and abuts the second annulus. The p-doped semiconductor portions (131, 132), the n-doped semiconductor portions (133, 134), the first metal semiconductor alloy regions 140, the second metal

SAMSUNG EX. 1002 - 3815/4148

semiconductor alloy regions 142, and the third metal semiconductor alloy regions 144 constitute two temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92) between which a semiconductor waveguide 136 is located. An optoelectronic device 160 overlies portions of the two temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92) and the semiconductor waveguide 136 as in the second embodiment. The two temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

In general, topological variations may be performed to the at least one temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92 and optionally 30 and 138) to any of the exemplary semiconductor structures described above. Further, additional temperature control devices having a similar structure may be added to any of the exemplary semiconductor structures described above.

While the invention has been described in terms of specific embodiments, it is evident in view of the foregoing description that numerous alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the invention is intended to encompass all such alternatives, modifications and variations which fall within the scope and spirit of the invention and the following claims.

SAMSUNG EX. 1002 - 3816/4148

CLAIMS

1. A semiconductor structure comprising:

a semiconductor waveguide having a first thickness and located on a top surface of an insulator layer;

a recessed semiconductor region of integral construction with said semiconductor waveguide, having a second thickness that is less than said first thickness, located on said insulator layer, and including a substantially undoped recessed semiconductor region;

a p-doped semiconductor region laterally abutting said substantially undoped recessed semiconductor region;

an n-doped semiconductor region laterally abutting said substantially undoped recessed semiconductor region and not abutting said p-doped semiconductor region; and

a recessed metal semiconductor alloy portion abutting said recessed semiconductor region, said p-doped semiconductor region, and said n-doped semiconductor region.

2. The semiconductor structure of Claim 1, wherein said semiconductor waveguide, said recessed semiconductor portion, said p-doped semiconductor portion, and said n-doped semiconductor portion comprise a same semiconductor material.

3. The semiconductor structure of Claim 1 or Claim 2, wherein said semiconductor waveguide, said recessed semiconductor portion, said p-doped semiconductor portion, and said n-doped semiconductor portion are single crystalline and are epitaxially aligned among one another.

4. The semiconductor structure of any preceding Claims, wherein said semiconductor waveguide comprises substantially undoped silicon or substantially undoped germanium.

5. The semiconductor structure of any preceding Claims, wherein said recessed semiconductor region includes a p-doped recessed semiconductor region which is a portion of said p-doped semiconductor region and an n-doped recessed semiconductor region which is a portion of said n-doped semiconductor region.

SAMSUNG EX. 1002 - 3817/4148

6. The semiconductor structure of any preceding Claims, further comprising:

another recessed semiconductor region of integral construction with said semiconductor waveguide, having said second thickness, located on said insulator layer, and including another substantially undoped recessed semiconductor region;

another p-doped semiconductor region laterally abutting said other substantially undoped recessed semiconductor region;

another n-doped semiconductor region laterally abutting said other substantially undoped recessed semiconductor region and not abutting said other p-doped semiconductor region; and

another recessed metal semiconductor alloy portion abutting said other recessed semiconductor region, said other p-doped semiconductor region, and said other n-doped semiconductor region, wherein said other recessed semiconductor region, said other p-doped semiconductor region, said other n-doped semiconductor region, and said other recessed metal semiconductor alloy portion are located on an opposite side of said recessed semiconductor region, said p-doped semiconductor region, said n-doped semiconductor region, and said recessed metal semiconductor alloy portion about said semiconductor waveguide.

7. A method of forming a semiconductor structure comprising:

forming shallow trench isolation structures laterally abutting a top semiconductor portion and vertically abutting a buried insulator layer in a top semiconductor layer of a semiconductor-on-insulator (SOI) substrate;

forming a semiconductor waveguide by patterning said top semiconductor portion;

forming a p-doped semiconductor region in said top semiconductor portion;

forming an n-doped semiconductor region not abutting said p-doped semiconductor region in said top semiconductor region; and

forming a recessed metal semiconductor alloy portion directly on a recessed region of said top semiconductor portion, wherein said recessed metal semiconductor alloy portion is formed directly on said p-doped semiconductor region and said n-doped semiconductor region.

SAMSUNG EX. 1002 - 3818/4148

8. The method of Claim 7, further comprising forming a pair of recessed line trenches in said top semiconductor portion, wherein a remaining sub-portion of said top semiconductor portion having a first thickness and located between said pair of recessed line trenches constitutes said semiconductor waveguide, wherein sub-portions of said top semiconductor portion directly underneath said pair of line trenches constitute recessed semiconductor regions of integral construction with said semiconductor waveguide having a second thickness that is less than said first thickness, and wherein sidewalls of two sup-portions of said top semiconductor portion having said first thickness are exposed to said pair of recessed line trenches.

9. The method of Claim 8, further comprising:

implanting p-type dopants into an area including one of said two sup-portions of said top semiconductor portion and a portion of one of said recessed semiconductor regions to form said p-doped semiconductor region; and

implanting n-type dopants into an area including the other of said two sup-portions of said top semiconductor portion and another portion of said one of said recessed semiconductor regions to form said n-doped semiconductor region.

10. The method of Claim 9, further comprising:

forming a dielectric layer on said semiconductor waveguide, said recessed semiconductor regions, said p-doped semiconductor region, and said n-doped semiconductor region; and

lithographically patterning said dielectric layer to form a dielectric material portion abutting a top surface and sidewalls of said semiconductor waveguide and a dielectric spacer that abuts a sidewall of said p-doped semiconductor region and a sidewall of said n-doped semiconductor region.

11. A semiconductor structure comprising a temperature control device and an optoelectronic device,

wherein said temperature control device includes:

a first metal semiconductor alloy region located on a substrate;

SAMSUNG EX. 1002 - 3819/4148

a p-doped semiconductor portion abutting said first metal semiconductor alloy region and located on said substrate;

an n-doped semiconductor portion abutting said first metal semiconductor alloy region located on said substrate; wherein said temperature control device is configured to pass current from said p-doped semiconductor portion, through said first metal semiconductor alloy region, and to said n-doped semiconductor portion or from said n-doped semiconductor portion, through said first metal semiconductor alloy region, and to said p-doped semiconductor portion, and

wherein said optoelectronic device includes a device that comprises a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to said temperature control device.

12. The semiconductor structure of Claim 11, wherein said optoelectronic device includes at least one of a laser, optical amplifier, an optical sensor, a waveguide, and a quantum well.

13. The semiconductor structure of Claim 11 or Claim 12, wherein said optoelectronic device includes a III-V compound semiconductor material.

14. The semiconductor structure of any of Claims 11 to 13, further comprising a dielectric material portion comprising a dielectric material and vertically abutting a bottom surface of said p-doped semiconductor portion and a bottom surface of said n-doped semiconductor portion.

15. The semiconductor structure of any of Claims 11 to 14, wherein said p-doped semiconductor portion laterally abuts said n-doped semiconductor portion.

16. The semiconductor structure of any of Claims 11 to 15, further comprising a substantially intrinsic semiconductor portion laterally abutting said p-doped semiconductor portion and said n-doped semiconductor portion and vertically abutting said first metal semiconductor alloy region, wherein said substantially intrinsic semiconductor portion has a resistivity greater than 1 Ohm-cm.

SAMSUNG EX. 1002 - 3820/4148

17. The semiconductor structure of any of Claims 11 to 16, wherein said temperature control device further comprises:

a second metal semiconductor alloy region vertically abutting said p-doped semiconductor portion;

a third metal semiconductor alloy region vertically abutting said n-doped semiconductor portion;

a first metal contact via abutting said second metal semiconductor alloy region; and

a second metal contact via abutting said third metal semiconductor alloy region.

18. A method of forming a semiconductor structure comprising a temperature control device and an optoelectronic device, said method including:

patterning a top semiconductor layer of a semiconductor-on-insulator substrate to form a p-doped semiconductor portion and an n-doped semiconductor portion;

forming a first metal semiconductor alloy region directly on said p-doped semiconductor portion and said n-doped semiconductor portion, wherein said p-doped semiconductor portion and an n-doped semiconductor portion and said first metal semiconductor alloy region constitute a portion of a temperature control device;

forming a current conduction path configured to pass current from said p-doped semiconductor portion, through said first metal semiconductor alloy region, and to said n-doped semiconductor portion or from said n-doped semiconductor portion, through said first metal semiconductor alloy region, and to said p-doped semiconductor portion; and

forming an optoelectronic device comprising a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to said temperature control device.

19. The method of Claim 18, further comprising:

removing a portion of a buried insulator layer underneath a sub-portion of said p-doped semiconductor portion and a sub-portion of said n-doped semiconductor portion to form a trench in said buried insulator layer; and

filling said trench with a low dielectric constant (low-k) material having a dielectric constant less than 3.0, wherein said optoelectronic device is formed over said low-k material.

SAMSUNG EX. 1002 - 3821/4148

20. The method of Claim 18 or Claim 19, further comprising forming a cavity laterally abutting a remaining portion of said buried insulator layer by removing said low-k material selective to said remaining portion of said buried insulator layer.

SAMSUNG EX. 1002 - 3822/4148

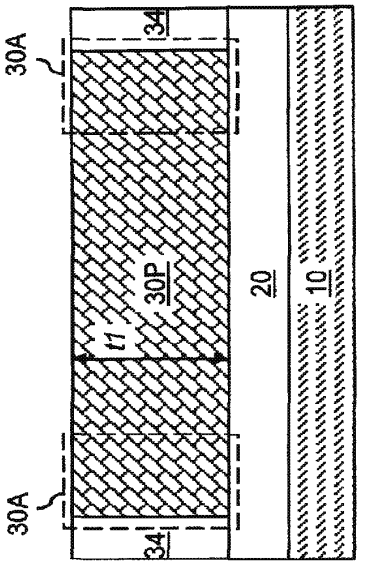


FIG. 1B

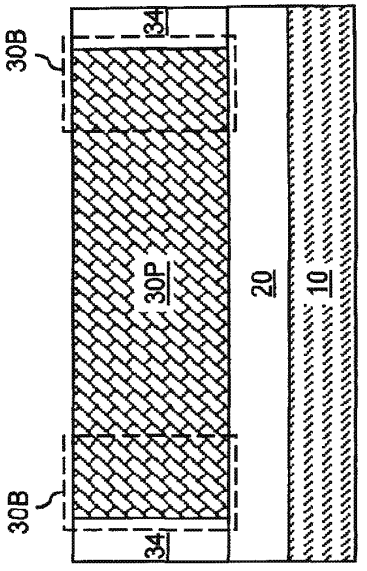


FIG. 1C

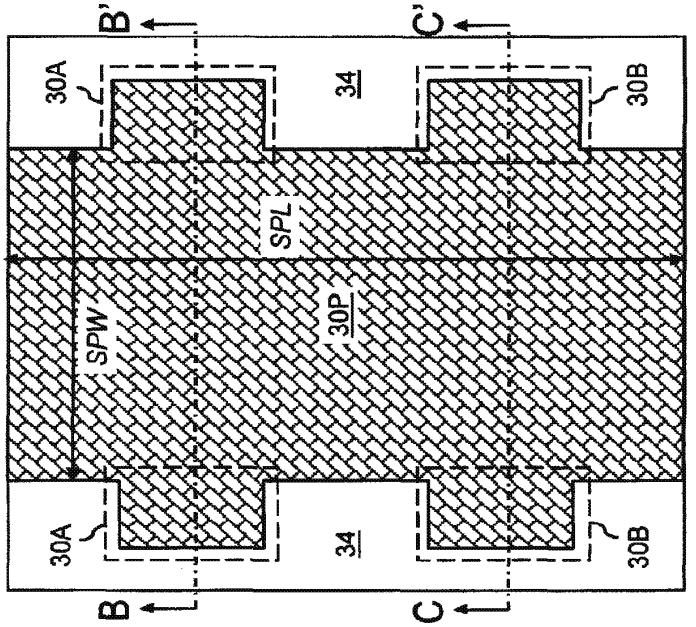


FIG. 1A

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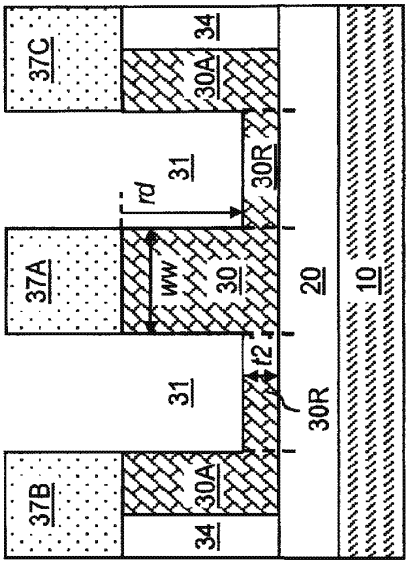


FIG. 2B

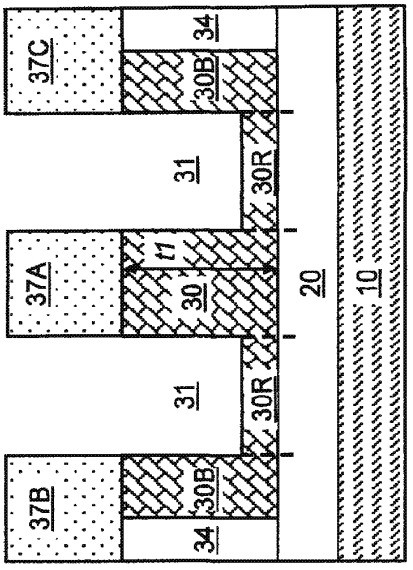


FIG. 2C

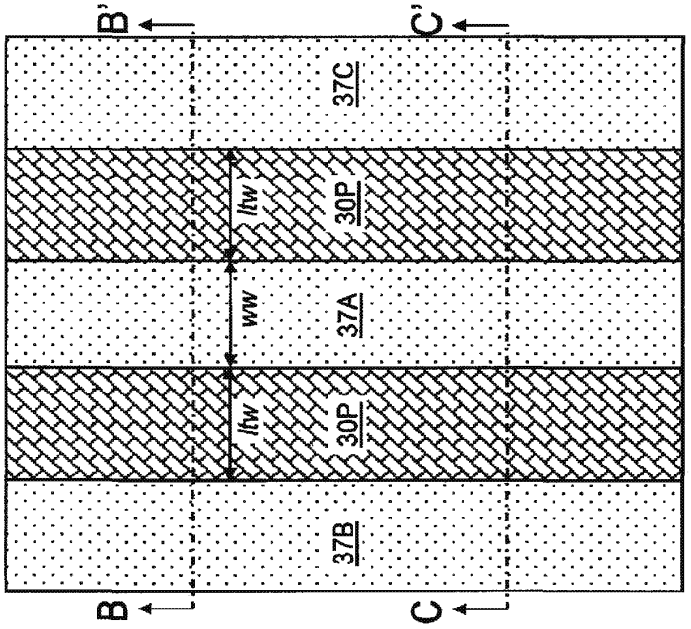


FIG. 2A

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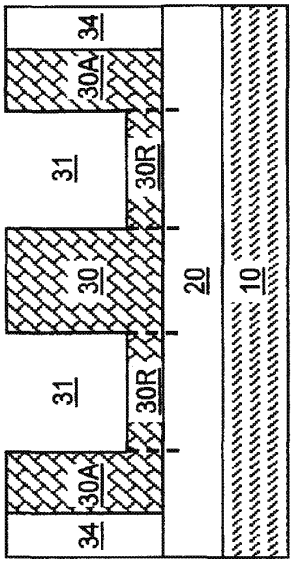


FIG. 3B

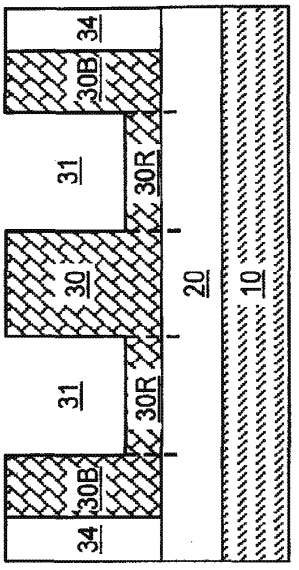


FIG. 3C

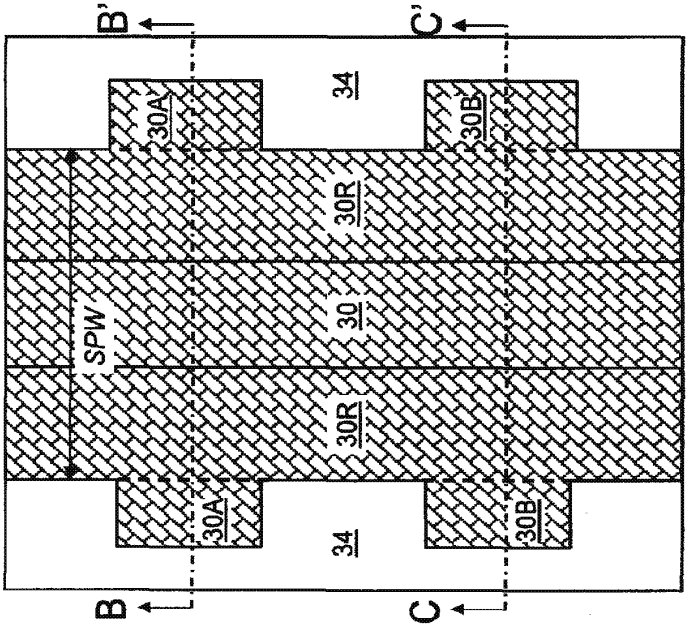


FIG. 3A

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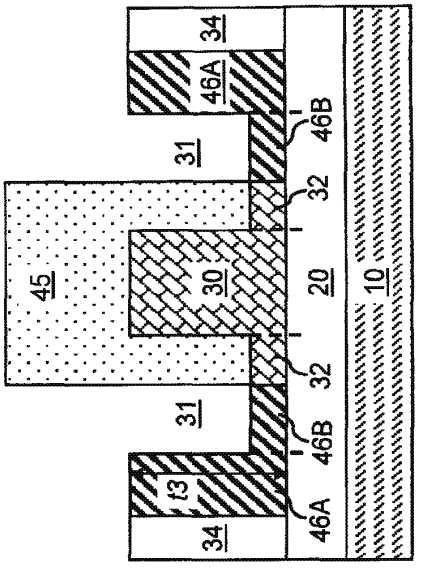


FIG. 4B

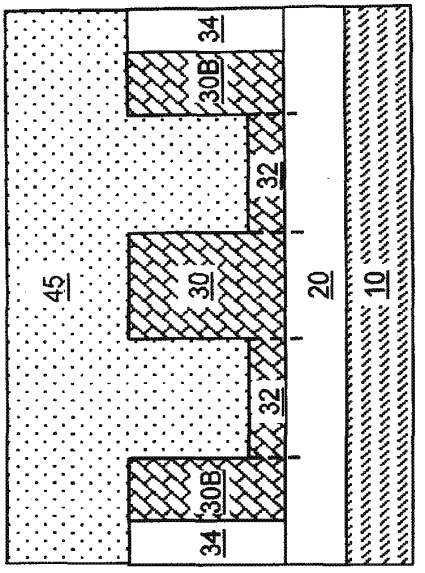


FIG. 4C

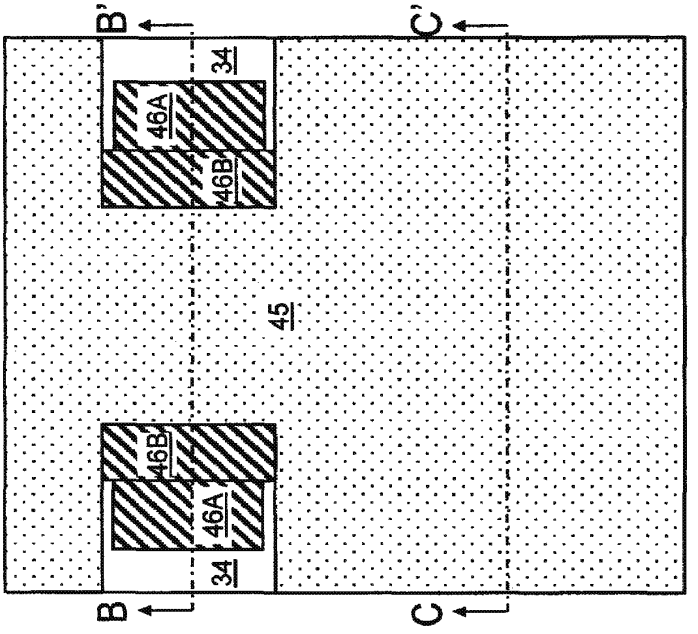


FIG. 4A

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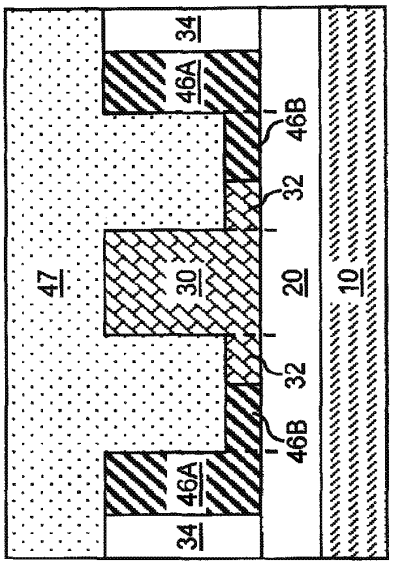


FIG. 5B

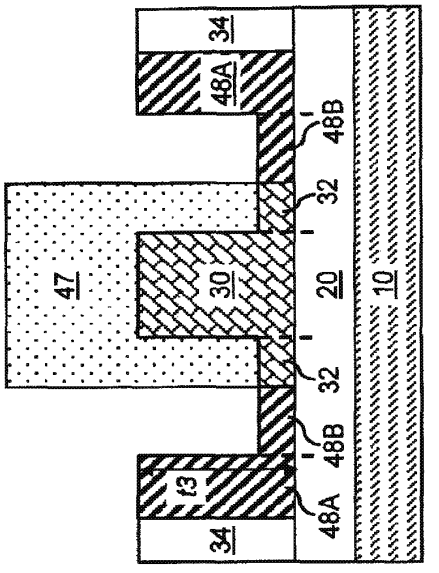


FIG. 5C

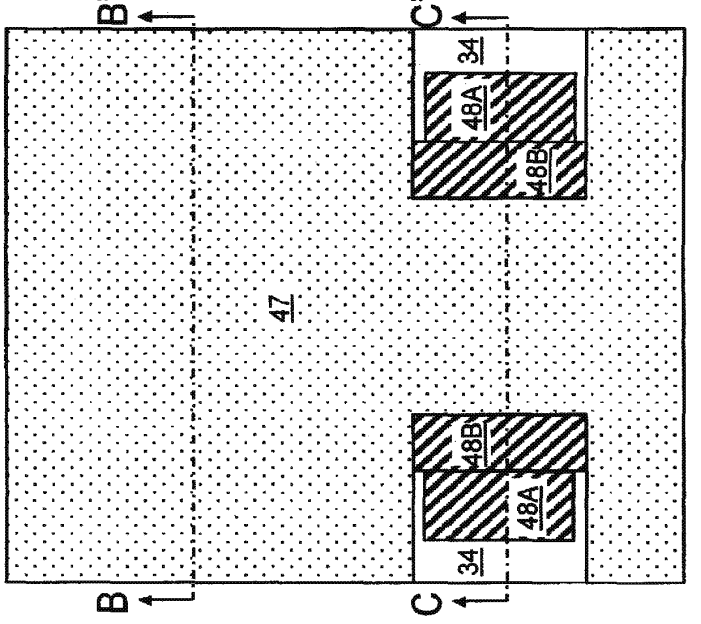


FIG. 5A

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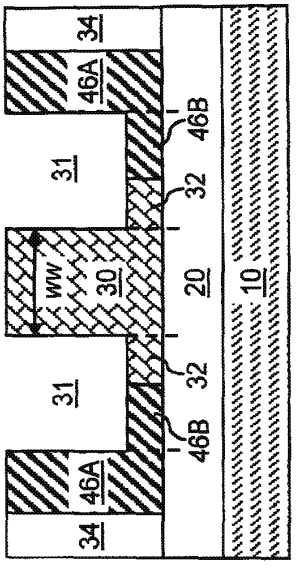


FIG. 6B

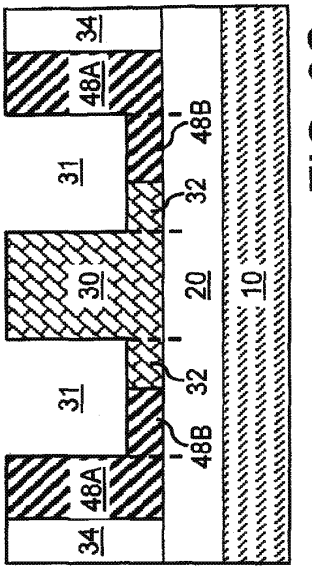


FIG. 6C

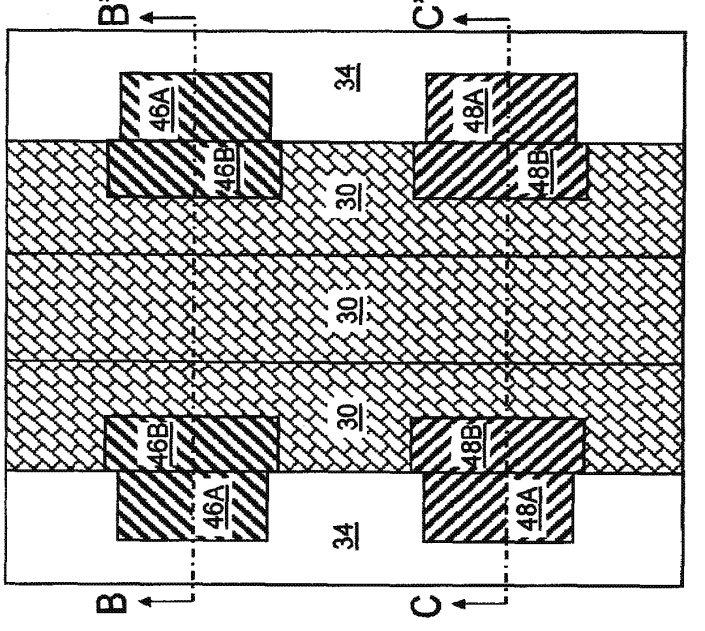


FIG. 6A

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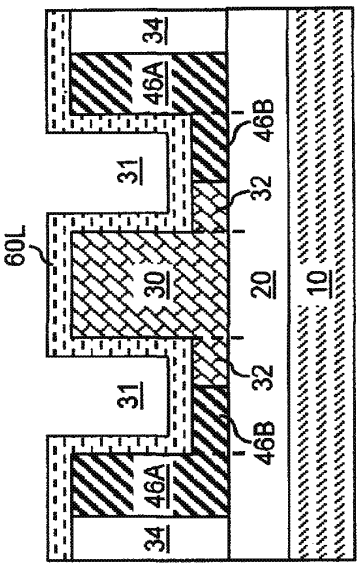


FIG. 7B

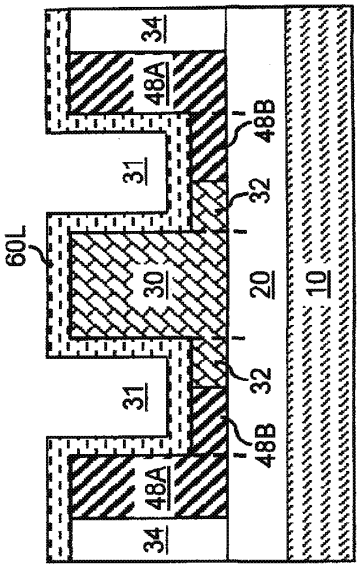


FIG. 7C

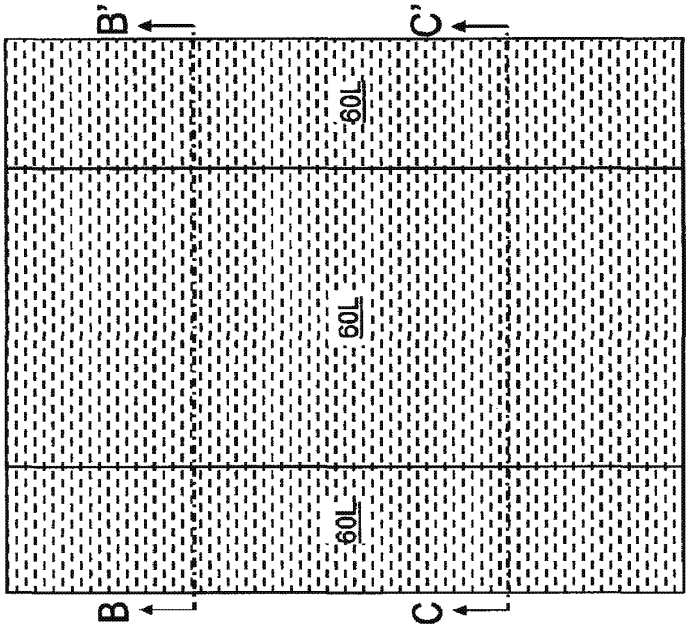


FIG. 7A

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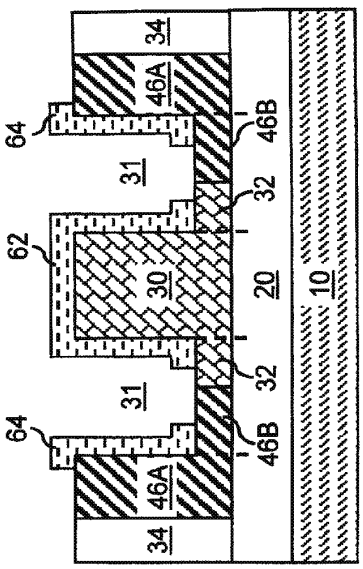


FIG. 8B

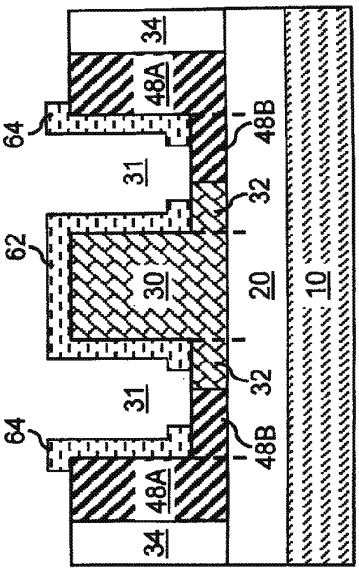


FIG. 8C

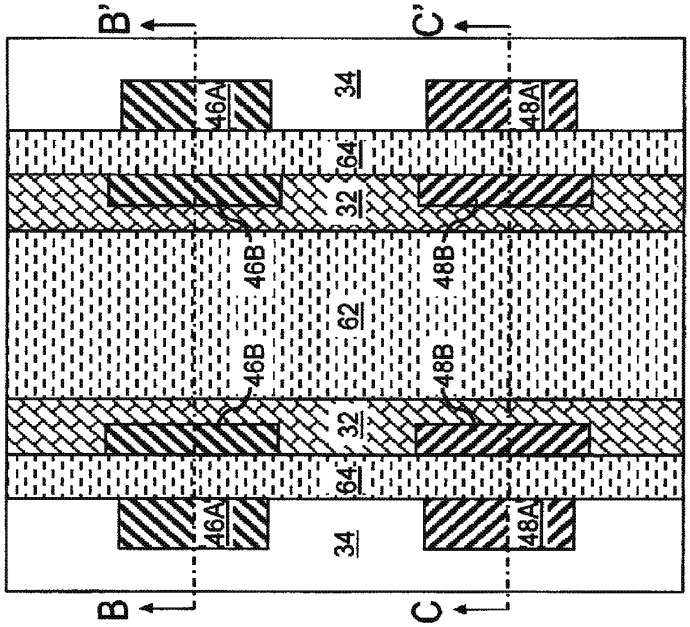


FIG. 8A

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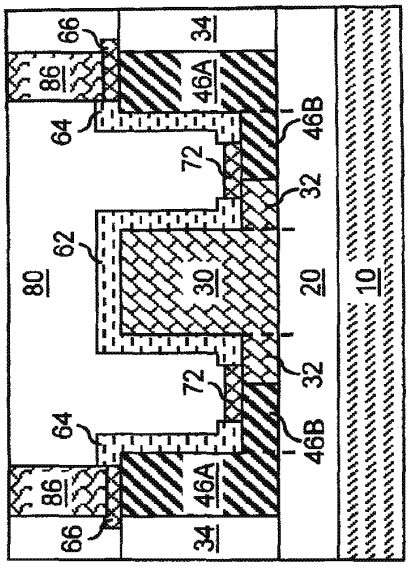


FIG. 9B

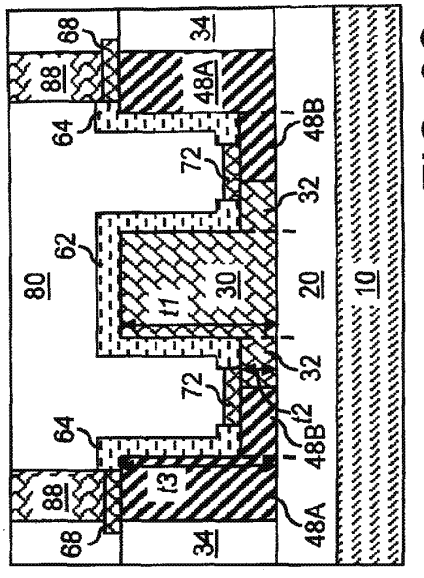


FIG. 9C

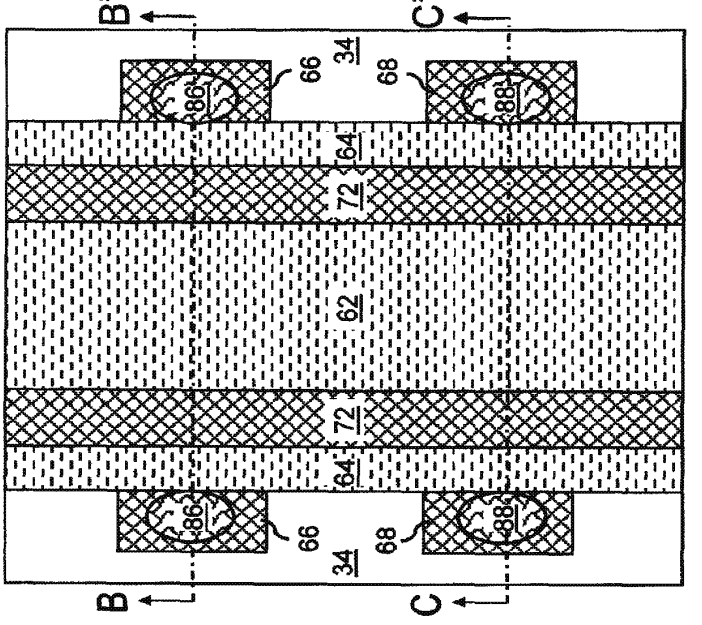


FIG. 9A

SAMSUNG EX. 1002 - 3831/4148

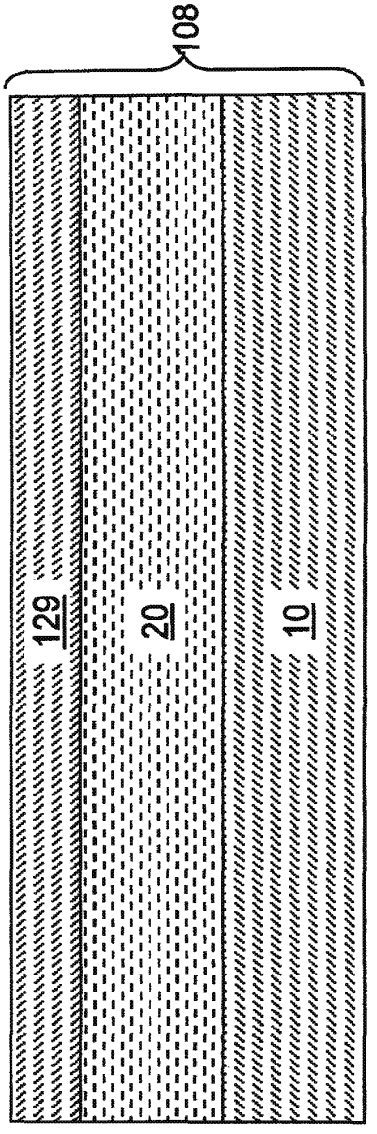


FIG. 10

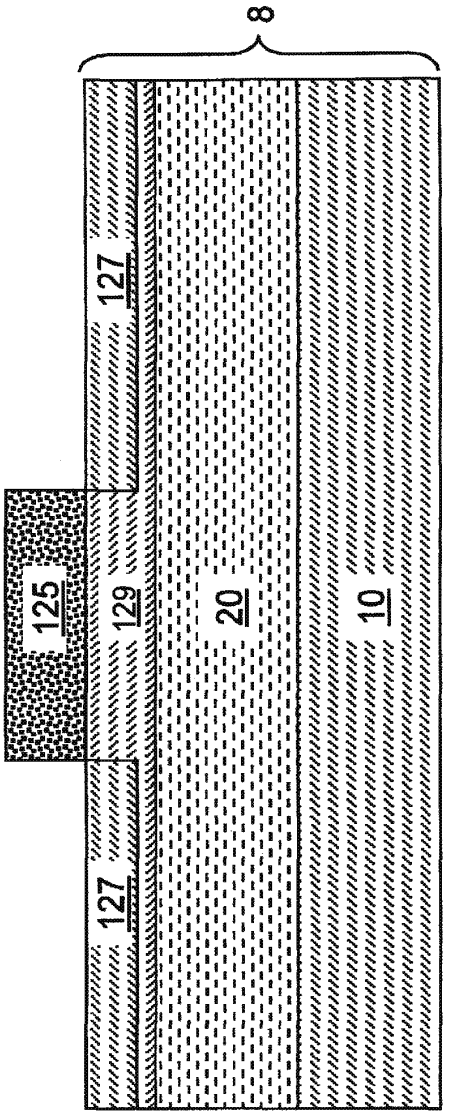


FIG. 11

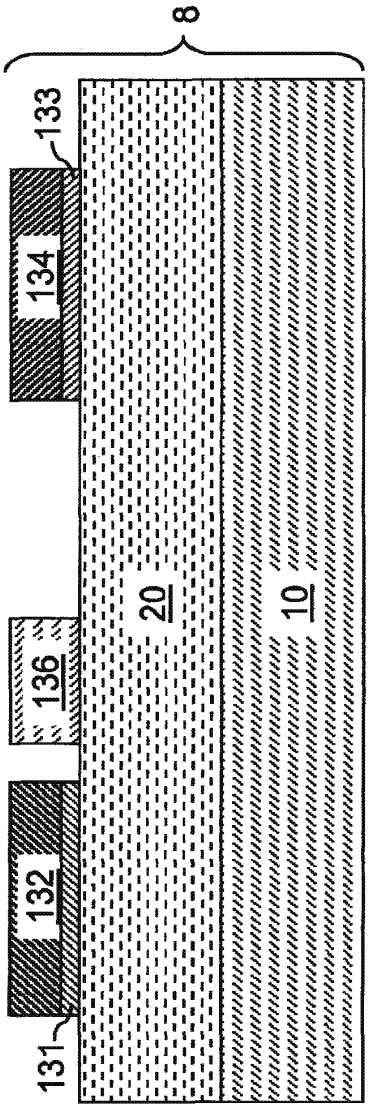


FIG. 12A

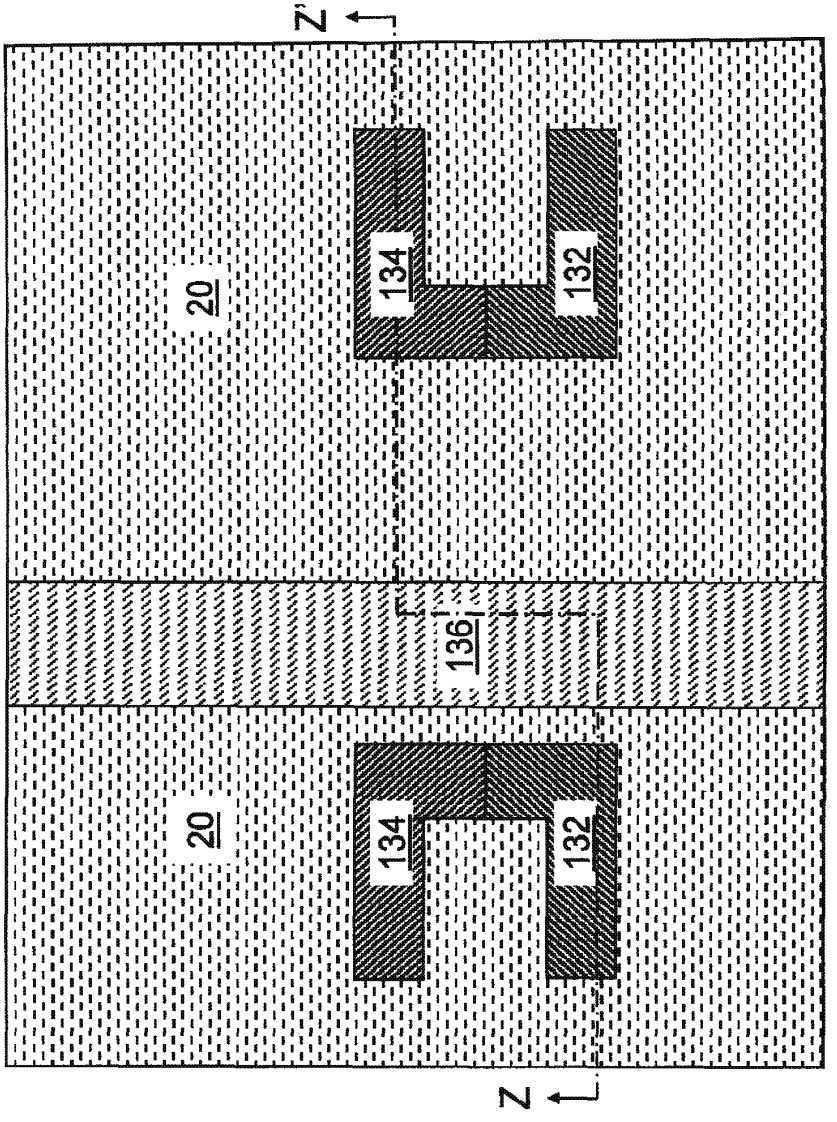


FIG. 12B

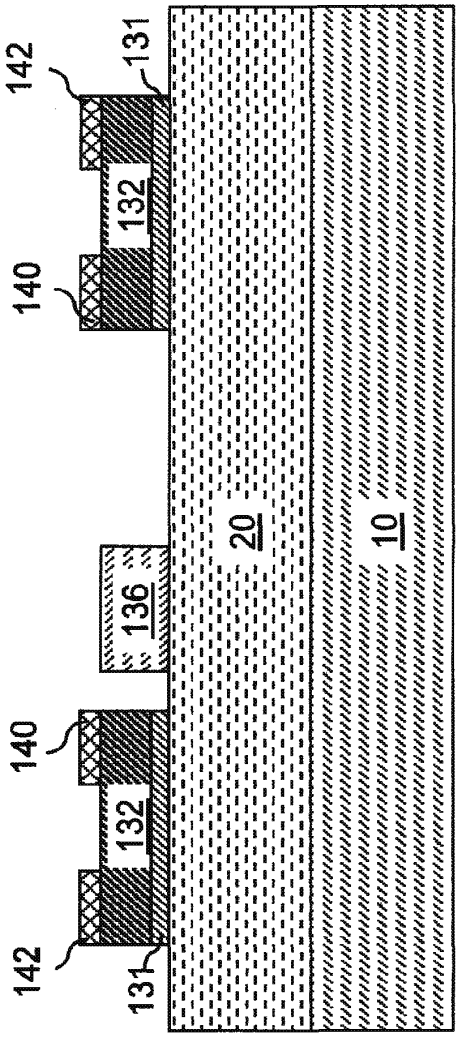


FIG. 13A

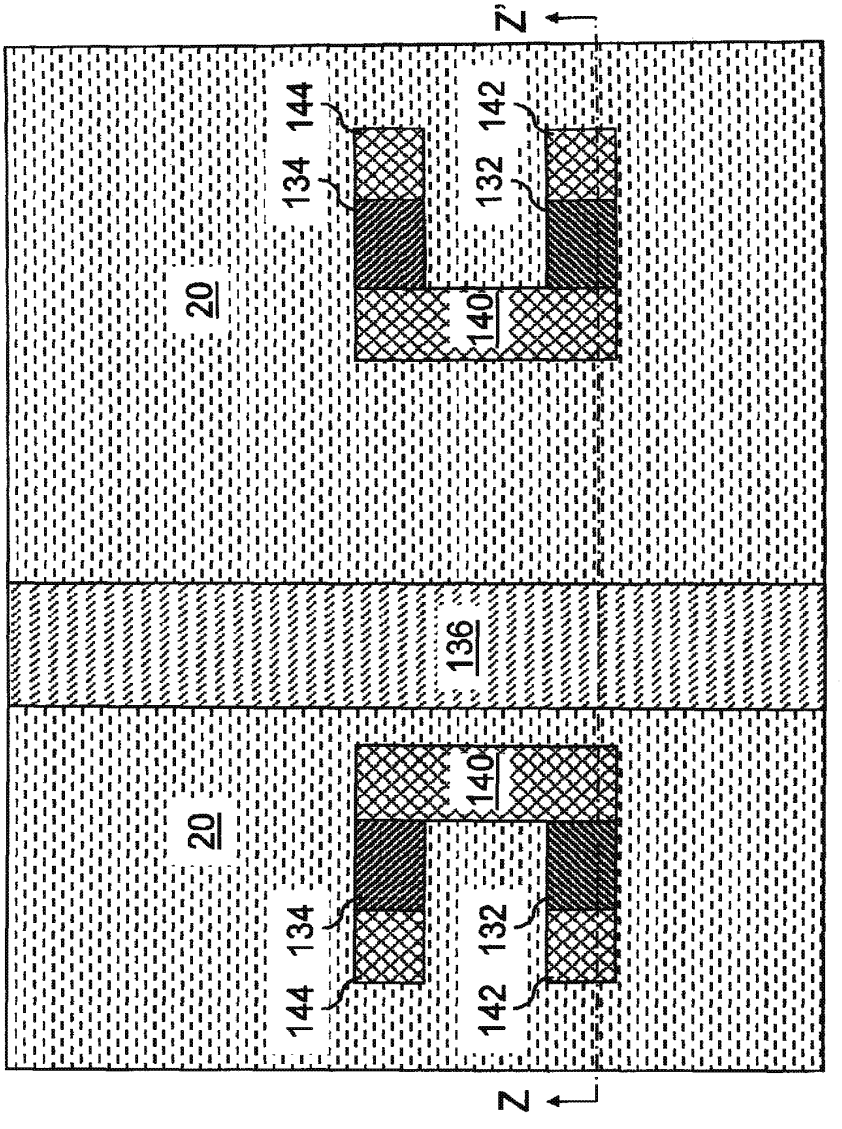


FIG. 13B

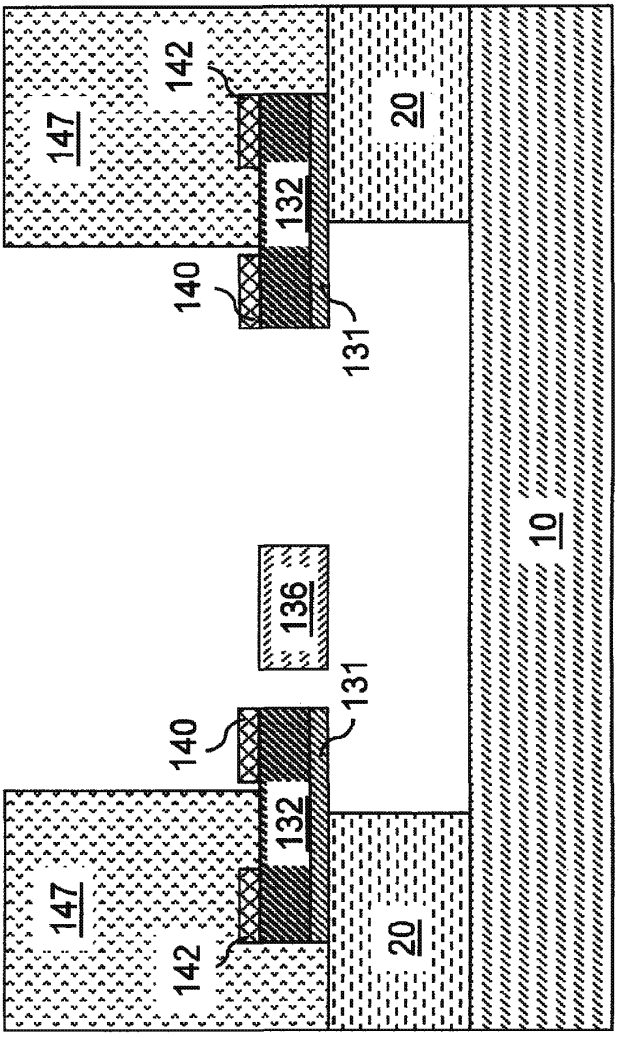


FIG. 14A

SAMSUNG EX. 1002 - 3838/4148

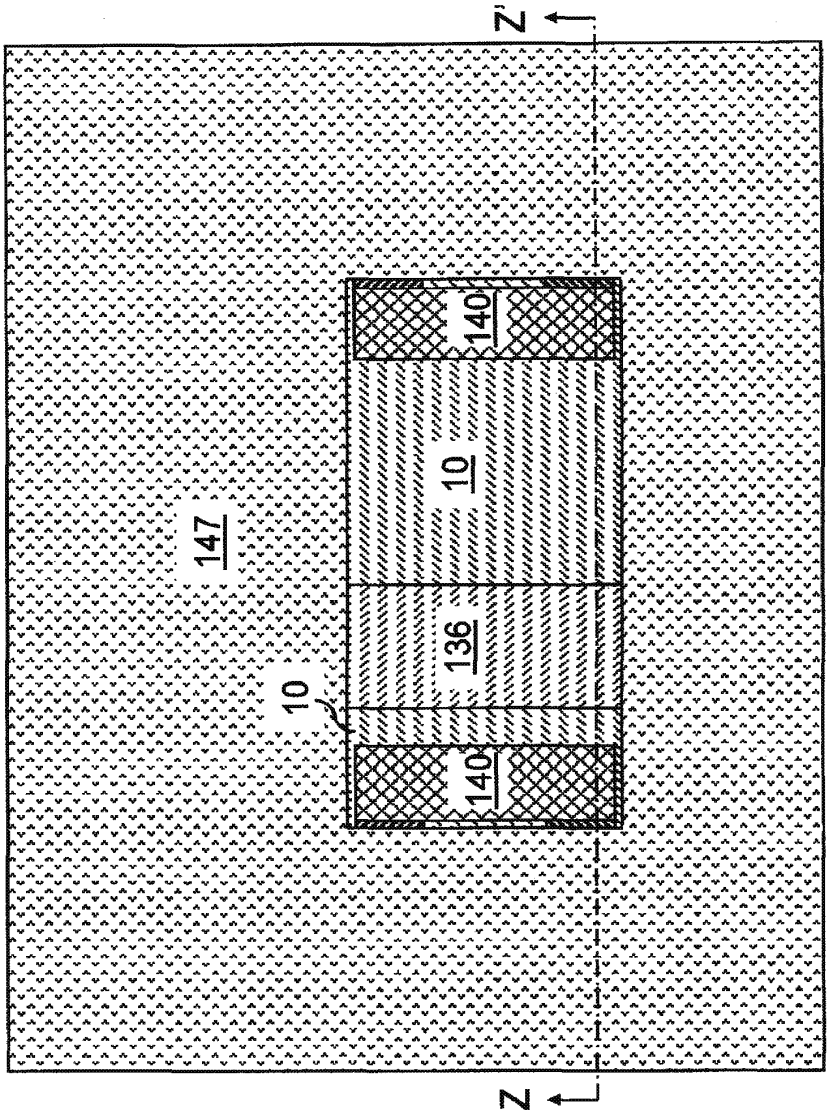


FIG. 14B

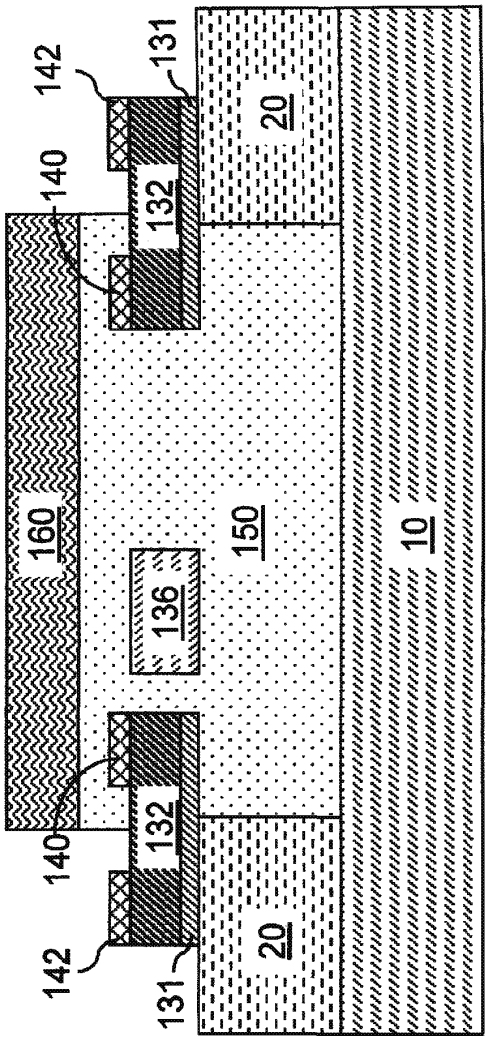


FIG. 15A

SAMSUNG EX. 1002 - 3840/4148

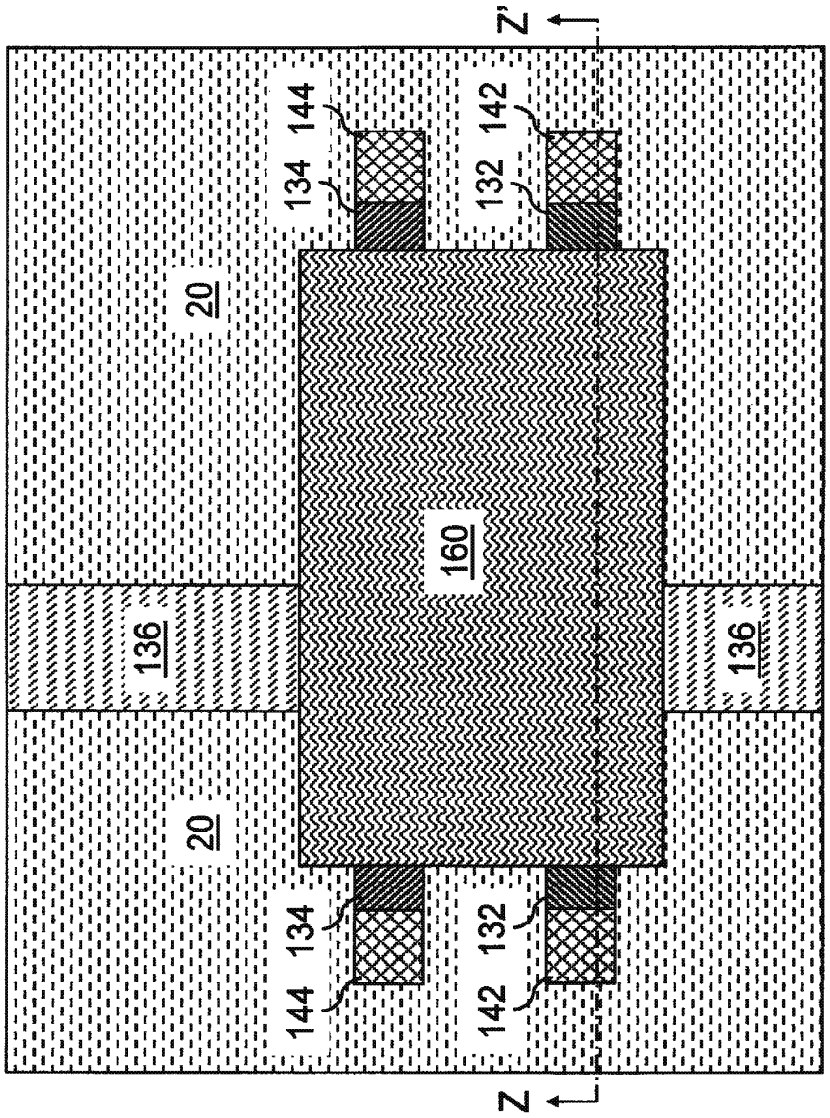


FIG. 15B

SAMSUNG EX. 1002 - 3841/4148

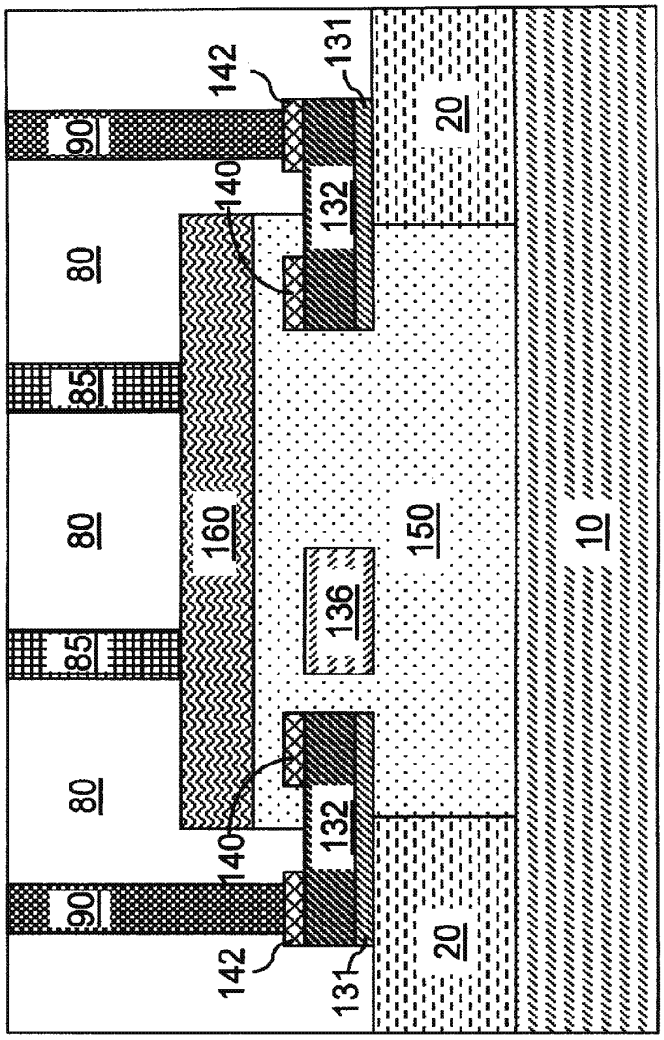


FIG. 16A

SAMSUNG EX. 1002 - 3842/4148

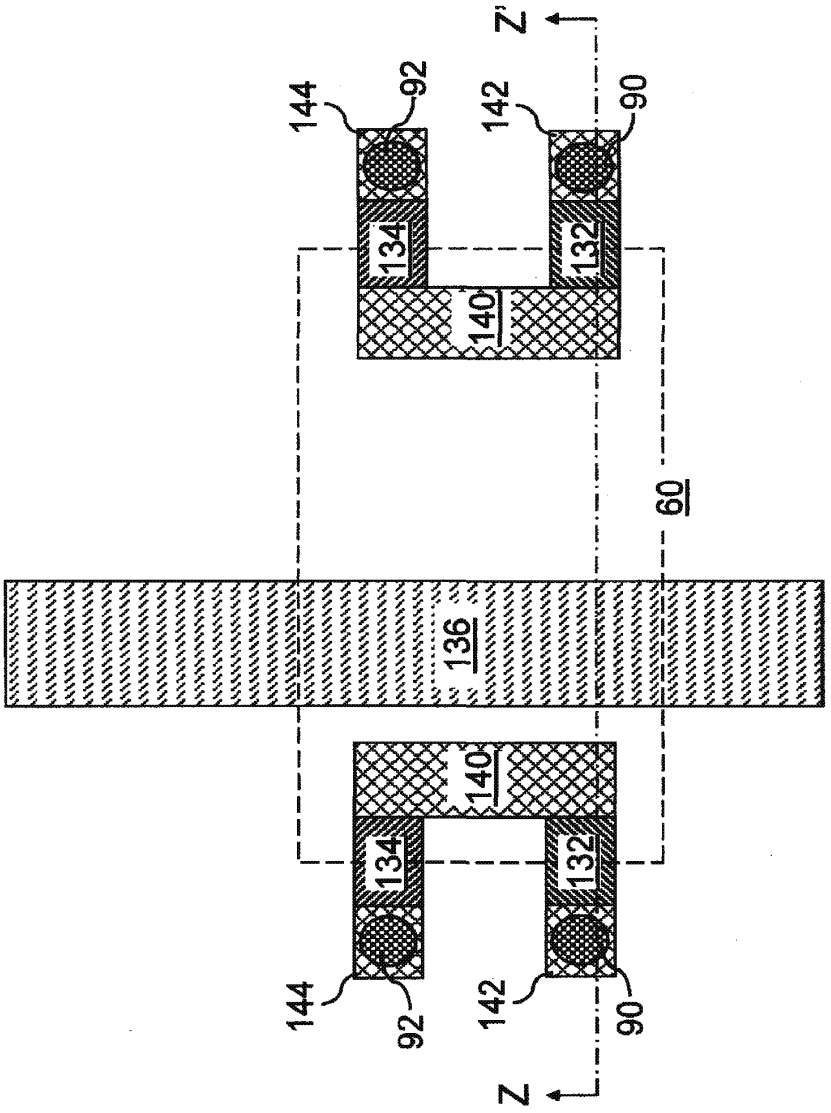


FIG. 16B

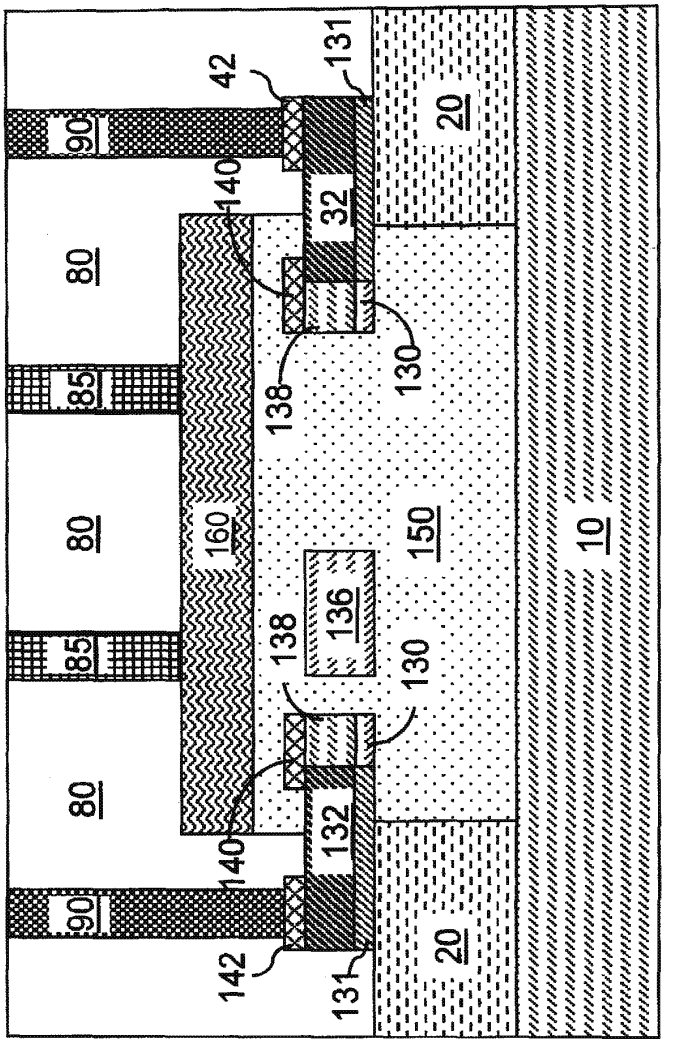


FIG. 17

SAMSUNG EX. 1002 - 3844/4148

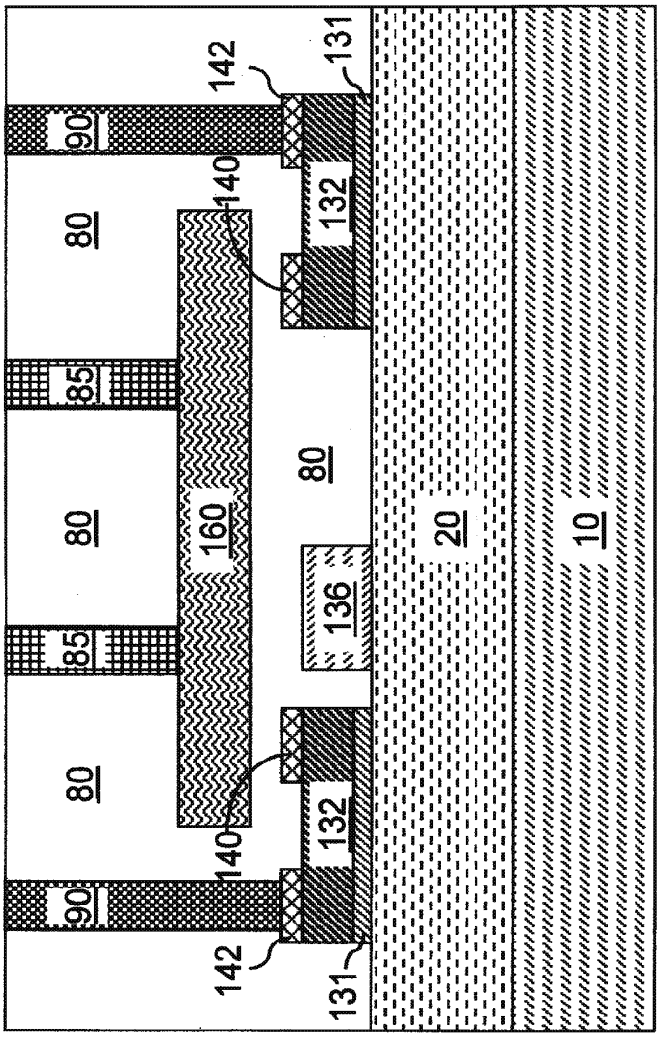


FIG. 18

SAMSUNG EX. 1002 - 3845/4148

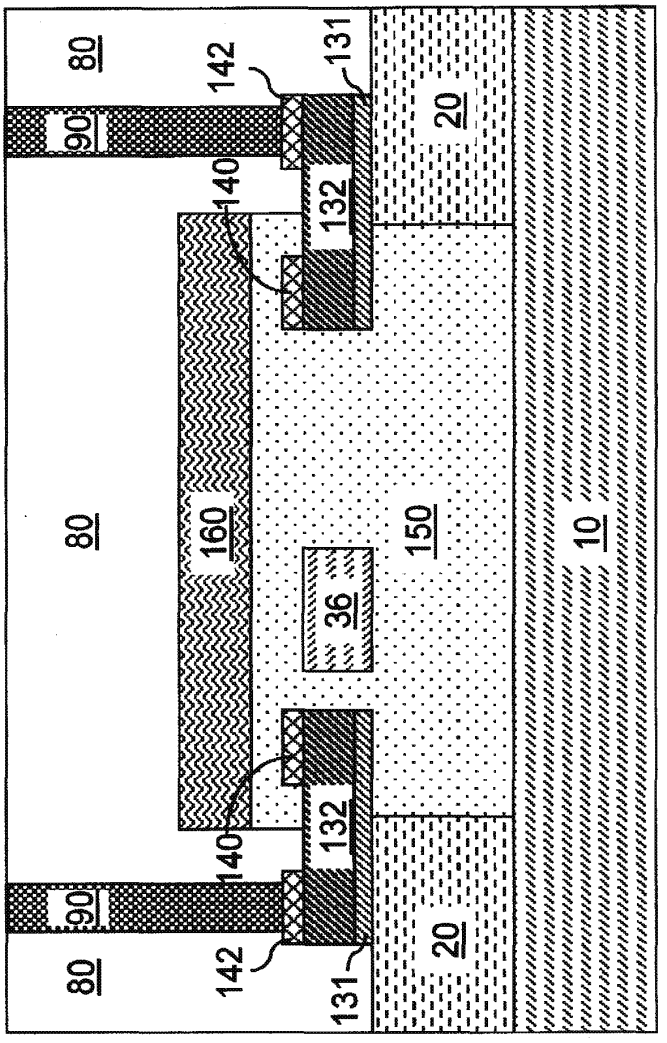


FIG. 19

SAMSUNG EX. 1002 - 3846/4148

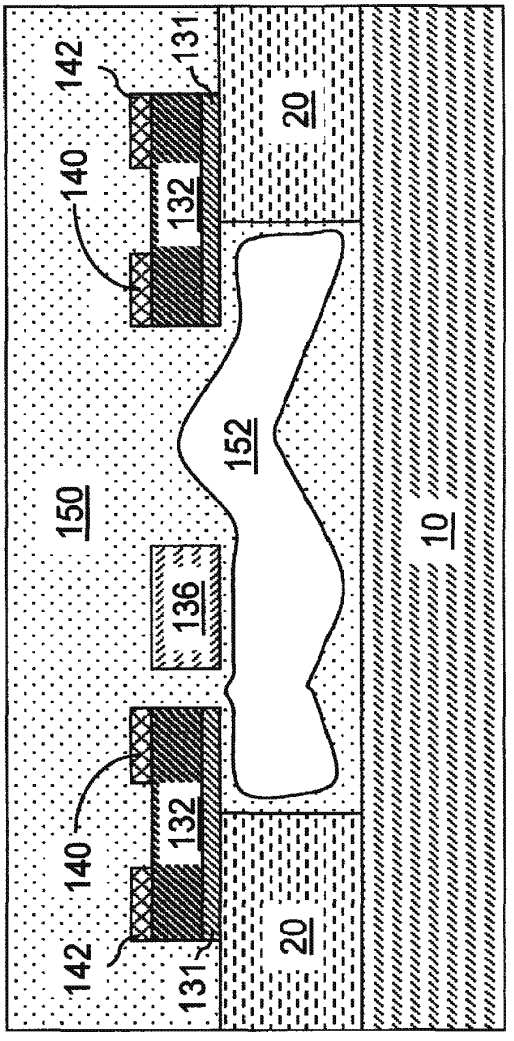


FIG. 20

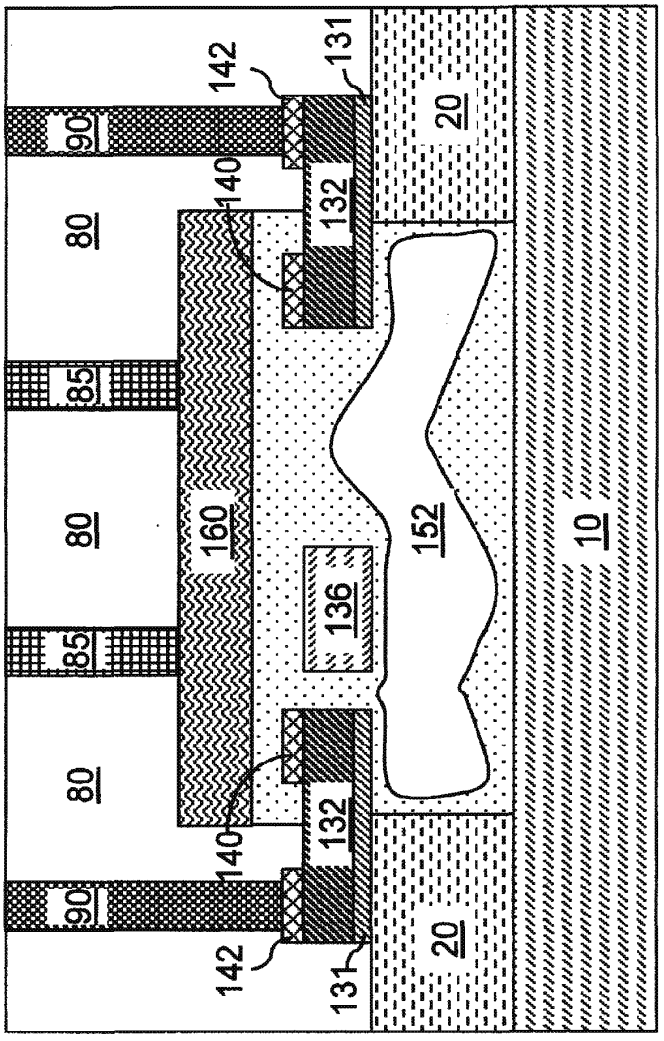


FIG. 21

SAMSUNG EX. 1002 - 3848/4148

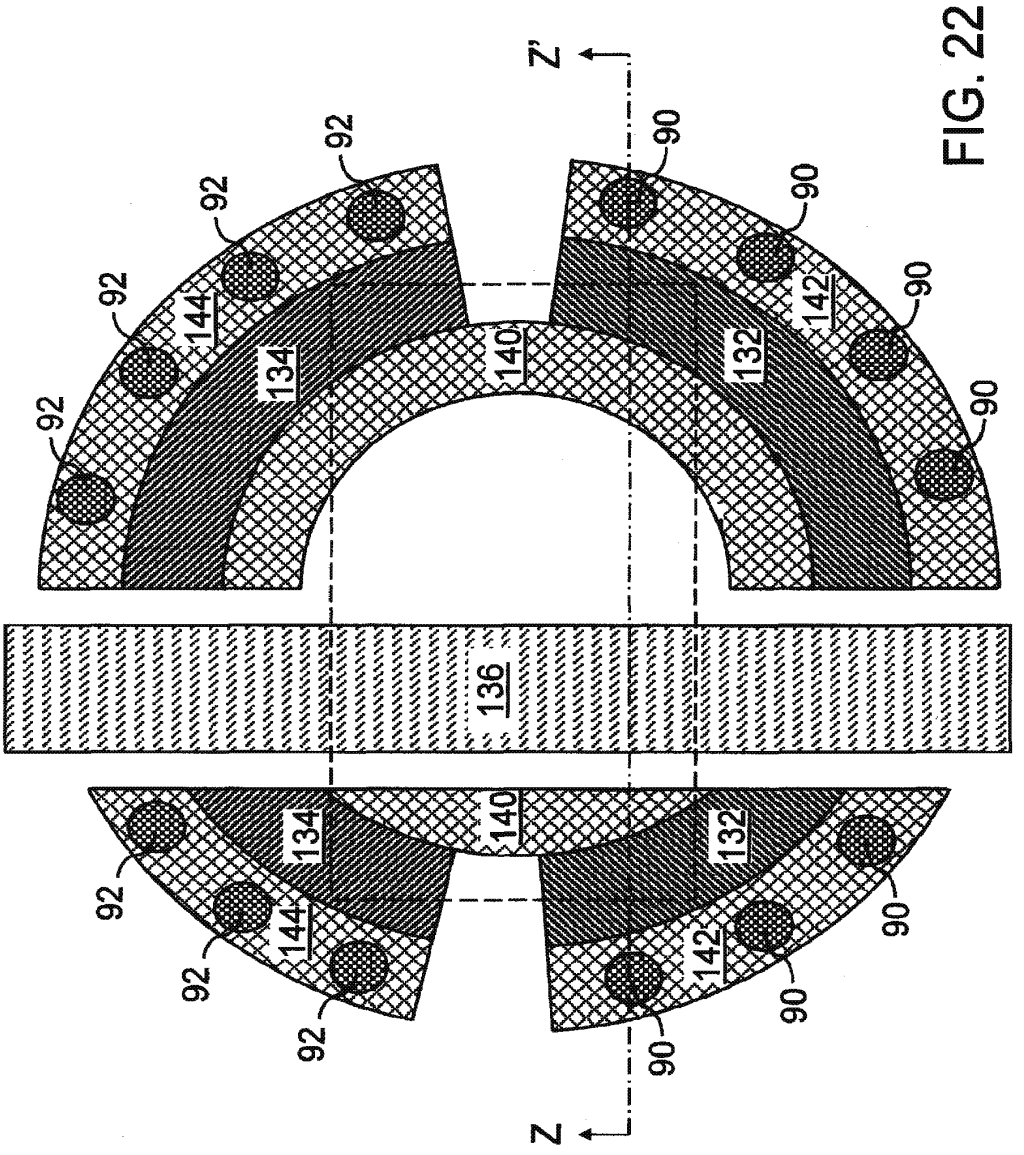


FIG. 22

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/059571

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L31/105 H01L31/18 H01L35/30 H01L23/38 G02B6/42
G02F1/01 G02F1/025
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H01L G02B G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 970 611 B1 (VAN DER VLIET FREDERIK MARCEL [US] ET AL) 29 November 2005 (2005-11-29) column 3, line 18 - column 11, line 64; figures 1A-8F	1-20
X	GB 2 332 284 A (BOOKHAM TECHNOLOGY LTD [GB]) 16 June 1999 (1999-06-16) page 9, line 11 - page 11, line 25; figures 1-4	1-20
A	US 7 340 709 B1 (MASINI GIANLORENZO [US] ET AL) 4 March 2008 (2008-03-04) column 4, line 4 - column 8, line 34; figures 1-8b	1-20

-/--

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 October 2010	21/10/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Albrecht, Claus

Form PCT/ISA/210 (second sheet) (April 2005)

SAMSUNG EX. 1002 - 3850/4148

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/059571

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005/207704 A1 (KEYSER THOMAS [US] ET AL) 22 September 2005 (2005-09-22) paragraph [0033] - paragraph [0050]; figures 1-8	1-20

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

SAMSUNG EX. 1002 - 3851/4148

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2010/059571

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6970611 B1	29-11-2005	NONE	
GB 2332284 A	16-06-1999	AU 745594 B2	21-03-2002
		AU 3718599 A	23-11-1999
		CA 2331069 A1	11-11-1999
		CN 1307691 A	08-08-2001
		EP 1073929 A1	07-02-2001
		WO 9957600 A1	11-11-1999
		JP 2002513952 T	14-05-2002
		US 6278822 B1	21-08-2001
US 7340709 B1	04-03-2008	NONE	
US 2005207704 A1	22-09-2005	NONE	

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SAMSUNG EX. 1002 - 3852/4148

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H01L 27/146 (2006.01) *H01L 27/148* (2006.01)

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17 September 2010 (17.09.2010)

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61/311,004 5 March 2010 (05.03.2010) US
61/311,107 5 March 2010 (05.03.2010) US

(71) Applicant *(for all designated States except US)*: **SIONYX, INC.** [—/US]; 100 Cummings Ctr., Suite 243-F, Beverly, MA 01915-6506 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **HADDAD, Homayoon** [—/US]; 16460 Sanderling CT., Beaverton, OR 97007 (US). **JIANG, Jutao** [CN/US]; 15121 Sw Kenton Dr., Tigard, OR 97224 (US). **MCKEE, Jeffrey** [US/US]; 22850 Sw Eno PL., Tualatin, OR 97224 (US). **MILLER, Drake** [US/US]; 13052 Sw Jacob CT., Tigard, OR 97224 (US). **FORBES, Leonard** [US/US]; 7340 Nw Mountain View Drive, Corvallis, OR 97330 (US). **PALSULE, Chintamani** [US/US]; 100 Cummings CTR., Suite 243-F, Beverly, MA 01915-6506 (US).

(74) Agents: **ALDER, Todd, B.** et al.; Thorpe North & Western, LLP, Po Box 1219, Sandy, UT 84091-1219 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) **Title**: PHOTOSENSITIVE IMAGING DEVICES AND ASSOCIATED METHODS

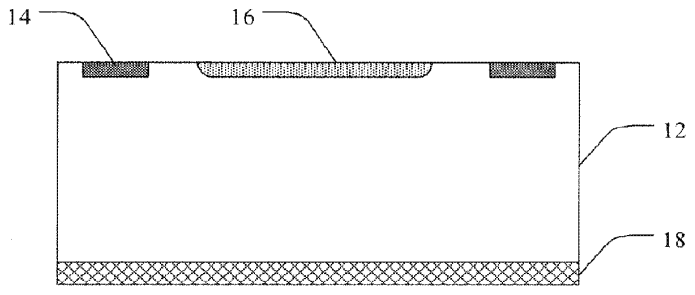


FIG. 1

(57) **Abstract**: Photosensitive devices and associated methods are provided. In one aspect, for example, a photosensitive imager device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. In one aspect, the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation. In another aspect, interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption wavelength as compared to a semiconductor substrate lacking a textured region.

WO 2011/035188 A2

SAMSUNG EX. 1002 - 3853/4148

PHOTOSENSITIVE IMAGING DEVICES AND ASSOCIATED METHODS

PRIORITY DATA

This application claims the benefit of U.S. Provisional Patent Application Serial No. 61/243,434, filed on September 17, 2009, U.S. Provisional Patent Application Serial No. 61/311,004 filed on March 5, 2010, and U.S. Provisional Patent Application Serial No. 61/311,107, filed on March 5, 2010, each of which is incorporated herein by reference.

BACKGROUND

The interaction of light with semiconductor materials has been a significant innovation. Silicon imaging devices are used in various technologies, such as digital cameras, optical mice, video cameras, cell phones, and the like. Charge-coupled devices (CCDs) were widely used in digital imaging, and were later improved upon by complementary metal-oxide-semiconductor (CMOS) imagers having increased performance. CMOS sensors are typically manufactured from silicon and can covert visible incident light into a photocurrent and ultimately into a digital image. Silicon-based technologies for detecting infrared incident electromagnetic radiation have been problematic, however, because silicon is an indirect bandgap semiconductor having a bandgap of about 1.1eV. Thus the absorption of electromagnetic radiation having wavelengths of greater than about 1100 nm is, therefore, very low in silicon.

SUMMARY

The present disclosure provides photosensitive devices and associated methods. In one aspect, for example, a photosensitive imager device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. In one aspect, the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation. In another aspect, interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region. In one specific aspect, the transfer

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SAMSUNG EX. 1002 - 3854/4148

element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

The textured region can be positioned in a variety of locations relative to the doped regions. In one aspect, for example, the textured region is positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In one specific aspect, the textured region has a surface morphology operable to direct electromagnetic radiation into or out of the semiconductor substrate. The surface morphology of the textured region relative to the semiconductor substrate can include a variety of configurations, including, without limitation, sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

In another aspect, the textured region can be positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions. In a more specific aspect, an additional textured region can be positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In this manner, textured regions can thus be positioned adjacent to multiple doped regions and opposite the multiple doped regions.

Various aspects of the textured region can vary depending on the desired configuration of the device. In one aspect, however, the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof. Numerous surface feature morphologies are contemplated, nonlimiting examples of which include cones, pillars, pyramids, micolenses, quantum dots, inverted features, and combinations thereof. Additionally, the textured region can be formed by a variety of processes. Nonlimiting examples of such texturing processes can include lazing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, and combinations thereof.

Additional layers and/or structures can be included in various devices according to aspects present disclosure. In one aspect, for example, a reflective layer can be coupled to the semiconductor substrate and positioned to maintain the electromagnetic radiation in the semiconductor substrate. In another aspect, a lens can be optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate.

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SAMSUNG EX. 1002 - 3855/4148

In another aspect of the present disclosure, a method of making a photosensitive imager device is provided. Such a method can include forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation and coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction.

In one aspect, the photosensitive imager device can be tuned to be selected to filter out specific electromagnetic radiation wavelengths. In one specific aspect, tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation. In another aspect, tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type and/or thickness of the textured region, dopant type of the textured region, doping profile of the texture region, dopant profile of the semiconductor substrate, material type and/or thickness of the semiconductor substrate, and combinations thereof.

In another aspect of the present disclosure, a photosensitive imager device is provided. Such a device can include a semiconductor substrate having multiple doped regions forming a least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and at least 4 transistors coupled to the semiconductor substrate and with at least one of the transistors electrically coupled to the at least one junction.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view of a photosensitive device in accordance with one aspect of the present disclosure;

FIG. 2 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 3 is a schematic view of a photosensitive device in accordance with yet another aspect of the present disclosure;

FIG. 4 is a schematic view of a photosensitive device in accordance with a further aspect of the present disclosure;

FIG. 5 is a schematic view of a photosensitive device in accordance with yet a further aspect of the present disclosure;

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SAMSUNG EX. 1002 - 3856/4148

FIG. 6 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 7 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

FIG. 8 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 9 is a schematic view of a photosensitive pixel device in accordance with yet a further aspect of the present disclosure;

FIG. 10 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure;

FIG. 11 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

FIG. 12 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 13 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure;

FIG. 14 is a schematic view of a photosensitive imager device in accordance with yet another aspect of the present disclosure;

FIG. 15 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 16 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure; and

FIG. 17 is a depiction of a method of making a photosensitive imager device in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

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SAMSUNG EX. 1002 - 3857/4148

Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the term "low oxygen content" refers to any material having an interstitial oxygen content that is less than or equal to about 60 ppm atomic.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations formed by the irradiation of laser pulses. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers) and nanopores. In another aspect, such a surface can include micron-sized structures (e.g. about 2 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the terms "surface modifying" and "surface modification" refer to the altering of a surface of a semiconductor material using laser radiation. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping of a semiconductor material.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified using laser radiation. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

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SAMSUNG EX. 1002 - 3858/4148

As used herein, the term "detection" refers to the sensing, absorption, and/or collection of electromagnetic radiation.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include

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SAMSUNG EX. 1002 - 3859/4148

not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

Electromagnetic radiation can be present across a broad wavelength range, including visible range wavelengths (approximately 350nm to 800nm) and non-visible wavelengths (longer than about 800nm or shorter than 350 nm). The infrared spectrum is often described as including a near infrared portion of the spectrum including wavelengths of approximately 800 to 1300 nm, a short wave infrared portion of the spectrum including wavelengths of approximately 1300 nm to 3 micrometers, and a mid to long wave infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as "infrared" portions of the electromagnetic spectrum unless otherwise noted.

Traditional silicon photodetecting imagers have limited light absorption/detection properties. For example, infrared light is mostly transparent to such silicon based detectors. While other materials (e.g. InGaAs) can be used to detect infrared electromagnetic radiation having wavelengths greater than about 1000 nm, silicon is still commonly used because it is relatively cheap to manufacture and can be used to detect wavelengths in the visible spectrum (i.e. visible light, 350 nm – 800 nm). Traditional silicon materials require substantial absorption depths to detect photons having wavelengths longer than approximately 700 nm. While visible light can be absorbed at relatively shallow depths in silicon, absorption of longer wavelengths (e.g. 900 nm) in silicon of a standard wafer depth (e.g. approximately 750 μm) is poor if at all. The devices of the present disclosure increase the absorption of semiconductor materials by decreasing the effective absorption length to longer wavelengths as compared to traditional materials. For example, the absorption depth of silicon can be reduced such that these longer wavelengths can be absorbed at depths of less than or equal to about 850 μm. In other words, by decreasing the

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SAMSUNG EX. 1002 - 3860/4148

effective absorption length these devices are able to absorb longer wavelengths (e.g. >1000 nm for silicon) within a thin semiconductor material. In addition to increasing the effective absorption length, the response rate or response speed can also be increased using thinner semiconductor materials.

The present disclosure additionally provides broadband photosensitive diodes, pixels, and imagers capable of detecting visible as well as infrared electromagnetic radiation, including associated methods of making such devices. A photosensitive diode can include a semiconductor substrate having multiple doped regions forming at least one junction, and at least one textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. In one aspect the multiple doped regions can include at least one cathode region and at least one anode region. In some aspects, doped regions can include an n-type dopant and/or a p-type dopant as is discussed below, thereby creating a p-n junction. In other aspects, a photosensitive device can include an i-type region to form a p-i-n junction.

A photosensitive pixel can include a semiconductor substrate having multiple doped regions forming at least one junction, at least one textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. A photosensitive imager can include multiple photosensitive pixels. Additionally, an electrical transfer element can include a variety of devices, including without limitation, transistors, sensing nodes, transfer gates, transfer electrodes, and the like.

Photosensitive or photodetecting imagers include photodiodes or pixels that are capable of absorbing electromagnetic radiation within a given wavelength range. Such imagers can be passive pixel sensors (PPS), active pixel sensors (APS), digital pixel sensor imagers (DPS), or the like, with one difference being the image sensor read out architecture. For example, a semiconducting photosensitive imager can be a three or four transistor active pixel sensor (3T APS or 4T APS). Various additional components are also contemplated, and would necessarily vary depending on the particular configuration and intended results. As and example, a 4T configuration can additionally include, among other things, a transfer gate, a reset, a source follower, and row select transistors. Additionally, devices having greater than 4 transistors are also within the present scope.

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SAMSUNG EX. 1002 - 3861/4148

Photosensitive imagers can be front side illumination (FSI) or back side illumination (BSI) devices, and there are advantages and disadvantages to both architecture types. In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, can scatter off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. In one aspect the lens can be a ulens. BSI imagers, one the other hand, are configured to have the depletion region of the junction extending to the opposite side of the device. In one aspect, for example, incident light enters the device via the light sensing portion and is mostly absorbed prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. As mentioned, the present disclosure can be adapted for either configuration. It should also be understood that devices according to aspects of the present disclosure can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures.

In one aspect, as is shown in FIG. 1, a photosensitive diode 10 can include a semiconductor substrate 12 having multiple doped regions 14, 16 forming at least one junction, and at least one textured region 18 coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. The different doped regions can have the same doping profile or different doping profiles, depending on the device. Such an architecture is a FSI design where light enters the semiconductor substrate from the direction of the multiple doped regions. While the device shown in FIG. 1 contains three doped regions, it should be noted that aspects containing one or more doped regions are considered to be within the present scope. Additionally, the semiconductor substrate can be doped, and thus can be considered to be a doped region in some aspects. It should also be noted that the photosensitive diode can be configured with a BSI architecture, and thus electromagnetic radiation would enter the semiconductor substrate from the direction of the textured region.

The various devices according to aspects of the present disclosure can exhibit increased quantum efficiency over traditional photosensitive devices. Any increase in the quantum efficiency makes a large difference in the signal to noise ratio. More complex structures can provide not only increased quantum efficiency but also good

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SAMSUNG EX. 1002 - 3862/4148

uniformity from pixel to pixel. In addition, devices of the present disclosure exhibit increased responsivity as compared to traditional photosensitive devices. For example, in one aspect the responsivity can be greater than or equal to 0.8A/W for wavelengths greater than 1000 nm for semiconductor substrate that is less than 100 μm thick.

Photosensitive imagers can be maintained under constant conditions (fixed voltage or current) to provide enhanced linearity and uniformity. Connections between the imager and the underlying device layers can be achieved using vias fabricated from a refractory metal, such as tungsten or tantalum. Placing storage elements under the imager may provide various photonic benefits. For example, the entire pixel array may be dedicated to signal processing. This may enable higher performance by permitting access to low level pixel signals. Furthermore, massively parallel operations can be performed by pixel processors. For example, analog to digital conversion, noise reduction (ie., true correlated double sampling), power conditioning, nearest neighbor pixel processing, compression, fusion, and color multiplexing operations can be performed.

A variety of semiconductor materials are contemplated for use with the devices and methods according to aspects of the present disclosure. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc

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SAMSUNG EX. 1002 - 3863/4148

telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows electromagnetic radiation detection and conversion functionality, and thus any such thickness of semiconductor material is considered to be within the present scope. In some aspects the laser processed region of the semiconductor increases the efficiency of the device such that the semiconductor material can be thinner than has previously been possible. Decreasing the thickness of the semiconductor reduces the amount of semiconductor material required to make such a device. In one aspect, for example, the semiconductor material has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm. In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

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SAMSUNG EX. 1002 - 3864/4148

Additionally, various types of semiconductor material are contemplated, and any such material that can be incorporated into an electromagnetic radiation detection device is considered to be within the present scope. In one aspect, for example, the semiconductor material is monocrystalline. In another aspect, the semiconductor material is multicrystalline. In yet another aspect, the semiconductor material is microcrystalline. It is also contemplated that the semiconductor material can be amorphous. Specific nonlimiting examples include amorphous silicon or amorphous selenium.

The semiconductor materials of the present disclosure can also be made using a variety of manufacturing processes. In some cases the manufacturing procedures can affect the efficiency of the device, and may be taken into account in achieving a desired result. Exemplary manufacturing processes can include Czochralski (Cz) processes, magnetic Czochralski (mCz) processes, Float Zone (FZ) processes, epitaxial growth or deposition processes, and the like. Whether or not low oxygen content is desired in the device can also affect the choice of a manufacturing process for the semiconductor material. Various processes produce semiconductor materials containing varying amounts of oxygen, and as such, some applications having more stringent tolerances with respect to oxygen levels may benefit more from specific manufacturing procedures as compared to others. For example, during CZ crystal growth oxygen from the containment vessel, usually a quartz crucible, can become incorporated into the crystal as it is pulled. Additionally, other sources of oxygen contamination are also possible with the CZ process. Such contamination may be reduced, however, through the use of non oxygen-containing crucible materials, as well as the development of other crystal growth methods that do not utilize a crucible. One such process is the FZ process.

Materials grown with the CZ method can also be made to have lowered oxygen concentration through enhancements to the crystal growth process, such as growing the crystal in the presence of a magnetic field (i.e. the mCz process). Also, gettering techniques can be employed to reduce the impact of oxygen or other impurities on the finished device. These gettering techniques can include thermal cycles to liberate or nucleate impurities, or selective ion implantation of species to serve as gettering sites for the impurities. For example, oxygen concentrated in the semiconductor can be removed by the performing a furnace cycle to form a denuded zone. During heating with an inert gas, oxygen near the surface of the semiconductor

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SAMSUNG EX. 1002 - 3865/4148

diffuses out of the material. During the furnace cycle but after the denuding step, nucleating and growing steps may be performed. Nucleating sites for precipitates are formed during the nucleating step, and the precipitates are grown from the nucleating sites during a growing step. The precipitates are formed from interstitial oxygen within the bulk of the semiconductor material and beneath the denuded zone. The precipitation of oxygen in the bulk of the semiconductor material can be desired because such precipitates can act as gettering sites. Such precipitate formation can also be performed to "lock up" interstitial oxygen into the precipitates and reduce the likelihood that such oxygen can migrates from the bulk of the semiconductor material into the denuded zone.

In those aspects where low oxygen content of the device is desired, further processing of the semiconductor material can be performed so as to minimize the introduction of oxygen. Oxygen can exist in different states or at different sites (for example, interstitially or substitutionally) within a semiconductor such as silicon, dependent upon the thermal processing the semiconductor has received. If the semiconductor is subjected to temperatures higher than, for example, about 1000° C, oxygen can form aggregates or clusters that serve as defect sites in the crystal lattice. These sites may result in trap states and a reduction in carrier lifetime within the semiconductor material and device can occur. At lower temperatures (for example, around 400° C to 700° C), oxygen can behave as electrically active thermal donors. Thus, oxygen can have a negative impact on carrier lifetime and on carrier mobility. In a device fabricated to have photoconductive gain, the presence of oxygen causing reduced carrier lifetime may result in reduced levels of photoconductive gain.

It may be beneficial, therefore, to produce semiconductor devices such that a low oxygen content is obtained or maintained. This can be accomplished in a variety of ways, including using semiconductor materials having low levels of oxygen contained therein to begin with, processing these materials in a manner that minimizes the uptake of oxygen into the semiconductor lattice, and utilizing techniques that eliminate or reduce oxygen that may be present in the semiconductor. Such processes and techniques can include, for example, annealing the semiconductor material and any laser treated region to lower temperatures as compared to previous annealing procedures. Annealing processes are discussed more fully below.

Additionally, texture processing of the semiconductor material and/or any annealing process can be performed in a substantially oxygen-depleted environment

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SAMSUNG EX. 1002 - 3866/4148

in order to minimize the introduction of oxygen into the semiconductor. An oxygen-depleted or substantially oxygen-depleted environment can include a variety of environments. In one aspect, for example, the oxygen-depleted environment can be an environment whereby oxygen from the air or other sources has been replaced with a gas or other fluid containing little to no oxygen. In another aspect, processing can occur in a vacuum environment, and thus contain little to no oxygen. Additionally, oxygen-containing materials or materials that introduce oxygen into the semiconductor, such as, for example, quartz crucibles, can be avoided. As a practical matter, the term "oxygen-depleted environment" can be used to describe an environment with low levels of oxygen, provided a semiconductor material can be processed therein within the desired tolerances. Thus, environments having low oxygen, or little to no oxygen, are environments in which a semiconductor can be processed as a low-oxygen content semiconductor while maintaining oxygen levels within the tolerances of the present disclosure. In one aspect, an oxygen-depleted environment can be an oxygen-free environment. Further details regarding low-oxygen content semiconductor materials can be found in US Patent Application No. 12/771848, filed on April 30, 2010, which is incorporated herein by reference.

The semiconductor material can have varying levels of interstitial oxygen depending on the desired efficiency of the device. In some aspects, oxygen content may be of no concern, and thus any level of oxygen within the lattice is acceptable. In other aspects, a low oxygen content is desired. In one aspect a semiconductor material can have an oxygen content that is less than or equal to about 50 ppm atomic. In another aspect, a semiconductor material can have an oxygen content that is less than or equal to about 30 ppm atomic. In yet another aspect, the semiconductor material can have an oxygen content less than or equal to about 10 ppm atomic. In another aspect the semiconductor can have an oxygen content less than about 5 ppm atomic. In yet another aspect the semiconductor can have an oxygen content less than about 1 ppm atomic.

As has been described, the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to increase the effective absorption length of the photosensitive pixel. The surface features can be cones, pyramids, pillars, protrusions, microlenses, quantum dots, inverted features and the like. Factors such

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SAMSUNG EX. 1002 - 3867/4148

as manipulating the feature sizes, dimensions, material type, dopant profiles, texture location, etc. can allow the diffusing region to be tunable for a specific wavelength. In one aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be absorbed. In another aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be reduced or eliminated via filtering.

Tuning can also be accomplished through the location of the texture region within the device, modifying the dopant profile(s) of regions within the device, dopant selection, and the like. Additionally, material composition near the textured region can create a wavelength specific photosensing pixel device. It should be noted that a wavelength specific photosensing pixel can differ from one pixel to the next, and can be incorporated into an imaging array. For example a 4 x 4 array can include a blue pixel, a green pixel, a red pixel, and infrared light absorbing pixel, or a blue pixel, two green pixels, and a red pixel.

Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor substrate. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The textured region can be formed by various techniques, including lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, additional material deposition, and the like. For example, pillar features can be incorporated into pixels by thinning or removing material from the backside of a FSI semiconductor substrate by using deep trench isolation and etching techniques. In one aspect material can be removed to a thickness of about 20 μm. Anisotropic etching can be used to produce a sloping backside pyramid structure, spherical, structure parabolic structure , a lens structure with reflectors, and the like. Such features on the backside of pillars will also serve to diffuse and reflect electromagnetic radiation.

In one aspect, the texturing process can be performed during the manufacture of the photosensitive device. In another aspect, the texturing process can be performed on a photosensitive device that has previously been made. For example, a CMOS, CCD, or other photosensitive element can be textured following manufacture. In this case, material layers may be removed from the photosensitive element to

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SAMSUNG EX. 1002 - 3868/4148

expose the semiconductor substrate or bulk material upon which a textured region may be formed.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete locations of the semiconductor substrate to be textured. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection. The laser treated region can be associated with the surface nearest the impinging electromagnetic radiation, or the laser treated surface can be associated with a surface opposite in relation to impinging electromagnetic radiation, thereby allowing the radiation to pass through the semiconductor material before it hits the laser treated region.

In one aspect, for example, a target region of the semiconductor material can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can be directed through a dopant carrier and onto the semiconductor surface. In this way, dopant from the dopant carrier is introduced into the target region of the semiconductor material. Such a region incorporated into a semiconductor material can have various benefits in accordance with aspects of the present disclosure. For example, the target region typically has a textured surface that increases the surface area of the laser treated region and increases the probability of radiation absorption via the mechanisms described herein. In one aspect, such a target region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of semiconductor material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the semiconductor. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the semiconductor material is chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the

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SAMSUNG EX. 1002 - 3869/4148

formation of surface features appearing as microstructures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the semiconductor material. In some aspects, the features or microstructures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed by the semiconductor material.

The type of laser radiation used to surface modify a semiconductor material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to the wavelength of the laser radiation, pulse width, pulse fluence, pulse frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsatile lasing of a semiconductor material. A short-pulsed laser is one capable of producing femtosecond, picosecond and/or nanosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm, and more specifically from about 200 nm to about 1200 nm. The pulse width of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse widths can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse widths can be in the range of from about 50 picoseconds to 100 nanoseconds. In another aspect, laser pulse widths are in the range of from about 50 to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a semiconductor target region can be from about 2 to about 1000. Further, the repetition rate or frequency of the pulses can be selected to be in a range of from about 10 Hz to about 10 μHz, or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2, or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2.

A variety of dopant materials are contemplated, and any such material that can be used in the laser treatment process to surface modify a semiconductor material according to aspects of the present disclosure is considered to be within the present

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SAMSUNG EX. 1002 - 3870/4148

scope. It should be noted that the particular dopant utilized can vary depending on the semiconductor material being laser treated, as well as the intended use of the resulting semiconductor material. For example, the selection of potential dopants may differ depending on whether or not tuning of the photosensitive device is desired.

A dopant can be either electron donating or hole donating. In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of between about 5×10^{14} and about 1×10^{16} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. SF_6 gas is a good carrier for the incorporation of sulfur into the semiconductor material via a laser process without significant adverse effects on the semiconductor material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

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SAMSUNG EX. 1002 - 3871/4148

The semiconductor substrate can be annealed for a variety of reasons, including dopant activation, semiconductor material damage repair, and the like. In those aspects including a laser textured region, the semiconductor material can be annealed prior to laser treatment, following laser treatment, during laser treatment, or both prior to and following laser treatment. Annealing can enhance the semiconductive properties of the device, including increasing the photoresponse properties of the semiconductor materials. Additionally, annealing can reduce damage done by the lasing process. Although any known anneal can be beneficial and would be considered to be within the present scope, annealing at lower temperatures can be particularly useful. Such a "low temperature" anneal can greatly enhance the photoconductive gain and external quantum efficiency of devices utilizing such materials. In one aspect, for example, the semiconductor material can be annealed to a temperature of from about 300° C to about 1100 C°. In another aspect, the semiconductor material can be annealed to a temperature of from about 500° C to about 900° C. In yet another aspect, the semiconductor material can be annealed to a temperature of from about 700° C to about 800° C. In a further aspect, the semiconductor material can be annealed to a temperature that is less than or equal to about 850° C.

The duration of the annealing procedure can vary according to the specific type of anneal being performed, as well as according to the materials being used. For example, rapid annealing processes can be used, and as such, the duration of the anneal may be shorter as compared to other techniques. Various rapid thermal anneal techniques are known, all of which should be considered to be within the present scope. In one aspect, the semiconductor material can be annealed by a rapid annealing process for a duration of greater than or equal to about 1 μs. In another aspect, the duration of the rapid annealing process can be from about 1 μs to about 1 ms. As another example, a baking or furnace anneal process can be used having durations that may be longer compared to a rapid anneal. In one aspect, for example, the semiconductor material can be annealed by a baking anneal process for a duration of greater than or equal to about 1 ms to several hours. As has been described, if low oxygen content semiconductor materials are used it may be beneficial to anneal such materials in a substantially oxygen-depleted environment.

As has been described, annealing can help reduce defects inherent to the semiconductor substrate and otherwise reduce electron/hole recombination. In other

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SAMSUNG EX. 1002 - 3872/4148

words, the annealing can help create electron states that effectively reduce the undesirable recombination processes. Annealing the semiconductor material may also improve the responsivity or photoconductive gain of the device. Photoconductive devices can have dopants, impurities, or defects that can introduce energy levels that can trap carriers. Trapping carriers and reducing recombination of photocarriers can lead to an increase in photoconductive gain of the device. The relationship of photoconductive gain and trapping time can be represented by Equation (I):

$$\text{Gain} = \tau_L/\tau_t \qquad \text{(I)}$$

where "τ_L" is the lifetime of an excess carrier and "τ_t" is the transit time of the carriers across the device. It is understood that the lifetime of an excess carrier can be increased by trapping a carrier species and reducing the recombination rate. An increase in gain can be achieved by trapping centers in the semiconductor that have millisecond trapping times at room temperature and short transit times in thinned lightly doped wafers. These trapping locations can decrease the recombination of carriers and therefore improve or increase the photoconductive gain of the device by allowing more electrons to traverse the different regions without being recombined.

Turning to FIG. 2, a reflecting layer 20 can be coupled to the semiconductor substrate 12. The reflecting layer can be coupled to any side or portion of the semiconductor substrate in order to reflect electromagnetic radiation back into the device. Accordingly, in one aspect the reflecting layer can be located on the semiconductor substrate opposite the incoming electromagnetic radiation. Thus, as is shown in FIG. 2, electromagnetic radiation passing though the semiconductor substrate and the textured region 16 can be reflected back into the semiconductor substrate. Additionally, a passivation layer 22 can be coupled to the semiconductor substrate. The passivation layer is shown coupled to the side of the semiconductor substrate facing the incoming electromagnetic radiation, however a passivation layer can be located anywhere on the device and still be within the present scope.

As has been described, location of the textured region can be used to provide enhancement and/or filtering of the incoming electromagnetic radiation. For example, a textured region located at the point of entry of the electromagnetic radiation into the photosensitive device tends to bend the electromagnetic radiation, particularly the blue wavelengths. Accordingly, one level of tuning can be accomplished by locating

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SAMSUNG EX. 1002 - 3873/4148

the textured region on the surface adjacent the incident electromagnetic radiation to purposely effectuate the filtering of blue wavelengths. Additionally, absorption of particular wavelengths of electromagnetic radiation occurs at different depths in the semiconductor layer and/or textured region. By increasing the absorption to green wavelengths, for example, the electrical signal as a result of green wavelengths can be increased in a diode or pixel. Certain traditional 4 pixel imagers have one red, one blue, and two green pixels, with the greater number of green pixels to account for increased sensitivity of the human eye to green colors. Thus in one aspect, a 4 pixel imager can have one blue, one red, and one green pixel having an increased green wavelength absorption. The fourth pixel can be used for an IR or other wavelength selective pixel depending on the desired application of the imager.

FIG. 3 shows a photosensitive device having textured regions 30 located on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation normally exiting through the sides of the device to be further defused and absorbed within semiconductor substrate. The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.

FIG. 4 shows a photosensitive device having a textured region 40 having a nonparallel surface with respect to the semiconductor substrate 12. Thus the overall configuration of the textured region can be designed to further enhance absorption and/or selectively tune the device. As has been described, the nonparallel surface can have a variety of configurations, such as, without limitation, nonparallel slope, a pyramid, an inverted pyramid, a concave shape, a convex shape, and the like. In some cases the configuration of the textured region can function to direct or focus electromagnetic radiation into the semiconductor substrate, and in other cases the configuration of the textured region can function to direct or focus electromagnetic radiation away from the semiconductor substrate.

As is shown in FIG. 5, a lens 50 can be coupled to the semiconductor substrate 12 on a side facing incoming electromagnetic radiation. Thus the lens can focus the electromagnetic radiation into the semiconductor substrate. In those aspects having circuitry or other structures disposed on the incoming electromagnetic radiation surface, the lens can further focus light around such structures, thereby reducing optical scattering and noise.

As is shown in FIG. 6, a textured region 60 is located on the semiconductor substrate 12 adjacent to the multiple doped regions 14, 16. The textured region can be

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SAMSUNG EX. 1002 - 3874/4148

associated with at least one of the doped regions as is shown, or the textured region can be distinct from the doped regions (not shown). Electromagnetic radiation can enter the photosensitive device at the side adjacent the doped regions, or alternatively at the side opposite the doped regions.

FIGs. 7-11 show various steps in the manufacture of a photosensitive pixel according to aspects of the present disclosure. FIG. 7 shows a cross-section of a front side illumination (FSI) photosensitive pixel device. The photosensitive pixel device can include a semiconductor substrate 72, and can be referred to as bulk semiconductor material. The semiconductor substrate includes at least one doped region 74 that can be doped with an electron donating or hole donating species to cause the region to become more positive or negative in polarity as compared to the semiconductor substrate. In one aspect, for example, the doped region can be p doped. In another aspect the doped region can be n doped. A highly doped region 76 can be formed on or near the doped region to create a pinned diode. In one example, the semiconductor substrate can be negative in polarity, and the doped region and the highly doped region can be doped with p+ and n- dopants respectively. In some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type doping of the regions can be used. It should be noted that in one aspect the highly doped region can be the textured region. In other words, textured surface features can be formed on or in the highly doped region.

The device of FIG. 7 can further include various metal regions 78, at least one via 80, a passivation layer 82, trench isolation 84, and an electrical transfer element 86. Trench isolation elements can maintain pixel to pixel uniformity by reducing optical and electrical crosstalk. The trench isolation can be shallow (FIG. 7) or deep (FIG. 12) trench isolation. The trench isolation can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like. These trench isolation regions can be configured to reflect incident light until it is absorbed, thereby increase the effective absorption length of the device.

As is shown in FIG. 8, a carrier substrate or carrier wafer 88 can be coupled to the photosensing pixel. In one aspect, the carrier substrate can be disposed on the passivation layer 82, although the carrier substrate can be disposed on any surface of the device. In one aspect, for example, the carrier substrate can be disposed on the semiconductor substrate (not shown). The carrier substrate can be coupled to the

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SAMSUNG EX. 1002 - 3875/4148

photosensing pixel by various techniques, and any such coupling mechanism is within the present scope. In one aspect, for example, the coupling can occur by way of a bonding layer or adhesive layer disposed on the device, for example, on the passivation layer. The support substrate can provide support to the semiconductor device both during and after manufacture, depending on whether or not the support is removed. The carrier substrate can be made of a semiconductor material that is the same or similar to the bulk semiconductor material, or it can be made of a different material.

As is shown in FIG. 9, a textured region 90 is coupled to the semiconductor substrate 72 opposite the doped regions 74,76. Thus light entering from the direction of the doped regions passes through the semiconductor substrate prior to contacting the textured region. The textured region can be disposed across an entire surface of the semiconductor substrate, as is shown in FIG. 9, or it can be disposed on one or more discrete regions (not shown).

As is shown in FIG. 10, an additional carrier support substrate 100 can be coupled to the device on an opposing side from the carrier support substrate 88. The additional carrier support substrate can be utilized for a variety of purposes, including providing additional support to the device, facilitating the removal of the first carrier support substrate, and the like. A reflective layer 102 can be disposed between the textured region 90 and the carrier support substrate. Thus the reflective layer can reflect electromagnetic radiation that passes through the textured region back toward the semiconductor substrate 72, thus reducing optical loss and backscattering. Thus, in some aspects a reflective layer can increase the quantum efficiency of the device. The reflective layer material can be any reflective material that can be incorporated into such a device. Nonlimiting examples can include materials such as silver, aluminum, and the like.

As is shown in FIG. 11, the carrier support substrate can be removed to expose the passivation layer 82 or any other material layer that was previously covered by the carrier support substrate. The additional carrier substrate 100 can be maintained in the device, removed from the device, or thinned to reduce the thickness of the substrate depending on the intended use of the device. The removal of material from the device, including the carrier support substrate and the additional carrier substrate, can be accomplished by a variety of methods including, without limitation, etching, chemical mechanical polishing, ion implanting (i.e. smart cut), and the like.

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Various types of trench isolation are contemplated, and any such isolation is considered to be within the present scope. As has been described, trench isolation can be shallow (FIG. 7, 84) or deep (FIG. 12, 120) trench isolation. The trench isolation can also include depths between shallow and deep, depending on the device design. Trench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features. Thus the trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device. Additionally, in some aspects pillar features can be incorporated into pixels by thinning or removing material from the semiconductor substrate using deep trench isolation and etching techniques. As is shown in FIG. 13, the textured region 130 can have a nonparallel surface with respect to the semiconductor substrate 72 as has been described. This nonparallel morphology, when included with the deep trench isolation 120, can effectively focus electromagnetic radiation into the semiconductor substrate from multiple sides.

It is also contemplated, that a non-bulk material can be formed or disposed near a doped region in the device. The addition of the non-bulk material can allow for electromagnetic radiation diffusing features to be formed on or in the non-bulk material. A metal layer defining an aperture can also be included in one aspect of the present disclosure. The metal layer can be formed near the doped regions and can have a light entering region that defines an aperture. This light entering region can also include an antireflecting material.

Fig. 14 shows a photosensitive imager comprising two photosensitive pixels 140. Each photosensitive pixel includes a boundary region 142 that can include metal circuitry and a textured region 144. Each photosensitive pixel can include at least one transistor 146 or other electrical transfer element. Additional read out and circuitry elements 148 can be utilized and shared by both photosensitive pixels.

Turning to FIG. 15, a backside illuminated (BSI) photosensitive pixel according to one aspect present disclosure is provided. A lens 150 and an anti-reflective coating 152 are disposed on the backside of the pixel following thinning and trench isolation. A color filter 154 can be optically coupled to the lens to allow specific wavelengths filtering of the electromagnetic radiation. A textured region 156 can be coupled to the semiconductor substrate 72 opposite the lens in order to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes

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SAMSUNG EX. 1002 - 3877/4148

through to the front side of the pixel. Thus the electromagnetic radiation can be focused within the semiconductor substrate to the combined action of the textured region and the trench isolation 120

Fig. 16 shows a front side illuminated (FSI) imager according to another aspect of the present disclosure. A lens 160 and an antireflecting passivation layer on 62 are coupled to the front side of the pixel. A textured region 90 and a reflecting layer 102 are coupled to the semiconductor substrate 72 opposite the lens to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through the semiconductor substrate. An aperture 164 formed in a metal or other reflective material layer 166 can increase the effectiveness of the optical cavity. Thus the lens focuses electromagnetic radiation through the aperture.

In other aspects of the present disclosure, various methods of making photosensitive diodes, pixels, and imagers, are contemplated. In one aspect, as is shown in FIG. 17, a method of making a photosensitive imager device can include forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation 170. The method also includes coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction 172. In one aspect, multiple pixels can be associated together to form an imager. A passivation layer can also be disposed on the photosensitive imager device to protect and/or reduce the dark current of the device.

In another aspect of the present disclosure, a method for making a photosensitive diode is provided. Such a method can include forming at least one cathode and at least one anode on a surface of a semiconductor substrate, coupling a textured region to the semiconductor substrate, and coupling a support substrate to the semiconductor substrate. The textured region can be located adjacent to the anode and cathode, opposite the anode and cathode, or both adjacent and opposite the anode and cathode. An electrical transfer on the can be electrically coupled to at least one of the anode and cathode to form a photosensitive pixel. In another aspect, the semiconductor substrate can be thinned to improve the response rate and/or speed of the device. A passivation layer can also be disposed on the photosensitive diode to protect and/or reduce the dark current of the device. An additional support substrate can be attached to the device to provide additional support. In one aspect, the

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SAMSUNG EX. 1002 - 3878/4148

additional support substrate can be located on the opposite side of the photosensitive diode from the support substrate. The support substrate can subsequently be removed to allow for further processing.

Of course, it is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present disclosure. Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the present disclosure and the appended claims are intended to cover such modifications and arrangements. Thus, while the present disclosure has been described above with particularity and detail in connection with what is presently deemed to be the most practical embodiments of the disclosure, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

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SAMSUNG EX. 1002 - 3879/4148

CLAIMS

What is claimed is:

1. A photosensitive imager device, comprising:

a semiconductor substrate having multiple doped regions forming a least one junction;

a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation; and

an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction.

2. The device of claim 1, wherein the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation.

3. The device of claim 1, wherein interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region.

4. The device of claim 1, wherein the transfer element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

5. The device of claim 1, further comprising a reflective layer coupled to the semiconductor substrate and positioned to maintain the electromagnetic radiation in the semiconductor substrate.

6. The device of claim 1, wherein the textured region is positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions.

7. The device of claim 6, wherein the textured region has a surface morphology operable to direct electromagnetic radiation into or out of the semiconductor substrate.

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SAMSUNG EX. 1002 - 3880/4148

8. The device of claim 7, wherein the surface morphology of the textured region relative to the semiconductor substrate is a member selected from the group consisting of sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and combinations thereof.

9. The device of claim 1, wherein the textured region is positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions.

10. The device of claim 9, further comprising an additional textured region positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions.

11. The device of claim 1, wherein the textured region is coupled directly to at least one of the multiple doped regions.

12. The device of claim 1, wherein the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

13. The device of claim 12, wherein surface features include a member selected from the group consisting of cones, pillars, pyramids, micolenses, quantum dots, inverted features, and combinations thereof.

14. The device of claim 1, wherein the textured region has been formed by a process selected from the group consisting of lazing, chemical etching, nanoimprinting, material deposition, and combinations thereof.

15. The device of claim 1, further comprising a lens optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate.

16. A photosensitive imager array, comprising at least two photosensitive imager devices of claim 1.

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SAMSUNG EX. 1002 - 3881/4148

17. The array of claim 16, further comprising at least one trench isolation positioned between the at least two photosensitive imager device.

18. A method of making a photosensitive imager device, comprising:

forming a textured region on a semiconductor substrate, wherein the semiconductor substrate has multiple doped regions forming a least one junction, and wherein the textured region is formed in a position to interact with electromagnetic radiation; and

coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction .

19. The method of claim 18, wherein forming the textured region is by a process selected from the group consisting of lazing, chemical etching, nanoimprinting, material deposition, and combinations thereof.

20. The method of claim 18, wherein forming the textured region includes irradiating a target region with laser radiation to form surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

21. The method of claim 20, wherein irradiating the target region includes exposing the laser radiation to a dopant such that the irradiation incorporates the dopant into the textured region.

22. The method of claim 20, wherein the irradiation is performed using a pulsed laser including a member selected from the group consisting of a femtosecond laser, a picosecond laser, a nanosecond laser, and combinations thereof.

23. The method of claim 18, further comprising tuning an electrical response of the photosensitive imager device.

24. The method of claim 23, wherein tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation.

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SAMSUNG EX. 1002 - 3882/4148

25. The method of claim 23, wherein tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type of the textured region, thickness of the textured region, dopant type of the textured region, doping profile of the texture region, doping profile of the semiconductor substrate, thickness of the substrate, and combinations thereof.

26. The method of claim 18, wherein the transfer element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

27. The method of claim 18, further comprising annealing the semiconductor substrate to a temperature of from about 300° C to about 1100° C.

28. A photosensitive imager device, comprising:

a semiconductor substrate having multiple doped regions forming a least one junction;

a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation; and

at least 4 transistors coupled to the semiconductor substrate and with at least one of the transistors electrically coupled to the at least one junction.

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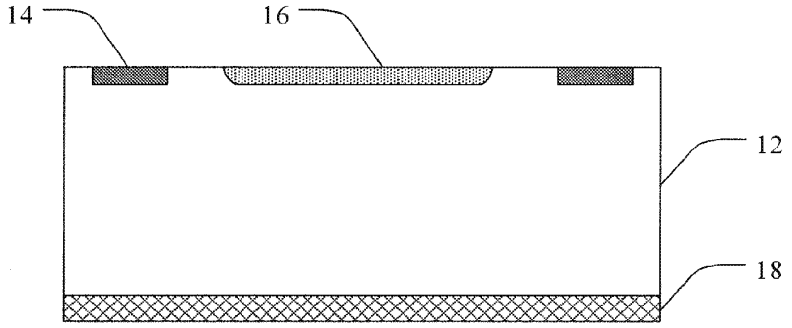


FIG. 1

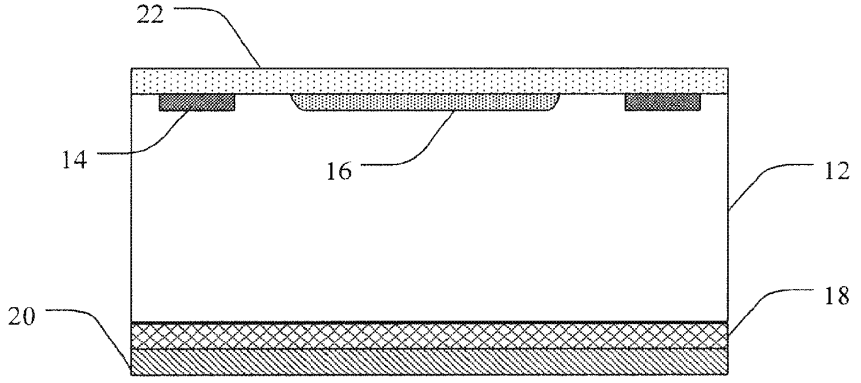


FIG. 2

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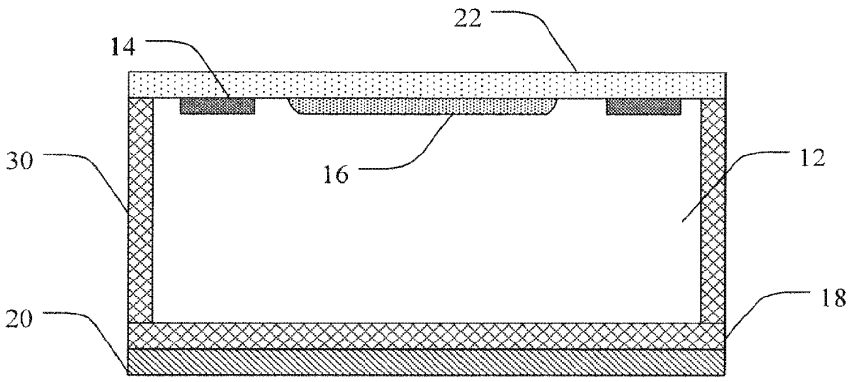


FIG. 3

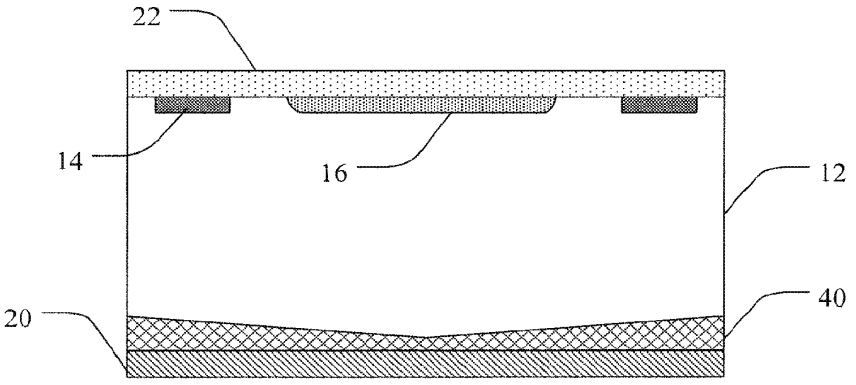


FIG. 4

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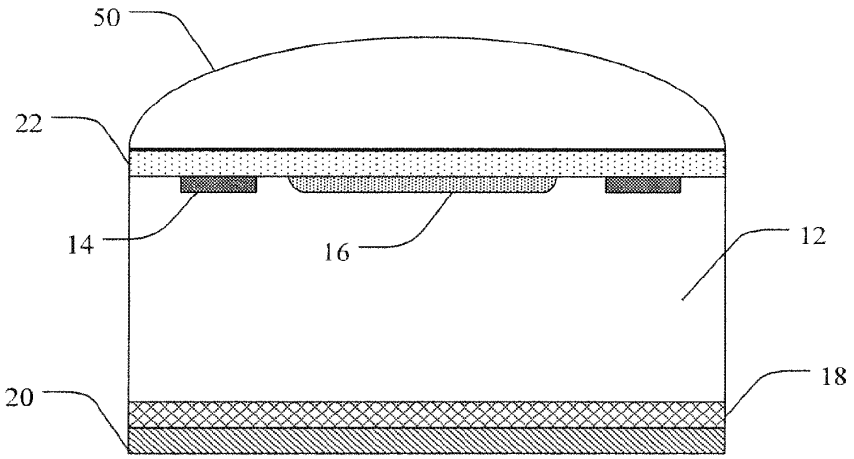


FIG. 5

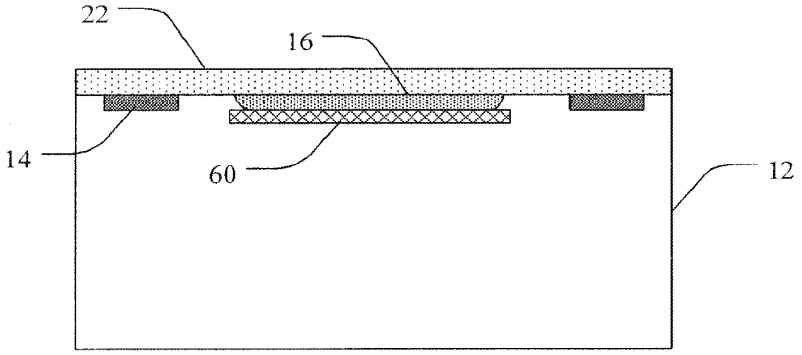


FIG. 6

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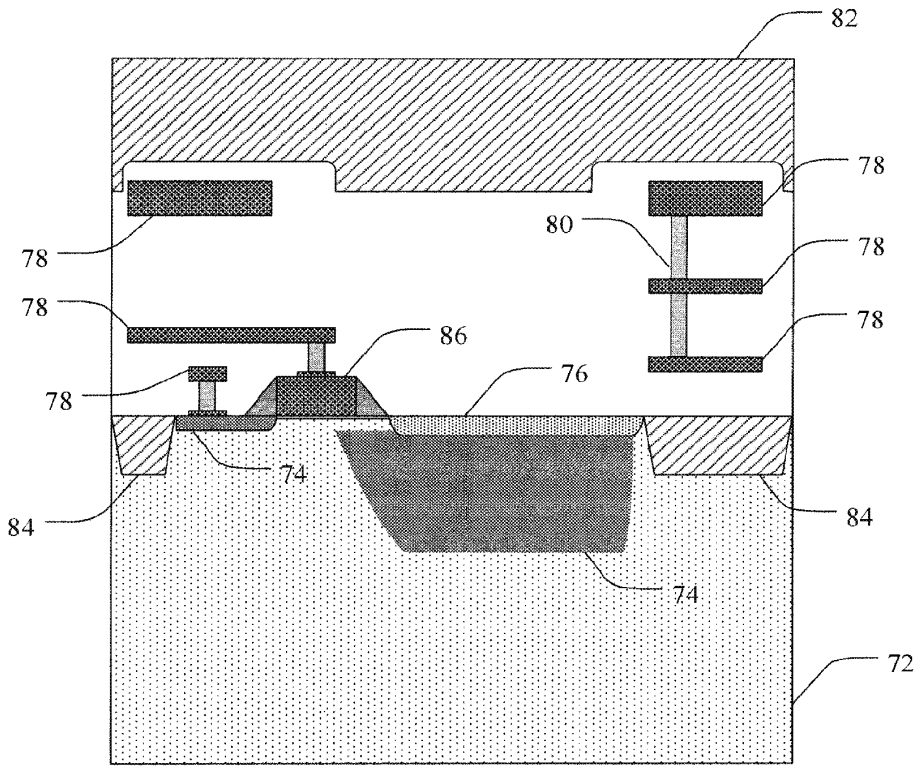


FIG. 7

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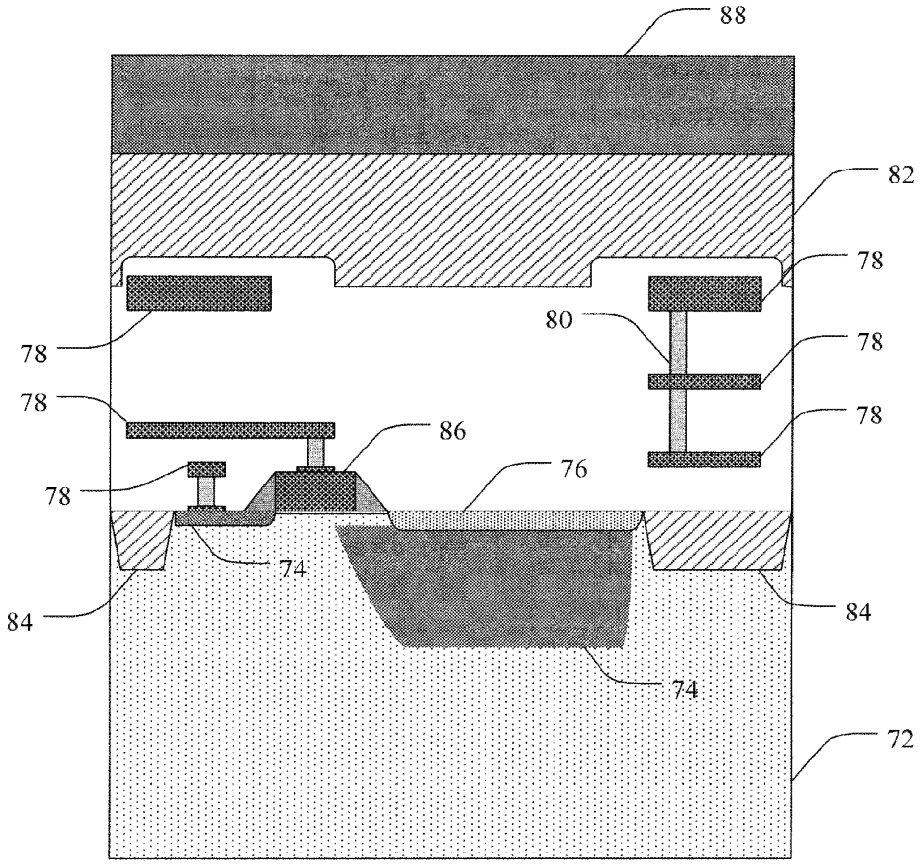


FIG. 8

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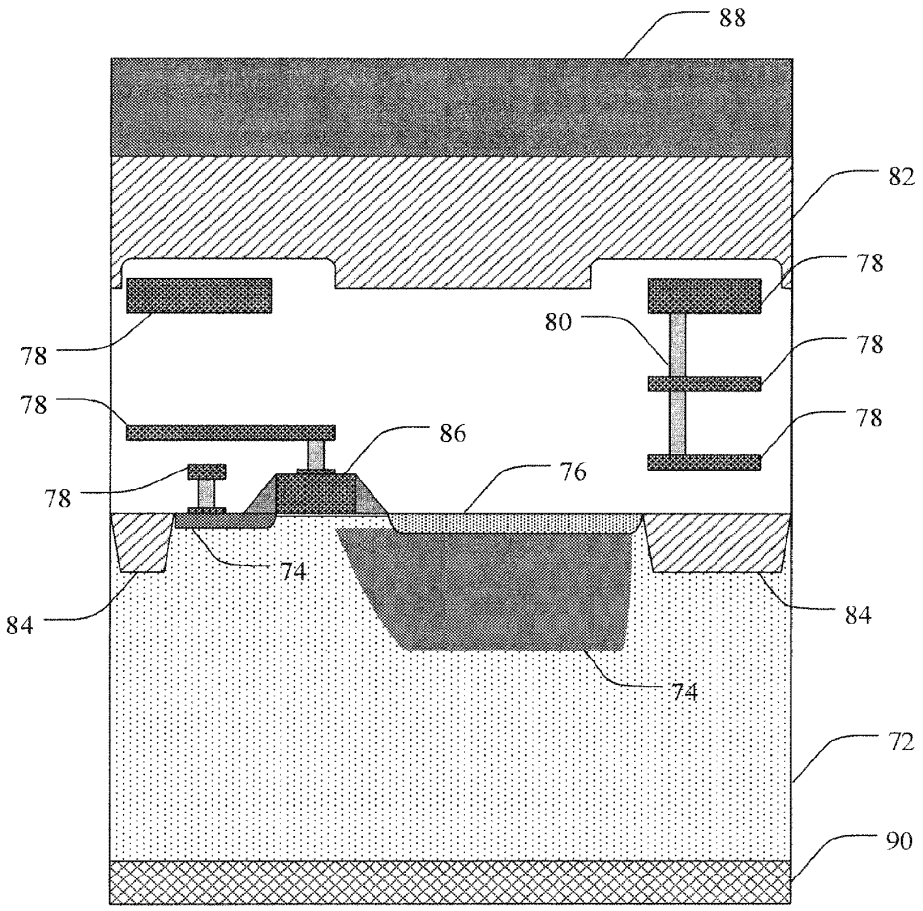


FIG. 9

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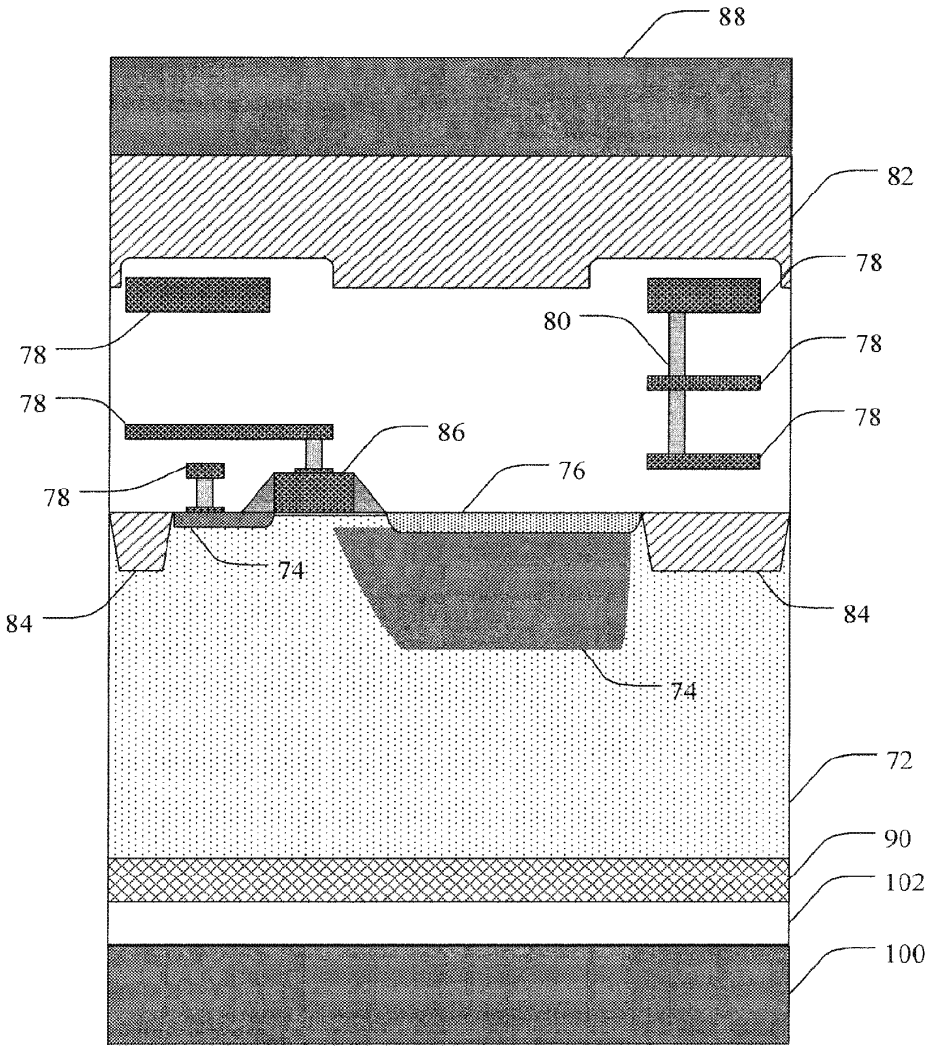


FIG. 10

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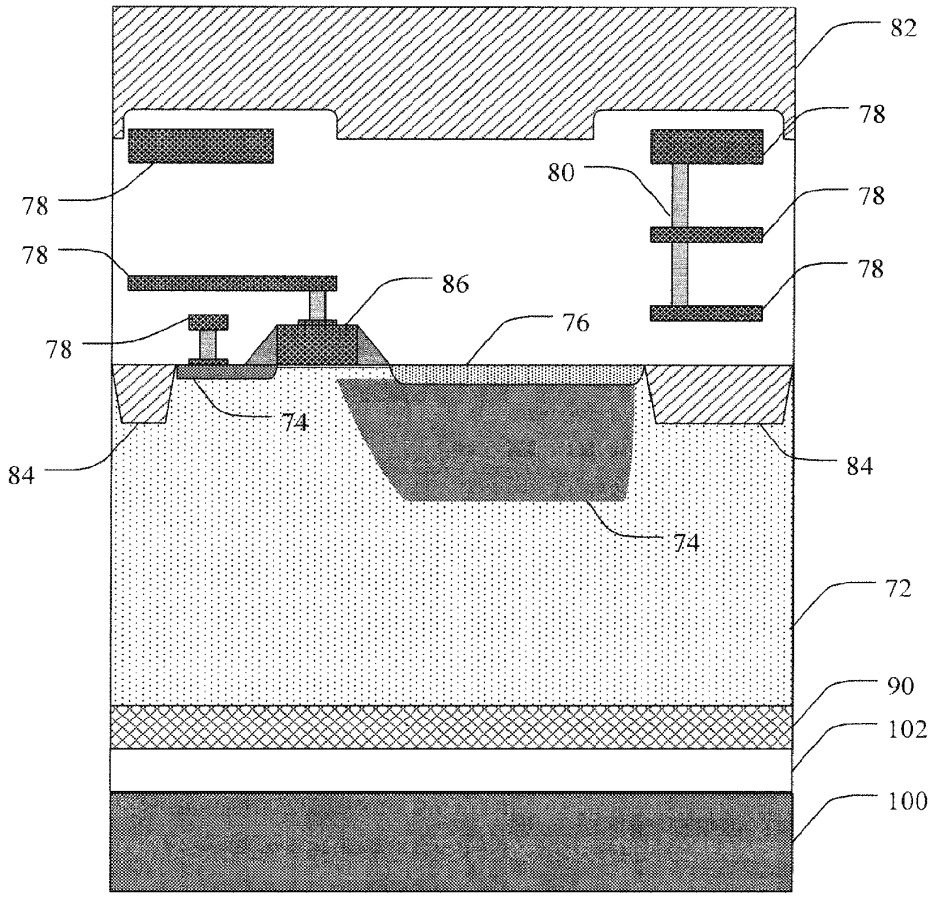


FIG. 11

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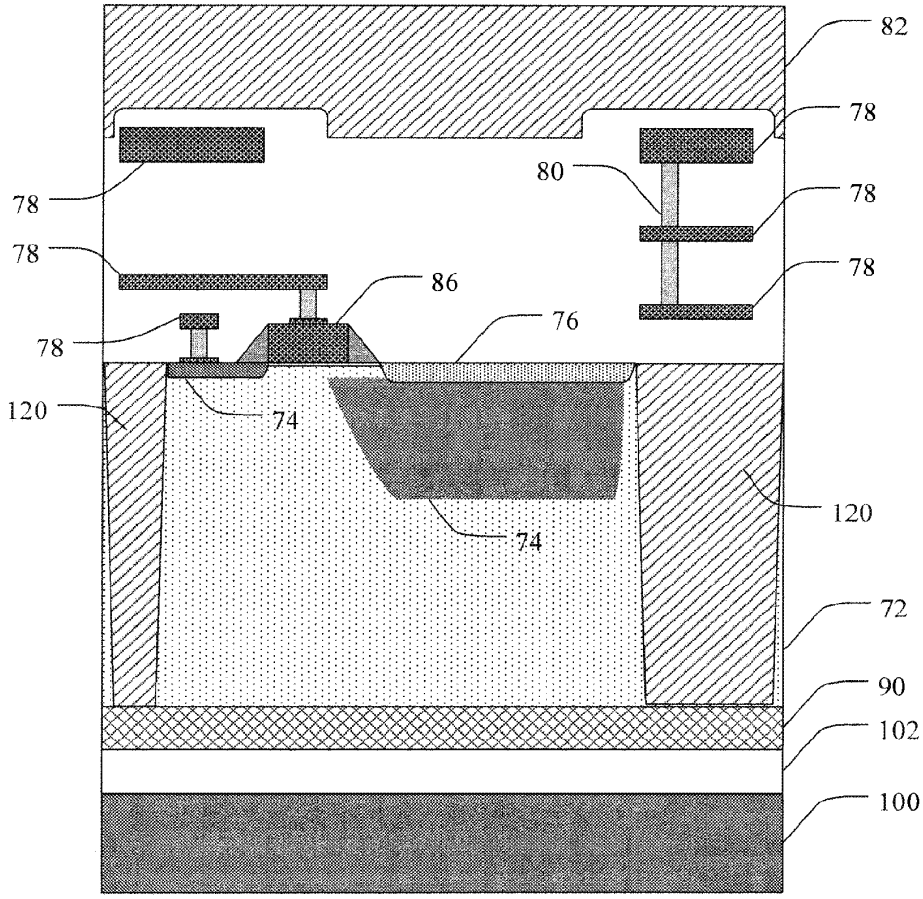


FIG. 12

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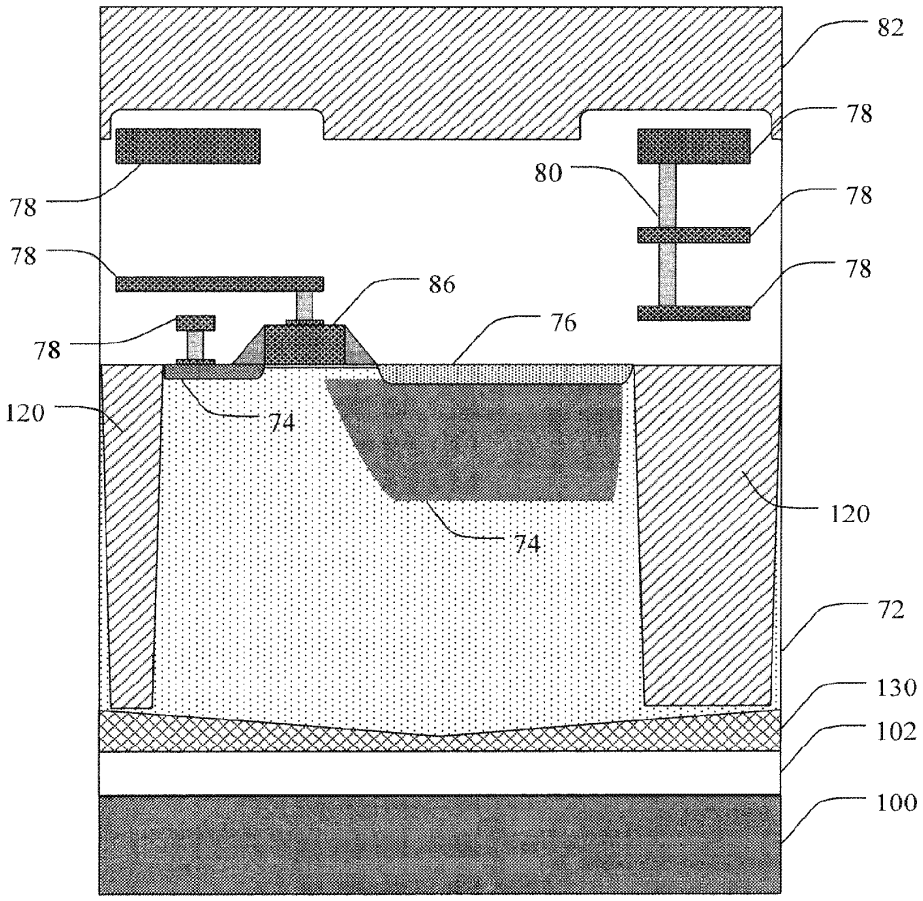


FIG. 13

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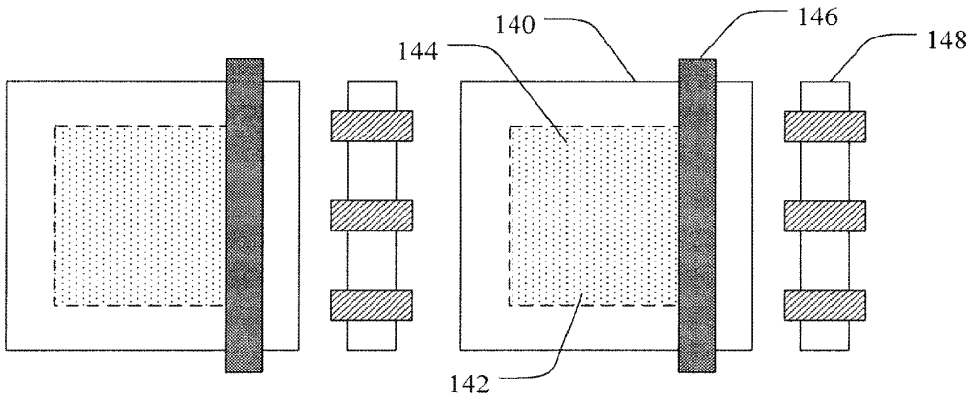


FIG. 14

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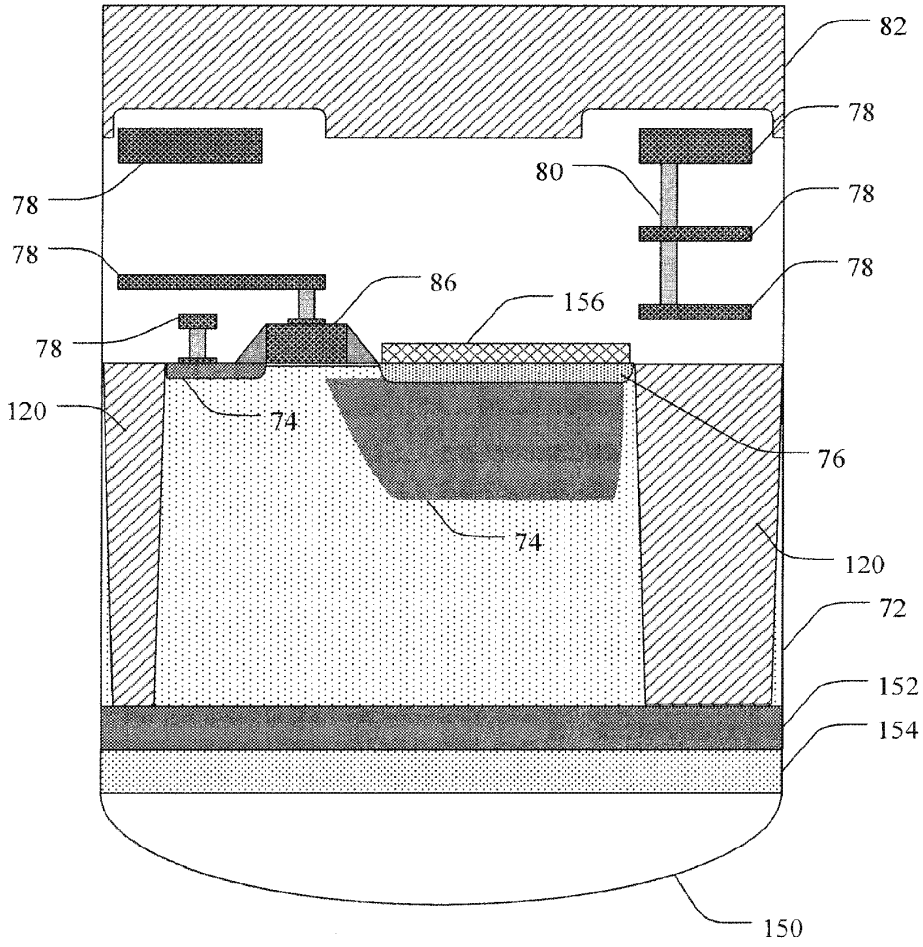


FIG. 15

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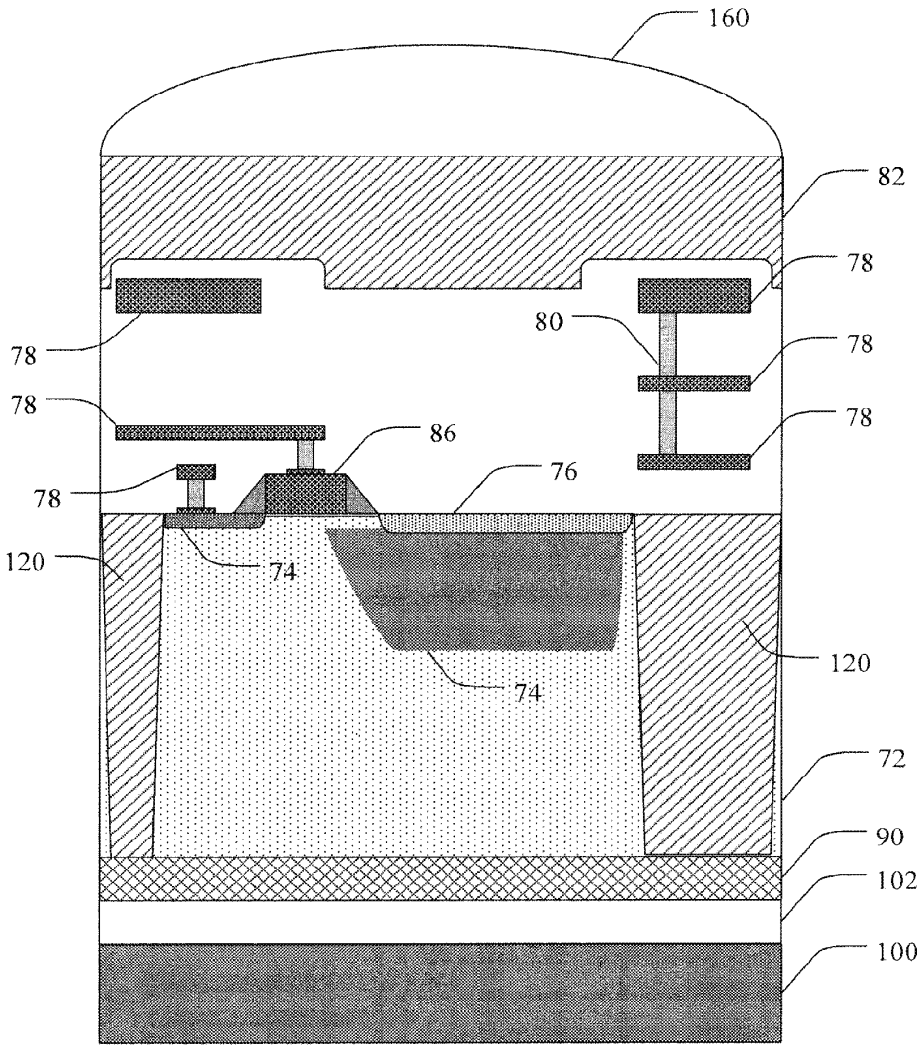


FIG. 16

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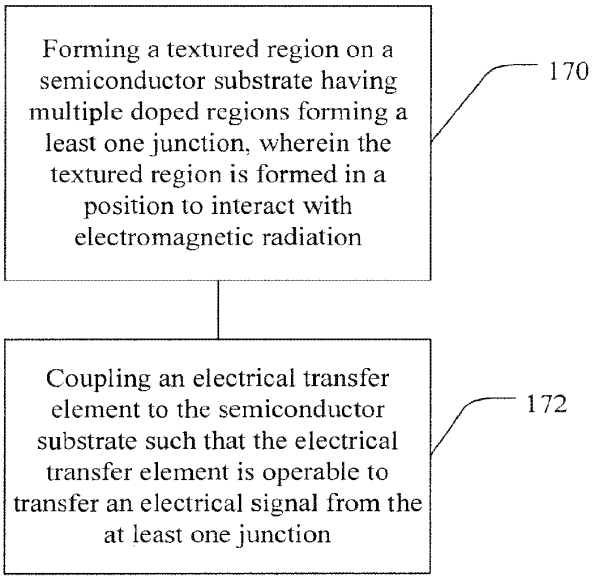


FIG. 17

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(54) **Title**: DEVICES HAVING ENHANCED ELECTROMAGNETIC RADIATION DETECTION AND ASSOCIATED METHODS

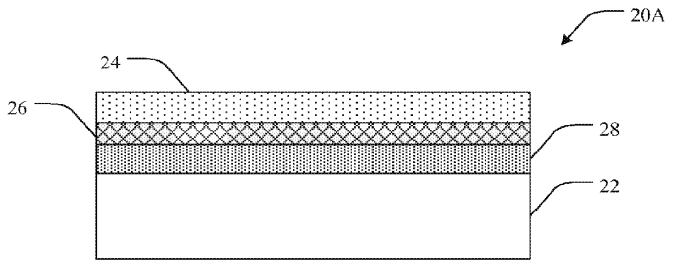


FIG. 2A

(57) **Abstract**: Photosensitive semiconductor devices and associated methods are provided. In one aspect, a semiconductor device can include a semiconductor substrate and a semiconductor layer coupled to the semiconductor substrate, where the semiconductor layer has a device surface opposite the semiconductor substrate. The device also includes at least one textured region coupled between the semiconductor substrate and the semiconductor layer. In another aspect, the device further includes at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer.

WO 2011/119618 A2

SAMSUNG EX. 1002 - 3898/4148

DEVICES HAVING ENHANCED ELECTROMAGNETIC RADIATION DETECTION AND ASSOCIATED METHODS

PRIORITY DATA

This application claims the benefit of U.S. Provisional Patent Application Serial No. 61/317,147, filed on March 24, 2010, which is incorporated herein by reference.

BACKGROUND

Semiconductor on Insulator (SOI) wafer technology is an outgrowth of MicroElectroMechanical Systems (MEMS) technologies. An SOI wafer is a stacked wafer substrate where a device wafer (typically silicon) is bonded to a dielectric layer that is bonded to a support wafer, otherwise known as a handle wafer. A typical process flow for the fabrication of SOI wafers can be as follows: two wafers are polished and coated with an oxide or other dielectric material. The wafers are mounted polished side face to face and bonded under high temperature and pressure. Then one of the two wafers is ground down using mechanical grinding and chemical mechanical polishing to a specific thickness. In this way it is possible to generate semiconductor wafers that are electrically isolated from the underlying substrate.

SUMMARY

The present disclosure provides semiconductor structures and devices that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. In one aspect, a semiconductor device is provided. Such a device can include a semiconductor substrate and a semiconductor layer coupled to the semiconductor substrate, where the semiconductor layer has a device surface opposite the semiconductor substrate. The device also includes at least one textured region coupled between the semiconductor substrate and the semiconductor layer. In another aspect, the device further includes at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer. In one aspect, the semiconductor layer is an epitaxially grown semiconductor layer. In another aspect, the semiconductor layer is a silicon layer. In a further aspect, a secondary semiconductor layer is disposed between the textured region and the semiconductor layer.

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SAMSUNG EX. 1002 - 3899/4148

Various positional configurations for the layers according to aspects of the present disclosure are contemplated, and any such configuration is considered to be within the present scope. In one specific aspect, for example, the dielectric layer is coupled between the semiconductor substrate and the textured region, and the textured region is disposed between the dielectric layer and the semiconductor layer. In one specific aspect, a reflective region is disposed between the semiconductor substrate and the textured region. In another specific aspect, the textured region is coupled directly to the semiconductor layer. In yet another specific aspect, a secondary semiconductor layer is disposed between the textured region and the semiconductor layer. In a further specific aspect, at least one cavity region disposed between the textured region and the dielectric layer. As another aspect of positional arrangement, the textured region is disposed between the semiconductor substrate and the dielectric layer, and the dielectric layer is disposed between the textured region and the semiconductor layer.

In one aspect of the present disclosure, a polysilicon layer is directly coupled to the dielectric layer. In another aspect, the polysilicon layer is disposed between multiple dielectric layers. In some aspects, the polysilicon layer can be doped.

In one aspect of the present disclosure, at least one photodiode optically active region is disposed on the device surface. In another aspect, the photodiode optically active region comprises a doped region. In yet another aspect, the device forms at least one photodetector. In a further aspect, the at least one photodetector is a plurality of photodetectors arranged in an array. In yet a further aspect, the textured region is arranged in a discontinuous pattern that corresponds spatially to the array of photodetectors. In another aspect, the device includes a plurality of isolation features in at least the semiconductor layer to isolate each photodetector in the array of photodetectors, where the isolation features isolate each photodetector electrically, optically, or both electrically and optically. In yet another aspect, the device includes at least one optical lens associated with the at least one photodetector. In a further aspect, the device includes at least one color filter associated with the at least one photodetector.

In one aspect of the present disclosure, the textured region is doped with a dopant to form an electrical back surface field. In another aspect, the electrical back surface field has been doped by a technique such as, without limitation, laser doping, ion implanting, diffusion doping, in situ doping, and the like, including combinations

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SAMSUNG EX. 1002 - 3900/4148

thereof. In yet another aspect, the textured region has a higher dopant concentration than the semiconductor layer. In a further aspect, the dopant has the same polarity as the semiconductor layer. Non-limiting examples of such dopants can include boron, indium, gallium, arsenic, antimony, phosphorus, and the like, including combinations thereof. Additionally, in other aspects a back surface field can be created by doping the semiconductor layer outside of the textured region. In one aspect, for example, the semiconductor layer is doped with a dopant to form an electrical back surface field, where the electrical back surface field is distinct from the textured region.

The present disclosure additionally provides methods of making semiconductor devices. In one aspect, one such method includes texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate. In one aspect, the semiconductor layer is an epitaxially grown semiconductor layer. In another aspect, texturing at least a portion of a surface of a semiconductor layer to form a textured region further includes forming the epitaxially grown semiconductor layer on a growth substrate and texturing at least a portion of a surface of the epitaxially grown semiconductor layer to form a textured region. In yet another aspect, the method includes removing the growth substrate to expose the epitaxially grown semiconductor layer. In an alternative aspect, the method can include forming an epitaxially grown semiconductor layer on the semiconductor layer on an opposite side from the textured region.

In another aspect, wafer bonding includes depositing a polysilicon layer on the first dielectric layer and then bonding the polysilicon layer between the first dielectric layer and the second dielectric layer. In yet another aspect, at least a portion of the polysilicon layer can be doped. It is also contemplated that the present scope can include multiple dielectric and/or semiconductor material layers disposed between the semiconductor substrate and semiconductor layer.

In a further aspect, texturing at least a portion of a surface of the semiconductor layer to form the textured region further includes forming an opening in the semiconductor substrate, the second dielectric layer, and the first dielectric layer to expose a portion of the semiconductor layer and texturing at least a portion of the exposed portion of the semiconductor layer to form the textured region.

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SAMSUNG EX. 1002 - 3901/4148

In another aspect, the present disclosure provides a method of protecting a textured region from contamination during manufacture of a semiconductor device. Such a method includes texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate, wherein the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

For a further understanding of the nature and advantage of the present disclosure, reference is being made to the following detailed description of embodiments and in connection with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view of a semiconductor structure in accordance with an embodiment of the present disclosure;

FIG. 2A is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2B is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2C is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2D is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 3 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 4 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 5 is a cross-sectional view of a semiconductor photodiode in accordance with another embodiment of the present disclosure;

FIG. 6 is a cross-sectional view of a semiconductor photodetecting imager in accordance with another embodiment of the present disclosure;

FIG. 7 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

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SAMSUNG EX. 1002 - 3902/4148

FIG. 8 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 9 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 10 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 11A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 11B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 11C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

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FIG. 13D is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure; and

FIG. 14 is a depiction of a method of making a semiconductor device in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations. Although any texturing technique is considered to be within the present scope, in one aspect the texturing is formed by the irradiation of laser pulses. Furthermore, while the characteristics of a textured surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers), nanopores, and the like. In another aspect, such a surface can include micron-sized structures (e.g. about 2 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm.

As used herein, the terms "surface modifying," "surface modification," and "texturing" can be used interchangeably, and refer to the altering of a surface of a

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SAMSUNG EX. 1002 - 3904/4148

semiconductor material using a texturing technique. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping the material.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified using laser radiation. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

As used herein, the term "absorptance" refers to the fraction of incident electromagnetic radiation absorbed by a material or device.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

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As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

The present disclosure provides semiconductor devices and associated methods that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. Additionally, the present disclosure provides an integrated approach for the fabrication and application of textured semiconductor materials resulting in enhancement of image sensors and photodetectors. Specific types of semiconductor texturing can enhance the spectral bandwidth, absorption, and quantum efficiency of a semiconductor material. Performance can also be enhanced through various architecture configurations. Such configurations can also significantly improve the process integration of a particular device architecture with traditional process flows such as, for example, traditional CMOS process flows.

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A device design having a textured region located on, for example, the back surface of a photodetector, provides significant performance benefits. The textured region can have surface features that can lead to higher recombination of photocarriers for short wavelengths (e.g. in the blue green part of the spectrum) due to the very shallow penetration of those wavelengths into the detecting volume of the device. By physically locating the textured on the back surface of the device, a pristine surface is provided for the collection of short wavelengths on the top surface (i.e. the light incident surface), and the longer wavelengths that penetrate deep into or through the detecting region of the semiconductor material are collected by or with the help of the textured region opposite the light incident surface. It should be noted that, in addition to backside illuminated, front side illuminated architectures are also contemplated to be within the present scope. In addition, enhanced performance and ease of manufacture can also be accomplished by locating a textured region within a semiconductor stack or wafer. In some aspects, the textured layer can be located within the semiconductor stack early in the manufacturing process prior to the deposition of structures or circuitry that may be negatively affected by a texturing process. Additionally, such a semiconductor stack can be sent to an outside fabrication process for further manufacturing without exposing technological details regarding the textured region embedded between the semiconductor layers or any interaction between the textured region and the semiconductor layers.

In one aspect, as is shown in FIG. 1, a semiconductor device 10 is provided. While various semiconductor functions are contemplated, in one aspect the semiconductor device can exhibit enhanced electromagnetic radiation detection. Such a device can include a semiconductor substrate 12 and a semiconductor layer 14 coupled to the semiconductor substrate. The semiconductor layer has a device surface 15 opposite the semiconductor substrate. The device also includes at least one textured region 16 located or coupled between the semiconductor substrate and the semiconductor layer. As such, the textured region is enclosed between the semiconductor substrate and the semiconductor layer. Subsequent processing of the semiconductor device such as, for example, the formation of structures on the device surface, does not affect this buried textured region. In one aspect, the textured region can be formed on the semiconductor substrate. In another aspect, the textured region can be formed on the semiconductor layer. Additionally, for FIG. 1 and subsequent figures, the textured region can be a single textured region as is shown, or the textured

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region can be multiple discrete textured regions. Also, the textured region can cover only a portion of the surface area between the semiconductor substrate and the semiconductor layer as is shown, or the textured region can cover the entire surface area there between.

In another aspect, as is shown in FIG. 2A, a semiconductor device 20A is provided. Such a device can include a semiconductor substrate 22 and a semiconductor layer 24 coupled to the semiconductor substrate. The device also includes at least one textured region 26 located or coupled between the semiconductor substrate and the semiconductor layer, and at least one dielectric layer 28 coupled between the semiconductor substrate and the semiconductor layer. While various utilities are contemplated for the dielectric layer, in one aspect such a layer can be used to wafer bond the semiconductor layer to the semiconductor substrate. In one aspect, the dielectric layer can be formed on the semiconductor substrate. In another aspect, the dielectric layer can be formed on the textured region. Also, in some aspects the textured region can be formed on the dielectric layer. Additionally, in one aspect the semiconductor layer can be an epitaxially grown semiconductor layer. Thus in some aspects, the textured region can be formed on the epitaxially grown semiconductor layer.

It should be noted that, for all aspects, the present scope can also include multiple dielectric layers and/or multiple semiconductor material layers disposed between the semiconductor substrate and semiconductor layer. Additionally, the semiconductor layer itself can be multiple semiconductor layers and the semiconductor substrate can include multiple layers. It should also be noted that the semiconductor substrate refers to a substrate for a semiconductor, and can be comprised of semiconductor materials and/or non-semiconductor materials.

FIG. 2B shows a semiconductor device 20B having a secondary semiconductor layer 27 located between the textured region and the semiconductor layer. A semiconductor layer 24 is formed on the secondary semiconductor layer. In one aspect the semiconductor layer is an epitaxially grown semiconductor layer. Thus in some aspects, the textured region can be formed on the secondary semiconductor layer or on the dielectric layer 28. It should be noted that all reference numbers in FIGs. 2B-D that have been reused from FIG. 2A denote the same or similar materials and/or structures whether or not further description is provided.

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SAMSUNG EX. 1002 - 3908/4148

FIG. 2C shows a semiconductor device 20C whereby the dielectric layer 28 coupled between the semiconductor layer and the textured region. In this case, the dielectric layer can be formed on the semiconductor layer 24, the textured region 28, or on both the semiconductor layer and the textured region. In one aspect, the textured region can be formed on the semiconductor substrate 22. In another aspect, the textured region can be formed on the dielectric layer.

Additionally, in some aspects, as is shown in FIG. 2D for semiconductor device 20D, the dielectric layer can be a plurality of dielectric layers 28. In the case of wafer bonding, for example, a first dielectric layer can be associated with the textured layer and a second dielectric layer can be associated with the semiconductor substrate. The first dielectric layer and the second dielectric layer are heated and pressed together, with or without the aid of further pressure, temperature, or plasma surface activation, to cause the dielectric layers to bond to one another, thus forming a single wafer-bonded structure. It should be noted, however, that wafer-bonding can be accomplished without one or more dielectric layers, and as such the present scope should also include wafer-bonding that lacks such dielectric materials. Additionally, in some aspects, the textured region can be located in between the plurality of dielectric layers (not shown).

A variety of semiconductor materials are contemplated for use with the devices and methods according to aspects of the present disclosure. Such materials can be utilized as the semiconductor layer and/or the semiconductor substrate, as well as for the secondary semiconductor layer and the epitaxially grown semiconductor layer. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

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SAMSUNG EX. 1002 - 3909/4148

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows the desired property or functionality of the semiconductor device, and thus any such thickness of semiconductor material is considered to be within the present scope. The textured region can increase the efficiency of the device such that, in some aspects, the semiconductor material can be thinner than has previously been possible. Decreasing the thickness reduces the amount of semiconductor material used to make such a device. In one aspect, for example, a semiconductor material such as the semiconductor layer has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm. In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor material can have a

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SAMSUNG EX. 1002 - 3910/4148

thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

Additionally, various configurations of semiconductor materials are contemplated, and any such material configuration that can be incorporated into a semiconductor device is considered to be within the present scope. In one aspect, for example, the semiconductor material can include monocrystalline materials. In another aspect, the semiconductor material can include multicrystalline materials. In yet another aspect, the semiconductor material can include microcrystalline materials. It is also contemplated that the semiconductor material can include amorphous materials.

As has been described, the semiconductor substrate can be of any size, shape, and material capable of supporting the semiconductor layer and associated components during manufacture and/or use. The semiconductor substrate can be made from various materials, including the semiconductor materials described above, as well as non-semiconductor materials. Non-limiting examples of such materials can include metals, polymeric materials, ceramics, glass, and the like. In some aspects, the semiconductor substrate and the semiconductor layer have the same or substantially the same thermal expansion properties.

Furthermore, the semiconductor material according to aspects of the present disclosure can comprise multiple layers. In some aspects, layers can vary in majority carrier polarity (i.e. donor or acceptor impurities). The donor or acceptor impurities are typically determined by the type of dopant/impurities introduced into the device either through a growth process, deposition process, epitaxial process, implant process, lasing process or other known process to those skilled in the art. In some aspects such semiconductor materials can include an n-type layer, an intrinsic (i-type) layer, and a p-type layer, thus forming a p-i-n semiconductor material stack that creates a junction and/or depletion region. A semiconductor material devoid of an i-type layer is also contemplated in accordance with the present disclosure. In other aspects the semiconductor material may include multiple junctions. Additionally, in some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type semiconductor layers can be used. The minus and positive signs are indicators of the relative magnitude of the doping of the semiconductor material.

As has been described, the textured region is buried between the semiconductor substrate and the semiconductor layer in various architectural

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SAMSUNG EX. 1002 - 3911/4148

arrangements. The textured can be of various thicknesses, depending on the desired use of the material. In one aspect, for example, the textured region has a thickness of from about 500 nm to about 100 μm. In another aspect, the textured region has a thickness of from about 500 nm to about 15 μm. In yet another aspect, the textured region has a thickness of from about 500 nm to about 2 μm. In a further aspect, the textured region has a thickness of from about 500 nm to about 1 μm. In another aspect, the textured region has a thickness of from about 200 nm to about 2 μm.

The textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to further increase the effective absorption length of the device. Non-limiting examples of shapes and configurations of surface features include cones, pillars, pyramids, microlenses, quantum dots, inverted features, gratings, protrusions, sphere-like structures, and the like, including combinations thereof. Additionally, surface features can be micron-sized, nano-sized, or a combination thereof. For example, cones, pyramids, protrusions, and the like can have an average height within this range. In one aspect, the average height would be from the base of the feature to the distal tip of the feature. In another aspect, the average height would be from the surface plane upon which the feature was created to the distal tips of the feature. In one specific aspect, a feature (e.g. a cone) can have a height of from about 50 nm to about 2 μm. As another example, quantum dots, microlenses, and the like can have an average diameter within the micron-sized and/or nano-sized range.

In addition to or instead of surface features, the textured region can include a textured layer. In one aspect, for example, the textured region can include a substantially conformal textured layer. Such a textured layer can have an average thickness of from about 1 nm to about 20 μm. In those aspects where the textured region includes surface features, the conformal textured layer can have a varying thickness relative to the location on the surface features upon which is deposited. In the case of cones, for example, the conformal textured layer can become thinner toward the tips of the cones. Such a conformal layer can include various materials, including, without limitation, SiO_2, Si_3N_4, amorphous silicon, polysilicon, a metal or metals, and the like, including combinations thereof. The conformal textured layer can also be one or more layers of the same or different materials, and can be formed during the creation of surface features or in a separate process.

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Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The materials used for making the textured region can vary depending on the design and the desired characteristics of the device. As such, any material that can be utilized in the construction of a textured region is considered to be within the present scope. In one aspect, for example, the texture region can be a textured portion of a specific material, such as a portion of the semiconductor layer or the semiconductor substrate. If the texture layer is to be associated with the semiconductor layer, for example, a surface facing the semiconductor substrate can be textured prior to an attachment process such as wafer bonding. In another aspect, the textured region can be formed from a material that is deposited onto the semiconductor layer or semiconductor substrate, or the textured layer itself can be deposited. Such materials can include a semiconductor material, a dielectric material, or the like, including combinations thereof. In one specific example, the deposited material can include a silicon material. In another specific example, the deposited material can be polysilicon. In yet another aspect, the deposited material can be a dielectric material.

The texturing process can texture the entire substrate to be processed or only a portion of the substrate. In one aspect, for example, a substrate such as the semiconductor layer can be textured and patterned by an appropriate technique over an entire surface to form the texture region. In another aspect, a substrate such as the semiconductor layer can be textured and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern.

In addition to surface features, the textured region can have a surface morphology that is designed to focus or otherwise direct electromagnetic radiation. For example, in one aspect the textured region has a surface morphology operable to direct electromagnetic radiation into the semiconductor layer. Non-limiting examples of various surface morphologies include sloping, pyramidal, inverted pyramidal, spherical, square, rectangular, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

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SAMSUNG EX. 1002 - 3913/4148

The textured region, including surface features as well as surface morphologies, can be formed by various techniques, including plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, selective epitaxial growth, and the like.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete target areas of a substrate to be textured, as well as entire surfaces. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection.

In one aspect, for example, a target region of the substrate to be textured can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a substrate material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can passed through a dopant carrier and onto the substrate surface. In this way, dopant from the dopant carrier is introduced into the target region of the substrate material. Such a region incorporated into a substrate material can have various benefits in accordance with aspects of the present disclosure. For example, the textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption. In one aspect, such a textured region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of a substrate material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the substrate. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the substrate at the target region is thus chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the formation of surface features appearing as structures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the substrate material.

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SAMSUNG EX. 1002 - 3914/4148

In some aspects, the features or structures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed.

The type of laser radiation used to surface modify a material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to, the wavelength of the laser radiation, pulse width, pulse fluence, pulse frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsatile lasing of a material. A short-pulsed laser is one capable of producing femtosecond, picosecond, and/or nanosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm, and more specifically from about 200 nm to about 1200 nm. The pulse width of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse widths can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse widths can be in the range of from about 50 picoseconds to 100 nanoseconds. In another aspect, laser pulse widths are in the range of from about 50 to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a target region can be from about 2 to about 1000. Further, the repetition rate or frequency of the pulses can be selected to be in a range of from about 10 Hz to about 10 μHz, or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2, or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2.

A variety of dopant materials are contemplated for both the formation of doped regions in the semiconductor layer and for doping of the textured region, and any dopant that can be used in such processes to modify a material is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the material being doped, as well as the intended use of the resulting material.

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SAMSUNG EX. 1002 - 3915/4148

A dopant can be either a charge donating or a charge accepting dopant species. More specifically, an electron donating or a hole donating species can cause a region to become more positive or negative in polarity as compared to the substrate upon which the rests. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped.

In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of from about 5×10^{14} to about 3×10^{20} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, $POCl_3$, P_2O_5, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. As one non-limiting example, SF_6 gas is a good carrier for the incorporation of sulfur into a substrate via a laser process without significant adverse effects on the material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic

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SAMSUNG EX. 1002 - 3916/4148

solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

In one aspect, the textured region can be doped with a dopant to form an electrical back surface field (EBSF). The EBSF impedes the movement of minority carriers from reaching the textured region, thus keeping such carriers away from potential recombination sites near the interface. Similarly, dark current generation can also be minimized by pinning the interface generation states at certain band energy states through band structure optimization so that the dark carrier generation mechanism is suppressed. Band structure optimization can be achieved by using a variety of methods. It should be noted that any method that forms an electrical field near or within the textured region can be used. Non-limiting examples of such methods can include shifting the Fermi level energy, bending the minority carrier band, inserting a material with a different bandgap, and the like, including combinations thereof.

In one aspect, for example, the band structure optimization can be realized by modifying the interface doping concentration. For example, for a p-type laser textured region, a more heavily p-doped layer that partially overlaps with the laser modified interface can be used. The conduction band thus bends toward the higher energy direction when reaching towards the more p-doped layer, and hence the laser modified interface. One specific aspect is a heavily doped p++ layer that partially overlaps with the laser modified interface layer in a p-epi substrate where both the p++ layer and the modified interface layer sit between the bottom of an epitaxial device layer and the top of a carrier wafer.

As such, in one aspect, the EBSF has been doped by a technique such as, without limitation, laser doping, ion implanting, diffusion doping, in situ doping, and the like, including combinations thereof. In another aspect, the textured region or the EBSF has a higher dopant concentration than the semiconductor layer. In yet another aspect, the dopant has the same polarity as the semiconductor layer. Various dopants for use in generating an EBSF are contemplated. Non-limiting examples include boron, indium, gallium, arsenic, antimony, phosphorus, and the like, including combinations thereof. It should also be noted that an EBSF can be produced in the semiconductor layer, the dielectric layer, or the semiconductor substrate. In one aspect, for example, semiconductor layer or the semiconductor substrate is doped with

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SAMSUNG EX. 1002 - 3917/4148

a dopant to form an electrical back surface field, where the EBSF is distinct from the textured region.

In another aspect, the band structure optimization can be realized by forming a heterojunction along a modified semiconductor interface. For example, a layer of amorphous silicon can be deposited on the textured region interface, thus forming a heterojunction that bends the minority carrier band towards the desired energy direction.

The dielectric layer can be made from a variety of materials, and such materials can vary depending on the device design and desired characteristics. One use for such a layer involves the coupling of the semiconductor layer to the semiconductor substrate. In some cases, wafer bonding can be used as a coupling technique. The dielectric layer can thus facilitate the attachment of these materials together, as has been described. The dielectric layer can be associated with the semiconductor layer, the semiconductor substrate, or both the semiconductor layer and the semiconductor substrate prior to bonding. In those aspects having a dielectric layer associated with both materials, the dielectric layers can be bonded directly together, or in some cases, bonded together with an intervening textured region. Additionally, in some aspects a textured region can be formed on one or more dielectric layers. In some aspects, a dielectric layer can be bonded to a semiconductor material such as, for example, polysilicon. In other aspects, the semiconductor layer and the semiconductor substrate can be bonded together without an intervening dielectric layer.

Non-limiting examples of dielectric layer materials can include oxides, nitrides, oxynitrides, and the like, including combinations thereof. In one specific aspect, the dielectric layer includes an oxide. In another aspect, the dielectric layer includes a buried oxide. Additionally, the dielectric layer can be of various thicknesses. In one aspect, for example, the dielectric layer has a thickness of from about 100 nm to about 4 microns. In another aspect, the dielectric layer has a thickness of from about 500 nm to about 2 microns. In yet another aspect, the dielectric layer has a thickness of from about 500 nm to about 1000 microns.

The devices according to aspects of the present disclosure can additionally include one or more reflecting regions. In one aspect, as is shown in FIG. 3, a photosensitive semiconductor device 30 can include a semiconductor substrate 32 and a semiconductor layer 34 coupled to the semiconductor substrate. The device also

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SAMSUNG EX. 1002 - 3918/4148

includes at least one textured region 36 located or coupled between the semiconductor substrate and the semiconductor layer, and at least one dielectric layer 38 coupled between the semiconductor substrate and the semiconductor layer. A reflecting region 39 is coupled to the semiconductor substrate, and positioned to interact with electromagnetic radiation. The reflecting region can be separated from the textured region by a dielectric layer as is shown, or the reflecting region can be associated directly with the textured region without an intervening dielectric layer. The reflecting region can be deposited over the entire interface between the semiconductor substrate and the next adjacent layer, or only over a portion of the interface. In some aspects, the reflecting region can be deposited over a larger area of the device compared to the textured region. The reflecting region can be positioned to reflect electromagnetic radiation that has passed through the texture region back through the textured region toward the semiconductor layer. In other words, as electromagnetic radiation passes through the semiconductor layer, a portion that is not absorbed contacts the textured region. Of that portion that contacts the textured region, a smaller portion may pass though the textured region to strike the reflecting region and be reflected back through the textured region toward the semiconductor layer.

A variety of reflective materials can be utilized in constructing the reflecting region, and any such material capable of incorporation into a photosensitive device is considered to be within the present scope. Non-limiting examples of such materials include a Bragg reflector, a metal reflector, a metal reflector over a dielectric material, a transparent conductive oxide such as zinc oxide, indium oxide, or tin oxide, and the like, including combinations thereof. Non-limiting examples of metal reflector materials can include silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like, including combinations thereof. In one aspect, a dielectric material can be coupled to the reflecting region along the side facing the textured region. In one specific aspect, the dielectric material can include an oxide layer and the reflecting region can include a metal layer. The surface of the metal layer on an oxide acts as a mirror-like reflector for the incident electromagnetic radiation from the backside.

Additionally, the textured surface of a metal on a roughened oxide can act as a diffusive scattering site for the incident electromagnetic radiation and also as a mirror-like reflector. Other aspects can utilize porous materials for the texturing. Porous polysilicon, for example, can be oxidized or oxide deposited and a reflective region

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SAMSUNG EX. 1002 - 3919/4148

such as a metal reflector can be associated therewith to provide a scattering and reflecting surface. In another aspect, aluminum can be subjected to anodic oxidation to provide porous aluminum oxide, a high dielectric constant insulator. This insulator can be coated with aluminum or other metals to provide a scattering and reflecting surface.

In one specific aspect, a reflective region can include a transparent conductive oxide, an oxide, and a metal layer. The transparent oxide can be textured and a metal reflector deposited thereupon. The textured surface of the metal on a roughened transparent conductive oxide can act as a diffusive scattering site for the incident electromagnetic radiation.

In another specific aspect, a Bragg reflector can be utilized as a reflective region. A Bragg reflector is a structure formed from multiple layers of alternating materials with varying refractive indexes, or by a periodic variation of some characteristic (e.g. height) of a dielectric waveguide, resulting in periodic variation in the effective refractive index in the guide. Each layer boundary causes a partial reflection of an optical wave. For waves whose wavelength is close to four times the optical thickness of the layers, the many reflections combine with constructive interference, and the layers act as a high-quality reflector. Thus the coherent super-positioning of reflected and transmitted light from multiple interfaces in the structure interfere so as to provide the desired reflective, transmissive, and absorptive behavior. In one aspect, the Bragg reflector layers can be alternating layers of silicon dioxide and silicon. Because of the high refractive index difference between silicon and silicon dioxide, and the thickness of these layers, this structure can be fairly low loss even in regions where bulk silicon absorbs appreciably. Additionally, because of the large refractive index difference, the optical thickness of the entire layer set can be thinner, resulting in a broader-band behavior and fewer fabrications steps.

Additional scattering can be provided by positioning a textured forward scattering layer on the side of the device that receives incident electromagnetic radiation. These forward scattering layers can be, without limitation, textured oxides or polysilicon without a reflector.

In another aspect, as is shown in FIG. 4, a photosensitive semiconductor device 40 can also include a polysilicon layer 42 disposes between multiple dielectric layers 38. It should be noted that all reference numbers in FIG. 4 that have been reused from previous figures denote the same or similar materials and/or structures

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SAMSUNG EX. 1002 - 3920/4148

whether or not further description is provided. The addition of the polysilicon layer can provide various improvements in manufacturing in some cases. For example, a rough surface of a textured region can be challenging to wafer bond. By depositing a thin dielectric layer followed by a thick polysilicon layer it can be possible to create a surface that can be polished. Thus, the polysilicon layer can be planarized and polished until smooth, and the resulting surface can be wafer bonded to the dielectric layer on the opposing material, e.g. the semiconductor substrate if the polysilicon is deposited on the semiconductor layer structure. It is also contemplated that such a process can be performed with only one dielectric layer or even without any dielectric layers being present. In another aspect, the polysilicon layer can be doped with a dopant. In yet another aspect, the polysilicon layer can be a monosilicon layer. In one specific aspect, the polysilicon layer is a monosilicon layer and the semiconductor layer is an epitaxial layer that has been etched from the backside to form the textured region.

In another aspect, as is shown in FIG. 5, a photodiode 50 having enhanced light detection performance is provided. The photodiode includes contacts 52 and a photodiode junction 54 formed on the semiconductor layer 34. In another aspect, as is shown in FIG. 6, a CMOS image sensor having improved light detection performance is provided. The CMOS image sensor includes photodiode junctions 64 and circuitry 62 formed on the semiconductor layer 34. It should be noted that all reference numbers in FIGs. 5 and 6 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. In this way, the textured region 36 can be introduced into fabrication process at the start of the flow, at a lower cost and lower technical risk approach. Because the textured region is buried within the semiconductor materials at an early stage in the flow, the textured region can be protected from contamination during the further fabrication of the device. Additionally, potentially proprietary details such as the specific architecture of the texture region can be protected from view during the later stages of fabrication. This method could further include a step of removing the semiconductor substrate. It is understood that once the semiconductor device is formed the semiconductor substrate may no longer be necessary in some cases. In this way the semiconductor device can be mounted on various substrates as necessary for specific applications.

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SAMSUNG EX. 1002 - 3921/4148

In one aspect, isolation features can be utilized in order to isolate various portions of the device from one another. For example, in one aspect a semiconductor device can include a plurality of isolation features in at least the semiconductor layer that function to isolate each photodetector in an array of photodetectors from one another. The isolation features isolate each photodetector electrically, optically, or both electrically and optically. Isolation features can thus maintain uniformity across an array by reducing optical and electrical crosstalk between the photodetectors. FIG. 7 shows a semiconductor device 70 having an array of photodetectors 72. It should be noted that all reference numbers in FIG. 7 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. The photodetectors are separated by a plurality of isolation features, in this case extending through the semiconductor layer 34 and the textured region 36. In one aspect, the isolation features extend through the semiconductor layer but not through the textured region. In another aspect, the isolation features extend beyond the textured region and into the dielectric layer or even into the semiconductor substrate. In some aspects, other structures such as polysilicon layers and reflective regions can contain isolation features. Accordingly, the isolation features can be deep or shallow, depending on the desired configuration of the device.

Isolation features can be made from various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, voids, and the like, including combinations thereof. Conductive materials used to fill the isolation feature etches or voids can be passivated in order to maintain electrical isolation. In other aspects, conductive materials can be utilized as vias. The isolation can be fabricated at the substrate level prior to fabrication of circuitry, the detector device, or the imaging array. In one aspect, voids can be created and either left as voids or filled with such materials to form the isolation features. For example, a layer surface can be photolithographically patterned and vertically etched to a desired depth (e.g. from the device surface of the semiconductor layer to the dielectric layer). Dielectric material can then be deposited conformally on surfaces within the etch until filled with the dielectric or other material. Any dielectric material remaining on the device surface of the semiconductor layer can be removed by chemical etching and/or mechanical polishing. As has been described, the isolation feature does not need to fully bisect the semiconductor structure, but

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SAMSUNG EX. 1002 - 3922/4148

rather only a portion can be isolated; this is known as shallow trench isolation as opposed to deep trench isolation.

Additionally, isolation features regions can be configured to reflect incident electromagnetic radiation until it is absorbed, thereby increase the effective absorption length of the device. In other aspects, the sides of isolation features can be doped. In some aspects, a doped isolation feature can form an electrical surface field, similar to an electrical back surface field as has been described. The isolation features can be formed before or after bonding of the semiconductor substrate to the semiconductor layer. Furthermore, the isolation features can be formed from either side of the semiconductor layer or from either side of the semiconductor substrate, depending on the depth and extent of the features.

In some aspects, the textured region can be arranged in a discontinuous pattern. As is shown in FIG. 8, for example, a semiconductor device 80 can have a discontinuous textured region 82. It should be noted that all reference numbers in FIG. 8 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. Such a discontinuous pattern may correspond to structures elsewhere in the device, such as the spatial pattern of an array of photodetectors on the device surface (not shown).

In other aspects, one or more cavities can be disposed in the semiconductor device and associated with the textured region or regions. As is shown in FIG. 9, for example, a semiconductor device 90 can include a cavity region 92 associated with the textured region 36. The cavity region can enhance the functionality of the textured region, and can be particularly effective when optically coupled to a reflective region, whether the reflective region is on the near side or the far side of the dielectric layer 38. FIG. 10 shows a semiconductor device 100 having a plurality of cavity regions 102 arranged in a discontinuous pattern to correspond with the discontinuous pattern of the textured region 82. The cavity regions shown in FIGs. 9 and 10 can be formed prior to wafer bonding or following wafer bonding. If a cavity region is formed following wafer bonding, etching through the semiconductor substrate 32 may be required, following which the etch cavity can be partially filled. Additionally, a cavity region can be formed before or after formation of the textured region. In those aspects whereby a cavity region is formed after formation of the textured region, the intervening material would be etched until reaching the textured region. In those aspects whereby a cavity region is formed prior to formation of the

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SAMSUNG EX. 1002 - 3923/4148

textured region, an etch can be formed into the semiconductor layer 34 and the textured region can be formed thereon through the etch cavity. The formation of the textured region in this manner can be accomplished prior to wafer bonding or following wafer bonding by etching through the semiconductor substrate. It should be noted that all reference numbers in FIGs. 9 and 10 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided.

The present disclosure additionally provides various methods. In one aspect, as is shown in FIG. 14, for example, a method of making a semiconductor device can include texturing at least a portion of a surface of a semiconductor layer to form a textured region 142, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer 144, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate 146. In another aspect, the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

In another aspect, a method of making a semiconductor device can include laser texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

In yet another aspect, a method of making a semiconductor device can include wet etch texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

In one specific aspect, FIGs. 11A-C show one method of manufacturing a semiconductor device. As is shown in FIG. 11A, a semiconductor material 114 can be textured to create a textured region 112, and a dielectric layer 115 can be deposited over the textured region. In one aspect, the textured region can be formed by laser processing the semiconductor material. In another aspect, the textured region can be formed by wet etching the semiconductor material. The dielectric layer can then be

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SAMSUNG EX. 1002 - 3924/4148

polished until smooth with a process such as CMP processing. The resulting structure can then be wafer bonded to a semiconductor substrate 116, as is shown rotated 180° in FIG. 11B, with the polished surface of the dielectric layer being bonded to the semiconductor substrate. The dielectric layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer formed on the semiconductor substrate (not shown). After wafer bonding, the semiconductor material can be polished to a specified thickness. In another aspect, an epitaxially grown semiconductor layer 118 can be grown on the polished surface of the semiconductor material to generate a low defect device region as shown in FIG. 11C.

In another aspect, FIGs. 12A-C show another method of manufacturing a semiconductor device. As is shown in FIG. 12A, a semiconductor material 124 can be textured to create a textured region 122, and a dielectric layer 125 can be deposited over the textured region. In one aspect, the semiconductor material can be an epitaxially grown semiconductor material. The dielectric layer can then be polished and a polysilicon layer 126 can be deposited thereupon, as is shown in FIG. 12B. In an alternative aspect, the polysilicon layer can be formed directly on the textured region without an intervening dielectric layer (not shown). The polysilicon layer can then be polished and wafer bonded to a semiconductor substrate 126, as is shown rotated 180° in FIG. 12C. The polysilicon layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer 129 formed on the semiconductor substrate. After wafer bonding, the semiconductor material can be polished to a specified thickness.

In another aspect, FIGs. 13A-D show another method of manufacturing a semiconductor device. As is shown in FIG. 13A, a semiconductor layer 134 can be epitaxially grown on a temporary semiconductor support 139. The epitaxially grown semiconductor layer is textured to create a textured region 132, and a dielectric layer 135 is deposited over the textured region as is shown in FIG. 13B. Following polishing, the dielectric layer is wafer bonded to a semiconductor substrate 136, as is shown rotated 180° in FIG. 13C. The dielectric layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer formed on the semiconductor substrate (not shown). The temporary semiconductor support can then be removed from the epitaxially grown semiconductor layer. This can be accomplished by any known process, such as wafer splitting, CMP processing, etc. The exposed epitaxial semiconductor layer can be further polished and thinned to produce a desired surface

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SAMSUNG EX. 1002 - 3925/4148

for further device deposition. In this manner semiconductor materials used to grow the epitaxial layer can be removed, leaving a higher quality surface with fewer crystal defects and dislocations.

Of course, it is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present disclosure. Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the present disclosure and the appended claims are intended to cover such modifications and arrangements. Thus, while the present disclosure has been described above with particularity and detail in connection with what is presently deemed to be the most practical embodiments of the disclosure, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

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SAMSUNG EX. 1002 - 3926/4148

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate;

a semiconductor layer coupled to the semiconductor substrate, the semiconductor layer having a device surface opposite the semiconductor substrate; and

at least one textured region coupled between the semiconductor substrate and the semiconductor layer.

2. The device of claim 1, further comprising at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer.

3. The device of claim 2, wherein the semiconductor layer is an epitaxially grown semiconductor layer.

4. The device of claim 2, wherein the semiconductor layer is a silicon layer.

5. The device of claim 2, further comprising a secondary semiconductor layer disposed between the textured region and the semiconductor layer.

6. The device of claim 2, wherein the dielectric layer is coupled between the semiconductor substrate and the textured region, and wherein the textured region is disposed between the dielectric layer and the semiconductor layer.

7. The device of claim 6, further comprising a reflective region disposed between the semiconductor substrate and the textured region.

8. The device of claim 6, wherein the textured region is coupled directly to the semiconductor layer.

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SAMSUNG EX. 1002 - 3927/4148

9. The device of claim 6, further comprising a secondary semiconductor layer disposed between the textured region and the semiconductor layer.

10. The device of claim 6, further comprising at least one cavity region disposed between the textured region and the dielectric layer.

11. The device of claim 2, further comprising a polysilicon layer directly coupled to the dielectric layer.

12. The device of claim 11, wherein the polysilicon layer is disposed between multiple dielectric layers.

13. The device of claim 2, wherein the textured region is disposed between the semiconductor substrate and the dielectric layer, and wherein the dielectric layer is disposed between the textured region and the semiconductor layer.

14. The device of claim 2, wherein the textured region is doped with a dopant to form an electrical back surface field.

15. The device of claim 14, wherein the electrical back surface field has been doped by a technique selected from the group consisting of laser doping, ion implanting, diffusion doping, in situ doping, and combinations thereof.

16. The device of claim 15, wherein the textured region has a higher dopant concentration than the semiconductor layer.

17. The device of claim 15, wherein the dopant has the same polarity as the semiconductor layer.

18. The device of claim 15, wherein the dopant is a member selected from the group consisting of boron, indium, gallium, arsenic, antimony, phosphorus, and combinations thereof.

SAMSUNG EX. 1002 - 3928/4148

19. The device of claim 2, wherein the semiconductor layer is doped with a dopant to form an electrical back surface field, and wherein the electrical back surface field is distinct from the textured region.

20. The device of claim 2, further comprising at least one photodiode optically active region disposed on the device surface.

21. The device of claim 2, wherein the photodiode optically active region comprises a doped region.

22. The device of claim 2, wherein the device forms at least one photodetector.

23. The device of claim 22, wherein the at least one photodetector is a plurality of photodetectors arranged in an array.

24. The device of claim 23, wherein the textured region is arranged in a discontinuous pattern that corresponds spatially to the array of photodetectors.

25. The device of claim 23, further comprising a plurality of isolation features in at least the semiconductor layer to isolate each photodetector in the array of photodetectors, wherein the isolation features isolate each photodetector electrically, optically, or both electrically and optically.

26. The device of claim 23, further comprising at least one optical lens associated with the at least one photodetector.

27. The device of claim 23, further comprising at least one color filter associated with the at least one photodetector.

28. A method of making a semiconductor device, comprising:

texturing at least a portion of a surface of a semiconductor layer to form a textured region;

depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric

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SAMSUNG EX. 1002 - 3929/4148

layer; and

wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

29. The method of claim 28, wherein the semiconductor layer is an epitaxially grown semiconductor layer.

30. The method of claim 29, wherein texturing at least a portion of a surface of a semiconductor layer to form a textured region further includes:

forming the epitaxially grown semiconductor layer on a growth substrate; and

texturing at least a portion of a surface of the epitaxially grown semiconductor layer to form a textured region.

31. The method of claim 30, further comprising removing the growth substrate to expose the epitaxially grown semiconductor layer.

32. The method of claim 28, further comprising forming an epitaxially grown semiconductor layer on the semiconductor layer on an opposite side from the textured region.

33. The method of claim 28, wherein wafer bonding further includes:

depositing a polysilicon layer on the first dielectric layer; and

bonding the polysilicon layer between the first dielectric layer and the second dielectric layer.

34. The method of claim 33, further comprising doping at least a portion of the polysilicon layer.

35. The method of claim 28, wherein texturing at least a portion of a surface of the semiconductor layer to form the textured region further includes:

forming an opening in the semiconductor substrate, the second dielectric layer, and the first dielectric layer to expose a portion of the semiconductor layer; and

texturing at least a portion of the exposed portion of the semiconductor layer to form the textured region.

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SAMSUNG EX. 1002 - 3930/4148

36. The method of claim 28, wherein texturing includes a technique selected from the group consisting of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

37. The method of claim 28, wherein texturing includes lasing.

38. A method of protecting a textured region from contamination during manufacture of a semiconductor device, comprising:

texturing at least a portion of a surface of a semiconductor layer to form a textured region;

depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the dielectric layer; and

wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate, wherein the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

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SAMSUNG EX. 1002 - 3931/4148

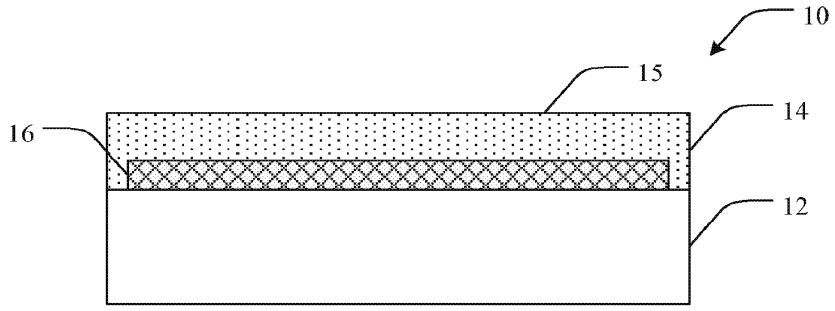


FIG. 1

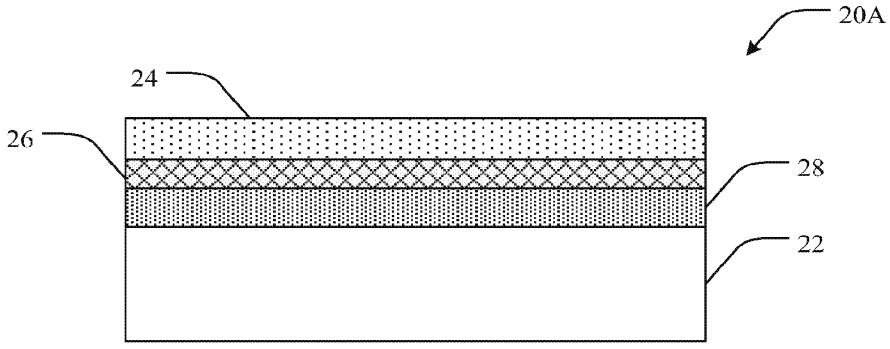


FIG. 2A

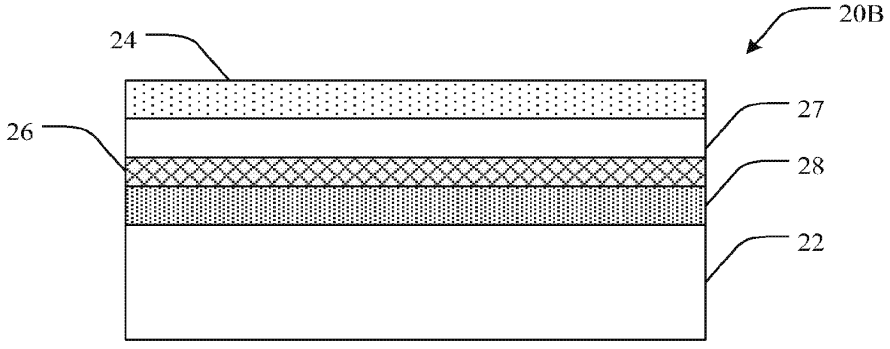


FIG. 2B

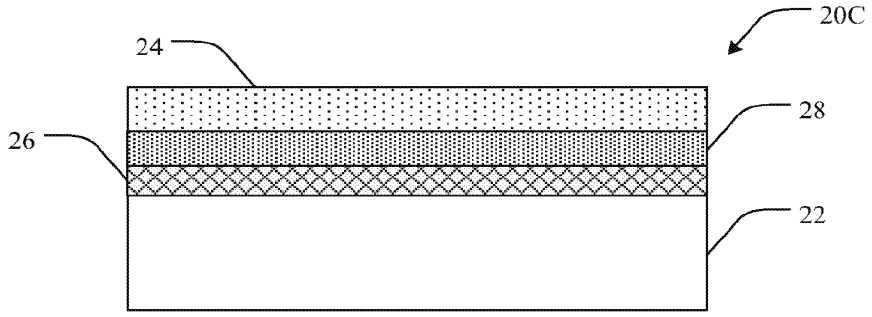


FIG. 2C

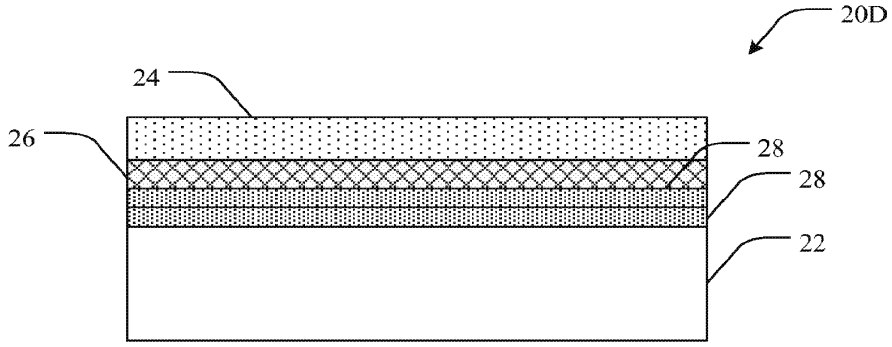


FIG. 2D

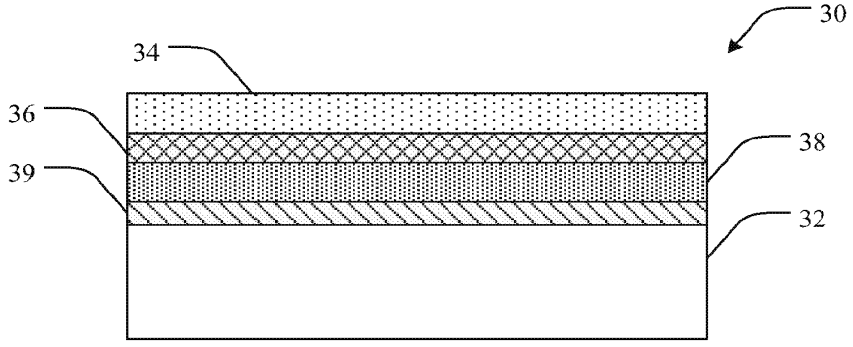


FIG. 3

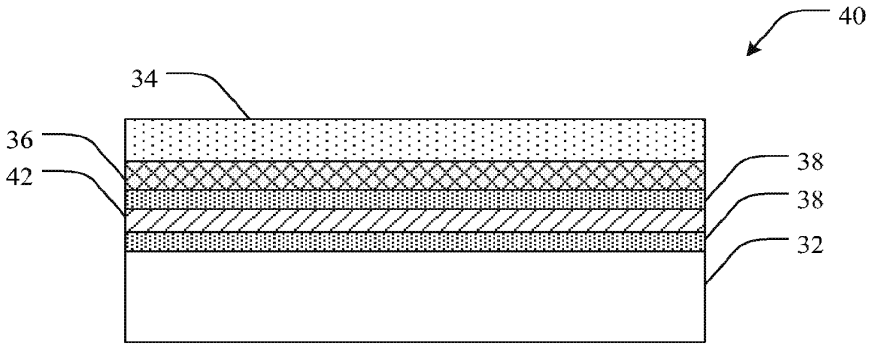


FIG. 4

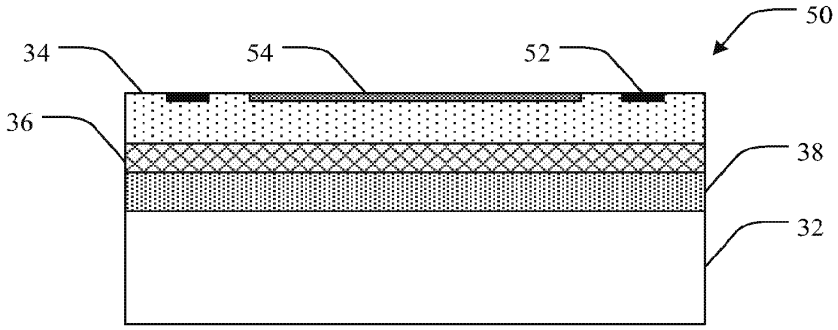


FIG. 5

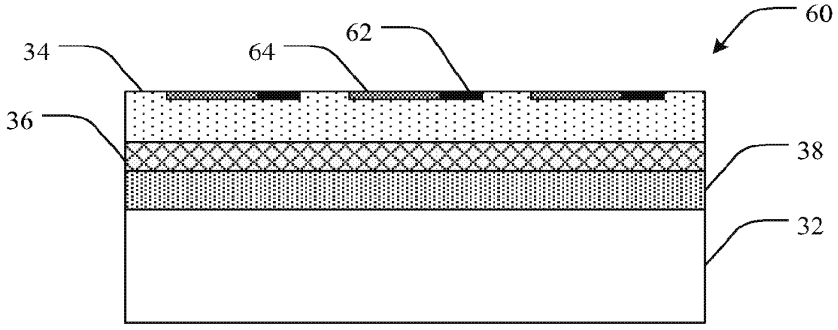


FIG. 6

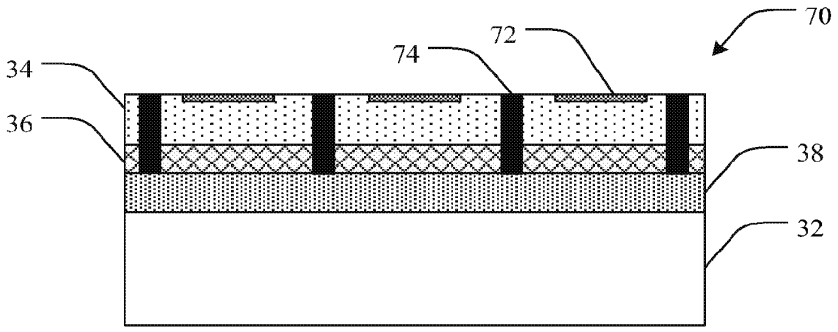


FIG. 7

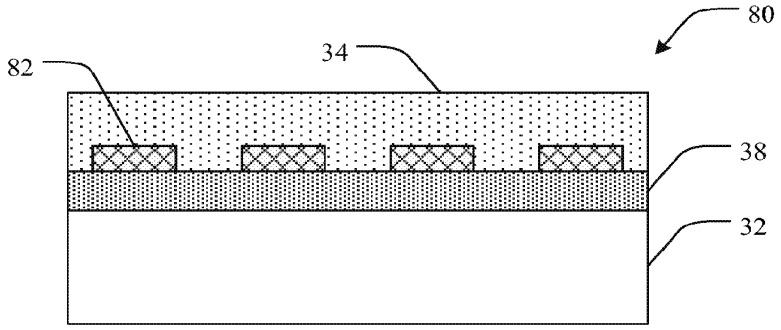


FIG. 8

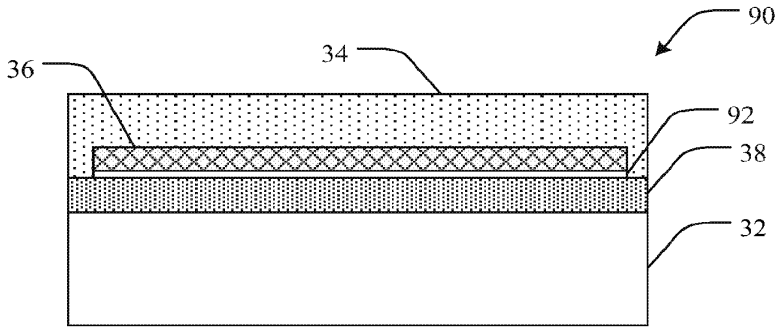


FIG. 9

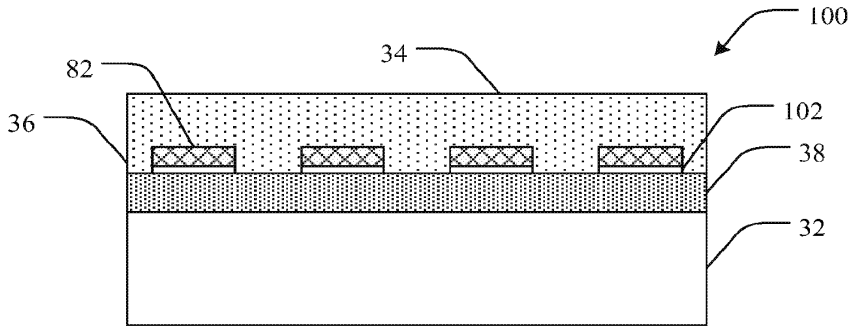


FIG. 10

SAMSUNG EX. 1002 - 3936/4148

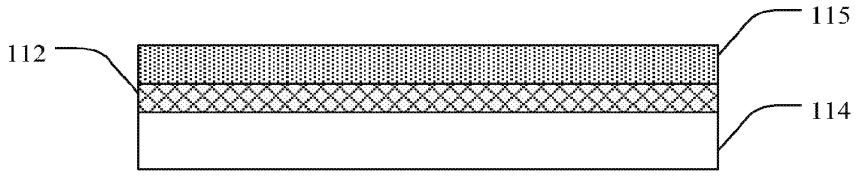


FIG. 11A

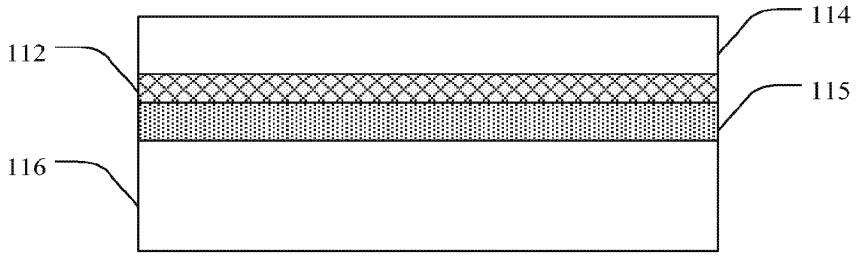


FIG. 11B

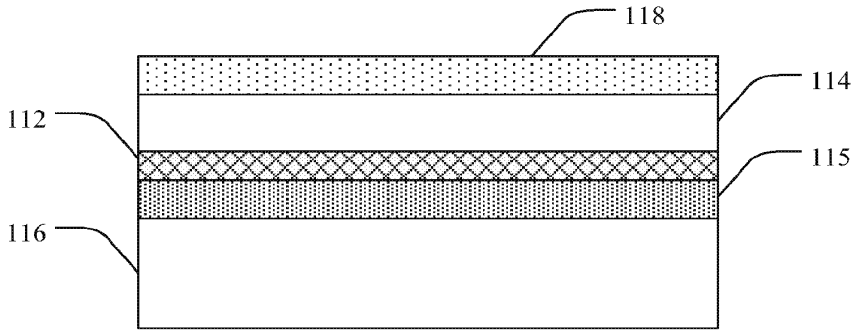


FIG. 11C

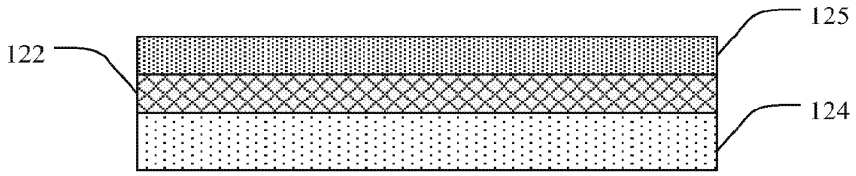


FIG. 12A

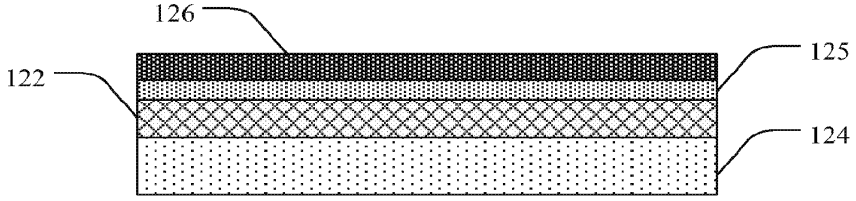


FIG. 12B

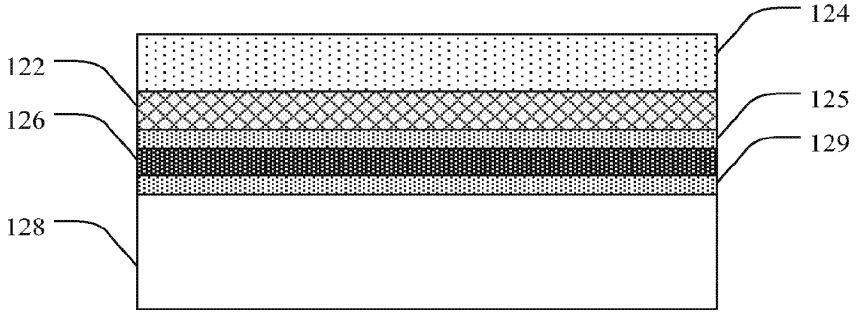


FIG. 12C

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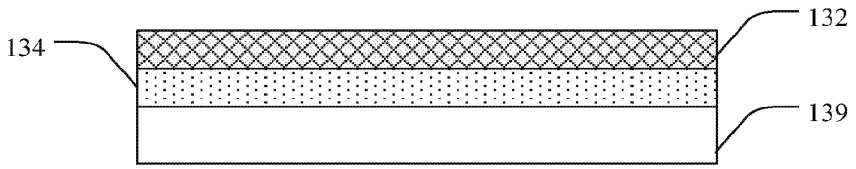


FIG. 13A

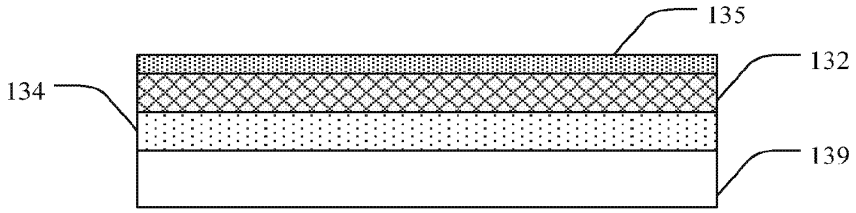


FIG. 13B

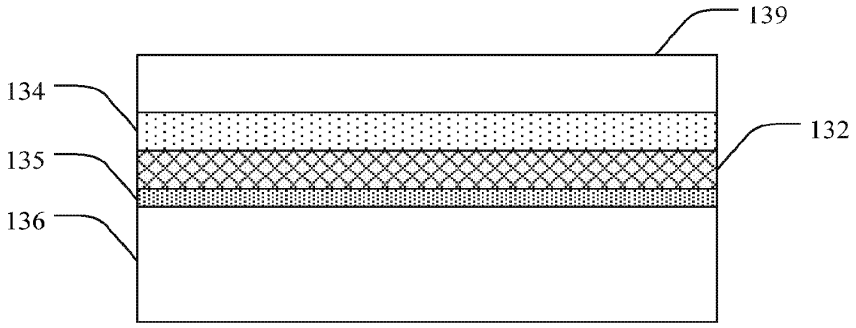


FIG. 13C

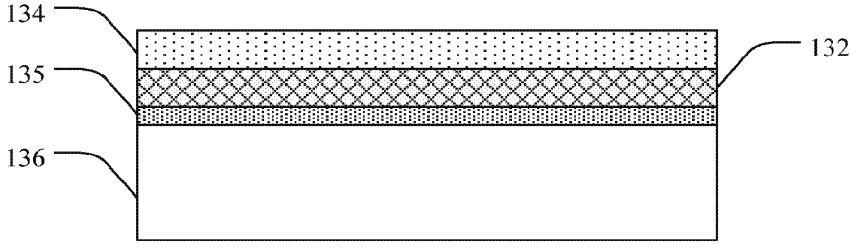


FIG. 13D

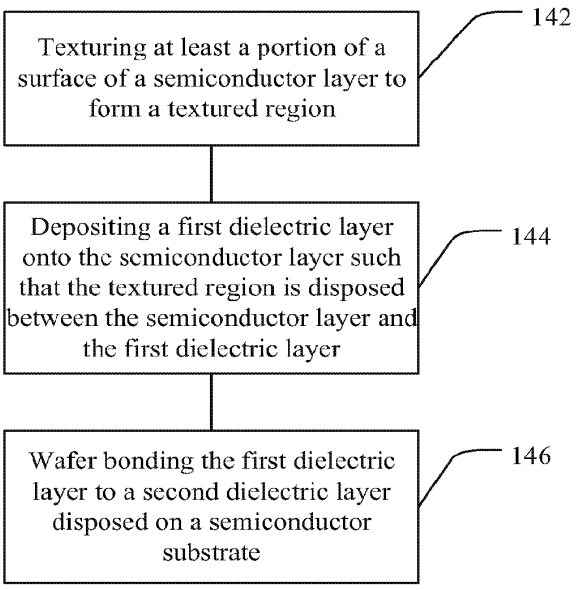

Texturing at least a portion of a surface of a semiconductor layer to form a textured region
142
Depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer
144
Wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate
146

FIG. 14

(12) 按照专利合作条约所公布的国际申请

(19) 世界知识产权组织
国 际 局

(43) 国际公布日
2012 年 12 月 27 日 (27.12.2012)

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(25) 申请语言: 中文

(26) 公布语言: 中文

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(72) 发明人; 及

(75) 发明人/申请人 (仅对美国): **胡笑平 (HU, Xiaoping)** [US/CN]; 中国广东省深圳市南山区蛇口沿山路以西、工业六路以北佳利泰大厦三楼 AC 单元、九楼 ABCDE 单元, Guangdong 518067 (CN)。

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(81) 指定国 (除另有指明，要求每一种可提供的国家保护): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW。

(84) 指定国 (除另有指明，要求每一种可提供的地区保护): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), 欧亚 (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), 欧洲 (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)。

本国际公布:

— 包括国际检索报告(条约第 21 条(3))。

(54) Title: MULTI SCENE DEPTH PHOTO SENSITIVE DEVICE, SYSTEM THEREOF, SCENE DEPTH EXPANDING METHOD, AND OPTICAL IMAGING SYSTEM

(54) 发明名称 : 多景深感光器件、系统、景深扩展方法及光学成像系统

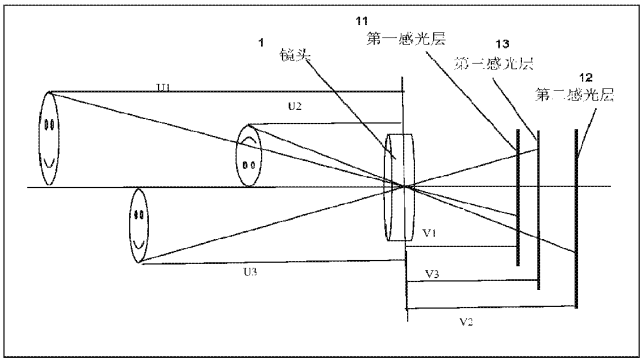


图 13 / FIG. 13

1 LENS
11 THE FIRST PHOTOSENSITIVE LAYER
12 THE SECOND PHOTOSENSITIVE LAYER
13 THE THIRD PHOTOSENSITIVE LAYER

(57) Abstract: A multi scene depth photo sensitive device, system thereof, scene depth expanding method and an optical imaging system are provide. The multi scene depth photo sensitive device comprises at least two photo sensitive pixel layers which can sense a light source, and the at least two photo sensitive pixel layers are disposed at a predetermined distance so that the different optical signals from the lens disposed at a a certain distance from the photo sensitive device can be focused on the different photo sensitive pixel layers. It is possible to realize focus automatically while avoiding utilizing electrodynamic element and mechanical element.

(57) 摘要: 提供一种多景深感光器件、系统、景深扩展方法及光学成像系统。多景深感光器件包括至少两个可感应到光源的感光象素层，至少两个感光象素层之间按预定的距离间隔设置，使来自距离感光器件特定距离的镜头的不同光信号被聚焦到不同的感光象素层。可以避免使用电动机构和机械部件而实现自动对焦。

WO 2012/174752 A1

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SAMSUNG EX. 1002 - 3941/4148

说 明 书

多景深感光器件、系统、景深扩展方法及光学成像系统

技术领域

本发明涉及感光领域，具体的说，涉及一种多景深感光器件、利用该多景深感光器件的感光系统、景深扩展方法以及一种光学成像系统与方法。

背景技术

本发明是本发明人稍早一点的《多光谱感光器件及其制作方法》（PCT/CN2007/071262），《多光谱感光器件及其制作方法》（中国申请号：200810217270.2），《多光谱感光器件》（中国申请号：200910105372.X），《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2），《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）的延续，旨在提供更为具体而且优选的多光谱感光器件在芯片及系统级别的实现。

感光系统，是一种通过光学镜头进行景物的捕捉、收集，并由感光器件，例如CMOS感光芯片进行景物的记录的系统。感光系统工作时，调节镜头，使距离镜头一定距离的景物清晰成像的过程，叫做对焦，该景物所在的点，称为对焦点，因为“清晰”具有相对性，所以对焦点前（靠近镜头）、后一定距离内的景物的成像都可以是清晰的，这个前后范围的总和称为景深。通常前景深小于后景深，即精确对焦后，对焦点前只有很短一段距离内的景物能清晰成像，而对焦点后很长一段距离内的景物都是清晰的。

获得宽景深清晰成像的系统是人们长期以来的研究目标之一。研究表明，景深的大小与镜头焦距有关，焦距长的镜头景深小，焦距短的镜头景深大。可见，镜头焦距调整是获得宽景深清晰成像的手段之一；另外，根据几何光学的基本成像公式（$\frac{1}{f}=\frac{1}{u}+\frac{1}{v}$，其中，f为镜头焦距，u为物距，即被摄物到镜头的距离，v为象距，即镜头到感光器件的距离），可见，象距的动态调整也是获得宽景深清晰成像的手段之一。

因此，现有感光系统中的自动对焦方式，都采用上述两种手段之一。例如，镜头由一组镜片构成，通过调整镜片之间的距离，从而可以调整镜头焦距或（镜头与感光器件的）象距（而实现光学变焦或对焦）；或者通过驱

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SAMSUNG EX. 1002 - 3942/4148

动例如 CMOS 感光器件位移，从而改变象距（而实现光学对焦）。然而，显然的，这两种方式的对焦，都需要电动机构和复杂、精密的机械部件来进行镜片或感光器件的位移驱动。这样，不仅显著增加了尺寸，也显著增加了成本和功耗。在很多的应用里，如手机照相和医用照相里，这些都是明显的不利因素。

一些不采用运动机构的宽景深系统因此被提出，试图在某些应用里取代自动对焦的需求。这种系统在手机照相的应用里，被称之为 EDoF (Extended Depth of Focus)，例如，DXO 公司提出的一种 EDoF 系统，通过特别的镜头设计，让感光器件中的红色感光象素聚焦在无穷远处，兰色感光象素聚焦在尽可能的近距(例如 50cm) 。而绿色感光象素聚焦在某个中间的位置。这样，无论物体处于哪个位置，总有一个颜色的图像是清楚或相对比较清楚的。之后，通过数学的手段，以比较清楚的颜色为主体，不够清楚的颜色为辅助信息，就能在比较宽的范围，还原和计算出较清楚的图像。

然而，采用单层感光器件，当红色感光象素聚焦在无穷远时，兰色感光象素的聚焦距离一般很难做得比 50cm 更小。此外，对于采用贝叶图案的感光器件，红色象素和兰色象素都只占感光象素的 1/4。因此，当需要以红色或兰色作为清晰度计算的主体时，图像的分辨率已经减少到以绿色为主体时的分辨率的一半以下。可见，这种方案有一定的局限性。

因此，仍然有必要对现有感光器件或系统进行改进。

发明内容

本发明所要解决的技术问题是，提供一种多景深感光器件、利用该多景深感光器件的感光系统、景深扩展方法以及一种光学成像系统与方法，其以物理的手段实现了自动对焦或多距离成像，避免使用电动机构和复杂、精密的机械部件，具有良好的景深扩展性能。

为解决上述技术问题，本发明采用了以下技术方案：

一种多景深感光器件，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

在本发明的一种实施例中，所述感光象素层包括化学镀膜感光象素层和半导体感光象素层中的至少一者。

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SAMSUNG EX. 1002 - 3943/4148

在本发明的一种实施例中，所述化学镀膜感光象素层包括量子点感光象素。

在本发明的一种实施例中，所述半导体感光象素层包括 CMOS 光敏二极管、CMOS 感光门、CCD 光敏二极管、CCD 感光门、和具有双向电荷转移功能的 CMOS 和 CCD 感光二极管和感光门。

在本发明的一种实施例中，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

在本发明的一种实施例中，波长更短的光信号被聚焦到离镜头更近的感光象素层。

在本发明的一种实施例中，所述感光象素层为两层，紫色光、兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

在本发明的一种实施例中，所述感光象素层为三层，紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层；兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层；红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层。

在本发明的一种实施例中，更远距离的光信号被聚焦到离镜头更近的感光象素层。

在本发明的一种实施例中，所述感光象素层为两层，无穷远处的光信号被聚焦到离镜头较近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头较远的感光象素层。

在本发明的一种实施例中，无穷远处的紫色光、兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，感兴趣最短距离的绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

在本发明的一种实施例中，所述感光象素层为三层，无穷远处的光信号被聚焦到离镜头最近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的光信号被聚焦到位于中间的感光象素层。

在本发明的一种实施例中，所述感光象素层为三层，无穷远处的紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层，感兴趣最短距离的红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层。

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在本发明的一种实施例中，所述感兴趣最短距离包括 2mm，5mm，7mm，1cm，2cm，3cm，5cm，7cm，10cm，20cm，30cm，40cm，50cm，60cm，70cm，80cm，100cm，或 150cm。

在本发明的一种实施例中，至少两个所述感光象素层之间设置有透光层。

在本发明的一种实施例中，所述感光象素层中的感光象素为正面感光象素、背面感光象素、或双向感光象素。

在本发明的一种实施例中，当感光象素为双向感光象素时，其感光选向方式为隔离选向、分时选向、分区选向、或象素选向。

在本发明的一种实施例中，所述感光象素层中的感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个互补谱段或子谱段；或者所述化学镀膜感光象素和半导体感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个正交谱段或子谱段。

在本发明的一种实施例中，所述互补谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱；

所述正交谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱。

在本发明的一种实施例中，每一感光象素层中的色彩排列包括同一排列、水平排列、垂直排列、对角排列、广义贝叶排列、YUV422 排列、横向 YUV422 排列、蜂窝排列、均布排列。

在本发明的一种实施例中，至少一个所述感光象素层中的部分或全部感光象素的正面、背面或双面设置有滤光膜，所述滤光膜的选频特性包括红外截止滤波、兰色带通、绿色带通、红色带通、青色带通、黄色带通、品红色带通、或可见光带通。

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在本发明的一种实施例中，所述感光象素层中的相邻两层各自设有读取电路；或者所述感光象素层的相邻两层共用读取电路。

在本发明的一种实施例中，所述读取电路为主动象素读取电路、被动象素读取电路、或主动象素与被动象素混合读取电路。

在本发明的一种实施例中，所述主动象素包括 3T、4T、5T 或 6T 主动象素。

在本发明的一种实施例中，所述读取电路的共用方式包括单层或上下层 4 点共享方式、单层或上下层 6 点共享方式、单层或上下层 8 点共享方式、或单层或上下层任意点共享方式。

在本发明的一种实施例中，所述读取电路包括用于对每一感光象素层的象素阵列中的紧邻的同行异列、异行同列、或异行异列的象素间进行两两合并采样，获得第一合并象素的采样数据的第一合并单元；以及用于对第一合并单元得到的第一合并象素的采样数据进行合并采样以获得第二合并象素的采样数据的第二合并单元。

在本发明的一种实施例中，所述读取电路还包括第三合并单元，用于对第二合并单元得到的第二合并象素的采样数据进行合并采样以获得第三合并象素的采样数据。

在本发明的一种实施例中，所述第一合并单元或第二合并单元的象素合并方式为相同或不同色彩象素间的电荷相加方式或信号平均方式，其中不同色彩象素间的象素合并方式遵照色彩空间变换的方式，以满足色彩重建的要求。

在本发明的一种实施例中，所述色彩空间变换包括 RGB 到 CyYeMgX 空间的变换、RGB 到 YUV 空间的变换、或 CyYeMgX 到 YUV 空间的变换，其中 X 为 R(红)、G(绿)、B(兰)中的任一种。

在本发明的一种实施例中，所述电荷相加方式通过象素直接并联或将电荷同时转移到读取电容（FD）中完成。

在本发明的一种实施例中，所述第一合并单元或第二合并单元的基于色彩的合并采样方式包括同色合并方式、异色合并方式、混杂合并方式、或选择性抛弃多余色彩合并方式，且第一合并单元和第二合并单元采用的合并采样方式不同时为同色合并方式。

在本发明的一种实施例中，所述第一合并单元或第二合并单元的基于位置的合并采样方式包括以下几种方式中的至少一种：直接输出到总线的信号自动平均方式、跳行或跳列方式、和逐个采样方式。

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在本发明的一种实施例中，所述第三合并单元的合并采样方式包括：色彩空间变换方式和后端数字图像缩放方式中的至少一种。

在本发明的一种实施例中，包括具有跨层读取功能的全局电子快门，所述全局电子快门包含多个可同时转移并读取一层或多层感光象素层的电荷或电压值的不感光的转移和读取象素。

在本发明的一种实施例中，所述多个不感光的转移和读取象素位于不感光象素转移和读取层；或者位于所述感光象素层。

在本发明的一种实施例中，每一感光象素层，设置有一个紧邻的不感光象素转移和读取层。

在本发明的一种实施例中，所述不感光的转移和读取象素由半导体电路制成。

本发明也提供了一种景深扩展方法，包括：

在感光器件中设置至少两个可感应到光源的感光象素层，并将至少两个所述感光象素层按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

在本发明的一种实施例中，通过来自不同感光象素层的具有不同清晰度的图像而获取一幅清晰图像。

本发明还提供了一种光学成像方法，包括：

设置镜头和包括至少两个可感应到光源的感光象素层的感光器件；将所述感光器件放置在距所述镜头特定距离，且至少两个所述感光象素层之间按预设距离间隔布置，使得来自镜头的不同光信号被聚焦到不同的所述感光象素层。

本发明还提供了一种光学成像系统，包括镜头和多景深感光器件，所述多景深感光器件布置在距所述镜头特定距离，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自所述镜头的不同光信号被聚焦到不同的所述感光象素层。

在本发明的一种实施例中，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

在本发明的一种实施例中，波长更短的光信号被聚焦到离镜头更近的感光象素层。

在本发明的一种实施例中，更远距离的光信号被聚焦到离镜头更近的感光象素层。

本发明还提供了一种感光系统，包括上述的感光器件。

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在本发明的一种实施例中，所述感光系统包括数码相机，照相手机，摄像机，视频或照相监控系统，图像识别系统，医学图像系统，军用、消防或井下图像系统，自动跟踪系统，立体影像系统，机器视觉系统，汽车视觉或辅助驾驶系统，电子游戏系统，网络摄像头，红外和夜视系统，多光谱成像系统，和电脑摄像头中的一种。

现有的感光系统，不仅自动对焦系统需要电动机构和复杂、精密的机械部件，而且对于 6mm 直径以上的镜头而言，为了实现在 10cm 至无穷远的宽距自动对焦，镜头的行程必须在 0.2mm 以上，也就是说，无穷远处清晰成像的象距与 10cm 处清晰成像的象距差，至少是 0.2mm，即 200um。众所周知，硅或其它半导体材料都是不透明的。光进入硅后，大约在 12um 处，就已经被吸收得所剩无几了。因此即使使用自动对焦系统，现有的感光系统也很难获得较宽的景深范围。

本发明的多景深感光器件、利用该多景深感光器件的感光系统、景深扩展方法，以及光学成像系统及方法，通过设置至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距感光器件特定距离的镜头的不同光信号被聚焦到不同的感光象素层，从而不同感光象素层可以得到不同景深的图像。从产品角度，感光器件可以制作成感光芯片独立存在，但从应用角度，例如光学成像，感光器件通常需要与镜头配合使用。镜头，依其大小、材料、曲面设计等具有不同的聚焦特性，例如以普通的手机镜头为例，其景深范围通常是无穷远到 2m，超出该景深范围，则需要采用自动对焦技术，例如通过调整感光器件到镜头的距离，也即调整象距到某一合适数据，才能获得例如 50cm-30cm 的清晰景象。而在本发明中，如果选定的应用镜头是手机镜头，则可以按下例在感光器件中设置两个感光象素层（称第一感光象素层和第二感光象素层），当与该选定的手机镜头配合时，感光器件被放置在距该镜头特定距离，此时，第一感光象素层到镜头的距离为第一象距，第二感光象素层到镜头的距离为第二象距（第一象距小于第二象距），此时，距镜头的特定距离以及两个感光象素层之间的预设距离，使得从无穷远到 2m 的景深范围的景物将可在第一感光象素层清晰成像，从 50cm-30cm 的景深范围的景物将可在第二感光象素层清晰成像。由此，实现了两个景深或景深扩展。需要注意的是，上述说明例中，感光象素层的数量和景深范围均仅为示例性数据，可以理解，通过对感光象素层的数量和相互间的预设距离调整，可以形成连

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续、交叠、互补、或正交的景深范围，多个感光象素层各自的景深范围叠加将使感光器件具有相当宽的景深范围，从而无需自动对焦即可获得宽景深范围内的清晰图像，避免使用电动机构和复杂、精密的机械部件，显著的节约了空间和成本。另一方面，在本发明中，通常至少可以从一个感光象素层获得较为完整的图像信息，从而图像具有相当高的清晰度，且无需繁琐的数学计算。

本发明将通过实施例描述这种新型的、威力巨大的混合多光谱感光象素组、感光器件和系统。这些优选实现方式，仅仅是作为举例来说明本发明的优点和实现方法而已，而不是为了限制这些发明的保护范围。

对于相关业界的有识之士而言，本发明的上述及其它目的和优点，在阅读过下面的优选的带有多个插图解释的实现案例的细节描述之后，将是十分明显的。

附图说明

图 1 是一个光谱分布的示意图。可见光一般是指 390nm 到 760nm 波长的光。一般由棱镜的分光效应而从可见光分出来看到的兰光波长在 440 - 490nm，绿光波长在 520 - 570nm，红光波长在 630 - 740nm，而在感光器件的设计中，一般把 390 - 500nm 划为兰色区，500-610nm 划为绿色区，610-760nm 划为红色区，但这种红、绿、兰的谱段的划分并不是绝对的。图中的红、绿、兰、青（兰绿复合）、和黄（绿红复合）的波形，是原色感光象素或补色（复合色）感光象素所需求的理想的波长响应曲线。如果作为基色的原色感光象素或补色（复合色）感光象素不具备类似的波长响应曲线，则很难重建人类所能看到绝大部分色彩。

图 2 是感光象素的 3T 读取电路。

图 3 是感光象素的 4T 读取电路。

图 4 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）和《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）提出的四点共享读取电路。

图 5 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）和《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）提出的两层六点共享读取电路。

图 6 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：

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200910105948.2）和《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）提出的两层八点共享读取电路。

图 7 是本人在《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）提出的任意 N 点共享读取电路。

图 8 是本人在《多光谱感光器件及其制作方法》（中国申请号：200810217270.2）和《多光谱感光器件》（中国申请号：200910105372.X）中提出的，上下层感光象素在感兴趣的光谱上互补或正交的双层感光器件的示意图。这种感光器件通过采用精心选择的彩色图案和排列，可以得到非常多优秀的双层感光器件。这些感光器件可以用于正面感光，背面感光，和双向感光。这些方法和原理，同样也可适用于本发明的多光谱感光器件。

图 9 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）中提出的一种在不同色彩象素间实现电荷合并的子采样方法。这种方法同样适用于本发明的多光谱感光器件。

图 10 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）中提出的采用色彩空间变换来实现的一种象素合并和子采样方法。这种方法同样适用于本发明的多光谱感光器件。

图 11 是本发明提出的一种用于景深扩展的两层感光器件的结构示意图，其中透光层的厚度，由所希望的两个感光平面的象距差（V2-V1）来决定。

图 12 是本发明提出的一种用于景深扩展的三层感光器件的结构示意图，其中透光层的厚度，由所希望的两个感光平面的象距差（V2-V1 或 V3-V2）来决定。

图 13 是第一种利用多层感光器件实现景深扩展的原理示意图。在这个示意图里，位于不同距离的物体，将清晰地聚焦在多层感光器件的不同感光象素层。因此，位于这三个距离之间的任一物体，都将清楚或者比较清楚地聚焦在一个，或者两个感光象素层，从而达到景深扩展的效果。图中，U1，U2，U3 是物距（即物体到镜头的距离），V1，V2，V3 是象距（即感光象素层到镜头的距离）。

图 14 是第二种同时利用特殊的镜头设计方法和多层感光器件来实现更好的景深扩展效果的原理示意图。对一般光学系统而言，波长更短的光，焦距更短。因此，对镜头进行特别的设计，可以让波长更短的光，聚焦在离镜头更近的感光象素层，或者说，离光源更近的感光象素层；而将波长更长

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的光，聚焦在离镜头更远的感光层，或者说，离光源更远的感光象素层；而将波长中等的光，聚焦在中间的感光层。这样，这种成像系统同时结合多光谱和多象距的特点，就能极大地扩展景深。这种系统，对于微距照相，有着无比的优势。

图 15 是实现图 11 所示的多景深感光器件的感光象素级别的原理示意图。通过调整透光层的厚度，可以调整两个感光象素层之间的距离，从而让两个感光象素层的感光象素，分别对应不同的景深。该例中，上下两个感光象素层均采用半导体感光象素层。

图 16（a）、（b）、（c）、（d）是实现图 11 所示的多景深感光器件的另一种感光象素级别的原理示意图。同样，通过调整透光层的厚度，可以调整两个感光象素层之间的距离，从而让两个感光象素层的感光象素，分别对应不同的景深。该例中，上层的感光象素层采用化学镀膜感光象素层，而下层的感光象素层采用半导体感光象素层，显然二者可以互换而不影响其实现多景深的效果。

图 15 和图 16 都只描绘了感光象素的情况，其它读取电路和辅助电路，因为可以与现有的相同，都被省略。

图 17（a）、（b）、（c）、（d）是实现图 11 所示的多景深感光器件的另一种感光象素级别的原理示意图。同样，通过调整透光层的厚度，可以调整上层的一个感光象素层与下层的另两个感光象素层之间的距离，从而让不同感光象素层的感光象素，分别对应不同的景深。在该例中，上层的一个感光象素层采用化学镀膜感光象素层，下层的另两个感光象素层采用半导体感光象素层，注意到，图 17（a）、（b）中的两个半导体感光象素层布置在一个半导体基层的两面，图 17（c）、（d）中的两个半导体感光象素层布置在一个半导体基层的一面。照射方向可以是该半导体基层的正面或是背面。另需注意的是，由于半导体的透光性限制，半导体基层厚度一般较薄，通常不满足景深扩展所需的感光象素层间隔距离的需求。因此，两个半导体感光象素层更多的用来实现多光谱的需求。

图 18（a）、（b）是实现图 11 所示的多景深感光器件的另一种感光象素级别的原理示意图。同样，通过调整透光层的厚度，可以调整上层的一个感光象素层与下层的另两个感光象素层之间的距离，从而让不同感光象素层的感光象素，分别对应不同的景深。在该例中，上层的一个感光象素层采用化学镀膜感光象素层，下层的另两个感光象素层分别采用半导体感

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光象素层和化学镀膜感光象素层。中间的半导体感光象素层（的两面）可以含有读取三个感光象素层所必需的读取象素和采样电路。

图 19（a）、（b）是实现图 12 所示的多景深感光器件的一种感光象素级别的原理示意图。注意到，在该例中，从上到下依次布置化学镀膜感光象素层、第一透光层、第一半导体感光象素层、第二透光层、第二半导体感光象素层。第一半导体感光象素层和第二半导体感光象素层分别实现在不同的两个半导体基层上，化学镀膜感光象素层与第一半导体感光象素层之间的距离通过调整第一透光层的厚度实现，第一半导体感光象素层与第二半导体感光象素层之间的距离通过调整第二透光层的厚度实现。读取和采样电路可以在位于中间的第一半导体感光象素层实现，也可以分布在两个半导体感光象素层。

对于具有两层半导体感光象素层的实施例，例如图 8 和图 15 等，如果将其中一个感光象素层中的感光象素去掉，做成专门用于读取电路和信号处理的层，则可以得到如图 20-23 所示的本发明提出的带有(具有跨层读取功能的)全局电子快门的感光器件。图 20-23 仅是展示了该带有(具有跨层读取功能的)全局电子快门的感光器件的感光象素层和不感光的转移和读取象素层，显然，结合前述，当保留定焦在不同景深的多个感光象素层时，则可以得到带有(具有跨层读取功能的)全局电子快门的多景深感光器件。

图 20 是本发明提出的两行共用一行转移象素（读取电容）的示意图。这实际上是《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7)中隔行扫描方式的一种新的实现。在这里，转移象素和感光象素不在同一层，因而可以获得更好的感光面积的使用效率，但同时增加了一倍的快门速度。重要的是，这种方式可以用于以化学感光材料(如量子感光膜)为感光象素层的感光器件。

图 21 是利用半导体的不良透光性能，将半导体基层厚度增加到一定厚度，使得下层的象素感不到光。然后，利用金属穿孔或是表面走线，外部连接的方式，将上层的感光象素信号，通过二极管或读取放大开关电路引到不感光象素层的读取象素上，在那里进行采样读取，从而将一个两层的感光器件退化成一个(具有跨层读取功能的)全局电子快门的单层感光器件。这个器件在结构上是双层的，但在效果上却是单层的。当这种方式用于图 17(a)所示的多层感光器件时，就能得到(具有跨层读取功能的)全局

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电子快门的多景深感光器件。

图 22 是本发明提出的以传统的(CMOS 和 CCD)半导体电路为基础的带有（具有跨层读取功能的）全局电子快门的多光谱两层感光器件的示意图。同样地，感光象素信号到不感光读取象素上的转移，由二极管或放大开关电路来控制的。

图 23 是本发明提出的另一种以化学感光材料(如量子感光膜)为基础的带有（具有跨层读取功能的）全局电子快门的多光谱两层感光器件的示意图，其中感光象素层采用化学感光材料(如量子感光膜)，而读取电路和信号处理层则是 CMOS 半导体层。注意到在该图示例中，每一个感光象素都对应有一个不感光的电荷转移象素，用于实现全局电子快门。这也是多层感光器件的为简单实现全局电子快门而特意进行的一种退化。

图 24 是本人在《一种感光器件及其读取方法、读取电路》(中国申请号：200910106477.7)提出的一种同时采用主动象素和被动象素来读取感光象素信号的读取电路。采用这种方法的好处是，能够极大地扩大感光器件的动态范围，并且成倍地节省图像预览时的功耗。这种混合读取电路在高灵敏度的多层多光谱感光器件和带有全局电子快门的多光谱感光器件里尤其有用。

图 25 是《一种多光谱感光器件及其采样方法》(中国申请号：200910105948.2）中用来描述该发明中提出的象素合并和子采样方法的采样控制电路示意图。本发明也将用到这种新型的象素合并和子采样方法。

具体实施方式

下面通过具体实施方式结合附图对本发明作进一步详细说明。

本发明将提出的多景深感光器件，其主要用途是景深扩展，即手机行业里目前所称的 EDoF(即 Extended Depth of Focus)。景深扩展尤其在照相手机中有着非常广泛的应用，然而，目前的景深扩展主要使用光学和数学手段，通常是利用光学变焦或自动对焦的方式实现景深调整，这要求电动机构和复杂、精密的机械部件的配合，因而将显著增加空间和成本。

本发明实施例所提出的多景深感光器件，结合多层感光器件的实现，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距感光器件特定距离的镜头的不同光信号被聚焦到不同的感光象素层，从而不同感光象素层构成了具有不同象距的

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感光平面，可以定焦不同的景深，由此扩展了感光器件的景深范围，相当于从多点光学对焦这一物理手段上实现了自动对焦，相应可以去除电动机构和复杂、精密的机械部件的配合，显著地节省了空间和成本。

所述感光象素层，包括化学镀膜感光象素层和半导体感光象素层中的至少一者。即上述至少两个感光象素层，可以全部是化学镀膜感光象素层，或者全部是半导体感光象素层，或者部分是化学镀膜感光象素层，部分是半导体感光象素层。其中，化学镀膜感光象素层包括量子点感光象素。半导体感光象素层包括 CMOS 光敏二极管、CMOS 感光门、CCD 光敏二极管、CCD 感光门、和具有双向电荷转移功能的 CMOS 和 CCD 感光二极管和感光门。

上述的感光象素层，分别用来感应不同的光信号。本发明中，关注的光信号特性主要包括光信号的频谱特性，即光的波长，以及光信号的距离特性，即光信号到镜头的距离。因此，光信号的不同，是指两个光信号之间，上述两个特性中至少有一者不同，即两个光信号之间，可能是波长不同，或者距离不同，或者波长和距离都不同。当然，由于自然界常见复色光，例如白光，因此如果需要得到不同波长的光，一般需要配合镜头设计，利用例如棱镜的分光效应，镜头材料或曲面设计对不同波长的光的不同折射率从而使不同波长的光分离并聚焦在不同的感光象素层上。

在聚焦不同波长的光信号的时候，一般地，波长更短的光信号被聚焦到离镜头更近的感光象素层。例如，感光象素层为两层，则聚焦在离镜头较近的感光象素层的光信号是紫色、兰色光、青色、或绿色光，聚焦在离镜头较远的感光象素层的光信号是绿色光、红色光、黄色光、可见光(白色光)、或红外光。又如，感光象素层为三层，则聚焦在离镜头最近的感光象素层的光信号是紫外光、兰色光、或青色光；聚焦在位于中间的感光象素层的光信号是绿色光、兰色光、黄色光、红色光、或可见光(白色光)；聚焦在离光源最远的感光象素层的光信号是红色光、黄色光、可见光、或红外光。

在聚焦不同距离的光信号的时候，一般地，更远距离的光信号被聚焦到离镜头更近的感光象素层。例如，感光象素层为两层，聚焦在离光源较近的感光象素层的是无穷远处的光信号，聚焦在离光源较远的感光象素层的是感兴趣最短距离的光信号。结合聚焦不同波长的光，还可以进一步设置为：无穷远处的紫外光、兰色光、青色光、或绿色光被聚焦到离光源较近的感光象素层；感兴趣最短距离的绿色光、红色光、黄色光、可见光(白

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色光)、或红外光被聚焦到离光源较远的感光象素层。

又如，感光象素层为三层，聚焦在离光源最近的感光象素层的是无穷远处的光信号，聚焦在离光源最远的感光象素层的是感兴趣最短距离的光信号，聚焦在位于中间的感光象素层的是无穷远处与感兴趣最短距离的一个中间距离的光信号。结合聚焦不同波长的光，还可以进一步设置为：无穷远处的紫外光、兰色光、青色光、或绿色光被聚焦到离光源最近的感光象素层；无穷远处与感兴趣最短距离的一个中间距离的绿色光、兰色光、黄色光、红色光、或可见光(白色光)被聚焦到位于中间的感光象素层；感兴趣最短距离的红色光、黄色光、可见光、或红外光被聚焦到离光源最远的感光象素层。

实施方式中，感兴趣最短距离包括 2mm，5mm，7mm，1cm，2cm，3cm，5cm，7cm，10cm，20cm，30cm，40cm，50cm，60cm，70cm，80cm，100cm，150cm。所谓感兴趣最短距离，是指用户关注的景物到镜头的最近距离。例如，感兴趣最短距离是 2mm，是指用户关注的景物到镜头的最近距离是 2mm，当景物到镜头的距离小于 2mm，则不再关注。

图 13 显示了距离与聚焦平面的关系。在该图中，位于不同距离的物体，将清晰地聚焦在多层感光器件的不同感光象素层。因此，位于这三个距离之间的任一物体，都将清楚或者比较清楚地聚焦在一个，或者两个感光象素层，从而从同一个感光器件，能够同时得到它们的清晰图像。

图 14 显示了波长与聚焦平面的关系，对一般光学系统而言，波长更短的光，焦距更短。因此，通过对镜头进行设计，可以让波长更短的光，聚焦在离镜头更近的感光象素层；波长更长的光，聚焦在离镜头更远的感光象素层；波长中等的光，聚焦在中间的感光象素层。这样，处于不同距离的物体，总有一个颜色，在一个感光层中是清楚的。于是，这种成像系统同时结合了多光谱和多象距的特点，每个感光层有自己的景深范围，并且对于不同波长的光，景深距离和范围不同，可以将各个感光层的景深范围进行整合，能够极大地扩展景深，对于微距照相，有着无比的优势。

由于可以从不同感光象素层得到具有不同清晰度的多个图像，因而这些图像之间可以相互参照，通过图像的整合、选用和舍弃，以及插值、增强、或反卷积等数学处理，而获得清晰的图像。

实施方式还包括在上述多景深感光器件中，实现一种具有跨层读取功能的全局电子快门，包括多个不感光的转移和读取象素，所述不感光的转移和

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读取象素的每一个能够用来转移和读取处在其它层的至少一个感光象素的电荷或电压值。从而多个不感光的转移和读取象素可同时转移并读取一层或多层感光象素层的电荷或电压值。多个不感光的转移和读取象素可以与感光象素位于同一象素层，显然，这意味着该象素层的感光灵敏度的下降。多个不感光的转移和读取象素也可以与感光象素位于不同的象素层，即形成独立的感光象素层和独立的不感光的转移和读取象素层，显然，这意味该具有跨层读取功能的全局电子快门只能在两层或多层感光器件中实现。

可以为每一个感光象素层设置一个紧邻的对应的不感光象素转移和读取层，所述不感光象素转移和读取层可同时转移对应的感光象素层的所有象素的电荷或电压值；或者可同时转移对应的感光象素层的奇数行或偶数行象素的电荷或电压值。图 20 显示了两行共用一行读取电容的设计，以实现逐行扫描的功能。不感光的转移和读取象素层，可以半导体电路做成。

图 21 显示了一种两层感光器件的退化实现，以获得单层的带有全局电子快门的单层感光器件。这种方法利用了半导体材料的不良透光性，将两半导体基层加厚，使得底层感不到光，而只能用于做象素读取。将这个方法用于图 17(a)所示的三层感光器件时，就能得到带全局电子快门的两层多景深感光器件。

图 22 和图 23 显示了一种具有跨层读取功能的全局电子快门的象素级别的实现。

文中出现的远近，上下等位置关系，均是指以光源为基准的相对位置。例如，上层感光象素层和下层感光象素层的描述，是指感光象素层水平放置，光源从上方垂直照射向感光象素层而言。显而易见，本文中的上下关系实际上具有更加广泛的含义，即，例如感光面垂直放置，光源从左侧或右侧，或者从前侧或后侧垂直照射向感光面，则所谓的上下关系，则等同于前后关系或者左右关系。不失一般性，本领域技术人员可以理解，其中的上方、下方等描述，可以用左侧、右侧、前侧、后侧等描述进行等同的替代。不同种类的感光象素层，如化学镀膜感光象素层或半导体感光象素层，其上下关系并无限制，何者处于上方，何者处于下方是可以根据需要任意设置的。下文所述的基层顶面和底面，同样表达类似含义，即以水平放置，光源从上方垂直照射向基层而言，此时，位于上方的基层表面称为顶面，位于下方的基层表面称为底面。可以理解，当基层垂直放置，光源从左侧或右侧，或者从前侧或后侧垂直照射向基层时，可等同替代为前侧

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面和后侧面，左侧面和右侧面的表述。

此外，也需特别注意术语“可感应到光源”和“感光”之间的差异，感光象素层的“感光”，指的是该象素具有感光能力，“可感应到光源”，指的是感光象素是否能够感应到光源的结果，即感光象素的感光能力是否得到发挥，例如，由于半导体的透光性限制，当在一个半导体基层的顶面和底面各布置一个半导体感光象素层时，如果该半导体基层厚度超出半导体的透光性限制，则光源向该半导体基层照射时，只有顶面的半导体感光象素层能够感应到光源，而底面的半导体感光象素层受半导体基层厚度限制而无法感应到光源，则称顶面的半导体感光象素层为可感应到光源的感光象素层，即感光象素的感光能力得以发挥；称底面的半导体感光象素层为不可感应到光源的感光象素层，即感光象素的感光能力未能发挥。注意到在后文中，利用不可感应到光源的感光象素层，可以形成不感光的转移和读取象素层。

当化学镀膜感光象素或半导体感光象素为双向感光象素时，则涉及到感光选向问题，即尽管能够双向感光，但不能接受同一时刻两个方向的光照，需要在一个时刻选择一个方向的光源照射，感光选向方式可以为隔离选向、分时选向、分区选向、或象素选向等等，也就是说，可以通过例如遮光膜遮挡等方式来实现分时刻、分区域、分象素的感光选向。双向照射的情况，例如图 8 所示。

感光象素层，大致相当于垂直于光源照射方向的感光平面，在这样的感光平面中，布置有多个感光象素（通常形成为多行多列的象素阵列），对于多个感光象素层中的每一感光象素层，其可能是平面混合型，也就是既布置有化学镀膜感光象素，也布置有半导体感光象素。另外的情形是，同一感光象素层中仅布置一种感光象素，如此，将形成化学镀膜感光象素层，或者半导体感光象素层。

在实施方式中，感光器件的同一位置（即由一层感光象素层的该象素位置上穿透而来的光照射到另一感光象素层上的位置）但不同层的感光象素，分别感应包含紫外线、可见光、近红外、和远红外中的一个互补谱段或子谱段；或者分别感应包含紫外线、可见光、近红外、和远红外中的一个正交谱段或子谱段。其中，互补谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近

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SAMSUNG EX. 1002 - 3957/4148

红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱；

正交谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱。

实施方式包括让感光器件中至少一层感应两个不同的光谱(即射频)谱段。对于每一感光象素层而言，其象素阵列的色彩排列包括同一排列(象素阵列中的象素色彩相同)、水平排列(象素阵列中的同一行象素色彩相同)、垂直排列(象素阵列中的同一列象素色彩相同)、对角排列(象素阵列中的同一对角线的象素色彩相同)、广义贝叶排列(象素阵列中的一条对角线上的象素色彩相同，另外一条对角线上的象素色彩不同)、YUV422 排列、横向 YUV422 排列、蜂窝排列、均布排列(四个象素均匀交错等距排列)等。

需要注意的是，本文中的术语“布置”，包含了各种在例如半导体基层或透光层上形成化学镀膜感光象素层或半导体感光象素层的制作工艺。例如，半导体基层为一个 N 型硅晶体基板，在该基板一面上的一个象素位置，根据色彩的深度需求，由该象素位置表面向基板内部做一定深度的 P 杂质置入，形成一个 P 掺杂层，该 P 掺杂层即形成为一个半导体象素，如果在该 P 掺杂层做另一定深度的 N 杂质置入，形成在 P 掺杂层中的 N 掺杂层，该 N 掺杂层即形成为另一半导体感光象素(与前一 P 掺杂层的半导体感光象素在不同感光象素层，但象素位置相对应)，可以按照《多光谱感光器件及其制作方法》(PCT/CN2007/071262)提供的方法，在 390nm 附近，500nm 附近，610nm 附近，和 760nm 附近设置分层线，使得任一分层线上下的对应点象素感应互补或正交的光谱。图 1 给出了一个分层线的设置的例子，即通过不同深度的杂质掺入，形成不同的色彩。在基板的该面进行化学镀膜溶液的涂抹加工，可以形成化学镀膜感光象素层，由于制作或者加工工艺的多样性，在本文中均以“布置”进行表述。

上述的两层半导体感光象素在不同深度上的布置，实现了在基板一个

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SAMSUNG EX. 1002 - 3958/4148

表面上的同一象素位置可以感应到至少两个谱段，从而提供了在该表面上的象素图案排列上的更好的灵活性以及更多的象素布置，能够大幅提高感光器件的灵敏度,解析度,和动态范围。

对于上述在半导体基板某一面的不同深度的掺杂加工，其同一位置最多布置两层感光象素，这是由于在同一位置布置 3 层，加工上难度极大，同时在布线上，由于各层间的引线需要相互隔离，3 层引线显然造成了布线上的困难。而在本发明中，采用同一面上最多布置两层上述的半导体感光象素层，并可结合平面上的象素图案排列完成彩色重建，因而可以实现更好的彩色感光性能。由于同一面上最多以深度掺杂方式布置两个半导体感光象素层，因而明显降低了立体加工工艺的难度，且在布线上，也相对简单。

对于基板，可以采用单面或者双面加工工艺，从而形成单面感光器件或者双面感光器件。双面感光器件，对于上述的深度掺杂加工，如果采用两个半导体感光象素层一者布置在基板的顶面，另一者布置在基板底面的双面布置方式，则对于每一面而言，其都简化为平面加工工艺，可以在一面上完成一个感光象素层的平面加工后，将基板进行翻转而在另一面同样以平面加工工艺完成另一感光象素层的加工，使得加工工艺近似于现有的单面单层感光器件的加工工艺，相对于上述的同一面的两层掺杂的立体加工而言，更为简单。另一方面，沿光照方向，在基板的某一位置，可以布置多层感光象素。

半导体感光象素层通常制作在半导体基层上，为了实现景深扩展，在实际制作中，通常采用增设透光层（例如透明玻璃层）来调整不同感光象素层之间的距离，例如，在一半导体基层上制作一层或多层半导体感光象素层，而后在该半导体基层上放置一透光层，而后，在该透光层上涂抹加工出一层化学镀膜感光象素层。通过透光层的不同厚度设置，相当于预设化学镀膜感光象素层和半导体感光象素层之间的间隔距离，进而实现景深扩展。

在很多的应用里，在化学镀膜感光象素层或半导体感光象素层的正面，背面，或双面并不涂任何滤光膜。但在另外一些应用里，如对于色彩还原要求特别高的专业相机或摄像机，实施方式包括使用滤光膜的方式。滤光膜设置在化学镀膜感光象素层或半导体感光象素层中的全部或部分感光象素的正面，背面，或双面。滤光膜的选频特性包括红外截止滤波、兰

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色带通、绿色带通、红色带通、青色带通、黄色带通、品红色带通、或可见光带通。滤光膜的使用是通过牺牲少数象素的灵敏度，来去除不想要的光谱的影响，减少上下左右象素之间的干涉（crosstalk），或者获得正交性更好的三原色或是更纯正的补色信号。

实施方式包括让所述多景深感光器件的多层感光象素层的相邻两层各自使用自己的读取电路。

实施方式包括让所述多景深感光器件的多层感光象素层的相邻两层共用置于其中一层的读取电路。

实施方式包括让所述多景深感光器件的读取电路位于半导体感光象素层，或独立的读取电路层。

所述多景深感光器件的读取电路的实施方式包括采用《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）和《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）中的象素读取和子采样方法。

实施方式包括在所述多景深感光器件的信号读取电路里采用主动象素读取电路、被动象素读取电路、或主动象素与被动象素混合读取电路。

所述主动象素包括 3T、4T、5T、或 6T 主动象素。3T 和 4T 的主动象素结构分别如图 2 和图 3 所示。

所述读取电路的共享方式包括无共享方式、单层或上下层 4 点共享方式、单层或上下层 6 点共享方式、单层或上下层 8 点共享方式、或单层或上下层任意点共享方式。4 点共享方式，6 点共享方式，8 点共享方式，和任意点共享方式，分别如图 4，图 5，图 6，和图 7 所示。

实施方式中，多景深感光器件的所述读取电路包括用于对每一感光象素层的象素阵列中的紧邻的同行异列、异行同列、或异行异列的象素间进行两两合并采样，获得第一合并象素的采样数据的第一合并单元；以及用于对第一合并单元得到的第一合并象素的采样数据进行合并采样以获得第二合并象素的采样数据的第二合并单元。

实施方式还包括：读取电路还包括第三合并单元，用于对第二合并单元得到的第二合并象素的采样数据进行合并采样以获得第三合并象素的采样数据。

在本发明的一种实施例中，所述的感光器件，所述第一合并单元或第二合并单元的象素合并方式为相同或不同色彩象素间的电荷相加方式或信号平均方式，其中不同色彩象素间的象素合并方式遵照色彩空间变换的方

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SAMSUNG EX. 1002 - 3960/4148

式，以满足色彩重建的要求。

上述的第一合并象素和第二合并象素来自于将子采样至少分为两个过程的处理，即第一合并采样过程和第二合并采样过程。第一合并采样过程和第二合并采样过程，通常发生在象素的行（合并）采样和列（合并）采样之间，主要对模拟信号进行，除电荷相加部分通常只在第一合并采样过程中做以外，其次序和内容通常是可以交换的。此外，也可以包括第三合并采样过程，第三合并采样过程发生在模数转换之后，主要对数字信号进行。

对于第一合并采样过程，是取象素阵列中两个紧邻的象素来进行合并。一方面，完成了紧邻象素的合并，将合并后的象素称为第一合并象素，需要理解的是，第一合并象素只是为本发明描述之便，利用该概念来指代进行第一合并过程后的象素，而不代表物理上，在象素阵列中存在一个“第一合并象素”;将两个紧邻象素合并采样后的数据称为第一合并象素的采样数据。紧邻，系指两个象素之间从水平，垂直，或对角方向上来看紧挨着，中间没有其它象素。紧邻的情况包含同行异列，异行同列，或异行异列。一般而言，在这种合并中，信号将至少是两个象素的信号平均，而噪声则会降低$\sqrt{N}$，因此，合并后，至少可以将信噪比提高$\sqrt{N}$倍，且这种合并可以在相同或不同色彩的象素之间进行。另一方面，由于两个合并的色彩可以不同，即色彩相加或平均，从色彩的三原色原理可知，两种原色的相加是另一种原色的补色，就是说，两个不同原色的象素合并，产生另一种原色的补色，从原色空间，变换到了补色空间，仅仅是发生了色彩空间变换，仍然可以通过不同的补色而完成彩色重建。也即通过这种方式，既能实现不同色彩的象素合并以提高信噪比，同时又能够进行彩色重建。整个子采样过程也因此得到优化，更加适应大数据量的象素阵列的高速需求。色彩空间变换的一个基本要求是，变换后的色彩的组合，能够（通过插值等手段）重建所需要的RGB（或YUV，或CYMK）色彩。

需要了解，由于通常象素阵列包含多个象素，第一合并采样只是将两个象素进行合并，显然，合并形成的第一合并象素也具有多个。对于不同的第一合并象素，其采用的色彩合并方式可以相同，也可以不同。当第一合并全部在相同的色彩间进行时，我们将之称为同色合并方式；当第一合并全部在不同的色彩间进行时，我们将之称为异色合并方式；当第一合并部分在相同色彩间进行、部分在不同色彩间进行，我们将之称为混杂合并

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方式；当对象素阵列中的一些多余的色彩进行抛弃（当然，抛弃是选择性的，例如，不能因此而影响到彩色重建），这样的色彩合并方式称为选择性抛弃多余彩色方式。

显然的，第二合并过程是对多个第一合并象素的操作，同样的，可以将色彩相同的第一合并象素进行合并；也可以将色彩不同的第一合并象素进行合并（当然，这种情况下可能导致三原色的全部相加而无法重建出彩色）。

上述的同色合并、异色合并、混杂合并等方式，是将合并采样做基于色彩的分类，另外，从合并采样的位置选取的角度，第一合并过程和第二合并过程的合并采样方式包括：直接输出到总线的信号自动平均方式、跳行或跳列方式，逐个采样方式，以及这些方式的两种或三种的同时使用。除电荷相加部分通常只能在第一合并采样过程中做以外，第一合并过程和第二合并过程，除了次序的不同外，其方式都是相同和可以交换的。

所谓直接输出到总线的信号自动平均方式，就是，将需要合并的信号（色彩相同或是不同），同时输出到数据采集总线上去，通过（电压）信号的自动平衡，来获得需要合并信号的平均值。所谓跳行或跳列方式就是跳过一些行或列，从而通过减少数据量的方式来实现（合并）采样。所谓逐个采样方式，实际上就是不做任何合并，依此读取原来的象素或第一合并象素。这三个方式有一些是可以同时使用的，例如，跳行或跳列方式可与直接输出到总线的信号自动平均方式或逐个采样方式同时使用。

第三合并采样过程的子采样方式包括色彩空间变换方式、后端数字图像缩放方式、以及这两个方式的串行使用。第一和第二合并过程主要是在模拟信号上进行，而第三子采样过程主要是在数字信号上进行，即模数转换之后进行。通过将处于不同空间位置的三个或四个色彩象素，当作同一个点上的值而转换到另一个色彩空间，就又可实现水平和（或）垂直方向上的数据减少，从而达到子采样的效果。而数字图像缩放方式，是最为直观常用的子采样方式。

在合并采样时可以实现电荷相加。目前的合并采样几乎都是只做到了电压或电流信号的平均，这种方式在合并 N 点时，最多只能将信噪比提高 $\sqrt{N}$ 倍。这是因为现有的合并采样都是 N 个相同色彩的象素共用一根输出线的方式进行合并采样，在这根输出线上，各个象素的电压或电流信号必然要进行（自动的）平均，因此，其信噪比的提高只是在于噪声合并后降

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SAMSUNG EX. 1002 - 3962/4148

低了$\sqrt{N}$，从而使信噪比提高最多$\sqrt{N}$倍。而采用本发明的电荷相加方式，例如通过读取电容存储电荷，实现电荷的累加，从而信号可以进行叠加而使得信噪比可以提高至少N倍， 比信号平均的方法高至少$\sqrt{N}$倍。也就是说，将N个信号以电荷相加的方法合并，理论上最高可以达到N^2个信号相平均的效果或更好(如下面所述)，这是效果非常显著的提高信噪比的手段。

紧邻象素相加，还带来另外一个显著的效果，就是，象素之间的相互干扰(cross-talking)效果被减弱。这是由于本来相互干扰的色彩，现在是合法的一体，也就是说，原来属于噪声的一部分信号，现在成了有效的信号部分，因此，N 个信号电荷相加带来信噪比的改进，可以接近理论上的上限，即$N\sqrt{N}$倍，从而，相当于N^3个信号相平均的效果。

在全图采样（即对一个图像的按最高分辨率进行采样）时，可以采用逐行扫描、隔行或跨行读取的方式，不需要提高时钟速度和采用帧缓存器，将大阵列图像的全图读取帧率在拍单张照时翻倍。如果增加AD转换器和行缓存，那么，全图读取帧率还可以提高更多。这个方法对于省去机械快门有非常重要的价值。

请注意本发明的逐行扫描、隔行或跨行读取的方式，与传统电视系统里的场扫描方式（interleaved scanning）是不同的。传统的场扫描方式，是隔行扫描，隔行读取，因此，奇数场和偶数场（无论是感光还是读取）在时间上差了一场，即半帧。而本发明的逐行扫描、隔行或跨行读取的方式，象素在感光时间顺序上却是与逐行扫描、逐行读取方式是完全一样的，只是行的读取次序做了变化。细节描述请见《一种多光谱感光器件及其采样方法》(中国申请号: 200910105948.2)和《一种感光器件及其读取方法、读取电路》(中国申请号: 200910106477.7) 。

在本发明的一种实施例中，所述的感光器件，所述色彩空间变换包括RGB到CyYeMgX空间的变换、RGB到YUV空间的变换、或CyYeMgX到YUV空间的变换，其中X为R(红)、G(绿)、B(兰)中的任一种。图10显示了一种利用色彩空间变换来实现子采样的一种方式。

实施方式中包括，上述电荷相加方式通过象素直接并联或将电荷同时转移到读取电容（FD）中完成。

如上所述，多景深感光器件中，第一合并单元或第二合并单元的基于色彩的合并采样方式包括同色合并方式、异色合并方式、混杂合并方式、或选择性抛弃多余色彩合并方式，且第一合并单元和第二合并单元采用的

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SAMSUNG EX. 1002 - 3963/4148

合并采样方式不同时为同色合并方式，也即两个合并单元中至少有一个合并单元不采用同色合并方式。

如上所述，第一合并单元或第二合并单元的基于位置的合并采样方式包括以下几种方式中的至少一种：直接输出到总线的信号自动平均方式、跳行或跳列方式、和逐个采样方式。亦即这几种基于位置的合并采样方式可以单独使用，也可以组合使用。

如上所述，在上述感光器件中，可以用色彩空间变换方式和后端数字图像缩放方式中的至少一种来实现所述第三合并采样单元的合并采样方式。

图 9 显示了一种异色象素电荷合并的方式。

实现上述子采样功能的是如图 25 所示的行地址解码控制器和列地址解码控制器。行地址解码控制器将输出两类信号，行选信号 Row[i]（每行一条线）和行控制矢量信号 RS[i]（每行一条或多条线），其中 i 为行的标号。类似地，列地址解码控制器将输出两类信号，列选信号 Col[j]（每列一条线）和列控制矢量信号 T[j]（每列一条或多条线），其中 j 为列的标号。

行选信号 Row[i]是用来做行的选择，而列选信号 Col[j]是用来做列的选择。这是两组相对标准的信号。行控制矢量信号 RS[i]是对现有 CMOS 行控制信号的扩展（每行一条线扩展到每行多条线），而列控制矢量信号 T[j]，有的 CMOS 感光器件根本没有，即使有，也是一列只有一个。

RS[i]和 T[j]用来控制感光象素的复位，清零，感光时间控制，电荷转移，象素合并，和象素读取。由于行列的对称性，RS[i]和 T[j]有很多种具体的实现方式。这些信号的具体实现方式并不受限。

如上所述，多光谱感光器件的全图采样方式包括逐行扫描、逐行读取方式或逐行扫描、隔行或跨行读取方式。

实施方式还包括制作一种感光系统，包括上述的多景深感光器件。

所述感光系统用于获取正面，背面，或双向的图像。

所述感光系统包括数码相机，照相手机，摄像机，视频或照相监控系统，图像识别系统，医学图像系统，军用、消防、和井下图像系统，自动跟踪系统，立体影像系统，机器视觉系统，汽车视觉或辅助驾驶系统，电子游戏系统，网络摄像头，红外和夜视系统，多光谱成像系统，和电脑摄像头。

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SAMSUNG EX. 1002 - 3964/4148

实施方式还包括实现一种景深扩展方法，包括步骤：在感光器件中设置至少两个可感应到光源的感光象素层，并将至少两个所述感光象素层按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号，被聚焦到不同的感光象素层。

景深扩展方法中，通过来自不同感光象素层的具有不同清晰度的图像而获取一幅清晰图像。

实施方式中还包括一种成像方法，或者说所述感光器件在成像中的应用，是设置镜头和包括至少两个可感应到光源的感光象素层的感光器件；将所述感光器件放置在距所述镜头特定距离，且至少两个所述感光象素层之间按预设距离间隔布置，使得来自镜头的不同光信号被聚焦到不同的所述感光象素层。

参见图 11-14，实施方式中还包括了一种光学成像系统，包括镜头和多景深感光器件，所述多景深感光器件布置在距所述镜头特定距离，包括至少两个可感应到光源的感光象素层；至少所述感光象素层之间按预设距离间隔布置，来自距所述感光器件特定距离的镜头的不同光信号，被聚焦到不同的感光象素层。

如图 13，可以是不同距离上的所有感兴趣波长的光，分别聚焦在每一感光象素层；或者如图 14，可以是相同距离上的不同波长的光，分别聚焦在每一感光象素层；也可以是不同距离上的不同波长的光，分别聚焦在每一感光象素层。

实施方式包括各个感光象素层聚焦的光，其波长按各个感光象素层距所述光学镜头从近到远逐渐增长。或者在各个感光象素层中，更远距离的光信号，被聚焦在离镜头更近的感光象素层。

例如，当包括两个可感应到光源的感光象素层，两个感光象素层分别位于镜头的第一象距和第二象距，可以通过光学镜头设计，将紫外光、兰色光、绿色光、青色光、或白色光聚焦在离镜头最近的感光象素层；相应的，将兰色光、绿色光、红色光、黄色光、或红外光聚焦在离镜头最远的感光象素层。

又如，当包括三个可感应到光源的感光象素层，三个感光象素层分别位于镜头的第一象距、第二象距、第三象距，可以通过光学镜头设计，将紫外光、兰色光、绿色光、或青色光聚焦在离镜头最近的感光象素层；相应的，将红色光、黄色光、可见光、或红外光聚焦在离镜头最远的感光象素层；相应的，将绿色光、黄色光、可见光、或红色光聚焦在中间的感光象素

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SAMSUNG EX. 1002 - 3965/4148

层。

又如，当包括四个可感应到光源的感光象素层，四个感光象素层分别位于镜头的第一象距、第二象距、第三象距、第四象距，可以通过光学镜头设计，将紫外光、兰色光、绿色光、或青色光聚焦在离镜头最近的感光象素层；相应的，将红色光、黄色光、白色光、或红外光聚焦在离镜头最远的感光象素层；相应的，将兰色光、绿色光、或青色光聚焦在离镜头第二近的感光象素层；相应的，将绿色光、红色光、白色光、或黄色光聚焦在离镜头第三近的感光象素层。

又如，当包括两个可感应到光源的感光象素层，两个感光象素层分别位于镜头的第一象距、第二象距，可以通过光学镜头设计，将紫外光或可见光聚焦在离镜头最近的感光象素层；将可见光或红外光聚焦在离镜头最远的感光象素层。

又如，当包括三个可感应到光源的感光象素层，三个感光象素层分别位于镜头的第一象距、第二象距、第三象距，可以通过光学镜头设计，将紫外光或白色光聚焦在离镜头最近的感光象素层；将白色光或红外光聚焦在离镜头最远的感光象素层；将白色光聚焦在中间的感光象素层。

又如，当包括四个可感应到光源的感光象素层，四个感光象素层分别位于镜头的第一象距、第二象距、第三象距、第四象距，可以通过光学镜头设计，将紫外光或白色光聚焦在离镜头最近的感光象素层；将白色光或红外光聚焦在离镜头最远的感光象素层；将白色光聚焦在离镜头第二近的感光象素层；将白色光聚焦在离镜头第三近的感光象素层。

需要注意的是，在上述例子中，对于包括所有感兴趣波长的光，例如白色光，如果说明白色光被聚焦到不同感光象素层，则其一般来源于不同距离，即例如离镜头最近的感光象素层聚焦的是无穷远处的白色光，离镜头最远的感光象素层聚焦的是感兴趣最短距离的白色光。即当两个感光象素层聚焦的光信号的频谱特性相同，则其必须具有不同的距离特性。

本发明的多景深感光器件，兼具多光谱的优异特性，可同时获得众多的彩色信号和其它光谱信号，例如在一种四层感光器件中，可沿光路按距光源从近到远布置一个感应紫外光的第一化学镀膜感光象素层、一个感应兰光，绿光，或青光的第一半导体感光象素层，一个感应红光，黄光，或绿光的第二半导体感光象素层，一个感应红外光的第二化学镀膜感光象素层。其中，第一半导体感光象素层和第二半导体感光象素层分别实现在两个半导体基层上，两个半导体基层之间设置一个具有预设厚度的透光层，

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SAMSUNG EX. 1002 - 3966/4148

第一化学镀膜感光象素层布置在第一半导体感光象素层所在基层的顶面上方；第二化学镀膜感光象素层布置在第二半导体感光象素层所在基层的底面下方。由此，不仅实现了景深扩展，且可几乎最大程度的利用入射光能量，在得到彩色的同时，也得到全光谱的信息，充分发挥不同感光材料的特点。这样一种四层多光谱感光器件，制作难度并不太高。如果结合采用前文中本人之前发明的先进采样和以电荷合并和色彩变换为显著特征的子采样电路和方法，更能够大幅地降低感光器件和系统的复杂度，从而为各种应用提供巨大的方便和崇高的性能。

本发明的多景深感光器件，首先实现的第一种特殊用途是景深扩展，现有的 EDoF 主要是使用了光学和数学的手段实现景深扩展，一般需要借助例如镜头等进行自动对焦，相比之下，本发明是直接的通过器件内的不同感光象素层按预设距离间隔设置这样的物理手段实现景深扩展。其次实现的第二种特殊用途是实现全局电子快门，现有的全局电子快门 (Global Shutter) 主要是使用了读取电路的手段，相比之下，本发明利用不感光的转移和读取象素，可以在不用机械快门的情况下，实现高象素的高速拍照。当这两种实现(即景深扩展和全局电子快门)，在同一个感光器件上得以集成的时候，多层多光谱感光器件的巨大威力就得以充分的发挥。因此，本发明在很多指标和性能上，大幅超越现有的方法。

本发明的多景深感光器件，借助于调整不同感光象素层的距离，除了大幅提高灵敏度以外，还能大幅提高系统景深范围，从而让图像更清楚，系统反应速度更快，应用面更宽，乃至消除某些应用中的自动对焦需求。本发明的多景深感光器件在其涵盖的景深范围，能够快速地获取清晰的图像，而不需要经过一个调焦的过程。景深扩展除了能够降低自动对焦的难度和成本外，甚至在某些应用中如手机照相，微距照相，或远距照相，能够彻底消除自动对焦的需求。景深扩展还能让同一张照片里处于不同距离的物体同时清楚，这在一些特殊应用中也是极有用的，而这是自动对焦所不能做到的，因为现有的自动对焦系统，只能让某个距离内的物体清楚成像，而不能让非常宽的一个范围内的物体都清楚。因此，本发明的景深扩展实现，在具有自动对焦能力的系统里，也仍然具备有很大的价值

由于本发明的多景深感光器件的高灵敏度，其感光速度也可大幅提高，从而为在很多应用中取下机械快门提供了可能。由此，在本发明的多景深感光器件中，还提出一种具有跨层读取功能的全局电子快门的实现，以期

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SAMSUNG EX. 1002 - 3967/4148

取代某些应用中可能需要的机械快门。全局电子快门作用是在一瞬间，将感光象素里的电荷或电压值拷贝到不感光的读取象素里去，以便读取电路从容的读出。

结合景深扩展全局电子快门的实现，将二者集成在一个感光器件上时，一个不需要自动对焦和机械快门的高性能、高速度、高象素感光系统，就可以芯片的方式来实现，大大地降低系统的尺寸、复杂度、功耗和成本，为很多新的应用提供了可能。

这种带有全局电子快门的或多景深的感光器件，可为感光系统省去机械快门或者省去自动对焦系统(或者降低对自动对焦系统的要求)，并在不加快感光器件时钟的情况下，实现高速的电子快门或清晰成像。

在极大地简化了感光系统的机械复杂度的要求的同时，本发明采用两层或多层的布局，结合先进的两层或多层互补或正交色彩图案排列的方法，能够最大化的利用入射光子的能量，不用或只用少许的彩色滤光膜，从而达到或接近到达光电转换效率的理论上限，并在完整地重建彩色的同时，获得其它光谱的图像，包括紫外线图像，近红外图像，和远红外图像。

当感光象素层与读取电路分层后，读取电路层的读取电路和处理计算可以做得非常精细和复杂，为单芯片感光系统的制作，提供了巨大的便利。

这种多景深感光器件可同时获得众多的彩色信号和其它光谱信号，采用本人之前发明的先进的采样和以电荷合并和色彩变换为显著特征的子采样电路和方法，能够大幅地降低感光器件和系统的复杂度，从而为各种应用提供巨大的方便和崇高的性能。

这种多景深感光器件，可用于正面感光，背面感光，或双向感光。通过精细布置各层感光器件的象素感应光谱段和各层色彩图案的合理布局，可以产生各种优选的多光谱感光器件，如高灵敏度彩色感光器件，高灵敏度彩色和红外感光器件，无杂色（杂色由插值引起的）的高灵敏度彩色或多光谱感光器件等等。

采用主动象素和被动象素读取相结合的手段，可以获得超低功耗感光器件，超高动态范围感光器件。

以上内容是结合具体的实施方式对本发明所作的进一步详细说明，不能认定本发明的具体实施只局限于这些说明。对于本发明所属技术领域的普通技术人员来说，在不脱离本发明构思的前提下，还可以做出若干简单推演或替换，都应当视为属于本发明的保护范围。

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SAMSUNG EX. 1002 - 3968/4148

权 利 要 求 书

1. 一种多景深感光器件，其特征在于，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

2. 如权利要求 1 所述的感光器件，其特征在于，所述感光象素层包括化学镀膜感光象素层和半导体感光象素层中的至少一者。

3. 如权利要求 2 所述的感光器件，其特征在于，所述化学镀膜感光象素层包括量子点感光象素。

4. 如权利要求 2 所述的感光器件，其特征在于，所述半导体感光象素层包括 CMOS 光敏二极管、CMOS 感光门、CCD 光敏二极管、CCD 感光门、和具有双向电荷转移功能的 CMOS 和 CCD 感光二极管和感光门。

5. 如权利要求 1-4 任一所述的感光器件，其特征在于，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

6. 如权利要求 5 所述的感光器件，其特征在于，波长更短的光信号被聚焦到离镜头更近的感光象素层。

7. 如权利要求 6 所述的感光器件，其特征在于，所述感光象素层为两层，紫色光、兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

8. 如权利要求 6 所述的感光器件，其特征在于，所述感光象素层为三层，紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层；兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层；红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层。

9. 如权利要求 5 所述的感光器件，其特征在于，更远距离的光信号被聚焦到离镜头更近的感光象素层。

10. 如权利要求 9 所述的感光器件，其特征在于，所述感光象素层为两层，无穷远处的光信号被聚焦到离镜头较近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头较远的感光象素层。

11. 如权利要求 10 所述的感光器件，其特征在于，无穷远处的紫色光、

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SAMSUNG EX. 1002 - 3969/4148

兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，感兴趣最短距离的绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

12. 如权利要求 9 所述的感光器件，其特征在于，所述感光象素层为三层，无穷远处的光信号被聚焦到离镜头最近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的光信号被聚焦到位于中间的感光象素层。

13. 如权利要求 12 所述的感光器件，其特征在于，所述感光象素层为三层，无穷远处的紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层，感兴趣最短距离的红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层。

14. 如权利要求 10-13 任一所述的感光器件，其特征在于，所述感兴趣最短距离包括 2mm, 5mm, 7mm, 1cm, 2cm, 3cm, 5cm, 7cm, 10cm, 20cm, 30cm, 40cm, 50cm, 60cm, 70cm, 80cm, 100cm, 或 150cm。

15. 如权利要求 1-14 任一所述的感光器件，其特征在于，至少两个所述感光象素层之间设置有透光层。

16. 如权利要求 1-15 任一所述的感光器件，其特征在于，所述感光象素层中的感光象素为正面感光象素、背面感光象素、或双向感光象素。

17. 如权利要求 16 所述的感光器件，其特征在于，当感光象素为双向感光象素时，其感光选向方式为隔离选向、分时选向、分区选向、或象素选向。

18. 如权利要求 1-17 任一所述的感光器件，其特征在于，所述感光象素层中的感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个互补谱段或子谱段；或者所述化学镀膜感光象素和半导体感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个正交谱段或子谱段。

19. 如权利要求 18 所述的感光器件，其特征在于，所述互补谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，

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SAMSUNG EX. 1002 - 3970/4148

黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱；

所述正交谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱。

20. 如权利要求 1-19 任一所述的感光器件，其特征在于，每一感光象素层中的色彩排列包括同一排列、水平排列、垂直排列、对角排列、广义贝叶排列、YUV422 排列、横向 YUV422 排列、蜂窝排列、均布排列。

21. 如权利要求 1-20 任一所述的感光器件，其特征在于，至少一个所述感光象素层中的部分或全部感光象素的正面、背面或双面设置有滤光膜，所述滤光膜的选频特性包括红外截止滤波、兰色带通、绿色带通、红色带通、青色带通、黄色带通、品红色带通、或可见光带通。

22. 如权利要求 1-21 任一所述的感光器件，其特征在于，所述感光象素层中的相邻两层各自设有读取电路；或者所述感光象素层的相邻两层共用读取电路。

23. 如权利要求 22 所述的感光器件，其特征在于，所述读取电路为主动象素读取电路、被动象素读取电路、或主动象素与被动象素混合读取电路。

24. 如权利要求 23 所述的感光器件，其特征在于，所述主动象素包括 3T、4T、5T 或 6T 主动象素。

25. 如权利要求 22 所述的感光器件，其特征在于，所述读取电路的共用方式包括单层或上下层 4 点共享方式、单层或上下层 6 点共享方式、单层或上下层 8 点共享方式、或单层或上下层任意点共享方式。

26. 如权利要求 22-25 所述的感光器件，其特征在于，所述读取电路包括用于对每一感光象素层的象素阵列中的紧邻的同行异列、异行同

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SAMSUNG EX. 1002 - 3971/4148

列、或异行异列的象素间进行两两合并采样，获得第一合并象素的采样数据的第一合并单元；以及用于对第一合并单元得到的第一合并象素的采样数据进行合并采样以获得第二合并象素的采样数据的第二合并单元。

27. 如权利要求 26 所述的感光器件，其特征在于，所述读取电路还包括第三合并单元，用于对第二合并单元得到的第二合并象素的采样数据进行合并采样以获得第三合并象素的采样数据。

28. 如权利要求 26 或 27 所述的感光器件，其特征在于，所述第一合并单元或第二合并单元的象素合并方式为相同或不同色彩象素间的电荷相加方式或信号平均方式，其中不同色彩象素间的象素合并方式遵照色彩空间变换的方式，以满足色彩重建的要求。

29. 如权利要求 28 所述的感光器件，其特征在于，所述色彩空间变换包括 RGB 到 CyYeMgX 空间的变换、RGB 到 YUV 空间的变换、或 CyYeMgX 到 YUV 空间的变换，其中 X 为 R(红)、G(绿)、B(兰)中的任一种。

30. 如权利要求 29 所述的感光器件，其特征在于，所述电荷相加方式通过象素直接并联或将电荷同时转移到读取电容（FD）中完成。

31. 如权利要求 26-30 所述的感光器件，其特征在于，所述第一合并单元或第二合并单元的基于色彩的合并采样方式包括同色合并方式、异色合并方式、混杂合并方式、或选择性抛弃多余色彩合并方式，且第一合并单元和第二合并单元采用的合并采样方式不同时为同色合并方式。

32. 如权利要求 26-31 所述的感光器件，其特征在于，所述第一合并单元或第二合并单元的基于位置的合并采样方式包括以下几种方式中的至少一种：直接输出到总线的信号自动平均方式、跳行或跳列方式、和逐个采样方式。

33. 如权利要求 27-32 所述的感光器件，其特征在于，所述第三合并单元的合并采样方式包括：色彩空间变换方式和后端数字图像缩放方式中的至少一种。

34. 如权利要求 1-33 所述的感光器件，其特征在于，包括具有跨层读取功能的全局电子快门，所述全局电子快门包含多个可同时转移并读取一层或多层感光象素层的电荷或电压值的不感光的转移和读取象素。

35. 如权利要求 34 所述的感光器件，其特征在于，所述多个不感光的转

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SAMSUNG EX. 1002 - 3972/4148

移和读取象素位于不感光象素转移和读取层；或者位于所述感光象素层。

36. 如权利要求 35 所述的感光器件，其特征在于，每一感光象素层，设置有一个紧邻的不感光象素转移和读取层。

37. 如权利要求 34-36 任一所述的感光器件，所述不感光转移和读取象素由半导体电路制成。

38. 一种景深扩展方法，其特征在于，包括：
在感光器件中设置至少两个可感应到光源的感光象素层，并将至少两个所述感光象素层按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

39. 如权利要求 38 所述的景深扩展方法，其特征在于，通过来自不同感光象素层的具有不同清晰度的图像而获取一幅清晰图像。

40. 一种光学成像方法，其特征在于，包括：
设置镜头和包括至少两个可感应到光源的感光象素层的感光器件；
将所述感光器件放置在距所述镜头特定距离，且至少两个所述感光象素层之间按预设距离间隔布置，使得来自镜头的不同光信号被聚焦到不同的所述感光象素层。

41. 一种光学成像系统，其特征在于，包括镜头和多景深感光器件，所述多景深感光器件布置在距所述镜头特定距离，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自所述镜头的不同光信号被聚焦到不同的所述感光象素层。

42. 如权利要求 41 所述的光学成像系统，其特征在于，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

43. 如权利要求 42 所述的光学成像系统，其特征在于，波长更短的光信号被聚焦到离镜头更近的感光象素层。

44. 如权利要求 42 所述的光学成像系统，其特征在于，更远距离的光信号被聚焦到离镜头更近的感光象素层。

45. 一种感光系统，其特征在于，包括如权利要求 1-35 任一所述的感光器件。

46. 如权利要求 45 所述的感光系统，其特征在于，所述感光系统包括数码相机，照相手机，摄像机，视频或照相监控系统，图像识别系统，医学图像系统，军用、消防或井下图像系统，自动跟踪系统，立体

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SAMSUNG EX. 1002 - 3973/4148

影像系统，机器视觉系统，汽车视觉或辅助驾驶系统，电子游戏系统，网络摄像头，红外和夜视系统，多光谱成像系统，和电脑摄像头中的一种。

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SAMSUNG EX. 1002 - 3974/4148

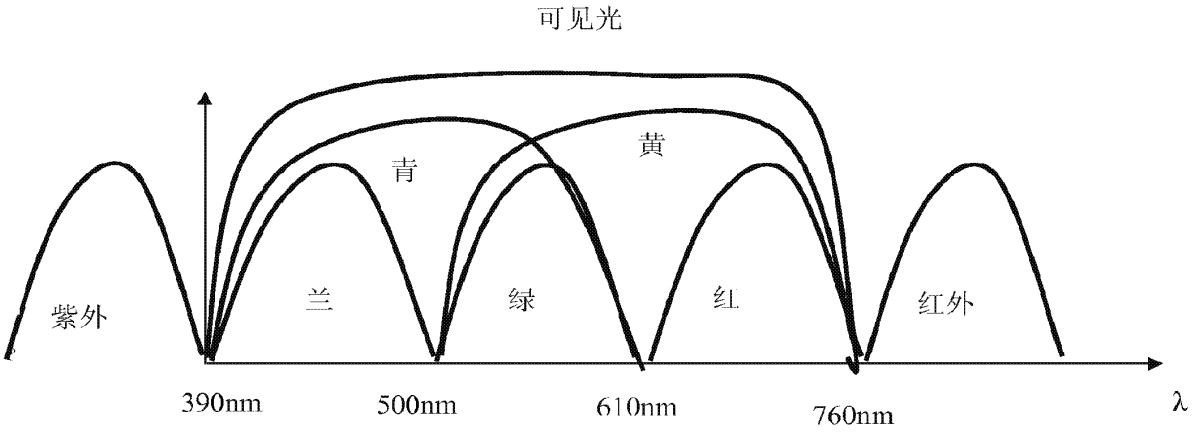


图 1

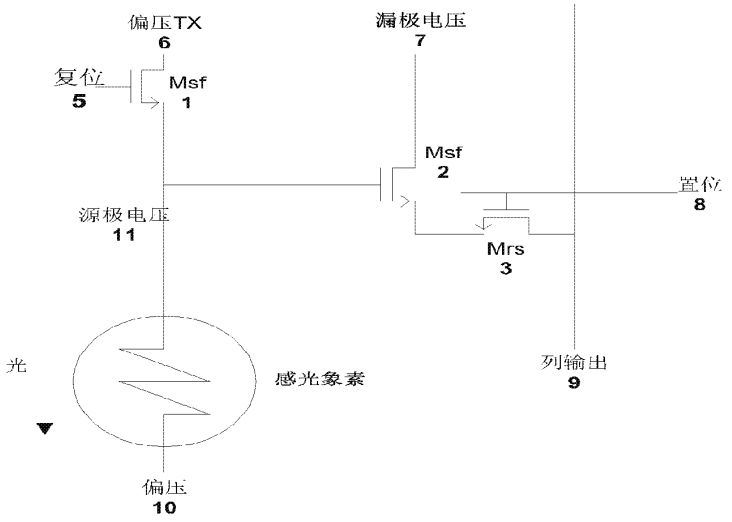


图 2

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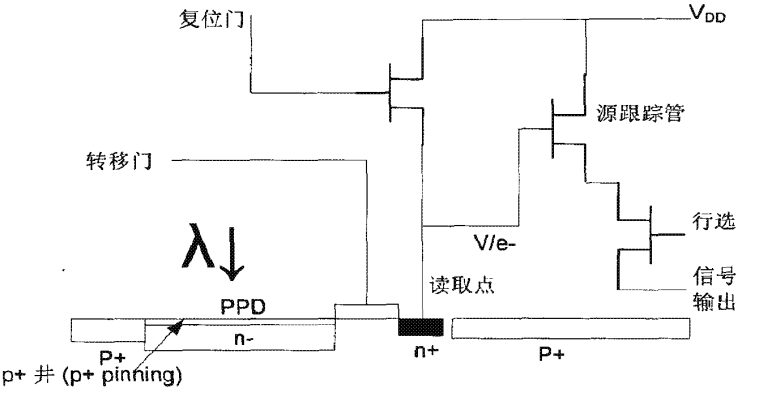


图 3

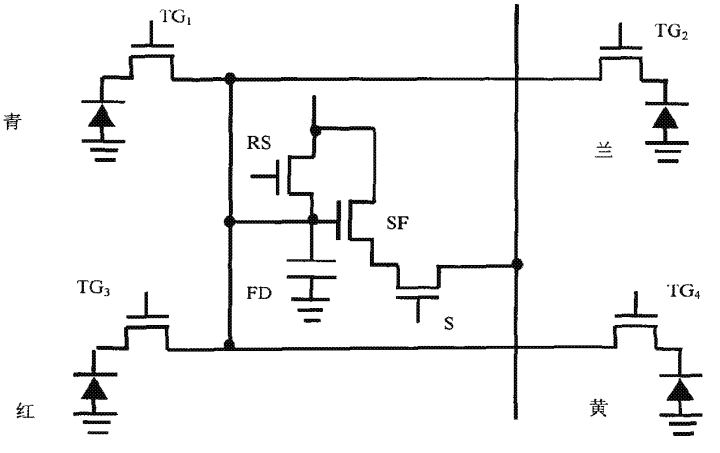


图 4

替换页(细则第26条)

SAMSUNG EX. 1002 - 3976/4148

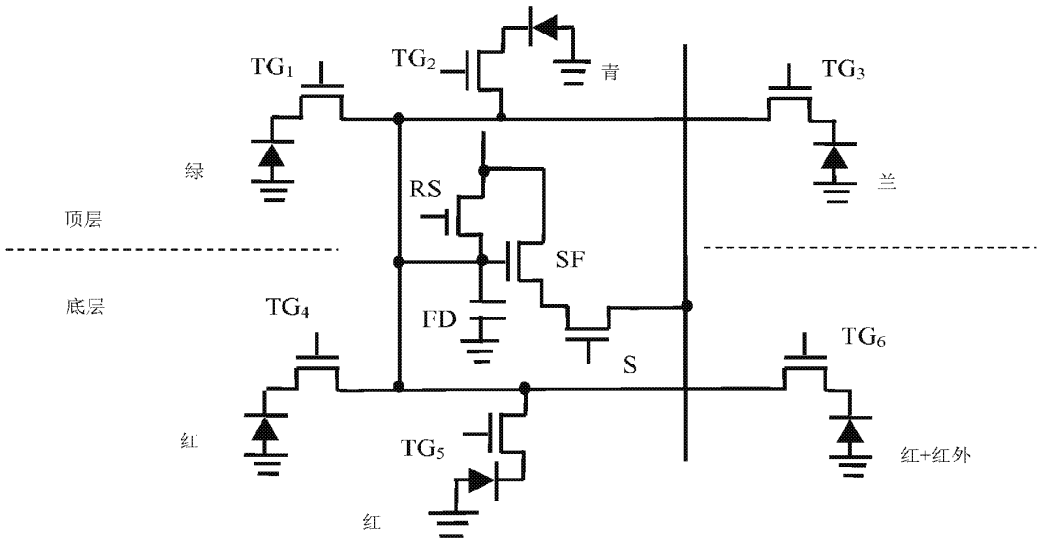


图 5

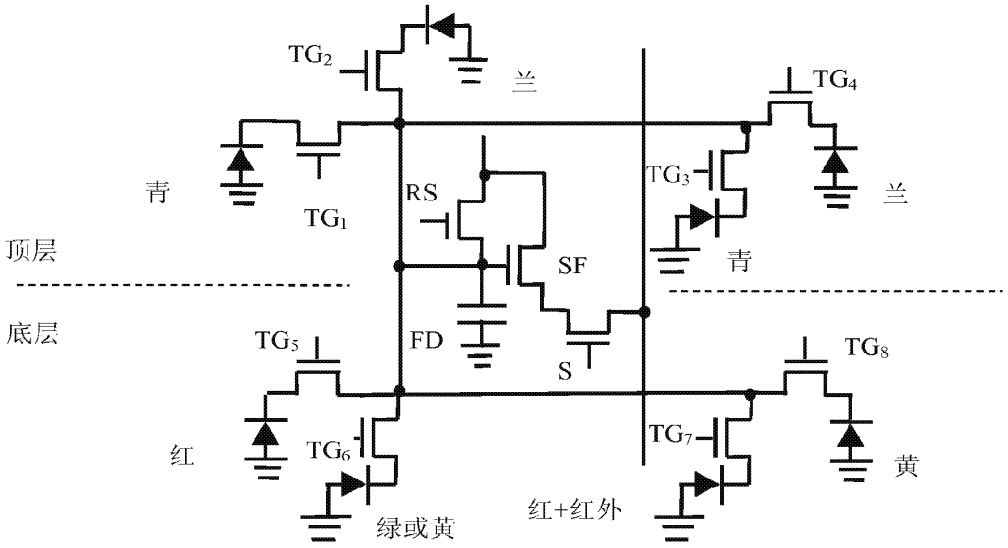


图 6

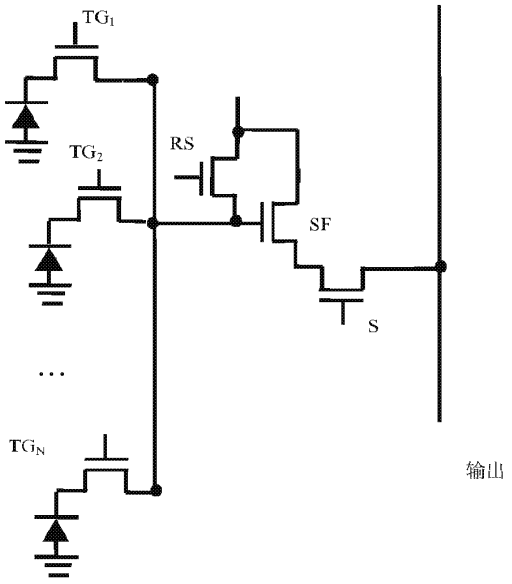


图 7

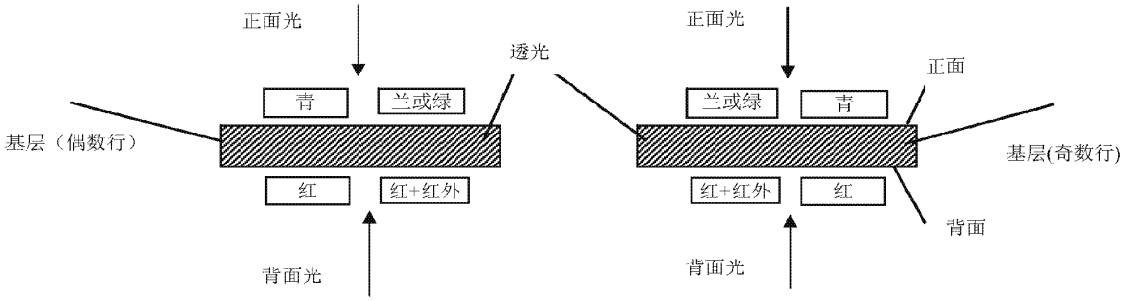


图 8

SAMSUNG EX. 1002 - 3979/4148

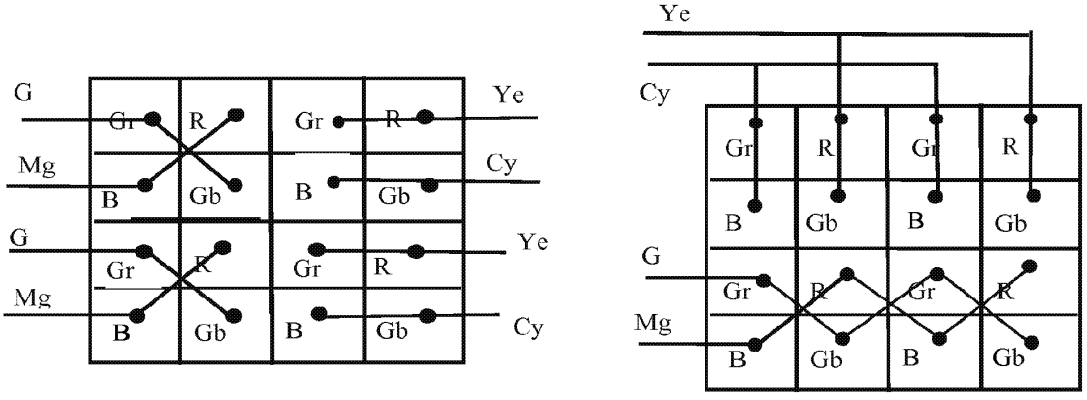


图 9

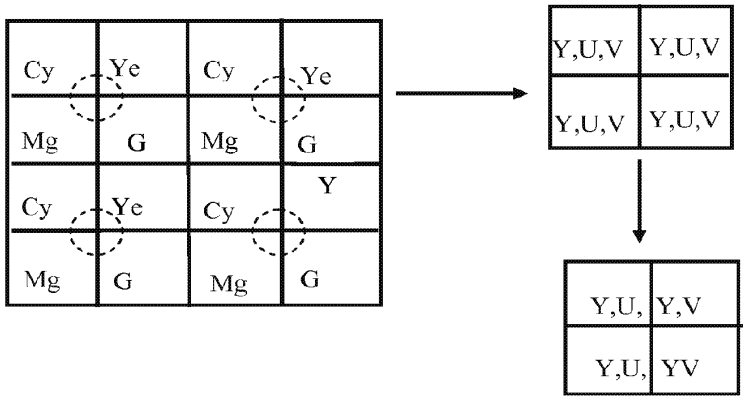


图 10

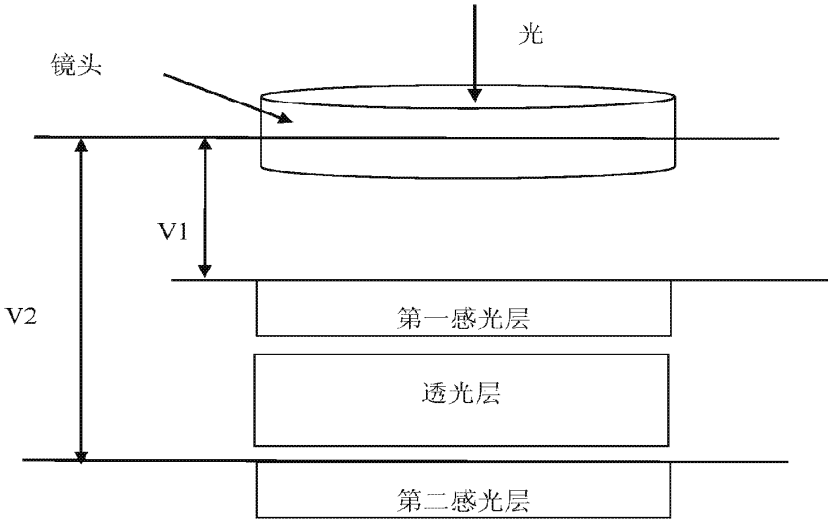


图 11

SAMSUNG EX. 1002 - 3981/4148

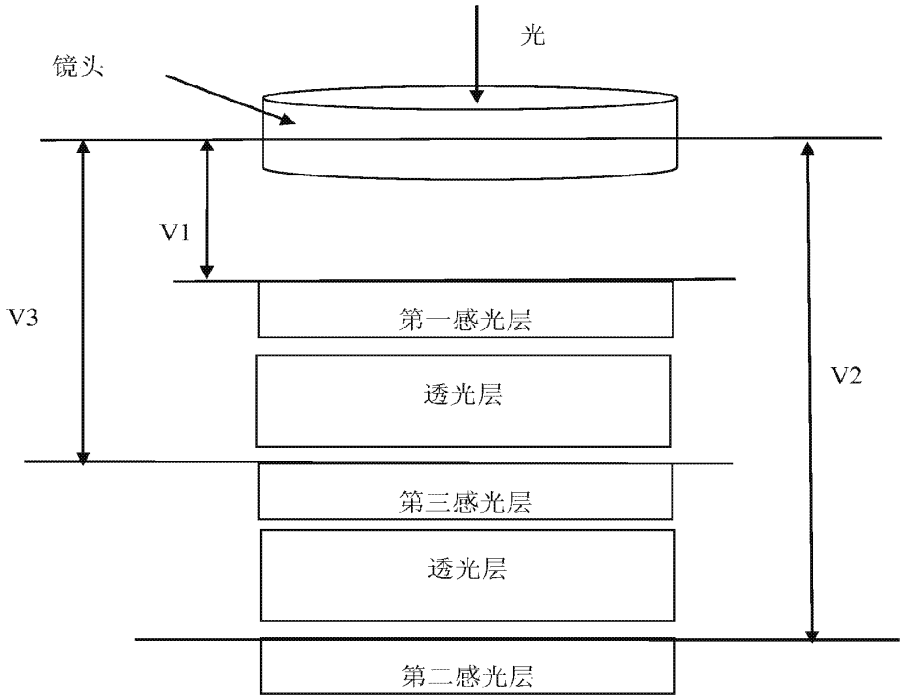


图 12

SAMSUNG EX. 1002 - 3982/4148

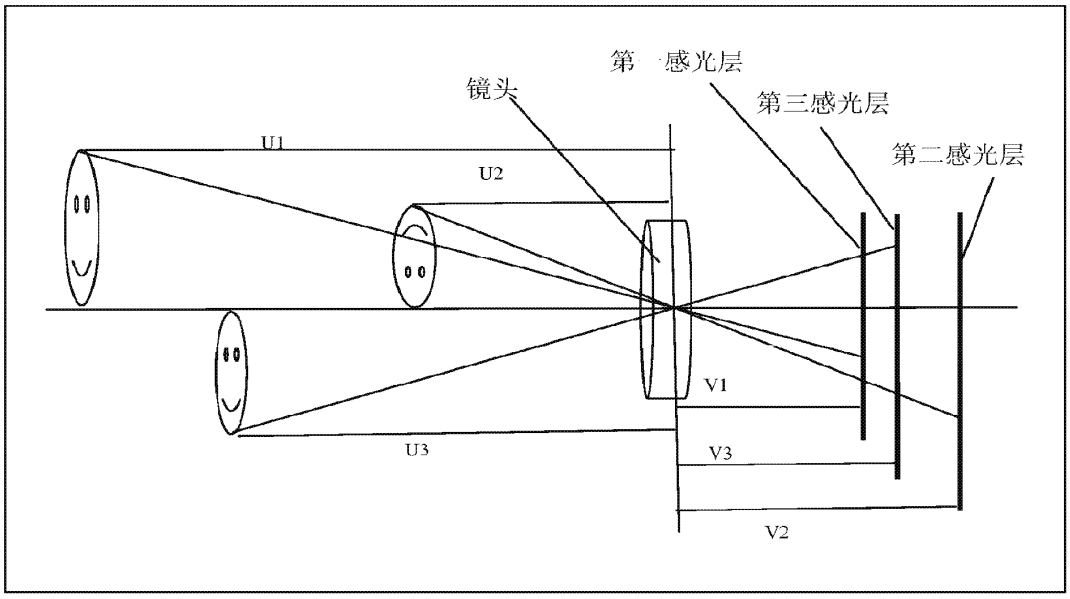


图 13

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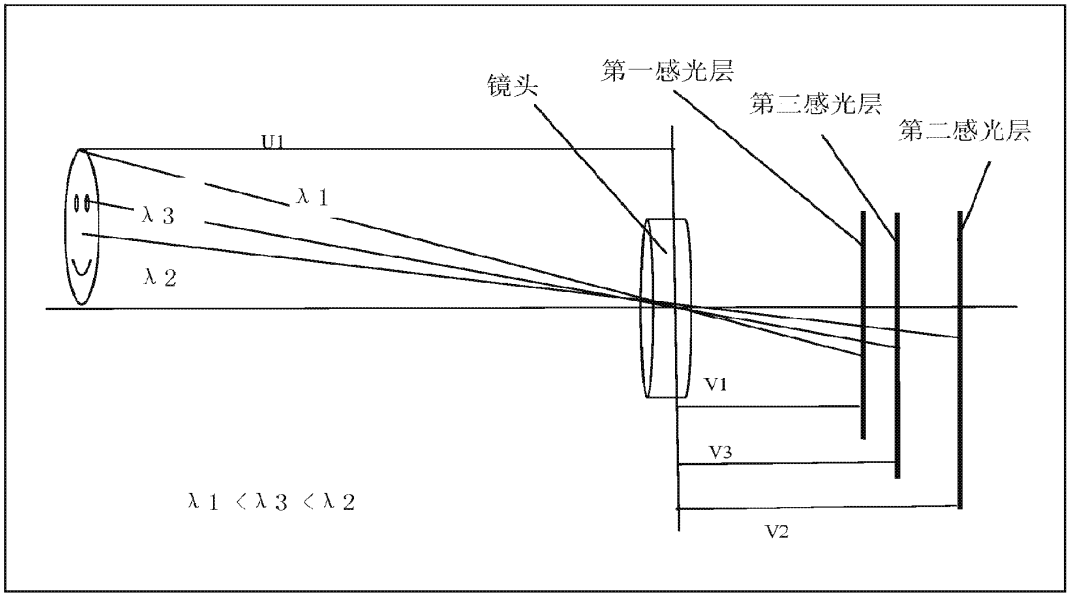


图 14

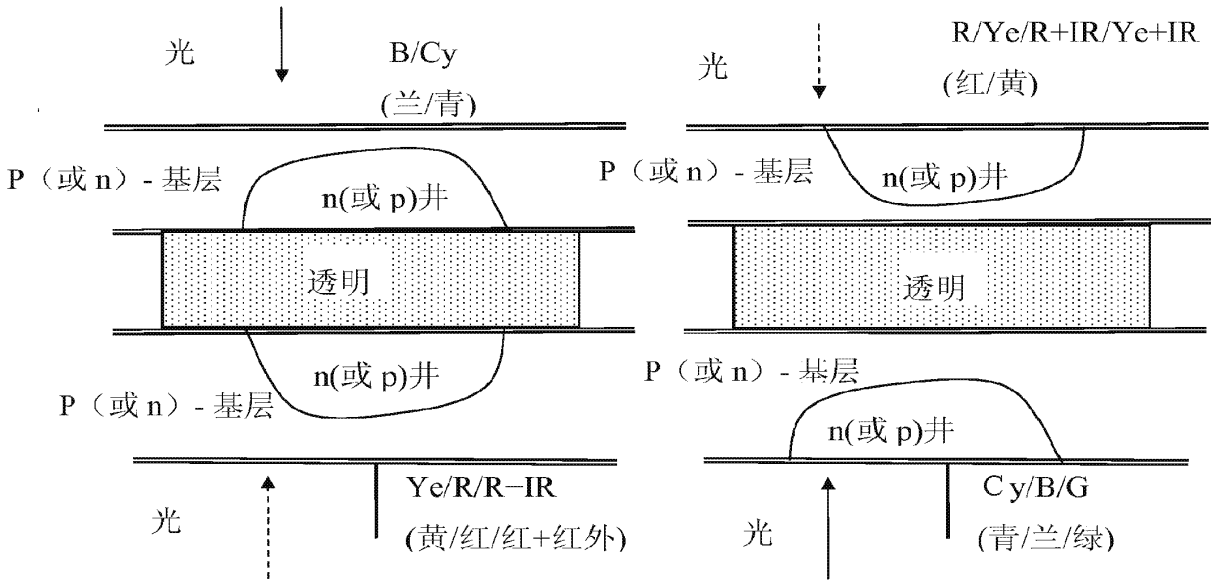


图 15

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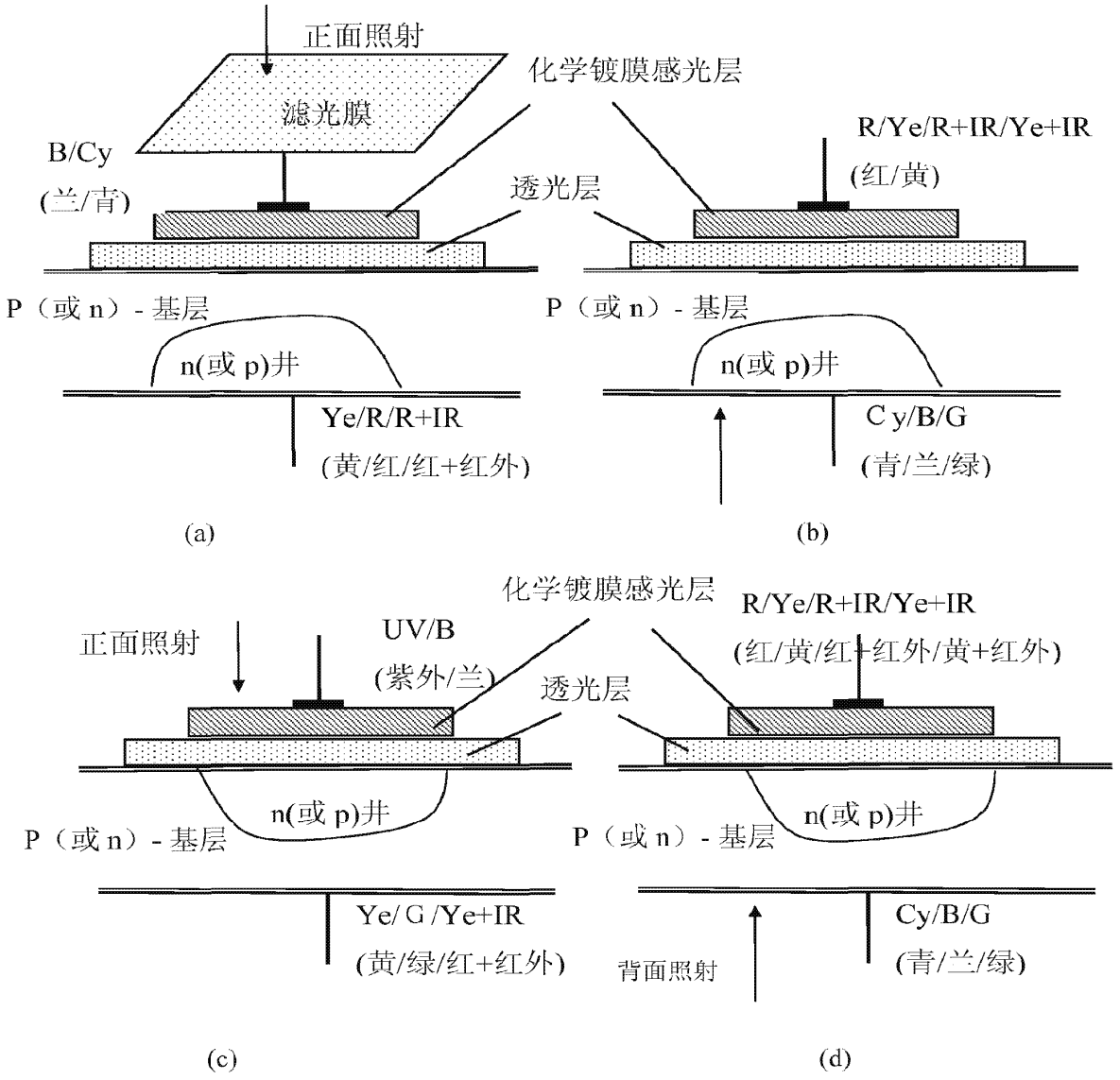


图 16

SAMSUNG EX. 1002 - 3986/4148

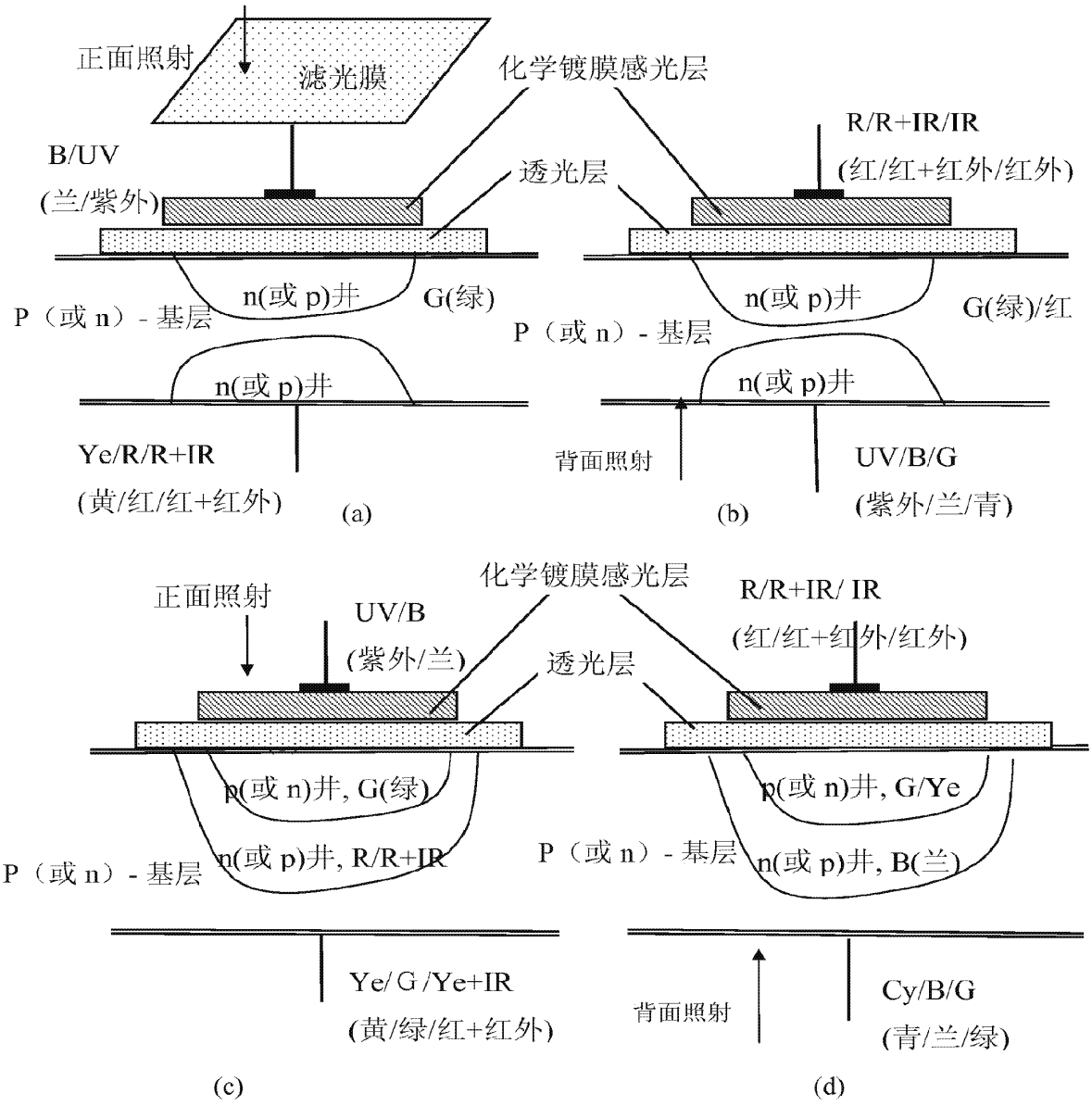


图 17

SAMSUNG EX. 1002 - 3987/4148

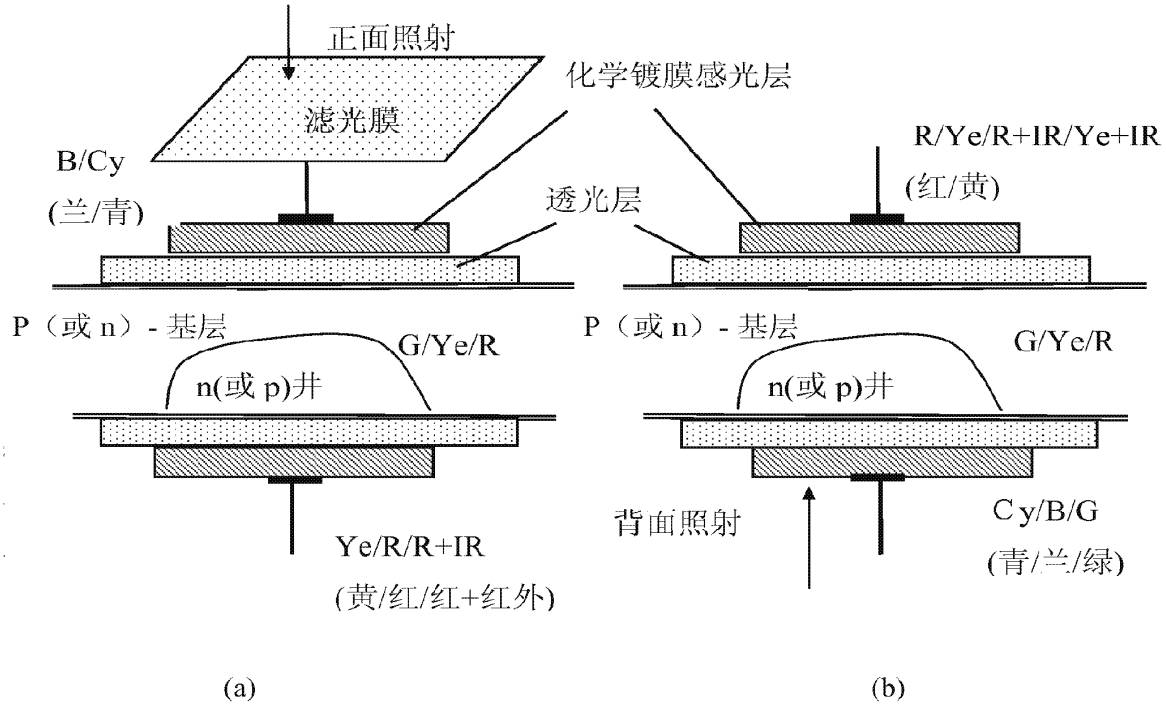


图 18

SAMSUNG EX. 1002 - 3988/4148

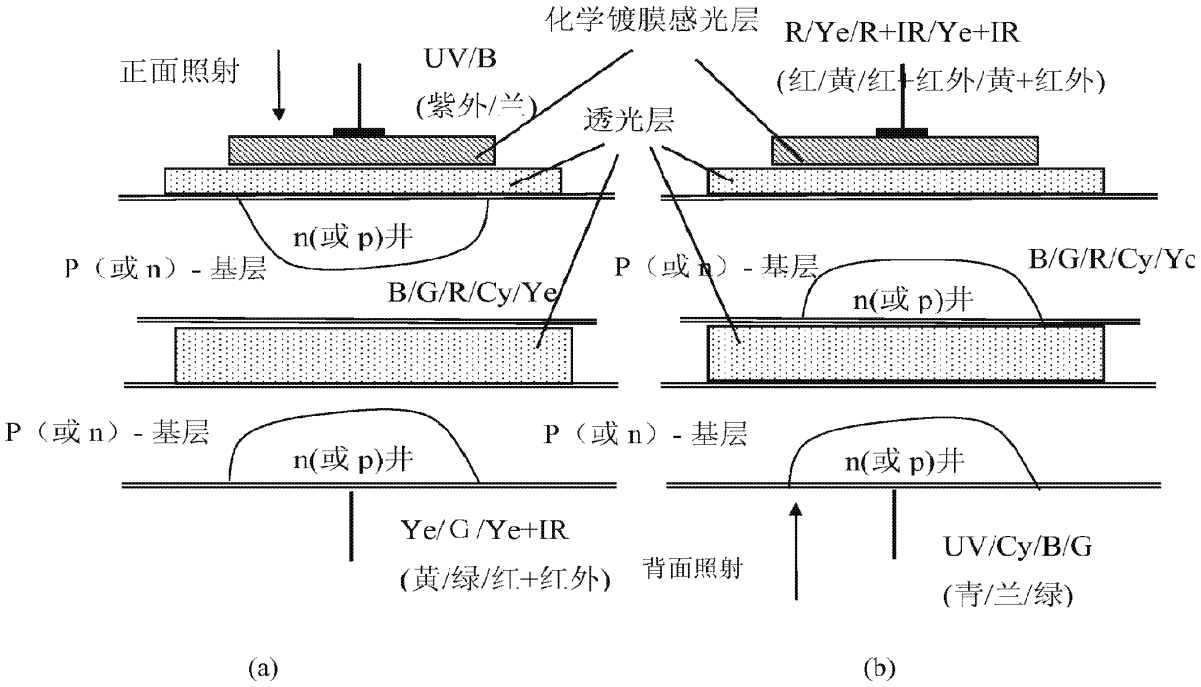

化学镀膜感光层
R/Ye/R+IR/Ye+IR
(红/黄/红+红外/黄+红外)
正面照射
UV/B
(紫外/兰)
透光层
n(或 p)井
P（或 n）- 基层
B/G/R/Cy/Ye
P（或 n）- 基层
B/G/R/Cy/Yc
n(或 p)井
P（或 n）- 基层
n(或 p)井
P（或 n）- 基层
n(或 p)井
Ye/G/Ye+IR
(黄/绿/红+红外)
背面照射
UV/Cy/B/G
(青/兰/绿)
(a)
(b)

图 19

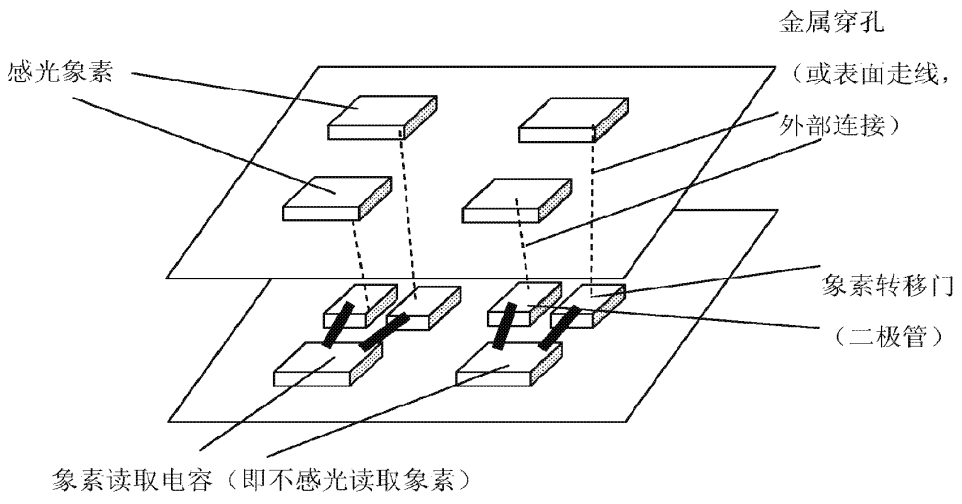


图 20

SAMSUNG EX. 1002 - 3990/4148

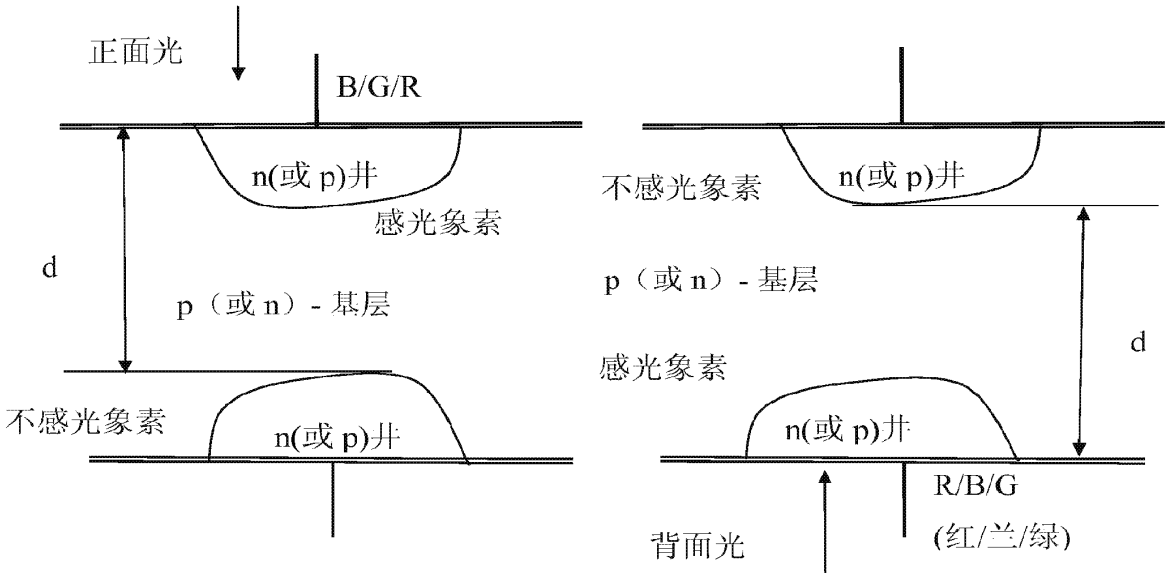


图 21

SAMSUNG EX. 1002 - 3991/4148

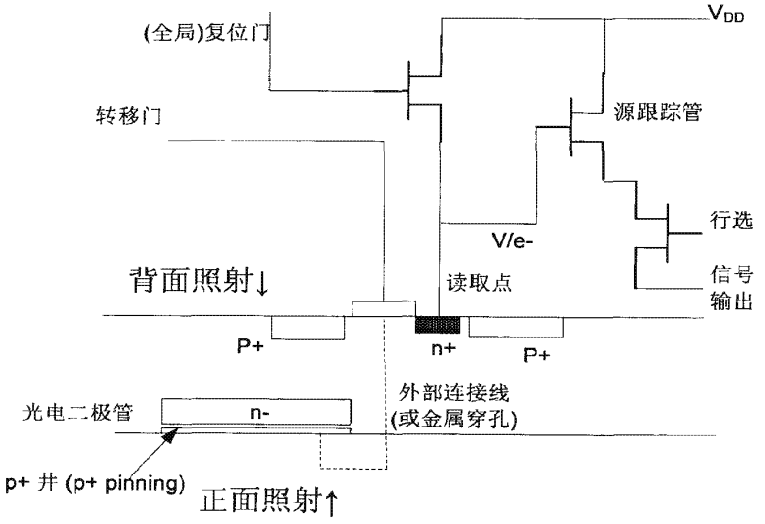


图 22

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SAMSUNG EX. 1002 - 3992/4148

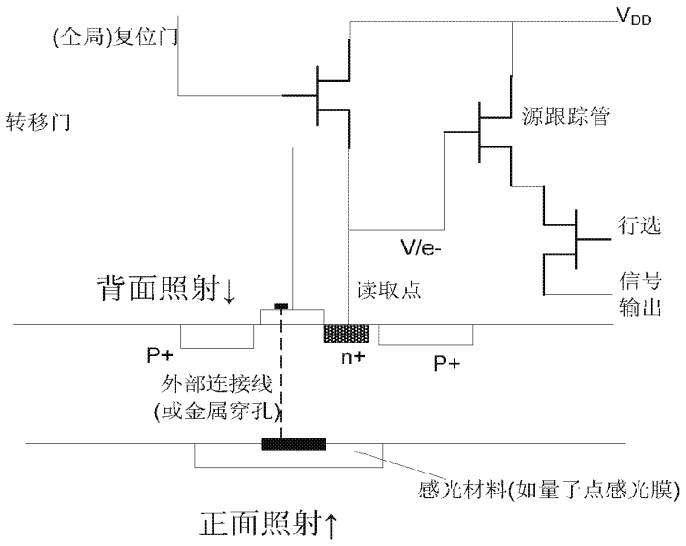


图 23

SAMSUNG EX. 1002 - 3993/4148

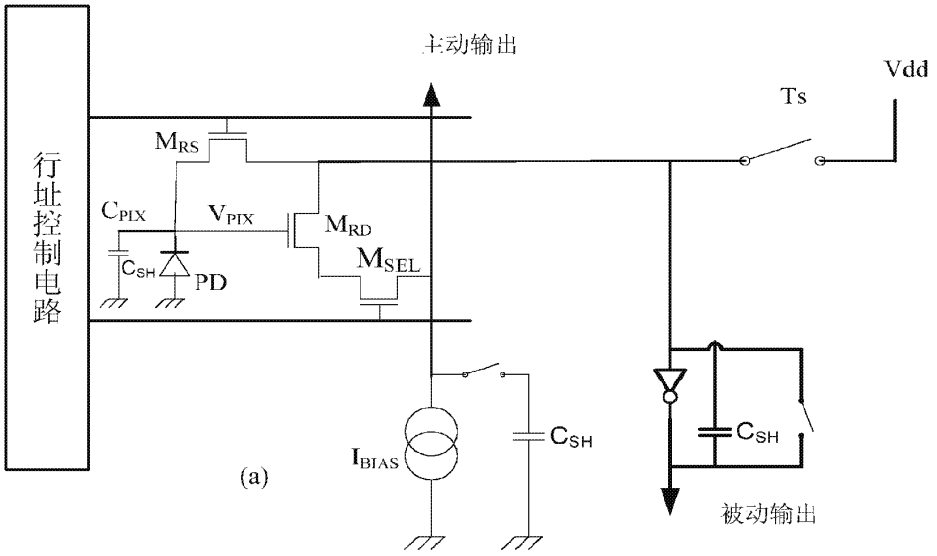


图 24

SAMSUNG EX. 1002 - 3994/4148

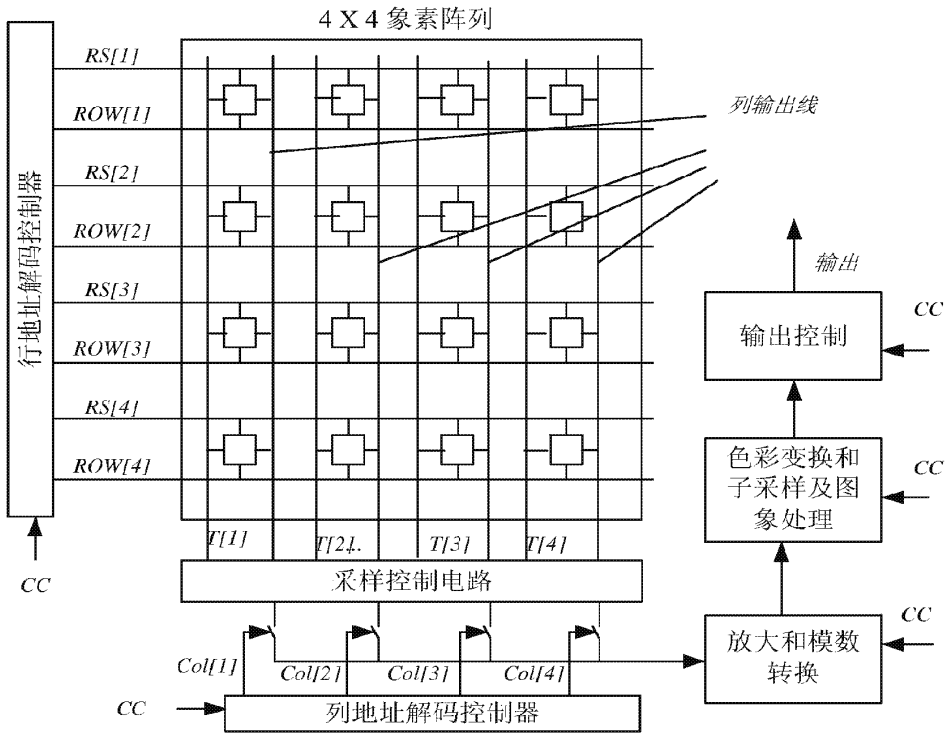


图 25

SAMSUNG EX. 1002 - 3995/4148

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/076338

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS,CNKI,WPI,EPODOC: photo sensitive pixel lens signal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN101345248B (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD et al) 14 Jul.2010 (14.07.2010) embodiment of the description figs. 5-16	1,4-14,18-21,38-46
Y		2-3,15-17,22-37
Y	CN101740587A (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD) 16 Jun.2010 (16.06.2010) figs. 9-14	15-17
Y	CN101807590A (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD) 18 Aug.2010 (18.08.2010) [0043]-[0057] of the description, figs. 7-17	15-17,22-25

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the prineiple or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 Mar.2012 (21.03.2012)	**29 Mar. 2012 (29.03.2012)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer ZHONG, Yi Telephone No. (86-10)62411594

Form PCT/ISA /210 (second sheet) (July 2009)

SAMSUNG EX. 1002 - 3996/4148

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/076338

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN101834974A (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD) 15 Sep.2010 (15.09.2010) claims, [0076]-[0091] of the description, figs. 1-26	25-37
Y	WO2008131313A2 (TIAN et al) 30 Oct.2008 (30.10.2008) The whole document	2-3, 25-37
X	US2006266921A1 (KANG et al) 30 Nov.2006 (30.11.2006) Figs.7-10	1,38,40,41,45
X	JP2005526458A (MICRON TECHNOLOGY INC) 2 Sep.2005 (02.09.2005) Fig. 3	1,38,40,41,45
E	CN102244083A (BORIS MULTI-MEDIA HOLDINGS INC) 16 Nov.2011 (16.11.2011) The whole document	1-5,20-33
E	CN102263114A (BORIS MULTI-MEDIA HOLDINGS INC) 30 Nov.2011 (30.11.2011) The whole document	1-46

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SAMSUNG EX. 1002 - 3997/4148

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/076338

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN101345248B	14.07.2010	CN101345248A	14.01.2009
		WO2009006776A1	15.01.2009
		EP2172973A1	07.04.2010
		US2010141771A1	10.06.2010
		KR20100057599A	31.05.2010
		CA2705315A1	15.01.2009
		INMUMNP201000137E	16.07.2010
		JP2010532869A	14.10.2010
CN101740587A	16.06.2010	None	
CN101807590A	18.08.2010	None	
CN101834974A	22.09.2010	None	
CN102244083A	16.11.2011	None	
CN102263114A	30.11.2011	None	
WO2008131313A2	30.10.2008	WO2008131313A3	11.12.2008
		US2009152664A1	18.06.2009
		EP2143141A2	13.01.2010
		US2010187404A1	29.07.2010
		US2010187408A1	29.07.2010
		US7923801B2	12.04.2011
		CN102017147A	13.04.2011
		US8013412B2	06.09.2011
		US8004057B2	23.08.2011
		US2011297915A1	08.12.2011
		US2011297815A1	08.12.2011
		US2011303897A1	15.12.2011
		US2011303898A1	15.12.2011
		US2011309238A1	22.12.2011
		US2011309236A1	22.12.2012
US2006266921A1	30.11.2006	JP2006332602A	07.12.2006
		CN1870282A	29.11.2006

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SAMSUNG EX. 1002 - 3998/4148

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/076338

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
		KR20060122136A	30.11.2006
		KR100665177B1	09.01.2007
		US7348539B2	25.03.2008
		TW200642077A	01.12.2006
		CN100481479C	22.04.2009
		TW306308B1	11.02.2009
		JP4418443B2	17.02.2010
JP2005526458A	02.09.2005	US2003211405A1	13.11.2003
		WO3098940A1	27.11.2003
		AU2003269305A1	02.12.2003
		US6783900B2	31.08.2004
		EP1506679A1	16.02.2005
		KR20050003456A	10.01.2005
		CN1669332A	14.09.2005
		EP1506679B1	27.12.2006
		KR100621086B1	14.09.2006
		DE60310706E	08.02.2007
		DE60310706T2	11.10.2007
		CN100375539C	12.03.2008

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SAMSUNG EX. 1002 - 3999/4148

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/076338

A. CLASSIFICATION OF SUBJECT MATTER

H01L27/146（2006.01）i
H04N5/335（2011.01）i

SIONYX1403000039.0014

SAMSUNG EX. 1002 - 4000/4148

国际检索报告

国际申请号 **PCT/CN2011/076338**

A. 主题的分类

见附加页

按照国际专利分类(IPC)或者同时按照国家分类和 IPC 两种分类

B. 检索领域

检索的最低限度文献(标明分类系统和分类号)

IPC： H01L

包含在检索领域中的除最低限度文献以外的检索文献

在国际检索时查阅的电子数据库(数据库的名称，和使用的检索词（如使用）)

CNABS，CNKI，WPI，EPODOC：感光 象素 镀膜 纳米 颗粒 pixel photo sensitive lens signal

C. 相关文件

类 型*	引用文件，必要时，指明相关段落	相关的权利要求
X	CN101345248B（博立码杰通讯（深圳）有限公司等）14.7 月 2010（14.07.2010）说明书实施例，附图 5-16	1，4-14，18-21，38-46
Y		2-3，15-17，22-37
Y	CN101740587A（博立码杰通讯（深圳）有限公司）16.6 月 2010（16.06.2010）附图 9-14	15-17
Y	CN101807590A（博立码杰通讯（深圳）有限公司）18.8 月 2010（18.08.2010）说明书第[0043]-[0057]，附图 7-17	15-17，22-25
Y	CN101834974A（博立码杰通讯（深圳）有限公司）15.9 月 2010（15.09.2010）权利要求书，说明书第[0076]-[0091]，附图 1-26	25-37

☒ 其余文件在 C 栏的续页中列出。 ☒ 见同族专利附件。

* 引用文件的具体类型：

"A" 认为不特别相关的表示了现有技术一般状态的文件

"E" 在国际申请日的当天或之后公布的在先申请或专利

"L" 可能对优先权要求构成怀疑的文件，或为确定另一篇引用文件的公布日而引用的或者因其他特殊理由而引用的文件（如具体说明的）

"O" 涉及口头公开、使用、展览或其他方式公开的文件

"P" 公布日先于国际申请日但迟于所要求的优先权日的文件

"T" 在申请日或优先权日之后公布，与申请不相抵触，但为了理解发明之理论或原理的在后文件

"X" 特别相关的文件，单独考虑该文件，认定要求保护的发明不是新颖的或不具有创造性

"Y" 特别相关的文件，当该文件与另一篇或者多篇该类文件结合并且这种结合对于本领域技术人员为显而易见时，要求保护的发明不具有创造性

"&" 同族专利的文件

国际检索实际完成的日期	国际检索报告邮寄日期
21.3 月 2012（21.03.2012）	**29.3 月 2012 (29.03.2012)**
ISA/CN 的名称和邮寄地址： 中华人民共和国国家知识产权局 中国北京市海淀区蓟门桥西土城路 6 号 100088 传真号： (86-10)62019451	受权官员 钟翊 电话号码：(86-10) **62411594**

PCT/ISA/210 表(第 2 页) (2009 年 7 月)

SAMSUNG EX. 1002 - 4001/4148

C(续). 相关文件

类　型	引用文件，必要时，指明相关段落	相关的权利要求
Y	WO2008131313A2（TIAN 等）30.10 月 2008（30.10.2008） 全文	2-3, 25-37
X	US2006266921A1（KANG 等）30.11 月 2006（30.11.2006） 图 7-10	1，38，40，41，45
X	JP2005526458A（微米技术有限公司）02.9 月 2005（02.09.2005） 附图 3	1，38，40，41，45
E	CN102244083A（博立多媒体控股有限公司）16.11 月 2011（16.11.2011） 全文	1-5，20-33
E	CN102263114A（博立多媒体控股有限公司）30.11 月 2011（30.11.2011） 全文	1-46

SIONYX1403000039.0016

SAMSUNG EX. 1002 - 4002/4148

国际检索报告
关于同族专利的信息

国际申请号
PCT/CN2011/076338

检索报告中引用的专利文件	公布日期	同族专利	公布日期
CN101345248B	14.07.2010	CN101345248A	14.01.2009
		WO2009006776A1	15.01.2009
		EP2172973A1	07.04.2010
		US2010141771A1	10.06.2010
		KR20100057599A	31.05.2010
		CA2705315A1	15.01.2009
		INMUMNP201000137E	16.07.2010
		JP2010532869A	14.10.2010
CN101740587A	16.06.2010	无	
CN101807590A	18.08.2010	无	
CN101837974A	22.09.2010	无	
CN102244083A	16.11.2011	无	
CN102263114A	30.11.2011	无	
WO2008131313A2	30.10.2008	WO2008131313A3	11.12.2008
		US2009152664A1	18.06.2009
		EP2143141A2	13.01.2010
		US2010187404A1	29.07.2010
		US2010187408A1	29.07.2010
		US7923801B2	12.04.2011
		CN102017147A	13.04.2011
		US8013412B2	06.09.2011
		US8004057B2	23.08.2011
		US2011297915A1	08.12.2011
		US2011297815A1	08.12.2011
		US2011303897A1	15.12.2011
		US2011303898A1	15.12.2011
		US2011309238A1	22.12.2011
		US2011309236A1	22.12.2012
US2006266921A1	30.11.2006	JP2006332602A	07.12.2006
		CN1870282A	29.11.2006
		KR20060122136A	30.11.2006
		KR100665177B1	09.01.2007
		US7348539B2	25.03.2008
		TW200642077A	01.12.2006
		CN100481479C	22.04.2009
		TW306308B1	11.02.2009
		JP4418443B2	17.02.2010
JP2005526458A	02.09.2005	CN100375539C	12.03.2008

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SAMSUNG EX. 1002 - 4003/4148

国际检索报告
关于同族专利的信息

国际申请号
PCT/CN2011/076338

检索报告中引用的专利文件	公布日期	同族专利	公布日期
		US2003211405A1	13.11.2003
		WO3098940A1	27.11.2003
		AU2003269305A1	02.12.2003
		US6783900B2	31.08.2004
		EP1506679A1	16.02.2005
		KR20050003456A	10.01.2005
		CN1669332A	14.09.2005
		EP1506679B1	27.12.2006
		KR100621086B1	14.09.2006
		DE60310706E	08.02.2007
		DE60310706T2	11.10.2007

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SAMSUNG EX. 1002 - 4004/4148

国际检索报告

国际申请号
PCT/CN2011/076338

A. 主题的分类

H01L27/146（2006.01）i

H04N5/335（2011.01）i

SIONYX1403000039.0019

SAMSUNG EX. 1002 - 4005/4148

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 July 2014 (17.07.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/110484 A2

(51) International Patent Classification:
H01L 27/146 (2006.01)

(21) International Application Number:
PCT/US2014/011236

(22) International Filing Date:
13 January 2014 (13.01.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/751,787 11 January 2013 (11.01.2013) US
61/759,996 1 February 2013 (01.02.2013) US

(71) Applicant: **DIGIMARC CORPORATION** [US/US]; 9405 Sw Gemini Drive, Beaverton, OR 97008 (US).

(72) Inventor: **RHOADS, Geoffrey, B.**; 26855 Sw Campbell Lane, West Linn, OR 97068 (US).

(74) Agent: **CONWELL, William, Y.**; Digimarc Corporation, 9405 Sw Gemini Drive, Beaverton, OR 97008 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

WO 2014/110484 A2

(54) Title: NEXT GENERATION IMAGING METHODS AND SYSTEMS

(57) Abstract: Novel imaging arrangements are detailed. One comprises an optical array sensor with plural photo-electron generating regions dispersed at two or more layers in the structure. Two of these photo-electron generating regions are vertically separated by at least 10 microns - making the sensor useful for sensing objects at focal distances ranging from less than ten inches, out to infinity. The photosites may be spectrally selective. One such arrangement includes a top CMOS sensor array that passes 25% or more of the visible incident light into the structure. A second CMOS sensor array can be provided at a bottom of the structure, for receiving light that was not transduced to photo-electrons elsewhere in the sensor. Another arrangement involves movement of a camera sensor, in a repetitive tracking/pop-back motion, to reduce motion blur in individual frames of a video sequence. A great number of other arrangements are also detailed.

SAMSUNG EX. 1002 - 4006/4148

NEXT GENERATION IMAGING METHODS AND SYSTEMS

Related Application Data

In the US, this application claims priority to copending provisional applications 61/751,787, filed January 11, 2013, and 61/759,996, filed February 1, 2013

Field of Technology

The present technology relates to camera systems.

Background and Introduction

Foveon, Inc. (now Sigma Corporation) produces image sensors comprising an array of photosites, each of which includes three vertically-stacked photodiodes. Each of the three photosites responds to different wavelengths of light (i.e., each has a different spectral sensitivity curve). The Foveon technology is detailed, e.g., in patents 6,727,521, 6,731,397, 6,841,816, 6,958,862, 6,998,660, and 7,339,216.

Lytro, Pelican Imaging and others produce light field cameras that capture 4D light field information about a scene, through use of microlenses. Such "plenoptic imaging" systems are detailed, e.g., in patent publications 20070252074, 20080131019, 20080266655, 20100026852, 20100265385, 20110069189, 20110080487, and 20110122308.

Various companies have developed transparent semiconductors, transistors and electrodes useful in CMOS image sensors. Exemplary technology is detailed in Samsung's patent applications 20110156114 and 20090101948. Familiar transparent electrode materials include tin-doped indium oxide, zinc oxide, and carbon nanotube films. Additional information is provided in Ginsley, et al, Handbook of Transparent Conductors, Springer, 534 pp., 2011.

The artisan is presumed to be familiar with technologies involved in fabrication of semiconductor image sensors, including the foregoing.

In accordance with one aspect of the present technology, photosensors are again stacked. However, the stacking is considerably thicker than the prior art, making possible

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camera sensors that provide multi-focal length imaging, e.g., between six inches and infinity.

Fig. 1 introduces certain concepts used in the technology. Plural layers P1 – P8 are stacked in an integrated structure, behind a lens system. Each layer comprises one or more photodetectors. The distance of each layer behind the lens corresponds to a different object distance, in accordance with the focal length of the lens. (I.e., the reciprocal of the object-lens distance, plus the reciprocal of the photodetector-lens distance, equals the reciprocal of the lens focal length.)

An image sensor can comprise a 2D array of such stacks, as illustrated schematically in Fig. 2.

The foregoing and many other features and advantages of the present technology will be apparent from the following detailed description, which proceeds with reference to the accompanying drawings.

Brief Description of the Drawings

Fig. 1 shows a stack comprising plural photodetectors.

Fig. 2 shows an array comprising a 2D array of the stacks of Fig. 1.

Fig. 3 shows a basic implementation using two stacked image sensors.

Fig. 3A shows an image sharpness curve for the implementation of Fig. 3.

Fig. 4 is similar to Fig. 3, but shows four stacked image sensors.

Figs. 5-8 show other variants employing stacked image sensors.

Fig. 9 shows a sparse color filter array.

Fig. 10 illustrates how photosites in different layers of a stack can be at different positions in the layers.

Fig. 11A show how the various photosites in the Fig. 10 arrangement may spatially relate, when viewed down through the stack.

Figs. 11B and 11C are similar to Fig. 11A, but illustrate other spatial relations.

Figs. 12A and 12B show different tree structures, by which photosites can be arranged relative to charge-conducting electrodes.

Fig. 13 is a diagram illustrating movement of a smartphone sensor as a function of time.

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Fig. 14 is a schematic illustration of part of a smartphone camera system according employing certain aspects of the present technology.

Figs. 15A and 15B illustrate 2D motion of a smartphone sensor as a function of time.

Figs. 16 and 17 outline the evolution of imaging systems, culminating with "Era 5" – the subject of the present technology.

Detailed Description

Fig. 3 shows a first particular embodiment, including first and second stacked image sensors, and a lens system. The first sensor is at an image plane corresponding to an object at an infinite distance from the lens system; the second sensor is at an image plane corresponding to an object at a distance of six inches. The two sensors have the same pixel dimensions (e.g., 1936 x 2592 pixels).

The first sensor is fabricated to pass at least some of the light incident on its top surface through its structure, and on towards the second image sensor. Such transmissivity can be achieved by appropriate design and fabrication of the charge transfer conductors and associated readout circuitry, so that some light passing through the photodetection region is not blocked by such structures. For example, the structures may be sized and placed so that gaps between them allow for the passage of some light. Some of the circuitry may be positioned to the periphery of the sensor – where light passage is not an issue. Still further, some of the conductors/circuitry can be fabricated using optically-transparent materials.

In the illustrated embodiment, the top sensor absorbs 25% of the incident light, and passes 75%. But this number is not critical. Even if it passed a tenth of this amount or less (e.g., 5%), advantageous results associated with the Fig. 3 arrangement would still be realized.

Light passing through the first sensor enters an optically transmissive medium. The thickness of the medium depends on the range of focal distances to be accommodated. An exemplary thickness for this medium is 100 microns, but depending on particular application requirements this thickness may be as small as 10 microns, or as large as many hundreds of microns.

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The medium can comprise various materials. Air is attractive for certain optical properties. However, interfaces between air and other optical materials are sometimes disfavored. Another suitable medium is glass. Another is a semiconductor. Still another is a fluid. Combinations can, of course, be used.

Light exiting this medium is incident on the second image sensor. This second sensor can be conventional in structure.

When a subject is at an infinite distance from the lens, the lens presents a focused image on the top sensor. Very high resolution sampling of this image is achieved by the top sensor (in accordance with the sensor's physical resolution).

Part of that focused light energy on the top sensor from the infinite-distance object passes through the first sensor, and through the intervening medium, and falls on the second sensor. There the image is no longer focused. The strong edges and contrasts that are associated with a focused image are lost. A very low contrast, highly blurred image results.

For an object at six inches distance from the lens, the situation is reversed. The lens casts a focused image on the bottom sensor (albeit with some of the light absorbed by its passage through the top sensor), yielding high resolution image data from the bottom sensor. At the top sensor, in contrast, the image is out of focus – with low contrast.

Not shown in Fig. 3 is an ancillary system that collects data output from the two image sensors, and makes them available for post-processing. In one mode, this post-processing can comprise simply adding output signals from corresponding pixels in the first and second sensors, yielding a frame of output image data having the same dimensions as the image data from the first and second sensors. (The output signals from the first sensor may be scaled by a factor of three to compensate for the fact that the bottom sensor receives three times the light absorbed by the top sensor.)

If the post-processing operation adds the images from the first and second sensors, an image sharpness curve like that shown in Fig. 3A results. At an object distance of six inches, maximally-sharp imagery is output by the second sensor. The first sensor, however, outputs a maximally-blurred image in this situation – contributing a low contrast noise signal.

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At distances greater than six inches, the image output by the second sensor becomes increasingly blurred – reducing the net sharpness of the combined output signal.

As the object distance approaches infinity, the sharpness of the image output by the first sensor increases – until its maximum value at infinity. Again, a low contrast noise signal is contributed by the other (second) sensor, which outputs maximally-blurred imagery for an object distance of infinity.

The just-discussed principles can be extended to any number of stacked photosensor arrays. Fig. 4 shows an arrangement employing three arrays. Again, the top and bottom sensors are positioned to capture focused images from objects at distances of infinity and six inches, respectively. However, the Fig. 4 arrangement includes a third sensor array positioned to capture focused imagery from objects at a distance of two feet.

The design of this third photosensor array can be similar to that of the top array, e.g., transmissive of part of the incident light (e.g., 75%). In this arrangement, approximately 50% of the incoming light is absorbed before being passed to the CMOS sensor at the bottom of the stack.

This arrangement produces a curve akin to Fig. 3A, but with three humps rather than two.

It will be noted that the third photodetector array in Fig. 4 is closer to the top sensor than the bottom sensor. Yet the top two sensors collect imagery from the largest range of focal distances, i.e., two feet to infinity. This is a consequence of the lens equation.

Figs. 5-8 illustrate still other stacking variants. Fig. 5 shows four sensor arrays. Like Fig. 4, the spacing of the arrays within the stack is non-uniform.

Fig. 6 shows a stack of five sensor arrays – this time with uniform spacing through the stack.

In some arrangements, such as Fig. 7, the sensors can be spaced in a random fashion.

Fig. 8 illustrates that in all such stacked-sensor embodiments, precise alignment of the sensors is not required. Any mis-alignment between sensors can be detected after fabrication (e.g., by analysis of test imagery), and compensated-for in post-processing.

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Nothing has yet been said about color. The human eye is much more sensitive to luminance (brightness) than color. Accordingly, color typically needn't be resolved as finely as luminance for most purpose. (For example, an image sensor with a million photosensor cells may produce only 250,000 samples of red information, and a like number of samples of blue, using a Bayer color filter.)

In the embodiments of Figs. 3 – 8, the bottom photosensor in the stack can employ a Bayer color filter for sampling red, green and blue at different photosites. The upper sensors can include a regular or random distribution of color filters as well, which may be sparse (i.e., some photosites have no filter).

Fig. 9 shows one form of sparse, regular color filter array, which may be tiled across the top image sensor in Fig. 3, or across the top and intermediate image sensors in Fig. 4. (In the latter case, the color filters on the sensors may be spatially staggered relative to each other.) In the depicted color filter array – as with the conventional Bayer pattern – green is sampled twice as frequently as red and blue. A variety of other such patterns, including some that are denser and some that are sparser, are straight-forward to implement.

In a variant embodiment, the component stacked photosensors can produce color information through use of Foveon-like technology. However, if a conventional Foveon sensor is used top the stack, then no light would penetrate to lower layers. One approach is to fabricate a sparse array of Foveon sensor pixels – interspersed with clear pixels. This enables passage of some of the incident light through the clear pixels to lower layers.

Second Class of Embodiments

The arrangements detailed above involve, conceptually – if not necessarily physically, a mechanical configuration of parts. In more sophisticated embodiments, a stacked photosensor structure is achieved in integrated fashion, using familiar semiconductor fabrication techniques (deposition, masking, lithography, doping, etc.).

Returning briefly to Fig. 1, imagine that each of the layers P1 – P8 is a volume of a semiconductor material, into which one or more photosensitive regions has been formed. Such an arrangement is shown in the exploded view of Fig. 10, in which the

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SAMSUNG EX. 1002 - 4012/4148

photosensitive regions (sometimes terms photosites) are shown by ovals. Physically, these ovals are three-dimensional in character – akin to M&M candies in configuration – encompassing a junction between a P-doped region and an N-doped region, and a depletion zone through which photo-electrons can be routed for collection (e.g., to charge-accumulating capacitors – not shown).

(In a different arrangement, the depicted ovals are physically realized by component structures that extend a greater distance in the vertical direction than in the horizontal.)

This second class of embodiment permits the size and placement of the photo-electron generating and collecting structures to be tailored as desired, e.g., to optimize quantum efficiency, achieve particular sampling objectives, etc.

For example, within the various layers along the Z-axis, the photosites can be spatially staggered (i.e., in the X-Y plane) to limit vertical occlusion of one by the other.

Fig. 11A shows one pattern of photosites – looking down through the stack along the Z-axis. (Only five photosites are shown, for clarity of illustration.) The photosites are symmetrically spaced within the X-Y boundaries of the stacked column. If each photosite absorbs 100% of the photons propagating vertically down through the stack that encounters the site, the depicted Fig. 11A arrangement would absorb 68% of the total electrons. That is, 68% of the X-Y area is occupied by photosites.

Other arrangements can, of course, be employed. Fig. 11B shows that the photosites in the different layers can be placed in random fashion in X-Y. Although this leads to lower quantum efficiencies, the stochastic sampling thereby effected has other desirable properties.

The photosite regions needn't be circular in aspect. Fig. 11C shows how hexagonal photosites can be employed – yielding still greater photon capture and efficiency.

In a particular arrangement, the Fig. 10 stack is 10 microns on a side, and the photosites have diameters of 1.75 microns. The total stack depth depends on the desired focal range; a stack depth of 100 microns is exemplary. (This roughly corresponds to a common smartphone configuration, which uses an f2.0 lens, spaced 3.85mm from the sensor array, and provides a focus range of six inches to infinity.)

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Continuing with the M&M analogy, the photosites may be of different colors. More accurately, they may have different spectral responses. A simple starting point is to provide each photosite with either a corresponding red, green or blue filter, so that it responds to photons only of the associated wavelength.

While that's a simple conceptualization of the idea, placement of color filters within an integrated circuit complicates its fabrication. Another approach to making different photosites responsive to different spectra is by the phenomenon popularized by Foveon – doping the semiconductor so that photons of different energies are more likely to penetrate to (and be detected in) different depths of the photosensor structure. Different doping can be used in different of the Fig. 2 stacks, so that across a given X-Y plane of the structure, different regions are attuned to different light frequencies. (That is, at a depth of 56 microns, not all photosites are maximally responsive to the same wavelength of light.)

Still another approach to making different photosites respond to different spectra is through use of dichroic mirrors or filters. Put simply, a frequency-selective mirror (thin film-based) can be fabricated under a photosite. If a quantum of light passes the photosite without dislodging a photo-electron, it next encounters the thin film structure. The dimensions of this structure are chosen to induce a reflection of certain wavelengths of light. Such light is reflected back towards the photosite it just passed (i.e., vertically, up through the stack) – giving this quantum of light a second chance to kick a photo-electron out of the semiconductor material in that photosite.

Yet another approach to realizing photosites having different spectral selectivities is through use of quantum dot material. Work at MIT's Tisdale Lab, at Delft University, and Invisage, has demonstrated use of quantum dot and film materials in image sensors. Related work is detailed, e.g., in Prins et al, Fast and Efficient Photodetection in Nanoscale Quantum-Dot Junctions, Nano Letters, Vol. 12, No. 11, October, 2012, pp. 5740-5743; Konstantatos et al, Solution-Processed Quantum Dot Photodetectors, Proc. IEEE, Vol. 97, No. 10, pp. 1666-1683, October, 2009; and in patent publications 7,476,904, 20070132052, 20110101205, 20110226934, 20100187404, and 20130032782.

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SAMSUNG EX. 1002 - 4014/4148

A particular implementation employs quantum dot material to transduce photons in the visible region into a short burst (e.g., nanosecond-scale burst) of electron/exciton energy, which is then measured and correlated to wavelength of the existing photon.

In one illustrative embodiment, such quantum dot transducers (with a scale of 2 – 20 nm) are distributed in a sensing volume 100 microns in thickness. Each quantum dot effectively serves as a photon-transduction pulser, with the pulse size (strength) correlating to incoming photon wavelength (i.e., color). Depending on implementation, there may be thousands of such dots per square micron through the device. The pulses may be quantized (desirably near the sites) to 6- or 8-bits of resolution.

While imaging science has long been fixated on tri-color systems (red/green/blue, and cyan/magenta/yellow), such arrangements optically pale in comparison to the capabilities of the human vision system. Better is to employ a richer spectral vocabulary. Thus, the spectral responses of the photosites employed in the present technology desirably are of more than three types (although in certain embodiments, single-, two- or three-spectral responses can be used). Four is on the low side. Different spectral responses numbering eight or more are be preferred.

In this regard, reference is made to published patent application 20130308045. It details, e.g., how multiple different (sometimes complex) spectra can be used to illuminate an object, so as to permit the object's spectrometry to be assessed more accurately than is possible with conventional R/G/B technology. In like fashion, use of multiple different spectral sensitivities by different photosites in the present technology similarly enables color imaging that exceeds the limitations of traditional tri-color systems.

Five years from now, smartphones desirably will include both the technology detailed in the just-cited application, and the sensor technology detailed herein.

Returning to and stretching the M&M analogy a bit, the electrons collected by the various photosites need to be routed for collection – typically by charge-storage capacitors (which may be formed at the bottom of the sensor array – beneath the last photosensitive regions). This routing can be effected by conductive electrodes (vias) that pass – typically vertically – through the integrated structure. In some implementations, these conductive electrodes are bundled – forming trunk-like structures. In such case, the

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SAMSUNG EX. 1002 - 4015/4148

M&M photosites may be regarded as leaves on branches (horizontal electrodes) that extend from this vertical trunk.

Transparent electrode materials can be used to limit absorption of light within the bulk of the structure. Nanowires can be employed for the vertical vias in the photosensor array. (See, e.g., Fan et al, Electrical and Photoconductive Properties of Vertical ZnO Nanowires in High Density Arrays, Applied Physics Letters, Vol. 89, No. 21, 2006; and patent publications 20070155025 and 20110315988.)

Figs. 12A and 12B illustrate the concept of such a tree. The trunk (comprising plural conductive vias) is represented by the darker vertical line. Photosites are coupled to the component electrodes of the trunk, for routing of their photo-electrons to charge-storing capacitors. Fig. 12A shows a regularly-arranged configuration. Fig. 12B shows one with more randomness.

These figures, of course, show only two dimensions. It will be recognized that additional photosites can exist in the third dimension, and can be similarly coupled to the tree trunk.

Note, too, that the number of photosites in each layer of the tree can be different. The photosites within any X-Y layer needn't be regularly and uniformly distributed. Some regions of a layer may be locally dense with photosites, while others can be relatively sparse. As with other design choices, application constraints will commonly dictate such details in any particular embodiment.

Although not shown in Fig. 10, a conventional image sensor (e.g., CMOS or Foveon) may be formed – or affixed – at the bottom of the integrated photosensor stack, to collect any remaining photons not transduced by the photosites throughout the volume.

Returning to Fig. 1, the illustrated light rays captured from nearby "Object 2," and focused by the lens down into zone P7, first pass through all of zones P1 – P6. The artisan will recognize that such light can kick-out photo-electrons in any of these zones P1-P6, on its way to P7.

Moreover, while the light rays converge in zone P7, they may pass through even that zone, and end up kicking-out photo-electrons in zone P8.

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SAMSUNG EX. 1002 - 4016/4148

Thus, all of the component zones may output electron charge due to light from Object 2. However, the electron count produced by zone P7 will exceed that from any of the other zones, due to the increase in the electric field near the focal zone.

Further Information on Blur and Sampling

Additional technical insight into the present technology may be gained by examining the important difference between what is popularly called "blur" on the one hand, and what may be called Explicit Angular Sampling, or just angular sampling.

One might say that blur is a physical phenomenon that has rather strict "depth of field" implications – primarily driven by the classic f-number of a lens being used, while angular sampling happens to be a core design principle of most embodiments of this technology, and helps explain why classic depth of field challenges can be overcome.

It is exceedingly well known in signal sampling theory and practice that the discrete sampling of a signal (one dimensional, two, or even three) needs only be slightly finer that the local undulatory properties of a signal (expressed deliberately in lay terminology to make the point). More colloquially, if it wiggles, sample it at three to five points per wiggle, and you should be fine. More technically, whereas Nyquist suggests that taking only two discrete samples per cycle of the highest frequency of a signal may suffice, engineering practice suggests a slight "oversampling" of a signal is desired for good measure, as it were.

Keeping the underlying issues still high-level (intuitive and even slightly pedestrian if the reader is a trained optical engineer), let us look at a simple scenario: a 4 millimeter focal length smart phone camera with an f2 aperture, or 2 millimeter aperture. We can further assume that the best focus "spot size" for a focused point is 2 microns. Simple ray-theory depth of field arguments tell us that for every 4 microns a sensor travels away from the "best focus" plane, the spot size will grow by 2 microns. Thus by 10 microns or so out of focus, the "spot size" of a point has grown to 5 microns. Optical engineers may rightly cringe at this over-simplification of "depth of field," but please tolerate the desire here to just point out that "blur" can happen very easily in modern smart phone cameras even with 10 to 20 micron out-of-focus conditions. 10 to 20 microns matter.

SAMSUNG EX. 1002 - 4017/4148

So continuing on with the pan-audience ray-trace storyline, once a typical f2 lens and planar-sensor is say 40 microns "out of focus," the "blur circle" as it is often called has grown to be 20 microns, 10 times worse than the pristine 2 micron tight-focus capability of the lens. Wiggle-wise, wiggles with ten times less detail need only have ten times sparser sampling, hence any pixels at 2 microns are ludicrously oversampling these "blurred" signals at this out-of-focus plane. In a nutshell, the conventional planar approach to image sampling inherits this rather stark depth-of-field phenomena and the culturally-ingrained idea of focus and blur (lack thereof).

Enter the third dimension of a sensor and the simple notion of sprinkling photosites at various depths inside a sensor, rather than simply in one plane (or three thinly packed planes for color sampling a la RGB and Foveon). In short, distribute 2 micron-ish photosites at various depths of a sensor from the front surface all the way to the furthest optically active surface, typically over a 100 micron thickness at least for a smart phone camera (4mm, f2 or f2.8). As noted, give these 3D splayed photosites various spectral selection properties while you're at it, no need to rigidly adhere to RGB models only (though adhering to these models is acceptable as well).

Nature's Teachings: Light Detection is a 3D Quantum Affair, not a 2D Sampling

Nature has provided us the examples of the faunal retina and the floral chlorophyll for study of light to energy transduction in general. Let's roll with that.

The closest engineering approach perhaps would be to view pixels not as photosites per se, but as micro-waveguides very much borrowing on rod/cone principles and chlorophyll-molecular-chain principles for more efficient photo-electron production. The 10 micron by 10 micron vertical cell cavity arrangement (Fig. 10) with "trees" of active photosites are near the same physical scale as single-mode optical fiber, and thus lend themselves very well to electromagnetic field modeling in the extreme details of semi-conductor and/or "nanotech material deposition" engineering of both the vertical structures as well as the individually active photo-electron generation sites.

Another well-known prior art which is general 2-dimensional in its primary application, but can be adapted easily to three dimensions, is the "dichroic filter." As noted, controlled layering of differing substances with differing optical densities,

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SAMSUNG EX. 1002 - 4018/4148

especially at the 1-2 micron scales of the optical photosites, can be an extra widget in the design toolbox as the spectral selection properties of these photosites is determined.

Moveable Sensors

In accordance with a further aspect of the present technology, a sensor in a smartphone or other such video camera system is disposed on a moveable mount, permitting motion of the sensor relative to the rest of the optical assembly (e.g., the lens).

Moveable lenses, sensors, and camera mounts have previously been employed for mechanical image stabilization, and such teachings can be employed in embodiments of the present technology. But the aim of the present technology is somewhat different.

For example, prior art mechanical image stabilization, as used in video cameras and film motion picture cameras, has largely sought to keep static features of a scene at consistent locations, frame to frame – despite unintended movement of the camera (e.g., caused by hand jitter).

When a video camera is moved in a deliberate fashion, e.g., in a panning motion, then arrangements like that marketed under the Steadicam brand are sometimes used to stabilize the camera mount (i.e., the lens and sensor together). This type of stabilization tends to isolate the camera from the operator's undesired, high frequency, movements. More uniform motions, however, such as panning, are not counter-acted by such arrangements.

Contemporary versions of Steadicam-like arrangements employ MEMS-based rate gyrosensors mounted to a gimbaled camera rig, to measure the angular rate of the camera's rotation. Signals from these gyrosensors are used to drive DC servomoters, coupled to the camera's rotational axes, to effect compensatory motions.

The present technology again contemplates panning, or other deliberate movements of the camera. But instead of mitigating motions that are ancillary to the desired movement (as with the above Steadicam-like arrangements), the present technology acts in concert with the desired movement, to reduce frame motion blur caused by such desired movement.

Consider the case of a pan (i.e., a rotation of a video camera around a vertical axis), in which the video camera captures a frame of imagery every thirtieth of a second.

SAMSUNG EX. 1002 - 4019/4148

(The exposure interval of each frame may be 30 milliseconds, and 3.33 milliseconds may elapse between frame exposures.)

If the camera is panned at a rate of six degrees per second, then each successive frame depicts a view through the lens that is advanced, relative to the prior frame, by an increment of 0.2 degrees. This horizontal change in the viewed scene causes an apparent movement of fixed image features across the sensor, also in a horizontal direction. If the camera lens has a field of view of 30 degrees, and projects the imaged scene onto a sensor having 480 columns of pixels, then each degree of view corresponds to 16 columns. From one frame to the next, the 0.2 degree change in camera orientation corresponds to a horizontal shift of about 3 columns of pixels.

In accordance with one embodiment of the present technology, a MEMS or piezo-electric actuator linearly shifts the camera sensor a horizontal distance of 3 pixel columns during the exposure of each of the frames – to counteract the panning-induced movement of the image on the sensor during that exposure period. At the end of the exposure period, the actuator quickly re-traces its travel in an opposite direction, to prepare for exposure of the next frame. This process repeats for each frame, so that the sensor alternately tracks the movement of the panning image, and then pops back to its original position. This operation may be termed a "track-pop" cycle.

Fig. 13 shows the movement of the camera sensor in a horizontal dimension as a function of time. The illustrative sensor has a horizontal dimension of 4.8 millimeters, so that each pixel row is 0.01 millimeters across (i.e., 10 microns). During the course of a single exposure interval, the sensor is moved three pixel rows, or 30 microns. In the brief inter-frame interval, the actuator pops quickly back to its original position.

Fig. 14 (not to scale) schematically shows a section view through part of a smartphone. A lens is positioned above an image sensor. The exterior surface of the lens terminates at a threaded opening into which an accessory lens (e.g., for additional light capture, or for microscopy) can be installed. The lens may include an auto-focus actuator (not shown) that mechanically moves the lens towards or away from the sensor. (If an image sensor of the sort described earlier is employed, then such mechanical focus arrangement is not needed.)

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SAMSUNG EX. 1002 - 4020/4148

The sensor is mounted for movement by a MEMS actuator 132, which can translate the sensor towards or away from the actuator. The actuator may provide a range of motion of 50 microns, on each side of the sensor's nominal position (i.e., aligned with the lens.)

It will be recognized that the foregoing description is necessarily simplified, for expository convenience. In actual practice, for example, the sensor may be translated in two directions, e.g. in "x" and "y." Two actuators can be used for this function, or a single, 2D actuator, can be employed. (An example of the latter, using comb electrodes that are controllably excited to move optical elements in two dimensions, is detailed in patent 6,914,710.)

Horizontal panning was assumed in the foregoing example. More generally, the nature of camera movement (e.g., angular panning, linear translation, etc.), and associated movement parameters, are desirably sensed by one or more 3D accelerometers and gyroscopes. Camera movement data can also be discerned from image sensor data, e.g., by tracking movement of scene features in the camera's field of view. Signals output from one or more such sensors are provided to the device processor, which computes the direction, magnitude, and timing of sensor movements that are needed to counteract motion of the image across the sensor during a frame exposure. Corresponding control signals are then sent to the sensor actuator(s).

More particularly, movement of the camera and/or movement of dominant subject matter in a scene both give rise to gross lateral shifts of the light fields falling on a sensor. The dynamic X-Y re-positioning of the sensor attempts to track, as best as possible, the global average of this shift. Desirably, these shifts are sensed, and used to generate appropriate control signals.

One approach is to utilize the now quite ubiquitous MEMS gyroscopes and accelerometers in order to determine the general movement characteristics of a camera on a frame-by-frame timescale. If one infers that a scene is largely not changing, the drive signals applied to the MEMS actuators can simply be an inversion of these measured movements of the camera. A second approach, which can be utilized separately or in combination with the first approach, is to use acquired pixel data from the sensor itself to measure and infer "residual tracking motion," for lack of a better term. In other words, it

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SAMSUNG EX. 1002 - 4021/4148

is a known prior art to determine the direction and extent of "motion blur" in a given image, providing for a measured value which after two such frames of such motion blur, can be used to assist in forming the drive signals for the MEMS track-pop actuation signals.

While the foregoing technology is described with reference to linear translation of the image sensor, in other embodiments different sensor movements can additionally, or alternatively, be employed. For example, the plane of the sensor may be tipped and/or tilted, so that its surface normal is non-parallel to the axis of the lens. Similarly, the sensor may be twisted (rotated) along its surface normal axis.

It will be recognized that the physical movement of the sensor needn't precisely counteract the movement of the image projected onto the sensor. Any similarity between such motions is an improvement over none. Likewise, while the exemplary embodiment included a 3.33 millisecond interval between exposures, during which interval the sensor popped back to its original position, this is not essential. The pop-back of the sensor to its original position can occur during the exposure. Due to the brevity of such movement, and the relatively small distance traveled, the consequent impairment of image quality may be acceptable in certain applications.

Additional Details re Light-Field Tracking MEMS

Companies such as Digital Optics Corporation and Tessera Technologies, Inc., among others, currently commercially supply MEMS-based Auto-Focus (AF) devices which provide the Z-axis displacement mechanism between a lens and a 2D sensor. As noted, aspects of the present technology posit use of such MEMS devices to also mechanically actuate motions in both the X and the Y direction: sensor plane relative to the plane of the lens. That is, the sensor would controllably shift at near 1-micron-level resolution relative to the parallel planes of the lens and sensor.

Current MEMs AF device specifications are nicely close to the specifications useful required for track-pop imaging cycles. In particular, full range actuation distances approaching 100 microns or even more are desirable, as will be discussed. Likewise, half-range movements in the single digit millisecond range and preferably even better are

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SAMSUNG EX. 1002 - 4022/4148

desirable, though as will be seen, a track-pop cycle program can be adapted to the specifications of whatever a given physical MEMS device can provide.

One aspect of track-pop cycling is to extend the prior art MEMS actuation from one axis to three. One way to do this is to do what many laboratory optical scientists do with much larger actuation stages than MEMS, and that is to simply bolt on a single actuation stage onto a second one but at an orthogonal manner, where the actuation of one stage moves the entire second stage along one given axis, then the second "riding" stage can then move a third body in some orthogonal direction, where that third body become yet a third MEMS actuation stage oriented "push axis" along the remaining orthogonal direction in 3-space (orthogonal to both of the first two stages). This long winded description mirrors the klunkiness and costliness of this approach, but it is important to note that this solution will unequivocally work.

A preferred approach to building 3-axes MEMS devices is to drive toward "close" to the same packaging form factor and dimensions of the current class of AF MEMS devices. The micron-level comb and spring structures currently laid out on nicely planar structures for 1-D AF have to "break the plane" at least in a higher level of assembly, if not at the raw manufacturing level. (In other words, individual one-axis MEMS actuation likely will still be manufactured as a 1-D actuation-axis structure, but it will need to be more finely sliced up, twisted and then re-assembled orthogonally with its identical or nearly identical siblings (other uni-axis actuators). One approach to doing this is to start with a current Z-axis (focus axis) version of a MEMS actuator, and then "float" this stage on two separate rail tracks, the first rail track attaching the top MEMS (the AF stage) to an X-axis stage which is itself pushed and pulled along the rail axis, then below this stage there is a 90 degree rotated rail (from the first rail) which attaches the X stage to the Y stage, with the Y-stage then having a push-pull MEMS structure activating the two stages along the second rail. In this approach, the elegant thin form factor of current AF MEMS devices can be "thickened" outside of the critical optical aperture area and still allow for the seating of a lens in relatively close proximity to a sensor (typically only a few millimeters between the back of a lens surface and the front of a sensor surface).

Once a 3-axis arrangement is in place, whether a klunky version or an elegant and thin one, the operation of shifting a sensor in close "tracking" to a light field projected

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SAMSUNG EX. 1002 - 4023/4148

onto that sensor can take place. The specifications of range of motion and response time then become parameters for determining the detailed timing of track and pop imaging. In general, the maximum speed of a MEMS actuation, projected through the focal length of a lens and then onto a scene being imaged, represents the very fastest motion that a scene can move in front of a camera and still be "tracked" by the MEMS motion. Likewise, when a given "tracking" has reached its full motion extent on the MEMS device, a command to end an exposure can take place, then kicking off the "pop" cycle which pops the MEMS actuation back to the other side of its full range. (If a particular MEMS axis represents the "long motion axis" of the current movement of the camera, the other axis will have a "pop" generally not quite as long as its full range).

In such arrangement, individual exposures of "tracked frames" last as long as the full range stroke of the long-motion axis MEMS device. For intuitive grounding of the basic lens and motion parameters, one can imagine a lens with 3.75mm focal length and a MEMS device with 100 microns full range motion. This gives a projected shift of just about 1.5 degrees, which, if one were to be panning (rotating) a camera operating at 30 frames per second, indicates that objects can move up to 45 degrees per second before they start to have residual blur beyond what the tracking can handle. Those practiced in these arts understand this situation is radically more nuanced than this simple example but the "order of magnitude" of how MEMS' full ranges, response times, focal lengths, etc. all play together is important to intuitively outline. Let us not forget as well that the "pop" phase usually posits turning off the exposing activities of the main sensor as the MEMS actuator(s) pop the sensor back to a new tracking starting point, and thus this "pop" time can represent a significant loss of information gathering if MEMS devices are not manufactured with an eye towards fast (ideally faster than one millisecond) full range popping capabilities. Much slower times can easily be made operational, the cost is simply dead time for light gathering.

Figs. 15A and 15B further illustrate the foregoing. Two plots are shown: Fig. 15A shows MEMS actuator displacement of the sensor in the "x" direction, and Fig. 15B is a similar illustration but in the "y" direction. The two actuator waveforms are synchronized, so that the track and pop phases coincide. The "x" actuator travels +/- 30 microns around a nominal position (i.e., from 0 – 60 microns, centered at 30 microns).

SAMSUNG EX. 1002 - 4024/4148

The "y" actuator is operated to move the sensor a smaller displacement, +/- 10 microns around its nominal position. It will be recognized that a single control signal (a timing waveform) can be scaled and offset to generate both the "x" and "y" control signals.

In the illustrated arrangement, the "track" interval (i.e., the frame exposure interval) is 5 milliseconds, and the "pop" interval is 2 milliseconds. Pop intervals that are less than 50% of the track intervals are typically utilized, with more preferable values for the pop interval being less than 20%, 10%, or even less than 5% or 2% of the track interval.

Motion-Stasis-Motion

In accordance with a further aspect of the present technology, an operational mode of the camera is controlled in accordance with a camera gesture. In a particular embodiment, a user signals interest in a scene when a phone is swept along a path to a point where it is briefly held, after which the phone is swept back in a contrary direction. The position at which it is briefly held indicates the user's interest in the scene viewed by the camera from that position.

Data from the phone sensors (accelerometers, gyroscopes, and feature tracking by the camera) are processed to classify the phone as either being in a "motion" phase, or a "stasis" phase. Each phase is characterized by motion parameter thresholds. For example, the "motion" phase may be characterized by any movement at a rate greater than one centimeter per second. (Such velocity can be derived by integrating data from the accelerometer sensor.) Stasis may be characterized by movement at a rate less than 0.5 centimeter per second.

To sense the just-described gesture, the device processor starts by looking for an initial motion phase. When that phase concludes, a time window (e.g., two seconds) starts within which the processor looks for a stasis phase. If stasis is not sensed within that interval (e.g., if the device moves at between 0.5 and 1 cm/second for more than 2 seconds), then the classifier resets – again looking for an initial motion phase.

If a stasis phase is sensed, it must persist for a threshold interval, which may be bounded both by minimum and maximum values. For example, the minimum value may be a value greater than 0.1, 0.2, or 0.5 seconds. The maximum value may be a value less

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SAMSUNG EX. 1002 - 4025/4148

than 1, 2 or 5 seconds. If the device is held in a stasis phase for the required threshold interval, then the process next looks for a retracting motion.

A retracting motion is a second "motion" phase, but one in which the motion is in a direction contrary to the initial motion phase. This can be defined mathematically in various ways, but the concept is familiar: if the user takes the phone from a rest position, sweeps it to a stasis position, and then returns it to (or near) the initial rest position, then that latter motion is a retraction motion.

One algorithmic definition begins by defining a first axis, which is that of a first vector between the device's position at the start of the initial motion phase, and its position at the stasis phase. (The actual path might be curved, but the start and end points define a straight line.) A retraction motion is tested by attributes of a second vector: namely, that between the device's position at the stasis phase, and its position at the end of the second motion phase. If this second vector has a component – when projected onto the first axis – that is larger than its projection onto any axis orthogonal to the first axis, and is in a direction opposite to that of the first vector, then the second motion phase is a retraction motion.

Put another way, if the first motion defines a first direction, then the second motion should have a principle component that is oriented in a direction opposite to that first direction, if the second motion is to be classified as a retraction motion.

Image frames may be captured throughout these phases, at a video capture rate (e.g., 30 frames per second). Or, video capture may commence only after device velocity falls below a threshold, e.g., 1 cm/second (such as at the end of the initial motion phase), and may terminate when the device velocity again rises above that threshold (such as at the beginning of the retraction motion phase).

Data from plural such image frames are combined in known fashion to synthesize one or more enhanced images, e.g., increasing the resolution, or extending the field of view, as contrasted with any single captured image frame. Desirably, two or more such composite images are created (e.g., from different virtual viewpoints), and are presented to the user on the device display. The user can flip or scroll between the composite images, using known image review UI paradigms, and select one or more for long term storage (e.g., in the Photo Library or Camera Roll data structures of the Apple iPhone).

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SAMSUNG EX. 1002 - 4026/4148

Ideally, the frames of video imagery from which the images presented to the user are composited, are gathered using a sensor of the type earlier described, providing 3D information. In such arrangement, there is no focal plane – outside of which subjects are out of focus. Instead, everything in the composite image is in focus.

Review

A far-from-complete list of some of the inventive arrangements provided by this technology includes the following:

An apparatus having an optical array sensor for use with a lens, where the sensor comprises a structure having a vertical thickness of at least 10 microns, with plural photo-electron generating regions (photosites) dispersed at two or more layers within that thickness (corresponding to differing lens focal planes). Two of these layers are vertically separated by at least 10 microns.

In other embodiments, two of these layers are vertically separated by at least 50 microns. A particular such sensor is useful for sensing objects at distances from the lens ranging from less than ten inches, out to infinity.

In some such arrangements, the photosites are spectrally selective, and there are at least two different types of spectral selection. Commonly there may be four or more. Desirably, the photosites are transmissive to light for non-spectrally-selected wavelengths of light.

In one particular sensor, the structure has a thickness of more than 50 microns, comprises three or more different layers of photosites. These three layers correspond to objects imaged at respective distances of (a) less than 10 inches, (b) between ten inches and three feet, and (c) greater than three feet.

The above-noted sensor may be provided with a first CMOS sensor array atop said structure, which serves as an entry surface onto which light entering the structure is first incident. This CMOS sensor array may pass 25% or more of the visible incident light into said structure.

Similarly, the above-noted sensor may be provided with a second CMOS sensor array at a bottom of the structure, for receiving light that was not transduced to photo-electrons elsewhere in the sensor.

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SAMSUNG EX. 1002 - 4027/4148

In some arrangements, both of the just-referenced CMOS sensors are provided, thereby sandwiching the structure. In such a configuration, a first fraction of incoming light is transduced to electrons by the first CMOS sensor atop the structure, another fraction of incoming light is transduced to electrons by the photosites in the structure, and a further fraction of the incoming light is transduced to electrons by the second CMOS sensor behind the structure.

In another particular sensor, there are at least four differing depth layers for the photo-electron generating regions in the structure. Each of these regions comprises plural photosites, and an X-Y arrangement of the photosites in one of said layers is staggered relative to an X-Y arrangement of the photosites in a successive layer.

The just-described sensor may have a density of photosites such that 25% or less of incident light reaches a CMOS sensor array at the back of the structure.

The above-noted sensors may include photosites arranged such that a line normal to the thickness passes through a first photosite in one layer and a second, different photosite in a different layer. These first and second photosites are desirably differently spectrally selective.

The above-noted sensors can include a first gated conduction path that couples a first photosite to a first transfer capacitor, and a second gated conduction path that couples a second photosite to a second transfer capacitor, where the first and second transfer capacitors are optically shielded from incident light.

Such a sensor can further include control circuitry for alternately gating the conduction paths on and off plural times per second, to produce raw video signal charge streams to the transfer capacitors.

Smartphones equipped with the above-described sensors, and a lens, are also contemplated.

The technology also includes an apparatus having a stack of plural photodetectors P_1 - P_N and a lens. The lens introduces light onto a first exterior surface of the stack, for passage through the stack towards a second exterior surface of the stack. The stack positions different of the photodetectors at different distances from the lens, so that they provide dominant responses to light captured from objects at different distances from the

SAMSUNG EX. 1002 - 4028/4148

lens in accordance with the photodetectors' distances from the lens. A distance between photodetectors P_1 - P_N in the stack is at least 20 microns.

Another such sensor includes four or more light-detecting volumes P_1, P_2, P_3 - P_N arranged so that light detected in volume P_2 has first passed through volume P_1, light detected in volume P_3 has first passed through volumes P_1 and P_2, etc.. A distance between volumes P_1 - P_N is at least 20 microns, permitting the sensor to provide object distance information when used with a lens that directs light from an object onto the sensor.

In the just-detailed sensor, the light-detecting volumes can be arranged in a stack along a stack axis. A first of the volumes has a first photosensitive region, and a second of said volumes has a second photosensitive region. A line between centers of these first and second photosensitive regions is not parallel to said stack axis.

Put another way, if the light-detecting volumes are arranged in a stack along a Z axis in an X, Y, Z Cartesian coordinate system, each of the light-detecting volumes each has an extent in X-Y space. In such view, a first of the volumes has a photosensitive region at a first X-Y location, and others of the volumes have respective photosensitive regions at other X-Y locations that are different than the first X-Y location. In such an arrangement, a light ray traveling through the sensor parallel to the Z axis encounters different of said photosensitive regions, depending on the ray's location in X-Y space.

Another arrangement employs a video camera system (e.g., in a smartphone) that includes a lens coupled to a body, and an image sensor (lying in an image plane). A uniform motion of this system (i.e., a deliberate motion, as contrasted with an unintended motion – such as hand jitter, which may also be present) is sensed while capturing video imagery. This capturing of video imagery comprises capturing a still image frame N times a second. The uniform motion of the system results in a uniform movement of image features across the image plane. During this video capture, a uniform physical tracking movement of the image sensor, within the camera body, is repeatedly performed. This tracking movement of the image sensor is in a direction that tracks the uniform movement of image features across the image plane. Each such tracking movement is followed by a uniform popping movement, which returns the image sensor back to an

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SAMSUNG EX. 1002 - 4029/4148

original position that it occupied at the beginning of said uniform tracking movement. These tracking and popping movements are repeated N times a second.

In some embodiments, each of the uniform tracking movement has a first time duration, and each of said uniform popping movements has a second time duration, where the second time duration is less than 20% of the first time duration.

The tracking and popping movements of the image sensor can be performed by repetitively and synchronously operating a pair of orthogonally-oriented MEMS actuators.

Other Comments

It will be recognized that references to transparent materials simply refer to a material that does not block 100% of the light energy of interest. A material that intercepts 99% of the light, and passes 1%, is still regarded as transparent. (If only 0.001% of the light passes, it is no longer regarded as transparent. Between .001% and 1% is a range that may or may not be regarded as transparent – depending on the particular application being served.)

While the embodiments of Fig. 3, etc., contemplated that the component image sensors are of the same resolutions, this is not required. In other arrangements the sensors can be of differing resolutions.

The detailed embodiment employs CMOS semiconductor image sensor technology. However, the principles of the detailed arrangement can be applied to any other type of image sensor arrangement, whether presently known (e.g., CCD or organic photosensors) or later developed.

The number of different layers of photosites employed in a particular embodiment is application dependent. Although eight layers are illustrated in Fig. 1, a lesser number (e.g., 3 or 6, etc.) or a greater number (e.g., 9 or 20 or 32, etc.) can be used. If each of the layers is 12 microns in thickness, a stack of eight yields a total stack depth of about 100 microns. A thicker or thinner stack may be desired, depending on the focal length of the lens, and the range of distances from which object images are to be captured. (The stack may be made thicker by increasing the number of photodetectors, or by increasing their component thicknesses.)

SAMSUNG EX. 1002 - 4030/4148

The thicknesses of the photosites can be non-uniform, e.g., in acknowledgement that the photon flux deeper in the structure is diminished by photon absorption in higher layers. Alternatively, or additionally, the gains of the corresponding output amplifiers can be non-uniform – with those driven by photosites deeper in the structure having higher gains than those associated with photosites closer to the lens. Still further, the doping of semiconductor structures in deeper photosensors can be different than the doping of corresponding semiconductor structures in higher photosensors.

While a single lens L is shown in Figs. 1 and 3 for clarity of illustration, it will be recognized that plural lenses can be used, e.g., a compound lens, or a lens for each pixel, or a lens per group of neighboring pixels, or lenticular lenses, etc. Combinations can also be used, e.g., a single object lens, in conjunction with a plurality of microlenses, as is known in certain light field architectures.

The details of the photodetectors, and their respective charge accumulation, latching, switching and reset circuitry are not detailed, as same are within the skills of the artisan in photosensor design.

Applicant's published applications 20110212717, 20110161076, 20120284012, and 20130223673, detail methods and arrangements that are useful in combination with the present technology. Publication 20110212717, for example, teaches that post-processing of sensor data is desirably performed by processing circuitry on the same substrate as the sensing elements. In the present case, such processing circuitry can take the raw signals from the various sensors/photosites, and process them to produce data streams optimized for their intended use (e.g., one data stream optimized for rendering to a user on a screen, another optimized for recognizing text from close focal distances, etc.).

It will be recognized that multiple features are taught by this specification, and different particular embodiments have been detailed that combine different of these features. However, it will be recognized that the features can be combined in myriad arrangements, too numerous to catalog. This disclosure should be regarded as teaching all combinations of the disclosed features.

To provide a comprehensive disclosure without unduly lengthening this specification, applicant incorporates by reference the documents identified herein, as well

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SAMSUNG EX. 1002 - 4031/4148

as the documents they respectively reference. All such documents are incorporated in their entireties, as if fully set forth herein. The artisan is presumed to be familiar with the teachings from such references.

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SAMSUNG EX. 1002 - 4032/4148

Claims:

1. Apparatus comprising an optical array sensor for use with a lens, the sensor comprising a structure having a vertical thickness of at least 10 microns, with plural photo-electron generating regions dispersed at two or more layers within that thickness, said layers corresponding to differing lens focal planes, two of said plural photo-electron generating regions being vertically separated by at least 10 microns.

2. The apparatus of claim 1 wherein said structure includes first and second planar arrays of photodetectors, said first and second planar arrays being vertically separated by at least 50 microns, wherein the sensor is useful for sensing objects at distances from the lens ranging from less than ten inches, out to infinity.

3. The apparatus of claim 1 wherein the photo-electron generating regions are spectrally selective and there are at least two different types of spectral selection.

4. The apparatus of claim 3 wherein the photo-electron generating regions are spectrally selective and there are at least four different types of spectral selection.

5. The apparatus of claim 3 wherein the photo-electron generating regions are transmissive to light for non-spectrally-selected wavelengths of light.

6. The apparatus of claim 1 wherein said structure has a vertical thickness of more than 50 microns, and the sensor comprises three or more photo-electron generating regions at said differing layers, the three regions corresponding to objects imaged at respective distances of (a) less than 10 inches, (b) between ten inches and three feet, and (c) greater than three feet.

7. The apparatus of claim 1 that further includes a first CMOS sensor array atop said structure, serving as an entry surface onto which light entering the structure is

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SAMSUNG EX. 1002 - 4033/4148

first incident, said first CMOS sensor array passing at least 25% of visible incident light into said structure.

8. The apparatus of claim 7 that further includes a second CMOS sensor array at a bottom of said structure, said first and second CMOS sensor arrays thereby sandwiching the structure, wherein a first fraction of incoming light is transduced to electrons by the first CMOS sensor atop the structure, and a second fraction of the incoming light is transduced to electrons by the second CMOS sensor behind the structure.

9. The apparatus of claim 8 in which a third fraction of the incoming light is transduced to electrons by photo-electron generating regions in the structure between the first and second CMOS sensor arrays.

10. The apparatus of claim 1 that further includes a CMOS sensor array at a bottom of said structure, for receiving light that was not transduced to electrons elsewhere in the sensor.

11. The apparatus of claim 10 wherein there are at least four differing depth layers for the photo-electron generating regions in the structure, each of the photo-electron generating regions comprising plural photosites, wherein an X-Y arrangement of the photosites in one of said layers is staggered relative to an X-Y arrangement of the photosites in a successive layer, and wherein a density of the photosites is such that 25% or less of incident light reaches the CMOS sensor array at the bottom of said structure.

12. The apparatus of claim 1 wherein there are at least four differing depth layers for the photo-electron generating regions in the structure, each of the photo-electron generating regions comprising plural photosites, wherein an X-Y arrangement of the photosites in one of said layers is staggered relative to an X-Y arrangement of the photosites in a successive layer.

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SAMSUNG EX. 1002 - 4034/4148

13. The apparatus of claim 1 in which each of the photo-electron generating regions comprises plural photosites, and a line along a vertical axis passes through a first photosite in one layer and a second, different photosite in a different layer, said first and second photosites being differently spectrally selective, the sensor further including a first gated conduction path coupling the first photosite to a first transfer capacitor, and a second gated conduction path coupling the second photosite to a second transfer capacitor, the first and second transfer capacitors being optically shielded from incident light.

14. The apparatus of claim 13 that further includes control circuitry for alternately gating said conduction paths on and off plural times per second, to produce raw video signal charge streams to said transfer capacitors.

15. The apparatus of claim 12 comprising a smartphone equipped with said sensor and a lens.

16. An apparatus including a vertical stack of plural photodetectors P_1 - P_N and a lens, the lens introducing light onto a first exterior surface of the stack, for passage through the stack towards a second exterior surface of the stack, the stack positioning different of the photodetectors at different distances from the lens, the different photodetectors providing dominant responses to light captured from objects at different distances from the lens in accordance with the photodetectors' distances from the lens, a vertical distance between photodetectors P_1 - P_N in said stack being at least 20 microns.

17. A sensor comprising four or more light-detecting volumes P_1, P_2, P_3 - P_N arranged so that light detected in volume P_2 has first passed through volume P_1, light detected in volume P_3 has first passed through volumes P_1 and P_2, etc., wherein a distance between volumes P_1 - P_N is at least 20 microns, permitting the sensor to provide object distance information when used with a lens that directs light from an object onto the sensor.

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SAMSUNG EX. 1002 - 4035/4148

18. The sensor of claim 17 in which:

said light-detecting volumes are arranged in a stack along a stack axis;

a first of said volumes has a first photosensitive region therein, and a second of said volumes has a second photosensitive region therein; and

a line between centers of said first and second photosensitive regions is not parallel to said stack axis.

19. The sensor of claim 17 in which:

said light-detecting volumes are arranged in a stack along a Z axis in an X, Y, Z Cartesian coordinate system, said light-detecting volumes each having an extent in X-Y space;

a first of said volumes has a photosensitive region at a first X-Y location; and

others of said volumes have respective photosensitive regions at other X-Y locations that are different than the first X-Y location;

wherein a light ray traveling through the sensor parallel to the Z axis encounters different of said photosensitive regions, depending on the ray's location in X-Y space.

20. A method employing a video camera system, said system including a lens coupled to a body, and an image sensor, the image sensor lying in an image plane, the method comprising the acts:

sensing a uniform motion of the video camera system while capturing video imagery, said capturing of video imagery comprising the capturing of a still image frame N times a second, said uniform motion of the video camera system resulting in a uniform movement of image features across the image plane, said uniform motion being deliberate rather than unintended;

repeatedly performing a uniform physical tracking movement of the image sensor, within the body, in a direction that tracks said uniform movement of image features across the image plane, followed by a uniform popping movement that returns the image sensor back to an original position it occupied at a beginning of said uniform tracking movement;

wherein said tracking and popping movements are repeated N times a second.

SAMSUNG EX. 1002 - 4036/4148

21. The method of claim 20 in which each of said uniform tracking movements is of a first time duration, and each of said uniform popping movements is of a second time duration, where the second time duration is less than 20% of the first time duration.

22. The method of claim 20 in which said tracking and popping movements of the image sensor are performed by repetitively and synchronously operating a pair of orthogonally-oriented MEMS actuators.

23. A method comprising:

sensing a first movement of a camera-equipped device, the first movement defining in a first direction;

following the sensed first movement, sensing a pause in movement of the device; and

following the sensed pause, sensing a second movement of the device, the second movement defining in a second direction;

wherein said second direction has a principle component that is oriented in a direction opposite to said first direction;

the method further including:

capturing frames of imagery at least during in an interval between the first and second movements of the device;

processing a first data set, comprising plural of said captured image frames, to yield a first composite data set;

processing a second, different, data set, comprising plural of said captured image frames, to yield a second composite data set; and

storing the first and second composite data sets for user review and selection.

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SAMSUNG EX. 1002 - 4037/4148

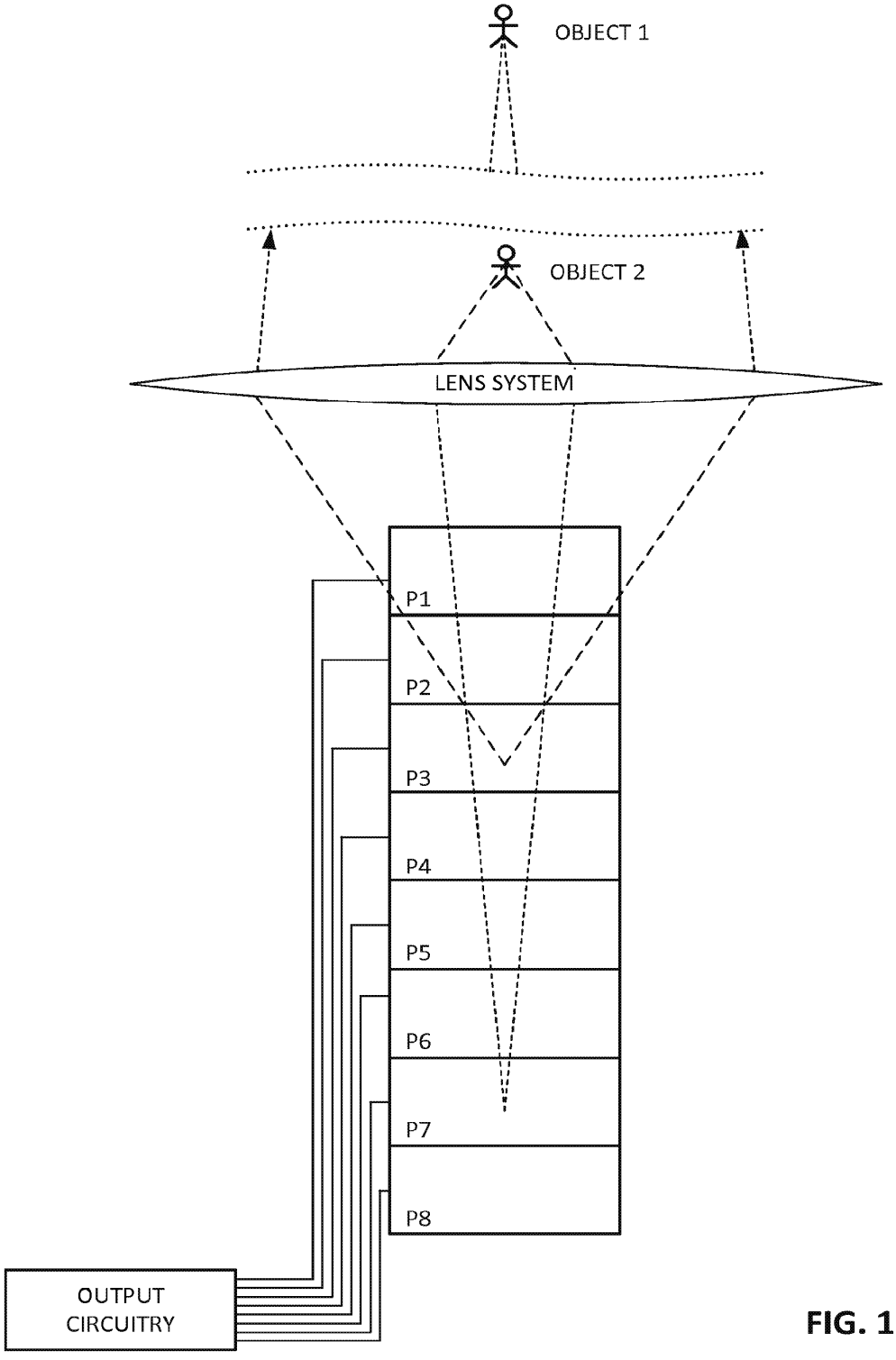

OBJECT 1
OBJECT 2
LENS SYSTEM
P1
P2
P3
P4
P5
P6
P7
P8
OUTPUT CIRCUITRY

FIG. 1

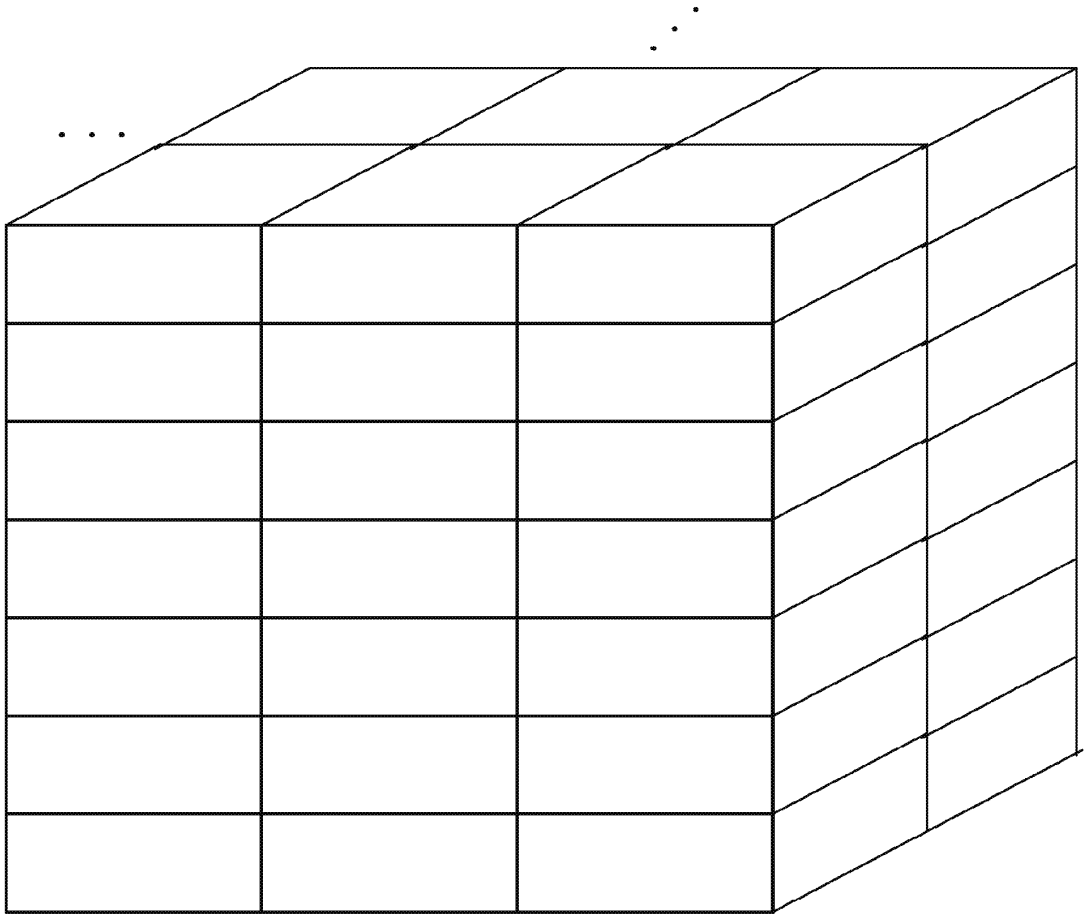


FIG. 2

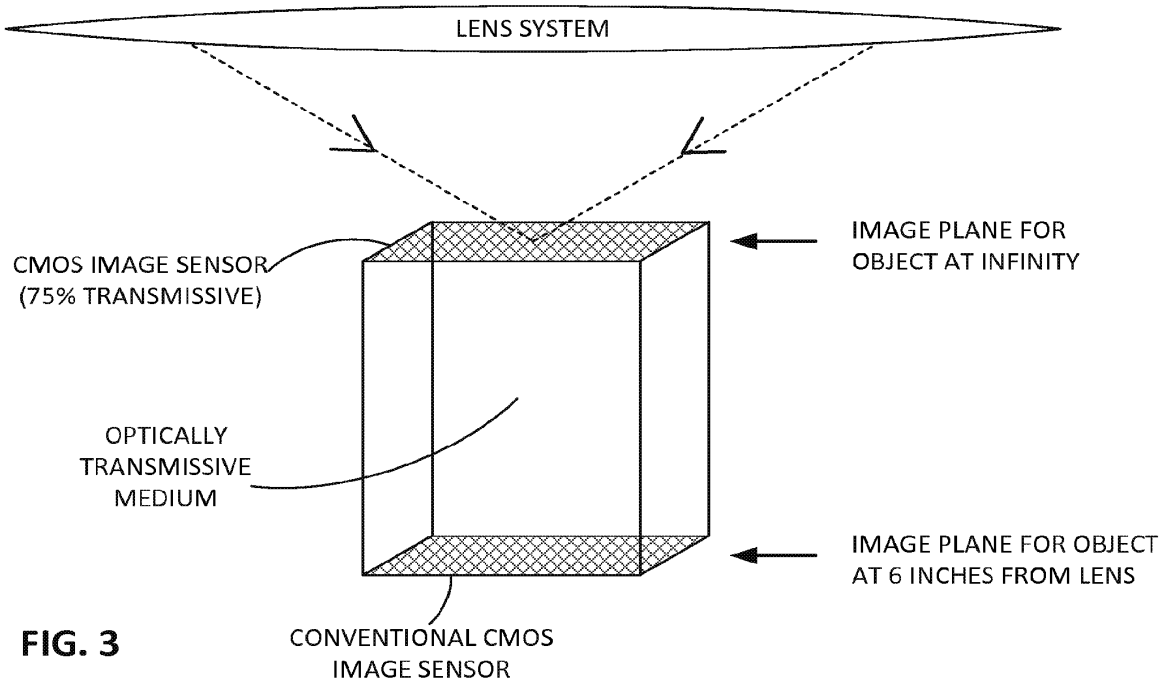


FIG. 3

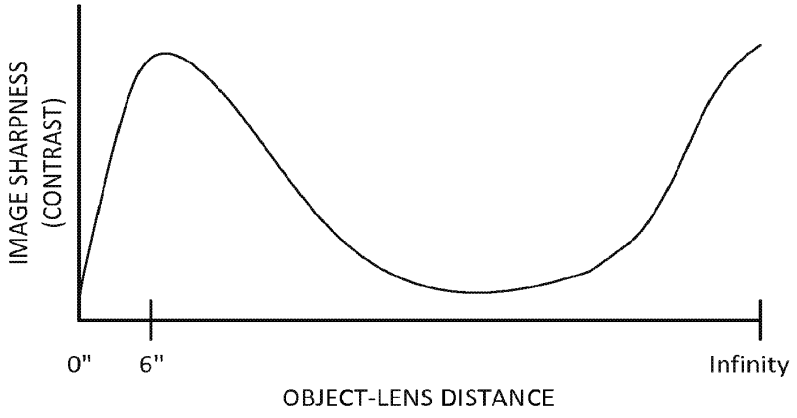


FIG. 3A

SAMSUNG EX. 1002 - 4040/4148

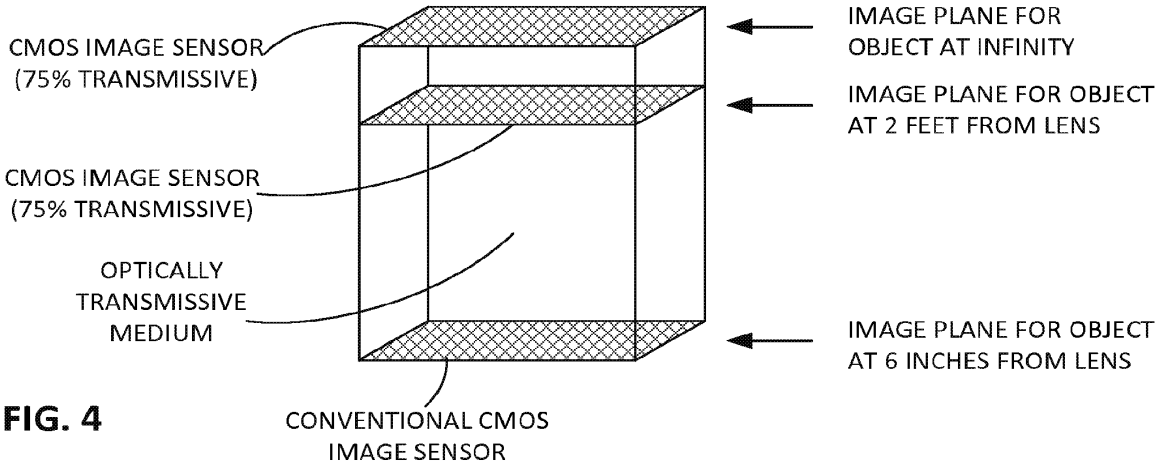


FIG. 4

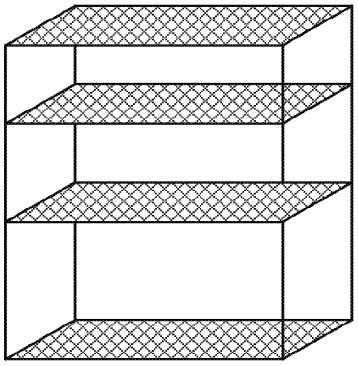


FIG. 5

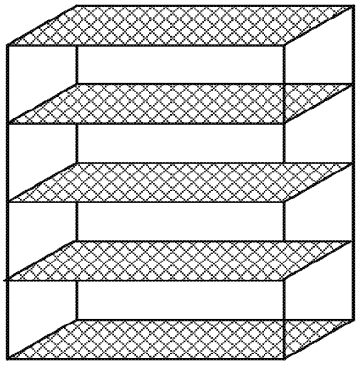


FIG. 6

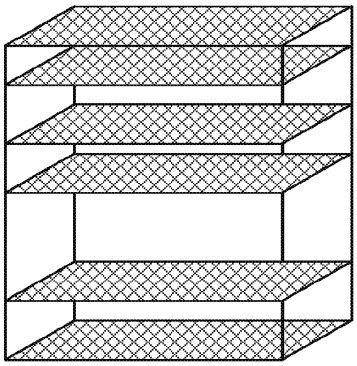


FIG. 7

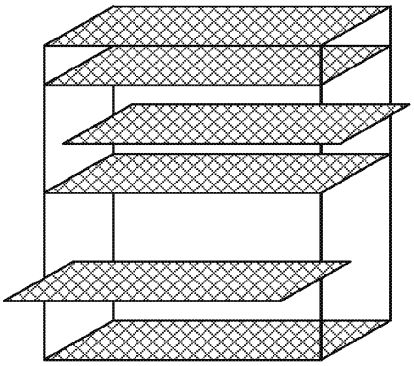


FIG. 8

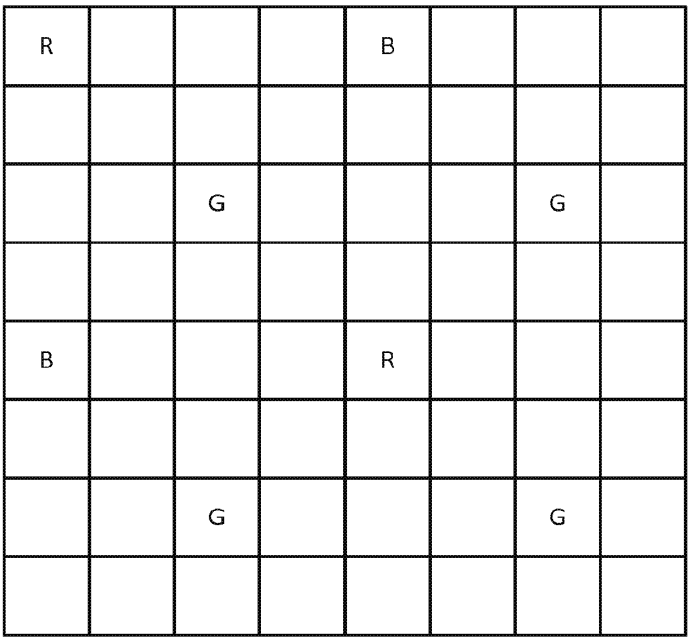


FIG. 9

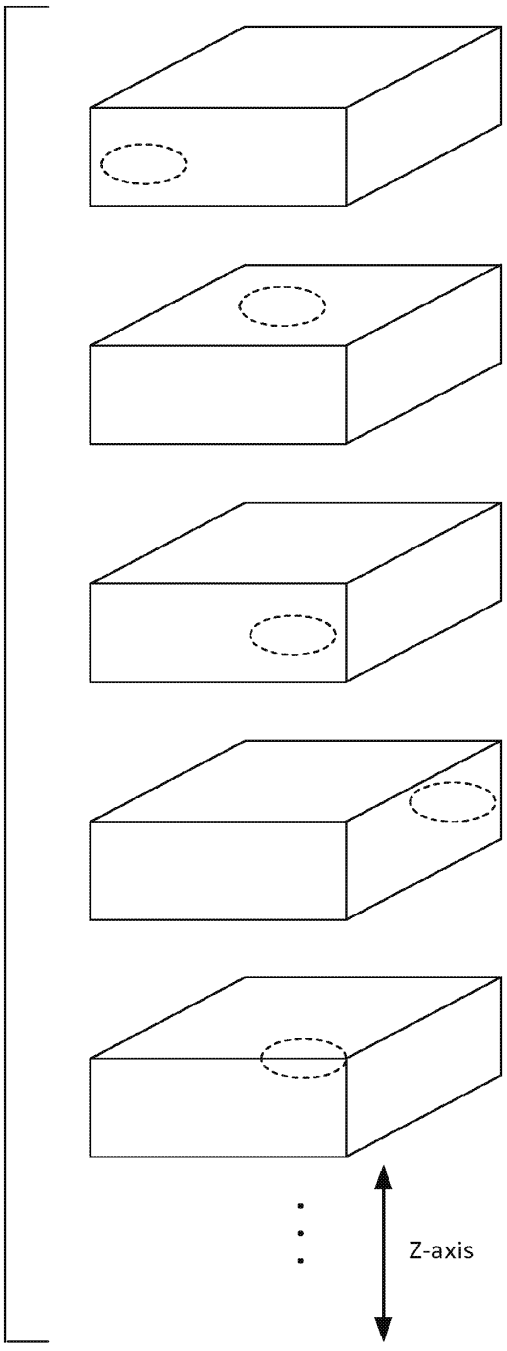


FIG. 10

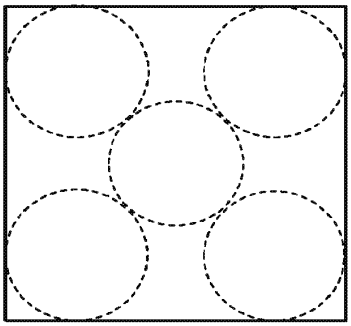


FIG. 11A

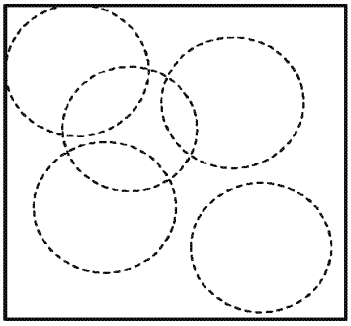


FIG. 11B

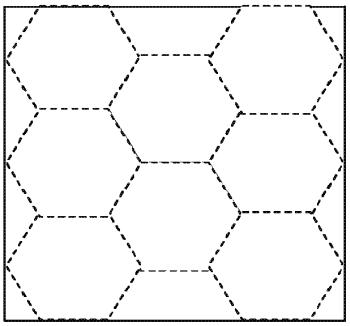


FIG. 11C

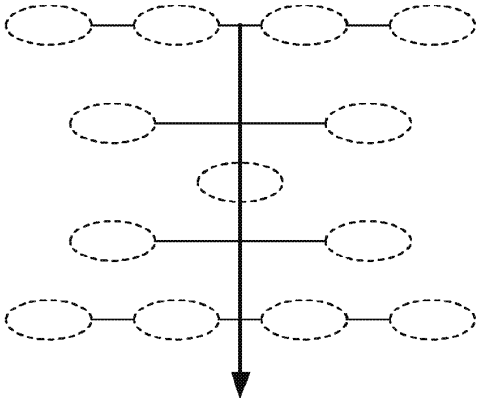


FIG. 12A

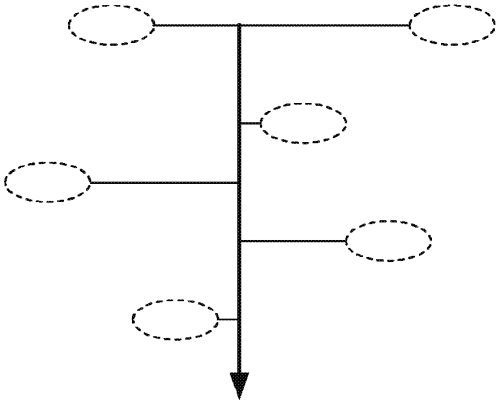


FIG. 12B

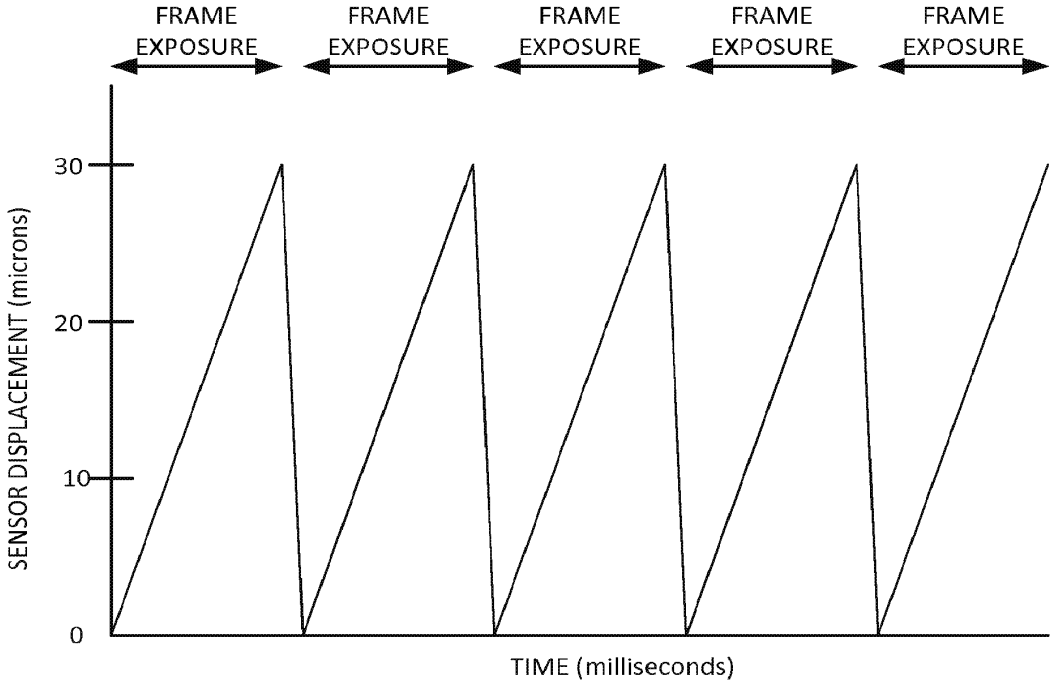


FIG. 13

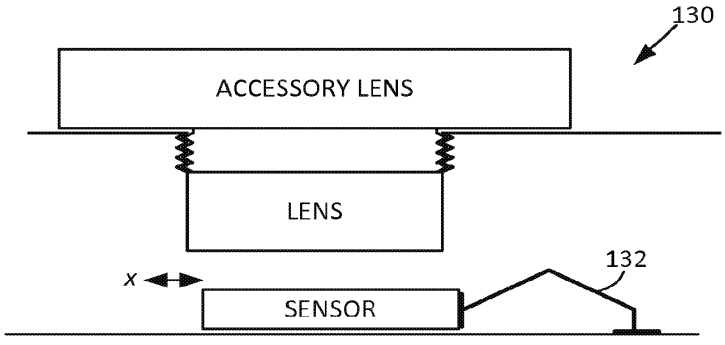


FIG. 14

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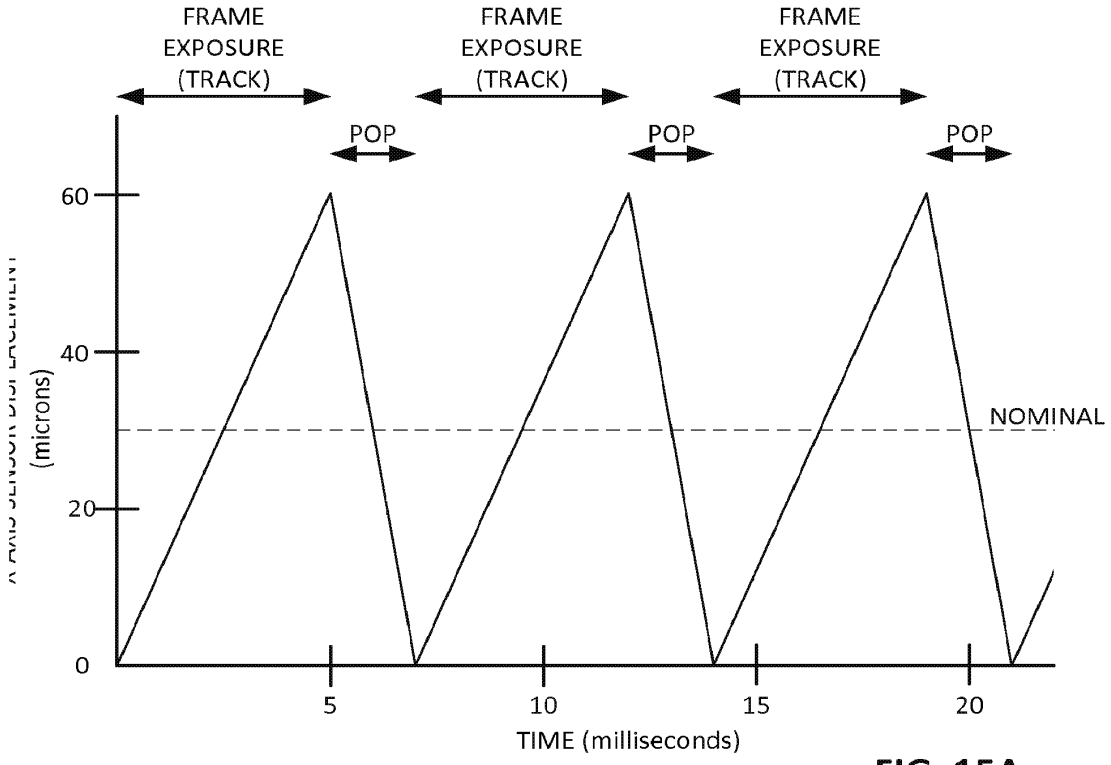


FIG. 15A

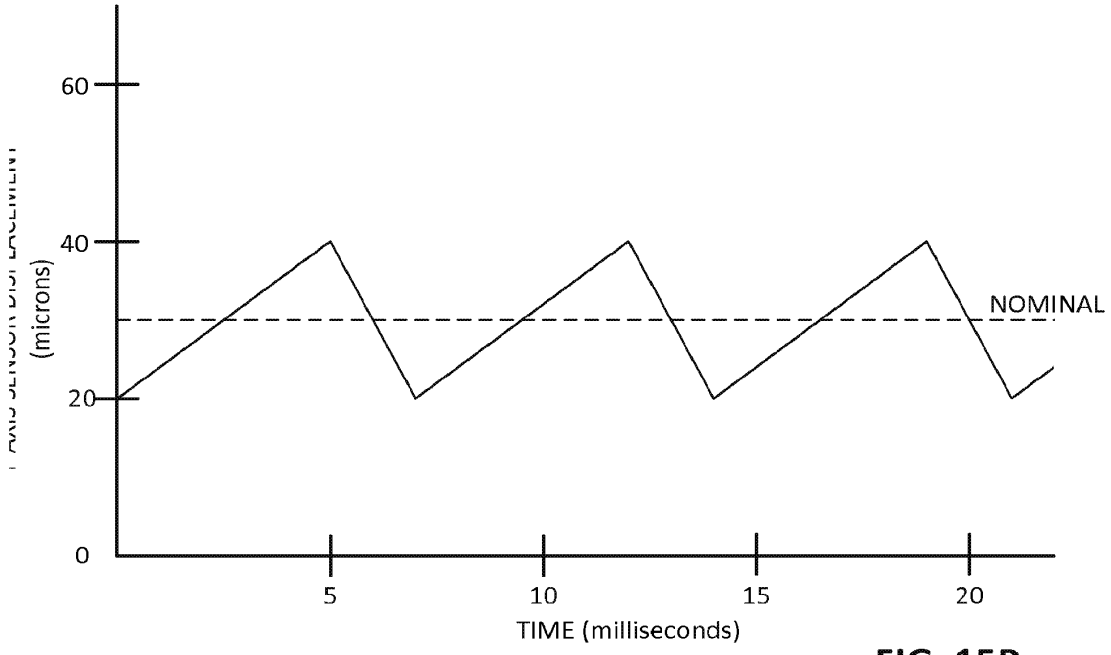


FIG. 15B

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Sensor/Camera Evolution

- Era 1: Analog Sensor, 1970 - 1990
  - A/D everything else off-chip
- Era 2: Digital CCD's & CMOS, 1990's early 2000's
  - Digital data, often compressed, exits chip
- Era 3: System on Chip Sensors, mid 2000's – present
  - Getting processing gates onto the sensor, still & video merging
- Era 4: Wafer-Level-Cameras late 2000's – present
  - Personal devices

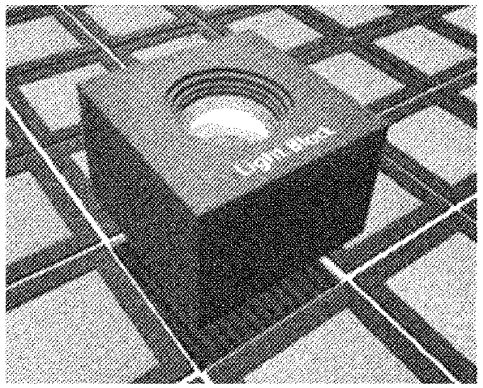


FIG. 16

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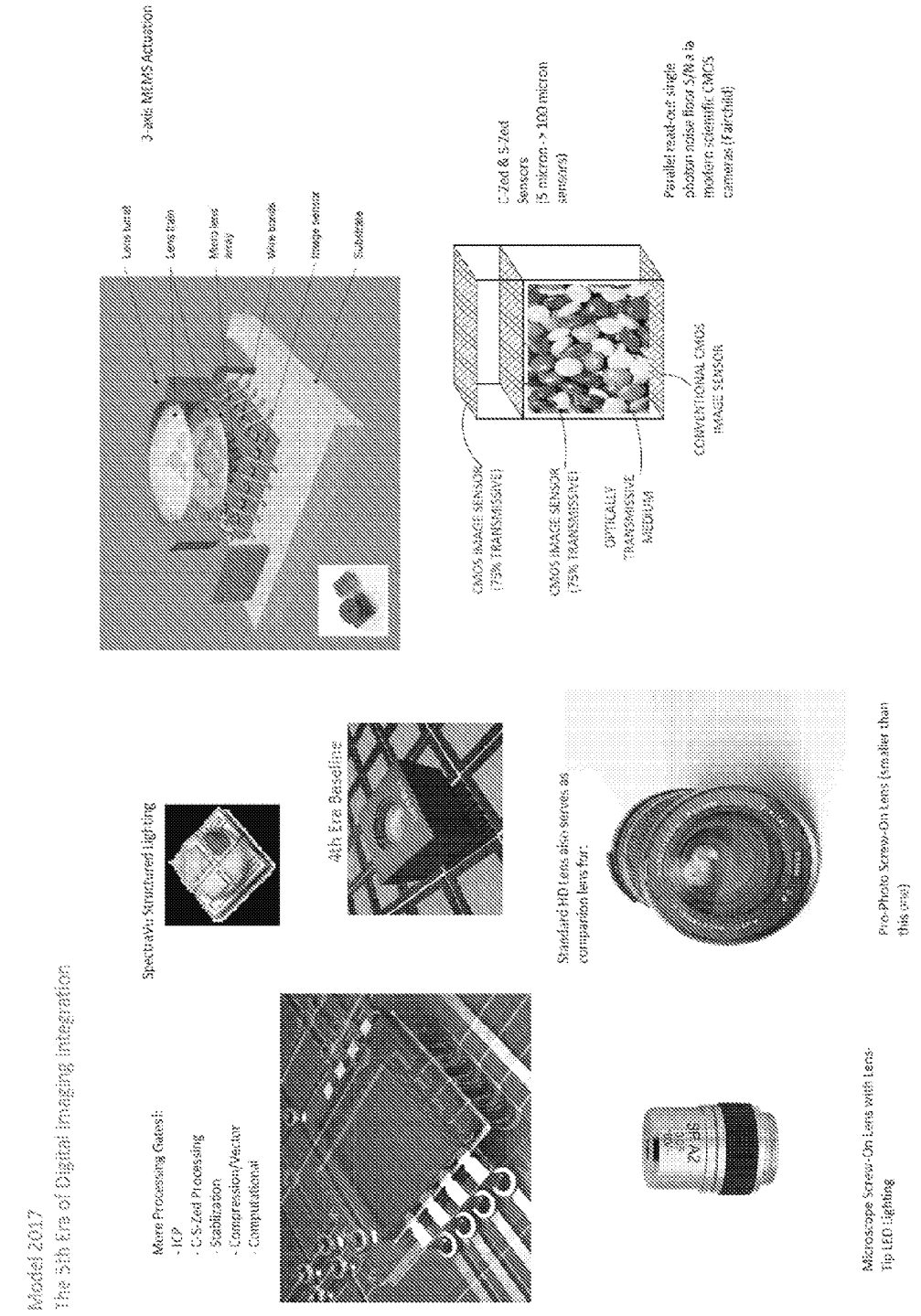


FIG. 17

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North-Holland

IN-SITU DOPING OF SILICON USING THE GAS IMMERSION LASER DOPING (GILD) PROCESS

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In this work we use built in diagnostic capabilities to demonstrate gas immersion laser doping (GILD) as an in-situ doping technique. A HeNe laser reflectivity apparatus measures the silicon melt time during doping, and our melt depth/diffusion simulation program, LASERMELT, is used to predict the silicon melt depth versus melt time. By combining these tools along with previously measured SIMS and RBS profiles, we obtain an accurate in-situ method of determining junction depths. LASERMELT also calculates the sheet resistance and the dopant profiles themselves. The ability to successfully determine these parameters in-situ, as well as fabricate ultra shallow junctions in a "low temperature" environment makes laser doping suitable for future ULSI processes.

1. Introduction

Very large scale integration (VLSI) and ultra large scale integration (ULSI) require a scaled reduction in both the lateral and vertical device dimensions in order to increase speed and packing density. In fig. 1 simple cross sections of a long channel and a short channel NMOS device illustrate a problem with scaling. Here we see that as the gate length, L, of the device becomes smaller for a constant source and drain junction depth, x_j, two problems will result: (i) the junction encroachment under the gate will become more significant, and (ii) the electric field due to the drain and source will become more and more significant in the channel. The junction encroachment can be controlled by suitable oxide spacer technology (see, for example, ref. [1]), but the two devices will only maintain the same electric field pattern in the channel region if the source and drain junction depths are decreased. For very shallow junctions, the device will return to the desired long channel behavior case in which the gate plays a dominant role in controlling the channel potential. However, as the junction depths decrease, the sheet resistance of the layers increases. This can lead to parasitic source and drain resistances that severely affect circuit speed, power consumption,

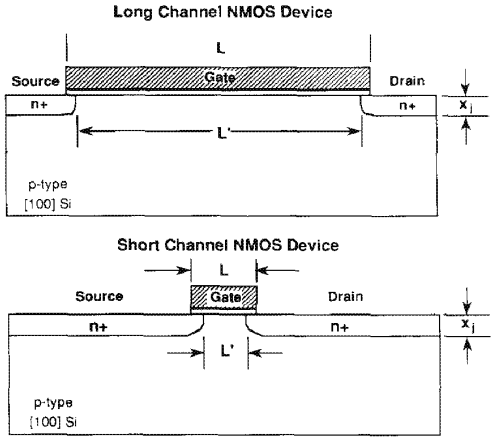


Fig. 1. Long channel and short channel NMOS devices. As L decreases for an constant x_j, the source and drain electrodes play a increasing role in the channel region by moving the electric field lines away from the device surface. Short channel behavior results because the gate no longer controls the majority of the channel charge. This problem is alleviated by reducing x_j so the two devices maintain the same electric field pattern.

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and logic swings. It is, therefore, clear why small geometry devices require shallow junctions with low sheet resistance values.

Shallow n^+ junctions for NMOS devices are routinely fabricated using low energy ^{75}As implants into Si. Unfortunately, for CMOS circuits a problem exists in fabricating shallow p^+ junctions with low sheet resistance because of the boron ion implantation tail [2]. The sheet resistance of a junction is inversely proportional to its depth, or

$$R_{\text{sheet}} = \rho / x_j, \tag{1}$$

where ρ is the resistivity given by:

$$\rho = \frac{1}{q(\mu_n n + \mu_p p)}. \tag{2}$$

Here n is the active electron concentration in the layer, p is the active hole concentration, and μ_n and μ_p are the electron and hole mobilities. It is clear that in order to make ρ and therefore R_{sheet} small for very shallow junctions, the electron concentration in the n^+ layers and the hole concentration in the p^+ layers must be very high. An example of this is shown in fig. 2 where R_{sheet} versus N_A is plotted for different values of x_j ranging from 0.05 to 0.2 μm. The data for this plot assumes that $N_A = p$, box-like profiles, and negligible electron concentration so that $\rho = (q\mu_p N_A)^{-1}$. The values of μ_p are taken from Masetti et al. [3]. This plot shows that in order to achieve sheet resistance values below 100 $\Omega/\square$, which is considered an upper limit for ULSI applications, it is necessary to have box-like profiles with peak active boron concentrations greater than 1×10^{20} cm^{-3} for junction depths less than 0.14 μm.

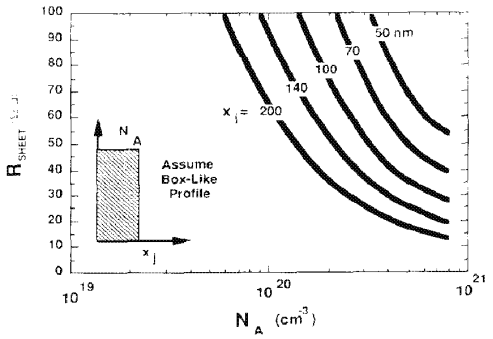


Fig. 2. R_{sheet} versus N_A for various values of x_j. A box-like profile is assumed. As the junction depth decreases, very high peak concentrations are needed to obtain low sheet resistance values.

A junction fabrication process that results in very shallow high concentration box-like junctions suitable for ULSI devices is the gas immersion laser doping (GILD) process (see, for example ref. [4–6]). The GILD process relies on a dopant gas being incorporated into a shallow molten region of the Si surface upon exposure to the XeCl ($\lambda = 308$ nm) pulsed excimer laser, and results in the formation of very shallow (200–2500 Å), high concentration ($> 5 \times 10^{20}$ cm^{-3}) p^+/n and n^+/p junctions. In this paper we describe in-situ junction depth, impurity profile, and sheet resistance determination using time-resolved diagnostic measurements and our laser doping modeling program, LASERMELT.

2. Experimental

In this section we describe the experimental setup, the modeling program, and the laser doping experiments performed which allow the parameters of junction depth, impurity profile, and sheet resistance to be determined in-situ. In-situ determination of these parameters allows for valuable feedback during the doping step itself. This will be necessary in future ULSI processes.

2.1. The GILD apparatus

A schematic of our research apparatus is shown in fig. 3. There are five main components necessary for the process namely: (i) the XeCl pulsed excimer laser, (ii) the optical system, (iii) the gas cell, (iv) the x–y stage, and (v) the computer to run the laser and the stage. A sixth important component (not shown) is the gas delivery system which allows vacuum levels down to 10^{-6} Torr to be obtained, and the various doping gases, B_2H_6 and BF_3 for p^+ and AsH_3 for n^+, to be introduced into the gas cell. Perhaps the two most important components in our system are the XeCl pulsed excimer laser and the beam homogenizing optics.

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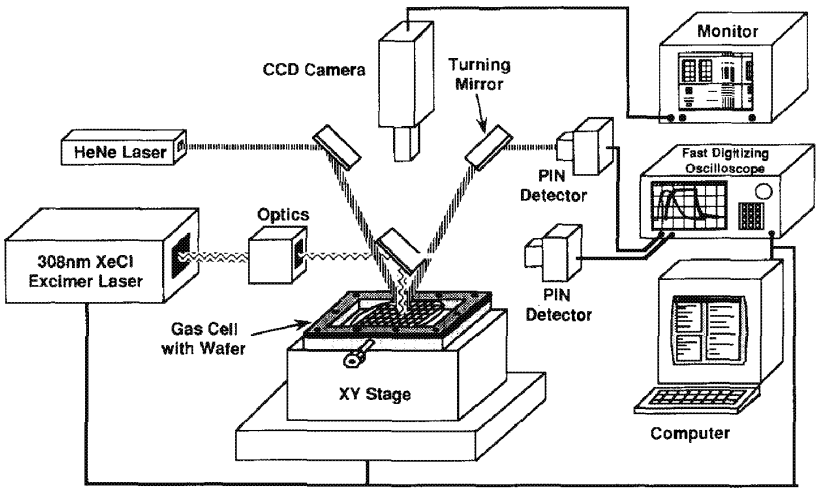


Fig. 3. Schematic of laser doping apparatus. Shown are the main doping related components: (i) 308 nm XeCl pulsed excimer laser, (ii) homogenizing optics, (iii) x–y stage and gas cell, and (iv) SUN workstation. Also shown are the diagnostic related components: (i) HeNe laser, (ii) CCD camera and monitor, (iii) PIN photodetectors, and (iv) fast digitizing oscilloscope.

The current excimer laser is a Questek model 2000 laser capable of producing 400 mJ of energy per laser pulse, and the beam homogenizing optical system is an XMR, Inc. homogenizer which redefines and homogenizes the beam to intensity variations of $< \pm 3\%$ across its present 4 mm $\times$ 4 mm area. Another part of the optical system is a series of high quality quartz beam splitters that are used to attenuate the laser beam by desired amounts. The laser pulse energy incident on the wafer can be changed by either changing the Questek output energy, or by keeping the energy constant and incorporating beam splitters having various transmission coefficients. Very precise control of the energy incident on the wafer is thus achieved by using a combination of both of these methods.

Once the beam passes through the optics system it is deflected onto the wafer surface with a turning mirror. This turning mirror is a 95% efficient reflector at 308 nm with the remaining 5% of the beam available for diagnostic purposes. The wafer is contained in a gas cell which has the appropriate dopant gas ambient, and doping is initiated by pulsing the laser one or more times at each wafer location. The wafer is stepped in the x and y directions by a highly accurate x–y micrometer stage. Both the stage and the number of laser pulses incident at each wafer location are currently controlled by a SUN workstation computer.

Additional equipment is shown in fig. 3 which enables in-situ diagnostic monitoring of the process. This equipment is: (i) a HeNe laser, (ii) a fast digitizing oscilloscope, (iii) two fast (< 1 ns rise time) Si PIN photodetectors, (iv) a CCD camera, and (v) a high resolution monitor. By incorporating this diagnostic equipment into the GILD apparatus, we can determine important process parameters such as time-resolved laser pulse full width at half maximum (FWHM) and silicon melt time. The laser pulse FWHM is measured by one of the Si photodetectors which detects the small amount of radiation transmitted by the turning mirror, while silicon melt time is determined using a HeNe ($\lambda = 632.8$ nm) laser as a silicon reflectivity probe [7]. It operates on the basis that the reflectivity of silicon increases from 34.7% for crystalline silicon to 73.4% for molten silicon at this wavelength. In addition, since the absorption depth of silicon at this wavelength changes from about 3 μm for crystalline silicon to about 100 Å for molten silicon, the HeNe laser becomes a very surface sensitive probe, and is thus very suitable for use in determining the silicon surface melt

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time. Since the HeNe and XeCl lasers are incident onto the same wafer location, the HeNe beam reflectivity change caused by the silicon melting due to the XeCl pulse can be detected by the other Si PIN photodetector. The ability to do time-resolved measurements on both the excimer laser pulse and the HeNe reflectivity change (hence silicon melt time) in-situ is necessary in order to adequately characterize the process. Both the HeNe laser intensity and the time-resolved laser pulse FWHM are stored on a fast HP 54111D digitizing oscilloscope.

2.2. The LASERMELT program

We now describe how our melt/depth simulation program, LASERMELT, is used to accurately model our present process. LASERMELT is a one-dimensional simulation program that has been adapted from a melt depth simulator originally written by Thompson [8] to specifically model our present GILD process in silicon for a 308 nm pulsed excimer laser. Since the main components of the program itself have already been described elsewhere [9], here we show only how it is used to provide accurate in-situ results which extends this previous work. LASERMELT combines the laser parameters of pulse shape and width, wavelength, energy fluence and number of pulses, with the silicon material parameters of solid and liquid reflectivity, thermal conductivity, enthalpy of melting, heat capacity, and absorption depth into a melt depth simulator which calculates the silicon melt depth and times. These results are combined with the process diffusion parameters (impurity diffusion in a liquid, segregation coefficient, and solubility limit in a liquid), and the doping parameters (gas pressure, sticking coefficient, and adsorbed dose) to predict impurity profiles, diffusion coefficients and layer sheet resistance values.

Currently LASERMELT accurately simulates our process because the temporal pulse FWHM of the XeCl excimer laser is obtained for each laser pulse by one of the fast Si PIN photodetectors (see fig. 3). This pulse intensity versus time is then digitized and used as the input energy term for the program which is in contrast to our earlier work. The digitized pulse and resultant silicon melt properties will be described later in this paper. Once the silicon melt time and melt depth have been determined, we can calculate the impurity profile and sheet resistance using previously determined liquid phase impurity diffusion coefficients and experimentally derived values of impurity dose per pulse. These experimental values are obtained using SIMS and RBS measurements on previously doped samples.

2.3. Doping experiments

The laser doping experiments are performed on wafers that have been patterned using a specially designed test mask [10] that allows detailed structural and electrical characterization of the GILD process. The starting material is $\langle 100 \rangle$ 3″ silicon wafers doped to $\sim 8 \times 10^{15}$ cm^{-3} n-type (for the p^+/n layer formation) and $\sim 3 \times 10^{15}$ cm^{-3} p-type (for then n^+/p layer formation). All wafers are cleaned, oxidized to a thickness of 5250 ± 100 Å in steam at 1150 °C, and patterned to form the isolated areas to be doped. The wafers are now ready for laser doping.

After removing the thin native oxide in a dilute hydrofluoric acid solution, the wafer is rinsed in DI water, dried, and immediately placed in the gas cell. The cell is then attached to the gas delivery system, and after three N_2 purges, the cell is pumped down to below 10^{-5} Torr. A turbomolecular pump insures that the process remains clean and free of pump oil. After pump down, the gas cell is filled with the desired doping ambient. At this point the chamber is sealed and the wafer is ready to be processed.

Laser doping is initiated by computer after a series of calibrations have been performed on test die to determine the laser energy and optical attenuation needed to achieve the desired silicon melt times. During the doping step itself, the time-resolved XeCl laser pulse and HeNe reflected intensity (silicon melt time) are measured for each pulse. This allows the silicon melt time to be correlated to the resultant junction depths as determined by subsequent SIMS and RBS measurements. An experimental matrix of conditions is produced by varying the laser parameters of energy fluence and number of doping pulses across

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the wafer. The relevant GILD experiments for this work utilize from 1 to 100 laser pulses at laser energy fluences that result in silicon melt times from 20 to 60 ns ($250 < x_j < 1800$ Å) in doping ambients of 1% and 10% BF_3 in He at 500 and 700 Torr for p^+ doping, and 0.1% and 1.0% AsH_3 in He at 500 Torr for n^+ doping. After laser doping, the doping profiles are determined by SIMS for the p^+/n layers and RBS for the n^+/p layers. In addition, since the test mask includes Hall samples, the active dopant dose and the sheet resistance values are simultaneously determined.

3. Results

In this section we describe laser doping results which emphasises the in-situ determination of junction depth and sheet resistance. Both experimental and simulation results are used to give accurate estimates of these parameters during the processing itself. Accurate prediction of junction parameters will be necessary for future ULSI processes.

The initial result obtained for our experiments is the in-situ measurement of the silicon melt time. In fig. 4 we have plotted a typical time-resolved trace from the fast digital oscilloscope showing the XeCl laser pulse and the reflected intensity from the HeNe laser. In this plot the laser pulse has a FWHM of 27.5 ns and the silicon reflectivity has changed (silicon has melted) for 39 ns. We find that the laser pulse FWHM ranges from 26 to 30 ns depending on the laser gas fill used. Actually most of our results are from FWHM values of around 27.5 ns. Traces like this can be taken for every doping pulse and related to the final junction profiles which allow a direct correlation between the silicon melt time and the junction depth by SIMS and RBS measurements.

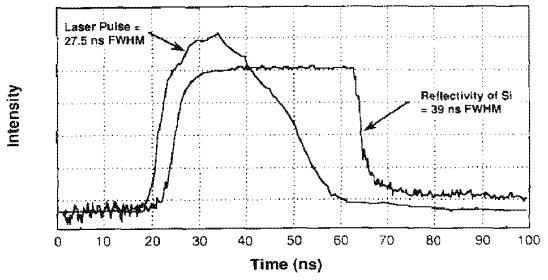


Fig. 4. Plot of XeCl laser pulse and reflected intensity of HeNe beam versus time from data obtained by the HP54111D fast digitizing oscilloscope. This laser pulse is about 27.5 ns FWHM and the silicon reflectivity change or melt time is about 39 ns FWHM. These values indicate that laser doping occurs in the nanosecond regime.

Because of data presented later in this section, a point should be made here about SIMS measurements and the detection resolution as governed by ion mixing. During SIMS analysis, the O_2 beam is not only sputtering the silicon surface, but implanting the top 100 to 150 Å as well. The result is that ion beam mixing occurs and the top layer becomes amorphous. The technique is, therefore, unable to resolve the depth to less than about 150 Å per concentration decade for the 12 keV O_2 beam used in these measurements [11]. This means that although our profiles are very abrupt (box-like), SIMS will still indicate a concentration slope of 150 Å/decade. This gives our profiles a characteristic tail that is not real. In this work we arbitrarily determine the "true" laser-doped junction depths by taking the half height of the peak concentration.

Since we measure the silicon melt times in-situ during the doping experiments, the corresponding SIMS profiles give a measure of the melt (or junction) depth versus silicon melt time. By taking many profiles, we can generate a curve of melt depth versus melt time which gives laser doping an in-situ junction depth determination capability. The data which we use to determine this relationship is derived from plots like that shown in fig. 5. Here we show four ^{11}B SIMS profiles formed using 50 doping pulses in 1% BF_3 at different laser energies resulting in silicon melt times of 22, 29, 39, and 50 ns. The corresponding junction depths are about 475, 725, 1100, and 1700 Å. Note that the profiles are very abrupt and the tails are due to SIMS resolution effects. By taking many such plots and correlating the junction depth with the silicon melt time, we can build up the very important plot of junction depth versus silicon melt time. This will be shown later along with our LASERMELT simulation results.

We now give LASERMELT simulation results for silicon melt depth calculations. In fig. 6, the

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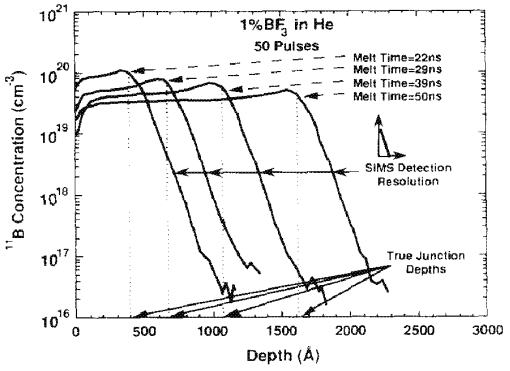


Fig. 5. SIMS profiles showing the change in junction depth versus the silicon melt time as measured in-situ during the process. The true junction depths are given; the profile tails are due to SIMS resolution limitations.

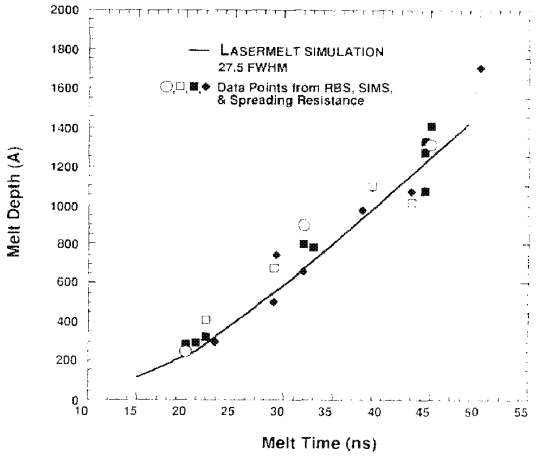


Fig. 7. LASERMELT and experimental silicon melt depth versus melt time. We assume that the melt depth equals the junction depth for the experimental data. The simulation result correlates very well with the experimentally determined junction depths.

silicon melt depth versus the time after the laser pulse starts is shown for different laser energy fluences. The laser pulse is digitized from the actual experiment and has a FWHM = 27.5 ns. From this plot, we see that the laser pulse begins at time $t = 0$ and at a later time, which is dependent on the laser energy fluence, the silicon begins to melt. For low values of laser energy fluence, such as 0.65 J cm^{-2}, this time is about 20 ns after the beginning of the laser pulse starts, shortening to about 10.5 ns at higher energies, such as 1.0 J cm^{-2}. The melt front position proceeds into the silicon until the maximum melt depth for the laser energy occurs. For the 1.0 J cm^{-2} case, this maximum occurs at about 1400 Å as marked on fig. 6. After this maximum melt depth is reached, the silicon recrystalizes at a velocity which is dependent on the ability of the silicon to conduct the heat away. This value is ~ 5.8 m s^{-1} for the 1.0 J cm^{-2} curve. This value is well below the value of 15 m s^{-1} which causes defect formation [12]. After the layer has recrystallized, we can determine the total silicon melt time for a given laser energy fluence. In fig. 6 the silicon melt time is determined to be ~ 49 ns for the 1.0 J cm^{-2} case.

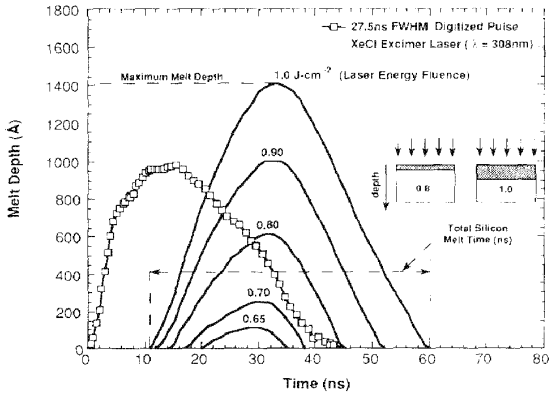


Fig. 6. LASERMELT simulation of silicon melt depth versus time after the pulse starts. Both the maximum melt depth and the melt time increase as the laser energy fluence increases. The maximum melt depth for 1.0 J cm^{-2} is predicted to be about 1400 Å and the melt time is about 49 ns.

By measuring the maximum silicon melt depth and melt time for each laser energy fluence, the important relationship of silicon melt depth versus melt time can be obtained. In fig. 7 we plot both the simulation and the experimental results (as determined by SIMS, RBS, and spreading resistance measurements) of melt (junction) depth versus silicon melt time, assuming that the junction depth equals the melt depth. Again this relationship is important because we measure the silicon melt time in-situ during the laser doping experiment. The results show excellent agreement between simulation and experiment. A spread in the experimental data exists because of the diffi-

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culty in determining exact junction depths for very shallow junctions. This result demonstrates that the *junction depth* can be determined in-situ during actual experiments by measuring the silicon melt time. Process steps with in-situ diagnostic capabilities will have significant advantages in future ULSI processes.

In addition to the junction depth, LASERMELT allows us to predict the sheet resistance and the doping profiles themselves for each laser doping condition. The input parameters necessary for LASERMELT to perform this calculation are the time-resolved laser pulse, the silicon melt time, the dose incorporated per pulse, and the diffusion coefficient of the dopant impurity in molten silicon. The time-resolved laser pulse and the silicon melt time combine to give the silicon melt depth, the impurity dose per pulse gives the total amount of impurity in the molten layer, and the diffusion coefficient determines the shape of the profile. During each doping pulse the time-resolved laser pulse and the silicon melt time are determined in-situ, and since the diffusion coefficients and the impurity dose per pulse can be determined from previous experiments, they can be considered constants for each different doping condition. This means that in-situ dopant profile and sheet resistance determination can be performed for all conditions in which the impurity dose per pulse is known, assuming that the impurity diffusion coefficients are constant in molten silicon.

We now show profile and sheet resistance results from LASERMELT. These results are compared with actual experimental data to show that accurate in-situ impurity and sheet resistance determination is possible with laser doping. A profile simulation for 1% BF_3 ambient doping is shown in fig. 8. Here the experimental conditions are 50 pulses using 22 ns silicon melt times for the shallow profile with an additional pulse of 43 ns for the deeper profile. SIMS results for these layers indicate peak concentrations of about 1×10^{20} and 6×10^{19} cm^{-3}, with junction depths of about 400 and 1100 Å, respectively. Note that the SIMS profile tails, ~ 150 Å/decade for the conditions used, are due to ion mixing as discussed earlier. Using the value of 9.75×10^{12} cm^{-2} atoms incorporated per laser pulse from earlier Hall measurements, and a previously determined value of $D_a = 4 \times 10^{-4}$ cm^2 s^{-1}, we see that excellent agreement is obtained between the simulated and experimental peak concentrations and junction depths for silicon melt times of 24.9 and 40 ns which are very close to our measured silicon melt times. Again, we stress that the SIMS tails should be ignored.

Simulated sheet resistance values are also determined using LASERMELT and the mobility model published by Massetti et al. [3]. The results

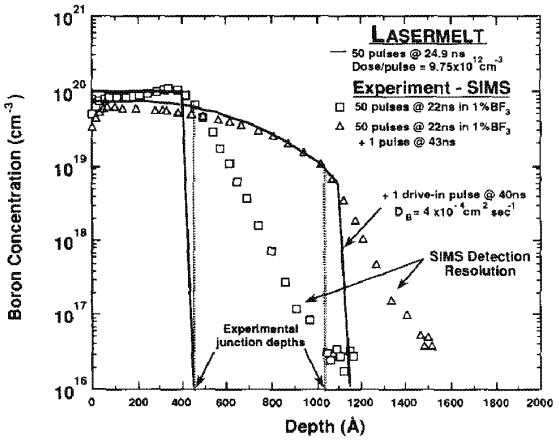


Fig. 8. LASERMELT and SIMS boron profiles. By using $D_B = 4 \times 10^{-4}$ cm^2 s^{-1} there is excellent agreement. Note that the SIMS profiles are limited by depth resolution and the true junction depths agree very well.

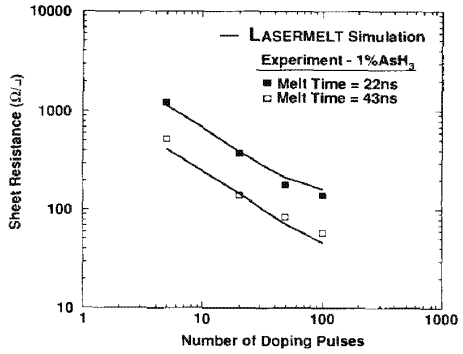


Fig. 9. Simulated and Hall sheet resistance versus the number of laser doping pulses for 0.1 and 1.0% AsH_3 doping. Excellent agreement is obtained between the simulation and experimental values.

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for 1% AsH_3 ambient doping are shown in fig. 9 for two different values of silicon melt times per pulse. The top points are for doping at 22 ns which has an experimentally determined Hall dose of 1.25×10^{13} atoms cm^{-2} per pulse, and the bottom points are for 43 ns (3.0×10^{13} atoms cm^{-2} per laser pulse) doping. The LASERMELT results (solid curves), using identical silicon melt times, show excellent agreement with the experimental data. The simulated lines are linear except at high pulse numbers where a slight degradation occurs due to a reduction in the average layer mobility.

4. Conclusions

In this work we have shown that the gas immersion laser doping (GILD) process is a doping technique that allows the junction depth, impurity doping profiles, and layer sheet resistance value to be determined in-situ using available diagnostic and simulation capabilities. The main diagnostic capabilities are the ability to measure the time-resolved laser pulse and the silicon melt time in-situ for each laser doping pulse. These measurements, when combined with our simulation program, LASERMELT, allow for the accurate determination of the impurity profiles and layer sheet resistance during the doping process itself. Ability to determine parameters such as these in-situ makes laser doping suitable for future ULSI device fabrication processes.

Acknowledgements

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Ion Implantation in Semiconductors—Part II: Damage Production and Annealing

JAMES F. GIBBONS, FELLOW, IEEE

Invited Paper

***Abstract*—Radiation damage is produced in a crystalline target whenever a moving ion transfers sufficient energy to a target atom to displace it from its lattice site. For conditions of practical importance in ion implantation, the radiation damage produced by the injected ions is severe, and the crystal must be carefully annealed if the chemical effects of the implanted ions are to dominate the residual damage. The purpose of this paper is to review work that has been performed over the past several years in an effort to understand implantation-produced damage and its annealing characteristics, especially in silicon.**

The subject is developed as follows. A qualitative description of the damage produced by an implanted ion is presented in Section I, followed by a partial inventory of the basic defects that are found in ion-implanted silicon (Section II). The structure of individual damage clusters produced by both heavy and light ions is then described in Section III, where theoretical predictions are compared to a variety of experimental data. This is followed with a section on the depth distribution of defects and damage clusters (Section IV); and the paper is then concluded with a section on the annealing characteristics of implantation-produced damage (Section V). The development is organized to give primary emphasis to those facts and ideas that are essential for applications of ion implantation in the fabrication of MOS and junction devices in silicon. A future paper will review the state of the art in compound semiconductors.

Manuscript received June 12, 1972; revised June 29, 1972. *This invited paper is one of a series planned on topics of general interest—The Editor.*

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INTRODUCTION

IN PART I of this series [1], we presented a review of the Lindhard, Scharff, and Schiøtt (LSS) theory [2] for the range distribution of ions implanted into amorphous targets, together with a description of the channeling process and some semiquantitative remarks concerning its effect on range distributions for ions implanted into crystalline targets. We also presented selected experimental results to provide some idea of the quality of agreement that one could expect between actual and theoretical range distributions.

The basic conclusions presented in that paper were 1) the LSS theory provides an adequate basis for predicting experimental range distributions in amorphous targets and in correctly misoriented single-crystal targets, and 2) the simple model proposed by Lindhard [3], which divides the incident beam into a random fraction and a channeled fraction, is at least qualitatively correct for single-crystal targets that are aligned with the incident ion beam parallel to a major crystal axis.

In the four years that have elapsed since Part I was published, the field of ion implantation in silicon has grown to maturity, and a large number of additional experiments on range distributions have been performed. These experiments

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have justified the conclusions stated above sufficiently well to warrant the use of the general LSS theory for the design of impurity profiles in a variety of semiconductor devices [4]; and range tables have been published [5] that can reduce the first-order design of a required impurity profile to a few simple calculations.[1]

During this same period of time, a great deal of effort has been devoted to the study of implantation-produced damage and its annealing characteristics, especially in silicon. Our purpose in this paper is to review this work and to present those conclusions from it that are essential for the application of ion implantation to the fabrication of silicon devices.

Our development of this subject will be as follows. We first give a qualitative description of the manner in which an implanted ion produces damage in a crystalline target, following this with an inventory of some of the basic types of defects that are found in ion-implanted silicon. Next we present some basic theoretical ideas that may be used to predict (or estimate) the structural characteristics of damage clusters and then compare these predictions with a variety of different experimental data. We follow this with a section on the depth distribution of defects and damage clusters and then conclude with a section on the annealing characteristics of implantation-produced damage.

As the subject unfolds, it will be clear that our knowledge of damage theory is much more elementary than our knowledge of range theory. However, experimental progress on all aspects of the problem has been very impressive, and annealing schedules have been developed that will reduce residual damage to levels that are satisfactory for the fabrication of both MOS and junction devices in silicon.

Since our review will cover a wide range of theoretical ideas and experimental results, it will perhaps be useful to start by providing a listing of the major topics covered by the paper, to which the reader may wish to refer for orientation as the subject develops. The separate sections are as follows:

Section I: The Concept of a Damage Cluster
Section II: Partial Inventory of Basic Defects in Silicon
Section III: Structural Characteristics of Implantation-Produced Damage in Silicon
Section IV: Damage Distribution Theory and Experiments
Section V: Annealing Characteristics of Implantation-Produced Damage.

I. The Concept of a Damage Cluster

An ion implanted into a target with an initial energy E_0 will ultimately come to rest, losing its energy in a series of collisions with the atoms and electrons of the target. Both of these energy-loss mechanisms are important in determining the range of the ion, but only the atomic (or nuclear) collisions can transfer enough energy to target atoms to produce radiation damage.[2] Furthermore, if the target is crystalline, the target atoms will be bound to their lattice positions with a certain energy, so that collisions of the projectile with the atoms of the target will only produce damage when the energy transferred to a target atom exceeds its *displacement threshold energy* E_d.

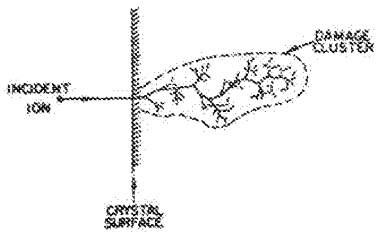


Fig. 1. Illustrating the formation of a damage cluster by collision cascades.

Collisions in which the energy transferred to a target atom, say E', is greater than E_d will displace that atom from its lattice site, and thus produce damage within the crystal. The displaced target atom may then be treated as a secondary projectile of energy $(E'-E_d)$, and it too will be brought to rest through a series of nuclear and electronic stopping events. In the course of its trajectory, the secondary projectile may have sufficiently energetic interactions with other target atoms to produce further displacements and a second generation of recoiling target atoms. The production of damage is therefore a cascade process in which the incident projectile is simply the primary damage-producing particle.

We can represent these various events qualitatively by a diagram such as the one shown in Fig. 1, where the track of the incident projectile serves as a tree trunk with branches that represent the trajectories of displaced target atoms. The envelope of all these displacements is referred to qualitatively as a "damage cluster," and will have a size and character that depends on a large number of factors, including especially the mass of the incident ion and its energy, the mass of a target atom, and the temperature of the target. It is also important to remember that the stopping processes are statistical in character, so two identical ions implanted under identical conditions will almost certainly produce differently shaped damage clusters.

Both the type and the amount of crystalline damage to be found within a given damage cluster are matters of great practical importance, since they determine the annealing mechanisms that can operate, and therefore the annealing temperatures and times that must be used to return the crystal to a relatively undamaged state in which the chemical effects of the implanted atom can dominate the residual damage. In the next section we present a partial inventory of the types of defects that can be generated in ion-implanted silicon, together with their annealing characteristics. We then proceed to a more exact picture of the implantation-produced damage to be expected for the extreme cases of very heavy and very light ions.

II. Partial Inventory of Basic Defects in Silicon

It is useful to begin with a brief list of some of the most important defects that have been observed in silicon, together with a summary of their physical characteristics. This will help us formulate a reasonable picture of the types of damage that we might expect to accompany the implantation of energetic ions.

[1] An important correction to the range tables is discussed in the Appendix to this paper.

[2] Insufficient energy is imparted to electrons under typical conditions for them to produce damage by a subsequent collision with a lattice atom.

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A. Vacancy-Interstitial Pair (Frenkel Defect)

A Frenkel defect is in principle formed by removing a silicon atom from its lattice site and placing it in a nearby interstitial position, as suggested in Fig. 2. Both the vacancy and the interstitial atom may play important roles in the formation of other defects, depending on the crystal temperature.

The vacancy has the crystallographic structure shown in Fig. 3, and can be identified by either its characteristic electron paramagnetic resonance (EPR) spectrum or infrared optical absorption. The vacancy can exist in several charge states, usually being doubly negative in n-type material ($V^{=}$) and neutral in p-type (V^{0}).

Using infrared absorption techniques, Vook and Stein [6] show that the charge state of the vacancy affects its annealing characteristics significantly, and hence the annealing rate for vacancies can be stimulated by light or electron injection. The vacancy annealing temperature is in the vicinity of 70 K for the double-negative state and 150 K for the neutral state. Vook and Stein attribute the growth of more complicated defects such as vacancy–oxygen pairs and vacancy–vacancy pairs (to be described shortly) to the liberation of vacancies from defect clusters and their subsequent recombination with themselves (for production of a divacancy) or other defects already present in the silicon. A vacancy can, of course, also recombine with an interstitial silicon atom to perfect the crystal structure on a local basis.

Much less is known about the detailed motion of interstitial atoms, though EPR studies also suggest that the interstitial atom is mobile, and that at temperatures as low as 4 K it can in some way migrate through the lattice until it encounters an impurity atom, which is then displaced into an interstitial site (see Fig. 2). The substitutional impurity is therefore converted to an interstitial impurity, a process which has been observed by Watkins [7] in p-type materials doped with B, Al, and Ga. The conversion process is called the *Watkins replacement mechanism*.

B. Vacancy–Impurity Pairs

In both n- and p-type silicon, vacancy–impurity pairs, including especially V+P, V+As, V+Sb, V+O, and V+Al, have been identified by both EPR techniques and infrared optical absorption measurements. These defects may form by diffusion of a simple vacancy to a lattice site adjacent to the impurity atom, and are therefore first observed at temperatures of about 70 K. Vacancy-group V defects anneal at temperatures in the vicinity of 400 to 500 K, while vacancy-group III defects anneal at approximately 500 K. The qualitative plot shown in Fig. 4, taken from Corbett [8], summarizes the situation for the common n-type dopants in silicon.

C. Divacancy

From the point of view of ion implantation, perhaps the most important simple defect is the divacancy, listed V+V in Fig. 4. The crystallographic form of the divacancy, as deduced from EPR measurements [8], is shown in Fig. 5.

Divacancies may form directly if an incident ion succeeds in displacing adjacent silicon atoms; and simple vacancies may also combine to form divacancies. These facts are suggested in Fig. 4, which also indicates that the divacancy is stable to temperatures of approximately 550 K, or 250°C. Since the divacancy is stable at temperatures in excess of

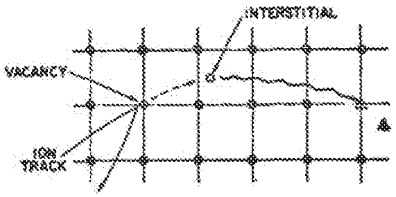


Fig. 2. Illustrating the formation of a vacancy-interstitial pair or Frenkel defect (and the Watkins replacement mechanism).

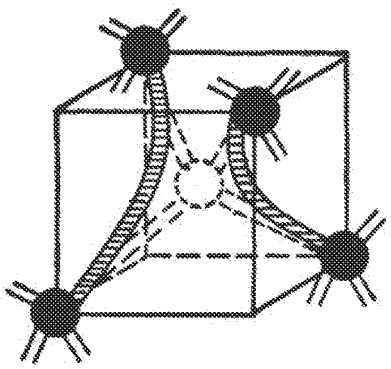


Fig. 3. Crystallographic structure of a vacancy.

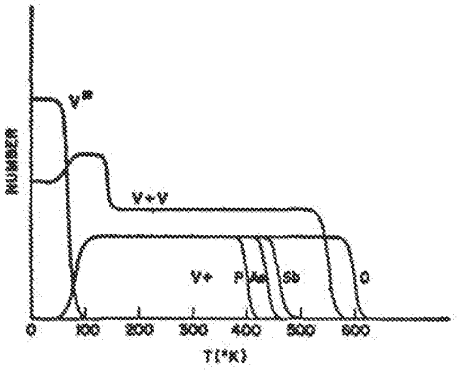


Fig. 4. Schematic illustration of loss of vacancies in n-type Si, formation of divacancies and vacancy-impurity pairs, and their subsequent annealing (after Corbett [8]).

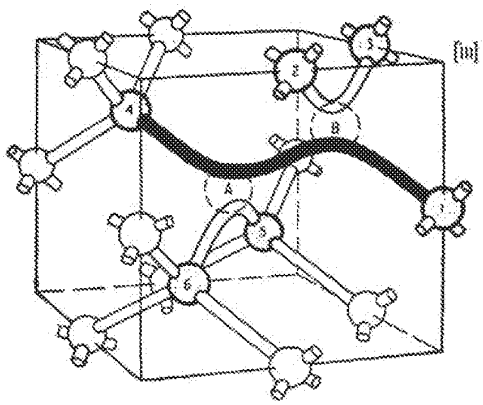


Fig. 5. Crystallographic structure of the divacancy (after Corbett [8]).

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room temperature, it is a prominent defect in silicon that has been implanted at room temperature.

D. Dislocation Lines and Loops

Dislocation lines and loops are also especially important in ion-implanted silicon because they can grow by either the agglomeration of simple defects or as a result of strain fields that accompany unannealed damage.

On interesting type of dislocation line, called a Frank–Read [9] source, can be visualized as a line of simple defects (vacancies, for example) along a row in the crystal, with the line being strongly pinned at its two end points P and P' by impurity atoms or perhaps defect clusters [see Fig. 6(a)]. The application of stress to the crystal will cause the line to bow as suggested in Fig. 6(b). Under some conditions, the stress required for continued bowing decreases as the bowing increases, so that eventually the dislocation loop will curl back on itself and surround the pinning points. The two ends may then unite so that a closed dislocation loop is formed; and the segment between the pinning points may straighten out to its original condition. The dislocation loop thus formed will continue to grow under applied stress; and the pinned segment will continue to generate successive loops. Ion implantation provides a possible mechanism for promoting the growth of a Frank–Read source if we simply replace the word "stress" in the description above by "lattice vacancies generated by an incident ion as it comes to rest." Strain produced by the volume expansion that accompanies heavily disordered regions [10] provides another possible mechanism to promote the growth of a Frank–Read source.

The special importance of dislocation loops and lines arises from the fact that, while they may change their length, shape, and location as the crystal is annealed, they do not generally disappear unless the crystal is subjected to a prolonged *vacuum* anneal at high temperatures (e.g., several hours at 1000°C) [51]. Dislocation lines of some type are essentially a permanent defect in ion-implanted silicon that is annealed in flowing nitrogen (or other inert gas).

E. Vacancy and Interstitial Platelets

A further type of defect that can be formed by the clustering of vacancies or interstitials is the vacancy platelet shown in Fig. 7. Fig. 8 gives a cross-sectional view of the platelet and also suggests that intersitial atoms can agglomerate to form platelets.

Once formed, these types of defects can grow in ion-implanted materials because they set up strain fields in the crystal that can be relieved by attracting the type of defect that was already used to form the platelet. Hence the platelet may grow by accumulation of implantation-generated vacancies or interstitials.

The strain field surrounding a platelet can also be reduced by the preferential adsorption of foreign atoms. For example, an atom that is smaller than a host atom will preferentially locate in a position such as the one shown in Fig. 9(a), while an impurity that is larger than a host atom will preferentially locate in a position such as the one shown in Fig. 9(b). Platelets and dislocation loops may therefore serve as effective sites for the adsorption of "wrong-sized" atoms, including especially common dopants such as boron and antimony in silicon.

Vacancy platelets are thought to anneal into dislocation loops at temperatures in the vicinity of 500–600°C.

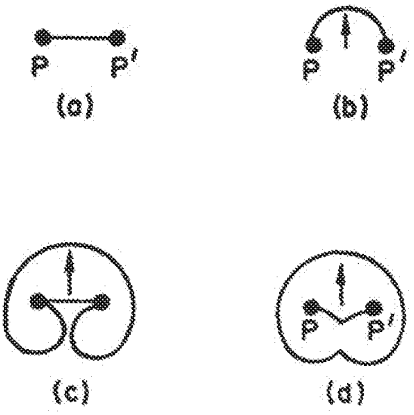


Fig. 6. Illustrating the mechanism of dislocation generation by a Frank–Read source.

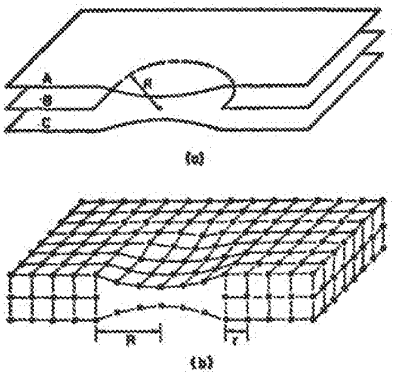


Fig. 7. Schematic illustration of the crystallographic nature of a dislocation loop. (a) Planar dislocation loop of radius R. (b) Atomic arrangement at a dislocation loop.

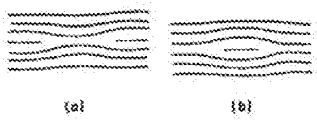


Fig. 8. Cross-sectional view of vacancy and interstitial platelets. (a) Vacancy platelet. (b) Interstitial platelet.

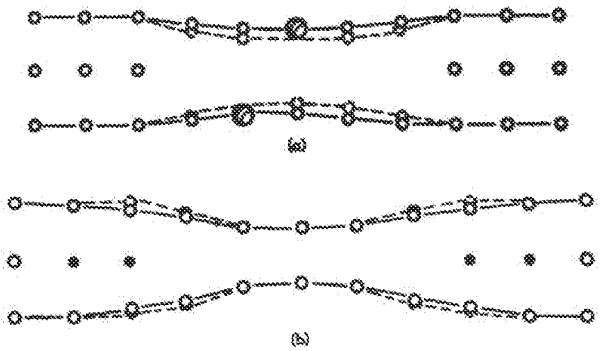


Fig. 9. (a) Illustrating the preferential absorption of large atoms on a dislocation loop. (b) Illustrating the preferential adsorption of small atoms on a dislocation loop.

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F. Spikes of Heavy Disorder and Amorphous Zones

Most of the preceding types of damage can be characterized as "simple defects" in the sense that they have well-defined lattice geometries, and formation kinetics that can be explained in terms of the motion of simple vacancies and interstitials. A different approach to the problem of radiation damage has been made by Brinkman [11], who argues that, when the cross section for displacement collisions becomes sufficiently large for a moving ion to displace one target atom per lattice plane, the volume affected is melted for a short period of time and then rapidly quenched. Such volumes are called "displacement spikes" and are presumed to anneal into small dislocation loops plus clusters of interstitials and vacancies as a result of the rapid quenching. Since the cross section for displacement collisions increases as a moving atom slows down, these displacement spikes will tend to form toward the end of the trajectory of an implanted ion.

Whether this particular mechanism can be invoked to explain damage in ion-implanted silicon is a matter of debate [52]. However, there is little doubt that large numbers of atoms *can* be displaced by a given projectile, and that when this occurs in a sufficiently small volume of space, the characteristics of the material will definitely change *toward* those of the amorphous state. It is, therefore, useful to consider the conditions under which a transformation from crystalline to amorphous material may occur.

The transformation process has been studied by Swanson *et al.* [12], who suppose that a defect-rich region of a crystal will transform spontaneously to a stable or metastable amorphous phase when the free energy of the amorphous region becomes equal to that of the defect-rich region. The defect concentration at which this transformation will occur can be estimated if a model of the amorphous material is assumed. Swanson *et al.* [12] show that, if the model of amorphous Ge developed by Richter and Breitling is used, in which tetrahedral bonding between individual atoms is maintained but one bond is stretched by 0.27Å, then the difference in energy of the amorphous state over the crystalline state is approximately 0.23 eV per elongated bond. This energy corresponds to a defect concentration of 0.04 of the atomic density, if each defect has an energy of 3 eV. When entropy changes are also included, Swanson *et al.* estimate that a Ge crystal containing a defect concentration of 0.02–0.04 atomic fraction will be unstable with respect to the amorphous state; and they suggest that a similar result should apply to Si.

From the point of view of ion implantation, the critical defect concentration computed by Swanson *et al.* should be taken as the lower limit at which the crystalline-to-amorphous transition might occur, since the derivation assumes that thermodynamic equilibrium has been achieved (in effect, the critical defect density is assumed to exist throughout the crystal). The defect concentration required to promote the crystalline-to-amorphous transition in an isolated damage cluster will most probably be higher than 0.04, perhaps by as much as an order of magnitude (cf. Vook and Stein [6]).

With regard to the annealing of amorphous zones, it is found that reasonably complete annealing of a *continuous* amorphous layer can occur at a temperature of approximately 600°C if the annealing is carried out for a period of approximately 30 min. *Isolated* amorphous regions will anneal at lower temperatures, as suggested by the computations of Nelson [13] shown in Fig. 10. Electron microscopy experiments suggest that isolated amorphous regions anneal by the liberation of vacancies, and yield dislocation lines and loops after annealing.

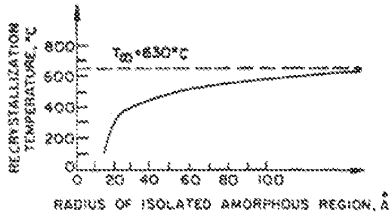


Fig. 10. Illustrating the theoretical recrystallization temperature of isolated amorphous regions embedded in a crystalline solid.

The manner in which divacancies, heavily disordered regions, and amorphous zones might be formed in the course of ion implantation will be described in the next section.

III. Structural Characteristics of Implantation-Produced Damage

In oversimplified terms, there are two basic types of damage clusters, corresponding to the implantation of very heavy and very light ions. Ions of intermediate mass generate damage clusters with structural characteristics that are intermediate between these two limiting cases. In what follows we will take the implantation of Sb into Si as representative of the heavy ion case; B, C, and O into Si as representative of the light ion case; and Si, P, and Ar into Si as representative of the intermediate case. In all cases we will be concerned with both the structural characteristics of individual damage clusters and the probable manner in which damage clusters interact to promote the crystalline-to-amorphous transition.

A. The Number of Displaced Atoms

It is appropriate to begin with a resume of the theoretical work of Kinchin and Pease [14], who obtained formulas from which one can estimate the number of atoms that will be displaced by a projectile as it comes to rest. Their estimate is based on the assumption that displacements result from a sufficiently strong Coulomb interaction between the projectile and the target atom. The effect of screening electrons is to cut off this interaction sharply at a radius of about $a_0/Z^{1/3}$, where a_0 is the Bohr radius and Z is the atomic number. A less restrictive analysis has been published by Sigmund [15], though the basic results are unchanged.

According to Kinchin and Pease, hard sphere collisions take place between the projectile and the target atoms when the energy of the moving atom is sufficiently low. An upper energy limit E_A for validity of this approximation can be computed by requiring the energy of the projectile to equal the Coulomb interaction potential of the two nuclei separated by the sum of the radii of their screening clouds. The result is

$$E_A = 2E_R Z_1 Z_2 (Z_1^{2/3} + Z_2^{2/3})^{1/2}(M_1 + M_2)/M_2 \quad (1)$$

where $E_R = 13.6$ eV; Z and M are atomic numbers and masses, respectively; and the subscripts 1 and 2 refer to projectile and target atoms, respectively. Values of E_A for Sb, Si, and B projectiles in a Si target are given in Table I.

When the projectile energy is less than E_A, Kinchin and Pease show that the number of target atoms displaced by a *primary recoil* should be

$$N_d = E/2E_d \quad (2)$$

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TABLE I
VALUES OF THE CRITICAL ENERGIES E_A, E_B, AND E_C FROM THE KINCHIN–PEASE THEORY

Critical Energy \ Ion	B	Si	Sb
E_A	7 keV	31.4 keV	480 keV
E_B	0.8 MeV	20 MeV	3 GeV
E_C	30 keV	120 keV	3 MeV

where E is the energy of the primary recoil and E_d is the displacement energy for a target atom, which we take to be about 15 eV. We mention here that, since (2) is linear in E, the total number of atoms displaced by a projectile can be estimated by inserting the total energy it deposits in nuclear collisions E_n into (2) (provided, of course, that its total energy $E<E_B$).

When $E>E_A$, Kinchin and Pease show that only some of the nuclear collisions will result in atomic displacements; and they define an energy E_B above which approximately half of the energy lost in Rutherford collisions is dissipated in lattice vibrations without producing displacements. The energy E_B has the value

$$E_B = \frac{\gamma E_A^2}{4E_d} \tag{3}$$

where $\gamma = 4\ M_1M_2/(M_1+M_2)^2$. Values of E_B are listed for the projectiles of interest in Table I.

When it is appropriate to do so, the number of atoms displaced by a projectile with $E>E_B$ can be estimated to be half the number given by (2). Under normal implantation conditions, however, this estimate is rarely useful because electronic excitation usually dominates the stopping process when $E>E_A$. To treat this case, Kinchin and Pease define E_C as the energy above which energy loss to electrons exceeds nuclear energy loss and show that, when the energy of the projectile is large compared to both E_C and E_B, the *total* number of atoms displaced by the projectile is approximately

$$N_t = \left[P(E_0 - E_C) + bE_C\right]/E_d \tag{4}$$

where E_0 is initial energy of the projectile, P is $\sim 10^{-3}$, and b is $\frac{1}{2}$ if $E_B>E_C$, $\frac{1}{4}$ if $E_B<E_C$. If $E_B \gg E_C$, the result is valid for $E_0>E_C$, independent of E_B.

For our purposes, E_C can be taken as the energy at which the nuclear stopping power S_n is equal to the electronic stopping power S_e. The values of E_C entered in Table I were obtained directly from the Johnson and Gibbons tables [5] for the ions of interest. In the following paragraphs, we will use the Kinchin–Pease formulas to study implantation-produced damage.

B. Experimental Criteria for Distinguishing Amorphous Silicon from Disordered Crystalline Silicon

The Kinchin–Pease formulas permit us to estimate the number of atoms displaced by a projectile as it comes to rest, and the LSS range theory can give us at least an approximate indication of the volume in which we can expect these displacements to occur. We therefore have enough theoretical information to estimate the average defect density in a given damage cluster. If this density reaches the level required for a crystalline-to-amorphous transition, we expect to find that the final damage cluster will be substantially amorphous. If the density does not reach the required level, we expect the silicon to be rich in simple defects (perhaps even heavily disordered), but not amorphous.

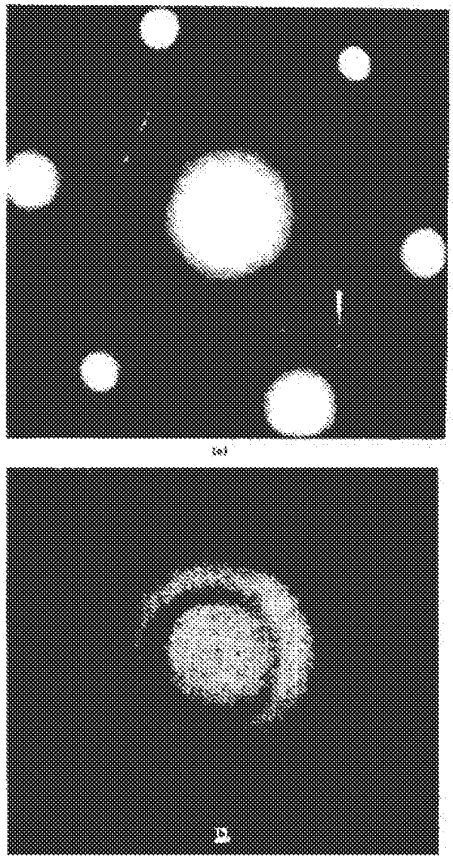


Fig. 11. Transmission electron micrographs of implanted silicon samples. (a) Lightly implanted. (b) Heavily implanted and/or amorphous.

To assist us in comparing these expectations with experiment, it is useful to list several criteria which can be used to distinguish disordered crystalline silicon from amorphous silicon. The following are especially noteworthy.

1) Transmission Electron Microscopy: A transmission electron micrograph of crystalline silicon shows a pattern of spots whose intensity and spacing depend on Bragg reflection conditions. In lightly damaged silicon, these spots will exhibit faint streaking, as shown in the electron micrograph of Fig. 11(a). As the silicon is driven toward the amorphous condition, the spot pattern will disappear and, in truly amorphous silicon, it will be replaced by a pattern of three concentric rings, called Debye–Scherrer rings. A Debye–Scherrer ring pattern for amorphous silicon is shown in Fig. 11(b) and will be discussed further in Section V.

2) Optical Absorption: Crystalline silicon has a sharp optical absorption edge at a wavelength of 1.1 μ, whereas amorphous silicon prepared at or below room temperature

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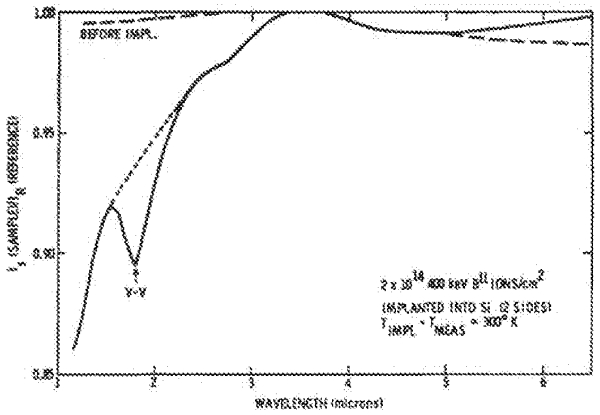


Fig. 12. Optical transmission of a 400-keV B ion-implanted sample; (2×10^{14} B^{11} ions/cm^2) into each of two faces referenced against an unimplanted sample. Dashed line indicates variations in the 100-percent line before implant.

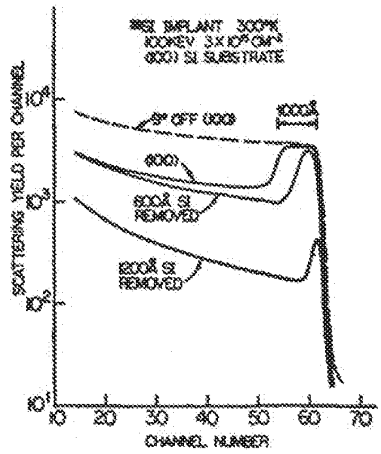


Fig. 13. Energy spectra of He ions backscattered from a Si sample whose surface has been damaged by ion implantation, showing the changes in aligned spectra (solid curves) after the removal of successive layers of Si. The spectrum for a nonchanneling beam direction remains essentially the same for all cases (broken curve).

has a more gradual optical absorption edge starting at about 1.25 μ. Disordered silicon that is not completely amorphous will also show a divacancy absorption band at a wavelength of 1.8 μ, though this band disappears when the material is truly amorphous. These features are exhibited in the optical transmission spectrum show in Fig. 12, the curve being taken from the paper of Stein *et al.* [16].

3) Backscattering: The yield of energetic (1.2 MeV) He^+ ions backscattered into a given solid angle is essentially the same for amorphous silicon and crystalline silicon that is oriented in a nonchanneling direction with respect to the He beam; but channeling directions can be found in crystalline material for which a large decrease in the backscattering yield is obtained.

These features are brought out especially clearly in the work of Chou [17] shown in Fig. 13. His sample consisted of a 1000-Å thick layer of amorphous silicon on a crystal substrate, which was prepared by bombarding a silicon crystal with a large dose of energetic silicon ions. As Fig. 13 shows, the backscattering yield is the same for the amorphous layer as for a crystalline target when the He beam is tilted 9° off the ⟨100⟩ axis.

When the amorphous layer is removed, the yield of backscattered He ions drops significantly as the alignment of the He beam is changed from 9° off ⟨100⟩ to the ⟨100⟩ axis. Hence from a backscattering viewpoint, damaged silicon appears to be amorphous when the backscattering yield is independent of the direction of the probing beam and has a magnitude equal to the yield obtained from a single crystal oriented in a nonchanneling direction. (A much more thorough explanation of both the process and the experimental technique is given in Mayer *et al.* [18].)

4) Electron Spin Resonance: The electron spin resonance signal for amorphous silicon consists of a symmetrical Lorentzian isotropic line with a g value of 2.006 [19]. The magnitude of the spin signal corresponds to a spin density of 2×10^{20} spins/cm^3. Undoped crystalline silicon shows no such line, though divacancies and other crystalline defects have readily identifiable spin resonance signals.

These features are clearly exhibited in the work of deWit and Ammerlan [20] shown in Fig. 14. For this experiment, silicon was bombarded with 50-keV P ions to a dose of 2×10^{15} ions/cm^2 at a dose rate of 10 μA/cm^2. The resulting spin

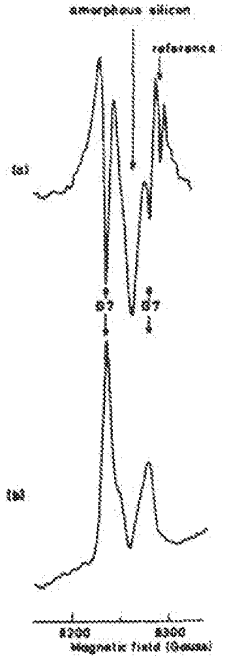


Fig. 14. EPR spectra in dispersion at 23.190 GHz for H∥ [111]. (a) In phase with magnetic-field modulation. (b) 90° out of phase. $T=4.2$K (after deWit and Ammerlan [20]).

resonance signal shows both the amorphous line and the characteristic divacancy spectrum. Both the divacancy line and the amorphous line disappear when the damaged material has been carefully annealed.

With these criteria in mind, we now consider the types of damage clusters to be expected for heavy and light ion implantation into silicon.

C. Heavy Ions

In a perfectly elastic head-on collision, an Sb projectile can transfer roughly 60 percent of its energy to a silicon atom. Hence in the course of its stopping, a 100-keV Sb atom im-

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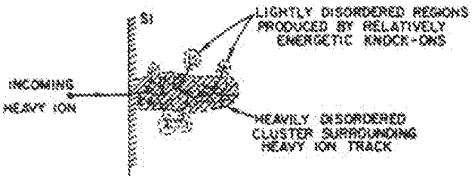


Fig. 15. Illustrating the damage cluster produced by a heavy ion.

planted into a silicon target can create primary silicon recoils with energies possibly as high as 60 keV. These recoiling atoms will then travel a significant distance in the crystal and can themselves produce significant damage. However, head-on collisions are unlikely events, so the damage produced by very energetic silicon recoils will be only a small part of the total.

The more typical situation is understood by observing that the nuclear stopping power S_n of a 100-keV Sb projectile in a silicon target is about 0.2 keV/Å over the entire trajectory [5]. Since the spacing between lattice planes in silicon is about 2.5 Å, this means that the Sb projectile loses about 500 eV per lattice plane on the average. We can expect the majority of this energy to be given to one primary silicon recoil atom, so the average recoil will have an energy approaching 500 eV. It would then have a range of roughly 25 Å. For comparison, the range of the 100-keV Sb ion is 500 Å, which is not substantially larger than the possible range of the average primary recoil atoms it creates.

Since we are dealing here with a case in which the projectile energy $E_0 < E_A$, we can use (2) to obtain the number of target atoms displaced by each primary recoil, and find $N_d \sim 15$.[3] In other words, the collision cascade of each primary recoil will contain roughly 15 displaced target atoms. Each collision cascade most likely contains only Frenkel defects and possibly divacancies; but if there is significant *overlap* of recoil trajectories, divacancies and more complicated defect structures may form spontaneously in the region of the overlap. If the overlap is sufficiently extensive, the majority of the damage can then be considered to lie within one large disordered region, as suggested in Fig. 15. Within this region, many of the target atoms will have been displaced from their original lattice sites, and if the defect density reaches a critical value, the cluster may become substantially amorphous.

To estimate the likelihood of this possibility, we observe that the volume of material that is initially disordered by a 100-keV Sb projectile is roughly

$$V \sim (25\ \text{Å})^2 \times 500\ \text{Å}.$$

Within this volume there are roughly 15 displacements per lattice plane, or 3000 total displacements. The average initial vacancy density will therefore be about $10^{22}/\text{cm}^3$, or about 0.2 atomic fraction. Since this is close to the displacement fraction required by Vook and Stein, and well above the lower limit given by Swanson *et al.*, a spontaneous crystalline-to-amorphous transition is likely to occur over a substantial portion of the cluster (especially since there is a strong tendency for low angle forward scattering of the primary recoils, and therefore the cluster volume is smaller than that just estimated). In any case, the density of displaced atoms and vacancies in the heavily disordered region is sufficiently high that we can certainly expect defect clusters that are stable at room temperature (e.g., divacancies, 4 vacancy complexes, etc.) to form *spontaneously* within the disordered zone.

Of course, not all of the displaced atoms are finally contained within the heavily disordered region, since both the displaced atoms and lattice vacancies produced at the extremity of the cluster can escape by diffusing into the lattice. Relaxation effects will also occur within the heavily disordered region along the ion track, so the final dimensions of the damage cluster will depend sensitively on the target temperature.

To compare these predictions with experimental data we consider the following results:

1) Davidson [21]: This author used transmission electron microscopy to study the crystalline-to-amorphous transition obtained when Sb ions were implanted into Si over the energy range from 40–100 keV, with ion doses covering the range from 5×10^{13}–10^{16} ions/cm^2. At the lower end of this dose range, the electron micrograph shows a spot pattern similar to that of crystalline silicon, but some streaking is apparent in the spots and the Debye–Scherrer ring pattern associated with amorphous material is faintly visible around the central spot. As the dose is increased to 10^{14} Sb ions/cm^2, the spot pattern gives way to the Debye–Scherrer pattern and the crystalline silicon is transformed to an amorphous layer extending from the surface to a depth that depends on the range of the Sb ion.

2) Mayer et al. [18]: These authors used the He backscattering technique to obtain a curve of relative "lattice disorder" versus dose for 40-keV Sb ions implanted into a room-temperature Si crystal.[4] Their results are shown in Fig. 16(a), in which it is seen that the lattice disorder appears to build up linearly with dose until the disorder saturates. Disorder saturation occurs for a dose of about 10^{14} ions/cm^2, and can easily be discerned by the fact that the bombarded area will have a hazy or "milky" appearance when compared to adjacent unirradiated silicon.

Since the saturation of lattice disorder occurs at exactly the dose where transmission electron microscopy shows the material to be amorphous, it is reasonable to conclude that individual damage clusters are substantially amorphous and that disorder saturation occurs when individual clusters overlap. Unfortunately the backscattering experiment measures an unknown combination of "true" lattice disorder (i.e., permanently displaced atoms) and lattice strain, and the conclusion above is therefore uncertain.

3) Stein et al. [16]: A partial resolution of this question is contained in the optical absorption experiments of Stein *et al.* These authors implanted 400-keV Sb ions into Si at room temperature, and then used optical absorption techniques to monitor the production of divacancies and the emergence of band edge absorption at the 1.25-μ wavelength. Their results are shown in Fig. 16(b), with the dose scale drawn to correspond to that of Mayer *et al.* The relatively abrupt increase in band-edge absorption for doses approaching 10^{14} ions/cm^2 clearly signals the development of an amorphous layer, as does the fact that the divacancy density decreases to zero at these same doses. At doses of 10^{13} ions/cm^2, however, the band-edge absorption is small and the divacancy density is both nonzero and increasing with increasing dose. A maximum

[3] The corrections published by Sigmund [15] will reduce N_d by 20 percent, which we neglect for purposes of estimation.

[4] Except where noted, all of the experiments to be described employed nonchanneling directions for implantation.

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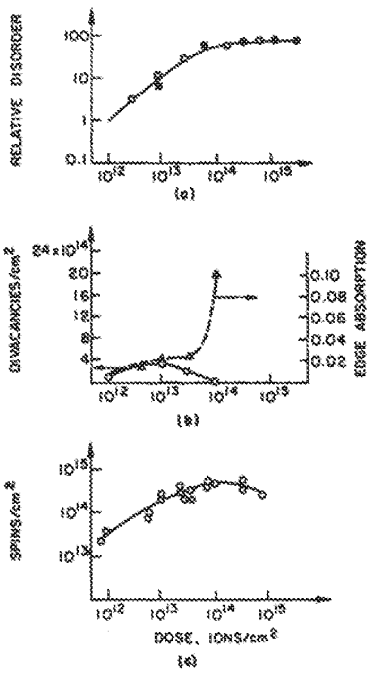


Fig. 16. Experimental observations of damage versus dose for Sb ions implanted into Si. (a) Relative disorder for 40-keV Sb implants, as measured by backscattering of 1.6-MeV He^+ ions. (b) Divacancy density and edge absorption for 400-keV Sb implants. (c) Spin density in amorphous ESR line for 80-keV Sb implants.

in the divacancy density can be seen to occur at a total dose of $\sim 10^{13}$ Sb ions/cm^2.

The number of divacancies measured is about 100 per ion at a dose of 10^{13} ions/cm^2, which accounts for a total of only 200 of the vacancies produced by each ion. To compare this with theory we note that each 400-keV Sb atom loses a total energy of about 220 keV in nuclear processes.[8] Hence the Kinchin–Pease estimate for the number of vacancies initially produced is $N_d \sim 7000$, which is clearly much greater than the final number that can be attributed to divacancies. Evidently, most of the vacancies have either been annihilated through recombination with interstitials; or, more likely, they have agglomerated into defect clusters that are stable at room temperature (such as 4-vacancy complexes,. vacancy platelets, etc.).

The relatively sharp change in band-edge absorption together with the fact that ions differing in mass by a factor of 100 all produce the same number of divacancies for the same total energy into atomic processes led Stein *et al.* to conclude that individual damage clusters produced by Sb atoms are most probably heavily disordered regions, not amorphous zones. On this view, amorphous zones would develop *only* as a result of cluster overlap.

4) Masuda et al. [22]: The final piece of experimental evidence we quote is the electron spin resonance work of Masuda *et al.* These authors measured the spin resonance signal following implantation of 80-keV Sb ions over a dose range from 10^{13} to 10^{15} ions/cm^2. For these conditions they observed *only* the isotropic Lorentzian line associated with amorphous material, obtaining a spin density that increased with dose in the manner shown in Fig. 16(c). Since the 80-keV Sb ion has a range of approximately 400 Å, the spin density at the peak of their curve corresponds to about 2×10^{22} spins/cm^3, which is in good agreement with the spin density for amorphous material. The fact that these authors do not see a divacancy spin resonance signal suggests that most of the divacancies in their material are in a neutral charge state, where they would exhibit no spin resonance.

Conclusion: Considering all of the data contained in Fig. 16 together with the quoted theoretical estimates, it seems reasonable to suppose that a given Sb ion will most likely produce a cluster containing both simple defects and regions with a substantial amorphous content, especially if the implantation is carried out at sufficiently low energies.[9] At higher energies the data perhaps allow a model in which most individual clusters are heavily disordered and cluster overlap produces amorphous zones. Electron spin resonance experiments on samples implanted with 10^{13} Sb ions/cm^2 at 400 keV could perhaps resolve this uncertainty, but such experiments have not yet been performed.

D. Light Ions

To compare light and heavy ions on a roughly equal basis, we now consider the likely character of the damage produced by a 100-keV B ion implanted into a silicon target at room temperature. At the beginning of its trajectory, the electronic stopping power S_e for a boron ion in a silicon target is about 0.02 keV/Å, while its nuclear stopping power S_n is only 0.002 keV/Å. Electronic stopping therefore dominates the stopping process until the energy of the projectile has been reduced to about 20 keV. (Hence $E_c \approx 20$ keV in Table I.)

Near the end of its range, the nuclear stopping power for the B projectile finally rises to about 0.01 keV/Å, and dominates the stopping process; however, the nuclear stopping power is still more than an order of magnitude less than the nuclear stopping power for Sb in Si.

The results of these facts are 1) the boron projectile will lose a substantial fraction of its total energy in electronic stopping processes, which do not produce damage; 2) primary recoil atoms are produced with much less energy on the average and therefore create much less damage; and 3) the range of the boron ion ($\sim 0.4\mu$ for 100 keV of initial energy) is much greater than the size of even the largest collision cascade produced by a primary recoil.

To make a quantitative estimate of the damage initially produced by the 100-keV B ion, we note that we are dealing here with a case in which $E > E_c$ over most of the trajectory. Hence the appropriate Kinchin–Pease estimate for the total number of displaced ions is given in (4) and yields $N_t \sim 700$. The majority of these displacements are produced near the end of the track after the projectile energy has been reduced to about E_c (see Fig. 17). To be specific, for a 100-keV boron ion, calculations to be presented in Section IV show that about 500 displacements will occur in the last 2000 Å of path length, leaving roughly 200 displacements to be distributed over the first 2000 Å. The damage cluster therefore consists primarily of simple Frenkel defects whose density increases to substantial values only near the end of the track. In such a case damage that is stable at room temperature is rarely produced *directly* by the projectile but only by subsequent dif-

[8] The manner in which the total energy deposited in nuclear processes is obtained will be described in Section IV.

[9] Additional computations in support of this view will be given in Section III-F.

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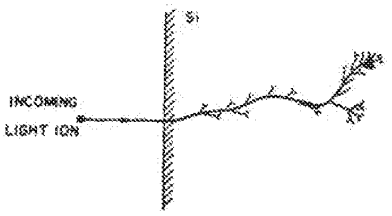


Fig. 17. Illustrating the damage produced by a light ion.

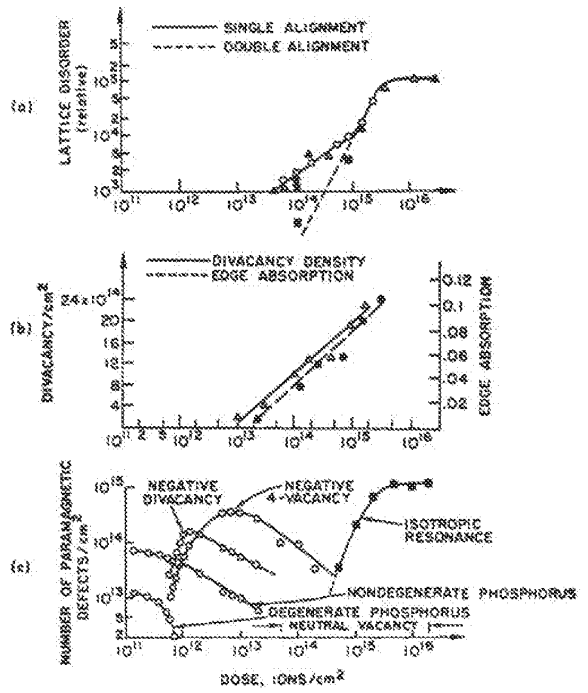


Fig. 18. Experimental observations of damage versus dose for light ion implants into room-temperature Si. (a) Relative lattice disorder for 150-keV C implants into Si as measured by single and double alignment backscattering. (b) Divacancy density and edge absorption following 400-keV B implant, as measured by infrared optical transmission. (c) Density of paramagnetic defects following 160-keV O^+ implants into Si, as measured by ESR.

fusion of vacancies to damage nucleation sites. Such a process is called *homogeneous damage nucleation* as opposed to the heterogeneous nucleation that takes place spontaneously in a heavily damaged region.

The experimental characteristics of boron-produced damage are similar to those of other light ions, so we consider B, C, and O together to develop a full experimental characterization of the damage produced by light ions.

1) Hirvonen et al. [23]: We begin by showing in Fig. 18(a) a curve of the relative lattice disorder produced by implantation of 150-keV C ions into a room-temperature Si target, the disorder being measured by backscattering of 1.6-meV He^+ ions. The measured lattice disorder is seen to increase with the *square root* of the ion dose until the dose reaches $\sim 2\times10^{15}$ ions/cm², after which the damage rises to saturation for a dose of 10^{16} ions/cm². The dose at which the curve departs from its square-root behavior turns out to be a function of the dose rate, changing from 2×10^{15} ions/cm² to about 5×10^{14} ions/cm² as the beam current is increased from 0.2 μA/cm² to 6 μA/cm². A similar dose rate dependence and sublinear build up of disorder has been observed by Eisen *et al.* [53] for boron implants performed at room temperature, with the critical dose levels being somewhat higher.

By using a double alignment technique for their backscattering measurements, in which the probing He beam enters the crystal along one channeling axis and the detector is mounted along another, Hirvonen *et al.* were able to show that a significant fraction of the disorder measured at low doses could be attributed to lattice strain rather than major displacements. Using their data, we show in Fig. 18 a dashed curve giving the relative disorder after the effects of lattice strain have been removed; and we take this curve to be representative of the number of Si atoms that are displaced significantly from their lattice sites. For later purposes we note that the disorder as measured by double alignment (DA) increases approximately with the square of the dose.

Both the dose rate dependence and the nonlinear buildup of disorder with dose are consistent with the prediction that the initial damage cluster consists of species that are mobile at room temperature and must diffuse to nucleation sites before they recombine to form damage that is stable at room temperature. A further indication of the importance of vacancy and interstitial atom diffusion is reducing residual damage in a light-ion room-temperature implant is contained in the work of Westmoreland *et al.* [24], who showed that lattice disorder saturated at a boron dose of 10^{15} ions/cm² if the implantation is performed at -150°C, where the simple defects are much less mobile. In effect, a dose of 10^{15} ions/cm² is sufficient to produce an amorphous layer at -150°C, whereas doses of $\sim10^{17}$ ions/cm² are required to produce an amorphous layer if a low-current (0.2 μA/cm²) B implantation is performed at room temperature.

2) Stein et al. [13]: To compare the foregoing results with optical absorption data, we show in Fig. 18(b) divacancy density and absorption edge measurements for 400-keV boron implants into room-temperature silicon. Here again, up to a total dose of 2×10^{15} (at a dose rate of 0.1 μA/cm²), we see no saturation in the divacancy density and no abrupt change in the band-edge absorption, which suggests that the defect clusters that form as a result of the vacancy diffusion have little if any amorphous content.

3) Brower and Beezhold [25]: Electron spin resonance experiments further confirm the picture previously developed, though the most thorough data have been obtained for oxygen implants rather than either carbon or boron. The work is that of Brower and Beezhold, who measured the type and density of paramagnetic defects produced in degerate n-type (phosphorus-doped) silicon as the dose of 160-keV O^+ ions was increased from 10^{13} ions/cm² to 2×10^{15} ions/cm². These authors find [see Fig. 18(c)] that in the dose range from 10^{13} to 10^{15} O^+ ions/cm² the main effect of the damage is to decrease the P^{31} hyperfine and free conduction electron spectra as these donor electrons are trapped at deeper levels. In the dose range from 10^{13} to 10^{14} O^+ ions/cm², spectra for the negative divacancy, the neutral phosphorus-vacancy, the neutral vacancy-oxygen, and a possible four-vacancy complex appear, and the total number of defects measured in these complexes agrees quite well with the number of vacancies computed from a Kinchin–Pease estimate. Furthermore, *no* amorphous spin resonance signal is observed until the dose reaches a level of about 5×10^{14} O^+ ions/cm²; but beyond this dose the amorphous signal grows *faster* than linearly, suggesting that the production of amorphous ma-

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terial occurs as a result of overlap of damage from several ion tracks (see Section III-G). The amorphous spin resonance signal finally saturates for fluences in excess of 5×10^{15} ions/cm^2.

Conclusion: It is clear from both the Kinchin–Pease estimate and the preceeding experiments that individual light ions most probably produce only Frenkel defects. The residual damage will then depend on a number of factors including prominently the target temperature and the types and densities of centers that are available for nucleation of stable damage. The production of a continuous amorphous layer at room temperature is possible, but it requires either a high dose or a high-dose *rate* (i.e., at a dose rate of 15 μA/cm^2, a dose of only 10^{15} boron ions/cm^2 will form an amorphous layer at *room temperature* in silicon; whereas a dose of about 10^{17} boron ions/cm^2 is required if the dose rate is reduced to 0.2 μA/cm^2. See Eisen *et al.* [53]).

E. Intermediate Ions

As we indicated previously, the damage produced by ions of intermediate mass has characteristics that are intermediate between the two limiting cases just discussed. Briefly:

1) Kinchin–Pease [15]: For a 100-keV Si atom implanted into Si, the total energy deposited in nuclear processes is about 60 keV, giving rise to about 2000 initial displacements. The range of the silicon atom is about 1700Å, corresponding to the average displacement of about 2 atoms per lattice plane. On this basis we except the damage as initially produced to be stable but not amorphous.

2) Mayer et al. [18]: Lattice disorder as measured by He backscattering is found to increase linearly with dose for P implants into Si, and to saturate at a dose of about 5×10^{14} ions/cm^2. Other measurements reveal little if any dose rate or temperature dependence at implantation temperatures below room temperature.

3) Matthews [26]: Electron microscope studies of Si implanted into Si at 40 keV suggest that at doses below about 5×10^{14}, the damage clusters are highly disordered as expected, but there is little evidence of amorphousness. However, the amorphous ring pattern begins to appear as the ion mass is increased, being faintly visible at doses of 1.5×10^{14} *argon* atoms implanted at 100-keV energy into a silicon target.

4) deWit and Ammerlaan [20]: Electron spin resonance experiments on a silicon sample impanted with 2×10^{15} phosphorus ions at an energy at 50 keV and a dose rate of 10 μA/cm^2 show both the characteristic divacancy spectrum and the amorphous spin resonance line. The divacancy introduction rate is found to be well below that measured by Stein *et al.* from which it is concluded that the Fermi level will be less than 0.55 eV from the valence band in damaged material, this being the position required to render most of the divacancies in a neutral charge state (and therefore unresponsive to the spin resonance excitation).

F. Electrical Estimates of Cluster Size

We have seen that, from a structural viewpoint, the general effect of implanting an ion into a room-temperature silicon target is to create a defect-rich cluster that may either spontaneously transform to an amorphous phase or relax by defect diffusion to yield a variety of defects that may lie some distance from the ion track. From an electrical standpoint, the defects produced act as carrier trapping centers in either case,

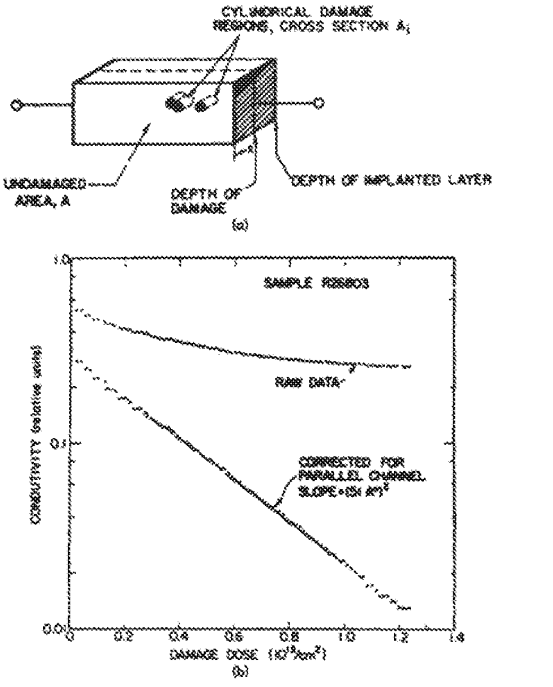


Fig. 19. Measurement of the electrical size of damage clusters (after Johnson). (a) Schematic illustration of sample used for measuring change of conductivity with ion dose. (b) Experimental data yielding an electrical cluster diameter of ~51 Å.

with the result that, prior to annealing, there is a monotonic decrease in the conductivity of a doped sample with ion dose.

If the implanted ions are of intermediate (or higher) mass, the implantation-produced defects are more nearly confined to a region of space surrounding the ion track. Within this region (or cluster), the trap density may become quite high, and the resistivity of the material within the cluster will approach that of intrinsic silicon, while material outside the cluster retains its original electrical properties. This effect offers the possibility of measuring what we will call the "electrical cluster diameter," an experiment that has been performed by Johnson [27]. We review his results here to develop an appreciation for the typical electrical size of damage clusters produced by intermediate ions of moderate energy.

A schematic illustration of Johnson's experiment is shown in Fig. 19(a), and consists of a conducting channel of thickness W into which Si atoms were implanted at room temperature. The energy of the Si atoms was chosen so that their penetration depth x_p was less than the channel thickness W. The total channel conductance therefore consists of a sum of contributions from damaged and undamaged portions of the channel.

Assuming the damage clusters to be right circular cylinders [see Fig. 19(a)], Johnson shows that the conductivity of the damaged portion of the channel may be written as

$$\sigma = \sigma_0 e^{-A_i\Phi}$$

where σ_0 is the initial conductivity, A_i is the cross-sectional area of the cluster, and Φ is the ion dose per unit area.[7] A plot of the total channel conductance versus dose should therefore

[7] The mathematical derivation of this result follows the general principles outlined in Section III-G of the present paper.

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consist of a constant term plus an exponentially decaying term.

The experimental data obtained by Johnson are shown in Fig. 19(b), where it is seen that the channel conductance follows the expected form exactly with an experimentally determined electrical cluster diameter of ~50 Å. Anticipating a later comparison we note here that the electrical cluster diameter should be larger than the structural cluster diameter because a depletion layer will form around the structural cluster (as a result of band-bending necessary to accommodate the change in resistivity).

G. The Production of Amorphous Material

The preceding sections of this paper show that both the structural and the electrical characteristics of implantation-damaged silicon will approach those of amorphous material if the ion dose, and with it the damage density, are sufficiently high. In particular, the results of the last section suggest that, prior to annealing, any impurity conduction effects arising from the doping characteristics of the implanted ion will be completely masked by implantation-produced damage. Hence, to obtain the desired impurity effects, we must anneal the crystal to repair the radiation damage.

It might be assumed that the difficulty of annealing would be roughly proportional to the amount of damage introduced by the bombardment; and on this basis it would be preferable to implant into heated targets at low dose rates so as to repair the damage introduced by individual clusters before the damage density builds up to large values. However, the opposite is usually the case: experimental results to be presented in the next section show that in silicon the production of an amorphous layer is generally desirable if high post-annealing electrical activity of the implanted species is to be guaranteed. Anticipating the importance of this result, we consider here the dose and temperature conditions that insure the production of an amorphous layer, relating these to the structural characteristics of damage clusters produced by heavy and light ions. Specifically, we assume that heavy ions create a sufficiently large defect density around the track of the ion to insure that individual damage clusters are amorphous, while for light ions we assume that significant overlap of individual clusters is necessary to achieve the amorphous condition. In what follows we present some simple mathematical models that describe these two cases. A more complete analysis has been published by Gibbons [28].

1) Heavy Ions: We consider first the idealized case where every implanted ion produces an amorphous cluster. If we assume that each cluster is a right circular cylinder with a fixed length R_p and an area A_i (projected on the surface of the crystal), then the rate of growth of amorphous material with dose can be written as

$$\frac{dA_A}{dN} = A_i\left(1 - \frac{A_A}{A_0}\right) \tag{5}$$

where N is the total dose, A_A the total surface area covered by amorphous clusters, and A_0 the total area being implanted. The factor within parentheses is just the probability that a given ion will hit in the undamaged area. The solution of (5) is

$$A_A = A_0(1 - e^{-A_i\Phi}) \tag{6}$$

where Φ is the total dose per unit area.

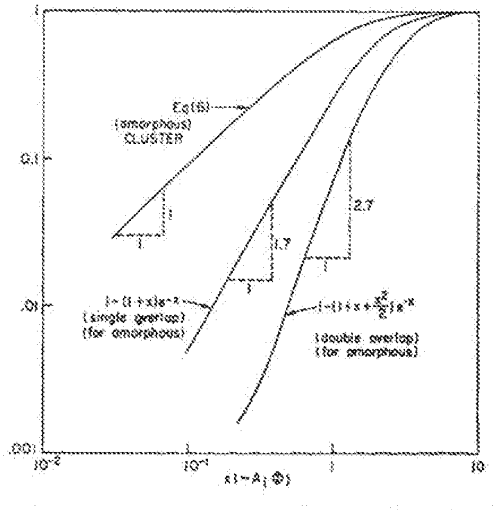


Fig. 20. Illustrating the growth of amorphous area for various degrees of cluster overlap.

A plot of (6), using log-log coordinates, is shown in Fig. 20. If this figure is compared with the disorder measurements of Mayer *et al.* given in Fig. 16(a) it is seen that this simple theory provides a good fit for the data; and in fact a projected cluster area $A_i = (19\ \text{Å})^2$ will cause theory to match experiment almost perfectly.

Given the simple exponential buildup of the damage, it is convenient to define the dose Φ^* required to produce an amorphous layer by $A_A = 0.9\ A_0$, which implies

$$A_i\Phi^* = 2.2. \tag{7}$$

The amorphizing dose thus depends inversely on A_i.

Of course, we know that the entire cluster is not amorphous, a fact which Morehead and Crowder [29] have taken into account by assuming that the highly disordered region initially formed by a heavy ion will relax to a stable phase consisting of an amorphous core surrounded by a sheath of lightly damaged crystalline material. They take the radius R of the cylindrical amorphous core to be

$$R(T) = R_0 - \delta R(T) \tag{8}$$

where R_0 is the radius the cluster would have if all of the initially displaced atoms were included in the disordered region. $\delta R(T)$ accounts for the decrease in R due to diffusion of simple defects from the extremities of the cluster into the surrounding crystalline material.

Using (8) to define the radius of the idealized cylindrical amorphous cluster produced by each ion, we have $A_i = \pi R^2(T)$ and, from (7),

$$\Phi^* = \frac{2.2}{\pi} R^{-2} \sim (R_0 - \delta R)^{-2}. \tag{9}$$

To obtain values for Φ^*, Morehead and Crowder assume that δR should be on the order of the vacancy diffusion length

$$\delta R \sim (D_v\tau)^{1/2} \tag{10}$$

and then substitute a standard exponential temperature dependence for D_v to obtain a final amorphizing dose of

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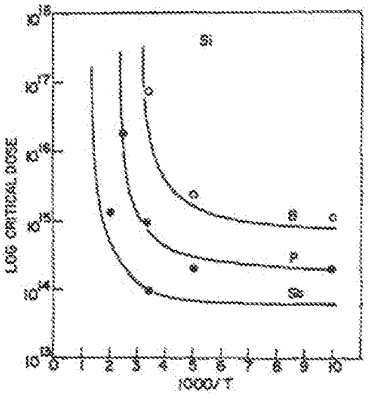


Fig. 21. Amorphizing dose versus T from the theory of Morehead and Crowder. Experimental points taken from ESR data.

TABLE II
TEMPERATURE AT WHICH THE MODEL OF MOREHEAD AND CROWDER PREDICTS THAT NO AMORPHOUS LAYER CAN FORM IN SILICON

Ion	B	P	As	Sb	Bi
T_∞, °K	306	430	600	730	910

$$\Phi^* = \frac{D_0}{\left[1 - K'(S_{n0})^{-1/2} \exp\left(-U/kT\right)\right]^{1/2}} \tag{11}$$

where K and U are adjustable constants, $D_0 = R_0^{-2}$, and S_{n0} is the energy-independent nuclear energy loss per unit path length [8]. K and U are chosen to be 115 $(\text{keV}/\mu)^{1/2}$ and 0.06 eV, respectively; and D_0 can be further expressed as

$$D_0 = E_D N_0 / S_{n0} \tag{12}$$

where E_D is the atomic displacement energy and N_0 the number of silicon atoms per cubic centimeter.

The fit between this model and experimental data taken from EPR measurements is shown in Fig. 21 and is seen to be quite reasonable, especially considering the extreme simplicity of the model. It is also interesting to note that for each ion (11) predicts a temperature T_∞ at which it would be impossible to form an amorphous layer. A list of values for T_∞ is given in Table II.

2) Light Ions: The difficulty in applying the previous model to light ions is that, as derived, it assumes individual clusters to have an amorphous core. Morehead and Crowder argue that the model will nonetheless provide a reasonable estimate of the amorphizing dose for ions that cannot produce individual amorphous clusters without predamage, even though the *approach* to saturation as a function of dose will be different for such ions. Indeed the agreement between their model and the experimentally observed boron dose required for amorphization gives reasonable support to this view. However, it is useful to consider other mathematical models that can predict both the approach to the saturation and the amorphizing dose, to see how they compare with experimental data.

For this purpose we again assume that an incident ion will produce a cylindrical cluster of length R and area A_1, but that overlap of clusters is required to produce an amorphous zone. The differential equations describing the production of amorphous material are then

$$\frac{dA_A}{dN} = A_1 \frac{A_D}{A_0} \tag{13a}$$

$$\frac{dA_D}{dN} = A_1 \left(\frac{A_u}{A_0} - \frac{A_D}{A_0}\right) \tag{13b}$$

$$\frac{dA_u}{dN} = -A_1 \frac{A_u}{A_0} \tag{13c}$$

where A_A represents the amorphous area, A_D the area that is damaged but not amorphous, and A_u the undamaged area. The solution which these equations yield for A_A is

$$A_A = A_0\left[1 - (1 + A_1\Phi)e^{-A_1\Phi}\right] \tag{14}$$

which is plotted in Fig. 20. Qualitatively this solution provides a much more rapid approach to saturation once the conditions for production of amorphous zones have become dominant (i.e., A_u small and A_D large). A straightforward extension of this model can be developed for cases in which n-tuple cluster overlap is required for the production of amorphous zones and yields

$$A_A = A_0\left[1 - \left(\sum_0^n \frac{(A_1\Phi)^k}{k!} e^{-A_1\Phi}\right)\right]. \tag{15}$$

To compare (14) and (15) with experimental data, we return to Fig. 18, where we see that both the atomic displacement as measured by double alignment channeling and the isotropic resonance as measured by EPR (under essentially identical implant conditions) increase somewhat faster than the square of the dose, which lies between (14) and (15). We take this to be in reasonable agreement with the simple cluster overlap theory. Furthermore, using $A_A = 0.9\ A_0$ to define saturation, we obtain from (14) the condition

$$(1 + A_1\Phi^*)e^{-A_1\Phi^*} = 0.1 \tag{16a}$$

or

$$A_1\Phi^* \sim 4. \tag{16b}$$

If it is assumed that diffusion effects still reduce A_1 in the manner suggested by Morehead and Crowder, then the simple cluster overlap model gives an amorphizing dose that is approximately 1.8 times that of the equivalent amorphous cluster model. By applying this factor to the data in Fig. 21, it can be seen that the cluster overlap model fits the data for boron better than the amorphous cluster model. However, one can argue that for lightly damaged clusters, diffusion might actually increase A_1 if defects diffuse away from their points of creation before forming a stable defect cluster. The variation of A_1 with temperature might then be considerably more complicated than that assumed.

3) Energy Deposition Model for the Production of Amorphous Material: A simpler criterion for the formation of amorphous material that does not require any specific view of the structure and/or overlap of individual clusters has been proposed by Stein *et al.* [13] and follows directly from an examination of Fig. 21. It is apparent in this figure that for any given ion the dose required to form an amorphous layer is essentially independent of temperature at low temperatures. We expect this to be the case since at low temperatures nearly all of the

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damage produced by a projectile will be retained as stable damage. On this basis, amorphousness at low temperatures should be predicted directly from a knowledge of energy deposition per unit volume. Following this clue, we observe that the standard nuclear stopping power [5] S_{n0} for B, P, and Sb projectiles is 91, 440, and 1800 keV/μ, respectively, and therefore the energy deposition per unit volume required to produce amorphous material (i.e., product of S_{n0} and dose) is

for B: $(91 \times 10^4)10^{15} \sim 9 \times 10^{20}$ keV/cm^3

for P: $(440 \times 10^4) \times 2 \times 10^{14} \sim 8 \times 10^{20}$ keV/cm^3

for Sb: $(1800 \times 10^4) \times 6 \times 10^{13} \sim 10.8 \times 10^{20}$ keV/cm^3.

Hence if the target temperature is such that essentially all of the damage produced by a projectile is stable, an energy deposition per unit volume of $\sim 10^{21}$ keV/cm^3 should produce amorphous silicon. We will use this criterion in Section IV to discuss damage distribution experiments.

With regard to a possible qualitative interpretation of this criterion, we note that the heat of fusion of a silicon crystal is 1800 J/g or about 0.7×10^{20} keV/cm^3, suggesting that a phenomenon akin to melting occurs in the formation of an amorphous layer. Of course, we expect the energy deposition for "melting" to be greater for implantation than for a thermal equilibrium process because the energy required to produce a Frenkel pair is greater for implantation. In fact the Frenkel formation energies are about 15 eV for collision displacement and about 2 eV for thermal displacement, so the ratio of "melting" energies might also be expected to be in the ratio of roughly 7:1, as they are.

IV. Damage Distribution Theory and Experiments

In the previous section we have described the damage produced by individual ions in terms of individual clusters, and we have visualized damage accumulation as resulting from an interaction of *identical* individual damage clusters. This approach provides a simple basis for understanding fundamental aspects of damage production, but it fails to account for one major feature: since all ions of a given type and initial energy do not have the same range, the individual damage clusters will not all have the same shape. In the simplest terms, we might expect heavy ions to produce "damage cylinders" with a Gaussian distribution of cylinder length that corresponds roughly to the Gaussian distribution in projected range for the given ion. Furthermore, the interaction of individual clusters to form amorphous material will be somewhat more complicated than we have been assuming. In this section, we will present a sequence of mathematical models and experimental results that can assist us in understanding the damage distribution problem and its practical consequences.

A. Basic Ideas

With respect to a given damage cluster, the foregoing sections indicate that the total amount of energy which an incident ion transfers to target atoms will be an important quantity in determining how much damage can be produced. We also know that the rate of energy transfer with distance may influence both the type of damage that is produced and the final shape of the cluster. The target temperature will clearly be an important factor in determining final damage; and the *electronic* energy loss of both the projectile and its recoils may be important because ionization of electrons from target atoms will increase the density of free electrons and can therefore affect the charge state and annealing characteristics of defects that were produced by either the ion under consideration or a previously implanted ion.

It is clear that the interplay of these factors is much too complicated to be included in a single comprehensive theory, so attempts to estimate the distribution of damage in ion-implanted material are usually limited to computations of how the total nuclear energy loss (or energy deposited in atomic processes) will be distributed in space, when the target is implanted with a total dose of Φ ions/cm^2.

The simplest (and definitely most approximate) treatment is that of Gibbons [30], which we review primarily to fix basic ideas, though we also note that the technique provides a simple means of rapidly estimating the energy deposition profile for any ion-substrate combination for which range calculations have already been made.

The quantity to be computed will be called the *primary energy deposition profile*. This term is chosen to call attention to the fact that we will only be concerned with how the statistical characteristics of the range distribution will affect the energy deposited by projectiles as they come to rest. No consideration is given to the question of what the host atoms do with the energy they receive (i.e., how their energy is divided between atomic and electronic processes, whether they are permanently displaced, and if so how much additional damage they produce). The primary energy distribution is thus only one of the quantities that must be known to develop a comprehensive theory of implantation-produced damage; though for light ions in a heavy substrate, some of the simpler features of the damage distribution might be expected to conform approximately to the primary energy deposition profile.[8]

The computation of the primary energy deposition profile would be relatively simple if all the injected ions had exactly the same range. The average nuclear energy loss rate would then be simply a plot of the Thomas–Fermi nuclear stopping power S_n, with the abscissa changed to read in terms of distance traveled rather than energy. Of course, all ions do not have the same range, so we must use separate S_n curves for each ion and add their effects together. To do this, we must first compute the energy distribution function $P(E|X, E_0)dE$, where PdE denotes the probability that an ion has energy between E and $E+dE$, given that it was injected into a target at $E=E_0$ and has reached a position X along its track. When P is known, the average nuclear energy loss rate at the position X can be found from

$$\langle S_n(X) \rangle = \int_0^\infty S_n(E) P(E|X, E_0)\, dE. \qquad (17)$$

In what follows we use the tabulated Thomas–Fermi nuclear stopping power for $S_n(E)$. In the application of the method presented here, the computation is carried out in the normalized units (ϵ) of Lindhard *et al.* [2], and an especially simple form for $P(E|X, E_0)dE$ is employed.

1) Procedure for Estimating $P(E|X, E_0)$: The energy distribution function can be found from a knowledge of the range statistics at intermediate energy E. The manner in which this is done is indicated qualitatively in Fig. 22. Here we

[8] In fact, the only difference between the primary energy deposition profile and the quantity dv/dx computed by Brice [31] is that energy given to recoils is divided into atomic and electronic fractions in the computation of v. However, since the average recoil has a relatively small energy, this refinement is also relatively unimportant, at least for light ions.

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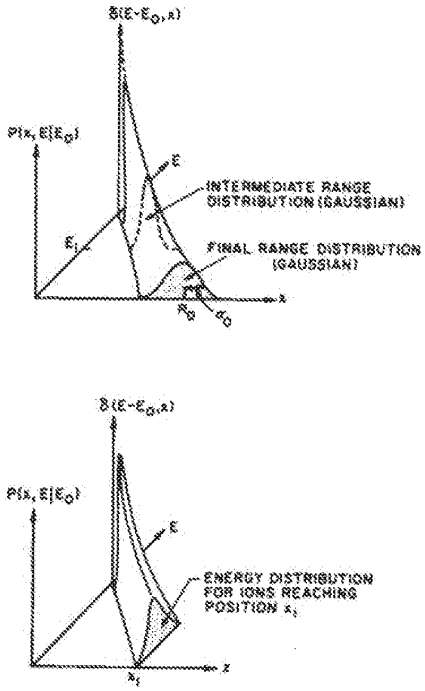


Fig. 22. Determination of energy distribution from generalized range distribution.

show the generalized range distribution function $P(X, E|E_0)$; i.e., a sketch of the probability that an ion has traveled a distance X and has an energy E, given that it was injected with energy E_0 into a target whose surface is at $x=0$. The distance traveled by the ion is measured along the x axis as in Fig. 22, and its energy is measured along the E axis.

At the surface of the target, all ions have an energy E_0, so $P(X, E|E_0)$ reduces to the delta function $\delta(E-E_0, x)$ at $x=0$. As the ion penetrates the target, however, it loses energy by nuclear and electronic interactions, and finally comes to rest at some position on the x axis. From the LSS theory, we know that the probability of coming to rest at a final position x_0 is described to a good approximation by a Gaussian probability distribution, in which x_0 has a mean value $R(0, E_0)$ and standard deviation $\sigma_R(0, E_0)$ [called (ΔR) in the LSS theory]. This is indicated in Fig. 22 by showing the generalized range distribution function to have a Gaussian cross section along the line $E=0$.

We also expect the range distribution at intermediate energies to be approximately Gaussian, so that it can be completely characterized by quoting a mean $R(E, E_0)$ and standard deviation $\sigma_R(E_1, E_0)$.

The exact way in which $R(E, E_0)$ and $\sigma_R(E, E_0)$ depend on E can be computed by numerical integration of generalized LSS equations as done by Brice [31] and Tsurushima and Tanone [32]; or approximations can be introduced to yield analytical solutions for $R(E, E_0)$ and $\sigma_R(E, E_0)$ [33]. For most purposes, the approximate formulas

$$R(E, E_0) = R(0, E_0)\left(1 - \frac{E}{E_0}\right) \tag{18a}$$

$$\sigma_R(E, E_0) = \sigma_R(0, E_0)\left(1 - \frac{E}{E_0}\right) \tag{18b}$$

are sufficiently accurate and have the advantage that R and σ_R may be obtained from tabulated final values of the range statistics, which makes the procedure to be developed directly applicable to a wide variety of ion-substrate combinations. In any case, a knowledge of R and σ_R, plus the assumption that the intermediate range distributions are Gaussian, will permit us to construct the generalized range distribution function.

Once the range distribution surface has been constructed, we can use it to determine, at least in principle, the energy distribution function for ions that have traveled a distance X_1. To do this we simply pass a plane perpendicular to the x axis through the point X_1. Such a plane will intersect the range distribution function in the required energy distribution curve, as suggested in Fig. 22(b).

The energy distribution curve will not in general be Gaussian, as is apparent by sketching the curve that is obtained when a test plane is passed through Fig. 22(a) at $X_1 = R(0, E_0)$. If X_1 is near the origin, however, then to a first approximation the energy distribution curve is Gaussian, having a mean and standard deviation that can be easily determined from $R(E, E_0)$ and $\sigma_R(E, E_0)$. As X_1 approaches R_0, a single Gaussian becomes a rather poor approximation, and it is then necessary to use two half-Gaussian distributions that join at E_1, having standard deviations σ_h and σ_l. The half-Gaussian applying over the range $0<E<E_1$ may also have to be truncated at $E=0$.

A somewhat poorer but conceptually very useful approximation is to assume that the energy distribution function is *rectangular;* i.e.,

$$P(E)dE = \frac{dE}{E_h - E_l}, \qquad E_l < E < E_h$$
$$= 0, \qquad \text{elsewhere} \tag{19}$$

where E_h and E_l are suitably chosen energies. Physically this distribution means that after traveling a distance X_1, the ion has an equal probability of being at any energy in the range $E_l<E<E_h$. We will show later that if comparison with experiment is used as the yardstick, the probability distribution given by (4) is in fact quite satisfactory for estimating $\langle S_n(X)\rangle$ [because P appears in the integrand, and the integration is carried over all energies. P would clearly be useless for estimating the contribution to $\langle S_n\rangle$ of ions having $E>E_h$ when they pass the plane in question].

To find appropriate values of E and σ_R for the Gaussian energy distributions, or E_h and E_l for the rectangular distributions, we refer to Fig. 23. Here we have sketched $R(E, E_0)$ and $\sigma_R(E, E_0)$ on E–x coordinates, which can be visualized as simply a projection of R and σ_R from the generalized range distribution curve onto the E–x plane. A horizontal line through the curves in Fig. 23(a) gives the values $R(E, E_0)$ and $\sigma_R(E, E_0)$ required to construct the intermediate range distribution shown in Fig. 23(b). [In practice, of course, the curves in Fig. 23(a) are constructed from a knowledge of $R(E, E_0)$ and $\sigma_R(E, E_0)$.] A vertical line at R_1 gives E_1, σ_h, and σ_l as shown in Fig. 23(a), and permits us to construct the *energy distribution at intermediate range* shown in Fig. 23(c). The values of E_h and E_l required for the rectangular distribution are simply obtained from the intersection of the vertical line with the uppermost and lowest curves in Fig. 23(a).

In this section we will use the rectangular energy distribution to estimate $\langle S_n(X)\rangle$ for boron in silicon, and will later compare the results with other methods of performing the

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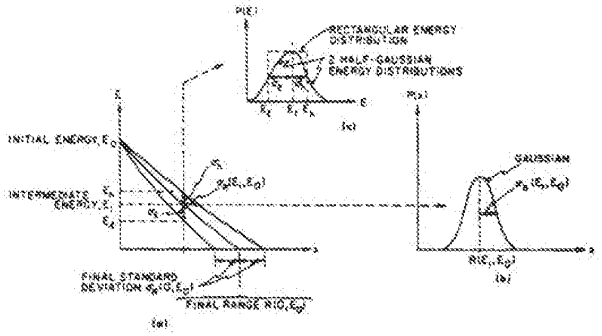
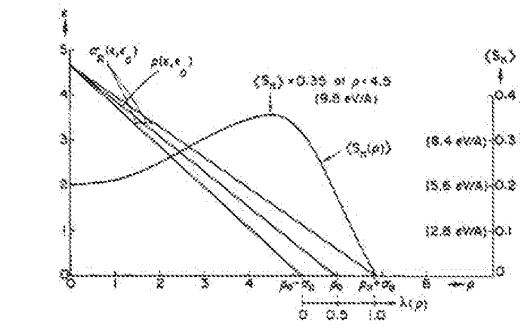


Fig. 23. Illustrating the development of the energy distribution function from range statistics. (a) Construction giving intermediate range and energy statistics. (b) Gaussian intermediate-range distribution. (c) Energy distribution at intermediate distance (two half-Gaussians).



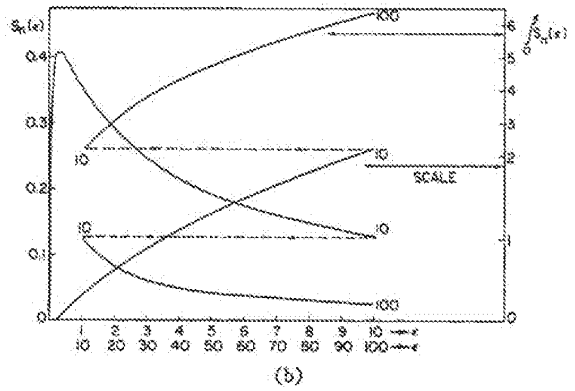


Fig. 24. Determination of $\langle S_n(X) \rangle$ for 40-keV B into Si. (a) Construction for obtaining $\langle S_n(X) \rangle$. (b) $\int_0^\epsilon S_n(\epsilon)d\epsilon$ versus ϵ for evaluating (20).

calculation. The comparison shows that the method gives a surprisingly accurate estimate of the spatial distribution of energy deposited into atomic processes for light ions in silicon and has the advantage over other methods that it can be easily extended to any ion-substrate combination for which range-energy computations have been previously performed.

3) Computation of $\langle S_n(X) \rangle$: To treat a case of practical interest, we show in Fig. 24(a) the generalized range-energy plot for a 40-keV B implant into silicon, in which we have used the Firsov formula to describe electronic stopping [3]. The normalized distance and energy units introduced by LSS are used to simplify the computations. Total range is used in this plot, instead of projected range, because we are interested in energy loss rates along the actual track. Corrections can be introduced at the end to convert the resulting distributions from range to projected range scales.

To compute $\langle S_n(\rho) \rangle$ from the plot given in Fig. 24, we first evaluate (17) using the rectangular energy distribution. The result is

$$\langle S_n(\rho) \rangle = \frac{\int_0^{\epsilon_k} S_n(\epsilon)d\epsilon - \int_0^{\epsilon_l} S_n(\epsilon)d\epsilon}{\epsilon_k - \epsilon_l}. \tag{20}$$

Since ϵ_k and ϵ_l are known, the evaluation can be carried out by first constructing a universal curve of the integral $\int_0^\epsilon S_n(\epsilon)d\epsilon$ and then simply reading off the values that are appropriate for the given values of ϵ_k and ϵ_l. The required curve of $\int_0^\epsilon S_n(\epsilon)d\epsilon$ is shown in Fig. 24(b). Using this curve at a convenient set of ρ values we obtain the $\langle S_n(\rho) \rangle$ curve shown in Fig. 24(a) over the ρ interval $0 < \rho < [\rho(0, \epsilon_0) - \sigma_R(0, \epsilon_0)]$ where $\rho(0, \epsilon_0)$ and $\sigma_R(0, \epsilon_0)$ are the normalized final range and standard deviation.

To compute $\langle S_n(\rho) \rangle$ beyond this interval requires us to make a minor adjustment in our computational procedure. The nature of the adjustment is best explained by recognizing that $\langle S_n \rangle$ arises from the averaged effects of a large number of injected ions. Because we are assuming the energy distribution to be rectangular, all of the injected ions contribute to $\langle S_n(\rho) \rangle$ so long as ρ is in the interval $0 < \rho < [\rho(0, \epsilon_0) - \sigma_R(0, \epsilon_0)]$. However, as we proceed beyond this interval, some of the ions have stopped and, therefore, cannot be included in computing $\langle S_n \rangle$. For example, at $\rho_0 = \rho(0, \epsilon_0)$, only half of the injected ions are still contributing to energy deposition.

We can include this effect in one of two ways. The simplest is shown in Fig. 24(a), where a new unit-length distance scale is set up to cover the interval $(\rho_0 - \sigma_R) < \rho < (\rho_0 + \sigma_R)$. If distance along this scale is denoted by $\lambda(\rho)$, then the value of $\langle S_n \rangle$ for ρ values in this interval is

$$\langle S_n \rangle = [1 - \lambda(\rho)] \frac{\int_0^{\epsilon_k} S_n(\epsilon)d\epsilon}{\epsilon_k}. \tag{21a}$$

As an alternative, we can extend the ϵ_l and ρ versus ϵ curves to negative values of ϵ, and then compute $\langle S_n \rangle$ from the formula

$$\langle S_n \rangle = \frac{\int_0^{\epsilon_k} S_n(\epsilon)d\epsilon}{\epsilon_k - \epsilon_l \text{ (extended)}}. \tag{21b}$$

However the computation is made, the result permits us to trace the behavior of $\langle S_n \rangle$ through the full ρ range. The $\langle S_n(X) \rangle$ curve for a 40-keV boron ion, shown in Fig. 24(a), was sketched by determining $\langle S_n(X) \rangle$ at the peak [which always occurs at approximately $\rho = \rho(0, \epsilon_0) - \sigma_R(0, \epsilon_0)$] and five other equally spaced points.

If we wish to plot $\langle S_n \rangle$ against normalized projected range, rather than total range, then we must first determine a functional relation between ρ_p and ρ,

$$\rho_p = f(\rho) \tag{22a}$$

and use it to rescale the horizontal axis. For a first approxima-

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TABLE III
COMPARISON OF $\langle S_n \rangle_{max}$ AND $(X_p)_{max}$ FOR B IN SI
($\langle S_n \rangle$ in eV/Å, $(X_p)_{max}$ in Å)

Energy, keV	40		80		120		200	
Parameter	$\langle S_n \rangle_{max}$	$(X_p)_{max}$	$\langle S_n \rangle_{max}$	$(X_p)_{max}$	$\langle S_n \rangle_{max}$	$(X_p)_{max}$	$\langle S_n \rangle_{max}$	$(X_p)_{max}$
Brice	10.3	881	9.2	1866	8.3	2800	7.5	4300
This work	9.8	955	8.8	2070	7.6	3100	7.1	4740

TABLE IV
DEPTH OF PEAK DISORDER FOR C IMPLANTED INTO SI
(Values Quoted in Å)

Energy keV	Feldman and Rogers	Brice	This Work
200	4,800	5,100	5,350
350	8,300	8,100	8,300
500	11,200	not computed	11,500

tion, we can use

$$\rho_p = \rho \frac{R_p(0, E_0)}{R(0, E_0)} \tag{22b}$$

where $R_p(0, E_0)$ and $R(0, E_0)$ are obtained from tables. A more accurate analytical formula is developed in [33].

We must also divide each ordinate of the curve by $(d\rho_p/d\rho)$. If (22b) is used to define the ρ_p-to-ρ relation, then

$$\frac{d\rho_p}{d\rho} \cong \frac{R_p(0, E_0)}{R(0, E_0)}.$$

Alternately the functional relation between R_p and R developed in [33] can be used to find $(d\rho_p/d\rho)$.

The mathematical effect of these transformations is to preserve the area under the $\langle S_n \rangle$ curve. There remains a question as to the physical significance of $\langle S_n \rangle$ when plotted on a projected distance scale, since energy is lost along the actual track, not the projected track. The projected distance scale would be the appropriate one to use if the average energy deposited per unit volume is required. The plot of $\langle S_n \rangle$ versus ρ (or R) would be the appropriate one for any damage process that depends on a threshold value of $\langle S_n \rangle$.

In any case, it is necessary to make the ρ-to-ρ_p corrections to compare the results of this work with the much more precise calculations of Brice [31] to be described in the next section. This is done in Table III, where $\langle S_n \rangle_{max}$ and its projected location are compared for B injected into Si at a range of initial energies. It should be mentioned that some discrepancy between the two calculations is expected from the fact that Brice uses Eisen's experimental electronic stopping cross section while the present work used Firsov electronic stopping, which is about 10 percent smaller.

It is seen from Table III that all corresponding values are within about 10 percent of each other. Furthermore, the full width at half maximum (FWHM) computed from the two methods are also within about 10 percent of each other, so the approximate method developed above gives a surprisingly realistic estimate of Brice's more accurate curve.

For a further comparison, we show in Table IV the peak damage depth obtained experimentally by Feldman and Rodgers [34] for C implanted into Si, together with the corresponding values of the position of the peak as computed by Brice and the present process. LSS electronic stopping is used for both calculations. As the table shows, the agreement is very satisfactory.

B. Brice [31]

A much more accurate computation of the distribution of energy deposited into atomic processes has been published by Brice who, following Lindhard *et al.* [35] defines the quantity ν as the total energy spent in atomic processes by *both* the projectile and its various recoil atoms, and then derives generalized LSS-type equations from which he is able to compute $(d\bar{\nu}/dx)$, the rate at which the *average* energy deposited into atomic processes varies with distance. His solution to these equations is based on the assumption that recoils do not move very far from their points of creation. This is a reasonable assumption for light ions, but becomes rather poor for heavy ones.

Brice's results are presented in the form of damage density contours, a representative sample of which is shown in Fig. 25(a) (for B in Si). The initial energy of the B projectile is located on the vertical axis of the figure, and a horizontal line through this point then gives the curve of $(d\bar{\nu}/dx)$ versus x_p, where x_p is used to represent distance into the target as projected onto the direction of incidence of the beam. Several horizontal sections through this contour plot are given in Fig. 25(b) to show how $(d\bar{\nu}/dx)$ varies for B at several different energies of interest in practical ion implantation work.

As mentioned previously, Brice's assumption that recoil atoms do not move too far from their original positions is reasonable for light ions, and therefore his plots of $(d\bar{\nu}/dx)$ versus x can be compared to actual damage distributions for these cases, especially when the annealing is inhibited. Comparison of Brice's results with experimental data obtained by Eisen *et al.* [35] show that for B in Si, Brice's $(d\bar{\nu}/dx)$ plots give reasonable estimates of the peak and FWHM, of the non-Gaussian damage distributions; and further, his computation of $(d\bar{\nu}/dx)$ for heavy ions is useful for estimating conditions that lead to a crystalline-to-amorphous transition, even though the details of the actual spatial distribution of damage are not accurately predicted from the $(d\bar{\nu}/dx)$ versus x curve for heavy ions. We will elaborate on this briefly in Section IV-D.

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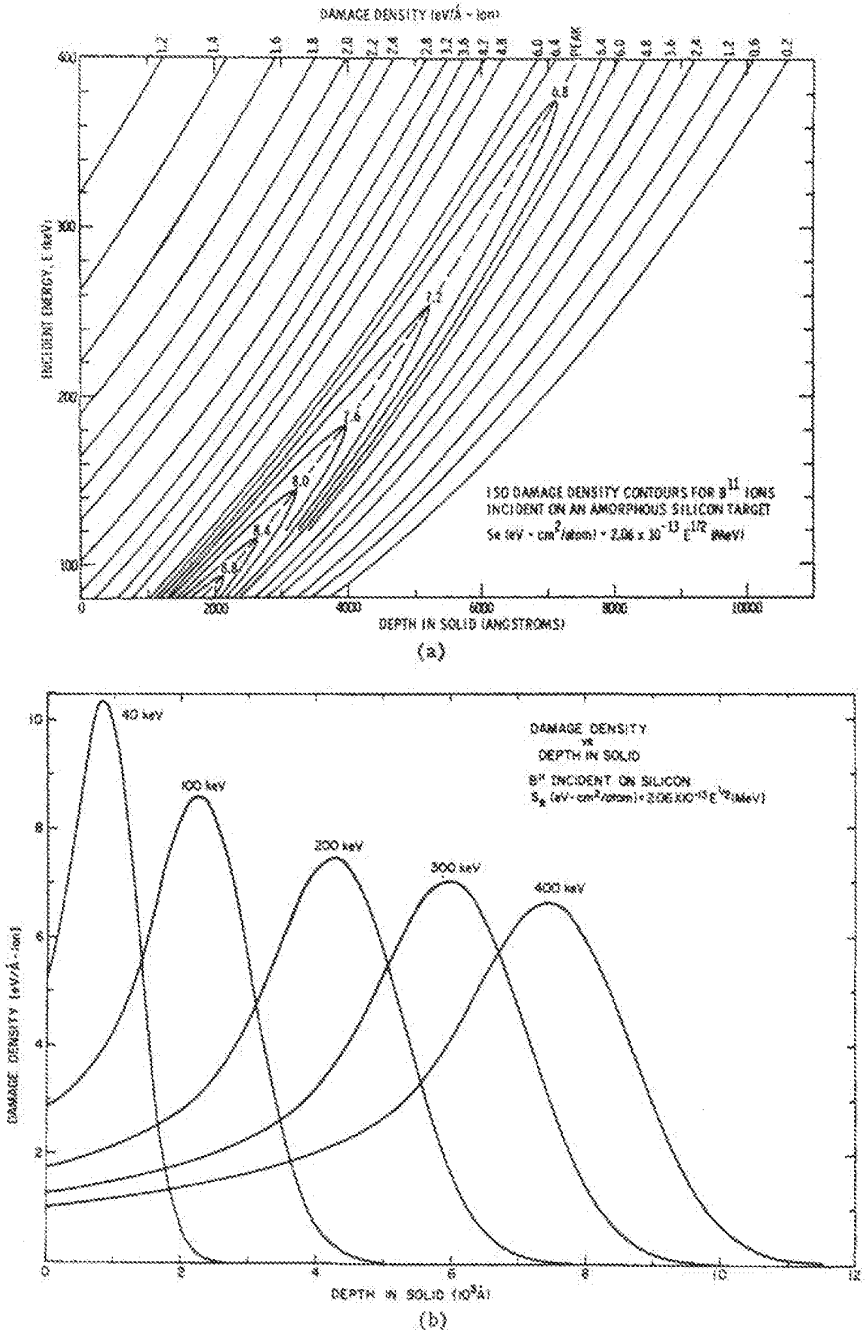


Fig. 25. (dW/dx) versus x_p as computed by Brice [34]. (a) (dW/dx) contours. (b) Depth distributions of (dW/dx) obtained from (a).

C. Sigmund and Sanders [36]

The most comprehensive attempt to produce a damage theory that will apply to a wide variety of ion implantation conditions is that of Sigmund and Sanders. To make the problem tractable, they limited their attention to a computation of the total energy deposited in atomic processes in a given volume of space by both the projectile *and* its recoil atoms. They formulated LSS-type integro-differential equations that describe this spatial distribution of deposited energy, and were able to find moments of the damage distribution in certain special cases (e.g., power law atomic interaction potential with neglect of electronic stopping). To minimize the effects of these simplifying assumptions, however, they expressed their damage distribution parameters in terms of the LSS projected *range* distribution parameters, computed from the power law interaction potential, with the suggestion that proportions between the damage distribution and the range distribution might be realistic even if the interaction potential used for the separate calculations was not. It is, therefore, possible to estimate the distribution of energy

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TABLE V

RANGE AND DAMAGE DISTRIBUTION PARAMETERS AS COMPUTED BY SIGMUND AND SANDERS

$\frac{M_{target}}{M_{ion}}$	$\frac{\langle x\rangle}{E/NC_1}$	$\frac{\langle \Delta x^2\rangle}{\langle x\rangle^2}$	$\frac{\langle y^2\rangle}{\langle x\rangle^2}$	$\frac{\langle xy^2\rangle}{\langle x\rangle\langle y^2\rangle}$	$\frac{\langle \Delta x^3\rangle}{\langle x^3\rangle}$
1/10	0.842	0.058	0.018	1.07	0.007
1/4	0.577	0.125	0.044	1.16	0.021
1/2	0.453	0.195	0.089	1.20	0.043
1	0.369	0.275	0.178	1.20	0.079
2	0.297	0.409	0.343	1.16	0.135
4	0.229	0.710	0.674	1.12	0.221
10	0.153	1.684	1.671	1.07	0.345

(a) Range Distribution Parameters

$\frac{M_{target}}{M_{ion}}$	$\frac{\langle x\rangle_D}{E/NC_1}$	$\frac{\langle \Delta x^2\rangle_D}{\langle x\rangle^2_D}$	$\frac{\langle y^2\rangle}{\langle x\rangle^2_D}$	$\frac{\langle xy^2\rangle_D}{\langle x\rangle_D\langle y^2\rangle_D}$	$\frac{\langle \Delta x^3\rangle_D}{\langle x\rangle^3_D}$
1/10	0.692	0.434	0.192	1.80	0.580
1/4	0.489	0.437	0.181	1.71	0.433
1/2	0.376	0.386	0.152	1.47	0.216
1	0.295	0.380	0.157	1.41	0.172
2	0.241	0.457	0.257	1.42	0.272
4	0.198	0.623	0.485	1.31	0.391
10	0.143	1.215	1.153	1.16	0.567

(b) Damage Distribution Parameters

deposited into atomic processes by using the Sigmund and Sanders tables of proportions together with, for example, the range data given in the tables of Johnson and Gibbons.

The Sigmund and Sanders tables that are most useful for estimating damage distributions in silicon are reproduced in Table V. The first column of the tables gives the mass of the incident ion relative to that of a substrate atom, while the remaining columns give the mean and standard deviation of the range distribution. The x dimension used by Sigmund and Sanders is measured along the path, while the y dimension is perpendicular to the path. Because higher order moments are difficult to calculate accurately, it is customary to use only the first and second moments of the damage distribution, and therefore the values in Table V are used to provide a *Gaussian estimate* of the damage distribution, whose parameters are related to the Gaussian LSS range distribution. For example, taking ratios from the second column of the tables, we find that B implanted into Si should produce a damage distribution with a mean at

$$\langle x\rangle_D \cong \frac{0.218}{0.264} R_p = 0.8\, R_p \tag{23}$$

where $\langle x\rangle_D$ is the projected depth for maximum damage (without annealing). The standard deviation in the damage distribution is given from ratios in the third column of the table as

$$\langle \Delta x\rangle_D \cong 0.75\, \langle \Delta R_p\rangle \tag{24}$$

which can be used together with (23) to construct a Gaussian estimate of the actual damage distribution.

As we will see later, the Sigmund and Sanders tables provide reasonable estimates of the mean and standard deviation of the actual damage distribution when annealing is inhibited. However, measured damage distributions are frequently not Gaussian, and in these cases the first and second moments may give a rather misleading representation of the actual damage distribution.

D. Estimates of Atomic Displacement Obtained from Spatial Distributions of Deposited Energy

Before turning to experimental measurements of damage distributions, we make a few remarks that will connect the computations of energy deposition just described to practical problems mentioned in previous sections.

1) Number of Displaced Atoms: Given a computation of $d\bar{\nu}/dx$, or $\langle S_n(X)\rangle$, it is clear that the Kinchin–Pease estimate for the number of atoms displaced by the "average" ion should become

$$N_d = E_n/2E_d \tag{25}$$

where E_n is simply the area under the $(d\bar{\nu}/dx)$ or $\langle S_n(X)\rangle$ curve. Since electronic stopping has already been included in

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the computation of $d\bar{\nu}/dx$ or $(S_n(X))$, the estimate given in (25) should be valid for any ion at any initial energy for which S_n and S_e give valid estimates of the stopping powers.

If we use this idea to compute N_s for 100-keV B ion, we find $E_n \sim 18$ keV and hence $N_s \sim 600$, which compares very favorably with the estimate of $N_s \sim 700$ given in Section III-D. Further inspection of the $(d\bar{\nu}/dx)$ curve shows that 12 keV of energy are deposited in the last 2000 Å of path length. Since a 100-keV B ion has a range of about 0.4 μ, we conclude that ~200 displacements occur in the first 0.2 μ and 400 displacements in the last 0.2 μ.

2) Production of Amorphous Material: Another very useful application of the energy deposition profile is obtained by combining it with the condition for amorphicity given by Stein *et al.* [13] to estimate when and *where* the substrate will become amorphous as the ion dose is increased. Two examples will outline the procedure.

a) Heavy ions: An "average" 100-keV Sb ion exhibits an $(S_n(X))$ of about 165 eV/Å or 1.65×10^7 keV/cm over its entire track. If it is assumed that all of the damage produced by such an ion is stable at room temperature, then the dose Φ^* required to produce an amorphous layer should be

$$(S_n(X))\Phi^* \sim 10^{21} \text{ keV/cm}^3$$

yielding $\Phi^* \sim 6 \times 10^{13}$ ions/cm², which is in very reasonable agreement with measured values.

b) Light ions: If we attempt to apply this criterion to a light ion such as boron, we must recognize that many of the defects produced can diffuse away from their points of creation unless the implantation is done at low temperature. Hence we attempt to predict only the damage distribution to be expected for low-temperature implants.

Taking again a 100-keV B ion, we find that $d\bar{\nu}/dx$ [or $(S_n(X))$] has a peak value of about 8.5 eV/Å at a projected depth of about 2200 Å. Hence a dose of

$$\Phi^* \sim 10^{21}/8.5 \times 10^8 \sim 1.2 \times 10^{15} \text{ ions/cm}^2$$

should be just sufficient to create a thin buried layer of amorphous material at a depth of 2200 Å. If the dose is increased to 2.5×10^{15} ions/cm², the required value of $(d\bar{\nu}/dx)$ for amorphousness should decrease to about 4.2 eV/Å, so the buried amorphous layer should start at about 1000 Å and proceed to a depth of about 3200 Å. The amorphous layer will extend to the surface when the dose is increased to the point where

$$\Phi^* \left.\frac{d\nu}{dx}\right|_{x=0} \sim 10^{21}$$

or, for 100-keV B, $\Phi^* \sim 4 \times 10^{15}$ ions/cm². These predictions are in reasonable agreement with the experimental data.

E. Experimental Results on Damage Distribution

As was pointed out in Section III, there are many experimental techniques that can be used to measure damage distributions, including prominently backscattering, electron spin resonance, and infrared absorption. In addition to these, damage distributions have been measured by decorating the damage with copper and then using radio tracer techniques to measure the copper distribution (Masters *et al.* [37]); and by taking advantage of contrast patterns that develop when a scanning electron microscope is used to observe an implanted crystal (Davidson and Booker [38]). For a complete summary of techniques and results, we refer the reader especially to the *Proceedings of the 1st International Conference on Ion Implantation* [39]. Here we summarize only typical results for our two representative cases of light and heavy ions and compare them with the theoretical predictions presented above.

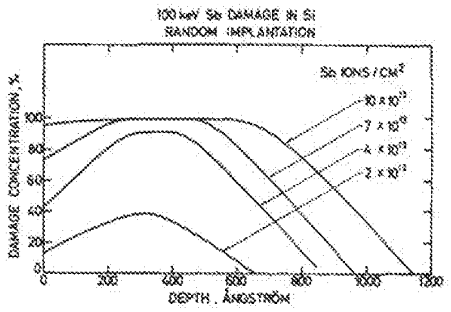


Fig. 26. Damage distribution measurements for 100-keV Sb implanted at random incidence into Si.

1) Heavy Ions: Using the He^+ backscattering technique, Bøgh *et al.* [40] have measured the damage concentration for 100-keV Sb implants into room temperature silicon with the results shown in Fig. 26. As the figure shows, the damage has a peak at approximately 320 Å and a half width of approximately 250 Å. Because the damage produced by recoils will occur at points that may lie some distance from the projectile track for this case, we must use the Sigmund–Sanders results to develop a comparison between theory and experiment. From Table V we find that the damage distribution should have its peak at a projected range of ~380 Å and a standard deviation of about 270 Å. Experiment and theory are thus in quite reasonable agreement, though the measured damage distribution is not Gaussian.

2) Light Ions: One of the newest and most useful techniques for rapidly assessing the damage produced during ion implantation is based on the fact that electron "channeling patterns" are produced when a scanning electron microscope is used to investigate a crystalline target. These patterns have been used by Davidson and Booker [38] to study both the dose and depth dependence of implantation-produced damage in silicon. The technique promises to be very useful for the rapid measurement of damage in other materials as well.

In this section we will give a brief description of the processes which produce contrast in an electron channeling pattern and then use these ideas to discuss the data obtained by Davidson and Booker.[5]

a) Basic characteristics of the electron channeling pattern (ECP): Electron channeling (or Coates–Kikuchi) patterns arise from the fact that, as an electron beam scans a crystalline surface, it will (or can be made to) sweep through an angle which is large compared to the Bragg angles for the crystal. The conditions for transmission and reflection of the electron beam are a function of the angle θ that the beam makes with the crystalline surface, showing highly irregular behavior when θ is swept through a Bragg angle. Consequently, if an SEM image is obtained by collecting high-

[5] The description of electron channeling patterns given here is intended to provide a concise summary of necessary facts with which the reader may be unfamiliar. It should not be inferred from the space allotted to electron channeling patterns that they are more important than other techniques for measuring damage distributions.

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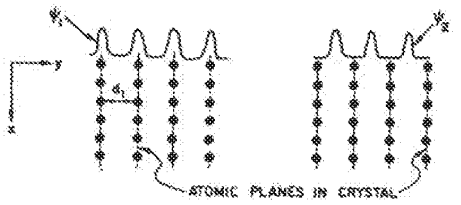


Fig. 27. Illustrating the two Bloch waves required to describe electronic motion in a crystal when an electron beam is incident at or near the Bragg angle.

energy backscattered electrons, it will show a sharp change in contrast each time the beam is swept through a Bragg angle.

To be somewhat more specific about the character of this contrast, it is necessary to consider the behavior of the Bloch waves that are required to describe electron motion in a crystal. For this purpose, we first recall that a Bloch wave is a traveling wave whose amplitude is spatially modulated with a periodicity that is determined by atomic spacings in the crystal.

From a quantum theoretical treatment of electron microscopy in crystalline foils, it is known that only two Bloch waves are required to describe electronic motion in a crystal when the external electron beam is incident at or near a Bragg angle. These two waves are shown in Fig. 27 along with a set of crystal planes. Both waves are visualized as traveling along the x axis, with the relevant modulation occurring along the y axis. As shown in Fig. 27, one of these waves, say Ψ_1, has its relative maxima on the atomic planes and nodes in between, while the other wave (Ψ_2) has its nodes on the atomic planes and relative maxima in between.

The amount of each wave that is required to meet the boundary conditions at the crystal surface depends on the angle θ between the external electron beam and the crystal planes. More specifically, the spacing between the crystal planes d_1 defines a Bragg angle θ_B according to the usual formula

$$\sin \theta_B \simeq \theta_B = \frac{\lambda}{d_1} \tag{26}$$

where λ is the wavelength associated with the electron's momentum ($\lambda = h/p$). If we denote the difference between θ and θ_B by α:

$$\alpha = \theta - \theta_B \tag{27}$$

then

1) when $\alpha = 0$, the two waves shown in Fig. 27 are equally excited, giving rise to a uniform injection of electrons along the crystal surface;
2) when $\alpha < 0$, Ψ_1 is preferentially excited;
3) when $\alpha > 0$, Ψ_2 is preferentially excited.

The effect of this preferential excitation is to produce bands of contrast each time θ is swept past θ_B. To see why this is so, we show in Fig. 28(a) a scanning electron microscope with a solid-state detector positioned so as to collect electrons that are scattered through a large angle. The physical process that produces large angle scattering (Rutherford scattering) requires that the electron be incident near the center of an atom (i.e., a small impact parameter is required). The number of such electrons is proportional to $|\Psi_1|^2$, and is therefore greater for $\alpha < 0$ than it is for $\alpha > 0$. Consequently, the number of electrons collected by the detector will have a local maximum in the region were $\alpha < 0$ and a local minimum where $\alpha > 0$. This behavior is illustrated in Fig. 28(b), and will give rise to bright-to-dark contrast; i.e., bright bands with dark edges.

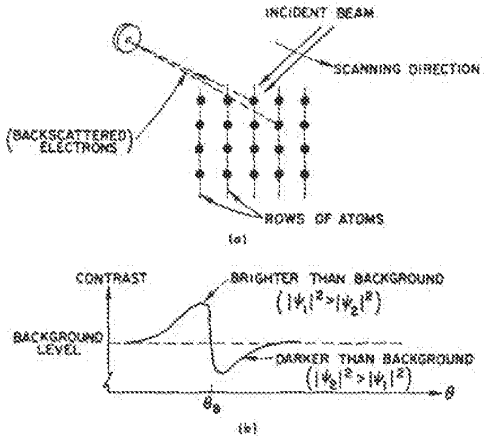


Fig. 28. Illustrating contrast obtained when an SEM is used to scan a single crystal. (a) Illustrating the SEM with detector arranged to monitor electrons backscattered through a large angle. (b) Illustrating the differential contrast that occurs when θ is swept through a Bragg angle.

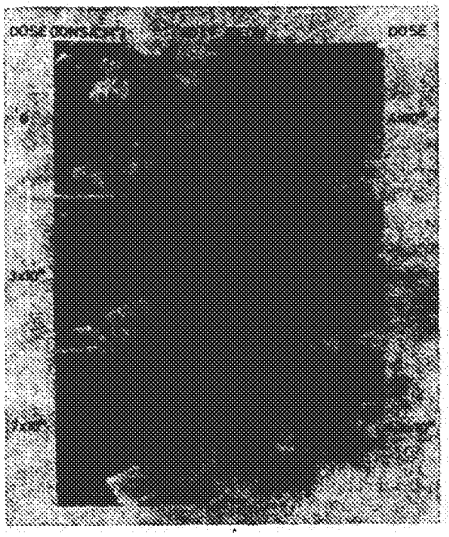


Fig. 29. Coates–Kikuchi patterns on Ne-implanted Si.

Now, if the electron beam is swept over a sufficiently large angle, it will pass through several directions of high symmetry [e.g., 110, 220, 440, etc.] as it scans the crystal surface. Each such direction will have a Bragg angle associated with the relevant spacing between atomic planes. Bright-to-dark contrast will be obtained each time the electron beam sweeps past one of these Bragg angles, so the pattern displayed on the screen of the scanning electron microscope will consist of a series of intersecting lines and bands. A pattern from a single crystal silicon specimen is shown in Fig. 29 for illustration (cf. photograph labeled 0 dose).

b) Dependence of electron channeling patterns on crystal perfection: As explained above, the contrast in an electron channeling pattern arises from the existence of the two special Bloch waves Ψ_1 and Ψ_2. The intensities of these two Bloch

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waves are rapidly attenuated in inelastic scattering processes (e.g., electron excitation within the atoms), and as a result the main contrast in the patterns comes from material that is within the first few hundred angstroms of the surface.

Furthermore, material that is amorphous does not give Bloch waves, and therefore does not contribute to contrast in an electron channeling pattern. In addition, material that is of poor quality will show contrast along the major (most open) directions in the crystal, but little or no contrast along directions of lower symmetry.

It follows from these facts that the quality of an electron channeling pattern (i.e., intensity of contrast and number of distinguishable bands) is a direct measure of crystalline perfection within the first few hundred angstroms of the surface.

c) Damage measurements in ion-implanted silicon: These ideas lead naturally to the technique used by Davidson and Booker to measure both the dose dependence and the depth distribution of the damage produced by Ne ions implanted at 80 keV into silicon.

i) Dose dependence: First, electron channeling patterns were taken from the surface of specimens that had been bombarded with 80-keV Ne ions to doses between 10^{14} and 4×10^{15} ions/cm^2. The patterns obtained by these authors are shown in Fig. 29, from which it is apparent that

1) very little change in contrast occurs for ion doses less than 7×10^{13}/cm^2;
2) beyond this dose, the number of lines that can be resolved decreases quite rapidly, and the pattern finally disappears at a dose of 4×10^{15} ions/cm^2.

ii) Depth distribution: To measure the depth distribution of the damage, Davidson and Booker employed the fact that contrast in an "electron channeling pattern" (ECP) arises from the first few hundred angstroms of the sample. By anodically stripping the silicon, they were able to measure pattern quality as a function of depth into the implanted layer.

Fig. 30 shows the results of such an experiment, using a dose of 7×10^{14} Ne ions implanted at 80 keV to produce the damage. The pattern is very good at the surface, nonexistent from 500 to 1500 Å, and then nearly perfect at 1800 Å and beyond. The absence of any pattern at the intermediate depths is evidence of a buried amorphous layer.

To be somewhat more quantitative about the depth distribution, Davidson and Booker measured the number of lines visible in the electron channeling patterns after successive removal of 470-Å layers of the target. The results are shown in Fig. 31, and give an excellent summary of the depth distribution of damage as a function of dose.

d) Comparison with theory: Since we are dealing here with a relatively light ion, recoils are relatively unimportant in determining the damage distributions, so we can use the Brice curves of $(d\mathcal{F}/dx)$ to estimate the characteristics of the damage. According to Brice, an 80-keV Ne ion has a peak $(d\mathcal{F}/dx)$ of approximately 23.5 eV/Å at a projected depth of ~900 Å, falling to 20 eV/Å at 500 Å and 1200 Å. $(d\mathcal{F}/dx)$ at the surface is about 15 eV/Å, and on the deeply penetrating side the $(d\mathcal{F}/dx)$ curve falls to about 3 eV/Å at a depth of ~1800 Å. From these numbers we expect a thin buried layer to form first at a depth of 900 Å for a dose of $\sim4.3\times10^{14}$ ions/cm^2. The buried layer should extend from 500 Å to 1200 Å when the dose is increased to 5×10^{14} ions/cm^2; and the amorphous layer should touch the surface when the dose reaches 7×10^{14} ions/cm^2. For larger doses, the amorphous layer will simply proceed into the target, being at a depth of 1800 Å for a dose of $\sim3\times10^{15}$ ions/cm^2.

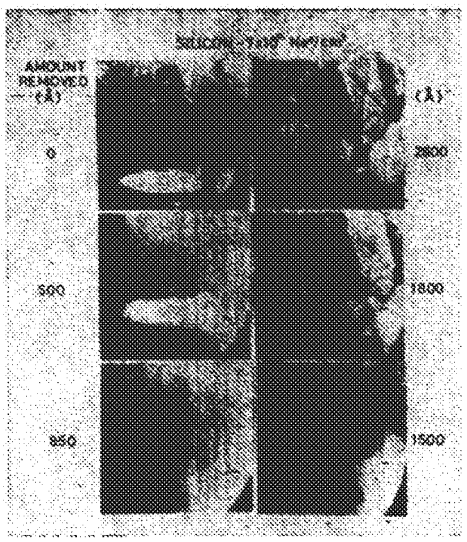


Fig. 30. SEM detection of depth distribution of damage in Ne-implanted Si.

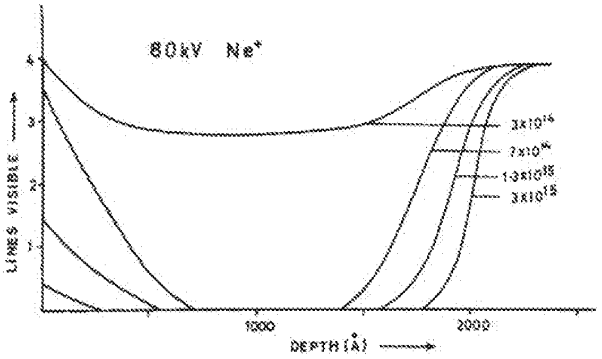


Fig. 31. Damage depth distribution obtained from Fig. 30.

These predictions fit the experimental results reasonably well, though the predicted width of the amorphous layer is greater than the experimentally observed width. The agreement can probably be improved by performing the implantations at low temperatures where the damage would be stable.

V. Annealing Characteristics of Ion-Implanted Silicon

It will be abundantly clear from the foregoing sections that ion-implanted crystals will normally contain a great deal of damage in the as-implanted state. If the purpose of the ion implantation is to introduce doping impurities, then this damage must be annealed in such a way that 1) implanted ions will be incorporated into electrically active (usually substitutional) sites in the crystal lattice and 2) residual defects are reduced to a level where carrier mobilities and lifetimes are usefully large. In this section we take up the topic of annealing, our first concern being to study the crystallographic perfection obtainable in annealed samples, as judged primarily by transmission electron microscopy. We will then review the electrical properties of annealed material and at-

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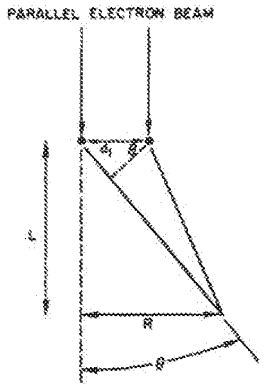


Fig. 32. Illustrating the Bragg condition for a pair of atoms separated by a distance d_1.

tempt to relate them to the crystallographic defects that remain after annealing.

A. Basic Characteristics of Transmission Electron Microscopy

One of the first techniques that was used to study damage in ion-implanted semiconductors and its annealing behavior was transmission electron microscopy. This technique permits one to study the nature of the crystalline-to-amorphous transition that may occur during bombardment, and to identify (at least in some cases) residual defects that are present after various annealing treatments. In this section we will discuss the type of information that is obtained from transmission electron microscopy and summarize the main characteristics of experimental patterns that are obtained from ion-implanted samples.

The complete interpretation of transmission electron microscopy is, of course, a very sophisticated topic. However, some of the most important characteristics of the electron diffraction patterns that are obtained from an ion-implanted sample can be understood as a superposition of two "limiting cases": the amorphous film and the perfect crystalline film. Our approach is therefore to present experimental patterns for these two cases, using the Bragg law to understand and interpret their general features. We then discuss intermediate cases in terms of these two.[16]

1) TEM in Amorphous Films: Two types of experimentally observed patterns are usually presented to describe the characteristics of a specimen. The first is called a diffraction pattern (or sometimes *scattering pattern*). It corresponds to low-power magnification in a light microscope and is obtained by projecting all of the electrons that emerge from the specimen onto the observation screen of the microscope. The other type of pattern is called a *bright (or dark) field micrograph*, and is obtained by permitting only those electrons that form a selected area of the diffraction pattern to reach the projection system of the microscope.

a) The diffraction pattern: A diffraction pattern for an amorphous film of silicon is shown in Fig. 11(b). The pattern consists of a central spot and a series of concentric rings, called Debye–Scherrer rings. The film from which this pattern was obtained was prepared by evaporating silicon onto a rock salt crystal at room temperature, and then dissolving the salt crystal in water.

To explain the characteristics of this pattern, it is useful to visualize an amorphous film as one in which there is no discernible periodicity in the arrangement of the atoms. Even in such a film, however, atoms will have nearest neighbors, next-nearest neighbors, and so on; and certain interatomic distances will occur with greater frequency than others. The Debye–Scherrer ring structure is a direct consequence of this fact.

The principal characteristics of the ring structure can be developed from an application of Bragg's law. For this purpose we show in Fig. 32 a pair of atoms separated by a distance d_1 and illuminated with a parallel beam of electrons. Constructive interference of the electron diffraction patterns from the individual atoms will occur on the image plane when the condition

$$\lambda = d_1 \sin \theta \tag{28a}$$

is satisfied, where θ is the angle at which constructive interference first occurs and λ is the wavelength associated with the electron's momentum.

A given ring on the Debye–Scherrer pattern is obtained by superposing the diffraction patterns obtained from all pairs of atoms with an atomic spacing d_1. Because the axes of these pairs are oriented at random with respect to each other, the Bragg condition will be satisfied at every point on the ring for at least some of the atom pairs.

For quantitative purposes it is customary to observe that, because $\lambda \ll d_1$, the Bragg condition reduces to

$$\lambda = d_1 \theta. \tag{28b}$$

Furthermore, because θ is small, we can also write

$$\tan \theta \cong \theta = R/L \tag{29}$$

where R is the distance from the center of the image plane to the point at which constructive interference occurs. Combining (28b) and (29) we find

$$R = \frac{L\lambda}{d} \tag{30}$$

which shows that distances in the image plane are reciprocal to distances in the object.

The quantitative relation between object and image distances given in (30) can be used to estimate average interatomic spacings, crystallite sizes, and other important properties of the film under observation.[17] For this purpose, a plot of intensity versus radius can be made by measuring the optical density of the diffraction pattern. An idealized result is illustrated in Fig. 33 for purposes of discussion. The distances to the intensity maxima (i.e., R_1, R_2, $\cdots$) give average interatomic spacings (d_1, d_2, $\cdots$), each of which is found by using (30).

If the film consists of a mosaic of small randomly oriented crystallites, a Debye–Scherrer ring pattern is still obtained in which the radial width of a ring [(ΔR) in Fig. 33] is related to

[16] The description of transmission electron microscopy given here is only intended to provide facts that are necessary to understand experimental results obtained on ion-implanted samples. A thorough discussion of the principles of TEM and the theory of interpretation may be found in R. Heidenreich, *Fundamentals of Transmission Electron Microscopy*, New York, Interscience, 1964.

[17] Actually, a Fourier analysis is required for exact calculation of interatomic spacings and crystallite sizes from a diffraction pattern. Distances estimated directly from a Debye–Scherrer pattern for one form of amorphous silicon are properly compared to those obtained for other preparations of amorphous silicon.

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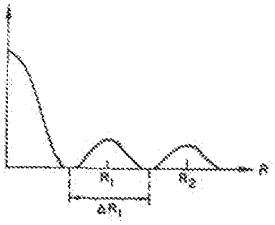


Fig. 33. Schematic illustration of optical density in a Debye-Scherrer pattern.

TABLE VI

AVERAGE INTERATOMIC SPACINGS IN EVAPORATED Si FILMS DEDUCED FROM DEBYE-SCHERRER RING PATTERN

	Ring 1	Ring 2	Ring 3
Richter & Breitling	3.22 Å	1.78 Å	1.18 Å
Crystalline Silicon	3.13 Å	1.92 Å	1.13 Å

the crystallite size Δ by the equation

$$(\Delta R) = \frac{2L\lambda}{\Delta} . \qquad (31)$$

From this relation it is clear that the width of the ring decreases with increasing crystalline size. Annealed silicon crystals exhibiting thin well-defined rings suggest that the annealed material has a number of grain boundaries within it.

It follows from this discussion that 1) in a truly amorphous structure (i.e., $\Delta \to 0$) it will be very difficult to distinguish the rings from each other; and 2) atoms in the evaporated silicon film represented in Fig. 11(b) must still possess *some* short-range order, since the ring structure is reasonably well defined.

A careful study of the Debye-Scherrer ring pattern obtained from evaporated Si films has been made by Richter and Breitling [41] who use the patterns to compute both average atomic spacings and crystallite sizes in their Si films. Their results on atomic spacing are shown in Table VI, together with the spacing between several prominent lattice planes in silicon for comparison. Richter and Breitling also concluded that the average crystalline size in the evaporated film was 10Å.

b) The bright field micrograph: The fact that electrons are scattered from the main beam into concentric rings, spots, or other features of the diffraction pattern, suggests that the central spot in the pattern will not be of uniform intensity. To study this possibility, it is customary to present a highly magnified portion of the central spot or *bright field micrograph*. Fine-scale fluctuations in the intensity of the central spot can then be studied in this highly magnified image.

A bright field micrograph taken from the central spot in Fig. 11(b) is shown in Fig. 34 and exhibits a generally speckled appearance with no evident structure. This is to be expected since the electrons that are scattered into the rings come from all parts of the main beam.

The dark-to-white contrast in such a figure can be reversed, and considerably greater sensitivity in measurement obtained, by employing what is called the *dark field* technique. For this purpose, the aperture which admits electrons into the projection system of the microscope is positioned so that only those electrons which are scattered into a specific area of one of the concentric rings are used to form the image. The arrangement is shown schematically in Fig. 35. In this configuration, the image will consist of a series of bright areas on a dark background, the bright regions locating those areas of the object from which the scattered electrons have come.

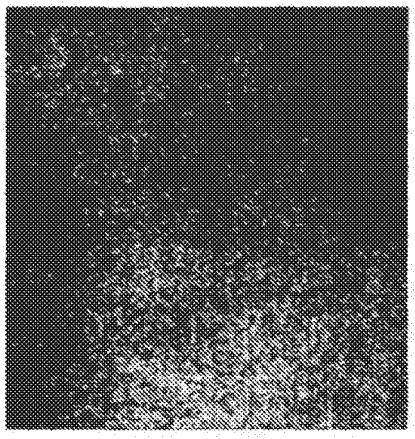


Fig. 34. Bright field image taken from central spot of the Debye-Scherrer pattern.

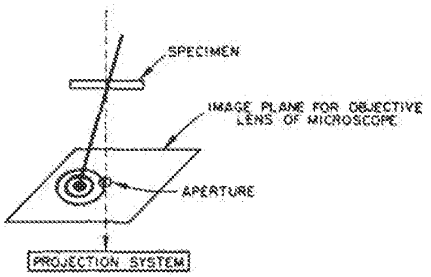


Fig. 35. Illustrating the arrangement for dark field microscopy.

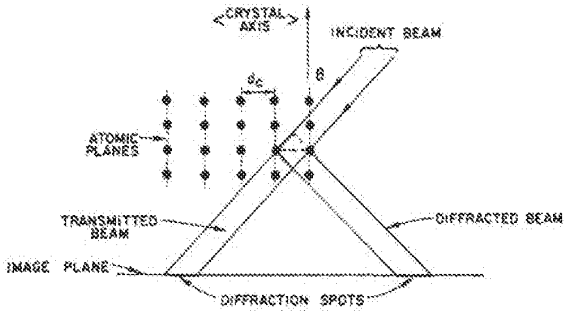


Fig. 36. Bragg condition for strong diffraction from atomic planes in a crystalline solid.

2) TEM in Crystalline Films: To turn to the other limiting case, we now consider the types of diffraction patterns that are obtained for a thin crystalline specimen.[18] To present the Bragg condition first, we show in Fig. 36 a schematic arrangement of crystal planes with spacing d_c, with a parallel

[18] In addition to the patterns described here, a thick specimen will also exhibit Kikuchi lines and bands.

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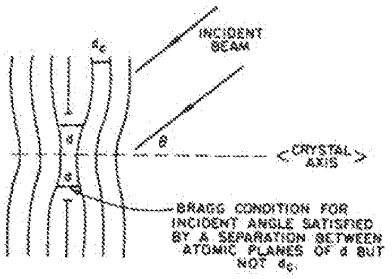


Fig. 37. Illustrating the dependence of Bragg condition on atomic spacing.

electron beam incident at an angle with respect to the crystal axis defined by the planes. As the figure suggests, electrons will be Bragg-diffracted from atoms in the various planes, with constructive interference occurring when

$$n\lambda = 2d_c \sin \theta. \tag{32}$$

The most evident features of the diffraction pattern for such a case will be a central spot together with a main diffracted spot (or spots). Subsidiary spots of less intensity may also appear, indicating that for the given θ a Bragg condition is also satisfied for higher order crystal planes.

Such a diffraction pattern is shown for a single crystal silicon specimen in Fig. 40 (region *B*). The corresponding selected area pattern taken from either the central spot or the diffracted spot shows a completely uniform electron intensity across the entire field of view.

On a coarse scale, the appearance of such a spot pattern gives a first indication that the specimen is crystalline. On a finer scale, the changes in the spot pattern that occur when the electron beam is swept through the Bragg angle are of considerable interest. For example, when θ is increased beyond the Bragg angle θ_B, all of the spots except the central one should disappear in a perfect crystal. However, if an imperfection is present in the crystal, the Bragg condition may be satisfied for the imperfection, even though it is not satisfied for the crystal as a whole.

A case of this type is the dislocation loop shown in Fig. 37. Here, the angle between the incident beam and the crystal axis is assumed to be smaller than that required by the Bragg condition. However, the Bragg condition is satisfied at a particular position along the dislocation, so some of the electrons that are illuminating the dislocation will be scattered out of the main beam. If the dislocation loop is sufficiently large (diameter ~50 Å) a bright field micrograph taken from the appropriate section of the central spot will then exhibit dark contrast along the line where the Bragg condition is satisfied.

B. Analysis of Ion-Implantation Damage Using Transmission Electron Micrographs

Using the foregoing ideas as a guide, we now briefly summarize the information on implantation-produced damage and annealing that has been obtained from TEM, beginning with the pioneering work of Mazey, Nelson, and Barnes.

1) Mazey, Nelson, and Barnes [42]: The experimental technique used by these authors was as follows: circular disks 0.3 cm in diameter and 500 μ thick were ultrasonically cut from polished single crystal slices of 5-Ω·cm n- or p-type silicon. The lapped slices were oriented so that a chosen crystal plane ([110], [111], or [100]) was within $\pm 1\frac{1}{2}°$ of the normal to the crystal surface. The samples were thinned for electron microscopy by drilling a saucer-shaped depression in the center of the disk and then chemically thinning the specimen from both sides with an $HF–HNO_3$ mixture. Thinning was carried out until perforation occurred in the central area.

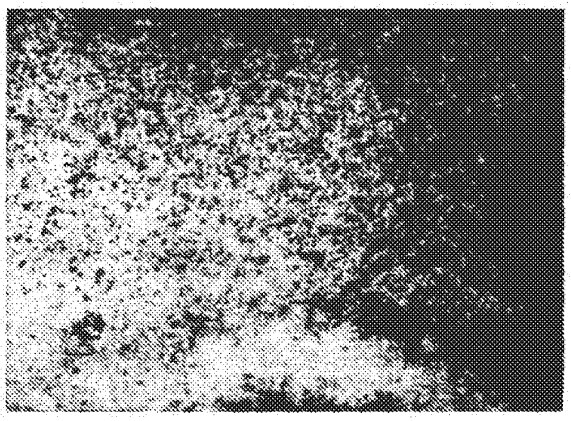


Fig. 38. Small regions of dark contrast appearing in Ne-implanted sample after a dose of ~10^{13} ions/cm^2.

The thinned samples were then bombarded at normal incidence with magnetically analyzed beams of various ions, including P^{28}, B^{11}, Ne^{20}, Si^{28}, and Xe^{136}. Various beam energies between 10 and 90 keV were employed, the target being held at room temperature in most cases.

a) Optical appearance of bombarded samples: During implantation, the part of the silicon being bombarded exhibited a continuous change in color, finally coming to a characteristic "milky" appearance for sufficiently large doses.[52] The milky regions were found to be slightly soluble in HF and could be removed. The amount of material removed for a dose of 36×10^{14} P^{31} ions/cm^2 at 40 keV was found by optical interference techniques to be 1100Å (see also Gibbons, Hechtl, and Tsurushima [54]).

b) Diffraction patterns and bright field micrographs for 80-keV Ne bombardment: Observations of both diffraction patterns and bright field micrographs were taken after progressive bombardment with 80-keV Ne ions, covering a dose range of 10^{13} to 10^{15} ions/cm^2 and encompassing the crystalline-to-amorphous transition. Selected diffraction patterns from these experiments are shown in Figs. 38 and 40.

Fig. 38 is a selected area pattern taken after a dose of 10^{14} Ne ions/cm^2. The figure shows small regions of dark contrast, having an average diameter of about 50 Å. The number of dark spots is ~$2–5\times10^{11}$/cm^2, which is much less than the ion dose. The diffraction pattern for this dose shows extra diffraction spots at low intensity, but no rings.

Increase of the dose to 10^{15} ions/cm^2 produces the changes summarized in Fig. 40. In Fig. 39 we illustrate the geometry of the thinned sample, including a mask provided by one of the bars of an overlying specimen support grid. In Fig. 40 we show an electron micrograph with diffraction patterns for each region inset in the figure.

Looking first at region *C*, we see that the diffraction pattern consists of three diffuse Debye–Scherrer rings, indicating that the material in this region is amorphous. Measurements

[52] A very clean sample bombarded in an oil-free vacuum of at least 10^{-8} torr will appear more nearly silver than milky.

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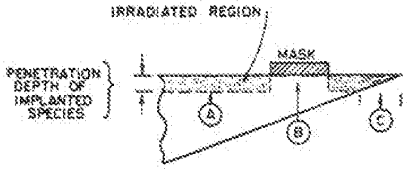


Fig. 39. Specimen geometry for electron microscope investigations of image.

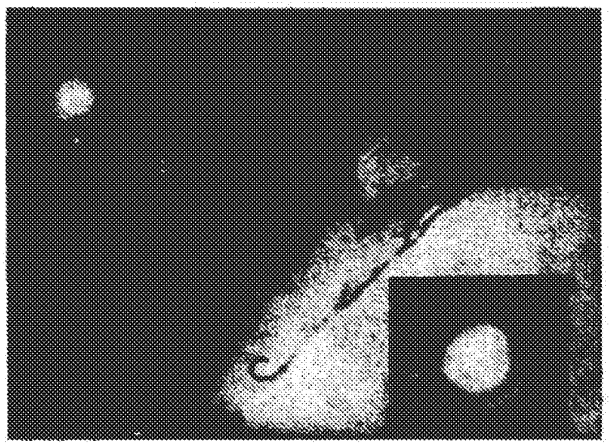


Fig. 40. Electron micrographs obtained from regions defined in Fig. 39 following implantation of 10^{15} Ne ions/cm^2 at 80 keV into a room-temperature Si target.

made on these rings give interatomic spacings that are identical to those of Richter and Breitling quoted earlier. By contrast, region *B* shows a diffraction pattern that is characteristic of single-crystal silicon, while region *A* shows both a spot pattern and a superposed ring structure. The nature of region *A* was further elucidated by inverting the specimen so that the electron beam was incident on the nonbombarded surface. The result is shown in Fig. 41, where concentric rings appear around both the central beams and all the strongly diffracted beams. This figure is clearly a superposition of the patterns obtained in regions *B* and *C*.

c) Annealing behavior of the damaged regions: After studying the as-implanted samples, Mazey *et al.* performed a series of annealing experiments, aimed primarily at elucidating the nature of the recovery of a sample which had been bombarded with sufficient dose to drive the surface layers of the sample amorphous.

Their results may be summarized as follows.

i) The individual zones (dark regions in Fig. 38), that are observed in a low dose implant, disappear when the silicon is annealed to a temperature in the the range 400–500°C. More recent work by Matthews [26] suggests that the individual zones give dislocation loops upon annealing.

ii) Recrystallization of a layer that is driven amorphous by the bombardment does not occur until about 630°C.

iii) If the amorphous layer is formed on single-crystal material, as in region *A* of Fig. 39, the recrystallization occurs epitaxially on the underlying substrate, with a large number of dislocation loops and dipoles being formed during the recrystallization. The epitaxial character of the recrystallization is inferred from the fact that the diffraction pattern returns to a crystalline spot pattern, but some of the spots are split and faint streaking is present, similar to that observed in the diffraction pattern of a conventional vapor-deposited epitaxial layer.

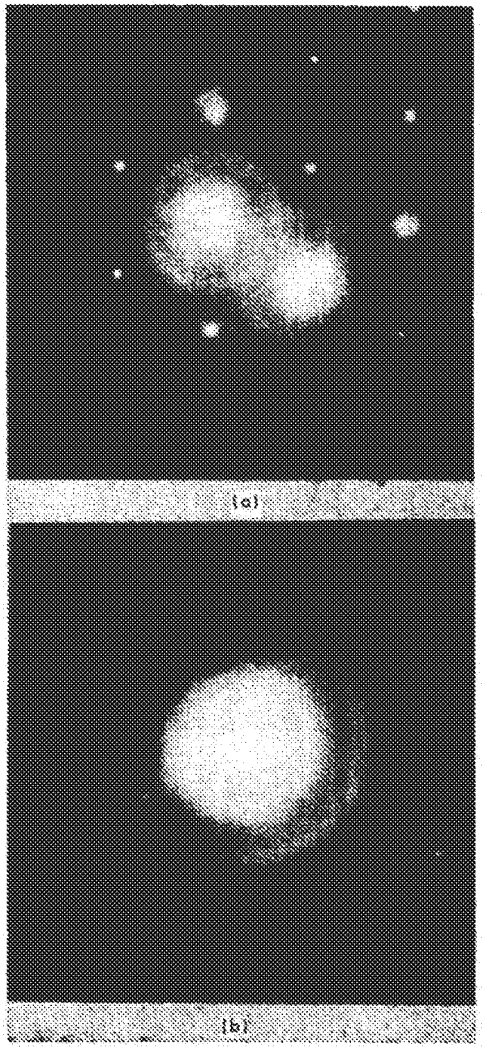


Fig. 41. (a) Region *A* in Fig. 39 illuminated from unbombarded side of specimen. (b) Region *A* illuminated normally.

iv) The dislocation loops become larger as the annealing temperature is progressively raised to 850°C. Such loops characterized all samples investigated by Mazey *et al.* after ion doses of $\geq 3 - 10^{14}$ cm^2, at all energies between 10 and 90 keV, irrespective of the ion species used. A representative loop distribution is shown in Fig. 42 for bombardment of 3×10^{15} B ions/cm^2 at 40 keV, followed by a 4-h anneal at 800°C.

v) In region *C*, where the ion range is greater than the sample thickness, recrystallization of the amorphous material produces a large number of randomly oriented crystallites. The diffraction pattern for this case shows numerous spots in well-defined rings, the lattice spacings of which are the same as those of crystalline silicon.

d) Hot-implant studies: Mazey *et al.* also reported on one series of experiments performed to study the nature of the damage produced when the silicon target was held at high temperature during the implantation. Two sample temperatures, 200 and 510°C, were chosen, and samples held at these temperatures were bombarded with Ne. It was found that a

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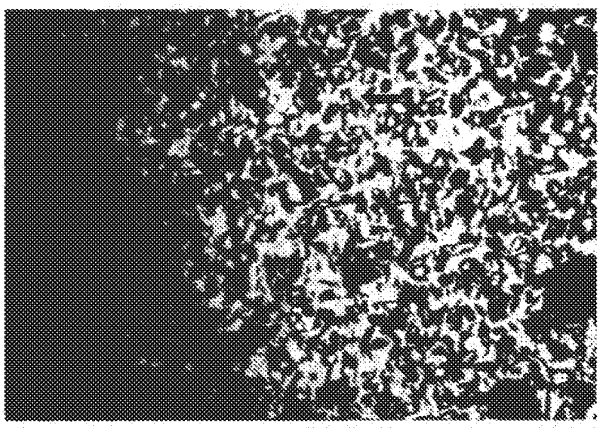


Fig. 42. Bright field micrograph showing dislocation loops and dipoles following implantation of 3×10^{15} B ions into [111] Si at room temperature. Sample annealed for 4 h at 800°C.

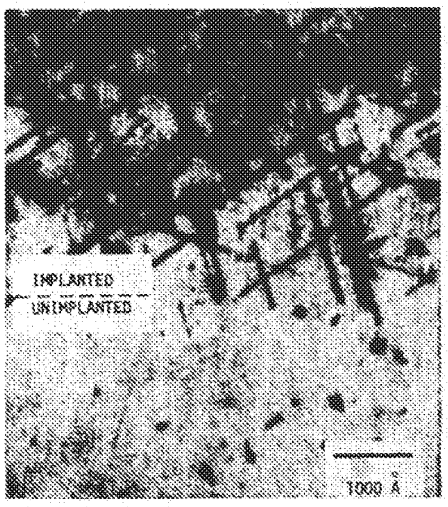


Fig. 43. Rod-like defects observed following B implantation and annealing. For details see Chadderton and Eisen [44].

dose of $\sim4\times10^{15}$ ions/cm² implanted at 30 keV was *not* sufficient to drive the silicon amorphous, at either temperature. However, a dense dislocation entanglement was observed in both cases.

2) Bicknell [43] *and Bicknell and Allen* [51]: These authors employed electron microscopy to study the defect structures that are formed in annealed boron-implanted silicon. Studies were performed on silicon implanted at room temperature with between 10^{14} and 10^{16} boron ions/cm² at energies of 20, 50, 75, and 100 keV. Electron micrographs were taken on both as-implanted samples and after annealing at a temperature in the range 580–780°C for half an hour.

In general, the experimental results of Bicknell and Allen agree with those of Mazey *et al.*, with the following new features:

a) During the annealing, many loop dislocations lying on {111} planes form in the implanted layer, and in specimens implanted at *room temperature* these loops are also accompanied by long straightedge dislocations running in all the ⟨110⟩ directions. However, these long rod-like structures do not appear in samples implanted with phosphorus even though many more loops are produced.

b) Using anodic stripping, the depth distribution of loops was measured for a dose of 2×10^{15} B^{11} ions/cm² implanted at 50 keV into a silicon target held at 280°C during the bombardment. By this means it was found that the loop defects were confined to a layer lying between 1000 and 2500 Å beneath the surface, with the majority of loops lying between 1000 and 1500 Å. For comparison, computations of the energy deposited into atomic processes by Brice show that the maximum damage should occur at a depth of approximately 1150 Å.

c) The rod-like defect structures, which can be as long as 1 μ, extend outside this layer. Electron micrographs of these rods, taken from the very thorough study of boron-implanted Si by Chadderton and Eisen [44], are shown in Fig. 43.

d) The rod-like structures do not appear if the implantation is performed at a target temperature of 280°C, though loops are still formed whose character was ascertained to be of both the interstitial and vacancy type.

e) Under all implant conditions, the loops decrease in number and increase in size from about 100 to 1000 Å as the samples are annealed progressively to 780°C.

3) Davidson [21]: A further TEM study of damage produced during ion implantation was carried out by Davidson with the specific objectives of determining how the residual defects in annealed samples could be related to parameters such as the irradiating ion, dose, and annealing treatment.

TABLE VII

Ion	Dose (ions/cm²)	Annealing Temperature 700°	800°	900°
B*	10^{14} – 10^{15} 10^{15} – 2×10^{16}	rod-like defects ⟨110⟩ ——→ large loops very many small loops (100Å)		
Al*	10^{14} – 10^{15} 10^{15} – 2×10^{15} $> 2\times10^{15}$	loops (250Å), many on {111} many small loops (100Å) ——→ dislocations N.I.S.		
P*	10^{15} – 4×10^{15} $> 4\times10^{15}$	very small defects (50–100Å) N.I.S.		
P*	10^{14} – 2×10^{15} $> 2\times10^{15}$	mostly large (400Å) loops on {111} N.I.S.		
Sb*	5×10^{13} – 2×10^{14} $> 2\times10^{14}$	small loops (50–200Å), poss. also ppts. N.I.S.		
Ne*	10^{14} – 6×10^{14}; 6×10^{14} – 2×10^{15} $> 2\times10^{15}$	rod-like defects ⟨110⟩ ——→ large loops many small loops ——→ dislocations N.I.S.		
Si*	$> 2\times10^{15}$	N.I.S.		

The samples used by this author were (111) polished silicon slices, both n- and p-type, with resistivities in the range 5–10 Ω·cm. These samples were irradiated at room temperature with B, Al, N, P, Sb, Ne, and Si ions, using energies in the range 40–100 keV. Disks suitable for the electron microscope specimen holder were then cut from the irradiated areas, annealed in an atmosphere of flowing nitrogen at temperatures up to 1000°C, and jet thinned to transparency in the central region.

Various types of defects were observed, using both bright- and dark-field techniques to elucidate their structure. Table VII gives a resume of the results obtained, relating defect structure to ion type, dose, and annealing temperature. Inspection of the table leads to the following conclusions:

a) In agreement with Bicknell, long (2-μ) rod-like defects

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are seen in boron-implanted samples implanted at room temperature. The new feature here is that the rods disappear when either 1) the dose is sufficiently high or 2) annealing is carried out at 900°C, as compared to Bicknell's maximum reported temperature of 780°C.

b) Rod-like defects were also obtained for Ne implants, so long as the dose remained below 6×10^{14} ions/cm^2.

c) Rod-like structures do not appear except for the lower dose Ne and B implants. Davidson suggests that the relative chemical *in*activity of these ions in an ordered silicon lattice may be responsible for the formation of the rod-like structures. On account of their size it is possible that these ions serve as effective clusters for dislocation line pinning.

d) With higher dose implants, all ions show many small loops or unidentified defects, having a size of 50–100 Å (except for phosphorus) and in some cases annealing into identifiable dislocations as the annealing temperature is raised to 900°C.

e) For every ion except boron, the highest doses employed produced a highly irregular structure in annealed crystals, denoted in the table by the symbol HIS. It is to be expected that a sufficiently high dose of boron would also give this result.

The crystallographic character of the highly irregular structure is elucidated in Figs. 44 and 45. Fig. 44 shows a diffraction pattern containing a large number of thin broken rings. This indicates the presence of a number of relatively large crystallites, suggesting that the regrowth of the damaged layer on the underlying substrate was not epitaxial in the usual sense. The dark field micrograph, shown in Fig. 45, shows white patches distributed over the entire area of the sample, indicating that the crystallites responsilbe for the ring pattern are distributed throughout the recrystallized material.

Taken together with the results of Mazey *et al.*, who observed essentially complete recovery of the transmitted image for somewhat lower doses (but still sufficient to produce an amorphous layer), one is lead to conclude that there are "degrees of amorphousness" insofar as epitaxial regrowth of the damaged layer is concerned. When too much disorder is introduced, the regrowth is more nearly polycrystalline.

This result is of practical significance for the following reason: we will see in the next paragraph that a high percentage of an implanted species is incorporated into electrically active sites if the target is driven amorphous before it is annealed. The HIS result suggests that other properties of the recrystallized layer, perhaps including even electrical activity of the implanted species, will be critically affected by the *dose* (and perhaps dose rate) of the ion that is used to make the target amorphous.

C. Electrical Characteristics of Annealed Material

By now a great deal of experimental data has been published concerning the electrical characteristics of well-annealed ion-implanted silicon. Most of these data have been obtained by studying the *majority carrier* properties of an ion-implanted layer with a view toward determining the annealing conditions under which 1) a large fraction of the implanted species can be incorporated into electrically active (usually substitutional) sites and 2) values of majority carrier mobility that are comparable to those in appropriately doped bulk material can be obtained.

Briefly stated, the results of all of these experiments lead to the following conclusions:

a) If the silicon is driven amorphous from the surface to a depth D *before* annealing (either by the implanted ions themselves or by a suitable dose of Si or other inert ion), then a 650°C 30-min anneal will recrystallize the amorphous layer epitaxially (though the regrown layer may perhaps exhibit microtwins and stacking faults). Measurements of differential carrier concentration and Hall mobility using anodic sectioning techniques show that for B, P, As, Sb, and Bi a large proportion of the ions within the regrown layer are incorporated into substitutional electrically active sites, even for peak concentrations in excess of 10^{20}/cm^3. Furthermore, very little motion of the implanted species occurs during regrowth, so if the silicon is made adorphous before the impurity ions are implanted (by pre-implanting Si, for example), the range distribution will be close to that predicted by LSS.

b) If the silicon is not driven amorphous before annealing, less electrical activity usually results. The exact effect depends on the ion and the annealing conditions, with boron being one of the most notorious—between 50- and 100-percent activity if the amorphous condition is reached prior to annealing and frequently less than 10 percent otherwise. *Negative annealing* (i.e., a decrease in carrier concentration with an increase in annealing temperature) is frequently observed in the 500–700°C temperature range, though reasonable electrical ac-

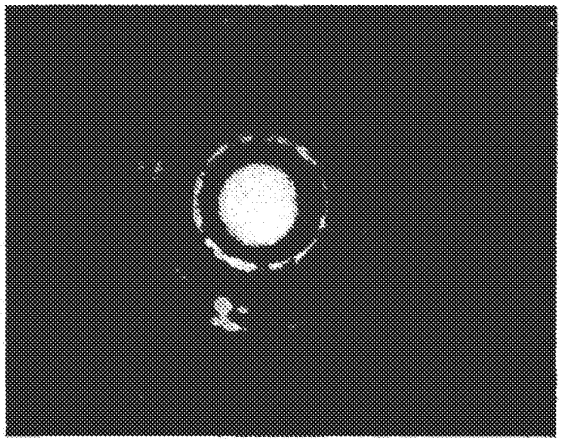


Fig. 44. Transmitted image of heavily bombarded Si annealed for 4 h at 900°C. Thin broken rings denote twinning in regrowth of amorphous layer.

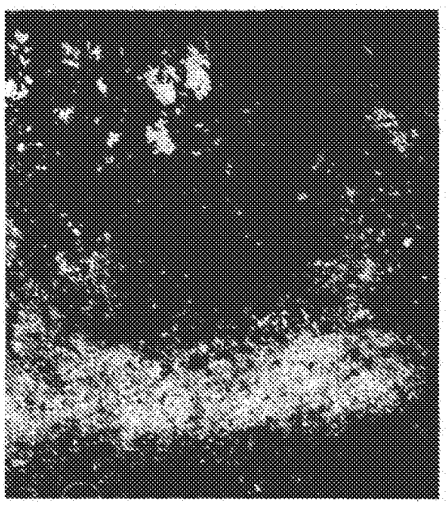


Fig. 45. Dark field micrograph taken from major ring of Fig. 44.

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tivity can still be obtained if annealing is performed at temperatures in the 800–900°C range.

c) Even when the silicon is driven amorphous to a depth D, there will be a portion of the crystal beyond the amorphous layer that is heavily damaged but not amorphous. In this transition region, the majority carrier electrical properties will be trap dominated until an annealing temperature of 800–900°C is reached. Important minority carrier trapping effects may persist to even higher annealing temperatures.

In what follows we concentrate primarily on the experimental evidence that supports these conclusions, giving only a brief discussion of proposed explanations for low electrical activity at the end of the section.

1) Influence of the Amorphous Phase: The first work to clearly point out the importance of the amorphous phase in obtaining high electrical activity appears to be that of Blamires *et al.* [45], while the most thorough experimental treatment available is that of Crowder [46]. A key paper has also been published by Davies [55], who pointed out the advantage that could be obtained by implanting boron ions at a low temperature (−195°C), where light-ion damage is stable and the ions themselves can make the silicon amorphous. We review these papers first to justify conclusions a) and c) above.

a) Blamires, Matthews, and Nelson [45]: These authors first studied the effect of various annealing treatments on samples that had all been implanted with boron to a dose of 10^{15} ions/cm^2 at an energy of 40 keV. The implant was performed at room temperature, after which separate samples were then annealed for 30 min at 630°, 800°, and 1000°C. Fig. 44 shows the carrier density profile resulting after each of these annealing steps, from which it is clear that less than 4 percent of the implanted ions are electrically active after the 630°C annealing step. The percentage of boron ions that find their way to electrically active sites increases as the annealing temperature is increased, ultimately reaching about 60 percent after a 30 min, 1000°C anneal, though there is also very considerable impurity redistribution occurring due to thermal diffusion.

The importance of the amorphous condition is shown in a second experiment, which consisted of implanting Ne at a dose of 10^{15} ions/cm^2 and energy of 80 keV into a room-temperature sample that had already been implanted with 10^{15} boron ions/cm^2 at 40 keV (as previously). The neon-implanted sample was then annealed at 630°C for 30 min, after which anodic sectioning measurements gave the carrier density profile shown by the heavy solid line in Fig. 46. The percentage activity has risen to about 20 percent from the previous value of 4 percent, and the carrier density is approximately Gaussian with parameters that are predicted by the LSS theory.[16]

The data of Davidson and Booker (Fig. 34) show that the neon implant has driven the silicon amorphous to a depth that will include most of the boron ions in the amorphous layer; following this step, epitaxial regrowth has incorporated a large proportion of these ions in electrically active sites.

b) Crowder [46]: This author implanted all commonly used Group III and V elements into both crystalline and amorphous silicon targets, annealed the implanted samples at 600°C for 30 min, and then measured carrier density and mobility profiles by differential conductivity and Hall-effect techniques. For intermediate to heavy ions, such as P, As, Sb, and Bi, the ion doses used were themselves sufficient to drive the crystal amorphous to a depth that included most of the implanted ions. For light ions, an amorphous phase was prepared on crystalline silicon by implanting 10^{15} Si ions/cm^2 at an energy of 300 keV, this treatment rendering the silicon amorphous to a depth of $\sim 0.6\ \mu$.

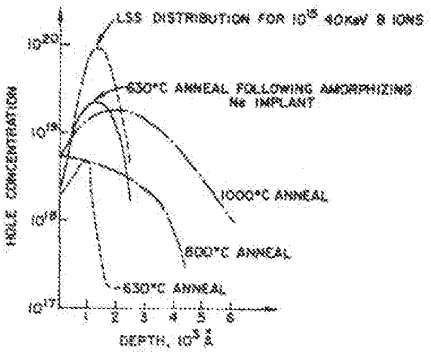


Fig. 46. Hole concentration profiles obtained following various annealing treatments. For details consult Blamires, Matthews, and Nelson [45].

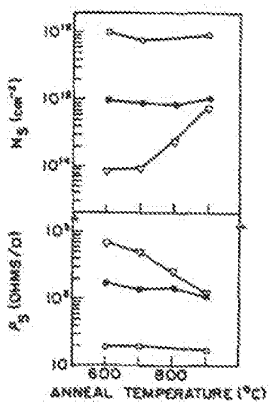


Fig. 47. N_s and ρ_s versus annealing temperature for 120-keV B^{11} implanted into amorphous Si (filled circles: 10^{15} ions/cm^2) and into crystalline Si in a random direction (open triangles: 10^{15} ions/cm^2). The implanted B dose for open circles was 1×10^{15} ions/cm^2. All implantations were conducted at room temperature.

The effect of the amorphous layer is again most clearly apparent in the case of boron, as shown in Fig. 47. Here the sheet carrier density (number of holes per square centimeter) is plotted against anneal temperature for doses of 10^{15} and 10^{16} boron ions/cm^2 implanted at an energy of 120 keV. Essentially 100-percent electrical activity is obtained for implants into an amorphous target following a 600°C 30-min anneal, while a 900°C anneal is necessary to obtain 100-percent activity if the boron is implanted into a room-temperature crystalline target. These results also agree well with those of Davies [55], who is able to obtain an amorphous phase prior to annealing by implanting 10^{15} B ions/cm^2 into a silicon crystal held at −195°C, after which a 600°C 30-min anneal is sufficient to achieve essentially 100-percent electrical activity.

A second point of interest, leading to conclusion c) stated above, is seen in the carrier concentration profile obtained by Crowder for P ions implanted into amorphous silicon at an energy of 280 keV (Fig. 48). At this energy about 5 percent of

[16] More recent experiments suggest that an even higher percentage electrical activity would have resulted had the amorphizing implantation been performed with Si ions. See for example Bauer [56].

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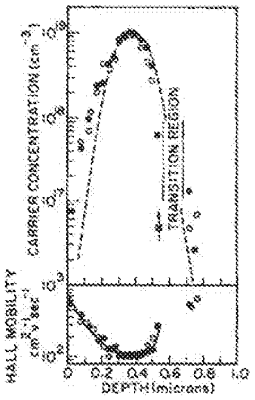


Fig. 48. Depth variation of the carrier concentration and Hall mobility for amorphous Si implanted with 3×10^{14} 280-keV P^{31} ions/cm². The depth of the amorphous Si layer was determined by interface fringes in optical absorption spectra as shown by the arrow. After implantation, the wafers were annealed at 600°C for 30 min. The dashed line represents a Gaussian approximation to the ion profile. The solid line represents the mobility computed for bulk Si of comparable resistivity.

the implanted ions should come to rest beyond the amorphous layer. The variation of conductivity and Hall coefficient after a 600°C 30-min anneal show that all implanted phosphorus ions are in electrically active sites in the regrown amorphous layer ($0<x<0.6\,\mu$); but beyond this point there is a region of high resistivity in which sheet resistance and Hall coefficient remained constant as layers were removed. After passing through this transition region, normal behavior was again obtained. Crowder interprets the transition region as being a heavily disordered layer in which defects that have not fully annealed after a 600°C 30-min treatment compensate the implanted phosphorus ions. Normal electrical activity is obtained in the transition region after a 900°C 30-min anneal [47].

For practical applications of ion implantation, the following conclusions drawn by Crowder are especially useful:

i) For Sb, Bi, Al, and Ga, all of which have a low solid solubility at elevated temperatures, the maximum electrically active fraction is obtained by annealing at temperatures near 600°C, where epitaxial regrowth of the amorphous layer occurs. Higher annealing temperatures reduce the electrically active fraction.

ii) For P, As, Sb, and Bi, essentially 100-percent electrical activity is obtained for ions lying in the regrown region up to peak concentrations of 10^{20}/cm³ ($2\text{–}4\times10^{20}$/cm³ for P, As, and Sb).

iii) Of all Group III elements implanted, only B could be obtained electrically active and uncompensated at high concentrations ($2\text{–}4\times10^{20}$/cm³), following implantation into amorphous Si and annealing at 600°C.

2) Electrical Activity in Implanted Layers that are not Driven Amorphous Prior to Annealing: We turn now to a review of studies that illustrate and analyze both the low electrical activity and the reverse annealing effects that can occur when the silicon is not driven amorphous. We concern ourselves with boron, phosphorus, and arsenic implants into room-temperature silicon targets on account of the importance of these ions in practical applications.

a) Seidel and MacRae [49]: The effects to be described are most apparent for boron-implanted silicon, which has been thoroughly studied by Seidel and MacRae. Their experiments were performed by implanting 150-keV boron ions at doses of 8×10^{12}, 10^{14}, and 10^{15} ions/cm² into a room-temperature silicon target and then carrying out both isochronal and isothermal annealing experiments. The results of the isochronal experiments are shown in Fig. 49, where the total fractional activity (p/Φ = number of holes/cm³/dose) is plotted as a function of temperature. 30-min annealing intervals were employed at each temperature.

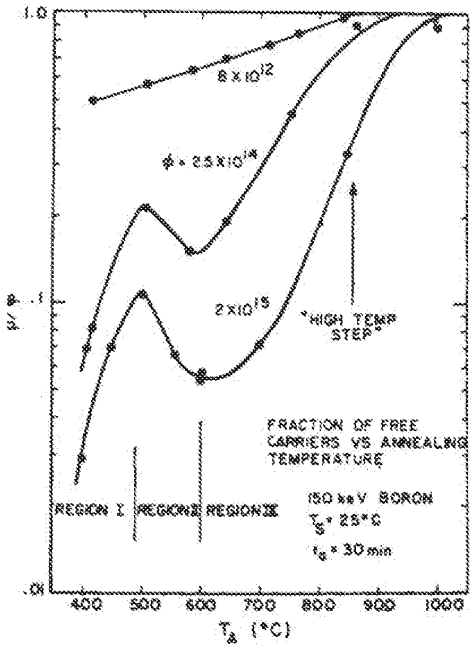


Fig. 49. Isochronal annealing data of Seidel and MacRae [47]. Implanted species: 150-keV B. Annealing time is 30 min.

To discuss the data, Seidel and MacRae divide the temperature axis into three distinct regions, as indicated on Fig. 49, and make the following remarks about the separate regions:

i) In region I, the increase in p with temperature arises from the annealing of compensating damage clusters. This conclusion follows from the fact that the boron substitutional density as measured by channeling techniques decreases slightly, and the carrier mobility as measured by Hall effect is very low.

ii) In region II, the region of negative annealing, the mobility rises to bulk values, and the substitutional boron concentration decreases markedly [48]. An interesting feature in region II is that, after an anneal of 600°C, the carrier mobility corresponds to the value expected for the ionized impurities only. The inactive boron ions evidently occupy sites where they are uncharged and therefore cannot scatter carriers effectively.

iii) In region III, all of the boron ions become electrically active and $p/\Phi\rightarrow1$ for annealing temperatures on the order of 900–1000°C.

It is also interesting to note that both the amount of negative annealing and the temperature for 90-percent electrical activity are functions of the dose. In particular, at a dose of $\sim10^{13}$ ions/cm², no negative annealing occurs, a fact that is useful for applications of low-dose boron implants.

From their isothermal data, Seidel and MacRae extract an activation energy of 5 eV for the annealing process and

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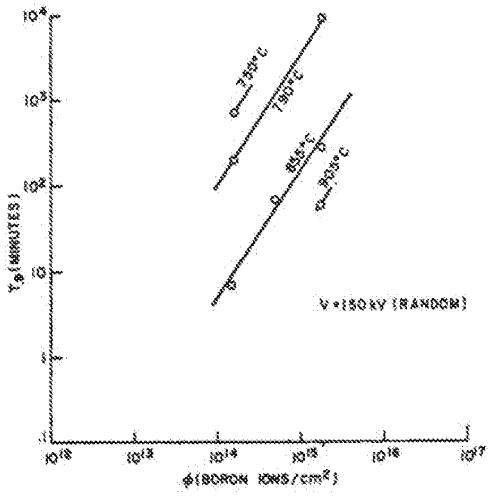


Fig. 50. Dependence of anneal time on dose. The time required to reach 90 percent of full activity, $T_{0.9}$, is plotted against dose of 150-keV B ions.

also determine the time required for the annealing to advance to a stage where 90 percent of the injected ions are electrically active. A very useful plot of these latter data is shown in Fig. 50, where the time for 90-percent electrical activity is plotted against dose with anneal temperature as a parameter. A horizontal line representing 30-min annealing time can be superimposed on their figure to facilitate comparison with the isochronal data given in Fig. 49.

Seidel and MacRae are able to interpret their data by assuming that first-order annealing kinetics apply, but that the annealing time constant is a function of the damage level; i.e., the annealing time for a fixed-percentage electrical activity in a region of high damage is longer than that for a region of low damage. Support for this viewpoint is lent by the fact that the best fit for their data is obtained with a spatial distribution of annealing time constants that has its maximum displaced toward the surface by an amount that is consistent with the damage distribution theory presented in Section IV.

b) Crowder and Morehead [61]: Turning our attention now to phosphorus implants, we first review the work of Crowder and Morehead, who studied the anneal behavior of 260–300-keV P implants into a nonchanneling direction in a room-temperature silicon target, with doses covering the range from 3×10^{13} to 5×10^{15} ions/cm^2. At the lower end of this dose range, the damage produced by the phosphorus ions is insufficient to create a continuous amorphous layer (*cf.* Section III-E), and results similar to those of Seidel and MacRae are obtained. In particular:

i) For doses *less* than 3×10^{13} P ions/cm^2, Crowder and Morehead obtain "substantially complete electrical activity" following a 30-min anneal at 600°C. (Compare this result with the data of Siedel and MacRae, who obtain 65-percent electrical activity for a dose of 8×10^{12} B^{11} ions/cm^2, following a 30-min 600°C anneal.)

ii) For doses between 3×10^{13} and 3×10^{14} P ions/cm^2, a 30-min 550°C anneal produces only about 5–10-percent electrical activity. However, the electrically active fraction increases as the anneal temperature is increased, with the final result that 90 percent of the implanted ions are electrically active after a 30-min anneal at a temperature between 800 and 900°C. Generally speaking, in this dose range, the lower the dose the lower the anneal temperature that is required to obtain a given percentage electrical activity.

iii) For doses greater than about 10^{15} P ions/cm^2, at least 80 percent of the implanted ions are electrically active following a 30-min 600°C anneal, as is expected from the fact that these doses are sufficient to drive the silicon amorphous.

Crowder and Morehead obtained completely similar results with As implants, with the dose for a given effect being lower for As implants than for P implants due to the fact that the damage produced by individual As ions is greater than that produced by individual P ions. Briefly, their results for As implants were as follows. For doses in the range of 3×10^{13} to 3×10^{14} As ions/cm^2, the silicon is not driven amorphous and low fractional electrical activity is obtained until relatively high annealing temperatures are used. As a case in point, Crowder and Morehead obtain about 10-percent electrical activity for a dose of 10^{14} As ions/cm^2 following a 30-min anneal at 550°C. The electrical activity increases to about 20 percent at an anneal temperature of 600°C and reaches about 75 percent at an anneal temperature of 800°C. For doses greater than 3×10^{14} As ions/cm^2, a continuous amorphous layer is produced and high electrical activity results when the sample is annealed at 600°C for 30 min.

c) Andersson and Swenson [62]: Experiments that generally confirm the results of Crowder and Morehead, and in addition shed some light on the physical processes taking place during annealing, have been performed by Andersson and Swenson. These authors studied the annealing behavior of 50-keV P implants into a room-temperature silicon target over a dose range of 10^{13} to 10^{15} P ions/cm^2, employing annealing temperatures in the range of 450° to 750°C. Following a 30-min 600°C anneal, they find a fractional electrical activity of ~50 percent for a dose of 10^{13} ions/cm^2; 15 percent for a dose of 10^{14} ions/cm^2; and 40 percent for a dose of 10^{15} ions/cm^2. (This last percentage does not disagree with the 80-percent figure obtained by Crowder and Morehead, since the quantity measured by Andersson and Swenson is sheet carrier density. For a 10^{15} cm^2 50-keV P implant, 40-percent sheet carrier activity actually corresponds to about 80-percent of the implanted ions in substitutional positions, since the implanted silicon will be heavily degenerate under these implantation conditions.)

Andersson and Swenson also measured sheet carrier density and carrier mobility as a function of temperature from 75 K to room temperature, and on the basis of these measurements they concluded the following.

i) Scattering centers with a compensating electrical activity are annealed in the temperature range from 450 to 550°C, because both the mobility and the sheet carrier density are found to increase in this range.

ii) At annealing temperatures above 500°C, phosphorus atoms are being incorporated into electrically active sites, since the sheet carrier density rises while the mobility decreases significantly.

These observations are in general agreement with those of Seidel and MacRae, though there is no evidence of negative annealing in the work of Andersson and Swenson.

From the standpoint of electrical activity, the pattern that emerges from all of the foregoing experiments is as follows. For low doses (and therefore low-volume concentrations of the injected ion), between 50 and 70 percent of the implanted ions can be incorporated into substitutional sites following a 30-min anneal at temperature of ~600°C. 90-percent elec-

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trical activity can be obtained by increasing the annealing temperature to 800–900°C. As the dose is increased, the electrically active fraction at any given anneal temperature *decreases*, though 90-percent activity can still be obtained if the annealing is carried out at a sufficiently high temperature for an adequately long period of time (cf. Fig. 50). Finally, if the implantation conditions are such as to produce a continuous amorphous layer, high electrical activity is obtained following a 600°C 30-min anneal, at least for those ions that lie within the regrown layer.

3) Characteristics of Annealed Layers that are Subjected to Further Bombardment: Insight into the conditions that produce negative annealing and the annealing mechanisms that operate during the low-temperature recovery of a damage layer has been provided by the experiments of Johnson [27], which we summarize here to round out our picture of annealing phenomena. Johnson's experiment, shown schematically in Fig. 19, consisted of introducing damage (by Si bombardment) into a previously implanted layer that had been well annealed. In addition to the estimate of cluster size described earlier, Johnson had an established starting point from which he was able to follow the course of the annealing at low temperatures; and he was also able to independently adjust the *position* of peak damage relative to the position of peak impurity density by an appropriate selection of energies. The results of his experiments with regard to damage annealing may be summarized as follows.

a) An annealing step occurs at a temperature of 150–200°C, which can be identified with the annealing of a vacancy-impurity pair (cf. Fig. 4). This result was obtained for B-, P-, and As-implanted layers.

b) Negative annealing is obtained when there is a reasonably close match of the damage and doping profiles, but not otherwise. In all cases where negative annealing was observed, the negative annealing was brought to completion by a 30-min anneal at a temperature in the range of 400–600°C.

c) In addition to the negative anneal, there is a smooth anneal that is apparent throughout the 200–700°C temperature range, leading to a final recovery of conductivity that is about 60 percent complete at an anneal temperature of 700°C (i.e., 60 percent of the loss of conductivity following Si bombardment is recovered following a 30-min 700°C anneal).

Johnson interprets the smooth anneal as a recrystallization of damage clusters that have a distribution in size, an interpretation that is in qualitative agreement with the recrystallization temperature estimates of Nelson shown in Fig. 10.

4) Possible Explanations for Negative Annealing: We conclude this section with a brief speculation as to why a match between damage and impurity profiles should be a cause of negative annealing. Two mechanisms have so far been proposed. From their observations of changes in the interstitial Si and B concentrations made by channeling measurements, North and Gibson [48] suggest that reverse annealing is due to a Watkins replacement mechanism, in which the silicon interstitial ions that promote the replacement (see Fig. 2) are obtained from the annealing of damaged clusters.[38] This is an attractive explanation, but does not clearly account for the concentrations dependence of the phenomenon.

An alternate explanation has been proposed by the author [49], who suggests that dislocation lines and loops formed during annealing may provide sites for the preferential adsorption of implanted ions, especially when there is a significant size mismatch between the implanted ion and the host atom. The physical basis for the model is suggested in Fig. 9, where it is seen that wrong-sized atoms will be preferentially adsorbed on dislocation loops to minimize the strain energy.

To give a semiquantitative estimate of the probable importance of this effect, we employ a formula derived by Hirth [50] from which one can estimate the number of impurity atoms N that will be adsorbed on a dislocation loop of length L in thermal equilibrium, the formula being

$$N = \left(\frac{\pi}{2}\right)\left(\frac{\beta}{kT}\right)^2 CL \ln \frac{R}{r} \tag{33}$$

where

R radius of the dislocation loop;
r equilibrium distance between host atoms;
C average concentration of impurity;

and

$$\beta = \frac{2\mu b_e}{3\pi}(v_s - v_a). \tag{34}$$

In (34), v_s is the volume of a solute atom, v_a is the volume of a host atom, b_e is a Burgers vector whose magnitude is approximately equal to the interatomic spacing in the crystal, and μ is a shear constant. Some especially interesting features of (33) are that the number of adsorbed impurity atoms is proportional to the impurity concentration, inversely proportional to the square of the absolute temperature, and proportional to the square of the difference in volumes of the two atomic species.

If we assume that damage clusters do not overlap, and that each implanted ion produces a 100-Å-diam dislocation loop after annealing, then the fractional number of impurity atoms adsorbed per unit volume is

$$\frac{n}{C} = 0.16 \times 10^{-18} C(r_s^3 - r_a^3)\left[\frac{900}{T(\mathrm{K})}\right]^2 \tag{35}$$

where r_s and r_a are the radii of the impurity and silicon atoms, respectively. The assumption of nonoverlapping damage clusters makes the result applicable primarily to moderate dose implants; to hot implants; or to the heavily damaged transition region between an amorphous layer and an underlying crystalline substrate. However, within these limitations theory fits experiment reasonably well. In particular, the results of Blamires *et al.* quoted earlier show that the electrically inactive fraction decreases from 0.96 to 0.81 to 0.43 as the temperature is increased from 600 to 800 to 1000°C. According to (35), the product of the inactive fraction and the (absolute temperature)^2 should be constant, a prediction that fits the data reasonably well. The concentration dependence also fits the isochronal data of Seidel and MacRae at anneal temperatures in the range of ~600–900°C when the spatial distribution of implanted ions is included in the estimate. A correlation with their isothermal data is more difficult to make, because it is difficult to include changes in total dislocation loop length that will occur for long anneal times.

Application of the adsorption theory to other ions is contained in [49].

[38] A similar explanation has been proposed by Fladda *et al.* [57].

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VI. Summary

The state of our knowledge regarding damage production in ion-implanted silicon is approximately as follows.

1) Both theory and experiment suggest that individual heavy ions implanted at room temperature into a nonchanneling direction in silicon produce heavily disordered damage clusters that contain both simple defects and regions with properties that approach those of amorphous material.

2) Both theory and experiment suggest that individual light ions implanted at room temperature into a nonchanneling direction in silicon produce damage clusters that contain primarily simple defects, some of which are unstable at room temperature. As a result there may be considerable room-temperature annealing, and cluster overlap is required for the formation of amorphous regions.

3) A spatial distribution of damage arises from the fact that there is a spatial distribution of ion stopping points. The characteristics of the damage distribution can be estimated with fair accuracy for any ion–substrate combination from the theory of Sigmund and Sanders, and with better accuracy for light ions from the theory of Brice. The primary energy-deposition profile provides a first approximation to the damage distribution and can be simply estimated directly from range tables.

4) Crystalline silicon can be driven amorphous by a sufficiently large ion dose. The critical dose depends on the ion, the substrate temperature, and the dose rate, the latter parameters being particularly important for a light ion. A convenient criterion for the production of amorphous material in situations where essentially all of the damage is stable is that the nuclear energy deposited per unit volume should be $\sim 10^{23}$ keV/cm^3.

With regard to annealing:

1) Isolated damage clusters anneal into dislocation loops and dipoles at temperatures between 200 and 600°C in time periods on the order to 30 min. Dislocation networks are still present after high-temperature (~1000°C) annealing, unless the annealing is carried out in a high vacuum and the sample surface is very clean.

2) Crystalline silicon that is driven amorphous by ion implantation can be regrown epitaxially on the underlying crystalline substrate at temperatures of about 600°C in a time period on the order of 30 min.

With regard to the electrical properties of ion-implanted silicon:

1) Under typical implantation conditions, defects override any possible chemical effects of the implanted ions until an annealing temperature of about 300–350°C is reached. Type conversion is first observed at annealing temperatures in this range.

2) If the silicon is driven amorphous prior to annealing, a large proportion of the ions in the amorphous layer will be incorporated into substitutional sites following a 600°C 30-min anneal, even for peak concentrations in excess of 10^{22}/cm^3. However, a heavily damaged transition region will exist between the amorphous layer and the crystalline silicon in which majority carrier properties will be trap dominated until an annealing temperature of 800–900°C is reached. Minority carrier properties may continue to be trap dominated beyond this point.

3) If the silicon is not driven amorphous prior to annealing, a variety of effects may occur, including negative annealing in the 300–600°C temperature range if the damage and impurity profiles match properly, and a fractional electrical activity that is dose dependent. For low doses, or more exactly low-volume concentrations of the implanted species, 50–70-percent fractional electrical activity can be obtained following a 600°C 30-min anneal; 90-percent activity can be obtained by increasing the annealing temperature to ~800–900°C. For larger doses, the electrical activity following a 600°C 30-min anneal decreases and may reach values as low as 5 percent; but 90-percent activity can still be obtained if a sufficiently high annealing temperature is employed.

We refer the reader to the literature [63], [64] for discussions on the effects of channeling on damage production and annealing.

Appendix

In this appendix we wish to call attention to an approximation that was used in the solution of the LSS equations for projected-range statistics given in Part I [1], and to indicate how the error introduced by the approximation may be minimized in practical computations of projected-range statistics.

The approximation arises in the evaluation of integrals of the form

$$I = \int_0^{T_m} \left\{ \langle X^m(E) \rangle - \langle X^m(E - T) \rangle \right\} d\sigma(T) \quad \text{(A.1)}$$

where $\langle X^m(E) \rangle$ is the mth moment of a range quantity. The second term in the integrand, $\langle X^m(E-T) \rangle$, may also appear multiplied by the cosine of sine of a laboratory scattering angle θ, depending on the range quantity that is being computed.

To evaluate the integral, it is customary to assume that the energy transferred to target atoms in passing through any thin section of target is small, so that $\langle X^m(E-T) \rangle$ can be expanded in a Taylor series in T. The result is, to first order in the Taylor expansion,

$$\begin{aligned} I &= \int_0^{T_m} \left\{ \langle X^m(E) \rangle - \langle X^m(E) \rangle + T \frac{d\langle X^m(E) \rangle}{dE} \right\} d\sigma(T) \\ &= \frac{d\langle X^m(E) \rangle}{dE} \int_0^{T_m} T \, d\sigma(T) \\ &= \frac{d\langle X^m(E) \rangle}{dE} (S_n + S_e). \end{aligned} \quad \text{(A.2)}$$

Thus the Taylor expansion permits us to express the integral in terms of the *first derivative* of $\langle X^m \rangle$ with respect to E, together with factors such as S_n and S_e, which are also expressible in terms of E, the projectile's energy.

If the first-order Taylor approximation is used to simplify all integrals required in the computation of range statistics, one obtains a series of *first-order* differential equations for $\langle R_p \rangle$, $\langle R_p^2 \rangle$, and $\langle R_p^3 \rangle$, these being the quantities required to compute the mean and standard deviation of the projected range. The solutions to these first-order equations are given in (28)–(30) in Part I, and are numerically evaluated by Johnson and Gibbons [5] for a variety of ion-substrate combinations.

The resulting range statistics have proved to be quite accurate as long as the ratio of the mass of a target atom to that of the projectile is large (i.e., $\mu = M_2/M_1 \gg 1$). However, when $\mu \ll 1$, as in the case of a heavy ion implant, it is found

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that the standard deviation in projected range as computed from the first-order differential equations is too small. (All other range quantities computed by the first-order differential equations remain reasonably accurate.) When this is the case, the Taylor expansion employed in the evaluation of (A.1) must be carried to second order in T, and *second-order* differential equations for all range quantities will result.

The effect of this correction has been studied by Brice [59] and Furukawa [60], who find that the second-order differential equations give a standard deviation in projected range that is significantly larger than that computed from the first-order equations when $\mu < 1$. The problem has also been studied by the present author [33], who finds that, for $\mu \ll 1$,

$$\sigma_p \simeq \left(1 - \frac{\mu}{2+\mu}\right)^{1/2} \sigma_R \qquad \text{(A.3)}$$

while for an arbitrary value of μ,

$$\frac{\sigma_p}{R_p} \cong \left[\frac{\mu+\gamma}{9}\,\frac{S_n(E_0)}{E_0}\,R\right]^{1/2}. \qquad \text{(A.4)}$$

The symbols in (A.3) and (A.4) are defined by

σ_p standard deviation in projected range (called ΔR_p by LSS),
σ_R standard deviation in total range (called ΔR by LSS),
$\mu = M_2/M_1$ mass of target atom/ion mass,
$\gamma = 4\dfrac{M_1 M_2}{(M_1+M_2)^2}$,
$S_n(E_0)$ nuclear stopping power at *initial* energy E_0,
E_0 initial energy,
R total range,
R_p projected range.

Values computed from (A.4) agree quite well with numerical values obtained by Brice [59] and Furukawa [60] for a wide variety of ions in silicon. It also turns out that, as suggested by (A.3), $\sigma_p \simeq \sigma_R$ when μ is small. That is, for $\mu < 1$, the standard deviation in projected range as computed from the second-order differential equations is very nearly equal to the standard deviation in total range (computed by either first- or second-order differential equations). Hence as a convenient rule of thumb, the standard deviation in projected range should be taken as the *larger* of the two numbers listed by Johnson and Gibbons, that is,

$$\sigma_p^{II} \simeq \sigma_p^{I} \quad \text{if} \quad \sigma_p^{I} > \sigma_R^{I}$$
$$\sigma_p^{II} \simeq \sigma_R^{I} \quad \text{if} \quad \sigma_R^{I} > \sigma_p^{I} \qquad \text{(A.5)}$$

where the superscripts refer to solutions obtained from the first- and second-order differential equations, respectively. The quantities bearing a I superscript are the quantities computed by Johnson and Gibbons [3]. The approximation given in (A.5) will give results that are within about 20–30 percent of experimental values [48].

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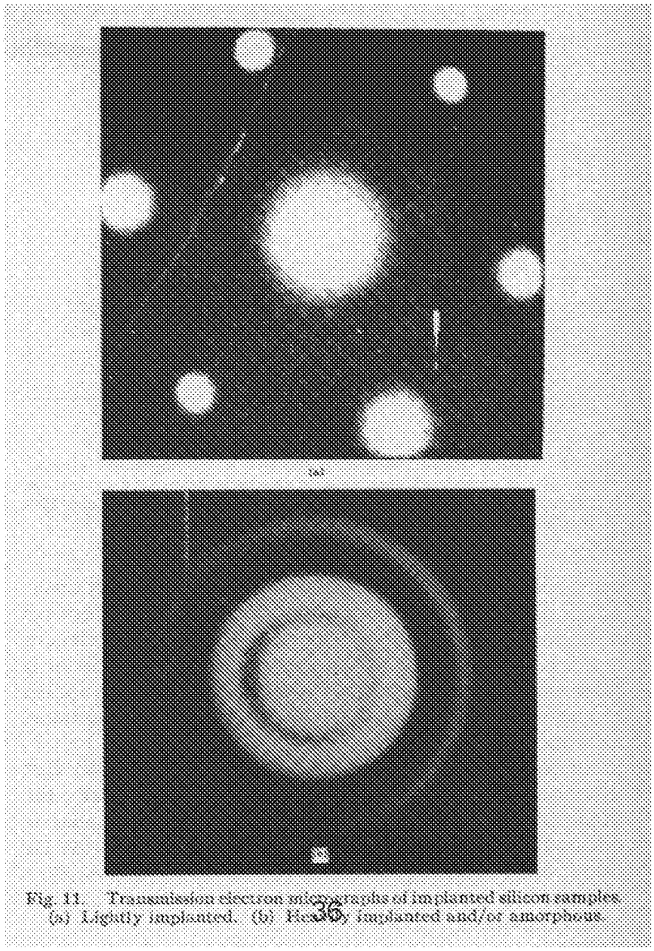


Fig. 11. Transmission electron micrographs of implanted silicon samples. (a) Lightly implanted. (b) Heavily implanted and/or amorphous.

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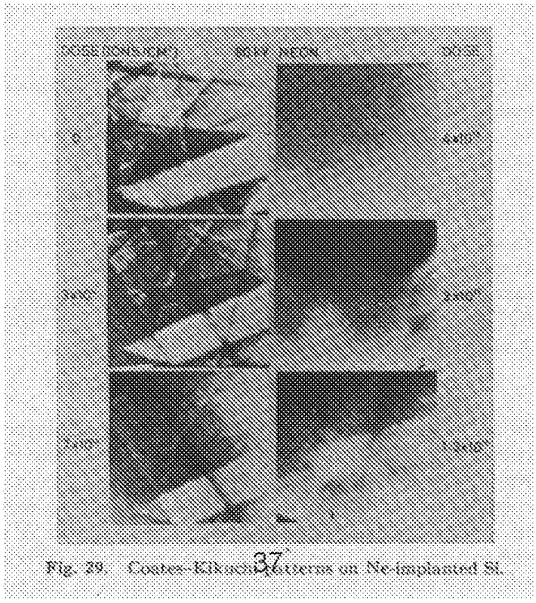


Fig. 29. Coates–Kikuchi patterns on Ne-implanted Si.

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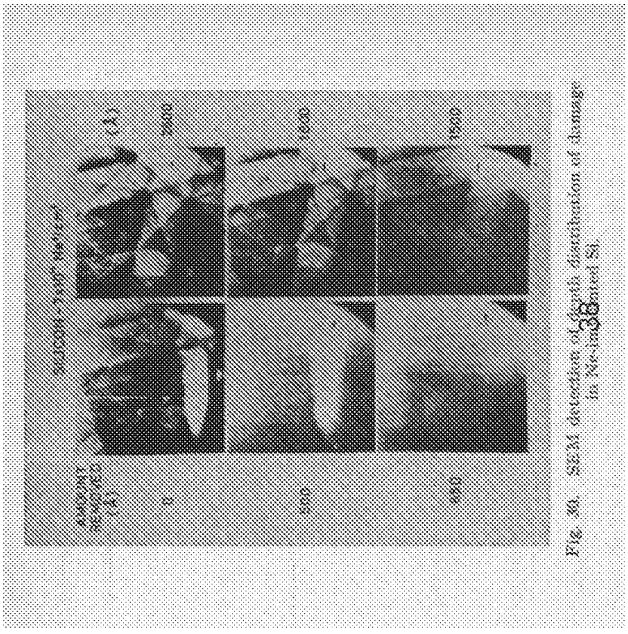


Fig. 30. SEM direction of depth distribution of damage in Nd:YAG and Si.

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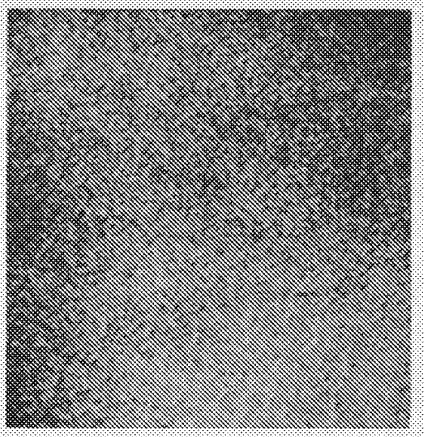


Fig. 34. Bright field image taken from central spot of the Debye-Scherrer pattern.

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Fig. 38. Small regions of dark contrast appearing in Ne-implanted sample after a dose of ~10^{16} ions/cm^2.

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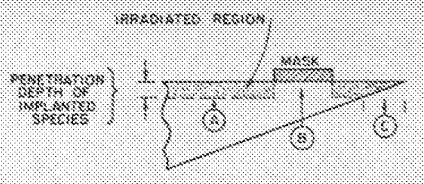


Fig. 39. Specimen geometry for electron microscope investigations of image.

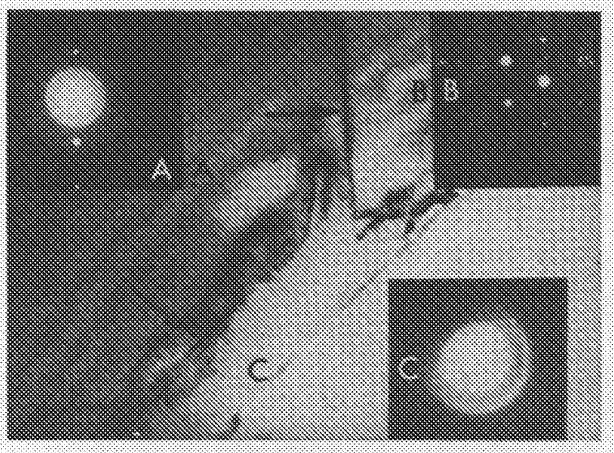


Fig. 40. Electron micrographs obtained from regions defined in Fig. 39 following implantation of 10^{15} ^{84}Kr ions/cm² at 80 keV into a room-temperature Si target.

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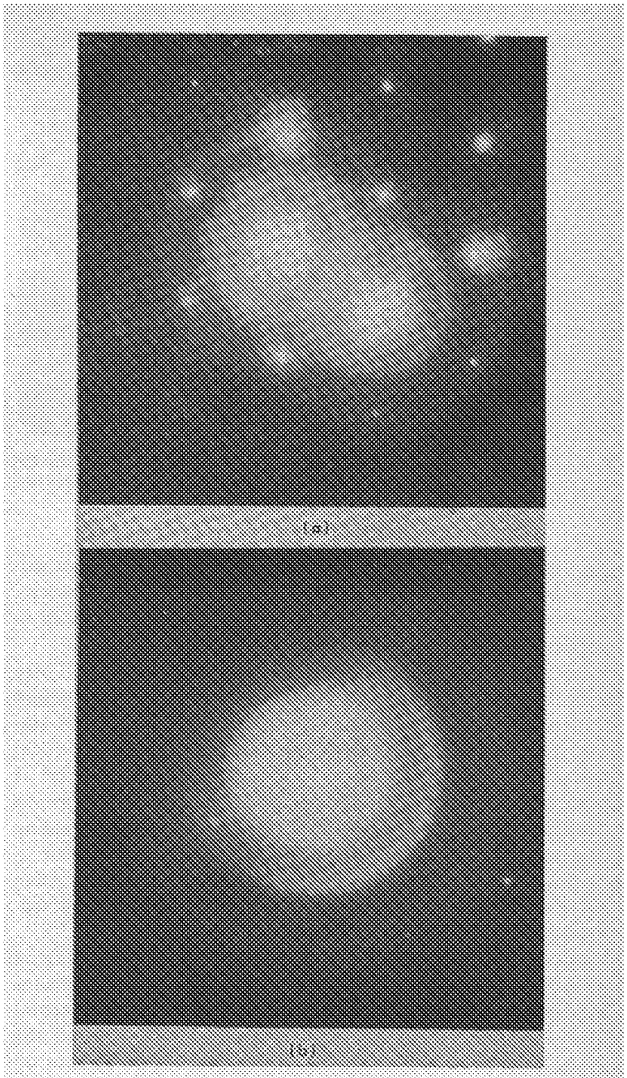


Fig. 41. (a) Region A in Fig. 39 illuminated from unbombarded side of specimen. (b) Region A illuminated normally.

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Fig. 42. Bright-field macrograph showing dislocation loops and dipoles following implantation of 2×10^{15} B ions/cm^2 into (111) Si at room temperature. Sample annealed at 4 h at 800°C.

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Fig. 4.3. Rod-like defects observed following B implantation and annealing. For details see Christensen and Elsen [44].

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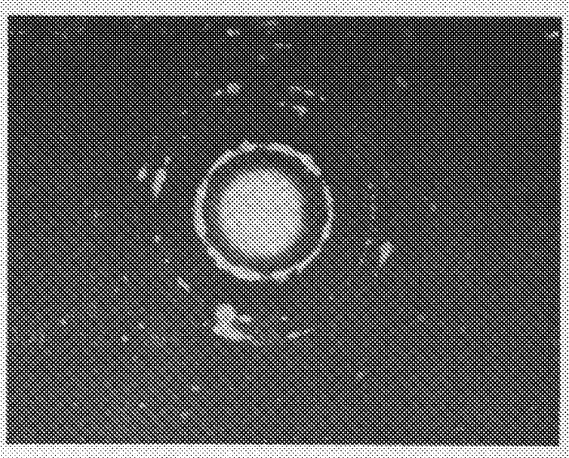


Fig. 44. Transmitted image of heavily bombarded Si annealed for 4 h at 900°C. Thin broken rings denote twinning in regrowth of amorphous layer.



Fig. 45. Dark field micrograph taken from major ring of Fig. 44.

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Depth from Defocus Using the Hermite Transform

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Abstract

This paper presents an algorithm for a dense computation of the difference in blur between two images. The two images are acquired by varying the intrinsic parameters of the camera. The image formation system is assumed to be passive. The algorithm is based on a local image decomposition technique using the Hermite polynomial basis. We show that any coefficient of the Hermite polynomial computed using the unfocused image is a function of the partial derivatives of the focused image and the blur difference. Hence, the blur difference can be computed by resolving a system of equations. An algorithm is presented for estimation of the blur in 1D and 2D images. The algorithm is tested using synthetic and real images. The results obtained are very encouraging.

1 Introduction

In this paper, we will present an algorithm for computing the difference in blur between two images. These two images are acquired by varying the intrinsic parameters of the camera. The image formation system is assumed to be passive. Specifically, let us consider a camera which generates grey-level images of a static 3D scene. Let us assume the perspective projection of a real world point onto the image. In the case of the thin lens, the image is formed by convolution of the ideal projected image and the camera point spread function (PSF) $g(x, y, \sigma(x, y))$, where $\sigma(x, y)$ is the blur parameter at the pixel (x, y). Usually, $\sigma(x, y)$ is assumed to be constant within a given window. Many functions are used to approximate the PSF of the camera. We are interested in the most common case, where PSF is approximated by:

$$g_\sigma(x, y) = \frac{1}{\pi\sigma^2} e^{-\frac{x^2+y^2}{\sigma^2}} \quad (1)$$

The image intensity at a given pixel (x, y) depends on the distance z between the camera lens and the corresponding point in the scene (Fig. 1). The relationship between the distance z and the blur σ is given by [5]:

$$z = \begin{cases} \frac{Fv}{v-F-kf\sigma} & \text{if } z > u \\ \frac{Fv}{v-F+kf\sigma} & \text{if } z < u \end{cases} \quad (2)$$

where u is the distance between the lens and the position of perfect focus, v the distance between the lens and the image plane, F the focal length, f the f-number, and k the proportionality coefficient between the blur circle radius and σ. This formula shows that estimation of depth z requires the estimation of f, F, v, k, and σ, which are independent of pixel location (x, y). They can be estimated by calibration [6]. The blur σ at a pixel (x, y) is measured by calculating the PSF function at this pixel.

The work of Pentland [4] was the first research in computer vision to test the use of defocus information as a depth cue. Since Pentland's work, many other schemes for the computation of blur have been proposed: inverse filtering [4, 5, 1, 9], depth recovery from edges [5, 2], and the S-Transform [8].

Our algorithm involves fitting the images by a Hermite polynomial basis. We will show that any coefficient of the Hermite polynomial computed using the unfocused image is a function of the partial derivatives of the focused image and the blur difference. Hence, the blur difference can be computed by resolving a system of equations. All computations required are local and are carried out in the spatial domain. Furthermore, no image model has been used to derive the algorithm. Consequently, our algorithm yields a dense estimation of blur. In the next section, we will start by describing the blur estimation rule for 1D images. Then we will present the extension of the 1D mathematical model to 2D images. The algorithm for blur estimation in 2D images is described in section 4. Section 5 presents the experimental results.

2 Blur Estimation in a 1D Signal

In this section we present the mathematical development behind blur estimation in the case of a 1D signal. Let us consider a focused image $I_c(x)$ and an

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unfocused image $I_b(x)$ of the same scene. The relationship between these images is:

$$I_b(x) = (I_c * g_\beta)(x) \tag{3}$$

where $g_\beta(x)$ is a Gaussian of variance β^2 and $*$ represents convolution. The parameter β is the blur difference between the two images. The relationship between β and z can be deduced. For example, let us consider the image $I_b(x)$ obtained by changing the parameter v by an amount δv in (Eq. 2). The depth z is given by:

$$\frac{1}{z} = \begin{cases} \frac{1}{F} - \frac{1}{2v+\delta v}\left(1 + \sqrt{1 + \frac{f^2(2v+\delta v)}{F^2 \delta v} k^2 \beta^2}\right) & \text{if } z > F \\ \frac{1}{F} - \frac{1}{2v+\delta v}\left(1 - \sqrt{1 + \frac{f^2(2v+\delta v)}{F^2 \delta v} k^2 \beta^2}\right) & \text{if } z < F \end{cases} \tag{4}$$

This equation shows that the depth can be computed from the intrinsic camera parameters and the blur difference β. It should be recalled that the camera parameters can be obtained by calibration. Now, we are faced with the problem of estimating β. To this end, we have developed an image decomposition technique, called the Hermite polynomial transform, in which the image is locally approximated by Hermite polynomials. The scheme involves fitting the image, within the Gaussian window $g_\sigma(x)$ in (Eq. 1), by a Hermite polynomial basis. The n^{th} Hermite polynomial $P_n(x)$ is defined by:

$$P_n(x) = (-1)^n e^{\frac{x^2}{\sigma^2}} \frac{d^n}{d(\frac{x}{\sigma})^n} e^{-\frac{x^2}{\sigma^2}} \tag{5}$$

The sequence $\{P_n(x)\}$ is orthonormal with respect to $g_\sigma(x)$ on $(-\infty, +\infty)$. Our choice of the Hermite polynomial is due to the fact that these polynomials are associated with the Gaussian function. Hence, they have interesting properties and their use in image processing is increasing [3]. In this mathematical model, the complete description of an image requires that the fitting process be repeated at a sufficient number of pixels within the window. We will consider the case of equidistant sample spacing T. The approximation of image $I_b(x)$ within this window by the polynomial basis $\{P_n(x)\}$ is:

$$I_b(x) = \frac{\sum_{n=0}^{\infty} \sum_{k=-K}^{K} c_n(kT) P_n(x - kT) \sqrt{g_\sigma(x - kT)}}{\sum_{k=-K}^{K} \sqrt{g_\sigma(x - kT)}} \tag{6}$$

where $2K + 1$ is the maximum number of samples in the window and $c_n(kT)$ is defined by:

$$c_n(kT) = (I_b * h_n)(kT) \tag{7}$$

where

$$h_n(x) = P_n(x) g_\sigma(x) = (-1)^n \frac{d^n}{d(\frac{x}{\sigma})^n} \frac{1}{\sqrt{\pi}\sigma} e^{-\frac{x^2}{\sigma^2}} \tag{8}$$

Substituting (Eq. 3) in (Eq. 7), we obtain:

$$c_n(kT) = (I_c * f_n)(kT) \tag{9}$$

where

$$f_n(x) = (g_\beta * h_n)(x) = (-1)^n \sigma^n \frac{d^n}{dx^n} \frac{1}{\sqrt{\pi}\alpha} e^{-\frac{x^2}{\alpha^2}} \tag{10}$$

and $\alpha^2 = \sigma^2 + \beta^2$. (Eqs. 7 and 9) show the relationship between image I_b and image I_c. We can use these two equations to estimate the blur. However, we are faced with solving a non-linear equation. Now we want to give a simple form of the relationship between these two images which will make the computation rule of β explicit. Let us consider the Taylor expansion of $I_c(kT - x)$ at kT:

$$I_c(kT - x) = \sum_{p=0}^{+\infty} \frac{(-x)^p I_c^{(p)}(kT)}{p!} \tag{11}$$

where $I_c^{(p)}(x)$ denotes the p^{th} derivative of $I_c(x)$. Substituting this equation in (Eq. 9), we obtain:

$$c_n(kT) = \sum_{p=0}^{+\infty} s_{n,p} I_c^{(p)}(kT) \tag{12}$$

where

$$s_{n,p} = \int_{-\infty}^{\infty} \frac{(-x)^p f_n(x)}{p!} dx \tag{13}$$

(Eqs. 7 and 12) show the relationship between image I_b and image I_c. In this relation, a coefficient $s_{n,p}$ is function of the p^{th} moment of $f_n(x)$. In other words, given $I_c(x)$, $I_b(x)$ and $f_n(x)$ we are able to estimate β. However, in moment-based schemes, calculating the moment directly entails a high computation cost. To overcome this difficulty, we propose an efficient computation procedure for $s_{n,p}$:

$$s_{n,p} = \begin{cases} (-1)^n \sigma^n \frac{(p-n-1)(p-n-3)\cdots 3\alpha^{p-n}}{(p-n)!2^{(p-n)/2}} \\ \quad \text{if } 0 < n < p \text{ and } p - n \text{ is even} \\ (-1)^n \sigma^n \quad \text{if } n = p \\ 0 \quad \text{otherwise} \end{cases} \tag{14}$$

By using (Eqs. 7, 12, and 14), the relation between the two images $I_b(x)$ and $I_c(x)$ is now given by:

$$\begin{cases} c_{2r}(kT) = \sum_{p \geq r}^{+\infty} s_{2r,2p} I_c^{(2p)}(kT) = (I_b * h_{2r})(kT) \\ c_{2r+1}(kT) = \sum_{p \geq r}^{+\infty} s_{2r+1,2p+1} I_c^{(2p+1)}(kT) = \\ (I_b * h_{2r+1})(kT) \end{cases} \tag{15}$$

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SAMSUNG EX. 1002 - 4103/4148

We are now able to compute the blur difference. For the sake of clarity, let us examine the use of coefficients c_0 and c_1 in (Eqs. 15) as an example. In the case of c_0, we assume that $\sum_{p>1} s_{0,2p} I_c^{(2p)}(kT) = 0$ and for c_1, we assume that $\sum_{p>1}^{+\infty} s_{1,2p+1} I_c^{(2p+1)}(kT) = 0$. According to (Eq. 14), $s_{0,0} = 1$, $s_{1,1} = -\sigma$, $s_{0,2} = \frac{\alpha^2}{4}$, and $s_{1,3} = -\sigma\frac{\alpha^2}{4}$. Thus (Eq. 15) becomes:

$$\begin{cases} c_0(kT) = I_c(kT) + \frac{\alpha^2}{4} I_c''(kT) = (I_b * h_0)(kT) \\ c_1(kT) = -\sigma I_c'(kT) - \sigma\frac{\alpha^2}{4} I_c'''(kT) = (I_b * h_1)(kT) \end{cases} \tag{16}$$

By resolving these two equations we obtain respectively:

$$\beta = \sqrt{4\frac{(I_b * h_0)(kT) - I_c(kT)}{I_c''(kT)} - \sigma^2} \tag{17}$$

or

$$\beta = \sqrt{4\frac{(I_b * h_1)(kT) + \sigma I_c'(kT)}{-\sigma I_c'''(kT)} - \sigma^2} \tag{18}$$

3 Extension to a 2D Image

The extension of the 1D scheme for blur estimation to the 2D case is straightforward. In fact, a 2D Hermite polynomial can be created by taking the tensor product of two sets of 1D Hermite polynomials; i.e, $\{P_0(x)P_0(y), \cdots, P_n(x)P_m(y), \cdots\}$, where n is the degree of x and m the degree of y. Since a Gaussian window $g_\sigma(x,y)$ is also separable, it is easy to show that $\{P_{n,m}(x,y)\}$ is orthogonal within $g_\sigma(x,y)$. Let us consider that kT_x and lT_y are the sample spacings in the window along the x and y axes. The decomposition of image $I_b(x,y)$ into localized polynomials is given by:

$$\begin{array}{l} I_b(x,y) = \sum_{n=0}^{+\infty}\sum_{m=0}^{+\infty}\sum_{k=-K}^{K}\sum_{l=-L}^{L} c_{n,m}(kT_x, lT_y) \\ P_{n,m}(x-kT_x, y-lT_y)\frac{\sqrt{g_\sigma(x-kT_x, y-lT_y)}}{w(x,y)} \end{array} \tag{19}$$

where
$w(x,y) = \sum_{k=-K}^{K}\sum_{l=-L}^{L}\sqrt{g_\sigma(x-kT_x, y-lT_y)}$,
$(2K+1)\times(2L+1)$ is the size of the sampling lattice and $c_{n,m}(kT_x, lT_y)$ is defined by:

$$c_{n,m}(kT_x, lT_y) = (I_b * h_{n,m})(kT_x, lT_y) \tag{20}$$

where $h_{n,m}(x,y) = P_{n,m}(x,y)g_\sigma(x,y)$. Both $P_{n,m}(x,y)$ and $g_\sigma(x,y)$ are separable; thus straightforward manipulations, as in the 1D case, give:

$$c_{n,m}(kT_x, lT_y) = \sum_{p=0}^{+\infty}\sum_{q=0}^{+\infty} s_{n,p,m,q} I_c^{(p)(q)}(kT_x, lT_y) \tag{21}$$

where $s_{n,p,m,q}$ is defined by:

$$s_{n,p,m,q} = \int_{-\infty}^{+\infty}\int_{-\infty}^{\infty}\frac{(-x)^p(-y)^q f_{n,m}(x,y)}{p!q!}dxdy \tag{22}$$

$f_{n,m}(x,y)$ is separable, thus $s_{n,p,m,q} = s_{n,p}s_{m,q} = \int_{-\infty}^{\infty}\frac{(-x)^p f_n(x)}{p!}dx\int_{-\infty}^{\infty}\frac{(-y)^q f_m(y)}{q!}dy$. Rapid calculation of $s_{n,p,m,q}$ is possible by using (Eq. 14). The coefficient $c_{n,m}(kT_x, lT_y)$ in (Eq. 21) becomes:

$$\begin{cases} c_{2r,2t}(kT_x, lT_y) = \sum_{p\geq r}^{+\infty}\sum_{q\geq t}^{+\infty} s_{2r,2p}s_{2t,2q} \\ \quad I_c^{(2p)(2q)}(kT_x, lT_y) \\ c_{2r,2t+1}(kT_x, lT_y) = \sum_{p\geq r}^{+\infty}\sum_{q\geq t}^{+\infty} s_{2r,2p}s_{2t+1,2q+1} \\ \quad I_c^{(2p)(2q+1)}(kT_x, lT_y) \\ c_{2r+1,2t}(kT_x, lT_y) = \sum_{p\geq r}^{+\infty}\sum_{q\geq t}^{+\infty} s_{2r+1,2p+1}s_{2t,2q} \\ \quad I_c^{(2p+1)(2q)}(kT_x, lT_y) \\ c_{2r+1,2t+1}(kT_x, lT_y) = \sum_{p\geq r}^{+\infty}\sum_{q\geq t}^{+\infty} s_{2r+1,2p+1} \\ \quad s_{2t+1,2q+1} I_c^{(2p+1)(2q+1)}(kT_x, lT_y) \end{cases} \tag{23}$$

We are now able to compute the blur difference between two 2D images. For clarity, let us take as an example the coefficients $c_{0,0}$, $c_{0,1}$, and $c_{1,0}$ in (Eqs. 23). Let us assume that the image is a cubic polynomial; that is $I_c^{(p)(q)}(kT_x, lT_y) = 0$, $\forall p+q > 3$. By using (Eqs. 14 and 20), we can rewrite the first three equations in (23):

$$\begin{cases} c_{0,0}(kT_x, lT_y) = I_c(kT_x, lT_y) + \frac{\alpha^2}{4}\nabla I_c(kT_x, lT_y) = \\ \quad (I_b * h_{0,0})(kT_x, lT_y) \\ c_{0,1}(kT_x, lT_y) = -\sigma I_c^{(0)(1)}(kT_x, lT_y) - \\ \quad \sigma\frac{\alpha^2}{4} I_c^{(2)(1)}(kT_x, lT_y) = (I_b * h_{0,1})(kT_x, lT_y) \\ c_{1,0}(kT_x, lT_y) = -\sigma I_c^{(1)(0)}(kT_x, lT_y) - \\ \quad \sigma\frac{\alpha^2}{4} I_c^{(1)(2)}(kT_x, lT_y) = (I_b * h_{1,0})(kT_x, lT_y) \end{cases} \tag{24}$$

where ∇ is the Laplacian. The first equation in (24) is the same as the one implemented by M. Subbarao and G. Surya [8]. These authors propose a spatial approach, called the S-Transform. They assume that the image is fitted by the cubic polynomial $p(x,y) = \sum_{m=0}^{3}\sum_{n=0}^{3-m} a_{n,m}x^m y^n$. In this case, they show that $I_c(x,y) = I_b(x,y) - \beta^2\nabla I_b(x,y)/4$, where ∇ is the Laplacian and β the blur difference. Thus, their model for blur estimation is a particular case of our blur estimation model.

4 Algorithm for Blur Estimation

We have presented the mathematical developments required for the computation of blur. Our next step is to specify an algorithm for the estimation of the blur difference β, based on these mathematical developments. Let us consider a finite summation in (Eq. 23)

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SAMSUNG EX. 1002 - 4104/4148

for a given n and m; that is $p \in [r, P]$ and $q \in [t, Q]$. The blur β is estimated by using (Eq. 20) and each equation in (23). In each window W centered at (x, y), we obtain four values of β, from which we choose the one which minimizes the following error:

$$e^2(x,y) = \sum_r \sum_s (I_b(x+r, y+s) - (I_c * g_\beta)(x+r, y+s))^2 \tag{25}$$

To summarize, given σ, T_x, T_y, N, M, P, and Q, the algorithm involves three steps: 1) the estimation of $c_{n,m}$ using (Eq. 20); 2) the estimation of four values of β using (Eq. 23); 3) the selection of the best β according to the quadratic error in (Eq. 25). The image derivatives $I_c^{(p)(q)}(x, y)$ can be estimated using differentiation techniques such as Sobel masks, Gaussian masks, polynomial fitting.

5 Experimental Results

We have tested the equations in (24) with two real images (Fig. 2.a and 2.b) of a toy house taken using an optical camera with different aperture and exposure time settings. The images have 384×320 pixels and 256 grey levels. They were given to us by Y. Xiong of the Robotics Institute at Carnegie Mellon University. The toy house is about two meters away from the camera. It is about 2.5 inches wide, 3 inches long, and 4.5 inches high. The partial derivatives of the image are computed by convolving the image with the appropriate derivatives of the Gaussian function. The scale σ is 1, the spacings $T_x = T_y = 1$. Figures 2.c, 2.d, and 2.e present the blur estimated using $c_{0,0}$ $c_{0,1}$, and $c_{1,0}$ (Eq. 24) respectively. In Fig. 2.c, the black regions are areas where the blur cannot be computed. As we can see in Figs. 2.d and 2.e, the use of $c_{0,1}$ and $c_{1,0}$ is recommended in the case of vertical and horizontal features respectively. The integration model of the three blur images (Figs., 2.c, 2.d, and 2.e) is given in Fig. 2.f. There are few black regions in this image. This means that the estimation of blur is more dense. Figs. 2.g and 2.h present the blur of Figs. 2.c and 2.f as a function of x and y.

It is clear that combination of the blurs estimated using equations $c_{0,0}$, $c_{0,1}$, and $c_{1,0}$ leads to more dense and accurate estimation of the blur. The algorithm is fast and allows parallel implementation. We have only tested a particular case of our algorithm ($c_{0,0}$, $c_{0,1}$, and $c_{1,0}$). In further work, we will test other rules for blur computation.

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SAMSUNG EX. 1002 - 4105/4148

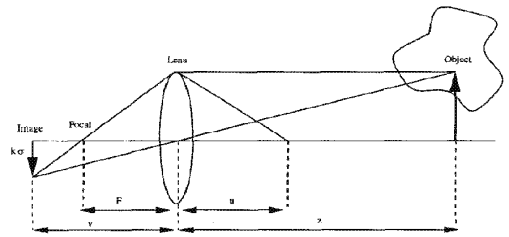


Figure 1: *Image formation in a thin lens.*

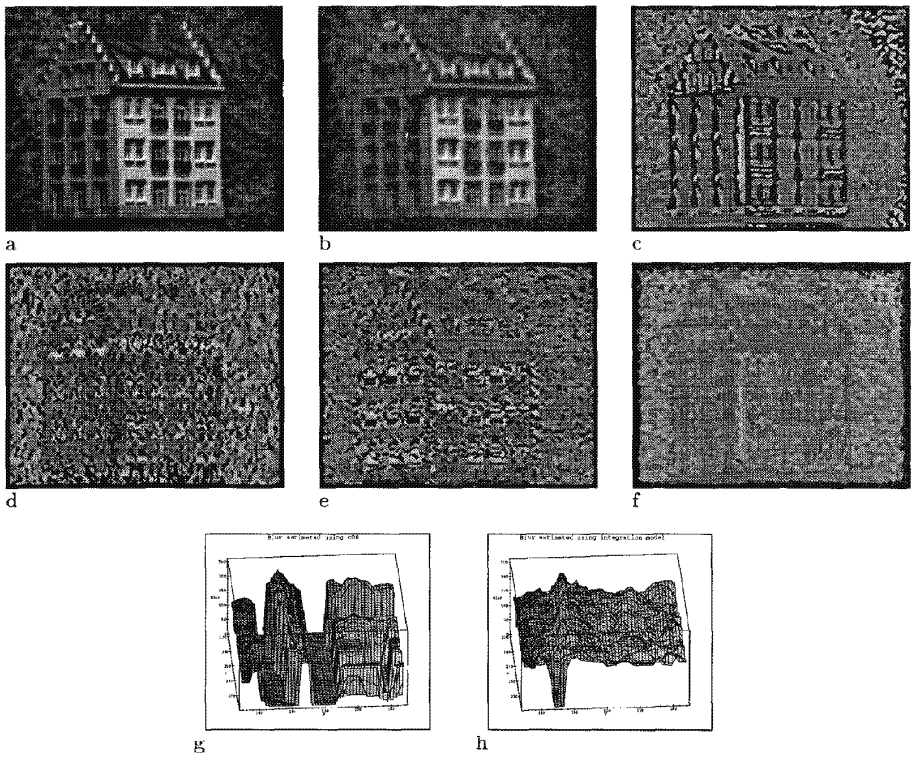


Figure 2: *An example for real images obtained by varying camera parameters. a) and b) Toy house. c), d), and e) describe the blur obtained by equations* $c_{0,0}$, $c_{0,1}$, *and* $c_{1,0}$ *(Eq. 24) respectively. f) Output of the integration model (Eq. 25). g) and h) The blur of c) and f) within a window, as a function of* x *and* y. *The window includes a part of vertical corner of the toy house.*

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SAMSUNG EX. 1002 - 4106/4148

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Production method for polycrystalline silicon solar cell texture surface

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Classification:	**- international:**	***H01L31/18***
	- cooperative:	Y02P70/521
Application number:	CN20081218734 20081029	
Priority number (s):	CN20081218734 20081029	

Abstract of CN101404307 (A)

The invention discloses a method for manufacturing a matte surface of a polysilicon solar cell. A laser beam is adopted to intensively scan the surface of a polysilicon wafer, thus causing silicon materials in the scanned region to generate fusion, gasification and spill reaction to form a micro-sized concave-convex structure on the surface of the polysilicon wafer, and the surface is etched and then is subject to surface cleaning by a chemical method to remove the damaged layer. The polysilicon wafer structure produced by the method can lead incident light to produce multiple reflection therein, increase the absorption of the incident light, achieve good surface anti-reflection effect and can cause little damage to the polysilicon wafer. The method solves the problem of manufacturing the matte surface of the polysilicon cell and can obtain the polysilicon wafer with surface reflectivity far less than the surface reflectivity of the silicon wafer manufactured by a pure chemical method. The method plays an important role of improving the light absorption and photoelectric conversion efficiency of the polysilicon solar cell.

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SAMSUNG EX. 1002 - 4107/4148

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权利要求书 1 页 说明书 4 页 附图 2 页

[54] 发明名称

一种多晶硅太阳电池绒面制作方法

[57] 摘要

本发明公开了一种多晶硅太阳电池绒面制作方法，该方法利用激光束在多晶硅片表面密集扫描，使扫描区域内的硅材料发生熔融、气化和溅出反应，在多晶硅片表面形成微米级的凹凸结构，刻蚀后采用化学方法做表面清洗和去除损伤层。采用本发明方法制成的多晶硅片结构可以使入射光在其中多次反射，增加对入射光的吸收，获得良好的表面减反射效果，并且对硅片的损伤影响较小。本发明解决了困扰多晶硅电池的制绒问题，可以获得远小于纯化学制绒的硅片表面反射率，对提高多晶硅太阳电池的光吸收以及光电转换效率有着重要作用。

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SAMSUNG EX. 1002 - 4108/4148

1、一种多晶硅太阳电池绒面制作方法，其特征在于，利用激光束在多晶硅片表面密集扫描，使扫描区域内的硅材料发生熔融、气化和溅出反应，在多晶硅片表面形成微米级的凹凸结构，刻蚀后采用化学方法做表面清洗和去除损伤层。

2. 根据权利要求 1 所述的多晶硅太阳电池绒面制作方法，其特征在于，采用功率 1~1000W、波长 1100~200nm 的脉冲或连续激光束，在经过聚焦后达到微米量级直径的光斑照射到硅片表面进行扫描。

3. 根据权利要求 1 或 2 所述的多晶硅太阳电池绒面制作方法，其特征在于，根据多晶硅片和激光束的性能，选择合适扫描刻蚀图样，在硅片表面密集刻蚀，形成均匀绒面。

4. 根据权利要求 1 或 2 所述的多晶硅太阳电池绒面制作方法，其特征在于，在多晶硅片表面所形成的微米级的凹凸结构的高宽比值达 0.1~2。

5. 根据权利要求 1 或 2 所述的多晶硅太阳电池绒面制作方法，其特征在于，刻蚀后采用碱液、酸液或两者配合，清洗硅片表面的残渣，并腐蚀刻蚀区域表面的损伤层。

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SAMSUNG EX. 1002 - 4109/4148

一种多晶硅太阳电池绒面制作方法

技术领域

本发明涉及一种多晶硅表面制绒的方法，具体地说是一种在多晶硅太阳电池表面制绒的方法。

技术背景

硅太阳电池利用 p-n 结的光生伏特效应实现光电转换，已经成为新能源发展主流之一。2007 年多晶硅太阳电池占世界太阳电池总产量的 45.2%，处在稳步上升阶段，困扰多晶硅电池的技术原因主要是晶界的存在和缺乏合适的表面制绒方法。表面减反射决定了太阳电池吸收入射光的比例，关系到电池最终光电转换效率，对于目前占主流的晶体硅太阳电池，未经表面处理的反射率一般超过 30%，经过碱液各向异性化学腐蚀形成表面微米级随机金字塔结构绒面后单晶硅电池表面反射率可以降到 10%，多晶硅电池由于表面晶粒的晶向差异，目前普遍采用的各向同性化学腐蚀只能将反射率降低到 20%左右。

由于绒面对电池效率具有直接、明显的作用，开发新的多晶硅表面制绒技术具有重要意义。这些技术首先要求能在多晶硅表面形成微米级且具有合适高宽比的凹凸结构，同时要求处理过程对硅片的电学性能没有明显的损害。最后应对生产要求，制绒技术还要做到在时间和成本上有较好控制，适合产业化。

发明内容

本发明的目的是提供一种多晶硅太阳电池绒面制作方法，采用该方法可以制作高性能多晶硅太阳电池绒面，并且具有产业化前景，使多晶硅电池在绒面的反射率达到甚至低于单晶硅的水平。

本发明的目的通过采取以下技术方案予以实现：

一种多晶硅太阳电池绒面制作方法，其特征在于，利用激光束在多晶硅片表面密集扫描，使扫描区域内的硅材料发生熔融、气化和溅出反应，在多晶硅片表面形成微米级的凹凸结构，刻蚀后采用化学方法做表面清洗和去除损伤层。

作为本发明的进一步完善，采用功率 1~1000W、波长 1100~200nm 的脉冲或连续激光束，在经过聚焦后达到微米量级直径的光斑照射到硅片表面进行扫描。

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作为本发明的进一步完善，根据多晶硅片和激光束的性能，选择合适扫描刻蚀图样，在硅片表面密集刻蚀，形成均匀绒面。

作为本发明的一种实施方式，在多晶硅片表面所形成的微米级的凹凸结构的高宽比值达 0.1~2。

作为本发明的一种实施方式，刻蚀后采用碱液、酸液或两者配合，清洗硅片表面的残渣，并腐蚀刻蚀区域表面的损伤层，以恢复正常的电学性能。

本发明制作绒面的主要手段是采用激光束刻蚀硅片表面，采用较大功率的脉冲或连续激光束，在经过聚焦（如激光束本身足够细则不用聚焦）后达到微米量级直径的光斑照射到硅片表面进行扫描，使照射区域的表面材料熔融，溅射甚至气化，从而形成沟槽坑洞等密集的凹凸结构，即绒面。最后用化学方法去除激光刻蚀区域表面形成的杂质层（氧化物、氮化物等）和损伤层。入射光照射到太阳电池表面会发生反射，只有一定比例的光能进入电池内部被吸收转化为电能，如果电池表面平整没有绒面结构，入射光只存在一次反射，如图 1 所示。而本发明方法制成的太阳电池表面可以具有高宽比达到 1 甚至更高的凹凸结构表面，光线入射到这样的结构，会在结构表面多次反射，如图 2 所示，每一次有一定比例的光进入到电池内部被吸收，从而提高了太阳电池吸收的光占入射光的比例，降低了电池表面光反射率，提高了太阳电池的光电转换效率。

本发明方法的具体处理步骤是：

（1）清洗硅片表面杂质，避免杂质在激光刻蚀过程扩散；

（2）选择合适的激光刻蚀图样，激光刻蚀的图样最简单的是平行线或交叉线阵列，也可设计点阵，或其他图样，图样的尺寸要配合激光束的刻蚀宽度和深度，阵列周期在几十到几百微米；

（3）选择合适的激光波长、光束模式、光斑大小、光束功率、脉冲频率和扫描速度等激光参数方案，做好设置；

（4）将硅片固定在工作台上，按预定的参数和图样利用激光束扫描做刻蚀；

（5）刻蚀后采用碱液、酸液或两者配合，清洗硅片表面的残渣，并腐蚀刻蚀区域表面的损伤层，之后便可进行太阳电池制作的其他工序。

与现有技术相比，本发明具有的有益效果是：

本发明利用激光刻蚀，可以在多晶硅表面形成高宽比大于 1 的微米结构，激

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SAMSUNG EX. 1002 - 4111/4148

光刻蚀区域的表面反射率可降低到 6%，经过化学处理后的表面反射率可以达到 10% ，在减反射效果上已经达到了单晶硅的水平。同时通过对样品少子寿命的检测，少子寿命的衰减可以控制到 30%，符合电池制作的要求。与各向异性化学腐蚀方法相比，本发明方法对晶向无要求，同样适用于单晶硅电池。

附图说明

图 1 为光线在没有绒面结构的电池表面发生反射的示意图；

图 2 为光线在制有绒面结构的电池表面发生反射的示意图；

图 2 为本发明实施例 1 制得样品的形貌图（扫描电镜拍摄图）；

图 3 为本发明实施例 2 制得样品的形貌图（扫描电镜拍摄图）。

具体实施方式

以下列举具体实施例对本发明进行说明。需要指出的是，实施例只用于对本发明作进一步说明，不代表本发明的保护范围，其他人根据本发明的提示做出的非本质的修改和调整，仍属于本发明的保护范围。

实施例 1

采用一台波长 1064nm 的 Nd：YAG 激光器；激光脉冲频率 1K~30KHz，振镜扫描，光速横模为低阶模式。设置激光脉冲频率为 1~7KHz，扫描速度为 20~100mm/s，激励电流为 18~25A。样品硅片为厚度 260 微米的多晶硅片，先对原始硅片做适当化学清洗去除表面附着杂质。刻蚀图样选用平行线阵列，线长 30mm，间距 1.6mm，激光刻蚀后用 20%NaOH 溶液清洗腐蚀 15 分钟，然后去离子水清洗，氮气烘干，即完成制绒过程，制得样品的形貌为密排槽形状，如图 3 所示。

实施例 2

采用一台波长 1064nm 的 Nd：YAG 激光器；激光脉冲频率 1K~30KHz，振镜扫描，光速横模为低阶模式。设置激光脉冲频率为 7~15KHz，扫描速度为 20~100mm/s，激励电流为 22~30A。样品硅片为厚度 260 微米的多晶硅片，先对原始硅片做适当化学清洗去除表面附着杂质。刻蚀图样选用平行线阵列，线长 30mm，间距 0.1~0.2mm，激光刻蚀后用 20%NaOH 溶液清洗腐蚀 2~6 分钟，再用 HF:HNO_3 混合溶液腐蚀 2~10 分钟，然后去离子水清洗，氮气烘干，即完成制绒过程，制得样品的形貌为密排类锥形凹坑形状，如图 4 所示，最佳表面反射率

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SAMSUNG EX. 1002 - 4112/4148

可达 10%。

实施例 3

采用一台波长 1064nm 的 Nd：YAG 激光器：激光脉冲频率 1K~30KHz，振镜扫描，光速横模为低阶模式。设置激光脉冲频率为 1~10KHz，扫描速度为 20~200mm/s，激励电流为 18~25A。样品硅片为厚度 330 微米的单晶硅片，先对原始硅片做适当化学清洗去除表面附着杂质。刻蚀图样选用平行线阵列，线长 30mm，间距 0.06~0.15mm，激光刻蚀后用 20%NaOH 溶液清洗 10~20 分钟，再用 HF:HNO_3 混合溶液腐蚀 2~10 分钟，然后去离子水清洗，氮气烘干，即完成制绒过程，制得样品的形貌为密排槽形状。

实施例 4

采用一台波长 532nm 的 Nd：YAG 激光器：激光脉冲频率 1K~50KHz，振镜扫描，光速横模为低阶模式。设置激光脉冲频率为 1~10KHz，扫描速度为 20~200mm/s，激励电流为 18~25A。样品硅片为厚度 260 微米的多晶硅片，先对原始硅片做适当化学清洗去除表面附着杂质。刻蚀图样选用垂直交叉平行线阵列，线长 30mm，间距 0.1~0.3mm，激光刻蚀后用 20%NaOH 溶液清洗 5~15 分钟，再用 HF:HNO_3 混合溶液腐蚀 2~15 分钟，然后去离子水清洗，氮气烘干，即完成制绒过程，制得样品的形貌为密排台状或类金字塔突起形状。

实施例 5

采用一台波长 532nm 的 Nd：YAG 激光器：激光脉冲频率 1K~50KHz，振镜扫描，光速横模为低阶模式。设置激光脉冲频率为 1~5KHz，扫描速度为 100~600mm/s，激励电流为 20~30A。样品硅片为厚度 260 微米的多晶硅片，先对原始硅片做适当化学清洗去除表面附着杂质。刻蚀图样选用平行线阵列，线长 30mm，间距 0.05~0.3mm，使用单个高能量激光脉冲打点，形成点状凹坑，激光刻蚀后用 HF:HNO_3 混合溶液腐蚀 2~15 分钟，然后去离子水清洗，氮气烘干，即完成制绒过程，制得样品的形貌为密排凹坑形状。

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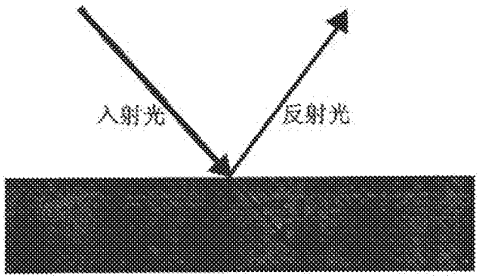


图 1

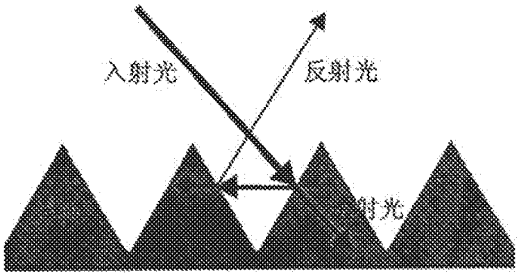


图 2

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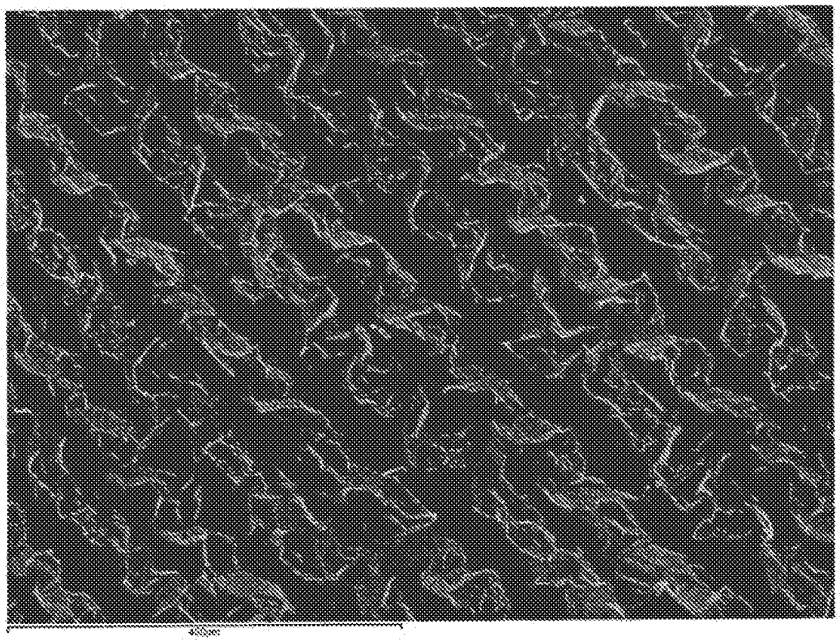


图 3

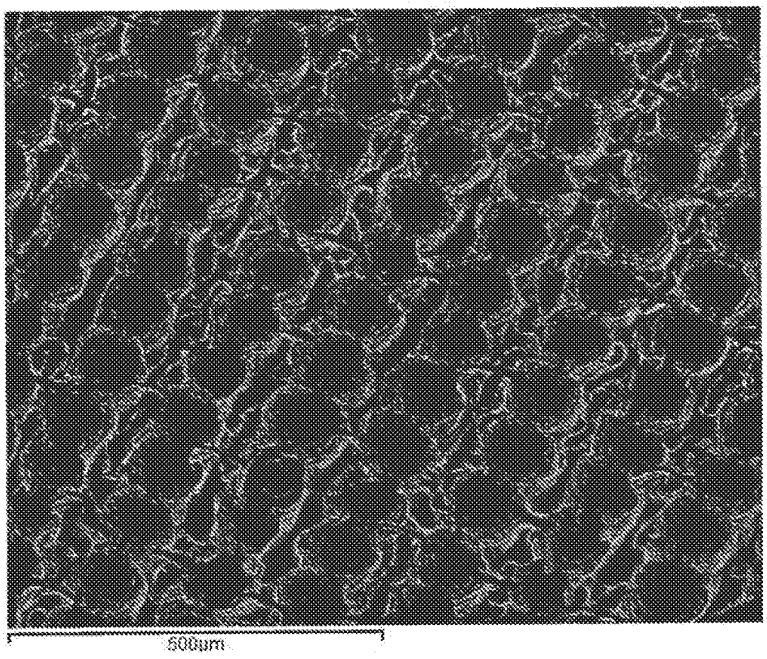


图 4

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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

136549 7590 10/31/2017

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER
PHAM, LONG

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/31/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/747,875	06/23/2015	Martin U. Pralle	143705.05211	1722

TITLE OF INVENTION: Pixel Isolation Elements, Devices and Associated Methods

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	01/31/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

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Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/747,875	06/23/2015	Martin U. Pralle	143705.05211	1722

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nonprovisional	SMALL	$480	$0	$0	$480	01/31/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG	2814	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
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4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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136549 7590 10/31/2017

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125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/31/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

SAMSUNG EX. 1002 - 4119/4148

Notice of Allowability	Application No. 14/747,875	Applicant(s) PRALLE ET AL.	
	Examiner LONG PHAM	Art Unit 2814	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE dated 7/26/17*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-2, 4-6, 10, 12-14,17, 19, 34-58*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 7/26/17
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/LONG PHAM/
Primary Examiner, Art Unit 2814

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	**Art Unit**
	LONG PHAM	2814

CPC						
Symbol					**Type**	**Version**
H01L		27	/	1463	F	2013-01-01
H01L		27	/	14627	I	2013-01-01
H01L		27	/	14629	I	2013-01-01
H01L		27	/	14685	I	2013-01-01
H01L		27	/	14625	I	2013-01-01
H01L		27	/	1462	I	2013-01-01
H01L		27	/	14607	I	2013-01-01
H01L		27	/	14645	I	2013-01-01
H01L		27	/	14689	I	2013-01-01
			/			
			/			
			/			
			/			
			/			
			/			

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	36	
/LONG PHAM/ Primary Examiner.Art Unit 2814	10/17/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3,6

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	**Art Unit**
	LONG PHAM	2814

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		H	0	1	L	27 / 146 (2006.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	36	
/LONG PHAM/ Primary Examiner.Art Unit 2814	10/17/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3,6

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	**Art Unit**
	LONG PHAM	2814

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	39	33	55										
2	2	18	40	34	56										
3	4	19	41	35	57										
4	5	20	42	36	58										
5	6	21	43												
6	10	22	44												
7	12	23	45												
8	13	24	46												
9	14	25	47												
10	17	26	48												
11	19	27	49												
12	34	28	50												
13	35	29	51												
14	36	30	52												
15	37	31	53												
16	38	32	54												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 36	
/LONG PHAM/ Primary Examiner.Art Unit 2814 (Primary Examiner)	10/17/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3,6

SAMSUNG EX. 1002 - 4123/4148

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application No.:	14747875
				Filing Date:	June 23, 2015
				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	2814
(use as many sheets as necessary)				Examiner Name:	Long Pham
Sheet	1	of	2	Attorney Docket No.:	143705.05211

U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document Number Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
	A1	4886958	Merryman	12/12/1989		
	A2	5351446	Langsdorf	10/4/1994		
	A3	5641969	Cooke et al.	6/24/1997		
	A4	5727096	Ghirardi et al	3/10/1998		
	A5	6327022	Nishi	12/4/2001		
	A6	6331885	Nishi	12/18/2001		
	A7	6340281	Haraguchi	1/22/2002		
	A8	7800684	Tatani	9/21/2010		
	A9	7897942	Bereket	3/1/2011		
	A10	8470619	Bour	6/1/2013		
	A11	8906670	Gray	12/1/2014		
	A12	9419159	Sakamoto et al.	8/16/2016		
	A13	9184204	Hu	11/10/2015		
	A14	9369641	Hu	6/14/2016		
	A15	20010044266	Katsuoka	11/22/2001		
	A16	20050040440	Murakami	2/24/2005		
	A17	20050088634	Kosugi	4/28/2005		
	A18	20090093100	Chen	5/6/2005		
	A19	20070103580	Noto	5/10/2007		
	A20	20080142686	Konno et al.	6/19/2008		
	A21	20080173620	Grek	7/24/2008		
	A22	20090027640	Shibazaki	1/29/2009		
	A23	20090114630	Hawryluk	5/7/2009		
	A24	20090101197	Morikawa	4/23/2009		
	A25	20100140768	Zafiropoulo	6/10/2010		
	A26	20110019050	Yamashita	1/27/2011		
	A27	20130135439	Kakuko et al.	5/30/2013		

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Cite No.	Foreign Patent Document Number Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear			T
	B1	CN101404307	Univ. Zhongshan	4/8/2009				

Examiner Signature	/LONG PHAM/	Date Considered	10/17/2017

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P/

SAMSUNG EX. 1002 - 4124/4148

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application No.:	14747875
				Filing Date:	June 23, 2015
				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	2814
(use as many sheets as necessary)				Examiner Name:	Long Pham
Sheet	2	of	2	Attorney Docket No.:	143705.05211

	B2	DE 19838439	Fraunhofer-Ges Forschung	4/27/2000				
	B3	EP 2509107	Boly Media Comm.	10/10/2012				
	B4	JP 2003258285	Sharp KK	9/12/2003				
	B5	JP H07235658	Sony Corp.	5/9/1995				
	B6	JP 2004047682	Toshiba Corp.	2/12/2004				
	B7	JP 2006210701	Sayno Electric Co.	8/10/2006				
	B8	JP 2006261372	Sony Corp.	9/28/2006				
	B9	JP 2006147991	Canon Inc.	6/8/2006				
	B10	JP 2006033493	Matsushita Electric Industrial Co. Ltd.	2/2/2006				
	B11	JP 2009152569	Semiconductor Energy Lab	7/9/2009				
	B12	KR 20090077274	LG Electronics Inc.	7/15/2009				
	B13	WO 2009147085	Thiel et al.	12/10/2009				
	B14	WO 2011003871	International Business Machines Corporation	1/13/2011				
	B15	WO 2011035188	Sionyx, Inc.	3/24/2011				
	B16	WO 2011119618	Sionyx, Inc.	3/22/2011				
	B17	WO 2012174752	Boly Media Comm.	12/27/2012				
	B18	WO 2014110484	Digimarc Corp.	7/17/2014				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
Examiner's Initials	**Cite No.**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or county where published**	**T**
	C1	**Carey, P.G. et al.**, "In-situ Doping of Silicon Using Gas Immersion Laser Doping (GILD) Process," Appl. Surf. Sci. 43, 325-332 (1989)	
	C2	**Gibbons, J.**, "Ion Implantation in Semiconductors-Part II; Damage Production and Annealing", proceedings of the IEEE Vol. 60, No. 9 pp. 1062-1096. Jun. 1972.	
	C3	**Ziou et al.**, "Depth from defocus using the hermite transform", IMAGE PROCESSING, 1998. ICIP 98. Intl. Conference on Chicago, IL. October 1998 pp. 958 - 962.	

Examiner Signature	/LONG PHAM/	Date Considered	10/17/2017

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P/

SAMSUNG EX. 1002 - 4125/4148

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	20	("20030214595" | "20030228883" | "20050093100" | "20060086956" | "20060128087" | "20070189583" | "20070237504" | "20080158398" | "20080192133" | "20080284884" | "20090308457" | "20100200658" | "20110292380" | "5101260" | "5600130" | "5626687" | "5635089" | "6082858" | "6204506" | "6907135").PN.	US-PGPUB; USPAT	OR	ON	2017/10/17 11:58

10/ 17/ 2017 11:59:08 AM
C:\ Users\ lpham\ Documents\ EAST\ Workspaces\ 14-747,875.wsp

SIONYX1403000040.0020

SAMSUNG EX. 1002 - 4126/4148

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	**Art Unit**
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/17/2016	07/15/2016	04/14/2017	10/17/2017					
	1	÷	✓	=	=					
	2	÷	✓	=	=					
	3	÷	-							
	4	÷	✓	=	=					
	5	÷	✓	=	=					
	6	÷	✓	=	=					
	7	÷	-							
	8	÷	-							
	9	÷	O	-						
	10	÷	O	=	=					
	11	÷	-							
	12	÷	✓	=	=					
	13	÷	✓	=	=					
	14	÷	✓	=	=					
	15	÷	-							
	16	÷	-							
	17	÷	✓	=	=					
	19	÷	✓	=	=					
	20	÷	-							
	34		O	=	=					
	35		O	=	=					
	36		O	=	=					
	37		✓	=	=					
	38		✓	=	=					
	39		✓	=	=					
	40		✓	=	=					
	41			=	=					
	42			=	=					
	43			=	=					
	44			=	=					
	45			=	=					
	46			=	=					
	47			=	=					
	48			=	=					
	49			=	=					
	50			=	=					

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	Art Unit
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/17/2016	07/15/2016	04/14/2017	10/17/2017					
	51			=	=					
	52			=	=					
	53			=	=					
	54			=	=					
	55			=	=					
	56			=	=					
	57			=	=					
	58			=	=					

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	Art Unit
	LONG PHAM	2814

CPC- SEARCHED		
Symbol	Date	Examiner
H01L27/1463,H01L27/14627,H01L27/14629,H01L27/14685,H01L27/14625,H01L27/1462,H01L27/14607,H01L27/14645,H01L27/14689	4/14/2017	LP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
UPDATED TEXT AND INTERFERENCE SEARCHES	10/17/2017	LP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
H01L	27/1463	4/14/2017	LP

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1722

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/747,875	06/23/2015 RULE	257	2814	143705.05211

APPLICANTS
SiOnyx, Inc., Beverly, MA;

INVENTORS
Martin U. Pralle, Wayland, MA;
Jeffrey McKee, Tualatin, OR;
Jason Sickler, Arlington, MA;

** **CONTINUING DATA** **********
This application is a CON of 13/841,120 03/15/2013 PAT 9064764
which claims benefit of 61/614,275 03/22/2012

** **FOREIGN APPLICATIONS** **********

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** ** SMALL ENTITY **
07/06/2015

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /LONG PHAM/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		MA	4	19	1

ADDRESS

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736
UNITED STATES

TITLE

Pixel Isolation Elements, Devices and Associated Methods

FILING FEE RECEIVED	FEES: Authority has been given in Paper	☐ All Fees
920	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

SAMSUNG EX. 1002 - 4130/4148

To: docketingbn@pepperlaw.com,davisdr@pepperlaw.com,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 136549

Oct 31, 2017 03:42:56 AM

Dear PAIR Customer:

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 136549 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
14747875	NOA	10/31/2017	143705.05211
	1449	10/31/2017	143705.05211

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

136549 7590 10/31/2017
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/747,875	06/23/2015	Martin U. Pralle	143705.05211	1722

TITLE OF INVENTION: Pixel Isolation Elements, Devices and Associated Methods

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	~~$480~~ $960	01/31/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG	2814	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Thomas J. Engellenner
2 Reza Mollaaghababa
3 Pepper Hamilton LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: SiOnyx, LLC
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Beverly, MA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 500436 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☒ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Andrew W. Schultz/ Date January 29, 2018
Typed or printed name Andrew W. Schultz Registration No. 66869

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

SAMSUNG EX. 1002 - 4132/4148

Electronic Patent Application Fee Transmittal

Application Number:	14747875
Filing Date:	23-Jun-2015
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Andrew W. Schultz/Irene Gommerstadt
Attorney Docket Number:	143705.05211

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

SAMSUNG EX. 1002 - 4133/4148

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**960**

Electronic Acknowledgement Receipt	
EFS ID:	31633513
Application Number:	14747875
International Application Number:	
Confirmation Number:	1722
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Andrew W. Schultz
Filer Authorized By:	
Attorney Docket Number:	143705.05211
Receipt Date:	29-JAN-2018
Filing Date:	23-JUN-2015
Time Stamp:	15:33:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$960
RAM confirmation Number	013018INTEFSW15344500
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

SAMSUNG EX. 1002 - 4135/4148

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	IssueFee.pdf	177972 453cc2518fb8e37d43e5ea3087ef5460b70b8db1	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30645 73e6fdc3eba17f6bdae0a32b3a7f200d4fdf7b03	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	208617		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SAMSUNG EX. 1002 - 4136/4148

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14747875
Filing Date	2015-06-23
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	14705.05211

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20030214595		2003-11-20	Mabuchi	
	2	20030228883		2003-12-11	Kusakari et al.	
Change(s) applied to document, /DD/ 6/1/2017	3	20050093100		2005-05-05	~~Tze-Chiang et al.~~ Chen et al.	
	4	20060086956		2006-04-27	Furukawa et al.	
	5	20060128087		2006-06-15	Bamji et al.	
	6	20070189583		2007-08-16	Shimada et al.	
	7	20070237504		2007-10-11	Nakashiba	
	8	20080158398		2008-07-03	~~Yoel et al.~~ Yaffe et al.	
	9	20080192133		2008-08-14	~~Takahiro et al.~~ Abiru et al.	
	10	20080284884		2008-11-20	~~Eiji et al.~~ Makino et al.	

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P/

SAMSUNG EX. 1002 - 4137/4148

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application No.:	14/747,875
				Filing Date:	June 23, 2015
				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	2814
(use as many sheets as necessary)				Examiner Name:	Long Pham
Sheet	7	of	20	Attorney Docket No.:	143705.05211

Change(s) applied to document, /D.D./ 6/1/2017

	A258	20010044175	Barret et al.	11/22/2001		
	A259	20020020893	Lhorte	2/21/2002		
	A260	20020024618	Imai	2/28/2002		
	A261	20020056845	Iguchi et al.	5/16/2002		
	A262	20020060322	Tanabe et al.	5/23/2002		
	A263	20020079290	Holdermann	6/27/2002		
	A264	20020117699	~~Roy~~ Francois	8/29/2002		
	A265	20020148964	Dausch et al.	10/17/2002		
	A266	20020182769	Campbell	12/5/2002		
	A267	20030029495	Mazur et al.	2/13/2003		
	A268	20030030083	Lee et al.	2/13/2003		
	A269	20030045092	Shin	3/6/2003		
	A270	20030057357	Uppal et al.	3/27/2003		
	A271	20030111106	Nagano et al.	6/19/2003		
	A272	20030210332	Frame	11/13/2003		
	A273	20030213515	Sano et al.	11/20/2003		
	A274	20040014307	Shin et al.	1/22/2004		
	A275	20040016886	Ringermacher et al.	1/29/2004		
	A276	20040041168	Hembree et al.	3/4/2004		
	A277	20040046224	Rossel et al.	3/11/2004		
	A278	20040077117	Ding et al.	4/22/2004		
	A279	20040080638	Lee	4/29/2004		
	A280	20040130020	Kuwabara et al.	7/22/2004		
	A281	20040161868	Hong	8/19/2004		
	A282	20040222187	Lin	11/11/2004		
	A283	20040252931	Belleville et al.	12/16/2004		
	A284	20050051822	Manning	3/10/2005		
	A285	20050062041	Terakawa et al.	3/24/2005		
	A286	20050101100	Kretchmer et al.	5/12/2005		
	A287	20050101160	Garg et al.	5/12/2005		
	A288	20050127401	Mazur et al.	6/16/2005		
	A289	20050134698	Schroeder et al.	6/23/2005		
	A290	20050150542	Madan	7/14/2005		
	A291	20050158969	Binnis et al.	7/21/2005		
	A292	20050211996	Krishna, et al.	9/29/2005		
	A293	20050227390	Shtein et al.	10/13/2005		
	A294	20060006482	Rieve, et al.	1/12/2006		
	A295	20060011954	Ueda et al.	1/19/2006		
	A296	20060011955	Baggenstoss	1/19/2006		
	A297	20060060848	Chang et al.	3/23/2006		
	A298	20060071254	Rhodes	4/6/2006		
	A299	20060079062	Mazur et al.	4/13/2006		
	A300	20060097172	Park	5/11/2006		
	A301	20060231914	Carey et al.	10/19/2006		

Examiner Signature	/LONG PHAM/	Date Considered	07/15/2016

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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SAMSUNG EX. 1002 - 4138/4148

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application No.:	14/747,875
				Filing Date:	June 23, 2015
				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	2814
(use as many sheets as necessary)				Examiner Name:	Long Pham
Sheet	6	of	20	Attorney Docket No.:	143705.05211

	A214	7741666	Nozaki, et al.	6/22/2010		
	A215	7745901	McCaffrey et al	6/29/2010		
	A216	7763913	Fan et al	7/27/2010		
	A217	7772028	Adkisson et al	8/10/2010		
	A218	7781856	Mazur et al.	8/24/2010		
	A219	7800192	Venezia, et al.	9/21/2010		
	A220	7816220	Mazur et al.	10/19/2010		
	A221	7828983	Weber et al	11/9/2010		
	A222	7847253	Carey et al.	12/7/2010		
	A223	7847326	Park, et al.	12/7/2010		
	A224	7855406	Yamaguchi et al	12/21/2010		
	A225	7875498	Elbanhawy, et al.	1/25/2011		
	A226	7880168	Lenchenkov	2/1/2011		
	A227	7884439	Mazur et al.	2/8/2011		
	A228	7884446	Mazur et al.	2/8/2011		
	A229	7910964	Kawahito et al.	3/22/2011		
	A230	7923801	Tian et al.	4/12/2011		
	A231	7968834	Veeder	6/28/2011		
	A232	8008205	Fukushima et al.	8/30/2011		
	A233	8013411	Cole	9/6/2011		
	A234	8030726	Sumi	10/4/2011		
	A235	8035343	Seman Jr.	10/11/2011		
	A236	8058615	McCaffrey	11/15/2011		
	A237	8080467	Carey et al.	12/20/2011		
	A238	8088219	Knerer et al.	1/3/2012		
	A239	8093559	Rajavel	1/10/2012		
	A240	8164126	Moon, et al.	4/24/2012		
	A241	8207051	Sickler et al.	6/26/2012		
	A242	8247259	Grolier et al.	8/21/2012		
	A243	8259293	Andreou et al.	9/4/2012		
	A244	8288702	Veeder	10/16/2012		
	A245	8476681	Haddad et al.	7/2/2013		
	A246	8564087	Yamamura et al.	10/22/2013		
	A247	8603902	Mazer et al.	12/10/2013		
	A248	8629485	Yamamura et al.	1/14/2014		
	A249	8680591	Haddad et al.	3/25/2014		
	A250	8742528	Yamamura et al.	6/3/2014		
	A251	8884226	Miyazaki, et al.	11/11/2014		
	A252	8916945	Sakamoto et al	12/23/2014		
	A253	8994135	Yamamura et al.	03/31/2015		
	A254	9190551	Yamamura et al.	11/17/2015		
	A255	RE43169	Parker	2/7/2012		
	A256	20010017344	Aebi	8/30/2001		
	A257	20010022768	Takahashi	9/20/2001		

Change(s) applied to document,
/D.D./
6/1/2017

Examiner Signature	/LONG PHAM/	Date Considered	07/15/2016

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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SAMSUNG EX. 1002 - 4139/4148

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/747,875	02/27/2018	9905599	143705.05211	1722

136549 7590 02/07/2018

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Martin U. Pralle, Wayland, MA;
SiOnyx, Inc., Beverly, MA;
Jeffrey McKee, Tualatin, OR;
Jason Sickler, Arlington, MA;

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To: docketingbn@pepperlaw.com,davisdr@pepperlaw.com,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 136549

Feb 08, 2018 03:34:35 AM

Dear PAIR Customer:

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 136549 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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Application	Document	Mailroom Date	Attorney Docket No.
14747875	ISSUE.NTF	02/07/2018	143705.05211

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

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Thank you for prompt attention to this notice,

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

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Application Number	14/747,875
Filing Date	23-Jun-2015
First Named Inventor	Martin U. PRALLE
Title	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
Art Unit	
Examiner Name	
Attorney Docket Number	143705.000332

SIGNATURE of Applicant or Patent Practitioner

Signature	/Gunnar G. Leinberg/	Date (Optional)	2022-09-01
Name	Gunnar G. Leinberg	Registration Number	35,584
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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SAMSUNG EX. 1002 - 4142/4148

Doc Code: PA..
Document Description: Power of Attorney

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 11951

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

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☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

SiOnyx, LLC

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Steven D. Saylor		
Title	President and CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

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This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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SAMSUNG EX. 1002 - 4143/4148

Electronic Acknowledgement Receipt

EFS ID:	46532872
Application Number:	14747875
International Application Number:	
Confirmation Number:	1722
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Gunnar G. Leinberg/Mary Frances Heeks
Filer Authorized By:	Gunnar G. Leinberg
Attorney Docket Number:	143705.05211
Receipt Date:	01-SEP-2022
Filing Date:	23-JUN-2015
Time Stamp:	10:55:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	20220901_Corrected_POA_with_Transmittal_143705_000332.pdf	328413 755dd3cc59ade6d26aa65e2a59087446d63ce628	no	2
Warnings:					

SAMSUNG EX. 1002 - 4144/4148

Information:	
Total Files Size (in bytes):	328413

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SAMSUNG EX. 1002 - 4145/4148

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/747,875	06/23/2015	Martin U. Pralle	143705.05211

CONFIRMATION NO. 1722

POWER OF ATTORNEY NOTICE



136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

Date Mailed: 09/16/2022

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/01/2022.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ylueng/

SIONYX1403000040.0040

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/747,875	06/23/2015	Martin U. Pralle	143705.000332

CONFIRMATION NO. 1722

POA ACCEPTANCE LETTER

11951
Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
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OC000000136285992

Date Mailed: 09/16/2022

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/01/2022.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ylueng/

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Application	Document	Mailroom Date	Attorney Docket No.
14747875	N570	09/16/2022	143705.000332
	N570	09/16/2022	143705.000332

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