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CONFIRMATION NO. 7315

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THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

FILING RECEIPT



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Date Mailed: 04/10/2012

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Applicant(s)

Martin U. Pralle, Wayland, MA;

Power of Attorney:

Todd Alder--54598

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/614,275**

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Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

Pixel Isolation Elements, Devices and Methods of Making the Same

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET – Page 1 of 2

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. electronically filed

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Martin U.	Pralle	Wayland, MA
<i>Additional inventors are being named on the _____ separately numbered sheets attached hereto.</i>		
TITLE OF THE INVENTION (500 characters max):		
Pixel Isolation Elements, Devices and Methods of Making the Same		
<i>Direct all correspondence to:</i> CORRESPONDENCE ADDRESS		
☒ The address corresponding to Customer Number: 20,551		
OR		
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ENCLOSED APPLICATION PARTS (check all that apply)		
☐ Application Data Sheet. See 37 CFR 1.76 ☐ CD(s), Number of CDs _____		
☒ Drawing(s) <i>Number of Sheets</i> <u>1</u> ☐ Other (specify) _____		
☒ Specification (e.g. description of the invention) <i>Number of Pages</i> <u>14</u>		
Fees Due: Filing Fee of \$220 (\$110 for small entity). If the specification and drawings exceed 100 sheets of paper, an application size fee is also due, which is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).		
METHOD OF PAYMENT OF THE FILING FEE AND APPLICATION SIZE FEE FOR THIS PROVISIONAL APPLICATION FOR PATENT		
☒ Applicant claims small entity status. See 37 CFR 1.27. \$125		
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PROVISIONAL APPLICATION COVER SHEET
Page 2 of 2

PTO/SB/16 (12-08)

Approved for use through 06/30/2010. OMB 0651-0032

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SIGNATURE /Todd B. Alder/ Date March 22, 2012

TYPED or PRINTED NAME Todd B. Alder, Ph.D. REGISTRATION NO. 54598
(if appropriate)

TELEPHONE (801) 566-6633 Docket Number: 3035-052.PROV

PIXEL ISOLATION ELEMENTS, DEVICES AND METHODS OF MAKING THE SAME

TECHNICAL FIELD

This application relates to image sensor pixels and elements for isolating neighboring pixels in the image sensor. More specifically, the isolation elements are configured to optically and electrically isolate neighboring pixels.

BACKGROUND

Image sensors are typically formed on various forms of silicon material. Many imagers are placed in many applications such as digital cameras, camcorders, computers and cell phones. Due to the ever decreasing size (foot print) of these applications, the image sensors are have likewise reduced in size. Backside illuminated (BSI) image sensors have increase in importance due to their small size as compared to Front side illuminated (FSI) image sensors. However, pixel size reduction is only acceptable without significant sacrifice in image quality. As pixel sizes continue to decrease, there is a reduction in image signal to noise as well an increase in electrical and optical cross-talk between adjacent sensor pixels. These effects have been offset by adding microlenses above each image sensor in front side pixel sensors to focus the light on the active detector regions, thereby increasing efficiency and reducing cross-talk.

Backside illuminated pixel sensors present different design considerations, the back surface is typically planar and can cause significant cross-talk due to reflection off the back surface. Trenches have been formed between adjacent pixels to reduce the amount of cross-talk experienced by the pixels.

SUMMARY

The present disclosure provides image sensors, front side or backside, 3D sensors and systems that incorporate a unique isolation element configured to reduce cross-talk. In one aspect, the image sensors of the present disclosure are capable of detecting visible and infrared light, whereas the isolation features can be designed and configured to reduce and in some cases eliminate electrical and/or optical cross-talk from straying visible and infrared light. The isolation element may be doped with dopant which enables the repelling of electrical carriers

from the side walls. Further the isolation elements may include materials having either a lower or higher refractive index than silicon based materials. When a higher refractive index material is disposed in a trench, the optical cross-talk is reduced due to the internal reflection off the higher refractive index material. Moreover, the isolation element may include surface features formed on the side walls of the trenches. The surface features can have an average peak to valley height of about 10nm to about 10 μ m. Lastly, the pixel can further include a textured region formed on a side opposite the incident radiation side. Such features can enable the device to detect infrared light.

BRIEF DESCRIPTION OF THE FIGURES

Fig. 1 illustrates a cross-sectional view of multiple image sensor pixels having a standard isolation element disposed therebetween, in accordance with the description of the present disclosure;

Fig. 2 shows a cross-sectional view of two adjacent pixels including an isolation element configured to reduce optical and electrical cross-talk in accordance with the present of the present disclosure; and

Fig. 3 shows a cross-sectional view of two adjacent pixels having an isolation element for reducing cross-talk and a textured region for enhancing reflection within the pixel, in accordance with yet another embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE INVENTION

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms “a,” and, “the” can include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to “a dopant” can include one or more of such dopants and reference to “the layer” can include reference to one or more of such layers.

As used herein, the terms “light” and “electromagnetic radiation” can be used interchangeably and can refer to light or electromagnetic radiation in the ultraviolet, visible, near

infrared and infrared spectra. The terms can further more broadly include electromagnetic radiation such as radio waves, microwaves, x-rays, and gamma rays. Thus, the term “light” is not limited to electromagnetic radiation in the visible spectrum. Many examples of light described herein refer specifically to electromagnetic radiation in the visible and infrared (and/or near infrared) spectra. For purposes of this disclosure, visible range wavelengths are considered to be from approximately 350nm to 800nm and non-visible wavelengths are longer than about 800nm or shorter than about 350 nm. The infrared spectrum includes a near infrared portion of the spectrum including wavelengths of approximately 800 to 1100 nm, a short wave infrared portion of the spectrum including wavelengths of approximately 1100 nm to 3 micrometers, and a mid to long wave infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as “infrared” portions of the electromagnetic spectrum unless otherwise noted.

As used herein, “quantum efficiency” (QE) is defined as the percentage of photons incident on an optoelectronic device that are converted into electrons. External QE (EQE) is defined as the current obtained outside of the device per incoming photon. As such, EQE therefore depends on both the absorption of photons and the collection of charges. The EQE is lower than the QE due to recombination effects and optical losses (e.g. transmission and reflection losses).

As used herein, the terms “3D” and “three dimensional” can be used interchangeably, and refer to obtaining distance information from electromagnetic radiation.

As used herein, the terms “disordered surface” and “textured surface” can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations. Such a surface topology can be formed by the irradiation of a laser pulse or laser pulses, chemical etching, lithographic patterning, interference of multiple simultaneous laser pulses, or reactive ion etching. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers) and nanopores. In another aspect, such a surface can include micron-sized structures (e.g. about 1 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm . A variety of

techniques can be utilized to measure the size of such structures. For example, for cone-like structures the above ranges are intended to be measured from the peak of a structure to the valley formed between that structure and an adjacent neighboring structure. For structures such as nanopores, the above ranges are intended to be approximate diameters. Additionally, the surface structures can be spaced at various average distances from one another. In one aspect, neighboring structures can be spaced at a distance of from about 50nm to about 50 μm from. In another aspect, neighboring structures can be spaced at a distance of from about 50nm to about 2 μm from. Such spacing is intended to be from a center point of one structure to the center point of a neighboring structure.

As used herein, the term “fluence” refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, “fluence” can be described as the energy density of one laser pulse.

As used herein, the terms “surface modifying” and “surface modification” refer to the altering of a surface of a semiconductor material using laser irradiation, chemical etching, reactive ion etching, lithographic patterning, etc. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping of a semiconductor material.

As used herein, the term “target region” refers to an area of a semiconductor material that is intended to be doped or surface modified. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

As used herein, the term “monolithic” refers to an electronic device in which electronic components are formed on the same substrate. For example, two monolithic pixel elements are pixel elements that are formed on the same semiconductor substrate.

As used herein, the term “substantially” refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is “substantially” enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute

completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained.

As used herein, the term “about” is used to provide flexibility to a numerical range endpoint by providing that a given value may be “a little above” or “a little below” the endpoint. As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity, and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of “about 1 to about 5” should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

The following disclosing relates to photosensitive diodes, pixels, and imagers capable of detecting visible and infrared light while exhibiting reduced optical and electrical cross-talk between neighboring pixels or diodes, including associated methods of making such devices. Such devices can additionally exhibit enhanced absorption and quantum efficiencies. In one aspect, for example, such an image sensor can include a plurality of photodiodes or pixels. Such

photodiodes or pixels may include at least a semiconductor substrate having a first side for receiving incident light and a second side opposite the first side. Both the first and second sides may include at least one doped region. Further the image sensor may include at least one isolation element or feature for at least partially separating and isolating neighboring pixels. Figure 1 illustrates a simplified drawing of an imager having a first pixel 102 and a second pixel 104, that are formed monolithically on a common silicon semiconductor substrate 106. Doped regions 108 and 110 can be disposed on either the first side 120 or second side 122 of the semiconductor substrate as shown in Figure 1. In the present figure, device is configured such that the first side is capable of receiving incident light. A textured region 112 having surface features, is created on the second side of the semiconductor substrate. The present architecture having the texture region on the back side can enable enhanced detection and absorption of electromagnetic radiation having wavelengths in the range of about 600nm to about 1200nm. It should be noted that this simple architecture can be used in either a FSI or BSI image sensor architecture.

In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, scatters off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. BSI imagers, on the other hand, are configured to have the light sensing portion of the device opposite the circuitry. Incident light enters the device via the light sensing portion and is mostly absorbed prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. As mentioned, the devices according to aspects of the present disclosure can be adapted for either configuration. It should also be understood that devices according to aspects of the present disclosure can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures.

Regarding the isolation elements, also referred to herein as trench isolation features, various processes can be employed to form the isolation elements. It should be noted that, the isolation features may extend from either the first surface or the second surface into the semiconductor material and depending on the depth of the trench can be considered either deep

trench isolation or shallow trench isolation. The dimensions of the trench can vary, depending on the application. For example, the trenches can have sloping side walls or have a bottle neck architecture. The depth of the trench isolation feature can be in the range of about 100nm to about 50 μ m. The width can be in the range of about 100nm to about 10 μ m. For simplicity, the figures in this disclosure show deep trench isolation but it should be understood by those skilled in the art that shallow trench isolation is applicable and deep trench isolation need not completely extend from one side to the other. The processes contemplate for forming trenches or other isolation features may include, reactive ion etch, isotropic plasma etch, wet chemical etch, laser irradiation and other known chemical etches by those skilled in the art.

For optical isolation from pixel to pixel, the large index of refraction mismatch can result in total reflection at the trench side walls. To prevent excessive dark current in the pixels, a passivation layer may be disposed on the side walls of the trench to prevent the generation of carriers and leakage current. Silicon nitride deposited over a thin grown oxide layer is commonly used, in this case the oxide may be a low temperature grown plasma oxide.

It can be shown through calculations that a low recombination velocity of silicon oxide and silicon nitride is the result of moderately high positive oxide charge (5×10^{11} to 1×10^{12} cm^{-2}) and relatively low midgap interface state density (1×10^{10} to 4×10^{10} $\text{cm}^{-2} \text{eV}^{-1}$). The addition of silicon oxide or nitride can reduce surface recombination and surface generation. Reducing the surface recombination can increase quantum efficiency of photon collection and surface generation can cause excessive dark current in the imagers thereby reducing the quality of the image.

Since the positive oxide charge of silicon nitride or silicon oxynitride is relatively low on silicon on insulator imagers a p-type layer can be adjacent the silicon oxide, silicon oxynitride and/or silicon nitride layers as an alternative embodiment. In this case the p-type layer will accumulate the surface or the backside of the p-type silicon layer and p-type sidewalls.

Other possible passivation techniques include a hot steam anneal of hydrogenated silicon nitride or the use of amorphous silicon.

Aluminum oxide can also be deposited in the trench to form an isolating barrier. Aluminum oxide can have low stress, a negative fixed charge and higher index of refraction than silicon oxide or low stress silicon oxynitride nitride. Low surface recombination velocities, as low as 10 cm/s can be obtained through various deposition processes of Al_2O_3 layers on the

silicon substrate. Low surface recombination can be achieved by field induced surface passivation due to a high density of negative charges stored at the interface. PECVD aluminum oxide is described here for the backside passivation of the backside and backside trenches in backside illuminated image sensors.

The index of refraction of the aluminum oxide can be increased slightly as required by the addition of other metallic elements to make ternary insulators like Aluminum Oxynitride (AlON), Hafnium Aluminum Oxide (HfAlO), Zirconium Aluminum Oxide (ZrAlO), Lanthanum Aluminum Oxide (LaAlO), Titanium Aluminum Oxide (TiAlO) or quaternary dielectrics like Hafnium Aluminum Oxynitride (HfAlON), Tantalum Aluminum Oxynitride (TaAlON), Lanthanum Aluminum Oxynitride (LaAlON).

Low temperature PECVD deposition processes are contemplated for the backside passivation of the backside and backside trenches in backside illuminated image sensors. As previously mentioned the large index of refraction mismatch between silicon and the insulators in the trenches results in reflection of the incident light and provides optical isolation. The trenches also provide electrical isolation.

An alternative embodiment is front side trenches on back side illuminated image sensors. Front side trenches and low temperature PECVD deposited insulators in the trenches can also be used as described here for backside illuminated image sensors. The large index of refraction mismatch between silicon and the insulators in the trenches results in reflection of the incident light and can provide the needed optical isolation.

In another aspect of the present disclosure, Figure 2 illustrates an imager have at least two pixels or photodiodes (102 and 104) and at least one isolation element 114. The isolation element may include at least two layers 116 comprised of material having a higher refractive index (n) than the semiconductor substrate 106. For explanation purposes, if the semiconductor substrate is comprised of crystalline silicon ($n \sim 3.49$ for a given wavelength) then layers 116 can be comprised of material with a higher refractive index than 3.49. Layer 118 can have a refractive index less than layer 116. Alternatively, layers 116 can have a lower refractive index than semiconductor substrate 106 if layer 118 has a high refractive index. For example, if semiconductor substrate is comprised of crystalline silicon ($n \sim 3.49$), then layer(s) 116 can be comprised of silicon dioxide ($n \sim 1.5$) and layer 118 can be comprised of a poly or amorphous silicon material ($n \sim 3.7 - 4.0$). In this embodiment the trench isolation feature will act a Bragg

reflector. Additionally, the silicon oxide and poly silicon layers can optically and electrically isolate the adjacent pixels. Layer 116 can have a thickness in the range of about 50nm to about 500nm. Layer 118 can have a thickness in the range of about 5nm to about 100nm. The main focus is to deposit adjacent materials having different indexes of refraction. The difference in refractive indexes and thickness can determine the intensity of the internal reflection of electromagnetic radiation. Notably, other materials such as metals, as well as other material not listed herein can be used to increase internal reflection of the light.

In still another aspect of the present disclosure, an photosensitive imager having at least two pixels (102 and 104) and at least one trench isolation region, as shown in Figure 3. The pixels can include a semiconductor substrate 106, having a first and second surface, 120 and 122 respectively; at least two doped regions 108 and 110, and a textured region formed on the opposite side of the side receiving the incident light, in this case the second side 122. The textured region can have surface features configured to reflect and disperse light. Methods for forming the textured region are disclosed herein. Further, the side walls 112 can include a texture region to increase the internal reflections of light. Regarding the isolation element 114 in Figure 3, the isolation element can include several layers of materials that can passivate the sidewalls and each have a different index of refraction. Further, a textured region or surface features can be formed on the side walls 112, of the trench (es). Again, the surface features can be of various heights and dimensions. The feature sizes and distances from nearest neighboring features can be adjusted to achieve optimum reflection for desired wavelengths.

Regarding the photodiodes themselves, a variety of semiconductor materials are contemplated for use with such devices. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include

at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $\text{Al}_x\text{Ga}_{1-x}\text{As}$), indium gallium arsenide (InGaAs, $\text{In}_x\text{Ga}_{1-x}\text{As}$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

Furthermore, the semiconductor device layer can be of any thickness that allows electromagnetic radiation detection and conversion functionality, and thus any such thickness of semiconductor device layer is considered to be within the present scope. In some aspects a textured region can be applied to the semiconductor device layer to increase the efficiency of the device such that the semiconductor device layer can be thinner than has previously been possible. Decreasing the thickness of the semiconductor reduces the amount of the often costly semiconductor material required to make such a device. In one aspect, for example, the semiconductor device layer has a thickness of from about 500 nm to about 50 μm . In another

aspect, the semiconductor device layer has a thickness of less than or equal to about 500 μm . In yet another aspect, the semiconductor device layer has a thickness of from about 2 μm to about 10 μm . In a further aspect, the semiconductor device layer can have a thickness of from about 5 μm to about 750 μm . In yet a further aspect, the semiconductor device layer can have a thickness of from about 5 μm to about 100 μm . In other aspects, the semiconductor device layer can have a thickness of from about 2 μm to about 5 μm .

One effective method of producing a textured region (i.e. quantum efficiency enhanced infrared light region) is through laser processing. Such laser processing allows discrete locations of the semiconductor substrate to be textured. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection. The laser treated region can be associated with the surface nearest the impinging electromagnetic radiation, or the laser treated surface can be associated with a surface opposite in relation to impinging electromagnetic radiation, thereby allowing the radiation to pass through the semiconductor material before it hits the laser treated region.

In one aspect, for example, a target region of the semiconductor material can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can be directed through a dopant carrier and onto the semiconductor surface. In this way, dopant from the dopant carrier is introduced into the target region of the semiconductor material. Such a region incorporated into a semiconductor material can have various benefits in accordance with aspects of the present disclosure. For example, the target region typically has a textured surface that increases the surface area of the laser treated region and increases the probability of radiation absorption via the mechanisms described herein. In one aspect, such a target region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of semiconductor material includes exposing the laser radiation to a dopant such that irradiation

incorporates the dopant into the semiconductor. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the semiconductor material is chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the formation of surface features appearing as microstructures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the semiconductor material. In some aspects, the surface features or microstructures can be on the order of 5 nm to 500 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed by the semiconductor material. In another aspect, the surface features can be from about 10 nm to about 20 μm in size.

The type of laser radiation used to surface modify a semiconductor material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to the wavelength of the laser radiation, pulse width, pulse fluence, pulse frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsatile lasing of a semiconductor material. A short-pulsed laser is one capable of producing femtosecond or picosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm , and more specifically from about 200 nm to about 1200 nm. The pulse width of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse widths can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse widths are in the range of from about 50 femtoseconds to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a semiconductor target region can be from about 2 to about 1000. Further, the repetition rate or frequency of the pulses can be selected to be in a range of from about 10 Hz to about 10 μHz , or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2 , or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2 .

It should be noted that other techniques for texturing the quantum efficiency enhanced infrared light region are considered to be within the present scope. Non-limiting examples include chemical etching, physical abrasion, material deposition, and the like.

A variety of dopant materials are contemplated, and any such material that can be used in the laser treatment process to surface modify a semiconductor material according to aspects of the present disclosure is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the semiconductor material being laser treated, as well as the intended use of the resulting semiconductor material. For example, the selection of potential dopants may differ depending on whether or not tuning of the photosensitive device is desired. Additionally, such dopant can be utilized in the textured region or in the other various doped regions of the device.

A dopant can be either electron donating or hole donating. In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H₂S, SF₆, SO₂, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of between about 5×10^{14} and about 1×10^{16} ions/cm². Non-limiting examples of fluorine-containing compounds can include ClF₃, PF₅, F₂ SF₆, BF₃, GeF₄, WF₆, SiF₄, HF, CF₄, CHF₃, CH₂F₂, CH₃F, C₂F₆, C₂HF₅, C₃F₈, C₄F₈, NF₃, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include B (CH₃)₃, BF₃, BCl₃, BN, C₂B₁₀H₁₂, borosilica, B₂H₆, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF₅, PH₃, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl₂, SiH₂Cl₂, HCl, SiCl₄, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH₃ and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H₂S, SF₆, or mixtures thereof. In

yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about $5.0 \times 10^{-8} \text{ mol/cm}^3$ to about $5.0 \times 10^{-4} \text{ mol/cm}^3$. SF_6 gas is a good carrier for the incorporation of sulfur into the semiconductor material via a laser process without significant adverse effects on the semiconductor material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

Additionally, the semiconductor device layer can be annealed for a variety of reasons, including dopant activation, semiconductor material repair, and the like. In those aspects including a laser textured region, the semiconductor material can be annealed prior to laser treatment, following laser treatment, during laser treatment, or both prior to and following laser treatment. Annealing can enhance the semiconductive properties of the device, including increasing the photoresponse properties of the semiconductor materials. Additionally, annealing can reduce damage done by the lasing process.

Of course, it is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present disclosure. Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the present disclosure and the appended claims are intended to cover such modifications and arrangements. Thus, while the present disclosure has been described above with particularity and detail in connection with what is presently deemed to be the most practical embodiments of the disclosure, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

Electronic Patent Application Fee Transmittal

Application Number:

Filing Date:

Title of Invention:

Pixel Isolation Elements, Devices and Methods of Making the Same

First Named Inventor/Applicant Name:

Martin U. Pralle

Filer:

Todd Brent Alder/Nicole Solomon

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First Named Inventor/Applicant Name:	Martin U. Pralle
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Provisional Cover Sheet (SB16)	3035052PROVtransmittal.pdf	1164907 50ae12426b98267dae523bf4f75d04bd8a7e3da0	no	2
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2		3035052PROVapplication.pdf	132585 f9e142afc9c29b08d812d4df2bcec50bd453bfb2	yes	15
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	Specification		1	14	
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Warnings:					
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3	Fee Worksheet (SB06)	fee-info.pdf	29421 c754001137a4cbab212d9f3b41eb0e9ead4d6cad	no	2
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