

CERTIFICATE OF TRANSLATION ACCURACY

I am a professional reviewer and coordinator specializing in translating Japanese, Korean, and Chinese to English and vice versa.

I served as Chief Examiner of the certified court interpreter test for the State of California and as a contract translator and interpreter for various federal agencies through the U.S. Department of State for more than a decade. I served as an instructor at the University of California at Berkeley and the Middlebury Institute of International Studies at Monterey (MIIS) Graduate Program in Translation.

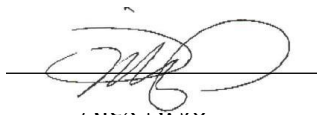
I have more than 30 years of experience reviewing thousands of technical, legal, and business documents from Japanese to English submitted to, among others, Japanese judicial authorities, U.S. federal courts, the U.S. International Trade Commission (ITC), and the USPTO Patent Trial and Appeal Board (PTAB).

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I certify under penalty of perjury that the foregoing is true and correct.

Executed this 28th day of October 2024 in Contra Costa County of the State of California.

By:

A handwritten signature in black ink, appearing to be 'M. B.', is written over a horizontal line.

Member, ATA

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(54) [Title of the Invention] SOLID-STATE IMAGING DEVICE

(57) ABSTRACT

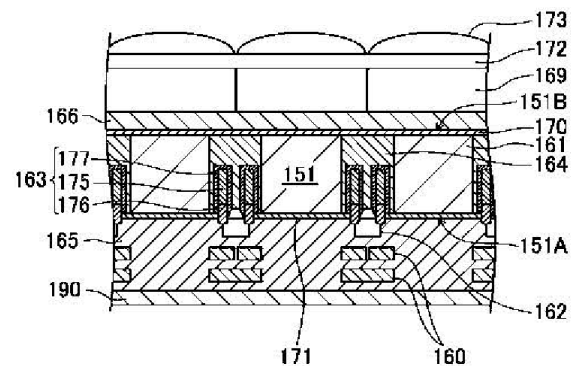
PROBLEM

To provide a back surface illuminated solid-state imaging device having high sensitivity and reduced color mixing.

RESOLUTION MEANS

The solid-state imaging device includes a semiconductor substrate 151, a plurality of photoelectric conversion units 161 formed on the semiconductor substrate 151, a partition part 163, a color filter 169, and an output circuit 162. The semiconductor substrate 151 has a light incident surface and a charge detection surface. The partition part 163 is formed between photoelectric conversion units 161 and has a silicon layer 175 embedded in the semiconductor substrate 151. The color filter 169 is formed on the light incident surface side, and the output circuit 162 is formed on the charge detection surface side. The silicon layer is made of amorphous silicon or polycrystalline silicon.

SELECTED DRAWING: FIG. 2



What is claimed is:

[Claim 1]

A solid-state imaging device, comprising:
a semiconductor substrate having a light incidence surface and a charge detection surface;
a plurality of photoelectric conversion units formed on the semiconductor substrate and containing first conductivity type impurity;
a partition part formed between the photoelectric conversion units and having a silicon layer embedded in the semiconductor substrate;
a color filter formed on the light incident surface side; and
an output circuit formed on the charge detection surface side;
wherein the silicon layer is made of amorphous silicon or polycrystalline silicon.

[Claim 2]

The solid-state imaging device according to claim 1, wherein the partition part has a side silicon oxide film formed between the silicon layer and the semiconductor substrate.

[Claim 3]

The solid-state imaging device according to claim 1, wherein the partition part has an upper silicon oxide film formed on the charge detection surface side of the silicon layer, and the upper silicon oxide film protrudes from the charge detection surface.

[Claim 4]

The solid-state imaging device according to claim 1, wherein the silicon layer contains phosphorus, boron or arsenic.

[Claim 5]

The solid-state imaging device according to claim 1, wherein a negative voltage is applied to the silicon layer.

[Claim 6]

The solid-state imaging device according to claim 1, wherein the position in the photoelectric conversion unit where the concentration of the first conductivity type impurity is a maximum is closer to the light incident surface than the position in the partition part closest to the light incident surface.

[Claim 7]

The solid-state imaging device according to claim 1, further comprising:
a second conductivity type layer formed on the light incident surface and containing a second conductivity type impurity;
wherein the partition part extends from the charge detection surface to the second conductivity type layer.

DETAILED DESCRIPTION OF THE INVENTION

TECHNICAL FIELD

[0001]

The present invention relates to a solid-state imaging device, and more particularly to a solid-state imaging device in which a charge is extracted from a surface opposite to a light incident surface.

BACKGROUND ART

[0002]

In recent years, metal-oxide-semiconductor (MOS) solid-state imaging devices have been attracting attention as devices capable of low power consumption operation and high speed imaging. MOS type solid-state imaging devices are increasingly being used in a wide range of fields, such as cameras for mobile devices, in-vehicle cameras, surveillance cameras, and the like.

[0003]

In a typical MOS solid-state imaging device, a plurality of pixels, each including a photoelectric conversion unit made of a photodiode, are arranged in an array. Each pixel has an output circuit for extracting the charge stored in the photoelectric conversion unit. The output circuit includes, for example, a transfer transistor, an amplification transistor, a selection transistor, a reset transistor, and the like. The charges photoelectrically converted in the photoelectric conversion unit are transferred to a floating diffusion layer by a transfer transistor. The charges transferred to the floating diffusion layer are amplified by the amplification transistor and transmitted to an output signal line provided for each column via a selection transistor selected by a vertical shift register.

The charges transmitted to the output signal line are output to an output terminal via a horizontal shift register. The excess charge accumulated in the floating diffusion layer is discharged by a reset transistor having a drain region connected to a power supply line.

[0004]

As solid-state imaging devices become smaller, studies are being conducted on back surface illuminated solid-state imaging devices in which an output circuit is formed on a surface opposite to the light incident surface on which light is incident. FIG. 7 depicts an example of a configuration of a back surface illuminated solid-state imaging device. As depicted in FIG. 7, a semiconductor substrate is formed with an n-type silicon layer (n- layer) 216 having a low impurity concentration, a p-type silicon layer (p- layer) 214 having a low impurity concentration stacked on the back surface side of the n- layer 216, and a p-type silicon layer (p+ layer) 212 having a high impurity concentration stacked on the back surface side of the p- layer 214. Furthermore, a pixel isolation region 228 made of a p-type impurity diffusion layer is formed on the front surface side of the n- layer 216. A p-type well region 234 having a low impurity concentration is formed below the pixel isolation region 228. A p-type silicon layer 222 having a high impurity concentration is formed on the front surface side of each light receiving region, and a silicon layer 224 containing n-type impurities is formed on the back surface side of the silicon layer 222. An insulating film 242 made of silicon oxide, silicon nitride, or the like that is transparent to incident light is formed on the back surface side of the p+ layer 212 of the semiconductor substrate. A high refractive index transparent layer 244 is formed on the light incident surface side of the insulating film 242. A color filter layer having a plurality of color filters 246 arranged in a horizontal direction is formed on the light incident surface of the high refractive index transparent layer 244. A light shielding member 248 for preventing color mixing (crosstalk) is formed between adjacent color filters 246, and a microlens 252 is formed on the color filter 246.

[0005]

An embedded member 218 made of a light-reflective material such as tungsten is formed inside the semiconductor substrate so as to separate adjacent pixels. An insulating film 219 made of silicon oxide or the like is formed between the embedded member 218 and the silicon layer. Incident light can be prevented from entering the photoelectric conversion region of a pixel provided at a position other than the pixel into which the incident light is incident by forming the embedded member 218, and thus the occurrence of color mixing can be prevented.

PRIOR ART DOCUMENTS

Patent Documents

[0006]

Patent Document 1: Japanese Unexamined Patent Application Publication 2009-88030

SUMMARY OF THE INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION

[0007]

However, conventional back surface illuminated solid-state imaging devices have the following problems. The embedded member embedded between the pixels is made of a material that reflects light, such as a metal or the like. A single crystal epitaxial layer cannot easily be formed on the embedded member because metal and silicon have different lattice constants. Therefore, the silicon layer formed on the embedded member contains many crystal defects. As a result, the charge generated when dark increases, and the sensitivity of the solid-state imaging device decreases.

[0008]

Furthermore, a conventional back surface illuminated solid-state imaging device employs a CCD-type charge readout configuration when reading out charges from a photoelectric conversion unit. Therefore, a light reflective material cannot be formed on the side of the semiconductor substrate where the read electrode is formed, and therefore obliquely incident light cannot be completely absorbed. For example, only about 90% of light with a wavelength of 650 nm is absorbed by a silicon material with a thickness of 10 μm . Color mixing cannot be reduced if the absorption of obliquely incident light is insufficient. Furthermore, metal is embedded in the silicon material, so the metal is thermally diffused into the silicon material by heat treatment during the process. This also increases crystal defects in the silicon layer and increases charges generated when dark, resulting in a decrease in sensitivity.

[0009]

In light of the foregoing, an object of the present invention is to provide a back surface illuminated solid-state imaging device having high sensitivity and reduced color mixing.

MEANS FOR SOLVING THE PROBLEM

[0010]

In order to achieve the above object, the present invention provides a solid-state imaging device having a partition part made of a silicon layer.

[0011]

Specifically the solid-state imaging device of the present invention contains:
a semiconductor substrate having a light incident surface and a charge detection surface; a plurality of photoelectric conversion units formed on the semiconductor substrate and containing first conductivity type impurity; a partition part formed between the photoelectric conversion units and having a silicon layer embedded in the semiconductor substrate; a color filter formed on the light incidence surface side; and an output circuit formed on the charge detection surface side; wherein the silicon layer is made of amorphous silicon or polycrystalline silicon.

[0012]

The solid-state imaging device of the present invention includes a partition part formed between photoelectric conversion units and having a silicon layer embedded in a semiconductor substrate. Therefore, heavy metals such as iron, copper, nickel, and the like, contained in the semiconductor substrate during the process of manufacturing the solid-state image device can be gettered into the silicon layer. Therefore, the charge generated when dark can be reduced, and the sensitivity of the solid-state imaging device can be improved. Furthermore, the color filters are formed on the light incident surface side and the output circuit is formed on the charge detection surface side, so the distance between the color filters and the photoelectric conversion units can be reduced. Therefore, color mixing caused by obliquely incident light can be reduced. Furthermore, even long wavelength light that reaches deep inside the substrate is less likely to penetrate into adjacent pixels when obliquely incident, and thus color mixing is reduced.

[0013]

In the solid-state imaging device of the present invention, the partition part may have a side silicon oxide film formed between the silicon layer and the semiconductor substrate. With this configuration, crystal defects on the side surface of the groove for forming the partition part can be reduced, and the charges generated when dark can be reduced in order to achieve high sensitivity.

[0014]

In the solid-state imaging device of the present invention, the partition part may have an upper silicon oxide film formed on the charge detection surface side of the silicon layer, and the upper silicon oxide film may protrude from the charge detection surface. With this configuration, the gate wiring can be formed on the partition part.

[0015]

In the solid-state imaging device of the present invention, the silicon layer may contain phosphorus, boron or arsenic. With this structure, gettering of heavy metals in the silicon layer can be more reliably performed.

[0016]

In the solid-state imaging device of the present invention, a negative voltage may be applied to the silicon layer. With this configuration, a hole accumulation layer can be formed on the surface of the groove that forms the partition part. Thereby, charges generated by interface states due to crystal defects can be reduced, and thus high sensitivity can be achieved.

[0017]

In the solid-state imaging device of the present invention, the position in the photoelectric conversion unit where the concentration of the first conductivity type impurity is maximum may be located closer to the light incident surface than the position in the partition part closest to the light incident surface. With this configuration, color mixing can be further reduced when light in the visible light spectrum is obliquely incident.

[0018]

The solid-state imaging device of the present invention may further include a second conductivity type layer formed on the light incident surface and containing second conductivity type impurities, and thus the partition part may reach the second conductivity type layer from the charge detection surface. With this configuration, color mixing can be further reduced when light in the visible light spectrum is obliquely incident.

EFFECT OF THE INVENTION

[0019]

The solid-state imaging device of the present invention can provide a back surface illuminated solid-state imaging device having high sensitivity and reduced color mixing.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020]

FIG. 1 is a circuit diagram depicting a solid-state imaging device according to an embodiment.

FIG. 2 is a cross-sectional view depicting a pixel portion of the solid-state imaging device according to an embodiment.

FIG. 3 is a cross-sectional view depicting a method for manufacturing a solid-state imaging device according to an embodiment of the present invention in the order of the steps.

FIG. 4 is a cross-sectional view depicting a method for manufacturing a solid-state imaging device according to an embodiment of the present invention in the order of the steps.

FIG. 5 is a cross-sectional view depicting a method for manufacturing a solid-state imaging device according to an embodiment of the present invention in the order of the steps.

FIG. 6 is a cross-sectional view depicting a variation example of the solid-state imaging device according to an embodiment.

FIG. 7 is a circuit diagram depicting a solid-state imaging device according to a conventional example.

DESCRIPTION OF THE EMBODIMENTS FOR PRACTICING THE INVENTION

[0021]

FIG. 1 depicts a circuit configuration of a solid-state imaging device according to an embodiment. In the solid-state imaging device of the present embodiment, a plurality of pixels 100, each of which includes a photoelectric conversion unit 161 containing a photodiode are arranged in a matrix. Each pixel 100 has an output circuit 162 for extracting the charge stored in the photoelectric conversion unit 161. The output circuit 162 includes a plurality of MOS transistors, such as a transfer transistor 103, an amplification transistor 104, a selection transistor 106, a reset transistor 105, and the like. For example, the charge photoelectrically converted in the photoelectric conversion unit 161 is transferred to a floating diffusion layer 102 by a transfer transistor 103. The charges transferred to the floating diffusion layer 102 are amplified by the amplification transistor 104 and transmitted to an output signal line 111 provided for each column via a selection transistor 106 selected by a vertical shift register 108. The charges transmitted to the output signal line 111 are output to an output terminal 112 via the horizontal shift register 109. The excess charge accumulated in the floating diffusion layer 102 is discharged by a reset transistor 105 having a drain region connected to a power supply line.

[0022]

FIG. 2 depicts a cross-sectional structure of the pixel 100. In FIG. 2, only three pixels are depicted. Photoelectric conversion units 161, which are n-type diffusion regions, are formed in a matrix on a semiconductor substrate 151, which is a silicon substrate. The surface of the semiconductor substrate 151 is a charge detection surface 151A, on which an output circuit 162 including a plurality of MOS transistors is formed. The back surface of the semiconductor substrate 151 is a light incident surface 151B, on which a plurality of color filters 169, lenses 173, and the like are formed.

[0023]

The output circuit 162 is formed between adjacent photoelectric conversion units 161, and a partition part 163 is formed between the photoelectric conversion unit 161 and the source/drain region of the transistor that constitutes the output circuit 162. An interlayer film 165 is formed on the charge detection surface 151A so as to cover the output circuit 162, and a plurality of wirings 160 are formed on the interlayer film 165. The wiring 160 includes a control line for driving an output circuit 162 and an output line for outputting an electric charge. An isolation diffusion layer 164, which is a p-type diffusion layer, is formed between adjacent photoelectric conversion units 161. Thereby, adjacent photoelectric conversion units 161 can be electrically isolated, and thus color mixing can be reduced.

[0024]

The color filters 169 are formed corresponding to the respective photoelectric conversion units 161. The color filter 169 includes a B filter that transmits short-wavelength light of about 450 nm with high efficiency, an R filter that transmits long-wavelength light of about 650 nm with high efficiency, and a G filter that transmits medium-wavelength light of about 550 nm with high efficiency, and forms a Bayer array or the like. An insulating film 166 made of silicon oxide (SiO₂), silicon nitride (SiN), or the like is formed between the color filter 169 and the light incident surface 151B. A lens 173 is formed on the color filter 169 via a planarizing layer 172.

[0025]

A high concentration p-type layer 170 is formed on the light incident surface 151B by diffusing a high concentration of p-type impurities from the light incident surface 151B to a certain depth. By forming the high concentration p-type layer 170, charges generated when dark due to crystal defects in the light incident surface 151B are prevented from flowing into the photoelectric conversion unit 161, thereby reducing noise. A high concentration p-type layer 171 is formed on the charge detection surface 151A. By forming the high concentration p-type layer 171, charges generated in the dark due to crystal defects in the charge detection surface 151A can be prevented from flowing into the photoelectric conversion unit 161, thereby reducing noise.

[0026]

In general, in a MOS solid-state imaging device, a color filter is formed on multilayer wiring. This increases the distance from the substrate surface to the color filter, resulting in a greater effect of color mixing due to obliquely incident light. However, in the solid-state imaging device of the present embodiment, the color filters and the multilayer wiring are formed on different surfaces of the substrate. Therefore, the distance from the substrate surface to the color filter can be reduced. Specifically, the distance from the substrate surface to the color filter, which was conventionally about 4 μm , can be reduced to about 1 μm . This reduces color mixing by half.

[0027]

Moreover, the partition part 163 in the solid-state imaging device of the present embodiment has a silicon layer 175 made of amorphous silicon or polycrystalline silicon. When an oxide film is embedded in the partition part, making the aspect ratio of the partition part to be 3 or more is difficult. However, the silicon layer 175 can be formed by the LPCVD method, which has excellent embedding properties. Therefore, the aspect ratio of the partition part 163 can be increased to about 10 to 20. Therefore, the depth of the partition part 163 can be increased, and color mixing due to obliquely incident light can be further reduced.

[0028]

Furthermore, in the present embodiment, the partition part 163 has a silicon layer 175 formed on the light incident surface 151B side, and an upper SiO_2 film 176 formed on the charge detection surface 151A side. Therefore, the gate wiring and the gate electrode serving as pulse transmission wiring can be formed on the partition part 163. Thereby the number of wiring layers can be reduced, enabling low-cost manufacture with a short TAT (Turn Around Time).

[0029]

Specifically, in the partition part 163 in the solid-state imaging device of the present embodiment, a silicon layer 175 is embedded in a partition groove that is 0.2 μm wide and approximately 2.0 μm deep from the charge detection surface 151A to a position approximately 0.3 μm deep from the charge detection surface 151A, and an upper SiO_2 film 176 made of silicon oxide is formed on the charge detection surface 151A side of the silicon layer 175. The upper SiO_2 film 176 is formed so as to protrude from the charge detection surface 151A by about 50 nm. With this configuration, the position where the concentration of n-type impurities in the photoelectric conversion unit 161 is maximum is closer to the charge detection surface 151A than the deepest position of the partition part 163 from the charge detection surface 151A. Thereby, intrusion of long wavelength light into adjacent pixels can be reduced. The color mixing characteristic calculated as the ratio of the output value of a pixel provided with an R filter to the output value of a pixel provided with a G filter adjacent to the pixel provided with an R filter is approximately 0.5%. Generally, the depth at which the intensity of light incident on a silicon substrate is reduced by half is about 0.3 μm when the wavelength is 450 nm, about 0.8 μm when the wavelength is 550 nm, and about 2.3 μm when the wavelength is 650 nm. In this manner, light with a longer wavelength reaches deeper into the silicon substrate, and color mixing caused by obliquely incident light is more likely to be noticeable.

[0030]

The partition part 163 also has a side SiO_2 film 177 formed on the bottom and side surfaces of the partition groove. Thereby, crystal defects occurring on the side surfaces of the separation trenches can be reduced, and a decrease in sensitivity caused by charges generated when dark can be suppressed. The side SiO_2 film 177 may have a thickness of, for example, about 10 nm.

[0031]

In the solid-state imaging device of the present embodiment, the silicon layer 175 may be set to a ground potential or a negative voltage may be applied. In a solid-state imaging device having about 300,000 pixels, if there are about 10,000 pixels having an output of 69 mV or more when dark, providing the side SiO_2 film 177 can reduce this to number to 1000 or less.

Furthermore, when a voltage of -3 V is applied to the silicon layer 175, a hole accumulation layer with a concentration of about $1 \times 10^{18}/\text{cm}^3$ can be formed on the side wall of the partition groove. Thereby, the charges generated from the interface states of crystal defects can be reduced, and the number of pixels with a dark output of 69 mV or more can be reduced to 10 pixels or less.

[0032]

The semiconductor substrate 151 may be an SOI substrate. In general, Fe and Ni elements are not easily diffused in an SOI substrate in order to diffuse through a buried oxide (BOX) layer of about 200 nm. Therefore, these elements are not gettered in the Si substrate and remain on the SOI layer. Therefore, the number of pixels having an output of 69 mV or more in the dark state increases, and the characteristics are degraded. If a gettering location is provided in the SOI layer in order to avoid this, crystal defects will be concentrated at the gettering location, increasing the charge generated by heat and increasing the number of pixels with a dark output of 69 mV or more. On the other hand, when the silicon layer 175 is provided in the partition part 163, Fe elements and Ni elements can be gettered to a location isolated from the photoelectric conversion unit 161. In this case, about 98% of the light can be absorbed from the silicon layer of the SOI substrate. Therefore, in a solid-state imaging device having about 300,000 pixels, the number of pixels having an output of 69 mV or more in the dark state can be reduced to 10 or fewer.

[0033]

In the solid-state imaging device of the present embodiment, the photoelectric conversion unit 161 is formed with an implantation energy of 200 keV to 2000 keV, and the impurity concentration may be set to $1 \times 10^{14}/\text{cm}^3$ to $1 \times 10^{17}/\text{cm}^3$. The isolation diffusion layer 164 may be formed with an implantation energy of 100 keV to 3000 keV and an impurity concentration of $1 \times 10^{15}/\text{cm}^3$ to $1 \times 10^{18}/\text{cm}^3$. The high concentration p-type layers 170 and 171 may be formed with an implantation energy of 1 keV to 100 keV, and have an impurity concentration of $1 \times 10^{17}/\text{cm}^3$ to $1 \times 10^{20}/\text{cm}^3$. By increasing the impurity concentration of the high concentration p-type layer 170, the lifetime of the generated charges is shortened, and the flow of charges generated due to crystal defects into the photoelectric conversion unit 161 can be prevented. Due to the high concentration p-type layer 171, a portion of the photoelectric conversion unit 161 in all pixels is at the same depth from the charge detection surface 151A, and the transfer of accumulated charges from the photoelectric conversion unit 161 to the floating diffusion unit is performed in a shallow portion of the photoelectric conversion unit 161.

[0034]

A method for manufacturing the solid-state imaging device of the present embodiment will be described below. First, as depicted in FIG. 3A, a silicon nitride film 189 having a thickness of 10 nm to 200 nm is formed by CVD on the charge detection surface 151A of a semiconductor substrate 151 such as an SOI substrate or a silicon substrate. Subsequently, openings are formed in the silicon nitride film 189 at locations corresponding to the partition parts by photolithography, dry etching, or the like.

[0035]

Next, as depicted in FIG. 3B, an isolation groove 174 having a width of 0.1 μm to 0.5 μm and a depth of 1 μm to 5 μm is formed on the charge detection surface 151A side of the semiconductor substrate 151 by dry etching, using the silicon nitride film 189 as a hard mask.

[0036]

Next, as depicted in FIG. 3C, a side SiO_2 film 177 made of SiO_2 and having a thickness of 5 nm to 20 nm is formed on the side surface of the partition groove 174 by thermal CVD or the like. Subsequently, a silicon layer 175 is formed in the partition groove 174 by CVD, and then etched back to remove a portion of the side SiO_2 film 177 that is about 0.1 μm to 0.3 μm above the partition groove 174. In order to prevent charges generated when dark due to crystal defects on the partition groove 174 from flowing into the photoelectric conversion unit 161, p-type impurities are preferably injected into the side walls of the partition groove 174 after forming the side SiO_2 film 177. The p-type impurity may be injected under the conditions of an injection energy of 5 to 30 keV and an injection concentration of $1 \times 10^{14}/\text{cm}^3$ to $1 \times 10^{19}/\text{cm}^3$.

[0037]

Next, as depicted in FIG. 3(d), an upper SiO₂ film 176 made of SiO₂ is formed by a CVD method on top of the silicon layer 175.

[0038]

Next, as depicted in FIG. 4A, the upper SiO₂ film 176 on the silicon nitride film 189 is removed by CMP, and then the silicon nitride film 189 is removed by wet etching. As a result, a partition part 163 is formed in which the upper SiO₂ film 176 protrudes above the semiconductor substrate by about 50 nm. Next, the photoelectric conversion unit 161, the diffusion layer of the output circuit 162, the high concentration p-type layer 171, the isolation diffusion layer 164, and the like are formed in desired regions by photolithography and ion implantation. Next, a gate oxide film (not depicted) is formed by thermal oxidation, and a gate electrode is formed by the CVD method.

[0039]

Next, as depicted in FIG. 4B, an interlayer film 165 and wiring 160 are formed by film formation using a sputtering method and a CVD method, and patterning is performed using a photolithography method and a dry etching method.

[0040]

Next, as depicted in FIG. 4C, a support substrate 190 is attached to the interlayer film 165. The support substrate 190 may be a silicon substrate or the like. A quartz substrate or the like may also be used.

[0041]

Next, as depicted in FIG. 5A, the surface of the semiconductor substrate 151 opposite to the charge detection surface 151A is back ground and wet etched to form a light incident surface 151B on which the photoelectric conversion unit 161 is exposed. Subsequently, a high concentration p-type layer 170 is formed on the light incident surface 151B side by ion implantation. The high concentration p-type layer 170 may be formed with an implantation energy of 1 keV to 100 keV and an impurity concentration of $1 \times 10^{17}/\text{cm}^3$ to $1 \times 10^{20}/\text{cm}^3$.

[0042]

Subsequently, as depicted in FIG. 5B, an insulating film 166 having a thickness of 0.05 μm to 1 μm is formed on the high concentration p-type layer 170 by a CVD method, and a color filter 169 is formed by a spin coating method. The color filter 169 may have, for example, a Bayer array. Subsequently, a lens 173 is formed via the planarizing layer 172 by spin coating and dry etching.

[0043]

The partition part 163 may have any depth from the charge detection surface 151A that is deeper than the position in the photoelectric conversion unit 161 where the impurity concentration is highest. Therefore, as depicted in FIG. 6, the partition part 163 may reach the high concentration p-type layer 170. In this case, for example, the thickness of the semiconductor substrate 151 may be set to 3 μm , and the partition groove that forms the partition part 163 may be set to have a width of 0.3 μm and a depth of 2.8 μm . When the partition part 163 reaches the high concentration p-type layer 170, the adjacent photoelectric conversion units 161 can be physically separated from each other. This enables further improvement to the color mixing properties. The ratio of the output value of a pixel provided with an R filter to the output value of a pixel provided with a G filter adjacent to the pixel provided with an R filter is ultimately about 0.01%.

INDUSTRIAL APPLICABILITY

[0044]

The solid-state imaging device according to the present invention is capable of improving sensitivity and reducing color mixing, and is particularly useful as a solid-state imaging device in which charges are extracted from the surface opposite to the light incident surface.

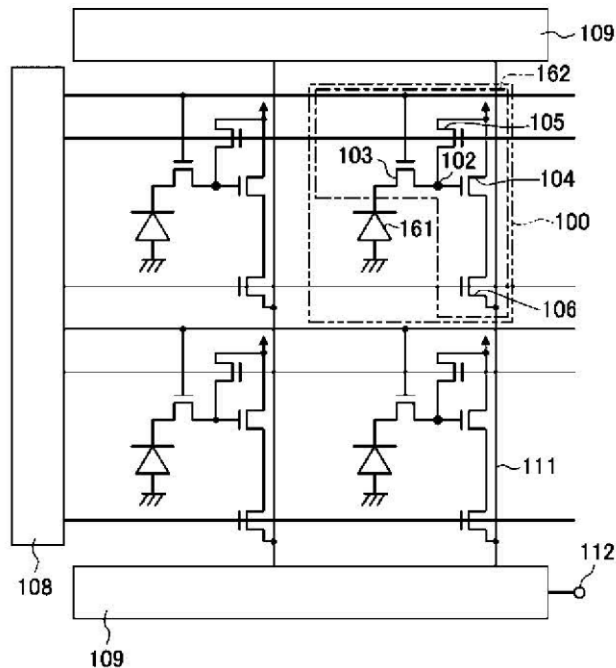
DESCRIPTION OF REFERENTIAL NUMERALS

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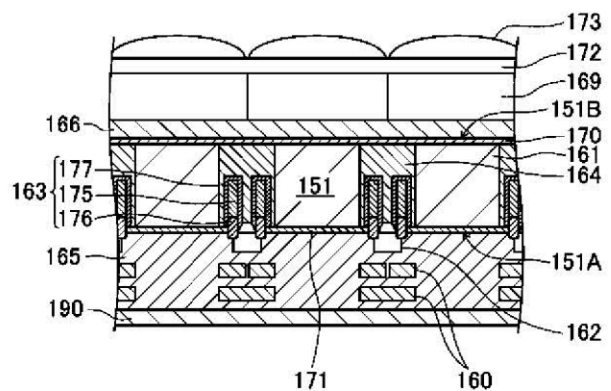
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- 102. Floating diffusion layer
- 103. Transfer transistor
- 104. Amplification transistor
- 105. Reset transistor
- 106. Selection transistor
- 108. Vertical shift register
- 109. Horizontal shift register

- 111. Output signal line
- 112. Output terminal
- 151. Semiconductor substrate
- 151A. Charge detection surface
- 151B. Light incident surface
- 160. Wiring
- 161. Photoelectric conversion unit
- 162. Output circuit
- 163. Partition part
- 164. Separation and diffusion layer
- 165. Interlayer film
- 166. Insulating film
- 169. Color filter
- 170. High concentration p-type layer
- 171. High concentration p-type layer
- 172. Planarization layer
- 173. Lens
- 174. Partition groove
- 175. Silicon layer
- 176. Upper SiO₂ film
- 177. Side SiO₂ film
- 189. Silicon nitride film
- 190. Support substrate

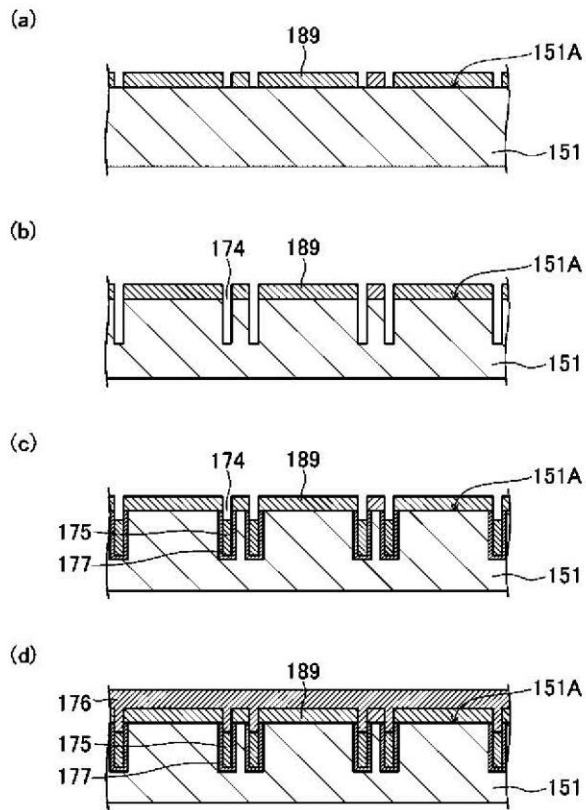
[FIG. 1]



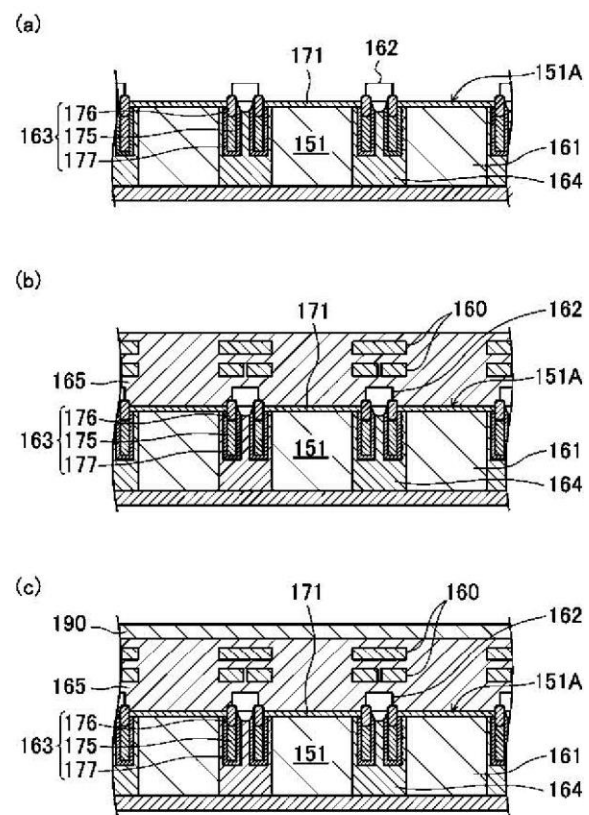
[FIG. 2]



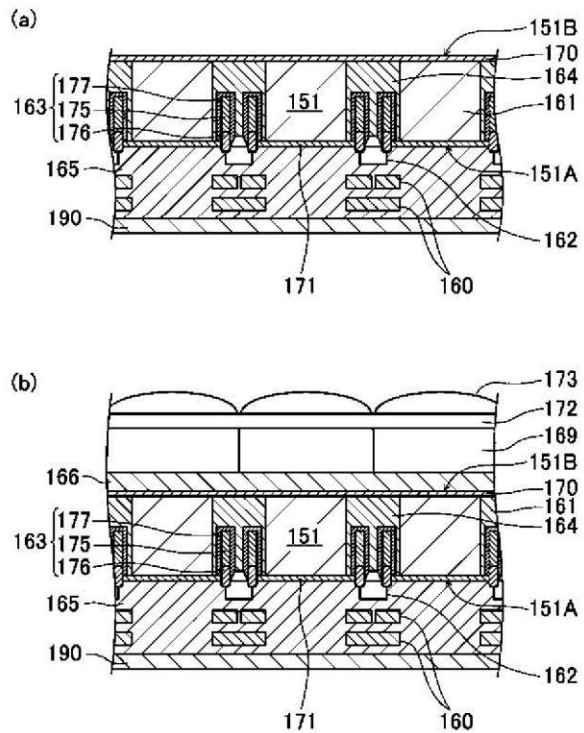
[FIG. 3]



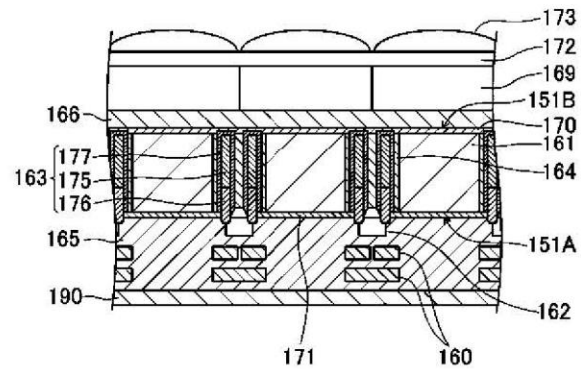
[FIG. 4]



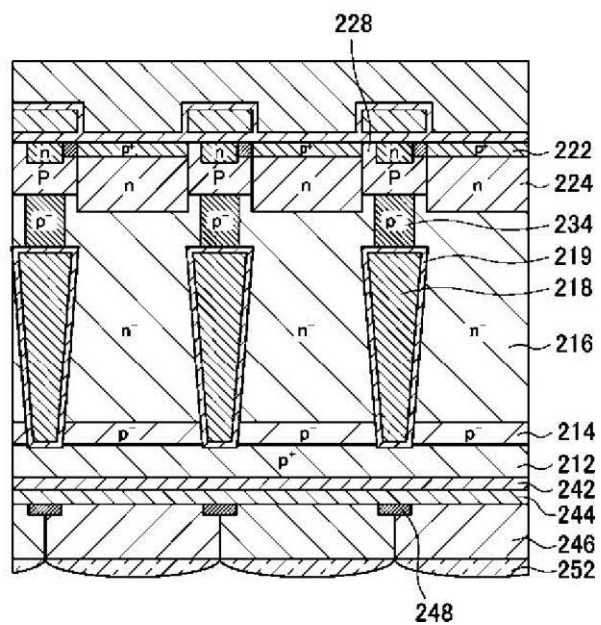
[FIG. 5]



[FIG. 6]



[FIG. 7]



Continued from front page

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