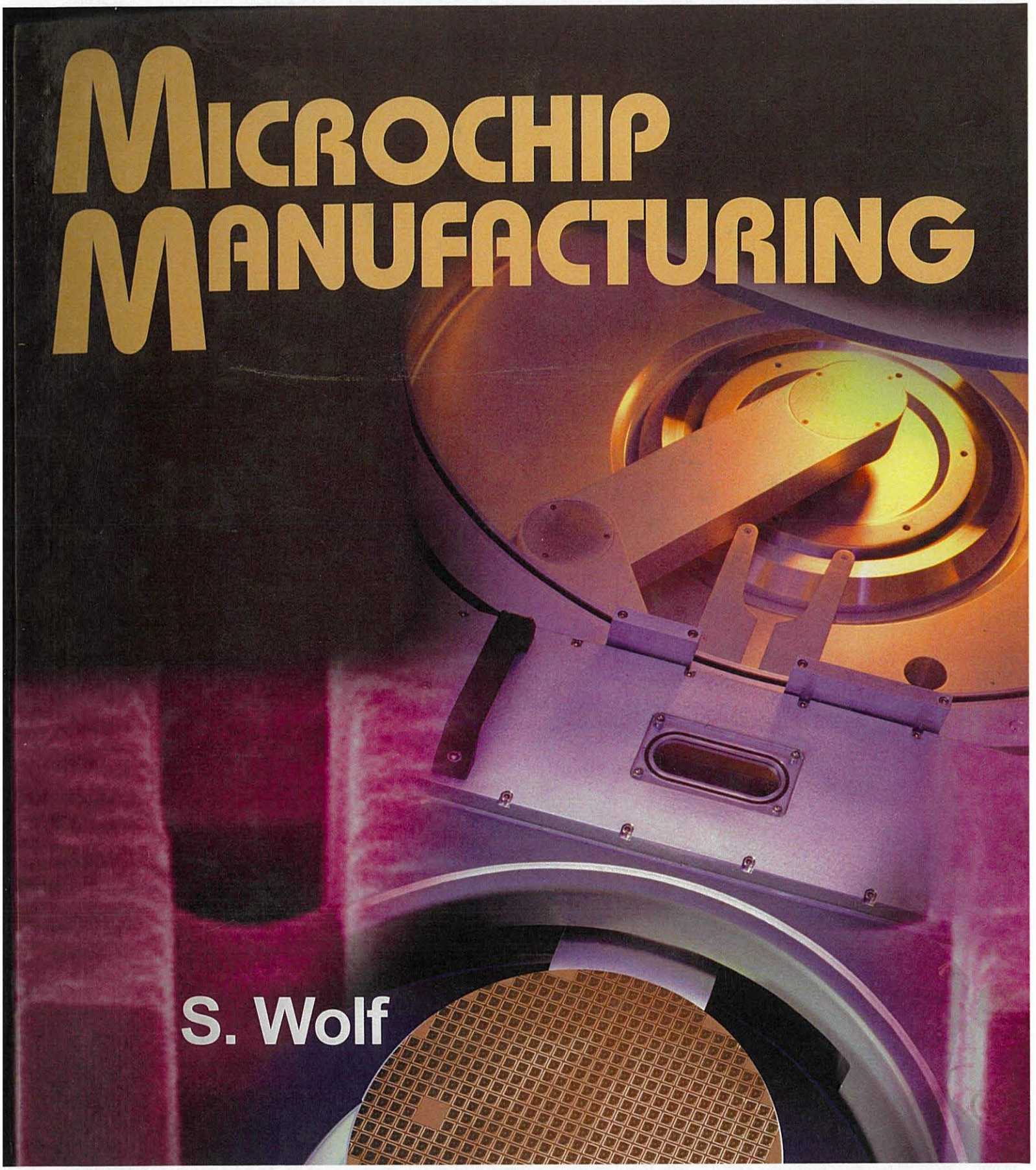
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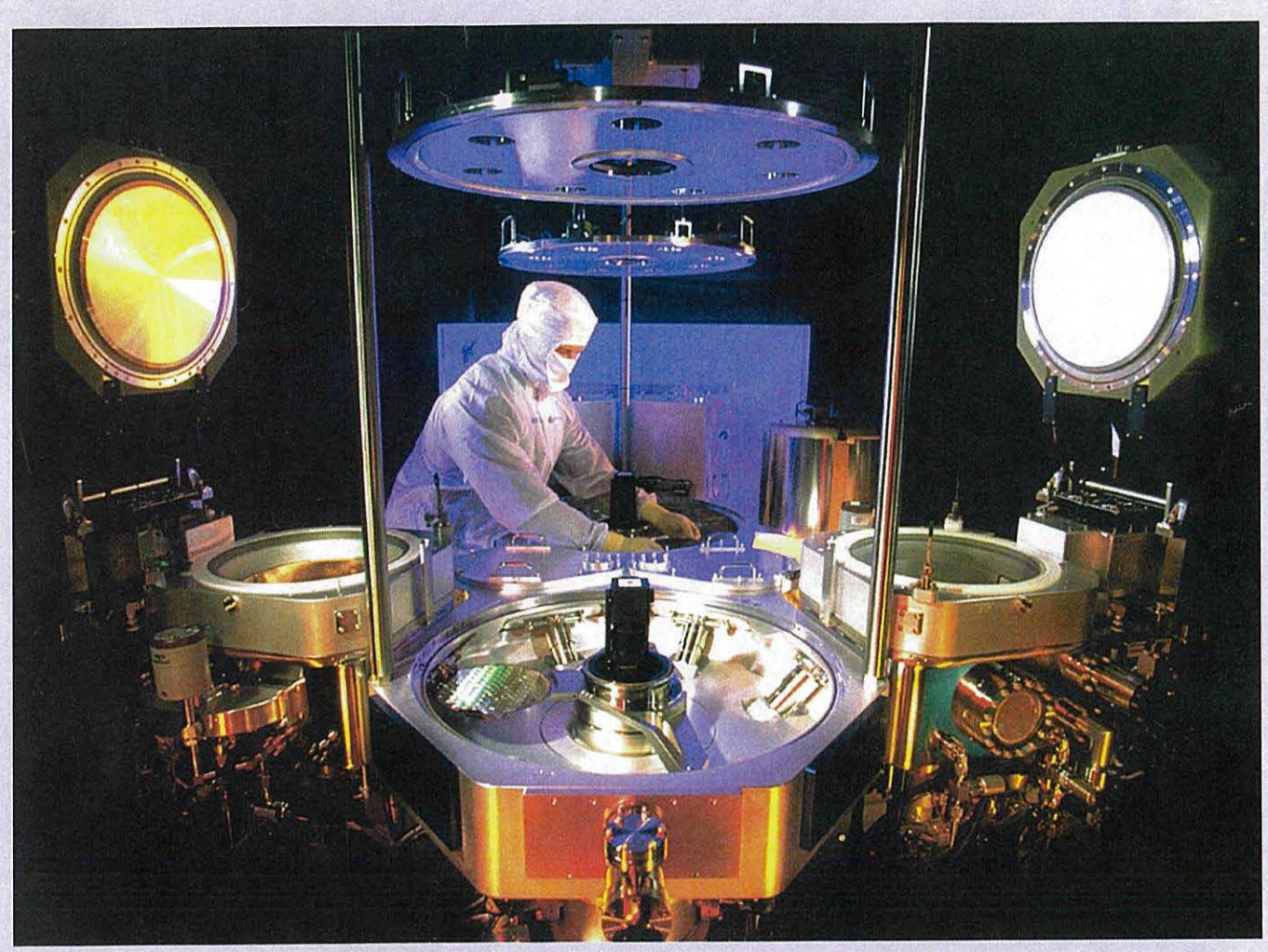
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Technician servicing a sputtering tool. Photograph courtesy of Applied Materials, Inc.

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Stanley Wolf Ph.D.

LATTICE PRESS
Sunset Beach, California

SAMSUNG EX. 1018 - 4/67

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Published by:

LATTICE PRESS
Post Office Box 340
Sunset Beach, California 90742, U.S.A.
http://www.latticepress.com

Cover design by: LATTICE PRESS Graphic Arts Department
Cover image: Lam's 2300 Excelan® dielectric etch system, shown against a SEM taken following an in-situ photoresist strip and dual-damascene etch. Courtesy of Lam Research Corporation.

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Library of Congress Cataloging in Publication Data
Wolf, Stanley, 1943 -

MICROCHIP MANUFACTURING

Includes Bibliographical references and Index
1. Integrated circuits - Very large scale
integration - Design and construction. 2. Silicon.
3. Metal-oxide semiconductors. 4. Silicon technology. I. Title

ISBN 0-9616721-8-8

Printed in the United States of America

Printing (last digit): 9 8 7 6 5 4 3 2 1

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PREFACE

Microchip Manufacturing is written for a wider audience than our previous books. The four-volume series *Silicon Processing for the VLSI Era* has long been popular among process engineers working in the field, and with students training for carrers in microelectronics. However, for readers studying the topic for the first time (or those not needing such in-depth information), these books may have been too daunting.

Thus, we set out to write a book that provides a more introductory and accessible treatment of this vital and fascinating technology. The chief innovation that makes the material easier to grasp is the use of *color illustrations* throughout. In fact, to our knowledge, it is the *first full-color technician/engineering-level textbook* ever produced on IC-fabrication technology.

The book also conveniently serves semester-long classes on IC fabrication in two academic curricula:

1. Introductory courses in undergraduate, four-year engineering programs of electrical, chemical, and mechanical engineering, materials science, and physics. The mathematical underpinning for such courses is provided in the Appendices. At least half the problems at the end of each chapter have been selected with such courses in mind.
2. As a basic book for two-year technician-training programs. Without referring to the Appendices, the remainder of the material contains only the level of mathematics that can be handled by students enrolled in a two-year Semiconductor Manufacturing Technology program.

Figures from the text (on CD), and a Solution Manual for the problems, are available to all adopting faculty.

The text should also appeal to many semiconductor-industry professionals, especially those peripherally involved with wafer-fabs. If you sell equipment, materials, and services to semiconductor manufacturers, it provides an understanding of the overall picture, and how your products fit in. IC designers, product engineers, test and field-service engineers, IP-lawyers, quality-control and reliability personnel, and sales and marketing workers will all benefit from its contents.

Many people helped make the publication of this book possible, and we thank and acknowledge their assistance here. First, several faculty members of the Digital Arts Department at Golden West College taught me the graphic-design programs needed to produce this book. Foremost among them was Sean Glumace, who was also an invaluable consultant when production-problems arose. Various companies (and people within) provided many of the beautiful photographs. They included: Chris Moran, Fred Helmrich, and Patricia Quon at Applied Materials; Shawn Lynch at Lam Research; Bob Klimo and Page Jasienski at Novellus Systems; Maureen Hart and Dan Ferrin at Axcelis Technologies; Chuck Gwynn at Intel Corp; and T.C. Smith (formerly of Motorola). Other individuals read parts of the manuscript and gave insightful feedback, including David Hata and Joseph McGuire. Special thanks goes to Jerry Healey, who offered significant technical help with computer issues, read several chapters, and afforded access to his technical archives. Helga Janssen sustained the backup-services that kept Lattice Press operating smoothly during the production-phase.

My family also delivered both direct and indirect assistance. My son, Ross, served as a hardware and software troubleshooter many times in a pinch. My daughter Jennifer gave marketing advice and an enthusiastic ear when spirits were low. My wife, Carrol Ann, not only helped prepare many of the graphic illustrations, proof-read many chapters, and typed the Index, but also took on the burden of handling the household administration, as I toiled over the manuscript. Without all of the above contributions, the book could not have been completed.

Stanley Wolf Ph.D.

P.S. Additional copies of this book (as well as copies of any of the volumes of the series - *SILICON PROCESSING FOR THE VLSI ERA*), can be ordered directly from the LATTICE PRESS website:

www.latticepress.com

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CHAPTER 2

SEMICONDUCTORS AND BASIC MATERIALS SCIENCE

CHAPTER CONTENTS

2.1 INTRODUCING SEMICONDUCTORS

2.2 THE NATURE OF MATTER: ATOMIC STRUCTURE

2.3 MOLECULES & COMPOUNDS

2.4 SOLIDS, LIQUIDS, AND GASES

2.5 CLASSIFYING MATERIALS BY THEIR ELECTRICAL PROPERTIES

2.6 SEMICONDUCTOR SILICON

2.7 OTHER SEMICONDUCTORS

"According to the theory of aero-lynamics, and as may be readily dem-nstrated through experiments, the Bumble Bee is unable to fly.

This is because the size, the weight, nd the shape of his body in relation o his wingspread make flying impos-ible."

BUT, the Bumble Bee, being igno-ant of these scientific truths goes head and flys anyway - and makes a ittle honey every day!"

Author Unknown

A wafer-transport carrier provides wafer protection, enabling greater fab productiv-ity. Photo courtesy of Entegris Inc.

Silicon is the most important semiconductor-material in use today. Electronic-devices in integrated-circuits are built on silicon wafers because silicon has a unique set of properties that make it best suited for making such devices.

In this chapter the basics of atomic-structure are first presented. This becomes the foundation for explaining the properties of silicon (and how it becomes possible to use it to build semiconductor-devices). This background information enables readers to better understand the details of the different steps used throughout wafer-fabrication.

2.1 INTRODUCING SEMICONDUCTORS

The integrated-circuits of so many of today's electronic-products are based on such semiconductor materials as silicon, gallium-arsenide, gallium-phosphide, etc. The unique physical and electrical properties of semiconductor-materials permits fabrication of such ICs. Thus, it is useful to introduce the fundamentals of semi conductors here. However, this subject rests on an understanding of the structure and bonding of atoms. Thus, both subjects make up the contents of this chapter.

2.2 THE NATURE OF MATTER: ATOMIC-STRUCTURE

The properties of semiconductor materials are based on the *structure of the atom.* All matter in the universe is made from approximately 100 materials known as *elements*. Each element has its own atomic-structure, and this uniqueness gives rise to the different properties of the elements.

An *atom* is the smallest object of matter that still retains the unique characteristics of each element. As an example, consider the element *gold,* whose properties include having a bright yellow-color and high electrical-conductivity; and being a soft, heavy metal. If a piece of gold is broken into smaller and smaller fragments, eventually an object is reached – a *gold-atom* - that still has the properties of gold. The gold-

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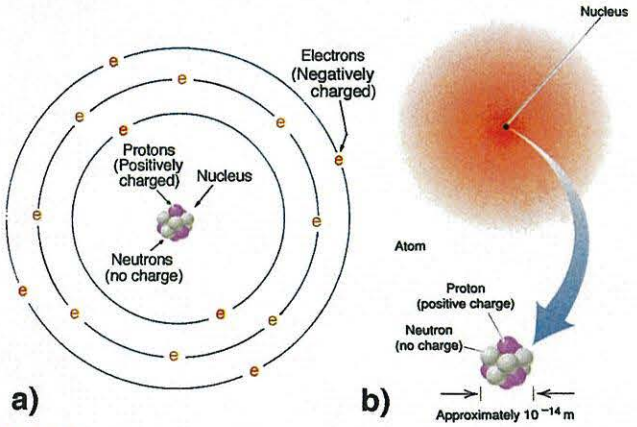


Fig. 2-1 (a) Schematic drawing of Bohr's model of the structure of the atom. (b) Illustration of the Quantum Mechanical model of the structure of the atom.

atoms themselves (as well as all other atoms) consist of *subatomic-particles* – protons, electrons, and neutrons. Each of these subatomic-particles also have their own properties. But, it is only when they are assembled together in a particular combination and configuration (an atom) that they form gold (or some other element).

2.2.1 The Structure of the Atom

The structure of atoms has only been understood since the beginning of the 20th century. The model of the atom proposed by Bohr in about 1920 was the first one that correctly explained the most important aspects of atomic-structure (Fig. 2-1a). While the model of the atom based on Quantum Mechanics (introduced in the 1930's) is even more correct (and its depiction of how electrons surround the nucleus is shown in Fig. 2-1b), Bohr's model of the atom is suitable for our level of discussion, and it is the one we will use for our discussions of atoms and the bonding that occurs among atoms.

Bohr's model says that protons and neutrons (which are 2000 times more massive than electrons) exist at the center of the atom, in the *nucleus*. The electrons, being much lighter, exist in stable orbits around the nucleus, somewhat like the planets that orbit the sun. Electrons and protons are also electrically-charged-particles. Protons have a positive-charge and electrons a negative-charge, but of equal magnitude. Since positive and negative charges attract one another, this force of electrical-attraction maintains the stability of the atomic-structure. Thus, in a neutral-atom, there are equal numbers of electrons and protons. For example, the simplest atom (*hydrogen*) has one of each.

Every element has a specific and unique number of protons. For instance, all helium (He) atoms have exactly two protons, while all oxygen (O) atoms have exactly eight. The number of protons in an atom is called its *atomic-number.*

The electron-orbits of an atom are called *shells,* and each shell can only contain up to a specific maximum number of electrons. For example, the first *atomic-shell* can contain up to only 2 electrons, while the second only up to 8. Once a shell is filled, addi-

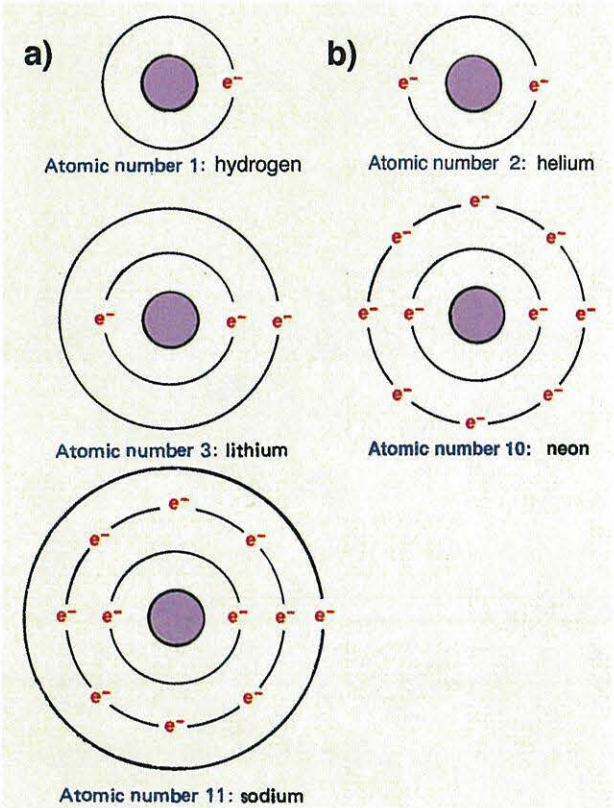


Fig. 2-2 The electronic structure of several atoms: (a) Left column – hydrogen, lithium, and sodium. (b) Right column – helium and neon.

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tional electrons must go into the next one. This means that *hydrogen* (atomic-number = 1) has one electron in the first-shell, and *helium* (atomic-number = 2) has two. But, in *lithium* (atomic-number = 3), the third electron must occupy a place in the second shell (see Fig. 2-2). Likewise, in *neon* (with an atomic-number = 10), the second-shell has eight electrons, but in sodium (whose atomic-number = 11), the 11^{th} electron must take a place in the third-shell (Fig. 2-2). The *outermost shell* is called the *valence-shell.*

Another useful fact to note is that hydrogen, lithium, and sodium have a common property - namely that each atom has only one-electron in its valence-shell. This illustrates another aspect of atoms, namely that elements with the same number of valence-shell-electrons have similar properties. This also implies that the electrons in the valence-shell generally have the most influence on the physical, chemical, and electrical-properties of an element. Thus, it is no accident that the three best electrical-conductors (copper, silver, and gold) have the same number of valence-shell-electrons.

2.2.2 The Periodic Table

The *Periodic Table* is a catalog of all of the elements, from the simplest to the most complex (Fig. 2-3). Each *element-box* of the Periodic Table provides information about the element. First, it identifies the element by an abbreviation of one or two letters, known as the *atomic-symbol.* (For instance, the atomic-symbol for hydrogen is H, and that for lithium is Li.) In the upper-left corner is the atomic-number (the number of protons), and at the bottom is the mass (see Fig. 2-4), given in *atomic-mass-units* (or *amu*). For example, oxygen has an atomic-number of 8, and an atomic-mass of ~16 (amu = 15.99), indicating that oxygen has 8 neutrons (as well as 8 protons) in its nucleus.

We are most interested in that part of the Table

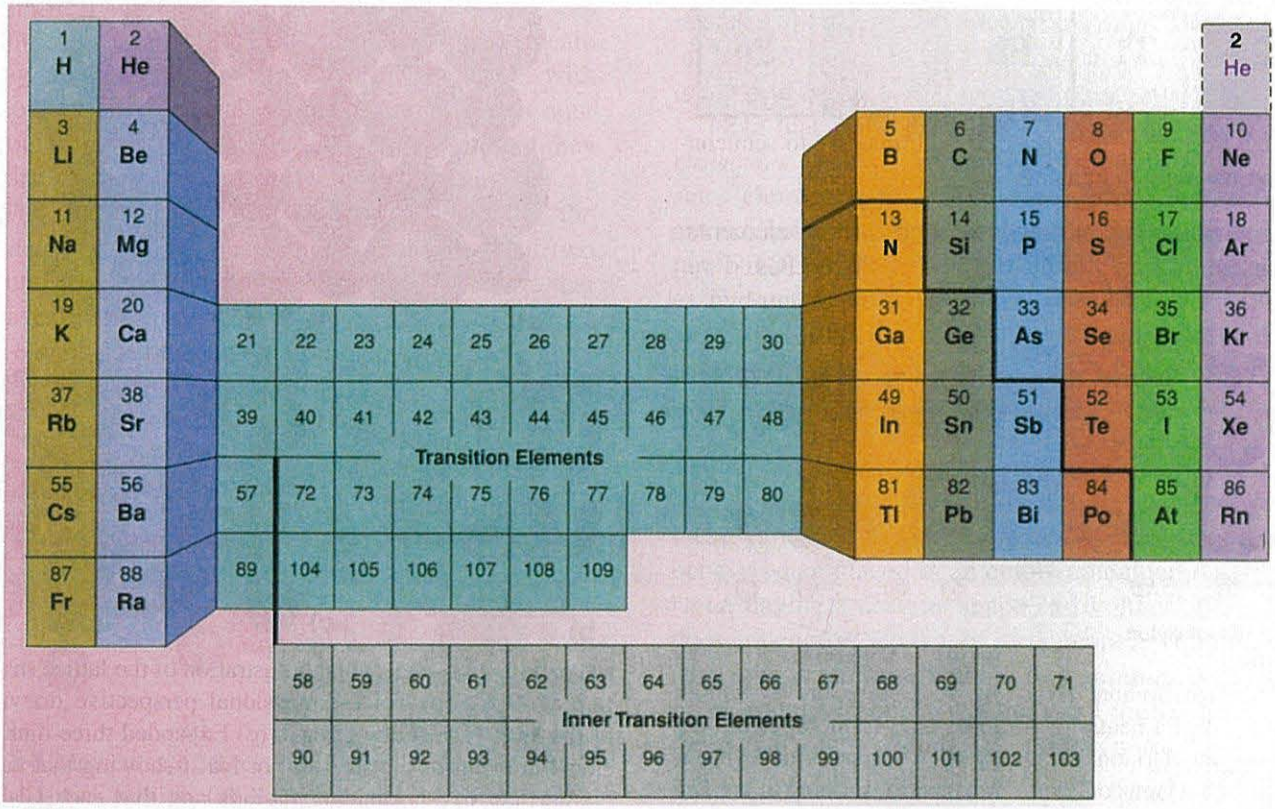


Fig. 2-3 The complete Periodic Table.

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	III A	IV A	V A	VI A
	5 B 10.81	6 C 12.01	7 N 14.01	8 O 16.00
II B	13 Al 26.98	14 Si 28.09	15 P 30.97	16 S 32.06
30 Zn 65.39	31 Ga 69.72	32 Ge 72.59	33 As 74.92	34 Se 78.96
48 Cd 112.4	49 In 114.8	50 Sn 118.7	51 Sb 121.8	52 Te 127.6
80 Hg 200.6	81 Tl 204.4	82 Pb 207.2	83 Bi 209.0	84 Po 209

Fig. 2-4 Portion of the Periodic Table relevant to semiconductor materials and doping.

shown in Fig. 2-4, since this contains those elements most widely found in the devices of silicon ICs.

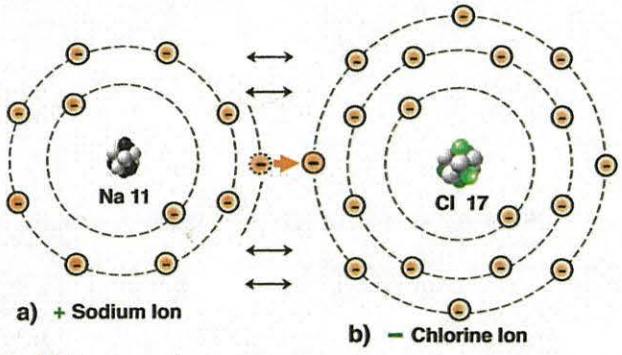


Fig. 2-5 (a) Sodium (Na) ion. A *positive* or "+" ion is formed when a neutral-atom loses one (or more) electrons. (b) Chlorine (Cl) ion. A *negative* or "-" ion is formed when a neutral-atom gains one (or more) electrons. Being of unlike-charge, the Na^+ and Cl^- ions attract one another.

Ions: An ion is formed when a (neutral) atom gains or loses one or more electrons. A neutral-atom becomes positively-charged when it loses an electron (forming a *positive-ion*), and negatively-charged when it gains one (forming a *negative-ion*). Ions with opposite charge attract one another, and this can lead to the formation of a chemical-bond, which results in an ionic-compound (see Sect. 2.4.4). As an example, sodium-atoms (Na) have a tendency to form positive-ions, since their lone valence-electron is easily lost (Fig. 2-5a). On the other hand, chlorine-atoms (Cl) are more likely to become negative-ions, as they tend to accept an extra electron to complete the filling of their valence-shell (Fig. 2-5b). Such Na^+ and Cl^- ions in close proximity will attract one another and arrange themselves in an ionic-compound NaCl (the common substance, *table-salt,* Fig. 2-6).

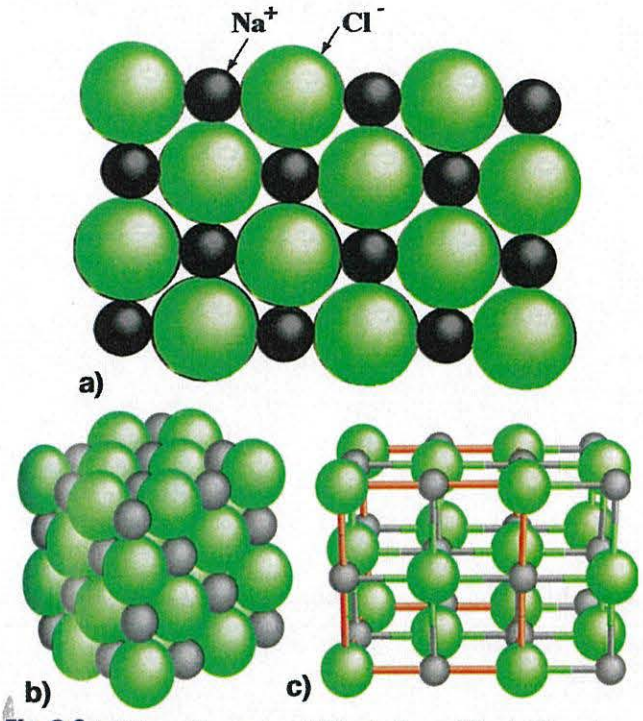


Fig. 2-6 (a) Two-dimensional illustration of the lattice structure of NaCl. (b) Three-dimensional perspective drawing of the lattice structure of NaCl. (c) Expanded three-dimensional drawing of the structure of NaCl showing that each Na-ion has six surrounding Cl-ions and that each Cl-ion likewise has six surrounding Na-ions.

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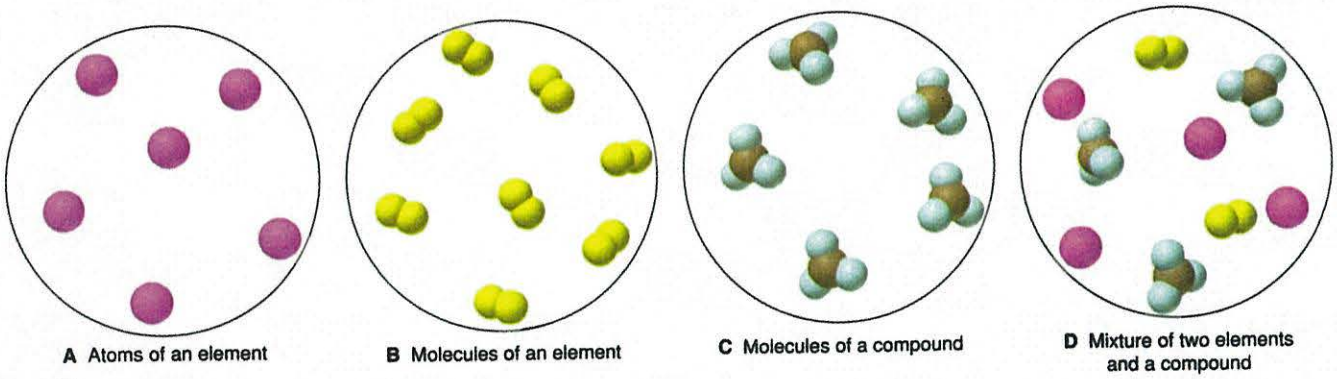


Fig. 2-7 (a) An *element* consists of identical atoms, but only some elements occur as individual atoms. (b) Some elements occur instead as molecules. (c) A *molecule* of a compound consists of a characteristic-number of atoms of two or more elements, chemically-bound together. (d) A *mixture* contains the individual units of two or more elements and/or compounds that are physically intermixed.

2.3 MOLECULES AND COMPOUNDS

Substances formed from a single one of the 100 element contain only one type of atom. These are the simplest materials that have unique physical and chemical properties (Fig. 2-7a). However, there are many more than 100 substances in existence, with the others being non-elemental materials. Such non-elemental substances are called *compounds*, and they consist of combinations of two or more elements.

The basic-unit of a *compound-material* is the *molecule*. Molecules are objects that consist of two or more atoms, chemically-bonded in a structure that behaves as an independent-unit (Figs. 2-7b and c). For example, consider the non-elemental-compound, *water*. The basic-unit of matter that retains the properties of water is a molecule consisting of one oxygen-atom and two hydrogen-atoms (Fig. 2-8b). The multiplicity of materials comes from the ability of atoms to bond together to form molecules.

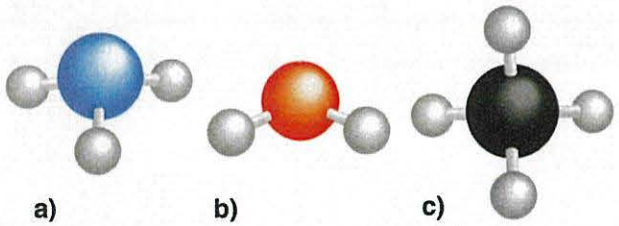


Fig. 2-8 Molecules of three familiar substances, drawn in ball-and-stick fashion. (a) Ammonia, NH_3. (b) Water, H_2O. (c) Methane, CH_4.

Although pictorial diagrams are used to depict particular molecules (Fig. 2-8), the more common way they are represented is with a *molecular-formula*. For instance, the molecular-formula of *water* is the familiar H_2O. Molecular-formulas indicate exactly the elements and their number in a compound material.

Note that some elements combine into *diatomic-molecules* (that is, composed of two atoms of the same element, Fig. 2-7b). These diatomic-molecules are examples of substances having a molecular-structure but are not compounds. The familiar process-gases hydrogen, nitrogen, and oxygen, in their natural state, are composed of diatomic-molecules, with molecular-formulas being H_2, N_2, and O_2, respectively.

2.4 SOLIDS, LIQUIDS, AND GASES

Matter can exist in three states: *solid*, *liquid*, or *gas* (Fig. 2-9). A clear distinction can be made between these various states on the basis of how substances behave when placed in an empty container. A *solid* is *rigid*, having a definite shape and volume. Its shape does not conform to that of its container. A *liquid* substance has a definite volume that assumes the shape of its container, but it will only fill the container to the extent of its volume. A *gas* occupies the entire space available to it, and its shape *and* volume are determined by its container. Most substances can

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exist in any of these three states, depending on the temperature, T, and pressure, *P*. For instance, water at atmospheric-pressure undergoes a change of state (from solid to liquid) at 0°C, and then turns from liquid to gas at 100°C. Most substances behave in a similar manner, although they change states at other specific values of T and *P*.

This book primarily describes the fabrication of electronic-devices built in *solid* materials (i.e., those in which electron-flow is controlled in semiconductors - the so-called *solid-state electronic-devices*). Examples of such devices include *pn*-diodes, bipolar-transistors, MOSFETs, ICs made on silicon-substrates (chips), and light-emitting diodes (LEDs). However, IC-fabrication also uses *liquid* chemicals and *gases*. Thus, knowledge about the materials science of all three states of matter is needed.

Units of Energy: Energy is transferred among substances during the various IC-fabrication-processes. It is important to understand the units of energy used when describing the events occurring in each process-step. The SI-unit of energy is the *joule* (*J*), which is defined (in an electrical-context), as the amount of energy required to move *one-coulomb* (*C*) of *electric-charge* through *one-volt (V)* of *potential-difference*.

However, *one-coulomb* of electric-charge corresponds to the charge on 6.2×10^{18} electrons. Thus, when events on the atomic-scale are being described (i.e., one-atom or one-electron at a time), it would be more convenient if they were expressed in units of energy more appropriate to the scale of such events (i.e., in units that are much smaller than a *joule*).

Such a smaller unit of energy is the *electron-volt* (*eV*). It corresponds to the energy needed to move a single-electron (which has only *one-electronic-charge q*) through a potential-difference of one-volt. Since *one-electronic-charge* = 1.6×10^{-19} C, then:

$$1 \text{ eV} = 1.6 \times 10^{-19} \text{ C} \cdot 1\text{V} = 1.6 \times 10^{-19} \text{ J} \qquad \textbf{(2.1)}$$

The electron-volt is used to describe the energy levels of electrons in atoms and the energies involved in various processes (e.g., the bombardment-energy of ions in etching-processes, the energy of ion-beams in ion-implantation-processes, and the energy of electron-beams in scanning-electron-microscopes).

2.5 CLASSIFYING MATERIALS BY THEIR ELECTRICAL-PROPERTIES

Electricity was introduced in Chap. 1. Here we add some important supplementary information with respect to the electrical-properties of solids. This is required for the topic of semiconductor-manufacturing, because the devices that are fabricated rely on all aspects of the electrical-conductivity of matter.

Solids can be categorized with respect to their ability to conduct electricity (i.e., to support an electrical current-flow), into three groups: **1**) conductors; **2**) insulators; and **3**) semiconductors.

2.5.1 Electrical-Conductors and Resistivity

Materials are classified as being *conductors* if large electrical-currents can easily be established in them by the application of an electric-field. A material is a good conductor only if a large number of electrons easily flow in it as electric-current. This circumstance occurs if the protons of the nucleus maintain a weak hold on the valence-electrons of an element. This condition exists in most metals (although other materials can also exhibit good electrical-conductivity).

The property that quantifies the degree to which a material is a good conductor is called its *conductivity* σ. The reciprocal of the conductivity is its *resistivity* $\rho = 1/\sigma$. The lower the resistivity of a material, the better is its conducting ability. The units of ρ are ohm-centimeters (Ω-cm). For example, aluminum (a very-good conducting metal) has a very-low value of ρ ($\rho_{Al} = 2.7 \times 10^{-6}$ Ω-cm, or 2.7 $\mu\Omega$-cm). Note that ρ is strictly a property that depends on the material and not the geometry of the electrical-component made from it. Figure 2-10 shows the conductivity of a variety of materials.

The property of a component made from a specific material that includes the geometrical-form of the material (and its resistivity) is called its *resistance* (*R*), and the units of resistance are *ohms* (Ω). The value of *R* of a resistor made of a specific material and

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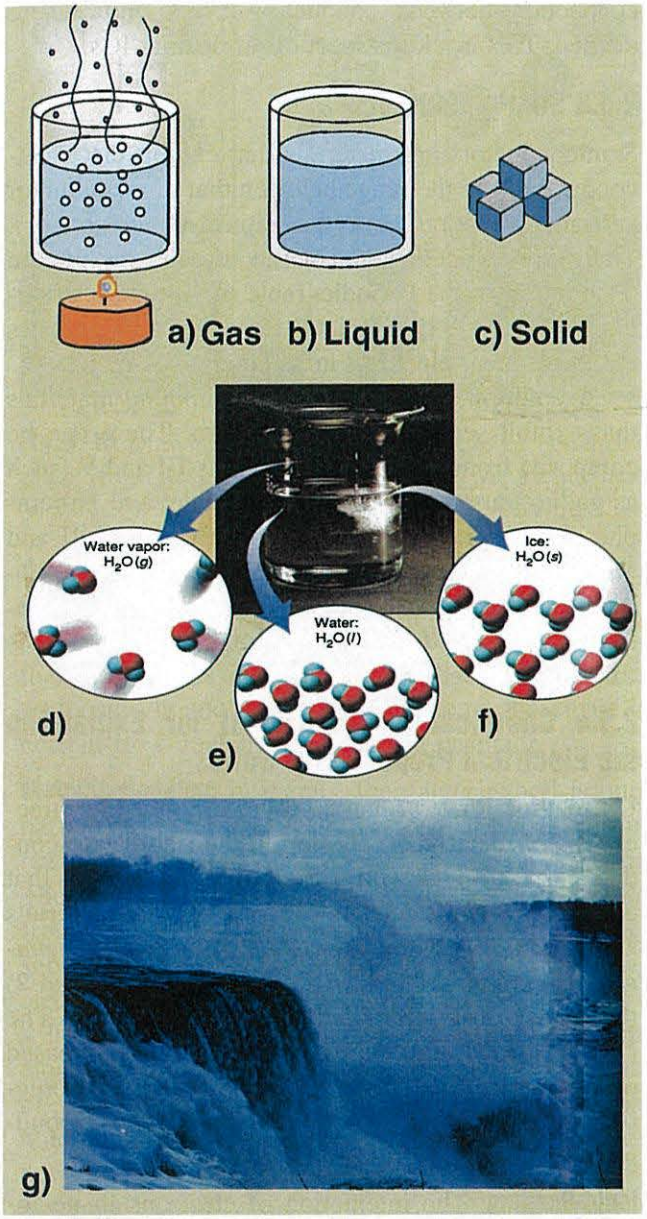


Fig. 2-9 Matter can exist in three states: (a) gas; (b) liquid; and (c) solid. For example, water can take three physical states: (d) water-vapor; (e) liquid water; or (f) ice. Despite the physical differences of water on the macroscopic level, all three states consist of the same individual H_2O molecules. (g) Niagara Falls in winter. Humid-wind, churning-water and rigid-ice display the power and beauty of the three states of water, co-existing at once.

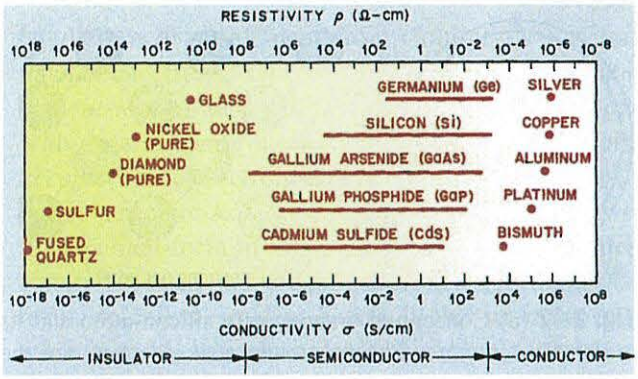


Fig. 2-10 Typical range of conductivities for insulators, semiconductors, and conductors.

having a particular geometrical-form is given by:

$$R\ (\Omega) = \rho\ l/A \qquad \textbf{(2.2)}$$

where l is the length of the resistor and A is the cross-sectional area (i.e., its width x thickness, see Fig. 2-11). The technology of fabricating the resistors used as circuit-components in integrated-circuits is described in Chap. 3. However, it should be noted here that the interconnect-wires in ICs are also made from thin-films of materials that have a low, but still finite, value of resistivity. As the feature-sizes of ICs get smaller, the resistance of these interconnect-wires (or *lines*) becomes a limiting-factor in the speed-performance of advanced ICs. The lower value of ρ of Cu (ρ_{Cu} = 1.7 $\mu\Omega$-cm) is the main reason why Cu-interconnects are replacing Al-interconnects in modern ICs (see Chap. 24).

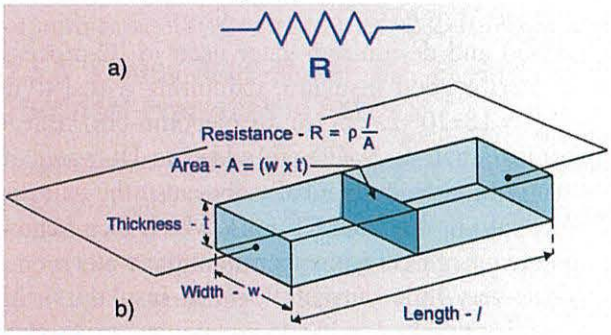


Fig. 2-11 (a) Circuit symbol of a *resistor*. (b) Relationship used to calculate the resistance of a circuit element from: (**1**) its physical dimensions (l, w, and t); and (**2**) the resistivity (ρ) of the material of which it is made.

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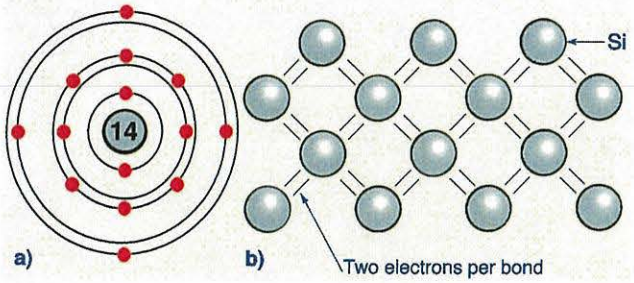


Fig. 2-12 (a) Conceptual drawing of a silicon-atom and its electronic structure. The four outermost electrons are the valence-electrons that participate in covalent-bonds. (b) A two-dimensional drawing of the covalent-bonding arrangement in a Si-lattice [i.e., viewed along a (100) direction].

2.5.2 Electrical-Insulators (Dielectrics)

Insulators (also called *dielectrics)* are materials at the other extreme of the conductivity-scale from metals and other conductors. In an insulator there are extremely-few mobile charge-carriers available to move in response to an applied electric-field. This is because the atoms of dielectric-materials hold their valence-electrons tightly, resulting in an absence of charge-transport (and thus, very-little current-flow).

Insulators therefore exhibit very-low conductivities (and very-high resistivities). For example, the resistivity of silicon-dioxide is $> 10^{18}$ Ω-cm - almost 24 orders-of-magnitude higher than the resistivity of aluminum! Other examples of insulators in everyday life are glass, rubber, plastics, and ceramics. Insulators used in IC-fabrication include silicon-dioxide and silicon-nitride.

Purified and de-ionized-water used in IC-processing is also a good insulator, exhibiting a resistivity $\rho_{DI\text{-}water} = 18x10^6$-Ω-cm (or 18 megohm-cm). But, if impurities (such as NaCl) are added to DI-water, its conductivity rises dramatically (because the salt dissociates into its Na^+ and Cl^- ions, which then behave as mobile charge-carrying species in the water).

Since very-little current flows in insulators, this property is exploited in ICs to isolate the various layers of conducting-interconnects. That is, thin-films of SiO_2 are deposited on the Si-substrate and between interconnect-layers. Openings are created to allow connection between conducting-layers only where desired. This is a key aspect of fabricating ICs.

2.5.3 Semiconductors

Semiconductors are materials that exhibit electrical-conductivity in the range between that of a conductor and an insulator (hence the name, *semiconductor*). There are two elemental-semiconductors, found in Column-IV of the Periodic-Table, *silicon* and *germanium.* Figure 2-12a depicts a Si-atom, and it shows that there are 4-electrons in its outermost-shell.

In addition, there are some compound-materials that exhibit semiconducting-behavior. These can be composed from elements of Columns-III and V (such as gallium-arsenide, gallium-phosphide, and indium-phosphide), or from elements from Columns-II and VI. Semiconductors display one set of electrical-properties when they are pure (*intrinsic*), but if they contain impurities (*dopants*), their electrical properties can be controlled by these dopants.

2.5.4 Chemical-Bonding-Model for Explaining the Electrical Properties of Solids

Up to this point we have only identified the three-classes of materials according to their ability to conduct current. In the next two sections, the models that account for such electrical-behavior in solid-materials are covered. There are two such models: **1**) the *chemical-bonding-model* (discussed in this section); and **2**) the *energy-band-model* (covered in Sect. 2.5.5). The chemical-bonding-model explains conductivity based on three-types of bonding found in solids: **a**) ionic-bonding; **b**) metallic-bonding; and **c**) covalent-bonding. Each type is described next.

Ionic-Bonding: The interaction of electrons in neighboring-atoms of a solid serves the important function of holding the solid together. As noted, at the end of Sect. 2.1, one type of such bonding is ionic-bonding, and the compound NaCl is held together in this way. As shown in Figs. 2-6b and c (and in Fig. 2-13a), each Na-ion is surrounded by 6 nearest-neighbor Cl^- ions, and vice-versa. That is, the positive Na^+-ions attract the negative Cl^--ions, and these coulombic-forces pull

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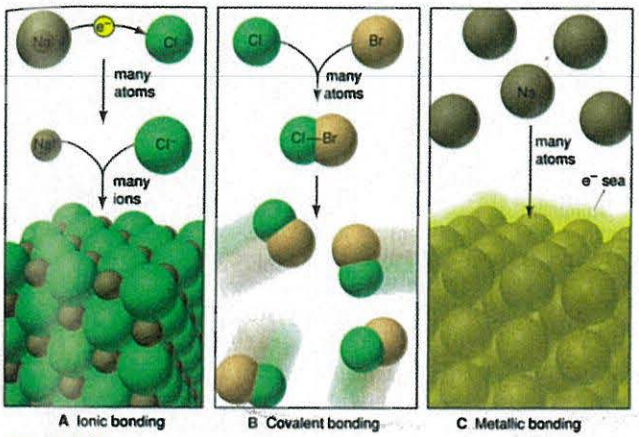


Fig. 2-13 Drawing showing the three types of bonding in solids (from the *chemical-bonding model* view): (a) Ionic-bonding. (b) Covalent-bonding. (c) Metallic-bonding.

the lattice together until the ions arrange themselves in a simple-cubic-lattice structure. An important consequence of this ionic-bonding in the NaCl-solid is that all electrons are tightly bound to atoms. There are no loosely-bound electrons available to participate in current-flow, making NaCl a good insulator.

Metallic-Bonding: In metals, the valence-shell is only partially filled, often with only one or two electrons (such as Na, which has only one valence-electron). These electrons in a metal can be easily removed from the valence-shell. In fact, in a pure metallic-substance, each metal-atom contributes a valence-electron to the crystal as a whole. Thus, the metal is a solid consisting of fixed (i.e., non-movable) ions with closed, completed outer-shells, immersed in a cloud of mobile-electrons (Fig. 2-13c). The forces that hold a metal-lattice together arise from an interaction between the *ionic-cores* and the *mobile-electrons*. This is termed *metallic-bonding*. In any case, the result is that in metals there are many mobile-electrons. These are free to move about the crystal when an electric-field is applied, giving rise to electric-current.

Covalent-Bonding: The third type of chemical-bonding is called *covalent-bonding*, and it occurs in elemental-solids formed of materials from Column-IV of the Periodic Table (C, Si, and Ge). That is, an isolated-atom of an element from Column-IV has four valence-electrons. Thus, each such atom is capable of *contributing* one valence-electron to form a bond with a neighboring-atom of the same type (and also *accepting* one electron for each such bond). Thus, a lattice-structure as shown in Fig. 2-13b (and in two-dimensional-form in Fig. 2-12b) can arise. The interaction between the electrons of neighboring-atoms forms so-called *covalent-bonds*. In this structure each atom (e.g., Si) has four nearest-neighbors, with whom a covalent-bond exists (and the structure is called a *diamond-lattice*, see also Chap. 9). Each electron-pair constitutes a covalent-bond. (Note that covalent-bonding also occurs in certain molecules, such as H_2.)

As occurs in the case of ionic-bonding, no mobile-electrons are available to the lattice in the covalent diamond-structure. From this argument, Si and Ge should be perfect-insulators. However, the situation shown in Fig. 2-12b strictly applies only to a Si (or Ge) lattice when it is at 0 K (i.e., at absolute-zero). But, if the lattice is at higher-temperature than 0 K (for instance, at room-temperature, 300 K), some of the covalent-bonds are broken by the thermal-energy of the lattice. This produces some mobile-electrons, which become available to participate in conduction. For the case of a pure-Si lattice at 300 K, there are only 10^{10} mobile-electrons/cm^3 created by such thermal bond-breaking (meaning that just *one in 10 trillion* electrons/cm^3 become available for conduction in pure-Si at room-temperature). Hence, the resistivity of pure-Si at 300 K is high ($\rho_{Si} = 2.2 \times 10^5$ Ω-cm).

2.5.5 Energy-Band-Model for Explaining the Electrical-Properties of Solids

While the *chemical-bonding-model* offers a simple way to introduce the concepts involving electrical-conductivity in solids, it does not provide insight about the energies involved in creating mobile-electrons (i.e., breaking covalent-bonds, etc.). On the other hand, the *energy-band-model* is capable of giving insight into the energies of such events, while still providing the same basis for conductivity-phenomena in solids as does the chemical-bonding-model. Thus,

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it is the more useful and more widely-employed model for describing conduction in solids.

The energy-band-model is based on the premise that when atoms bond-together to form a crystalline-solid, the energy-levels associated with their outer-orbits may (or may not) overlap as shown in Fig. 2-14. (This phenomenon arises from the Quantum Mechanical aspects of atomic-structure.) Since there are so many atoms in close-proximity in a solid, these energy-levels are so close together that they actually appear as *bands of energies* (as shown in Fig. 2-14 and 15). Diagrams like those of Figs. 2-14 and 15 are thus called *energy-band-diagrams*. The upper energy-bands are called *conduction-bands* and the lower energy-bands are called *valence-bands*. Electrons in a conduction-band (see Fig. 2-14c) can move freely in the solid (i.e., they are mobile-electrons), and can hence conduct current when an electric-field is applied. Electrons in the valence-band remain bonded to their respective atoms and are not capable of participating in electrical-conduction. Since the valence-band has a lower potential-energy, electrons tend to stay in it. Figure 2-16 shows the correlation between the *chemical-bonding* and *energy-band* models.

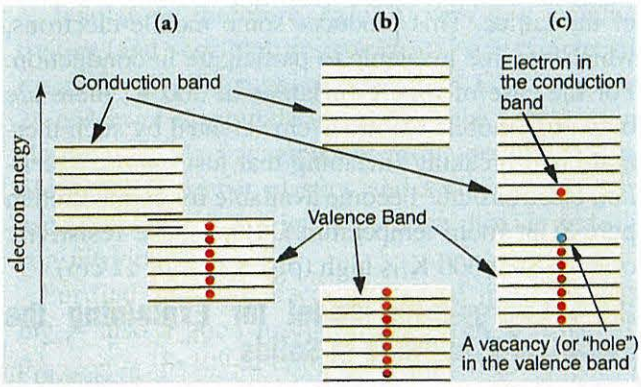


Fig. 2-14 Energy-levels in solids form bands of energies. These bands are depicted using *energy-band diagrams* as shown in this figure: (a) The valence-band and conduction-band overlap one another; (b) The valence-band and conduction-band are separated by a wide *energy-gap*, which prevents electrons from easily getting into the conduction-band. In this drawing, the conduction-band is empty; (c) The valence-band and conduction-band are separated by a smaller *energy-gap*, allowing electrons to more easily get excited into the conduction-band.

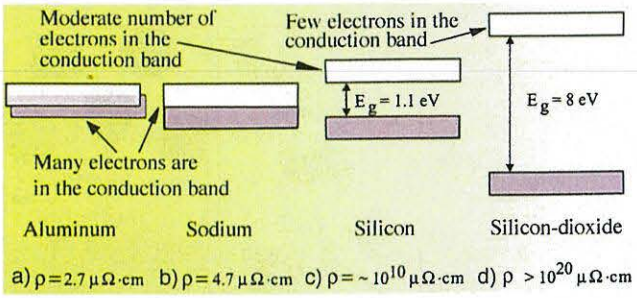


Fig. 2-15 This figure shows the energy-bands, the band-gap, and the resistivities (ρ) of: (a) Al; (b) Na; (c) Si; and (d) SiO_2. Note that the *band-gap* E_g of insulators (like SiO_2, or diamond) is wide, and thus there are few-electrons in the conduction-band (and ρ is very-high). In metals there is either no band-gap, or it is very small. Thus, many electrons are always in the conduction-band (and ρ is very-small). In semiconductors (like Si, Ge, or GaAs), the band-gap is smaller than in insulators. Thus, thermal-excitation of electrons into the conduction band is moderately easy, and this makes ρ in-between the values of a metal and insulator.

Note that there can be a separation (or *energy-gap*, E_g) between the two bands. In fact, the upper-edge of the valence-band is denoted in the energy-band diagram as E_v, and the lower edge of the conduction-band as E_c. Their difference is the energy-gap, E_g ($E_g = E_c - E_v$).

However, in *metals* there is either no energy-gap between these bands, or the valence-band and conduction-band may even overlap (Figs. 2-15a and 2-15b). In either case, the thermal-energy of the lattice can easily cause electrons to move from the valence-band up into the conduction-band. Thus, at 300 K the conduction-band of metals has many mobile-electrons, and a large current can flow, even when only a very-small electric-field is applied.

In the case of *insulators* and *semiconductors*, a finite energy-gap exists between the valence-band and conduction-bands (also referred to as the *forbidden-gap*). In these materials, an electron in the valence-band must receive enough energy from some source (e.g., thermal or optical) to allow it to jump-up into the conduction-band. The larger the energy-gap, the fewer the number of electrons that will be able to be

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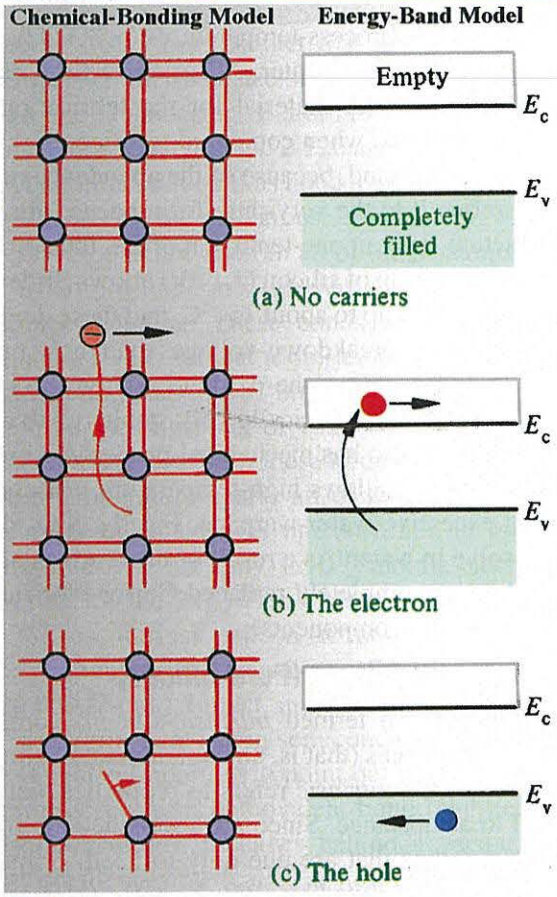


Fig. 2-16 Correlation between the *chemical-bonding model* (CB) and the *energy-band model* (EB) with respect to electrical-conduction. (a) *All bonds are intact* (CB), or *there are no electrons in the conduction-band* (EB). In either case, there are no carriers, so no current-flow is possible. (b) Electrons become available to carry current either by *breaking a bond to become "free"* (CB) or by *getting excited into the conduction-band to become "free."* (EB). (c) Holes can carry current by *making a vacancy among the bonds* (CB) - to allow other electrons to rearrange themselves - or by *the creation of a vacancy in the energy-levels of the valence-band* (EB).

excited into the conduction-band of that material.

For *insulators*, such as glass or plastic, the energy-gap is so wide ($E_{g_{SiO_2}}$ = 8-eV, see Fig. 2-15d), that very-few electrons end-up being excited into its conduction-band. Thus, very-little current can flow in insulators. Note that photons of visible-light have energies in the range of 1.8-2.8-eV. Thus, when they pass through a diamond (which is an insulator whose E_g = 5.0-eV), their energy is too-small to excite electrons into the conduction-band of the diamond. Thus, they pass through diamond without being absorbed. This is why diamonds are transparent.

For semiconductors, the energy-gap is smaller than in an insulator. For example, the energy-gaps are 1.1-eV in silicon, 0.66-eV in germanium, and 1.40-eV in gallium-arsenide (Fig. 2-15c). Since the energy-gap of silicon is smaller than the energy of visible-light photons, such photons have enough energy to excite electrons into the conduction-band of silicon. Thus, visible-light photons are absorbed as they pass through silicon, making silicon an opaque-material.

2.6 SEMICONDUCTOR SILICON

Silicon (Si) is presently the most important semiconductor-material for the electronics-industry, with VLSI and ULSI technology being based almost entirely on this substance. Silicon is the second-most-abundant element (after oxygen), making up about 25% of the earth's crust. Its atomic-number is 14, and it is found in Column-IV of the Periodic Table. Silicon has a high melting-point (1420°C). It is opaque (with a silvery-gray color), and is a hard and brittle material that fractures easily.

A key-fact to remember is that there are about $5x10^{22}$ atoms/cm^3 in single-crystal-silicon (Fig. 2-17). This number is important because it gives a benchmark for comparison when dealing with the concentration of impurity-dopants in silicon. The parameter-values of some of the other most useful properties of silicon are given on the endsheet.

Solid-state-electronics was launched with the invention of the bipolar-transistor in 1947. Germanium (Ge) was the first semiconductor-material used to make transistors, but it was largely replaced by silicon for the following reasons: The narrow-bandgap (0.66-eV) limits the operation of Ge-devices to temperatures below 100°C. (Ge also melts at the relatively-low-temperature of 937°C.) In addition, IC planar-processing needs a layer on

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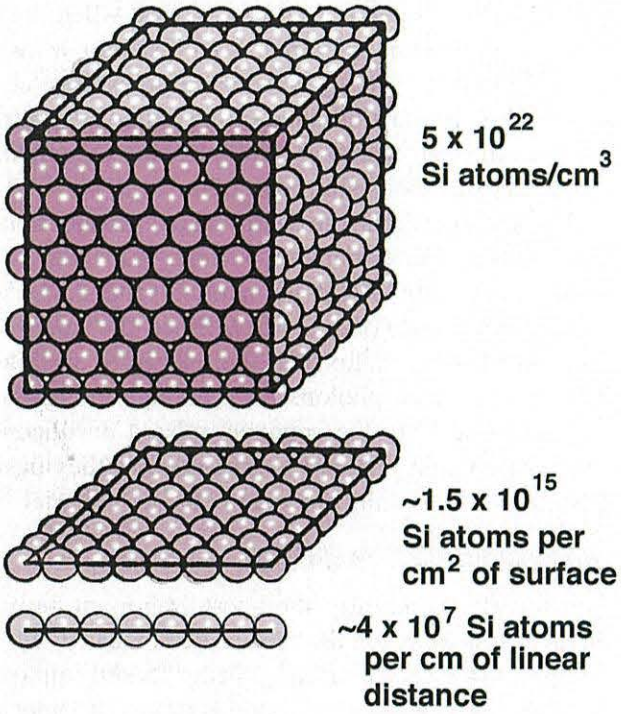


Fig. 2-17 Drawing showing the number of atoms contained in one cubic-centimeter of solid-silicon.

the semiconductor-surface that can serve as a good chemical-barrier (to protect the wafer-material from external-contaminants) and as a passivation-layer. While the oxide of germanium (GeO_2) could serve as such a layer, it has some severe limitations. First, it is unstable at high-process-temperatures (> 800°C), but worse, it dissolves in water. All of these limitations make Ge an inferior material for the fabrication of integrated-circuits, when compared to silicon.

On the other hand, because of the abundance of Si, cost to refine it to the very-pure-form needed for IC-manufacture is about one-tenth that of Ge. In addition, the larger-bandgap of silicon (1.1 eV) allows Si-devices to be operated up to about 150°C, and these devices also have higher breakdown-voltages than those made from Ge. Furthermore, the oxide of silicon, SiO_2, is easy to form and is chemically very-stable (up to over 1500°C). SiO_2 also has mechanical-properties similar to silicon, which allows high-temperature processing without excessive wafer-warpage. Finally, SiO_2 does not dissolve in water. As a result of these advantages, Si has almost completely replaced Ge for fabricating microelectronic components.

2.6.1 Intrinsic-Silicon (Pure-Silicon)

Pure-silicon (also termed *intrinsic-silicon*) contains no other substances (that is, no contaminants or impurities). The term *intrinsic* refers to properties that are natural to a substance. Since intrinsic-silicon is pure, it has properties that are due only to itself. Some of the properties exhibited by *impure-silicon* (also called *extrinsic* or *doped* silicon) can be due to the impurities it contains.

The semiconductor properties of intrinsic crystal-

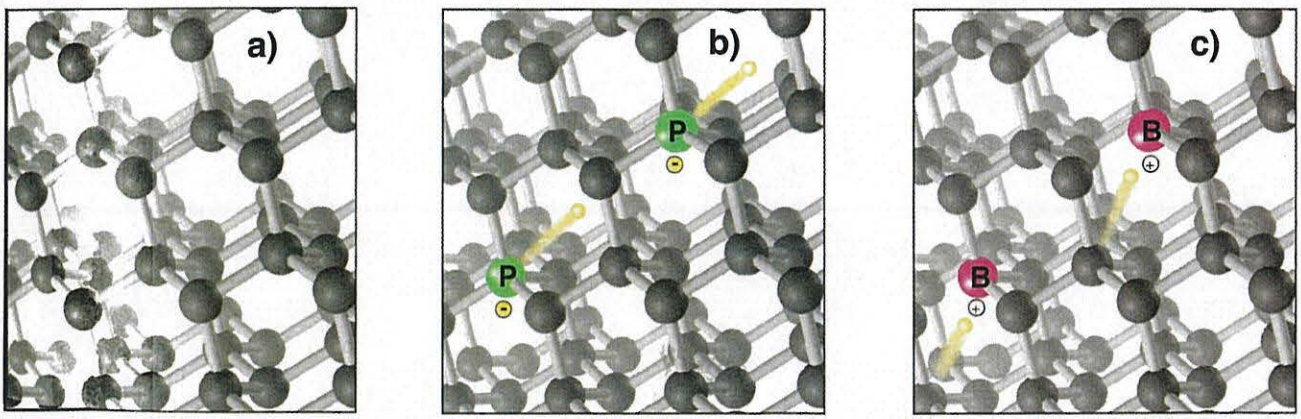


Fig. 2-18 (a) Illustration of a pure (intrinsic) Si-lattice, showing the covalent-bonds. (b) A Si-lattice doped with *phosphorus* (P) atoms, forming *n*-type Si. (c) A Si-lattice doped with boron (B) atoms, forming *p*-type Si.

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line-Si arise from the fact that its atoms have four electrons in their valence-shell. It shares each of them with one neighboring-Si-atom to form four covalent-bonds (as shown in Figs. 2-12b and 2-18a). The atoms in crystalline-silicon thus bond together through covalent-bonds to share electrons. This bonding also completes the valence-shell in all of the Si-atoms.

Many of silicon's properties arise from such covalent-bonding. These bonds are strong, making silicon a stable-solid at room-temperature. (They also hold Si together up to high-temperatures, giving it the high melting-point of 1420°C). It is also hard to remove electrons from these strong-bonds. In fact, at room-temperature nearly all of the Si-valence-shells are fully occupied. (As noted earlier, at room-temperature, there are only $1x10^{10}$ mobile-electrons per cm^3 out of the $2x10^{23}$ valence-electrons per cm^3 in Si.) Thus, intrinsic-silicon at room-temperature is a poor-conductor (it's resistivity is high, with a value of 220,000 Ω-cm.). In fact, in its intrinsic-form, Si is not of much practical use in semiconductor-technology.

It is also important to point out that when an electron escapes from its covalent-bond (and becomes a mobile-electron), it leaves behind a vacant spot in that covalent-bond (called a *hole*, Fig. 2-19). Thus, intrinsic-silicon contains an *equal number* of mobile-electrons and holes (that is, neither mobile-electrons nor holes are in the majority).

2.6.2 Extrinsic-Silicon (Doped-Silicon)

The high-resistivity of intrinsic-silicon can be decreased by adding small quantities of certain other elements (*impurities*) through a process called *doping*. This process allows such *doped-silicon* to become suitable for fabricating semiconductor-devices. Even the presence of very-small quantities of such impurities can dramatically decrease the resistivity of intrinsic-silicon. For example, by adding only one dopant-atom (e.g., boron or phosphorus) for each million silicon-atoms, the resistivity will drop from 220,000 Ω-cm to 0.2 Ω-cm. This represents a decrease in the resistivity by a factor of over one-million! The more impurity-atoms that are added, the better the conductivity of the Si. As noted earlier, *doped-silicon* is also called *extrinsic* or *impure silicon*.

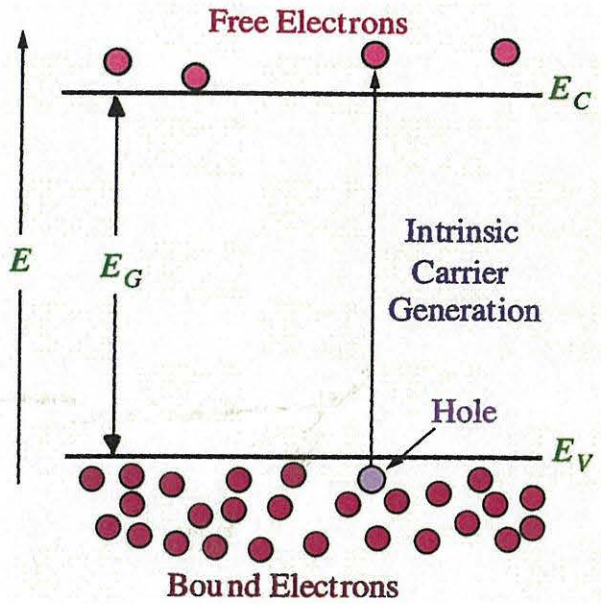


Fig. 2-19 Simple band-diagram representation of intrinsic (pure) silicon. The process of *intrinsic-carrier-generation* is also illustrated.

Doping of silicon (and other semiconductors) has another important benefit, namely that current can take place through the flow of either negative-charge (electron-movement), or positive-charge (i.e., through the flow of *holes* – a subject described in more detail in Sect. 2.6.5). The latter phenomenon is called *hole-flow*, and is unique to semiconductors. Thus, not only can silicon be doped into a much wider, useful resistivity-range (from 0.001-Ω-cm to 1000-Ω-cm), but by choosing the right *type* of dopant, it can be made either electron-rich (*n*-type), or hole-rich (*p*-type). The ability to create both *p*-type and *n*-type regions allows such devices as *pn*-diodes, bipolar-transistors, NMOSFETs and PMOSFETs to be built in silicon.

2.6.3 Dopants in Silicon (Donors and Acceptors)

As noted previously, Si is found in Column-IV of the Periodic Table, and thus has four valence-electrons. Elements from the two adjacent-Columns in the Periodic Table are commonly used for doping

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Si, namely those in Column-III and in Column-V. Elements in Column-III (for example boron, B) have three valence-electrons, while those in Column-V (for example, phosphorus P, or arsenic, As) have five.

When Column-III-dopants (e.g., boron) are added to Si, the material is called *p*-type-silicon, and *p*-type-dopants are called *acceptors* (as discussed in Sect. 2.6.5). When dopants from Column-V (e.g., P or As) are added to silicon, the material is called *n*-type-Si, and *n*-type-dopants are called *donors* (for reasons also described in Sect. 2.6.4). The energy-band-diagram of an *n*-type-dopant such as P, donating an electron to the conduction-band is shown in Fig. 2-20a.

2.6.4 *n*-Type Silicon

The addition of dopants from Column-V to silicon increases silicon's-conductivity for the following reason: Phosphorus (or arsenic) atoms in silicon can replace a Si-atom at a given lattice-site. However, such dopants have an extra-electron in their valence-shell, and these extra-electrons cannot participate in covalent-bonding. In addition, such extra-electrons are easily broken away from the P (or As) atom (see Fig. 2-18b and 2-20a) to become a *mobile-electron* (or *carrier*) - which then can contribute to current-flow. Such an electron is said to be *donated* to the silicon-material for the purpose of electrical-conduction. If $10^{15}/cm^3$ (or more) donors are added to the silicon, and each donates one mobile-electron, the number of donated-carriers will far exceed the number present in intrinsic-silicon at room-temperature ($10^{15}/cm^3 >> 10^{10}/cm^3$). In this way, the addition of even a small-percentage of *n*-type dopants dramatically increases the concentration of mobile-electrons (10^{15} dopant atoms/cm^3 represents about 1-dopant-atom per 10-million-silicon-atoms, or 0.0001%), and yet this vastly increases the conductivity of silicon.

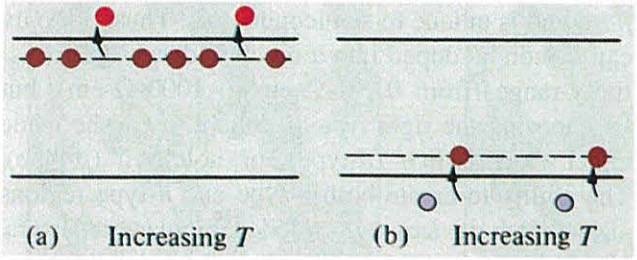


Fig. 2-20 Energy-band diagram of silicon that has donors and acceptors on lattice-sites. The energy-levels that these impurities produce are also shown in the diagram. The mechanisms of how mobile-electrons arise from the presence of donor-atoms and holes from the presence of acceptor-atoms in the lattice is also shown from the perspective of the energy-band model.

Electrons will be attracted to the positive-terminal of a battery that is connected to the silicon (Fig. 2-21a). Any *mobile-electrons* move in the direction toward the positive-terminal, and this organized-movement of charge-carriers creates an electron-current in the semiconductor. Note that since there are many more mobile-electrons created by the donor dopant-atoms in *n*-type-silicon than there are holes, the mobile-electrons are called the *majority-carriers* in *n*-type silicon. On the other hand, holes present in *n*-type-Si are called *minority-carriers*.

2.6.5 *p*-Type-Silicon (Holes)

The introduction of dopants from Column-III (*p*-type dopants) contributes to the conductivity of silicon in a somewhat more complex-manner than does the presence of *n*-type-dopants in Si. That is, boron-atoms can also replace Si-atoms on lattice-sites. However, B only has three electrons in its valence-shell. Thus, it can *accept* an electron from a neighboring silicon-covalent-bond (Fig. 2-18c and 2-20b). But this creates a vacancy in that bond (which, as we noted earlier, is called a *hole*). If a voltage is applied to *p*-type silicon (for example using a battery), an electron near the hole will be attracted toward the positive-terminal of the battery and will jump to fill the hole (Fig. 2-21b). However, this will leave the hole in the spot from which this electron jumped. It is seen that the hole moves continuously in the opposite-direction to that of electron-movement. When all is said and done, the hole will have moved to the edge of the semiconductor near the negative-terminal. For someone measuring current-flow in this circuit with just an ammeter, however, it appears that there is a current due to the movement of positive-charge carriers (the holes),

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while it is actually due to the sum of the electrons moving in the opposite-direction. Nevertheless, the apparent-current due to hole-movement can be treated just like another-component of the total-electric-current present in a semiconductor. An energy-band diagram of a *p*-type dopant (acceptor) accepting an electron from the valence-band, is shown in Fig. 2-20b.

The notion of treating the movement of vacancies in the valence-band of silicon (i.e., holes) as one form of electric-current may seem odd. However, there are other everyday-phenomena we routinely accept in the same spirit. For example, if a nearly-full bottle of shampoo is turned upside down, we say that a bubble inside the bottle rises to the top. In fact, what is occurring is that the shampoo is flowing down to the bottom. But it is easier to see this event as a rising bubble. Hole-movement in the silicon is much like the bubbles that rise in upside-down shampoo-bottles.

In any case, each B-atom causes the creation of a hole. If there are a substantial-number of B-atoms in a Si-lattice, this will produce a situation where the number of holes exceeds the number of intrinsic mobile-electrons. Thus, the current in *p*-type-semiconductors will be predominantly due to *hole-flow*. Furthermore, since there are many more valence-band-holes in *p*-type silicon than there are mobile-electrons, holes are the *majority-carriers* in *p*-type-silicon (and the mobile-electrons are the *minority-carriers)*.

2.6.6 Dependence of Resistivity on Doping-Concentration in Silicon

Metals have a resistivity (ρ) range limited to 10^{-4} to 10^{-6} Ω-cm (only a factor of 100). Given a specific metal, this means there is only one practical way to change the resistance of a device made from this metal to a greater-degree than allowed by the resistivity-range. For example, if a resistor was being designed, the physical-dimensions of the resistor would have be changed (according to Eq. 2-2) to allow a larger-resistance-value to be obtained.

On the other hand, semiconductor-materials allow a change in the value of the resistivity (through the addition of dopant) over a much wider-range (i.e., from 0.001-Ω-cm to 1000-Ω-cm – a factor of over 1,000,000). Thus, this allows much-greater flexibility in the design of resistors built in silicon than in metal. (It can also be seen that the higher the doping-concentration in Si, the lower the resistivity-value.)

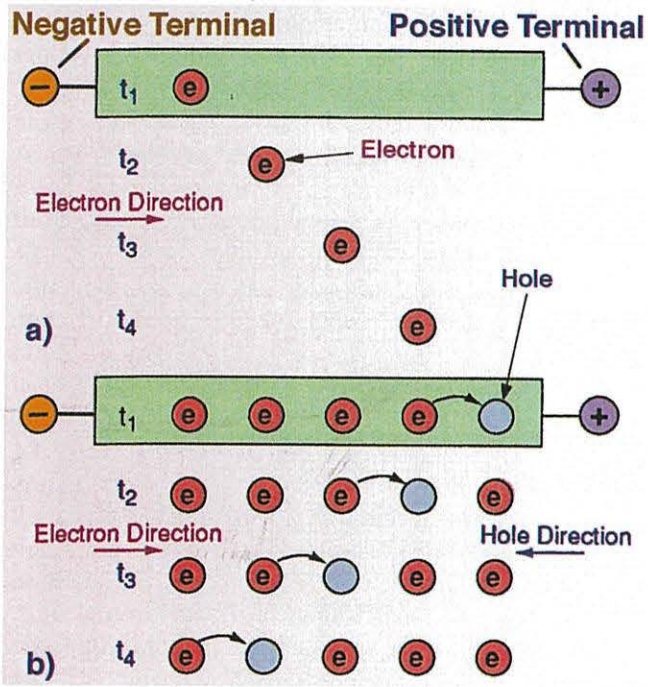


Fig. 2-21 (a) Conceptual drawing of current due to *electron-flow* in a semiconductor. Note that the electrons move toward the positive-terminal of the power-supply. (b) Conceptual drawing of current due to *hole-flow* in semiconductors. Holes move toward the negative-terminal, as electrons move toward the positive-terminal.

Figure 2-22 illustrates how the resistivity in silicon depends on the doping-level. The *y*-axis is labeled as the *dopant-concentration* (in units of #/cm^3). The *x*-axis gives the resistivity (in units of Ω-cm). Note that there are two curves in this figure: one for *n*-type-doping and the other for *p*-type. They show that for the same value of doping-concentration, *n*-type-doped-silicon has a lower resistivity than *p*-type. As discussed in the next section, this occurs because electrons (the dominant-carriers in *n*-type-silicon) move more rapidly than do holes (the dominant-carriers in *p*-type-silicon).

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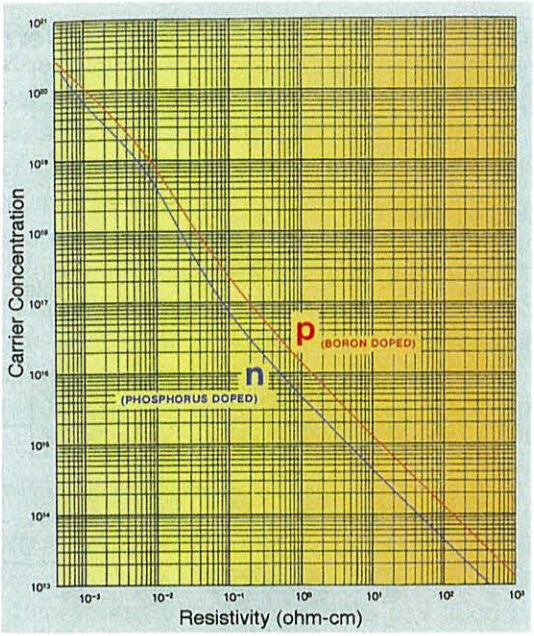


Fig. 2-22 Resistivity vs. doping for *n*- and *p*-type silicon.

The data in this figure also indicate that it takes the presence of only 0.000001% to 0.1% of a dopant to cause Si to have a useful-range of resistivity. Information in this figure is used to select the correct doping-concentration in Si to give the desired resistivity in a particular device-region. This amount of dopant is then carefully introduced into the silicon during the semiconductor-manufacturing process to achieve this precise-resistivity. The process-technologies used to introduce dopants into Si are *chemical-diffusion* (see Chap. 11), and *ion-implantation* (see Chap. 12).

2.6.7 Carrier-Mobility (and Its Impact on Transistor Performance)

We have shown that there are two-types of charge-carriers in a semiconductor: *electrons* and *holes*. Both holes and mobile-electrons are caused to move in silicon when acted on by an electric-field. For the same value of electric-field-strength, electrons travel more easily (and therefore more rapidly) through silicon than do holes. The speed of movement of a charge-carrier (either an electron or hole) for a given electric-field-strength is called the *carrier-mobility*, with holes having a lower-mobility than electrons in Si. This means that if the same number of electrons and holes are flowing in an identical electric-field, the electron-flow will produce the larger-component of electric-current. This effect is important in the selection and design of transistors. That is, it is the basis of why *npn*-bipolar-transistors are generally preferred over their *pnp*-counterparts, and why digital-logic-circuits built with NMOSFETs operate at higher clock-speeds than those built with PMOSFETs.

2.7 OTHER SEMICONDUCTOR MATERIALS

Silicon (Si) and germanium (Ge) are the two *elemental*-semiconductor-materials from Column-IV of the Periodic Table. It was noted that Si is the most widely-used material for making semiconductor-devices today, but it should also be mentioned that the first transistors were fabricated in 1947 using Ge. Germanium is still used in some specialty-semiconductor-devices, such as high-power *pn*-diodes.

The other types of semiconductor-materials are *compound-semiconductors*. They are materials consisting of two (or more) elements. The applications of devices using these alternative-semiconductor-materials are many, including optical-devices (LEDs, infrared-detectors, solar-cells, and semiconductor-lasers), high-frequency communications-chips (rf- and microwave-circuits for wireless-applications), and special high-power-devices. Although these devices are important, the total-sales each year for such alternative-semiconductor devices-still makes it a niche-market. That is they consist of only about 2% of the total-sales of semiconductor-devices (with the rest going to silicon-based devices).

The most-widely used alternative-semiconductors consist of materials from Columns III and V of the Periodic Table (the so-called III-V compounds, such as GaAs, GaP, and InP). GaAs is the most widely used alternative-semiconductor-material. It is primarily employed in high-frequency-devices in communications-systems. The high-mobility of electrons in GaAs allows such devices to operate at speeds about 3-times faster than comparable silicon-devices. This

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makes them suitable for such high-frequency operation. GaP (and GaAsP) is used to make light-emitting diodes (LEDs). GaN is used to make blue and white LEDs.

Other compound-semiconductors are II-VI -materials, such as CdSe, and ZnSe. These make up a small-market ($179 million in 2001). CdTe is used to make infrared-detectors, and ZnSe to make blue-LEDs.

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1. M. Silberberg, *Chemistry: The Molecular Nature of Matter and Change,* Mosby, St. Louis, 1996.

2. D. A. Neamen, *Semiconductor Physics and Devices, 3rd Ed.* McGraw-Hill, New York, 2003.

3. W.E. Beadle *et al., Quick Reference Manual for Silicon Integrated Circuit Technology,* Wiley, 1985.

PROBLEMS

1. Explain the electrical difference between a conductor, an insulator, and a semiconductor.

2. What is a *semiconductor*? List three of the most commonly used semiconductor materials.

3. Why is it necessary to dope silicon in order to build solid-state devices? How does the resistivity of a semiconductor change with dopant concentration?

4. Which substances have higher resistivities, metals or intrinsic semiconductors?

5. What is the majority carrier in *p*-type semiconductors? Name 2 elements that are *p*-type dopants in silicon.

6. Does a *p*-type semiconductor exhibit negative or positive current? Explain your answer.

7. Define the term *minority-carrier.* What carriers are the minority-carriers in *n*-type silicon?

8. At the same doping concentration-value, which has the higher electrical-conductivity, *n*-doped or *p*-doped silicon?

9. What is the distinction between the concentration N_D of an *n*-type impurity in a wafer, and the concentration *n* of majority carriers in the same wafer?

10. A 1-mm thick silicon wafer having a diameter of 20-cm contains 6.77 mg of boron ($_{11}B^5$), uniformly distributed in substitutional sites. Find: (a) the boron concentration, in atoms/cm^3, and (b) the average distance between boron-atoms.

11. Aluminum has an atomic density of 6.02×10^{22} atoms/cm^3. What is the mass-density (g/cm^3)? If the Al atoms are stacked uniformly in a cubic-array, how many atoms/cm^2 are in the top atomic-layer. What is the center-to-center spacing of the Al atoms?

12. Find the concentration of electrons and holes in silicon doped as follows: (a) undoped (intrinsic) silicon; (b) arsenic doped with 10^{16} atoms/cm^3; (c) phosphorus doped with 10^{20} atoms/cm^3. For this problem, use the expression $pn = n_i^2$, where n_i is the intrinsic carrier-concentration at 300 K.

13. Find the electron and hole concentrations in silicon at 300 K (a) for 1×10^{15} boron atoms/cm^3, and (b) for 1×10^{16} atoms/cm^3. Note, that in solving part (b), that each boron dopant atom creates one hole, and each arsenic atom creates one electron. Their presence cancels each other out, and the net majority carrier-concentration that results is $N_A - N_D$.

14. The intrinsic carrier-concentration n_i in silicon (cm^{-3}) is given by:

$$n_i = 3.1 \times 10^{16}\, T^{3/2} \exp(-6.03\ \text{eV}/kT)$$

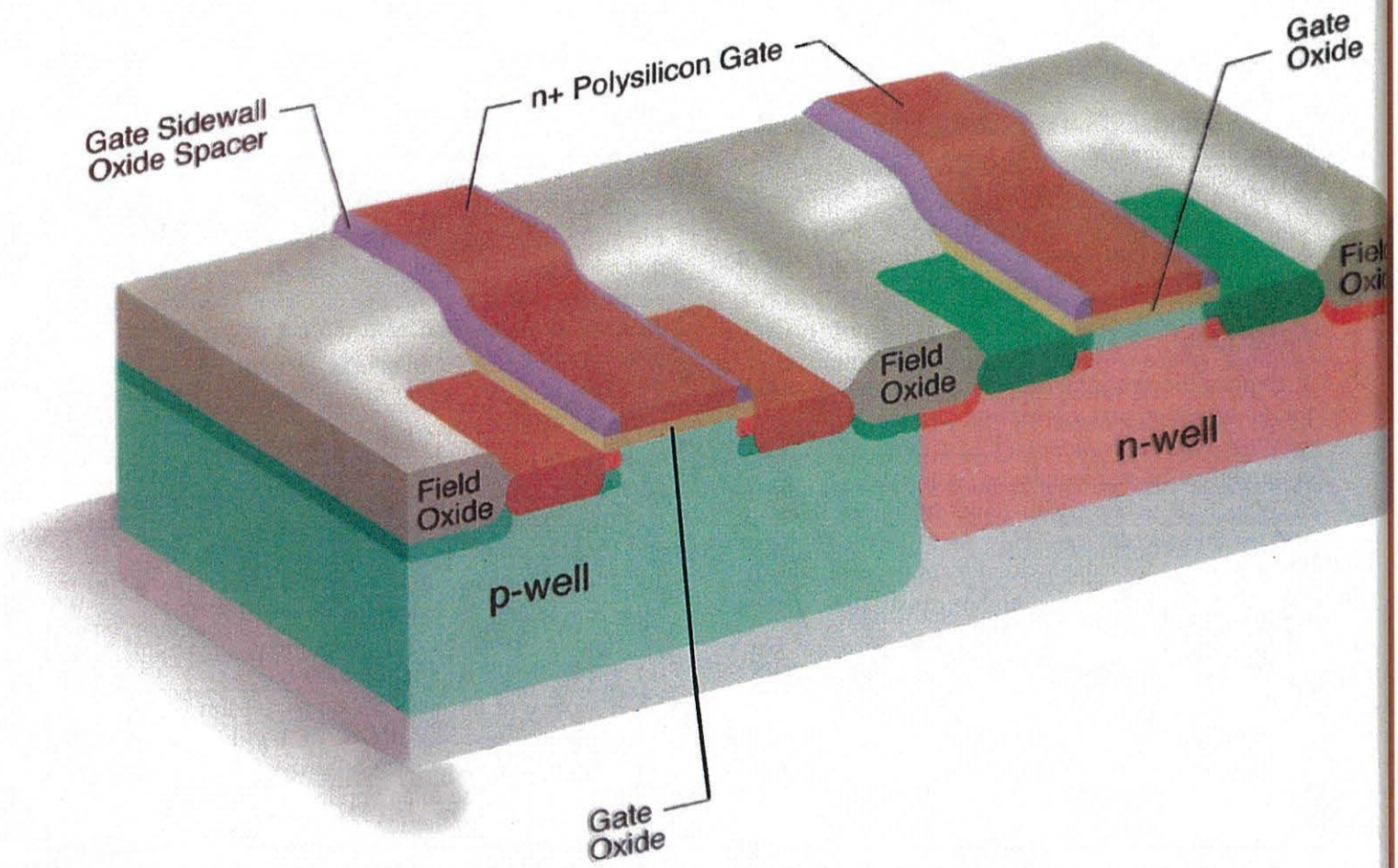
where T is in kelvin, and k is Boltzmann's constant. Use this equation to find n_i at: (a) room temperature; and (b) 800°C, and (c) 1000°C.

15. Plot the value of n_i versus T from 600°C to 1200°C, making the calculation every 100°C.

16. Find the resistivity of pure-silicon (in Ω-cm) at: (a) 300 K; (b) 77 K; and (c) 1000 K.

17. If a piece of intrinsic silicon is 100-μm in length, and has a cross-sectional area of 1-μm^2, how much current would flow in such a "resistor" at room-temperature in response to an applied voltage of 1-volt?

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Gate Sidewall
Oxide Spacer
n+ Polysilicon Gate
Gate
Oxide
Field
Oxide
Field
Oxide
n-well
p-well
Gate
Oxide

CHAPTER 7

BASICS OF THIN-FILMS

CHAPTER CONTENTS

7.1 STAGES OF GROWTH OF AMORPHOUS AND POLY-CRYSTALLINE THIN-FILMS

7.2 MECHANICAL-PROPERTIES OF THIN FILMS

7.3 MEASUREMENT OF ELECTRICAL PROPERTIES OF THIN-FILMS

"To render a problem tractable, we must concentrate on its most important features."

Andrew. S. Grove, *Physics and Technology of Semiconductor Devices,* Wiley, 1967.

Illustration of the various stages in the growth of polycrystalline and amorphous thin-films.

Various *thin-films* are used in the fabrication of ULSI devices.[1,2,3,5] Examples of some are illustrated in Fig. 7-1, which depicts the cross-section of a MOSFET and interconnect-layers on an IC. It can be seen that thin-films used in integrated-circuits include metals, semiconductors, and insulators. Their structure can be *crystalline* (e.g., epitaxial-silicon layers), *polycrystalline* (polysilicon, aluminum, tungsten, and copper films), or *amorphous* (silicon-dioxide or silicon-nitride films). They can also be deposited using a variety of different techniques (the subjects of later chapters of the book).

Since thin-films are so widely used in VLSI and ULSI devices, it is important to have an understanding of their chemical and physical properties, and the mechanisms by which they are formed. The purpose of this chapter is to provide such background information on thin-films.

The thin-films used in ULSI fabrication must satisfy many chemical, structural, and electrical requirements. For example, film-composition and thickness must be strictly controlled to allow effective-etching of IC structures. Very-low densities of both particulate-defects and film-imperfections (such as pin-holes), become critical for the small-linewidths,

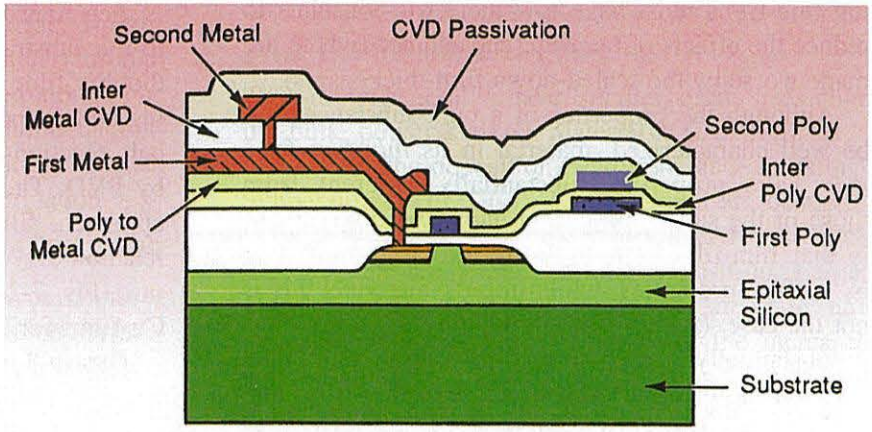


Fig. 7-1 Cross-section of an IC device-structure showing examples of the many kinds of thin-films used to build them.

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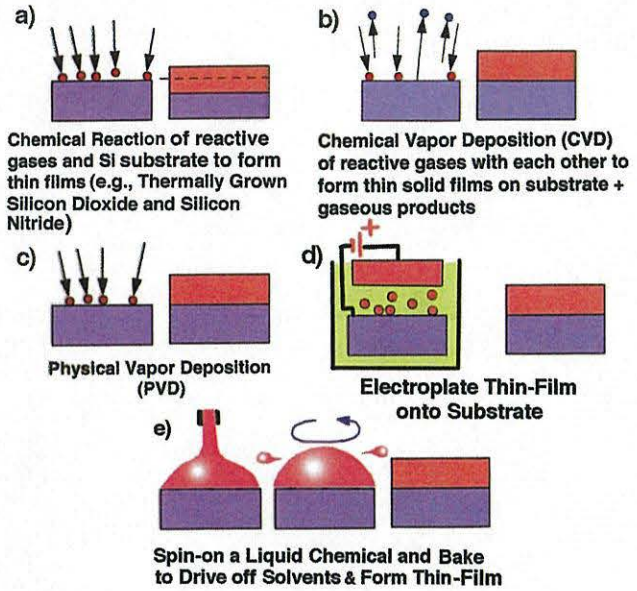


Fig. 7-2 Various methods used to form thin-films in ICs include: (a) Thermal-oxidation; (b) CVD; (c) PVD (d) Electroplating; and (e) Spin-On Liquid-Chemical & Bake.

high-densities, and large areas necessary for ULSI. These small geometries also create highly rugged topography for overlying films to cover. Therefore, excellent-adhesion, low-stress, and conformal-step coverage are required of a ULSI thin-film. If possible, its own surface contours should reduce or even planarize the underlying-steps. Finally, non-conducting thin-films must have low dielectric-constants to reduce the effects of parasitic-capacitance (which are made worse by the scaled-down film-thicknesses).

Although the properties of a bulk-substance may be well characterized, material in its *thin-film form* may have properties substantially different from those of the same material in *bulk-form*. One reason is that thin-film properties are strongly influenced by surface-properties, while in bulk-materials this is not the case. (A thin-film, by its very definition, has a substantially higher surface-to-volume ratio than does a bulk-material.) The structure of thin-films and their method of preparation also play a vital role in determining the film-properties.

The formation of such films is accomplished by a large variety of techniques that can be divided into three groups (see Fig. 7-2):

Group-1. *Film-growth* by interaction of a vapor-deposited species with the substrate (Fig. 7-2a);

Group-2. *Film-formation* by deposition without causing changes to the substrate material (Figs. 7-2b, 7-2c, and 7-2d);

Group-3. Coating of the substrate with a liquid, which is then dried to form the solid thin-film (Fig. 7-2e).

Group-1 includes thermal-oxidation and nitridation of single-crystal (and polycrystalline) silicon (Chap. 13), and the formation of silicides by direct-reaction of a deposited-metal and the substrate.

We see that **Group-2** includes another three subclasses of deposition. The first of these is *chemical vapor deposition* (CVD, Fig. 7-2b), in which solid-films are formed on a substrate by the *chemical-reaction* of vapor-phase species that contain the required constituents. (When a CVD-process is used to form *single-crystal* thin-films, the process is termed *epitaxy* and this is the subject of Chap. 17. The formation of *amorphous* and *polycrystalline* thin-films by CVD is discussed in Chap. 16.) The second of these is *physical vapor deposition* (PVD), in which the species of the thin-film are *physically* dislodged from a source to form a vapor (Fig. 7-2c). This vaporized-material is then transported across a reduced-pressure region to the substrate (wafer), where it condenses to form the thin-film. PVD includes the processes of sputtering and evaporation (Chap. 15). Note that no chemical- reactions occur during formation of thin-films by PVD. The last subclass is *electroplating*. In this approach, films are formed by an electrochemical-reaction of a liquid-electrolyte and a wafer immersed in it (Fig. 7-2d). Electroplating is used to deposit thin Cu-films for advanced interconnects (see Chap. 24).

Group-3 involves *deposition of a liquid on a substrate to form a thin-film* (most commonly by spin-coating, Fig. 7-2e). This is discussed in Ch. 18 as part of the *photoresist-processing* topic, and in Chap. 24, Sect. 24.3.3, which covers *spin-on low-k dielectrics*.

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The purpose of this chapter is to cover the terminology and properties of thin-films, in general. That is, basic background-information on the growth-mechanisms, structure, mechanical properties, and electrical properties of thin-films is provided for readers not well acquainted with materials-science concepts. By defining these properties early-on, it is not necessary to repeat such information each time a new thin-film deposition method is introduced. The specific formation and associated processing of particular films is described in detail in later chapters.

7.1 STAGES OF GROWTH OF AMORPHOUS AND POLYCRYSTALLINE THIN-FILMS

There are many types of *amorphous* and *polycrystalline* thin-films used in IC processing. Deposition of such thin-films on a substrate different from the film itself (for example, Al on SiO_2), involves the condensation of atoms in vapor-form (in this case Al) onto a solid-substrate. Such solid-film formation processes take place in three stages (see the chapter faceplate):

1. Nucleation
2. Coalescence
3. Continuous film-growth.

Since important properties of such polycrystalline films depend on how these stages occur, it useful to discuss each of them in more detail.

Condensation of vapor-atoms on a surface is initiated by formation of small *clusters* (or *nuclei*) through the random gathering of several adsorbed-atoms. The enlargement of these nuclei to form a continuous thin-film is termed *growth*. Often nucleation and growth can occur simultaneously during film-formation.

7.1.1 The Various Stages of Thin-Film Formation

In order for atoms in a vapor-phase to turn into a solid-film, they must condense on the solid-surface. Such condensation requires that there is an attraction between the vapor-atoms and the surface when the surface is struck by them. If sufficient attraction exists to allow an atom to become attached (*adsorbed*) onto a surface, it is then called an *adatom*. Such adatoms may continue to move about the surface by hopping from one location to another (*surface-migration*). The energy for surface-migration can be supplied by a heated substrate-surface. However, in the course of such hopping, some adatoms may also re-evaporate from the surface back into the vapor-phase.

Such migrating-adatoms may encounter other adatoms on the surface. If they are sufficiently attracted to one another, small clusters of adatoms will start to form, called *nuclei*, and their formation is known as *nucleation*. Nuclei are much less mobile than individual-adatoms, and they tend to remain at the locations where they are formed. The onset of *condensation* is thus marked by the initial formation of such nuclei.

After the formation of sufficiently large-sized nuclei, the *film-growth stage* begins. Film-growth has been studied with the aid of electron-microscopy, and several-substages of growth have been observed (see Faceplate). The *island-stage* occurs when nuclei grow in three-dimensions. This stage is followed by *coalescence*, where nuclei contact each other and form new larger and rounded shapes. Eventually during coalescence, larger-islands take on a crystallographic appearance, in the form of hexagonal-shapes. The large islands continue to grow, leaving behind channels or holes of exposed substrate (*channel-stage*). Finally, a *continuous-film* is formed.

7.1.2 The Structure of Thin-Films

Thin-films generally have smaller grain-sizes than do bulk polycrystalline materials. *Grain-size* is a function of the deposition-conditions and annealing-temperatures (Fig. 7-3). Larger grains are observed in thicker-films. This effect is enhanced by raising the substrate-temperature during deposition. Larger grains are expected for increased substrate and annealing temperatures as a result of the increased surface-mobility of adatoms. Annealing a film at a temperature equal to that at which it was deposited does not produce as large grains.

Surface-roughness of films (see Fig. 7-4) occurs as a result of the randomness of the deposition-process.

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Real films almost always show surface-roughness, even though this represents a higher energy-state than that of a perfectly-flat film. Depositions at high-temperatures tend to show less surface-roughness. This is because increased surface-mobility from the higher substrate temperatures can lead to leveling of the peaks and valleys. On the other hand, higher-temperatures can lead to the development of crystal-facets, which may continue to grow in favored-directions, leading to *increased* surface-roughness. At low-temperatures, surface-roughness (as measured by surface area) tends to increase with increased film-thickness.

The *density* of a thin-film provides insight about its physical structure. Density is usually found by weighing a film and measuring its volume (area x thickness). If a film is porous after being deposited, it usually has a lower-density than does bulk-material.

The *crystallographic-structure* of thin-films depends on the adatom-mobility, and can vary from a highly disordered (or amorphous-like) state, to a well-ordered state (e.g., *epitaxial-growth* on a single-crystal substrate). *Amorphous-structures* are frequently observed for deposited dielectrics such as SiO_2 and Si_3N_4, while most metal thin-films have a *polycrystal-line-structure*. Silicon-films can be either amorphous, polycrystalline, or single-crystal, depending on the deposition-parameters and the substrate material.

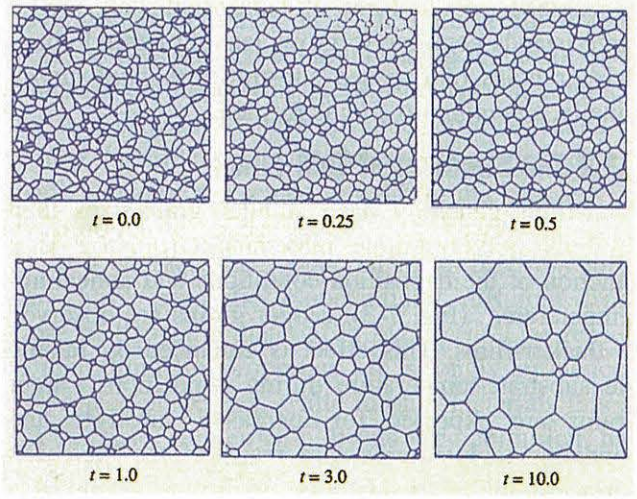


Fig. 7-3 Simulation of normal grain-growth in a polycrystalline thin-film at elevated temperature with time.[7] Reprinted with permission of TMS (The Minerals, Metals, and Materials Society) .

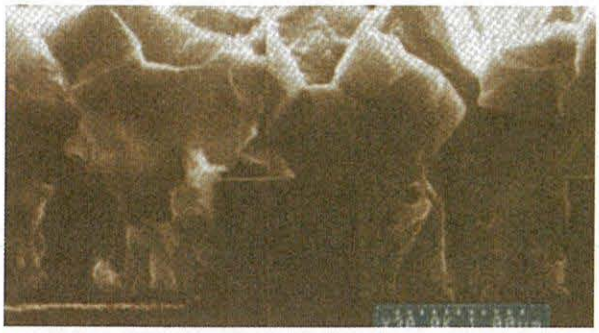


Fig. 7-4 CVD tungsten-film, deposited under conditions that produces severe surface-roughness.

7.1.3 Factors that Influence Epitaxial-Deposition of Thin-Films

Epitaxial-growth is another way that thin-films can be formed. However, these growth-mechanisms are quite different from the polycrystalline and amorphous film-growth described above. That is, *epitaxial-growth* is the phenomenon that can occur on a crystal-surface such that the deposited-film has an ordered structure. Typically, it is formed with a single-crystal structure of its own. If the film and the substrate are composed of the same material, this growth is termed *homo-epitaxy* (e.g., Si-on-Si, and GaAs-on-GaAs), while if the film and substrate are different materials, such growth is termed *heteroepitaxy* (e.g., single-crystal Si on crystalline Al_2O_3 [sapphire], also called *silicon-on-sapphire* [SOS]).

A *single-crystal substrate* is the most important factor needed for epitaxial-growth to occur. However, some *crystal-symmetry* must also exist between the deposited-film and the substrate, and the *lattice parameters* of each material must also be close to the same value. That is, to achieve epitaxy, the lattice-misfit (which is the percentage-difference between the lattice-constant of the deposit and that of the substrate-plane in contact), must also be small. The *deposition-temperature* also plays a role in epitaxy. That is, the likelihood that epitaxial-growth will occur

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is increased by elevated temperatures, clean substrate-surfaces, and increased adatom-energy.

The *deposition-rate* also plays a role in epitaxy. Lower deposition-rates favor epitaxy, while higher deposition-rates lead to polycrystalline or amorphous films. Three growth-regimes are observed for the deposition of Si on a clean Si-substrate: **1**) at low-temperature and high deposition-rates the deposits are amorphous; **2**) at high substrate-temperatures and low deposition-rates, they tend to be single-crystal; and **3**) at intermediate-conditions, polycrystalline-films tend to form. Chapter 17 discusses the growth of epitaxial silicon-films in more detail.

7.2 MECHANICAL PROPERTIES OF THIN-FILMS

7.2.1 Adhesion of Thin-Films

The adhesion of grown and deposited films used in ULSI processing must be excellent (both *as-deposited*, and after subsequent processing). Film-delamination from the substrate would result in device-failure. Thus, excellent-adhesion is critical to maintaining the electrical and mechanical integrity of the structure, particularly in multilevel-metal interconnects.

A simple *qualitative* technique for measuring the adhesion of thin-films is the *tape-test*. It consists of pressing a piece of adhesive-tape to the film (Fig. 7-5b). When the tape is pulled off, the film is either removed (in whole or in part), or remains on the substrate. This method is qualitative, and if the film remains on the substrate, this test does not provide any data about the magnitude of the adhesion-forces. If the film is removed, a *quantitative-value* of the adhesion can be obtained by measuring the force to remove it. Nevertheless, for most films used in VLSI processing, failure of the tape-test implies that the film is probably unsuitable for device-fabrication.

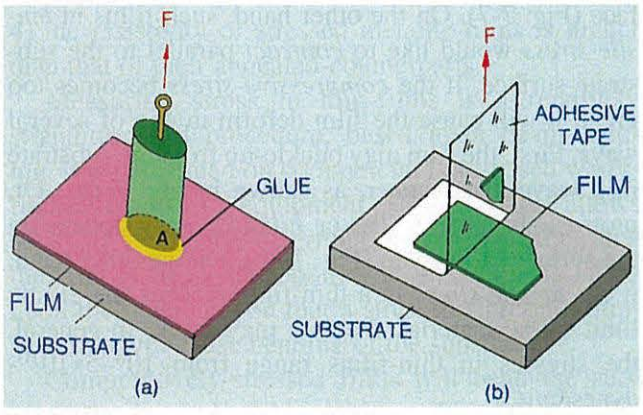


Fig. 7-5 Measuring adhesion of a thin-film to a substrate: (a) pull-off test; (b) tape-test.

A relatively simple *quantitative* pull-test for measuring adhesion involves attaching a small metal-pin to the film-surface (after surrounding film-material has been removed, and with an epoxy that does not react with the film material, Fig. 7-5a). An increasing force is applied normal to the substrate-surface, until either the *film-substrate* or *film-epoxy* bond fails.

Adhesion is strongly effected by the cleanliness of the substrate. Contamination generally results in reduced-adhesion, as does an adsorbed gas-layer. Effective-cleaning of the substrate prior to deposition is therefore important to insure good film-adhesion.

In some applications it is necessary to include a layer of a strong oxide-forming element between an oxide-substrate and such metal thin-films as tungsten, copper, and gold (which all adhere-poorly to oxide surfaces). Various layers have been used to serve as such intermediate "adhesion" (or "glue") layers, including titanium and chromium.

7.2.2 Stress in Thin-Films

Nearly all thin-films are found to be in a state of internal stress, regardless of the means by which they have been produced. The stress may be *compressive* or *tensile*. Such stresses arise because films are usually deposited at elevated-temperatures. Generally, the film and the substrate have different *coefficients-of-thermal-expansion* (CTE). Thus, when they cool down to room-temperature, the film (which must tightly-adhere to the substrate) does not have the same length as it would have if could have cooled without being attached to the substrate.

By analogy, an Al-thin-film and a Si-wafer can be considered to be two springs made of Al and Si, respectively (and each having the same initial length, as shown in Fig. 7-6a). For this example, we assume

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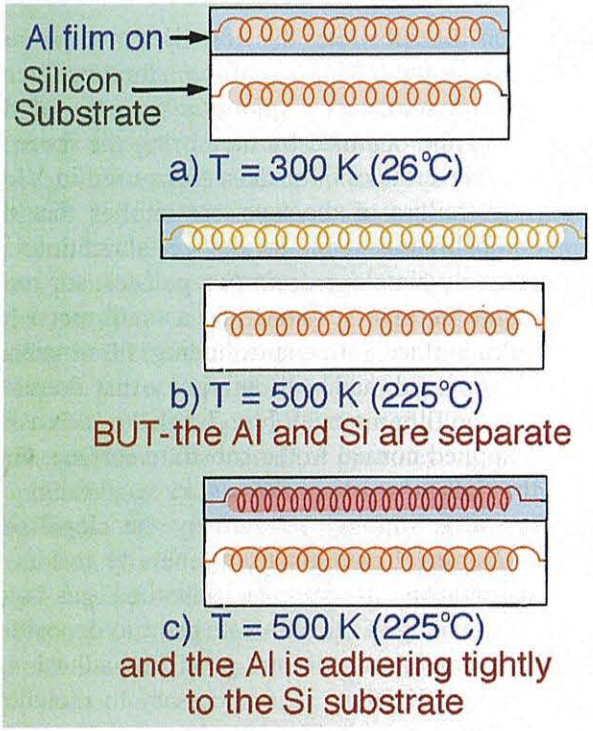


Fig. 7-6 An example of how *compressive-stress* arises in a thin-film adhering to a thicker substrate, using coil-springs as an analogy: (a) An Al-thin film (1-μm thick) is deposited on a silicon wafer that is much thicker (500-μm thick). Assume that at room-temperature there is no stress in the Al film, and both the Al-film and the Si wafer are like coil-springs at their natural-length at that temperature; (b) If the temperature is raised, the materials will expand. Since the CTE of Al ($23x10^{-6}$ $°C^{-1}$) is much larger than that of Si ($2x10^{-6}$ $°C^{-1}$), if the Al-film and the Si were not attached to one another, the Al would expand more than the Si-wafer in the lateral direction; (c) But since the Al-film adheres tightly to the Si wafer, it cannot expand as much it could, and thus ends up being like a compressed coil-spring.

that at *room-temperature* the springs are not stressed (i.e., neither spring is compressed or extended). Let us consider what happens if we heat the springs to the same elevated-temperature while they are unattached. In this case, each is free to expand to the degree dictated by their respective CTE. (This implies that the Al-spring - with a larger CTE - becomes longer than the Si-spring, see Fig. 7-6b). Nevertheless, such

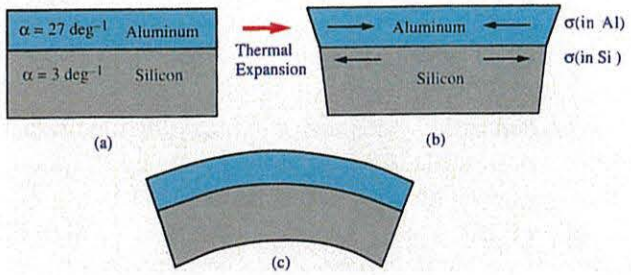


Fig. 7-7 Thermal-expansion-differences between Al and Si, shown in (a), lead to stresses in the Al thin-film and Si substrate, shown in (b). In this case, tensile-stress develops on top of the Si substrate and compressive-stress develops in the Al thin-film. (c) Illustrates the bending of the structures (exaggerated) that occurs due to these forces.

unconstrained, heated-springs are not yet stressed by heating. (In other words, "free" springs do not become compressed or extended when heated.) However, if two such *tightly-adherent* springs are heated, the Al-spring cannot expand to the length it could when not-attached to the Si-spring. Instead, its tendency to expand is constrained by the thicker Si-wafer, putting it into a compressed state (Fig. 7-6c). Note that even if the ends of such compressed-springs remain fixed, their stress can be released if the spring pops outward somewhere along its length. Such stress-relief events occur in thin-films on Si-wafers, as discussed next.

From the above analogy, we see that if thin-films formed on a Si-wafer become compressively stressed, they would like to *expand* parallel to the substrate surface (Fig. 7-7). On the other hand, such films in *tensile-stress* would like to *contract* parallel to the substrate-surface. If the *compressive-stress* becomes too great, it will cause the film deform in one of several ways. First, the film may buckle-up from the substrate in a wave-like manner, as shown in Fig. 7-8a. Or, protrusions (small hills, or *hillocks*) may appear on the surface of the film (Fig. 7-8b). On the other hand, if the *tensile-stress* in a thin-film exceeds the elastic limit of the material, the film may crack. In general, the stresses in thin-films range from 10^8–$5x10^{10}$-dynes/cm^2.

Highly-stressed films of either kind thus are generally undesirable for VLSI applications. Some of the

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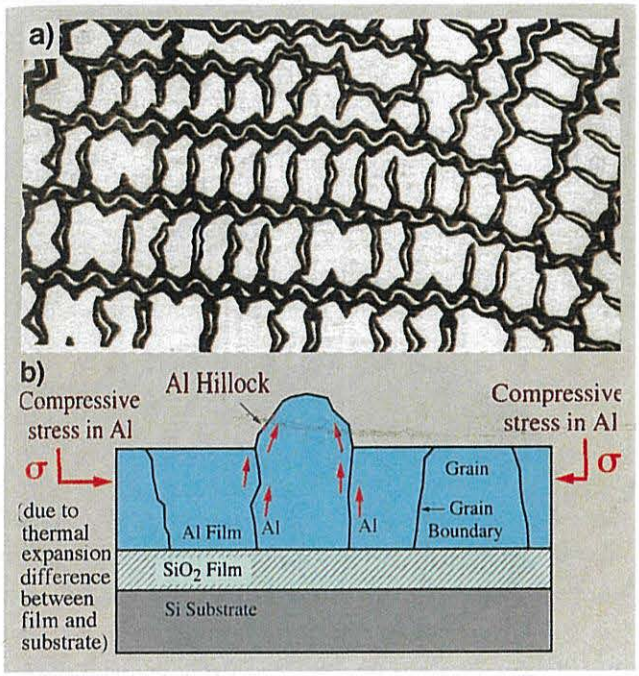


Fig. 7-8 (a) Tungsten thin-film on mica at 300°C, showing buckle waves. (b) Schematic-illustration of *hillock-formation* due to compressive-stress in an Al-film on a silicon-wafer (with an SiO_2 layer grown on it's surface). Aluminum-diffusion along grain-boundaries is indicated.[4] Reprinted with permission.

problems they cause are: **1**) they are more likely to exhibit poor-adhesion; **2**) they are more susceptible to corrosion; **3**) brittle films, such as inorganic-dielectrics, may undergo cracking in tensile-stress; and **4**) the resistivity of stressed metallic-films is higher than that of their annealed-counterparts.

Measuring stress in thin-films is a relatively straightforward procedure, based upon beam-bending. It is performed on commercial laser-based wafer-flatness measuring-equipment. This technique allows stress to be directly determined on the substrate that the film is deposited upon. The procedure is based upon the phenomenon that a stressed-film on a thin-substrate will cause bending of the substrate.

Compressively-stressed films will bend the substrate so that it becomes *convex* (Fig. 7-9a), while tensile-stressed films will make it *concave* (Fig. 7-9b). With Si-wafers, the film is deposited on one side, and stress is determined by measuring the deflection of the wafer-center. Use of laser flatness-equipment allows direct-measurement of the wafer-deflection.

7.3 MEASUREMENT OF ELECTRICAL PROPERTIES OF THIN-FILMS

The *sheet-resistance* R_S of a conducting thin-film is one of its most important electrical-characteristics. This is because R_S is frequently used to monitor the deposition of conducting-film processes and deposition-chamber performance. The concept behind the sheet-resistance parameter can be explained as follows. The resistance of a rectangular-shaped section of film of length = l, width = b, and thickness = t (measured in the direction parallel to the film), is given by:

$$R = \frac{\rho l}{t b} \qquad (7.1)$$

where R is the resistance of the film and ρ is its' resistivity. If the film-length equals its width and (i.e., l = b), Eq. 7-1 then becomes:

$$R = \rho/t = R_S \qquad (7.2)$$

where R_S is defined as the sheet-resistance in units of Ω/*square* of the film. Note that R_S is independent of the size of the square, and depends only on the film-resistivity and thickness of the film. As shown in Fig. 7-10, for a given thin-film, the sheet-resistance is the same for each of the squares. If the thickness and sheet-resistance are known, the film-resistivity can be calculated from:

$$\rho = R_S t \qquad (7.3)$$

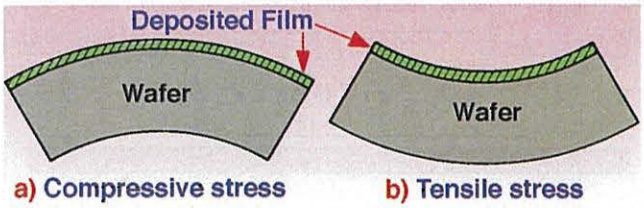


Fig. 7-9 (a) Compressive-stress causes *convex* bending of the substrate. (b) Tensile-stress causes *concave* bending.

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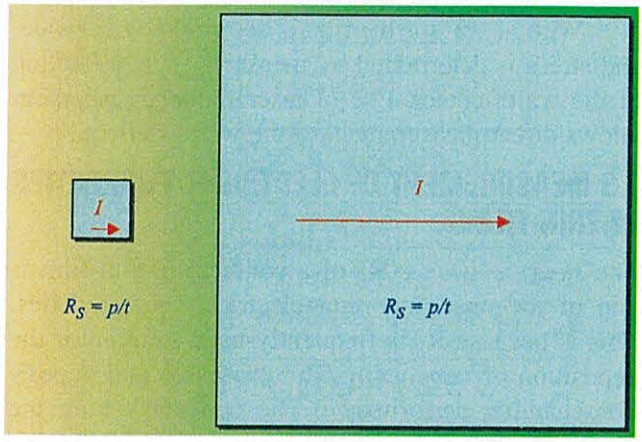


Fig. 7-10 The *sheet-resistance* R_S is the same for these two squares.

The sheet-resistance, R_S, can be measured by several techniques. In the direct-measurement method, a conductor strip is fabricated (Fig. 7-11). The voltage-drop across the strip-length is measured while a current is driven through the conductor. The resistance of the strip is given by R = V/I. The number of squares are counted between the voltage terminals, and R_S = R/N (where N is the number of squares, i.e., N = l/b).

A second method which does not require the use of a conducting strip is the *4-point-probe method* (Fig. 7-12).[6] It is the more commonly-used method

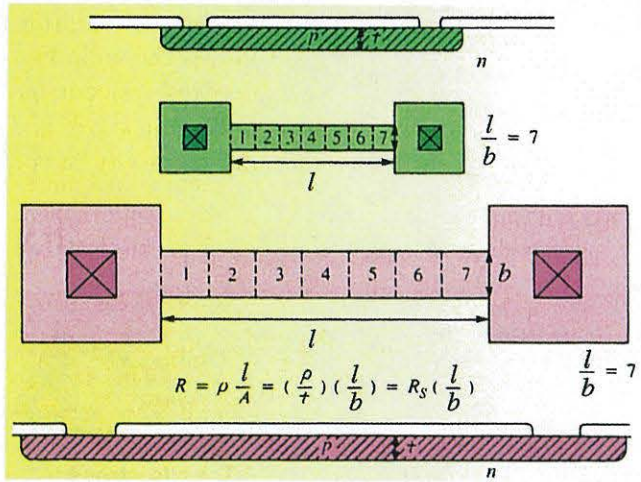


Fig. 7-11 Top- and side-views of two diffused-resistors of different physical size, but with equal values of resistance. Each resistor has a ratio of *l/b* equal to 7 squares.

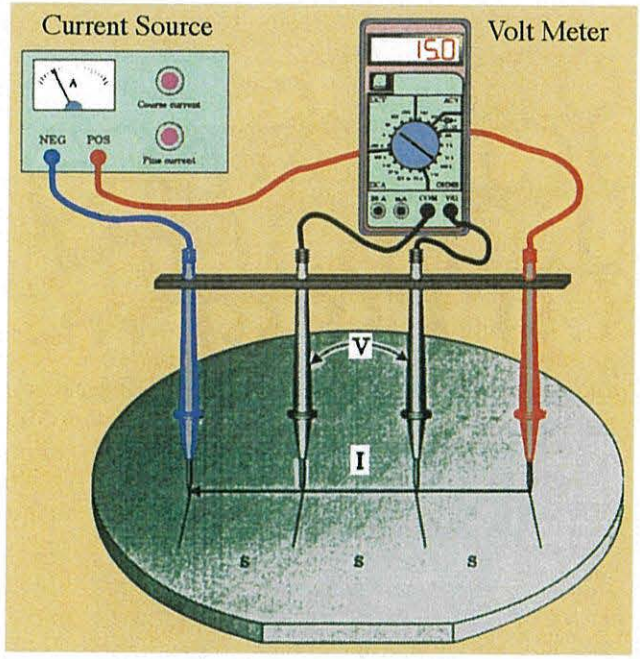


Fig. 7-12 Schematic of a *4-point-probe* measurement setup.

of measuring R_S. A fixed-current is passed between the two outer-probes, and the voltage across the inner two probes is measured. If the sample is semi-infinite (with regards to the probe spacings), and the probe-spacings, s, are equal, then the resistivity ρ is given by:

$$\rho = \frac{t\,V\,2\pi}{I\ln(2)} = 4.532\,\frac{t\,V}{I}\ \text{(ohm-cm)} \qquad \textbf{(7.4)}$$

If the material on which the probe is placed is an infinitely-thin slice on an insulating substrate, then Eq. 7-4 reduces to an equation for R_S;

$$R_S = 4.53\,\frac{V}{I}\ \text{(ohms/square)} \qquad \textbf{(7.5)}$$

Commercial equipment for measuring R_S in thin metal-films and semiconductor-layers is available.

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PROBLEMS

1. If a thin-film has a sheet-resistance of 1-kΩ/square, find the maximum resistance that can be fabricated on a 2.5 x 2.5-mm chip, for 2-μm lines and 4-*μm pitch* (i.e., the distance between the centers of the lines).

2. What is the total-number of squares in the straight diffused resistor depicted in Fig. 3-2?

3. What is the sheet resistance of a 1-μm-thick Al:Cu line with a resistivity of 3.2-$\mu\Omega$-cm?

4. Repeat Problem **3** for a polysilicon-line with a resistivity of 500-$\mu\Omega$/square.

5. The *coefficient of thermal expansion* (CTE) of Si at 100°C is $2.6\text{x}10^{-6}$/°C. How much would a 10-mm chip increase in length if heated by 300°C (assuming that the CTE is constant)?

6. A thin-film of Al ($\rho = 2.5\text{x}10^{-6}$ Ω-cm) is deposited, with a length of 0.1-cm, a thickness of 1-μm, and a width of 2.5-μm: (a) What is the resistance R (in Ω) of the strip; (b) For a current of 10-mA flowing along the strip, what voltage would you measure along the length, and how many watts are dissipated? (c) If the thickness of the Al strip is doubled, what is the resistivity? (d) If the ρ of half the length of the strip is doubled, what is the resistance of the strip?

7. Metal lines of varying widths are to be fabricated. Before being patterned, the sheet resistance of the metal film is measured and found to be 2.5-Ω/sq. Find the total resistance of 0.5, 1.0, 2.0, and 5.0 μm wide and 1-cm long lines. What other information is still needed before it can be determined what type of metal makes up these lines?

8. Explain why *compressive-stresses* in thin-films can cause *convex-bending,* and *tensile-stresses* can cause *concave-bending* of the substrates on which they are deposited.

9. The linear thermal-coefficient-of-expansion of Al is of the order of $25\text{x}10^{-6}$ cm/cm/°C, and that for Si is $2.6\text{x}10^{-6}$ cm/cm/°C. Using this information, offer an explanation as to why thin-films of Al on Si substrates exhibit hillocks, after being subjected to elevated temperatures (e.g., > 250°C).

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CHAPTER 9

SILICON: SINGLE-CRYSTAL GROWTH

CHAPTER CONTENTS

9.1 CRYSTAL TERMINOLOGY

9.2 MANUFACTURING SINGLE-CRYSTAL SILICON

9.3 CZOCHRALSKI CRYSTAL GROWTH

9.4 CRYSTAL-DEFECTS IN SILICON

9.5 POINT-DEFECTS IN SILICON CRYSTALS

9.6 ONE-DIMENSIONAL DEFECTS (DISLOCATIONS)

9.7 AREA-DEFECTS IN SILICON CRYSTALS

9.8 BULK-DEFECTS AND PRECIPITATON

9.9 OXYGEN IN SILICON

9.10 GETTERING

"To see a world in a grain of sand,
and Heaven in a wild flower,
Hold infinity in the palm of your hand,
and Eternity in an Hour."

Robert Blake

Illustration of several process steps during Czochralski (CZ) crystal growth.

In the next two chapters we show how *single-crystal silicon starting-material* is produced.[1-6] In Chap. 9, we first explain how raw-material is processed to obtain *electronic-grade polysilicon* (*EGS*). Then the Czochralski-method of growing single-crystal silicon from such EGS is described. The crystalline-defects that occur in silicon (and techniques for suppressing their formation) are also covered in this chapter.

The technology for forming *silicon wafers* from single-crystal ingots is covered in Chap. 10. This includes a discussion of the material, electrical, and structural characteristics that such wafers must possess in order to be suitable for VLSI (and ULSI) fabrication.

9.1 TERMINOLOGY OF CRYSTAL-STRUCTURE

Solid-matter exists in crystalline and amorphous forms (Fig. 9-1). In crystalline-solids, the atoms which make up the solid are spatially arranged in a periodic-fashion. If this periodic-arrangement exists throughout the entire solid, the substance is defined as being formed of a *single-crystal*. If the solid is composed of many small single-crystal regions, the solid is referred to as *polycrystalline-material*. Nevertheless, within any single-crystal region, the structure appears exactly the same at one point as it

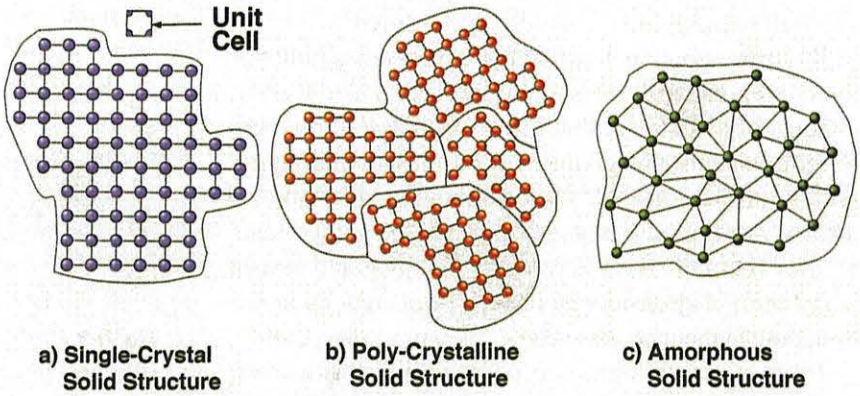


Fig. 9-1 The three different forms of solid-material: (a) Single-Crystal. (b) Poly-Crystalline. (c) Amorphous.

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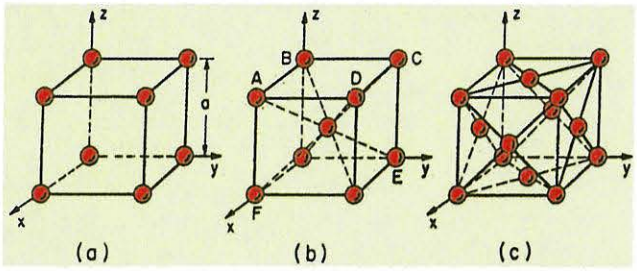


Fig. 9-2 Cubic-crystal unit-cells: (a) Simple Cubic SC; (b) Body-Centered Cubic BCC; (c) Face-Centered Cubic FCC.

does at a series of equivalent points. An *amorphous-material* has no such long-range periodic-structure. The *starting Si-material* (*wafers*) on which VLSI and ULSI circuits are built, have single-crystal form.

The periodic-arrangement of atoms in a crystal is called the *lattice*. The crystal-lattice always contains a volume representative of the entire lattice (referred to as a *unit-cell*), which is regularly repeated throughout the crystal (Fig. 9-1a). The importance of unit-cells is that crystals as a whole can be studied by analyzing such representative volumes. For example, distances of nearest-neighbor atoms in a lattice can be found.

The simplest crystal-lattices are the three *cubic lattices* seen in Fig. 9-2: (a) *Simple Cubic* [SC]; (b) *Body-Centered Cubic* [BCC], and (c) *Face-Centered Cubic* [FCC]. The dimension **a** for a cubic-cell is called the *lattice-constant,* but the distance of nearest-neighbor atoms may be smaller than **a**. For example, in an FCC-lattice the nearest-neighbor distance is one-half the diagonal of a cube face, or $(\mathbf{a}\sqrt{2})/2$.

The directions in a lattice are expressed as a set of three integers, with the same relationship as the components of a vector in that direction. These three vector-components are given in multiples of the *basis-vectors* of the unit-cell. For example in cubic lattices, the *body-diagonal* (see Fig. 9-3c) has the components of 1a, 1b, and 1c. Therefore, this diagonal exists along the [111]-direction. (The [ ]-brackets are used to denote a specific direction.)

From a crystallographic point of view, however, many directions in a crystal are equivalent, depending only on the arbitrary choice of orientation for the axes. Such equivalent directions are expressed with angular brackets < >. For example, the crystal-directions [100], [010], and [001] in a cubic-lattice are all crystallographically equivalent, and are collectively referred-to as <100> directions.

It is also useful to describe *planes* in a crystal (see also Fig. 9-3). Note that ( ) parentheses are used to denote a specific plane. For *cubic-lattices*, direction [*h k l*] is perpendicular to a plane with the identical three integers (*h k l*). This fact makes it convenient to analyze cubic-lattices. That is, if either a *direction or a plane* in a cubic-lattice is known, its perpendicular-counterpart can be quickly determined without further calculation. For example, the (100)-plane is perpendicular to the [100]-direction.

Silicon has a *diamond cubic-lattice*, a structure which can be represented as two interpenetrating face-centered-cubic lattices (Fig. 9-4a). Thus, the simplicity of analyzing and visualizing cubic-lattices can be extended to characterization of silicon-crystals. The three-dimensional representation of a diamond-lattice unit-cell is shown in Fig. 9-4b and 9-4c.

In studying the diamond-lattice unit-cell, it is evident that each atom has four nearest-neighbors (see Fig. 9-4c). The importance of this fact becomes evident when the electronic-structure of silicon is considered. That is, since Si is a Column-IV element, and has four valence-electrons, each of these electrons in the Si crystal-lattice is shared with one of its four nearest-neighbor Si-atoms. (This nearest-neighbor atom likewise contributes one of its electrons to the

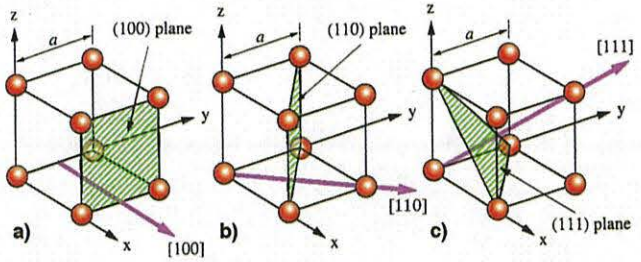


Fig. 9-3 Crystal-planes and major directions for a cubic-lattice. The heavy-arrows in each figure correspond to crystal-directions designated by the brackets [hkl]. The shaded-areas are the corresponding crystal-planes, designated by the brackets (hkl).

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bond.) As discussed in Chap. 2, the two valence-electrons shared between nearest-neighbor atoms form a *covalent-bond* and such interactions of electrons in neighboring-atoms of a solid serve the function of holding the crystal together. Since all valence-electrons in a perfect Si-crystal are involved in such shared bonding-pairs, none are available as free-electrons to conduct electrical-current (as long as they remain localized in the bonding region). However, covalently-bonded electrons can be excited, becoming free to participate in conduction. (Note in Si, **a** = 5.43-Å, and the nearest-neighbor distance is 2.43-Å.)

In several processing technologies, reference is made to various planes and directions in silicon-crystals - especially to the (100), (110), and (111) planes (and directions). This is because various structural-properties of Si depend on crystal-orientation, as do many ULSI fabrication-steps. For example {111}-planes have the highest-density of atoms. Therefore {111}-planes oxidize more rapidly than do {100}-planes (since more atoms per unit surface-area are available for the oxidation-reaction). Also, all MOS-devices are fabricated on {100}-wafers, since the smallest surface-state densities are observed on such orientations. Finally, Fig. 9-4d illustrates the open structure of the silicon-lattice. Unobstructed channels can be seen to exist when crossing the Si-crystal along <110>-directions (i.e., perpendicular to the {110}-plane shown in Figs. 9-3b and 12-9d).

Actual solid-materials in the form of single-crystals differ to some extent from the ideal crystal-structure discussed in this section. To begin with, even ideal-crystals possess *surfaces* at their boundaries, and at a surface, the atoms are incompletely-bonded. In addition, real crystals have a variety of imperfections (called *crystalline-defects*) which significantly alter the properties of the crystal. (More information about defects in Si and their impact on crystal and device properties is given later in the chapter.)

It is useful to note the units used to specify dopant and contaminant-concentrations in Si. Usually they are given in *atoms/cm*^{3}, but sometimes in *parts per million atoms* (*ppma*). Since there are about $5\text{x}10^{22}$ Si

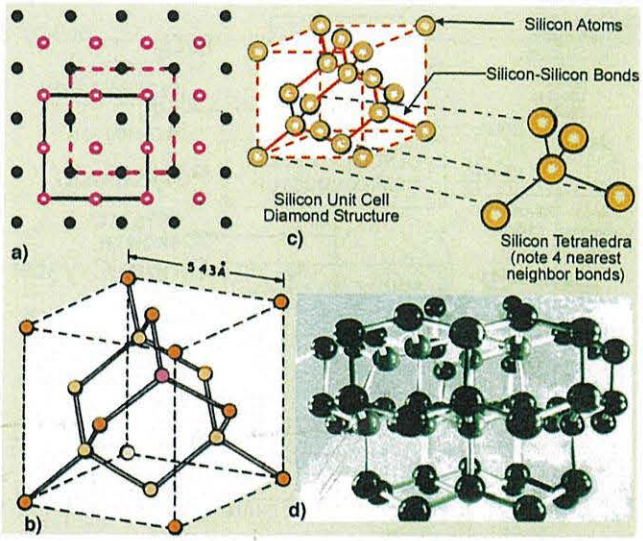


Fig. 9-4 (a) Top-view (along any <100>-direction) of an extended diamond-lattice unit-cell. The open-circles indicate one FCC sub-lattice and the solid-circles indicate the interpenetrating FCC-lattice; (b) Schematic-drawing of the diamond-lattice unit-cell; (c) Schematic drawing of the diamond-lattice unit-cell that also shows the four nearest-neighbors of each silicon-atom. (d) Photograph of the diamond-lattice showing an example of the open channels that occur along some crystal-directions.

atoms/cm^3 in single-crystal-Si, an impurity concentration of $5\text{x}10^{16}$/cm^3 is equivalent to 1-ppma. Other concentration levels can likewise be converted.

9.2 MANUFACTURING SINGLE-CRYSTAL SILICON

The fabrication of VLSI and ULSI takes place on silicon-substrates (wafers) possessing very-high crystalline perfection. Polycrystalline-material cannot be used, since it would exhibit inadequately-short minority-carrier-lifetimes, due to the defects occurring at the grain-boundaries of the polycrystalline-grains. The method of obtaining such highly-pure single-crystal Si for ICs, involves several steps (Fig. 9-5):

1. Raw-material (*sand*), is refined by a complex, multi-stage process which produces *electronic-grade polysilicon*, EGS.
2. This polysilicon is used to grow single-crystal silicon by *Czochralski (CZ)* growth or *float-zone (FZ)* growth. Single-crystal Si is commercially

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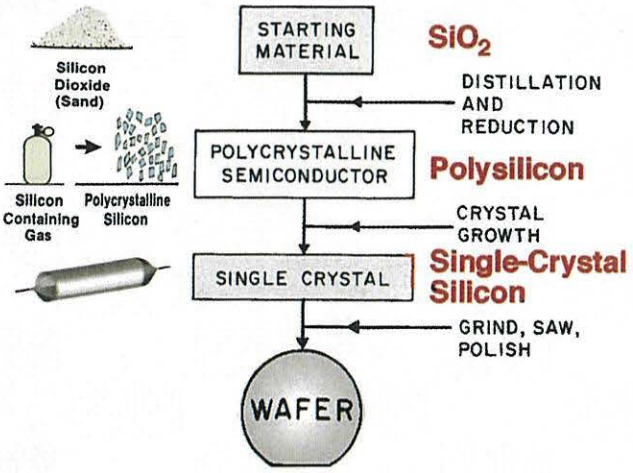


Fig. 9-5 Process sequence from starting-material to polished-wafer.

available in either {100}- or {111}-orientations.

In CZ-growth, single-crystal ingots are pulled from molten-silicon contained in a crucible. Czochralski-silicon is preferred for ULSI applications since it can withstand thermal-stresses better than FZ-material, and it is able to offer an internal-gettering mechanism that can remove unwanted impurities from the device-structures on wafer-surfaces. Float-zone crystals, because they are grown without making contact to any container or crucible, can attain higher-purity (and thereby higher-resistivity) than CZ-silicon. Devices and circuits calling for ultra-high-purity starting material (e.g., high-voltage or high-power devices) are sometimes fabricated from FZ-silicon.

9.2.1 From Raw Material to Electronic-Grade Polysilicon (EGS)

Single-crystal silicon is grown from melts of *electronic-grade polycrystalline silicon* (*EGS*). Since the CZ-process (which is used to grow most single-crystal silicon) adds impurities to the resultant ingot, the EGS must be extraordinarily pure. In fact, in order to achieve controlled-doping during subsequent single-crystal growth, EGS must have impurity-levels in the parts-per-billion atoms (*ppba*) range (or $10^{13}/cm^3$), making it the *purest-material routinely available on earth*. The raw-sand from which EGS is refined, contains high-levels of impurities (e.g., aluminum levels of $\sim 3x10^{20}/cm^3$). Thus, the refining-process must reduce these impurities by approximately *eight orders of magnitude!* Such a radical refining-procedure involves four major stages (Fig. 9-6):

1. Reduction of *silica* (*sand*) to *metallurgical-grade silicon* (*MGS*) with a purity of ~98%;
2. Converting *MGS* to *trichlorosilane* ($SiHCl_3$);
3. Purification of this $SiHCl_3$ by distillation;
4. Chemical vapor deposition (CVD) of Si from the purified $SiHCl_3$ as *EGS*.

Metallurgical-grade silicon is produced by heating silica with carbon in a reducing ambient (Fig. 9-6a):

$$SiO_2(solid) + 2C(solid) \rightarrow Si\ (solid) + 2CO(gas) \quad \textbf{(9.1)}$$

Metallurgical-grade silicon is mainly used in the manufacture of aluminum or for producing silicone-polymers. That is, most silicon manufactured every year is consumed by such applications, and only a

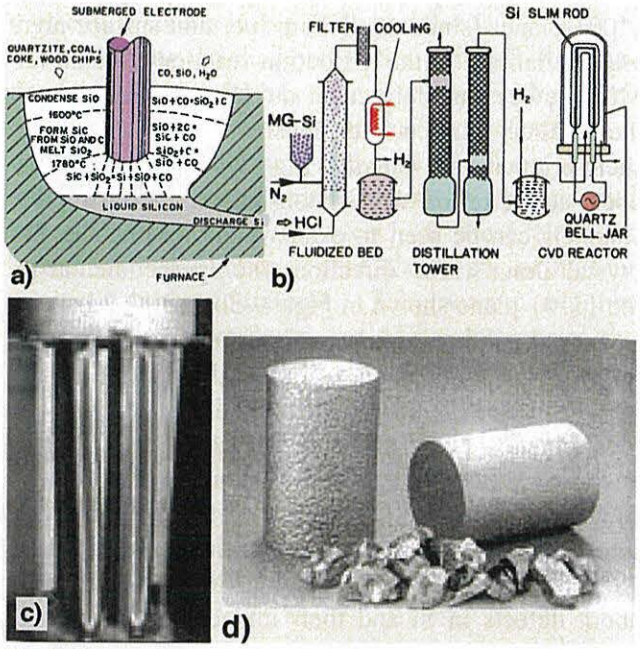


Fig. 9-6 (a) Schematic of submerged-electrode arc-furnace for production of MGS. Reprinted with permission of the publisher, the Electrochemical Society. (b) Schematic of fluidized-bed, distillation-tower, and CVD-reactor developed by Siemens. (c) and (d) EGS in polysilicon-form.

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small-fraction is further refined into EGS for silicon-wafers. The main impurities in MGS are Al and Fe.

These are removed in *Stage* **2** (Fig. 9-6b) in which trichlorosilane ($SiHCl_2$) is formed by the reaction of HCl and Si (MGS):

$$Si(sol) + 3HCl\ (gas) \rightarrow SiHCl_3\ (liq) + H_2\ (gas) \quad \textbf{(9.2)}$$

$SiHCl_3$ is a liquid at room-temperature (boiling point 31.8°C), and can be purified by distillation (*Stage* **3**, i.e., in a distillation-tower, as shown in Fig. 9-6b).

In *Stage* **4**, the highly-purified $SiHCl_3$ is converted back into polycrystalline-Si (*EGS*) by CVD in the presence of hydrogen:

$$2SiHCl_3\ (gas) + 2H_2\ (gas) \rightarrow 2Si\ (sol) + 6HCl \quad \textbf{(9.3)}$$

The process (first proposed by Siemens GmbH in the late 1950s) takes place in a reactor (rightmost chamber in Fig. 9-6b). The starting-surface is a thin silicon-rod which serves as a nucleation-surface for the depositing silicon. For large rods (200-mm in diameter and several meters long), the deposition process takes several-hundred hours. Figure 9-6c shows some examples of such EGS polysilicon-rods. In 1995 the worldwide-consumption of EGS was ~12-million kilograms ($1.2x10^{10}$ gm).

9.3 CZOCHRALSKI (CZ) CRYSTAL-GROWTH

Czochralski (CZ) growth, named for its inventor, involves the crystalline-solidification of atoms from a liquid-phase at an interface. The basic production-process for producing such CZ-Si has undergone remarkably little change since it was pioneered in the early 1950s.

The simplicity of the process and the relatively high-degree of crystal-purity helped establish the CZ-process as the dominant Si-crystal-growing technology in the early-years of the semiconductor industry. The development of dislocation-free ingot growth and automatic diameter-control in the late 1960s lead to a rapid growth in the sizes of ingot-diameters and crystal-melts. Further increases in charge-size and diameters were driven by the economic-advantages of even larger ingots. As shown in Fig. 9-7, by 1998 300-mm diameter crystals had become available, grown with

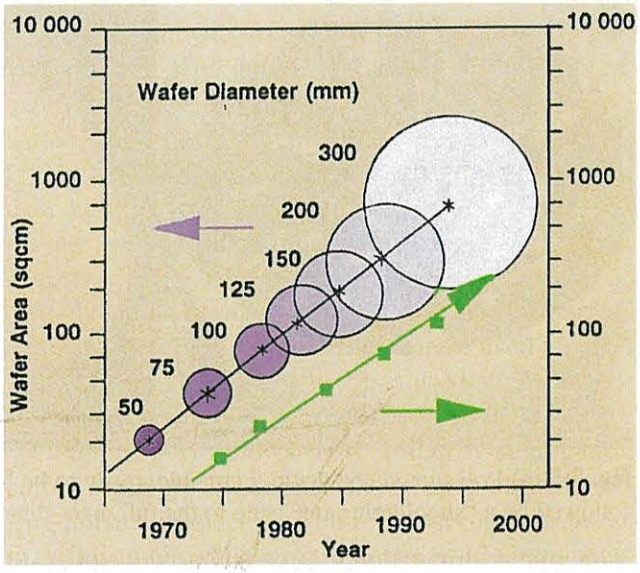


Fig. 9-7 The increase with time of CZ-silicon diameter.

150-kg charges. Typical commercial-ingots are grown 0.5–2.5-m in length, and a 100-kg charge can grow an ingot with a diameter of 200-mm, roughly 1-m long.

In this section we introduce the most important aspects of CZ-growth, focusing on the details that impact the material-properties of the silicon-wafers for ULSI. These include: **a**) the sequence of steps in the growth of the ingot; **b**) how impurities are incorporated into the ingot; **c**) the components of CZ crystal-growing equipment; and **d**) the evaluation of CZ silicon-crystals in ingot-form.

9.3.1 Czochralski Crystal-Growth Sequence

The steps used in growing a CZ Si-crystal are shown in the photographs on the chapter faceplate (p. 144). A schematic diagram of a CZ crystal-grower in which this process is performed is given in Fig. 9-14.

A fused-silica crucible is first loaded with a charge of undoped-EGS, together with a precise-amount of diluted silicon-alloy (Fig. 9-8a). The growth-chamber is then pumped out, backfilled with an inert-gas (to limit incorporation of atmospheric-gases into the melt during growth), and the charge is melted (the melting-point of silicon is 1421°C). Next, a slim seed-crystal of silicon (≈5-mm in diameter and 100–300-mm long)

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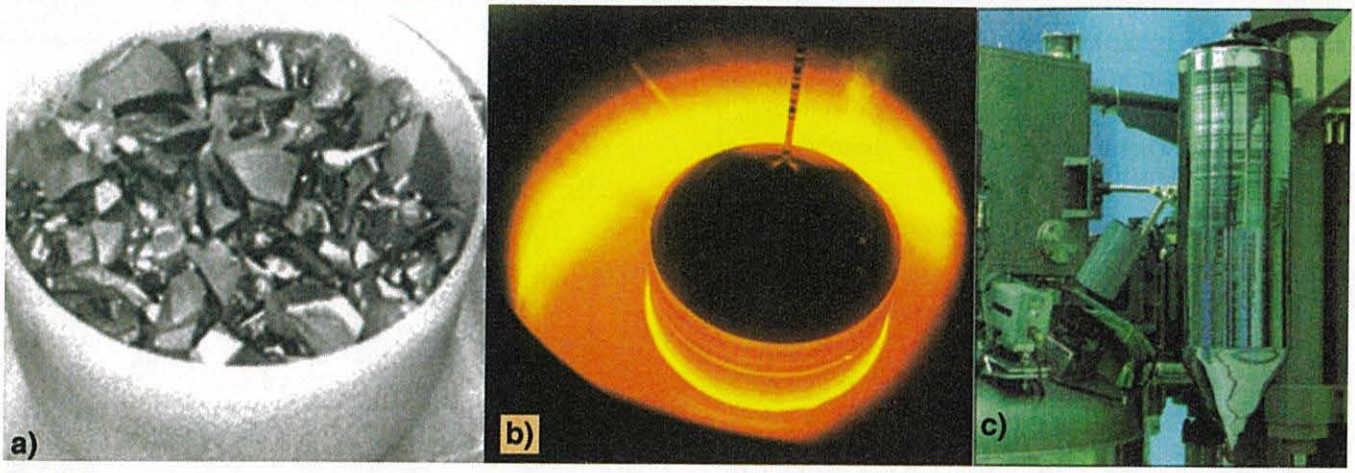


Fig. 9-8 (a) Polysilicon chunks in a crucible, ready to be loaded into CZ-crystal-puller. (b) A thin neck-region is first grown, followed by a "shouldering-out" step to the full ingot-diameter. (c) 300-mm single-crystal CZ Si-ingot.

with precise orientation is lowered into the molten-Si. The seed-crystal is withdrawn at a controlled rate. Both the seed-crystal and crucible are rotated during the pulling-process, but in opposite directions.

The initial pull-rate is relatively rapid so that a thin neck (~3-mm in diameter) is produced (Fig. 9-8b). As was first discovered by Dash, by forming this thin neck, the growing-ingot can achieve a macroscopically dislocation-free crystalline state. At that point, the melt-temperature is reduced and stabilized so that the desired ingot-diameter can be formed (*shouldering-out step*). This diameter is subsequently maintained by precise-monitoring of the pull-rate. The pulling continues until the charge is nearly exhausted, at which point the ingot is withdrawn to form the *tang* (*tail-off*). A shutdown-procedure of the furnace completes the process. Figure 9-8c shows a 300-mm ingot after it has been removed from the crystal-puller.

When CZ Si-crystals were first grown, the process required skilled operators to control all the important growth-parameters, including melt-temperature, ingot-diameter, pull-rate, and rotation. Today, such parameters are automatically-monitored, resulting in more reproducible-control of these aspects of the pulling-process. A variety of growth-process sequences can be carried out by modern crystal-growth systems, with "one-button" operations that automatically take the system from *meltdown* to *shutdown*.

9.3.2 Incorporation of Impurities into the Crystal

Impurities are incorporated into the CZ-crystal as it solidifies, together with the silicon. The desired impurities are included in the melt by adding precise amounts of silicon-alloy (heavily doped with the impurity of choice) into the crucible with the EGS. As the silicon grows, however, only a fraction of the impurity-concentration that was present in the molten volume that solidified (as specified by the value of the *segregation-coefficient* k_o of the impurity), gets incorporated into the crystal. The remaining-fraction remains in the melt (Fig. 9-9). As the ingot grows, the melt-volume is consumed, and therefore decreases. However, a fraction of the impurity arriving at the solidifying-interface between the melt and solid is continuously-rejected by the crystal and stays in the melt. If k_o is less than 1 (as is the case for most impurities in silicon, as shown in Table 9-1), the melt becomes progressively more concentrated with the impurity. As a result, as the ingot grows, the molten-material arriving at the melt-crystal interface contains an ever-larger proportion of impurity-atoms. Since the same *fraction* of total-impurities present in the arriving materials gets incorporated into the crystal, the ingot also becomes more heavily doped along its length.

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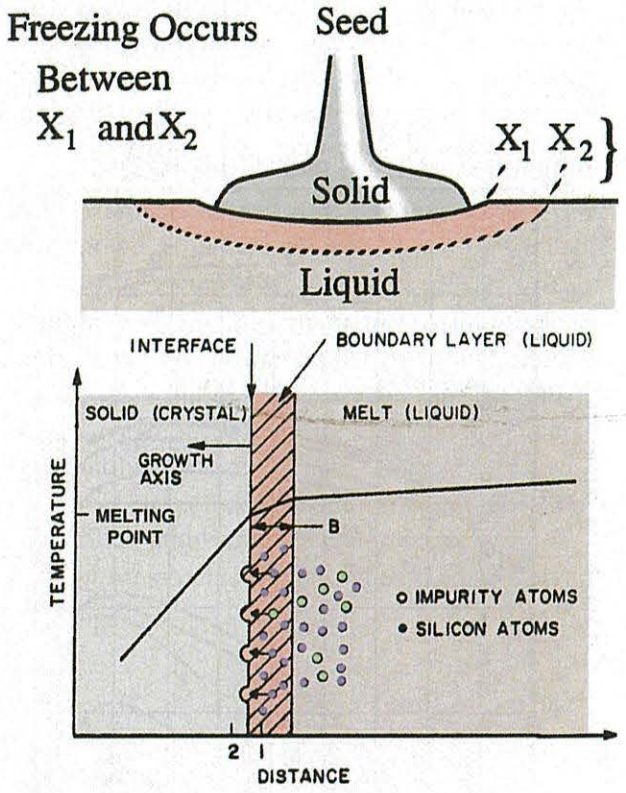


Fig. 9-9 *Impurity-segregation phenomena* near the melt-solid interface during CZ Si-growth.

Figure 9-10 shows how the predicted impurity-concentration in an ingot will vary for various k_o-values (including those of B and P). The information in Fig. 9-10 indicates that when k_o is close to 1 (e.g., for B, $k_o = 0.8$), it is less-difficult to achieve relatively-level resistivity values along the length of the ingot. But when $k_o << 1$ (e.g., for P, $k_o = 0.3$, or for Sb, $k_o = 0.023$), the impurity-concentration along the ingot length will vary much more.

Starting-wafers are available with specific impurity-concentrations from 10^{14}-10^{19}-atoms/cm^3 to meet the needs of various device-applications. The amount of an impurity that can be added into the melt is

Table 9-1 SEGREGATION COEFFICIENTS FOR COMMON IMPURITIES IN SILICON

IMPURITY	Al	As	B	O	P	Sb
k_o	0.002	0.3	0.8	1.25	0.35	0.023

is constrained by its *solubility-limit*. As shown in Fig. 9-12b, two *n*-type dopants (arsenic and phosphorus) have solubility-limits in Si that exceed 10^{20}/cm^3 at the Si melting-temperature, but boron is the only *p*-type dopant whose solubility-limit in Si that is greater than $1x10^{20}$ cm^3. Note that solubility is an issue for the electrically-active impurities in silicon for another reason. In some device-regions, high-concentrations of *p* or *n* dopants are required. Only those impurities with sufficiently-high solubilities can be used for such applications. That is why boron is used almost exclusively as the *p*-type dopant in silicon-devices.

Figure 9-11 shows how impurity-segregation during ingot-growth impacts the fraction of the ingot-length that can meet a given resistivity-specification. In this example, wafers must meet a 8–12 Ω-cm resistivity-range specification (~$0.8–1.2x10^{15}$/cm^3 impurity-concentration). About 80% of the ingot-length can provide such wafers if it is B-doped, but only 50% can be used if the ingot is P or As doped. If we also include the loss of ingot-material due to removal of grinding damage, the crystal-material-yields drop to 66% and 40% respectively.

Solid-Solubility: As defined in Chap. 5, a *solvent* is a substance capable of dissolving another substance

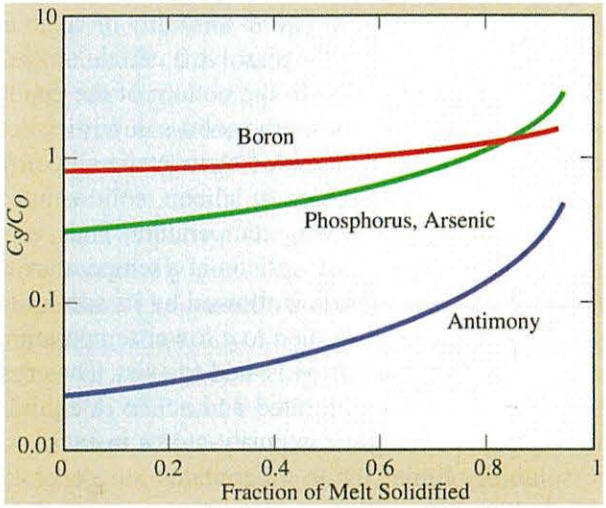


Fig. 9-10 Curves of growth from the melt, showing the doping-concentration in a solid as a function of the fraction solidified, with examples of some impurities in Si.

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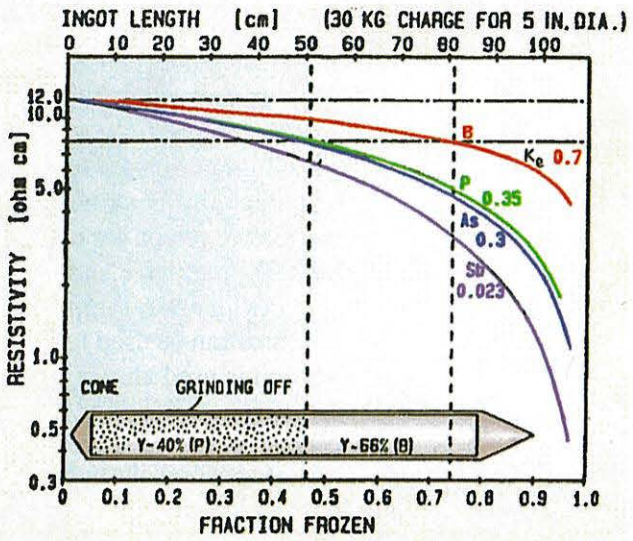


Fig. 9-11 Examples of resistivity distributions for several dopants along the ingot-length.

to form a *solution*. In Chap. 5, the solvents discussed were liquids, but solutions can also exist in solids. In single-crystal silicon (e.g., Si-wafers), the silicon is the *solvent*, and the impurities are the *solutes*. One important aspect of solutes in a solid-solvent that needs to be addressed here is *solid-solubility*. This is the maximum concentration an impurity can be dissolved under equilibrium conditions. (A familiar analogy is the maximum *liquid-solubility* of sugar in coffee. The coffee can only dissolve a certain amount of sugar before collecting in the bottom of the cup as a solid.) Figure 9-12a shows the solid-solubilities versus temperature for a variety of elements in silicon.[8]

For almost all impurities in silicon, solid-solubility decreases with decreasing temperature. Thus, if an impurity is introduced into silicon at a temperature at the maximum-concentration allowed by its solubility, and the crystal is then cooled to a lower-temperature, a *supersaturation-condition* is said to exist. The crystal ceases to be supersaturated and achieves equilibrium by precipitating the impurity-atoms in excess of the solubility-limit. While precipitates are generally undesirable, in some cases their presence can be a benefit. This is the case for oxygen-precipitates in silicon wafers, as covered in Sects. 9.9 and 9.10.

As noted above, solubility of the electrically-active impurities in silicon is also an important matter. In general, it is desired that the electrically-active impurities have a high solid-solubility in Si (e.g., $>10^{20}$/cm^{-3}), to allow a wide-range of resistivities to be

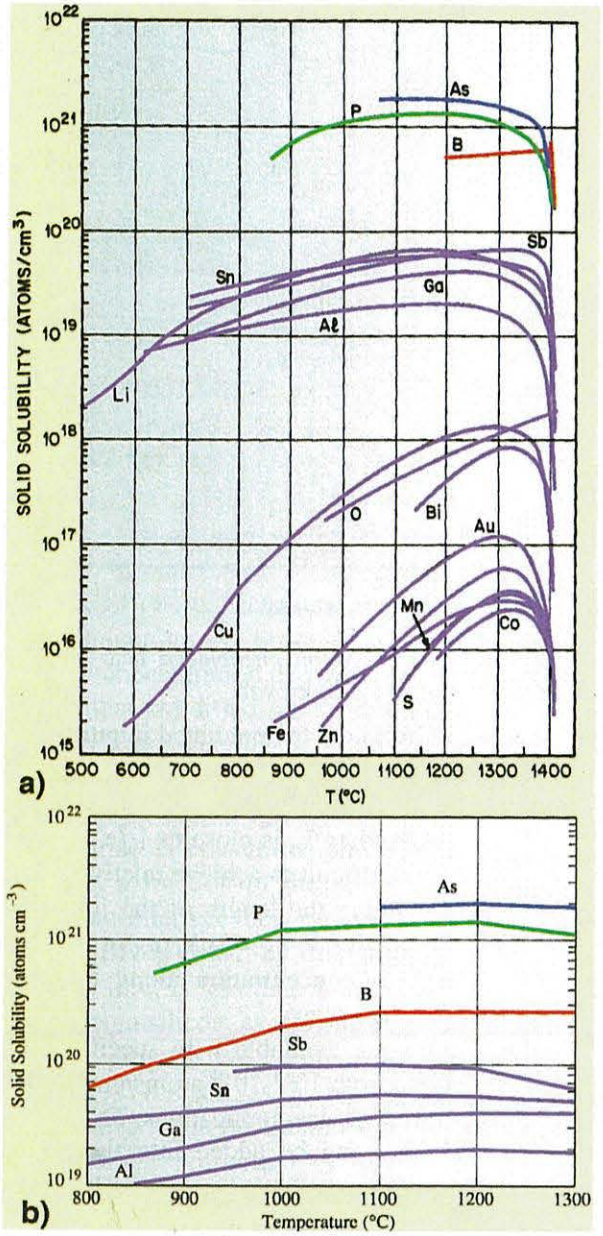


Fig. 9-12 (a) *Solid-solubility* of impurity elements in Si. (b) Details of the curves shown in (a) for the impurity dopants of Si.[8] Reprinted permission from Lucent Technologies.

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formed in the various regions of devices. However, as discussed earlier (and as shown in Fig. 9-12b), there are only a few electrically-active elements that have high solid-solubilities in silicon.

9.3.3 Czochralski-Silicon Growing Equipment

The systems used to grow Czochralski Si-crystals (also known as *pullers* (Figs 9-13 and 9-14), consist of four subsystems as shown in Fig. 9-13:

1. *Furnace*: crucible, susceptor, rotation mechanism, heater and power supply, & growth chamber.
2. *Crystal-pulling mechanism*: seed-cable or chain, rotation-mechanism, seed-chuck, and crystal-handling device.
3. *Ambient control:* chamber gas-source, flow controller, and vacuum/exhaust system.
4. *Control system:* computer-based controller, and sensors.

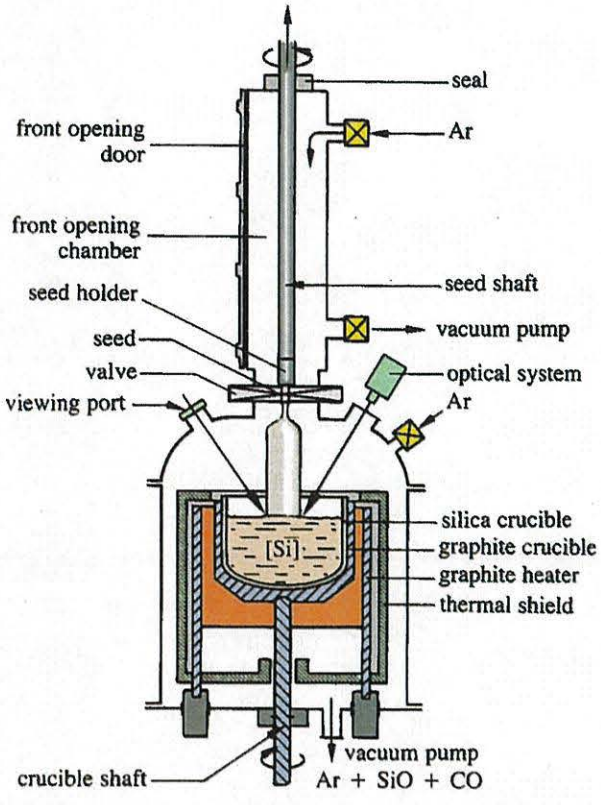


Fig. 9-13 Schematic drawing of CZ-ingot-puller.[4]

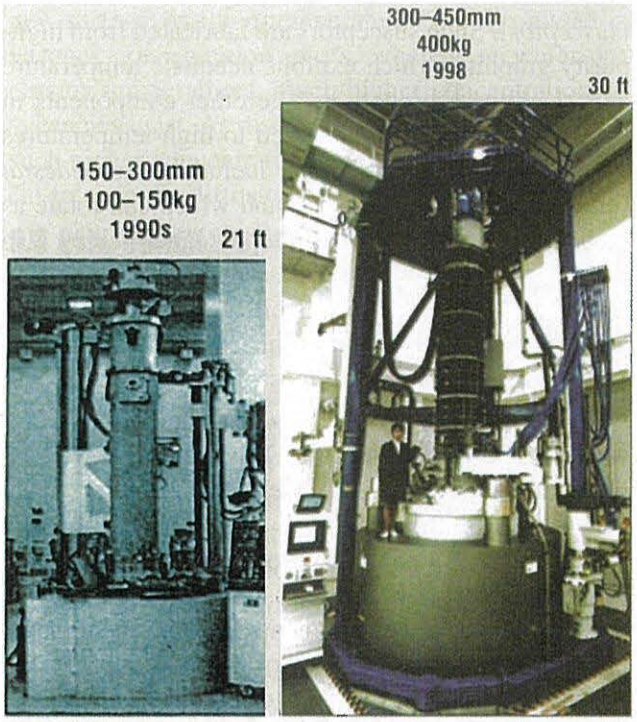


Fig. 9-14 (a) Modern CZ-pullers for 200-mm and 300-mm wafers. Courtesy of Ferrofluidics/Kayex.

Furnace: The material chosen for CZ-silicon crucibles is fused-silica. It has a high melting-point, good thermal-stability, and is relatively non-reactive with molten-silicon. The molten-silicon to some extent does corrode the fused-silica crucible, especially during the higher temperature melt-in period. Thus, substantial quantities of oxygen become dissolved into the melt. Some of this oxygen becomes incorporated into the crystal, initially taking the form of an interstitial-impurity. The presence of this oxygen can have potentially good and bad effects on the crystal properties. The purity of the crucible-silica is also important, since any impurities can limit the upper values of resistivity of ingots grown in the crucible (the levels of B and P in Si are typically 8–10 ppma). In addition, silica has no distinct melting-point, but gradually softens with increasing temperature.

Near the melting-point of silicon, the silica-material of the crucible becomes so soft that it requires the support of a heat-resistant and rigid outer-crucible

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(*susceptor*). Such susceptors are fabricated from high-purity graphite, which exhibits adequate temperature and cleanliness properties. The other components in the chamber that are subjected to high-temperatures are also made from graphite, including the *pedestal* (on which the susceptor sits, and which can rotate as well as raise or lower the susceptor [and thereby also the crucible and melt]), *heater elements*, *insulation,* and a *heat shield*. The silicon-charge is melted by graphite resistance-heaters connected to a power-supply. Large pullers require tens of kilowatts of power for operation.

Crystal-Pulling Mechanism: The mechanism which pulls the crystal from the melt (and simultaneously rotates it), must do this with minimal vibration and sufficient precision. Most systems use a cable or chain to pull the crystal. The hot-crystals have become too large to be manually handled. Thus, automated unloading-systems are used to transport ingots from the furnace to the cropping and evaluation areas.

Ambient Control: The environment in the chamber must be kept free of reactive-gases (O, CO, etc.). This is accomplished by filling the chamber with an inert-gas (e.g., Ar). During the process, this gas is swept out of the chamber, together with any CO and SiO that may be evolving in the chamber, and replaced with fresh inert-gas. A typical consumption-rate of inert-gas for this purpose is ~1500 liters/kg of silicon grown. Ingot-growth at a reduced-pressure in the chamber can also be used to alter evaporation from the melt.

Control System: The process-parameters, such as pull-rate, crucible-rotation, seed-rotation, melt-temperature, gas-flow, and crystal-diameter, are controlled in modern pullers with digital-computer systems. As mentioned earlier, completely automated cycles (one-button operation) require manual-intervention only for loading the crucible with EGS. Recipes that result in various crystal-properties are stored in the computer memory, allowing the system to produce nearly identical crystals from run-to-run. Other control-system features may include: central-computer interfacing capability, data-logging and printing, CRT terminals, and tape or magnetic-disk program storage.

Ingot-diameters during growth are controlled by focusing an infrared temperature-sensor on the melt-crystal interface, and monitoring changes of the meniscus-temperature. The pull-rate mechanism and chamber heater is slaved to the sensor-output, and the diameter is adjusted by changes in the pull-rate. The level of the melt is detected by laser-beam reflection.

9.4 CRYSTALLINE-DEFECTS IN SILICON

Real crystals differ from the ideal in that they possess *imperfections* or *defects*.[7] Some, due to impurity dopant-atoms, are absolutely necessary for creating devices in the crystal. Other defects may be helpful if present in moderate density. Most however, are undesirable, regardless of the density in which they are found in a crystal. Table 9-2 lists crystalline defects according to their geometry. There are *zero-dimensional* (or *point-defects*), *one-dimensional* (or *line-defects*), *two-dimensional* (or *area-defects*), and *three-dimensional* (or *volume-defects*), as shown in Fig. 9-15.

9.5 POINT-DEFECTS IN SILICON CRYSTALS

The various forms of zero-dimensional or point-defects are shown in Fig. 9-16. In crystal regions where no point-defects exist, each site on the lattice

Table 9-2 CRYSTALLINE-DEFECTS IN SILICON

Type	Dimension	Examples
Point	0	Vacancy, Interstitial, Frenkel Defects (Intrinsic - silicon self-interstitials) (Extrinsic - dopants, oxygen, carbon, metals)
Line	1	Straight Dislocations (edge or screw) Dislocation Loops
Area	2	Stacking-Faults Grain-Boundaries Crystal-Surfaces
Volume	3	Precipitates, Voids (Oxygen Precipitates, Metal Precipitates)

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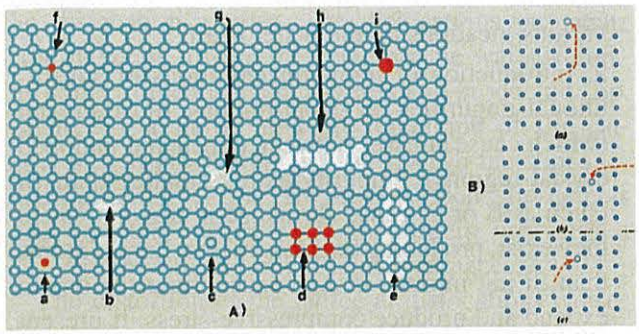


Fig. 9-15 (A) Various crystal defects in a simple-cubic lattice: (a) interstitial impurity-atom; (b) edge-dislocation; (c) self-interstitial; (d) coherent-precipitate of substitutional atoms; (e) dislocation-loop formed by agglomeration of self-interstitials; (f) substitutional-atom widening the lattice; (g) vacancy; (h) dislocation-loop formed by agglomeration of vacancies; (i) substitutional-impurity-atom compressing the lattice. (B) Point-defects: (a) Schottky-defect; (b) interstitial arriving from surface; (c) Frenkel-defect.

is occupied by an atom. If an atom is missing from one of these sites a *vacancy* exists in the lattice. In the event that an atom leaves a lattice site and *moves to the external surface* of the crystal, a *Schottky-defect* is created (Fig. 9-15Ba). That is, in a Schottky-defect a vacancy is created in the lattice, but the displaced atom does not remain in the bulk of the crystal. It moves instead to a location on its surface. If an atom is found at some non-lattice site in the crystal, it is said to lie at an *interstitial-site*. Silicon-atoms at interstitial-sites in a Si-crystal are called *self-interstitials*, and self-interstitial atoms may originate from a lattice-site in the crystal, or from the crystal-surface. Vacancies and self-interstitials are classified as *intrinsic point-defects*.

In any solid, lattice-atoms are in continuous vibration about their equilibrium positions. The amplitude of these vibrations increases as the temperature is raised and may become large enough for an occasional atom to leave its equilibrium-position entirely and move to a location at the surface (Schottky-defect). This requires energy to be supplied to the solid since the bonds holding the atom to its neighbors must be broken, and additional energy is also needed to create new surface. At room-temperature (300 K) only a tiny vacancy-concentration exists, whereas at wafer-processing temperatures, much-higher concentrations of vacancies exist. As discussed in more detail in Ref. 1, such higher concentrations of point-defects play critical roles in the diffusion of impurities in silicon.

9.6 ONE-DIMENSIONAL DEFECTS (DISLOCATIONS)

One-dimensional (or *line*) defects in crystals take the form of *dislocations*. They may be *edge*-dislocations, *screw*-dislocations, or *mixed*-dislocations (which contain both screw and edge components). Dislocations are an important class of defects in silicon crystals, and a full-treatment of their properties, formation, growth, and movement is a complex subject. Readers are directed to Ref. 1 for more details.

An *edge-dislocation* is shown in Fig. 9-17a. Note that the upper-half of the crystal contains an *extra half-plane* of atoms squeezed into the same space normally occupied by the atoms of an ideal crystal. The *dislocation* occurs at the termination of the sheet of extra-atoms. An edge-dislocation could be theoretically created by slicing the lattice and inserting an extra half-plane of atoms into the slice as shown in Fig. 9-17b. In the example shown in Fig. 9-17b stresses exist in the crystal as a result of the dislocation. The lattice planes in the upper-half of the lattice near the dislocation are in *compressive* stress, while those in the lower half are in *tensile* stress. The *dislocation line* in an edge-dislocation is the line connecting all

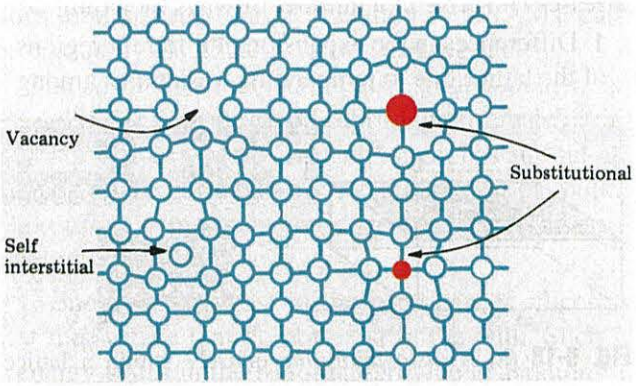


Fig. 9-16 Various *point-defects* in a simple-cubic lattice.

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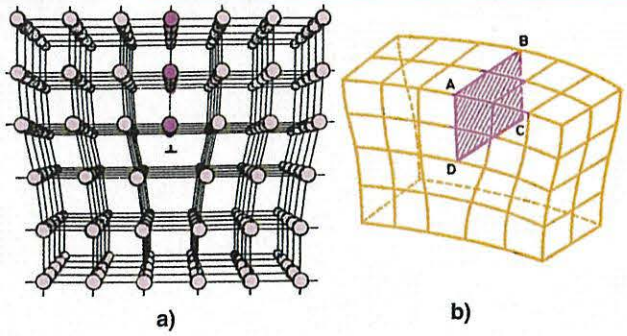


Fig. 9-17 (a) Model of an edge-dislocation. (b) Positive edge-dislocation formed by inserting an extra half-plane of atoms in ABCD.

the end-atoms on the extra half-plane.

The *dislocation-line* must either terminate on an external surface of the crystal (see Fig. 9-18 for example), or form a closed-curve if the dislocation lies entirely within the crystal (a *dislocation-loop*). That is, in a dislocation-loop an extra-plane of atoms (or a missing-plane of atoms) that exists entirely within the interior of the crystal must have a dislocation along the outer-edge of the plane (Fig. 9-18).

Dislocations can form during ingot-growth or can be introduced into Si wafers by subjecting them to various other non-equilibrium process-conditions. That is, dislocations can arise during thermal-processing by the growth and multiplication of the microscopic dislocation-loops formed during ingot cooling. They can also be generated from dislocations originating at the surface in response to stresses created in the wafers during later process-steps. Such stresses can arise in a number of ways including:

1. Differences in the expansion of different regions of the lattice due to temperature-variations among various locations on the wafer itself.

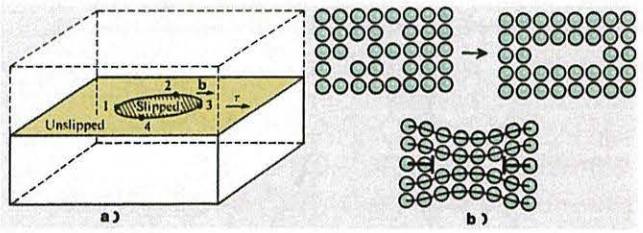


Fig. 9-18 (a) A *dislocation-line* entirely within a lattice, forming a closed loop. (b) Formation of a *dislocation-loop* by agglomeration and collapse of *vacancies*.

2. Introduction of high-concentrations of substitutional-impurities in local-regions of a crystal (which cause stresses between doped and undoped crystal-regions). Impurity-atoms smaller than Si (such as B or P) cause shrinkage in regions where they exist, producing tensile-stresses. Larger atoms than Si put into the crystal cause these regions to expand and produce compressive-stress. If present in high-enough concentrations, stresses caused by substitutional-impurities produce dislocations, and these are known as *misfit-dislocations*;

3. Compressive-stresses from volume mismatches that arise from the formation of SiO_2 precipitates in CZ-silicon.

4. Stresses caused by differences in the coefficient of thermal-expansion between a layer present on the surface and that of the crystal. An example is the stress caused during the formation of LOCOS isolation-structures. LOCOS-isolation involves the growth of thermal-oxide on local-regions of the wafer surface, and suppression of the oxidation on other areas (by the presence of nitride layers). Dislocation-causing stresses result from tensile-stress intrinsic to SiN, and from the volume-expansion of oxide formed in the field-regions.

Dislocations in *wafers* can be induced by thermal-stress during furnace-operations. Upon removing heated-wafers from a furnace, the edges of the wafers cool faster than their centers (especially when wafers are held vertically and spaced closely in wafer-boats). Wafer-edges radiate heat to the cooler surroundings while their centers are surrounded by the heated adjacent-wafers. The resultant temperature-difference from edge-to-center causes the edges to undergo relatively more contraction than the centers. If the induced-stress exceeds the *yield-strength* of the silicon, dislocations (seen as *slip-defects*) are formed.

The thermally-induced dislocations as a result of wafer-cooling upon being withdrawn from a furnace are generated at the wafer-edge, where surface irregularities and lattice-damage act preferentially as

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the dislocation-sources. The dislocations propagate from the edge toward the center of the wafer, relieving some of the mechanical-stress and producing slip. Figure 9-19a shows an *x*-ray topograph of slip-patterns in a <111> wafer, and Fig. 9-19b the slippage-distribution of 9-19a. To prevent such slip-defects (and resultant wafer-warpage), wafers are pushed very-slowly into and out of heated furnaces.

The distortion of the lattice at dislocations causes them to become sites that are energetically-favored to be occupied by impurity-atoms. That is, diffusing impurity-atoms are more likely to be *captured* at dislocation-sites because they distort the lattice less at such sites than elsewhere in a perfect-lattice. This results in a lower free-energy of the crystal. Impurity-atoms larger than Si occupy regions nearby the dislocation that are in compression, while those smaller than silicon locate in the tensile-stressed portions. In addition, there is also a chemically-active dangling-bond sticking out from each atom on the edge of a dislocation, which also helps trap impurities.

These phenomena are very important in silicon processing, as dislocations can trap fast-diffusing metal-impurities in silicon. The effect can either be harmful to device operation - or if correctly harnessed - can be used to advantage (that is, through the intentional application of gettering techniques, see Sect 9.10). When impurities have segregated themselves at dislocation-sites, the dislocation is said to be *decorated* with them, while *pure* dislocations are free of any impurities.

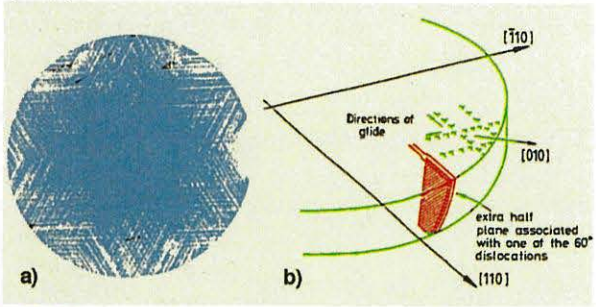


Fig. 9-19 (a) A (111)-oriented Si wafer in which the severe slip has been delineated by etching to show the emergence of the dislocations. (b) Schematic of the slippage-distribution of (a).

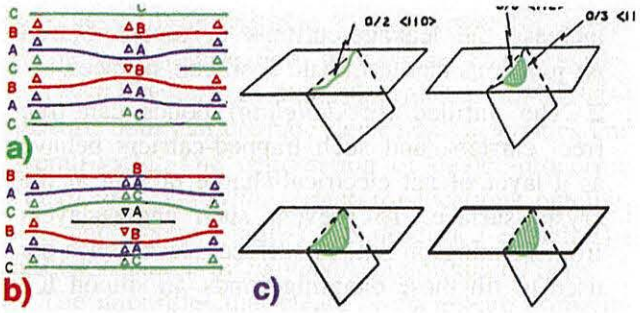


Fig. 9-20 (a) Intrinsic and (b) extrinsic-stacking-faults in a FCC lattice. (c) Generation of an extrinsic-stacking-fault from a dislocation at a surface.

9.7 AREA-DEFECTS IN SILICON CRYSTALS

Area-defects in single-crystals include *stacking-faults*, *crystal-surfaces themselves*, and *grain-boundaries*.

Stacking-faults are the most important area-defects that degrade the device-performance of integrated-circuit components. As shown in Fig. 9-20a, the removal of an extra-plane of Si-atoms creates an *intrinsic* stacking-fault, while the insertion of an extra-plane creates an *extrinsic* stacking-fault (Fig. 9-20b). Dislocations formed during oxidation are known as *oxidation-induced stacking-faults* (OISF). Stacking-faults cause problems in silicon-devices because they are bounded by dislocations, and fast-diffusing impurities from the surrounding lattice can be absorbed at these dislocations. Various device-degrading effects are caused when such stacking-faults become electrically-active as the result of absorbing metallic-impurities. For example, excess reverse-bias currents in *pn*-junctions, and storage-time degradation in DRAMs, can be caused by electrically-active stacking-faults.

The *surface* of a crystal is also an area-defect, as the periodicity of the lattice abruptly terminates at a surface. Thus, a surface-atom no longer has all four of the nearest-neighbors that it would have in the bulk. There are two important consequences of such disruptions in lattice-periodicity.

1. Energy-states exist in the band-gap of silicon at the surface that do not exist in the bulk. Such energy-states in the band-gap provide generation-recombination (g-r) centers for carriers, which

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increase the leakage-currents in reverse-biased *pn*-junctions that terminate at silicon-surfaces.

2. The unfilled (or *dangling*) bonds can trap free- carriers, and such trapped-carriers behave as a layer of net electrical-charge present at the crystal-surface. To prevent such charge-layers from forming on silicon surfaces, techniques are used to fill these dangling-bonds. In silicon IC-processing the most important of these techniques involves the growth of thermal-SiO_2 on the wafer-surface (which is effective in satisfying the vast majority of such bonds), together with hydrogen-annealing to tie up as many as possible of those bonds remaining after SiO_2 growth.

Grain-boundaries are another important area-defect (Fig. 9-21). Si-atoms with only three nearest neighbors are more chemically-reactive than those having all-four bonds completed. They are also more prone to trap free-carriers or to attach an impurity-atom to complete their last unfilled-bond. This makes silicon

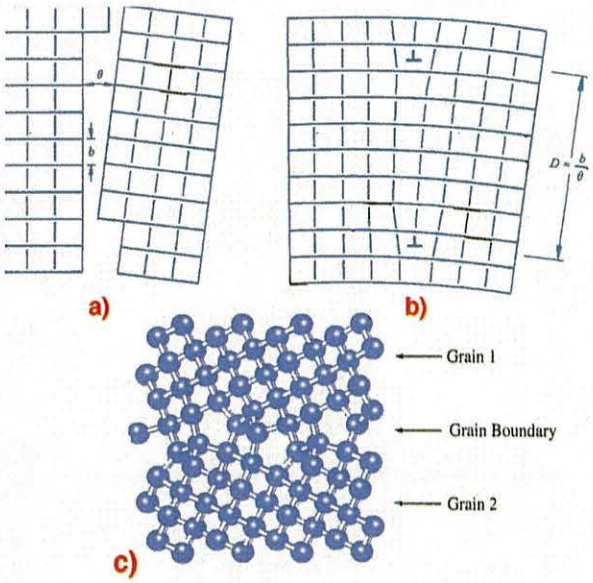


Fig. 9-21 Dislocation model of grain-boundary. Two grains with an angle of misorientation θ are shown in (a). As the two grains form a wedge-shaped intersection, certain rows of atoms cannot extend their full lengths and the dislocation (b) results. (c) 3-D perspective drawing of grain-boundary.

with many grain-boundaries (i.e., polySi films) full of sites that can: **1**) trap mobile-carriers originating in the bulk-regions of the crystal-grains; or **2**) segregate electrically-active impurities from the bulk to the grain-boundaries. The electrical-conductivity of poly-Si is significantly impacted by the extent to which grain-boundaries exist in such films (see Chap. 16).

It is also easier for substitutional-impurities to move along grain-boundary diffusion-paths than along diffusion-paths in the bulk for two reasons. The grain-boundary region is a more open structure that enhances the diffusivity of impurities. Also, fewer bonds must be broken by an impurity-atom to enable it to diffuse if located on a grain-boundary site than if it occupies a site in the bulk-crystal. Grain-boundary diffusion thus allows uniform distribution of dopants in polySi-films to be achieved at lower-temperatures than in single-crystal layers. Grain-boundary diffusion is also an important phenomenon in other polycrystalline-films encountered in IC fabrication, including Al, Ti, WSi_X, and TiN films (see Chap. 15).

9.8 BULK-DEFECTS AND PRECIPITATION

Bulk (or volume) defects in crystals include *voids* and *local amorphous-regions*, but the most important volume defects are *precipitates* of extrinsic or intrinsic point-defects. The formation and growth of precipitates is a complex subject, but basically precipitates first form (or *nucleate*) as tiny-particles called *nuclei*. The nature of the structure of such nuclei is difficult to determine because they are so small.

The nucleation process in a solid-lattice happens in one of two ways: **a**) *heterogeneous-nucleation*, which involves nucleation at a *crystalline-defect* of the lattice, such as a dislocation, grain-boundary, or impurity; and **b**) *homogeneous-nucleation*, which involves the formation of nuclei by a random assembly of solute-atoms in an otherwise *defect-free crystal-lattice*. In the latter case, the solute-atoms coincidentally cluster at some location, thereby forming a *nucleus*. Homogeneous-nucleation is more likely when a large supersaturation of solute-atoms exists in the crystal. In addition, the more-rapidly solute-atoms can dif-

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fuse, the more-quickly will precipitation take place. In dislocation-free Si-ingots and starting-wafers, homogeneous-nucleation is the dominant nucleation-mechanism of bulk (i.e., three-dimensional) defects.

9.9 OXYGEN IN SILICON

Other than in heavily-doped crystals, the most abundant impurity in Czochralski (CZ) Si crystals is oxygen, with concentrations ranging from 4.5×10^{17}-1×10^{18} atoms/cm^3 (9–20 ppma). Oxygen is incorporated into CZ-Si as a result of crucible-erosion during CZ growth. The majority of the oxygen (~95%) in the as-grown crystal is atomically-dissolved and occupies interstitial-sites. The diffusivity of oxygen is moderately-high, whereas its solubility decreases strongly at lower-temperatures (see Fig. 9-12a). These two properties make oxygen the most-important precipitate-forming element in CZ-silicon. Precipitation-behavior impacts all of the important effects influenced by the presence of oxygen in silicon: including: **a**) *surface oxygen-precipitates*; and **b**) *bulk oxygen-precipitates* (that are the basis of intrinsic-gettering).

The presence of SiO_2-precipitates near the wafer-surface degrades the quality of thin gate-oxides and causes oxygen-induced stacking-faults (which can induce device failures by excessive leakage-currents). Such SiO_2-precipitates must be eliminated from regions near the wafer-surface. The procedure employed to prevent oxygen-precipitates from forming near the wafer-surface involves the creation of a *denuded-zone*, or a zone that contains less interstitial-oxygen than required to form oxygen-precipitates (Fig. 9-22). Special thermal-steps at the beginning of a wafer-fabrication run are used to form such denuded-zones.

Bulk oxygen-precipitates can act as sites that trap fast-diffusing metallic-impurities *(gettering-sites)*, and thus their presence can be used as a helpful effect. Such oxygen-precipitates can be created in bulk-silicon containing appropriate oxygen-levels, through the use of a sequence of thermal-steps. Details about this process are found in Ref. 1.

9.10 GETTERING

Unwanted crystalline-defects and impurities can be introduced during silicon crystal-growth or subsequent wafer-fabrication processes. The presence of crystalline-defects and impurities is undesirable because both can degrade device-characteristics and overall-yield. The degradation of device-properties by *extended crystalline-defects* (dislocations, precipitates, and stacking-faults) was described earlier. The problems caused by *impurities* are discussed here.

The impurities that create problems are primarily metals, and include Cu, Ni, Au, and Fe. These metallic-impurities are highly-mobile and diffuse long distances in Si-crystals at moderate process-temperatures. Thus, there is high-probability they will migrate to extended defect-sites, and be captured there by them. Extended-defects in device-regions of a wafer

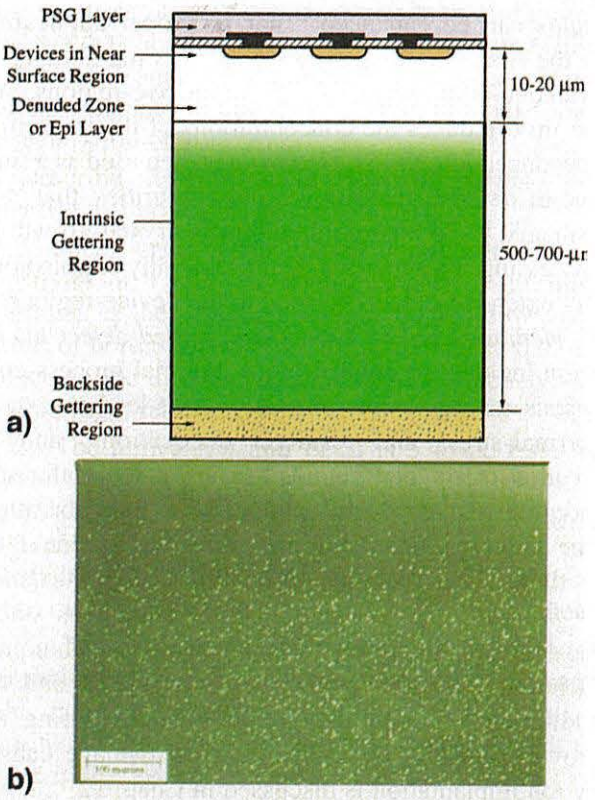


Fig. 9-22 a) Wafer-gettering strategies showing a *surface-denuded-zone, intrinsic-gettering-region,* and *backside-gettering*.[9] (b) SEM photograph of a cross-section of a Si wafer with a denuded-zone at the surface and oxygen-precipitates in the bulk (Courtesy of MEMC).

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which capture metal-impurities give rise to larger leakage-currents and lower breakdown voltages.

Eliminating the effects of impurities and defects involve four approaches: **1**) keep new extended-defects from forming; **2**) prevent extended-defects from occurring in the device-regions; **3**) keep metallic impurities from getting into the wafer; and **4**) stop any metallic-impurities that have gotten in from ending-up in device-regions (Fig. 9-23). Technique-**4** is referred to as *gettering,* a term originally used to describe the process in which an appropriate material (such as cesium), was used to getter (remove) the last traces of gas in vacuum-tubes, so that the required high-vacuums within the glass tube could be attained.

By combining the four approaches, product-yields can be enhanced. That is, proper application of the first-two approaches minimizes the number of extended-defects that exist in the active-regions, and the third reduces the concentrations of the impurities introduced into the Si. *Gettering* is then used as a final line-of-defense to remove any impurities that still managed to be incorporated during crystal-growth or processing. This reduces their probability of poisoning any extended-defects formed in the device-regions.

Methods used to suppress extended-defect nucleation include: **a**) control of the thermal process-conditions during wafer fabrication that lead to excess thermal-stress and resultant dislocations; and **b**) creation of oxygen denuded-zones at the wafer-surface regions in which active-devices are fabricated. The latter procedure eliminates oxygen-precipitates in these device-regions. *Elimination of pre-existing or process-induced extended-defects* such as stacking-faults, is achieved by using various techniques, including elevated temperatures (>1200°C) and the addition of HCl to the growth-ambient during the growth of SiO_2. Healing crystalline-damage caused by ion implantation is discussed in Chap. 12.

The use of Technique-**3**, namely *the control of unwanted-impurities* (especially metals), involves identification and removal of the sources of contamination. Some examples of contaminant-sources that have been identified include: **a**) stainless-steel fixtures in ion-implanters that ended up being sputtered during the ion-implant process; **b**) impurities originating from the sputtering of chamber-walls and fixtures of reactive-ion-etching systems; **c**) the diffusion of heavy-metals from the heater-coils through the fused-silica walls of diffusion-furnaces; and **d**) release of transition-metals (e.g., Fe and Ti) by the SiC-coated susceptors of epitaxial-reactors.

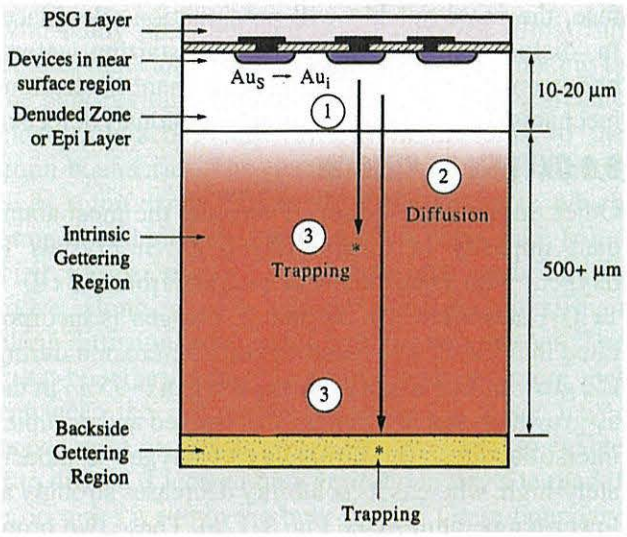


Fig. 9-23 Three-step gettering process: (1) release; (2) diffusion; and (3) trapping. (Gold [Au] is used as an example of the impurity being gettered.)[9] Used with permission.

9.10.1 Basic Gettering Principles

Gettering removes transition-metal impurities from device-regions by 3 steps (Fig. 9-23):

1. The metal-impurities to be gettered are released into solid-solution from any stable-precipitate form they have assumed.
2. They then diffuse through the silicon.
3. They are then "captured" at a position away from the device-regions by either: **a**) the formation of chemical-pairs (e.g., Fe-B pairs) with other impurities, such as boron present in the crystal, or **b**) deliberately created extended-defects (dislocations or precipitates). Metal-impurities are prevented from being released into the wafer during subsequent heat-treatment.

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Gettering processes are divided into two categories: extrinsic and intrinsic. *Extrinsic-gettering* exploits damage or stress on the surface of the silicon-wafer. This creates extended-defects or chemically-reactive sites at which the mobile-impurities are captured. Normally such sites are generated on the backside of bare starting-wafers using ion-implant damage or the deposition of a polysilicon-layer. *Intrinsic-gettering* involves localizing-impurities at extended-defects or regions of high-concentration of electrical-impurities (such as boron) which exist within the bulk-material of the Si-wafer, and whose origin is due to an "intrinsic" property of the starting-wafer, such as its oxygen or boron content acquired during CZ crystal-growth. More details on gettering are found in Refs. 1 and 2..

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PROBLEMS

1. Why is it necessary to use single-crystal wafers on which to build microchips?

2. List 5 advantages that silicon has over other semiconductor materials.

3. Define a *unit-cell.* Draw a cubic unit-cell, and the <100> and <111> planes of the cubic lattice. Show atoms present on a <110>-plane of an FCC unit cell.

4. Describe the operation of a crystal puller. Why do wafers made with CZ process contain large concentrations of oxygen, while those made with FZ do not?

5. A CZ grown crystal is doped with boron. Why is the boron-concentration higher at the tail-end of the ingot than at the seed-end?

6. The equation that gives the impurity concentration along the length of a CZ ingot C_s is given as:

$$C_s = k_o C_o (1- X)^{k_o-1}$$

where k_o is the segregation-coefficient (see Table 9-1), X is the melt-fraction that has solidified, and C_o is the initial impurity-concentration in the melt. Using this equation, plot the doping distribution of: (a) arsenic; and (b) phosphorus, at distances of 20, 40, 60, 80, and 90 cm from the seed-end of a 100-cm long ingot that has been pulled from a melt with an initial doping concentration of 10^{16} cm^{-3}.

7. Describe the differences between *extrinsic* and *intrinsic* gettering.

8. A silicon crystal doped with boron is to have a resistivity of 4.0 Ω-cm when one half of the ingot is grown. If the Si charge weighs 60 kg, how many grams of boron-doped Si with a resistivity of 0.02-Ω-cm should be introduced into the melt to achieve the desired ingot resistivity?

9. (a) The *lattice-constant* of Si is 5.43-Å. Find the nearest-neighbor distance in a diamond-lattice having this lattice-constant. (b) Calculate the density of Si from the lattice constant, the atomic weight, and Avogadro's number. Compare the results with those given on the Table found on the back book-endsheet.

10. Si has an atomic-density of $5x10^{22}$ atoms/cm^3. For this problem, assume they are packed in a simple cubic-lattice structure (and not in a diamond lattice) with $5x10^{19}$ As atoms/cm^3 uniformly distributed. (a) What is the average-spacing between Si atoms? (b) How many atoms would lie on the outermost layer (a monolayer), (c) What would be the average spacing between As atoms?

11. Explain why a dislocation must terminate on itself or on a surface (or on a volume-defect).

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