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I served as Chief Examiner of the certified court interpreter test for the State of California and as a contract translator and interpreter for various federal agencies through the U.S. Department of State for more than a decade. I served as an instructor at the University of California at Berkeley and the Middlebury Institute of International Studies at Monterey (MIIS) Graduate Program in Translation.

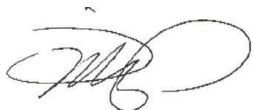
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I certify under penalty of perjury that the foregoing is true and correct.

Executed this 20th day of November 2024 in Contra Costa County of the State of California.

By:



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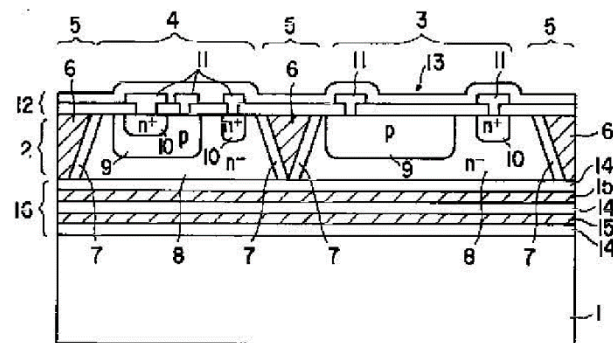
(54) [Title of the Invention] SEMICONDUCTOR LIGHT RECEIVING ELEMENT AND METHOD OF MANUFACTURING THEREOF

(57) ABSTRACT
PROBLEM

To provide a semiconductor light receiving element that is integrated using a dielectric isolation method and exhibits high light receiving efficiency in the infrared region, and a manufacturing method thereof.

RESOLUTION MEANS

Semiconductor light receiving elements that are mutually dielectrically isolated can be obtained by forming on a semiconductor substrate a multi-reflection film where films having a first refractive index and films having a second refractive index are alternately laminated, bonding an element layer and a semiconductor substrate via the multi-reflection film, forming a plurality of element regions by applying the dielectric isolation method to the element layer, and forming the light receiving elements and the like on these element regions. The multi-reflection film insulates the semiconductor substrate and the element layer from each other, while at the same time, reflects incident light onto the light receiving element formed in the element region so as to be incident on the light receiving element again, thereby equivalently doubling the thickness of the element layer and obtaining a semiconductor light receiving element that exhibits high light receiving efficiency even in the infrared region where the absorption coefficient of silicon is low.



- | | | |
|--|---------------------------|------------------------------|
| 1 : Silicon substrate | 6 : Polysilicon | 11 : Electrode |
| 2 : Element layer | 7 : SiO ₂ film | 12 : Passivation film |
| 3 : Element region (light receiving element) | 8 : n ⁺ layer | 13 : Light receiving surface |
| 4 : Element region (transistor) | 9 : p-type layer | 14 : SiO ₂ film |
| 5 : Dielectric isolation | 10 : n ⁺ layer | 15 : Polysilicon film |
| | | 16 : Multi-reflection film |

What is claimed is:

[Claim 1] A semiconductor light receiving element formed in an element layer on a semiconductor substrate, wherein the element layer includes a multi-reflection film in which a film having a first refractive index and a film having a second refractive index are alternately stacked at an interface with the semiconductor substrate; and the multi-reflection film insulates and isolates the element layer from the semiconductor substrate, reflects the transmitted light transmitted through the semiconductor light receiving element formed on the element layer, and impinges the reflected light again on the semiconductor light receiving element.

[Claim 2] A semiconductor light receiving element formed in an element layer on a semiconductor substrate, wherein the element layer includes a plurality of element regions mutually separated by a dielectric film, provided on the semiconductor substrate; wherein the plurality of element regions further include a multi-reflection film in which a film having a first refractive index and a film having a second refractive index are alternately laminated at an interface with the semiconductor substrate; and the multi-reflection film insulates and isolates the element region and the semiconductor substrate, reflects the transmitted light transmitted through the semiconductor light receiving element formed on the element layer, and impinges the reflected light again on the semiconductor light receiving element.

[Claim 3] The semiconductor light receiving element according to claim 2, wherein the dielectric film is made of a multi-reflection film in which a film having a first refractive index and a film having a second refractive index are alternately laminated.

[Claim 4] The semiconductor light receiving element according to any one of claims 1, 2, or 3, wherein the film having the first refractive index is made of a polycrystalline semiconductor, and the film having the second refractive index is made of a dielectric body.

[Claim 5] The semiconductor light receiving element according to claim 4, wherein the polycrystalline semiconductor is made of one of either silicon or germanium, and the dielectric body is made of one of SiO_2 , Si_3N_4 , SiO_x ($1 \leq x \leq 2$), SiN_x ($1 \leq x \leq 1$), SiO_xN_y ($1 \leq x + y \leq 2$), PSG, BSG, BPSG, Al_2O_3 , AlN, (Ba, Sr) TiO_3 , TiO_2 , and Ta_2O_5 .

[Claim 6] The semiconductor light receiving element according to any one of claims 1, 2, or 3, wherein the films having the first and second refractive indexes are each made of one of the following materials: SiO_2 , Si_3N_4 , SiO_x ($1 \leq x \leq 2$), SiN_x ($1 \leq x \leq 1$), SiO_xN_y ($1 \leq x + y \leq 2$), PSG, BSG, BPSG, Al_2O_3 , AlN, (Ba, Sr) TiO_3 , TiO_2 , and Ta_2O_5 ; and the film having the second refractive index is made of a material different from the film having the first refractive index.

[Claim 7] A method of manufacturing a semiconductor light receiving element, comprising the steps of: forming a multi-reflection film by alternately laminating SiO_2 films and polycrystalline silicon films on a first main surface of a first silicon substrate; bonding a first main surface of a second silicon substrate to a surface of the SiO_2 film or the polycrystalline silicon film which constitutes a final film of the multi-reflection film in

clean air;

increasing the bonding strength by heat treating the bond; and removing a certain thickness from a second main surface of the second silicon substrate that has been subjected to the above step, and further polishing the surface to form an element layer of a prescribed thickness.

[Claim 8] A method of manufacturing a semiconductor light receiving element, comprising the steps of: forming a multi-reflection film by alternately laminating SiO_2 films and polycrystalline silicon films on one main surface of a first silicon substrate;

polishing a surface of the polycrystalline silicon film which is the final film of the multi-reflection film;

bonding a first main surface of a second silicon substrate and the surface of the surface-polished polycrystalline silicon film in clean air;

increasing the bonding strength by heat treating the bond; and removing a certain thickness from a second main surface of the second silicon substrate that has been subjected to the above step, and further polishing the surface to form an element layer of a prescribed thickness.

[Claim 9] A method of manufacturing a semiconductor light receiving element, comprising the steps of:

forming a first multi-reflection film by alternately laminating SiO_2 films and polycrystalline silicon films on one main surface of a first silicon substrate;

forming a second multi-reflection film by alternately laminating SiO_2 films and polycrystalline silicon films on one main surface of a second silicon substrate;

making a final film of the first multi-reflection film of a SiO_2 film;

making the final film of the second multi-reflection film of a polycrystalline silicon film;

bonding the surface of the SiO_2 film and the surface of the polycrystalline silicon film in clean air;

increasing the bonding strength by heat treating the bond; and removing a certain thickness from a first or second main surface of the second silicon substrate that has been subjected to the above step, and further polishing the surface to form an element layer of a prescribed thickness.

[Claim 10] The manufacturing method of a semiconductor light receiving element according to claim 9, wherein the surface of the polycrystalline silicon film forming the final film is surface polished.

DETAILED DESCRIPTION OF THE INVENTION

[0001]

TECHNICAL FIELD OF THE PRESENT INVENTION

The present invention relates to a semiconductor light receiving element, and more particularly to a semiconductor light receiving element that exhibits high light receiving efficiency in the infrared region, and a method for manufacturing the same.

[0002]

CONVENTIONAL TECHNOLOGY

Conventionally, a stand-alone light receiving element formed on a silicon substrate was configured to efficiently absorb the energy of incident light into the silicon substrate by making the silicon substrate sufficiently thick to generate electron-hole pairs within the silicon substrate, thereby achieving high light receiving efficiency.

[0003] However, for example, if an attempt is made to arrange an array of light receiving elements on a silicon substrate, or to integrate light receiving elements and optical signal amplification transistors on the same substrate to form an optical integrated circuit, the introduction of element isolation technology becomes indispensable.

[0004] Generally, p-n junction isolation, which is easy to form, is often used as an element isolation method for integrated circuits. However, in the case of an optical integrated circuit, if light is incident on the p-n junction for isolating elements, the reverse-biased p-n junction exhibits photoconductivity, and therefore cannot fulfill the role of isolating elements.

Therefore, a dielectric isolation method, in which an element region on a silicon substrate is surrounded by an insulating film such as SiO₂, must be used in order to isolate elements in an optical integrated circuit.

[0005] In recent years, silicon wafer bonding technology has been developed to enable mutual bonding of silicon substrates via a SiO₂ film. A method has been developed in which the silicon wafer bonding technology is combined with a dielectric isolation method where a dielectric film is embedded in a trench or V-groove, in order to electrically isolate element regions into islands.

[0006] However, this method has certain restrictions on the depth of the trench or V-groove due to problems in processing technology, so the thickness of the element layer cannot be made sufficiently thick, and the thickness of the element layer capable of achieving dielectric isolation is limited to a range of at most 10 μ m to 20 μ m.

[0007] FIG. 6 is a cross-sectional view of a semiconductor light receiving element for an optical integrated circuit, which is manufactured using conventional silicon wafer bonding technology. The semiconductor light receiving element depicted in FIG. 6 includes a silicon substrate 1, an element layer 2 in which an element is formed, an element region 3 for forming a light receiving element in the element layer, and an element region 4 in which a transistor for amplifying a received light signal is formed. Hereinafter, 3 and 4 are collectively referred to as element regions.

[0008] The dielectric isolation region 5 between the element regions 3 and 4 is formed by embedding polysilicon 6 in a V-groove with a SiO₂ film 7 or the like interposed therebetween as a dielectric body. The dielectric isolation does not necessarily have to use a V-groove, but a method of forming a trench or the like and filling the trench with a dielectric material such as SiO₂ may also be used.

[0009] The light receiving element is formed by using an n⁻ layer 8 of the element layer 2, a p-type layer 9, and an n⁺ layer 10 for making an n-side contact. The p-n⁻-n⁺ structure including elements 9, 8 and 10 constitutes a pin type light receiving element. The n⁺ layer 10 is used as an emitter diffusion layer, a collector contact layer and p-type layer 9 are used as a base region, and an n⁻-type layer 8 is used as a collector region in the element region 4 forming the transistor.

[0010] Reference numeral 11 denotes electrodes of the light receiving element and the transistor, and 12 denotes a passivation film which covers the electrodes and the wiring connecting the electrodes. The passivation film can also serve as an antireflection film on the light receiving surface 13.

[0011] In the conventional optical integrated circuit depicted in FIG. 6, a silicon substrate 1 and an element layer 2 are bonded via a dielectric film such as a SiO₂ film 14, and after bonding, a manufacturing process using normal dielectric isolation is applied as is to form the light receiving elements and transistors in the element regions 3 and 4 of the element layer 2, respectively.

[0012] As described above, in this case, the thickness of the element layer is limited to a range of 10 μ m to 20 μ m due to restrictions on dielectric isolation, so the light in the infrared region, where the optical absorption coefficient of silicon is relatively small, that is incident from the light receiving surface 13 is not sufficiently absorbed by the element layer 2, and passes through the SiO₂ film 14, and is absorbed by the thick silicon substrate 1 to generate electron-hole pairs.

[0013] The electron-hole pairs thus generated in the silicon substrate 1 are blocked by the SiO₂ film 14 and cannot reach the light receiving element, and therefore disappear without being converted into electrical energy. Therefore, in order to increase the light receiving efficiency of the light receiving element, the element layer must be made thicker to increase the light absorption rate of the element layer.

[0014] Herein, the wavelength dependence of light absorption in silicon will be considered with reference to FIG. 7. The horizontal axis of the graph represents the depth from the silicon surface, the vertical axis represents the light absorption rate of silicon, and the parameters of each curve depicted at the bottom of the graph represent the wavelength of light. At a wavelength of 660 nm in the visible region, the absorptance of silicon with a thickness of 10 μ m or more exceeds 95%, so a light receiving element formed in an element layer with a thickness of 10 μ m to 20 μ m exhibits high light receiving efficiency. However, at a wavelength of 950 nm or more in the infrared region, a 10 μ m thick element layer does not provide sufficient light absorption.

[0015] For example, when using a GaAs light emitting element that is a representative infrared light emitting element in the infrared region and exhibits high light emitting efficiency at a wavelength of 940 nm as the light source, even if the thickness of the element layer is increased to 20 μ m, the light absorption rate by the silicon is approximately 30%, and most of the incident light is transmitted through the SiO₂ film 14 and absorbed by the silicon substrate 1, as seen from FIG. 7, resulting in a significant decrease in the light receiving efficiency of the light receiving element.

[0016]

PROBLEM TO BE SOLVED BY THE INVENTION

As described above, in conventional light receiving elements using silicon wafer bonding technology, the element regions are mutually separated by a dielectric isolation method in which a dielectric body is embedded in a V-groove or trench, so the thickness of the element layer must be thinned to about 10 μ m to 20 μ m. This poses the problem of a significant decrease in light receiving efficiency in the infrared region.

[0017] In light of the foregoing, an object of the present invention is to provide a light receiving element that exhibits sufficiently high light emitting efficiency in the infrared region, even when the thickness of the element layer is in a range of 10 μ m to 20 μ m.

[0018]

MEANS FOR SOLVING THE PROBLEM

The semiconductor light receiving element of the present invention is a semiconductor light receiving element formed in an element layer on a semiconductor substrate, wherein the element layer includes a multi-reflection film in which a film having a first refractive index and a film having a second refractive index are alternately stacked at an interface with the semiconductor substrate; and the multi-reflection film insulates and isolates the element layer from the semiconductor substrate, reflects the transmitted light transmitted through the semiconductor light receiving element formed on the element layer, and impinges the reflected light again on the semiconductor light receiving element.

[0019] Furthermore, the semiconductor light receiving element of the present invention provides that the element layer includes a plurality of element regions mutually separated by a dielectric film, provided on the semiconductor substrate; wherein the plurality of element regions further include a multi-reflection film in which a film having a first refractive index and a film having a second refractive index are alternately laminated at an interface with the semiconductor substrate; and the multi-reflection film insulates and isolates the element region and the semiconductor substrate, reflects the transmitted light transmitted through the semiconductor light receiving element formed on the element layer, and impinges the reflected light again on the semiconductor light receiving element.

[0020] Preferably, the dielectric film that mutually isolates the element regions is made of a multi-reflection film in which a film having a first refractive index and a film having a second refractive index are alternately laminated.

[0021] More preferably, the film having the first refractive index is made of a polycrystalline semiconductor, and the film having the second refractive index is made of a dielectric material. Preferably, the polycrystalline semiconductor is made of one of either silicon or germanium, and the dielectric body is made of one of SiO_2 , Si_3N_4 , SiO_x ($1 \leq x \leq 2$), SiN_x ($1 \leq x \leq 1$), SiO_xN_y ($1 \leq x + y \leq 2$), PSG, BSG, BPSG, Al_2O_3 , AlN, (Ba, Sr) TiO_3 , TiO_2 , and Ta_2O_3 .

[0022] Preferably, the films having the first and second refractive indexes are each made of one of the following materials: SiO_2 , Si_3N_4 , SiO_x ($1 \leq x \leq 2$), SiN_x ($1 \leq x \leq 1$), SiO_xN_y ($1 \leq x + y \leq 2$), PSG, BSG, BPSG, Al_2O_3 , AlN, (Ba, Sr) TiO_3 , TiO_2 , and Ta_2O_3 ; and the film having the second refractive index is made of a material different from the film having the first refractive index.

[0023] The method of manufacturing a semiconductor light receiving element of the present invention includes the steps of: forming a multi-reflection film by alternately laminating SiO_2 films and polycrystalline silicon films on a first main surface of a first silicon substrate; bonding a first main surface of a second silicon substrate to a surface of the SiO_2 film or the polycrystalline silicon film which constitutes a final film of the multi-reflection film in clean air; increasing the bonding strength by heat treating the bond; and removing a certain thickness from a second main surface of the second silicon substrate that has been subjected to the above step, and further polishing the surface to form an element layer of a prescribed thickness.

[0024] Furthermore, the method of manufacturing a semiconductor light receiving element of the present invention

includes the steps of: forming a multi-reflection film by alternately laminating SiO_2 films and polycrystalline silicon films on one main surface of a first silicon substrate; polishing a surface of the polycrystalline silicon film which is the final film of the multi-reflection film; bonding a first main surface of a second silicon substrate and the surface of the polycrystalline silicon film in clean air; increasing the bonding strength by heat treating the bond; and removing a certain thickness from a second main surface of the second silicon substrate that has been subjected to the above step, and further polishing the surface to form an element layer of a prescribed thickness.

[0025] Furthermore, the method of manufacturing a semiconductor light receiving element of the present invention includes the steps of: forming a first multi-reflection film by alternately laminating SiO_2 films and polycrystalline silicon films on one main surface of a first silicon substrate; forming a second multi-reflection film by alternately laminating SiO_2 films and polycrystalline silicon films on one main surface of a second silicon substrate; making a final film of the first multi-reflection film of a SiO_2 film; making the final film of the second multi-reflection film of a polycrystalline silicon film; bonding the surface of the SiO_2 film and the surface of the polycrystalline silicon film in clean air; increasing the bonding strength by heat treating the bond; and removing a certain thickness from a first or second main surface of the second silicon substrate that has been subjected to the above step, and further polishing the surface to form an element layer of a prescribed thickness. Preferably, the surface of the polycrystalline silicon film forming the final film is surface polished.

[0026]

DESCRIPTION OF THE EMBODIMENTS FOR PRACTICING THE INVENTION

An embodiment of the present invention is described below in detail with reference to the drawings. FIG. 1 is a diagram depicting the structure of a silicon light receiving element according to a first embodiment of the present invention. It should be noted that the same reference numerals are used to designate parts corresponding to those in FIG. 6, and detailed descriptions thereof will be omitted.

[0027] The difference from a conventional structure is that a multi-reflection film 16 is formed between the silicon substrate 1 and the element layer 2, in which SiO_2 films 14 and polysilicon films 15 are alternately laminated. Herein, impurities are preferably not added to the polysilicon film 15, in order to prevent absorption of light by free electrons or holes.

[0028] In this manner, by forming the multi-reflection film 16 between the element layer 2 forming the light receiving element and the silicon substrate 1, optimizing the thicknesses of the SiO_2 film 14 and the polysilicon film 15 for the wavelength of the incident light from the light receiving surface 13, almost 100% of the incident light passing through the element layer 2 can be reflected by the multi-reflection film 16. When light is incident perpendicularly on the multi-reflection film 16, the reflectance R_{2N+1} of the multi-reflection film is given by the following equation (1).

[0029]

[Equation 1]

$$R_{2N+1} = \left(\frac{1 - \left(\frac{n_2}{n_1}\right) \left(\frac{n_2}{n_1}\right) \left(\frac{n_2}{n_3}\right)^{2N}}{1 + \left(\frac{n_2}{n_1}\right) \left(\frac{n_2}{n_1}\right) \left(\frac{n_2}{n_3}\right)^{2N}} \right)^2 \text{----- (1)}$$

[0030] Herein, N represents the number of repetitions of the double film made of SiO₂ and polysilicon, n₁ represents the refractive index of the silicon constituting the element layer 2, n₂ and n₃ represent the refractive indexes of the SiO₂ film 14 and the polysilicon film 15, respectively, and n₁ represents the refractive index of the silicon substrate 1.

[0031] If the thicknesses of n₁ and n₁ are both infinite, the thicknesses of n₂ and n₃ are d₂ and d₃, and the wavelength of incident light in air is λ₀, the film thicknesses of the SiO₂ film 14 and the polysilicon film 15 are set to establish the relationship n₂ · d₂ = n₃ · d₃ = λ₀/4. The result of formula (1) indicates that the reflectance R_{2N+1} approaches 100% as N increases, and as the refractive index ratio n₂/n₃ of the double film constituting the multi-reflection film decreases.

[0032] FIG. 2 depicts the relationship between the number of repetitions N and the reflectance R_{2N+1} for the multi-reflection film 16 made of the SiO₂ films 14 and the polysilicon films 15. For example, a reflectance of 90% or more can be obtained by optimizing the thickness of the layers, including a total of five layers including three SiO₂ layers and two polysilicon layers. It should be noted that when N=2, or in other words, when there are two layers of SiO₂ and two layers of polysilicon, the reflectance does not reach 90%, but when there are three layers of SiO₂ films, the reflectance will be 90% or more.

[0033] As depicted in FIG. 6, in a light receiving element using conventional silicon wafer bonding technology, the SiO₂ film 14 was provided simply to insulate the element layer 2 from the silicon substrate 1 so that the transmitted light that passed through the element layer from the light receiving surface 13 further passes through the SiO₂ film 14 and is absorbed by the silicon substrate 1, and thus the reflection by the SiO₂ film 14 was negligibly small.

[0034] As depicted in the first embodiment, the reflectance of the multi-reflection film 16 can be increased to 90% or more, which can be considered to be an unexpectedly great effect, by replacing the conventional insulating film containing one SiO₂ film 14 with a multi-reflection film 16 configured of three SiO₂ film layers and two polysilicon film layers alternately stacked as depicted in FIG. 1.

[0035] The process of laminating a SiO₂ film and a polysilicon film has a proven track record in the manufacture of semiconductor integrated circuits, and a major advantage of this process is thought to be that there are no processing problems.

[0036] In this manner, the transmitted light that enters the light receiving element from the incident surface 13 and passes through the element layer 2 is almost completely reflected by the multi-reflection film 16 and passes through the element layer 2 again, thereby effectively improving the light receiving efficiency to the same extent as if the thickness d of the element layer were 2d.

[0037] In addition, the improvement in light receiving efficiency is due to light reflection, so not only is an effect of simply doubling the thickness of the element layer provided, but the generation of electron-hole pairs by reflected light

occurs closer to the depletion layer of the light receiving element than when light is incident on an element layer that is twice as thick, so the time required for the electron-hole pairs to diffuse into the depletion layer can be significantly reduced.

[0038] In other words, it is noteworthy that an improvement in the light receiving efficiency and an improvement in the operating speed of the integrated silicon light receiving element are simultaneously achieved by interposing the multi-reflection film 16 of the present invention between the silicon substrate 1 and the element layer 2.

[0039] Regarding the improvement of the light receiving efficiency, for example, when a GaAs infrared light emitting element with a wavelength of 940 nm is used as the light source, if the thickness of the element layer is 20 μm, the light absorption effect of silicon for a round trip of 40 μm is effectively achieved, and therefore the absorptance of incident light in the element layer 2 can be improved to approximately 70%. In other words, the light receiving efficiency can be easily increased to more than twice that of a conventional configuration.

[0040] As described above, the operating speed of the light receiving element is also greatly improved at this time, so if the multi-reflection film 16 of the present invention is used between the silicon substrate 1 and the element layer 2, the gain-bandwidth product of the light receiving system of the optical integrated circuit including the light receiving element and the amplifying transistor can be greatly improved.

[0041] In addition, when a GaAlAs light emitting element with a wavelength of 880 nm is used as a light source, the light absorption rate of a light receiving element using the silicon wafer bonding technique of the conventional structure depicted in FIG. 6 was about 60% when the thickness of the element layer 2 was 20 μm. However, if the light receiving element structure having the multi-reflection film 16 of the present invention depicted in FIG. 1 is used, the light absorption rate can be improved to about 90%.

[0042] Next, a method for manufacturing a silicon light receiving element according to a second embodiment of the present invention will be described with reference to FIG. 3. The structure of the light receiving element of the present invention is characterized in that the silicon substrate 1 and the element layer 2 are bonded together via a multi-reflection film 16. After good bonding has been achieved, a conventional dielectric isolation process using a V-groove or trench or the like can be used as is. Therefore, the following embodiment will focus on and describe in detail only this bonding process.

[0043] As depicted in FIG. 3(a), a SiO₂ film 14 formed by thermal oxidation and a polysilicon film 15 formed by CVD (Chemical Vapor Deposition) are alternately deposited on a silicon substrate 1. As described above, the thickness of the film at this time differs depending on the wavelength range used by the light receiving element, and is set such that the product of the film thickness and the refractive index is ¼ of the wavelength of light in air.

[0044] Needless to say, better results can be obtained if the film growth method uses MOCVD (Metal-Organic Chemical Vapor Deposition) or MBE (Molecular Beam Epitaxy), which have high controllability of film thickness.

[0045] When growing the SiO₂ film 14 on the silicon substrate 1, the surface of the silicon substrate 1 is preferably cleaned. However, good results can be obtained by simply using the polished surface of a wafer purchased with normal specifications as a silicon wafer for mass production.

[0046] The element layer 2 depicted in FIG. 3(a) is a silicon wafer before bonding, and has a polished surface 2a of a wafer having the same specification as the silicon substrate 1. The SiO₂ bonding surface 14a of the final SiO₂ film 14 formed in the above process and the polished surface 2a of the element layer 2 are bonded together. At this time, favorable results can be obtained by cleaning the polished surface 2a of the element layer 2, which is to be the bonding surface, with a hydrophobic etching solution, and the adhesive surface 14a of the SiO₂ film 14 on the substrate 1 with a hydrophilic etching solution.

[0047] As depicted in FIG. 3B, the silicon substrate 1 and a silicon wafer that will become the element layer 2 are bonded together in a clean environment of class 10 or less. Herein, class 10 or less means a cleanliness level where the number of particles with a size of 0.5 μm or less per 1 ft³ is 10 or less, and favorable results can be obtained by working on a clean bench placed in a normal semi-clean room. In this case, bringing into close contact refers to simply bringing the bonding surfaces into close mutual contact without applying any particular pressure.

[0048] After bonding the silicon substrate 1 and the silicon wafer that will become the element layer 2 via the multi-reflection film 16, the members are heat-treated in an oxidizing atmosphere at a temperature of 800°C to 1100°C for one hour or more to increase the adhesive strength. The oxidizing atmosphere herein refers to a mixed gas of oxygen and nitrogen, or a hydrogen combustion oxidizing atmosphere in which a small amount of hydrogen is mixed into oxygen.

[0049] An SiO₂ film 14b is formed on each of the surfaces of the silicon substrate 1 and the element layer 2 opposite to the bonding surface by using an oxidizing atmosphere, so the stress generated on the front and back of each wafer during heat treatment is balanced, and warping of the wafer can be significantly reduced even when a large wafer is used.

[0050] The bonded state depicted in FIG. 3(b) obtained in this manner is extremely strong, so the unnecessary thickness of the silicon wafer that will become the element layer 2 can be easily removed using a grinder down to the cutting surface 17 of the grinder.

[0051] The cut surface 17 of the grinder contains many scratches and defects, and semiconductor elements cannot be formed on that surface. Therefore, CMP (Chemical-Mechanical Polishing) is further performed to remove material down to the CMP polished surface 18. In this manner, the element layer 2 having a thickness of 10 μm to 20 μm is formed on the multi-reflection film 16 on the silicon substrate 1.

[0052] Subsequently, the processes of forming the dielectric isolation region 5 in the element layer 2 and forming the light receiving element and the transistor for amplifying the optical signal can be performed by directly using the manufacturing process of a semiconductor integrated circuit using normal dielectric isolation technology.

[0053] Next, a method for manufacturing a silicon light receiving element according to a third embodiment of the present invention will be described with reference to FIG. 4. The third embodiment is characterized in that the uppermost layer of the multi-reflection film formed on the silicon substrate is a thick polysilicon film, and this thick polysilicon film and the element layer are bonded together.

[0054] In other words, a multi-reflection film 16 containing three layers of SiO₂ films 14 and two layers of polysilicon films 15 is formed on a silicon substrate 1 in the same manner as in the first embodiment. Subsequently, a final layer polysilicon film 19 thicker than polysilicon film 15 is formed.

[0055] When a polysilicon film is formed by a CVD method, the smoothness of the surface is usually lost during the polycrystallization process, and thus the surface is likely to have extremely fine irregularities (cloudy surface). When the polysilicon film 15 containing these fine irregularities and the SiO₂ film 14 are laminated, the smoothness of the surface of the SiO₂ film 14 may be lost, depending on the growth conditions.

[0056] At this time, as depicted in FIG. 3A, if the element layer bonding surface 2a is bonded to the final SiO₂ bonding surface 14a which has lost smoothness, voids may occur at the interface, adversely affecting the yield of the bonding process.

[0057] To avoid this problem, in the third embodiment, as depicted in FIG. 4, a thick polysilicon film 19 is formed as the final layer, and fine irregularities are removed by CMP polishing.

[0058] The smoothed CMP polished surface 20 and the adhesive surface 2a of the element layer 2 are then surface-treated with a hydrophilic or hydrophobic cleaning solution, and then bonded in a clean atmosphere. A strong adhesive state can be obtained by heat-treating the surface at 800°C to 1100°C for one hour or more.

[0059] In this case, there is no difference in refractive index between the final layer polysilicon film 19 and the element layer 2 made of single crystal silicon, so the fact that the thickness of the polysilicon film 19 is different from the thickness of the polysilicon film 15 of the multi-reflection film 16 has no effect on the reflectance of the multi-reflection film 16. For example, no problems will arise even if some error occurs in the parallelism between the CMP polished surface 20 and the multi-reflection film 16 due to CMP polishing.

[0060] Next, a method for manufacturing a silicon light receiving element according to a fourth embodiment of the present invention will be described with reference to FIG. 5. In the fourth embodiment, a multi-reflection film having a higher reflectance is formed between the silicon substrate 1 and the element layer 2, so there is an advantage of increasing the number of layers of the multi-reflection film.

[0061] For example, when forming a seven-layer multi-reflection film including four SiO₂ layers and three polysilicon layers, if all of the layers are formed on the silicon substrate 1, the distortion caused by the multi-reflection film may become excessive, causing the silicon substrate 1 to warp, which may reduce the bonding yield with the element layer 2.

[0062] In this case, as depicted in FIG. 5, the above-mentioned warpage problem can be significantly alleviated if a multi-reflection film is formed separately on the polished surface of the upper part of the silicon substrate 1 and on the polished surface of the lower part of the silicon wafer constituting the element layer 2, and the surface 14a of the central SiO₂ film is bonded to the CMP polished and cleaned surface 23 of the polysilicon film 15.

[0063] At this time, there is a risk that the thickness of the final polysilicon film 15 formed on the element layer 2 may deviate from the design value of the multi-reflection film due to an error occurring in the CMP polished surface 23. However, in this case, FIG. 5 depicts that an additional polysilicon film 21 and an additional SiO₂ film 22 are further added to provide the total five-layer multi-reflection film depicted in FIG. 3, and thus the overall reflectivity can be increased.

[0064] Note that the present invention is not limited to the aforementioned embodiment. For example, in the first embodiment, the multi-reflection film 16 was formed between the silicon substrate 1 and the element layer 2, but the present invention is not necessarily limited to this case. If the SiO₂ film 7 in the element isolation region 5 is also a multi-reflection film, the film can be used as a part of the reflection surface when scattered light is incident from the incident surface 13.

[0065] In the second to fourth embodiments, the method of forming a multi-reflection film containing a SiO₂ film and a polysilicon film mainly by the CVD method has been described. However, if the MOCVD method or the MBE method is used, the accuracy of the film thickness can be improved and the smoothness of the multi-reflection film can be improved. Furthermore, if plasma technology is used in

combination to make the polysilicon film amorphous and provide means for use as a structural element of the multi-reflection film, the smoothness of the polysilicon film can be further improved and the CMP polishing process for the bonding surface can be eliminated.

[0066] Furthermore, in the first to fourth embodiments, a polysilicon film is used as the film having a high refractive index. However, the present invention is not limited to polysilicon films. For applications in a longer wavelength region, a germanium film can be used in the same manner, as depicted in Table 1. For applications in a wider wavelength region, films made of compound semiconductor materials having various band gaps can be used for the same purpose. In this case, the silicon substrate 1 and the element layer 2 may be made of germanium or a compound semiconductor.

[0067] In the first to fourth embodiments, the film having a high refractive index is not necessarily limited to a semiconductor material, but may be, for example, any one of Si₃N₄, Al₂O₃, TiO₂, Ta₂O₅, (Ba,Sr) TiO₃, and the like as depicted in Table 1, and may be combined with a film having a low refractive index, such as SiO₂, PSG (Phospho-Silicate-Glass), or BSG (Boro-Silicate-Glass).

[0068] Other dielectric materials that can be used for this purpose include SiO_x (1 ≤ x ≤ 2), SiN_x (1 ≤ x ≤ 1), SiO_xN_y (1 ≤ x + y ≤ 2), BPSG (Boro-Phospho-Silicate-Glass), AlN, and the like. [0069] Furthermore, although the present invention has been described as being applied to a pin-type light receiving element, naturally, the present invention can also be applied to a normal p-n junction type light receiving element, a phototransistor, or a photoconductive element that does not have a pn junction. Additionally, various other modifications can be implemented without departing from the fundamental gist of the present invention.

[0070]

[Table 1]

Material Name	Refractive index
Si	3.5
Ge	4.0
SiO ₂	1.43~1.46
Si ₃ N ₄	1.96
Al ₂ O ₃	1.7
PSG	1.45~1.48
BSG	1.45~1.48
TiO ₂	1.96~2.6
Ta ₂ O ₅	1.77
(Ba,Sr)TiO ₃	2.3

[0071]

EFFECT OF THE INVENTION

As described above, when attempting to form an integrated semiconductor light receiving element using silicon wafer

bonding technology, conventionally, a silicon substrate and an element layer are bonded via a SiO₂ film, and light receiving elements and the like are formed in this element layer.

Therefore, the element regions in which these elements are formed must be mutually isolated using a dielectric isolation method in which a dielectric body is embedded in a V-groove, trench, or the like. Therefore, the thickness of the element layer must be thinned to about 10 μm to 20 μm , which poses the problem that the light receiving efficiency of the integrated semiconductor light receiving element drops significantly in the infrared region where the light absorption coefficient of silicon is low.

[0072] With the semiconductor light receiving element and the manufacturing method of the present invention, a multi-reflection film is formed by alternately stacking, for example, polysilicon films and SiO_2 films instead of the SiO_2 film conventionally used as an insulating film between the silicon substrate and the element layer, and the silicon substrate and the element layer are bonded via the multi-reflection film, thereby mutually insulating the films, and at the same time, the incident light of the light receiving element formed in the element layer is reflected by the multi-reflection film, effectively doubling the thickness of the element layer, and thereby enabling a light receiving element to be achieved that exhibits sufficiently high light emitting efficiency in the infrared region, even when the thickness of the element layer is in the range of 10 μm to 20 μm .

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view depicting a structure of an integrated semiconductor light receiving element according to a first embodiment of the present invention.

FIG. 2 is a graph depicting the relationship between the number of repetitions of the multi-reflection film of the present invention and the reflectance.

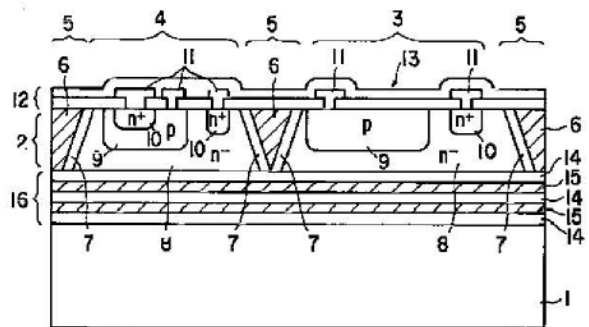
FIG. 3 is a diagram depicting a silicon wafer bonding method used in forming a semiconductor light receiving element according to a second embodiment of the present invention.

FIG. 4 is a diagram depicting a silicon wafer bonding method used in forming a semiconductor light receiving element according to a third embodiment of the present invention. FIG. 5 is a diagram depicting a silicon wafer bonding method used in forming a semiconductor light receiving element according to a fourth embodiment of the present invention. FIG. 6 is a cross-sectional view depicting the structure of a conventional integrated semiconductor light receiving element. FIG. 7 is a graph depicting the relationship between the depth from the silicon surface and the optical absorptance, using wavelength as a parameter.

DESCRIPTION OF REFERENTIAL NUMERALS

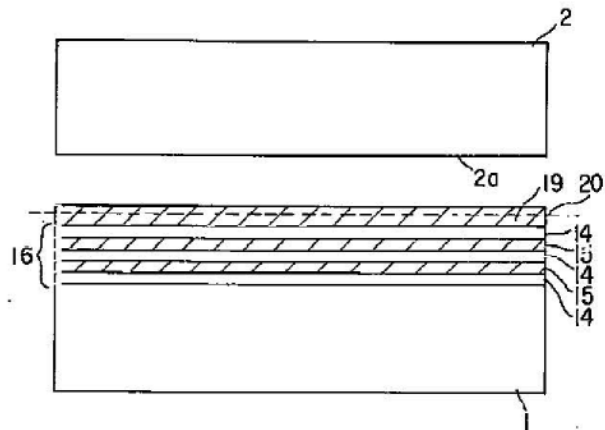
1. Silicon substrate
2. Element layer
- 2a. Element layer bonding surface
3. Element region (light receiving element)
4. Element region (transistor)
5. Dielectric isolation region
6. Polysilicon
7. SiO_2 film
8. n^- layer
9. p-type layer
10. n^+ layer
11. Electrode
12. Passivation film
13. Light receiving surface
14. SiO_2 film
- 14a. SiO_2 bonding surface
- 14b. SiO_2 film
15. Polysilicon film
16. Multi-reflection film
17. Grinder cutting surface
- 18, 20, 23. CMP polished surface
19. Thick polysilicon film
21. Additional polysilicon film
22. Additional SiO_2 film

[FIG. 1]



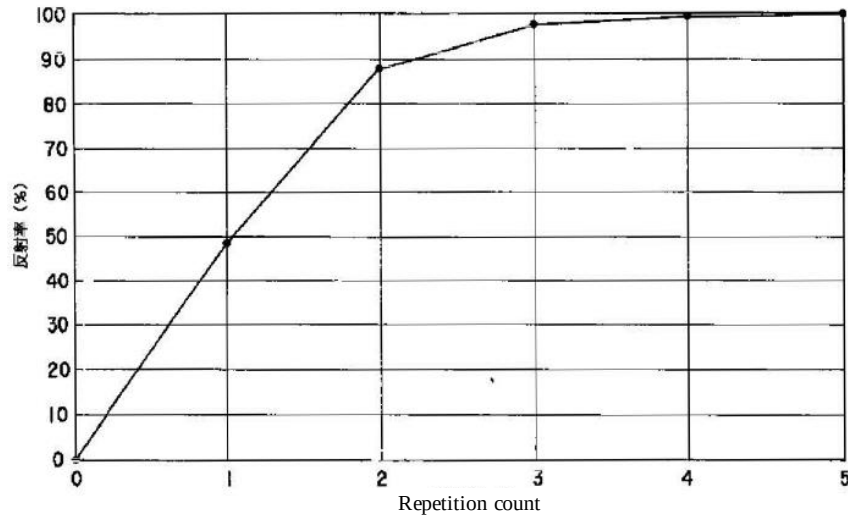
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|--|-------------------------|------------------------------|
| 1 : Silicon substrate | 6 : Polysilicon | 11 : Electrode |
| 2 : Element layer | 7 : SiO_2 film | 12 : Passivation film |
| 3 : Element region (light receiving element) | 8 : n^- layer | 13 : Light receiving surface |
| 4 : Element region (Transistor) | 9 : p-type layer | 14 : SiO_2 film |
| 5 : Dielectric isolation | 10 : n^+ layer | 15 : Polysilicon film |
| | | 16 : Multi-reflection film |

[FIG. 4]

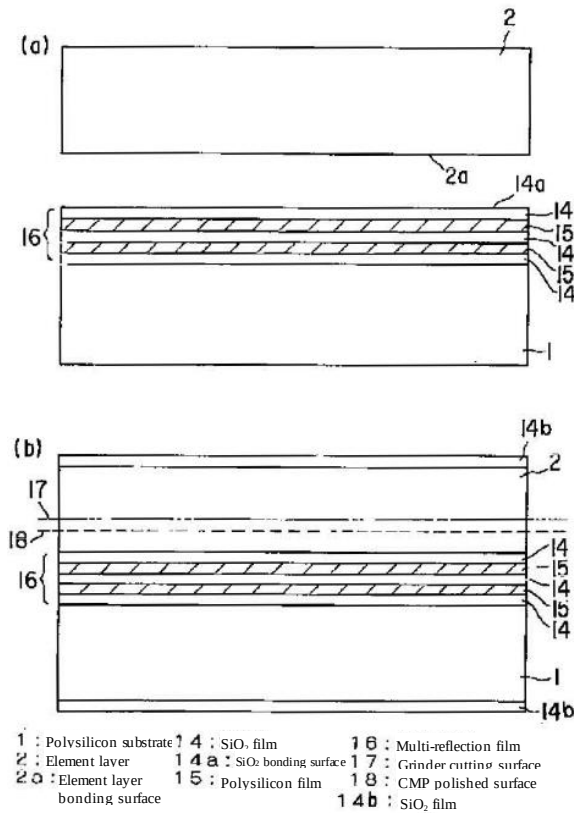


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|------------------------------------|--------------------------------------|--------------------------------|
| 1 : Silicon substrate | 14 : SiO_2 film | 16 : Multi-reflection film |
| 2 : Element layer | 14a : SiO_2 bonding surface | 19 : Floating polysilicon film |
| 2a : Element layer bonding surface | 15 : Polysilicon film | 20 : CMP polished surface |

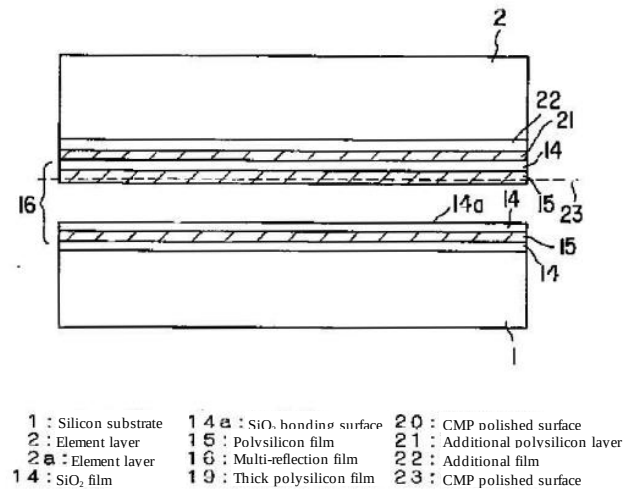
[FIG. 2]



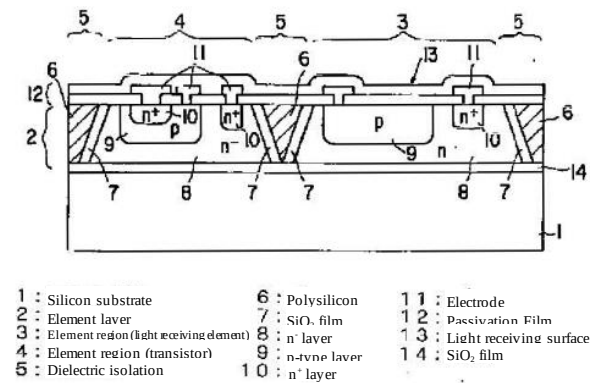
[FIG. 3]



[FIG. 5]



[FIG. 6]



[FIG. 7]

