

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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Samsung Electronics Co., Ltd.,  
Petitioner,

v.

SiOnyx, LLC,  
Patent Owner.

Case No. IPR2025-00165  
Patent No. 9,905,599

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**DECLARATION OF MICHAEL LEBBY IN SUPPORT OF PETITION FOR  
*INTER PARTES* REVIEW OF U.S. PATENT NO. 9,905,599**

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## **I. INTRODUCTION**

1. I, Michael Lebby, declare as follows.

2. I have been retained as a technical consultant on behalf of Samsung Electronics Co., Ltd., (“Samsung” or “Petitioner”), which I understand to be the petitioner in the present proceeding. I have been asked to consider whether the references listed as Exhibits 1006-1011 below disclose or render obvious the limitations recited in claims 1-36 of U.S. Patent No. 9,905,599 (Ex-1001, “’599 patent”). I have also been asked to consider the state of the art and the “prior art,” i.e., references, available before the time of the alleged invention of the ’599 patent. My opinions are provided in this declaration.

3. I am being compensated at my standard consulting rate for my time. My compensation is in no way contingent on the results of these or any other proceedings relating to the ’599 patent.

## **II. BACKGROUND AND QUALIFICATIONS**

4. A description of my professional background and qualifications is provided below. An additional account of my work experience and qualifications is included in my *curriculum vitae*, which is Ex-1004 (“CV”).

5. I am currently the CEO and CTO at GenusTechnik Inc., which provides consulting services in areas that include image sensors, photonics, optoelectronics, semiconductors as used in image sensors and other optical applications.

6. In addition, I am currently the Chairman, CEO, and Director of the Board of Directors for Lightwave Logic. As CEO, I successfully guided Lightwave Logic to up-list to NASDAQ in September 2021 organically (i.e., without the raising of financing), and I led the company to acceptance in the Russell 3000 index in 2022.

7. I have led and run optoelectronics start-ups, and I have commercialized optoelectronic and photonics technologies into volume manufacturing. I have also worked as a Corporate Venture Capitalist specializing in optical communications, photonics, sensing, electronics, and semiconductors, and I am currently a technical expert advising the European Commission regarding evaluation of numerous photonic technology proposals, including image sensor proposals. I am a Fellow Member of the National Academy of Inventors (NAI), the IEEE, and Optica (OSA), and I was voted Photonic Integrated Circuit (PIC) business leader of the year by the PIC International Conference in 2018.

8. In particular, my technical expertise has included the design of components for photonics technology that can source light as well as receive and detect light. These components include LEDs, ICs, lasers, photodetectors, diodes, image sensors, etc. In many of my industrial and commercial roles in the photonics industry I have used, designed, optimized, and improved photonic materials, components, and packages both through solutions of engineering problems as well as patents and publications.

9. Over the course of my career in photonics, optoelectronics, and optical technology in general, I have worked in nearly every aspect of the field, including optical assembly, laser diodes, photodetectors, image sensors, LEDs, integrated circuits (e.g. drivers, and other basic electronic digital and analog functions), as well as fiber optics. In particular, I have designed optoelectronic devices such as LEDs, laser diodes (VCSELs – vertical cavity surface emitting lasers), photodiodes, image sensors, and solar cells with a focus on efficient optical device design that maximizes device performance. For example, I have worked on improving light extraction efficiency in laser diodes as well as LEDs, where these devices are utilized in modules. I have also worked on arrays of detectors for sensing applications.

10. I started my career in 1977 at the Ministry of Defense (United Kingdom), in the Royal Electrical and Mechanical Engineers as a telecommunications apprentice. At the Ministry of Defense, I studied material and characterization issues relating to Gallium Arsenide (GaAs) and Indium Phosphide (InP) optoelectronic devices, as well as semiconductor device design, fabrication, and characterization, particularly with materials using III-V semiconductors. I also worked with silicon for integrated circuits, silicon photonics, and ceramic-based radio-frequency (RF) electronic packaging that included low-temperature co-fired ceramic. These devices and materials were utilized in photonic-based transceiver packages and modules. I also worked on electronics, motors, sensors, and other technologies that combined photonics with electronics.

11. I attended the University of Bradford, where I obtained a Bachelor's of Engineering (Electrical Engineering), with honors, in 1984, an MBA in 1985 and a Ph.D. (Electrical Engineering) in 1987. My Ph.D. thesis related to the characterization and fabrication of both optoelectronic and electronic semiconductor devices that included the detection of light. In 2004, I was awarded a Doctor of Engineering (a Doctorate degree higher than a Ph.D.) from the University of Bradford for my "Technical Contributions to Optoelectronics." This was only the second time in the University of Bradford's history that a Doctor of Engineering was granted based on industry experience.

12. While attending the University of Bradford and for a few years thereafter, i.e., from 1985 to 1989, I worked as a researcher in the Photonics Research Department of AT&T Bell Labs ("Bell Labs"). At Bell Labs, I focused my research on novel device designs using III-V semiconductor material systems including FETs, bipolar transistors, LEDs, laser diodes, and photodetectors. My research at Bell Labs became the subject of my Ph.D. thesis.

13. After completing my Ph.D. at the University of Bradford and my work at Bell Labs, I became a Research and Development Manager ("R&D Manager") in the photonics division of Motorola's Corporate R&D Labs ("Motorola"). I worked at Motorola from 1989 to 1998, where my responsibilities included research and development in optical interconnects, electrical and fiber optic connectors,

optical/electrical engines, electronic ICs, displays, laser devices, LEDs, optical lenses, image sensors, and optical waveguides, as well as the packaging and reliability of mobile product prototypes. Some of the prototypes on which I worked included moving parts with motors (both standard as well as semiconductor MEMs based), and phased array optical beams that could direct and re-direct optical beams. While at Motorola, I was the inventor or co-inventor on over 150 utility patents, and I received a special award from the Chairman of Motorola in 1998 for exemplary patent accomplishments. At that time, I had the highest number of issued utility patents in the history of Motorola.

14. As an R&D Manager at Motorola, I initiated Motorola's work in optical interconnect technology (known at Motorola as "Optobus"<sup>TM</sup>) and associated optical connectors, electronics, and photonics components, and I was also involved in research and development on the IC chip designs that this parallel interconnect module utilized. In this project, transparent plastics were developed and molded onto standard metallic lead frames for both light-emitting devices (e.g., LEDs, VCSELs) and photodetectors, which collect light and convert it into an electronic signal. These transparent lead frame packages were developed in volume production at Motorola. I also worked on various techniques to improve both photonics based detectors such as photodetectors, image sensors as well as photonics based emitters such as lasers and LEDs, both as individual components as well as in arrays of multiple components.

15. In 1998, I left Motorola to join TE Connectivity (previously Tyco Electronics) as Director of Technology and Business Development. In that role, I helped develop technology strategy for optical communications, optoelectronic transceivers, and fiber optic connector and adapter products for the Global Optoelectronics Division. My work included designing and characterizing photodetectors, sensors, LEDs, laser-based photonic packages and modules for product manufacturing.

16. In 1999, I joined Intel Capital (“Intel”) as Director of Business Development and as a corporate investor. My work at Intel included sourcing, negotiating, and closing private placement equity deals in the optical networking, photonic component, interconnect, optical lens, image sensor, and semiconductor industries. My work at Intel also included investigating the investment of Intel Capital equity in photonic devices, optical beams, and other technologies to support the physical movement of optical signals. I also was one of the founders of Intel’s silicon photonics division, which worked to establish a fabrication facility in South San Jose to investigate silicon based image sensors and the integration of silicon FET electronics with optoelectronics into the same silicon semiconductor wafer.

17. From 2005 to 2010, I served as the Executive Director, President, and CEO of the Optoelectronic Industry Development Association (OIDA) – a trade association that represented photonics manufacturers in the fields of photonic sensing,

fiber optics, display, defense, aerospace, LED lighting and automotive/motor vehicles.

I was responsible for organizing technical conferences, workshops and forecasts using industry roadmaps, all of which featured a portfolio of photonics technology that included: optical sensors, free-space optics, optical interconnects, fiber optics, optical communications, automotive photonic technologies, wavelength division multiplexing, LEDs, displays and their associated packaging.

18. In 2010, I became the General Manager and CTO of Translucent, Inc., a start-up company that developed and manufactured silicon and rare earth oxide-based epitaxial semiconductor wafers.

19. I was employed by Glyndŵr University from 2013 to 2015 as a Professor of Optoelectronics, where I focused on the design, simulation, and testing of high-speed, low-power photonic integrated circuits, optoelectronic integrated circuits, laser diodes, optics, and solar cells for applications that included communications, automotive, displays, sensing, and energy.

20. From 2013 to 2015, I was also employed as the President and CEO of OneChip Photonics Corporation, where I additionally served as an elected independent board member. In these roles, I focused on technical, business, and operational strategy for fiber optic communications based on InP photonic integrated circuits, as well as optoelectronic integrated circuits for fiber optic transceivers that incorporated electrical and optical multiplexing schemes using fiber optic connectors.

21. Over the course of my career, I have also led panels and given numerous keynote and invited presentations, speeches, and talks at workshops and conferences, including on photonic and optoelectronic materials, devices, components, packages as well as photonics technology in general.

22. Due to my passion for optics, I have been elected to the London Guild of Spectacle Makers. A more detailed description of my education, as well as my training and experience in the relevant technology, is included in my CV.

23. I hold over 340 combined issued USPTO patents and USPTO published patent applications that have been derived from over 230 issued U.S. utility patents, mostly in the field of optoelectronics, photonics, electronics, and semiconductors. I have been cited by the USPTO to be in the most prolific seventy-five inventors in the United States from 1988 to 1997.

24. I have authored approximately sixty-five (65) publications, and have achieved over 400 media events that include: technical articles, books, chapters, invited speaker events at conferences as well as for interviews that included TV, video, radio, and social, industrial, professional media in general. This includes technical, business-related, and financial conferences as a contributed, invited, and keynote speaker. Details can be found in my CV. Over the past decade, I have been a project reviewer and technical expert for the European Commission on numerous occasions.

25. I have also served as an expert witness on numerous patent matters, including 50 IPR proceedings and 5 PGR proceedings. I have also served on over 60 oral depositions that include ITC and District court proceedings.

26. A complete listing of these patents, publications, articles, lectures, and other public media is included with my CV.

27. On the basis of my education and the experience described above, I believe I am qualified to give the opinions set out herein.

### **III. MATERIALS REVIEWED**

28. I am not an attorney and offer no legal opinions, but in my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art. See Section VI.C below for the level of ordinary skill in the art for this declaration.

29. In preparing this declaration, I reviewed the '599 patent, including the claims of the patent in view of the specification, and I have reviewed the prosecution history of the '599 patent and numerous publications and technical references from and preceding the time of the alleged invention. More specifically, I have reviewed each of the following:

| <b>Exhibit</b> | <b>Description</b>                                               |
|----------------|------------------------------------------------------------------|
| 1001           | U.S. Patent No. 10,224,359 (the "'599 patent")                   |
| 1002           | File History for U.S. Patent No. 9,905,599                       |
| 1005           | Provisional Application No. 61/614,275 ('275 Provisional)        |
| 1006           | Int'l Publication No. WO 2011/035188 A2 (Haddad188)              |
| 1007           | U.S. Patent Application Publication No. 2012/0033119 (Shinohara) |

| <b>Exhibit</b> | <b>Description</b>                                                                                                                                                                                    |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1008           | Japanese Patent Application Publication No. 2011-119558 (Mori)                                                                                                                                        |
| 1009           | Certified English Translation of Japanese Patent Application Publication No. 2011-119558 (Mori)                                                                                                       |
| 1010           | U.S. Patent No. 7,675,099 (Hwang)                                                                                                                                                                     |
| 1011           | U.S. Patent No. 7,709,775 (Konno)                                                                                                                                                                     |
| 1012           | Samsung's Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)                                                                                                                                |
| 1013           | SiOnyx's Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)                                                                                                                                 |
| 1014           | Email from N. Subhedar re: Claim Construction M&C Follow-Up (Sept. 8, 2024)                                                                                                                           |
| 1015           | Joint Proposed Claim Construction Chart, Inv. No. 337-TA-1403 (Nov. 1, 2024)                                                                                                                          |
| 1016           | U.S. Patent Publication No. 2009/0160000 (Kim)                                                                                                                                                        |
| 1017           | E. Fred Schubert, LIGHT-EMITTING DIODES (2nd ed. 2006)                                                                                                                                                |
| 1018           | Stanley Wolf, MICROCHIP MANUFACTURING (2004) (Excerpts)                                                                                                                                               |
| 1019           | U.S. Patent Application Publication No. 2012/0025199 (Chen)                                                                                                                                           |
| 1020           | U.S. Patent No. 8,288,836 (Oshiyama)                                                                                                                                                                  |
| 1021           | Sadao Adachi, Optical Constants of Crystalline and Amorphous Semiconductors, Numerical Data and Graphical Information (1st Ed. 1999) (Excerpt)                                                        |
| 1022           | U.S. Patent No. 4,644,553                                                                                                                                                                             |
| 1023           | George Hass & Calvin D. Salzberg, <i>Optical Properties of Silicon Monoxide in the Wavelength Region from 0.24 to 14.0 Microns</i> , Vol. 44 No. 3, JOURNAL OF THE OPTICAL SOCIETY OF AM., 181 (1954) |
| 1024           | F. Lopez & E. Bernab  , <i>Refractive Index of Vacuum-Evaporated SiO Thin Films: Dependence on Substrate Temperature</i> , ELECTRONICS & OPTICS, 13 (1990)                                            |
| 1025           | Japanese Patent Application Publication No. JP H11-330501 (Suzunaga)                                                                                                                                  |
| 1026           | Certified English Translation of Japanese Patent Application Publication No. JP H11-330501 (Suzunaga)                                                                                                 |
| 1027           | U.S. Provisional Patent Application No. 61/311,004 (the “’004” Application)                                                                                                                           |
| 1028           | Japanese Patent Application Publication No. 2009-188316 (Yamada)                                                                                                                                      |
| 1029           | Certified English Translation of Japanese Patent Application Publication No. 2009-188316 (Yamada)                                                                                                     |

| Exhibit | Description                                                                                                                                                                        |
|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1030    | Gier et al., <i>Controlling the optical properties of hafnium dioxide thin films deposited with electron cyclotron resonance ion beam deposition</i> , THIN SOLID FILMS 771 (2023) |

#### IV. RELEVANT LEGAL STANDARDS

30. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to forming my opinions. I have applied the following understanding of the law.

31. I have been informed that a patent claim may be “anticipated” if each element of that claim is present either explicitly or inherently in a single prior art reference, and that the elements should be arranged in the reference as in the claim. Petitioner’s counsel has informed me that for a claimed limitation to be inherently present, the prior art need not expressly disclose the limitation, so long as the claimed limitation necessarily flows from a disclosure in the prior art.

32. I have been informed that a patent claim can be considered to have been obvious to a person of ordinary skill in the art at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time the application was filed.

33. I have been informed that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

34. I have been informed that a single reference can render a patent claim obvious if any differences between that reference and the claims would have been obvious to a person of ordinary skill in the art. Alternatively, the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to one having ordinary skill in the art. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider, among other factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, and when combined, would yield predictable results;
- whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;

- whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

35. Petitioner's counsel has informed me that one of ordinary skill in the art has ordinary creativity and is not an automaton. Petitioner's counsel has informed me that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

36. I understand that various objective or "real world" factors may be indicative of non-obviousness. I understand that such factors include:<sup>1</sup>

- the commercial success of the claimed invention;
- the existence of a long-felt, unresolved need for a solution to the problem solved by the claimed invention;
- failed attempts to solve the problem solved by the claimed invention;
- copying of the claimed invention;

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<sup>1</sup> I am not aware of any objective evidence of non-obviousness having been identified in connection with the '599 patent.

- unexpected results of the claimed invention;
- praise for the claimed invention by others in the relevant field; and
- willingness of others to accept a license under the patent because of the merits of the claimed invention.

## **V. TECHNOLOGY BACKGROUND**

37. Since the early 2000s, digital cameras and camcorders have become increasingly popular, largely due to the development of advanced image sensors. These sensors play a critical role in converting visual information into electrical signals, which are then processed to create digital images or videos. At the heart of an image sensor lies an array of light-sensitive pixels, each of which is a photodiode capable of detecting light. The photodiode's function is to convert incoming light photons into electrons; the quantity of electrons collected at each pixel determines the pixel's brightness. By assembling this data across all pixels, the sensor constructs a coherent image or video corresponding to the captured scene.

38. In an ideal scenario, an image sensor would achieve perfect efficiency, converting every photon that strikes it into a collected electron. However, in practice, some photons are lost during the conversion process. The efficiency of this conversion is quantified by a metric known as external quantum efficiency, or quantum efficiency for short. The '599 patent defines quantum efficiency as the ratio of electrons collected per photons incident on an optoelectronic device. '599 Patent, 4:30-35. Some incident

photons may be lost because they are reflected off before reaching the semiconductor layer including a photodiode; others may be lost because they pass through the semiconductor layer without being absorbed. To mitigate such losses, it is common practice to include in an image sensor microstructures that let more light into the semiconductor layer including a photodiode, as well as microstructures that reflect and scatter light that leaves the semiconductor layer back into the semiconductor layer.

39. One such well-known form of reflector is what is known as a distributed Bragg reflector (“DBR”), which is a structure formed by alternating materials with different refractive indices. Because of the different refractive indices of the layers, each layer boundary causes a partial reflection of light, and increasing the number of layers can thereby increase reflectivity. Schubert, 171. Distributed Bragg reflectors are known to be “well suited for inclusion between the substrate and the active layers” in semiconductor-based optical structures such as LEDs and optical sensors. *See* Ex-1017, 170.

40. Photodiodes are typically fabricated by doping a semiconductor layer to create a junction, which is used for sensing light. A photodiode junction is then connected to a neighboring metallization layer, which carries the electrical signal to external circuits that integrate the signals from all pixels to form a complete image. In the design of image sensors, the side of the semiconductor layer where the photodiode junction and the metallization layer are located is referred to as the “front side,” while

the opposite side is known as the “backside.” Image sensors can be designed to receive light from either the front side (front side illuminated, or FSI) or the backside (backside illuminated, or BSI), each offering different advantages and trade-offs.

41. Front side illuminated sensors are easier and less costly to manufacture, but they suffer from greater light loss because the incident light must pass through the metallization layer before reaching the photodiode junction. This can reduce the sensor’s overall efficiency and image quality, especially in low-light conditions. Conversely, backside illuminated sensors are more challenging and expensive to produce but offer superior performance because the incident light directly reaches the photodiode junction without passing through the metallization layer. This design reduces light loss and improves the sensor’s quantum efficiency, leading to better image quality, particularly in demanding lighting environments.

## **VI. OVERVIEW OF U.S. PATENT NO. 9,905,599**

### **A. Summary**

42. The ’599 patent relates to image sensor pixels and elements for trapping light within such pixels. ’599 patent, 6:15-19. The patent states that a reduction in the size of pixels in an image sensor can sacrifice image quality. ’599 patent, 1:22-24. According to the patent, reduced pixel size for image sensors tends to increase electrical and optical cross-talk between adjacent pixels, and image signal to noise tends to decrease. ’599 patent, 1:24-26. The patent purportedly provides for

semiconductor devices with, for example, “enhanced light detection properties.”

’599 patent, 6:12-15. An exemplary embodiment from the ’599 patent is depicted below.

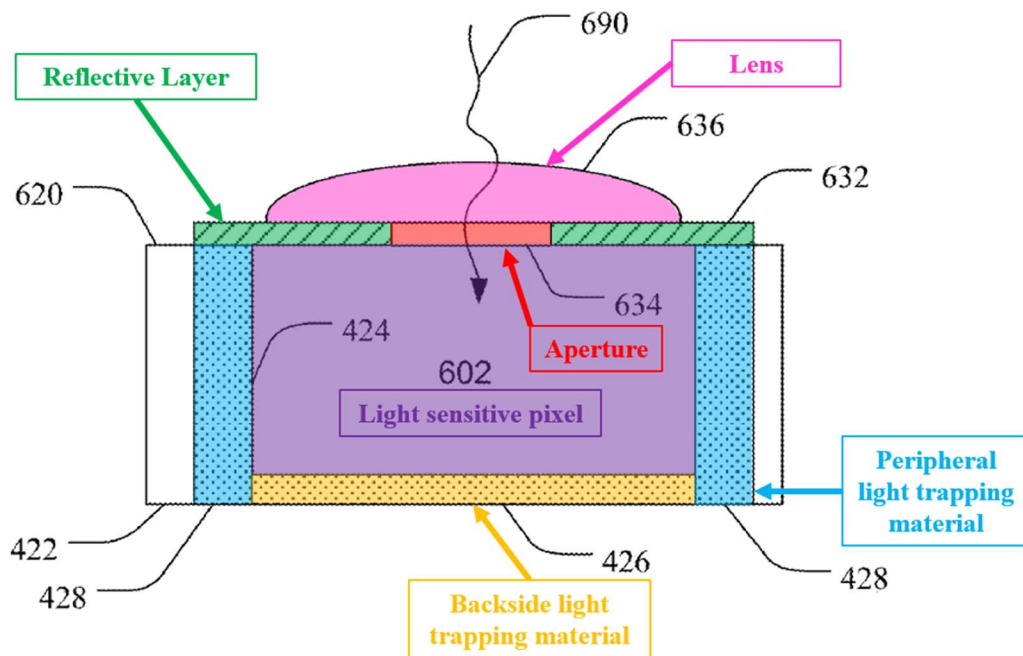


**Fig. 6**

’599 patent, Fig. 6 (annotated).

43. Figure 6 is a cross-sectional view of a light trapping pixel in accordance with an embodiment discussed in the patent. ’599 patent, 3:44-46. I understand that during prosecution the applicant stated that the claims of the ’599 patent are directed towards the embodiment depicted in Figure 6. *See* Ex-1002, 92 (“Applicants elect the species 6 corresponding to FIG. 6 of Applicants’ specification”).

44. The patent relates to “light trapping elements” that can “isolate neighboring pixels in an image sensor.” ’599 patent, 6:17-19. The isolation elements

can be configured “to optically and/or electrically isolate neighboring pixels from one another in addition to trapping light within the pixel.” ’599 patent, 6:19-21. The patent also refers to isolation elements as “trench isolation features” or “sidewalls.” ’599 patent, 7:41-43.

45. The patent broadly asserts that a “variety of reflective materials can be utilized in constructing the isolation features in order to provide optical isolation, light trapping, and/or electrical isolation,” and that “any such material capable of incorporation into a photosensitive device” is within the patent’s scope. ’599 patent, 7:63-67. Examples of such materials include a Bragg reflector or a metal reflector, including for example “silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like.” ’599 patent, 7:67-8:8. The isolation elements can be doped to affect properties of the material with respect to electrical isolation. ’599 patent, 8:12-15.

46. According to the patent, a light sensitive pixel can have “a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery.” ’599 patent, 1:41-46. Furthermore, the pixel can include “a backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall.” ’599 patent, 1:46-49. Light that contacts the peripheral light

trapping material or backside light trapping material is “reflected back toward the pixel.” ’599 patent, 1:49-52. The patent states that “light entering the pixel that is not absorbed will interact with and be reflected internally” by backside or peripheral sidewall light trapping materials, for example. ’599 patent, 12:27-30. Light is “effectively maintained inside the pixel until it is absorbed.” ’599 patent, 12:30-31. There may also be an “array” of light trapping pixels. ’599 patent, 1:52-53.

47. The isolation element can include at least two layers comprising material having a lower optical refractive index<sup>2</sup> as compared to the material of a third layer disposed or sandwiched between those two layers. ’599 patent, 8:34-39. In this case, the isolation element functions as a Bragg reflector. ’599 patent, 8:39-42. The patent states that a large index of refraction “mismatch” can result in “total reflection at the trench side walls.” ’599 patent, 9:25-27.

48. The pixel may also include a “textured region.” ’599 patent, 6:44-46. A textured region “typically” has a textured surface that “increases the surface area and increases the probability of radiation absorption.” ’599 patent, 15:26-29.

49. The pixel may also include “a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel.” ’599 patent

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<sup>2</sup> Herein I use the term “refractive index” to refer to optical refractive index.

2:29-32. The '599 patent further notes that “[i]n some aspects it can be beneficial to include a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.” ’599 patent 2:32-35; *see also* ’599 patent 11:64-12:31.

**B. Priority Date**

50. The application that led to the '599 patent was filed on June 23, 2015. It claims priority through a chain of continuation applications to Provisional Application No. 61/614,275, filed on March 22, 2012 (the “’275 Provisional”) (Ex-1005).

51. I have been asked to review the '275 Provisional and consider whether it discloses each aspect of the claimed invention of the '599 patent. I have concluded that it does not.

52. For example, both independent claims of the '599 Patent, i.e., claims 1 and 19, require “a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel” and that “the reflective layer is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into the pixel.” ’599 Patent, claims 1, 19. However, the '275 Provisional contains no disclosure of “a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel.” Furthermore, given that there is no disclosure in the '275 Provisional of the claimed

“reflective layer,” there is also no aperture. I have also reviewed the drawings of the ’275 Provisional and confirmed that none of the drawings depict a reflective layer coupled to the light incident side having an aperture.

53. This lack of disclosure makes sense given the prosecution history of the ’599 Patent. During the prosecution of the ’599 Patent, I understand that the applicant entered a species election directed at Figure 6 of the application, Ex-1002, 92. The embodiment of Figure 6 of the application is not depicted or described in the ’275 Provisional.

54. I understand this lack of disclosure may affect the priority date of the ’599 Patent. However, I also understand that regardless of whether the ’599 Patent can claim priority back to the ’275 Provisional, all of the references relied upon below are prior art to the ’599 Patent.

### **C. Level of Ordinary Skill in the Art**

55. It is my understanding that factors defining the level of ordinary skill in the art include: (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of technology; and (5) the educational level of active workers in the field.

56. In my opinion, a person of ordinary skill in the art (“POSITA”) as of March 2012 would have had a Bachelor’s degree in engineering, physics, or a related

or equivalent field, and two or more years of experience researching, developing, designing, and/or evaluating image sensors using photonics. A person with less or different education but more relevant practical experience, or vice versa, may also meet this standard. In my opinion, the definition of the level of ordinary skill in the art would be the same as of March 2013.

57. I met this definition of a POSITA as of March 2012. I applied this definition of a POSITA in forming my opinions in this declaration. I understand that SiOnyx, LLC (“SiOnyx” or “Patent Owner”) asserted the ’599 patent in a related case, *Sensors with Pixels and Products Containing the Same*. Inv. No. 337-TA-1403 (the “Related Case”). I understand that Patent Owner’s expert in the Related Case opined that “[t]he level of ordinary skill for the Asserted Patents should be defined as a person having at least a bachelor’s degree in electrical engineering, materials science, or physics, (or an equivalent technical degree), at least two years of experience in optoelectronics, and at least three years of work experience in semiconductor manufacturing. Further a master’s degree or Ph.D. in a relevant field may substitute for some work experience or vice versa.” I met Patent Owner’s definition of a POSITA as of March 2012. My opinion remains the same under Patent Owner’s definition.

**D. Claim Construction**

58. I understand that in this proceeding, the claims should be construed in accordance with their ordinary and customary meaning in light of the specification, as understood by one of ordinary skill in the art. I have therefore applied those plain and ordinary meanings in my analysis, except where otherwise noted.

59. I understand that, in the Related Case, Petitioner and Patent Owner have proposed competing constructions for certain terms of the '599 patent. *See* Ex-1012; Ex-1013; Ex-1014; Ex-1015. To the extent those constructions bear on my analysis I address them below.

**VII. CLAIMS ANALYSIS**

**A. Ground 1: Claims 19-20, 26-32, and 34-36 are Rendered Obvious Based on Haddad188**

**1. Overview of Haddad188**

60. World Intellectual Property Organization Patent Publication No. 2011/035188 (“Haddad188”) (Ex-1006) is an international patent application publication that I understand is prior art to the '599 patent. It is directed to an optoelectronic device, i.e., a photosensitive device, which “can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the

semiconductor substrate and operable to transfer an electrical signal from the at least one junction.” Haddad188, 1:24-30.

61. An exemplary embodiment from Haddad188 is depicted below.

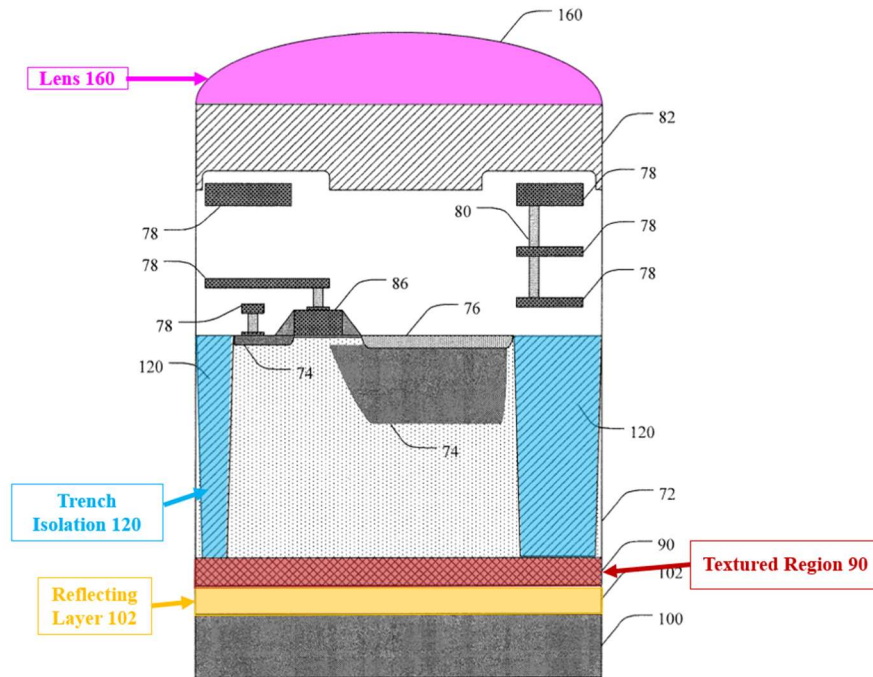


FIG. 16

Haddad188, Fig. 16 (annotated).

62. Haddad188’s Figure 16 “is a schematic view of a photosensitive pixel device.” Haddad188, 4:21. Among other things, it depicts a lens 160 as well as “[a] textured region 90 and a reflecting layer 102 are coupled to the semiconductor substrate 72 opposite the lens to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through the semiconductor substrate.” Haddad188, 25:5-9. In connection with this embodiment, Haddad188 also describes that “[a]n aperture 164 formed in a metal or other reflective material layer 166 can

increase the effectiveness of the optical cavity. Thus the lens focuses electromagnetic radiation through the aperture.” Haddad188, 25:9-11. Finally, as shown above, this embodiment of Haddad188 has trench isolation 120.

## 2. Claim 19:

### a) 19[pre]: “A light trapping device, comprising:”

63. To the extent the preamble is limiting, Haddad188 teaches or suggests it.

64. Haddad188 discloses “a front side illuminated (FSI) imager,” *see, e.g.*, Figure 16, otherwise referred to as a “photosensitive pixel device.” Haddad188, 25:4-5, 4:21-22.

65. Haddad188 discloses a “reflecting layer 102 ... coupled to the semiconductor substrate 72 opposite the lens,” which provides “reflection of the incident electromagnetic radiation that passes through the semiconductor substrate.” Haddad188, 25:6-9. Haddad188’s Figure 16 embodiment further comprises a “trench isolation 120,” which Haddad188 explains can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device.” Haddad188, 24:7-9. Finally, in its description of this embodiment, Haddad188 also discloses “[a]n aperture 164 formed in a metal or other reflective material layer 166” which “can increase the

effectiveness of the optical cavity.” Haddad188, 25:9-11.<sup>3</sup> These reflective layers allow Haddad188’s image sensor to trap light by reflecting light back into the pixel. Accordingly, Haddad188’s image sensor constitutes a *light trapping device*.

- b) **19[a]: “at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;”**

66. Haddad188 teaches or suggests this limitation.

67. Haddad188 discloses *at least one light sensitive pixel*. Figure 16 of Haddad188 “is a schematic view of a photosensitive pixel device.” Haddad188, 4:21-22. Haddad188’s Figure 16 embodiment includes a semiconductor substrate 72, including doped regions 74 and highly doped region 76. *See, e.g.*, Haddad188, 25:6-9, 22:9-20. As Haddad188 explains, “[a] highly doped region 76 can be formed on or near the doped region to create a pinned diode,” i.e., a photodiode. Haddad188, 22:13-14.

68. Haddad188 discloses *a light incident surface* and *a backside surface opposite the light incident surface*, as illustrated below:

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<sup>3</sup> The aperture 164 and reflective material layer 166 are not shown in Figure 16 of Haddad188. However, Haddad188 describes those elements as part of the front side illuminated imager of Figure 16. *See* Haddad188, 25:4-11.

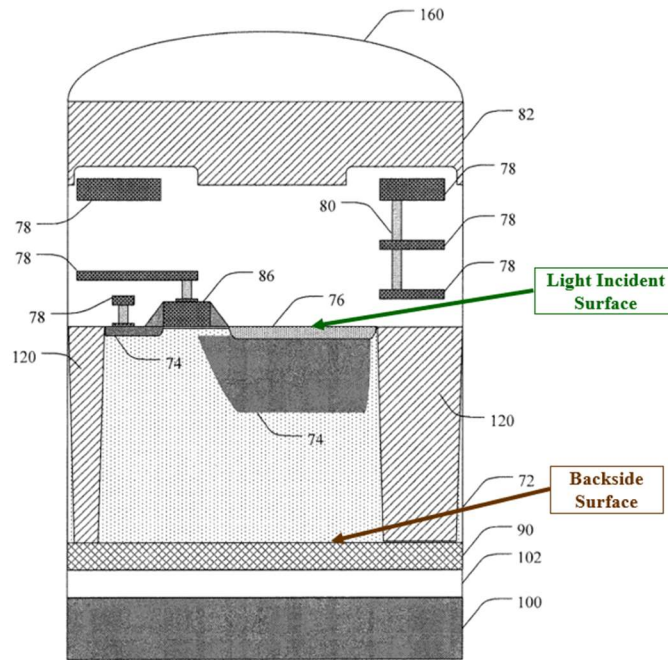


FIG. 16

Haddad188 Fig. 16 (annotated).

69. Light passes through the lens 160, through an aperture 164 (not shown), and through the top surface of the semiconductor substrate 72 (i.e., the light incident surface). *See* Haddad188, 25:4-11. A textured region 90 and a reflecting layer 102 are coupled to the bottom surface of the semiconductor substrate 72 (i.e., the backside surface). *See* Haddad188, 25:6-9; *see also* Haddad188, 20:22-23 (“[T]he reflective layer can be located on the semiconductor substrate opposite the incoming electromagnetic radiation.”). Accordingly, the top surface of the semiconductor substrate 72 is a *light incident surface* and bottom surface of the semiconductor substrate 72 is a *backside surface opposite the light incident surface*.

70. Haddad188 further discloses *a peripheral sidewall*. Each pixel includes *a peripheral sidewall* where the semiconductor substrate 72 meets trench isolation 120 (i.e., the side wall of trench isolation 120), as shown below:

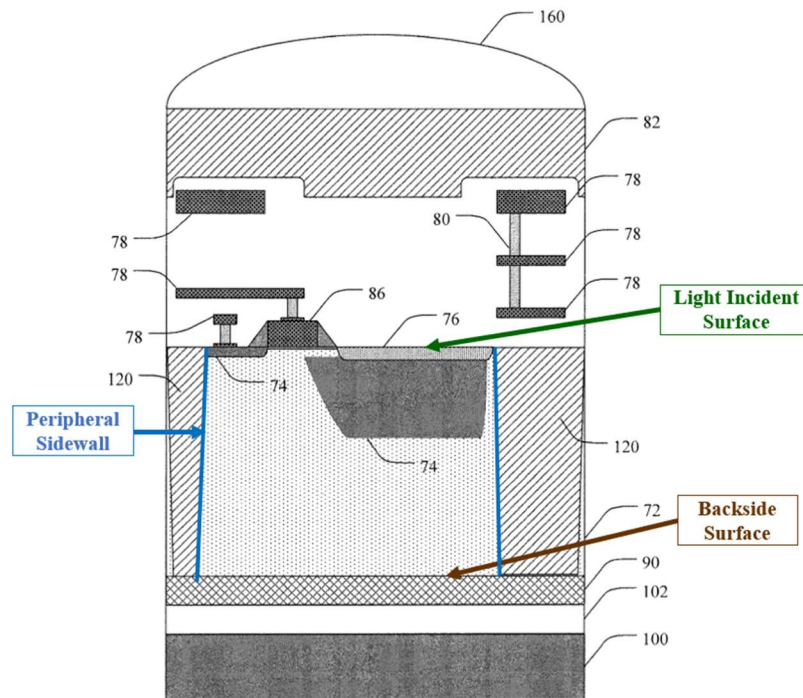


FIG. 16

Haddad188 Fig. 16 (annotated).

71. Haddad188's description of Figure 16 is silent as to the function of trench isolation 120. However, Haddad188 elsewhere discloses that the "trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device." Haddad188, 24:5-9. *See also* Haddad188, 22:25-29. As Haddad188 explains, "[t]rench isolation elements can maintain pixel to pixel uniformity by reducing optical and electrical crosstalk." Haddad188, 22:23-24.

72. As shown in Figure 16, Haddad188's peripheral sidewall *extends at least partially around the pixel periphery*. This is consistent with the role of the trench isolation 120, e.g., reducing optical and electrical crosstalk. A POSITA would understand that the more that trench isolation 120 extends around the periphery, the more that light and current will be prevented from moving between pixels, and the less of a chance that crosstalk will occur.

**c) 19[b]: “a backside light trapping material at least partially covering the backside surface;”**

73. Haddad188 teaches or suggests this limitation.

74. Haddad188 discloses *a backside light trapping material at least partially covering the backside surface*. Haddad188 discloses “reflecting layer 102” which is “coupled to the semiconductor substrate 72 opposite the lens.” Haddad188, 25:6-7. As Haddad188 explains, “textured region 90 and ... reflecting layer 102 are coupled to the semiconductor substrate 72 opposite the lens to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through the semiconductor substrate.” Haddad188, 25:6-9.<sup>4</sup> Elsewhere, Haddad188 describes the purposes of its reflecting layer as reflecting “electromagnetic radiation passing though [*sic*] the semiconductor substrate and the textured region ... back

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<sup>4</sup> All emphasis added except where otherwise noted.

into the semiconductor substrate.” Haddad188, 20:20-23. Accordingly, Haddad188’s reflective layer constitutes a *backside light trapping material*.

75. As shown below, Haddad188’s backside light trapping material (*i.e.*, the reflecting layer 102) *at least partially covers the backside surface*:

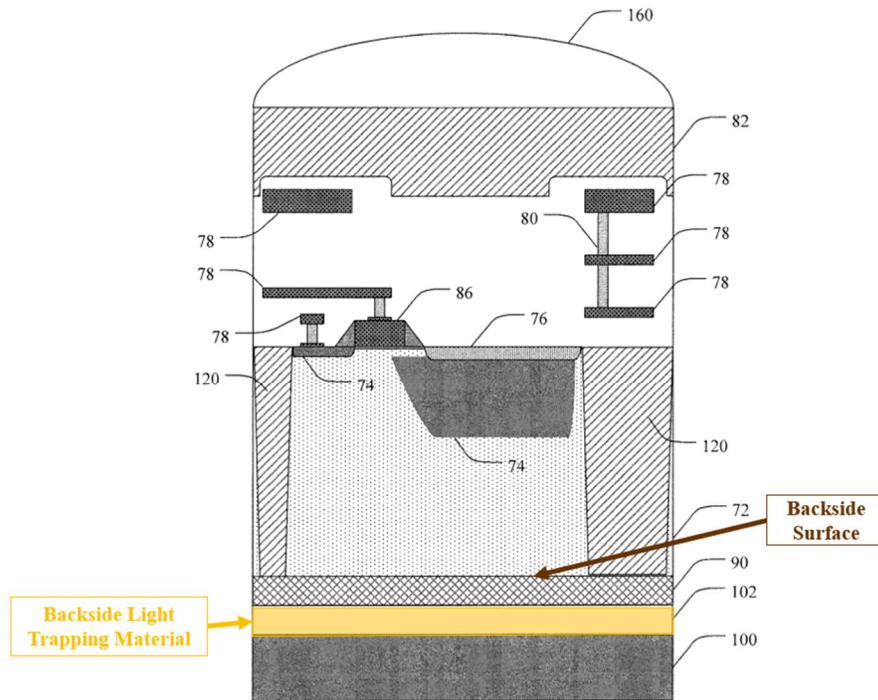


FIG. 16

Haddad188 Fig. 16 (annotated).

**d) 19[c]: “a peripheral light trapping material substantially covering the peripheral sidewall;”**

76. Haddad188 teaches or suggests this limitation.

77. Haddad188 discloses *a peripheral light trapping material*, *i.e.*, “trench isolation 120.” Trench isolation 120 “can be configured to reflect incident electromagnetic radiation,” and thus trap light. Haddad188, 24:7-8. According to

Haddad188, “[t]he trench isolation can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like.” Haddad188, 22:25-27. Haddad188 further explains that “[t]hese trench isolation regions can be configured to reflect incident light until it is absorbed, thereby increase the effective absorption length of the device.” Haddad188, 22:27-30.

78. As shown below, the material comprising trench isolation 120 *substantially cover[s] the peripheral sidewall*:

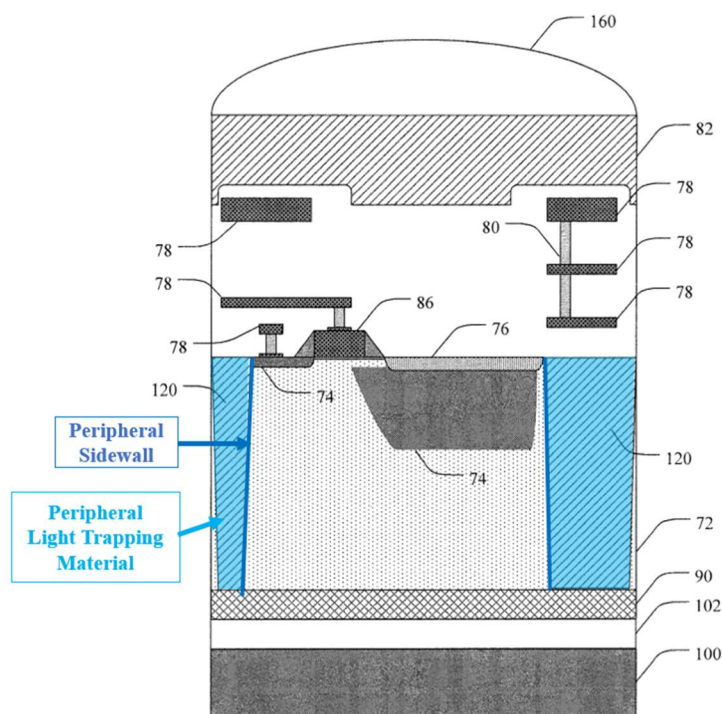


FIG. 16

Haddad188 Fig. 16 (annotated).

- e) **19[d]: “a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device; and”**

79. Haddad188 teaches or suggests this limitation.

80. Haddad188 discloses a “textured region 90 and a reflecting layer 102 are coupled to the semiconductor substrate 72 opposite the lens to provide diffusive scattering of the incident electromagnetic radiation.” Haddad188, 25:6-9. As Haddad188 explains elsewhere, “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31; *see also* Haddad188, 15:14-19 (“Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device.... This increase in absorption length increases the quantum efficiency of the device.”).

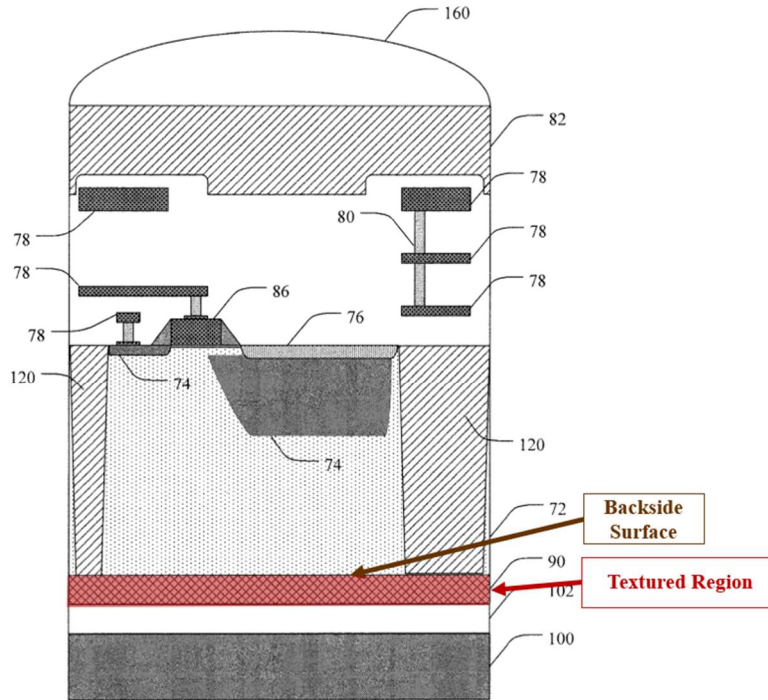


FIG. 16

Haddad188 Fig. 16 (annotated).

81. Accordingly, Haddad188 discloses *a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device.*

**f) 19[e]: “a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel;”**

82. Haddad188 teaches or suggests this limitation.

83. Haddad188 discloses *a reflective layer*, i.e., “a metal or other reflective material layer 166.” Haddad188, 25:9-10.

84. Haddad188 further discloses that the reflective material layer 166 *has an aperture to allow entry of light into the pixel*. Haddad188, 25:9-10 (“An aperture 164 formed in a metal or other reflective material layer 166 can increase the

85. While the reflective material layer 166 is discussed in the text of the specification, Haddad188's figures do not depict the reflective material layer 166. One of the provisional applications that Haddad188 claims the benefit of, however, does. Specifically, Haddad188 claims priority to "U.S. Provisional Patent Application Serial No. 61/311,004" (the "'004 Application") and notes that the '004 Application "is incorporated herein by reference." Haddad188, 1:4-8. Figure 10 of the '004 Application, shown below, depicts the reflective material 244 and aperture 246 disposed on the light incident side of the semiconductor substrate 202, above the highly doped region 206. '004 Application (Ex-1027) at 9.



'004 Application Fig. 10 (annotated).

86. A POSITA would understand that Haddad188's reflective material layer 166, containing aperture 164, would be similarly located in the embodiment shown in Figure 16, as shown in the modified Figure 16 below. This would allow the lens 160 to focus electromagnetic radiation through the aperture and into the doped regions, as Haddad188 describes. *See* Haddad188, 25:10-11. A POSITA would further understand that this placement would allow the reflective material layer 166 to increase the effectiveness of the optical cavity because the reflective material layer 166 would reflect light striking it from inside the pixel back into the pixel. *See* Haddad188, 25:10-11 ("An aperture 164 formed in a metal or other reflective material layer 166 can increase the effectiveness of the optical cavity.").

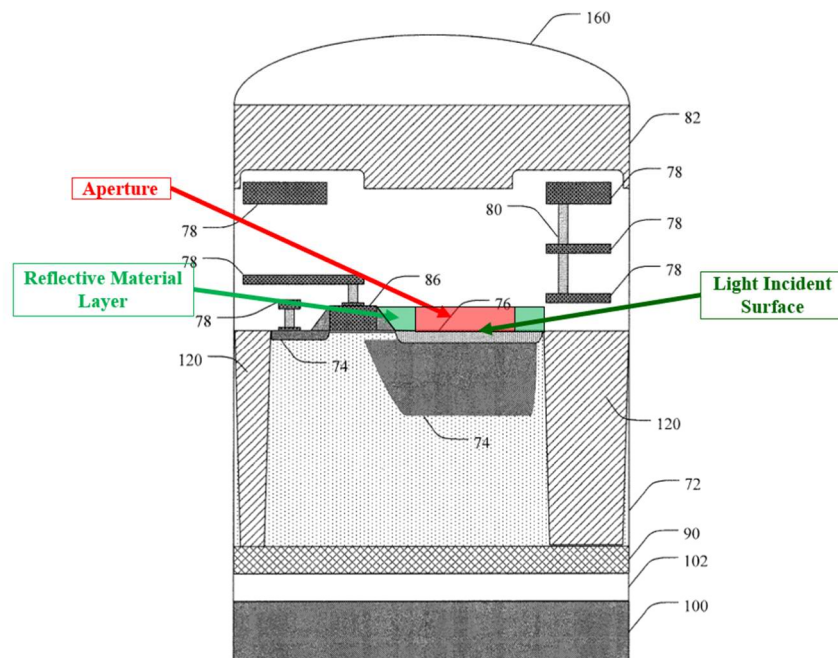


FIG. 16

Haddad188 Fig. 16 (modified).

87. Indeed, the '004 Application's disclosure with respect to its Figure 10 is substantially similar to Haddad188's disclosures with respect to its Figure 16, as shown below.

| <b>Haddad188, 25:4-11</b>                                                                                                                                                                                                                                 | <b>'004 Application (Ex-1027) at 9</b>                                                                                                                                                                                                                                                                                                                                                                          |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Fig. 16 shows a front side illuminated (FSI) imager according to another aspect of the present disclosure.                                                                                                                                                | Fig. 10 shows a front side illuminated, FSI, imager according to another embodiment of the invention.                                                                                                                                                                                                                                                                                                           |
| A lens 160 and an antireflecting passivation layer on 62 are coupled to the front side of the pixel.                                                                                                                                                      | A lens 240, and antireflecting passivation layer, 216, are placed on the front side of the pixel 200 after semiconductor fabrication is completed.                                                                                                                                                                                                                                                              |
| A textured region 90 and a reflecting layer 102 are coupled to the semiconductor substrate 72 opposite the lens to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through the semiconductor substrate. | A light scattering layer 236, and reflecting layer 238, are placed on the back of the pixel to give diffusive scattering and reflection of the incident light 232, that reaches the back of the pixel. This results in the incident light being confined in a cavity by reflections on all sides and a maximum possible absorption of particularly the longer wavelengths not strongly absorbed by the silicon. |
| An aperture 164 formed in a metal or other reflective material layer 166 can increase the effectiveness of the optical cavity.                                                                                                                            | Fig. 10 also shows the use of an aperture 246 formed by metal or other reflective material 244, to increase the effectiveness of the optical cavity.                                                                                                                                                                                                                                                            |
| Thus the lens focuses electromagnetic radiation through the aperture.                                                                                                                                                                                     | Lens 240, serves to focus the light through the aperture 246.                                                                                                                                                                                                                                                                                                                                                   |

88. Accordingly, a POSITA would understand that Haddad188 discloses, or at least renders obvious, *a reflective layer*, i.e., reflective material layer 166, *coupled*

*to the light incident side, and having an aperture, i.e. aperture 164, to allow entry of light into the pixel.*

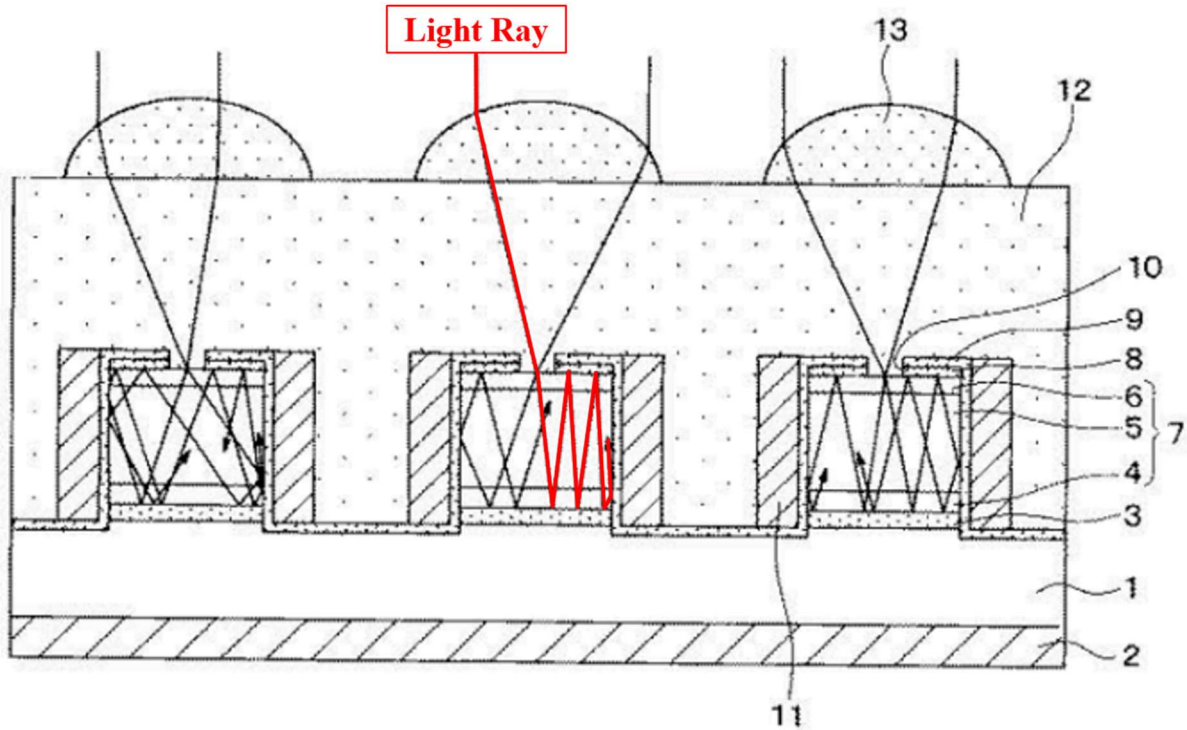
- g) 19[f]: “wherein the reflective layer is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into the pixel.”**

89. Haddad188 teaches or suggests this limitation.

90. The reflective layer of Haddad188 (*i.e.*, the reflective material layer 166) *is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into the pixel.* Haddad188’s Figure 16 embodiment includes both a backside reflecting layer 102 and the frontside reflective material layer 166 (as noted above, the trench isolation 120 can also be reflective). As Haddad188 explains, the purpose of its reflective layers is “to maintain electromagnetic radiation in the semiconductor substrate,” by “reflecting incident light until it is absorbed.” *See, e.g.*, Haddad188, 2:29-31; *see also* Haddad188, 20:19-25, Haddad188, 22:22-29.

91. A POSITA would understand that Haddad188’s design, including reflective frontside, backside, and side surfaces is operable to reflect at least a portion of light multiple times off of the reflective material layer 166 (*e.g.*, back into the pixel back into the pixel). Indeed, such reflection was well-known at the time of the art, as evidenced by the light path depicted in annotated Figure 1 of Yamada, below

(showing light ray reflected by first reflective film 3, second reflective film 8, and third reflective film 11):



Yamada Fig. 1 (annotated).

3. **Claim 20:** “The device of claim 19, wherein at least one of the backside light trapping material and the peripheral light trapping material reflects light incident thereon back into the pixel.”

92. Haddad188 teaches or suggests this limitation. Both *the backside light trapping material* (i.e., Haddad188’s reflecting layer 102) and *the peripheral light trapping material* (i.e., Haddad188’s trench isolation 120) *reflects light incident thereupon back into the pixel.*

93. Haddad188 discloses that *the backside light trapping material* (Haddad188's reflecting layer 102) *reflects light incident thereon back into the pixel*. Haddad188 discloses that the "textured region 90 and a reflecting layer 102 ... provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through the semiconductor substrate." Haddad188, 25:6-9. Elsewhere, Haddad188 indicates that the function of the reflecting layer is "to reflect electromagnetic radiation back into the device." Haddad188, 20:19-22. Accordingly, a POSITA would understand that Haddad188's reflecting layer 102 (*backside light trapping material*) *reflects light incident thereon back into the pixel*.

94. In addition, Haddad188 discloses that *the peripheral light trapping material reflects light incident thereon back into the pixel*. Haddad188 explains that "the trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device." Haddad188, 24:7-9. A POSITA would understand that in order for the trench isolation of Haddad188 to reflect incident electromagnetic radiation until it is absorbed, the trench isolation would have to reflect the electromagnetic radiation back into the pixel. Accordingly, a POSITA would understand that Haddad188's trench isolation 120 (*peripheral light trapping material*) *reflects light incident thereon back into the pixel*.

**4. Claim 26: “The device of claim 19, wherein the peripheral sidewall extends completely around the pixel periphery.”**

95. Haddad188 teaches or suggests this limitation.

96. Haddad188 does not include a plan view showing the extent to which the trench isolation 120 surrounds the pixel; however, Haddad188 discloses that the trench isolation is used to “maintain pixel uniformity by reducing optical and electrical crosstalk,” i.e., to ensure that light and charge cannot move from one pixel to the next. 22:23-24. A POSITA would have understood that the greater the coverage the more the optical and electrical crosstalk could be reduced. Accordingly, it would have at least been obvious to a POSITA to make the trench isolation extend completely around the pixel periphery in order to “maintain pixel to pixel uniformity by reducing optical and electrical crosstalk.” Haddad188, 22:23-24.

97. Indeed, this was a well-known technique. For example, Hwang provides an example of pixels comprising a *peripheral sidewall extending completely around the pixel periphery*, as shown in Figure 1 below:

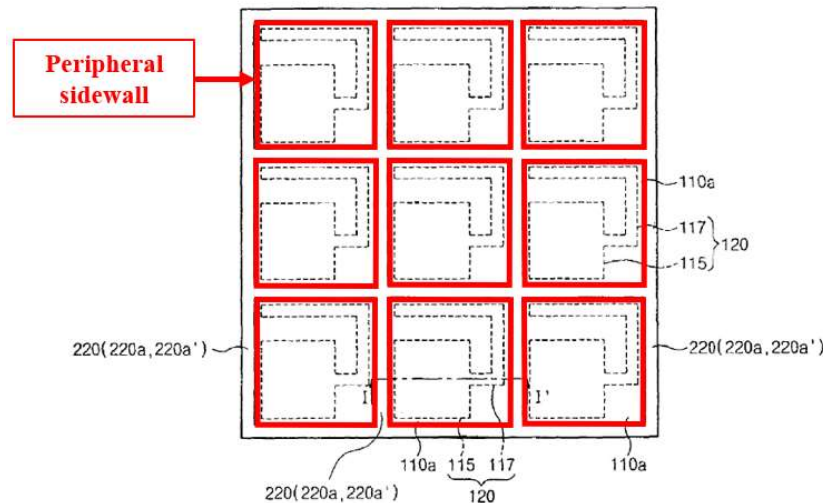


**Fig. 1**

Hwang, Fig. 1 (annotated); *see also* Hwang, 6:15-17 (“The sidewall multi-layered reflection layer 220 encloses the side walls of the pixel semiconductor patterns 110a.”).

98. Yamada similarly discloses that each of its embodiments “is configured such that the entire side surfaces of the PIN photodiode 7 is covered by the third reflective films 11.” Yamada, [0056]. Consistent with Haddad188’s teachings, Yamada explains that “the PIN photodiode 7 is surrounded by the ... third reflective film 11, so when light is incident to the PIN photodiode 7, that light is reflected by ... the third reflective films 11 so as to be confined within the PIN photodiode 7.” Yamada, [0036].

99. Accordingly, it would have at least been obvious based on Haddad188’s teaching to form *the peripheral sidewall extending completely around the pixel periphery*.

5. **Claim 27: “The device of claim 19, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”**

100. Haddad188 teaches or suggests this limitation.

101. Figure 16 of Haddad188 shows the trench sidewall extending from the light incident surface to the backside surface.

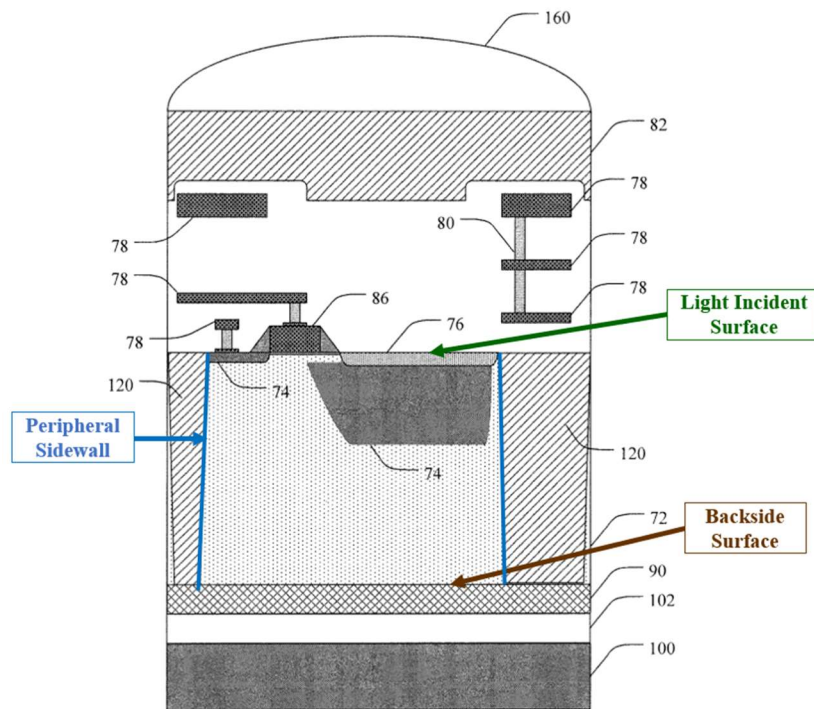


FIG. 16

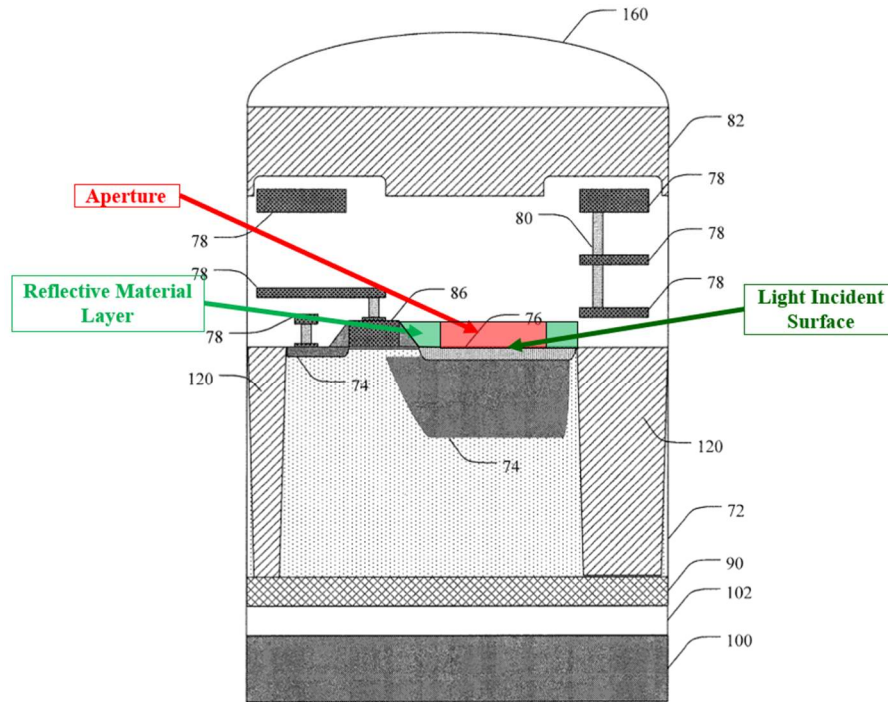
Haddad188 Fig. 16 (annotated); *see also* Haddad188, 22:24-25 (“The trench isolation can be shallow (FIG. 7) or deep (FIG. 12) trench isolation.”).

6. **Claim 28: “The device of claim 19, wherein said aperture has an effective surface area of less than about 90% of total area of the incident light surface.”**

102. Haddad188 teaches or suggests this limitation.

103. As explained with respect to claim 19 above, Haddad188 discloses a reflective material layer 166 coupled to the light incident side having an aperture 164 to allow entry of light into the pixel. However, Haddad188 is silent as to the aperture's effective surface area. It would have been obvious for a POSITA to design the aperture to have *an effective surface area of less than about 90% of total area of the incident light surface*.

104. As can be seen and as discussed above with respect to claim 19[d], Haddad188 discloses a front side illuminated imager, wherein the light incident surface is covered by circuitry, such as an electrical transfer element 86 and various metal regions 78. *See* Haddad188, 22:21-23. Such circuitry naturally limits the amount of effective surface area available for incident light to enter the pixel. *See, e.g.,* Haddad188, 9:3-8 (“The light, however, can scatter off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise.”).



Haddad188 Fig. 16 (modified).

105. Haddad188’s aperture is formed by a “reflective material layer” which is used to “increase the effectiveness of the optical cavity.” Haddad188, 25:9-10. A POSITA would understand that the reflective material layer does so by reflecting incident light back into the pixel so that it can be further absorbed. A POSITA would have understood that increasing the size of the aperture would allow more light to be collected. However, a POSITA would further understand that if the aperture is too large, incident light will not be reflected back into the pixel but rather will escape through the aperture.

106. Similar image sensors have been created balancing the same competing considerations having apertures with *an effective surface area of less than about 90%*

of total area of the incident light surface. For example, Ex-1016 (“Kim”) discloses photodiodes that contain an aperture (i.e., an opening 107) formed of reflective films 106 that reflects light back into the photodiodes. Kim [0018] (“[l]ight 105 reflected from photodiodes 102 can return to photodiodes 102 after being reflected by reflected films 106”). Kim discloses that the “openings 107 can occupy between 70 to 90% of the uppermost surface area of photodiodes 102.” Kim, [0015].

107. By way of another example, Konno discloses a photo-detector 101 comprising a reflecting layer 121 with a light entrance window 128 (i.e., an aperture).

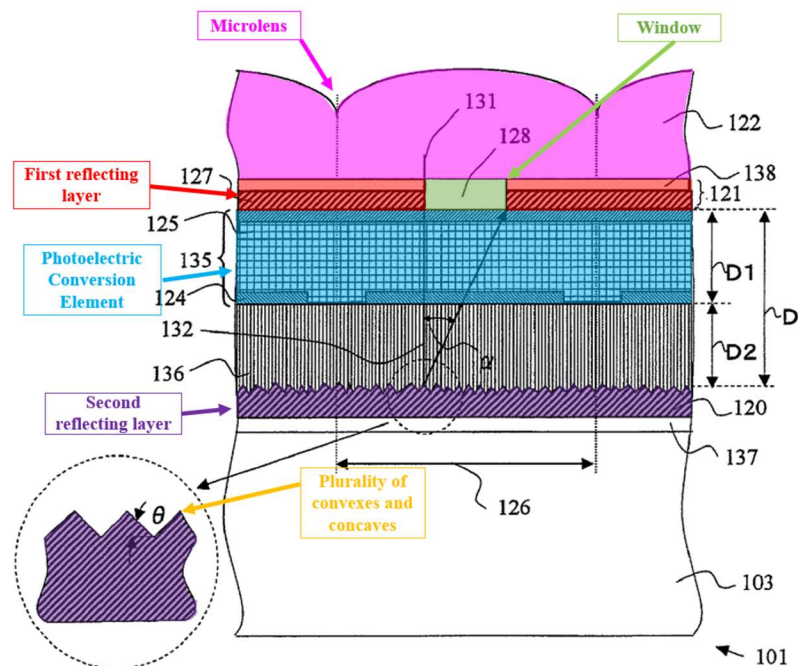


Fig.7

Konno Fig. 7 (annotated).

108. Konno explains that:

The width (diameter) of the light entrance window 128 [i.e., the width of the aperture] is appropriately determined on the basis of the relation to width 126 of the pixel [i.e., the width of the incident light surface], thickness of the transparent layer 136 to be explained later, and the like. For example, when the width 126 of pixel is 100  $\mu\text{m}$ , it [i.e., the width of the aperture] is 20  $\mu\text{m}$ .

Konno, 8:66-9:3.<sup>5</sup>

109. Accordingly, Konno also discloses an aperture having an effective surface area of less than about 90% of total area of the incident light surface.

110. Thus, it would have been obvious to a POSITA to choose an aperture area of less than about 90%, in particular given the constraints of Haddad188 being a front-side imager device.

111. Nevertheless, designing the aperture to be less than about 90% of the incident light surface total surface area would be nothing more than a design choice,

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<sup>5</sup> Konno explains that “[t]he light entrance window 128 may have various shapes. For example, it may be a slot along the direction perpendicular to the sectional line A indicated in FIG. 1, or it may have a round shape or a polygonal shape.” Konno, 8:63-66. Regardless of the shape, a POSITA would understand that the length of the aperture cannot be greater than the length of the pixel. Therefore, an aperture with Konno’s dimensions must have an effective surface area of less than about 90% of total area of the incident light surface.

as evidenced by the '599 patent's failure to identify any particular benefit of doing so. *See* '599 patent, 12:9-14.

**7. Claim 29: “The device of claim 19, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.”**

112. Haddad188 teaches or suggests this limitation.

113. Haddad188 discloses a lens 160 *functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel*, as shown in modified Figure 16 below. Specifically, Haddad188 discloses that “the lens [160] focuses electromagnetic radiation through the aperture.” Haddad188, 25:10-11; *see also* Haddad188, 9:6-8 (“A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry.”). As can be seen below, once the electromagnetic radiation goes from the lens to the aperture, it must go into the pixel.

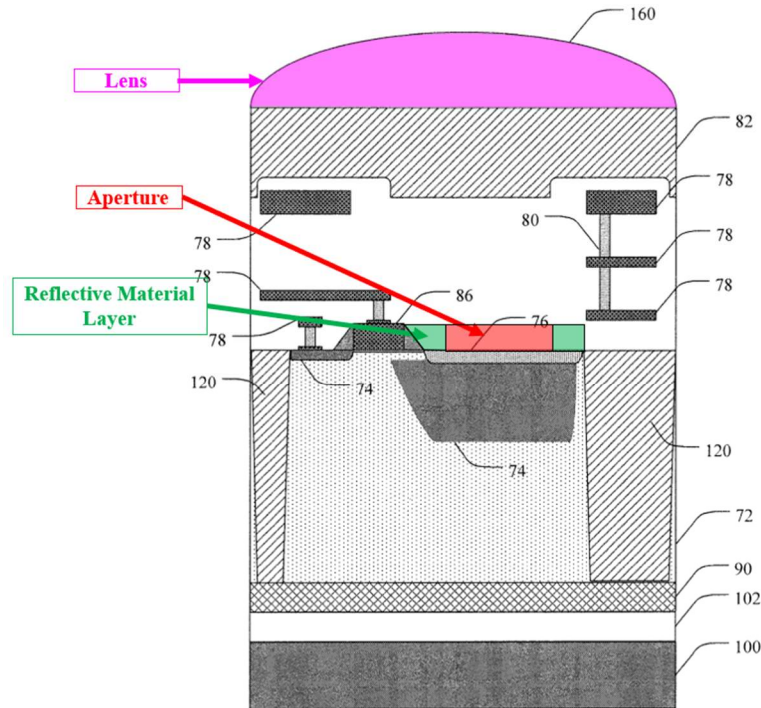


FIG. 16

Haddad188 Fig. 16 (modified).

114. Accordingly, Haddad188 discloses *a lens operable to focus incident light through the aperture and into the pixel.*

8. **Claim 30: “The device of claim 19, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”**

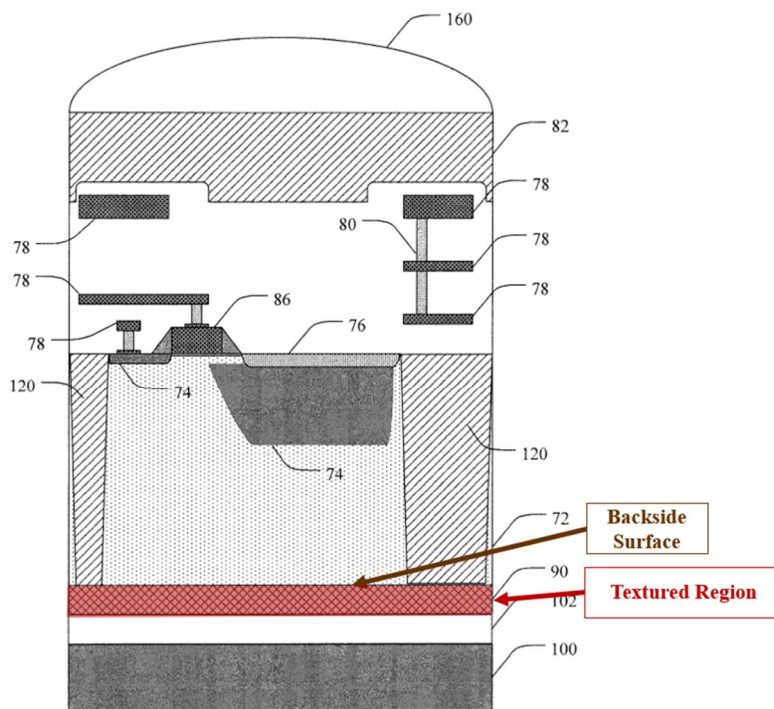
115. Haddad188 teaches or suggests this limitation.

116. Haddad188 discloses that its *backside light trapping material* (i.e., reflecting layer 102) “can be any reflective material that can be incorporated into such a device.” Haddad188, 23:24-25. Haddad188 specifically discloses “[n]onlimiting examples can include materials such as silver, aluminum, and the like,” i.e., a *metal layer*. Haddad188, 23:15-26.

**9. Claim 31: “The device of claim 19, wherein said textured region comprises a textured film layer.”**

117. Haddad188 teaches or suggests this limitation.

118. As shown below, Haddad188 discloses that the texture region can comprise a textured film layer.



Haddad188 Fig. 16 (annotated).

119. In particular, Haddad188 teaches or suggests that “[t]he textured region can be formed by various techniques, including lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, additional material deposition, and the like.” Haddad188, 15:20-29.

120. Accordingly, Haddad188 teaches or suggests *wherein said textured region comprises a textured film layer*.

**10. Claim 32: “The device of claim 31, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”**

121. Haddad188 teaches or suggests this limitation.

122. Haddad188 is silent as to the material used for his textured region 90. However, Haddad188 discloses that “[a] variety of semiconductor materials are contemplated for use with [its] devices,” including “amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon.” Haddad188, 10:17-30. Haddad188 further discloses that its reflective layers can include metals “such as silver, aluminum, and the like.” Haddad188, 23:24-26. Given that these materials are already being using in the construction of Haddad188’s imager, it would have been obvious to a POSITA that any of amorphous silicon, polysilicon, or metal could likewise be used to form the textured film layer. Not only are these materials commonly used in semiconductor manufacturing, but there are efficiencies that are gained in reusing the same materials, including costs, simplicity, ease of manufacturing, etc. Finally, most of these materials are silicon based and all of them have been widely used in semiconductor fabrication for almost sixty years. Accordingly, a POSITA would be familiar with the fabrication, design, and use of such materials.

123. A POSITA would have had an expectation of success in using these materials, given that, for example, Haddad188 separately discloses forming a textured region directly on the semiconductor substrate, *see, e.g.*, Haddad188, 3:2-5, which, as discussed above, Haddad188 discusses being amorphous silicon or polysilicon. All of these materials are also compatible with Haddad188's disclosure that the textured region 90 can be formed via, for example, "additional material deposition." Haddad188, 15:20-22. For example, depositing dielectrics had been a routine step of silicon fabrication process flows and fabrication techniques for many years prior to the '599 patent.

124. Accordingly, Haddad188 teaches or suggests *a textured film layer comprising any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.*

**11. Claim 34: "The device of claim 19, wherein the backside light trapping material substantially covers the backside surface."**

125. Haddad188 teaches or suggests this limitation.

126. As can be seen below, the *backside light trapping material (i.e., the reflecting layer 102) substantially covers the backside surface*, consistent with its role in reflecting incident electromagnetic radiation that passes through the semiconductor substrate. *See, e.g.*, Haddad188, 25:6-9; *see also* Haddad188, 23:19-22.



Backside  
Surface

**12. Claim 35: “The device of claim 19, wherein the backside light trapping material completely covers the backside surface.”**

128. As can be seen below, the *backside light trapping material* (i.e., the  
 ing layer 102) *completely covers the backside surface*, consistent with its role in  
 ing incident electromagnetic radiation that passes through the semiconductor  
 ate, and the fact that the Figure 16 embodiment is a front side illuminated imager.  
 g., Haddad188, 25:4-9, Haddad188, 23:19-22.

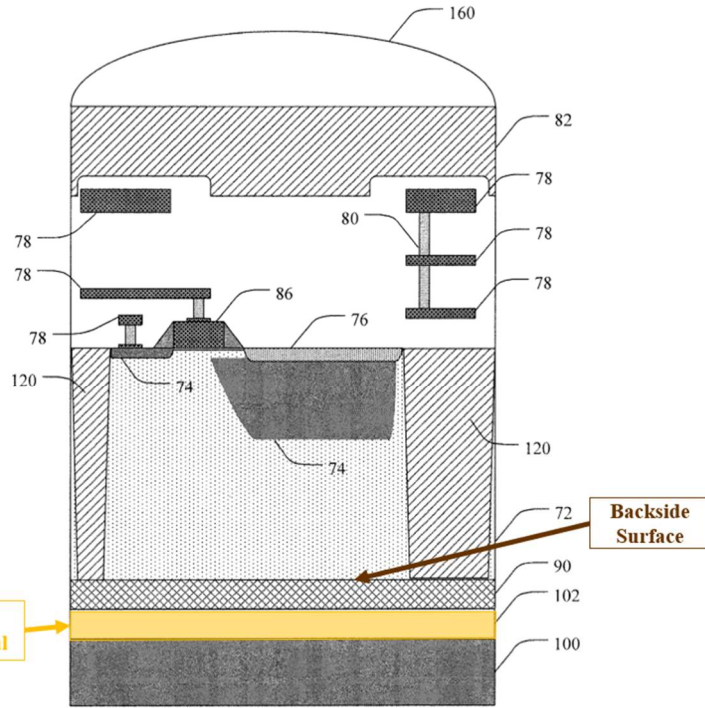


FIG. 16

Haddad188 Fig. 16 (annotated).

**13. Claim 36: “The device of claim 19, wherein said peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.”**

129. Haddad<sup>188</sup> teaches or suggests this limitation.

130. As can be seen below, the *peripheral sidewall* (i.e., trench sidewall) *extends through the pixel substantially from the light incident surface to the backside surface.*

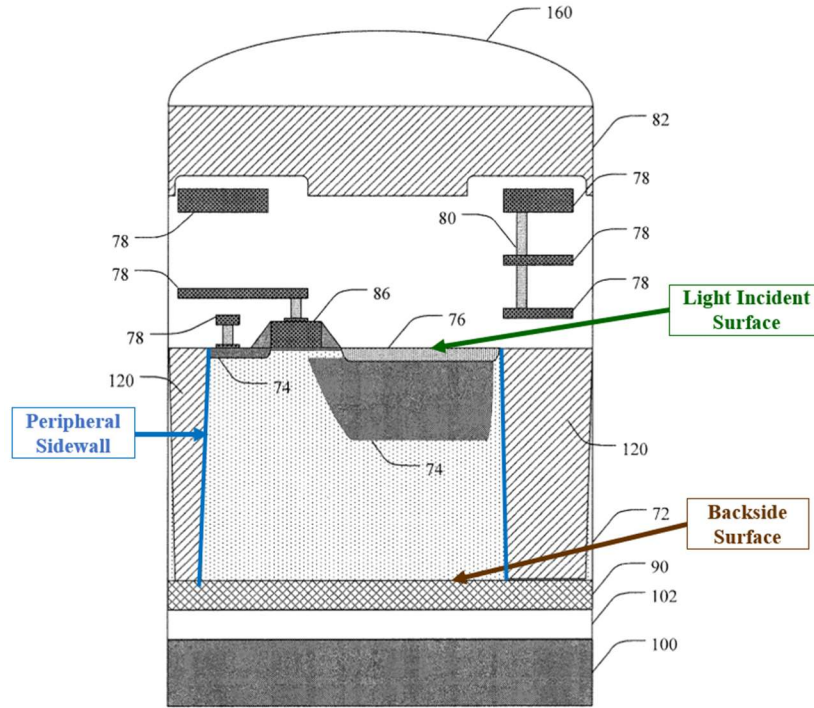


FIG. 16

Haddad188 Fig. 16 (annotated); *see also* Haddad188, 22:24-25 (“The trench isolation can be shallow (FIG. 7) or deep (FIG. 12) trench isolation.”).

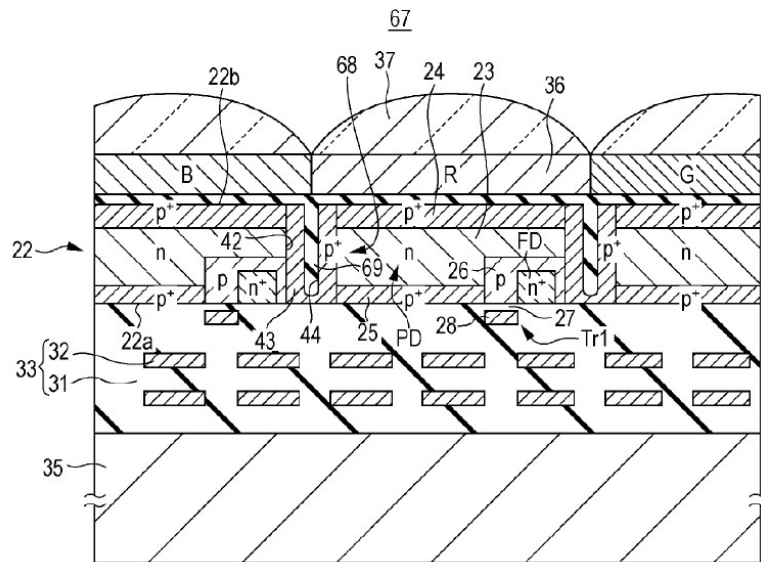
**B. Ground 2: Claim 33 is Obvious Based on Haddad188 and Shinohara**

**1. Overview of Shinohara**

131. U.S. Patent Application Publication No. 2012/0033119 (“Shinohara”) (Ex-1007) is a U.S. patent application that I understand is prior art to the ’599 patent. It is directed to “a solid state imaging device,” including a number of pixels separated by “element isolation region[s].” Shinohara, Abstract (“A solid state imaging device having a backside illuminated structure, includes: a pixel region in which pixels each having a plurality of pixel transistors are arranged in a two-dimensional matrix; an

element isolation region isolating the pixels which is provided in the pixel region and which includes a semiconductor layer provided in a trench by an epitaxial growth; and a light receiving surface at a rear surface side of a semiconductor substrate which is opposite to a multilayer wiring layer.”).

132. An exemplary embodiment from Shinohara is depicted below.



Shinohara, Fig. 9A.

133. Shinohara’s Figure 9A is a schematic structural view showing a section of a solid-state imaging device. Shinohara, [0032]. Like the ’599 patent, Shinohara describes “an element isolation region for isolating pixels from each other.” Shinohara, [0006]. Shinohara explains that selecting an insulating film 69 with a negative fixed charge, can enhance the operation of the device. *See, e.g.*, Shinohara, [0095].

**2. Claim 33: “The device of claim 19, wherein the peripheral light trapping material comprises any of aluminum oxide and hafnium oxide.”**

134. Haddad188 in view of Shinohara teaches or suggests this limitation.

135. Shinohara discloses a *peripheral light trapping material that comprises any of aluminum oxide or hafnium oxide*. Specifically, Shinohara describes “an element isolation region 68 for isolating pixels.” Shinohara, [0090]. As shown below, Shinohara’s isolation region is formed with “an insulating film 69” formed within a “void 44” in the “p-type semiconductor layer 43.” Shinohara, [0090].

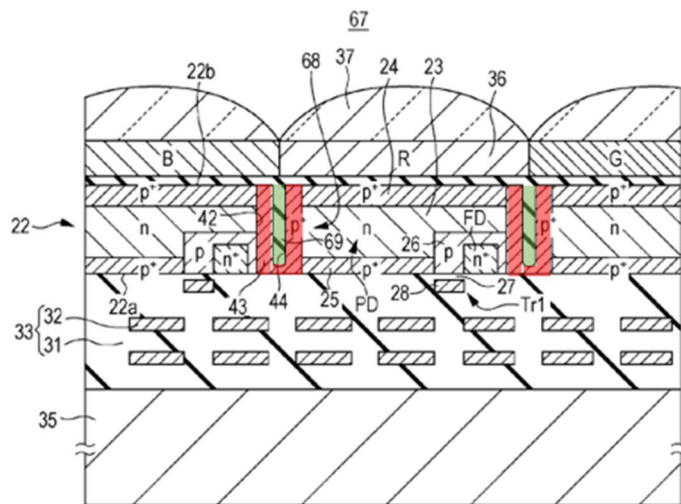
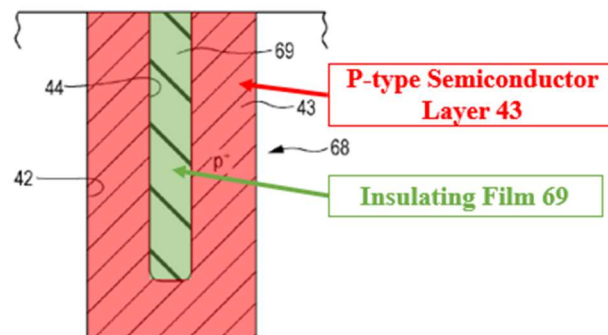


FIG. 9B



Shinohara Fig. 9 (annotated).

136. Shinohara explains that it is advantageous to make the “insulating film 69” a material having a negative fixed charge. Shinohara explains that “[w]hen the insulating film having a negative fixed charge is used as the insulating film 69, the hole pinning state by the p-type semiconductor layer 43 of the element isolation region 68 can be enhanced.” Shinohara, [0095]. In particular, “the generation of ... dark current can be further suppressed.” Shinohara, [0095]. Shinohara discloses examples of negative fixed charge materials, including, “hafnium dioxide ( $\text{HfO}_2$ )” or “dialuminum trioxide ( $\text{Al}_2\text{O}_3$ ).” Shinohara, [0091]. *See also* ’599 Patent, 9:53-59 (using “aluminum oxide” and “ $\text{Al}_2\text{O}_3$ ” interchangeably), 10:47-48 (“Hafnium oxide, which has a refractive index of about 1.9).<sup>6</sup>

137. A POSITA would be motivated to use Shinohara’s isolation region 68—including either of hafnium oxide or aluminum oxide—in place of Haddad188’s trench isolation 120 to achieve the benefit described above. Indeed, Haddad188 discloses that “[a] passivation layer can also be disposed on the photosensitive imager device to protect and/or reduce the dark current of the device.” Haddad188, 25:21-22. A

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<sup>6</sup> Based on this disclosure, A POSITA would recognize that “hafnium oxide” as used in the ’599 patent refers to  $\text{HfO}_2$ , which has a refractive index of about 1.9. Ex-1030, 7 (showing refractive index of  $\text{HfO}_2$  is between 1.70 and 1.91). Furthermore, hafnium oxide is commonly used to refer to  $\text{HfO}_2$ .

POSITA would have an expectation of success doing so, as Haddad188 explains that the “trench isolation [120] can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like.” Haddad188, 22:25-29. Furthermore, Shinohara’s isolation region 68 serves the same purpose as Haddad188’s trench isolation 120, e.g., Shinohara explains that “inclined incident light is reflected at the interface between the silicon and the insulating film [of the isolation region 68] and does not leak outside from the pixel, and hence no color mixture occurs.” Shinohara, [0094].

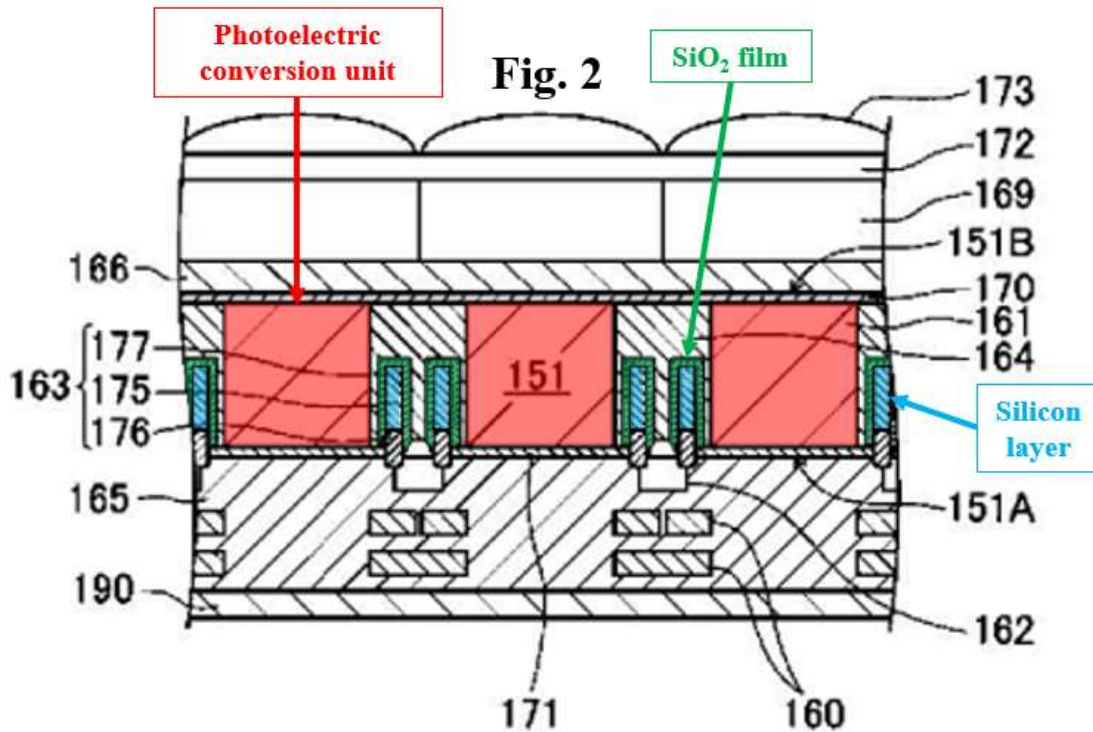
138. Accordingly, this limitation would have been obvious based on Haddad188 in view of Shinohara.

**C. Ground 3: Claims 1-14, 16-18, and 21-25 Are Rendered Obvious by Haddad188 in view of Mori**

**1. Overview of Mori**

139. Japanese Patent Application Publication No. 2011-119558 (“Mori”) (English translation, Ex-1008, original document, Ex-1009) is a Japanese patent application publication that I understand is prior art to the ’599 patent.

140. Mori is directed to a “solid-state imaging device”—i.e., an image sensor—in which the pixels are separated by a “partition part” comprising silicon and silicon oxide layers. Mori, [0012]-[0013]. An exemplary embodiment from Mori is depicted in Figure 2 below.



Mori, Fig. 2 (annotated).

141. Figure 2 is a cross-sectional view depicting three pixels in Mori's imaging device. Mori, [0020], [0022]. Specifically, Figure 2 depicts three "[p]hotoelectric conversion units 151," (i.e., pixels, highlighted red) which each "contain[] a photodiode." Mori, [0021]. Figure 2 also depicts a multi-layered "partition part 163" that separates these pixels, Mori, [0023], and serves to reduce "color mixing [or 'crosstalk'] due to obliquely incident light," Mori, [0027]. This partition part "has a silicon layer 175 formed on the light incident surface 151B side" (highlighted blue), Mori, [0028], and "a side SiO<sub>2</sub> film 177 formed on its bottom and side surfaces" (highlighted green), Mori, [0030]. Figure 2 also depicts an "isolation diffusion layer 164, which is a p-type diffusion layer." Mori, [0023].

142. Mori teaches that this multi-layer Si/SiO<sub>2</sub> partition solves a problem in conventional imaging devices, in which a partition member “made of a light-reflective material such as tungsten is formed inside the semiconductor substrate so as to separate adjacent pixels.” Mori, [0005]. As Mori explains:

A single crystal epitaxial layer cannot easily be formed on the embedded member because metal and silicon have different lattice constants. *Therefore, the silicon layer formed on the embedded member contains many crystal defects.* As a result, the charge generated when dark increases, and the sensitivity of the solid-state imaging device decreases.

Mori, [0007]. That is, the crystal defects can cause what is known in the art as “dark current”—i.e., the unwanted flow of electric charge when no light is incident on the photodiode (when the pixel should be “off”). *See* Ex-1020, 1:25-28 (“dark current, which is detected as a very small current when an electric charge (electron) generated from a minute defect in a substrate interference of a light receiving surface is input as a signal”).

143. To address these problems, Mori provides for a partition part having a silicon layer (e.g. layer 175) “made of amorphous silicon or polycrystalline silicon,” Mori, [0011], and a “side silicon oxide film [e.g., SiO<sub>2</sub> film 177] formed between the silicon layer and the semiconductor substrate embedded in a semiconductor substrate,” Mori, [0013]. “With this configuration, crystal defects on the side surface of the groove

for forming the partition part can be reduced, and the charges generated when dark can be reduced in order to achieve high sensitivity.” Mori, [0013].

144. Mori also discloses doping the SiO<sub>2</sub> film layer in order to further mitigate dark current stemming from crystal defects. Figure 3C below illustrates the formation of the Si/SiO<sub>2</sub> partition. First, the side SiO<sub>2</sub> film 177 is “formed on the side surface of [a] partition groove 174.” Mori, [0036]. Then, “[i]n order to prevent charges generated when dark due to crystal defects in the partition groove 174 from flowing into the photoelectric conversion unit 161, p-type impurities are preferably injected into the side walls of partition groove 174 after forming the side SiO<sub>2</sub> film 177.” Mori, [0036]. That is, the SiO<sub>2</sub> film 177 on the side walls is doped with p-type impurities, resulting in an excess of positively charged carriers (or “holes”). “Subsequently, a silicon layer 175 is formed in the partition groove 174,” in order to complete formation of the Si/SiO<sub>2</sub> partition. Mori, [0036].

**Fig. 3(b)**

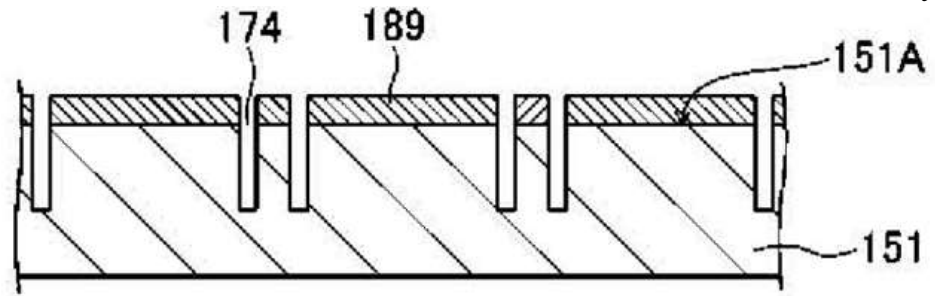
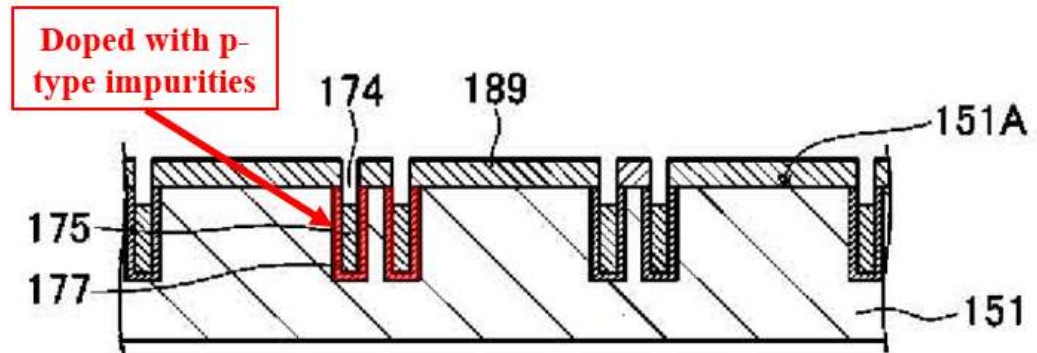


**Fig. 3(c)**



Mori, Figs. 3(b)-(c) (annotated).

## 2. Claim 1

### a) 1[pre]: “A light trapping device, comprising:”

145. To the extent the preamble is limiting, Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 19[pre] above.

### b) 1[a]: “at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;”

146. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 19[a] above.

**c) 1[b]: “a backside light trapping material at least partially covering the backside surface;”**

147. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 19[b] above.

**d) 1[c]: “a peripheral light trapping material substantially covering the peripheral sidewall, wherein said peripheral light trapping material is doped with a dopant to create a surface field; and”**

148. This limitation is obvious based on Haddad188 in view of Mori.

149. Haddad188 teaches or suggests *a peripheral light trapping material substantially covering the peripheral sidewall* for the reasons discussed for Ground 1, claim 19[c] above.

150. Haddad188 is broad in its disclosure of what its trench isolation can be made of: “trench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features.” Haddad188, 24:5-7. Haddad188 further explains that “[t]hese trench isolation regions can be configured to reflect incident light until it is absorbed, thereby increase the effective absorption length of the device.” Haddad188, 22:27-30.

151. Mori discloses a “partition part 163” that separates its pixels, and that, like Haddad188’s trench isolation 120, serves to reduce “color mixing [or ‘crosstalk’] due to obliquely incident light.” Mori, [0027]. Mori discloses that its partition part 163

has a silicon layer (e.g. layer 175) “made of amorphous silicon or polycrystalline silicon,” Mori, [0011], and a “side silicon oxide film [e.g., SiO<sub>2</sub> film 177] formed between the silicon layer and the semiconductor substrate embedded in a semiconductor substrate,” Mori, [0013]. Mori explains that “[w]ith this configuration, crystal defects on the side surface of the groove for forming the partition part can be reduced, and the charges generated when dark can be reduced in order to achieve high sensitivity.” Mori, [0013], [0029]-[0030].

152. It would have been obvious to use an Si/SiO<sub>2</sub> isolation element like that of Mori in Haddad188’s photosensitive pixel device to obtain the benefits described by Mori, i.e., reduced dark current and high sensitivity, and a POSITA would have had an expectation of success in doing so with predictable results. Indeed, it was well-known that layers of silicon and SiO<sub>2</sub> could be used as reflectors, *see, e.g.*, Schubert, 163, 173 (explaining that Si/SiO<sub>2</sub> DBRs “yield high reflectivity”), 177 (explaining that Si and SiO<sub>2</sub> are “natural candidates” for omnidirectional reflectors.”). In fact, Si/SiO<sub>2</sub> reflectors were commonly used as light trapping materials in similar image sensors. *See, e.g.*, Hwang, 9:25-30 (using silicon and silicon dioxide as alternating layers in its backside reflection layer); Suzunaga, [0035] (“The process of laminating a SiO<sub>2</sub> film and a polysilicon film has a proven track record in the manufacture of semiconductor integrated circuits, and a major advantage of this process is thought to be that there are no processing problems”). A POSITA would have further understood that the

reflectivity of the isolation element could be increased by increasing the number of alternating layers of Si and SiO<sub>2</sub> alternated in the isolation element. *See, e.g.*, Schubert 170 (“DBR’s reflectivity can be increased by increasing the number of reflector pairs...”).

153. It would have further been obvious to dope the light trapping material *with a dopant to create a surface field*. In particular, Mori teaches that it is advantageous to dope the silicon dioxide layer (Mori’s SiO<sub>2</sub> layer 177) with p-type impurities. As Mori explains, “[i]n order to prevent charges generated when dark due to crystal defects in the partition groove 174 from flowing into the photoelectric conversion unit 161, p-type impurities are preferably injected into the side walls of the partition groove 174 after forming the side SiO<sub>2</sub> film 177.” Mori, [0036].

154. The ’599 patent does not explain how doping peripheral light trapping material operates to create a surface field. Rather, its only disclosure relating to such doping is that: “[I]t can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.” ’599 patent, 10:14-18. Mori’s doped SiO<sub>2</sub> film 177 along the side of its pixel (photoelectric conversion unit 161) would constitute a *peripheral light trapping material doped with a dopant to create a surface field* to the extent that is contemplated by the limited disclosure of the ’599 patent.

155. As a POSITA would recognize, doping Mori's silicon dioxide layer with p-type impurities would lead to an excess of positive charges, creating an electric field at the surface of the layer. In other words, Mori teaches that its silicon dioxide layer *is doped with a dopant to create a surface field*.

- e) **1[d]: “a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel;”**

156. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 19[e] above.

- f) **1[e]: “wherein the reflective layer is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into the pixel.”**

157. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 19[f] above.

- 3. **Claim 2: “The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material reflects light incident thereon back into the pixel.”**

158. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 20 above.

- 4. **Claim 3: “The device of claim 1, wherein said peripheral light trapping material has a refractive index of less than about 2.1.”**

159. This limitation is obvious based on Haddad188 in view of Mori.

160. As discussed above with respect to claim 1[c], a POSITA would be motivated to use a multi-layer reflector comprising SiO<sub>2</sub> films. Silicon dioxide has a refractive index of about 1.46, which is *less than about 2.1*. See, e.g., Suzunaga [Table 1] (listing the refractive index of silicon dioxide as 1.43-1.46); Hwang, 9:28-29; Ex-1017, 181.

**5. Claim 4: “The device of claim 1, wherein said peripheral light trapping material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.”**

161. This limitation is obvious based on Haddad188 in view of Mori. As discussed above with respect to claim 1[c], a POSITA would be motivated to use a multi-layer reflector (e.g., a Bragg reflector) comprising SiO<sub>2</sub> films. Silicon dioxide is *an oxide*. Accordingly, Haddad188 in view of Mori teaches or suggests a *peripheral light trapping material* that includes an oxide.

**6. Claim 5: “The device of claim 4, wherein said peripheral light trapping material is selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.”**

162. This limitation is obvious based on Haddad188 in view of Mori. As discussed above with respect to claim 1[c], a POSITA would be motivated to use a multi-layer reflector (e.g., a Bragg reflector) comprising SiO<sub>2</sub> films. Accordingly, Haddad188 in view of Mori teaches or suggests a *peripheral light trapping material* that is *silicon dioxide*.

**7. Claim 6: “The device of claim 1, wherein the dopant is boron or antimony.”**

163. This limitation is obvious based on Haddad188 in view of Mori.

164. As explained for claim 1[c] above, it would have been obvious in view of Mori to dope the silicon dioxide layer of a multi-layer reflector with p-type impurities—i.e., a p-type dopant. It further would be obvious to use boron as the p-type dopant, given that boron is one of the most commonly used p-type dopants for Si-based systems. *See, e.g.*, Ex-1018 (explaining that Column-IV materials (e.g., Si) are commonly doped with Column-III-dopants (e.g., boron)). A POSITA would have recognized that using boron as a p-type dopant for silicon-based systems is a known technique that would have yielded predictable results, particularly in light of boron’s similar use as a p-type dopant in other similar light trapping devices. *See, e.g.*, Ex-1021, [0011] (“[t]he substrate 35 is a silicon substrate doped with a P-type dopant such as boron, in which case the substrate 35 is a P-type substrate”). Furthermore, Haddad188 itself discloses using boron as a dopant. Haddad188, 18:5-7 (“non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof”). Additionally, this limitation would have been obvious, because a POSITA would have had a limited number of types of p-type dopants from which to choose, therefore, it would have been obvious to a POSITA to try using boron as the p-type dopant.

165. Accordingly, Haddad188 in view of Mori teaches or suggests that *the dopant is boron or antimony*.

**8. Claim 7: “The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.”**

166. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 26 above.

**9. Claim 8: “The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”**

167. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 27 above.

**10. Claim 9: “The device of claim 1, wherein said aperture has an effective surface area of less than about 90% of total area of the incident light surface.”**

168. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 28 above.

**11. Claim 10: “The device of claim 1, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.”**

169. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 29 above.

- 12. Claim 11: “The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”**

170. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 30 above.

- 13. Claim 12: “The device of claim 1, further comprising a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device.”**

171. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 19[d] above.

- 14. Claim 13: “The device of claim 12, wherein said textured region comprises a textured film layer.”**

172. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 31 above.

- 15. Claim 14: “The device of claim 13, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”**

173. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 32 above.

- 16. Claim 16: “The device of claim 1, wherein the backside light trapping material substantially covers the backside surface.”**

174. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 34 above.

**17. Claim 17: “The device of claim 1, wherein the backside light trapping material completely covers the backside surface.”**

175. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 35 above.

**18. Claim 18: “The device of claim 1, wherein said peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.”**

176. Haddad188 teaches or suggests this limitation for the reasons discussed for Ground 1, claim 36 above.

**19. Claim 21: “The device of claim 19, wherein said peripheral light trapping material has a refractive index of less than about 2.1.”**

177. This limitation is obvious based on Haddad188 in view of Mori for the reasons discussed for Ground 3, claim 3 above.

**20. Claim 22: “The device of claim 19, wherein said peripheral light trapping material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.”**

178. This limitation is obvious based on Haddad188 in view of Mori for the reasons discussed for Ground 3, claim 4 above.

**21. Claim 23: “The device of claim 22, wherein said peripheral light trapping material is selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.”**

179. This limitation is obvious based on Haddad188 in view of Mori for the reasons discussed for Ground 3, claim 5 above.

**22. Claim 24: “The device of claim 19, wherein said peripheral light trapping material is doped with a dopant to create a surface field.”**

180. This limitation is obvious based on Haddad188 in view of Mori for the reasons discussed for Ground 3, claim 1[c] above.

**23. Claim 25: “The device of claim 24, wherein the dopant is boron or antimony.”**

181. This limitation is obvious based on Haddad188 in view of Mori for the reasons discussed for Ground 3, claim 6 above.

**D. Ground 4: Claim 15 is Obvious Based on Haddad188, Mori, and Shinohara**

**1. Claim 15: “The device of claim 1, wherein the peripheral light trapping material comprises any of aluminum oxide and hafnium oxide.”**

182. This limitation is obvious based on Haddad188 in view of Mori and Shinohara.

183. Shinohara discloses a *peripheral light trapping material that comprises any of aluminum oxide or hafnium oxide*. Shinohara describes “an element isolation region 68 for isolating pixels.” Shinohara, [0090]. As shown below, Shinohara’s isolation region is formed with “an insulating film 69” formed within a “void 44” in the “p-type semiconductor layer 43.” Shinohara, [0090].

A cross-sectional view of a semiconductor device. It shows a central vertical layer labeled 69, which is green and has diagonal hatching. This layer is surrounded by a red layer labeled 43. The red layer has a wavy top surface. A red arrow points from the text 'P-type Semiconductor Layer 43' to the red layer. A green arrow points from the text 'Insulating Film 69' to the green layer. Other labels include 44, 42, and 68, which point to various features on the left side of the device.

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or “dialuminum trioxide ( $\text{Al}_2\text{O}_3$ ).” Shinohara, [0091]. *See also* ’599 Patent, 9:53-59 (using “aluminum oxide” and “ $\text{Al}_2\text{O}_3$ ” interchangeably), 10:47-48 (“Hafnium oxide, which has a refractive index of about 1.9”).<sup>7</sup>

185. A POSITA would be motivated to use either of Shinohara’s hafnium oxide or aluminum oxide in Haddad188’s trench isolation 120 to achieve the benefit described above. Indeed, Haddad188 discloses that “[a] passivation layer can also be disposed on the photosensitive imager device to protect and/or reduce the dark current of the device.” Haddad188, 25:21-22. And Mori’s doping process similarly results in “charges generated when dark [being] reduced,” i.e., reduced dark current. Mori, [0013]. A POSITA would have had an expectation of success in substituting Shinohara’s hafnium oxide or aluminum oxide in place of the silicon in the Si/SiO<sub>2</sub> layers used according to the combination of Haddad188 and Mori discussed above. *See, e.g.*, Suzunaga, [0067] (“[T]he film having a high refractive index is not necessarily limited to a semiconductor material, but may be for example, any one of ...  $\text{Al}_2\text{O}_3$  ... and the like as depicted in Table 1, and may be combined with a film

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<sup>7</sup> Based on this disclosure, A POSITA would recognize that “hafnium oxide” as used in the ’599 patent refers to HfO<sub>2</sub>, which has a refractive index of about 1.9. Ex-1030, 7 (showing refractive index of HfO<sub>2</sub> is between 1.70 and 1.91). Furthermore, hafnium oxide is commonly used to refer to HfO<sub>2</sub>.

having a low refractive index, such as  $\text{SiO}_2$ ....”). Shinohara surrounds its negative fixed charge material with a p-type semiconductor layer 43. As discussed above, utilizing Mori’s doping process results in a more heavily doped region, similar to Shinohara’s p-type semiconductor layer 43. A POSITA would therefore recognize that the modification is structurally compatible.

186. Accordingly, this limitation would have been obvious based on Haddad<sup>188</sup> in view of Mori and Shinohara.

**E. Ground 5: Claims 19-23, 26-32, 34, and 36 are Obvious Based on Hwang and Konno**

**1. Overview of Hwang**

187. U.S. Patent No. 7,675,099 (“Hwang”) (Ex-1010) is a U.S. patent that I understand is prior art to the ’599 patent. It is directed to “an image sensor with an increased spectral sensitivity,” that is “capable of minimizing interference between neighboring pixels” through use of a “base multi-layered reflection layer” and a “side wall multi-layered reflection layer.” Hwang, 1:52-67.

188. Hwang identifies a problem in that longer wavelength light is less likely to be absorbed completely by a photodiode, thus reducing spectral sensitivity. Hwang, 1:41-48. Similar to the ’599 patent, Hwang is concerned with improving image quality by increasing the percent of incident light absorbed by the photodiode. Hwang, 1:31-36. As Hwang explains, “[t]he higher the percentage of incident light absorbed by the photodiode, the higher the spectral sensitivity.” Hwang, 1:31-34.

189. To that end, Hwang discloses an image sensor with base and sidewall

image sensor and a cross-sectional view of an image sensor, respectively. Hwang,

4:59-63.

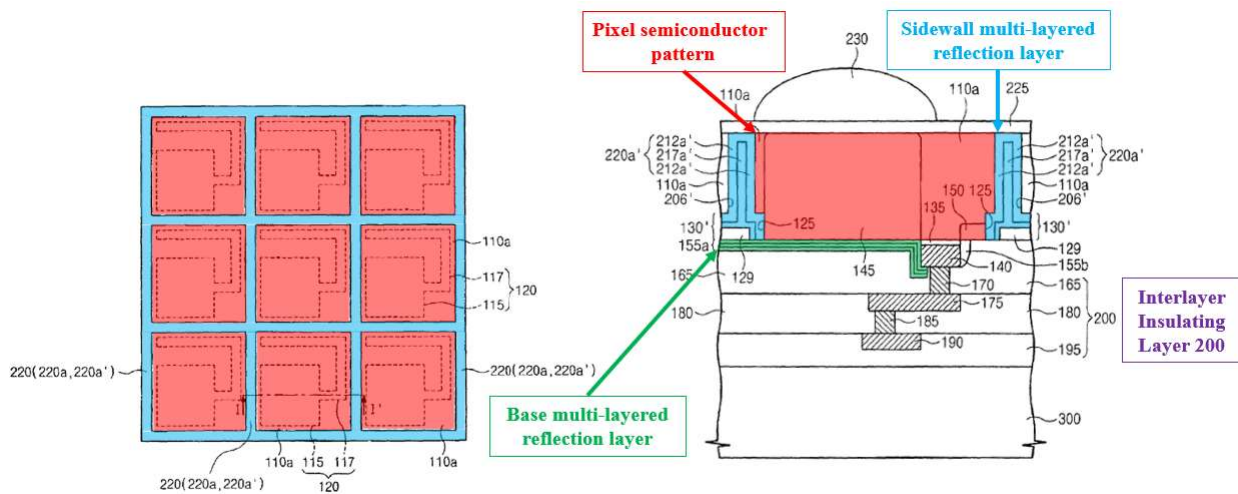


**Fig. 1**

**Fig. 6**

Hwang Figs. 1, 6.<sup>8</sup> Figure 6 depicts a “pixel semiconductor pattern 110a [that] has a

photodiode 145 disposed therein,” Hwang, 5:57-58, “[a] base multi-layered

<sup>8</sup> Figure 6 uses differently arranged sidewall multi-layered reflection layers than Hwang's first embodiment (Figure 2) but otherwise is the same as Hwang's first embodiment. *See* Hwang, 11:57-60. Therefore, a POSITA would appreciate that Hwang's disclosures for elements in Figure 2 (including layer 220 comprising layers 210 and 215) are pertinent to corresponding elements in Figure 6 (including layer 220a' comprising layers 212a' and 217a').

reflection layer 155a,” Hwang, 7:45-47, and a “sidewall multi-layered reflection layer 220a’,” Hwang, 11:64-67.

190. As Hwang explains, these base and sidewall reflection layers serve to increase light sensitivity of the sensor and reduce interference across pixels:

[A] base multi layered reflection layer is disposed between the photodiode and the interlayer insulating layer. Thus, light that is incident on the photodiode is ***reflected by the base multi-layered reflection layer*** and re-enters the photodiode. Resultantly, the ***sensitivity of the image sensor is improved***.

Also, a sidewall multi-layered reflection layer encloses the sidewalls of the pixel semiconductor patterns forming the photodiode. Therefore, incidence of the light reflected by the base multi-layered reflection layer on neighboring pixels can be minimized. As a result, interference between pixels can be minimized by the sidewall multi-layered reflection layer.

191. Hwang, 15:36-48; *see also* Hwang, 8:61-9:14, 10:19-40. Thus, as explained further below, Hwang discloses a *light trapping device* including a *backside light trapping material* (base reflection layer) and *peripheral light trapping material* (sidewall reflection layer), in accordance with the challenged claims.

## 2. Overview of Konno

192. U.S. Patent No. 7,709,775 (“Konno”) (Ex-1011) is a U.S. patent that I understand is prior art to the ’599 patent. It is directed to a “solid-state imaging element,”—i.e., an image sensor. Konno, Abstract. Like the ’599 patent, Konno is

concerned with increasing image quality by using reflective surfaces to increase the amount of incident light absorbed by the photodiode. *See generally* Konno, 2:49-55.

193. For example, as shown in Figure 7 below, the “second reflecting layer 120 and the first reflecting layer 121 sandwich the ... photoelectric conversion element 135.” Konno, 8:22-25. As Konno explains, “[t]he second reflecting layer 120 and the first reflecting layer 121 have a function of confining photons which entered into the solid-state imaging element [] between the both,” Konno, 8:31-33, and, as a result “most of the photons can be absorbed with the photoelectric conversion film 125,” Konno, 10:8-13, to improve sensitivity. Konno explains that the “second reflection layer 120, ...can be formed by forming a thin film of a metal such as aluminum and silver by deposition or the like.” Konno, 8:31-38. Figures 3 and 8 also depict a “microlens 122” which “concentrates photons which entered into the solid-state imaging element 110, and leads them to the light entrance window 128.” Konno, 9:4-9. Figure 7 of Konno further depicts transparent layer 136 that is textured by forming “concaves and convexes on [its] surface.” Konno, 14:38-42.

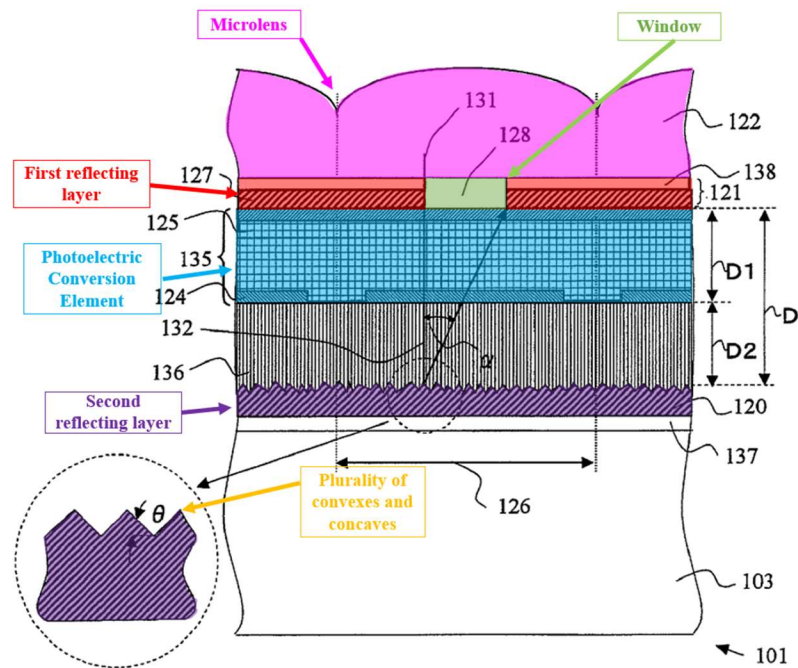


Fig.7

Konno, Figs. 3, 7 (annotated).<sup>9</sup>

194. Konno further explains that its sensor includes “a transparent layer or layers disposed between the first electrode and first reflecting layer and/or between the second electrode and the second reflecting layer.” Konno, 3:16–19. The shape of these transparent and reflecting layers “makes it possible to reflect photons . . . and therefore

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<sup>9</sup> Figure 7 is a sectional view of the photo-detector of Kono’s second embodiment. *See* Konno, 13:50-57. Konno explains that “[t]he other configurations are the same as those of the first embodiment.” Konno, 13:57-59. Accordingly, disclosures that Konno makes with respect to the first embodiment are discussed herein with respect to the second embodiment.

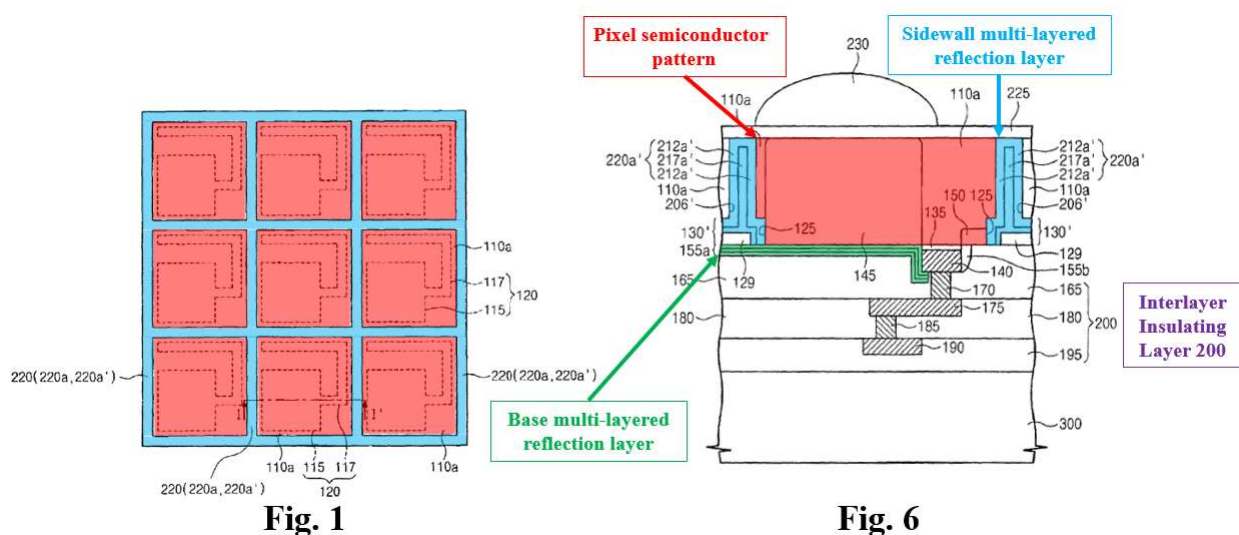
the amount of photons to be detected again by the photoelectric conversion film 125 can be increased” and that this structure “can be manufactured by, for example, forming concaves and convexes on the surface of the transparent layer 136 ... and then depositing a metal thereon to produce the reflecting layer 120.” Konno, 13:66-14:3, 14:38-45.

### 3. Claim 19

#### a) 19[pre]: “A light trapping device, comprising:”

195. To the extent the preamble is limiting, Hwang teaches or suggests it.

196. Hwang discloses an “image sensor that converts incident light to electrical signals.” Hwang, 1:14-18. For example, Figure 1 shows “a plan view of an image sensor,” Hwang, 4:59-60, and Figure 6 shows a “sectional view of FIG. 1 ... for describing an alternate embodiment of an image sensor...” Hwang, 5:8-10.



Hwang Figs. 1, 6 (annotated).

197. Hwang discloses a “sidewall multi-layered reflection layer 220a’ is disposed within a groove 206’ formed between pixel semiconductor patterns 110a’.” Hwang, 11:64-66. Hwang further discloses “[a] base multi-layered reflection layer 155a is interposed between the photodiode 145 and the interlayer insulating layer 200,” Hwang, 7:45-47, which as discussed below could be replaced with Konno’s second reflecting layer 120.

198. These reflective layers allow Hwang’s image sensor to trap light by reflecting light back into the pixel. *See, e.g.*, Hwang, 9:10-11 (“The light reflected by the ... surfaces [of the base multi-layered reflection layer 155a] is incident again on the photodiode 145.”); 10:28-35 (“Light ... is also reflected by the [surfaces] within the sidewall multilayered reflection layer 220 [layer 220a’ in Figure 6]. As a result ... absorption efficiency of external light is increased.”); 15:36-48. Accordingly, Hwang’s image sensor constitutes a *light trapping device*.

**b) 19[a]: “at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;”**

199. Hwang teaches or suggests this limitation.

200. Hwang’s image sensor comprises *at least one light sensitive pixel*. For example, Hwang’s image sensor includes “a plurality of pixel semiconductor patterns 110a,” that are “arranged two-dimensionally in rows and columns,” Hwang, 5:52-59, as shown in annotated Figures 1 and 6 below. Hwang explains that “[e]ach

pixel semiconductor pattern 110a has a photodiode 145 disposed therein.” Hwang, 5:57-58. As Hwang further explains, “[a] photodiode is a representative type of light receiver. When external light is incident on a depletion region in the photodiode, electron-hole pairs are generated, and the external light is converted to electrical signals.” Hwang, 1:23-29. Therefore, each pixel semiconductor pattern 110a comprises a *light sensitive pixel*.<sup>10</sup>

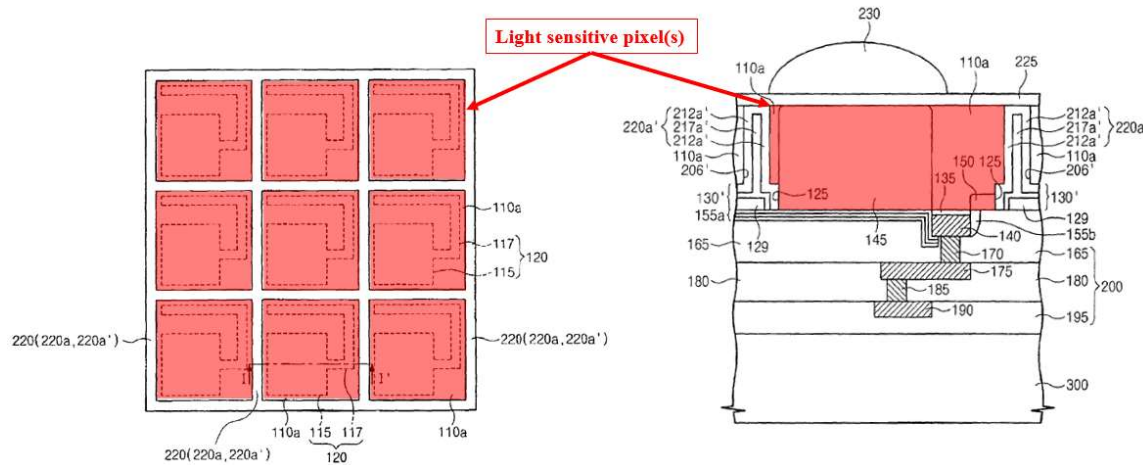


Fig. 1

Fig. 6

Hwang Figs. 1, 6 (annotated).

<sup>10</sup> While Hwang calls element 145 a “photodiode,” a POSITA would understand that term (i.e., the structure that converts light into an electrical signal) encompasses more than just element 145, and would further include the surrounding pixel semiconductor patterns 110a. The photodiode comprises a junction created between the differently doped semiconductor regions. See Hwang, 5:52-6:6 (“photodiodes 145 form a PN junction with the pixel semiconductor pattern 110a”).

201. Hwang further discloses that each pixel has a *light incident surface* and a *backside surface opposite the light incident surface*, as illustrated below.

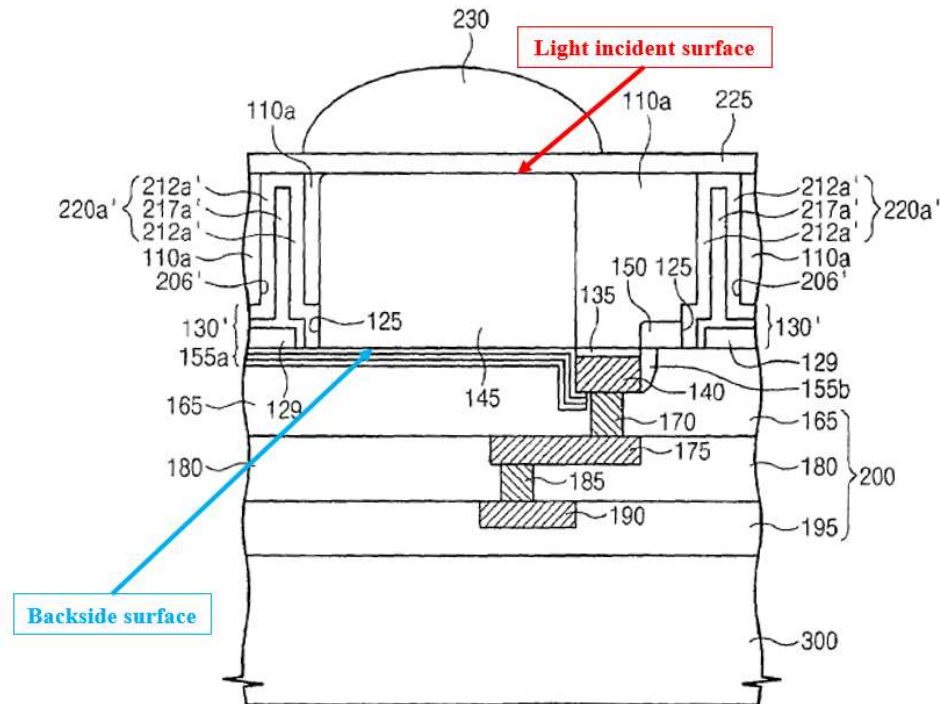


**Fig. 6**

Hwang, Fig. 6 (annotated).

202. Hwang explains that “[t]he pixel semiconductor patterns 110a have first and second surfaces in parallel, i.e., that face one another,” where “the first surface of a pixel semiconductor pattern 110a is more proximate to the substrate 300 than is the second surface.” Hwang, 6:37-40.

203. Hwang’s “second surface” constitutes a *light incident surface*. Hwang explains that “[a] color filter 225 is disposed on the second surface of the pixel semiconductor pattern 110a, and a micro lens 230 that covers the photodiode 145 is disposed on the color filter 225. External light passes through the micro lens 230 and

the color filter 225, and is incident on the second surface of the photodiode 145.”

Hwang, 8:17-22.

204. Hwang’s “first surface,” in turn, constitutes a *backside surface opposite the light incident surface*. Hwang explains that “the first surface of a pixel semiconductor pattern 110a is more proximate to the substrate 300 than is the second surface.” Hwang, 6:38-40. “[T]he first surface of the photodiode 145 is coplanar with the first surface of the pixel substrate pattern 110a.” Hwang, 6:63-65. “The first surface of the floating doped region 150 shares the same surface with the first surface of the pixel semiconductor pattern 110a.” Hwang, 7:40-42.

205. Each pixel further has a *peripheral sidewall*, as illustrated below.

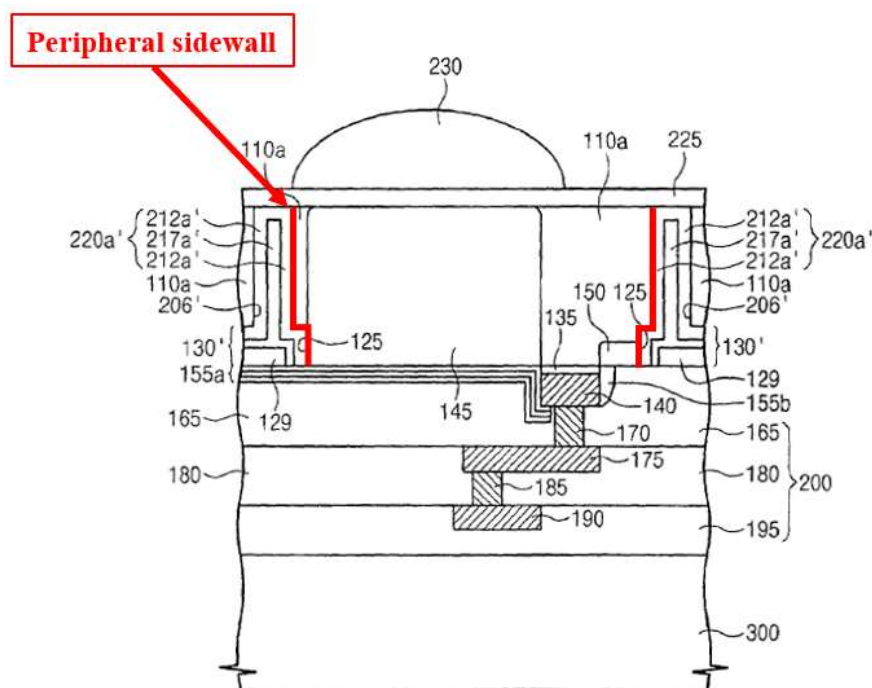


**Fig. 6**

Hwang, Fig. 6 (annotated).

206. Hwang discloses a “sidewall multi-layered reflection layer 220a’ is disposed within a groove 206’ formed between pixel semiconductor patterns 110a’.” Hwang, 11:64-66. Hwang further discloses that “[a] sidewall multi-layered reflection layer 220 [layer 220a’ in Figure 6] is provided between the side walls of the pixel semiconductor pattern 110a,” as shown in Figure 6. Hwang, 6:7-9. That is, Hwang discloses that its pixel semiconductor pattern 110a includes a *peripheral sidewall* where the pixel 110a contacts the sidewall reflection layer 220a’.

207. Hwang further discloses the peripheral sidewall *extending at least partially around the pixel periphery*. As illustrated in Figure 1 below, “[t]he sidewall multi-layered reflection layer 220 [layer 220a’ in Figure 6] encloses the side walls of the pixel semiconductor patterns 110a.” Hwang, 6:15-17. Thus, the *peripheral sidewall* (where the pixel 110a contacts the sidewall reflection layer 220a’) *extend[s] at least partially around the pixel periphery*.

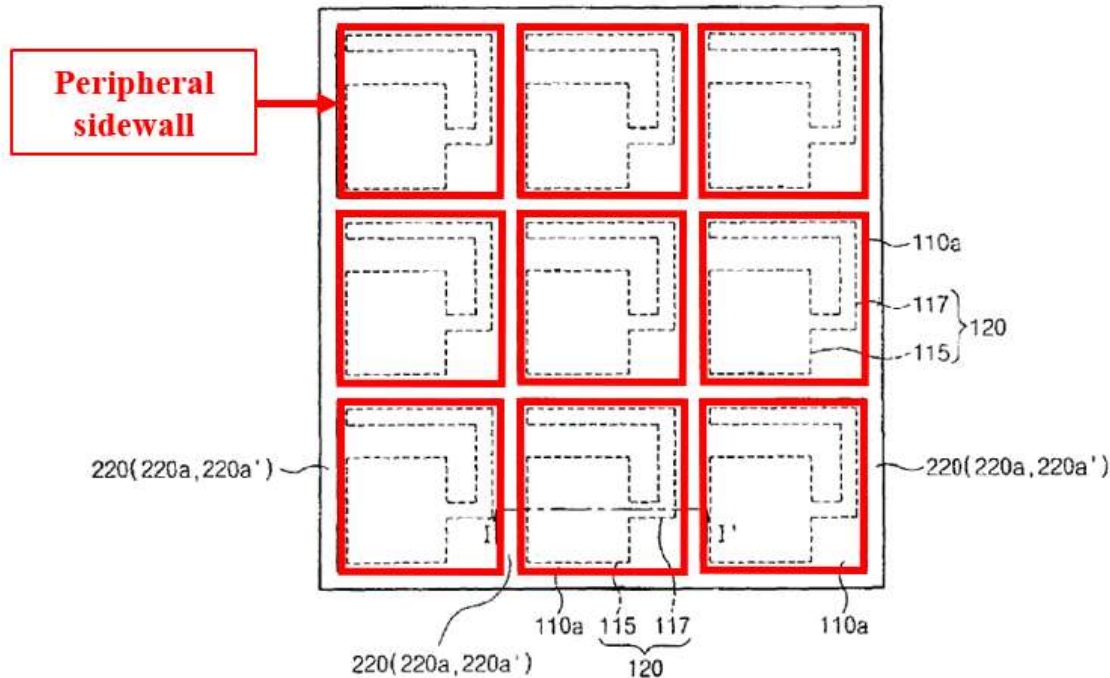


**Fig. 1**

Hwang, Fig. 1 (annotated).

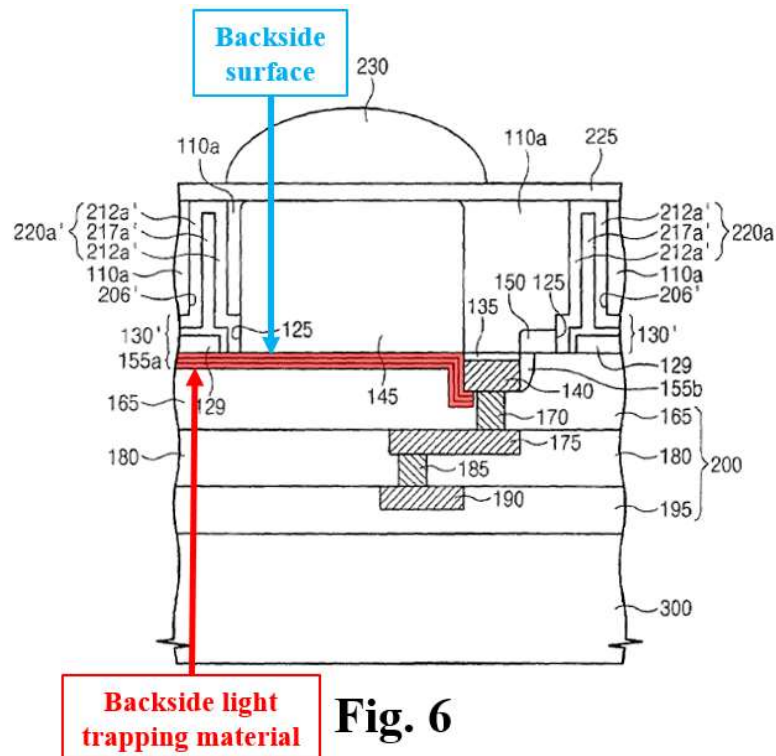
208. Accordingly, Hwang's image sensor comprises *at least one light sensitive pixel* that meets the requirements of this limitation.

- c) 19[b]: "a backside light trapping material at least partially covering the backside surface;" and  
19[d]: "a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device; and"

209. These limitations would have been obvious based on Hwang in view of Konno.

210. *First*, Hwang's image sensor includes a *backside light trapping material at least partially covering the backside surface* of the pixel. Hwang

discloses that a “base multi-layered reflection layer 155a is interposed between the photodiode 145 and the interlayer insulating layer 200,” Hwang, 7:45-47, as shown in the annotated Figures below.



Hwang Fig. 6 (annotated).

211. This base reflection layer 155a traps light by reflecting light back into the pixel, and therefore constitutes a *light trapping material*. As Hwang explains, “external light incident on the second surface of the photodiode 145 is reflected by the first boundary surface and at least one second boundary surface within the base multi-layered reflection layer 155a.” Hwang, 9:6-10. Therefore, the light reflected by the multi-layered reflection layer 155a “is incident again on the photodiode,” thus “increas[ing] the light sensitivity of the image sensor.” Hwang, 9:11-14. Further,

Hwang's base multi-layer reflection layer 155a *at least partially cover[s] the backside surface*. Hwang explains that "the base multi-layered reflection layer 155a contacts the first surface of the pixel semiconductor pattern 110a on which the photodiode 145 is formed," as shown in Figure 6 above. Hwang, 8:32-35. As explained for limitation 19[a] above, the "first surface" constitutes the claimed *backside surface* of the pixel.

212. Konno discloses in its Figure 7 embodiment a solid-state imaging element including a transparent layer 136 that is textured by "forming concaves and convexes on [its] surface." Konno, 14:38-42. Figure 7 below depicts the textured features of transparent layer 136 (including the complimentary texturing of the second reflecting layer 120).

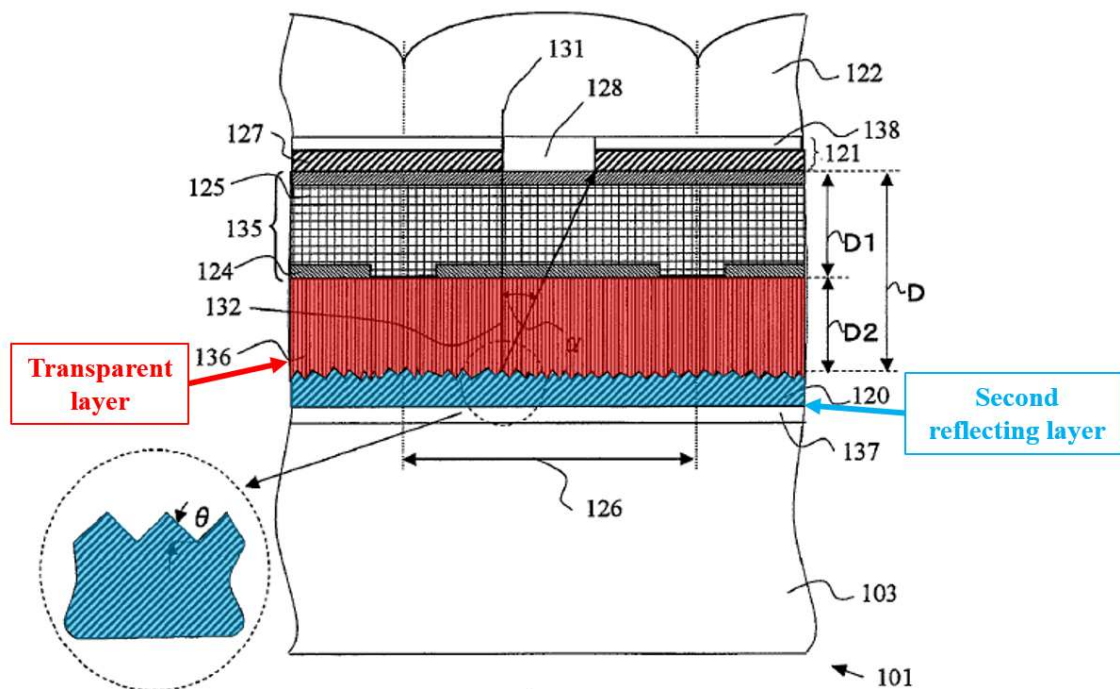


**Fig. 7**

Konno, Fig. 7 (annotated).

213. Konno's "transparent layer 136" comprises a *textured region*. The '599 patent states that "[t]he textured region 312 can have surface features configured to reflect and disperse light." '599 patent, 11:2-4. The texturing can be created "across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern." '599 patent, 14:47-52. Konno likewise discloses that the concaves and convexes are formed "on the surface of the transparent layer 136 before producing the reflecting layer 120, and then depositing a metal thereon to produce the reflecting layer 120." Konno, 14:38-42. According to Konno, "by providing a transparent layer in the solid-state imaging element of the present invention, convexes or concaves or a structure effective for reflecting or scattering photons can be realized in the reflecting layer adjacent to the transparent layer." Konno, 3:58-62. As in the '599 patent, Konno discloses that "[t]he concaves and convexes of the transparent layer 136 can be formed by a known technique such as sputtering and microlithography." Konno, 14:42-45.

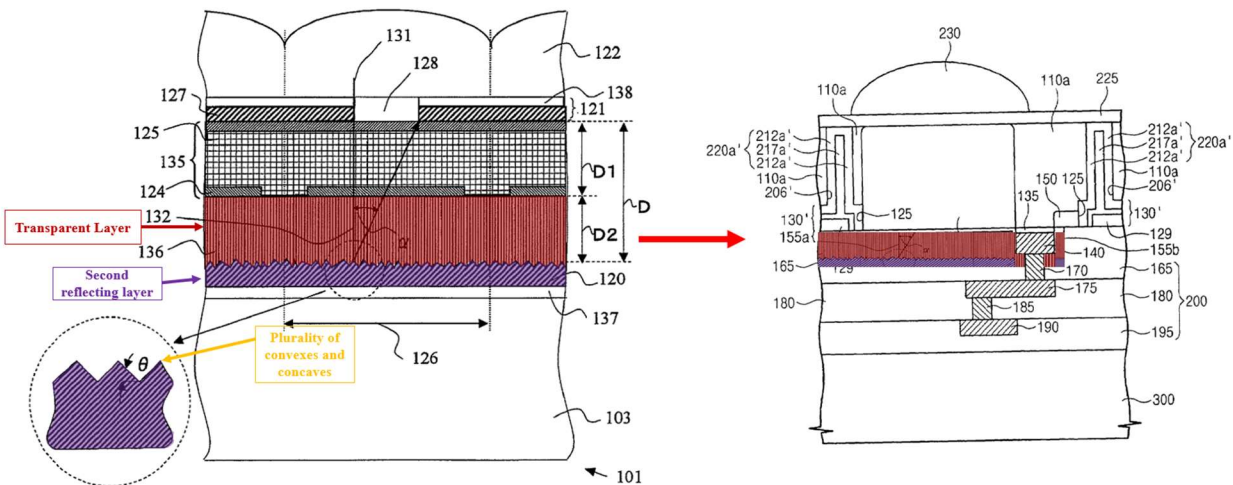
214. Konno discloses that the textured layer is *positioned to interact with light incident thereon to increase quantum efficiency of the device*. As shown in Figure 7 above, Konno's transparent layer is formed between the backside surface of photoelectric conversion element 135 and reflecting layer 120. *See also* Konno, 2:56-57 (disclosing "a structure where the first reflecting layer and the second

reflecting layer sandwich the photoelectric conversion means together with the transparent layer”). Konno further discloses that the transparent layer “transmits photons” and “can provide concaves and convexes which realizes a large reflection angle.” Konno, 4:54-58, 15:2-6. Konno explains that texturing the transparent layer “makes it possible to reflect photons which entered from the light entrance window 128 to the first reflecting layer 121, and therefore the amount of photons to be detected again by the photoelectric conversion film can be increased.” Konno, 13:66-14:3.

215. Konno’s solid-state imaging element includes a second reflecting layer 120 constituting *a backside light trapping material*. Specifically, Konno discloses “[t]he second reflection layer 120,” which “can be formed by forming a thin film of a metal such as aluminum and silver by deposition or the like,” as shown in annotated Figure 7 above. Konno, 8:31-38.

216. A POSITA would have been motivated to replace Hwang’s base multi-layered reflection layer 155a with Konno’s textured transparent layer 136 and second reflecting layer 120 to similarly cover the backside surface. As discussed above, Konno explains that texturing the transparent layer “makes it possible to reflect photons which entered from the light entrance window 128 to the first reflecting layer 121, and therefore the amount of photons to be detected again by the photoelectric conversion film can be increased.” Konno, 13:66-14:3.

217. Hwang similarly discloses a benefit to configuring its image sensor such that light that reflects off the backside reflecting material also reflects off of the peripheral light reflecting material in order to increase the path of the light and maximize the absorption efficiency of the pixel. *See* Hwang, 10:28-35 (“[l]ight that is reflected from the first and second boundary surfaces,” i.e. light that reflects off of the base multi-layered reflection layer, “is also reflected by the third boundary surface and also the fourth boundary surface within the sidewall multi-layered reflection layer 220” and that, as a result, “the absorption efficiency of external light is increased.”); *see also* Hwang, 8:61-9:14. A POSITA would be furthermore motivated to alter Hwang to incorporate Konno’s transparent and reflecting layers to achieve this mutually-recognized goal.



Konno, Fig. 7 (annotated); Hwang, Fig. 6 (annotated, modified).

218. Konno further explains that “when the reflecting layers 120 and 121 consist of metals, it is also possible to electrically connect at least one of these to ground or electrode potential of a read-out circuit, a control circuit, a power supply or the like.” Konno, 12:29-31. Konno explains that “[b]y using such a [metal] structure, error signals and noises generated in output signals of the photodetector 101 by external noises which flow in from the outside and flow into the photo-detector 101 and detected in the photoelectric conversion element 135, wiring or the like can be thereby reduced.” Konno, 12:33-38.

219. A POSITA would have had a reasonable expectation in making such a modification, i.e., replacing Hwang’s base multi-layered reflection layer 155a with Konno’s textured transparent layer 136 and second reflecting layer 120. For example, the textured transparent layer 136 and second reflecting layer 120 could be incorporated into Hwang between the manufacturing steps occurring immediately after what is shown in Figure 22, or in between the manufacturing steps shown in Hwang’s substantially similar embodiment depicted in Figures 8 and 9.

220. Konno explains that its transparent layer 136 is “formed from a material which transmits photons, for example, glass....” Konno, 9:35-41. Hwang already discloses forming a layer of SiO<sub>2</sub>, i.e., glass, on the backside surface. Hwang, 8:40-52 (“The base multi-layered reflection layer 155a can include a first base multi-layered reflection layer 151....”); Hwang, 9:25-30 (explaining that the “first base multi-layered

reflection layer 151” is “formed of silicon [di]oxide (with a refractive index of approximately 1.46).”). Accordingly, a POSITA would recognize that the transparent layer 136 and second reflecting layer 120 could be readily implemented in Hwang.

221. Therefore, it would have been obvious in view of Konno to form *a backside light trapping material at least partially covering the backside surface, along with a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device*, in Hwang’s image sensor.

**d) 19[c]: “a peripheral light trapping material substantially covering the peripheral sidewall;”**

222. Hwang teaches or suggests this limitation.

223. Hwang’s image sensor includes *a peripheral light trapping material substantially covering the peripheral sidewall*. Hwang discloses that a “sidewall multi-layered reflection layer 220a’ is disposed within a groove 206’ formed between pixel semiconductor patterns 110a,” as shown in Figure 6 below. Hwang, 11:64-66. Hwang also discloses that “sidewall multi-layered reflection layer 220 [layer 220a’ in Figure 6] is disposed between the side walls of the pixel semiconductor pattern 110a.” Hwang, 9:41-43.

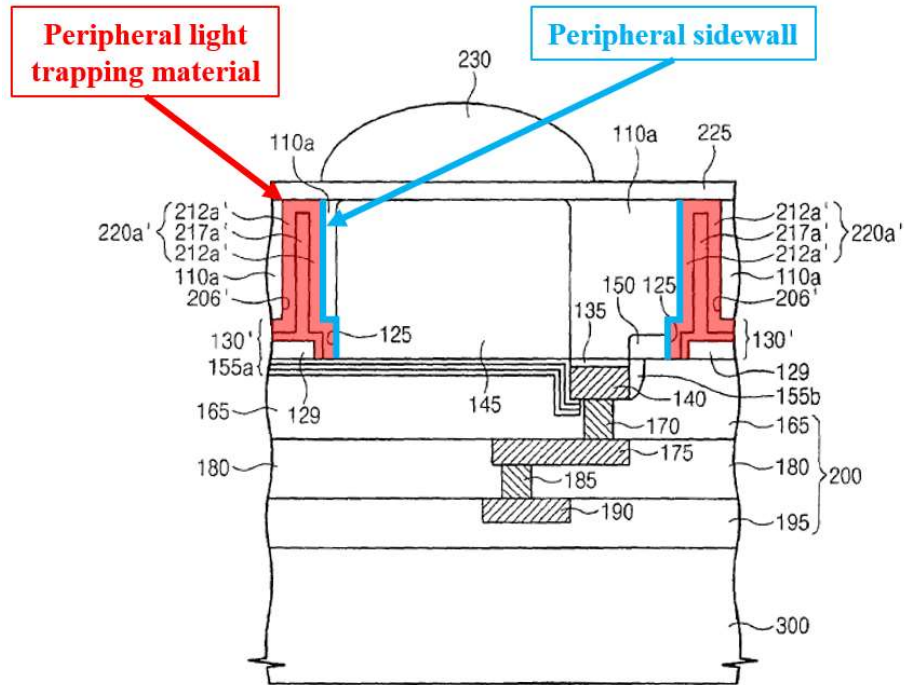


**Fig. 6**

Hwang, Fig. 6 (annotated).

224. This sidewall reflection layer 220a' serves to reflect light and minimize interference across pixels, and therefore constitutes a *light trapping material*. As Hwang explains, “the sidewall multi-layered reflection layer 220 [layer 220a' in Figure 6] minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels. Therefore, interference of the image sensor can be minimized.” Hwang, 10:23-27. Additionally, light “is also reflected by [surfaces] within the sidewall multilayered reflection layer 220 [layer 220a' in Figure 6]. As a result, the portion of the light reflected toward the sidewall multi-layered reflection layer 220 [220a' in Figure 6] ... is incident again on the photodiode 145, so that the absorption efficiency of external light is increased.” Hwang, 10:29-35.

225. Further, Hwang's sidewall reflection layer 220*a*' *substantially cover[s] the peripheral sidewall*. Hwang explains that "[t]he sidewall multi-layered reflection layer 220 [220*a*' in Figure 6] encloses the side walls of the pixel semiconductor pattern 110*a*," Hwang, 6:15-17, and that "[t]he sidewall multi-layered reflection layer 220 [220*a*' in Figure 6] can contact the side walls of the pixel semiconductor patterns 110*a*," as shown in Figure 6. Hwang, 9:43-45.

226. Accordingly, Hwang's sidewall multi-layered reflection layer 220*a*' comprises *a peripheral light trapping material at least partially covering the peripheral sidewall*.

- e) **19[e]: "a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel;"**

227. This limitation would have been obvious based on Hwang in view of Konno.

228. Konno's solid-state imaging element includes a first reflecting layer 121 that constitutes a *reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel*, as recited in this limitation. As part of its image sensor, Konno discloses that its "solid-state imaging element 110 has a structure where a reflecting layer (second reflecting layer) 120, a transparent layer 136, a photoelectric conversion element 135, a reflecting layer (first reflecting layer 121) and microlens 122 are formed on a substrate 103," to improve detection

sensitivity, as shown in the annotated Figure 3 below. Konno, 8:18-22. A “light entrance window 128 [i.e., an aperture] through which the incident photons 132 transmit is formed in the first reflecting layer 121.” Konno, 8:56-58.

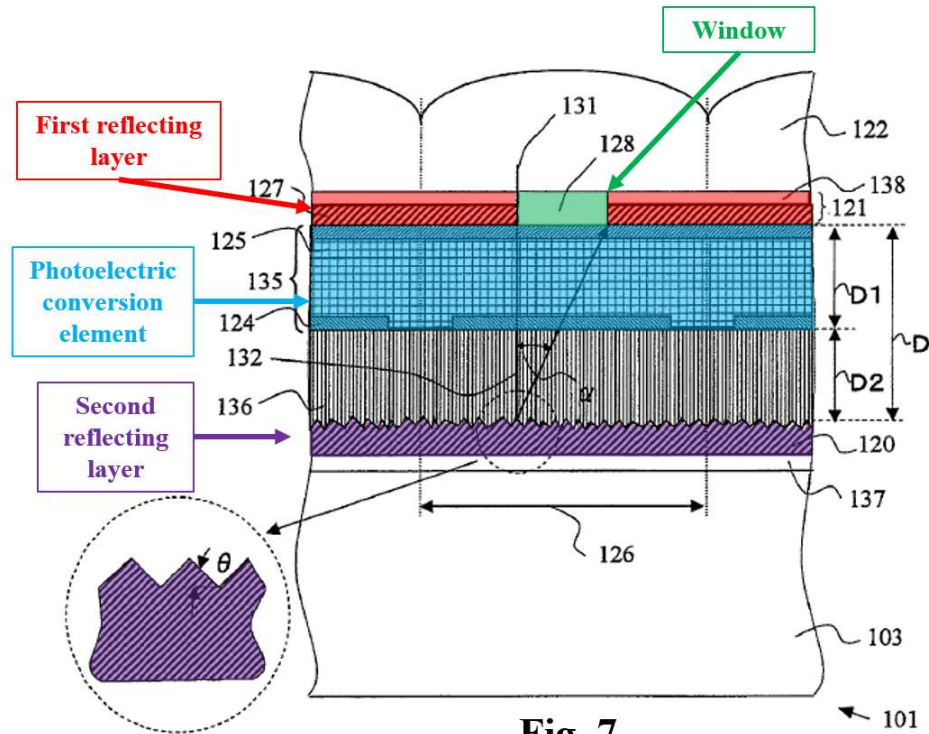


**Fig. 7**

Konno, Fig. 7 (annotated).

229. Konno explains that “photons which entered from the light entrance window 128 can be effectively confined between the first and second reflection layers 121 and 120 to ... improve detection sensitivity.” Konno, 11:65-12:3. Konno explains that “a part of the photons which passed through the photoelectric conversion film 125 reach the reflecting surface 127 of the first reflecting layer [121], are reflected again, and reach the photoelectric conversion film 125 ....” Konno, 10:4-8.

230. Konno explains that “[t]he second reflecting layer 120 and the first reflecting layer 121 have a function of confining photons which entered into the solid-state imaging element 110 between the both.” Konno, 8:31-33. Konno further explains that because “the photons which entered into the solid-state imaging element 110 are reciprocated between the second reflecting layer 120 and the first reflecting later 121, [the] amount of reciprocating photons ... can be increased....” Konno, 10:14-18. As Konno explains, “photons which entered from the light entrance window 128 can be effectively confined between the first and second reflection layers 121 and 120 to increase the amount of photons participating in photoelectric conversion by the photoelectric conversion element 135 and thereby improve detection sensitivity.” Konno, 11:65-12:3.

231. It would have been obvious to use Konno’s first reflective layer 121 and light entrance window 128 in Hwang’s image sensor to reduce loss of light reflected from the photodiodes and improve light efficiency, as taught by Konno.



Konno, Fig. 7 (annotated); Hwang, Fig. 6 (annotated, modified).

232. This modification would result in Hwang's image sensor having a *reflective layer* (the first reflective layer) *coupled to the light incident side* (i.e., Hwang's "second surface" at the top of the pixel semiconductor pattern 110a," as discussed above for Ground 5, element 19[a]) *having an aperture to allow entry of light into the pixel*.

233. A POSITA would have been motivated to make this modification, as adding Konno's first reflective layer 121 and light entrance window 128 to Hwang's image sensor would allow for light to be reflected from the first reflective layer back into Hwang's semiconductor pattern 110a, thus increasing its efficiency. Specifically, Konno explains that using the first reflective layer 121 allows for "[t]he second reflecting layer 120 and the first reflecting layer 121 [to] have a function of confining

photons which entered into the solid-state imaging element [] between the both....”

Konno, 8:31-33. A POSITA would have had a reasonable expectation of success because, for example, Hwang’s base multi-layered reflection layer 155a would serve to reflect light back to Konno’s first reflective layer 121.

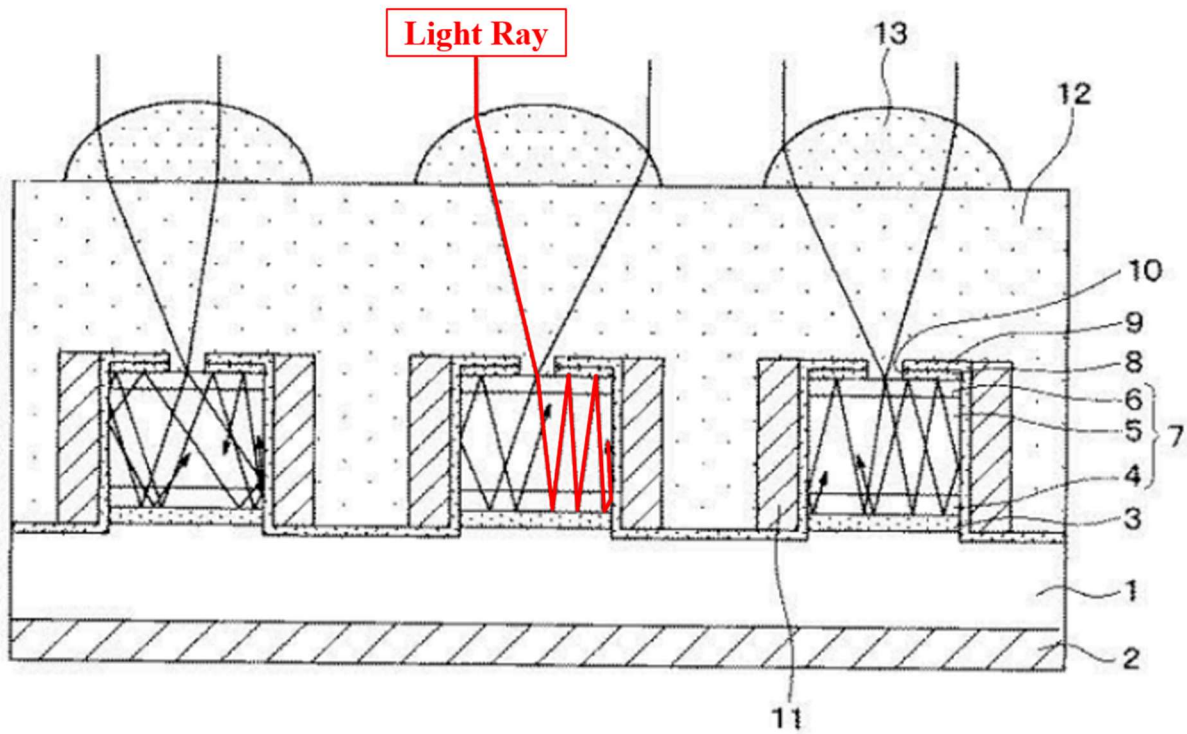
234. A POSITA would have had a reasonable expectation of success in implementing the reflective layer of Konno in the image sensor of Hwang. A POSITA would recognize that the first reflective layer 121 and light entrance window 128 could be readily implemented in Hwang’s image sensor. For example, in the manufacturing steps shown for Hwang’s substantially similar embodiments in figures 13/14 and 16/17, Hwang explains that “[a] color filter 225 is disposed on the second surface of the pixel semiconductor pattern 110a.” Hwang, 8:17-18. A POSITA would recognize that the first reflective layer 121 and light entrance window 128 could be placed between Hwang’s color filter 225 and its pixel semiconductor pattern 110a, similar to how in Konno the first reflective layer 121 and light entrance window 128 are formed above the photoelectric conversion element 135. *See generally* Konno, 8:18-30, Figs. 3-4.

- f) **19[f]: “wherein the reflective layer is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into the pixel.”**

235. This limitation would have been obvious based on Hwang in view of Konno.

236. As discussed for claim 19[e] above, it would have been obvious in view of Konno to use Konno's first reflective layer 121 (i.e., a *reflective layer coupled to the light incident side*) in Hwang's image sensor. In such a structure, this first reflective layer 121 would constitute a *reflective layer that is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into the pixel*. As explained for claims 19[b] and 19[c] above, Hwang's image sensor as modified by Konno includes both a second reflecting layer 120 and a peripheral reflecting layer 220a'. As explained above for claim 20 below, the purpose of its backside and peripheral reflecting layers is to reflect light back into the pixel.

237. A POSITA would understand that Hwang's image sensor, including reflective backside, peripheral, and (as modified by Konno) frontside surfaces is operable to reflect at least a portion of light multiple times off of the first reflective layer 121 (e.g., back into the pixel back into the pixel). Indeed, such reflection was well-known at the time of art, as evidenced by the light path depicted in annotated Figure 1 of Yamada, below (showing light ray reflected by first reflective film 3, second reflective film 8, and third reflective film 11):



Yamada Fig. 1 (annotated).

4. **Claim 20:** “The device of claim 19, wherein at least one of the backside light trapping material and the peripheral light trapping material reflects light incident thereon back into the pixel.”

238. This limitation would be obvious based on Hwang in view of Konno.

239. *First*, Hwang discloses that *the peripheral light trapping material* (i.e., Hwang’s sidewall multi-layered reflection layer 220a’) *reflects light incident thereon back into the pixel*. Hwang discloses that “[l]ight that is reflected from the first and second boundary surfaces is also reflected by the third boundary surface and also the fourth boundary surface within the sidewall multi-layered reflection layer 220 [220a’ in Figure 6],” i.e., the peripheral light trapping material, and that “[a]s a result, the

portion of the light reflected toward the sidewall multi-layered reflection layer 220 [220a' in Figure 6] from the light reflected by the first and second boundary surfaces is incident again on the photodiode 145, so that the absorption efficiency of external light is increased.” Hwang, 10:28-35.

240. **Second**, Hwang, as modified by Konno, includes a *backside light trapping material* (i.e., Konno’s second reflecting layer 120) that *reflects light incident thereon back into the pixel*. Hwang discloses that “external light incident on the second surface [the light incident surface] of the photodiode 145 is reflected by the first boundary surface and at least one secondary boundary surface within the base multi-layered reflection layer 155a,” i.e., the backside light trapping material, and that “[t]he light reflected by the first and second boundary surfaces is incident again on the photodiode 145.” Hwang, 9:6-14. External light would similarly be reflected back into the pixel after modifying Hwang’s image sensor to include Konno’s second reflecting layer 120. *See, e.g.*, Konno, 13:66-14:3 (“This makes it possible to reflect photons which entered from the light entrance window 128 to the first reflecting layer 121, and therefore the amount of photons to be detected again by the photoelectric conversion film 125 can be increased.”).

241. Accordingly, this limitation would have been obvious in view of Hwang and Hwang in view of Konno.

**5. Claim 21: “The device of claim 19, wherein said peripheral light trapping material has a refractive index of less than about 2.1.”**

242. Hwang teaches or suggests this limitation.

243. Hwang discloses that the *peripheral light trapping material* includes a material having *a refractive index of less than about 2.1*. Hwang discloses that “sidewall multi-layered reflection layer 220a’ includes a first sidewall reflection layer 212a’ and a second sidewall reflection layer 217a’.” Hwang, 11:64-12:12. Hwang explains that “[t]he first sidewall reflection layer 210 [212a’ in Figure 6] can be a silicon oxide layer or a layer of air (with a refractive index of 1).” Hwang, 10:2-5. As Hwang explains, silicon oxide has a refractive index of approximately 1.46. Hwang,

9:28-30.<sup>11</sup> In such a structure, the peripheral light trapping material would include a material (i.e., silicon dioxide) with *a refractive index of less than about 2.1*.

**6. Claim 22: “The device of claim 19, wherein said peripheral light trapping material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.”**

244. Hwang teaches or suggests this limitation. As discussed for Ground 5, claim 21 above, Hwang discloses a peripheral light trapping material containing first sidewall reflection layer 212a' that is “formed of silicon oxide...” Hwang, 10:2-5 *see also* Hwang, 8:40-52, 9:25-30. In such a structure, the peripheral light trapping material would include a material comprising *an oxide* (i.e., silicon dioxide).

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<sup>11</sup> While Hwang describes layer 210 as “silicon oxide,” a POSITA would understand this to be a reference to “silicon dioxide,” given the description of its refractive index being “approximately 1.46.” Hwang, 9:29-29. It is well known that the refractive index of silicon dioxide is 1.46, Schubert, 181 (“SiO<sub>2</sub> ( $\bar{n} \approx 1.46$ )”), whereas the refractive index of silicon monoxide is at least around 1.8-2.2, Ex-1023, Abstract (refractive index of “silicon monoxide” (“SiO”) ranges from 2.15 to 1.95 in the 0.40 to 0.70 micron wavelength); Ex-1024, 17 & Fig. 2 (refractive index of “silicon monoxide” ranges from about 1.8 to about 1.9 in the 1 to 5 micron wavelength range).

7. **Claim 23: “The device of claim 22, wherein said peripheral light trapping material is selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.”**

245. Hwang teaches or suggests this limitation. As discussed for Ground 5, claim 21 above, Hwang discloses a peripheral light trapping material containing first sidewall reflection layer 212a' that is “formed of silicon [di]oxide....” Hwang, 10:2-5 *see also* Hwang, 8:40-52, 9:25-30. In such a structure, the peripheral light trapping material would include a material comprising silicon dioxide.

8. **Claim 26: “The device of claim 19, wherein the peripheral sidewall extends completely around the pixel periphery.”**

246. Hwang teaches or suggests this limitation. As discussed for claim 1[a] above, Hwang discloses that “[t]he sidewall multi-layered reflection layer 220 [220a' in Figure 6] encloses the side walls of the pixel semiconductor patterns 110a.” Hwang, 6:15-17. Therefore, as shown in annotated Figure 1 below, the *peripheral sidewall* where the pixel 110a contacts the sidewall reflection layer 220 [220a' in Figure 6] *extends completely around the pixel periphery*.

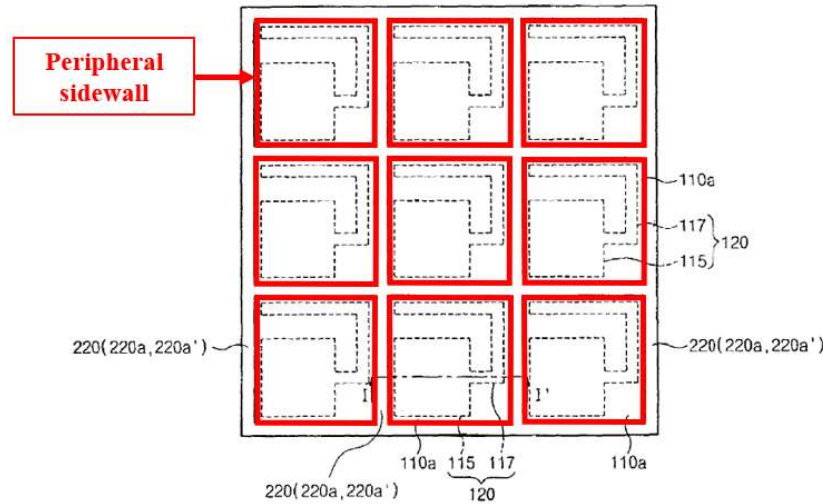


**Fig. 1**

Hwang, Fig. 1 (annotated).

9. **Claim 27:** “The device of claim 19, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”

247. Hwang teaches or suggests this limitation. As explained above for claim 19[a], the *peripheral sidewall* where the pixel semiconductor pattern 110a contacts the sidewall multi-layered reflection layer 220a' extends from the light incident surface to the backside surface, as illustrated in the annotated figure below.

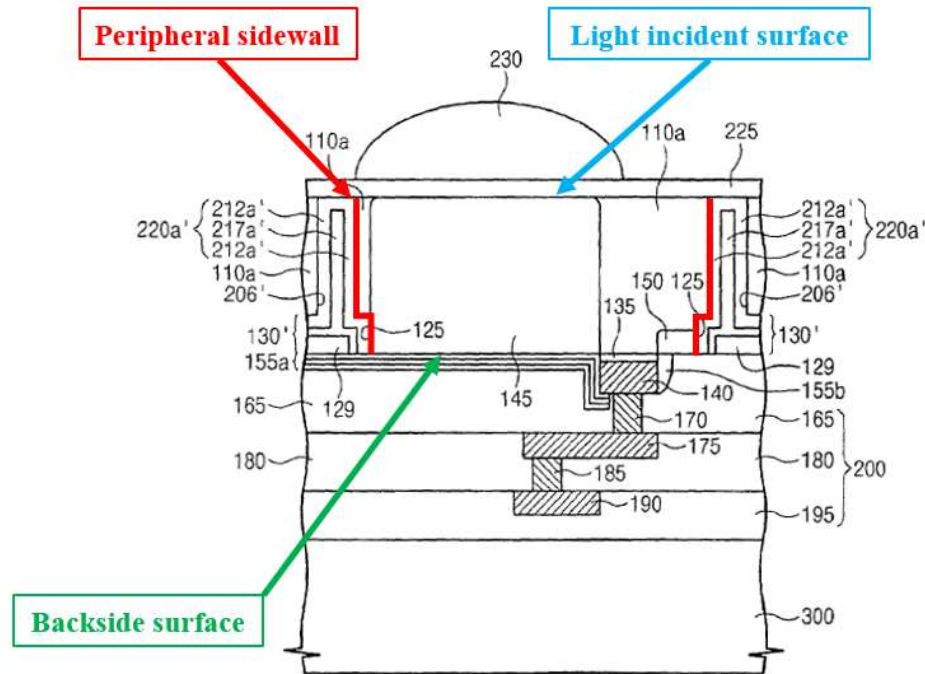


**Fig. 6**

Hwang, Fig. 6 (annotated).

- 10. Claim 28: “The device of claim 19, wherein said aperture has an effective surface area of less than about 90% of total area of the incident light surface.”**

248. This limitation would have been obvious based on Hwang in view of Konno.

249. As discussed for claim 19[e] above, it would have been obvious in view of Konno to use Konno’s first reflective layer 121 and light entrance window 128 (i.e., its *aperture*) in Hwang’s image sensor. In such a structure, Hwang’s image sensor has a reflective layer (first reflective layer 121) coupled to the light incident side (Hwang’s second surface) having an aperture (light entrance window 128) to allow entry of light into the pixel. Additionally, in such a structure, Hwang’s image

sensor would have an *aperture* having an *effective surface area of less than about 90% of total area of the incident light surface*. Specifically, Konno discloses that:

The width (diameter) of the light entrance window 128 [i.e., the width of the *aperture*] is appropriately determined on the basis of the relation to width 126 of the pixel [i.e., the width of the *incident light surface*], thickness of the transparent layer 136 to be explained later, and the like. For example, when the width 126 of pixel is 100  $\mu\text{m}$ , it [i.e., the width of the *aperture*] is 20  $\mu\text{m}$ .

Konno, 8:66-9:3.<sup>12</sup>

250. Indeed, having an aperture with an *effective surface area of less than about 90% of total area of the incident light surface* was well-known. Other similar image sensors balanced the competing considerations of increasing the size of the aperture to allow more light to be collected, but keeping the aperture small enough to prevent internal light from escaping, and designed apertures with an *effective surface*

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<sup>12</sup> Konno explains that “[t]he light entrance window 128 may have various shapes. For example, it may be a slot along the direction perpendicular to the sectional line A indicated in FIG. 1, or it may have a round shape or a polygonal shape.” Konno, 8:63-66. Regardless of the shape, a POSITA would understand that the length of the aperture cannot be greater than the length of the pixel. Therefore, an aperture with Konno’s dimensions must have an effective surface area of less than about 90% of total area of the incident light surface.

*area of less than about 90% of total area of the incident light surface.* For example, Ex-1016 (“Kim”) discloses photodiodes that contain an aperture (*i.e.*, an opening 107) formed of reflective films 106 that reflects light back into the photodiodes. Kim [0018] (“[l]ight 105 reflected from photodiodes 102 can return to photodiodes 102 after being reflected by reflected films 106”). Kim discloses that the “openings 107 can occupy between 70 to 90% of the uppermost surface area of photodiodes 102,” *i.e.*, the *incident light surface*. Kim, [0015].

251. Finally, designing the aperture to be less than about 90% of the incident light surface total surface area would be nothing more than a design choice, as evidenced by the ’599 patent’s failure to identify any particular benefit of doing so. *See* ’599 patent, 12:9-14.

**11. Claim 29: “The device of claim 19, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.”**

252. This limitation would have been obvious based on Hwang in view of Konno.

253. Konno’s solid-state imaging element includes a microlens 122 *functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel*. Specifically, Konno discloses “[t]he microlens 122 is formed from convex lenses ... and it concentrates photons which entered into the solid-

state imaging element 110, and leads them to the light entrance window 128,” as shown in annotated Figure 3 below. Konno, 9:4-9.

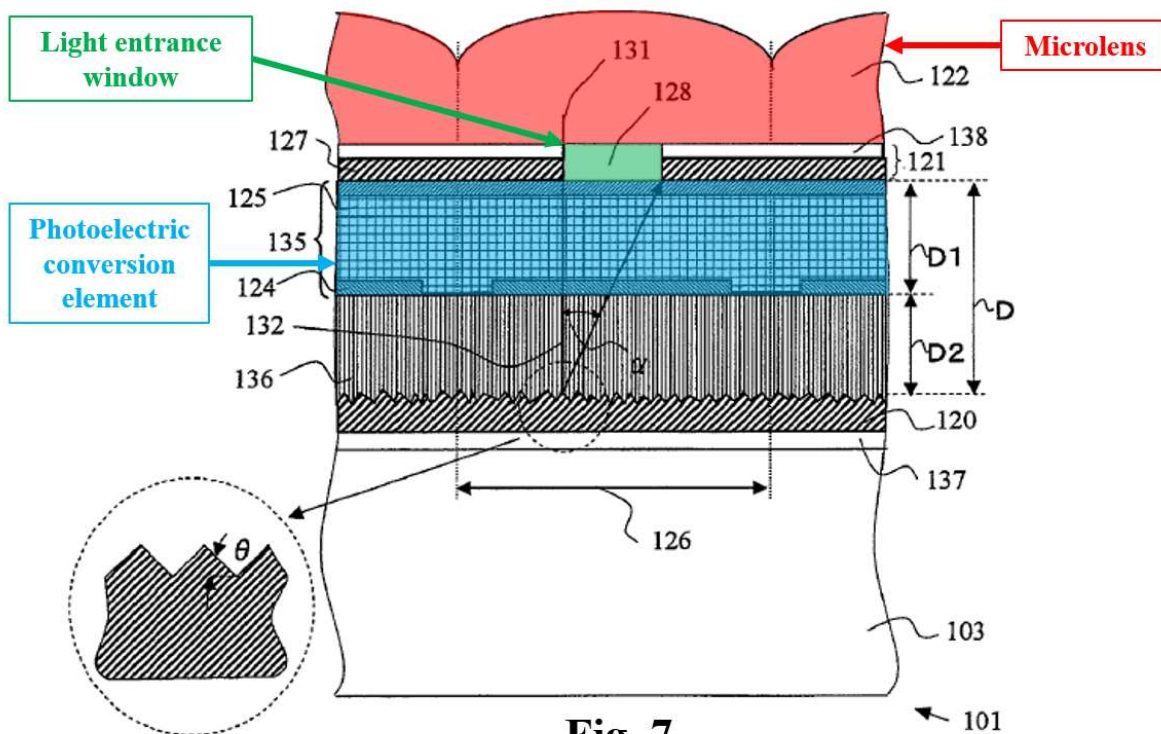


**Fig. 7**

Konno, Fig. 7 (annotated).

254. Using such a lens in Hwang’s image sensor would have been obvious. Like Konno, Hwang discloses a “micro lens,” and explains that “[e]xternal light passes through the micro lens 230 and the color filter 225, and is incident on the second surface of the photodiode 145.” Hwang, 8:20-22. As explained for claim 19[e] above, it would have been obvious to incorporate Konno’s first reflecting layer 121 and light entrance window 128 (i.e., its *aperture*) into Hwang’s imager device.

255. As explained for claim 19[e] above, Hwang’s imager device incorporating Konno’s aperture would result in light that passes through the lens being

focused through the aperture and into the pixel. When incorporating Konno's first reflecting layer 121 and light entrance window 128 into Hwang's image sensor, it would be obvious that such a lens should be configured to concentrate the light through the window (as taught in Konno), in order to ensure that the light enters the pixel. That is, it would be obvious to use a lens that is *functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel*. This modification results in Hwang's image sensor having a *lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel*.

256. Moreover, a POSITA would reasonably expect success in using such a lens in Hwang's image sensor, as Hwang already includes a microlens, and configuring a lens to direct light in a desired manner is straightforward and commonplace when designing light sensors.

**12. Claim 30: "The device of claim 19, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer."**

257. This limitation would have been obvious based on Hwang in view of Konno.

258. As explained in claim 19[b] above, it would have been obvious in view of Konno to use Konno's second reflecting layer 120 in Hwang's image sensor. Konno explains that the "[t]he second reflection layer 120 ... can be formed by forming a thin film of a metal such as aluminum and silver by deposition or the like." Konno, 8:31-

38; *see also* Konno, 13:57-59 (explaining that only the “shape” of the second reflecting layer 120 differs between the first and second embodiments).

259. Accordingly, this limitation would have been obvious based on Hwang in view of Konno.

**13. Claim 31: “The device of claim 19, wherein said textured region comprises a textured film layer.”**

260. This limitation would have been obvious based on Hwang in view of Konno.

261. As discussed for claim 19[d] above, it would have been obvious to incorporate Konno’s textured transparent layer 136 into Hwang’s image sensor. In such a structure, Hwang’s image sensor would have a *textured region [that] comprises a textured film layer* (transparent layer 136).

**14. Claim 32: “The device of claim 31, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”**

262. This limitation would have been obvious based on Hwang in view of Konno.

263. As discussed for claim 19[d], Konno discloses that its transparent layer 136 can be “formed from a material which transmits photons, for example, glass.” Konno, 9:35-37. As also explained above, given that Hwang’s base multi-layered reflection layer 155a already includes SiO<sub>2</sub>, i.e., glass, it would have been obvious to

use silicon dioxide as a textured film layer in Hwang's image sensor, as modified by Konno.

264. Accordingly, this limitation would have been obvious based on Hwang in view of Konno.

**15. Claim 34: "The device of claim 19, wherein the backside light trapping material substantially covers the backside surface."**

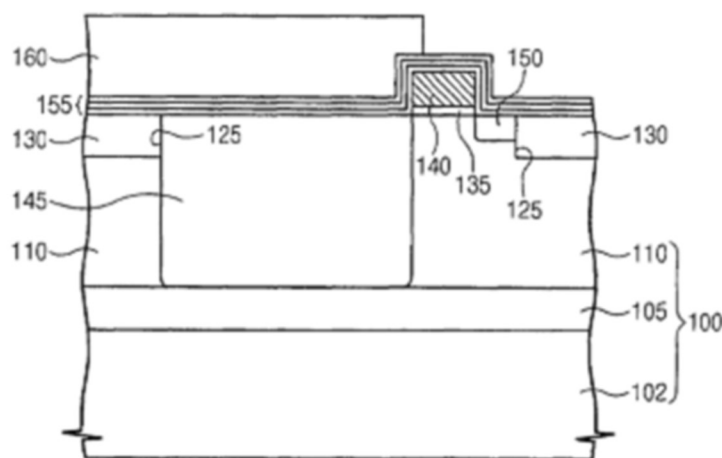
265. This limitation would have been obvious based on Hwang in view of Konno.

266. As explained above for claim 19[b], Hwang's image sensor, as modified by Konno includes a *backside light trapping material* (Konno's second reflecting layer 120). It would have been obvious based on Hwang's and Konno's teachings to have the backside light trapping material *substantially cover[] the backside surface*. As explained for claim 19[b] above, Hwang's base multi-layered reflection layer 155a serves to reflect light back into the pixel, i.e., cause light to be "incident again on the photodiode," to "increase the light sensitivity of the sensor." Hwang, 9:11-14. Konno provides a similar disclosure. 14:66-15:2 ("Further, the concavo-convex surface of the second reflecting not absorbed by the photoelectric conversion film 125 between both the reflecting layers.").

267. A POSITA would have been motivated to make the backside light trapping material cover as much area as possible in order to increase the amount of light reflected back into the pixel, thus increasing the sensitivity of the sensor.

268. Hwang itself acknowledges this, as Hwang's Figure 6 depicts the base multi-layered reflection layer covering substantially all of the backside surface of the photodiode. In Figure 9, Hwang depicts multi-layered reflection layer 155a completely covering the backside surface, including both photodiode 145 and pixel semiconductor pattern 110a.

Fig. 9

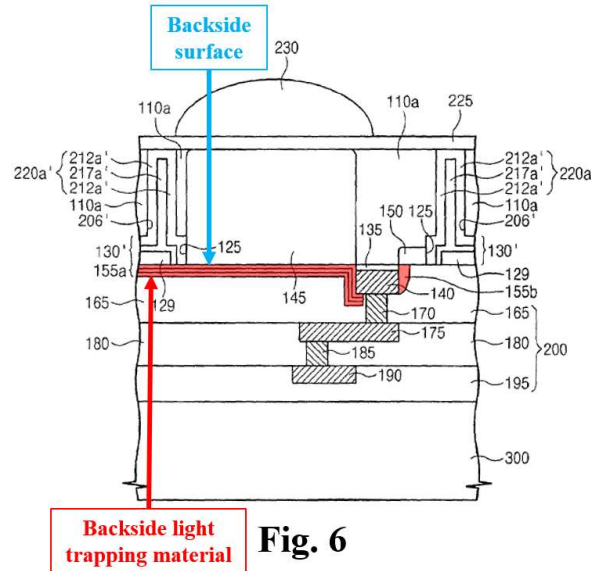


Hwang, Fig. 9. A small portion of the multi-layered reflection layer may need to be etched away around gate electrode 140 in order to form the transistor connecting the pixel to the rest of the circuitry. But a POSITA would understand that the multi-layered reflection layer would still substantially cover the backside surface. *See also* Hwang, 4:56–58 (“The drawings are not necessarily to scale, emphasis instead being placed upon illuminating aspects of the invention.”).

269. As discussed above, the base multi-layered reflection layer is included so that “light that is incident on the photodiode is reflected by the base multi-layered

reflection layer and re-enters the photodiode” so that “the sensitivity of the image sensor is improved.” Hwang, 15:38–41. The base multi-layered reflection layer *substantially covers* the backside surface in order to maximize the amount of light reflected back toward the pixel. This understanding is supported by Hwang’s express disclosure that base multi-layered reflection layer 155a can even be “extended to cover a portion of the second surface of the gate electrode 140.” Hwang, 7:45-51. Hwang’s disclosure that gate spacer 155b “can include the same material as the base multi-layered reflection layer 155a,” Hwang, 7:53-55, further supports a POSITA’s understanding that *the light trapping material substantially covers the backside surface*, as this configuration minimizes the area not covered by the base multi-layered reflection layer.

270. Konno similarly depicts second reflecting 120 covering the entire backside. *See* Konno, Fig. 7. A POSITA would be motivated to ensure that Konno’s second reflecting layer 120 covers at least as much of the backside as Hwang’s base multi-layered reflection layer 155a to achieve the same results.



Hwang, Fig. 6 (annotated).

271. Accordingly, this limitation would have been obvious based on Hwang in view of Konno.

**16. Claim 36: “The device of claim 19, wherein said peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.”**

272. Hwang teaches or suggests this limitation. As explained above for claim 27, the *peripheral sidewall* where the pixel semiconductor pattern 110a contacts the sidewall multi-layered reflection layer 220a' *extends through the pixel substantially from the light incident surface to the backside surface*, as illustrated in the annotated figure below.

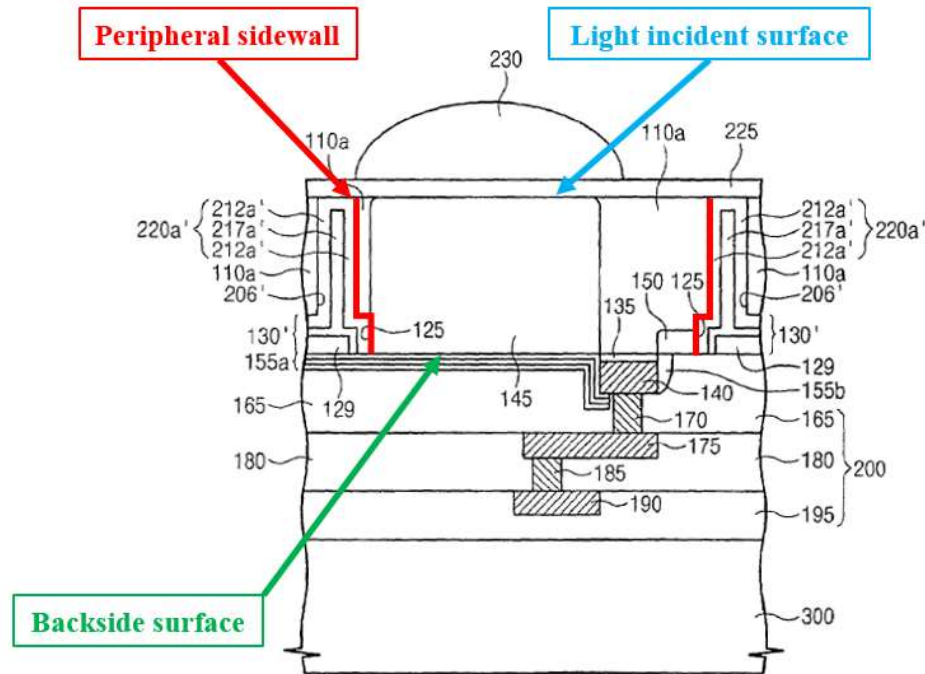


**Fig. 6**

Hwang, Fig. 6 (annotated).

**F. Ground 6: Claim 33 is Obvious Based on Hwang, Konno, and Shinohara**

- 1. Claim 33: “The device of claim 1, wherein the peripheral light trapping material comprises any of aluminum oxide and hafnium oxide.”**

273. This limitation would have been obvious based on Hwang in view of Konno and Shinohara.

274. Shinohara discloses a *peripheral light trapping material that comprises any of aluminum oxide or hafnium oxide*. Specifically, Shinohara describes “an element isolation region 68 for isolating pixels.” Shinohara, [0090]. As shown below,

Shinohara's isolation region is formed with "an insulating film 69" formed within a "void 44" in the "p-type semiconductor layer 43." Shinohara, [0090].

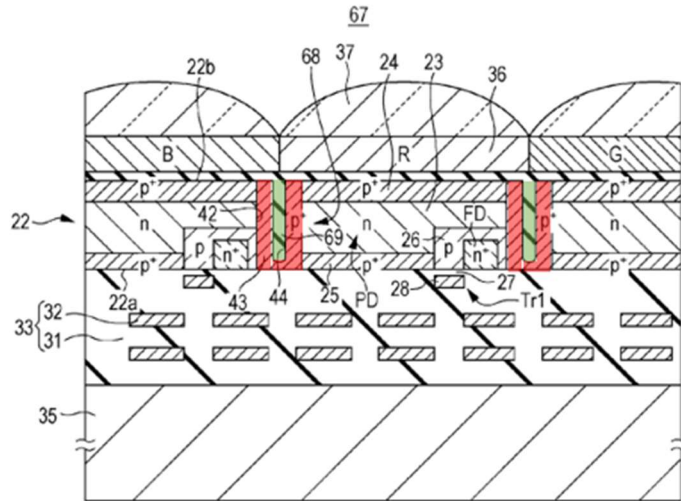
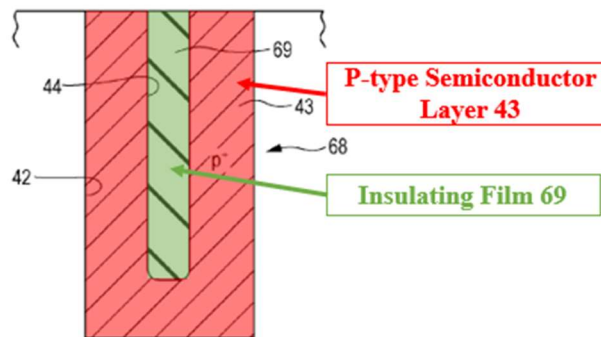


FIG. 9B



Shinohara Fig. 9 (annotated).

275. Shinohara explains that it is advantageous to make the "insulating film 69" a material having a negative fixed charge. Shinohara explains that "[w]hen the insulating film having a negative fixed charge is used as the insulating film 69, the hole pinning state by the p-type semiconductor layer 43 of the element isolation region 68 can be enhanced." Shinohara, [0095]. In particular, "the generation of ...

dark current can be further suppressed.” Shinohara, [0095]. Shinohara discloses examples of negative fixed charge materials, including, “hafnium dioxide ( $\text{HfO}_2$ )” or “dialuminum trioxide ( $\text{Al}_2\text{O}_3$ ).” Shinohara, [0091]. *See also* ’599 Patent, 9:53-59 (using “aluminum oxide” and “ $\text{Al}_2\text{O}_3$ ” interchangeably), 10:47-48 (“Hafnium oxide, which has a refractive index of about 1.9).<sup>13</sup>

276. A POSITA would be motivated to use Shinohara’s isolation region 68—including either of hafnium oxide or aluminum oxide—in place of Hwang’s sidewall multi-layered reflection layer 220a’ to achieve the benefit described above, i.e., to limit dark current. A POSITA would have had an expectation of success in doing so. Shinohara’s isolation region 68 serves the same purpose as Hwang’s sidewall multi-layered reflection layer 220a’, e.g., Shinohara explains that “inclined incident light is reflected at the interface between the silicon and the insulating film [of the isolation region 68] and does not leak outside from the pixel, and hence no color mixture occurs.” Shinohara, [0094].

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<sup>13</sup> Based on this disclosure, A POSITA would recognize that “hafnium oxide” as used in the ’599 patent refers to  $\text{HfO}_2$ , which has a refractive index of about 1.9. Ex-1030, 7 (showing refractive index of  $\text{HfO}_2$  is between 1.70 and 1.91). Furthermore, hafnium oxide is commonly used to refer to  $\text{HfO}_2$ .

277. Accordingly, this limitation would have been obvious based on Hwang in view of Konno, and Shinohara.

**G. Ground 7: Claims 1-14, 16, 18, and 24-25 are Obvious Based on Hwang, Konno, and Mori**

**1. Claim 1**

**a) 1[pre]: “A light trapping device, comprising:”**

278. To the extent the preamble is limiting, Hwang teaches or suggests it for the same reasons discussed for Ground 5, claim 19[pre] above.

**b) 1[a]: “at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;”**

279. Hwang teaches or suggests this limitation for the reasons discussed for Ground 5, claim 19[a] above.

**c) 1[b]: “a backside light trapping material at least partially covering the backside surface;”**

280. Hwang teaches or suggests this limitation.

281. Hwang’s image sensor includes a *backside light trapping material at least partially covering the backside surface* of the pixel. Hwang discloses that a “base multi-layered reflection layer 155a is interposed between the photodiode 145 and the interlayer insulating layer 200,” Hwang, 7:45-47, as shown in the annotated Figures below.

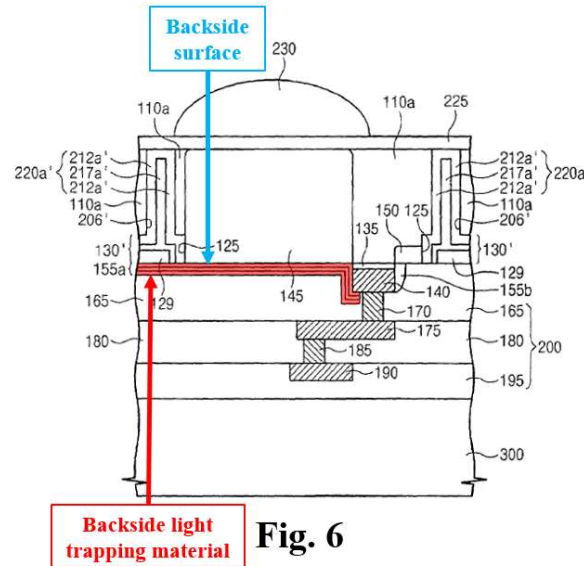


Fig. 6

Hwang Fig. 6 (annotated).

282. This base reflection layer 155a traps light by reflecting light back into the pixel, and therefore constitutes a *light trapping material*. As Hwang explains, “external light incident on the second surface of the photodiode 145 is reflected by the first boundary surface and at least one second boundary surface within the base multi-layered reflection layer 155a.” Hwang, 9:6-10. Therefore, the light reflected by the multi-layered reflection layer 155a “is incident again on the photodiode,” thus “increas[ing] the light sensitivity of the image sensor.” Hwang, 9:11-14. Further, Hwang’s base multi-layer reflection layer 155a *at least partially cover[s] the backside surface*. Hwang explains that “the base multi-layered reflection layer 155a contacts the first surface of the pixel semiconductor pattern 110a on which the photodiode 145 is formed,” as shown in Figure 6 above. Hwang, 8:32-35. As explained for limitation 19[a] above, the “first surface” constitutes the claimed *backside surface* of the pixel.

283. Accordingly, Hwang's base multi-layer reflection layer 155*a* comprises *a backside light trapping material at least partially covering the backside surface*.

284. In addition this limitation would have been obvious based on Hwang in view of Konno, for the reasons discussed above with respect to claim 19[b] and [d].

**d) 1[c]: “a peripheral light trapping material substantially covering the peripheral sidewall, wherein said peripheral light trapping material is doped with a dopant to create a surface field; and”**

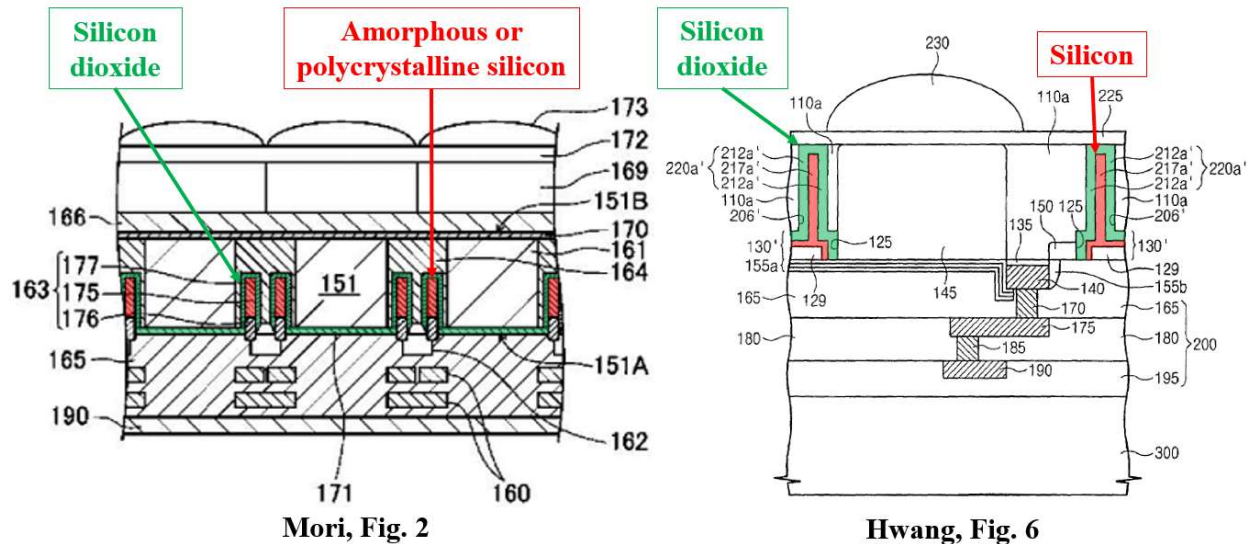
285. This limitation would be obvious based on Hwang in view of Mori.

286. Hwang's image sensor includes a *peripheral light trapping material* (sidewall multi-layered reflection layer 220*a'*) *substantially covering the peripheral sidewall*. As explained for Ground 5, claim 19[c] above, Hwang's image sensor includes a *peripheral light trapping material* (sidewall multi-layered reflection layer 220*a'*) *substantially covering the peripheral sidewall*. Hwang discloses that “sidewall multi-layered reflection layer 220*a'* [i.e., its *peripheral light trapping material*] includes a first sidewall reflection layer 212*a'* and a second sidewall reflection layer 217*a'*.” Hwang, 11:64-12:12. As illustrated in annotated Figure 6 below, Hwang explains that “[t]he first sidewall reflection layer 210 [212*a'* in Figure 6] can be a silicon oxide layer....,” and that “[t]he second sidewall reflection layer 215 [217*a'* in Figure 6] can be a silicon layer.” Hwang, 10:2-5.

287. Mori similarly discloses a multi-layer partition disposed between adjacent pixels of an image sensor and comprising a layer of silicon (silicon layer 175)

sandwiched between layers of silicon dioxide (side SiO<sub>2</sub> film 177), as shown in Mori's

Figure 2. That is, both references utilize a similar silicon/silicon dioxide film disposed at the pixel sidewalls:



Mori, Fig. 2 (annotated); Hwang, Fig. 6 (annotated). *See also* Mori, Fig. 6 (depicting partition part 163 spanning along the entire side of photoelectric conversion unit 161). And in both references, the silicon/silicon dioxide film is used to mitigate against interference between pixels. *Cf.* Hwang, 15:46-48 (“interference between pixels can be minimized by the sidewall multi-layered reflection layer”) with Mori, [0027] (Si/SiO<sub>2</sub> partition serves to reduce “color mixing [or ‘crosstalk’] due to obliquely incident light”).

288. Mori further teaches that it is advantageous in such a film to dope the silicon dioxide layer (Mori's SiO<sub>2</sub> layer 177) with p-type impurities, as explained in the overview of Mori above. *See* Mori, [0036]. As Mori explains, this doping is

advantageous in order to mitigate dark current stemming from crystal defects—i.e., to “prevent charges generated when dark due to crystal defects in the partition groove 174 from flowing into the photoelectric conversion unit 161.” Mori, [0036].

289. Accordingly, Mori teaches that Mori’s side SiO<sub>2</sub> film *is doped with a dopant to create a surface field* as set forth in this limitation. The ’599 patent does not explain how doping the peripheral light trapping material operates to create a surface field. Rather, its only disclosure relating to such doping is that: “[I]t can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.” ’599 patent, 10:14-18. That is, the ’599 patent teaches that doping in such a manner as in Mori serves to increase electrical isolation between the pixels via a surface field. Thus, Mori’s doped SiO<sub>2</sub> film 177 along the side of its pixel (photoelectric conversion unit 161) would constitute a *peripheral light trapping material doped with a dopant to create a surface field* to the extent that is contemplated by the limited disclosure of the ’599 patent.

290. As a POSITA would recognize, doping Mori’s silicon dioxide layer with p-type impurities would lead to an excess of positive charges, creating an electric field at the surface of the layer. In other words, Mori teaches that its silicon dioxide layer *is doped with a dopant to create a surface field*.

291. Based on Mori's teaching, it is obvious to similarly dope Hwang's silicon oxide layers 212a'—such that this *peripheral light trapping material* (Hwang's silicon oxide layers) *is doped with a dopant to create a surface field* in the same manner as Mori's SiO<sub>2</sub> film. Hwang's silicon oxide layer 212a' adjoins the side of Hwang's pixel (pixel semiconductor pattern 110a), just like Mori's side SiO<sub>2</sub> film 177 adjoins Mori's pixel. A POSITA would have recognized that doping Hwang's silicon oxide layer 212a' with p-type impurities would similarly mitigate dark current stemming from crystal defects in Hwang's sensor.

292. A POSITA would reasonably expect success in making this modification, given that Hwang has the same arrangement of a silicon/silicon dioxide film disposed at the sidewall between pixels as in Mori. A POSITA would recognize that this doping could be readily implemented in Hwang's sensor. Moreover, this doping could be readily implemented in Hwang's image sensor, e.g., in the manufacturing steps shown in Hwang's figures 20/21 after applying layer 212a' in grooves 206'.

293. Therefore, it would have been obvious in view of Mori for the *peripheral light trapping material substantially covering the peripheral sidewall* in Hwang to be *doped with a dopant to create a surface field*.

- e) **1[d]: “a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel;”**

294. This limitation would have been obvious based on Hwang in view of Konno for the reasons discussed for Ground 5, claim 19[e] above.

- f) **1[e]: “wherein the reflective layer is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into the pixel.”**

295. This limitation would have been obvious based on Hwang in view of Konno for the reasons discussed for Ground 5, claim 19[f] above.

2. **Claim 2: “The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material reflects light incident thereon back into the pixel.”**

296. This limitation would have been obvious based on Hwang and Hwang in view of Konno for the reasons discussed for Ground 5, claim 20 above.

3. **Claim 3: “The device of claim 1, wherein said peripheral light trapping material has a refractive index of less than about 2.1.”**

297. Hwang teaches or suggests this limitation for the reasons discussed for Ground 5, claim 21 above.

4. **Claim 4: “The device of claim 1, wherein said peripheral light trapping material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.”**

298. Hwang teaches or suggests this limitation for the reasons discussed for Ground 5, claim 22 above.

5. **Claim 5: “The device of claim 4, wherein said peripheral light trapping material is selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.”**

299. Hwang teaches or suggests this limitation for the reasons discussed for Ground 5, claim 23 above.

6. **Claim 6: “The device of claim 1, wherein the dopant is boron or antimony.”**

300. This limitation would have been obvious based on Hwang in view of Mori.

301. As explained for Ground 7, claim 1[c] above, it would have been obvious in view of Mori to dope Hwang’s silicon dioxide layer with p-type impurities—i.e., a p-type dopant. It further would be obvious to use boron as the p-type dopant, given that boron is one of the most commonly used p-type dopants for Si-based systems. *See, e.g.*, Ex-1018 (explaining that Column-IV materials (e.g., Si) are commonly doped with Column-III-dopants (e.g., boron)). A POSITA would have recognized that using boron as a p-type dopant for silicon-based systems is a known technique that would have yielded predictable results, particularly in light of boron’s similar use as a p-type dopant in other similar light trapping devices. *See, e.g.*, Ex-1019, [0011] (“[t]he substrate 35 is a silicon substrate doped with a P-type dopant such as boron, in which case the substrate 35 is a P-type substrate”). Additionally, this limitation would have been obvious, because a POSITA would have had a limited

number of types of p-type dopants from which to choose, therefore, it would have been obvious to a POSITA to try using boron as the p-type dopant.

302. Accordingly, Hwang in view of Mori teaches or suggests that *the dopant is boron or antimony*.

**7. Claim 7: “The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.”**

303. Hwang teaches or suggests this limitation for the reasons discussed for Ground 5, claim 26 above.

**8. Claim 8: “The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”**

304. Hwang teaches or suggests this limitation for the reasons discussed for Ground 5, claim 27 above.

**9. Claim 9: “The device of claim 1, wherein said aperture has an effective surface area of less than about 90% of total area of the incident light surface.”**

305. This limitation would have been obvious based on Hwang in view of Konno for the reasons discussed for Ground 5, claim 28 above.

**10. Claim 10: “The device of claim 1, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.”**

306. This limitation would have been obvious based on Hwang in view of Konno for the reasons discussed for Ground 5, claim 29 above.

- 11. Claim 11: “The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”**

307. This limitation would have been obvious based on Hwang in view of Konno for the reasons discussed for Ground 5, claims 19[b] and 30 above.

- 12. Claim 12: “The device of claim 1, further comprising a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device.”**

308. This limitation would have been obvious based on Hwang in view of Konno for the reasons discussed for Ground 5, claim 19[d] above.

- 13. Claim 13: “The device of claim 12, wherein said textured region comprises a textured film layer.”**

309. This limitation would have been obvious based on Hwang in view of Konno for the reasons discussed for Ground 5, claim 31 above.

- 14. Claim 14: “The device of claim 13, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”**

310. This limitation would have been obvious based on Hwang in view of Konno for the reasons discussed for Ground 5, claim 32 above.

- 15. Claim 16: “The device of claim 1, wherein the backside light trapping material substantially covers the backside surface.”**

311. This limitation would have been obvious based on Hwang, as well as Hwang in view of Konno, for the reasons discussed for Ground 5, claim 34 above.

- 16. Claim 18: “The device of claim 1, wherein said peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.”**

312. Hwang teaches or suggests this limitation for the reasons discussed for Ground 5, claim 36 above.

- 17. Claim 24: “The device of claim 19, wherein said peripheral light trapping material is doped with a dopant to create a surface field.”**

313. This limitation would have been obvious based on Hwang in view of Mori for the reasons discussed for Ground 7, claim 1[c] above.

- 18. Claim 25: “The device of claim 24, wherein the dopant is boron or antimony.”**

314. This limitation would have been obvious based on Hwang in view of Mori for the reasons discussed for Ground 7, claim 6 above.

**H. Ground 8: Claim 15 is Obvious Based on Hwang, Konno, Mori, and Shinohara**

- 1. Claim 15: “The device of claim 19, wherein the peripheral light trapping material comprises any of aluminum oxide and hafnium oxide.”**

315. This limitation would have been obvious based on Hwang in view of Konno, Mori, and Shinohara.

316. Shinohara discloses a *peripheral light trapping material that comprises any of aluminum oxide or hafnium oxide*. Specifically, Shinohara describes “an element isolation region 68 for isolating pixels.” Shinohara, [0090]. As shown below,

Shinohara's isolation region is formed with "an insulating film 69" formed within a "void 44" in the "p-type semiconductor layer 43." Shinohara, [0090].

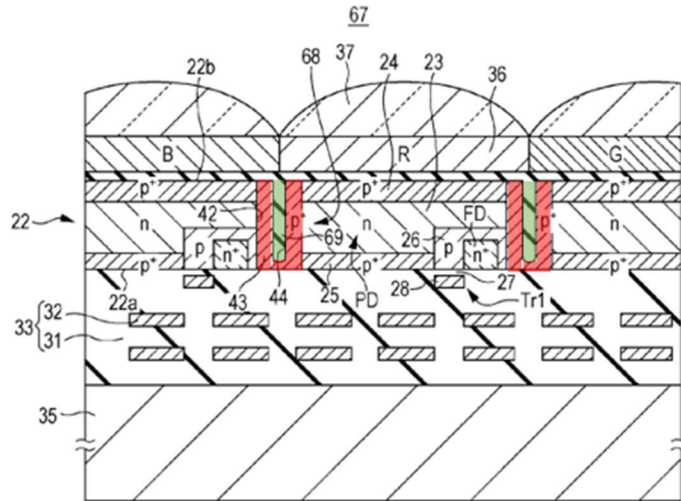
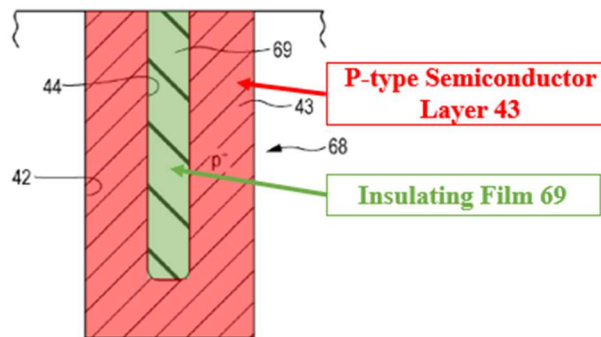


FIG. 9B



Shinohara Fig. 9 (annotated).

317. Shinohara explains that it is advantageous to make the "insulating film 69" a material having a negative fixed charge. Shinohara explains that "[w]hen the insulating film having a negative fixed charge is used as the insulating film 69, the hole pinning state by the p-type semiconductor layer 43 of the element isolation region 68 can be enhanced." Shinohara, [0095]. In particular, "the generation of ...

dark current can be further suppressed.” Shinohara, [0095]. Shinohara discloses examples of negative fixed charge materials, including, “hafnium dioxide ( $\text{HfO}_2$ )” or “dialuminum trioxide ( $\text{Al}_2\text{O}_3$ ).” Shinohara, [0091]. *See also* ’599 Patent, 9:53-59 (using “aluminum oxide” and “ $\text{Al}_2\text{O}_3$ ” interchangeably), 10:47-48 (“Hafnium oxide, which has a refractive index of about 1.9).<sup>14</sup>

318. A POSITA would be motivated to use either Shinohara’s hafnium oxide or aluminum oxide in Hwang’s sidewall multi-layered reflection layer 220a’ to achieve the benefit described above, i.e., reduce dark current. A POSITA would have had an expectation of success in substituting Shinohara’s hafnium oxide or aluminum oxide in place of the silicon used as the second sidewall reflection layer 217a’ in the Si/ $\text{SiO}_2$  layers used in Hwang’s sidewall multi-layered reflection layer 220a’. *See, e.g.*, Suzanaga, [0067] (“[t]he film having a high refractive index is not necessarily limited to a semiconductor material, but may be for example, any one of ...  $\text{Al}_2\text{O}_3$  ... and the like as depicted in Table 1, and may be combined with a film having a low refractive index, such as  $\text{SiO}_2$ ...”). Shinohara surrounds its negative

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<sup>14</sup> Based on this disclosure, A POSITA would recognize that “hafnium oxide” as used in the ’599 patent refers to  $\text{HfO}_2$ , which has a refractive index of about 1.9. Ex-1030, 7 (showing refractive index of  $\text{HfO}_2$  is between 1.70 and 1.91). Furthermore, hafnium oxide is commonly used to refer to  $\text{HfO}_2$ .

fixed charge material with a p-type semiconductor layer 43. As discussed above, utilizing Mori's doping process results in a more heavily doped region, similar to Shinohara's p-type semiconductor layer 43. A POSITA would therefore recognize that the modification is structurally compatible.

319. Accordingly, this limitation would have been obvious based on Hwang in view of Konno, Mori, and Shinohara.

## **VIII. CONCLUSION**

320. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on November 29, 2024

Respectfully submitted,



Michael Lebby