

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
PETITIONER,

V.

INFINEON TECHNOLOGIES AUSTRIA AG,
PATENT OWNER.

IPR2025-00175
U.S. Patent 8,686,562

DECLARATION OF YUJI ZHAO, Ph.D.

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	SUMMARY OF OPINIONS.....	1
III.	QUALIFICATIONS AND BACKGROUND.....	2
IV.	MATERIALS CONSIDERED	7
V.	LEGAL STANDARDS	10
A.	Level of Ordinary Skill	12
B.	Prior Art.....	12
C.	Anticipation	13
D.	Obviousness.....	13
VI.	TECHNOLOGY OVERVIEW.....	18
A.	Group III-V Material Devices	18
B.	HEMTs	20
C.	Ohmic and Schottky Contacts	22
D.	Gate Contacts	25
E.	Gate Dielectrics	26
F.	Contact Metals.....	27
1.	Titanium as Metal Layers	27
2.	Aluminum or Aluminum Silicon as Metal Layers	28
3.	Diffusion Barrier Layers	29
G.	Refractory Metal Nitrides.....	29
VII.	THE '562 PATENT	31
A.	Overview	31

VIII. CLAIM CONSTRUCTION	32
IX. LEVEL OF ORDINARY SKILL IN THE ART	33
X. GROUNDS OF UNPATENTABILITY.....	34
A. Ground 1: Usui Anticipates Claims 1, 2, and 4-7	35
1. Usui	35
2. Claim 1	37
a. [1pre]: An electrical contact for use on a semiconductor device, said electrical contact comprising:	37
b. [1a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;.....	37
c. [1b]: said capping layer consisting only of a refractory metal nitride, ...	38
d. [1c]: said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.....	39
3. Claim 2 – The electrical contact of claim 1, wherein said capping layer comprises titanium nitride (TiN).....	40
4. Claim 4 – The electrical contact of claim 1, wherein said plurality of metal layers includes respective first, second, and third metal layers, wherein said second metal layer is formed between said first metal layer and said third metal layer, and said capping layer is formed on said third metal layer.....	40
5. Claim 5 – The electrical contact of claim 4, wherein said first metal layer and said third metal layer of said electrode stack comprise titanium (Ti).	42

6.	Claim 6 – The electrical contact of claim 4, wherein said second metal layer of said electrode stack comprises aluminum (Al).....	42
7.	Claim 7 – The electrical contact of claim 6, wherein said second metal layer of said electrode stack further comprises silicon (Si).....	42
B.	Ground 2: Usui in View of Yu Renders Obvious Claims 3, 8, 12-13, and 17.....	43
1.	Overview of the Combination and Motivations to Combine	43
a.	Claim 3 – A POSITA would have been motivated to implement Usui’s capping layer as tantalum nitride, as taught by Yu.....	43
b.	Claims 8 and 13 – A POSITA would have been motivated to implement Usui’s electrical contact in a group III-V semiconductor device as taught by Yu.....	45
c.	Claims 12 and 17 – A POSITA would have been motivated to implement Usui’s device as a III-V device with a gate insulator layer, as taught by Yu.....	46
2.	Claim 3 – The electrical contact of claim 1, wherein said capping layer comprises tantalum nitride (TaN).	47
3.	Claim 8 – The electrical contact of claim 1, wherein said electrical contact is configured for implementation on a group III-V semiconductor device.....	48
4.	Claim 12 – The electrical contact of claim 8, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.	49
5.	Independent Claim 13	50

a.	[13pre]: An electrical contact for use on a group III-V semiconductor device, said electrical contact comprising:	50
b.	[13a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;.....	50
c.	[13b]: said capping layer consisting only of a metal selected from the group consisting of titanium nitride (TiN) and tantalum nitride (TaN),.....	50
d.	[13c]: said metal forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.....	50
6.	Claim 17 – The electrical contact of claim 13, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.....	50
C.	Ground 3: Usui in View of Yu and Further in View of Adesida Renders Obvious Claims 9, 11, 14, and 16	51
1.	Overview of the Combination and Motivations to Combine	51
a.	Claims 9 and 14 - A POSITA would have been motivated to implement Usui's electrical contact on a group III-V semiconductor device, as taught by Yu, comprises a high electron mobility transistor (HEMT) as taught by Adesida.....	51
b.	Claims 11 and 16 - A POSITA would have been motivated to implement Usui's electrical contact as a gate electrode making Schottky contact, as taught by Adesida, with said group III-V semiconductor device as taught by Yu.....	53

2.	Claim 9 – The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).	54
3.	Claim 11 – The electrical contact of claim 8, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.....	54
4.	Claim 14 – The electrical contact of claim 13, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).	56
5.	Claim 16 – The electrical contact of claim 13, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.....	56
D.	Ground 4: Usui in View of Yu and Further in View of Sugimoto Renders Obvious Claims 10 and 15	56
1.	Overview of the Combination and Motivation to Combine	56
2.	Claim 10 – The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.....	58
3.	Claim 15 – The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.....	59
E.	Ground 5: Yu in View of Usui Renders Obvious Claims 1-8, 12, 13, and 17	60
1.	Yu.....	60
2.	Overview of the Combination and Motivations to Combine	63

a.	Claims 1 and 13 – A POSITA would have been motivated to form Yu’s capping layer of a refractory metal nitride thicker than the bottommost metal layer, as taught by Usui	64
b.	Claims 6 and 7 – A POSITA would have been motivated to form Yu’s metal layers of Al and Si, as taught by Usui	66
3.	Claim 1	67
a.	[1pre]: An electrical contact for use on a semiconductor device, said electrical contact comprising:	67
b.	[1a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;.....	68
c.	[1b]: said capping layer consisting only of a refractory metal nitride, ...	68
d.	[1c]: said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.....	69
4.	Claim 2 – The electrical contact of claim 1, wherein said capping layer comprises titanium nitride (TiN).....	72
5.	Claim 3 – The electrical contact of claim 1, wherein said capping layer comprises tantalum nitride (TaN).	73
6.	Claim 4 – The electrical contact of claim 1, wherein said plurality of metal layers includes respective first, second, and third metal layers, wherein said second metal layer is formed between said first metal layer and said third metal layer, and said capping layer is formed on said third metal layer.....	74

7.	Claim 5 – The electrical contact of claim 4, wherein said first metal layer and said third metal layer of said electrode stack comprise titanium (Ti).	75
8.	Claim 6 – The electrical contact of claim 4, wherein said second metal layer of said electrode stack comprises aluminum (Al).....	76
9.	Claim 7 – The electrical contact of claim 6, wherein said second metal layer of said electrode stack further comprises silicon (Si).....	77
10.	Claim 8 – The electrical contact of claim 1, wherein said electrical contact is configured for implementation on a group III-V semiconductor device.....	78
11.	Claim 12 – The electrical contact of claim 8, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.	79
12.	Independent Claim 13	80
a.	[13pre]: An electrical contact for use on a group III-V semiconductor device, said electrical contact comprising:	80
b.	[13a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;.....	80
c.	[13b]: said capping layer consisting only of a metal selected from the group consisting of titanium nitride (TiN) and tantalum nitride (TaN),.....	80
d.	[13c]: said metal forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.....	81

13.	Claim 17 – The electrical contact of claim 13, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.	81
F.	Ground 6: Yu in View of Usui and Adesida Renders Obvious Claims 9, 11, 14, and 16.....	81
1.	Overview of the Combination and Motivations to Combine	81
a.	Claims 9 and 14 – A POSITA would have been motivated to implement Yu’s device as a HEMT, as taught by Adesida.....	82
b.	Claims 11 and 16 – A POSITA would have been motivated to implement Yu’s electrical contact as a gate electrode making a Schottky contact, as taught by Adesida	83
2.	Claim 9 – The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).	84
3.	Claim 11 – The electrical contact of claim 8, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.....	85
4.	Claim 14 – The electrical contact of claim 13, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).	87
5.	Claim 16 – The electrical contact of claim 13, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.....	87
G.	Ground 7: Yu in view of Usui and Sugimoto Render Obvious Claims 10 and 15	87

1.	Overview of the Combination and Motivation to Combine	87
2.	Claim 10 – The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.....	89
3.	Claim 15 – The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.....	90
XI.	CONCLUSION.....	90

I. INTRODUCTION

1. I have been retained by Innoscience America, Inc. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office.

2. I am over 21 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

3. I understand that this proceeding involves U.S. Patent No. 8,686,562 (“the ’562 patent,” Ex-1001).

4. I have been asked by Petitioner to provide my opinion on whether the claims of the ’562 patent would have been anticipated and/or obvious to a person of ordinary skill in the art at the time of the earliest possible priority date of the ’562 patent. In performing my analysis, I have been asked to assume that the priority date of the ’562 patent is August 25, 2009, and my opinions are set forth below.

5. Throughout this declaration, I refer to specific pages, figures, and/or line numbers of various exhibits. These citations are illustrative and are not intended to suggest that they are the only support for the propositions for which they are cited.

II. SUMMARY OF OPINIONS

6. This declaration considers claims 1-17 of the ’562 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for

these opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

7. Based on my experience and knowledge of the art at the time of the applicable priority date, it is my opinion that claims 1-17 of the '562 patent would have been anticipated and/or obvious based on the asserted grounds discussed below.

8. I am being compensated for my time at my normal hourly rate. My compensation is in no way contingent upon the nature of my findings, the presentation of my findings in testimony, or the outcome of this proceeding.

III. QUALIFICATIONS AND BACKGROUND

9. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below.

10. I am competent to write this declaration.

11. I am an independent consultant. All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in GaN materials science and electronics, and on the documents and information referenced in this declaration. I am over 18 years of age and, if I am called upon to do so, I am competent to testify as to the matters set forth herein.

12. In formulating my opinions, I have relied upon my training, knowledge, and experience in the relevant art. Provided as Exhibit 1003 is a copy of my current

curriculum vitae, which details my education and experience, and a list of all other cases in which, during the previous 8 years, I testified as an expert at trial or by deposition. The following provides a brief overview of some of my experience that is relevant to the matters set forth in this declaration.

13. I have a B.S. in Microelectronics from Fudan University, and an M.S. and Ph.D. in Electrical and Computer Engineering from University of California Santa Barbara (UCSB).

14. I have more than 10 years of experience in the area of GaN materials science and electronics, where I am widely recognized as a leader in the GaN electronics field. I have extensive, hands-on experience with GaN devices, including epitaxial growth, device fabrication, device wiring, and packaging. I have served as a Professor in Electrical and Computer Engineering, and I have taught many undergraduate and graduate classes on semiconductor electronics, including GaN devices fabrication and testing. In addition, I have given numerous invited lectures and seminars on GaN device technologies for many of the world's leading TSMC, MIT, Stanford University, and IEEE.

15. For my graduate studies, I worked with Prof. Shuji Nakamura at UCSB, who is recognized as the world's top scientist in the GaN research, who received the Nobel Prize in Physics in 2014 for his work on GaN materials and LEDs. I also worked with Prof. Umesh Mishra, who is a pioneer in the research of GaN high

electron mobility transistors (HEMTs) and an elected member of U.S. National Academy of Engineering, which is considered to be among the highest recognitions in engineering-related fields. While at UCSB, I was a key researcher and a project leader in the Solid State Lighting and Energy Center (SSLEC), which is the world's leading research center for GaN materials and electronics research with an annual research budget of over \$5M. I have personally fabricated, tested, and packaged hundreds of GaN devices. My research work on GaN materials and devices led to the filing of several patent applications, over 100 media reports in six languages (including highlights in Science, Semiconductor Today, and Yahoo), and numerous papers and invited conference presentations, along with recognition from the SSLEC in years 2010 through 2012 with the "Outstanding Research Achievement Award."

16. After my Ph.D., I continued my research on GaN devices as an Assistant Professor at Arizona State University. I was the founder and Director of GaN Device Research Group at Arizona State University, which is funded by DoD, DOE, NASA, SFAz (Science Foundation of Arizona). The focus of the research group is on GaN devices including HEMTs. This research group engages over five faculty members, and over twenty postdoctoral researchers and graduate students, and is one of the largest GaN research laboratories in the US, including state of the art equipment and methods to fabricate, analyze and test GaN HEMTs. In July 2021,

I joined Rice University to lead the GaN research efforts, where I am currently a tenured Full Professor in the Department of Electrical and Computer Engineering.

17. I have served as PI or co-PIs for several large-scale US research programs on GaN power electronics. For example, I am the leading PI for the DOE ARPAe PNDIODES project, which is a \$3M program for GaN power devices for electric vehicle applications. I am currently Co-PIs for two US national semiconductor centers, including the DOE ULTRA EFRC - a \$12 Million national research center focusing on power electronics, and the DARPA/SRC JUMP 2.0 CHIMES Center - a \$32.7 Million national center focusing on next generational 3D chips supported by Intel, TSMC, Samsung, and IBM. Both centers have extensive GaN electronics research efforts. Since August 2014, I have been awarded over \$50 million in collaborative research funding.

18. I am a member of two of the largest professional engineering societies: the Institute of Electrical and Electronics Engineers, Inc. ("IEEE") and the Materials Research Society ("MRS"). These professional societies address, among other things, GaN materials, devices, and packaging.

19. I have served on various conference committees (invited to participate) on leading semiconductor device conferences, including the Device Research Conference (DRC), the International Conference on Metal Organic Vapor Phase

Epitaxy (ICMOVPE), and the Lester Eastman Conference on High Performance Devices (LEC). All of these conferences have large GaN devices sessions.

20. I have written five book chapters on GaN devices, two of which are directly related to GaN electronics and HEMTs. I have over 250 journal and conference publications on various subjects related to semiconductor devices, among which over 80 publications are directly on GaN electronics and HEMTs. A full list of my publications (articles and book chapters) on GaN electronics is included in my CV.

21. In 2010 through 2013, I received the UCSB Outstanding Research Achievement Award for contributions to fabrication high performance GaN devices. In 2015, I received the Bisgrove Scholar Faculty Award for research work in developing GaN electronics for communication and medical applications. In 2015, I received the NASA Early Career Faculty Award. In 2016, I received the DoD DTRA Young Investigator Award. In 2017, I received the Arizona State University Fulton Outstanding Assistant Professor Award for research work in GaN devices including HEMTs. In 2017, I was selected as an honorable Faculty Scientist to showcase NASA research to Congress at Capitol Hill, where I reported my research to Rep. Lamar Smith, the Chairman of the Congress Committee on Science, Space, and Technology. In 2019, I received the MIT Technology Review Innovators Under 35 (TR 35) – China Award for my contributions in GaN research. In 2019, I received

the Presidential Early Career Award in Science and Engineering (PECASE) from the White House, which is the highest honor given by the US government to early-career scientists and engineers. In 2023, I received TMS Frontiers of Materials Award for my contributions to GaN materials and electronics research.

22. Based on my education and experience, I believe that I have a detailed understanding of the state of the art during the relevant period.

IV. MATERIALS CONSIDERED

23. In forming my opinions, I have reviewed and considered the following documents and any other document cited in this declaration.

Exhibit	Description
Ex-1001	U.S. Patent No. 8,686,562 (“the ’562 patent”)
Ex-1002	Expert Declaration of Dr. Yuji Zhao (“Zhao”)
Ex-1003	Curriculum Vitae of Dr. Yuji Zhao
Ex-1004	U.S. Patent No. 5,943,601 to Usui et al. (“Usui”)
Ex-1005	U.S. Patent Publication No. 2010/0052066 to Yu et al. (“Yu”)
Ex-1006	U.S. Patent Publication No. 2008/0023726 to Adesida et al. (“Adesida”)
Ex-1007	U.S. Patent No. 7,777,252 to Sugimoto et al. (“Sugimoto”)
Ex-1008	Pearton et al., <i>Gallium Nitride Processing for Electronics, Sensors and Spintronics</i> , Springer, 10.1007/1-84628-359-0. (2006)
Ex-1009	Adachi, <i>Properties of Group-IV, III–V and II–VI Semiconductors</i> , John Wiley & Sons, Ltd, 10.1002/0470090340 (2005)

Exhibit	Description
Ex-1010	U.S. Patent Publication No. 2007/0164321 to Sheppard et al. (“Sheppard”)
Ex-1011	Mishra et al., <i>Semiconductor Device Physics and Design</i> , Springer (2008)
Ex-1012	Wu et al., <i>Very-High Power Density AlGaIn/GaN HEMTs</i> , IEEE Transactions on Electronic Devices, Vol. 48, No. 3, March 2001
Ex-1013	Quay, <i>Gallium Nitride Electronics</i> , Springer, 10.1007/978-3-540-71892-5. (2008)
Ex-1014	Mishra et al., <i>AlGaIn/GaN HEMTs—An Overview of Device Operation and Applications</i> , Proceedings of the IEEE, Vol. 90, No. 6, June 2002
Ex-1015	Neaman, <i>Semiconductor Physics and Devices</i> , 3 rd edition (2002)
Ex-1016	Voss, <i>Thermally Stable Ohmic and Schottky Contacts to GaN</i> , University of Florida, 2008
Ex-1017	Krämer, <i>Fabrication and characterization of metal-semiconductor contacts for application in Al_xGa_{1-x}N/GaN HEMTs</i> , (Oct. 31, 2000)
Ex-1018	Kuzmick et al., <i>Technology and Performance of InAlN/AlN/GaN HEMTs With Gate Insulation and Current Collapse Suppression Using ZrO₂ or HfO₂</i> , IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 55, No. 3, Mar. 2008
Ex-1019	Wu et al., <i>Aluminum, magnesium, and gold contacts to contamination free n-GaN surfaces</i> , Journal of Applied Physics, Vol. 89, No. 1, Jan. 1, 2001
Ex-1020	Foresi et al., <i>Metal contacts to gallium nitride</i> , Appl. Phys. Lett., Vol. 62, No. 22, May. 31, 1993
Ex-1021	Kayali et al., <i>GaAs MMIC Reliability Assurance Guideline for Space Applications</i> , JPL Publication 96-25, Dec. 15, 1996

Exhibit	Description
Ex-1022	U.S. Patent Publication No. 2009/0250816 to Chin et al. (“Chin”)
Ex-1023	U.S. Patent No. 7,335,590 to Suh et al. (“Suh”)
Ex-1024	U.S. Patent No. 6,607,976 to Chen et al. (“Chen”)
Ex-1025	Excerpts from Bauccio, Michael, <i>Refractory Metals</i> , ASM Metals Reference Book, ASM International, American Society for Metals, ISBN 978-0-87170-478-8, (1993)
Ex-1026	Preuss, <i>Finer Copper Wires Make for Faster Integrated Circuits</i> , Berkeley Lab, https://www2.lbl.gov/Science-Articles/Archive/integrated-circuits-copper.html , Apr. 5, 1999
Ex-1027	Cockeram, <i>The Diffusion Bonding of Silicon Carbide and Boron Carbide Using Refractory Metals</i> , USDOE Contract No. DE-AC11-98PN38206, Nov. 22, 1999
Ex-1028	Kim, <i>Atomic Layer Deposition of Metal and Nitride Thin films: Current Research Efforts and Applications for Semiconductor Device Processing</i> , RC22737 (W0303-012), Mar. 5, 2003
Ex-1029	U.S. Patent No. 6,844,258 to Fair et al. (“Fair”)
Ex-1030	U.S. Patent No. 4,980,752 to Jones, Jr. (“Jones”)
Ex-1031	U.S. Patent No. 5,635,763 to Inoue et al. (“Inoue”)
Ex-1032	U.S. Patent No. 6,646,352 to Ohmi et al. (“Ohmi”)
Ex-1033	Order Staying and Conditionally Closing Case, Infineon Tech. Austria AG v. Innoscience (Suzhou) Tech. Company, Ltd., No. 4:24-cv-01553 (N.D. Ca. Aug. 30, 2024), ECF No. 56
Ex-1034	Excerpts from Prosecution History of the ’562 Patent
Ex-1035	Excerpts from Rooy, E.L., <i>Introduction to Aluminum and Aluminum Alloys</i> , Metals Handbook, 10 th Edition, Volume 2 Properties and Selection: Nonferrous Alloys and Special-Purpose Materials, ASM International, ISBN 978-0-87170-378-1, (October 1990)

Exhibit	Description
Ex-1036	Pierson, Hugh O., <i>The Refractory Nitrides</i> , Handbook of Refractory Carbides and Nitrides, Properties, Characteristics, Processing and Applications, ISBN 978-0-8155-1392-6, (1996)

24. I have also relied on my education, experience, research, training, and knowledge in the relevant art, and my understanding of any applicable legal principles described in this declaration.

25. All the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my understanding of how a person of ordinary skill in the art would have understood the claims of the '562 patent at the time of the invention.

26. I reserve the right to supplement and amend any of my opinions in this declaration based on documents, testimony, and other information that becomes available to me after the date of this declaration.

V. LEGAL STANDARDS

27. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this

declaration, I have tried to faithfully apply these legal standards to the challenged claims.

28. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious in view of the prior art as of the effective filing date of the patent.

29. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all the limitations of the claim to which it refers.

30. I have been asked to provide my opinions as to whether the cited prior art discloses or renders obvious claims 1-17 of the ’562 patent from the perspective of a person of ordinary skill in the art at the ’562 patent’s earliest possible priority date in 2009, as described in more detail below.

31. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

32. For the purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill

33. I have been informed that a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

34. I have been instructed to assume that a person of ordinary skill in the art is not a specific, real individual but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Prior Art

35. I have been advised and understand that the information used to evaluate whether an invention was new and not obvious when made is generally referred to as “prior art.” I understand that prior art includes patents and printed publications that existed before the earliest priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the effective filing date of the claimed invention and

that a printed publication is prior art if it was publicly available before the effective filing date of the claimed invention.

C. Anticipation

36. I have been informed that, under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claim.

D. Obviousness

37. I have been informed that for obviousness under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

38. I have been informed that an obviousness analysis includes the following considerations:

- a. Determining the scope and content of the prior art;

- b. Ascertaining the differences between the prior art and the claims at issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of nonobviousness (if available).

39. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the challenged claims is August 25, 2009. My opinions would not change if I assumed a later date of invention.

40. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

41. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention.

I have also been informed that a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art. However, I have also been informed that, while taking these previous statements into account, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

42. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods would have been obvious if it yielded predictable results;
- b. The substitution of one known element for another would have been obvious if it yielded predictable results;
- c. The use of a known technique to improve similar devices, systems, or methods in the same way would have been obvious if it yielded predictable results;

- d. The application of a known technique to a device, system, or method that is ready for improvement would have been obvious if it yielded predictable results;
- e. Any need or problem known in the field and/or addressed by a prior art reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

43. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation would have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields, market demand—not scientific literature—may drive design trends. I have been

informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

44. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would have yielded nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art, and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

45. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to

combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

46. I am not aware of any evidence of secondary considerations that would support a determination of nonobviousness of the claimed subject matter in the '562 patent.

47. I have been informed that, in an obviousness analysis, prior art must be analogous to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. TECHNOLOGY OVERVIEW

A. Group III-V Material Devices

48. Group III-V semiconductor materials have been viewed as promising for semiconductor device applications for at least three decades prior to the time of the alleged invention (August 25, 2009). Ex-1008, 2. Group III-V semiconductors include one group III element (Boron (B), Aluminum (Al), Gallium (Ga), and Indium (In)) and one group V element (Nitrogen (N), Phosphorus (P), Arsenic (As), and Antimony (Sb)). Ex-1009, 6. As members of the III- nitrides (group III-V semiconductors) family, AlN, GaN, InN and their alloys are all wide band-gap

materials. Ex-1008, 2. In view of the available wide range of direct bandgaps, GaN alloyed with AlN and InN may span a continuous range of direct bandgap energies throughout much of the visible spectrum well into the UV wavelengths, which makes the nitride system attractive for optoelectronic device applications, such as LEDs, laser (LDs), and detectors. Ex-1008, 2. A POSITA knew that the addition of III-nitrides to the family of device-quality semiconductors is essential for developing full-color displays and coherent sources for high-density optical storage technologies. Ex.-1008, 3.

49. Group III-nitrides were also known to be beneficial for high temperature and high-power electronics applications due to their two intrinsic properties: (1) their wide bandgap nature, and (2) their high breakdown fields. Ex-1008, 3. For example, the wide bandgap materials allow GaN power devices to operate with less cooling and fewer high-cost processing steps associated with complicated structures designed to maximize heat extraction. Ex-1008, 3. Additionally, GaN was known to have excellent electron transport properties, including good mobility, and high saturated drift velocity. Ex-1008, 4. These properties make GaN adequate for general electronics, and particularly promising for microwave rectifiers. Ex-1008, 4.

50. Additionally, group III-nitrides were known to support heterostructure technology. Ex-1008, 5. Quantum well, modulation-doped hetero-interface, and

heterojunction structures can all be made in this system, giving access to new spectral regions for optical devices and new operation regimes for electronic devices. Ex-1008, 5. Group III–nitrides were also known to have high mechanical and thermal stability. Ex-1008, 5.

B. HEMTs

51. High Electron Mobility Transistors (HEMTs), also known as a modulation doped field effect transistor (MODFET), were used for high power and/or high frequency applications by the time of the alleged invention (August 25, 2009). Ex-1010, [0004]. In a HEMT device, a two-dimensional electron gas (2DEG) may be formed at the heterojunction of two semiconductor materials with different bandgap energies. Ex-1010, [0004]. The smaller bandgap material may have a higher electron affinity than the wider bandgap material. Ex-1010, [0004]. The 2DEG is an accumulation layer in the undoped (“unintentionally doped”) smaller bandgap material, and can contain a relatively high sheet electron concentration. Ex-1010, [0004]. Additionally, electrons that originate in the wider bandgap semiconductor may transfer to the 2DEG, allowing a relatively high electron mobility due to reduced ionized impurity scattering. Ex-1010, [0004]. This combination of relatively high carrier concentration and relatively high carrier mobility were known to give the HEMT a relatively large transconductance, and may provide a performance

advantage over metal-semiconductor field effect transistors (MESFETS) for high-frequency applications. Ex-1010, [0004].

52. HEMTs were the most widely used heterostructure field effect transistors (FETs) by the time of the alleged invention (August 25, 2009). Ex-1011, 375. It had been shown that in HEMTs, the polar charges created at interfaces by piezoelectric and/or spontaneous polarization may also be exploited to create free charge. Ex-1011, 375. This approach was dominant in nitride-based devices. Ex-1011, 375.

53. Group III-V, such as Group III-nitride based, semiconductor devices comprising HEMTs were well-known before the time of the invention. *See, e.g.*, Ex-1011, Fig. 8.13(a)-(b) at 376, Fig. 8.22 at 393, Fig. 8.29 at 402, 402-403; Ex-1014 at 1023-1024; Ex-1010, [0044]. “Group III nitride” refers to those semiconducting compounds formed between nitrogen and the elements in Group III of the periodic table, usually aluminum (Al), gallium (Ga), and/or indium (In). Ex-1010, [0044]. *See also* ¶¶48-50. The term also refers to ternary and quaternary compounds such as AlGa_N and AlInGa_N. Ex-1010, [0044]. As had been well understood by a POSITA by August 2009 (the time of the alleged invention), the Group III elements can combine with nitrogen to form binary (e.g., GaN), ternary (e.g., AlGa_N, AlIn_N), and quaternary (e.g., AlInGa_N) compounds. Ex-1010, [0044]. These compounds may all have empirical formulas in which one mole of nitrogen is combined with a total

of one mole of the Group III elements. Ex-1010, [0044]. Accordingly, formulas such as $\text{Al}_x\text{Ga}_{1-x}\text{N}$, where $0 \leq x \leq 1$, may be used to describe these compounds. Ex-1010, [0044].

54. AlGaIn/GaN (group III-V semiconductor) HEMTs were known to have several benefits in power generation at high frequencies due to the high breakdown field and excellent electron transport properties. Ex-1012, 586. By the time of the alleged invention, GaN HEMTs were the most widespread and most advanced electronic nitride devices. Ex-1013, 71; Ex-1014, 1023. HEMTs were known to make full use of heterostructures and the advantageous breakdown and transport properties of undoped GaN. Ex-1013, 71. By the time of the alleged invention, AlGaIn–GaN HEMTs had demonstrated extremely promising results for use in broadband power amplifiers in base station applications due to the high sheet carrier concentration, electron mobility in the 2DEG channel and high saturation velocity. Ex-1008, 214.

C. Ohmic and Schottky Contacts

55. The interface between the metal and the semiconductor material can comprise either an ohmic contact or a Schottky contact, and both “ohmic and Schottky contacts” were known to be of “critical importance with respect to device functionality, performance, and long-term reliability” by the time of the alleged invention (August 25, 2009). Ex-1013, 144.

56. Ohmic contacts are formed from metal-semiconductor junctions or contacts that have a linear, non-rectifying I-V (current-voltage) characteristic. Ex-1011, 229. An ohmic contact is a low-resistance junction providing conduction in both directions between the metal and the semiconductor. Ex-1015, 344. Ideally, the current through the ohmic contact is a linear function of applied voltage, and the applied voltage should be very small. Ex-1015, 344. A POSITA knew about the two general types of ohmic contacts: (1) The ideal nonrectifying barrier, and (2) the tunneling barrier. Ex-1015, 344.

57. Ohmic contacts allow current to flow into and out of a semiconductor material without distortion of the signal. Ex-1016, 22. The most critical component of an ohmic contact is low specific contact resistance, which minimizes the power consumption of the contact and the internal heating of the contact, thereby prolonging device operation with predictable performance. Ex-1016, 22. The formation of ohmic contacts at a semiconductor surface requires a high density of states near the interface to push the Fermi-level in the semiconductor close to the conduction band. Ex-1013, 145. The vast majority of ohmic contacts depend on having a thin layer of very highly doped semiconductor material immediately adjacent to the metal-semiconductor interface. Ex-1017, 32. The heavy doping reduces the depletion width to such an extent that electrons can tunnel through the spiked barrier easily in either direction (from metal to semiconductor or from

semiconductor to metal). Ex-1011, 229, Fig. 5.7. Ohmic contacts were known to serve as the drain and source contacts in group III-V (e.g., $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$) HEMTs. Ex-1017, 1.

58. Schottky contacts are formed from metal-semiconductor junctions or contacts that have non-linear diode characteristics similar to those of the p-n diode, except that for many applications, it has a much faster response since carrier transport is unipolar. Ex-1011, 219.

59. Schottky contacts allow little or no current to flow through the contact until a critical voltage is reached, above which large amounts of current flow, which is called the forward biased region. Ex-1016, 25. In the reverse bias region, voltage is applied in the opposite direction and no current flows initially. Ex-1016, 25. However, if the voltage is pushed to a high enough value, then breakdown occurs, where a large amount of current flows through the contact and the contact is generally destroyed. Ex-1016, 25. Ideal Schottky contacts are formed in the absence of semiconductor/metal interface anomalies like dangling bonds, lattice imperfections, or impurities, which form so-called surface states (electronic states found at the surface of materials). Ex-1016, 25. When a metal and semiconductor are brought together, the Fermi levels must align such that a charge exchange occurs between the two materials. Ex-1016, 25. When this alignment in Fermi levels occurs, a space charge or depletion region is formed and a barrier to current flow is created.

Ex-1016, 25. Schottky contacts were known to have excellent rectifying properties, which make them suitable for high frequency applications. Ex-1017, 87. Schottky contacts were known to serve as the gate contacts in group III-V (e.g., $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$) HEMTs. Ex-1017, 1, 87. In these applications, Schottky contacts should have a high breakdown voltage and a low reverse current. Ex-1017, 2, 87.

D. Gate Contacts

60. FETs, including HEMTs (also known as MODFETs), were known to be made from a wide variety of materials, including group III-V materials by the time of the alleged invention (August 25, 2009). Ex-1011, 356; *see* Zhao ¶¶53-54. The basic concept of a FET is that electrons (or holes) flow from the source to the drain through an active channel of the device. Ex-1011, 356. The conductivity of the channel is modulated by a potential applied to the gate. Ex-1011, 356. This results in the modulation of the charge density flowing in the channel. Ex-1011, 356. It is important to isolate the gate from the channel so that no current flows into the gate. Ex-1011, 356.

61. The gate isolation is performed in a variety of ways, leading to many different devices. Ex-1011, 356. For example, in metal-semiconductor FETs, the gate forms a Schottky barrier with the semiconductor and the gate current is small in the useful range of gate voltages. Ex-1011, 356. HEMTs (MODFETs) use a large bandgap semiconductor to isolate the gate from the active channel. Ex-1011, 356.

Schottky contacts serve as the gate contacts in HEMTs. Ex-1017, 87; *see* Zhao ¶¶58-59.

E. Gate Dielectrics

62. Metal insulator and metal-oxide-based FETs were commonly used for III-nitride material systems by the time of the alleged invention (August 25, 2009). Ex-1013, 189. Dielectric materials are insulating materials commonly provided under gate structures to address gate leakage current in AlGaN/GaN HEMTs. Ex-1018, 937; Ex-1011, 396. Several materials were known to be used as insulating gate interfaces. Ex-1013, 189. In some applications, the conduction band offset of the gate dielectric and the semiconductor material underneath the gate dielectric leads to strong gate leakage currents. Ex-1013, 190. Gate stack materials (*see* ¶¶60-61) and gate dielectric materials may be selected to achieve desirable dielectric breakdown and leakage currents. Ex-1013, 190. In some applications, high-k dielectrics are attractive materials to increase charge control in GaN FETs. Ex-1013, 190. In some metal-insulator-semiconductor applications, the principal advantage of the device is the reduction of the gate-leakage by orders of magnitude. Ex-1013, 190. Moreover, a POSITA would have understood that an insulated gate electrode is a common structure in semiconductor devices and microelectronics. One commonly used device that was well known is the insulated gate bipolar transistor (IGBT).

F. Contact Metals

63. Metals are necessary to connect semiconductors to the “outside world” of voltage sources and circuits by the time of the alleged invention (August 25, 2009). Ex-1011, 216. Metals were known to be used as interconnects (i.e., low resistance conductors), to form Schottky barriers, to form ohmic contacts, and to form gates in transistors. Ex-1011, 216.

64. In semiconductor circuits, interconnects provide pathways through which charge travels from one point to another. Ex-1011, 216. Interconnects play an extremely important role in circuit performance. Ex-1011, 216. The metal strips making up the interconnect must be able to carry adequate current and make adequate contact with the devices. Ex-1011, 216.

65. Metal contacts in III-V nitride semiconductors were known to be “exceedingly important” in nearly all applications. Ex-1019, 425. It was well-known by August 2009 that a variety of metals can be chosen to form either a Schottky contact or an ohmic contact GaN devices. Ex-1020, 2861.

1. Titanium as Metal Layers

66. Titanium was commonly used in interconnect materials by the time of the time of the alleged invention (August 25, 2009) (Ex-1011, 220), including in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ and GaN (group III-V semiconductors) HEMT devices (Ex-1017, 2, 30, 50). Titanium was commonly used in metallization structures for Schottky

contacts and ohmic contacts with $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ and GaN (group III-V semiconductors). Ex-1017, 2, 30, 50, 97.

67. Using titanium as a bottommost metal layer in a metallization structure (e.g., depositing titanium on a group III-V material) was known to serve as an adhesion layer to provide good mechanical stability, dissolve the native oxide on the surface of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ material, and create nitrogen vacancies by reacting with nitrogen atoms from the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ material at the interface, rendering the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ material to be highly n-type doped. Ex-1017, 50. Additionally, it was well-known that using a thin layer of titanium as the bottommost metal layer in a metallization structure improves adhesion and provides a barrier for metal diffusion into the underlying semiconductor layer. Ex-1021, 92.

2. Aluminum or Aluminum Silicon as Metal Layers

68. Aluminum was commonly used as interconnect materials by August 25, 2009 (Ex-1011, 216), including in GaN (a group III-V semiconductor) devices (Ex-1020, 2859). In bulk, aluminum was known to be a good conductor and its alloys, such as aluminum silicon, were commonly used as metal contacts. Ex-1011, 216-217. A POSITA would know that aluminum was common, low-cost, and provide better adhesives to the metal stack, and improve thermal and mechanical properties of the structure. Ex-1035, 3, 7, 9-10, 12-14. A POSITA would know that

aluminum and aluminum alloys would have similar results and effects as a metal layer in a contact.

69. Aluminum was a well-known, common metal used in various contacts including Schottky contacts (Ex-1019, 427-428) and ohmic contacts (Ex-1019, 426-427).

3. Diffusion Barrier Layers

70. Diffusion barrier layers are layers that were known to prevent metals, such as copper, from diffusion into contacting materials by the time of the alleged invention (August 25, 2009). Ex-1022, Abstract. Diffusion barrier layers were known to be formed as a bottommost metal layer of a metallization structure. Ex-1022, Abstract, Figs. 1a and 1b, [0020]-[0023]. By August 2009, limiting the thickness of diffusion barrier layers (bottommost metal layers) was well-known. Ex-1022, Abstract; Ex-1023, 3:33-37; Ex-1024, 3:9-15. For example, fabricating thin diffusion barrier layers were known to be advantageous for fabricating devices with smaller feature sizes. Ex-1022, Abstract. Moreover, a POSITA would have understood that a thin diffusion barrier layer is preferred to save costs and fabrication time.

G. Refractory Metal Nitrides

71. Refractory metals are a class of metals that were known for resistance to heat and wear by the time of the alleged invention (August 25, 2009). Ex-1025,

120. The most common definition of refractory metals were metals comprising a melting point above 2,204°C, such as niobium, molybdenum, tantalum, tungsten and rhenium. *Id.* A wider definition of refractory metals included metals such as titanium. Ex-1027, 1.

72. By August 25, 2009, refractory metals had been known to be chemically bound with nitrogen to form refractory metal nitrides, such as TiN and TaN. Ex-1026, 2. Titanium nitride and tantalum nitride were well-known and widely used refractory metal nitrides (Ex-1026, 2) which possess a combination of useful mechanical and chemical properties such as hardness and heat resistance (Ex-1036, 156-157, 160). By August 2009, it was common and well-known to use titanium nitride as a diffusion barrier, conducting electrode, and antireflection coating layer in interconnect stacks due to its good thermal and mechanical properties and low resistivity. Ex-1028, 46. By August 25, 2009, it was common and well-known to use tantalum nitride in interconnect structures (e.g., as a diffusion barrier) due to its high thermal, mechanical, and chemical stability. Ex-1028, 56. It was well-known that titanium nitride and tantalum nitride could be used interchangeably as a diffusion barrier in semiconductor devices. Ex-1026, 2; Ex-1023, 3:39-43; Ex-1024, Abstract, 1:58-61.

73. By August 25, 2009, it was also well-known that refractory metal nitride capping layers are effective for reducing metal electromigration and

diffusion, such as copper electromigration and copper diffusion. Ex-1029, Abstract. It was well-known that metals, such as copper, can readily diffuse into surrounding materials, leading to line-to-line leakages and eventual device failure. Ex-1029, 1:29-34. Refractory metal nitride capping layers were known to be effective in preventing copper electromigration and diffusion in semiconductor devices. Ex-1029, 2:47-51.

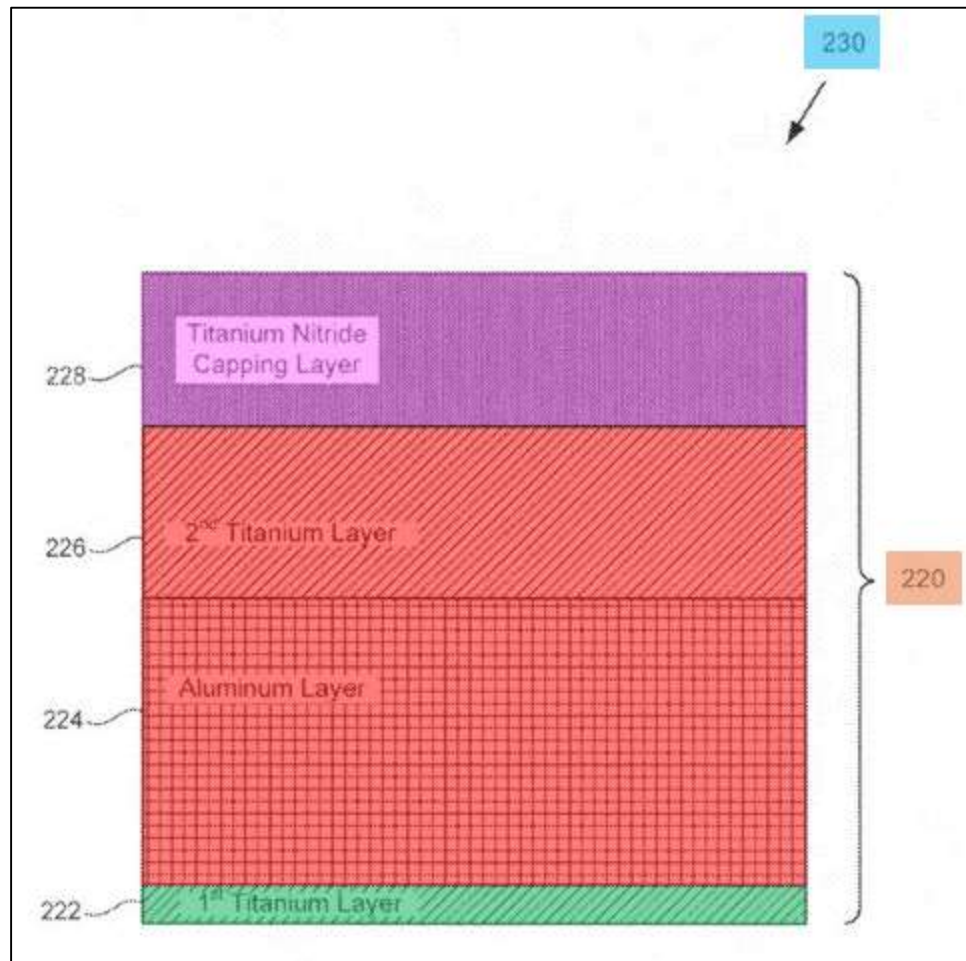
VII. THE '562 PATENT

A. Overview

74. The '562 patent describes an electrical contact capping layer alternative to gold capping layers, which may be costly and may diffuse through the electrode stack, making it difficult to integrate III-nitride power semiconductor devices with silicon devices. '562 patent, 1:44-55. Its electrical contact applies to group III-V semiconductor devices, including high electron mobility transistors (HEMT). '562 patent, 2:43-55.

75. Figure 2 shows **electrical contact 230**, corresponding to any of a source electrode, drain electrode or gate electrode. '562 patent, 3:39-42. **Electrical contact 230** comprises **electrode stack 220**, which includes **capping layer 228** consisting only of a refractory metal nitride, such as titanium nitride, over metal layers such as **titanium layer 226**, **aluminum layer 224**, and **titanium layer 222**. *Id.*, 3:39-45.

Capping layer 228 has a thickness greater than that of the bottommost metal layer, **titanium layer 222**. '562 patent, Fig. 2, 4:25-27, 5:15-17.



'562 patent, Fig. 2 (annotated).

VIII. CLAIM CONSTRUCTION

76. I understand that the United States Patent and Trademark Office interprets claim terms in an *inter partes* review proceeding under the same claim construction standard that is used in a United States federal court. I understand that, under this standard, the meaning of claim terms is considered from the viewpoint of a person of ordinary skill in the art at the time of the alleged invention.

77. I have been informed that claim terms are generally given their ordinary and customary meaning as understood by one of ordinary skill in the art in light of the specification and the prosecution history pertaining to the patent. I understand, however, that claim terms are generally not limited by the embodiments described in the specification.

78. I understand that in addition to the claims, specification, and prosecution history, other evidence may be considered to ascertain the meaning of claim terms, including textbooks, encyclopedias, articles, and dictionaries. I have been informed that this other evidence is often less significant and less reliable than the claims, specification, and prosecution history.

79. I understand that a district court has yet to construe the claim terms of this patent. At this time, I do not see the need to construe any terms of the challenged claims for the purposes of this proceeding. Therefore, in preparing my analysis, I have applied the ordinary and customary meaning that each claim term would have to a person of ordinary skill in the art in light of the '562 patent's specification and prosecution history. If any claim terms are differently construed, I reserve the right to reassess my opinions under said constructions.

IX. LEVEL OF ORDINARY SKILL IN THE ART

80. In rendering the opinions set forth in this declaration, I have been asked to consider the '562 patent's claims and the prior art through the eyes of a person of

ordinary skill in the art (which I may also refer to as “one skilled in the art,” “skilled artisan,” “POSITA,” or similar variations). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

81. Taking into consideration the factors described in Section V.A, it is my opinion that a POSITA at the time of the purported invention would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design. Additional education could substitute for professional experience and vice versa.

82. I met the criteria for a POSITA as of the earliest alleged priority date of the '562 patent.

X. GROUNDS OF UNPATENTABILITY

83. Based on my review of the materials set forth above, including my application of the knowledge of a person of ordinary skill in the art (“POSITA”), it is my opinion that claims 1-17 of the '562 patent are anticipated or would have been obvious to a POSITA. In particular, it is my opinion that claims 1-17 of the '562 patent would have been anticipated and/or obvious to a POSITA at the effective filing date of the '562 patent, based on the grounds shown below:

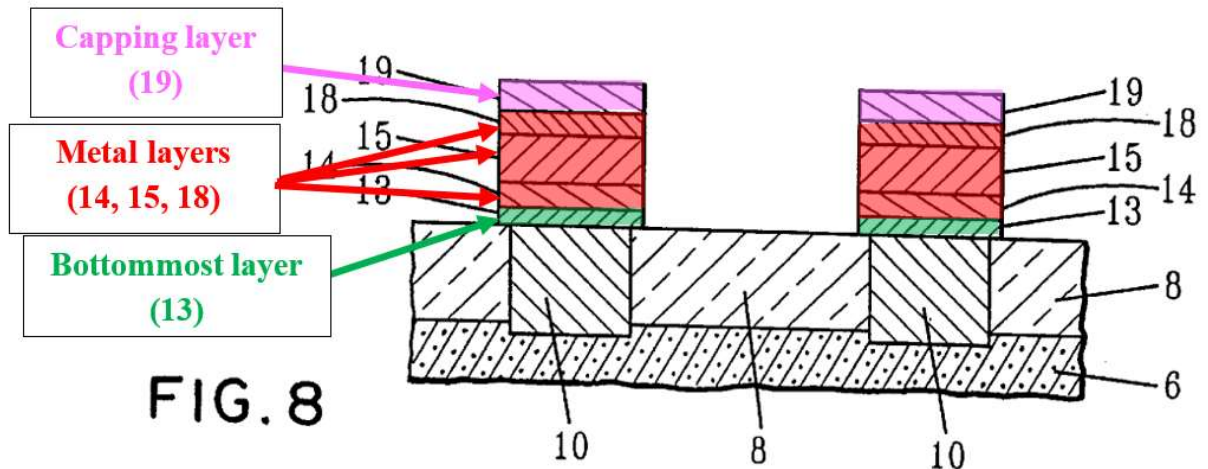
Grounds	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§102	Usui
2	3, 8, 12, 13 and 17	§103	Usui and Yu
3	9, 11, 14 and 16	§103	Usui, Yu, and Adesida
4	10 and 15	§103	Usui, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§103	Yu and Usui
6	9, 11, 14, and 16	§103	Yu, Usui, and Adesida
7	10 and 15	§103	Yu, Usui, and Sugimoto

A. Ground 1: Usui Anticipates Claims 1, 2, and 4-7

1. Usui

84. Usui relates to metallization structures for forming electrical connections with enhanced electromigration. Usui, Abstract, 5:11-16. Usui discloses using metal layers that allow subsequently applied metallic layers to be carefully controlled, which is essential to achieve the necessary properties of the structure. Usui, 3:29-37.

85. Usui's metallization structure has **capping layer 19 (capping layer)** that is thicker than **underlayer 13 (bottommost metal layer)** (Usui, 3:29-33, 4:5-8) and **layer 15 (second metal layer)** comprising **aluminum** or an **aluminum alloy**, with typical aluminum alloys like **silicon**. *id.*, 3:39-43.



Usui, Fig. 8 (annotated).

86. As I explain in my Technology Overview section, by August 2009, it was well-known that metallization structures limit the thickness of the bottommost metal layer to carefully control subsequently applied metallic layers (Usui, 3:29-37) and that aluminum and aluminum alloys are common, low-cost, provide better adhesives to the metal stack, and improve thermal properties of the structure. Additionally, any of the materials disclosed by Usui are viable options for **layer 15 (second metal layer)** according to Usui, which allows for design choice and creativity of a POSITA in assembling various devices using different materials depending on the application. A POSITA would have been motivated to use aluminum or aluminum silicon as **layer 15 (second metal layer)** in Usui's device, and done so with a reasonable expectation of success, because metallization structures with layers made of aluminum or aluminum silicon were well known by

August 2009 and constituted a simple design choice depending on the application of the device.

87. Usui is analogous to the '562 patent because it is in the same field of endeavor, forming electrical contacts for semiconductor devices (Usui, Abstract; '562, Abstract), and addresses the same problem of providing enhanced or simplified fabrication as the '562 patent (Usui, 4:1-3; '562, 1:25-29, 1:56-62).

2. Claim 1

a. **[1pre]: An electrical contact for use on a semiconductor device, said electrical contact comprising:**

88. If limiting, Usui discloses [1pre] because Usui is directed to a metallization structure, featuring group IVA metals (e.g., transition metals including titanium, zirconium, hafnium, and rutherfordium) (Usui, Abstract) for forming electrical connections (contacts) (*id.*, Abstract).

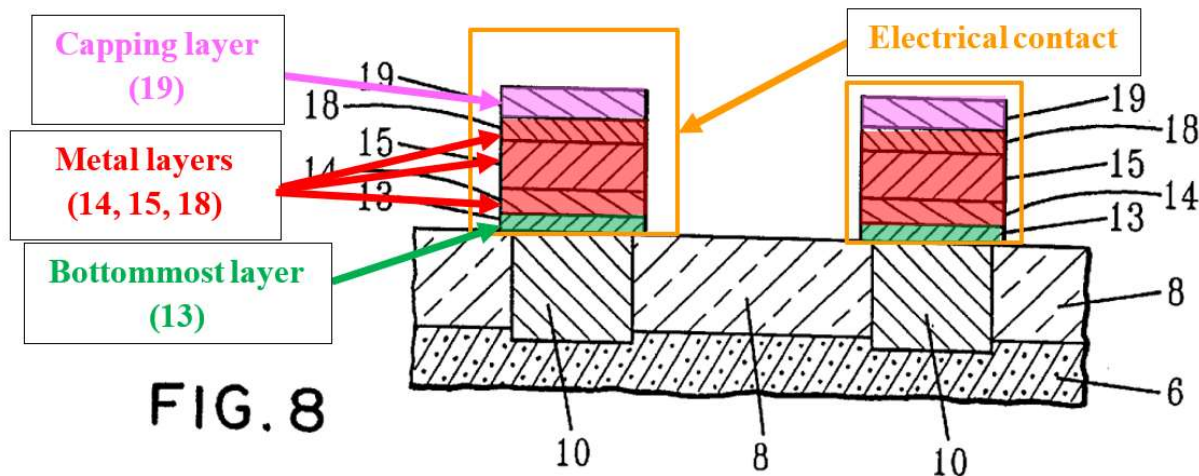
b. **[1a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;**

89. Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8.

90. Usui discloses a plurality of metal layers. Usui's **layer 18** comprises titanium (**metal layer**) (Usui, 4:4-5, Figs. 1 and 8), **layer 15** comprises aluminum or aluminum alloy (**metal layer**) (*id.*, 3:38-41, Figs. 1 and 8), **layer 14** comprises

titanium nitride (**metal layer**) (*id.* 3:58-60, Figs. 1 and 8) and **underlayer 13** comprises titanium (**bottommost metal layer**) (collectively, a plurality of metal layers). *Id.*, 5:38, 52, Figs. 1 and 8.

91. Usui discloses a capping layer. Usui's **capping layer 19** is **titanium nitride** and is formed above the plurality of **metal layers** (Usui, 5:54-59) forming a top of the **metallization structure (electrical contact)**. *Id.*, Abstract, 3:2-8, Figs. 1 and 8.



Usui, Fig. 8 (annotated).

- c. [1b]: said capping layer consisting only of a refractory metal nitride,

92. Usui discloses [1b] because its **capping layer 19** is formed only of **titanium nitride (refractory metal nitride)** (Usui, 5:54-59). A POSITA would have known that titanium nitride is a “refractory metal nitride.”

93. As I explained in Section VI.G, refractory metals are a class of metals known for resistance to heat and wear. Section VI.G. The most common definition of refractory metals are metals comprising a melting point above 2,204°C, such as niobium, molybdenum, tantalum, tungsten and rhenium. Section VI.G. A wider definition of refractory metals includes metals such as titanium. Section VI.G. Titanium nitride was a well-known and widely used refractory metal nitride which possesses a useful combination of useful mechanical and chemical properties such as hardness and corrosion and heat resistance. Section VI.G.

- d. **[1c]: said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.**

94. Usui discloses [1c] because its **capping layer 19** is **titanium nitride (refractory metal nitride)** (Usui, 5:54-59) and forms a top of the **metallization structure (electrical contact)**. *Id.*, Abstract, 3:2-8, Figs. 1 and 8. Usui's underlayer 13 is the bottommost layer of its metal layers. Usui's **underlayer 13** comprises a thickness between about 90-110 Å and is described as being critical to the layered metal structure because by limiting the thickness of the underlayer, the structure and texture of subsequently applied metallic layers may be carefully controlled. *Id.*, 3:29-35. Usui's **capping layer** has a thickness of about 150-800 Å, more typically about 200-500 Å (*id.*, 4:5-8), which is greater than the thickness of **underlayer 13 (bottommost layer** of plurality of metal layers). *Id.*, 5:38, 52, Figs. 1 and 8.

3. Claim 2 – The electrical contact of claim 1, wherein said capping layer comprises titanium nitride (TiN).

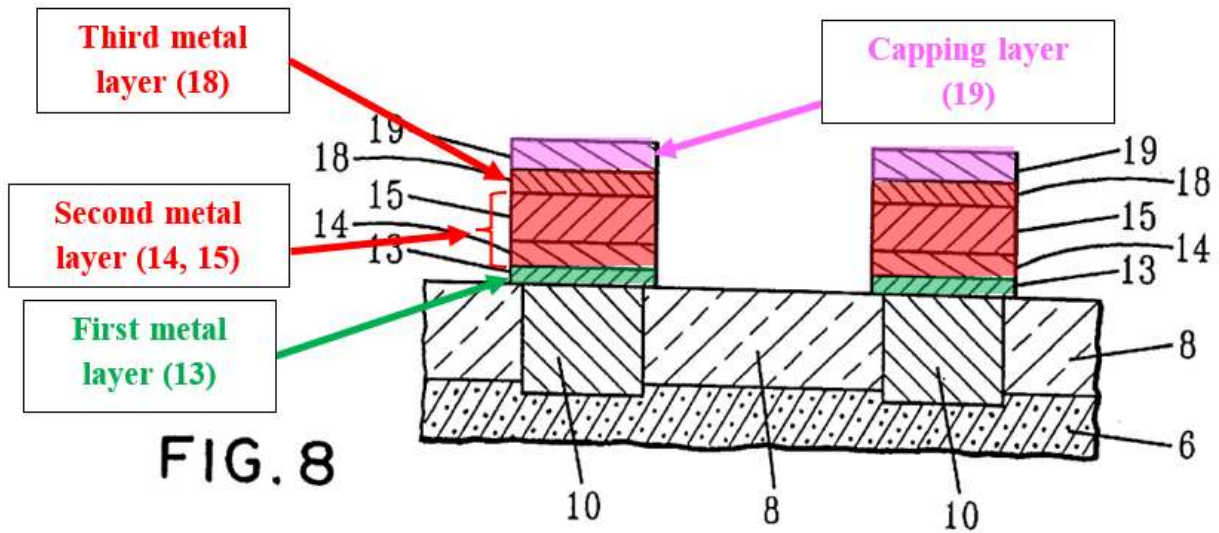
95. Usui discloses claim 2 because its **capping layer 19** is **titanium nitride**.

Usui, 5:54-59.

4. Claim 4 – The electrical contact of claim 1, wherein said plurality of metal layers includes respective first, second, and third metal layers, wherein said second metal layer is formed between said first metal layer and said third metal layer, and said capping layer is formed on said third metal layer.

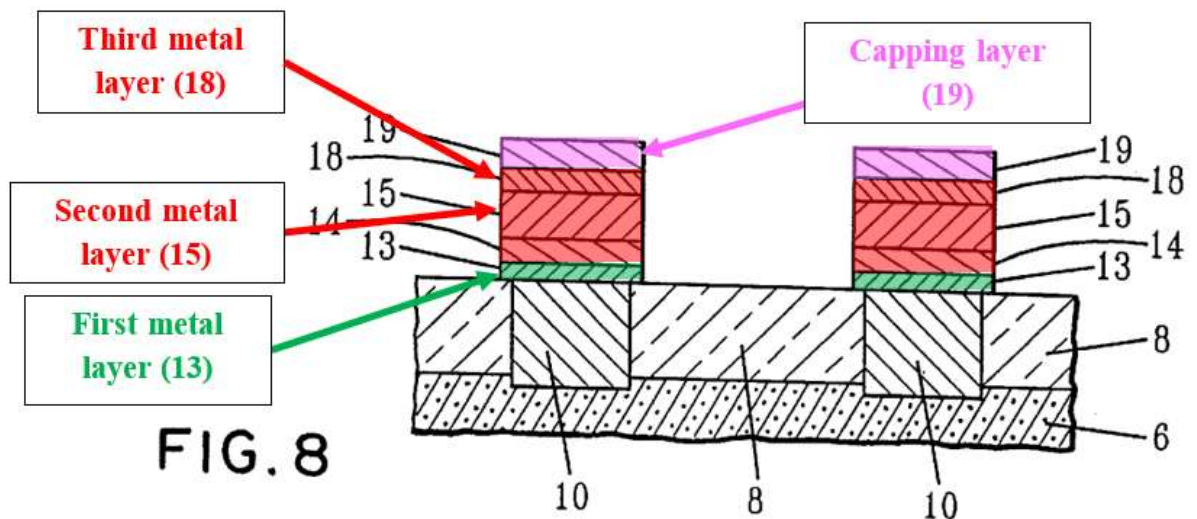
96. Usui discloses claim 4 because it has three metal layers (first, second, and third) with the second formed between the first and third layer, and with a capping layer on top of the third layer.

97. Usui's **layer 18** is titanium and sits directly beneath the capping layer (**third metal layer**) (Usui, 4:4-5, Figs. 1 and 8), **layer 14, 15** comprises aluminum or aluminum alloy (**second metal layer**) and sits between layer 18 (third layer) and underlayer 13 (bottommost layer) (*id.*, 3:38-41, Figs. 1 and 8), and **underlayer 13** beneath the second metal layer (**bottommost first metal layer**) (*id.*, 5:38, 52, Figs. 1 and 8). Usui's **capping layer 19** is formed on **layer 18 (third metal layer)**. *Id.*, 5:54-59.



Usui, Fig. 8 (annotated).

98. Additionally, Usui's **layer 15** comprises aluminum or aluminum alloy (**second metal layer**) and sits between layer 18 (third layer) and underlayer 13 (bottommost layer) (*id.*, 3:38-41, Figs. 1 and 8).



Usui, Fig. 8 (annotated).

5. Claim 5 – The electrical contact of claim 4, wherein said first metal layer and said third metal layer of said electrode stack comprise titanium (Ti).

99. Usui discloses claim 5 because its first metal layer and its third metal layer comprise titanium.

100. Usui's **underlayer 13 (bottommost first metal layer)** is titanium (Usui, 5:23-24) and **layer 18 (third metal layer)** is titanium (*id.*, 5:51-52).

6. Claim 6 – The electrical contact of claim 4, wherein said second metal layer of said electrode stack comprises aluminum (Al).

101. Usui discloses claim 6 because its **layer 15 (second metal layer)** comprises aluminum or an aluminum alloy. Usui, 3:38-41, Figs. 1 and 8. Usui's aluminum or aluminum alloy layer, **layer 15 (second metal layer)**, is described as a highly textured layer with improved electromigration performance. *Id.*, 3:49-56.

7. Claim 7 – The electrical contact of claim 6, wherein said second metal layer of said electrode stack further comprises silicon (Si).

102. Usui discloses claim 7 because its **layer 15 (second metal layer)** comprises an aluminum alloy, where typical metal alloys include alloying metal such as **silicon** (Usui, 3:38-43, Figs. 1 and 8). Specifically, Usui discloses “[t]ypical aluminum alloys include alloying metal such as copper, magnesium, silicon, lanthanides such as vanadium and yttrium; and palladium” (*id.*).

103. While in Usui, an aluminum alloy comprising silicon is one of 7 possible alloys, the use of an aluminum alloy featuring silicon, in my opinion, still

have been immediately apparent to one of ordinary skill in the art because such an alloy is customary and well-known in the field.

104. For example, Ex-1030 discloses an interconnect for use in integrated circuits and describes a *preferred* embodiment where an aluminum-based film 14 is an aluminum-silicon alloy (Ex-1030, Abstract, 3:25-27, Figs. 1(a)-1(c)). Ex-1031 discloses a multilayered semiconductor device including an interconnection layer and an interconnect featuring an aluminum-silicon-copper alloy layer 43 on which a titanium based alloy layer 44 is deposited on (Ex-1031, Abstract, 7:44-54, Fig. 13).

B. Ground 2: Usui in View of Yu Renders Obvious Claims 3, 8, 12-13, and 17

1. Overview of the Combination and Motivations to Combine

105. Usui does not expressly disclose that its capping layer is tantalum nitride, that its electrical contact is used in a III-V semiconductor device, or a gate insulator layer. Each of these, however, were commonly known in the art and expressly taught by Yu. Sections VI.A, VI.D, VI.E, VI.G.

a. Claim 3 – A POSITA would have been motivated to implement Usui’s capping layer as tantalum nitride, as taught by Yu.

106. Usui’s **capping layer** is not expressly comprised of **tantalum nitride** (claim 3), but Yu expressly discloses a **capping layer** comprising **tantalum nitride**. Yu, [0036].

107. By August 2009, it was common and well-known to use tantalum nitride in interconnect structures due to its high thermal, mechanical, and chemical stability. Section VI.G. Further, as I explained in Section VI.G, it was well-known that titanium nitride and tantalum nitride could be used interchangeably in semiconductor devices. For example, Ex-1032 discloses a cap layer formed of tantalum nitride (Ex-1032, claim 13).

108. It is my opinion that a POSITA would have appreciated that replacing the titanium nitride of Usui with the tantalum nitride of Yu is merely a suitable design alternative because Yu discloses both titanium nitride (the material expressly disclosed in Usui as the second metal layer) and tantalum nitride may be employed—combining prior art elements according to known techniques to a known device ready for improvements in thermal, mechanical and chemical stability, to yield predictable results. *See* Section VI.G.

109. In my opinion, a POSITA would have been motivated to use a tantalum nitride layer to obtain predictable results and would have expected success because tantalum is a known refractory metal and using tantalum nitride as a capping layer in an electrode stack had known benefits and was known in the art. *See* Section VI.G.

b. Claims 8 and 13 – A POSITA would have been motivated to implement Usui’s electrical contact in a group III-V semiconductor device as taught by Yu.

110. Usui does not expressly disclose that its electrical contact is configured for implementation on a group III-V semiconductor device, as taught by Yu. By August 2009, as I explained in Section VI.A, group III-V semiconductor devices were well-known and widely used. For example, group III–nitride semiconductors are essential for developing full-color displays and coherent sources for high-density optical storage technologies. Section VI.A. Group III- nitrides were also known to be beneficial for high temperature and high-power electronics applications. Section VI.A. Group III–nitrides can support heterostructure technology and have high mechanical and thermal stability. Section VI.A. Additionally, GaN was known to have excellent electron transport properties, including good mobility, and high saturated drift velocity. Section VI.A.

111. Usui describes its electrical connections are useful to provide connections or wirings between active and/or passive devices of an integrated circuit (Usui, 1:11-15) (i.e., the devices disclosed in Yu). A POSITA would have been motivated to implement the electrical contacts as taught by Usui in group III-V semiconductor devices, as taught by Yu, as group III-V semiconductor devices are commonly used in the field for active and/or passive devices—combining prior art

elements according to known techniques to a known device ready for improvement to yield predictable results. *See* Section VI.A.

c. Claims 12 and 17 – A POSITA would have been motivated to implement Usui’s device as a III-V device with a gate insulator layer, as taught by Yu.

112. Usui does not expressly disclose an electrical contact implemented with a gate insulator layer underlying a first metal layer of the electrode stack to provide an insulated gate electrode for the group III-V semiconductor device (claims 12 and 17), but Yu does. Yu discloses a multilayer active III-V based semiconductor device (i.e., a thin film transistor) featuring an **interfacial dielectric layer 214** and a **high-k dielectric layer 216 (gate insulator layer)** (Yu, [0039]) underlying a metal **diffusion barrier/protection layer 218 (first metal layer)** (Yu, [0029]).

113. Usui describes an electrical contact suitable to provide connections or wirings between active and/or passive devices of an integrated circuit (Usui, 1:11-15). Usui further discloses towards a contact for improving electromigration characteristics (Usui, 2:33-35).

114. By August 2009, as I explained in Section VI.A, Group III-V based materials were well-known for being promising materials for semiconductor device applications as such materials comprise a wide bandgap and high breakdown fields. Further, as I explained in Section VI.D, it was well-known that an important design aspect in thin film transistors is isolating the gate from the channel so that no current

flows. To a POSITA it would have been obvious to implement the electrical contact of Usui with Yu's gate insulator layer because Usui discloses the importance of improving electromigration characteristics and such layers are commonly provided under gate structs to address gate leakage— combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. Section VI.E.

2. Claim 3 – The electrical contact of claim 1, wherein said capping layer comprises tantalum nitride (TaN).

115. Usui in view of Yu renders obvious claim 3 because Yu discloses a capping layer 226 comprised of **tantalum nitride** and it would have been obvious to implement Usui's capping layer as tantalum nitride. (Yu, Fig. 2, [0036]). Yu discloses “the capping layer 226 may comprise polycrystalline silicon; silicon containing materials; germanium containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, **tantalum nitride**, nickel silicide, cobalt silicide, other proper conductive materials, and combinations thereof” (emphasis added) (*id.*).

116. It would have been obvious to implement Usui's capping layer as comprising tantalum nitride as explained in Section X.B.1.a.

3. Claim 8 – The electrical contact of claim 1, wherein said electrical contact is configured for implementation on a group III-V semiconductor device.

117. Usui in view of Yu renders claim 8 obvious because Yu discloses a semiconductor transistor device with a semiconductor substrate comprising silicon, germanium, **a group III-V material** (Yu, [0023]).

118. Usui discloses an electrical contact suitable to provide connections or wirings between active and/or passive devices of an integrated circuit for improving electromigration characteristics (Usui, 1:11-15, 2:33-35), such as the device disclosed by Yu.

119. As I explained in Section VI.A, by August 2009, Group III-V based materials are well-known as being promising materials for semiconductor devices such as the transistor of Yu. As Usui's device provides improved electromigration characteristics, it would have been obvious for the POSITA to place the Usui contact in the III-V semiconductor transistor of Yu as such materials (i.e., III-V materials) are commonplace within the field and was known in the art, as evidenced by Section X.B.1.b. *See* Sections VI.A, VI.D.

4. **Claim 12 – The electrical contact of claim 8, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.**

120. Usui in view of Yu renders claim 12 obvious because Yu discloses a semiconductor transistor device with a semiconductor substrate comprising silicon, germanium, **a group III-V material** (Yu, [0023]). Yu discloses an **interfacial dielectric layer 214** and a **high-k dielectric layer 216 (gate insulator layer)** (Yu, [0039]) underlying a metal **diffusion barrier/protection layer 218 (first metal layer)** (Yu, [0029]).

121. Usui discloses an electrical contact suitable to provide connections or wirings between active and/or passive devices of an integrated circuit for improving electromigration characteristics (Usui, 1:11-15, 2:33-35).

122. By August 2009, Group III-V based materials were well-known as being promising materials for semiconductor devices such as the transistor of Yu. As Usui's device provides improved electromigration characteristics, it would have been obvious for the POSITA to place the Usui contact in the transistor of Yu and to further include the gate insulator layer as such layers are commonplace within the field and was known in the art, as evidenced by Section X.B.1.c. *See* Sections VI.A, VI.D, VI.E.

5. Independent Claim 13

- a. [13pre]: An electrical contact for use on a group III-V semiconductor device, said electrical contact comprising:**

123. [13pre] is identical to [1pre] and claim 8. [13pre] is obvious as explained for [1pre] and claim 8.

- b. [13a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;**

124. [13a] is identical to [1a]. [13a] is obvious as explained for [1a].

- c. [13b]: said capping layer consisting only of a metal selected from the group consisting of titanium nitride (TiN) and tantalum nitride (TaN),**

125. [13b] is identical to claims 2 and 3. [13b] is obvious as explained for claims 2 and 3.

- d. [13c]: said metal forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.**

126. [13c] is identical to [1c]. [13c] is obvious as explained for [1c].

- 6. Claim 17 – The electrical contact of claim 13, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.**

127. Claim 17 is identical to claim 12, but depends from claim 13. Claim 17 is obvious as explained for claim 12.

C. Ground 3: Usui in View of Yu and Further in View of Adesida Renders Obvious Claims 9, 11, 14, and 16

1. Overview of the Combination and Motivations to Combine

128. Usui and Yu do not expressly disclose its electrical contact being configured for implementation on a HEMT, or its electrical contact being implemented as a gate electrode making Schottky contact.

129. Adesida is analogous to the '562 patent because it is in the same field of endeavor, forming electrical contacts for semiconductor devices (Adesida, Abstract; '562, Abstract), and addresses the same problem of providing enhanced or simplified fabrication as the '562 patent (Adesida, [0015]-[0017], [0032]-[0034]). Consistent with the '562 patent, Adesida discloses a gate electrode making Schottky contact and power electrodes (source and drain electrodes) making ohmic contact. Adesida, [0031]. Similar to Yu, Adesida also discloses a III-V semiconductor device (*id.*).

a. Claims 9 and 14 - A POSITA would have been motivated to implement Usui's electrical contact on a group III-V semiconductor device, as taught by Yu, comprises a high electron mobility transistor (HEMT) as taught by Adesida.

130. Usui and Yu do not expressly disclose a high electron mobility transistor (HEMT), as taught by Adesida. As I explained in Section VI.B, by August 2009, as I explained in Section VI.B, it was well-known that HEMTs are used for high power and/or high frequency applications. HEMTs were the most widely used

heterostructure field effect transistors. Section VI.B. As I explained in Section VI.B, it was well-known that the combination of relatively high carrier concentration and relatively high carrier mobility can give the HEMT a relatively large transconductance, and may provide a performance advantage over metal-semiconductor field effect transistors (MESFETS) for high-frequency applications.

131. Usui discloses the importance of enhanced electromigration. Usui, Abstract. A POSITA would have been motivated to implement the electrical contacts as taught by Usui and Yu in group III-V semiconductor HEMT, as taught by Adesida, because group III-V material HEMTs were well-known at the time for providing relatively high carrier mobility (Section VI.B) and thus enhanced electromigration and both Yu and Adesida are directed towards the use of III-V semiconductor devices. Furthermore, it was well-known at the time that including the Usui-Yu device on a HEMT, as taught by Adesida, and constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications) - combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *See* Sections VI.A, VI.B.

- b. Claims 11 and 16 - A POSITA would have been motivated to implement Usui's electrical contact as a gate electrode making Schottky contact, as taught by Adesida, with said group III-V semiconductor device as taught by Yu.**

132. Usui and Yu do not expressly disclose an electrical contact implemented as a gate electrode making Schottky contact. But Adesida does. Like Yu, Adesida teaches the use of a III-V semiconductor device. As I explained in Section VI.C, by August 2009, it was well-known that Schottky contacts are of critical importance with respect to device functionality, performance, and long-term reliability. It was well-known that Schottky contacts serve as gate contacts in group III-V devices and have excellent rectifying properties, which make them suitable for high frequency applications. Section VI.C.

133. Usui discloses the importance of enhanced electromigration. Usui, Abstract. A POSITA would have been motivated to implement the electrical contacts as taught by Usui-Yu as a gate electrode making Schottky contact, as taught by Adesida, because both Yu and Adesida disclose the use of III-V semiconductor devices. Furthermore, Schottky contacts are well known for their suitability for high frequency applications and therefore enhanced electromigration. Furthermore, it was well-known at the time that implementing the Usui-Yu contact as a Schottky contact, as taught by Adesida, constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications)—

combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *See* Sections VI.A, VI.B, VI.C.

2. Claim 9 – The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).

134. Usui in view of Yu and Adesida renders obvious claim 9 because Adesida discloses a HEMT. Adesida explains that its device is a “**high electron mobility transistor (HEMT)**, which is a field-effect **HEMT** formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT).” Adesida, [0031]. A HEMT is an active device which Usui explicitly states its electrical contacts are suitable for (Usui, 1:11-15). It would have been obvious to implement the electrical contact of Usui-Yu on HEMTs, as taught by Adesida, because both Yu and Adesida disclose III-V semiconductor devices and as I further explained in Sections X.C.1, X.C.1.a, VI.A, VI.B.

3. Claim 11 – The electrical contact of claim 8, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

135. Usui in view of Yu and Adesida renders obvious claim 11 because Adesida discloses “a field-effect device, comprising: a layered semiconductor structure that includes a channel layer and at least one layer over the channel layer; spaced apart source and drain contacts disposed over said at least one layer and

communicating with the channel layer; and an iridium gate, between the source and drain contacts, **forming a Schottky barrier contact on said at least one layer.**"

Adesida, [0016].

136. Adesida discloses a HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105, on which is an **In_{0.52}Al_{0.48}As barrier layer 150 (group III-V semiconductor device)**. InAlAs is a well-known group III-V material—as I discussed in Sections VI.A, X.C.1, and X.C.1.b. Adesida, Fig. 5 and [0031]. **Gate 190 (gate electrode)** is formed as a **Schottky barrier contact (Schottky contact)** on the **In_{0.52}Al_{0.48}As barrier layer 150 (group III-V semiconductor device)**. Adesida, Fig. 5 and [0031].

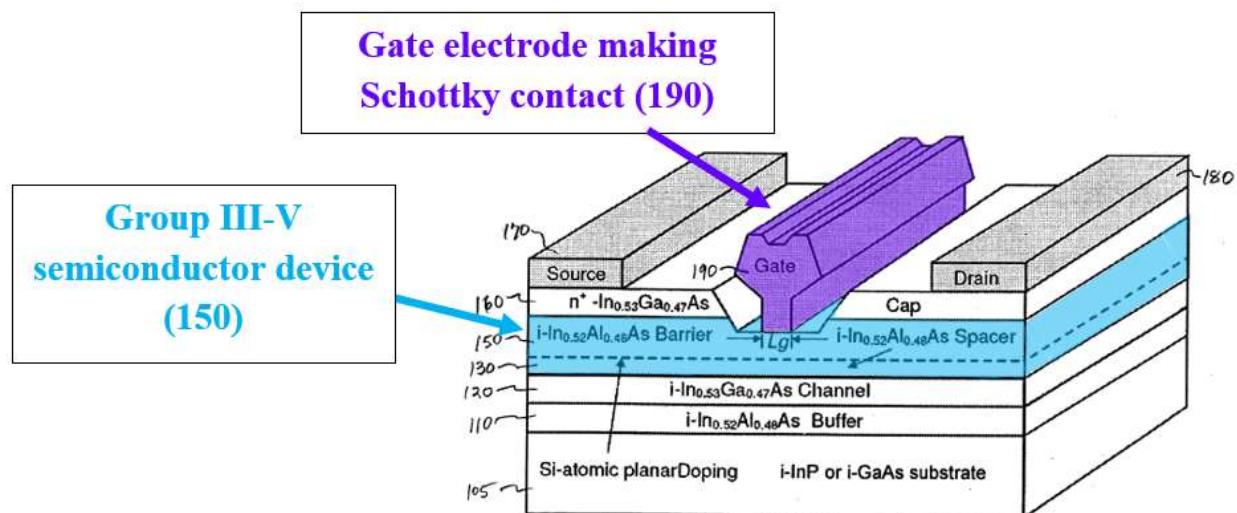


Figure 5

Adesida, Fig. 5 (annotated).

137. It would have been obvious to implement the electrical contact of Usui-Yu in a device with a gate electrode making Schottky contact, as taught by Adesida, as I explained in Sections VI.A, VI.B, VI.C, VI.D, X.C.1, X.C.1.b.

4. Claim 14 – The electrical contact of claim 13, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).

138. Claim 14 is identical to claim 9, but depends from claim 13. Claim 14 is obvious as explained for claim 9.

5. Claim 16 – The electrical contact of claim 13, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

139. Claim 16 is identical to claim 11, but depends from claim 13. Claim 16 is obvious as explained for claim 11.

D. Ground 4: Usui in View of Yu and Further in View of Sugimoto Renders Obvious Claims 10 and 15

1. Overview of the Combination and Motivation to Combine

140. Usui and Yu do not expressly disclose an electrical contact being implemented as a power electrode making ohmic contact, but Sugimoto does.

141. Like Yu, Sugimoto discloses a group III-V semiconductor device (Sugimoto, 9:7-9). Sugimoto further discloses a device with an AlGaN top layer. Sugimoto, Figs. 1, 3, 5, 7. AlGaN is a well-known group III-V material. *See* Section VI.A. Sugimoto further discloses the III-V semiconductor device is a HEMT. Sugimoto, 1:22-67.

142. Sugimoto is analogous to the '562 patent because it is in the same field of endeavor, forming electrical contacts for semiconductor devices (Sugimoto, 9:24-51; '562, Abstract), and addresses the same problem of providing enhanced or simplified fabrication as the '562 patent (Sugimoto, 6:3-7:12, 7:26-39, 7:56-60, 8:30-44). The '562 patent defines “[s]ource electrode 136 and drain electrode 138 are power electrodes ohmically coupled to the heterojunction formed by GaN layer 112 and AlGaIn layer 114.” '562 patent, 3:19-21. Consistent with the '562 patent, Sugimoto discloses a gate electrode making Schottky contact with a group III-V device and power electrodes (source and drain electrodes) making ohmic contact with the group III-V device. Sugimoto, 9:39-51. Sugimoto discloses that its “**drain electrode 42 and the source electrode 46 make ohmic contact with the top surface of the AlGaIn layer 34.**” Sugimoto, 9:39-51.

143. As I explained in Section VI.C, by August 2009, it was well-known that ohmic contacts were of critical importance with respect to device functionality, performance, and long-term reliability. It was well-known that ohmic contacts serve as source and drain contacts in group III-V devices and allow current to flow into and out of a semiconductor material without distortion of the signal. Section VI.C. It was well-known that the most critical component of an ohmic contact is its low specific contact resistance, which minimizes the power consumption of the contact and the internal heating of the contact, thereby prolonging device operation with

predictable performance. Section VI.C. Furthermore, ohmic contacts allow charges to flow easily between conductors without excess power dissipation, have linear current-voltage characteristics, and do not introduce voltage drops or power loss. Section VI.C. Such characteristics are essential for high-frequency operation used by devices such as the HEMT of Sugimoto. *See* Sections VI.B, VI.C.

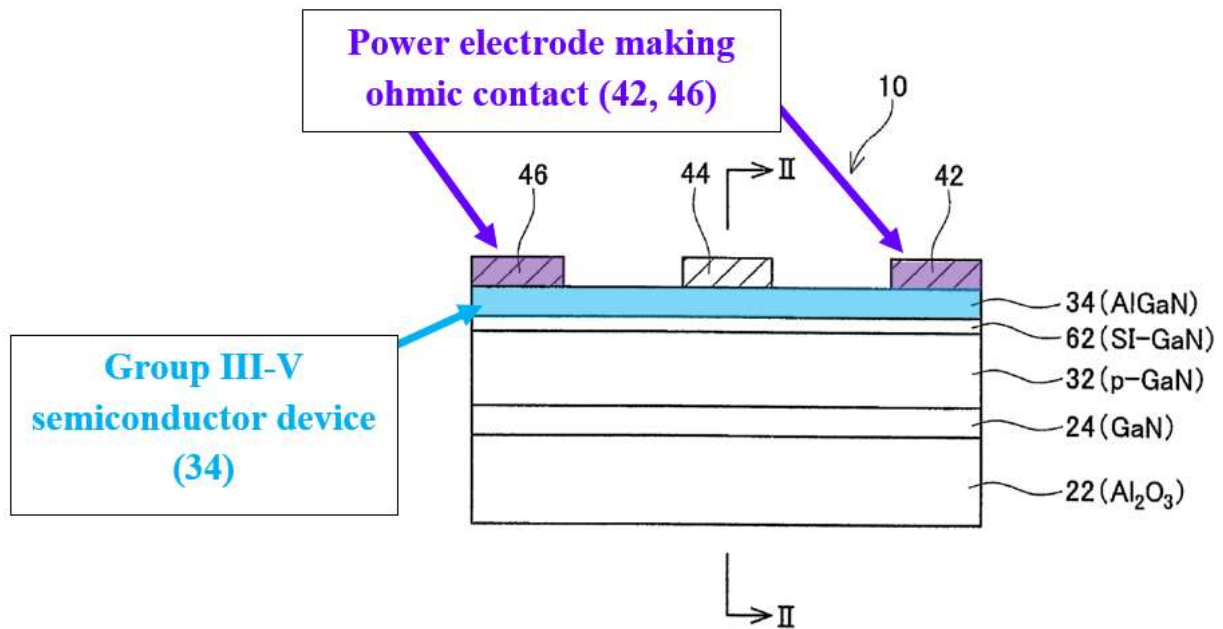
144. Usui disclosed the importance of enhanced electromigration. Usui, Abstract. A POSITA would have been motivated to implement the contact of Usui - Yu as a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide improved current flow (i.e., enhanced electromigration) and Sugimoto, like Yu, also teaches the use of III-V semiconductor devices. Furthermore, such a combination is the result of combining prior art elements according to known techniques to a known device ready for improvement to yield predicable results. Sections VI.B and VI.C; Adesida, [0031], Fig. 5.

2. Claim 10 – The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.

145. Usui in view of Yu and Sugimoto render obvious claim 10 because Sugimoto discloses a HEMT device with a power electrode making an ohmic contact.

146. Sugimoto discloses that its “**drain electrode 42 (power electrode)** and the **source electrode 46 (power electrode)** make **ohmic contact** with the top surface

of the **AlGaN layer 34 (group III-V semiconductor device)**.” (Sugimoto, 9:39-51).



Sugimoto, Fig. 1 (annotated).

147. As I explained in Sections VI.A, VI.B, VI.C, X.D.1, it would have been obvious to implement the electrical contact of Usui-Yu as a power electrode making an ohmic contact, as taught by Sugimoto because both Yu and Sugimoto disclose III-V semiconductor devices and ohmic contacts were typically employed in high-frequency operation devices, such as a HEMT.

3. Claim 15 – The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.

148. Claim 15 is identical to claim 10, but depends from claim 13. Claim 15 is obvious as explained for claim 10.

E. Ground 5: Yu in View of Usui Renders Obvious Claims 1-8, 12, 13, and 17

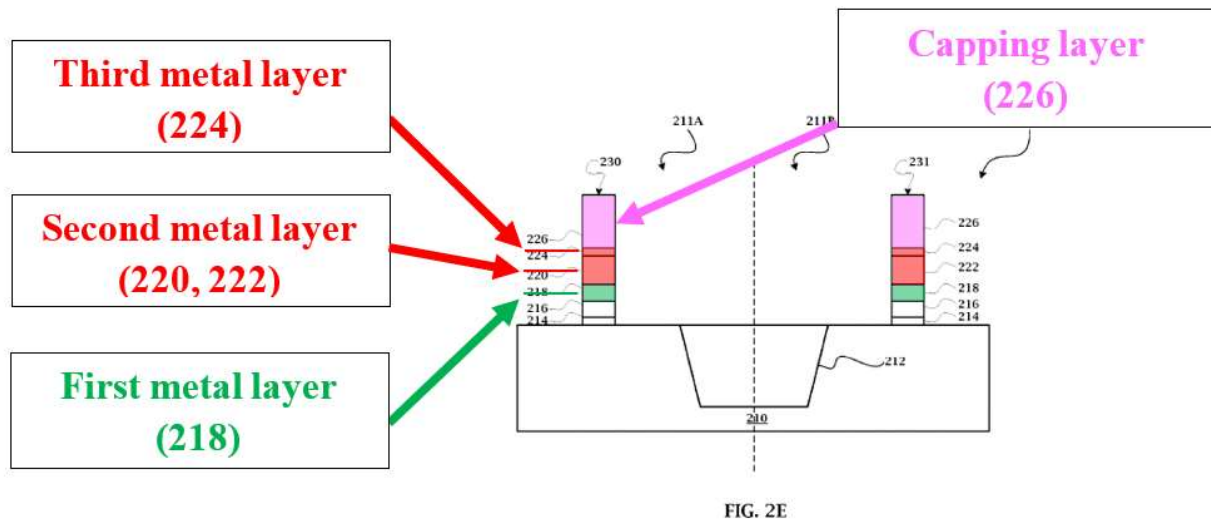
1. Yu

149. Yu discloses semiconductor devices with electrical connections (e.g., contacts) (Yu, [0040]) and forms metal layers of metal gate stacks with correct work function values and better thermal stability. Yu, [0033]. The work function represents the energy required to remove an electron from the semiconductor to the “free” vacuum level. Ex-1011, 147. In other words, the work function represents the barrier that restricts the flow of electrons in a material. Ex-1011, 229. One configuration involves using metal layers that provide optimal tuning of the work functions of the varying compositions of metal layers. Yu, [0033].

150. Like the '562 patent, Yu lists characteristics and variations of its device with trade-offs that were well-known by August 2009. For example, Yu's semiconductor device includes a semiconductor substrate comprising silicon, germanium, a **group III-V material**, or a group II-VI material. Yu, [0023]. Any of these materials were suitable options for the semiconductor device according to Yu, which allows for the design choice and creativity of a POSITA in assembling various devices using different materials depending on the application. A POSITA would have been motivated to implement Yu's device as a group III-V material semiconductor device, as Yu discloses, because semiconductor devices made of group III-V materials were well-known by August 2009 and constituted a simple

design choice depending on the application of the device. *See* Section VI.A. Additionally, by August 2009, it was well-known to refer to a semiconductor device with a group III-V semiconductor material in the substrate as a group III-V semiconductor device. *See* Section VI.A.

151. Yu's device includes **capping layer 226 (capping layer)** comprising polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, **titanium nitride**, **tantalum nitride**, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof ('562 patent, claims 2 and 3). Yu, [0036]. Any of these materials were suitable options for **capping layer 226 (capping layer)** according to Yu, which allows for the design choice and creativity of a POSITA in assembling various devices using different materials depending on the application. A POSITA would have been motivated to use titanium nitride or tantalum nitride as **capping layer 226 (capping layer)** in Yu's device, as Yu discloses, because by August 2009 titanium nitride and tantalum nitride were well-known refractory metal nitrides and widely used for their good thermal and mechanical properties and low resistivity and constituted a simple design choice depending on the application of the device. *See* Section VI.G.



Yu, Fig. 2E (annotated).

152. Yu's device also includes **diffusion barrier/protection layer 218** (**first metal layer**) comprising **titanium**, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof (Yu, [0029]) and **diffusion barrier layer 224** (**third metal layer**) comprising **titanium**, titanium nitride, tantalum, tantalum nitride, other suitable material, and/or combinations thereof (*id.*, [0035]) ('562 patent, claim 5). Any of these materials were suitable options for **diffusion barrier/protection layer 218** or **diffusion barrier layer 224** according to Yu, which allows for the design choice and creativity of a POSITA in assembling various devices using different materials depending on the application. A POSITA would have been motivated to use titanium as **diffusion barrier/protection layer 218** and **diffusion barrier layer 224** in Yu's device, as Yu discloses, because diffusion barrier layers made of titanium were well-known by August 2009 and

constituted a simple design choice depending on the application of the device. *See* Sections VI.F.1, VI.F.3. Yu's device also includes **capping layer 226** (**capping layer**) is preferably 600Å and **diffusion barrier/protection layer 218** (**bottommost layer**) is preferably 20Å (i.e., the **capping layer** is *preferably* thicker than the **bottommost layer**). This disclosure is made with respect to the **capping layer** being polysilicon (Yu, [0036], [0040]), which is not a **refractory metal nitride** as is stated in claims 1 and 13. However, Yu teaches the **capping layer** may be titanium nitride and tantalum nitride, which are **refractory metal nitrides**. Yu's device also includes **metal layers 220, 222** (**second metal layer**) comprise a doped-conducting metal oxide (DCO), where the DCO comprises "... ZnO doped with Al, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf, and/or combinations thereof...) (Yu, [0033]).

153. Yu is analogous to the '562 patent because it is in the same field of endeavor, semiconductor devices featuring an electrode stack featuring a plurality of metal layers (Yu, Abstract, Fig.2E, gate stacks 230 and 231; '562 patent, Abstract) and addresses the same problem, fabrication of semiconductor materials with improved characteristics (Yu, Abstract; '562 patent, 1:25-29, 1:56-62) as the '562 patent.

2. Overview of the Combination and Motivations to Combine

154. Claims 1-8, 12, 13, and 17 are directed to an electrical contact for use on a semiconductor device, including a capping layer thicker than a bottommost

metal layer ('562 patent, claims 1 and 13) and a second metal layer comprising aluminum or an aluminum and silicon ('562 patent, claims 6 and 7). Yu at least suggests these limitations, and Usui expressly discloses them. A POSITA would have found it obvious to combine Yu and Usui to achieve claims 1, 6, 7, and 13 because their combination is combining prior art elements according to known methods to yield predictable results, a simple substitution of one known element for another to obtain predictable results and applying known techniques to a known device ready for improvement to yield predictable results.

- a. **Claims 1 and 13 – A POSITA would have been motivated to form Yu's capping layer of a refractory metal nitride thicker than the bottommost metal layer, as taught by Usui.**

155. Yu expressly discloses every element of claims 1 and 13 except a **refractory metal nitride capping layer** having a thickness greater than that of a **bottommost layer** (claim element [1c]). While Yu discloses the **capping layer** is *preferably* 600Å and the **bottommost layer** 20Å (i.e., the **capping layer** is *preferably* thicker than the **bottommost layer**), this disclosure is made with respect to the **capping layer** being polysilicon (Yu, [0036], [0040]), which is not a **refractory metal nitride** as is stated in claims 1 and 13. However, Yu teaches the **capping layer** may be titanium nitride and tantalum nitride, which are **refractory metal nitrides**. A POSITA would have been motivated to replace Yu's polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed

thicknesses because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation as I explained in Section VI.G.

156. To the extent Yu does not expressly disclose a **refractory metal nitride capping layer** having a thickness greater than that of a **bottommost layer**, Usui does. As Usui recognizes, “by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention.” Usui, 3:29-37. This benefit of limiting the bottommost metal layer of an electrode stack was well-known by August 2009, as I explained in Sections VI.F.1, VI.F.3.

157. Moreover, Yu expressly discloses that **diffusion barrier/protection layer 218 (bottommost layer** of plurality of metal layers) (Yu, [0029], Fig. 2E) may be “any suitable thickness.” *Id.*, [0029] and [0036].

158. A POSITA would have been motivated to apply known techniques of limiting the thickness of Usui **underlayer 13 (bottommost metal layer)** to **diffusion barrier/protection layer 218 (bottommost layer)** in Yu’s known device ready for improvement to yield predictable results and would have expected success because limiting the thickness of the bottommost metal layer had known benefits and was known in the art—combining prior art elements according to known

techniques to a known device ready for improvement to yield predictable results.

Sections VI.F.1, VI.F.3.

b. Claims 6 and 7 – A POSITA would have been motivated to form Yu’s metal layers of Al and Si, as taught by Usui.

159. Yu expressly discloses **metal layers 220, 222 (second metal layer)** comprise a doped-conducting metal oxide (DCO), where the DCO comprises “... ZnO doped with Al, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf, and/or combinations thereof...” (Yu, [0033]). While Al (claim 6) and Al further comprising Si (claim 7) are one of many possible combinations disclosed in Yu, the POSITA would have been motivated to provide such a combination as the benefits of such are well known, as I explained in Section VI.F.2. By August 2009, it was well-known that aluminum and aluminum alloys are common, low-cost, provide better adhesives to the metal stack, and improve thermal properties of the structure (Section VI.F.2).

160. To the extent that Yu does not expressly disclose **second metal layer** featuring Al and further comprising Si, Usui expressly teaches this combination of materials. A POSITA would have been motivated to implement Usui’s **layer 15 (second metal layer)** as a simple substitution in **metal layers 220, 222 (second metal layer)** of Yu’s device to obtain predictable results and would have expected success because using aluminum or aluminum silicon as a metal layer in an electrode stack had known benefits and was known in the art—combining prior art elements

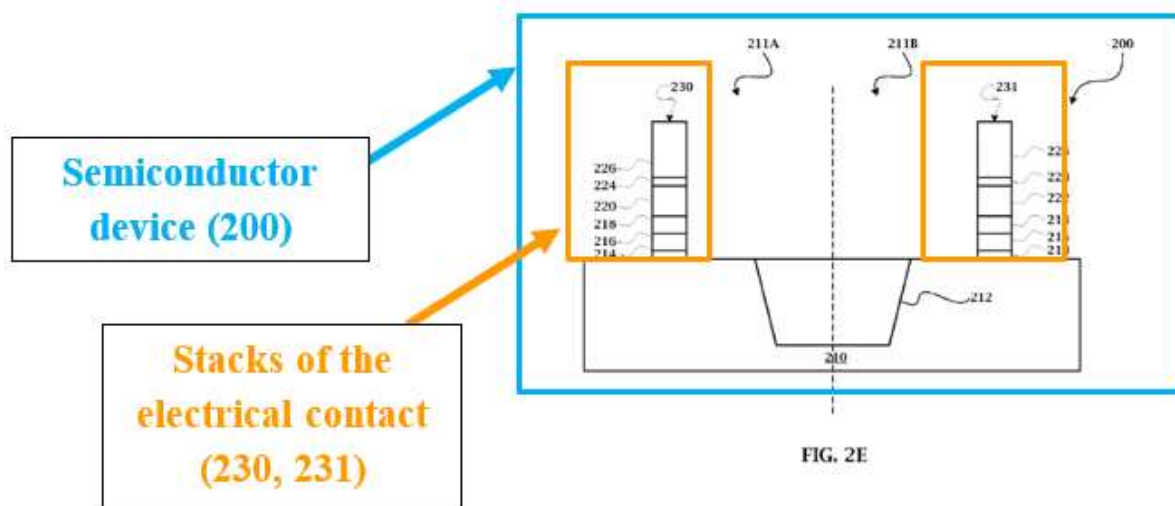
according to known techniques to a known device and simple substitution of one known element for another ready for improvement to yield predicable results.

Section VI.F.2.

3. Claim 1

- a. **[1pre]: An electrical contact for use on a semiconductor device, said electrical contact comprising:**

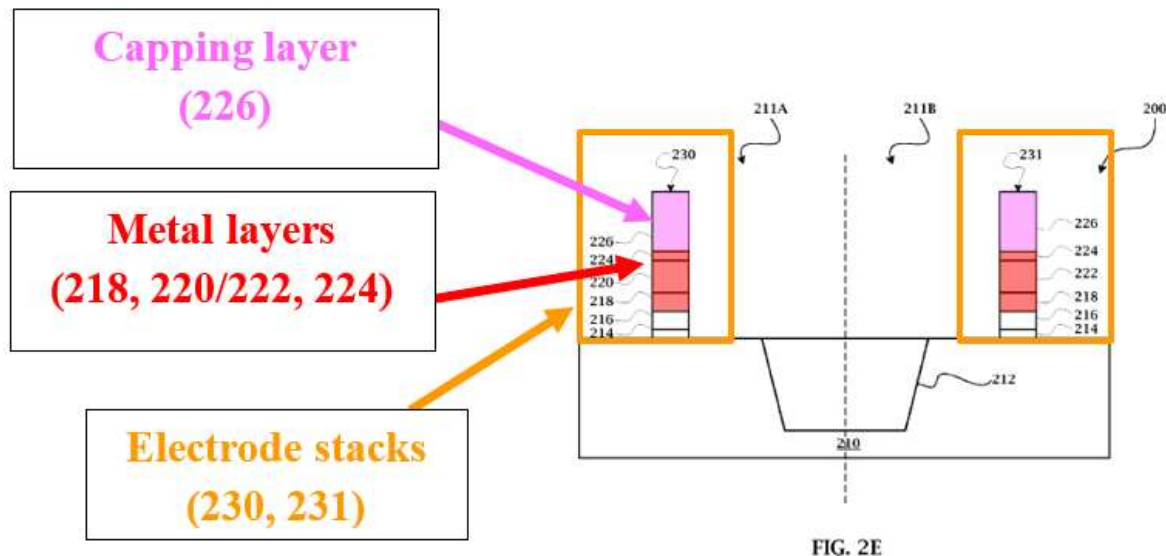
161. If limiting, Yu discloses [1pre] because it discloses “various contacts/vias and multilayer interconnect features (e.g., metal layers and interlayer dielectrics) may be formed on the substrate 210 and configured to connect the various features or structures of the semiconductor device 200,” including metal gate stacks 230 and 231 (stacks of the electrical contacts). Yu, [0040] and Fig. 2E.



Id., Fig. 2E (annotated).

- b. [1a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;

162. Yu discloses [1a] because it discloses **metal gate stacks 230, 231** (**electrode stacks**) each including a metal **diffusion barrier/protection layer 218** (**first metal layer**) (*id.*, [0029]), **metal layers 220, 222** (*id.*, [0035]) (**second metal layer**), a metal **diffusion barrier layer 224** (*id.*, [0035]) (**third metal layer**), and a **capping layer 226** (*id.*, [0036]) (**capping layer**) formed over the metal layers.



Id., Fig. 2E (annotated).

- c. [1b]: said capping layer consisting only of a refractory metal nitride,

163. Yu discloses [1b] because it discloses that **capping layer 226** (**capping layer**) (*id.*, [0036]) is **titanium nitride** or **tantalum nitride** (**refractory metal**

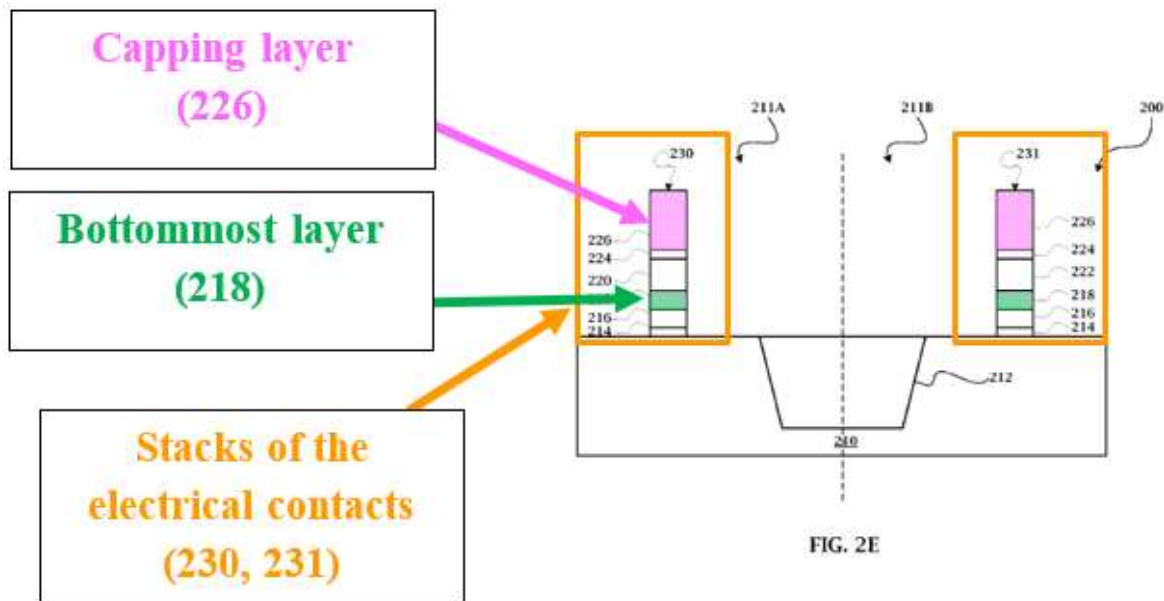
nitride) (*id.*). A POSITA would have known that titanium nitride and tantalum nitride are each a “refractory metal nitride.” *See* Sections VI.G, X.E.2, X.E.2.a.

164. As I explained in Section VI.G, refractory metals are a class of metals known for resistance to heat and wear. The most common definition of refractory metals are metals comprising a melting point above 2,204°C, such as niobium, molybdenum, tantalum, tungsten and rhenium. Section VI.G. A wider definition of refractory metals includes metals such as titanium. Section VI.G. Titanium nitride was a well-known and widely used refractory metal nitride which possesses a useful combination of useful mechanical and chemical properties such as hardness and corrosion and heat resistance. Section VI.G.

- d. **[1c]: said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.**

165. Yu at least suggests [1c] because it discloses **capping layer 226** is **titanium nitride** or **tantalum nitride (refractory metal nitride)** (*id.*, [0036]) forming a top of **metal gate stacks 230, 231 (electrode stacks of the electrical contact)** (*id.*, [0040], Fig. 2E) and having a thickness of about 200-1,000 Å, preferably about 600 Å (*id.*, [0036]), which is greater than the thickness of **diffusion barrier/protection layer 218 (bottommost layer of plurality of metal layers)** (*id.*, [0029], Fig. 2E), which is 20 Å (*id.*, [0029]). As I explained in Sections X.E.2 and X.E.2.a, a POSITA would have understood these thicknesses apply to Yu’s capping

and bottommost layer regardless of whether Yu's capping layer is comprised of polysilicon or titanium nitride or tantalum nitride.

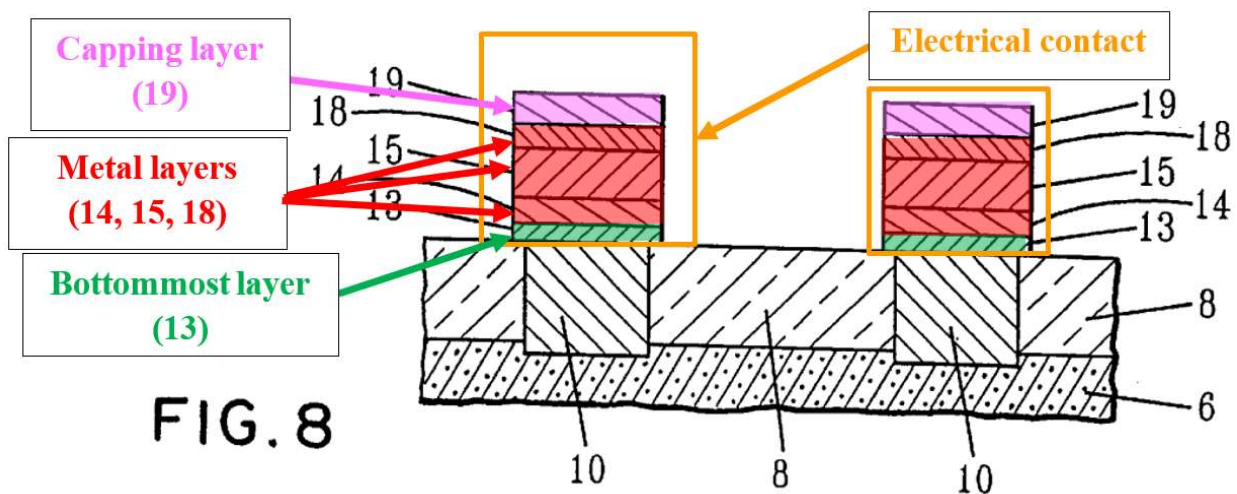


Id., Fig. 2E (annotated).

166. Layer 214 and 216 cannot be the bottommost layer of the “plurality of **metal layers**” because they are dielectric layers not “metal layers.” Layer 214 is an interfacial dielectric layer and layer 216 is a high-k dielectric layer. *Id.*, [0039]. Dielectric layers are insulating (Section VI.E) whereas metal layers are conductive (i.e., current flows in metals) (Ex-1011, 50). Therefore, interfacial dielectric layer 214 and high-k dielectric layer 216 cannot be the bottommost layer of the plurality of **metal** layers.

167. To the extent Yu does not expressly disclose that its capping layer is a refractory metal nitride, the use of a refractory metal nitride would have been

obvious over Yu and Usui. Usui expressly discloses a capping layer comprising only a refractory metal nitride thicker than a bottommost layer, as was known in the art (see Sections X.A.1, X.A.2.d, X.E.2, X.E.2.a). Usui expressly discloses that its **capping layer 19** is **titanium nitride (refractory metal nitride)** (Usui, 5:54-59) forming a top of the **metallization structure (electrical contact)** (*id.*, Abstract, 3:2-8, Figs. 1 and 8) and having a thickness of about 150-800 Å, more typically about 200-500 Å (*id.*, 4:5-8), which is greater than the thickness of **underlayer 13** (**bottommost layer** of plurality of metal layers) (*id.*, 5:38, 52, Figs. 1 and 8), which is 90-110 Å (*id.*, 3:29-33).



Id., Fig. 8 (annotated).

168. A POSITA would have been motivated to and had a reasonable expectation of success to implement Yu's **capping layer 226** as a refractory metal nitride with a greater thickness than its **bottommost layer 218**, as expressly taught by Usui to carefully control the structure and texture of the subsequently to applied

metallic layers—a benefit recognized by Usui—as I explained in Sections X.E.2, X.E.2.a; Usui, 3:29-37.

4. Claim 2 – The electrical contact of claim 1, wherein said capping layer comprises titanium nitride (TiN).

169. Yu at least suggests claim 2 because it discloses **capping layer 226** (**capping layer**) (*id.*, [0036]) comprises **titanium nitride** (*id.*). Yu’s device includes **capping layer 226** (**capping layer**) comprising polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, **titanium nitride**, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. Yu, [0036].

170. To the extent Yu does not expressly disclose that its capping layer comprised of titanium nitride is of a thickness greater than the thickness of its bottommost layer, Usui similarly discloses a capping layer comprised of titanium nitride at a thickness greater than a bottommost layer, as explained for [1c] and claim 2, Ground 1. (Sections X.A.2.c, X.A.2.d, X.A.3, X.E.2, X.E.2.a). A POSITA would have been motivated to use titanium nitride as **capping layer 226**, as Yu discloses, in Yu’s device at a thickness greater than that of Yu’s bottommost layer, as suggested by Yu and disclosed by Usui, because, as Usui recognizes, “by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. *See* Sections X.E.2, X.E.2.a. This is essential

in achieving the necessary properties of the structure of the present invention.” Usui, 3:29-37. This benefit of limiting the bottommost metal layer of an electrode stack was well-known by August 2009, as I explained in Sections VI.F.1 and VI.F.3. And capping layers made of titanium nitride were well-known by August 2009 and constituted a simple design choice depending on the application of the device—as I explained in Sections X.E.2, X.E.2.a, and VI.G.

5. Claim 3 – The electrical contact of claim 1, wherein said capping layer comprises tantalum nitride (TaN).

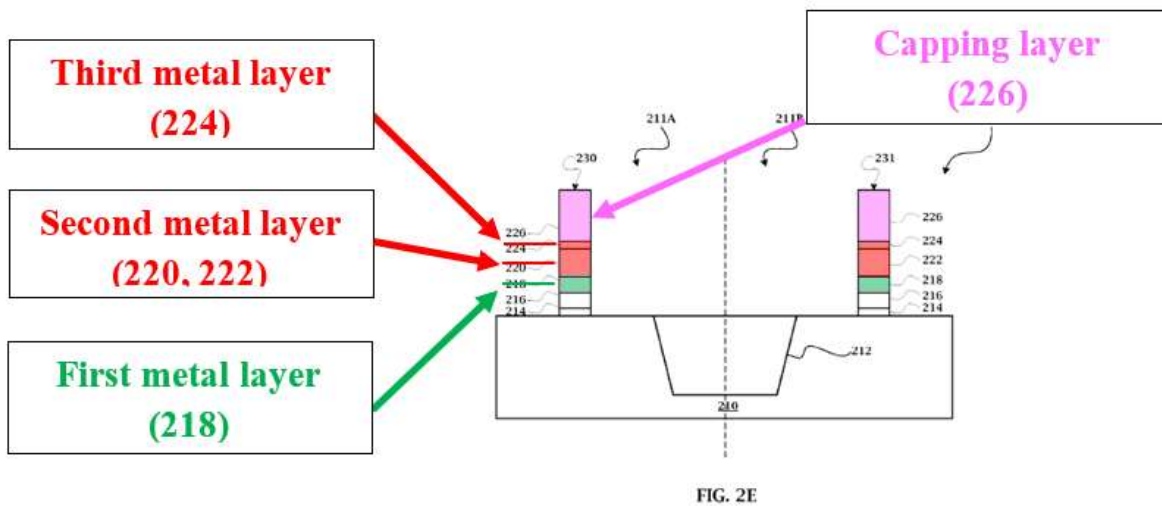
171. Yu at least suggests claim 3 because it discloses **capping layer 226** (**capping layer**) (*id.*, [0036]) comprising **tantalum nitride** (*id.*). Yu’s device includes **capping layer 226** (**capping layer**) comprising polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, **tantalum nitride**, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. Yu, [0036].

172. To the extent Yu does not expressly disclose that its capping layer comprised of tantalum nitride is of a thickness greater than the thickness of its bottommost layer, this would have been obvious in view of Usui, which discloses a capping layer of nitride materials at a thickness greater than a bottommost layer, as explained for [1c]. Section X.E.3.d. A POSITA would have been motivated to use tantalum nitride as **capping layer 226** in Yu’s device, in Yu’s device at a thickness

greater than that of Yu's bottommost layer, as suggested by Yu and disclosed by Usui, because, as Usui recognizes, "by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention." Usui, 3:29-37. This benefit of limiting the bottommost metal layer of an electrode stack was well-known by August 2009, as I explained Sections VI.F.1 and VI.F.3. And capping layers made of tantalum nitride were well-known by August 2009 and constituted a simple design choice depending on the application of the device—as I explained in Sections VI.G, X.E.2, and X.E.2.a.

6. Claim 4 – The electrical contact of claim 1, wherein said plurality of metal layers includes respective first, second, and third metal layers, wherein said second metal layer is formed between said first metal layer and said third metal layer, and said capping layer is formed on said third metal layer.

173. Yu discloses claim 4 because it discloses **metal layers 220, 222** (**second metal layer**) (Yu, [0035]) being formed between **diffusion barrier/protection layer 218** (**first metal layer**) (*id.*, [0029]) and **diffusion barrier layer 224** (**third metal layer**) (*id.*, [0035]), and **capping layer 226** (**capping layer**) (*id.*, [0036]) being formed on **diffusion barrier layer 224** (**third metal layer**) (*id.*, [0035]).



Id., Fig. 2E (annotated).

7. **Claim 5 – The electrical contact of claim 4, wherein said first metal layer and said third metal layer of said electrode stack comprise titanium (Ti).**

174. Yu discloses claim 5 because it discloses **diffusion barrier/protection layer 218 (first metal layer)** being **titanium** (Yu, [0029]) and **diffusion barrier layer 224 (third metal layer)** being **titanium** (*id.*, [0035]). Yu's device includes **diffusion barrier/protection layer 218 (first metal layer)** and **diffusion barrier layer 224 (third metal layer)** comprising **titanium**, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. Yu, [0029], [0035].

8. Claim 6 – The electrical contact of claim 4, wherein said second metal layer of said electrode stack comprises aluminum (Al).

175. Yu at least suggests claim 6 because Yu discloses **metal layers 220, 222 (second metal layer)** comprise a doped-conducting metal oxide (DCO), where the DCO comprises “... ZnO doped with Al, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf, and/or combinations thereof...” (Yu, [0033]). While **aluminum** is one of many possible doping materials for **metal layers 220, 222 (second metal layer)** disclosed in Yu, a POSITA would have understood the well-known benefits of using aluminum in metal layers in an electrode stack, as I explained in Section VI.F.2.

176. To the extent Yu does not expressly disclose that its second metal layer comprises aluminum, Usui discloses an aluminum second metal layer, and it would have been obvious to use aluminum as the second metal layer in Yu’s devices (as I explained in Sections X.E.2 and X.E.2.b). Usui explains that **layer 15 (second metal layer)** comprises **aluminum** or an aluminum alloy. Usui, 3:38-43, Figs. 1 and 8. A POSITA would have been motivated to similarly implement Yu’s second metal layer as comprising aluminum, as taught by Usui, because Usui explains that its aluminum or aluminum alloy layer, **layer 15 (second metal layer)**, is a highly textured layer with improved electromigration performance. *Id.*, 3:49-56.

177. Moreover, as I explained in Section VI.F.2, by August 2009, it was well-known that aluminum is common, low-cost, provides better adhesives to the metal

stack, and improves thermal properties of the structure. Therefore, a POSITA would have been motivated to use aluminum as **layer 15 (second metal layer)** as a simple substitution in **metal layers 220, 222 (second metal layer)** of Yu's device to obtain predictable results and would have expected success because using aluminum as a metal layer in an electrode stack had known benefits and was known in the art. *See* Sections VI.F.2 and X.E.2.b.

9. Claim 7 – The electrical contact of claim 6, wherein said second metal layer of said electrode stack further comprises silicon (Si).

178. Yu at least suggests claim 7 because Yu discloses **metal layers 220, 222 (second metal layer)** comprise a doped-conducting metal oxide (DCO), where the DCO comprises "... ZnO doped with Al, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf, and/or combinations thereof..." (Yu, [0033]). While **aluminum** further comprising **silicon** is one of many possible material combinations for **metal layers 220, 222 (second metal layer)** disclosed in Yu, would have understood the well-known benefits of using aluminum and silicon in metal layers in an electrode stack, as I explained in Section VI.F.2.

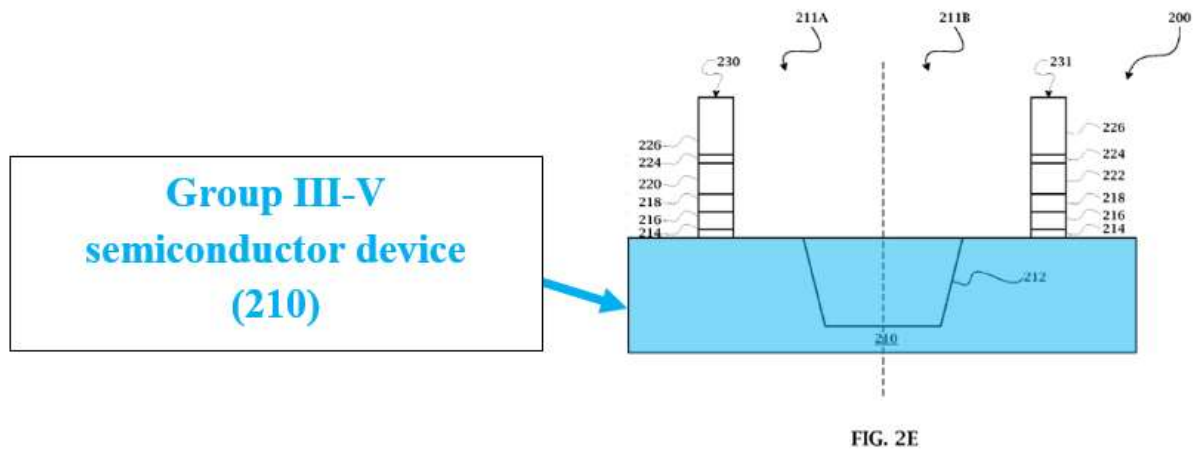
179. To the extent Yu does not expressly disclose that its second metal layer comprises aluminum and silicon, Usui discloses an aluminum silicon second metal layer, and it would have been obvious to use aluminum silicon as the second metal layer in Yu's devices (as I explained in Sections X.E.2 and X.E.2.b). Usui explains

that **layer 15 (second metal layer)** comprises **aluminum silicon**. Usui, 3:38-43, Figs. 1 and 8. Specifically, Usui discloses “[t]ypical aluminum alloys include alloying metal such as copper, magnesium, silicon, lanthanides such as vanadium and yttrium; and palladium” (*id.*). A POSITA would have been motivated to similarly implement Yu’s second metal layer as comprising aluminum and silicon, as taught by Usui, because Usui explains that its aluminum or aluminum alloy layer, **layer 15 (second metal layer)**, is a highly textured layer with improved electromigration performance. *Id.*, 3:49-56.

180. Moreover, a POSITA would have been motivated to use aluminum silicon as **layer 15 (second metal layer)** as a simple substitution in **metal layers 220, 222 (second metal layer)** of Yu’s device to obtain predictable results and would have expected success because using aluminum silicon as a metal layer in an electrode stack had known benefits and was known in the art. Sections VI.F.2, X.E.2, X.E.2.b. For example, it was well-known that aluminum silicon is common, low-cost, provides better adhesives to the metal stack, and improves thermal properties of the structure. Section VI.F.2.

10. Claim 8 – The electrical contact of claim 1, wherein said electrical contact is configured for implementation on a group III-V semiconductor device.

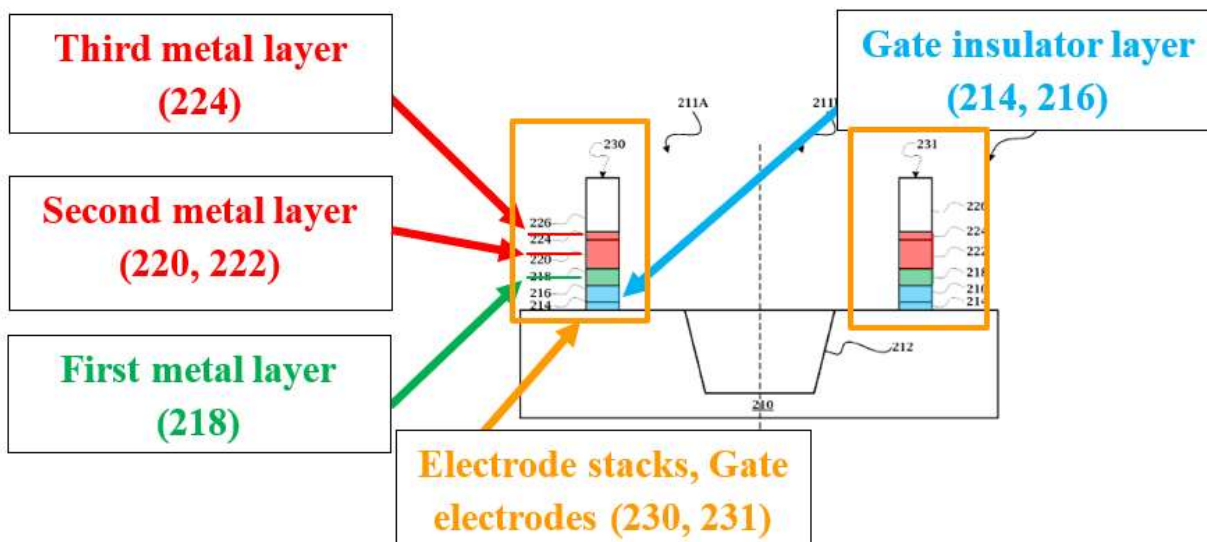
181. Yu discloses claim 8 because it discloses “the semiconductor substrate 210 comprises silicon, germanium, a **group III-V** material.” Yu, [0023].



Id., Fig. 2E (annotated).

11. **Claim 12 – The electrical contact of claim 8, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.**

182. Yu discloses claim 12 because it discloses the **interfacial dielectric layer 214** and the **high-k dielectric layer 216 (gate insulator layer)** (Yu, [0039]) underlying a metal **diffusion barrier/protection layer 218 (first metal layer)** (*id.*, [0029]) of **metal gate stacks 230, 231 (electrode stack)** to provide insulated **metal gate stacks 230, 231 (gate electrode)** for the group III-V semiconductor device (*id.*, [0023]). Dielectric materials are insulating materials commonly provided under gate structures—as I explained in Section VI.E.



Id., Fig. 2E (annotated).

12. Independent Claim 13

- a. [13pre]: An electrical contact for use on a group III-V semiconductor device, said electrical contact comprising:

183. [13pre] is identical to [1pre] and claim 8. [13pre] is obvious as explained for [1pre] and claim 8.

- b. [13a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;

184. [13a] is identical to [1a]. [13a] is obvious as explained for [1a].

- c. [13b]: said capping layer consisting only of a metal selected from the group consisting of titanium nitride (TiN) and tantalum nitride (TaN),

185. [13b] is identical to claims 2 and 3. [13b] is obvious as explained for claims 2 and 3.

- d. [13c]: said metal forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.**

186. [13c] is identical to [1c]. [13c] is obvious as explained for [1c].

- 13. Claim 17 – The electrical contact of claim 13, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.**

187. Claim 17 is identical to claim 12, but depends from claim 13. Claim 17 is obvious as explained for claim 12.

F. Ground 6: Yu in View of Usui and Adesida Renders Obvious Claims 9, 11, 14, and 16

1. Overview of the Combination and Motivations to Combine

188. Yu and Usui do not expressly disclose that their group III-V devices are HEMTs or a gate electrode making a Schottky electrical contact with a group III-V device.

189. Consistent with the '562 patent, Adesida discloses a gate electrode making Schottky contact with a group III-V device and power electrodes (source and drain electrodes) making ohmic contact with the group III-V device. Adesida, [0031]. Adesida discloses a semiconductor device with various contacts and metallization (Adesida, [0031]-[0032]) and forming a thermally stable gate metal (Adesida, [0030]). Adesida discloses “a field-effect device, comprising: a layered semiconductor structure that includes a channel layer and at least one layer over the

channel layer; spaced apart source and drain contacts disposed over said at least one layer and communicating with the channel layer; and an iridium **gate**, between the source and drain contacts, **forming a Schottky barrier contact on said at least one layer.**” Adesida, [0016]. Adesida further states that its device is a “**high electron mobility transistor (HEMT)**, which ... is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT),” where the HEMT device comprises an undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer formed beneath the gate. Adesida, [0031], Fig. 5. $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ is a well-known group III-V material. *See* Section VI.A.

a. Claims 9 and 14 – A POSITA would have been motivated to implement Yu’s device as a HEMT, as taught by Adesida.

190. Yu does not expressly disclose a semiconductor device comprising a high electron mobility transistor (HEMT), but Adesida does, and by August 2009, it was well-known that HEMTs are used for high power and/or high frequency applications. Section VI.B. As I explained in Section VI.B, HEMTs were the most widely used heterostructure field effect transistors. It was well-known that the combination of relatively high carrier concentration and relatively high carrier mobility gives the HEMT a relatively large transconductance and provide a performance advantage over metal-semiconductor field effect transistors (MESFETS) for high-frequency applications. Section VI.B.

191. Yu describes the need of providing a semiconductor device with an improved work function. Yu, Abstract. A work function is defined as the amount of energy required to eject electrons from a surface. A POSITA would have been motivated to implement Yu's device as a HEMT, as taught by Adesida, because HEMTs were well-known at the time for providing high carrier mobility and therefore improved work function characteristics, as desired by Yu. Furthermore, it was well-known at the time that modifying the Yu device to comprise a HEMT constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications)— combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *See* Section VI.B.

b. Claims 11 and 16 – A POSITA would have been motivated to implement Yu's electrical contact as a gate electrode making a Schottky contact, as taught by Adesida.

192. Yu does not expressly teach an electrical contact implemented as a gate electrode making a Schottky contact, but Adesida does, and as I explained in Section VI.C, by August 2009, it was well-known that Schottky contacts were of critical importance to device functionality, performance, and long-term reliability. It was well-known that Schottky contacts serve as gate contacts in group III-V devices, have a fast response for many applications due to their unipolar carrier transport, and

have excellent rectifying properties, which make them suitable for high frequency applications. Sections VI.C, VI.D.

193. Yu describes the need of providing a semiconductor device with an improved work function. Yu, Abstract. A work function is defined as the amount of energy required to eject electrons from a surface. A POSITA would have been motivated to implement Yu's device as a gate electrode making a Schottky contact, as taught by Adesida, because Schottky contacts were well-known at the time for providing a fast response for many applications due to their unipolar carrier transport. Furthermore, modifying the Yu device to include a Schottky contact constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications)— combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *See* Sections VI.B, VI.C.

2. Claim 9 – The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).

194. Yu in view of Usui and Adesida renders obvious claim 9 because Adesida discloses a HEMT, and it would have been obvious to implement Yu-Usui's group III-V semiconductor devices as HEMTs (as I explained in Sections VI.A, VI.B, X.F.1, X.F.1.a).

195. Adesida explains that its device is a “high electron mobility transistor **(HEMT)**, which ... is a field-effect **HEMT** formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT).” Adesida, [0031].

3. Claim 11 – The electrical contact of claim 8, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

196. Yu in view of Usui and Adesida renders obvious claim 11 because Adesida discloses a group III-V device with a gate electrode making a Schottky contact with the group III-V device, and it would have been obvious to implement Yu or Yu-Usui’s group III-V semiconductor devices with gate electrodes making Schottky contacts (as I explained in Sections VI.A, VI.B, VI.C, VI.D, X.F.1, X.F.1.b).

197. Adesida discloses “a field-effect device, comprising: a layered semiconductor structure that includes a channel layer and at least one layer over the channel layer; spaced apart source and drain contacts disposed over said at least one layer and communicating with the channel layer; and an iridium gate, between the source and drain contacts, **forming a Schottky barrier contact on said at least one layer.**” Adesida, [0016].

198. For example, Adesida discloses a HEMT formed on an **indium phosphide substrate or gallium arsenide substrate 105**, on which is an **In_{0.52}Al_{0.48}As barrier layer 150 (group III-V semiconductor device)**. InAlAs is a well-known

group III-V material—as I discussed in Section VI.A. Adesida, Fig. 5, [0031]. **Gate 190 (gate electrode)** is formed as a **Schottky barrier contact (Schottky contact)** on the **In_{0.52}Al_{0.48}As barrier layer 150 (group III-V semiconductor device)**. Adesida, Fig. 5 and [0031].

199. Consistent with the '562 patent, Adesida discloses **gate 190 (gate electrode)** formed as a **Schottky barrier contact (Schottky contact)** on the group III-V device and **source 170** and **drain 180 (power electrodes)** making ohmic contact with the group III-V device. Adesida, Fig. 5 and [0031].

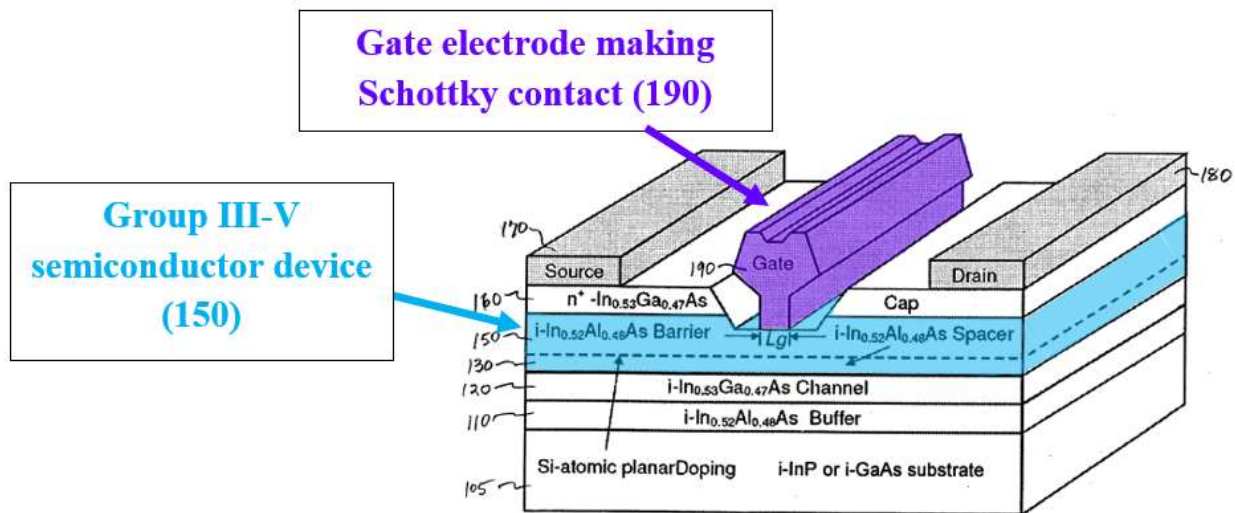


Figure 5

Adesida, Fig. 5 (annotated).

- 4. Claim 14 – The electrical contact of claim 13, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).**

200. Claim 14 is identical to claim 9, but depends from claim 13. Claim 14 is obvious as explained for claim 9.

- 5. Claim 16 – The electrical contact of claim 13, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.**

201. Claim 16 is identical to claim 11, but depends from claim 13. Claim 16 is obvious as explained for claim 11.

G. Ground 7: Yu in view of Usui and Sugimoto Render Obvious Claims 10 and 15

1. Overview of the Combination and Motivation to Combine

202. Yu and Usui do not expressly disclose that their group III-V devices have a power electrode making an ohmic electrical contact.

203. Like Yu, Sugimoto discloses a group III-V semiconductor device (Sugimoto, 9:7-9) with an AlGaN top layer. Sugimoto, Figs. 1, 3, 5, 7. AlGaN is a well-known group III-V material. Section VI.A. Sugimoto further discloses the III-V semiconductor device is a HEMT. Sugimoto, 1:22-67.

204. The '562 patent defines “[s]ource electrode 136 and drain electrode 138 are power electrodes ohmically coupled to the heterojunction formed by GaN layer 112 and AlGaN layer 114.” '562 patent, 3:19-21. Consistent with the '562 patent, Sugimoto discloses a gate electrode making Schottky contact with a group III-V

device and power electrodes (source and drain electrodes) making ohmic contact with the group III-V device. Sugimoto, 9:39-51. Sugimoto discloses that its “**drain electrode 42** and the **source electrode 46** make **ohmic contact** with the top surface of the **AlGaIn layer 34**.” Sugimoto, 9:39-51.

205. As I explained in Section VI.C, by August 2009, it was well-known that ohmic contacts are of critical importance with respect to device functionality, performance, and long-term reliability. It was well-known that ohmic contacts serve as source and drain contacts in group III-V devices and allow current to flow into and out of a semiconductor material without distortion of the signal. Section VI.C. It was well-known that the most critical component of an ohmic contact is its low specific contact resistance, which minimizes the power consumption of the contact and the internal heating of the contact, thereby prolonging device operation with predictable performance. *See* Section VI.C.

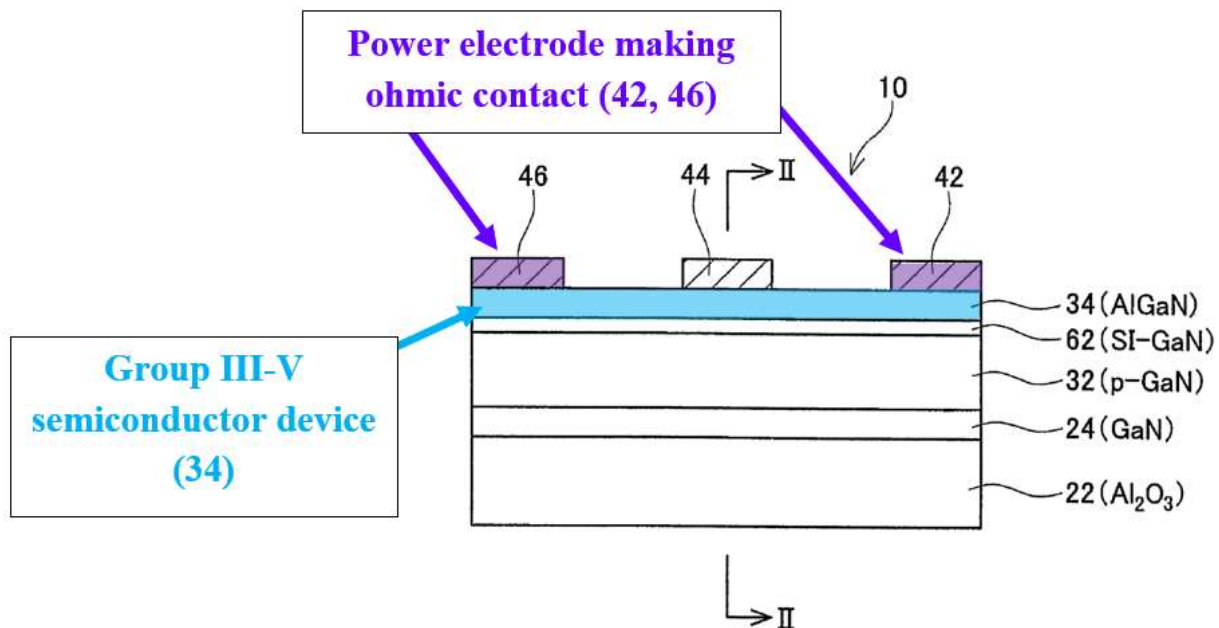
206. Yu disclosed the importance of an improved work function and thermal stability. Yu, Abstract. A POSITA would have been motivated to implement the devices of Yu and Yu-Usui with a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide reduced internal heating of the contact and improved current flow (i.e., improved work function values). Furthermore, such a combination is the result of combining prior art

elements according to known techniques to a known device ready for improvement to yield predictable results. *See* Sections VI.B, VI.C; Adesida, [0031], Fig. 5.

2. Claim 10 – The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.

207. Yu in view of Usui and Sugimoto render obvious claim 10 because Sugimoto discloses a device with a power electrode making an ohmic contact, and it would have been obvious to implement Yu or Yu-Usui's group III-V semiconductor devices with power electrodes making ohmic contacts (as I explained in Sections VI.C, X.G.1).

208. Sugimoto discloses that its “**drain electrode 42 (power electrode)** and the **source electrode 46 (power electrode)** make **ohmic contact** with the top surface of the **AlGaIn layer 34 (group III-V semiconductor device)**.” Sugimoto, 9:39-51.



Sugimoto, Fig. 1 (annotated).

3. **Claim 15 – The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.**

209. Claim 15 is identical to claim 10, but depends from claim 13. Claim 15 is obvious as explained for claim 10.

XI. CONCLUSION

210. For the reasons set forth in Sections VI-X, it is my opinion that one skilled in the art would have found claims 1-17 of the '562 patent to be anticipated or obvious.

211. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to

cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

212. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date:11/15/2024

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Yuji Zhao', written above a horizontal line.

Yuji Zhao, PhD