

Technology and Performance of InAlN/AlN/GaN HEMTs With Gate Insulation and Current Collapse Suppression Using ZrO₂ or HfO₂

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Abstract—We present the technology and performance of InAlN/AlN/GaN MOS HEMTs with gate insulation and surface passivation using ZrO₂ or HfO₂. About 10-nm-thick high- k dielectrics were deposited by MOCVD before the ohmic contact processing. Plasma pretreatment allowed the reduction of the temperature of the ohmic contact annealing at 600 °C. The insulation and passivation of 2- μ m gate-length MOS HEMTs lead to a gate leakage current reduction by four orders of magnitude and a 2.5 $\times$ increase of the pulsed drain-current if compared with a Schottky barrier (SB) HEMT. A dc characterization shows 110 mS mm⁻¹ transconductance and 0.9 A mm⁻¹ drain-currents that represent improvements in comparison to the similar SB HEMT and that is explained by a mobility-dependent carrier depletion effect.

Index Terms—GaN, HEMTs, InAlN/GaN.

I. INTRODUCTION

InAlN/GaN-BASED HEMTs can be superior in comparison to more conventional AlGaN/GaN HEMTs primarily because of the substantially higher polarization-induced 2-D electron gas (EG) density n_0 in the device channel and because of a possibility to grow strain-free InAlN/GaN heterostructure [1]–[4]. On the other hand, it has been observed that, similarly to a AlGaN/GaN system, a Schottky barrier (SB) height on InAlN remains to be only about 1 eV or less, and the gate leakage at high drain biases might even prevent the complete HEMT pinch-off [2]. Similarly, it was suggested that the filling of surface states in the gate–drain area of the InAlN/GaN HEMT by electrons emitted from the reverse-biased gate depletes 2-D EG and lead to the transients known as the current collapse effect [5]. The collapse of the HEMT characteristics was manifested as the drop in the linear part of the

pulsed output characteristics if compared with the dc characteristics while a coincidence of those two characteristics was obtained by current saturation. The phenomenon of the current collapse was described analytically by dynamical changes of the drain parasitic resistance [5]. On the other hand, if the pulsed characteristics showed voltage-dependent difference to the dc curves (pulsed values being higher) at the current saturation, the phenomenon was explained by a reduced self-heating effect in the pulsed operation. This was analytically described using the temperature-dependent source resistance [5], [6]. Alternatively, the carrier trapping may also happen in the barrier layer, GaN buffer layer [7], or in the dielectric layer [8], if the device gate is insulated, and that may cause instabilities of the HEMT threshold voltage V_T .

Gate leakage current is an important factor that limits the performance and reliability of conventional high-power AlGaN/GaN HEMTs [9]. Thus, a thin dielectric oxide layer is often inserted between the gate metal and the AlGaN barrier layer leading to the approach of the MOS HEMT [9]–[14]. The dielectric was also used to cover the bare surface between the HEMT contacts [10], [13]. Consequently, the AlGaN surface traps were passivated and the current collapse reduction was obtained simultaneously with the gate insulation [10], [13]. On the other hand, by applying the gate insulation, the gate to channel separation increases, and a shift of V_T due to a gate-to-source capacitance C_{GS} decrease can be observed [9]–[13], [14]. Furthermore, if we adopt $g_m = v_{sat}C_{GS}/L_G$ [11] where g_m is the device intrinsic transconductance, v_{sat} the electron saturation velocity, and L_G the gate length, g_m is supposed to decrease proportionally to C_{GS} . The use of high-permittivity (high- k) insulating materials such as already reported for AlGaN/GaN (Al₂O₃ ($k_{ox} \sim 9$) [12], HfO₂ ($k_{ox} \sim 20$ –25) [10] or ZrO₂ ($k_{ox} \sim 23$ –30) [13]–[15]) has eliminated these drawbacks. Despite high k , ZrO₂ and HfO₂ materials provide band gaps higher than the bandgap of lattice-matched InAlN (4.7 eV for In_{0.17}Al_{0.83}N [16] versus 5.7 eV for HfO₂ and 7.8 eV for ZrO₂ [15]). Moreover, in recent reports on high- k -based AlGaN/GaN MOS HEMTs, it was reported that an extrinsic transconductance g_{me} [11], [12] and/or a cutoff frequency f_T [10], [11] can even be increased with the gate insulation. The reason for that was not satisfactorily explained yet.

In our paper, we present InAlN/AlN/GaN MOS HEMTs with ZrO₂ or HfO₂ dielectrics for the gate insulation and surface passivation. We show that the gate leakage current is substantially reduced, and the drain-current collapse is

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suppressed if compared with InAlN/AlN/GaN SB HEMT. Moreover, we observed an increase in g_{me} and that is explained by considering various mechanisms of the drain-current saturation in the GaN-based HEMTs.

II. EXPERIMENTAL

In_{0.18}Al_{0.82}N/AlN/GaN lattice-matched heterostructure system was grown by metal-organic chemical vapor deposition (MOCVD) on sapphire substrate [4]. A 1.1-nm-thick AlN spacer was applied between InAlN (12.6-nm-thick) and GaN (1.5 μm) to increase the 2-D EG mobility μ [4]. The n_0 and μ values at room temperature using the Hall method were determined to be $2.7 \times 10^{13} \text{ cm}^{-2}$ and $1060 \text{ cm}^2(\text{V}\cdot\text{s})^{-1}$, respectively, giving a sheet resistance of $237 \Omega/\square$. Ar-based reactive-ion etching (RIE) was used for the mesa insulation. Subsequently, the wafer was divided into three parts. Ti/Al/Ni/Au ohmic contacts were deposited directly on the masked InAlN of the first sample, which was reserved for a processing of a reference SB HEMT. On the two rest of the parts of the wafer, ~ 10 -nm-thick HfO₂ or ZrO₂ layer (d_{ox}) was deposited by MOCVD prior to the ohmic contact processing, and this sequence facilitated a thorough chemical etching of samples (1:1 buffered HF, HCl, NH₃:H₂O₂) before the oxide deposition. Moreover, there was no risk of the MOCVD chamber contamination by contact species. Hafnium or zirconium-trifluoroacetylacetonate (Hf/Zr(tfacac)₄) have been selected as a precursor substance for the oxide deposition, the process temperature was 450°C [17]. The film thickness was measured *ex situ* by ellipsometry on dummy Si sample that was placed close to an InAlN/AlN/GaN sample during the deposition. The ellipsometry model, which is used to calculate the film thickness, is well established for dielectric/Si systems, and consequently, we used Si and not InAlN/AlN/GaN sample for the thickness monitoring. After the oxide deposition, SF₆-based RIE was used to open the windows for the ohmic contacts.

Simultaneously with the HEMT processing, we checked the thermal stability of ZrO₂ and HfO₂. We compared the MOS I - V characteristics where the oxide was subjected to the rapid thermal annealing (RTA) with the samples where RTA was not performed (not shown). The duration of all RTA cycles was 2 min in N₂ atmosphere. We found that oxides are intact at 600°C and start to degrade at 700°C .

In MOS HEMTs, the ohmic contact RTA was applied after the dielectric deposition, and thus, a modification of the "conventional" recipe for ohmic contacts, which requires RTA at 800°C for 2 min [2], was needed. We have tested plasma pretreatment (SiCl₄-based RIE for 15 s) before the ohmic contact metals were evaporated to decrease the temperature of annealing, similar to that already reported for AlGaN/GaN [18].

After finalizing the optimized ohmic contact level, Ni/Au is used as a gate metal for both the SB and MOS HEMTs. Gates have the geometry of $2 \mu\text{m} \times 100 \mu\text{m}$ and the source-to-drain distance was $8 \mu\text{m}$. Gate leakage characteristics and HEMT parameters were measured using conventional dc characterization methods [2]. Channel sheet resistance R_{sheet} of the processed HEMTs (with and without passivation) is measured using trans-

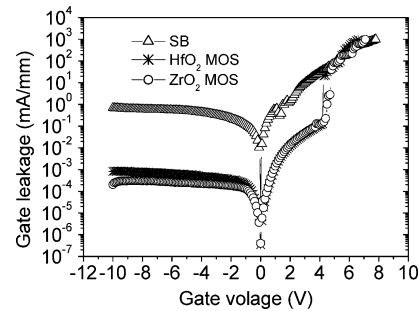


Fig. 1. Gate I - V characteristics of ZrO₂- and HfO₂-based InAlN/AlN/GaN MOS HEMTs compared with SB HEMTs.

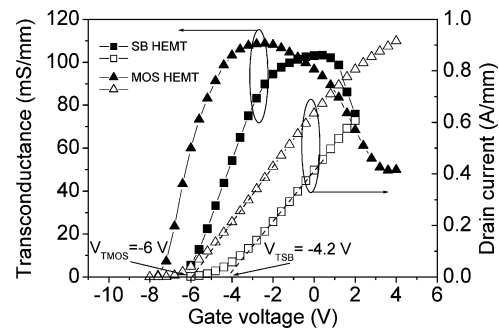


Fig. 2. Transfer and transconductance characteristics of ZrO₂-based InAlN/AlN/GaN MOS HEMT compared with SB HEMTs at $V_{DS} = 8 \text{ V}$. V_{TSB} and V_{TMS} are the threshold voltages of the SB and MOS HEMT, respectively.

mission line model (TLM) test structures [19]. For the current collapse investigation, we pulse the HEMT gate contact from the "OFF-state" level of -10 V to a chosen V_{GS} value while the constant voltage V_{DS} is applied on the drain. The pulse was 100 ns and the HEMT transient output characteristics were compared with the dc curves.

III. RESULTS AND DISCUSSIONS

For RTA at 600°C without the RIE pretreatment the ohmic contact resistance R_C was shown to have an unacceptable value of $12 \Omega\cdot\text{mm}$. On the other hand, SiCl₄-based plasma pretreatment led to the R_C value as low as $1 \Omega\cdot\text{mm}$. Consequently, plasma pretreatment and RTA at $600^\circ\text{C}/2 \text{ min}$ was used for the MOS HEMT processing. R_C of SB HEMTs (no pretreatment/RTA at 800°C) was less than $0.3 \Omega\cdot\text{mm}$.

Fig. 1 shows the gate I - V characteristics of InAlN/AlN/GaN HEMTs. Strong reduction in the leakage currents of the MOS gates, by about four orders of magnitude in comparison to SB HEMT, is observed. At $V_{GS} = -10 \text{ V}$, the MOS gate leakage current was below $1 \mu\text{A mm}^{-1}$. The leakage of the ZrO₂-based gates was lower than the leakage of HfO₂-based gates, however, the difference seems to be not significant enough to exclude inhomogeneity across the cleaved InAlN/AlN/GaN sample. From the MOS I - V breakdown at $\sim 4 \text{ V}$, we roughly estimate the oxides electrical strength to be $\sim 4 \text{ MV cm}^{-1}$. Thicker d_{ox} may result in less leakage and higher breakdown voltages in the forward bias, however, one also needs to consider deterioration of g_{me} with increased d_{ox} .

In Fig. 2, we show g_{me} and transfer characteristics of the SB InAlN/AlN/GaN HEMT in comparison to ZrO_2 -based MOS HEMT. The maximal g_{me} is increased after the gate insulation from about 105 mS mm^{-1} for SB HEMT to about 110 mS mm^{-1} for MOS HEMT even though the V_T is shifted from -4.2 to -6 V . The shift ΔV_T was due to the dielectric insertion as $\Delta V_T = V_{PO} \times d_{ox} \times k_{InAlN} / (d_{InAlN} \times k_{ox})$ [14] where V_{PO} denotes the SB HEMT pinch-off voltage. The formula neglects eventual pinning of the Fermi level at the interface states and the change of the flat band voltage. For simplicity, the influence of the AlN spacer is neglected too. The V_T for the ZrO_2 -based MOS HEMT corresponds to $k_{ox} \sim 20$ – 22 justifying the aforementioned formula.

Fig. 2 also shows an increase in the maximal drain-current I_{DS} from about 0.65 to 0.9 A mm^{-1} . A similar trend was observed for the HfO_2 -based MOS HEMT (not shown) where the V_T is shifted to -7.3 V , I_{DS} is increased to 0.9 A mm^{-1} , and g_{me} is only slightly decreased to 95 mS mm^{-1} if compared with the SB HEMT. I_{DS} reaches high values despite the sapphire-substrate-related self-heating effect and the large device geometry ($2 \mu\text{m}$ gate length, $8 \mu\text{m}$ S–D distance). This can be explained by high n_0 in InAlN/AlN/GaN system.

We note that experimentally observed larger V_T shift for HfO_2 -based MOS HEMT cannot be expected if we assume similar k_{ox} for ZrO_2 and HfO_2 [10]. Only, eventual pinning of the Fermi level at InAlN/ HfO_2 interface states may change V_T [14], however, as shown later, both studied high- k materials are found to be very effective in InAlN surface passivation, and hence, Fermi level pinning is not likely. We assume that possible differences in the deposition rates of ZrO_2 or HfO_2 on Si and InAlN surfaces and/or spatial inhomogeneity in the deposition chamber, which resulted in thicker HfO_2 , can be the reason for different V_T .

Fig. 3(a) shows dc and pulsed output characteristics of the SB HEMT that can be compared with the characteristics of the ZrO_2 -based MOS HEMT shown in Fig. 3(b). Fig. 3(a) (SB HEMT) confirms a clear lag of the transient I_{DS} behind the dc values (especially for $V_{GS} = 0 \text{ V}$) in the linear part of the characteristics and increase of the knee voltage as anticipated for the current collapse phenomena [5]. The intersection of the pulsed and dc SB HEMT characteristics at $V_{DS} = 15 \text{ V}$ indicates appearance of the self-heating (in the dc mode) as V_{DS} increases and characteristic approaches saturation [5], [6]. For $V_{GS} = 0 \text{ V}$, the transients are shown at two time instances (100 and 200 ns). Higher values obtained for 200 ns indicate gradual surface de-trapping in the SB HEMT.

On the other hand, linear part of the output characteristics of InAlN/AlN/GaN MOS HEMT [see Fig. 3(b)] shows coincidence of the pulsed and the dc current characteristics suggesting a stable InAlN surface potential. For low V_{DS} in the linear part of the output characteristics, we can assume a minimal self-heating effect even in the dc mode of operation, and thus, the coincidence with the pulsed characteristics suggests an effective surface passivation. Higher values of the MOS HEMT pulsed I_{DS} in comparison to dc ones in the saturation part of I_{DS} and a clear dependence of the current difference on V_{DS} comply with expectations valid for the device with strong self-heating

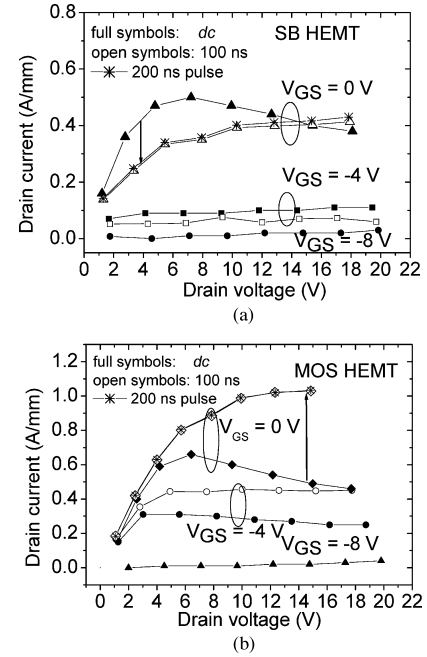


Fig. 3. DC and pulsed output characteristics. (a) InAlN/AlN/GaN SB HEMT. (b) ZrO_2 -based InAlN/AlN/GaN MOS HEMT. Gate contact was pulsed from -10 V to set V_{GS} . V_{DS} was sequentially increased, duration of the pulse was 100 ns. Difference between the pulsed and dc characteristics are marked by an arrow. For $V_{GS} = 0 \text{ V}$, characteristics are also shown at 200 ns.

effect [5], [6]. Transition from 100 to 200 ns showed no effect on the characteristics of the MOS HEMT as the time constant of the thermal transients in GaN-based HEMTs on sapphire is expected to be substantially longer ($\sim 140 \mu\text{s}$) [20].

In the dc mode of operation, we observed a current enhancement only by about 20% in MOS HEMT if compared with the SB HEMT (see Fig. 3). However, the pulsed I_{DS} at $V_{GS} = 0 \text{ V}$ is up to a $2.5\times$ higher for MOS HEMT if compared with the SB HEMT, and that clearly demonstrate the superiority of the HEMT with the surface passivation by dielectrics. We note that almost similar performance enhancement was observed for both ZrO_2 and HfO_2 -based MOS HEMTs.

To evaluate an eventual carrier trapping either in the GaN buffer or in the high- k material itself, we checked the stability of V_T . We extracted V_T from dc transfer characteristics (see Fig. 2) and from the pulsed transfer characteristics (pulses from “OFF-state” condition for 100 ns, not shown). No time-domain V_T shift could be obtained, indicating a low level of additional trapping. The low density of trapped electrons and low surface potential at InAlN/dielectric interface was further validated by measuring R_{sheet} of the SB and MOS HEMTs (in the steady state). For SB HEMT we observed an increased value of $R_{sheet} \sim 500 \Omega/\square$ (compared with $237 \Omega/\square$ measured by Hall method just after the InAlN/AlN/GaN growth) probably because of a gradual oxidation and/or contamination of InAlN surface before and during the HEMT processing. On the other hand, extremely low $R_{sheet} \sim 110$ (135) $\Omega/\square$ has been observed if the InAlN surface is thoroughly etched and subsequently passivated by ZrO_2 (HfO_2) (Section II), indicating a low surface potential and/or high carrier mobility in the channel.

We discuss the origin of g_{me} enhancement (or only a slight decrease for HfO_2) in $\text{InAlN}/\text{AlN}/\text{GaN}$ MOS HEMTs if compared with SB HEMT, which contradicts general expectations [11], [12]. It was reported elsewhere [21] that intrinsic μ value of $\text{AlGaIn}/\text{GaIn}$ 2-D EG (i.e., below the gate) may drastically deteriorate if the gate metal makes intimate contact with the semiconductor ($1400 \text{ cm}^2(\text{V}\cdot\text{s})^{-1}$ for the bare surface versus $\mu \cong 600 \text{ cm}^2(\text{V}\cdot\text{s})^{-1}$ for SB on 10-nm-thick AlGaIn). However, if the gate insulation is used, μ value was not affected [21]. The effect was explained by different electrostatic potential induced by the SB gate and by MOS contact system. It was assumed that a built-in potential of the SB contact applied to the thin barrier layer changes the shape of the quantum well and increases scattering in the channel [21]. We may assume a similar behavior also in $\text{InAlN}/\text{AlN}/\text{GaIn}$, however, for $V_{PO} \gg 3 L_g \times v_{sat}/\mu$, a complete velocity saturation model of HEMTs is anticipated and g_m is not dependent on μ [22]. Only if the aforementioned inequality is not fulfilled, then V_{DS} that is needed for the onset of the velocity saturation is large enough to cause a substantial EG depletion along the low-field mobility part of the channel. Consequently, only a reduced number of carriers reach velocity saturation, which is transformed into g_m dependence on μ [22]. Thus, for typical GaN-based HEMTs with $\mu \approx 1000 \text{ cm}^2(\text{V}\cdot\text{s})^{-1}$, one may need $L_g \ll 1 \mu\text{m}$ in order to reach the maximal (i.e., μ -independent) g_m , details will be given elsewhere [23]. Otherwise, g_{me} of the MOS GaN HEMT can be similar or even higher than those of the SB HEMT due to the intrinsic μ improvement, and this may explain the presented observations. We note that the condition for the complete velocity saturation model is more difficult to reach and the increase of g_{me} is more easily obtained for low V_{PO} , i.e., if high- k and/or thinner insulators are used. This explains the most pronounced g_{me} increase for ZrO_2 -based MOS HEMT.

Finally, we can conclude that our experimental research on ZrO_2 and HfO_2 -based $\text{InAlN}/\text{AlN}/\text{GaIn}$ MOS HEMTs indicate an effective reduction of the current collapse, no evidence of charge trapping in the dielectrics and no Fermi level pinning (at least for ZrO_2) at the dielectric/ InAlN interface. Consequently, the studied dielectrics indicate optimal interfaces for $\text{InAlN}/\text{AlN}/\text{GaIn}$ HEMTs. Microwave performances of various newly processed submicrometer $\text{InAlN}/\text{AlN}/\text{GaIn}$ MOS HEMTs will be presented in our next paper to support the present findings.

IV. CONCLUSION

We have presented the technology and performance of $\text{InAlN}/\text{AlN}/\text{GaIn}$ MOS HEMTs using ZrO_2 or HfO_2 as a gate insulation and surface passivation. The plasma pretreatment of ohmic contacts enable to use a reduced temperature for the annealing. The strong reduction of the gate current leakage has been observed after the gate insulation together with a clear suppression of the drain-current collapse effect. g_{me} of the HEMTs have been increased by passivation and that is explained by analysis of the HEMT current saturation mechanism dependence on mobility.

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