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Finer Copper Wires Make for Faster Integrated Circuits

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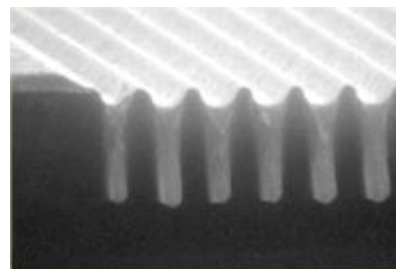
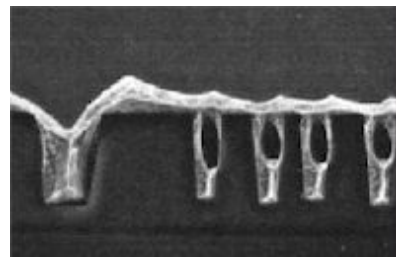
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BERKELEY, CA — Othon Monteiro of the Department of Energy's Lawrence Berkeley National Laboratory has devised a new way to inlay copper wires in the semiconductor wafers used to create integrated circuits. In the May/June 1999 issue of the *Journal of Vacuum Science and Technology B*, Monteiro discusses his method of "ion-assisted trench filling," which promises to open the way to ever more densely packed chips beyond the year 2000.

A National Technology Roadmap issued by the Semiconductor Industry Association predicts that new lithography methods will reduce today's smallest chip features, already as fine as 250 nanometers (billionths of a meter), to 180 nanometers in 1999, 100 nanometers by 2006, and even finer dimensions in the years beyond—making it possible to pack hundreds of millions more electronic devices on a chip.

Many of these microscopic devices must be interconnected by metal wires, which are made by filling tiny trenches in the surface of the semiconductor wafer. Multiple levels are connected by penetrating a layer to make contacts with layers above and below. The standard stuff of such wires has long been aluminum or aluminum alloys and, in interlayer connectors, tungsten.

"As device sizes get smaller, the electrical properties of aluminum will not meet the new requirements," says Monteiro, a materials scientist in the Plasma Applications Group of Berkeley Lab's Accelerator and Fusion Research Division. "We need lower resistivity and greater resistance to electromigration." Electromigration is the drift of metal atoms when the conductor carries



STANDARD METHODS OF INLAYING METALS IN ETCHED NANOSCALE TRENCHES MAY LEAVE VOIDS AND FRACTURES (ABOVE). ION-ASSISTED TRENCH FILLING CAN PRODUCE

high current densities, which can create voids. He adds, "We also need something that's compatible with lower dielectric-constant materials," which have been introduced by chip manufacturers to improve insulation and reduce circuit delays.

PERFECT METAL INLAYS (BELOW).

Copper is much more conductive than aluminum, allowing finer wires with lower resistive losses. Copper is also significantly less vulnerable to electromigration than aluminum and less likely to fracture under stress. Unfortunately, "copper is poisonous to silicon," Monteiro says. "It readily diffuses into silicon and causes deep-level defects."

Less than two years ago the first commercial copper-wired chips were announced by IBM and Motorola. To keep the copper from migrating into the dielectric and poisoning it, a diffusion barrier was used, which lined the trench walls between the copper and the substrate. Motorola used titanium nitride as a barrier. Other possible barrier materials include tantalum, tantalum alloys, and tantalum nitride.

IBM and Motorola produced their copper-wired chips by electroplating the copper over the diffusion barrier. Although Monteiro's ion-assisted technique can be used either in conjunction with electroplating or by itself, it has several advantages over electroplating. It can produce thinner, more uniform layers of metals in a variety of architectures. It can be used in narrower trenches with higher depth-to-width aspect ratios. It can fill trenches from the bottom up, automatically eliminating uneven deposition that can lead to voids in the metal lines—or it can produce conformal thin films that mirror the shape of the patterned wafer.

To employ the technique, a substrate wafer etched with trenches is placed under a plasma source. A pulsed-bias voltage is applied to the substrate and can be tuned to accelerate ions toward both the sides and bottom of the trench—in which case a layer builds up evenly—or preferentially to the bottom, filling the trench from the bottom up. The process is terminated when the precise desired thickness of the material has been applied.

Films consisting of multiple layers are readily deposited using different cathode materials—copper, tantalum, tantalum nitride, and a variety of other materials can be applied in this way. Copper metalization, for example, may begin by depositing a conformal film of tantalum 20 to 50 nanometers thick. Ions of copper are then deposited on top of the tantalum layer. The process can be halted when the new material has formed a thin conformal coating, or deposition can be continued until the trench is filled completely. Another possibility is to use the thin copper layer as a "seed layer" and fill the trench electrochemically.

To facilitate closer packing and multilevel connections, trenches are getting proportionally deeper as they get narrower. "Deep trenches etched into the dielectric must be filled completely, without voids or defects," Monteiro says. "With current technology, the deeper the trench, the more likely there will be defects."

At present, "dual-Damascene" methods are used to etch the trenches, fill them electrolytically, then mechanically polish away the excess metal using a chemically active slurry (the term is borrowed from the way the Arab swordsmiths of medieval Damascus inlaid their famous weapons). Etching and filling narrow structures with high aspect ratios will be especially difficult for dual-Damascene architectures.

Multilayer film methods will be essential, but a problem with common vapor-deposition techniques is that material builds up at the top of the trench and closes it off, leaving a void below. In ion-assisted deposition, however, the highly charged ions drive straight into the trench, dislodging excessive build-up before it accumulates.

"The challenge is to address narrower paths," Monteiro says. "Our goal is to get from 250 nanometers to 100 nanometers, at a 10-to-one aspect ratio. And I'm confident we can go even below that."

Monteiro, who has applied for a patent on ion-assisted trench filling, says that what amazes him about the semiconductor industry "is that they know where they want to be without knowing how they're going to get there, but somehow they always do." Monteiro's new technique is one of the latest technologies to come to the industry's rescue.

The Berkeley Lab is a U.S. Department of Energy national laboratory located in Berkeley, California. It conducts unclassified scientific research and is managed by the University of California. Visit our web site at <http://www.lbl.gov>.