

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
PETITIONER,

V.

INFINEON TECHNOLOGIES AUSTRIA AG,
PATENT OWNER.

IPR2025-00175
U.S. Patent 8,686,562

PETITION FOR *INTER PARTES* REVIEW

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LIST OF EXHIBITS

Exhibit	Description
Ex-1001	U.S. Patent No. 8,686,562 (“the ’562 patent”)
Ex-1002	Expert Declaration of Dr. Yuji Zhao (“Zhao”)
Ex-1003	Curriculum Vitae of Dr. Yuji Zhao
Ex-1004	U.S. Patent No. 5,943,601 to Usui et al. (“Usui”)
Ex-1005	U.S. Patent Publication No. 2010/0052066 to Yu et al. (“Yu”)
Ex-1006	U.S. Patent Publication No. 2008/0023726 to Adesida et al. (“Adesida”)
Ex-1007	U.S. Patent No. 7,777,252 to Sugimoto et al. (“Sugimoto”)
Ex-1008	Pearton et al., <i>Gallium Nitride Processing for Electronics, Sensors and Spintronics</i> , Springer, 10.1007/1-84628-359-0. (2006)
Ex-1009	Adachi, <i>Properties of Group-IV, III–V and II–VI Semiconductors</i> , John Wiley & Sons, Ltd, 10.1002/0470090340 (2005)
Ex-1010	U.S. Patent Publication No. 2007/0164321 to Sheppard et al. (“Sheppard”)
Ex-1011	Mishra et al., <i>Semiconductor Device Physics and Design</i> , Springer (2008)
Ex-1012	Wu et al., <i>Very-High Power Density AlGaIn/GaN HEMTs</i> , IEEE Transactions on Electronic Devices, Vol. 48, No. 3, March 2001
Ex-1013	Quay, <i>Gallium Nitride Electronics</i> , Springer, 10.1007/978-3-540-71892-5. (2008)
Ex-1014	Mishra et al., <i>AlGaIn/GaN HEMTs—An Overview of Device Operation and Applications</i> , Proceedings of the IEEE, Vol. 90, No. 6, June 2002

Exhibit	Description
Ex-1015	Neaman, <i>Semiconductor Physics and Devices</i> , 3 rd edition (2002)
Ex-1016	Voss, <i>Thermally Stable Ohmic and Schottky Contacts to GaN</i> , University of Florida, 2008
Ex-1017	Krämer, <i>Fabrication and characterization of metal-semiconductor contacts for application in Al_xGa_{1-x}N/GaN HEMTs</i> , (Oct. 31, 2000)
Ex-1018	Kuzmuk et al., <i>Technology and Performance of InAlN/AlN/GaN HEMTs With Gate Insulation and Current Collapse Suppression Using ZrO₂ or HfO₂</i> , IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 55, No. 3, Mar. 2008
Ex-1019	Wu et al., <i>Aluminum, magnesium, and gold contacts to contamination free n-GaN surfaces</i> , Journal of Applied Physics, Vol. 89, No. 1, Jan. 1, 2001
Ex-1020	Foresi et al., <i>Metal contacts to gallium nitride</i> , Appl. Phys. Lett., Vol. 62, No. 22, May. 31, 1993
Ex-1021	Kayali et al., <i>GaAs MMIC Reliability Assurance Guideline for Space Applications</i> , JPL Publication 96-25, Dec. 15, 1996
Ex-1022	U.S. Patent Publication No. 2009/0250816 to Chin et al. (“Chin”)
Ex-1023	U.S. Patent No. 7,335,590 to Suh et al. (“Suh”)
Ex-1024	U.S. Patent No. 6,607,976 to Chen et al. (“Chen”)
Ex-1025	Excerpts from Bauccio, Michael, <i>Refractory Metals</i> , ASM Metals Reference Book, ASM International, American Society for Metals, ISBN 978-0-87170-478-8, (1993)
Ex-1026	Preuss, <i>Finer Copper Wires Make for Faster Integrated Circuits</i> , Berkeley Lab, https://www2.lbl.gov/Science-Articles/Archive/integrated-circuits-copper.html , Apr. 5, 1999

Exhibit	Description
Ex-1027	Cockeram, <i>The Diffusion Bonding of Silicon Carbide and Boron Carbide Using Refractory Metals</i> , USDOE Contract No. DE-AC11-98PN38206, Nov. 22, 1999
Ex-1028	Kim, <i>Atomic Layer Deposition of Metal and Nitride Thin films: Current Research Efforts and Applications for Semiconductor Device Processing</i> , RC22737 (W0303-012), Mar. 5, 2003
Ex-1029	U.S. Patent No. 6,844,258 to Fair et al. (“Fair”)
Ex-1030	U.S. Patent No. 4,980,752 to Jones, Jr. (“Jones”)
Ex-1031	U.S. Patent No. 5,635,763 to Inoue et al. (“Inoue”)
Ex-1032	U.S. Patent No. 6,646,352 to Ohmi et al. (“Ohmi”)
Ex-1033	Order Staying and Conditionally Closing Case, Infineon Tech. Austria AG v. Innoscience (Suzhou) Tech. Company, Ltd., No. 4:24-cv-01553 (N.D. Ca. Aug. 30, 2024), ECF No. 56
Ex-1034	Excerpts from Prosecution History of the ’562 Patent
Ex-1035	Excerpts from Rooy, E.L., <i>Introduction to Aluminum and Aluminum Alloys</i> , Metals Handbook, 10 th Edition, Volume 2 Properties and Selection: Nonferrous Alloys and Special-Purpose Materials, ASM International, ISBN 978-0-87170-378-1, (October 1990)
Ex-1036	Pierson, Hugh O., <i>The Refractory Nitrides</i> , Handbook of Refractory Carbides and Nitrides, Properties, Characteristics, Processing and Applications, ISBN 978-0-8155-1392-6, (1996)

I. INTRODUCTION

Petitioner requests cancelation of claims 1-17 of the '562 patent, which alleges priority to 2009 and claims an electrical contact with a refractory metal nitride capped electrode stack.

Independent claims 1 and 13 require a capping layer formed over a plurality of metal layers, where the capping layer consists only of a refractory metal nitride and has a thickness greater than that of a bottommost layer of the metal layers. Dependent claims 2-12 and 14-17 recite well-known elements: (i) the capping layer consisting only of titanium nitride (TiN) or consisting only of tantalum nitride (TaN), (ii) the first and third metal layer of the electrode stack comprising titanium (Ti), (iii) the second metal layer of the electrode stack comprising aluminum (Al) or aluminum and silicon, (iv) implementing the electrical contact on a group III-V semiconductor device, (v) the group III-V semiconductor device comprising a high electron mobility transistor (HEMT), (vi) implementing the electrical contact as a power electrode (source or drain electrode) making ohmic contact with the group III-V semiconductor device, (vii) implementing the electrical contact as a gate electrode making Schottky contact with the group III-V semiconductor device, (viii) implementing the electrical contact with a gate insulator layer underlying the electrode stack to provide an insulated gate electrode, which were all conventional features by 2009.

II. RELIEF REQUESTED

Petitioner requests review under the following:

Exhibit	Prior Art
Ex-1004	Usui (filed on April 30, 1997, and issued on August 24, 1999) qualifies as prior art under pre-AIA 35 U.S.C. §§ 102 (a), (b), and (e).
Ex-1005	Yu (filed on April 15, 2009, and published on March 4, 2010) qualifies as prior art under pre-AIA 35 U.S.C. § 102(e).
Ex-1006	Adesida (filed on May 24, 2007, and published on January 31, 2008) qualifies as prior art under pre-AIA 35 U.S.C. §§ 102 (a), (b), and (e).
Ex-1007	Sugimoto (filed on January 17, 2007, and issued on August 17, 2010) qualifies as prior art under pre-AIA 35 U.S.C. § 102(e).

Grounds	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	Usui
2	3, 8, 12, 13 and 17	§ 103	Usui and Yu
3	9, 11, 14 and 16	§ 103	Usui, Yu, and Adesida
4	10 and 15	§ 103	Usui, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	Yu and Usui
6	9, 11, 14, and 16	§ 103	Yu, Usui, and Adesida
7	10 and 15	§ 103	Yu, Usui, and Sugimoto

III. STATEMENT OF FACTS

Pursuant to 37 C.F.R. § 42.22(c), Petitioner submits the following statement of facts. These facts are supported by Dr. Zhao's declaration that provides an overview of the state of the art and a background of the technology at issue. Zhao ¶¶48-73.

1. As of August 25, 2009, Group III-nitride semiconductor materials and devices were known. Zhao ¶¶48-50.
2. As of August 25, 2009, High Electron Mobility Transistors (HEMTs), also known as a modulation doped field effect transistor (MODFET), were known and used for high power and/or high frequency applications. Zhao ¶¶51-54.

3. As of August 25, 2009, ohmic contacts and Schottky contacts were known to be of critical importance with respect to device functionality, performance, and long-term reliability. Zhao ¶¶55-59.
4. As of August 25, 2009, Ohmic contacts were known to serve as drain and source contacts in group III-V HEMTs. Zhao ¶¶56-57.
5. As of August 25, 2009, Schottky contacts were known to serve as gate contacts in group III-V HEMTs. Zhao ¶¶58-59.
6. As of August 25, 2009, gate electrodes were known to modulate the conductivity of the channel in various devices, including group III-V HEMTs. Zhao ¶¶60-61.
7. As of August 25, 2009, an insulated gate electrode was a known structure in semiconductor devices and microelectronics. Zhao ¶62.
8. As of August 25, 2009, dielectric materials were known insulating materials commonly provided under gate electrodes to address gate leakage current in HEMTs. Zhao ¶62.
9. As of August 25, 2009, a variety of metals, including titanium, aluminum, and aluminum alloys, were known to be used in contact structures. Zhao ¶¶63-69.
10. As of August 25, 2009, thin bottommost metal layers of a metallization structure were known to improve adhesion and provide a

barrier for metal diffusion into the underlying semiconductor layer.

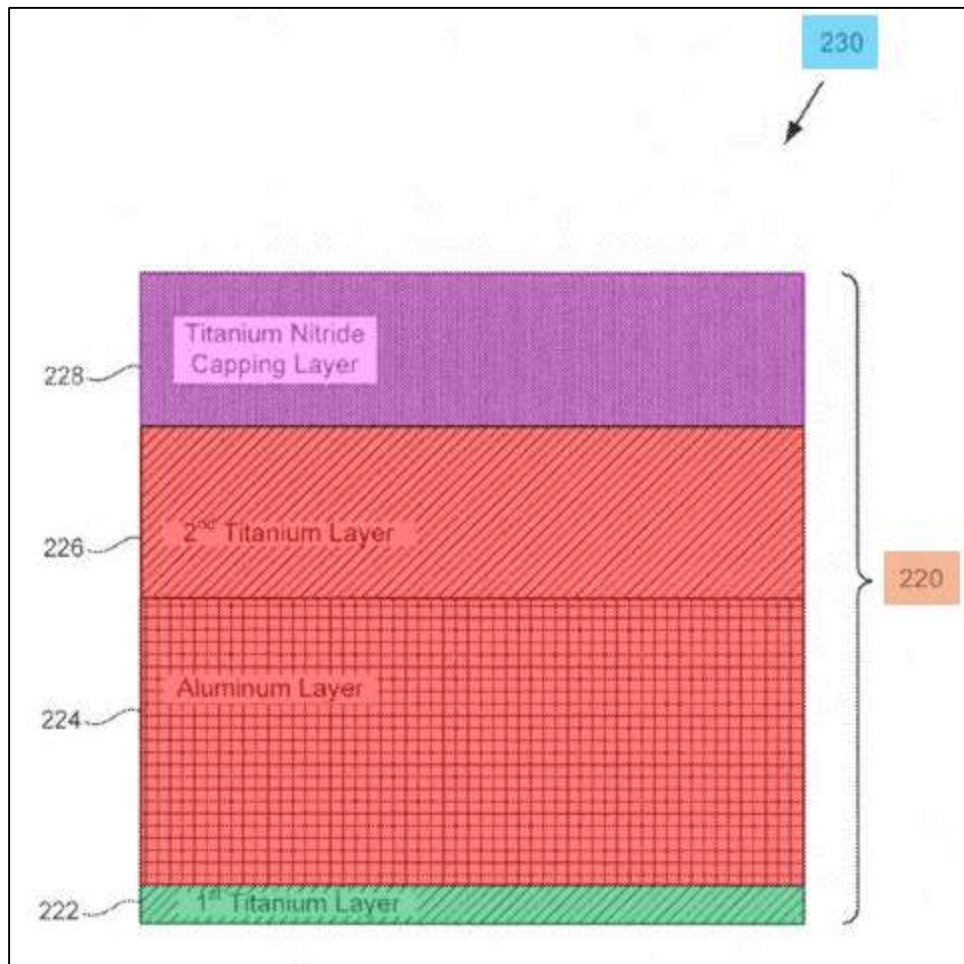
Zhao ¶¶67, 70.

11. As of August 25, 2009, refractory metal nitrides were a class of metals known for resistance to heat and wear. Zhao ¶¶71-73.

IV. '562 PATENT

The '562 patent describes an electrical contact capping layer alternative to gold capping layers, which may be costly and may diffuse through the electrode stack, making it difficult to integrate III-nitride power semiconductor devices with silicon devices. '562 patent, 1:44-55. Its electrical contact applies to group III-V semiconductor devices, including high electron mobility transistors (HEMT). '562 patent, 2:43-55.

Figure 2 shows **electrical contact 230**, corresponding to any of a source electrode, drain electrode or gate electrode. '562 patent, 3:39-42. **Electrical contact 230** comprises **electrode stack 220**, which includes **capping layer 228** consisting only of a refractory metal nitride, such as titanium nitride, over metal layers such as **titanium layer 226**, **aluminum layer 224**, and **titanium layer 222**. *Id.*, 3:39-45. **Capping layer 228** has a thickness greater than that of the bottommost metal layer, **titanium layer 222**. '562 patent, Fig. 2, 4:25-27, 5:15-17; Zhao ¶¶74-75.



'562 patent, Fig. 2 (annotated).

V. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design. Additional education could substitute for professional experience and vice versa. Zhao, ¶¶80-82.

VI. CLAIM CONSTRUCTION

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). For the purposes of this IPR, the plain meaning of each term can be applied. Zhao ¶¶76-79.

VII. CLAIMS 1-17 ARE INVALID

The '562 patent lists characteristics and variations of electrical contacts without disclosing that these features were novel or inventive. These features had various trade-offs that were well-known by the time of the alleged invention (August 25, 2009). The only feature the '562 patent describes as purportedly novel is the refractory metal nitride capping layer, which is disclosed by both Usui and Yu.

The '562 patent discloses a capping layer having a thickness greater than a thickness of the bottommost metal layer. '562 patent, 4:25-27, 5:13-17, claims 1 and 13. The '562 also discloses the capping layer consisting only of a refractory metal nitride and that the refractory metal nitride may be TiN or TaN. '562 patent, 5:17-22, claims 1 and 13. As Dr. Zhao explains, these features and their advantages were well-known by August 25, 2009. Zhao ¶¶63-67, 70-73.

The '562 patent discloses an electrode stack with a first titanium layer, an aluminum layer, and a second titanium layer ('562 patent, 3:42-45), where the aluminum layer may include silicon and where other metals (e.g., nickel) may be

used instead of titanium in the electrode stack ('562 patent, 3:65-4:3). '562 patent, claims 5-7. The '562 patent discloses a group III-V semiconductor device, which may comprise a high electron mobility transistor (HEMT). '562 patent, 2:53-55, claims 8-9 and 14. As Dr. Zhao explains, these features and their advantages were well-known by August 25, 2009. Zhao ¶¶48-54, 63-69.

The '562 patent further discloses the electrical contact being implemented as a power electrode (i.e., source and drain electrodes) making ohmic contact with the group III-V semiconductor device. '562 patent, 3:19-23, claims 10 and 15.

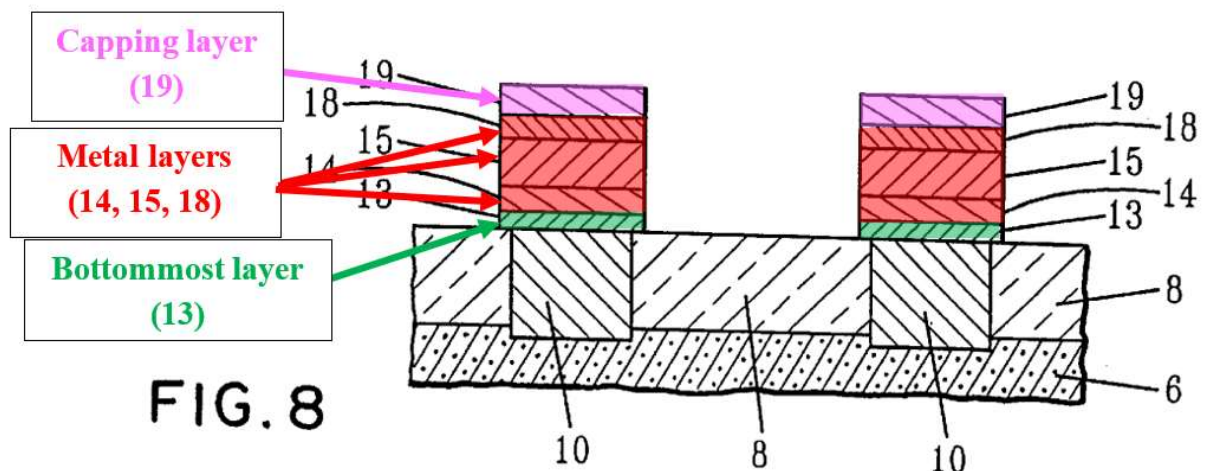
The '562 patent also discloses the electrical contact being implemented as a gate electrode making Schottky contact with the group III-V semiconductor device or with a gate insulator layer underlying the first metal layer of the electrode stack. '562 patent, 3:19-23, 31-35, claims 11-12 and 16-17. These features and their advantages were well-known by August 25, 2009. Zhao ¶¶55-62.

A. Ground 1: Usui Anticipates Claims 1, 2, and 4-7

1. Usui

Usui relates to metallization structures for forming electrical connections with enhanced electromigration. Usui, Abstract, 5:11-16. Usui discloses using metal layers that allow subsequently applied metallic layers to be carefully controlled, which is essential to achieve the necessary properties of the structure. Usui, 3:29-37. Zhao ¶84.

Usui's metallization structure has **capping layer 19** (**capping layer**) that is thicker than **underlayer 13** (**bottommost metal layer**) (Usui, 3:29-33, 4:5-8) and **layer 15** (**second metal layer**) comprising **aluminum** or an **aluminum alloy**, with typical aluminum alloys like **silicon**. *Id.*, 3:39-43.



Usui, Fig. 8 (annotated); Zhao ¶85.

As Dr. Zhao explains, by August 25, 2009, it was well-known that metallization structures limit the thickness of the bottommost metal layer to carefully control subsequently applied metallic layers (Usui, 3:29-37; Zhao ¶¶66-67, 70, 86) and that aluminum and aluminum alloys are common, low-cost, provide better adhesives to the metal stack, and improve thermal properties of the structure (Zhao ¶¶68-69, 86). Additionally, any of the materials disclosed by Usui are viable options for **layer 15** (**second metal layer**) according to Usui, which allows for design choice and creativity of a POSITA in assembling various devices

using different materials depending on the application. A POSITA would have been motivated to use aluminum or aluminum silicon as **layer 15 (second metal layer)** in Usui's device, and done so with a reasonable expectation of success, because metallization structures with layers made of aluminum or aluminum silicon were well known by August 2009 and constituted a simple design choice depending on the application of the device. Zhao ¶¶68-69, 86.

Usui is analogous to the '562 patent because it is in the same field of endeavor, forming electrical contacts for semiconductor devices (Usui, Abstract; '562, Abstract), and addresses the same problem of providing enhanced or simplified fabrication as the '562 patent (Usui, 4:1-3; '562, 1:25-29, 1:56-62). Zhao ¶87.

2. Claim 1

a. [1pre]: An electrical contact for use on a semiconductor device, said electrical contact comprising:

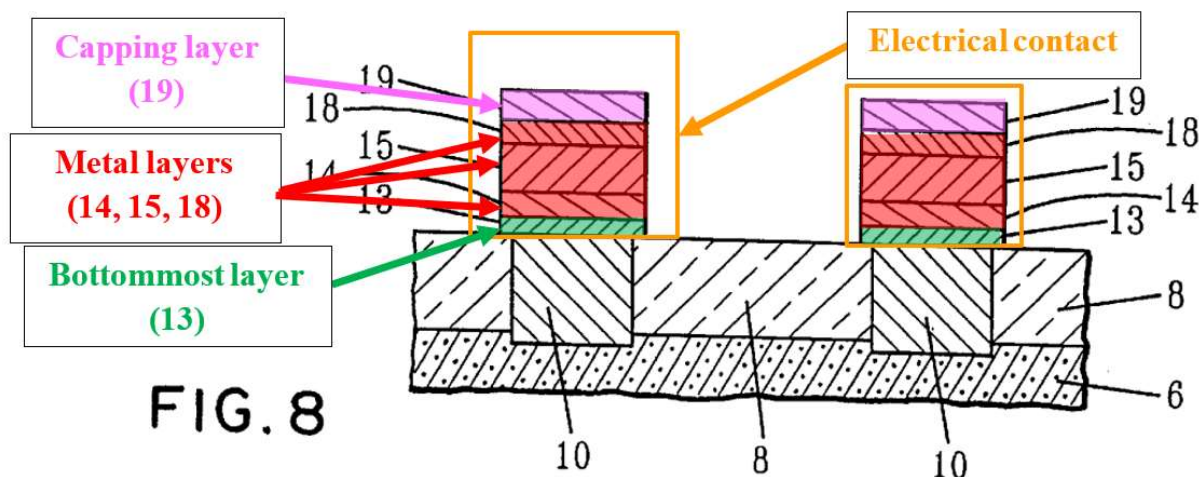
If limiting, Usui discloses [1pre] because Usui is directed to a metallization structure, featuring group IVA metals (e.g., transition metals including titanium, zirconium, hafnium, and rutherfordium) (Usui, Abstract) for forming electrical connections (contacts) (*id.*, Abstract). Zhao ¶88.

- b. [1a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;

Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8; Zhao ¶89.

Usui discloses a plurality of metal layers. Usui's **layer 18** comprises titanium (**metal layer**) (Usui, 4:4-5, Figs. 1 and 8), **layer 15** comprises aluminum or aluminum alloy (**metal layer**) (*id.*, 3:38-41, Figs. 1 and 8), **layer 14** comprises titanium nitride (**metal layer**) (*id.* 3:58-60, Figs. 1 and 8) and **underlayer 13** comprises titanium (**bottommost metal layer**) (collectively, a plurality of metal layers). *Id.*, 5:38, 52, Figs. 1 and 8; Zhao ¶90.

Usui discloses a capping layer. Usui's **capping layer 19** is **titanium nitride** and is formed above the plurality of **metal layers** (Usui, 5:54-59) forming a top of the **metallization structure (electrical contact)**. *Id.*, Abstract, 3:2-8, Figs. 1 and 8.



Usui, Fig. 8 (annotated); Zhao ¶91.

- c. **[1b]: said capping layer consisting only of a refractory metal nitride,**

Usui discloses [1b] because its **capping layer 19** is formed only of **titanium nitride (refractory metal nitride)** (Usui, 5:54-59). A POSITA would have known that titanium nitride is a “refractory metal nitride.” Zhao ¶¶71-73, 92.

As Dr. Zhao explains, refractory metals are a class of metals known for resistance to heat and wear. Zhao ¶71 (citing Ex-1025, 120). The most common definition of refractory metals are metals comprising a melting point above 2,204°C, such as niobium, molybdenum, tantalum, tungsten and rhenium. *Id.* A wider definition of refractory metals includes metals such as titanium. *Id.* (citing Ex-1027, 1). As Dr. Zhao explains, titanium nitride was a well-known and widely used refractory metal nitride which possesses a useful combination of useful mechanical and chemical properties such as hardness and heat resistance. Zhao ¶¶72, 93 (citing Ex-1026, 2; Ex-1036, 156-157, 160).

- d. **[1c]: said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.**

Usui discloses [1c] because its **capping layer 19** is **titanium nitride (refractory metal nitride)** (Usui, 5:54-59) and forms a top of the **metallization structure (electrical contact)**. *Id.*, Abstract, 3:2-8, Figs. 1 and 8. Usui’s underlayer

13 is the bottommost layer of its metal layers. Usui's **underlayer 13** comprises a thickness between about 90-110 Å and is described as being critical to the layered metal structure because by limiting the thickness of the underlayer, the structure and texture of subsequently applied metallic layers may be carefully controlled.

Id., 3:29-35. Usui's **capping layer** has a thickness of about 150-800 Å, more typically about 200-500 Å (*id.*, 4:5-8), which is greater than the thickness of **underlayer 13** (**bottommost layer** of plurality of metal layers). *Id.*, 5:38, 52, Figs. 1 and 8; Zhao ¶94.

3. Claim 2 – The electrical contact of claim 1, wherein said capping layer comprises titanium nitride (TiN).

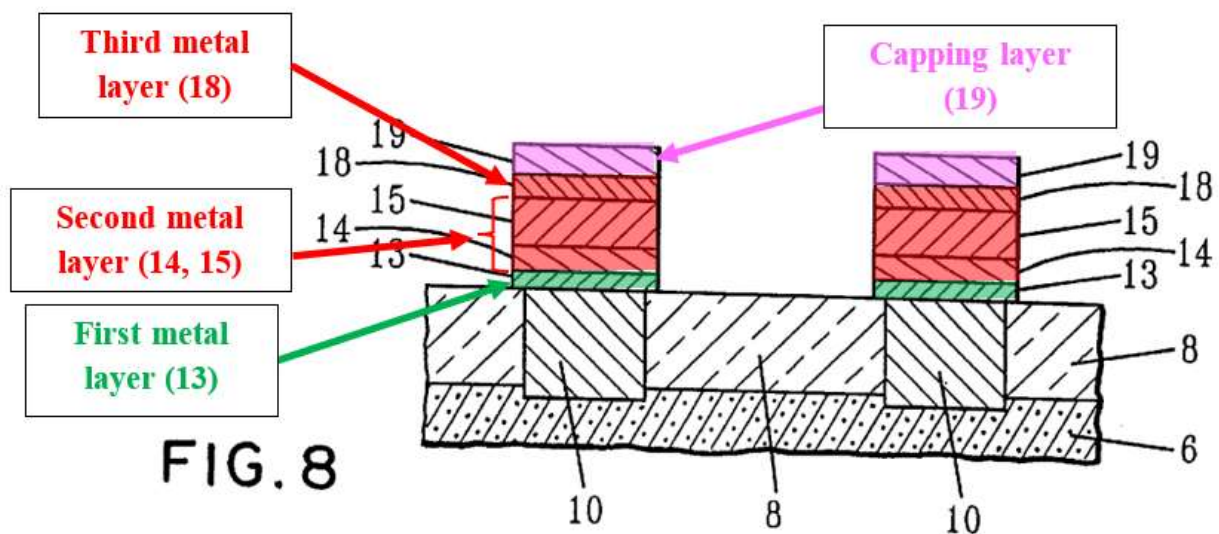
Usui discloses claim 2 because its **capping layer 19** is **titanium nitride**.
Usui, 5:54-59. Zhao ¶95.

4. Claim 4 – The electrical contact of claim 1, wherein said plurality of metal layers includes respective first, second, and third metal layers, wherein said second metal layer is formed between said first metal layer and said third metal layer, and said capping layer is formed on said third metal layer.

Usui discloses claim 4 because it has three metal layers (first, second, and third) with the second formed between the first and third layer, and with a capping layer on top of the third layer. Zhao ¶96.

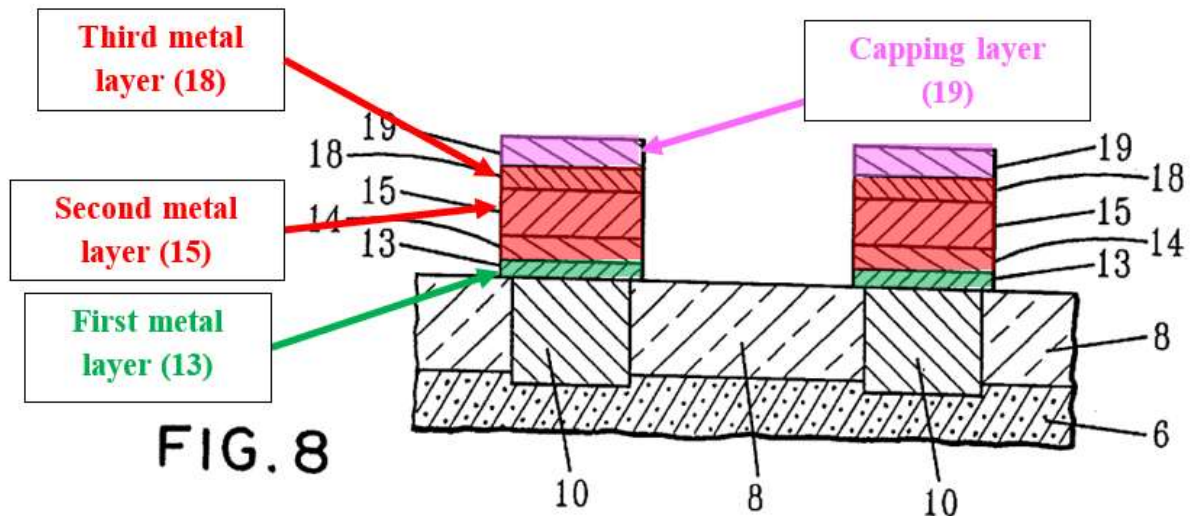
Usui's **layer 18** is titanium and sits directly beneath the capping layer (**third metal layer**) (Usui, 4:4-5, Figs. 1 and 8), **layer 14, 15** comprises aluminum or

aluminum alloy (**second metal layer**) and sits between layer 18 (third layer) and underlayer 13 (bottommost layer) (*id.*, 3:38-41, Figs. 1 and 8), and **underlayer 13** beneath the second metal layer (**bottommost first metal layer**) (*id.*, 5:38, 52, Figs. 1 and 8). Usui's **capping layer 19** is formed on **layer 18 (third metal layer)**. *Id.*, 5:54-59.



Usui, Fig. 8 (annotated); Zhao ¶97.

Additionally, Usui's **layer 15** comprises aluminum or aluminum alloy (**second metal layer**) and sits between layer 18 (third layer) and underlayer 13 (bottommost layer) (*id.*, 3:38-41, Figs. 1 and 8).



Usui, Fig. 8 (annotated); Zhao ¶98.

5. **Claim 5 – The electrical contact of claim 4, wherein said first metal layer and said third metal layer of said electrode stack comprise titanium (Ti).**

Usui discloses claim 5 because its first metal layer and its third metal layer comprise titanium. Zhao ¶99.

Usui's **underlayer 13 (bottommost first metal layer)** is titanium (Usui, 5:23-24) and **layer 18 (third metal layer)** is titanium (*id.*, 5:51-52). Zhao ¶100.

6. **Claim 6 – The electrical contact of claim 4, wherein said second metal layer of said electrode stack comprises aluminum (Al).**

Usui discloses claim 6 because its **layer 15 (second metal layer)** comprises aluminum or an aluminum alloy. Usui, 3:38-41, Figs. 1 and 8. Usui's aluminum or aluminum alloy layer, **layer 15 (second metal layer)**, is described as a highly

textured layer with improved electromigration performance. *Id.*, 3:49-56. Zhao ¶101.

7. Claim 7 – The electrical contact of claim 6, wherein said second metal layer of said electrode stack further comprises silicon (Si).

Usui discloses claim 7 because its **layer 15 (second metal layer)** comprises an aluminum alloy, where typical metal alloys include alloying metal such as **silicon** (Usui, 3:38-43, Figs. 1 and 8). Specifically, Usui discloses “[t]ypical aluminum alloys include alloying metal such as copper, magnesium, **silicon**, lanthanides such as vanadium and yttrium; and palladium” (*id.*). Zhao ¶102. And, as Dr. Zhao explains, using an aluminum-silicon alloy was known and preferred in the art for use in integrated circuits. Zhao ¶¶103-104 (citing Ex-1030, Abstract, 3:25-27, Figs. 1(a)-1(c); Ex-1031, Abstract, 7:44-54, Fig. 13).

B. Ground 2: Usui in View of Yu Renders Obvious Claims 3, 8, 12-13, and 17

1. Overview of the Combination and Motivations to Combine

Usui does not expressly disclose that its capping layer is tantalum nitride, that its electrical contact is used in a III-V semiconductor device, or a gate insulator layer. Each of these, however, as Dr. Zhao explains, were commonly known in the art and expressly taught by Yu. Zhao ¶¶48-50, 60-62, 71-73, 105.

a. Claim 3 – A POSITA would have been motivated to implement Usui’s capping layer as tantalum nitride, as taught by Yu.

Usui’s **capping layer** is not expressly comprised of **tantalum nitride** (claim 3), but Yu expressly discloses a **capping layer** comprising **tantalum nitride**. Yu, [0036]. Zhao ¶106.

As Dr. Zhao explains, by August 2009, it was common and well-known to use tantalum nitride in interconnect structures due to its high thermal, mechanical, and chemical stability. Zhao ¶¶71-73. Indeed, Dr. Zhao explains that it was well-known that titanium nitride and tantalum nitride could be used interchangeably in semiconductor devices. Zhao ¶72 (citing Ex-1026, 2; Ex-1023, 3:39-43; Ex-1024, Abstract, 1:58-61). For example, Ex-1032 discloses a cap layer formed of tantalum nitride (Ex-1032, claim 13). Zhao ¶107.

A POSITA would have appreciated that replacing the titanium nitride of Usui with the tantalum nitride of Yu is merely a suitable design alternative because Yu discloses both titanium nitride (the material expressly disclosed in Usui as the second metal layer) and tantalum nitride may be employed—combining prior art elements according to known techniques to a known device ready for improvements in thermal, mechanical and chemical stability, to yield predictable results. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 401, 416-17 (2007); Zhao ¶¶71-73, 108.

A POSITA would have been motivated to use a tantalum nitride layer to obtain predictable results and would have expected success because tantalum is a known refractory metal and using tantalum nitride as a capping layer in an electrode stack had known benefits and was known in the art. *KSR Int'l Co.*, 550 U.S. at 416-19; Zhao ¶¶71-73, 109.

b. Claims 8 and 13 – A POSITA would have been motivated to implement Usui's electrical contact in a group III-V semiconductor device as taught by Yu.

Usui does not expressly disclose that its electrical contact is configured for implementation on a group III-V semiconductor device, as taught by Yu. By August 2009, as Dr. Zhao explains, group III-V semiconductor devices were well-known and widely used. Zhao ¶¶48-50 (citing Ex-1008, 2-5). For example, group III-nitride semiconductors are essential for developing full-color displays and coherent sources for high-density optical storage technologies. Zhao ¶48. Group III-nitrides were also known to be beneficial for high temperature and high-power electronics applications. Zhao ¶49. Group III-nitrides can support heterostructure technology and have high mechanical and thermal stability. Zhao ¶50. Additionally, GaN was known to have excellent electron transport properties, including good mobility, and high saturated drift velocity. Zhao ¶¶49, 110.

Usui describes its electrical connections are useful to provide connections or wirings between active and/or passive devices of an integrated circuit (Usui, 1:11-

15) (i.e., the devices disclosed in Yu). A POSITA would have been motivated to implement the electrical contacts as taught by Usui in group III-V semiconductor devices, as taught by Yu, as group III-V semiconductor devices are commonly used in the field for active and/or passive devices—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int’l Co.*, 550 U.S. at 416-17; Zhao ¶¶48-50, 111.

c. Claims 12 and 17 – A POSITA would have been motivated to implement Usui’s device as a III-V device with a gate insulator layer, as taught by Yu.

Usui does not expressly disclose an electrical contact implemented with a gate insulator layer underlying a first metal layer of the electrode stack to provide an insulated gate electrode for the group III-V semiconductor device (claims 12 and 17), but Yu does. Yu discloses a multilayer active III-V based semiconductor device (i.e., a thin film transistor) featuring an **interfacial dielectric layer 214** and a **high-k dielectric layer 216 (gate insulator layer)** (Yu, [0039]) underlying a metal **diffusion barrier/protection layer 218 (first metal layer)** (Yu, [0029]). Zhao ¶112.

Usui describes an electrical contact suitable to provide connections or wirings between active and/or passive devices of an integrated circuit (Usui, 1:11-15). Usui further discloses towards a contact for improving electromigration characteristics (Usui, 2:33-35). Zhao ¶113.

By August 2009, as Dr. Zhao explains, Group III-V based materials were well-known for being promising materials for semiconductor device applications as such materials comprise a wide bandgap and high breakdown fields. Zhao ¶¶49, 114 (citing Ex-1008, 3). Further, Dr. Zhao explains that it was well-known that an important design aspect in thin film transistors is isolating the gate from the channel so that no current flows. Zhao ¶¶60, 114 (citing Ex-1011, 356). To a POSITA it would have been obvious to implement the electrical contact of Usui with Yu's gate insulator layer because Usui discloses the importance of improving electromigration characteristics and such layers are commonly provided under gate structures to address gate leakage— combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 401, 416-17; Zhao ¶¶62, 114.

2. Claim 3 – The electrical contact of claim 1, wherein said capping layer comprises tantalum nitride (TaN).

Usui in view of Yu renders obvious claim 3 because Yu discloses a capping layer 226 comprised of **tantalum nitride** and it would have been obvious to implement Usui's capping layer as tantalum nitride. (Yu, Fig. 2, [0036]). Yu discloses “the capping layer 226 may comprise polycrystalline silicon; silicon containing materials; germanium containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, **tantalum nitride**, nickel

silicide, cobalt silicide, other proper conductive materials, and combinations thereof” (emphasis added) (*id.*). Zhao ¶115.

It would have been obvious to implement Usui’s capping layer as comprising tantalum nitride as explained in Section VII.B.1.a. Zhao ¶116.

3. Claim 8 – The electrical contact of claim 1, wherein said electrical contact is configured for implementation on a group III-V semiconductor device.

Usui in view of Yu renders claim 8 obvious because Yu discloses a semiconductor transistor device with a semiconductor substrate comprising silicon, germanium, **a group III-V material** (Yu, [0023]). Zhao ¶117.

Usui discloses an electrical contact suitable to provide connections or wirings between active and/or passive devices of an integrated circuit for improving electromigration characteristics (Usui, 1:11-15, 2:33-35), such as the device disclosed by Yu. Zhao ¶118.

As Dr. Zhao explains, by August 2009, Group III-V based materials are well-known as being promising materials for semiconductor devices such as the transistor of Yu. Because Usui’s device provides improved electromigration characteristics, it would have been obvious for the POSITA to place the Usui contact in the III-V semiconductor transistor of Yu as such materials (i.e., III-V materials) are commonplace within the field and was known in the art, as evidenced by Section VII.B.1.b. Zhao ¶¶48-50, 60-61, 119.

4. **Claim 12 – The electrical contact of claim 8, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.**

Usui in view of Yu renders claim 12 obvious because Yu discloses a semiconductor transistor device with a semiconductor substrate comprising silicon, germanium, **a group III-V material** (Yu, [0023]). Yu discloses an **interfacial dielectric layer 214** and a **high-k dielectric layer 216 (gate insulator layer)** (Yu, [0039]) underlying a metal **diffusion barrier/protection layer 218 (first metal layer)** (Yu, [0029]). Zhao ¶120.

Usui discloses an electrical contact suitable to provide connections or wirings between active and/or passive devices of an integrated circuit for improving electromigration characteristics (Usui, 1:11-15, 2:33-35). Zhao ¶121.

As Dr. Zhao explains, by August 2009, Group III-V based materials were well-known as being promising materials for semiconductor devices such as the transistor of Yu. As Usui's device provides improved electromigration characteristics, it would have been obvious for the POSITA to place the Usui contact in the transistor of Yu and to further include the gate insulator layer as such layers are commonplace within the field and was known in the art, as evidenced by Section VII.B.1.c. Zhao ¶¶48-50, 60-62, 122.

5. Independent Claim 13

- a. [13pre]: An electrical contact for use on a group III-V semiconductor device, said electrical contact comprising:**

[13pre] is identical to [1pre] and claim 8. [13pre] is obvious as explained for [1pre] and claim 8. Zhao ¶123.

- b. [13a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;**

[13a] is identical to [1a]. [13a] is obvious as explained for [1a]. Zhao ¶124.

- c. [13b]: said capping layer consisting only of a metal selected from the group consisting of titanium nitride (TiN) and tantalum nitride (TaN),**

[13b] is identical to claims 2 and 3. [13b] is obvious as explained for claims 2 and 3. Zhao ¶125.

- d. [13c]: said metal forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.**

[13c] is identical to [1c]. [13c] is obvious as explained for [1c]. Zhao ¶126.

- 6. Claim 17 – The electrical contact of claim 13, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.**

Claim 17 is identical to claim 12, but depends from claim 13. Claim 17 is obvious as explained for claim 12. Zhao ¶127.

C. Ground 3: Usui in View of Yu and Further in View of Adesida Renders Obvious Claims 9, 11, 14, and 16

1. Overview of the Combination and Motivations to Combine

Usui and Yu do not expressly disclose its electrical contact being configured for implementation on a HEMT, or its electrical contact being implemented as a gate electrode making Schottky contact. Zhao ¶128.

Adesida is analogous to the '562 patent because it is in the same field of endeavor, forming electrical contacts for semiconductor devices (Adesida, Abstract; '562, Abstract), and addresses the same problem of providing enhanced or simplified fabrication as the '562 patent (Adesida, [0015]-[0017], [0032]-[0034]). Consistent with the '562 patent, Adesida discloses a gate electrode making Schottky contact and power electrodes (source and drain electrodes) making ohmic contact. Adesida, [0031]. Similar to Yu, Adesida also discloses a III-V semiconductor device (*id.*). Zhao ¶129.

a. Claims 9 and 14 - A POSITA would have been motivated to implement Usui's electrical contact on a group III-V semiconductor device, as taught by Yu, comprises a high electron mobility transistor (HEMT) as taught by Adesida

Usui and Yu do not expressly disclose a high electron mobility transistor (HEMT), as taught by Adesida. By August 2009, Dr. Zhao explains it was well-known that HEMTs are used for high power and/or high frequency applications. Zhao ¶51 (citing Ex-1010, [0004]). HEMTs were the most widely used

heterostructure field effect transistors. Zhao ¶52. Dr. Zhao explains it was well-known that the combination of relatively high carrier concentration and relatively high carrier mobility can give the HEMT a relatively large transconductance, and may provide a performance advantage over metal-semiconductor field effect transistors (MESFETS) for high-frequency applications. Zhao ¶¶51, 130 (citing Ex-1010, [0004]).

Usui discloses the importance of enhanced electromigration. Usui, Abstract. A POSITA would have been motivated to implement the electrical contacts as taught by Usui and Yu in group III-V semiconductor HEMT, as taught by Adesida, because group III-V material HEMTs were well-known at the time for providing relatively high carrier mobility (Zhao ¶51) and thus enhanced electromigration and both Yu and Adesida are directed towards the use of III-V semiconductor devices. Furthermore, it was well-known at the time that including the Usui-Yu device on a HEMT, as taught by Adesida, and constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications)—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, at 416-17; Zhao ¶¶48-54, 131.

- b. Claims 11 and 16 - A POSITA would have been motivated to implement Usui's electrical contact as a gate electrode making Schottky contact, as taught by**

**Adesida, with said group III-V semiconductor device
as taught by Yu**

Usui and Yu do not expressly disclose an electrical contact implemented as a gate electrode making Schottky contact. But Adesida does. Like Yu, Adesida teaches the use of a III-V semiconductor device. By August 2009, Dr. Zhao explains it was well-known that Schottky contacts are of critical importance with respect to device functionality, performance, and long-term reliability. Zhao ¶55 (citing Ex-1013, 144). It was well-known that Schottky contacts serve as gate contacts in group III-V devices and have excellent rectifying properties, which make them suitable for high frequency applications. Zhao ¶¶59, 132.

Usui discloses the importance of enhanced electromigration. Usui, Abstract. A POSITA would have been motivated to implement the electrical contacts as taught by Usui-Yu as a gate electrode making Schottky contact, as taught by Adesida, because both Yu and Adesida disclose the use of III-V semiconductor devices. Furthermore, Schottky contacts are well known for their suitability for high frequency applications and therefore enhanced electromigration. Furthermore, it was well-known at the time that implementing the Usui-Yu contact as a Schottky contact, as taught by Adesida, constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications)—combining prior art elements according to known techniques to a known device

ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 416-17; Zhao ¶¶48-59, 133.

2. Claim 9 – The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).

Usui in view of Yu and Adesida renders obvious claim 9 because Adesida discloses a HEMT. Adesida explains that its device is a “**high electron mobility transistor (HEMT)**, which is a field-effect **HEMT** formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT).” Adesida, [0031]. A HEMT is an active device which Usui explicitly states its electrical contacts are suitable for (Usui, 1:11-15). It would have been obvious to implement the electrical contact of Usui-Yu on HEMTs, as taught by Adesida, because both Yu and Adesida disclose III-V semiconductor devices and as further explained in Sections VII.C.1, VII.C.1.a. Zhao ¶¶48-54, 134.

3. Claim 11 – The electrical contact of claim 8, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

Usui in view of Yu and Adesida renders obvious claim 11 because Adesida discloses “a field-effect device, comprising: a layered semiconductor structure that includes a channel layer and at least one layer over the channel layer; spaced apart source and drain contacts disposed over said at least one layer and communicating

with the channel layer; and an iridium gate, between the source and drain contacts, forming a Schottky barrier contact on said at least one layer.” Adesida, [0016].

Zhao ¶135.

Adesida discloses a HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105, on which is an **In_{0.52}Al_{0.48}As barrier layer 150 (group III-V semiconductor device)**. InAlAs is a well-known group III-V material. Adesida, Fig. 5 and [0031]; Zhao ¶¶48-50; Sections VII.C.1, VII.C.1.b. **Gate 190 (gate electrode)** is formed as a **Schottky barrier contact (Schottky contact)** on the **In_{0.52}Al_{0.48}As barrier layer 150 (group III-V semiconductor device)**. Adesida, Fig. 5 and [0031]. Zhao ¶136.

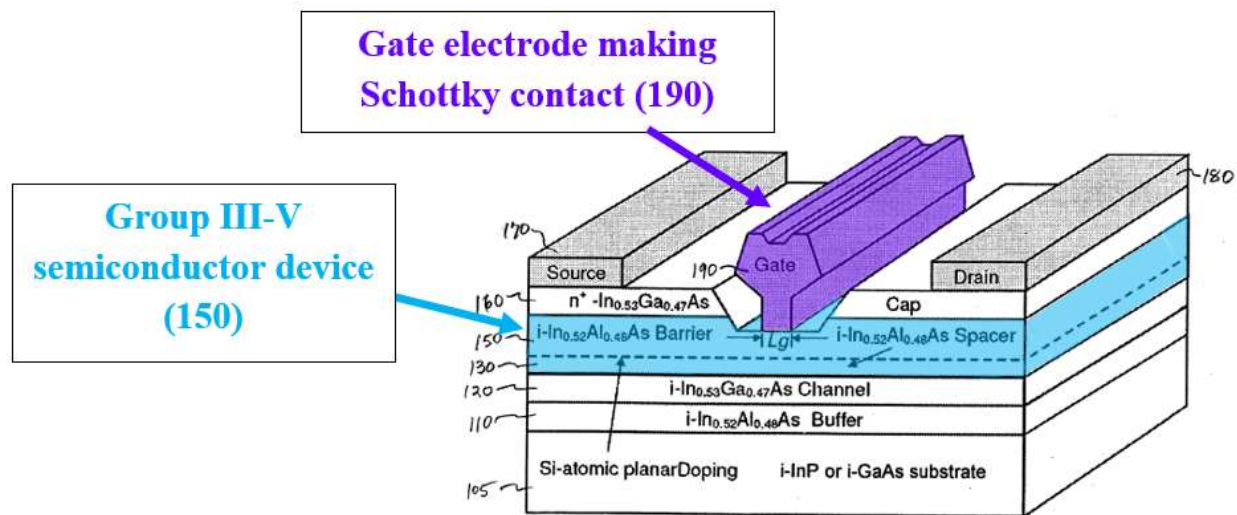


Figure 5

Adesida, Fig. 5 (annotated).

It would have been obvious to implement the electrical contact of Usui-Yu in a device with a gate electrode making Schottky contact, as taught by Adesida. Zhao ¶¶48-61, 137; Sections VII.C.1, VII.C.1.b.

4. Claim 14 – The electrical contact of claim 13, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).

Claim 14 is identical to claim 9, but depends from claim 13. Claim 14 is obvious as explained for claim 9. Zhao ¶138.

5. Claim 16 – The electrical contact of claim 13, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

Claim 16 is identical to claim 11, but depends from claim 13. Claim 16 is obvious as explained for claim 11. Zhao ¶139.

D. Ground 4: Usui in View of Yu and Further in View of Sugimoto Renders Obvious Claims 10 and 15

1. Overview of the Combination and Motivation to Combine

Usui and Yu do not expressly disclose an electrical contact being implemented as a power electrode making ohmic contact, but Sugimoto does. Zhao ¶140.

Like Yu, Sugimoto discloses a group III-V semiconductor device (Sugimoto, 9:7-9). Sugimoto further discloses a device with an AlGaN top layer. Sugimoto, Figs. 1, 3, 5, 7. AlGaN is a well-known group III-V material. Zhao ¶¶48-50.

Sugimoto further discloses the III-V semiconductor device is a HEMT. Sugimoto, 1:22-67. Zhao ¶141.

Sugimoto is analogous to the '562 patent because it is in the same field of endeavor, forming electrical contacts for semiconductor devices (Sugimoto, 9:24-51; '562, Abstract), and addresses the same problem of providing enhanced or simplified fabrication as the '562 patent (Sugimoto, 6:3-7:12, 7:26-39, 7:56-60, 8:30-44). The '562 patent defines “[s]ource electrode 136 and drain electrode 138 are power electrodes ohmically coupled to the heterojunction formed by GaN layer 112 and AlGa_N layer 114.” '562 patent, 3:19-21. Consistent with the '562 patent, Sugimoto discloses a gate electrode making Schottky contact with a group III-V device and power electrodes (source and drain electrodes) making ohmic contact with the group III-V device. Sugimoto, 9:39-51. Sugimoto discloses that its “**drain electrode 42** and the **source electrode 46** make **ohmic contact** with the top surface of the **AlGa_N layer 34**.” Sugimoto, 9:39-51. Zhao ¶142.

Dr. Zhao explains that by August 2009, it was well-known that ohmic contacts were of critical importance with respect to device functionality, performance, and long-term reliability. Zhao ¶55 (citing Ex-1013, 144). It was well-known that ohmic contacts serve as source and drain contacts in group III-V devices and allow current to flow into and out of a semiconductor material without distortion of the signal. Zhao ¶57 (citing Ex-1016, 22; Ex-1017, 1). Dr. Zhao

explains it was well-known that the most critical component of an ohmic contact is its low specific contact resistance, which minimizes the power consumption of the contact and the internal heating of the contact, thereby prolonging device operation with predictable performance. Zhao ¶57 (citing Ex-1016, 22). Furthermore, ohmic contacts allow charges to flow easily between conductors without excess power dissipation, have linear current-voltage characteristics, and do not introduce voltage drops or power loss. Zhao ¶56 (citing Ex-1015, 344). Such characteristics are essential for high-frequency operation used by devices such as the HEMT of Sugimoto. Zhao ¶¶51-57, 143.

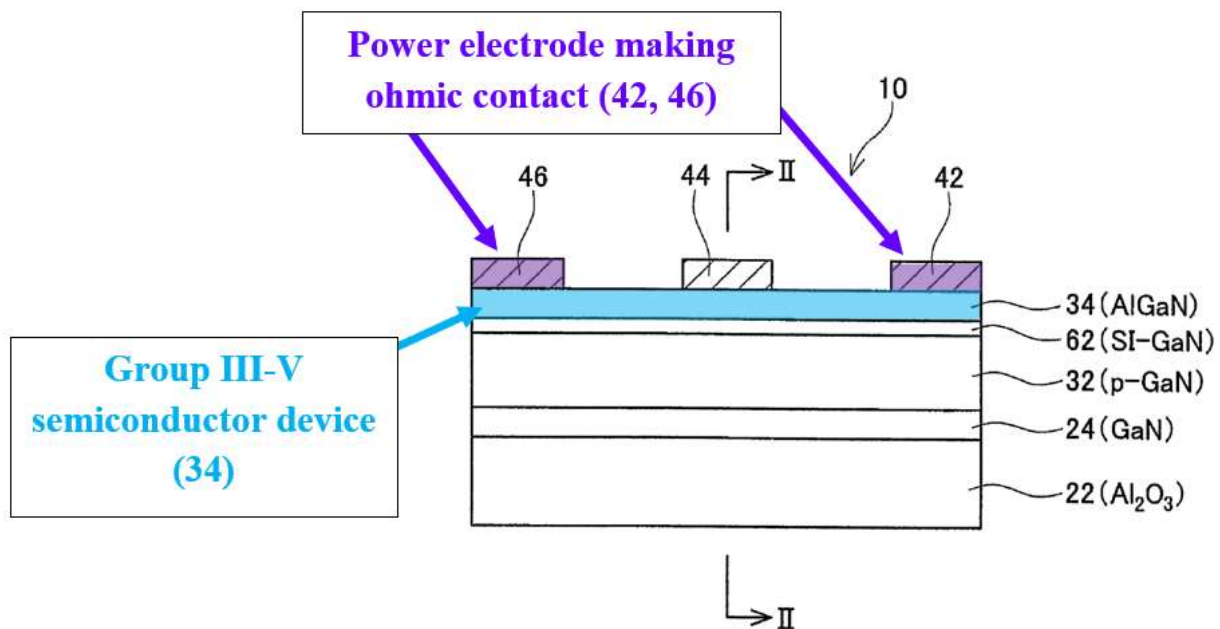
Usui disclosed the importance of enhanced electromigration. Usui, Abstract. A POSITA would have been motivated to implement the contact of Usui-Yu as a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide improved current flow (i.e., enhanced electromigration) and Sugimoto, like Yu, also teaches the use of III-V semiconductor devices. Furthermore, such a combination is the result of combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, at 416-17; *Adesida*, [0031], Fig. 5; Zhao ¶¶51-57, 144.

2. Claim 10 – The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode

making ohmic contact with said group III-V semiconductor device.

Usui in view of Yu and Sugimoto render obvious claim 10 because Sugimoto discloses a HEMT device with a power electrode making an ohmic contact. Zhao ¶145.

Sugimoto discloses that its “**drain electrode 42 (power electrode)** and the **source electrode 46 (power electrode)** make **ohmic contact** with the top surface of the **AlGaN layer 34 (group III-V semiconductor device)**.” (Sugimoto, 9:39-51). Zhao ¶146.



Sugimoto, Fig. 1 (annotated).

It would have been obvious to implement the electrical contact of Usui-Yu as a power electrode making an ohmic contact, as taught by Sugimoto (as

explained in Zhao ¶¶48-57; Section VII.D.1) because both Yu and Sugimoto disclose III-V semiconductor devices and ohmic contacts were typically employed in high-frequency operation devices, such as a HEMT (explained in Zhao ¶¶51-57). Zhao ¶147.

3. Claim 15 – The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.

Claim 15 is identical to claim 10, but depends from claim 13. Claim 15 is obvious as explained for claim 10. Zhao ¶148.

E. Ground 5: Yu in View of Usui Renders Obvious Claims 1-8, 12, 13, and 17

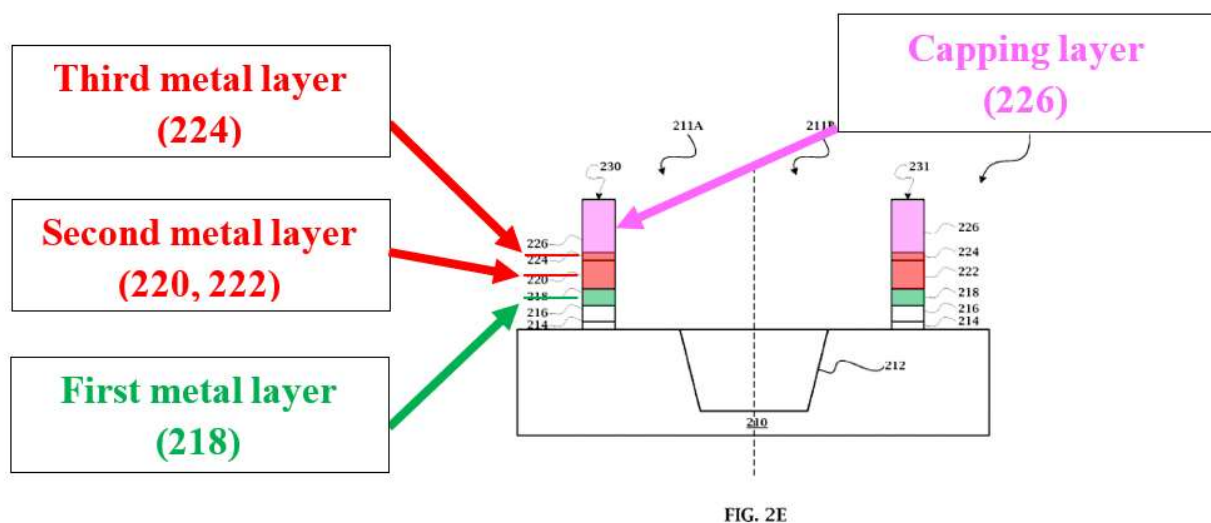
1. Yu

Yu discloses semiconductor devices with electrical connections (e.g., contacts) (Yu, [0040]) and forms metal layers of metal gate stacks with correct work function values and better thermal stability. Yu, [0033]. The work function represents the energy required to remove an electron from the semiconductor to the “free” vacuum level. Ex-1011, 147; Zhao ¶149. In other words, the work function represents the barrier that restricts the flow of electrons in a material. Ex-1011, 229. Zhao ¶149. One configuration involves using metal layers that provide optimal tuning of the work functions of the varying compositions of metal layers. Yu, [0033]; Zhao ¶149.

Like the '562 patent, Yu lists characteristics and variations of its device with trade-offs that were well-known by August 2009. For example, Yu's semiconductor device includes a semiconductor substrate comprising silicon, germanium, a **group III-V material**, or a group II-VI material. Yu, [0023]. Any of these materials were suitable options for the semiconductor device according to Yu, which allows for the design choice and creativity of a POSITA in assembling various devices using different materials depending on the application. A POSITA would have been motivated to implement Yu's device as a group III-V material semiconductor device, as Yu discloses, because semiconductor devices made of group III-V materials were well-known by August 2009 and constituted a simple design choice depending on the application of the device. Zhao ¶¶48-50, 150. Additionally, by August 2009, it was well-known to refer to a semiconductor device with a group III-V semiconductor material in the substrate as a group III-V semiconductor device. Zhao ¶¶48-50, 150.

Yu's device includes **capping layer 226 (capping layer)** comprising polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, **titanium nitride**, **tantalum nitride**, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof ('562 patent, claims 2 and 3). Yu, [0036]. Any of these materials were suitable options for **capping layer 226 (capping layer)**

according to Yu, which allows for the design choice and creativity of a POSITA in assembling various devices using different materials depending on the application. A POSITA would have been motivated to use titanium nitride or tantalum nitride as **capping layer 226 (capping layer)** in Yu's device, as Yu discloses, because by August 2009 titanium nitride and tantalum nitride were well-known refractory metal nitrides and widely used for their good thermal and mechanical properties and low resistivity and constituted a simple design choice depending on the application of the device. Zhao ¶¶71-73, 151.



Yu, Fig. 2E (annotated).

Yu's device also includes **diffusion barrier/protection layer 218 (first metal layer)** comprising **titanium**, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof (Yu, [0029]) and **diffusion barrier layer 224 (third metal layer)** comprising **titanium**, titanium

nitride, tantalum, tantalum nitride, other suitable material, and/or combinations thereof (*id.*, [0035]) ('562 patent, claim 5). Any of these materials were suitable options for **diffusion barrier/protection layer 218** or **diffusion barrier layer 224** according to Yu, which allows for the design choice and creativity of a POSITA in assembling various devices using different materials depending on the application. A POSITA would have been motivated to use titanium as **diffusion barrier/protection layer 218** and **diffusion barrier layer 224** in Yu's device, as Yu discloses, because diffusion barrier layers made of titanium were well-known by August 2009 and constituted a simple design choice depending on the application of the device. Zhao ¶¶66-67, 70, 152.

Yu's device also includes **capping layer 226** (**capping layer**) is preferably 600Å and **diffusion barrier/protection layer 218** (**bottommost layer**) is preferably 20Å (i.e., the **capping layer** is *preferably* thicker than the **bottommost layer**). This disclosure is made with respect to the **capping layer** being polysilicon (Yu, [0036], [0040]), which is not a **refractory metal nitride** as is stated in claims 1 and 13. However, Yu teaches the **capping layer** may be titanium nitride and tantalum nitride, which are **refractory metal nitrides**. Zhao ¶152.

Yu's device also includes **metal layers 220, 222** (**second metal layer**) comprise a doped-conducting metal oxide (DCO), where the DCO comprises "...

ZnO doped with Al, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf, and/or combinations thereof...) (Yu, [0033]). Zhao ¶152.

Yu is analogous to the '562 patent because it is in the same field of endeavor, semiconductor devices featuring an electrode stack featuring a plurality of metal layers (Yu, Abstract, Fig. 2E, gate stacks 230 and 231; '562 patent, Abstract) and addresses the same problem, fabrication of semiconductor materials with improved characteristics (Yu, Abstract; '562 patent, 1:25-29, 1:56-62) as the '562 patent.

Zhao ¶153.

2. Overview of the Combination and Motivations to Combine

Claims 1-8, 12, 13, and 17 are directed to an electrical contact for use on a semiconductor device, including a capping layer thicker than a bottommost metal layer ('562 patent, claims 1 and 13) and a second metal layer comprising aluminum or an aluminum and silicon ('562 patent, claims 6 and 7). Yu at least suggests these limitations, and Usui expressly discloses them. A POSITA would have found it obvious to combine Yu and Usui to achieve claims 1, 6, 7, and 13 because their combination is combining prior art elements according to known methods to yield predictable results, a simple substitution of one known element for another to obtain predictable results and applying known techniques to a known device ready for improvement to yield predictable results. Zhao ¶154.

- a. **Claims 1 and 13 – A POSITA would have been motivated to form Yu’s capping layer of a refractory metal nitride thicker than the bottommost metal layer, as taught by Usui**

Yu expressly discloses every element of claims 1 and 13 except a **refractory metal nitride capping layer** having a thickness greater than that of a **bottommost layer** (claim element [1c]). While Yu discloses the **capping layer** is *preferably* 600Å and the **bottommost layer** 20Å (i.e., the **capping layer** is *preferably* thicker than the **bottommost layer**), this disclosure is made with respect to the **capping layer** being polysilicon (Yu, [0036], [0040]), which is not a **refractory metal nitride** as is stated in claims 1 and 13. However, Yu teaches the **capping layer** may be titanium nitride and tantalum nitride, which are **refractory metal nitrides**. A POSITA would have been motivated to replace Yu’s polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed thicknesses because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation as explained by Dr. Zhao. Zhao ¶¶71-73, 155 (citing Ex-1025, 120; Ex-1026, 2; Ex-1028, 46, 56; Ex-1023, 3:39-43; Ex-1024, Abstract, 1:58-61; Ex-1029, Abstract, 1:29-34, 2:47-51).

To the extent Yu does not expressly disclose a **refractory metal nitride capping layer** having a thickness greater than that of a **bottommost layer**, Usui does. As Usui recognizes, “by limiting the thickness of this underlayer 13, the

structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention.” Usui, 3:29-37. This benefit of limiting the bottommost metal layer of an electrode stack was well-known by August 2009, as explained by Dr. Zhao. Zhao ¶¶70, 156 (citing Ex-1022, Abstract; Ex-1023, 3:33-37; Ex-1024, 3:9-15).

Moreover, Yu expressly discloses that **diffusion barrier/protection layer 218 (bottommost layer** of plurality of metal layers) (Yu, [0029], Fig. 2E) may be “any suitable thickness.” *Id.*, [0029] and [0036]. Zhao ¶157.

A POSITA would have been motivated to apply known techniques of limiting the thickness of Usui **underlayer 13 (bottommost metal layer)** to **diffusion barrier/protection layer 218 (bottommost layer)** in Yu’s known device ready for improvement to yield predictable results and would have expected success because limiting the thickness of the bottommost metal layer had known benefits and was known in the art—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int’l Co.*, 550 U.S. at 401, 416-17; Zhao ¶¶66-67, 70, 158.

b. Claims 6 and 7 – A POSITA would have been motivated to form Yu’s metal layers of Al and Si, as taught by Usui

Yu expressly discloses **metal layers 220, 222 (second metal layer)** comprise a doped-conducting metal oxide (DCO), where the DCO comprises “... ZnO doped with Al, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf, and/or combinations thereof...” (Yu, [0033]). While Al (claim 6) and Al further comprising Si (claim 7) are one of many possible combinations disclosed in Yu, the POSITA would have been motivated to provide such a combination as the benefits of such are well known, as explained by Dr. Zhao. Zhao ¶¶68-69 (citing Ex-1020, 2859; Ex-1011, 216; Ex-1019, 426-428). By August 2009, it was well-known that aluminum and aluminum alloys are common, low-cost, provide better adhesives to the metal stack, and improve thermal properties of the structure (Zhao ¶¶68-69). Zhao ¶159.

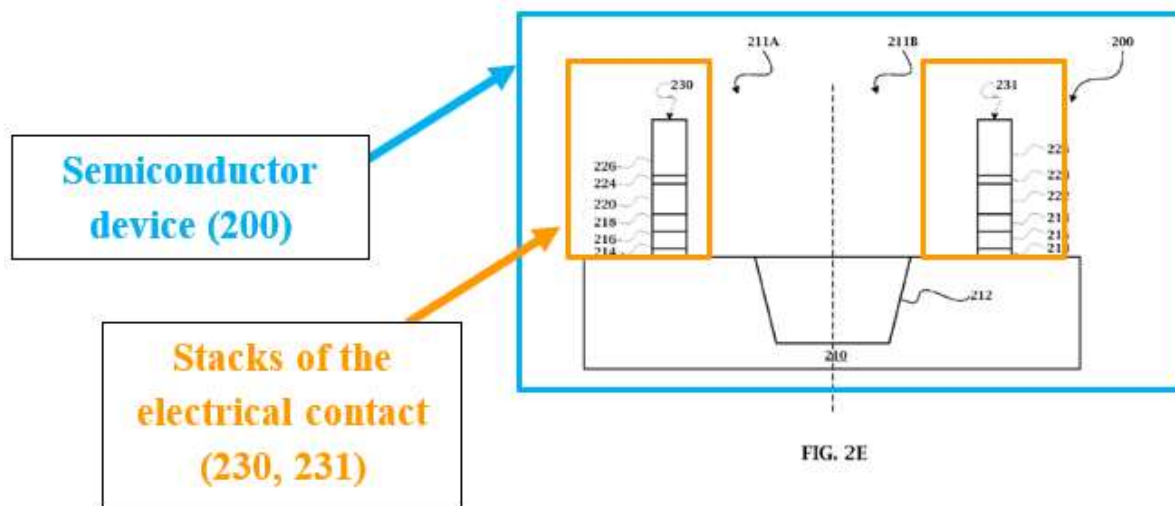
To the extent that Yu does not expressly disclose **second metal layer** featuring Al and further comprising Si, Usui expressly teaches this combination of materials. A POSITA would have been motivated to implement Usui’s **layer 15 (second metal layer)** as a simple substitution in **metal layers 220, 222 (second metal layer)** of Yu’s device to obtain predictable results and would have expected success because using aluminum or aluminum silicon as a metal layer in an electrode stack had known benefits and was known in the art—combining prior art elements according to known techniques to a known device and simple substitution

of one known element for another ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 416-19; Zhao ¶¶68-69, 160.

3. Claim 1

- a. [1pre]: An electrical contact for use on a semiconductor device, said electrical contact comprising:

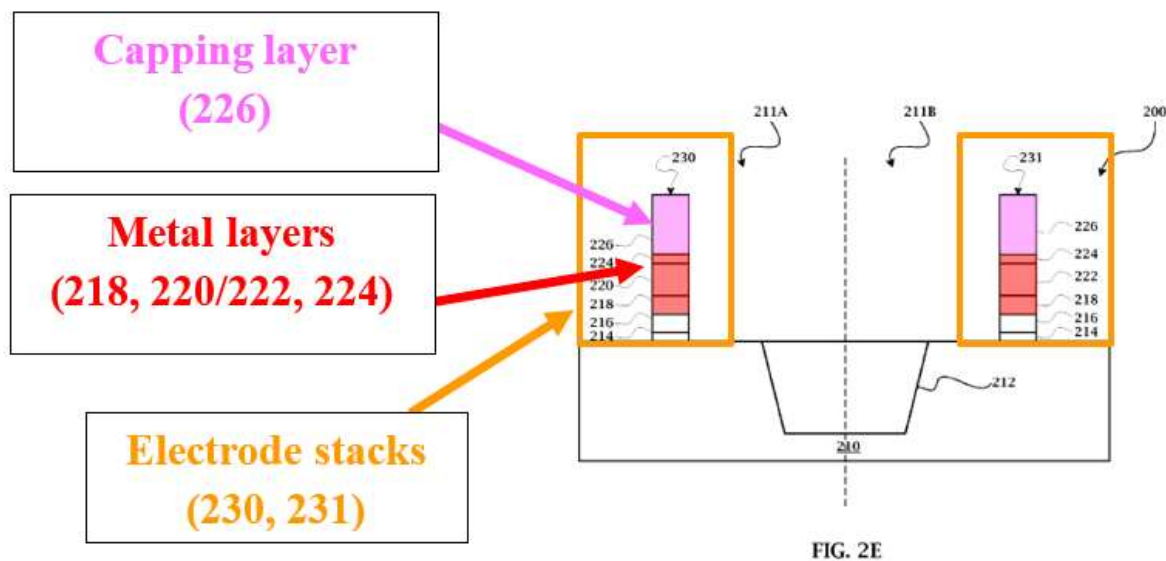
If limiting, Yu discloses [1pre] because it discloses “various contacts/vias and multilayer interconnect features (e.g., metal layers and interlayer dielectrics) may be formed on the substrate 210 and configured to connect the various features or structures of the semiconductor device 200,” including metal gate stacks 230 and 231 (stacks of the electrical contacts). Yu, [0040] and Fig. 2E.



Id., Fig. 2E (annotated); Zhao ¶161.

- b. [1a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;

Yu discloses [1a] because it discloses **metal gate stacks 230, 231** (**electrode stacks**) each including a metal **diffusion barrier/protection layer 218** (**first metal layer**) (*id.*, [0029]), **metal layers 220, 222** (*id.*, [0035]) (**second metal layer**), a metal **diffusion barrier layer 224** (*id.*, [0035]) (**third metal layer**), and a **capping layer 226** (*id.*, [0036]) (**capping layer**) formed over the metal layers.



Id., Fig. 2E (annotated); Zhao ¶162.

- c. [1b]: said capping layer consisting only of a refractory metal nitride,

Yu discloses [1b] because it discloses that **capping layer 226** (**capping layer**) (*id.*, [0036]) is **titanium nitride** or **tantalum nitride** (**refractory metal nitride**) (*id.*). A POSITA would have known that titanium nitride and tantalum

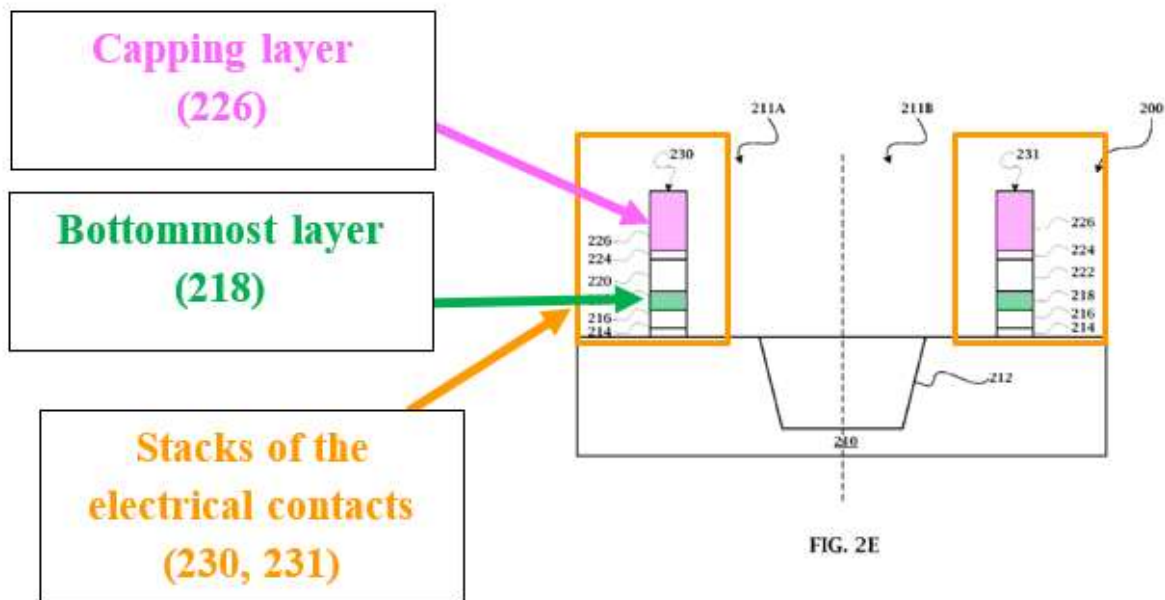
nitride are each a “refractory metal nitride.” Sections VII.E.2, VII.E.2.a; Zhao ¶¶71-73, 163.

As explained by Dr. Zhao, refractory metals are a class of metals known for resistance to heat and wear. Zhao ¶71 (citing Ex-1025, 120). The most common definition of refractory metals are metals comprising a melting point above 2,204°C, such as niobium, molybdenum, tantalum, tungsten and rhenium. Zhao ¶71 (citing Ex-1025, 120). A wider definition of refractory metals includes metals such as titanium. Zhao ¶71 (citing Ex-1027, 1). Titanium nitride was a well-known and widely used refractory metal nitride which possesses a useful combination of useful mechanical and chemical properties such as hardness and corrosion and heat resistance. Zhao ¶¶72, 164.

- d. **[1c]: said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.**

Yu at least suggests [1c] because it discloses **capping layer 226** is **titanium nitride** or **tantalum nitride (refractory metal nitride)** (*id.*, [0036]) forming a top of **metal gate stacks 230, 231 (electrode stacks of the electrical contact)** (*id.*, [0040], Fig. 2E) and having a thickness of about 200-1,000 Å, preferably about 600 Å (*id.*, [0036]), which is greater than the thickness of **diffusion barrier/protection layer 218 (bottommost layer of plurality of metal layers)** (*id.*,

[0029], Fig. 2E), which is 20 Å (*id.*, [0029]). As explained in Sections VII.E.2 and VII.E.2.a, a POSITA would have understood these thicknesses apply to Yu's capping and bottommost layer regardless of whether Yu's capping layer is comprised of polysilicon or titanium nitride or tantalum nitride.

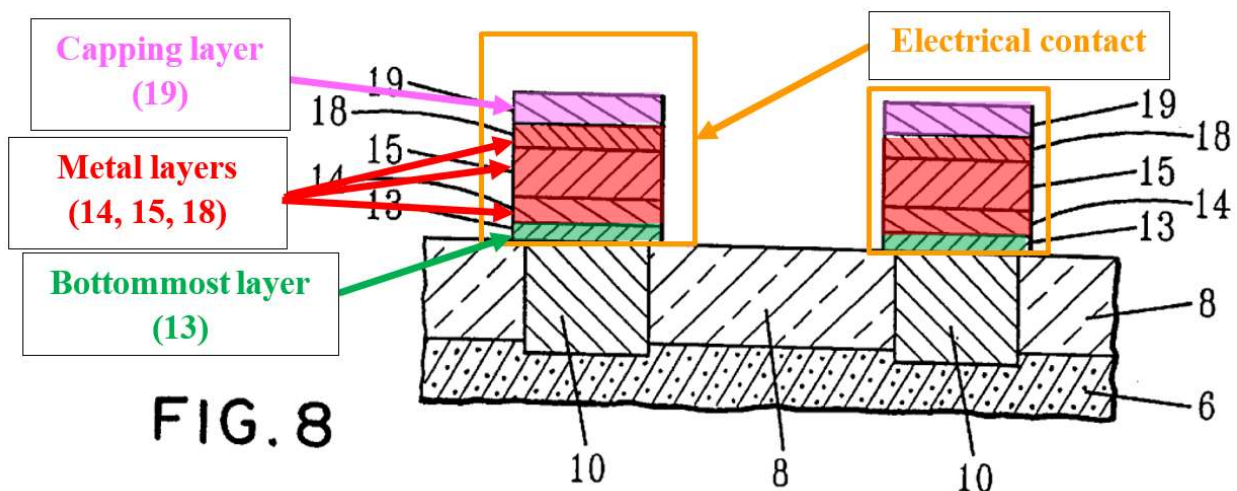


Id., Fig. 2E (annotated); Zhao ¶165.

Layer 214 and 216 cannot be the bottommost layer of the “plurality of **metal layers**” because they are dielectric layers not “metal layers.” Layer 214 is an interfacial dielectric layer and layer 216 is a high-k dielectric layer. *Id.*, [0039]. Dielectric layers are insulating (Zhao ¶62) whereas metal layers are conductive (i.e., current flows in metals) (Ex-1011, 50). Therefore, interfacial dielectric layer

214 and high-k dielectric layer 216 cannot be the bottommost layer of the plurality of **metal** layers. Zhao ¶166.

To the extent Yu does not expressly disclose that its capping layer is a refractory metal nitride, the use of a refractory metal nitride would have been obvious over Yu and Usui. Usui expressly discloses a capping layer comprising only a refractory metal nitride thicker than a bottommost layer, as was known in the art (Sections VII.A.1, VII.A.2.d, VII.E.2, VII.E.2.a). Usui expressly discloses that its **capping layer 19** is **titanium nitride (refractory metal nitride)** (Usui, 5:54-59) forming a top of the **metallization structure (electrical contact)** (*id.*, Abstract, 3:2-8, Figs. 1 and 8) and having a thickness of about 150-800 Å, more typically about 200-500 Å (*id.*, 4:5-8), which is greater than the thickness of **underlayer 13 (bottommost layer** of plurality of metal layers) (*id.*, 5:38, 52, Figs. 1 and 8), which is 90-110 Å (*id.*, 3:29-33). Zhao ¶167.



Id., Fig. 8 (annotated).

A POSITA would have been motivated to and had a reasonable expectation of success to implement Yu's **capping layer 226** as a refractory metal nitride with a greater thickness than its **bottommost layer 218**, as expressly taught by Usui to carefully control the structure and texture of the subsequently to applied metallic layers—a benefit recognized by Usui—as explained in Sections VII.E.2, VII.E.2.a; Usui, 3:29-37; Zhao ¶168.

4. Claim 2 – The electrical contact of claim 1, wherein said capping layer comprises titanium nitride (TiN).

Yu at least suggests claim 2 because it discloses **capping layer 226** (**capping layer**) (*id.*, [0036]) comprises **titanium nitride** (*id.*). Yu's device includes **capping layer 226** (**capping layer**) comprising polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, **titanium nitride**, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. Yu, [0036]; Zhao ¶169.

To the extent Yu does not expressly disclose that its capping layer comprised of titanium nitride is of a thickness greater than the thickness of its bottommost layer, Usui similarly discloses a capping layer comprised of titanium nitride at a thickness greater than a bottommost layer, as explained for [1c] and claim 2,

Ground 1. (Sections VII.A.2.c, VII.A.2.d, VII.A.3, VII.E.2, VII.E.2.a). A POSITA would have been motivated to use titanium nitride as **capping layer 226**, as Yu discloses, in Yu's device at a thickness greater than that of Yu's bottommost layer, as suggested by Yu and disclosed by Usui, because, as Usui recognizes, "by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention." Usui, 3:29-37; Sections VII.E.2, VII.E.2.a. This benefit of limiting the bottommost metal layer of an electrode stack was well-known by August 2009, as explained by Dr. Zhao. Zhao ¶70 (citing Ex-1022, Abstract; Ex-1023, 3:33-37; Ex-1024, 3:9-15). And capping layers made of titanium nitride were well-known by August 2009 and constituted a simple design choice depending on the application of the device. Sections VII.E.2, VII.E.2.a; Zhao ¶¶71-73, 170.

5. Claim 3 – The electrical contact of claim 1, wherein said capping layer comprises tantalum nitride (TaN).

Yu at least suggests claim 3 because it discloses **capping layer 226** (**capping layer**) (*id.*, [0036]) comprising **tantalum nitride** (*id.*). Yu's device includes **capping layer 226** (**capping layer**) comprising polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, **tantalum nitride**,

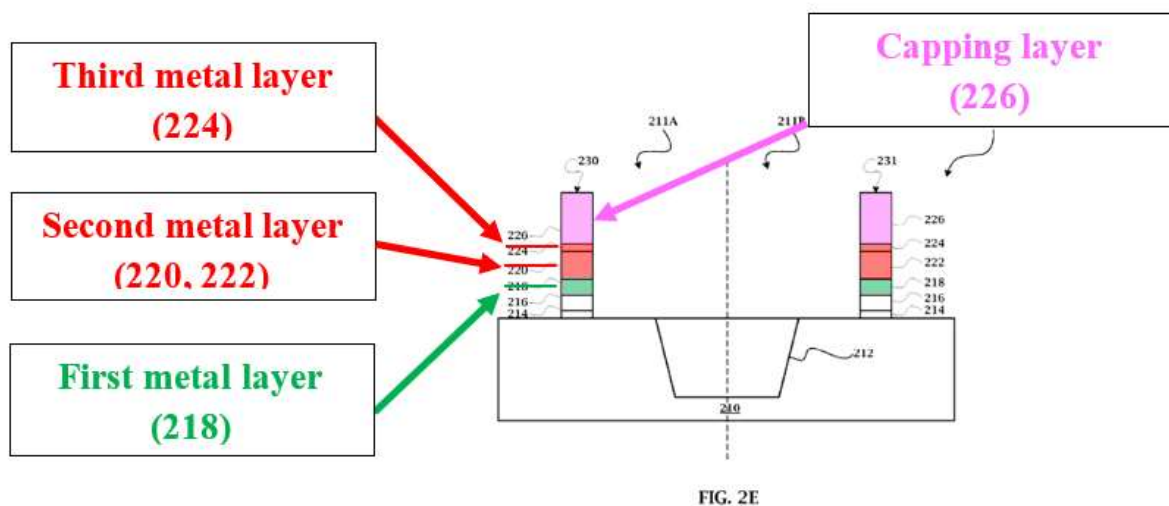
nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. Yu, [0036]; Zhao ¶171.

To the extent Yu does not expressly disclose that its capping layer comprised of tantalum nitride is of a thickness greater than the thickness of its bottommost layer, this would have been obvious in view of Usui, which discloses a capping layer of nitride materials at a thickness greater than a bottommost layer, as explained for [1c]. Section VII.E.3.d. A POSITA would have been motivated to use tantalum nitride as **capping layer 226** in Yu's device, in Yu's device at a thickness greater than that of Yu's bottommost layer, as suggested by Yu and disclosed by Usui, because, as Usui recognizes, "by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention." Usui, 3:29-37. This benefit of limiting the bottommost metal layer of an electrode stack was well-known by August 2009, as explained by Dr. Zhao. Zhao ¶70 (citing Ex-1022, Abstract; Ex-1023, 3:33-37; Ex-1024, 3:9-15). And capping layers made of tantalum nitride were well-known by August 2009 and constituted a simple design choice depending on the application of the device—as explained in Sections VII.E.2, VII.E.2.a; Zhao ¶¶71-73, 170-172.

6. **Claim 4 – The electrical contact of claim 1, wherein said plurality of metal layers includes respective first, second, and third metal layers, wherein said second metal layer is**

formed between said first metal layer and said third metal layer, and said capping layer is formed on said third metal layer.

Yu discloses claim 4 because it discloses **metal layers 220, 222** (**second metal layer**) (Yu, [0035]) being formed between **diffusion barrier/protection layer 218** (**first metal layer**) (*id.*, [0029]) and **diffusion barrier layer 224** (**third metal layer**) (*id.*, [0035]), and **capping layer 226** (**capping layer**) (*id.*, [0036]) being formed on **diffusion barrier layer 224** (**third metal layer**) (*id.*, [0035]).



Id., Fig. 2E (annotated); Zhao ¶173.

7. **Claim 5 – The electrical contact of claim 4, wherein said first metal layer and said third metal layer of said electrode stack comprise titanium (Ti).**

Yu discloses claim 5 because it discloses **diffusion barrier/protection layer 218** (**first metal layer**) being **titanium** (Yu, [0029]) and **diffusion barrier layer 224** (**third metal layer**) being **titanium** (*id.*, [0035]). Yu's device includes

diffusion barrier/protection layer 218 (first metal layer) and **diffusion barrier layer 224 (third metal layer)** comprising **titanium**, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. Yu, [0029], [0035]; Zhao ¶174.

8. Claim 6 – The electrical contact of claim 4, wherein said second metal layer of said electrode stack comprises aluminum (Al).

Yu at least suggests claim 6 because Yu discloses **metal layers 220, 222 (second metal layer)** comprise a doped-conducting metal oxide (DCO), where the DCO comprises “... ZnO doped with **Al**, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf, and/or combinations thereof...”) (Yu, [0033]). While **aluminum** is one of many possible doping materials for **metal layers 220, 222 (second metal layer)** disclosed in Yu, a POSITA would have understood the well-known benefits of using aluminum in metal layers in an electrode stack, as explained by Dr. Zhao. Zhao ¶¶68-69, 175.

To the extent Yu does not expressly disclose that its second metal layer comprises aluminum, Usui discloses an aluminum second metal layer, and it would have been obvious to use aluminum as the second metal layer in Yu’s devices (explained in Sections VII.E.2, VII.E.2.b). Usui explains that **layer 15 (second metal layer)** comprises **aluminum** or an aluminum alloy. Usui, 3:38-43, Figs. 1 and 8. A POSITA would have been motivated to similarly implement Yu’s second

metal layer as comprising aluminum, as taught by Usui, because Usui explains that its aluminum or aluminum alloy layer, **layer 15 (second metal layer)**, is a highly textured layer with improved electromigration performance. *Id.*, 3:49-56; Zhao ¶176.

Moreover, as Dr. Zhao explains, by August 2009, it was well-known that aluminum is common, low-cost, provides better adhesives to the metal stack, and improves thermal properties of the structure. Zhao ¶¶68-69. Therefore, a POSITA would have been motivated to use aluminum as **layer 15 (second metal layer)** as a simple substitution in **metal layers 220, 222 (second metal layer)** of Yu's device to obtain predictable results and would have expected success because using aluminum as a metal layer in an electrode stack had known benefits and was known in the art. *KSR Int'l Co.*, 550 U.S. at 416-19; Sections VII.E.2, VII.E.2.b; Zhao ¶¶68-69, 177.

9. Claim 7 – The electrical contact of claim 6, wherein said second metal layer of said electrode stack further comprises silicon (Si).

Yu at least suggests claim 7 because Yu discloses **metal layers 220, 222 (second metal layer)** comprise a doped-conducting metal oxide (DCO), where the DCO comprises "... ZnO doped with Al, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf, and/or combinations thereof...) (Yu, [0033]). While **aluminum** further comprising **silicon** is one of many possible material combinations for **metal layers**

220, 222 (second metal layer) disclosed in Yu, would have understood the well-known benefits of using aluminum and silicon in metal layers in an electrode stack, as explained by Dr. Zhao. Zhao ¶¶68-69, 178 (citing Ex-1035, 3, 7, 9-10, 12-14).

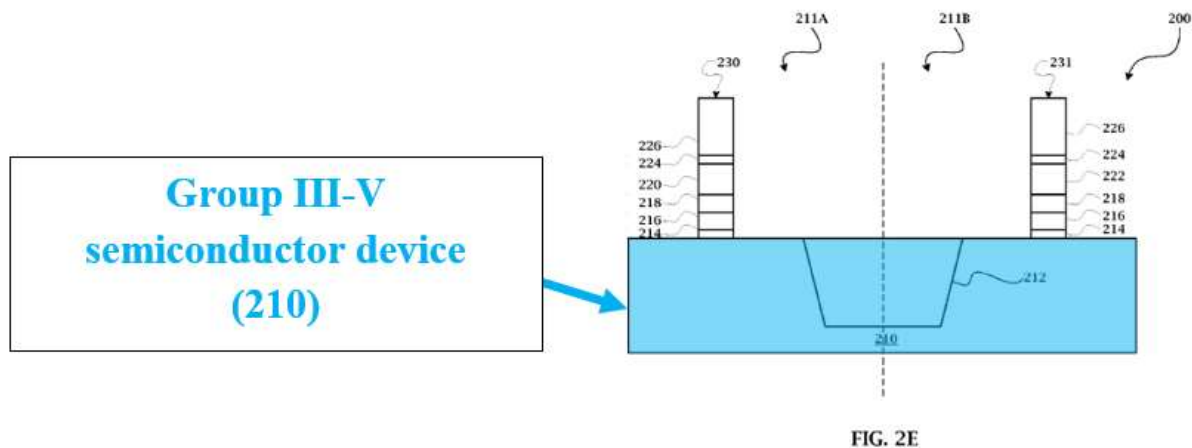
To the extent Yu does not expressly disclose that its second metal layer comprises aluminum and silicon, Usui discloses an aluminum silicon second metal layer, and it would have been obvious to use aluminum silicon as the second metal layer in Yu's devices (explained in Sections VII.E.2, VII.E.2.b). Usui explains that **layer 15 (second metal layer)** comprises **aluminum silicon**. Usui, 3:38-43, Figs. 1 and 8. Specifically, Usui discloses "[t]ypical aluminum alloys include alloying metal such as copper, magnesium, silicon, lanthanides such as vanadium and yttrium; and palladium" (*id.*). A POSITA would have been motivated to similarly implement Yu's second metal layer as comprising aluminum and silicon, as taught by Usui, because Usui explains that its aluminum or aluminum alloy layer, **layer 15 (second metal layer)**, is a highly textured layer with improved electromigration performance. *Id.*, 3:49-56; Zhao ¶179.

Moreover, a POSITA would have been motivated to use aluminum silicon as **layer 15 (second metal layer)** as a simple substitution in **metal layers 220, 222 (second metal layer)** of Yu's device to obtain predictable results and would have expected success because using aluminum silicon as a metal layer in an electrode stack had known benefits and was known in the art. *KSR Int'l Co.*, 550 U.S. at 416-

19; Sections VII.E.2, VII.E.2.b; Zhao ¶¶68-69. For example, it was well-known that aluminum silicon is common, low-cost, provides better adhesives to the metal stack, and improves thermal properties of the structure. Zhao ¶¶68, 180.

10. Claim 8 – The electrical contact of claim 1, wherein said electrical contact is configured for implementation on a group III-V semiconductor device.

Yu discloses claim 8 because it discloses “the semiconductor substrate 210 comprises silicon, germanium, a **group III-V** material.” Yu, [0023].

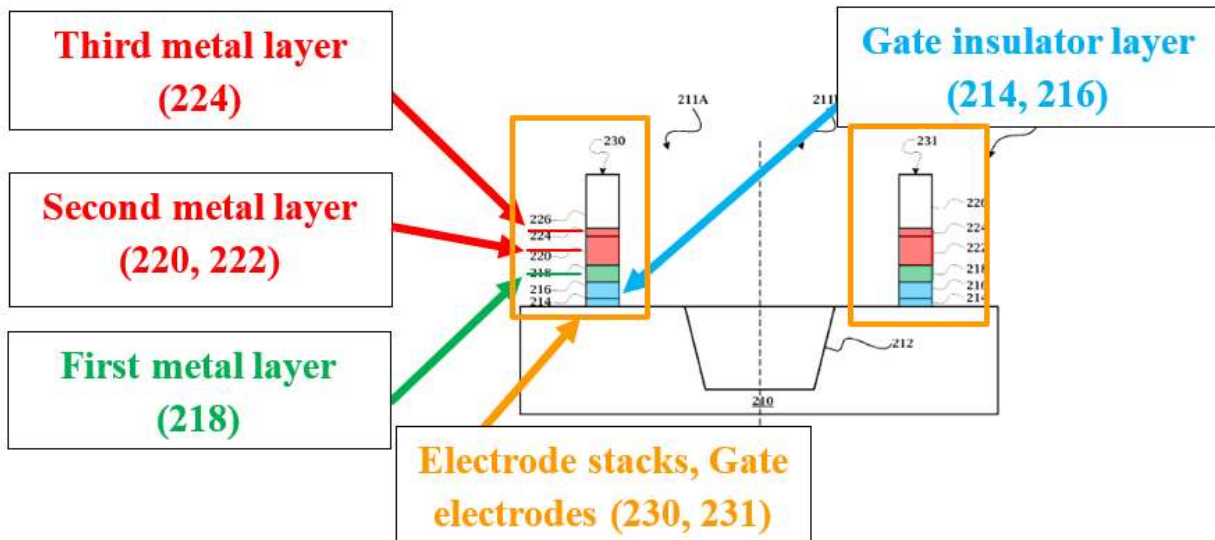


Id., Fig. 2E (annotated); Zhao ¶181.

11. Claim 12 – The electrical contact of claim 8, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

Yu discloses claim 12 because it discloses the **interfacial dielectric layer 214** and the **high-k dielectric layer 216 (gate insulator layer)** (Yu, [0039])

underlying a metal **diffusion barrier/protection layer 218 (first metal layer)** (*id.*, [0029]) of **metal gate stacks 230, 231 (electrode stack)** to provide insulated **metal gate stacks 230, 231 (gate electrode)** for the group III-V semiconductor device (*id.*, [0023]). Dielectric materials are insulating materials commonly provided under gate structures—as explained by Dr. Zhao. Zhao ¶62 (citing Ex-1018, 937; Ex-1011, 396).



Id., Fig. 2E (annotated); Zhao ¶182.

12. Independent Claim 13

- a. [13pre]: An electrical contact for use on a group III-V semiconductor device, said electrical contact comprising:

[13pre] is identical to [1pre] and claim 8. [13pre] is obvious as explained for [1pre] and claim 8. Zhao ¶183.

- b. [13a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;**

[13a] is identical to [1a]. [13a] is obvious as explained for [1a]. Zhao ¶184.

- c. [13b]: said capping layer consisting only of a metal selected from the group consisting of titanium nitride (TiN) and tantalum nitride (TaN),**

[13b] is identical to claims 2 and 3. [13b] is obvious as explained for claims 2 and 3. Zhao ¶185.

- d. [13c]: said metal forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.**

[13c] is identical to [1c]. [13c] is obvious as explained for [1c]. Zhao ¶186.

- 13. Claim 17 – The electrical contact of claim 13, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.**

Claim 17 is identical to claim 12, but depends from claim 13. Claim 17 is obvious as explained for claim 12. Zhao ¶187.

F. Ground 6: Yu in View of Usui and Adesida Renders Obvious Claims 9, 11, 14, and 16

1. Overview of the Combination and Motivations to Combine

Yu and Usui do not expressly disclose that their group III-V devices are HEMTs or a gate electrode making a Schottky electrical contact with a group III-V device. Zhao ¶188.

Consistent with the '562 patent, Adesida discloses a gate electrode making Schottky contact with a group III-V device and power electrodes (source and drain electrodes) making ohmic contact with the group III-V device. Adesida, [0031].

Adesida discloses a semiconductor device with various contacts and metallization (Adesida, [0031]-[0032]) and forming a thermally stable gate metal (Adesida, [0030]). Adesida discloses “a field-effect device, comprising: a layered semiconductor structure that includes a channel layer and at least one layer over the channel layer; spaced apart source and drain contacts disposed over said at least one layer and communicating with the channel layer; and an iridium **gate**, between the source and drain contacts, **forming a Schottky barrier contact on said at least one layer.**” Adesida, [0016]. Adesida further states that its device is a “**high electron mobility transistor (HEMT)**, which ... is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT),” where the HEMT device comprises an undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer formed beneath the gate. Adesida, [0031], Fig. 5. $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ is a well-known group III-V material. Zhao ¶¶48-50, 189.

a. Claims 9 and 14 – A POSITA would have been motivated to implement Yu’s device as a HEMT, as taught by Adesida

Yu does not expressly disclose a semiconductor device comprising a high electron mobility transistor (HEMT), but Adesida does, and Dr. Zhao explains that by August 2009, it was well-known that HEMTs are used for high power and/or high frequency applications. Zhao ¶51 (citing Ex-1010, [0004]). HEMTs were the most widely used heterostructure field effect transistors. Zhao ¶51 (citing Ex-1011, 375). It was well-known that the combination of relatively high carrier concentration and relatively high carrier mobility gives the HEMT a relatively large transconductance and provide a performance advantage over metal-semiconductor field effect transistors (MESFETS) for high-frequency applications. Zhao ¶¶51, 190 (citing Ex-1010, [0004]).

Yu describes the need of providing a semiconductor device with an improved work function. Yu, Abstract. A work function is defined as the amount of energy required to eject electrons from a surface. A POSITA would have been motivated to implement Yu’s device as a HEMT, as taught by Adesida, because HEMTs were well-known at the time for providing high carrier mobility and therefore improved work function characteristics, as desired by Yu. Furthermore, it was well-known at the time that modifying the Yu device to comprise a HEMT constituted a simple design choice depending on the application of the device (e.g.,

high power and/or high frequency applications)— combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int’l Co.*, 550 U.S. at 416-17; Zhao ¶¶51-54, 191.

b. Claims 11 and 16 – A POSITA would have been motivated to implement Yu’s electrical contact as a gate electrode making a Schottky contact, as taught by Adesida

Yu does not expressly teach an electrical contact implemented as a gate electrode making a Schottky contact, but Adesida does, and Dr. Zhao explains that by August 2009, it was well-known that Schottky contacts were of critical importance to device functionality, performance, and long-term reliability. Zhao ¶55 (citing Ex-1013, 144). It was well-known that Schottky contacts serve as gate contacts in group III-V devices, have a fast response for many applications due to their unipolar carrier transport, and have excellent rectifying properties, which make them suitable for high frequency applications. Zhao ¶¶58-59, 192 (citing Ex-1011, 219; Ex-1017, 1, 87).

Yu describes the need of providing a semiconductor device with an improved work function. Yu, Abstract. A work function is defined as the amount of energy required to eject electrons from a surface. A POSITA would have been motivated to implement Yu’s device as a gate electrode making a Schottky contact, as taught by Adesida, because Schottky contacts were well-known at the time for

providing a fast response for many applications due to their unipolar carrier transport. Furthermore, modifying the Yu device to include a Schottky contact constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications)— combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int’l Co.*, 550 U.S. at 416-17; Zhao ¶¶55, 58-59, 193.

2. Claim 9 – The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).

Yu in view of Usui and Adesida renders obvious claim 9 because Adesida discloses a HEMT, and it would have been obvious to implement Yu-Usui’s group III-V semiconductor devices as HEMTs (explained in VII.F.1, VII.F.1.a). Zhao ¶¶51-54, 194.

Adesida explains that its device is a “**high electron mobility transistor (HEMT)**, which ... is a field-effect **HEMT** formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT).” Adesida, [0031]. Zhao ¶195.

3. Claim 11 – The electrical contact of claim 8, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

Yu in view of Usui and Adesida renders obvious claim 11 because Adesida discloses a group III-V device with a gate electrode making a Schottky contact

with the group III-V device, and it would have been obvious to implement Yu or Yu-Usui's group III-V semiconductor devices with gate electrodes making Schottky contacts (explained in Sections VII.F.1, VII.F.1.b). Zhao ¶¶48-55, 58-61, 196.

Adesida discloses “a field-effect device, comprising: a layered semiconductor structure that includes a channel layer and at least one layer over the channel layer; spaced apart source and drain contacts disposed over said at least one layer and communicating with the channel layer; and an iridium gate, between the source and drain contacts, **forming a Schottky barrier contact on said at least one layer.**” Adesida, [0016]. Zhao ¶197.

For example, Adesida discloses a HEMT formed on an **indium phosphide substrate or gallium arsenide substrate 105**, on which is an **In_{0.52}Al_{0.48}As barrier layer 150 (group III-V semiconductor device)**. InAlAs is a well-known group III-V material—as discussed by Dr. Zhao (Zhao ¶¶48-50). Adesida, Fig. 5, [0031]. **Gate 190 (gate electrode)** is formed as a **Schottky barrier contact (Schottky contact)** on the **In_{0.52}Al_{0.48}As barrier layer 150 (group III-V semiconductor device)**. Adesida, Fig. 5 and [0031]. Zhao ¶198.

Consistent with the '562 patent, Adesida discloses **gate 190 (gate electrode)** formed as a **Schottky barrier contact (Schottky contact)** on the group III-V

device and **source 170** and **drain 180** (power electrodes) making ohmic contact with the group III-V device. Adesida, Fig. 5 and [0031].

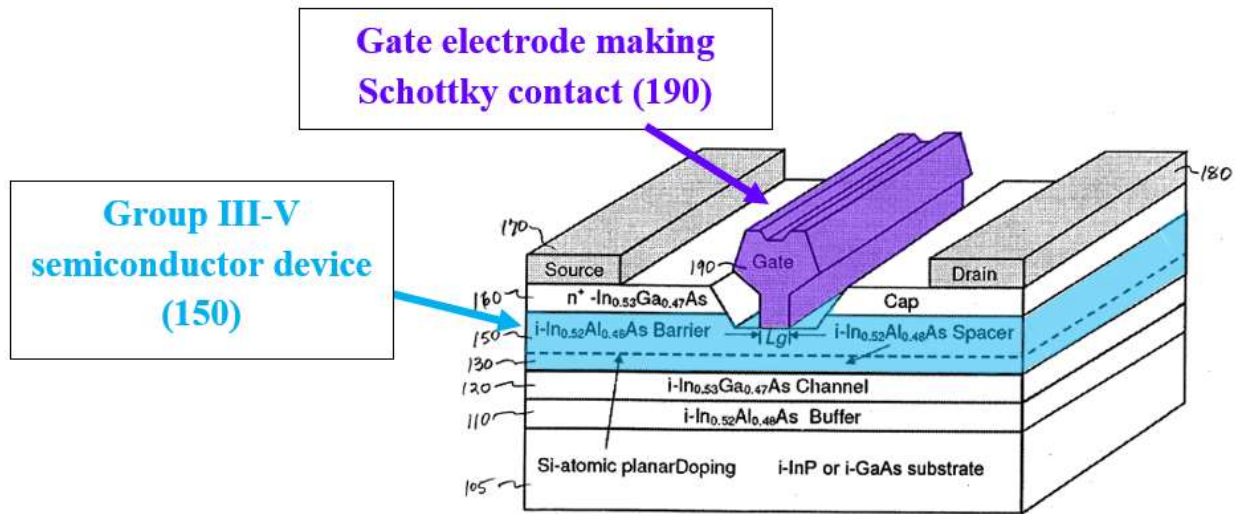


Figure 5

Adesida, Fig. 5 (annotated); Zhao ¶199.

4. **Claim 14 – The electrical contact of claim 13, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).**

Claim 14 is identical to claim 9, but depends from claim 13. Claim 14 is obvious as explained for claim 9. Zhao ¶200.

5. **Claim 16 – The electrical contact of claim 13, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.**

Claim 16 is identical to claim 11, but depends from claim 13. Claim 16 is obvious as explained for claim 11. Zhao ¶201.

G. Ground 7: Yu in view of Usui and Sugimoto Render Obvious Claims 10 and 15

1. Overview of the Combination and Motivation to Combine

Yu and Usui do not expressly disclose that their group III-V devices have a power electrode making an ohmic electrical contact. Zhao ¶202.

Like Yu, Sugimoto discloses a group III-V semiconductor device (Sugimoto, 9:7-9) with an AlGa_N top layer. Sugimoto, Figs. 1, 3, 5, 7. AlGa_N is a well-known group III-V material. Zhao ¶¶48-50. Sugimoto further discloses the III-V semiconductor device is a HEMT. Sugimoto, 1:22-67. Zhao ¶203.

The '562 patent defines “[s]ource electrode 136 and drain electrode 138 are power electrodes ohmically coupled to the heterojunction formed by Ga_N layer 112 and AlGa_N layer 114.” ’562 patent, 3:19-21. Consistent with the ’562 patent, Sugimoto discloses a gate electrode making Schottky contact with a group III-V device and power electrodes (source and drain electrodes) making ohmic contact with the group III-V device. Sugimoto, 9:39-51. Sugimoto discloses that its “**drain electrode 42 and the source electrode 46 make ohmic contact with the top surface of the AlGa_N layer 34.**” Sugimoto, 9:39-51. Zhao ¶204.

By August 2009, Dr. Zhao explains that it was well-known that ohmic contacts are of critical importance with respect to device functionality, performance, and long-term reliability. Zhao ¶55 (citing Ex-1013, 144). It was well-known that ohmic contacts serve as source and drain contacts in group III-V

devices and allow current to flow into and out of a semiconductor material without distortion of the signal. Zhao ¶57 (citing Ex-1016, 22; Ex-1017, 1). It was well-known that the most critical component of an ohmic contact is its low specific contact resistance, which minimizes the power consumption of the contact and the internal heating of the contact, thereby prolonging device operation with predictable performance. Zhao ¶57, 205 (citing Ex-1016, 22).

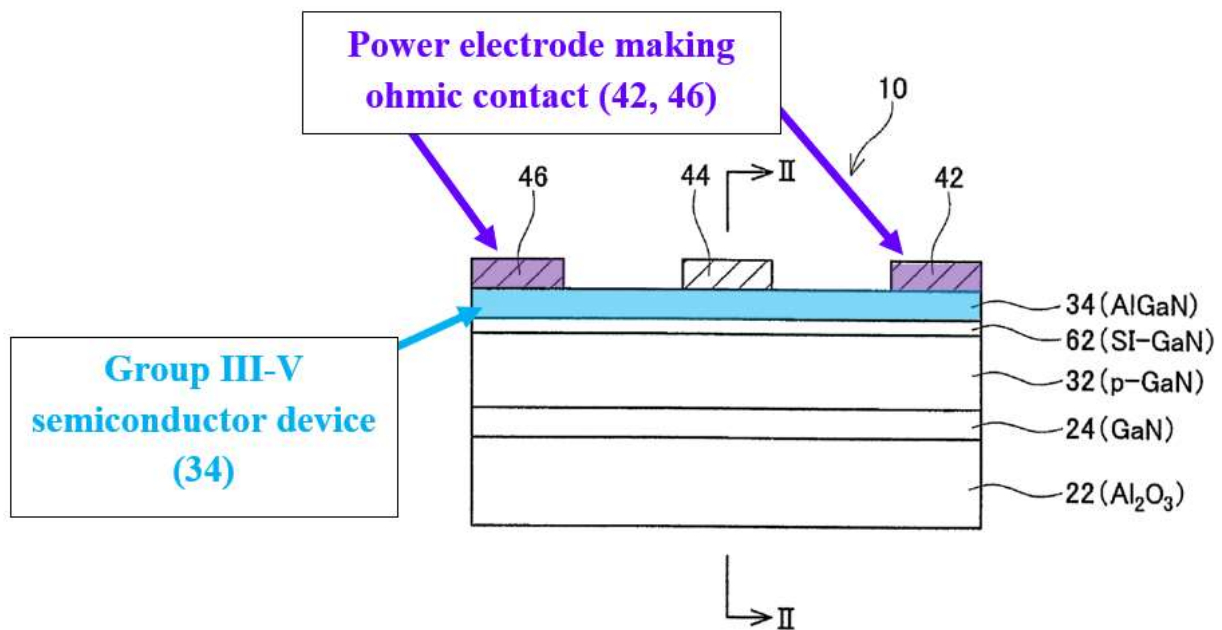
Yu disclosed the importance of an improved work function and thermal stability. Yu, Abstract. A POSITA would have been motivated to implement the devices of Yu and Yu-Usui with a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide reduced internal heating of the contact and improved current flow (i.e., improved work function values). Furthermore, such a combination is the result of combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 416-17; *Adesida*, [0031], Fig. 5; Zhao ¶¶51-57, 206).

2. Claim 10 – The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.

Yu in view of Usui and Sugimoto render obvious claim 10 because Sugimoto discloses a device with a power electrode making an ohmic contact, and

it would have been obvious to implement Yu or Yu-Usui's group III-V semiconductor devices with power electrodes making ohmic contacts (explained in Section VII.G.1). Zhao ¶¶55-57, 207.

Sugimoto discloses that its “**drain electrode 42 (power electrode)** and the **source electrode 46 (power electrode)** make **ohmic contact** with the top surface of the **AlGaN layer 34 (group III-V semiconductor device)**.” Sugimoto, 9:39-51.



Sugimoto, Fig. 1 (annotated); Zhao ¶208.

3. **Claim 15 – The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.**

Claim 15 is identical to claim 10, but depends from claim 13. Claim 15 is obvious as explained for claim 10. Zhao ¶209.

VIII. DISCRETIONARY DENIAL IS NOT WARRANTED

A. *Fintiv* Denial Is Improper

In view of the Office’s interim guidance dated June 21, 2022 (“*Interim Procedures*”), *Fintiv* does not apply. The Interim Procedures state “the PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding,” so the parallel ITC Investigation does not implicate *Fintiv*. *Interim Procedures*, 7.

The *Fintiv* factors in view of the parallel district court action weigh strongly in favor of institution because the district court case has minimal investment from the Court or Parties, does not have a trial date, and has been stayed. *Infineon Techs. Austria AG v. Innoscience (Suzhou) Tech. Co., Ltd. et al.*, No. 3:24-cv-01553, (N.D. Cal. March 13, 2024) (Ex. 1033).

B. 35 U.S.C. §325(d) Denial Is Improper

The factors in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8, 17-18 (PTAB Dec. 15, 2017) and *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, 8-11 (PTAB Feb. 13, 2020) (precedential) favor institution.

Advanced Bionics, step 1 (*BD* factors (a), (b), (d)) favor institution because none of the cited references were before the Office during prosecution, much less meaningfully addressed by the Office. Ex. 1034; Ex-1001, Cover.

Advanced Bionics, step 2, (*BD* factors (c), (e), (f)) favor institution because the cited references are not cumulative of those before the Office during prosecution because the references cited herein teach “an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers” and “said capping layer consisting only of a refractory metal nitride, said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers”—as the Applicant distinguished over the prior art to obtain allowance. Ex. 1034, 32-46, 56-68, 78-91, 98-109, 118-128, 138-144 (Oct. 8, 2013, Applicant Arguments/Remarks; April 17, 2013, Applicant Arguments/Remarks; September 24, 2012, Applicant Arguments/Remarks; August 23, 2012, Applicant Arguments/Remarks; March 7, 2012, Applicant Arguments/Remarks; September 26, 2011, Applicant Arguments/Remarks).

IX. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party-in-Interest

The real parties-in-interest are Innoscience America, Inc.; Innoscience (Zhuhai) Technology Company, Ltd.; and Innoscience (Suzhou) Technology Holding Company, Ltd.

B. Related Matters

To the best of Petitioner's knowledge, the '562 patent is involved in:

Name	Number	Forum	Filed
<i>Infineon Techs. Austria AG v. Innoscience (Suzhou) Tech. Co., Ltd. et al.</i>	3:24-cv-01553	N.D. Cal.	March 13, 2024
<i>In re Certain Semiconductor Devices and Products Containing the Same</i>	337-TA-1414	ITC	July 26, 2024

C. Lead and Backup Counsel Information

Petitioner provides the following designation of counsel:

Lead Counsel	Back-Up Counsel
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Petitioners consent to electronic service at the following email address:

Innoscence-Infineon-IPRs@finnegan.com.

D. Standing

The '562 patent is available for IPR. Petitioner is not barred or estopped.

X. CONCLUSION

Petitioner requests the Board institute this IPR and find all claims unpatentable.

Dated: November 18, 2024

By: /Lionel M. Lavenue/
Lionel M. Lavenue, Lead Counsel
Reg. No. 46,859

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), the undersigned hereby certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,686,562 contains 12,595 words, excluding parts of this Petition exempted under § 42.24(a), as measured by the word-processing system used to prepare this paper.

Dated: November 18, 2024

By: /Lionel M. Lavenue/
Lionel M. Lavenue, Lead Counsel
Reg. No. 46,859

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing **Petition for *Inter Partes* Review of U.S. Patent No. 8,686,562, Power of Attorney, and Exhibits 1001 through 1036** were served on November 18, 2024, by FedEx Priority Overnight, on the following correspondence address of record indicated in the Patent Office's Patent Center website for the '562 patent:

Michael Farjami
FARJAMI & FARJAMI LLP
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Mission Viejo, California 92691

Dated: November 18, 2024

By: /Lisa C. Hines
Lisa C. Hines
Case Manager
Finnegan, Henderson, Farabow,
Garrett & Dunner, L.L.P