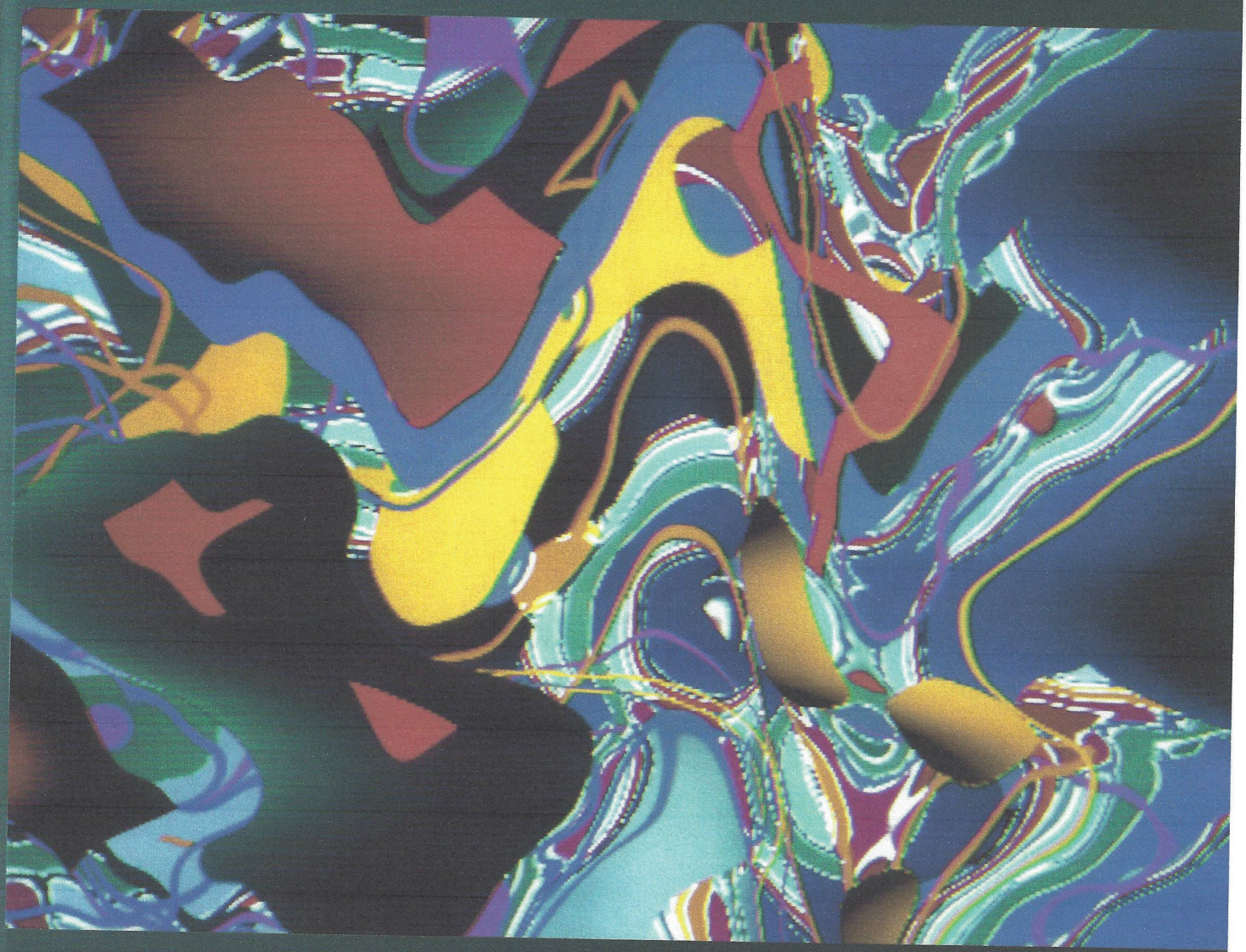
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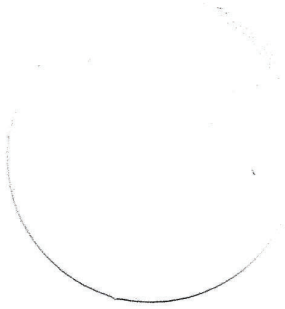
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SEMICONDUCTOR MANUFACTURING TECHNOLOGY

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ADVANCED MICRO DEVICES



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CHAPTER 10

OXIDATION

A cornerstone of silicon IC wafer fabrication is the ability to thermally grow an oxide layer on the surface of a silicon wafer. A major development from the 1950s was *oxide masking*, which patterned and etched openings in a thermally grown oxide layer to diffuse dopants into the silicon substrate. This development was a key factor in developing a process to fabricate large quantities of transistors.[1] In this way, oxidation played a major role in the development of silicon planar technology and remains viable today, which explains the widespread usage of silicon in wafer fabrication.

With the proper manufacturing control, oxide layers have high quality, stability, and desirable dielectric properties. Because of these qualities, oxidation is critical, especially for the thin oxide that is an essential part of the gate structure for MOS technology. Thermal oxide is used as a dielectric material, as well as for device isolation, oxide screens for implants, stress-relief oxides (pad oxides), and reoxidizing nitride and polysilicon surfaces for photoresist adhesion and stress reduction.

Oxides can be either deposited or grown. The focus in this chapter will be on thermally grown oxides. We will review the nature of oxide films and how they are grown, including detailed information on the growth mechanism and the high-temperature chamber where growth occurs.

OBJECTIVES

After studying the material in this chapter, you will be able to:

1. Describe an oxide film for semiconductor manufacturing, including its atomic structure, its various uses, and its benefits.
2. State the chemical reaction for oxidation, and describe how oxide grows on silicon.
3. Explain selective oxidation and give two examples.
4. Identify the three types of thermal processing equipment, describe the five parts of a vertical furnace, and discuss the attributes of a fast ramp vertical furnace.
5. Explain what is a rapid thermal processor, its usage and design.
6. Describe the critical aspects of the oxidation process, including its quality measures and some common troubleshooting problems.

INTRODUCTION

Oxide on a silicon wafer is created by either the grown or deposited method. A *grown oxide layer* occurs on a wafer by providing externally supplied high-purity oxygen in an elevated-temperature environment to react with the silicon substrate. The high-temperature oxidation process occurs in the diffusion area of the wafer fab. This is the first process area when a silicon wafer enters the fabrication process (see Figure 10.1 on page 226). A *deposited oxide layer* is generated by using an external silicon source and O_2 and reacting these materials in a chamber to form a thin film on the wafer surface. This chapter will cover the basic technology of oxidation and explain the high-temperature process of thermal oxidation. Chapter 11 will cover the deposition of oxide and other materials.

Since a silicon wafer is a flat surface (planar), oxide is grown or deposited essentially as a layer. Because of this, it is referred to as a *thin film*. Once a layer is on the wafer surface, it is then modified during subsequent processing to attain the necessary three-dimensional shape used in the formation of circuit components, such as a trench capacitor or gate oxide. This modification produces three-dimensional shapes on the wafer surface referred to as *topography* or *surface topology*.

Oxide growth is a natural phenomenon that occurs by exposing the silicon wafer to oxygen at an elevated temperature. The ability to grow an oxide film on silicon is often listed as a significant reason for the use of silicon as the most common semiconductor substrate material (another major reason is silicon's relatively high melting temperature). We use the term "grow" to indicate that temperature is used to cause the oxide to grow out of the silicon semiconductor material, actually consuming silicon in the process.

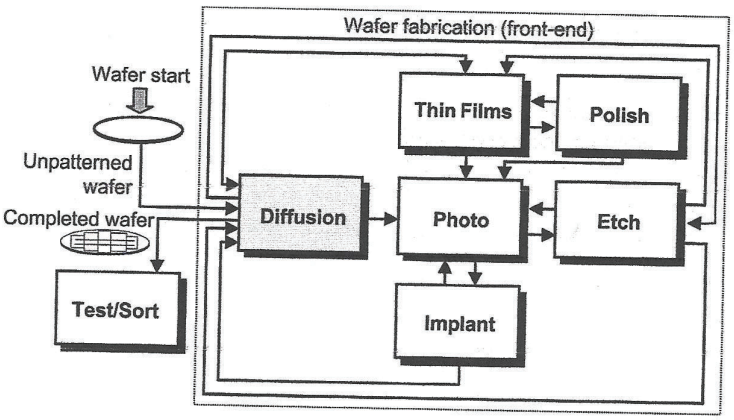


FIGURE 10.1 Diffusion Area of Wafer Fabrication
(Used with permission from Advanced Micro Devices)

The amount of thermal exposure (i.e., temperature multiplied by time) for a wafer during processing is referred to as the *thermal budget.* The thermal budget requirement for wafer fabrication is rapidly dropping.[2] A goal throughout semiconductor processing is to minimize the amount of thermal (heat) exposure to the wafer. As the critical dimension on device structures decreases to 0.18 μm and beyond, scaling requirements dictate shallower junction depths. To minimize the unacceptable diffusion of dopants out of a shallow junction region, the thermal budget must decrease accordingly. Another problem caused by excessive thermal budget is the increase in ohmic contact resistance of metal-layer interconnects (see Chapter 12), which increases the overall resistance of the conductive paths. A factor in determining the process conditions for many wafer fabrication process steps is the ability to minimize the thermal budget, either by reduced temperature or by minimizing the time at temperature.

OXIDE FILM

An oxide layer is grown on silicon typically at thermal oxidation temperatures between 750°C to 1100°C. An oxide layer grown on silicon is referred to as *thermal oxide* or *thermal silicon dioxide* (SiO_2). Since silicon dioxide is an oxide material, the two terms are used interchangeably. Another term for silicon dioxide is *glass*. Silicon dioxide is a dielectric material and will not conduct electricity.

Nature of Oxide Film

When a silicon surface is exposed to oxygen, an amorphous silicon dioxide film grows immediately. Although undoped silicon is a semiconductor material, SiO_2 is an insulator. The atomic structure of this SiO_2 film consists of a silicon atom surrounded by four oxygen atoms (see Figure 10.2). We can refer to this atomic structure as a silicon dioxide *tetrahedron cell.* Amorphous SiO_2 has no long-range periodic crystal order at the atomic level. Long-range order is absent because the tetrahedra are not arranged in a regular, three-dimensional array as in a crystal.[3]

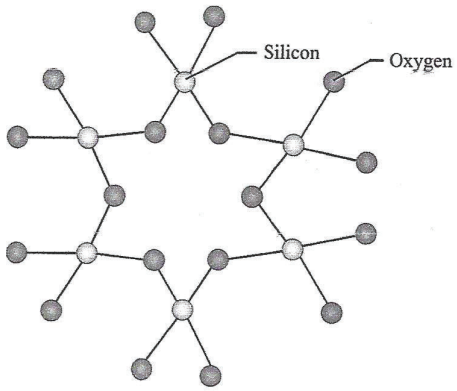


FIGURE 10.2 Atomic Structure of Silicon Dioxide
(Used with permission from International SEMATECH)

Silicon dioxide is a form of intrinsic (pure) glass with a melting temperature of 1732°C.[4] Thermally grown SiO_2 has strong adhesion to silicon and exhibits excellent dielectric properties. A layer of SiO_2 always covers the wafer surface because silicon oxidizes immediately upon exposure to air with a few monolayers of native oxide (a monolayer is one layer of atoms on a surface). Over time, the native oxide layer will thicken to an upper limit of about 40 Å, even at 25°C room temperature.[5] This type of oxide is nonuniform and usually considered a contaminant, with little use in semiconductor fabrication. There are some applications for use of native oxide in wafer fabrication, such as part of a dielectric film stack in memory cells. Native oxide grown from air is contaminated, but native oxide grown in chemical baths using high-purity chemicals is very clean.

Uses of Oxide Film

Oxide is important for silicon semiconductor fabrication because of its ease of formation and its excellent interface with the underlying silicon material. It is the most common layer used in semiconductor fabrication. Different ways in which an oxide layer is used to fabricate a microchip are:

- Device scratch protection and contaminant isolation
- Field isolation to confine charged carriers (termed surface passivation)
- Dielectric material in the gate oxide or memory cell structures
- Impurity-mask barrier during doping
- Dielectric layer between metal conductor layers

Device Protection and Isolation ■ Silicon dioxide grown on the surface of the wafer serves as an effective barrier to isolate and protect sensitive devices in the silicon. SiO_2 physically protects devices because it is a very hard and nonporous (dense) material that effectively insulates active devices in the silicon surface. The hard SiO_2 layer will protect the silicon from scratches and processing damage that might occur during fabrication. Transistors have traditionally been electrically isolated by thermally growing thick SiO_2 in the region between them using the LOCOS process (discussed later in this chapter). However, this process is unacceptable for sub-0.25 μm technology and has been replaced by shallow trench isolation (STI). The STI process uses deposited oxide as the main dielectric (see Chapters 9 and 11).

Surface Passivation ■ A major benefit from thermally grown SiO_2 is the reduction in the surface-state density of silicon that occurs by tying up dangling silicon bonds. This action is referred to as *surface passivation,* which prevents the deterioration of the electronic properties and reduces current-leakage paths of the semiconductor caused by moisture, ions or other external contaminants.[6] The hard SiO_2 layer will protect the silicon from scratches and processing damage that might occur during backend final fabrication. SiO_2 growth on the silicon surface can serve to tie up electrically active contaminants (mobile ionic contaminants) in the oxide layer away from the active surface of the silicon. Passivation is also important for controlling the leakage current of

junction devices and growing a stable gate oxide.[7] For the oxide layer to function as a good passivation layer, it has a quality requirement to be a uniform thickness and not have pinholes or voids in the material.

Another factor in using the oxide layer to passify the wafer surface is the oxide thickness. Adequate oxide thickness is necessary to prevent electrical charging in a metal layer caused by a charge buildup in the silicon wafer surface, much like charge storage and breakdown characteristics of ordinary capacitors. This charging would lead to electrical shorting and other undesirable electrical effects. A thick layer of oxide that inhibits charge buildup from metal layers is the *field oxide layer,* which typically is between 2,500 Å to 15,000 Å thick (see Figure 10.3).

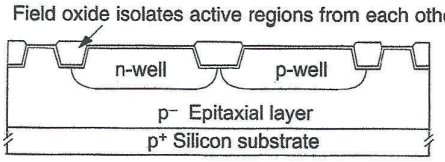


FIGURE 10.3 Field Oxide Layer

Silicon dioxide also has a coefficient of thermal expansion very similar to that of silicon. During high-temperature processing, the wafer will expand and then contract during cooling. The SiO_2 will expand and contract at close to the same rate as silicon, thus minimizing wafer warpage during the thermal excursions. This action also prevents film stress from separating the oxide film from the silicon substrate.

Gate Oxide Dielectric ■ An extremely thin layer of oxide is used as the dielectric material for the important *gate oxide structure* common in MOS technology (see Figure 10.4). The gate oxide is thermally grown because of its high quality and stability with the underlying semiconductor silicon. SiO_2 has a high dielectric strength of 10^7 volts/cm and high resistivity of approximately 10^{17} ohms-cm.[8]

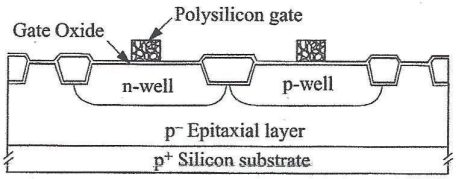


FIGURE 10.4 Gate Oxide Dielectric

The thickness of the gate oxide is chosen specifically for the scaling requirements of the device technology. For 0.18-μm generation technology, a typical gate oxide thickness is 20 ± 1.5 Å. The gate oxide has a specific thickness so that it scales properly with the entire gate structure to permit induction of a charge in the silicon wafer under the oxide. The widespread use of MOS technology in the ULSI era has made the formation of the gate oxide a primary concern in process development. A critical aspect of device reliability is *gate oxide integrity.* The gate structure in a MOS device is the part that controls the flow of electrical current through the device. Because this oxide is fundamental to the proper function of microchips based on field-effect technology, it is essential that it have high quality, with excellent film-thickness uniformity and no contaminants. Any contamination that degrades the proper functioning (integrity) of the gate oxide structure must be scrupulously controlled.

Dopant Barrier ■ Silicon dioxide can be used as an effective barrier to selectively introduce dopants into the silicon surface (see Figure 10.5). Once an oxide layer is grown on the silicon surface, then mask openings are etched into the SiO_2 to create windows where dopant materials can enter the wafer. The oxide protects the surface of silicon from impurity diffusion where there are

no openings and therefore allows selective impurity doping. Dopants have a slow rate of movement through SiO_2 when compared to silicon, requiring only a thin oxide layer to block dopants (note that this rate is temperature dependent).

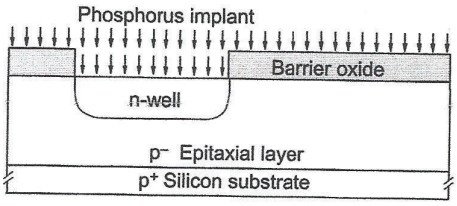


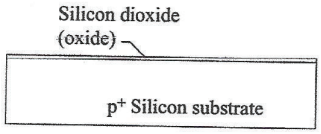
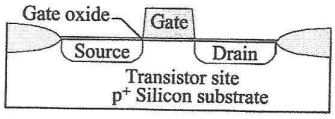
FIGURE 10.5 Oxide Layer Dopant Barrier

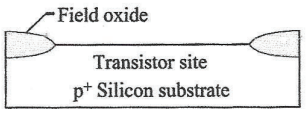
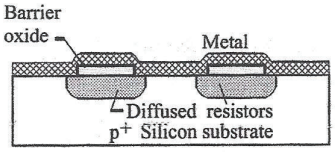
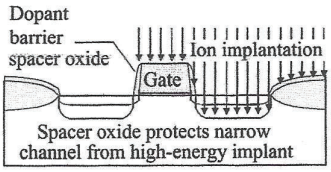
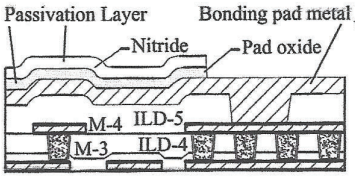
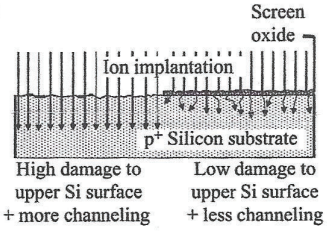
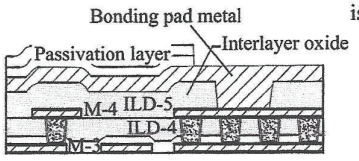
A thin oxide layer (e.g., 150 Å) is also grown in areas where ion implant occurs. This oxide screen serves to reduce damage to the silicon wafer and obtain better control over the depth that the dopant is implanted into the silicon by reducing channeling effects (see Chapter 17). Once implantation is done, HF (hydrofluoric acid) can be used to selectively remove the oxide, resulting in a planar silicon surface again.

Dielectric Between Metal Layers ■ Under normal conditions, silicon dioxide will not conduct electricity. For this reason, SiO_2 is an effective insulator between metal layers on the microchip. Silicon dioxide prevents shorting of an upper metal layer to the underlying metal layer, just as the insulator material on an electrical cord prevents an electrical short. The oxide quality is critical with no holes or voids allowed. This oxide is often doped to produce more effective flow properties and to better minimize the diffusion of contaminants (i.e., it acts as a getter). It is typically deposited using chemical vapor deposition (not thermally grown) and will be covered in more detail in Chapter 11.

A summary of different types of oxides and their uses in semiconductor fabrication is shown in Table 10.1.[9]

TABLE 10.1 Oxide Applications

Application	Purpose	Structure	Comments
Native Oxide	This oxide is a contaminant and is generally undesirable. Sometimes used in memory storage or film passivation.		Growth rate at room temperature is 15 Å per hour up to a maximum thickness of about 40 Å.
Gate Oxide	Serves as a dielectric between the gate and source-drain parts of MOS transistor.		Common gate oxide film thickness range from about 20 Å to several hundred Å. Dry thermal oxidation is the preferred growth method.

Application	Purpose	Structure	Comments
Field Oxide	Serves as an isolation barrier between individual transistors to isolate them from each other.		Common field oxide film thickness ranges from 2,500 Å to 15,000 Å. Wet oxidation is the preferred growth method.
Barrier Oxide	Protects active devices and silicon from follow-on processing.		Thermally grown to several hundred angstroms thickness.
Dopant Barrier	Masking material for depositing or implanting dopants into wafer.		Dopants diffuse into unmasked areas of silicon by selective diffusion.
Pad Oxide	Provides stress reduction for silicon nitride (Si_3N_4).		Thermally grown and very thin.
Implant Screen Oxide	Used to reduce implant channeling and damage.		Thermally grown.
Insulating Barrier Between Metal Layers	Serves as a protective layer between metal lines.		This oxide is not thermally grown, but is deposited.