

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AMERICAS CORP.,
Patent Owner.

Case No. IPR2025-00175
Patent No. 8,686,562

PATENT OWNER'S PRELIMINARY RESPONSE

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37 C.F.R. § 42.104	13, 15, 34
37 C.F.R. § 42.22	14, 15, 36
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LISTING OF EXHIBITS

Exhibit	Description
2001	Excerpts from Merriam Webster's Collegiate Dictionary (10th ed.) (2001)
2002	U.S. Patent Application Publication No. 2008/0251828 A1 ("Meng")
2003	U.S. Patent Application Publication No. 2011/0247549 A1 ("Sachs")
2004	Quirk, M., & Serda, J. (2001) Semiconductor Manufacturing Technology. Prentice Hall.
2005	Stewart, C.M., "Interim Processes for PTAB Workload Management," Memorandum dated March 26, 2025

I. INTRODUCTION

Institution should be denied on the merits¹ because the Petition fails to carry Petitioner's burden to demonstrate that any Challenged Claim (claims 1-17) in U.S. Patent No. 8,686,562 ("the '562 Patent") is unpatentable.

Every Challenged Claim is directed to an electrical contact for use on a semiconductor device. The electrical contact comprises "an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers." The capping layer has "a thickness greater than that of a bottommost layer of said plurality of metal layers" of the electrode stack.

The Petition presents two sets of grounds. Grounds 1-4 (the "Usui-based grounds") rely on Usui to meet the above-discussed limitations relating to an electrode stack. Grounds 5-7 (the "Yu-based grounds") rely on Yu to meet the claimed electrode stack. But neither Usui nor Yu teaches the claimed electrode stack comprising a capping layer that is formed over a plurality of metal layers and

¹ The '562 Patent is the subject of a parallel ITC Investigation No. 337-TA-1414, involving Petitioner and Patent Owner. Pursuant to the Interim Processes for PTAB Workload Management Memorandum issued on March 26, 2025, "the patent owner may submit discretionary denial briefing within one month of the date of this memorandum." EX-2005, 3.

has a thickness greater than that of a bottommost layer of the plurality of metal layers.

A. Petitioner Fails to Explain its Construction of “Electrode Stack”

The Petition alleges that all claim terms should be given their plain meaning. But the Petition never explains what plain meaning Petitioner ascribes to “electrode stack.” Petitioner simply alleges in conclusory fashion that certain structures in Usui and Yu are “electrode stacks,” without ever explaining how or why that is allegedly so. That is reason enough why the Petition fails.

As the Federal Circuit explained *en banc* in *Phillips*, the specification is always highly relevant and usually dispositive in construing terms in a patent. Yet, Petitioner ignores the ’562 Patent’s teachings of what an “electrode stack” is. In the ’562 Patent, “electrode stack” refers to a stack of layers that form an “electrode.” Each electrode described in the ’562 Patent is either (1) a transistor source or drain electrode that makes electrical (ohmic) contact with a nonmetallic semiconductor part of the transistor, or (2) a transistor gate electrode that controls the flow of electrons between the transistor’s source and drain. The Petition does not even attempt to establish that any structure in Usui or Yu is an “electrode stack” as that term is used in the ’562 Patent. That should end the matter.

To the extent Petitioner suggests that “electrode stack” should be given some broader meaning divorced from the context of the ’562 Patent, Petitioner never

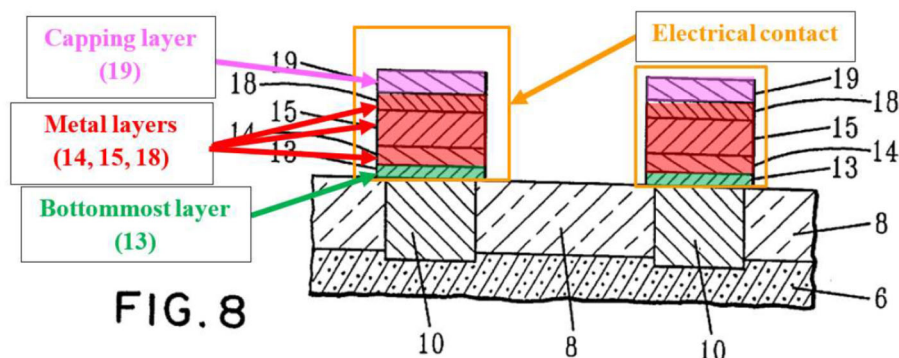
even attempts to establish what that broader meaning would be, let alone submit evidence to substantiate any (unexplained) broader meaning. Without conceding that dictionary definitions would be the proper way to interpret “electrode stack” rather than the intrinsic evidence, Infineon notes that the structures in Usui and Yu that Petitioner relies on do not meet even a broad dictionary definition of “electrode.” *See infra* § II.D.1 (citing a dictionary that defines an “electrode” as a conductor used to establish electrical contact with a nonmetallic part of a circuit, or an element in a semiconductor device (e.g., a transistor) that emits or collects electrons (or holes) or controls the movement of electrons (or holes) in the semiconductor device – and explaining that the structures Petitioner relies on in Usui and Yu do not meet either definition).

Petitioner fails to give “electrode stack” its proper meaning. The prior art structures that Petitioner maps to the claimed “electrode stack” are not electrode stacks consistent with its usage in the ’562 Patent or even with a broad dictionary definition of “electrode.” That is fatal to all grounds.

B. Usui-Based Grounds 1-4 Fail

The Petition annotates Usui’s Fig. 8 as shown below and simply states that the five highlighted metal layers form an electrode stack. Based on that, Petitioner alleges that Usui discloses an electrode stack with a bottommost layer 13 that is thinner than a capping layer 19. As discussed *infra* §§ II-III, Petitioner’s assertion

fails because the Petition never establishes that the relied-upon layers in Usui form an electrode stack.



Petitioner's Annotations to Usui, Fig. 8

The Petition provides no claim construction analysis and cites no intrinsic or extrinsic evidence establishing what, according to Petitioner, the alleged plain meaning of “electrode stack” is. The Petition also never explains how or why the five-layer Usui structure that Petitioner relies upon is an electrode stack. The Petition merely points to Usui Fig. 8 and states in conclusory fashion that these layers form an electrode stack, despite Usui never characterizing this structure in that way.

The Petition is required by statute to state its grounds with particularity. The Board's rules require that the Petition identify how the claim is to be construed and provide a detailed explanation of how and why the evidence establishes that the prior art meets the construed claim. The Petition fails to meet any of these requirements for the claimed “electrode stack.” The Usui-based grounds fail for that reason alone.

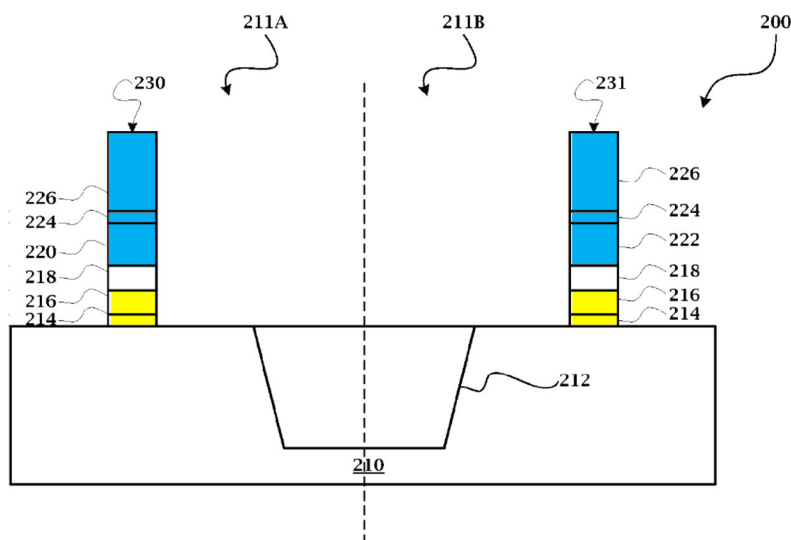
The Usui-based grounds also fail because the Petition does not cite a single piece of *evidence* that supports its conclusory assertion that the identified five-layer Usui structure is an electrode stack. The expert declaration cannot and does not save Petitioner because it does nothing more than repeat the Petition’s conclusory assertions word-for-word.

The Petition’s above-discussed failures are far from inconsequential. The 5-layer Usui structure that Petitioner identifies as an electrode stack is referred to by Usui as an “interconnect metallization” structure. Usui’s interconnect metallization structure does not establish electrical contact with a nonmetallic part of a circuit. Instead, it is connected to a *metal* interplanar stud connection 10 that in turn connects to nonmetallic semiconductor material in Usui. Petitioner never alleges that the metal stud 10 is the bottommost metal layer of an electrode stack. Perhaps that is because Usui Fig. 8 depicts the metal stud 10 as far thicker than the capping layer. If metal stud 10 were the bottommost metal layer of an electrode stack, then Usui Fig. 8 discloses a capping layer that is thinner – not thicker as required by every Challenged Claim – than that bottommost metal layer.

Petitioner fails to establish that Usui discloses “an electrode stack” having a capping layer with “a thickness greater than that of a bottommost layer of said plurality of metal layers” of the electrode stack as required by every Challenged Claim. That is fatal to the Usui-based grounds.

C. Yu-Based Grounds 5-7 Fail

Yu discloses a CMOS device with two metal gate stacks 230 and 231 as shown in Yu's Fig. 2E annotated below. Each metal gate stack has metal layers that form an electrode (highlighted blue), insulating oxide layers (highlighted yellow) and a diffusion barrier/protection layer 218 that separates the gate electrode from the oxide layers to prevent the materials in the gate electrode and the oxide layers from diffusing into each other.

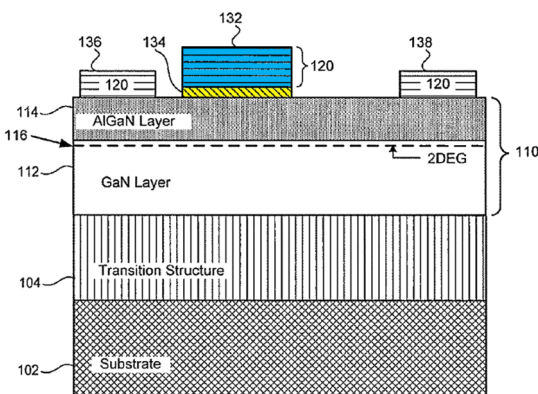


Yu, Fig. 2E (annotated)

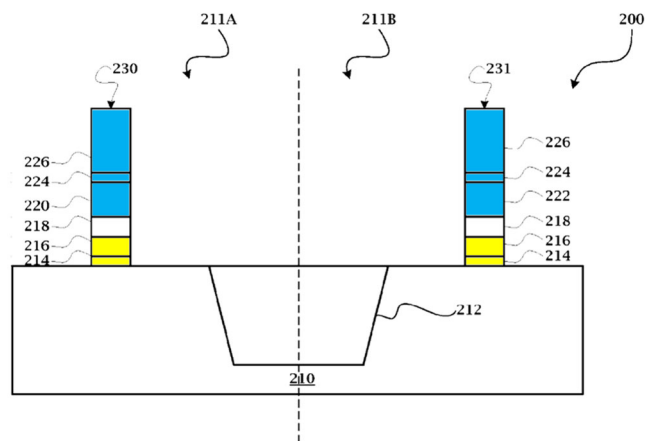
Petitioner alleges that the diffusion barrier/protection layer 218 is the bottommost metal layer of an electrode stack. But as discussed *infra* §§ IV-V, nothing supports that assertion. As with the Usui-based grounds, the Petition never explains what Petitioner contends is the alleged plain meaning of “electrode stack” and cites no *evidence* to support its assertion that diffusion barrier/protection layer 218 is part of Yu’s electrode and thus part of Yu’s “electrode stack.”

The Petition does nothing more than use a parenthetical to equate Yu's *entire* metal gate stack (230 or 231) with the claimed electrode stack. Petition, 42 (“metal gate stacks 230, 231 (electrode stacks)”). Petitioner provides no analysis and cites no *evidence* to support the assertion that the *entire* metal gate stack (230 or 231) is an electrode stack.

Worse yet, Petitioner's assertion that the claimed “electrode stack” includes Yu's entire metal gate stack is directly refuted by the intrinsic evidence. As illustrated below, the '562 Patent (below left) discloses a gate electrode 132 (highlighted blue) stacked with a gate insulating layer 134 (highlighted yellow).



'562 Patent, Fig. 1 (annotated)



Yu, Fig. 2E (annotated)

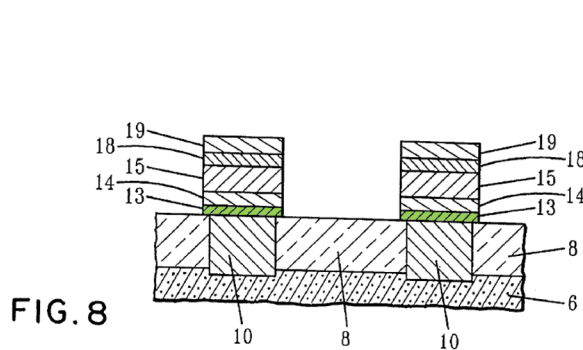
The '562 Patent is explicit that the “electrode stack 120” comprises only the metal layers that form the gate electrode and does *not* include the gate insulating layer 134 that is stacked with the gate electrode. This directly refutes Petitioner's assertion that Yu's *entire* metal gate stack (including insulating layers 214 and

216) is an “electrode stack” as claimed. The Yu-based grounds fail because Petitioner fails to establish that Yu’s diffusion barrier/protection layer 218 – which Petitioner alleges is the bottommost layer of the plurality of metal layers of Yu’s electrode stack – is even part of Yu’s electrode stack.

The Yu-based grounds also fail even if Yu’s diffusion barrier/protection layer 218 is considered to be the bottommost metal layer in Yu’s electrode stack (it is not), because Petitioner fails to establish that its Yu-USUI combination has a capping layer formed from a refractory metal nitride that is thicker than this alleged bottommost metal layer as required by every Challenged Claim.

Yu discloses capping layers formed from various materials but *does not* report a thickness for the capping layer when formed from a refractory metal nitride. Absent such a teaching, Petitioner relies on Yu’s thickness for a polysilicon capping layer and alleges in conclusory fashion that a POSA would have used the same thickness when the capping layer is instead formed from a refractory metal nitride. Nothing supports that assertion. Petitioner offers no reason why a POSA would have chosen the same thickness and cites no *evidence* supporting that assertion. That is particularly problematic because Yu teaches that the preferred thickness for the capping layer can vary by as much as three times depending on the material used.

Recognizing the deficiencies in Yu's failure to disclose the claimed relative thickness between a refractory metal nitride capping layer and the electrode stack's bottommost metal layer, Petitioner also alleges that Usui would have motivated a POSA to make Yu's diffusion barrier/protection layer 218 thinner than Yu's refractory metal nitride capping layer. Nothing supports that assertion. Petitioner seizes on Usui's disclosure of the benefits of controlling thickness for the bottommost layer 13 of Usui's "interconnect metallization" structure that is an interconnection for Usui's metal stud 10 as shown in Usui Fig. 8 below. Petitioner's assertion that this would have motivated a POSA to control the thickness of the diffusion barrier/protection layer 218 in Yu's gate electrode – which serves a different purpose in a different type of structure – is entirely unsupported. The Yu-based grounds fail for this additional reason.



Usui, Fig. 8 (annotated)

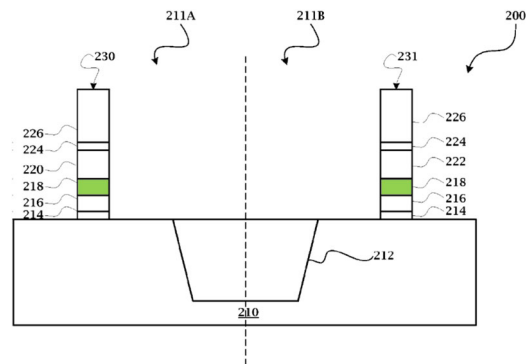


FIG. 2E

Yu, Fig. 2E (annotated)

* * *

As detailed below, Petitioner fails to carry its burden of demonstrating a reasonable likelihood of proving any Challenged Claim unpatentable. Institution should be denied.

II. GROUND 1 FAILS BECAUSE PETITIONER FAILS TO ESTABLISH THAT USUI’S INTERCONNECT METALLIZATION STRUCTURE IS AN ELECTRODE STACK AS CLAIMED

Ground 1 alleges that independent claim 1 and dependent claims 2 and 4-7 are anticipated by Usui. Petition, 3, 8-16.

Independent claim 1 is directed to an electrical contact for use on a semiconductor device. *See* Limitation [1pre].² The electrical contact comprises “an *electrode stack*”³ including a plurality of metal layers and a capping layer formed over said plurality of metal layers.” *See* Limitation [1a]. The capping layer has “a thickness greater than that of a bottommost layer of said plurality of metal layers” of the electrode stack. *See* Limitation [1c].

Other than repeating the claim language and alleging that Usui “discloses” what Limitation [1a] requires, *the Petition entirely ignores the requirement of an “electrode stack.”* Petition, 11-12. The Petition never construes the term “electrode stack,” never explains what an “electrode” or “electrode stack” is, and

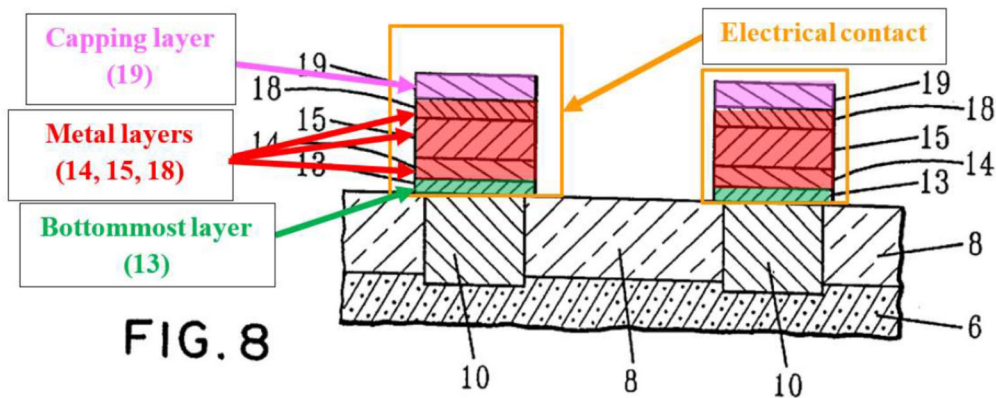
² Patent Owner herein adopts the Petition’s claim limitation labelling.

³ All emphasis is added unless otherwise indicated.

presents no evidence or argument to establish that the Usui structure the Petition identifies as meeting Limitation [1a] – Usui’s “interconnect metallurgy structure” (Usui, 3:23) – is an “*electrode* stack.” That is reason enough why Ground 1 fails.

Worse yet, Usui’s interconnect metallurgy structure is not an “electrode stack” as that term is used in the ’562 Patent or even under a broad dictionary definition of “electrode.” As shown from the Petition’s annotated FIG. 8 (reproduced below from the Petition, 11), Usui’s interconnect metallurgy structure is connected to “an interplanar stud connection 10,” which Usui says is a “device contact metallization” that “make[s] connection to a device substrate 6.” Usui, 3:24-27, 5:14-15.⁴ Petitioner never explains why, if there is an electrode in Usui FIG. 8 at all, the electrode is not the “device contact metallization 10” that “make[s] connection to a device substrate 6.” Usui, 3:24-27, 5:14-15.

⁴ Usui describes this structure in connection with FIG. 1 which is identical to FIG. 8. See Usui, 3:2-8 (FIG. 8 is the last of FIGs. 2-8 that illustrate the process for making FIG. 1’s device).



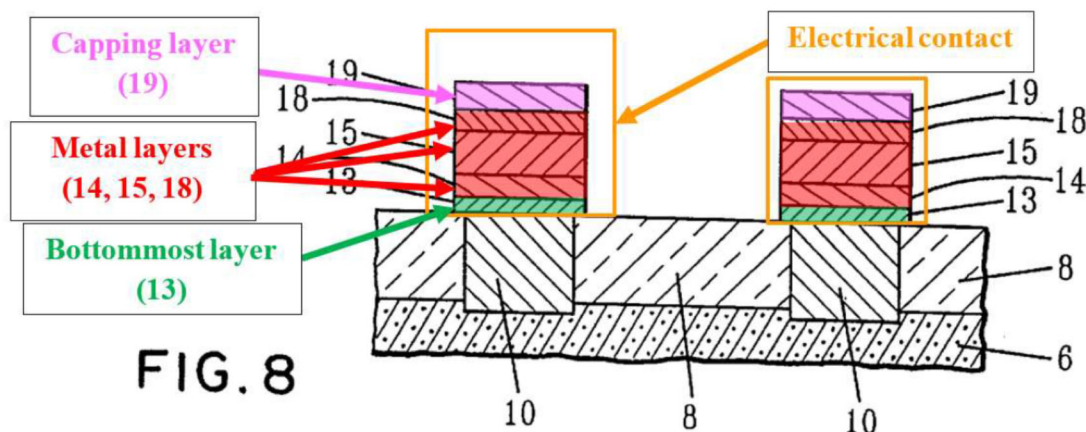
Petitioner's Annotations to Usui, Fig. 8

As detailed below, Ground 1 fails because Petitioner fails to establish that Usui's interconnect metallurgy structure is an electrode stack as claimed.

A. Petitioner Fails to Construe "Electrode Stack"

The Board's rules governing this proceeding include two rules that specify "Content" the Petition "must" have. *See* 37 C.F.R. §§ 42.22 and 42.104.

For each claim challenged, the Petition "***must***" identify "how the challenged claim is to be construed" and "[h]ow the ***construed*** claim is unpatentable." 37 C.F.R. § 42.104(b)(3)-(4). Petitioner's Claim Construction section alleges that "the plain meaning of each term can be applied." Petition, 7. But the Petition never explains what Petitioner alleges to be the "plain meaning" of "electrode" or "electrode stack." Instead, the Petition simply alleges in conclusory fashion that "Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metals." Petition, 11 (annotating Usui FIG. 8 as shown below).



Petitioner's Annotations to Usui, Fig. 8

It is not Patent Owner's burden to explain the proper construction of "electrode stack," or how and why Usui's interconnect metallization structure that Petitioner relies upon fails to meet it. Instead, it is Petitioner's burden to explain what the alleged "plain meaning" of "electrode stack" is (Petition, 7 and 11) and how and why Usui's interconnect metallization structure meets that plain meaning. 37 C.F.R. § 42.104(b)(3)-(4). The Petition fails to meet that burden.

This is reason enough why Ground 1 fails. The Petition fails to have the required ("must") content identifying "how the challenged claim is to be construed" and "[h]ow the *construed* claim is unpatentable." 37 C.F.R. § 42.104(b)(3)-(4).

B. No Evidence Supports Petitioner’s Assertion that Usui’s Interconnect Metallization Structure is an “Electrode Stack”

Limitation [1a] recites an “electrode stack.” Petitioner alleges that Usui’s interconnect metallization structure (layers 13-15 and 18-19) is an “electrode stack.” Petition, 11. The Petition never explains how or why that is allegedly so.

By statute, the Petition “*may only be considered if*” it identifies its grounds “with particularity.” 35 U.S.C. § 312(a)(3). To be considered, the Petition’s “content” “must include” a “detailed explanation of the significance of the evidence.” 37 C.F.R. § 42.22(a)(2). The Petition fails to meet these requirements. The Petition provides *no* explanation – let alone a “detailed” one – of how or why Usui’s “interconnect metallurgy structure” (layers 13-15 and 18-19) is allegedly an electrode stack as claimed. Usui, 3:23.

Worse yet, the Petition cites no *evidence* that supports its conclusory assertion that Usui’s interconnect metallization structure (layers 13-15 and 18-19) is an “electrode stack.” The Petition’s mapping of Limitation [1a] to Usui alleges that Usui’s interconnect metallization structure (layers 13-15 and 18-19) is an “electrode stack” only in its opening sentence, and that sentence only cites “Usui, Fig. 8; Zhao ¶89.” Petition, 11. But Usui Fig. 8 does not label Usui’s interconnect metallization structure (layers 13-15 and 18-19) an “electrode stack” or otherwise provide any support for Petitioner’s assertion that Usui’s interconnect metallization structure (layers 13-15 and 18-19) is an “electrode stack.”

The remainder of the Petition’s mapping of Limitation [1a] to Usui only cites additional disclosures in Usui for other reasons, e.g., to purportedly establish that layers 13-15 and 18 are metal and that capping layer 19 is titanium nitride. Petition, 11 (citing Usui, Fig. 1, 3:38-41, 3:58-60, 4:4-5, 5:38, 5:52, 5:54-59). None of the cited disclosures characterize Usui’s interconnect metallization structure (layers 13-15 and 18-19) as an electrode stack. And Petitioner never even alleges that they do.

The Petition does not cite a single piece of evidence establishing that Usui’s interconnect metallurgy structure is an electrode stack. Ground 1 fails for this additional reason.

C. The Expert Declaration Cannot and Does Not Save Petitioner

Nothing in the expert declaration can save Petitioner from the Petition’s failures to explain how “electrode stack” is to be construed, and how and why Usui’s interconnect metallization structure (layers 13-15 and 18-19) is purportedly an “electrode stack” as claimed. This is “content” that the *Petition* must have, and arguments cannot be incorporated by reference into the Petition from the expert declaration. 37 CFR §§ 42.22, 42.104(b)(3)-(4), and 42.6(a)(3); *Instrumentation Lab. Co., v. HemoSonics LLC*, IPR2017-00855, Paper 55 at 20 (Feb. 13, 2019) (citing 37 C.F.R. § 42.6(a)(3) and explaining: “Arguments and information that are not presented and developed in the Petition, but instead are incorporated by

reference, are not entitled to consideration, as it is improper to incorporate by reference arguments from one document into another document.”).

Even if the Board were to wade into the Zhao declaration, it does not remedy the Petition’s failures. The Petition’s purported mapping of Limitation [1a] to Usui cites Zhao ¶¶89-91. Petition, 11-12. Those paragraphs do ***nothing but repeat the Petition’s failed arguments word-for-word***. Compare Zhao ¶¶89-91 with Petition, 11-12. Like the Petition, Dr. Zhao never explains what the alleged plain meaning of “electrode stack” is and never explains how or why Usui’s interconnect metallization structure (layers 13-15 and 18-19) is an electrode stack. Dr. Zhao’s conclusory assertion that Usui’s metallization structure is an “electrode stack” as claimed is unsupported by any reasoned analysis or corroborating evidence, so it warrants no weight under the Board’s precedential *Xerox v. Bytemark*, IPR2022-00624, Paper 9, 15 (Aug. 24, 2022) (precedential) (“[T]he cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight.”); *see also id.* (quoting 37 C.F.R. § 42.65(a): “Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

D. Petitioner’s Assertion that Usui’s Interconnect Metallization Structure is an Electrode Stack is Inconsistent with the Intrinsic Evidence and Any Reasonable Meaning of Electrode

Despite bearing no burden in this proceeding, Patent Owner explains below that Petitioner’s assertion that Usui’s interconnect metallization structure (layers 13-15 and 18-19) is an “electrode stack” is inconsistent with how a POSA⁵ would have understood the term.

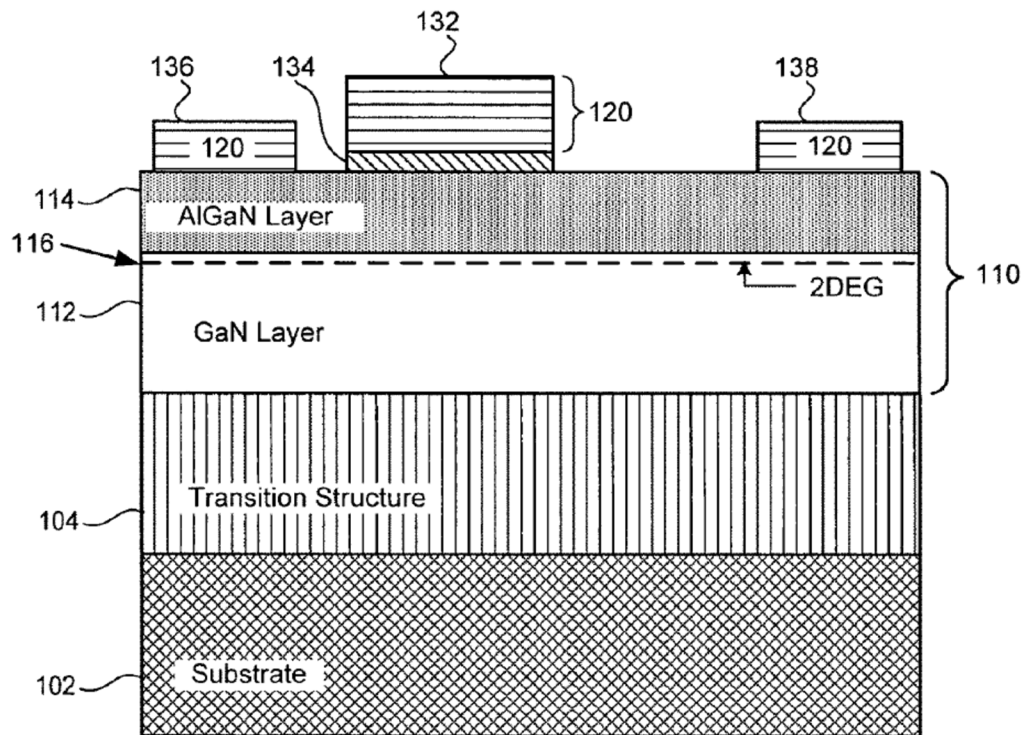
1. Petitioner Fails to Establish that Usui’s Interconnect Metallization Structure is an “Electrode Stack” as Described in the ’562 Patent

As the Federal Circuit re-emphasized *en banc* in *Phillips*, “the specification ‘is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (citing *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

The ’562 Patent specification describes source, drain, and gate electrodes for a transistor and illustrates these electrodes in Fig. 1, reproduced below. EX-1001, 2:58-60 (“Structure 100 also includes a plurality of electrical contacts including

⁵ For purpose of this Preliminary Patent Owner Response only, Patent Owner does not challenge the Petition’s POSA definition (Petition, 6) because the Petition fails even if Petitioner’s POSA definition is adopted.

source electrode 136, drain electrode 138, and insulated gate electrode 132.”), 3:19-35 (describing source electrode 136, drain electrode 138, and gate electrode 132). The semiconductor in Fig. 1 of the ’562 Patent is a compound semiconductor formed from gallium nitride (GaN) layer 112 and aluminum gallium nitride (AlGaN) layer 114. EX-1001, 1:7-15, 2:53-65.

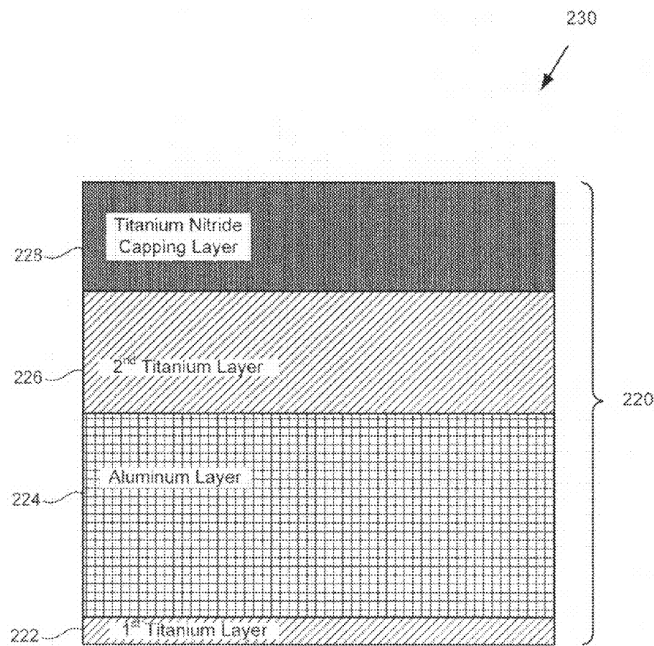


’562 Patent, Fig. 1

“Source electrode 136 and drain electrode 138” – each formed by an “electrode stack 120” – are “power electrodes” that directly contact, and are “*ohmically coupled* to[,] the semiconductor.” EX-1001, 3:19-28, 1:33-43. Fig. 1’s gate electrode 132 is “an insulated gate electrode” that is also formed by an electrode stack 120, but gate electrode 132 is separated from the semiconductor by an insulating oxide layer 134 so it does not directly contact the semiconductor. *Id.*,

3:21-33. “In other embodiments... gate electrode 132 comprising electrode stack 120 may make Schottky contact with GaN body 110.” EX-1001, 3:31-35. In that alternate embodiment, there is no insulating layer between the gate electrode and the semiconductor because it was well-known that a “Schottky” barrier is a contact between metal and a semiconductor. *See* EX-1011, 219.

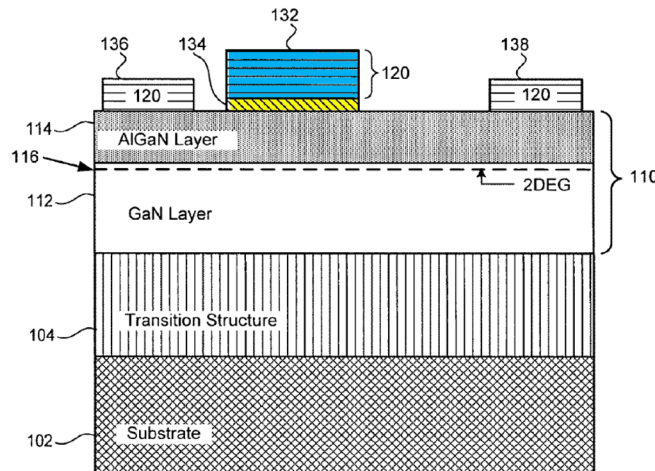
The '562 Patent specification discloses an embodiment of the inventive electrical contact comprising an electrode stack as shown in Fig. 2 (reproduced below), which the specification says “may... correspond to *any* of source electrode 136, drain electrode 138, or insulated gate electrode 132, in FIG. 1.” EX-1001, 3:36-45.



'562 Patent, Fig. 2

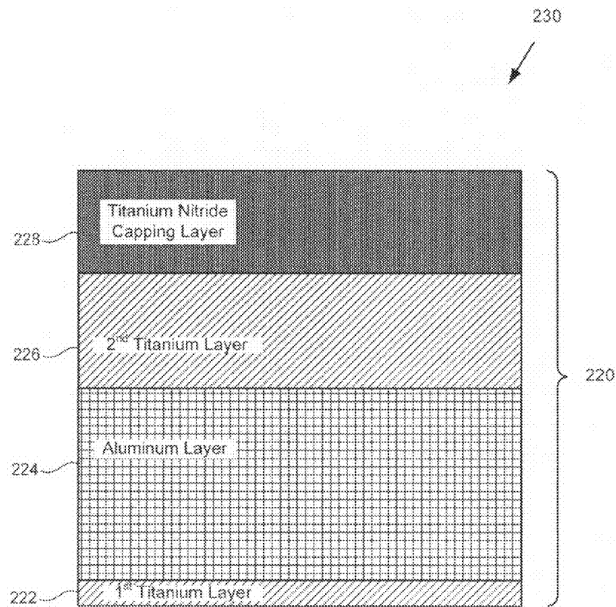
As shown in Fig. 1 of '562 Patent annotated below, the insulated gate electrode 132 (highlighted blue) is stacked over “gate insulating layer 34”

(highlighted yellow). EX-1001, 3:28-35. Gate electrode 132 is formed by the “electrode stack 120” and does not include gate insulating layer 134 that “underl[ies]” the “electrode stack 120.” *Id.*, 3:28-31, Fig. 1 (identifying the “electrode stack 120” as not including insulating layer 134). Indeed, the same “electrode stack 120” forms the source and drain electrodes 136 and 138, which do not have an insulating layer 134. *Id.*, 3:23-28, Fig. 1.



'562 Patent, Fig. 1 (annotated)

Furthermore, Fig. 2 is a more detailed illustration of an “[e]lectrode stack 220” that “corresponds to electrode stack 120 in FIG. 1.” EX-1001, 3:42-43. As seen from Fig. 2 (below), electrode stack 220 does not include an insulating layer. The specification is clear that Fig. 2’s “[e]lectrical contact 230 may... correspond to any of source electrode 136, drain electrode 138, or *insulated gate electrode* 132 in FIG. 1.” *Id.*, 3:40-42.



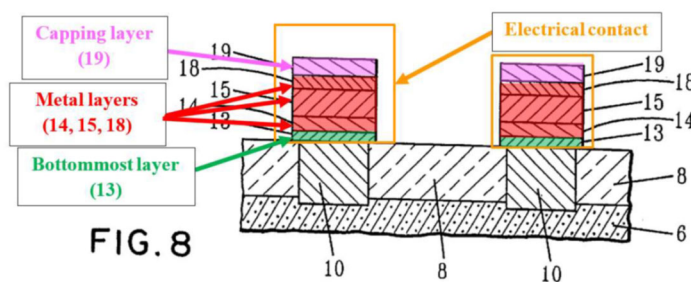
'562 Patent, Fig. 2

As seen from the foregoing, the '562 Patent specification uses the term “electrode stack” to refer to a stack of layers that together form an electrode, and describes three types of electrodes: (1) a “power electrode[]” that is in direct contact with (i.e., “*ohmically coupled* to”) the nonmetallic semiconductor material⁶ (EX-1001, 3:19-28, 1:33-43); (2) a transistor gate electrode that controls the flow of electrons or holes through the transistor and also makes direct “Schottky contact” with the nonmetallic semiconductor (*id.*, 3:31-35); and (3) a transistor gate electrode that controls the flow of electrons or holes through the transistor but does not directly contact the semiconductor because it is “an insulated gate

⁶ This type of electrode is used in the '562 Patent to form the source and drain electrodes for a transistor.

electrode” separated from the semiconductor by an insulating layer 134 (*id.*, 3:21-33). *See also* EX-1015, 503-505 (corroborating the functions of transistor source, drain, and gate electrodes).

The Petition does not even *try* to establish that the Usui structure that Petitioner identifies as purportedly being an “electrode stack” (*see* annotated Usui FIG. 8 reproduced below from the Petition at 11) is an electrode stack as described in the ’562 Patent. The identified Usui structure is an “interconnected metallurgy structure⁷...[that] preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 to make connection to a device substrate 6.” Usui, 3:24-27; *see also id.*, 5:14-15 (referring to the interplanar stud connection as “device contact metallization 10”), 3:2-8 (FIGs. 2-8 illustrate the process for making FIG. 1’s device).⁸



Petitioner’s Annotations to Usui, Fig. 8

⁷ Usui also calls this a “metallization structure.” Usui, 3:38.

⁸ Usui’s FIGs. 1 and 8 are identical.

Usui never says that its interconnect metallization structure (layers 13-15 and 18-19) is an “electrode” or forms an “electrode stack.” And Usui’s interconnect metallization structure is not (1) a power electrode that makes direct ohmic contact with the nonmetallic semiconductor material (EX-1001, 3:19-27, 1:33-43); (2) a transistor gate electrode that makes direct “Schottky contact” with the nonmetallic semiconductor (*id.*, 3:31-35); or (3) an insulated transistor gate electrode (*id.*, 3:21-33).

That should end the matter because Petitioner has failed to establish that the Usui structure it identifies is an “electrode stack” as recited in the ’562 Patent.

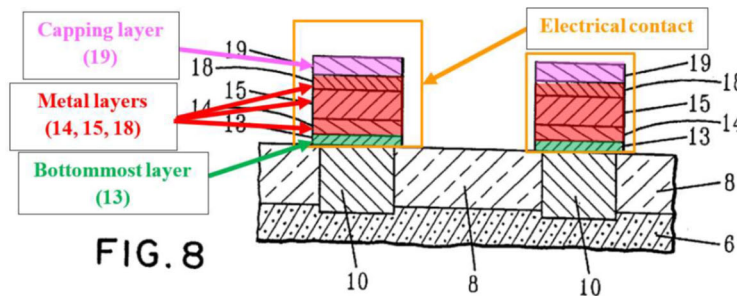
2. Petitioner Fails to Establish that Usui’s Interconnect Metallization Structure is an “Electrode Stack” Even Under a Broader Meaning Divorced From the ’562 Patent Specification

The Petition alleges that “the plain meaning of each [claim] term can be applied.” Petition, 7. But the Petition never explains what it alleges the “plain meaning” to be for the claim term “electrode stack.” Infineon disagrees that any broad meaning divorced from the context of the specification would be appropriate for the reasons discussed *supra* § II.D.1 (discussing *Phillips*). Without conceding that dictionary definitions are the appropriate way to interpret “electrode stack,” Infineon notes that the structure in Usui that Petitioner relies on is not an “electrode” even under a broad dictionary definition.

For example, Merriam-Webster's Collegiate Dictionary defines "electrode" as "1: a conductor used to establish electrical contact with a nonmetallic part of a circuit; and 2: an element in a semiconductor device (as a transistor) that emits or collects electrons or holes or controls their movements." EX-2001, 371. The '562 Patent's electrodes meet these definitions. Definition 1 is met by Fig. 1's source and drain electrodes that are "ohmically coupled" to the semiconductor, and by the embodiment of the gate electrode that "make[s] Schottky contact with" the semiconductor, because these electrodes are each a conductor used to establish electrical contact with a nonmetallic (semiconductor) part of a circuit. EX-1001,1:33-43, 3:19-21, 3:31-35. The source, drain, and gate electrodes in the '562 Patent also all meet definition 2, because each is "an element in a semiconductor... transistor" and the source and drain electrodes "emit[]" or "collect[]" electrons while the gate electrode "control[s] the movement of electrons" between the source and drain regions of the transistor.

Usui's interconnect metallization structure, on the other hand, does not meet *either* definition. Usui's interconnect metallization structure (layers 13-15 and 18-19) does not meet definition 1 because it is not "a conductor used to establish electrical contact with a *nonmetallic part of a circuit.*" Usui's interconnect metallization layer is instead connected to the "interplanar stud connection 10" and it is the stud connection 10 that "make[s] connection to a

device substrate 6.” Usui, 3:24-27; *see also* Petitioner’s annotated version of Usui’s Fig. 8 reproduced again below. Interplanar stud connection 10 is **metal**. Usui, 5:14-15 (“device contact **metallization** 10”). Thus, Usui’s interconnect metallization structure (layers 13-15 and 18-19) is connected to the **metal** stud connection 10. Usui’s interconnect metallization structure (layers 13-15 and 18-19) is not “a conductor used to establish electrical contact with a **nonmetallic part of a circuit**” and is thus not an “electrode” under Merriam-Webster’s definition 1. EX-2001, 371.



Petitioner’s Annotations to Usui, Fig. 8

Usui’s interconnect metallization structure also does not meet Merriam-Webster’s definition 2. Usui never teaches that its interconnect metallization structure (layers 13-15 and 18-19) is “an element ***in a semiconductor device*** (as a transistor) that emits or collects electrons or holes or controls their movements.” EX-2001, 371. Usui’s interconnect metallization structure is not an electrode of a semiconductor device and indeed is not part of a semiconductor device at all. Instead, as its “***interconnect metallurgy***” name signifies (Usui, 3:23-27), Usui’s

interconnect metallization structure is used to “form[] electrical connections or wiring such as *between* active and/or passive *devices* of an integrated circuit structure” (Usui, 1:11-14).

3. Petitioner Ignores Usui’s Device Contact Metallization 10

Petitioner seeks to characterize Usui’s *interconnect* metallization structure (layers 13-15 and 18-19) as an electrode stack in an attempt to meet claim 1’s requirement that the capping layer is thicker than the bottommost layer of the plurality of metal layers of the electrode stack. *See* Limitation [1c]. But Petitioner ignores Usui’s “*device contact* metallization 10” which Fig. 8 illustrates as thicker than the capping layer 19. Petitioner cannot meet its burden to show that Usui’s interconnect metallization structure is an “electrode stack” by ignoring Usui’s metal structure 10 that provides a device contact to Usui’s nonmetallic semiconductor substrate. EX-2001, 371 (“a conductor used to establish electrical contact with a *nonmetallic part of a circuit*” is an electrode).

E. Ground 1 Conclusion

As explained above, Ground 1 fails because (1) Petitioner fails to meet its burden to explain how “electrode stack” is to be construed under Petitioner’s alleged “plain meaning”; (2) Petitioner fails to meet its burden to explain how or why Usui’s interconnect metallization structure is an electrode stack as claimed; (3) Petitioner submits no evidence supporting Petitioner’s conclusory and unexplained assertion that Usui’s interconnect metallization structure is an

“electrode stack” as claimed; and (4) Petitioner ignores that Usui’s interconnect metallization structure is connected to device contact metallization 10 that provides a device contact to the nonmetallic semiconductor substrate.

Ground 1 fails for each of these independent reasons.

III. GROUNDS 2-4 FALL WITH GROUND 1

Ground 2 challenges independent claim 13. Like claim 1, independent claim 13 is directed to an electrical contact for use on a semiconductor device, where the electrical contact comprises “an *electrode stack* including a plurality of metal layers and a capping layer formed over said plurality of metal layers,” where the capping layer forms a top of the electrical contact and is thicker than a “bottommost layer of said plurality of metal layers” of the electrode stack. *See* Limitations [13pre]-[13a] and [13c].

Ground 2 only relies on Yu as a secondary reference to address independent claim 13’s requirement for a Ground III-V semiconductor device. Ground 2 relies on Usui’s same interconnect metallization structure to meet the limitations in claim 13 that relate to an electrical contact comprising an “electrode stack.” Petition, 18-19 (“A POSITA would have been motivated to implement the *electrical contacts as taught by Usui* in group III-V semiconductor devices, as taught by Yu”). Indeed, the Petition relies entirely on Ground 1’s showing for how Usui purportedly meets claim 1’s corresponding limitations to meet claim 13’s

Limitations [13a] and 13[c] that require an “*electrode* stack including a plurality of metal layers and a capping layer,” where the capping layer forms a top of the electrical contact and is thicker than a “bottommost layer of said plurality of metal layers” of the electrode stack. Petition, 23 (alleging that “[13a] is identical to [1a]. [13a] is obvious as explained for [1a]” and that “[13c] is identical to [1c]. [13c] is obvious as explained for [1c]”). Thus, Ground 2’s showing for independent claim13 inherits all of the fatal flaws identified above for Ground 1.

Grounds 2-4 also address certain dependent claims. Petition, 3. The showings in Grounds 2-4 for the dependent claims inherit the Petition’s failure for the independent claim from which they depend. Thus, Grounds 2-4 inherit all the above-discussed flaws in Ground 1 and fail for the same reasons.

IV. GROUND 5 (OBVIOUSNESS OVER YU AND USUI) FAILS

A. Overview of Yu

Yu is directed to a particular technique for forming a metal gate electrode for a CMOS device, and explains that:

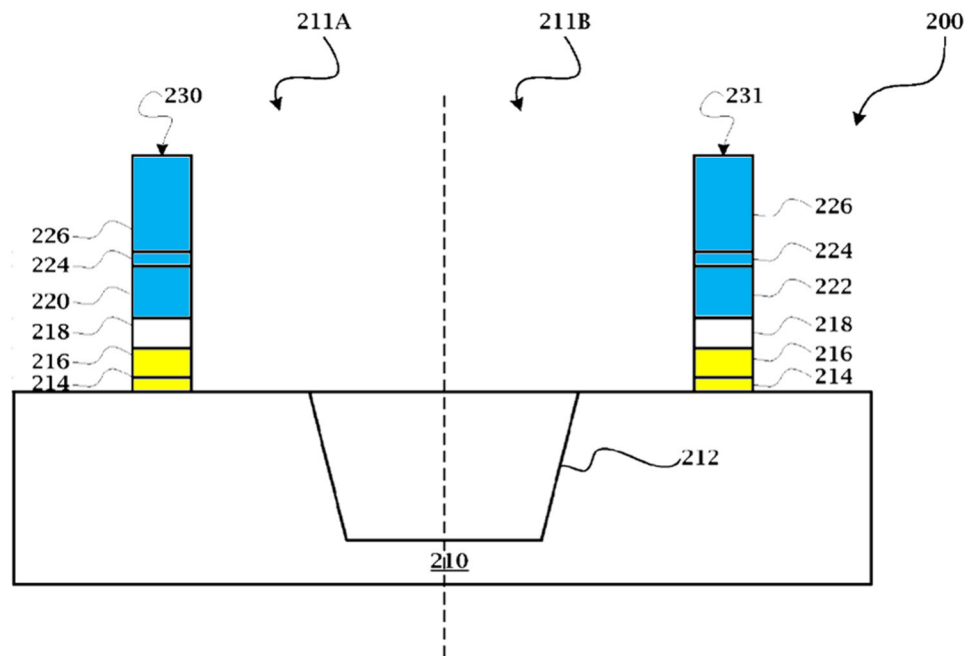
CMOS devices have typically been formed with a gate oxide and polysilicon gate electrode. There has been a desire to replace the gate oxide and *polysilicon gate electrode* with a high-k gate dielectric and *metal gate electrode* to improve device performance as feature sizes continue to decrease. Current processing utilizes metal, metal carbide, and/or metal nitride for the gate electrode. However, such materials provide insufficient work function values and present thermal stability

issues, particularly when utilized in an n-type MOS device (NMOS) and a p-type MOS device (PMOS), which require different work functions for their respective gate electrode.

Yu, [0004].

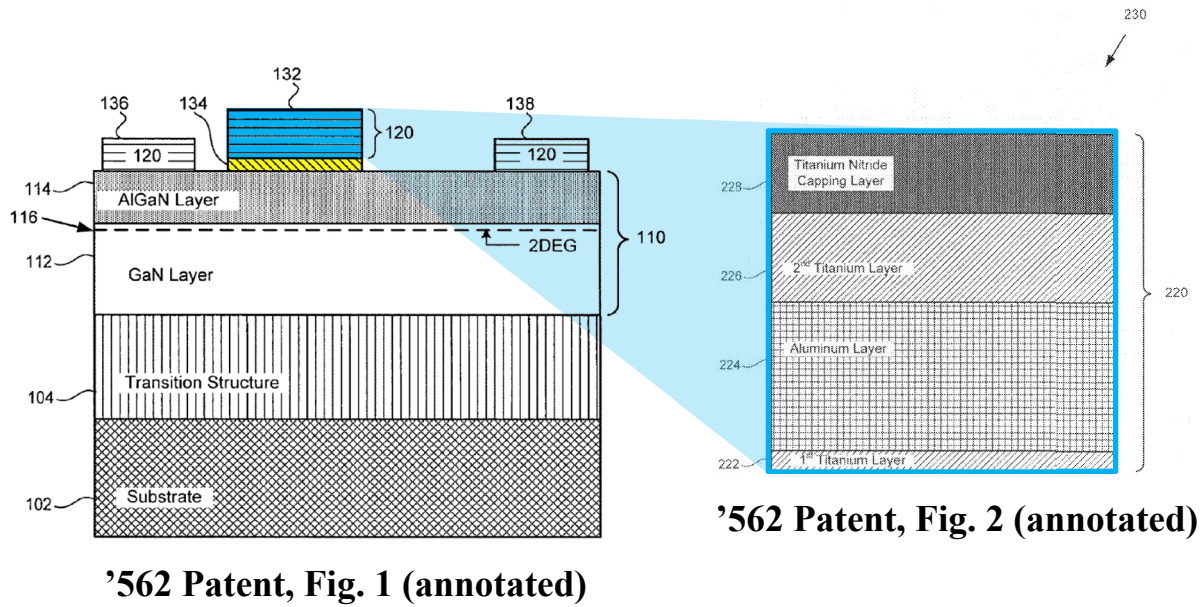
Yu addresses the above-discussed problem by providing a CMOS device whose two transistors have metal gate electrodes formed from different metal layers. A first gate electrode includes a “first metal layer 220 compris[ing] a material with a first work function” and the second gate electrode includes a “second metal layer 222 compris[ing] a material with a second work function.”

Yu, [0030]; *see also* Yu, Fig. 2E (annotated below) and [0033] (“metal layers 220, 222 [are provided] with correct work function values”). Thus, Yu’s goal of providing “different work functions for their respective gate electrode” is achieved by providing different work functions for the metal layers 220 and 222. Yu, [0004], [0030], [0033].

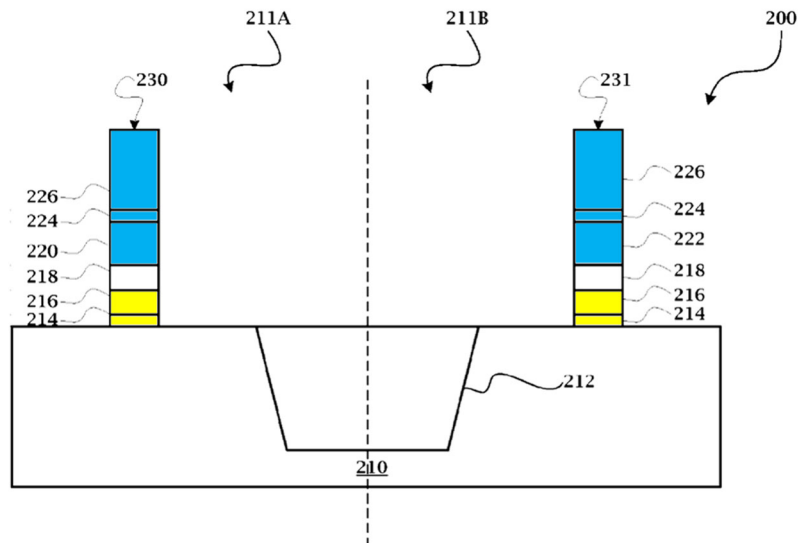


Yu, Fig. 2E (annotated)

Yu's electrodes are insulated gate electrodes. As discussed *supra* § II.D.1, the '562 Patent discloses an insulated gate electrode in which the gate electrode 132 (blue) is stacked with an insulating layer 134 (yellow) as shown in Fig. 1 (below left). EX-1001, 2:58-60 ("gate electrode 132"), 3:19-35 ("gate electrode 132"). The electrode stack in Fig. 2 (below right) forms the "gate electrode 132, in Fig. 1." *Id.*, 3:40-43 (Fig 2's "[e]lectrode stack 220" "corresponds to electrode stack 120 in FIG. 1"). Thus, the '562 Patent is clear that the "electrode stack" for a gate electrode includes only the metal layers that form the electrode and not other layers like insulating layer 134 that are stacked with the gate electrode but do not form part of the gate electrode.



Like the '562 Patent's insulated gate electrode (blue above) is stacked with another layer (yellow above), Yu's gate electrodes (blue below) are stacked with other layers (white and yellow below).

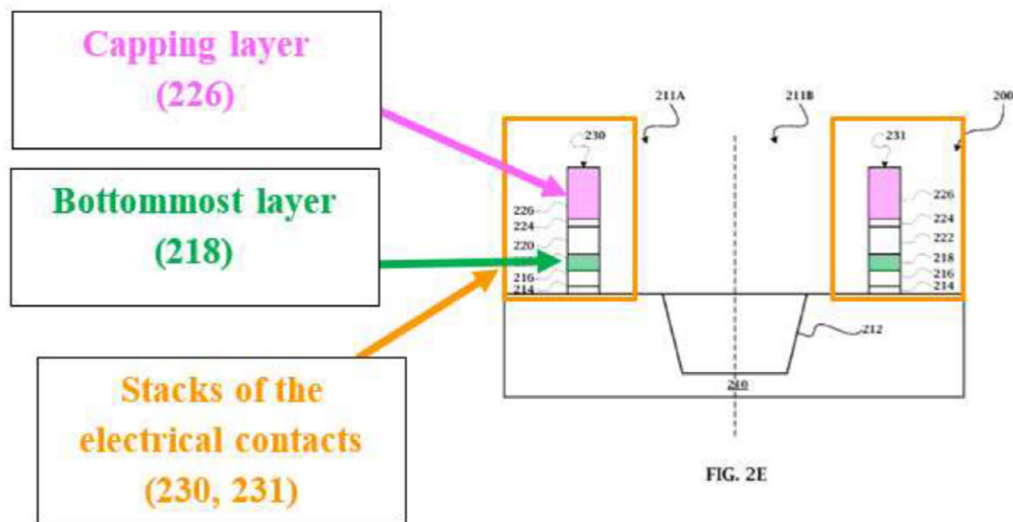


Yu refers to the entire stack as a “metal gate stack.” Yu, [0038]-[0039]. Metal gate stacks 230 and 231 have the different metal layers (220 and 222, respectively) with the different work functions as discussed above, but their structures are otherwise the same. Each includes two conducting oxide layers 214, 216 (yellow above) that sit atop the semiconductor (Yu, [0028]-[0030]), a “diffusion barrier layer” 218 that separates the metal layer (220 or 222, blue above) from the oxide layers to prevent material from diffusing between the metal and oxide layers (Yu, [0029]), a capping layer 226 (Yu, [0036]), and a diffusion barrier layer 224 that separates the capping layer from the metal layer (220 and 221) to prevent the materials in those layers from diffusing into each other (Yu, [0035]).

B. Ground 5 Fails Because Petitioner Fails to Establish that Yu’s Diffusion Barrier/Protection Layer 218 is a Layer of Yu’s Electrode Stack

As discussed *supra* § II, every Challenged Claim recites an electrical contact comprising “an electrode stack including a plurality of metal layers and a capping layer,” where the capping layer forms a top of the electrical contact and is thicker than a ***bottommost layer*** of the plurality of metal layers of the electrode stack. *See* Limitations [1pre]-[1c] and [13pre]-[13c].

Petitioner alleges that Yu’s layer 218 meets the claimed “bottommost layer.” Petition, 35-37, 43-46. This is illustrated, for example, by Petitioner’s annotated version of Yu’s Fig. 2E reproduced below. *See* Petition, 44.



Petitioner's Annotations to Yu, Fig. 2E

As Petitioner admits, Yu's layer 218 is a "diffusion barrier/protection layer." Yu, [0029]; Petition, 43 ("diffusion barrier/protection layer 218"). Yu explains that layer 218 is "optional" and "may be omitted." Yu, [0029]. Diffusion barrier layers were well-known. *See e.g.*, EX-2002, [0057]-[0058], Fig. 6. They are disposed between two layers of material to prevent the separated materials from diffusing into each other. *See id.* Diffusion barrier layers had been used to separate a gate electrode from an oxide layer – just like Yu's layer 218 does. *Id.* POSAs understood that the barrier layer is not part of the gate electrode – it separates the gate electrode from the oxide layer. *Id.*

1. Petitioner Fails to Construe "Electrode Stack"

The Petition alleges in conclusory fashion that the entire "metal gate stack" (230 or 231) in Yu is an "electrode stack" as claimed. Petition, 42. But as with

Ground 1 (*see supra* § II.A), the Petition never explains how the term “electrode stack” is to be construed. Petitioner’s Claim Construction section alleges that “the plain meaning of each term can be applied.” Petition, 7. But the Petition never explains what Petitioner alleges to be the “plain meaning” of “electrode stack.” That fails to carry Petitioner’s burden (“*must*”) to identify “how the challenged claim is to be construed” and “[h]ow the *construed* claim is unpatentable.” 37 C.F.R. § 42.104(b)(3)-(4). That is reason enough why Ground 5 fails.

2. No Evidence Supports Petitioner’s Conclusory Assertion that Yu’s Entire Metal Gate Stack is an Electrode Stack

The Petition cites no intrinsic or extrinsic *evidence* to support Petitioner’s conclusory assertion that Yu’s *entire* metal gate stack is an electrode stack. Petition, 42.

Petitioner alleges that neither of the oxide layers 214 and 216 at the bottom of Yu’s metal gate stacks 230 and 231 can be the claimed “bottommost layer of said plurality of metal layers” because layers 214 and 216 are not metal. Petition, 44-45. Petitioner further alleges that Yu’s diffusion barrier/protection layer 218 can be metal. Petition, 42. Patent Owner does not challenge either of those assertions. But even if accepted as true, those assertions do not remotely establish that Yu’s diffusion barrier/protection layer 218 is a layer of Yu’s *electrode stack*.

Limitation [1c] recites “a bottommost layer of said plurality of metal layers.” The antecedent for “*said* plurality of metal layers” is in Limitation [1a], which

recites “an *electrode stack* including a plurality of metal layers.” Thus, to meet Limitation [1c], Petitioner needed to identify a “bottommost layer of said plurality of metal layers” in Yu’s “*electrode stack*.” See Limitations [1a] and [1c].

Petitioner makes no such showing.

Petitioner alleges that Yu’s diffusion barrier/protection layer 218 meets the bottommost layer in Limitation [1c] because it is the “*bottommost layer of plurality of metal layers*” in Yu’s metal gate stacks 230 and 231. Petition, 43-44.⁹ Petitioner merely equates – by using a parenthetical – Yu’s *entire* metal gate stack (230 and 231) with the claimed “electrode stack.” Petition, 42 (“Yu discloses [1a] because it discloses **metal gate stacks 230, 231 (electrode stacks)**”) (coloring original).

The Petition never construes “electrode stack” (*supra* § II.A) and never explains how or why Yu’s *entire* metal gate stack (230 and 231) is an “electrode stack” as claimed. The Petition provides *no* explanation – let alone the required “detailed explanation” – of the significance of the cited evidence in purportedly

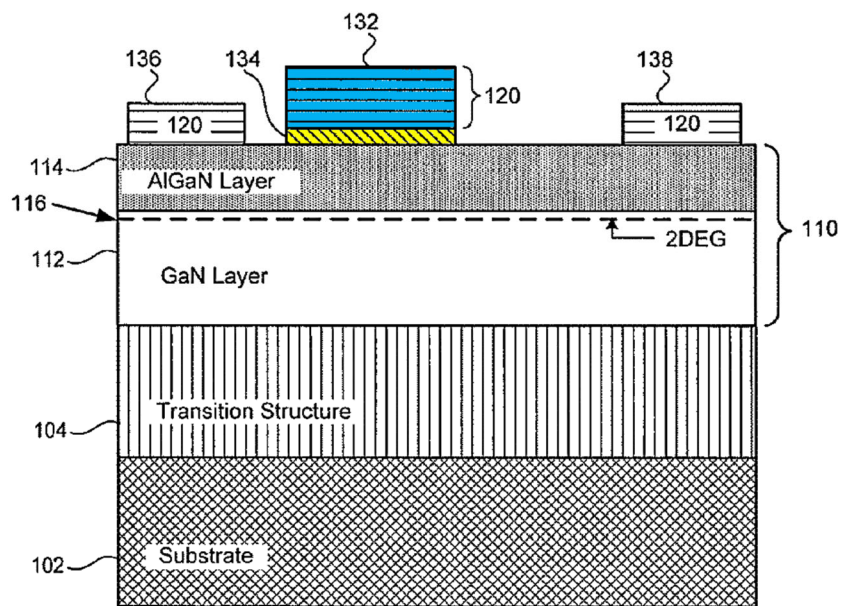
⁹ Ground 5 relies entirely on the Petition’s showing for Limitation [1c] to meet Limitation [13c]. Petition, 55 (“[13c] is identical to [1c]. [13c] is obvious as explained for [1c].”).

establishing that Yu's *entire* gate metal stack is an electrode stack as claimed. 37 C.F.R. § 42.22(a)(2).

In addition, none of the Petition's cited evidence supports Petitioner's conclusory assertion that Yu's entire metal gate stack is an electrode stack. For Limitation [1a], the Petition cites Yu, [0029] and [0035]-[0036]. Petition, 42. But none of those paragraphs characterizes Yu's entire metal gate stack as an electrode stack. The only other evidence the Petition cites is "Zhao ¶162." Petition, 42. In that paragraph Dr. Zhao just parrots the Petition's Limitation [1a] argument *word-for-word*. This conclusory testimony is devoid of any analysis or evidence to support Petitioner's assertion that Yu's *entire* metal gate stack is an "electrode stack" as claimed and warrants no weight. *Xerox*, IPR2022-00624, Paper 9, 15.

3. Petitioner's Assertion that Yu's Entire Metal Gate Stack is an "Electrode Stack" is Refuted by the Intrinsic Evidence

As shown by comparing Fig. 1 of '562 Patent and Fig. 2E of Yu (both annotated below), the '562 Patent discloses a metal gate stack that shares similarities with Yu's metal gate stack. Both stacks include not only a gate electrode (highlighted blue) but also at least one other layer (highlighted yellow) that is not part of the gate electrode.



'562 Patent, Fig. 1 (annotated)

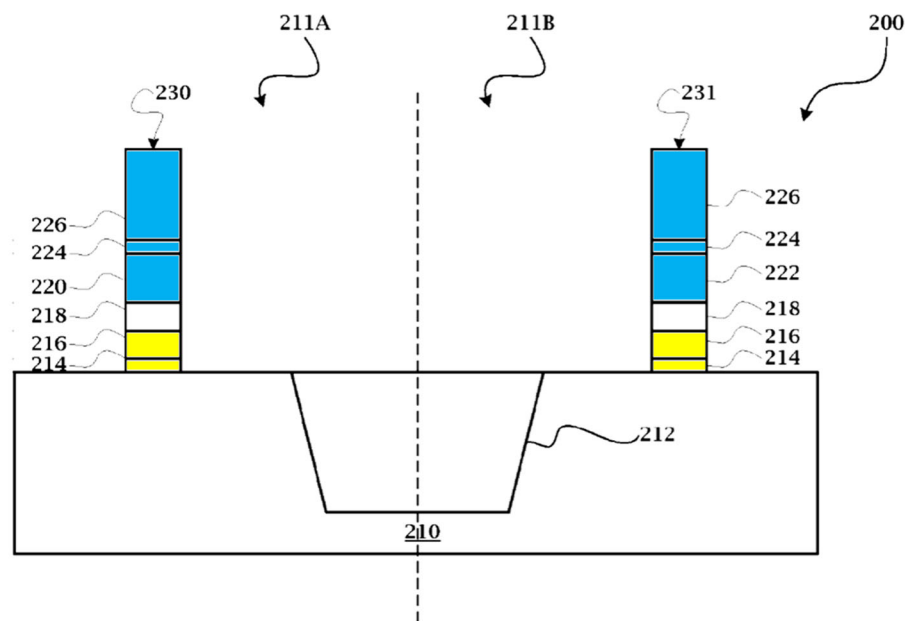
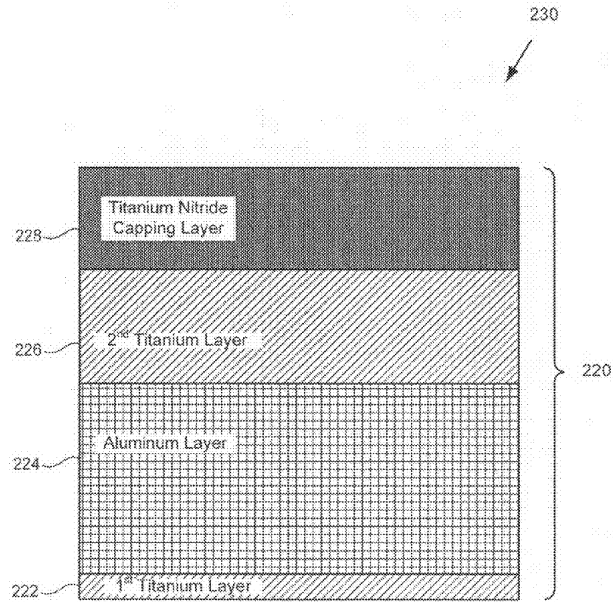


FIG. 2E

Yu, Fig. 2E (annotated)

The '562 Patent explains that Fig. 1 illustrates a “gate electrode 132” stacked with a “gate insulating layer 134.” EX-1001, 3:28-31. The '562 Patent specification is explicit that the “electrode stack 120” for this gate electrode does *not* include gate insulating layer 134. *Id.* Fig. 1’s labelling of “electrode stack 120” makes clear that the electrode stack is comprised of the stacked metal layers that form the gate electrode 132 and does *not* include gate insulating layer 134. Indeed, the same “electrode stack 120” is used for the source and drain electrodes 136 and 138 that do not have an insulating layer 134. *Id.*, 3:23-25, Fig. 1. The gate insulating layer 134 “underl[ies] the electrode stack 120” rather than being part of the electrode stack. *Id.*, 3:28-31. Furthermore, Fig. 2’s “[e]lectrode stack 220” “corresponds to electrode stack 120 in FIG. 1” (*id.*, 3:42-43) and does not include an insulating layer. *Id.*, Fig. 2 (reproduced below), 3:40-43 (Fig. 2’s “[e]lectrical contact 230 may... correspond to... [the] *insulated gate electrode* 132 in Fig. 1”). The specification could not be clearer that the “electrode stack” for the gate electrode does not include the insulating layer 134 that is stacked with the gate electrode.



'562 Patent, Fig. 2

As seen from the foregoing, the '562 Patent specification is clear that the “electrode stack” includes only stacked layers that form the electrode; if the electrode is stacked with other layers, those other layers are not part of the electrode stack. The Federal Circuit has made clear that “the specification ‘is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.’” *Phillips*, 415 F.3d at 1315 (citing *Vitronics*, 90 F.3d at 1582).

The above-identified intrinsic evidence – all of which the Petition ignores – directly refutes Petitioner’s conclusory assertion that Yu’s entire metal gate stack (230 or 231) is an “electrode stack” as claimed. Petition, 42. Yu’s entire metal gate stack (230 or 231) cannot be an “electrode stack” as claimed because it includes a dielectric layer (214 or 216) that performs the same insulating function

as insulating layer 134 in the '562 Patent.¹⁰ Yu, [0022], [0027]-[0028]. Yu, [0039]. The intrinsic evidence makes clear that such an oxide layer is distinct from and not part of the claimed “electrode stack.” Thus, Petitioner’s conclusory assertion that Yu’s entire metal gate stack 230 or 231 is an “electrode stack” as claimed is wrong.

4. Petitioner’s Failure to Correctly Identify an “Electrode Stack” in Yu is Fatal to Ground 5

Limitations [1c] and [13c] require that the material that forms the capping layer have “a thickness greater than that of a bottommost layer of *said* plurality of metal layers” that are included in the “electrode stack” per Limitations [1a] and [13a].

The *only* showing the Petition makes in attempting to meet Limitations [1c] and [13c] is that each of Yu’s *entire* metal gate stacks 230, 231 is an electrode stack, diffusion barrier/protection layer 218 is the bottommost metal layer of that alleged electrode stack, and capping layer 226 is purportedly thicker than diffusion

¹⁰ The '562 Patent’s gate insulating layer 134 can be silicon dioxide (SiO₂) (EX-1001, 3:28-31) which is a “silicon oxide,” the material referenced in Yu for dielectric layer 214. Yu, [0027] (“interfacial layer 214 may include a grown silicon oxide layer...”); EX-2003, [0130] (confirming that silicon dioxide is a silicon oxide); EX-2004, 225-230 (same).

barrier/protection layer 218. Petition, 43-46. But as detailed *supra* §§ IV.B.2-IV.B.3, Petitioner fails to establish that Yu’s entire metal gate stack (230, 231) is an “electrode stack” and thus Petitioner fails to establish that Yu’s diffusion barrier/protection layer 218 is even among the layers of Yu’s “electrode stack,” let alone its bottommost metal layer.

Thus, Ground 5 fails because Petitioner fails to establish that Yu discloses that its capping layer has “a thickness greater than that of a bottommost layer of *said* plurality of metal layers” included in the “electrode stack,” as required by all Challenged Claims. Limitations [1a]-[1c] and [13a]-[13c].

C. Petitioner Fails to Show that Yu and Usui Render Obvious an Electrical Contact with a Capping Layer of a Refractory Metal Nitride that is Thicker Than Yu’s Alleged Bottommost Layer

Even if the Board were to find that Yu’s diffusion barrier/protection layer 218 is the bottommost layer of Yu’s electrode stack (it is not), Petitioner still fails to establish that Yu and Usui render obvious any Challenged Claim.

Every Challenged Claim requires a capping layer that is *both* (1) formed from a “refractory metal nitride” or from TiN or TaN¹¹ and (2) is thicker than Yu’s

¹¹ Claim 1 requires that the “capping layer consist[] only of a refractory metal nitride” and claim 13 requires that the “capping layer consist[] only of a metal

alleged bottommost electrode stack layer 218. Petitioner fails to establish that Yu and Usui render obvious a capping layer meeting both requirements.

Yu discloses various materials for forming a capping layer. However, Petitioner admits that Yu does not “expressly disclose[]” what is required by any Challenged Claim because Yu does not disclose that its capping layer 226 is thicker than the alleged bottommost metal layer (layer 218) of the electrode stack when capping layer 226 is formed from a material that meets any Challenged Claim. Petition, 38 (“Yu expressly discloses every element of claims 1 and 13 *except a refractory metal nitride capping layer* having a thickness greater than that of a bottommost layer (claim element [1c]).”).

Petitioner points to Yu’s disclosure of a thickness for the capping layer when it is formed from polysilicon, which Petitioner concedes is “***not*** a refractory metal nitride as is stated in claims 1 and 13.” Petition, 38. Despite that, Petitioner alleges that the Challenged Claims are rendered obvious for two alternative reasons, alleging that: (1) a POSA would have been motivated to make Yu’s capping layer the same thickness when formed from a refractory metal nitride as when formed from polysilicon, and (2) Usui would have motivated a POSA to

selected from the group consisting of titanium nitride (TiN) and tantalum nitride (TaN).” See Limitations [1b] and [13b].

make Yu's refractory metal nitride capping layer thicker than Yu's diffusion barrier/protection layer 218. Petition, 38-39. As detailed below, neither assertion is supported by the evidence.

1. Yu Does Not Disclose a Refractory Metal Nitride Capping Layer that is Thicker Than Yu's Alleged Bottommost Layer 218

Yu describes a large number of materials or "combinations thereof" that could be used to form its capping layer 226. Yu, [0036]. The Petition seizes on Yu's disclosure that capping layer 226 can be made from titanium nitride or tantalum nitride because those are refractory metal nitrides. Petition, 42. But Yu never discloses a thickness for the capping layer 226 when it is formed from either of those materials (*see* Yu, [0036]) and Petitioner never alleges otherwise.

Petitioner states that "[w]hile Yu discloses the **capping layer** is *preferably* 600Å and the **bottommost layer** 20Å (i.e., the **capping layer** is *preferably* thicker than the **bottommost layer**), this disclosure is made with respect to the **capping layer** being polysilicon (Yu, [0036], [0040]), which is not a **refractory metal nitride** as is stated in claims 1 and 13." Petition, 38 (emphasis original). The 600Å thickness is the only thickness of the capping layer 226 that Petitioner cites

and it is for a capping layer made of polysilicon¹² which Petitioner admits does not meet any Challenged Claim. *Id.*, see also Yu, [0036] (disclosing a thickness of about 200-1,000 Å and “preferably about 600 Å” for a polysilicon capping layer 226).

2. Petitioner’s Assertion that a POSA Would Have Used the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Capping Layer is Unsupported

Petitioner alleges that “A POSITA would have been motivated to replace Yu’s polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed thicknesses because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation as explained by Dr. Zhao. Zhao ¶¶71-73, 155 (citing Ex-1025, 120; Ex-1026, 2; Ex-1028, 46, 56; Ex-1023, 3:39-43; Ex-1024, Abstract, 1:58-61; Ex-1029, Abstract, 1:29-34, 2:47-51).” Petition, 38 (highlighting added). Petitioner makes two distinct assertions respectively highlighted yellow and blue.

Patent Owner does not dispute Petitioner’s assertion (highlighted yellow) that a POSA had reason to use titanium nitride or tantalum nitride as the material to

¹² Yu discloses a different thickness (about 50-1,000 Å and “preferably about 200 Å”) when the capping layer 226 is an “aluminum-based, tungsten, or copper material.”

form Yu's capping layer, nor that these refractory metal nitrides had known benefits. Petition, 38. Indeed, Yu expressly discloses that titanium nitride or tantalum nitride can be used for the capping layer 226. Yu, [0036].

However, the Petitioner's separate assertion (highlighted blue) that a POSA would have been motivated to "us[e] the same disclosed thickness" that Yu teaches for a polysilicon capping layer when making the capping layer from a refractory metal nitride is entirely unsupported. Petition, 38.

a. Petitioner Alleges No Reason Why a POSA Would Have Chosen the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Nitride Layer

Establishing obviousness requires a supportable, evidence-based *reason why* a POSA would have combined various teachings in the art in the manner claimed. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007); *TQ Delta, LLC v. CISCO Sys., Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) (reversing the Board's obviousness determination: "'a conclusory assertion with no explanation is inadequate to support a finding that there would have been a motivation to combine' because '[t]his type of finding, without more, tracks the *ex post* reasoning *KSR* warned of and fails to identify any actual *reason why* a skilled artisan would have combined the elements in the manner claimed.'" (internal citation omitted)).

The only reason Petitioner alleges a POSA would have “been motivated to replace Yu’s polysilicon with either its disclosed titanium nitride or tantalum nitride” is the argument highlighted yellow above. Petition, 38 (alleging a POSA would have done so “because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation as explained by Dr. Zhao” and citing Zhao ¶¶71-73).

The Petition does not even allege, let alone establish with evidence, any reason why a POSA would have chosen the “same... thickness[]” that Yu discloses for its polysilicon capping layer when the capping layer is instead formed from a refractory metal nitride. Petition, 38. Dr. Zhao’s declaration cannot save Petitioner because arguments cannot be incorporated by reference into the Petition from the Zhao declaration. 37 CFR § 42.6(a)(3) (“Arguments must not be incorporated by reference from one document into another document.”).

But even if the Board were to wade into the Zhao declaration to evaluate the alleged “obvious design alternation [*sic*] ...explained by Dr. Zhao” (Petition, 38), Dr. Zhao also never alleges, let alone establishes, any reason why a POSA would have used the same thickness Yu discloses for a polysilicon capping layer when the capping layer is formed from a refractory metal nitride. In § IV.C.2.b below, Patent Owner walks through the cited paragraphs from Dr. Zhao. Most of these paragraphs say nothing about the “thickness” of any layer. Only Zhao ¶155

mentions thickness and it does so in conclusory language that does nothing but repeat the Petition's argument word-for-word. Thus, like the Petition, Dr. Zhao never alleges any *reason why* a POSA would have used the "same... thickness[]" that Yu discloses for its polysilicon capping layer when the capping layer is instead formed from a refractory metal nitride. Petition, 38 (citing Zhao ¶¶71-73, 155).

Petitioner's failure to provide a supportable reason why a POSA allegedly would have chosen the "same... thickness[]" that Yu discloses for its polysilicon capping layer when the capping layer is formed from a different material – a refractory metal nitride (Petition, 38) – is particularly egregious given that Yu discloses that the material chosen for the capping layer significantly impacts the thickness that should be used. Yu, [0036]. While Petitioner fails to acknowledge it, the "prefer[red]" thickness of 600Å that Yu reports for a polysilicon capping layer is not the only capping layer thickness that Yu discloses. Petition, 38. When the capping layer is formed from other materials ("aluminum-based, tungsten, or copper material"), Yu discloses a very different "prefer[red]" thickness of "about 200 Å" that is less than *one-third* of the preferred thickness for a polysilicon capping layer. Yu. [0036].

Petitioner's failure to even allege, let alone support with evidence, any reason why a POSA would have chosen the "*same*... thickness[]" that Yu discloses for its polysilicon capping layer when the capping layer is formed from a

refractory metal nitride is fatal to Petitioner's assertion that Yu alone suggests to a POSA the use of a capping layer of a refractory metal nitride that is thicker than Yu's alleged bottommost layer 218 (Petition, 38). *KSR*, 550 U.S. at 418; *TQ Delta*, 942 F.3d at 1359 (a "reason" is required).

b. No Evidence Supports Petitioner's Assertion that a POSA Would Have Chosen the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Nitride Layer

Even if the Petition is read as alleging some reason why a POSA would have chosen the "same... thickness[]" that Yu discloses for its polysilicon capping layer when the capping layer is formed from a refractory metal nitride (it does not), any such assertion fails because it is not supported by *any evidence*. Petition, 38.

Petitioner's assertion that a "POSITA would have been motivated to replace Yu's polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed thicknesses because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation as explained by Dr. Zhao" cites "Zhao ¶¶71-73, 155." Petition, 38 (highlighting added).

None of these cited paragraphs supports the assertion (in blue above) that a POSA would have used Yu's same thickness for a polysilicon capping layer when the layer is instead formed from a refractory metal nitride. As detailed below, Zhao ¶¶71-73 never refer to thickness at all and Zhao ¶155 just repeats the Petition's argument *word-for-word*.

Zhao ¶71 explains what refractory metals are and provides examples. Zhao ¶71 never mentions a refractory metal *nitride* layer and never mentions any *thickness* for any layer, let alone for a capping layer.

Zhao ¶72 explains that refractory metal nitrides were known, provides some examples, and explains different known uses (e.g., as a diffusion barrier layer) for a refractory metal nitride layer *other* than as a capping layer. Zhao ¶72 never mentions any *thickness* of a refractory metal nitride layer for any purpose, let alone for a capping layer.

Zhao ¶73 explains that it “was also well-known that refractory metal nitride capping layers are effective” for various reasons. Zhao ¶73 never mentions any *thickness* of a refractory metal nitride capping layer.

Zhao ¶155 does nothing but parrot the Petition’s argument in the first paragraph on page 38 of the Petition *word-for-word*. *Compare* Petition, 38 *with* Zhao ¶155. Dr. Zhao’s naked conclusory assertion that a POSA would have used the “same... thickness[]” for a refractory metal nitride capping layer that Yu teaches is preferred for a polysilicon capping layer warrants no weight under the Board’s precedential *Xerox* decision because it merely repeats the Petition’s arguments word-for-word without providing any reasoned analysis or corroborating evidence. *Xerox*, IPR2022-00624, Paper 9, 15 (“[T]he cited declaration testimony is conclusory and unsupported, adds little to the conclusory

assertion for which it is offered to support, and is entitled to little weight.”); *see also id.* (quoting 37 C.F.R. §42.65(a): “Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight”). And just like the Petition, Zhao ¶155 never explains any ***reason why*** a POSA would have chosen Yu’s disclosed thickness for a polysilicon capping layer when using a refractory metal nitride capping layer despite Yu’s disclosure of different thicknesses for the capping layer when formed from different materials. Yu, [0036]; *see supra* § IV.C.2.a (Yu’s preferred thickness when the capping layer is formed from other materials is less than ***one-third*** of the preferred thickness for a polysilicon capping layer).

While the Petition promises that the cited paragraphs of the Zhao declaration “explain[]” a reason why a POSA would have used the “same... thickness” for a refractory metal nitride capping layer as for a polysilicon capping layer (Petition, 38), there is no such explanation in the cited paragraphs of Dr. Zhao’s declaration.

The Petition does not cite a single piece of credible ***evidence*** that supports its assertion that a POSA would have chosen the “same... thickness[]” that Yu discloses for its polysilicon capping layer when the capping layer is formed from a refractory metal nitride. Petition, 38.

c. Petitioner Does Not Identify the Thickness of Yu's Diffusion Barrier/Protection Layer 218 When it is Made of Titanium as Alleged in the Yu-USUI Combination

Petitioner alleges that the thickness of Yu's diffusion barrier/protection layer 218 is 20Å. Petition, 38 ("Yu discloses the **bottommost layer** [is] 20Å"). The 20Å thickness that Yu teaches is for a diffusion barrier/protection layer 218 formed from titanium *nitride* (TiN). Yu, [0029] ("the diffusion barrier/protection layer 218 comprises TiN, which is deposited by PVD to a thickness of approximately 20Å."). But Petitioner's Yu-USUI combination does *not* use a *TiN* diffusion barrier/protection layer 218. Instead, Petitioner alleges that a "POSITA would have been motivated to use *titanium* as **diffusion barrier/protection layer 218**... in Yu's device." Petition, 36. Petitioner relies on titanium for Yu's alleged bottommost layer 218 because Ground 5 relies on USUI's teachings to "limit[] the thickness of... underlayer 13" (Petition, 38-39) and USUI's underlayer 13 is formed from titanium (USUI, 3:27-31). Titanium nitride and titanium are different materials.

Petitioner does not cite any teaching in Yu of a thickness for the diffusion barrier/protection layer 218 when formed of titanium as used in Petitioner's Yu-USUI combination. Petition, 36. The only thickness that Petitioner cites is 20Å, which is for a TiN "embodiment." Yu, [0029]. Yu does not say that this thickness applies for the diffusion barrier/protection layer 218 for all materials. Instead, Yu

says that “in alternate embodiments, the diffusion barrier layer 218 comprises any suitable thickness.” Yu, [0029]. Yu provides no teaching of a “suitable thickness” for the diffusion barrier/protection layer 218 when formed of titanium as used in Petitioner’s Yu-USui combination. Petition, 36.

* * *

As seen from the foregoing, Petitioner’s assertion that Yu teaches that its capping layer 226 is thicker than its diffusion barrier/protection layer 218 is based on thickness values that Yu reports for *different materials for both layers* than are used in Petitioner’s Yu-USui combination.¹³ Yu teaches nothing about the thickness of these layers when formed from the materials in Petitioner’s Yu-USui combination. Yu simply does not teach a refractory metal nitride capping layer 226 that is thicker than a titanium diffusion barrier layer 218 as Petitioner alleges.

¹³ Petitioner relies on a capping layer thickness for a polysilicon layer rather than a refractory metal nitride (TiN or TaN) layer, as discussed *supra* § IV.C.2.b, and a diffusion barrier/protection layer 218 thickness for a TiN layer rather than the Ti layer in Petitioner’s Yu-USui combination, as discussed *supra* § IV.C.2.c.

3. Petitioner’s Assertion that Usui Would Have Motivated a POSA to Form Yu’s Refractory Metal Nitride Capping Layer to be Thicker Than Yu’s Diffusion Barrier/Protection Layer Fails

Recognizing the shortcomings in Yu, which fails to disclose the relative thicknesses required by the Challenged Claims, Petitioner relies on Usui:

To the extent Yu does not expressly disclose a **refractory metal nitride capping layer** having a thickness greater than that of a **bottommost layer**, Usui does. As Usui recognizes, “by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention.” Usui, 3:29-37.

Petition, 38-39.

Petitioner’s assertion fails for numerous reasons detailed below.

a. The Capping Layer Being Thicker than the Bottommost Layer of the Electrode Stack’s Metal Layers is a Missing Limitation Not Taught by Yu or Usui

Petitioner’s assertion that Usui’s underlayer 13 is the bottommost metal layer of an *electrode stack* fails for the reasons discussed in connection with Ground 1 because Petitioner fails to establish that Usui’s interconnect metallization structure (Usui layers 13-15 and 18-19) is an electrode stack. *See supra* § II.

Thus, neither Yu nor Usui teaches an electrode stack having a capping layer that is thicker than the bottommost layer of the plurality of metal layers of the

electrode stack. This is a limitation of every Challenged Claim (*see* Limitations [1a]-[1c] and [13a]-13[c]) and it is missing from Petitioner’s prior art.

The Federal Circuit has repeatedly held that for “common sense” or expert testimony alone to supply a claim limitation missing from the prior art, “the limitation in question [must be] unusually simple and the technology particularly straightforward.” *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016); *see also DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1374 (Fed. Cir. 2018) (“[W]e have invoked common sense to fill in a ***missing*** limitation ***only*** when the limitation in question was unusually simple and the technology particularly straightforward.”) (internal quotes and citations omitted).

In *Arendi*, the Federal Circuit reversed the Board’s finding of obviousness when not all limitations were disclosed by the prior art. 832 F.3d at 1366. The claimed technology related to a method of identifying duplicate entries in a database and the prior art disclosed a computerized address book. *Id.*, 1358-59. The Board reasoned that “it would have been obvious to... search for duplicate telephone entries when entering a telephone number in an electronic address book...” *Id.*, 1360. The Federal Circuit disagreed, noting that the prior art reference did “not mention or imply that a search of any kind is involved with the ‘Add to address book’ function.” *Id.*, 1363. The “only documentary support the Board recited was the declaration of... Appellees’ expert.” *Id.*, 1364. The Federal Circuit found that the Board erred by

relying on “*conclusory statements* and unspecific expert testimony regarding searches in general,” which was “particularly problematic considering the fact that a key limitation” of the patent – identifying duplicate entries – “was missing from the prior art.” *Id.*, 1366.

In *DSS Tech.*, the Federal Circuit again reversed the Board’s finding of obviousness when not all limitations were disclosed by the prior art. 885 F.3d at 1375. The claimed technology related to a communication network with a single base station and multiple peripheral devices, where each was “energized in low duty cycle RF bursts” intermittently. *Id.*, 1369-70. The prior art taught *peripheral devices* that operated in this manner, but *not the base station*. *Id.*, 1373. The Board found that it would have been obvious “to have the base station operate in an analogous manner” to the peripheral devices. *Id.* The Federal Circuit disagreed because the limitation at issue was “not ‘unusually simple,’ and the technology is not ‘particularly straightforward.’” *Id.*, 1375 (quoting *Arendi*).

Petitioner does not even attempt to establish that its reliance on expert testimony to supply a claim limitation – an electrode stack having a capping layer that is thicker than the bottommost layer of the plurality of metal layers of the electrode stack – that is missing from both of Petitioner’s prior art references (Yu and Usui) is consistent with Federal Circuit precedent. The Board routinely denies institution in such circumstances.

The Board’s *Xerox* decision involved a “mobile ticketing system for detecting fraudulent activity” and the claimed method required a step of “stor[ing] in a data record associated with the account a data value indicating the fraudulent activity.” *Xerox*, IPR2022-00624, Paper 9, 6. While the prior art (“Terrell”) taught that “the purchaser of the ticket could be blocked from further use of the system,” the petitioner did not allege that Terrell disclosed storing a data value indicating the fraudulent activity as claimed. *Id.*, 14. Instead, petitioner alleged that POSAs “‘would find it obvious’ that ‘blocking the account of the purchaser’ would includ[e] ‘storing a data value indicating the fraudulent activity in a data record associated with the user account.’” *Id.* “Petitioner’s only evidence in support of its assertion... [was] the opinion of its Declarant, Dr. Jones.” *Id.*, 15. In denying institution, the Board not only found that Dr. Jones failed to adequately support his opinions, but that petitioner ran afoul of the Federal Circuit’s *Arendi* decision. *Xerox*, 16. The Board noted that “[p]etitioner has not alleged” that “the limitation in question [is] unusually simple and the technology particularly straightforward,” “much less provided support for such an allegation.” *Id.* (quoting *Arendi*).

The Board reached a similar result in *Apple v. Mullen Indus. LLC*, IPR2023-00087, Paper 10, 19-20 (May 3, 2023). That case involved “systems and methods for determining a device’s location” (*id.*, 3) and the claims required the “device to display indicia of two locations other than its own” (*id.*, 15). The

prior art (“Sheha”) disclosed “displaying the location of a caller and a called device on a screen, but [did] not disclose displaying multiple locations of other users.” *Id.*, 17. Petitioner alleged “it would have been obvious to display the locations of second and third devices simultaneously.” *Id.* Petitioner’s only evidence was “the opinion of its Declarant, Mr. Williams.” *Id.*, 17-18. In addition to finding that Mr. Williams failed to adequately support his opinions (*id.*, 18), the Board found that petitioner ran afoul of *Arendi*. *Id.*, 19-20 (“[p]etitioner has not alleged” that “the limitation in question [is] unusually simple and the technology particularly straightforward,” “much less provided support for such an allegation.” The Board denied institution at least in part on that basis. *Id.* (quoting *Arendi*).

Just like the petitioners in *Xerox* and *Apple*, Petitioner does not even allege that the missing claim limitation of an electrode stack having a capping layer that is thicker than the bottommost layer of the metal layers of the electrode stack (*see* Limitations [1a]-[1c] and [13a]-13[c]) is unusually simple or that the claimed technology is particularly straightforward.

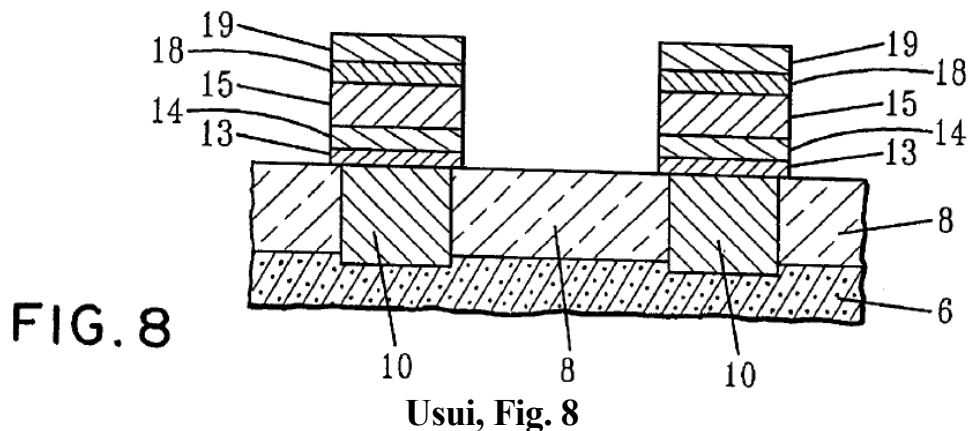
Petitioner’s failure to establish that this is one of the rare exceptions to the rule forbidding reliance on expert testimony alone to meet a claim limitation missing from the prior art is further reason why Ground 5 fails.

b. Usui's Teachings About its Interconnect Metallurgy Structure Would Not Have Motivated Any Change to Yu's CMOS Gate Electrode

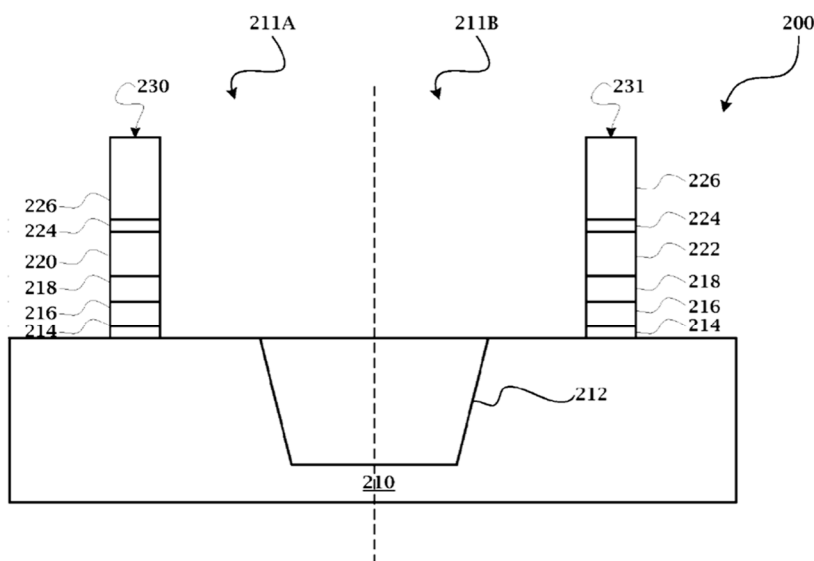
As Petitioner acknowledges, Usui teaches that “limiting the thickness of... underlayer 13... is essential in achieving the necessary properties of the structure of *the present invention*.” Petition, 38-39 (quoting Usui, 3:29-37). Usui’s “present invention” is “an interconnect metallurgy structure” that connects to an interplanar stud 10 that in turn makes a connection to the device substrate. Usui, 3:23-27.

Unlike Usui, Yu has nothing to do with an “interconnect metallurgy structure.” Instead, Yu is directed to gate electrodes for a CMOS device. Yu, Title, [0004]-[0005], [0021]. Petitioner fails to establish that Usui’s teachings about how to purportedly make a better interconnect metallurgy structure would have motivated a POSA to make any change to Yu’s CMOS gate electrode.

Petitioner relies on Usui’s “underlayer 13.” Underlayer 13 is the bottom layer of Usui’s interconnect metallurgy structure and is “deposited” on “planar insulator 8 and contact stud 10.” Usui, 5:11-14, Fig. 8 (reproduced below). Usui teaches that “by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers [of the interconnect metallurgy structure] is carefully controlled.” Usui, 3:29-37; *see also* Petition, 38-39 (quoting same).



In Yu's device, Petitioner alleges that the claimed bottommost layer is met by Yu's diffusion barrier/protection layer 218. Petition, 39. But as discussed *supra* § IV.B.3, Yu's diffusion barrier/protection layer 218 is **not** deposited on a contact stud and is **not** the underlayer of Yu's metal gate stack 230 or 231. As seen in Yu's Fig. 2E (reproduced below), the underlayer of Yu's metal gate stack is the interfacial dielectric layer 214 that is "formed over the substrate 210." Yu, [0027].



Quite simply, Usui’s disclosure about how to “achiev[e] the necessary properties of the [interconnect metallurgy] structure of [Usui’s] ***present invention***” (Usui, 3:23-37) would not have motivated a POSA to make any change to Yu’s CMOS gate electrode. Petitioner’s assertion that Usui would have motivated a POSA to make Yu’s diffusion barrier/protection layer 218 thinner than Yu’s capping layer 226 fails for this additional reason.

4. Petitioner’s Reliance on *KSR*’s Known Elements/Predictable Results Rationale Fails

Petitioner asserts that Usui’s teaching to limit the thickness of underlayer 13 in Usui’s interconnect metallization structure would have motivated a POSA to limit the thickness of Yu’s diffusion barrier/protection layer 218 because this would have been nothing more than “combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results.” Petition, 39 (citing *KSR*); *see also* Petition, 37.

The *KSR* rationale Petitioner relies on only applies when the elements are combined without “change in their respective functions.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-416 (2007) (describing as obvious “a combination which only unites old elements ***with no change in their respective functions***”); *see also* MPEP §2143(I)(A) (Feb. 2023) (proving obviousness based on “Combining Prior Art Elements According to Known Methods To Yield Predictable Results” requires that a POSA “could have combined the [known] elements as claimed by

known methods *with no change in their respective functions*") (citing, *inter alia*, *KSR*, 550 U.S. at 416).

The "function" of Usui's underlayer 13 is that it provides connection to interplanar stud connection 10 and "by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers [of the interconnect metallurgy structure] is carefully controlled." Usui, 3:29-37, 5:11-14 and Fig. 8; *see also* Petition, 38-39 (quoting same). But the function of Usui's thin underlayer 13 is dramatically changed in Petitioner's Yu-Usui combination in which the allegedly thin layer is the diffusion barrier/protection layer 218. The diffusion barrier/protection layer 218 does not connect to an interconnect stud, is not the bottommost layer of Yu's metal gate stack, and its function is to prevent the diffusion of materials between Yu's metal layers (220, 221) and oxide layers (214, 216). Yu, [0029]-[0030]; *see also* EX-2002, [0057]-[0058], Fig. 6.

Thus, *KSR*'s "combining prior art elements according to known techniques to a known device ready for improvement to yield predicable results" rationale (Petition, 39) plainly does not support Petitioner's Yu-Usui combination. Nothing does. That is an additional reason why Ground 5 fails.

V. GROUNDS 6-7 FALL WITH GROUND 5

Grounds 6-7 add additional secondary references to Ground 5's Yu-Usui combination to address certain dependent claims. Petition, 3. Petitioner does not

rely on these secondary references to meet any of the limitations in independent claim 1 or independent claim 13 and instead relies entirely on Ground 5's showing to meet independent claims 1 and 13. Petition, 55-64. Thus, Grounds 6-7 inherit all the above-discussed flaws with Ground 5 and fail for the same reasons.

VI. CONCLUSION

For the reasons stated above, institution should be denied.

Respectfully submitted,
Infineon Technologies Americas Corp.

Date: April 11, 2025

/ Richard Giunta/

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** contains 11,905 words excluding; a table of contents, a table of authorities, a certificate of service or word count, or appendix of exhibits or claim listing. Patent Owner has relied on the word count feature of the word processing system used to create this paper in making this certification.

Date: April 14, 2025

/MacAulay Rush/
MacAulay Rush
Paralegal
WOLF, GREENFIELD & SACKS, P.C.

CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.6 (e)(4)

I certify that on April 14, 2025, I will cause a copy of the foregoing document, including any exhibits filed therewith, to be served via electronic mail, as previously consented to by Petitioner, upon the following:

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