

INNOSCIENCE'S INITIAL INVALIDITY CONTENTIONS

US 8,686,562 B2

APPENDIX B-3

***In the Matter of:
CERTAIN SEMICONDUCTOR DEVICES, AND PRODUCTS
CONTAINING THE SAME***

Investigation No. 337-TA-1414

APPENDIX B-3
INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 8,686,562 B2¹
U.S. Patent Publication No. 2010/0052066 (“Yu”)

U.S. Patent Publication No. 2010/0052066 (“Yu”), filed on April 15, 2009 (Innoscence 1414-00004344 - Innoscence 1414-00004375), qualifies as prior art to U.S. Patent No. 8,686,562 (the ‘562 Patent) at least under 35 U.S.C. § 102(e).²

The following list identifies one or more references cited in certain grounds for invalidity of claims 1, 2, 8-11, and 13-16 of the ‘562 Patent based on Yu:

- U.S. Patent No. 5,943,601 (“Usui”) was filed on April 30, 1997 (Innoscence 1414-00003742 - Innoscence 1414-00003753), qualifies as prior art to the ‘562 Patent at least under 35 U.S.C. §§ 102(a), 102(b), and/or (e)
- U.S. Patent Publication No. 2008/0023726 (“Adesida”) was filed on May 24, 2007, (Innoscence 1414-00004284 - Innoscence 1414-00004297). Adesida qualifies as prior art at least under 35 U.S.C. §§ 102(a), (b), and/or (e).
- U.S. Patent No. 7,777,252 to Sugimoto et al. (“Sugimoto”) was filed on January 17, 2007 (Innoscence 1414-00003905 - Innoscence 1414-00003921). Sugimoto qualifies as prior art at least under 35 U.S.C. § 102(e).

As illustrated below, one or more claims of the ‘562 Patent are invalid as expressly and/or inherently anticipated by Yu, including asserted claim 1. Additionally, to the extent that Yu is found not to anticipate, expressly or inherently, claim 1 of the ‘562 Patent, it is invalid as obvious in view of Yu alone or in combination with other prior art references, including, but not limited to, the prior art discussed below, the prior art identified in the Respondents’ Invalidity Contentions, and the prior art described in additional claim charts attached as Appendices B-1 through B-4. Exemplary invalidity grounds based on the Usui reference include the following, although these examples are by no means limiting:

¹ The claim chart below is meant to illustrate how the reference identified above invalidates the asserted claim. By not discussing other portions of the reference below, Respondents do not waive their right to rely on other portions of the reference; instead, Respondents expressly reserve their right to rely on other portions of the reference. These contentions are not an admission by Respondents that any accused products, including any past or current version of these products, are covered by or infringe Complainant’s asserted claim, particularly once the claim is construed by the ALJ, and do not constitute an admission by Respondents as to the proper construction of any asserted claim and citations may be based on Complainant’s apparent construction of the claim. These contentions are not an admission by Respondents as to the proper scope of any asserted claim or the proper construction of any asserted claim. Respondents reserve the right to modify, amend, or supplement these contentions as additional information becomes available.

² All statutory citations refer to pre-AIA law.

- Obviousness based on Yu (claims 1, 2, 8, and 13);
- Obviousness based on Yu in combination with Usui (claims 1, 2, 8, and 13);
- Obviousness based on Yu in combination with Adesida (claims 9, 10, 11, 14, 15, and 16);
- Obviousness based on Yu in combination with Usui and Adesida (claims 9, 10, 11, 14, 15, and 16);
- Obviousness based on Yu in combination with Sugimoto (claims 9, 10, 11, 14, 15, and 16);
- Obviousness based on Yu in combination with Usui and Sugimoto (claims 9, 10, 11, 14, 15, and 16).

The citations included in the table below are exemplary only and are not intended to be limiting or exhaustive. Respondents reserve the right to cite additional disclosures and evidence in support of their positions as the Investigation develops further.

Additionally, Respondents may be basing the arguments below on claim interpretations suggested in Complainants' infringement and domestic industry claim charts provided with the Complaint, as best as they can be deciphered. By applying the prior art in this way, Respondents do not concede their agreement with Complainant's positions, nor do these Invalidity Contentions constitute any admission regarding claim scope. Nor are Respondents asserting any claim construction positions through these charts. Moreover, preambles generally are not limiting, and nothing in these contentions should be deemed an admission that the preamble in the asserted claims is limiting.

As these proceedings further develop, Respondents intend to amend or supplement these exemplary disclosures and any related contentions as appropriate, and in a manner consistent with all applicable rules governing this Investigation. In particular, Respondents reserve the right to rely on (1) uncited portions of the identified prior art; (2) other prior art not identified herein; (3) references that show the state of the art (irrespective of whether such references themselves qualify as prior art to the asserted patents); (4) factual testimony from the inventors or authors of the prior art references; and/or (5) expert testimony, to provide context to or aid in understanding the prior art and the state of the art at the time of the alleged inventions.

Descriptions of Exemplary Obviousness Combinations Based on Yu

Yu and each of the additional references cited below are analogous art to the '562 Patent. They are directed to forming electrical contacts for semiconductor devices. *See* '562 Patent at Abstract, 3:19-21; Usui at Abstract, 1:5-14, 2:33-39; Yu at Abstract, ¶¶ [0018], [0033], [0040]; Adesida at Abstract, ¶¶ [0015]-[0017], [0031]-[0034]; Sugimoto at Abstract, 9:24-51, 6:3-7:39, 7:56-60, 8:30-44, 9:39-51. Because they are all directed to the same type of devices and their fabrication methods, a person of ordinary skill in the art would have

appreciated that Yu and the additional references cited below come from the same field of endeavor and provide disclosures that relate to one another.

The combination of Yu with one or more of the additional references would involve one or more of: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; use of a known technique to improve similar devices in the same way; applying a known technique to the device ready for improvement to yield predictable results; obvious trying given a finite number of identified, predictable solutions, and a reasonable expectation of success; known work in one field of endeavor that prompts variations for use in the same field based on design incentives or market forces; and a teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at claim 1.

For example, by August 2009, it was common and well-known that various thicknesses of layers in an electrode stack will yield different properties. Specifically, Yu discloses electrode stacks where the bottommost metal layer has a thickness of about 20 angstroms and the capping layer has a thickness of about 200 to 1,000 angstroms, preferably 600 angstroms. Yu, [0029], [0036]. Additionally, Yu expressly discloses that diffusion barrier/protection layer 218 (bottommost layer of plurality of metal layers) (Yu, [0029], Fig. 2E) may be “any suitable thickness.” *Id.*, [0029] and [0036]. To the extent that Yu does not expressly disclose a refractory metal nitride capping layer having a thickness greater than that of a bottommost metal layer, Usui does. Yu and Usui are both directed to improving thermal characteristics, thermal stability, and device characteristics in semiconductor devices. *See* Yu, Abstract, [0006], [0017], [0019], [0020], [0032], [0033], [0061], [0085], [0109]; Usui, Abstract, 1:6-9, 5:11-16. As Usui recognizes, “by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention.” Usui, 3:29-37. This benefit of limiting the bottommost metal layer of an electrode stack was well-known by August 2009. Moreover, Usui discloses electrode stacks where the bottommost metal layer has a thickness of about 90 to 110 angstroms and the titanium nitride capping layer has a thickness of about 150 to 800 angstroms. Usui, 3:29-32, 4:6-8. A POSITA would have been motivated to apply known techniques of limiting the thickness of Usui underlayer 13 (bottommost metal layer) to diffusion barrier/protection layer 218 (bottommost metal layer) in Yu’s known device ready for improvement to yield predictable results and would have expected success because limiting the thickness of the bottommost metal layer had known benefits and was known in the art—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int’l Co.*, 550 U.S. at 401, 416-17. For example, diffusion barrier layers are layers that were known to prevent metals, such as copper, from diffusion into contacting materials by August 2009. Chin (Innoscence 1414-00176331 - Innoscence 1414-00176340), Abstract. Diffusion barrier layers were known to be formed as a bottommost metal layer of a metallization structure. *Id.*, Abstract, Figs. 1a and 1b, [0020]-[0023]. By August 2009, limiting the thickness of diffusion barrier layers (bottommost metal layers) was well-known. *Id.*, Abstract; Suh (Innoscence 1414-00176341 - Innoscence 1414-00176371), 3:33-37; Chen (Innoscence 1414-00176372 - Innoscence 1414-00176381), 3:9-15. For example, fabricating thin diffusion barrier layers were known

to be advantageous for fabricating devices with smaller feature sizes. Chin, Abstract. Moreover, a POSITA would have understood that a thin diffusion barrier layer is preferred to save costs and fabrication time.

For example, Yu teaches the capping layer may be titanium nitride or tantalum nitride, which are refractory metal nitrides. A POSITA would have been motivated to replace Yu's polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed thicknesses because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation. To the extent Yu does not expressly disclose a refractory metal nitride capping layer having a thickness greater than that of a bottommost layer, Usui does. As Usui recognizes, "by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention." Usui, 3:29-37. This benefit of limiting the bottommost metal layer of an electrode stack was well-known by August 2009. Moreover, Yu expressly discloses that diffusion barrier/protection layer 218 (bottommost layer of plurality of metal layers) (Yu, [0029], Fig. 2E) may be "any suitable thickness." *Id.*, [0029] and [0036]. A POSITA would have been motivated to apply known techniques of limiting the thickness of Usui underlayer 13 (bottommost metal layer) to diffusion barrier/protection layer 218 (bottommost layer) in Yu's known device ready for improvement to yield predictable results and would have expected success because limiting the thickness of the bottommost metal layer had known benefits and was known in the art—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 401, 416-17.

By August 2009, group III-V semiconductor devices were well-known and widely used. For example, group III-nitride semiconductors are essential for developing full-color displays and coherent sources for high-density optical storage technologies. Group III-nitrides were also known to be beneficial for high temperature and high-power electronics applications. Group III-nitrides can support heterostructure technology and have high mechanical and thermal stability. Additionally, GaN was known to have excellent electron transport properties, including good mobility, and high saturated drift velocity. Usui describes its electrical connections are useful to provide connections or wirings between active and/or passive devices of an integrated circuit (Usui, 1:11-15) (i.e., the devices disclosed in Yu, Adesida, and Sugimoto). A POSITA would have been motivated to implement the electrical contacts as taught by Usui in group III-V semiconductor devices, as taught by Yu, Adesida, and Sugimoto, as group III-V semiconductor devices are commonly used in the field for various semiconductor devices and structures—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 416-17. A POSITA would have known of metallization techniques and resulting performance of the metals and metal alloys irrespective of the semiconductors used for the field effect transistor (FET) itself. Because Usui's device provide improved thermal characteristics, thermal stability, and device characteristics in semiconductor devices, it would have been obvious for the POSITA to place the contact of Usui in the III-V semiconductor transistors of Yu, Adesida, and Sugimoto as such materials (i.e., III-V materials) are commonplace within the field and was known in the art. For example, group III-V semiconductor materials have been viewed as promising for semiconductor device applications for at least three

decades prior to the time of the alleged invention (August 25, 2009). Pearton (Innoscence 1414-00009126 - Innoscience 1414-00009508), 2. Group III-V semiconductors include one group III element (Boron (B), Aluminum (Al), Gallium (Ga), and Indium (In)) and one group V element (Nitrogen (N), Phosphorus (P), Arsenic (As), and Antimony (Sb)). Adachi (Innoscence 1414-00174101 - Innoscience 1414-00174130), 6. As members of the III- nitrides (group III-V semiconductors) family, AlN, GaN, InN and their alloys are all wide band-gap materials. Pearton, 2. In view of the available wide range of direct bandgaps, GaN alloyed with AlN and InN may span a continuous range of direct bandgap energies throughout much of the visible spectrum well into the UV wavelengths, which makes the nitride system attractive for optoelectronic device applications, such as LEDs, laser (LDs), and detectors. Pearton, 2. A POSITA knew that the addition of III-nitrides to the family of device-quality semiconductors is essential for developing full-color displays and coherent sources for high-density optical storage technologies. Pearton, 3. Group III-nitrides were also known to be beneficial for high temperature and high-power electronics applications due to their two intrinsic properties: (1) their wide bandgap nature, and (2) their high breakdown fields. Pearton, 3. For example, the wide bandgap materials allow GaN power devices to operate with less cooling and fewer high-cost processing steps associated with complicated structures designed to maximize heat extraction. Pearton, 3. Additionally, GaN was known to have excellent electron transport properties, including good mobility, and high saturated drift velocity. Pearton, 4. These properties make GaN adequate for general electronics, and particularly promising for microwave rectifiers. Pearton, 4. Additionally, group III-nitrides were known to support heterostructure technology. Pearton, 5. Quantum well, modulation-doped hetero-interface, and heterojunction structures can all be made in this system, giving access to new spectral regions for optical devices and new operation regimes for electronic devices. Pearton, 5. Group III-nitrides were also known to have high mechanical and thermal stability. Pearton, 5.

By August 2009, it was well-known that high electron mobility transistors (“HEMTs”) are used for high power and/or high frequency applications. Sheppard (Innoscence 1414-00014701 - Innoscience 1414-00014715), [0004]. HEMTs were the most widely used heterostructure field effect transistors. Mishra 2007 (Innoscence 1414-00007977 - Innoscience 1414-00008559), 375. It had been shown that in HEMTs, the polar charges created at interfaces by piezoelectric and/or spontaneous polarization may also be exploited to create free charge. Mishra 2007, 375. This approach was dominant in nitride-based devices. Mishra 2007, 375. In a HEMT device, a two-dimensional electron gas (2DEG) may be formed at the heterojunction of two semiconductor materials with different bandgap energies. Sheppard, [0004]. The smaller bandgap material may have a higher electron affinity than the wider bandgap material. Sheppard, [0004]. The 2DEG is an accumulation layer in the undoped (“unintentionally doped”) smaller bandgap material and can contain a relatively high sheet electron concentration. Sheppard, [0004]. Additionally, electrons that originate in the wider bandgap semiconductor may transfer to the 2DEG, allowing a relatively high electron mobility due to reduced ionized impurity scattering. Sheppard, [0004]. It was well-known that the combination of relatively high carrier concentration and relatively high carrier mobility gives the HEMT a relatively large transconductance and provide a performance advantage over metal-semiconductor field effect transistors (MESFETS) for high-frequency applications. Sheppard, [0004]. Yu describes the need of providing a semiconductor device with an improved work function. Yu, Abstract. A work function is defined as the amount of energy required to eject electrons from a surface. A POSITA would have

been motivated to implement Yu's device as a HEMT, as taught by Adesida and Sugimoto, because HEMTs were well-known at the time for providing high carrier mobility and therefore improved work function characteristics, as desired by Yu. Furthermore, it was well-known at the time that modifying the Yu device to comprise a HEMT constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications)— combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 416-17. *See* Sheppard, [0004]; Mishra 2007, 375. A POSITA would have known of metallization techniques and resulting performance of the metals and metal alloys irrespective of the semiconductors used for the field effect transistor (FET) itself.

As discussed above, Adesida and Sugimoto are group III-V devices and the use of group III-V devices in HEMTs was well-known. Moreover, a POSITA would have known that the function of the source, drain, and gate would not change if the material changed from silicon to a group III-V material. Group III-V, such as Group III-nitride based, semiconductor devices comprising HEMTs were well-known before the time of the invention. *See, e.g.*, Mishra 2007, Fig. 8.13(a)-(b) at 376, Fig. 8.22 at 393, Fig. 8.29 at 402, 402-403; Mishra 2002 (Innoscence 1414-00007967 - Innoscience 1414-00007976) at 1023-1024; Sheppard, [0044]. "Group III nitride" refers to those semiconducting compounds formed between nitrogen and the elements in Group III of the periodic table, usually aluminum (Al), gallium (Ga), and/or indium (In). Sheppard, [0044]. The term also refers to ternary and quaternary compounds such as AlGa_N and AlInGa_N. Sheppard, [0044]. As had been well understood by a POSITA by August 2009, the Group III elements can combine with nitrogen to form binary (e.g., GaN), ternary (e.g., AlGa_N, AlIn_N), and quaternary (e.g., AlInGa_N) compounds. Sheppard, [0044]. These compounds may all have empirical formulas in which one mole of nitrogen is combined with a total of one mole of the Group III elements. Sheppard, [0044]. Accordingly, formulas such as Al_xGa_{1-x}N, where $0 \leq x \leq 1$, may be used to describe these compounds. Sheppard, [0044]. AlGa_N/GaN (group III-V semiconductor) HEMTs were known to have several benefits in power generation at high frequencies due to the high breakdown field and excellent electron transport properties. Wu 2001 (Innoscence 1414-00010157 - Innoscience 1414-00010161), 586. By the time of the alleged invention, GaN HEMTs were the most widespread and most advanced electronic nitride devices. Quay (Innoscence 1414-00009509 - Innoscience 1414-00010000), 71; Mishra 2002, 1023. HEMTs were known to make full use of heterostructures and the advantageous breakdown and transport properties of undoped GaN. Quay, 71. By the time of the alleged invention, AlGa_N-GaN HEMTs had demonstrated extremely promising results for use in broadband power amplifiers in base station applications due to the high sheet carrier concentration, electron mobility in the 2DEG channel and high saturation velocity. Pearton, 214.

Like Yu, Adesida and Sugimoto teach the use of a III-V semiconductor device. By August 2009, it was well-known that Schottky contacts were of critical importance to device functionality, performance, and long-term reliability. Quay, 144. It was well-known that Schottky contacts serve as gate contacts in group III-V devices, have a fast response for many applications due to their unipolar carrier transport, and have excellent rectifying properties, which make them suitable for high frequency applications. Krämer (Innoscence 1414-00007816 - Innoscience 1414-00007966), 87. Yu describes the need of providing a semiconductor device with an improved work

function. Yu, Abstract. A work function is defined as the amount of energy required to eject electrons from a surface. A POSITA would have been motivated to implement Yu's device as a gate electrode making a Schottky contact, as taught by Adesida and Sugimoto, because Schottky contacts were well-known at the time for providing a fast response for many applications due to their unipolar carrier transport (Mishra 2007, 219) and because Yu, Adesida, and Sugimoto disclose the use of III-V semiconductor devices. Furthermore, modifying the Yu device to include a Schottky contact constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications)—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 416-17. For example, Schottky contacts were known to have a fast response since carrier transport is unipolar. Mishra 2007, 219. Schottky contacts were known to serve as the gate contacts in group III-V (e.g., $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$) HEMTs. Krämer, 1, 87. In these applications, Schottky contacts should have a high breakdown voltage and a low reverse current. Krämer, 2, 87.

Adesida explains that its device is a “high electron mobility transistor (HEMT), which is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT).” Adesida, [0031]. InP and GaAs are well-known group III-V materials. *See* Adachi, 6. A HEMT is an active semiconductor device which Yu and Usui explicitly state its electrical contacts are suitable for (Yu, [0023], [0040]; Usui, 1:11-15). It would have been obvious to implement the electrical contacts of Yu and Usui on HEMTs, as taught by Adesida, because both Yu and Adesida disclose III-V semiconductor devices.

Adesida discloses “a field-effect device, comprising: a layered semiconductor structure that includes a channel layer and at least one layer over the channel layer; spaced apart source and drain contacts disposed over said at least one layer and communicating with the channel layer; and an iridium gate, between the source and drain contacts, **forming a Schottky barrier contact on said at least one layer.**” Adesida, [0016] (emphasis added).

Adesida discloses a HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105, on which is an **$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150 (group III-V semiconductor device)**. InAlAs is a well-known group III-V material. Adesida, Fig. 5 and [0031]; *see* Adachi, 6. **Gate 190 (gate electrode)** is formed as a **Schottky barrier contact (Schottky contact)** on the **$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150 (group III-V semiconductor device)**. Adesida, Fig. 5 and [0031].

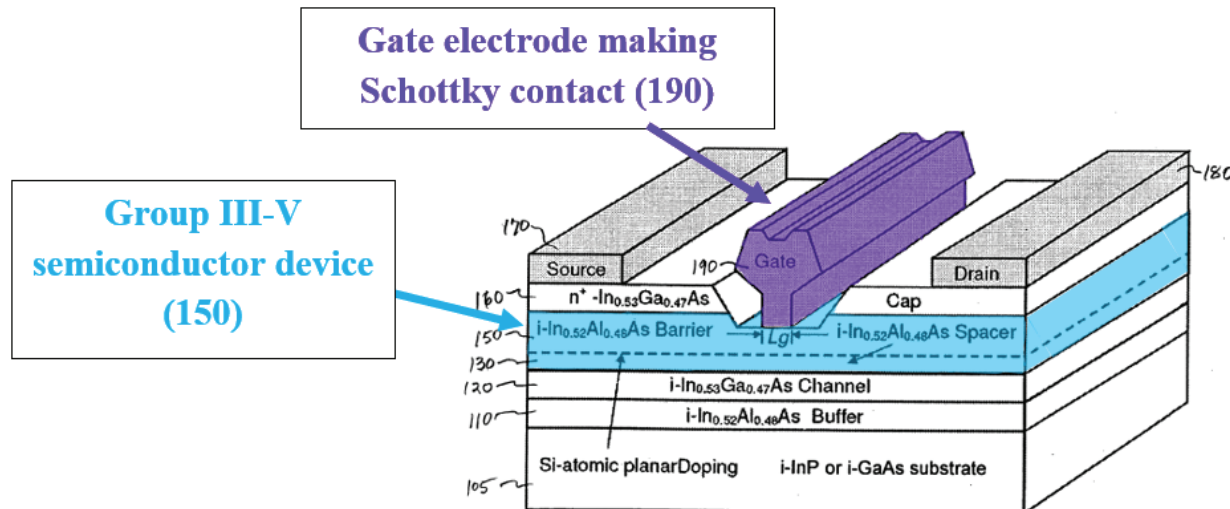


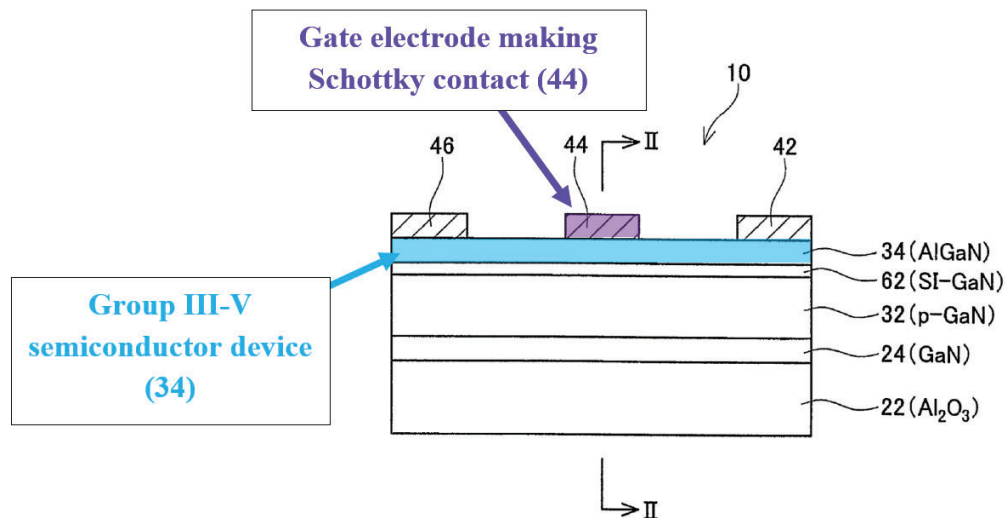
Figure 5

Adesida, Fig. 5 (annotated). It would have been obvious to implement the electrical contacts of Yu and Usui in a device with a gate electrode making Schottky contact, as taught by Adesida, as discussed above.

For example, like Yu, Sugimoto discloses a group III-V semiconductor device (Sugimoto, 9:7-9). Sugimoto further discloses a device with an AlGaIn top layer. Sugimoto, Figs. 1, 3, 5, 7. AlGaIn is a well-known group III-V material. *See* Adachi, 6. Sugimoto further discloses the III-V semiconductor device is a HEMT. Sugimoto, title, 1:22-67. A HEMT is a semiconductor device which Yu and Usui explicitly state its electrical contacts are suitable for (Usui, 5:11-16; Yu, [0023], [0040]). It would have been obvious to implement the electrical contacts of Yu and Usui on HEMTs, as taught by Sugimoto, because both Yu and Sugimoto disclose III-V semiconductor devices.

Sugimoto discloses “[t]he gate electrode 44 directly contacts with the top surface of the AlGaIn layer 34, and **forms a Schottky contact with the AlGaIn layer 34.**” Sugimoto, 9:39-51 (emphasis added).

Sugimoto discloses a HEMT formed on AlGaIn layer 34 (group III-V semiconductor device). AlGaIn is a well-known group III-V material. Sugimoto, Fig. 1, title, 9:39-51; *see* Adachi, 6. Gate electrode 44 (gate electrode) is formed as a Schottky contact (Schottky contact) on the AlGaIn layer 34 (group III-V semiconductor device). Sugimoto, Fig. 1 and 9:39-51.



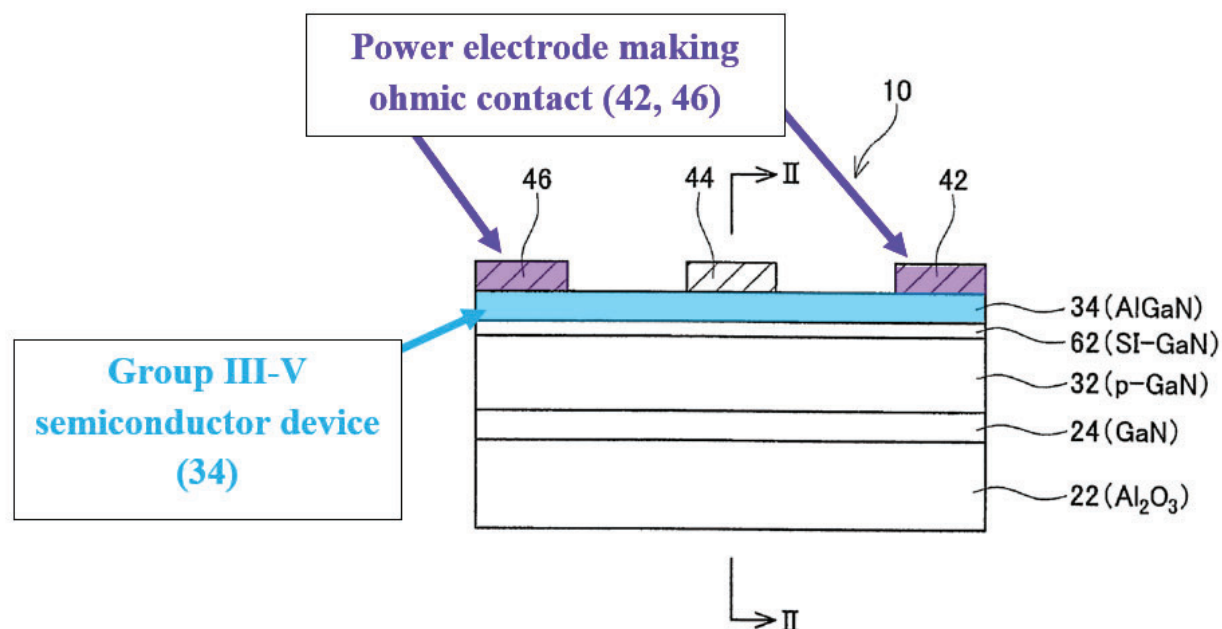
Sugimoto, Fig. 1 (annotated). It would have been obvious to implement the electrical contacts of Yu and Usui in a device with a gate electrode making Schottky contact, as taught by Sugimoto, as discussed above.

For example, by August 2009, it was well-known that ohmic contacts were of critical importance with respect to device functionality, performance, and long-term reliability. Quay, 144. It was well-known that ohmic contacts serve as source and drain contacts in group III-V devices and allow current to flow into and out of a semiconductor material without distortion of the signal. Voss (Innoscence 1414-00010001 - Innoscence 1414-00010144), 22; Krämer, 1. It was well-known that the most critical component of an ohmic contact is its low specific contact resistance, which minimizes the power consumption of the contact and the internal heating of the contact, thereby prolonging device operation with predictable performance. Voss, 22. Furthermore, ohmic contacts allow charges to flow easily between conductors without excess power dissipation, have linear current-voltage characteristics, and do not introduce voltage drops or power loss. Neaman (Innoscence 1414-00008560 - Innoscence 1414-00009125), 344. Such characteristics are essential for high-frequency operation used by devices such as the HEMT of Sugimoto. *See* Pearton, 214; Sheppard, [0004], [0044]; Mishra 2007, 229, 375, 376, 393, 402-403; Wu 2001, 586; Quay, 71, 145, 144; Mishra 2002 at 1023-1024; Neaman, 344; Voss, 22; Krämer, 32. Usui disclosed the importance of enhanced electromigration. Usui, Abstract. A POSITA would have been motivated to implement the contacts of Yu and Usui as a power electrode making an ohmic contact, as taught by Adesida and Sugimoto because such a combination would provide improved current flow (i.e., enhanced electromigration) and Adesida and Sugimoto, like Yu, also teach the use of III-V semiconductor devices. Furthermore, such a combination is the result of combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, at 416-17; Adesida, [0031], Fig. 5; Sugimoto, 9:39-

51, Fig. 1. It would have been obvious to implement the electrical contacts of Yu and Usui as a power electrode making an ohmic contact, as taught by Adesida and Sugimoto because Yu, Adesida, and Sugimoto disclose III-V semiconductor devices and ohmic contacts were typically employed in high-frequency operation devices, such as a HEMT. *See* Pearton, 214; Sheppard, [0004], [0044]; Mishra 2007, 229, 375, 376, 393, 402-403; Wu 2001, 586; Quay, 71, 144-145; Mishra 2002, 1023-1024; Neaman, 344; Voss, 22; Krämer, 1, 32.

Sugimoto is analogous to the '562 patent because it is in the same field of endeavor, forming electrical contacts for semiconductor devices (Sugimoto, 9:24-51; '562, Abstract), and addresses the same problem of providing enhanced or simplified fabrication as the '562 patent (Sugimoto, 6:3-7:12, 7:26-39, 7:56-60, 8:30-44). The '562 patent defines “[s]ource electrode 136 and drain electrode 138 are power electrodes ohmically coupled to the heterojunction formed by GaN layer 112 and AlGaN layer 114.” '562 patent, 3:19-21. Consistent with the '562 patent, Sugimoto discloses a gate electrode making Schottky contact with a group III-V device and power electrodes (source and drain electrodes) making ohmic contact with the group III-V device. Sugimoto, 9:39-51. Sugimoto discloses that its “**drain electrode 42 and the source electrode 46 make ohmic contact with the top surface of the AlGaN layer 34.**” Sugimoto, 9:39-51 (emphasis added).

Sugimoto discloses that its “**drain electrode 42 (power electrode)** and the **source electrode 46 (power electrode)** make **ohmic contact** with the top surface of the **AlGaN layer 34 (group III-V semiconductor device)**.” (Sugimoto, 9:39-51).



Sugimoto, Fig. 1 (annotated). It would have been obvious to implement the electrical contacts of Yu and Usui as a power electrode making an ohmic contact, as taught by Sugimoto because both Yu and Sugimoto disclose III-V semiconductor devices and ohmic contacts were typically employed in high-frequency operation devices, such as a HEMT. *See* Pearton, 214; Sheppard, [0004], [0044]; Mishra 2007, 229, 375, 376, 393, 402-403; Wu 2001, 586; Quay, 71, 144-145; Mishra 2002, 1023-1024; Neaman, 344; Voss, 22; Krämer, 1, 32.

Adesida discloses “Spaced apart **source 170** and **drain 180 ohmic contacts** are formed on the n⁺ In_{0.53}Ga_{0.47}As cap layer **160**.” Adesida, [0031] (emphasis added).

Adesida discloses a HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105, on which is an **In_{0.52}Al_{0.48}As barrier layer 150 (group III-V semiconductor device)**. InAlAs is a well-known group III-V material. Adesida, Fig. 5 and [0031]; *see* Adachi, 6. **Source 170** and **drain 180 ohmic contacts (power electrodes)** make **ohmic contact** with the **n⁺ In_{0.53}Ga_{0.47}As cap layer 160** and **In_{0.52}Al_{0.48}As barrier layer 150 (group III-V semiconductor device)**. Adesida, Fig. 5 and [0031].

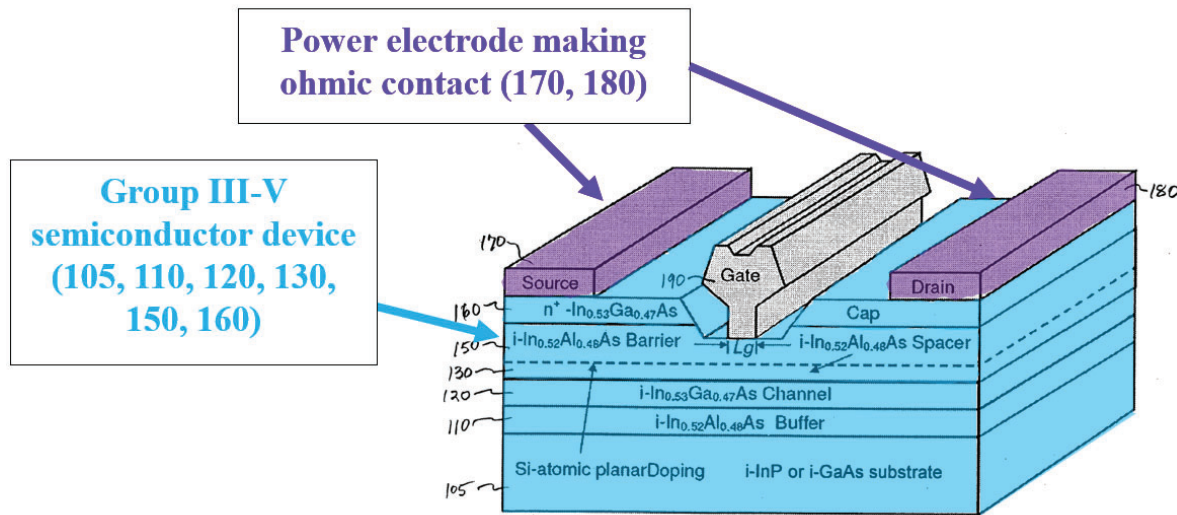
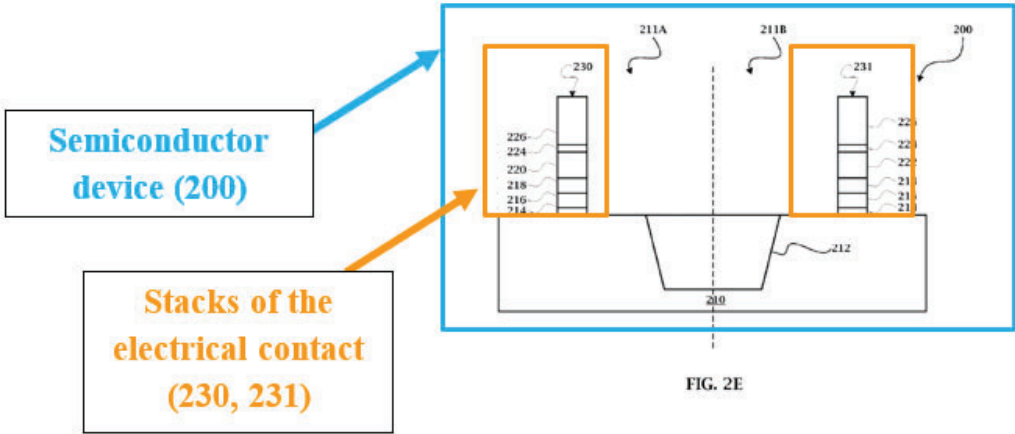


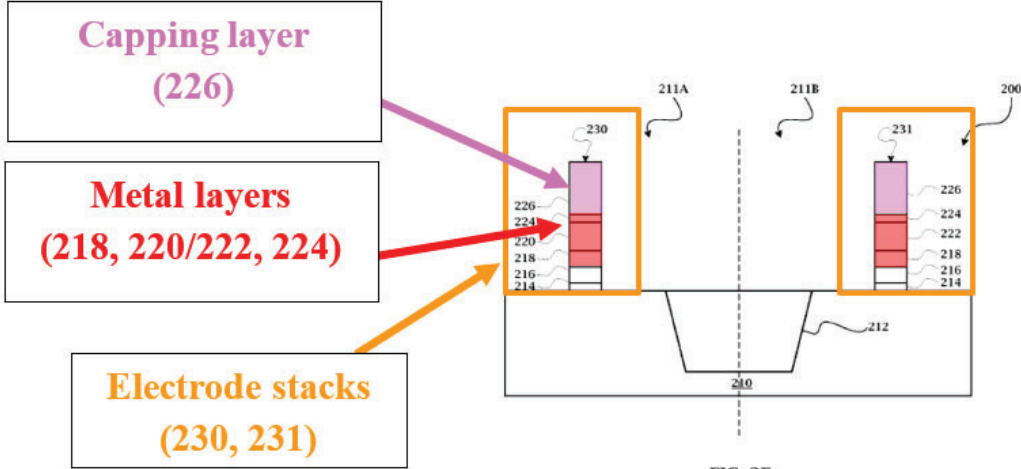
Figure 5

Adesida, Fig. 5 (annotated). It would have been obvious to implement the electrical contacts of Yu and Usui as a power electrode making an ohmic contact, as taught by Adesida because both Yu and Adesida disclose III-V semiconductor devices and ohmic contacts were typically employed in high-frequency operation devices, such as a HEMT. See Pearton, 214; Sheppard, [0004], [0044]; Mishra 2007, 229, 375, 376, 393, 402-403; Wu 2001, 586; Quay, 71, 144-145; Mishra 2002, 1023-1024; Neaman, 344; Voss, 22; Krämer, 1, 32.

Claim 1	Exemplary Disclosure based on Yu and Related Combinations
[1p] An electrical contact for use on a semiconductor device, said electrical contact comprising:	Yu, alone or in combination with one or more references, discloses and/or renders obvious an electrical contact for use on a semiconductor device, said electrical contact comprising. For example, Yu discloses the following, at [0040]: It is understood that the semiconductor device 200 may undergo further CMOS or MOS technology processing to form various features known in the art. For example, gate sidewall spacers may be formed on both sides of the metal gate stacks 230, 231 by a deposition and etching process. In some embodiments, lightly doped regions (referred to as LDD regions) may be formed in the substrate 210 using any suitable process, such as ion implantation, and any suitable dopants. In another example, source and drain regions (referred to as S/D regions) may be formed in the substrate 210 using ion implantation or diffusion with suitable dopants (depending on the configuration of the device such as NMOS and PMOS) and located proximate to each end of the metal gate stacks 230, 231 (the high-k gate dielectric and metal gate electrode), respectively. In still another example, various contacts/vias and multilayer interconnect features (e.g., metal layers and interlayer dielectrics) may be formed on the substrate 210 and configured to connect the various features or structures of the semiconductor device 200. Yu discloses the following, at Fig. 2E (annotated):

Claim 1	Exemplary Disclosure based on Yu and Related Combinations
	 FIG. 2E
[1a] an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;	Yu, alone or in combination with one or more references, discloses and/or renders obvious an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers. For example, Yu discloses the following, at [0029]: In some embodiments, a diffusion barrier/protection layer 218 is formed over the high-k dielectric layer 216. The diffusion barrier/protection layer 218 may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present embodiment, the diffusion barrier/protection layer 218 comprises TiN, which is deposited by PVD to a thickness of approximately 20 Å. In alternate embodiments, the diffusion barrier/protection layer may be formed by any suitable process, such as CVD, PVD, ALD, thermal oxide, plating, and/or combinations thereof. Further, in alternate embodiments, the diffusion barrier layer 218 comprises any suitable thickness. It is understood that the diffusion barrier layer 218 may be omitted in alternate embodiments.

Claim 1	Exemplary Disclosure based on Yu and Related Combinations
	Yu discloses the following, at [0035]: A diffusion barrier layer 224 may be formed over the semiconductor device 200, particularly, metal layers 220, 222 as illustrated in FIG. 2D. The diffusion barrier layer may comprise titanium, titanium nitride, tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present embodiment, the diffusion barrier layer 224 comprises TiN, which is deposited by PVD to a thickness of approximately 50 Å. In alternate embodiments, the diffusion barrier layer may be formed by any suitable process, such as CVD, PVD, ALD, thermal oxide, plating, and/or combinations thereof. Further, in alternate embodiments, the diffusion barrier layer 224 comprises any suitable thickness. It is understood that the diffusion barrier layer 224 may be omitted for alternate embodiments. Yu discloses the following, at [0036]: At step 110, referring to FIGS. 1 and 2D, a capping layer 226 is formed over the metal layers 220, 222, and in the present embodiment, over the diffusion barrier layer 224. The capping layer 226 may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer 226 comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer 226 may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer 226 may comprise any suitable thickness. The capping layer 226 may be formed by CVD, PVD, ALD, thermal oxide, plating, other suitable processes, and/or combinations thereof. In some embodiments, the capping layer 226 comprises aluminum and/or tungsten. For example, in some embodiments, the capping layer 226 comprises aluminum formed by CVD. It is understood that, in alternate embodiments, the capping layer 226 may comprise multilayer structures. Yu discloses the following, at Fig. 2E (annotated):

Claim 1	Exemplary Disclosure based on Yu and Related Combinations
	 FIG. 2E
[1b] said capping layer consisting only of a refractory metal nitride,	Yu, alone or in combination with one or more references, discloses and/or renders obvious said capping layer consisting only of a refractory metal nitride. For example, Yu discloses the following, at [0036]: At step 110, referring to FIGS. 1 and 2D, a capping layer 226 is formed over the metal layers 220, 222, and in the present embodiment, over the diffusion barrier layer 224. The capping layer 226 may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer 226 comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer 226 may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å,

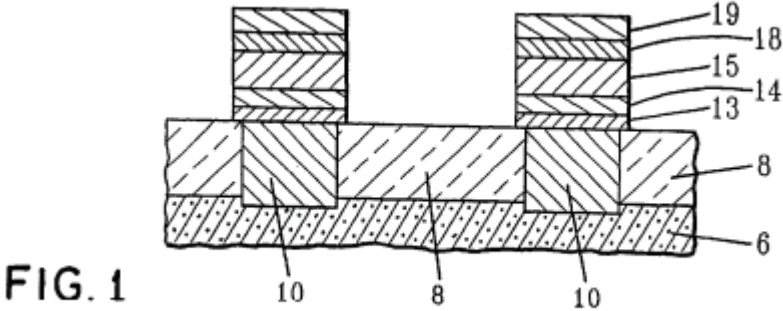
Claim 1	Exemplary Disclosure based on Yu and Related Combinations
	preferably about 200 Å. In alternate embodiments, the capping layer 226 may comprise any suitable thickness. The capping layer 226 may be formed by CVD, PVD, ALD, thermal oxide, plating, other suitable processes, and/or combinations thereof. In some embodiments, the capping layer 226 comprises aluminum and/or tungsten. For example, in some embodiments, the capping layer 226 comprises aluminum formed by CVD. It is understood that, in alternate embodiments, the capping layer 226 may comprise multilayer structures.
[1c] said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.	Yu, alone or in combination with one or more references, discloses and/or renders obvious said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers. For example, Yu discloses the following, at [0029]: In some embodiments, a diffusion barrier/protection layer 218 is formed over the high-k dielectric layer 216. The diffusion barrier/protection layer 218 may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present embodiment, the diffusion barrier/protection layer 218 comprises TiN, which is deposited by PVD to a thickness of approximately 20 Å. In alternate embodiments, the diffusion barrier/protection layer may be formed by any suitable process, such as CVD, PVD, ALD, thermal oxide, plating, and/or combinations thereof. Further, in alternate embodiments, the diffusion barrier layer 218 comprises any suitable thickness. It is understood that the diffusion barrier layer 218 may be omitted in alternate embodiments. Yu discloses the following, at [0036]: At step 110, referring to FIGS. 1 and 2D, a capping layer 226 is formed over the metal layers 220, 222, and in the present embodiment, over the diffusion barrier layer 224. The capping layer 226 may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In

Claim 1	Exemplary Disclosure based on Yu and Related Combinations
	the present embodiment, the capping layer 226 comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer 226 may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer 226 may comprise any suitable thickness. The capping layer 226 may be formed by CVD, PVD, ALD, thermal oxide, plating, other suitable processes, and/or combinations thereof. In some embodiments, the capping layer 226 comprises aluminum and/or tungsten. For example, in some embodiments, the capping layer 226 comprises aluminum formed by CVD. It is understood that, in alternate embodiments, the capping layer 226 may comprise multilayer structures. Yu discloses the following, at [0039]: In one example, for patterning the metal gate stacks 230, 231, a layer of photoresist is formed over the capping layer 226 by a suitable process, such as spin-on coating, and then patterned to form a patterned photoresist feature by a proper lithography patterning method. The pattern of the photoresist can then be transferred by a dry etching process to the underlying layers (i.e., the interfacial dielectric layer 214, the high-k dielectric layer 216, the diffusion barrier/protection layer 218, the first metal layer 220, the second metal layer 222, the diffusion barrier layer 224, and the capping layer 226) to form the metal gate stacks 230, 231 as shown in FIG. 2E. The photoresist layer may be stripped thereafter. In another example, a hard mask layer is formed over the capping layer 226; a patterned photoresist layer is formed on the hard mask layer; the pattern of the photoresist layer is transferred to the hard mask layer and then transferred to the electrode layers to form the electrode layers and dielectric layers of the gate structures. It is understood that the above examples do not limit the processing steps that may be utilized to form the metal gate stacks 230, 231. Yu discloses the following, at [0040]: It is understood that the semiconductor device 200 may undergo further CMOS or MOS technology processing to form various features known in the art. For example, gate sidewall spacers may be formed on both sides of the metal gate stacks 230, 231 by a deposition and etching process. In some embodiments, lightly doped regions (referred to as LDD regions) may be formed in

Claim 1	Exemplary Disclosure based on Yu and Related Combinations
	the substrate 210 using any suitable process, such as ion implantation, and any suitable dopants. In another example, source and drain regions (referred to as S/D regions) may be formed in the substrate 210 using ion implantation or diffusion with suitable dopants (depending on the configuration of the device such as NMOS and PMOS) and located proximate to each end of the metal gate stacks 230, 231 (the high-k gate dielectric and metal gate electrode), respectively. In still another example, various contacts/vias and multilayer interconnect features (e.g., metal layers and interlayer dielectrics) may be formed on the substrate 210 and configured to connect the various features or structures of the semiconductor device 200. Yu discloses the following, at Fig. 2E (annotated): The diagram, labeled FIG. 2E, shows a cross-sectional view of a semiconductor device 200. A substrate 210 is shown with a trench 212. Two gate stacks, 230 and 231, are formed on the substrate. Each gate stack consists of a capping layer 226, a bottommost layer 218, and intermediate layers 224, 222, 216, and 214. Arrows point from the text labels to the corresponding layers in the diagram. This limitation is obvious in view of Yu and Usui. Usui discloses the following, at 5:49-65: Onto the aluminum-copper interconnect metallization 15 is then deposited about 50 to about 250 angstroms of a group IVA metal, preferably titanium, as layer 18 similar to the previously

Claim 1	Exemplary Disclosure based on Yu and Related Combinations
	deposited metal layer 13 discussed above. Deposition and composition of layer 18 can be carried out in the same way as for layer 13. From FIG. 5, onto the metal layer 18 is then blanket deposited the suitable capping layer 19 to complete the interconnect metallurgy at this level. The capping layer is preferably titanium nitride and can be deposited in the same manner as the titanium nitride layer 14. The purpose of this layer is to limit the amount of light reflection during the subsequent photoresist steps and to act as a protective layer against corrosion during subsequent processing. Therefore, any layer which would similarly satisfy the requirements of reducing the amount of light reflection and provide protective anodic capping during subsequent processing would be usable for this layer. Usui discloses the following at Abstract: A metallization structure is fabricated by depositing an underlayer of a group IVA metal having a thickness of about 90 to about 110 angstroms, and depositing a layer of aluminum and/or an aluminum alloy. The metallization structure obtained exhibits enhanced electromigration and is highly textured and is especially suitable for forming electrical connections or wiring. Usui discloses the following, at 1:5-14: The present invention is concerned with a method for fabricating a metallization structure and is especially concerned with producing a structure having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics. Moreover, the process of the present invention provides highly textured aluminum <111> layers. The structures fabricated by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure. Usui discloses the following, at 2:33-39: However, there still remains room for improvement of the electromigration characteristics. Accordingly, an objective of the present invention is to provide a structure that exhibits enhanced electromigration performance along with being hillock free and without a

Claim 1	Exemplary Disclosure based on Yu and Related Combinations
	concomitant loss in the dry etchability characteristic and corrosion resistant characteristic of the structure. Usui discloses the following, at 3:22-37: FIG. 1 is a cross-sectional view of the preferred embodiment of an interconnect metallurgy structure according to the present invention. Referring to FIG. 1, the interconnect metallurgy preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 to make connection to a device substrate 6. The metallurgy structure includes an underlayer of a group IVA metal and preferably a layer of titanium. Critical to the success of the present invention is having the thickness of this underlayer 13 being between about 90 angstroms to about 110 angstroms. As will be demonstrated hereinbelow, by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention. Usui discloses the following at 3:56-4:9: Also, although not required, according to preferred aspects of the present invention a capping layer is provided above layer 15. The capping layer when present, enhances the lithographic processing since it acts as an anti-reflective layer aiding in controlling line width. Preferred capping layers are titanium nitride and combinations of as layer 18 of a group IVA metal, preferably titanium with a titanium nitride layer 19. Typically the titanium nitride layer is about 150 to about 800 angstroms and more typically about 200 to about 500 angstroms. Typically, the titanium layer is about 50 angstroms to about 200 angstroms. Usui discloses the following, at 5:34-39: Referring now to FIG. 3, following the deposition of the layer 13, a titanium nitride layer 14 is formed by sputter deposition of titanium nitride to the desired thickness. Titanium nitride layer 14 may be formed in the same chamber used for deposition of the titanium layer 13 or in a different apparatus.

Claim 1	Exemplary Disclosure based on Yu and Related Combinations
	Usui discloses the following, at 3:2-8: FIG. 1 is a cross-sectional view of a preferred embodiment of an interconnect metallurgy according to the present invention. FIGS. 2-8 are a cross-sectional view of the process for fabricating the preferred interconnect metallurgy of the present invention in a step-by-step fashion. Usui discloses the following, at Fig. 1:  FIG. 1 Usui discloses the following, at Fig. 8 (annotated):

Claim 1	Exemplary Disclosure based on Yu and Related Combinations
	FIG. 8 See also Chin, Abstract, Figs. 1a and 1b, [0020]-[0023]; Suh, 3:33-37; Chen, 3:9-15.

Claim 2	Exemplary Disclosure based on Yu and Related Combinations
[2p] The electrical contact of claim 1,	Yu, alone or in combination with one or more references, discloses and/or renders obvious the electrical contact of claim 1. <i>See supra</i> claim 1.
[2a] wherein said capping layer comprises titanium nitride (TiN).	Yu, alone or in combination with one or more references, discloses and/or renders obvious wherein said capping layer comprises titanium nitride (TiN). For example, Yu discloses the following, at [0036]: At step 110, referring to FIGS. 1 and 2D, a capping layer 226 is formed over the metal layers 220, 222, and in the present embodiment, over the diffusion barrier layer 224. The capping layer 226 may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium,

Claim 2	Exemplary Disclosure based on Yu and Related Combinations
	tantulum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer 226 comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer 226 may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer 226 may comprise any suitable thickness. The capping layer 226 may be formed by CVD, PVD, ALD, thermal oxide, plating, other suitable processes, and/or combinations thereof. In some embodiments, the capping layer 226 comprises aluminum and/or tungsten. For example, in some embodiments, the capping layer 226 comprises aluminum formed by CVD. It is understood that, in alternate embodiments, the capping layer 226 may comprise multilayer structures. Usui discloses the following, at 5:49-65: Onto the aluminum-copper interconnect metallization 15 is then deposited about 50 to about 250 angstroms of a group IVA metal, preferably titanium, as layer 18 similar to the previously deposited metal layer 13 discussed above. Deposition and composition of layer 18 can be carried out in the same way as for layer 13. From FIG. 5, onto the metal layer 18 is then blanket deposited the suitable capping layer 19 to complete the interconnect metallurgy at this level. The capping layer is preferably titanium nitride and can be deposited in the same manner as the titanium nitride layer 14. The purpose of this layer is to limit the amount of light reflection during the subsequent photoresist steps and to act as a protective layer against corrosion during subsequent processing. Therefore, any layer which would similarly satisfy the requirements of reducing the amount of light reflection and provide protective anodic capping during subsequent processing would be usable for this layer. <i>See also</i> Bauccio, 120; Cockeram, 1; Preuss, 2; Pierson, 156-157, 160; Kim, 46, 56; Suh, 3:39-43; Chen, Abstract, 1:58-61; Fair, Abstract, 1:29-34, 2:47-51.

Claim 8	Exemplary Disclosure based on Yu and Related Combinations
[8p] The electrical contact of claim 1,	Yu, alone or in combination with one or more references, discloses and/or renders obvious the electrical contact of claim 1. <i>See supra</i> claim 1.
[8a] wherein said electrical contact is configured for implementation on a group III-V semiconductor device.	Yu, alone or in combination with one or more references, discloses and/or renders obvious wherein said electrical contact is configured for implementation on a group III-V semiconductor device. For example, Yu discloses the following, at [0023]: The semiconductor substrate 210 may comprise an elementary semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and GaInAsP; any other suitable material; and/or combinations thereof. In one embodiment, the alloy semiconductor substrate may have a gradient SiGe feature in which the Si and Ge composition change from one ratio at one location to another ratio at another location of the gradient SiGe feature. In another embodiment, the alloy SiGe is formed over a silicon substrate. In another embodiment, a SiGe substrate is strained. Furthermore, the semiconductor substrate may be a semiconductor on insulator, such as a silicon on insulator (SOI), or a thin film transistor (TFT). In some examples, the semiconductor substrate may include a doped epi layer or a buried layer. In other examples, the compound semiconductor substrate may have a multilayer structure, or the silicon substrate may include a multilayer compound semiconductor structure. In the present embodiment, the semiconductor substrate 210 comprises silicon, germanium, a group III-V material, or a group II-VI material. Yu discloses the following, at Fig. 2E (annotated):

Claim 8	Exemplary Disclosure based on Yu and Related Combinations
	FIG. 2E

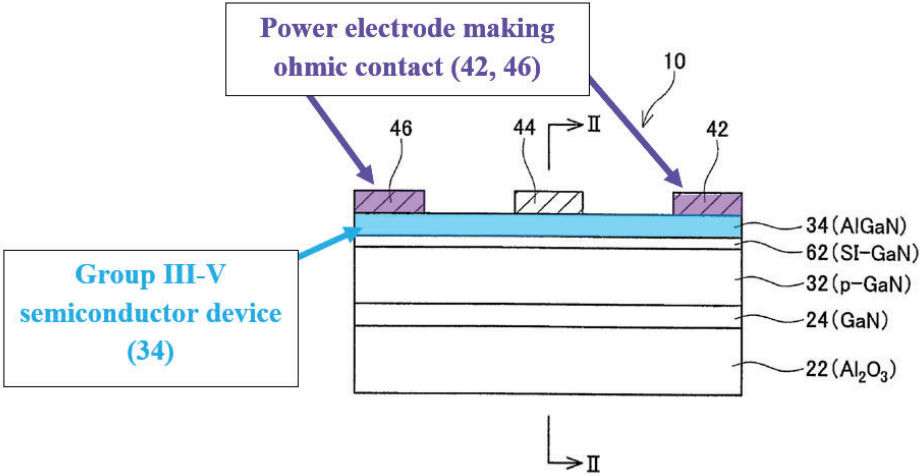
Claim 9	Exemplary Disclosure based on Yu and Related Combinations
[9p] The electrical contact of claim 8,	Yu alone or in combination with one or more references discloses and/or renders obvious the electrical contact of claim 8. <i>See supra</i> claim 8.
[9a] wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).	Yu, alone or in combination with one or more references, discloses and/or renders obvious wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT). For example, Yu discloses the following, at [0023]: The semiconductor substrate 210 may comprise an elementary semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and GaInAsP; any other suitable material; and/or

Claim 9	Exemplary Disclosure based on Yu and Related Combinations
	combinations thereof. In one embodiment, the alloy semiconductor substrate may have a gradient SiGe feature in which the Si and Ge composition change from one ratio at one location to another ratio at another location of the gradient SiGe feature. In another embodiment, the alloy SiGe is formed over a silicon substrate. In another embodiment, a SiGe substrate is strained. Furthermore, the semiconductor substrate may be a semiconductor on insulator, such as a silicon on insulator (SOI), or a thin film transistor (TFT). In some examples, the semiconductor substrate may include a doped epi layer or a buried layer. In other examples, the compound semiconductor substrate may have a multilayer structure, or the silicon substrate may include a multilayer compound semiconductor structure. In the present embodiment, the semiconductor substrate 210 comprises silicon, germanium, a group III-V material, or a group II-VI material. This limitation is obvious in view of Yu and Adesida; obvious in view of Yu, Usui, and Adesida; obvious in view of Yu and Sugimoto; and obvious in view of Yu, Usui, and Sugimoto. Usui discloses the following, at 1:5-14: The present invention is concerned with a method for fabricating a metallization structure and is especially concerned with producing a structure having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics. Moreover, the process of the present invention provides highly textured aluminum <111> layers. The structures fabricated by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure. Adesida discloses the following, at [0031]: FIG. 5 shows, in cross-section, an example of a type of device that can be utilized in practicing a form of the invention. The device of FIG. 5 is a high electron mobility transistor (HEMT), which, in this example, is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT) on which is deposited an insulating $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer layer. In this diagram, there is shown an undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel layer 120, and, over this layer,

Claim 9	Exemplary Disclosure based on Yu and Related Combinations
	a spacer layer 130 of undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$, a thin Si-atomic planar doping region, and an undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150, and, except in the notched central region, a heavily doped n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer 160. Spaced apart source 170 and drain 180 ohmic contacts are formed on the n^+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer 160, and the gate 190, which is shown as a T-gate in this example, is formed with a Schottky barrier contact of length L_g on the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150. Sugimoto discloses the following, at title: III-V HEMT DEVICES. Sugimoto discloses the following, at 1:55-58: The on-resistance here means a magnitude of resistance between the drain electrode and the source electrode while the predetermined gate voltage is applied to the gate electrode of HEMT. <i>See also</i> Sheppard, [0004], [0044]; Mishra 2007, 375, 376, 393, 402-403; Mishra 2002, 1023-1024; Wu 2001, 586; Quay, 71; Pearton, 214.

Claim 10	Exemplary Disclosure based on Yu and Related Combinations
[10p] The electrical contact of claim 8,	Yu, alone or in combination with one or more references, discloses and/or renders obvious the electrical contact of claim 8. <i>See supra</i> claim 8.
[10a] wherein said electrical contact is implemented as a power electrode making ohmic contact with said	Yu, alone or in combination with one or more references, discloses and/or renders obvious wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device. For example,

Claim 10	Exemplary Disclosure based on Yu and Related Combinations
group III-V semiconductor device.	Yu discloses the following, at [0023]: The semiconductor substrate 210 may comprise an elementary semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and GaInAsP; any other suitable material; and/or combinations thereof. In one embodiment, the alloy semiconductor substrate may have a gradient SiGe feature in which the Si and Ge composition change from one ratio at one location to another ratio at another location of the gradient SiGe feature. In another embodiment, the alloy SiGe is formed over a silicon substrate. In another embodiment, a SiGe substrate is strained. Furthermore, the semiconductor substrate may be a semiconductor on insulator, such as a silicon on insulator (SOI), or a thin film transistor (TFT). In some examples, the semiconductor substrate may include a doped epi layer or a buried layer. In other examples, the compound semiconductor substrate may have a multilayer structure, or the silicon substrate may include a multilayer compound semiconductor structure. In the present embodiment, the semiconductor substrate 210 comprises silicon, germanium, a group III-V material, or a group II-VI material. This limitation is obvious in view of Yu and Adesida; obvious in view of Yu, Usui, and Adesida; obvious in view of Yu and Sugimoto; and obvious in view of Yu, Usui, and Sugimoto. Usui discloses the following, at 1:5-14: The present invention is concerned with a method for fabricating a metallization structure and is especially concerned with producing a structure having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics. Moreover, the process of the present invention provides highly textured aluminum <111> layers. The structures fabricated by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure.

Claim 10	Exemplary Disclosure based on Yu and Related Combinations
	Sugimoto discloses the following, at 9:39-51: A gate electrode 44 (an example of an electrode) formed from a stacked structure of nickel (Ni) and gold (Au) is located at a center, relative to the page, of a top surface of the AlGaN layer 34. The gate electrode 44 directly contacts with the top surface of the AlGaN layer 34, and forms a Schottky contact with the AlGaN layer 34. A drain electrode 42 and a source electrode 46, both formed from a stacked structure of titanium (Ti) and aluminum (Al), are disposed at left and right sides relative to the page, with the gate electrode 44 being located between the two. The drain electrode 42 and the source electrode 46 make ohmic contact with the top surface of the AlGaN layer 34. The SI-GaN layer 62 is essentially formed from an intrinsic type semiconductor layer. Sugimoto discloses the following at Fig. 1, (annotated):  Adesida discloses the following, at [0031]:

Claim 10	Exemplary Disclosure based on Yu and Related Combinations
	FIG. 5 shows, in cross-section, an example of a type of device that can be utilized in practicing a form of the invention. The device of FIG. 5 is a high electron mobility transistor (HEMT), which, in this example, is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT) on which is deposited an insulating $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer layer. In this diagram, there is shown an undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel layer 120, and, over this layer, a spacer layer 130 of undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$, a thin Si-atomic planar doping region, and an undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150, and, except in the notched central region, a heavily doped n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer 160. Spaced apart source 170 and drain 180 ohmic contacts are formed on the n^+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer 160, and the gate 190, which is shown as a T-gate in this example, is formed with a Schottky barrier contact of length L_g on the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150. Adeseida discloses the following, at Fig. 5 (annotated):

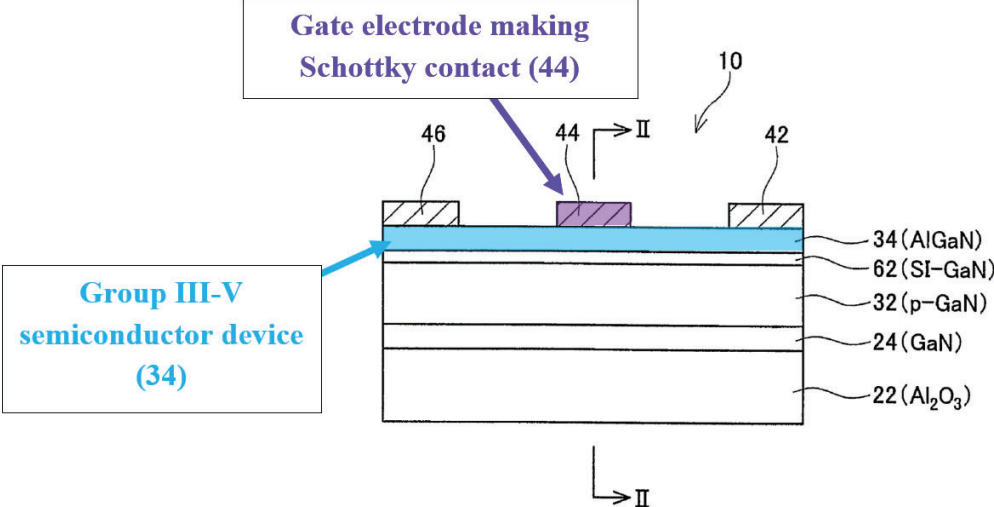
Claim 10	Exemplary Disclosure based on Yu and Related Combinations
	Power electrode making ohmic contact (170, 180) Group III-V semiconductor device (105, 110, 120, 130, 150, 160) <i>Figure 5</i> See also Quay, 71, 144, 145; Voss, 22; Krämer, 1, 32; Neaman, 344; Pearton, 214; Sheppard, [0004], [0044]; Mishra 2007, 229, 375, 376, 393, 402-403; Wu 2001, 586; Mishra 2002 at 1023-1024.

Claim 11	Exemplary Disclosure based on Yu and Related Combinations
[11p] The electrical contact of claim 8,	Yu, alone or in combination with one or more references, discloses and/or renders obvious the electrical contact of claim 8. <i>See supra</i> claim 8.
[11a] wherein said electrical contact is implemented as a gate electrode making Schottky	Yu, alone or in combination with one or more references, discloses and/or renders obvious wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

Claim 11	Exemplary Disclosure based on Yu and Related Combinations
contact with said group III-V semiconductor device.	For example, Yu discloses the following, at [0023]: The semiconductor substrate 210 may comprise an elementary semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and GaInAsP; any other suitable material; and/or combinations thereof. In one embodiment, the alloy semiconductor substrate may have a gradient SiGe feature in which the Si and Ge composition change from one ratio at one location to another ratio at another location of the gradient SiGe feature. In another embodiment, the alloy SiGe is formed over a silicon substrate. In another embodiment, a SiGe substrate is strained. Furthermore, the semiconductor substrate may be a semiconductor on insulator, such as a silicon on insulator (SOI), or a thin film transistor (TFT). In some examples, the semiconductor substrate may include a doped epi layer or a buried layer. In other examples, the compound semiconductor substrate may have a multilayer structure, or the silicon substrate may include a multilayer compound semiconductor structure. In the present embodiment, the semiconductor substrate 210 comprises silicon, germanium, a group III-V material, or a group II-VI material. This limitation is obvious in view of Yu and Adesida; obvious in view of Yu, Usui, and Adesida; obvious in view of Yu and Sugimoto; and obvious in view of Yu, Usui, and Sugimoto. Usui discloses the following, at 1:5-14: The present invention is concerned with a method for fabricating a metallization structure and is especially concerned with producing a structure having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics. Moreover, the process of the present invention provides highly textured aluminum <111> layers. The structures fabricated

Claim 11	Exemplary Disclosure based on Yu and Related Combinations
	by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure. Adesida discloses the following, at [0016]: Another form of the invention is directed to a field-effect device, comprising: a layered semiconductor structure that includes a channel layer and at least one layer over the channel layer; spaced apart source and drain contacts disposed over said at least one layer and communicating with the channel layer; and an iridium gate, between the source and drain contacts, forming a Schottky barrier contact on said at least one layer. In an embodiment of this form of the invention, said at least one layer includes a layer of InAlAs, and the iridium gate is deposited on the InAlAs layer to form a Schottky barrier contact on the InAlAs layer. The gate can comprise at least one further metal layer disposed on the iridium gate. As one example, the iridium gate can further include titanium, platinum, and gold over the iridium, thereby comprising an Ir/Ti/Pt/Au gate. Adesida discloses the following, at [0031]: FIG. 5 shows, in cross-section, an example of a type of device that can be utilized in practicing a form of the invention. The device of FIG. 5 is a high electron mobility transistor (HEMT), which, in this example, is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT) on which is deposited an insulating $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer layer. In this diagram, there is shown an undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel layer 120, and, over this layer, a spacer layer 130 of undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$, a thin Si-atomic planar doping region, and an undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150, and, except in the notched central region, a heavily doped n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer 160. Spaced apart source 170 and drain 180 ohmic contacts are formed on the n+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer 160, and the gate 190, which is shown as a T-gate in this example, is formed with a Schontky barrier contact of length L_g on the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150.

Claim 11	Exemplary Disclosure based on Yu and Related Combinations
	Adeseida discloses the following, at Fig. 5 (annotated): The diagram shows a cross-section of a semiconductor device. At the top, there are three electrodes: Source (170), Gate (190), and Drain (180). The Gate electrode is a Schottky contact (190) on an $n^+ \text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer (160). Below this is an $i\text{-In}_{0.52}\text{Al}_{0.48}\text{As}$ Barrier layer (150). Under the barrier is an $i\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ Channel layer (130), followed by an $i\text{-In}_{0.52}\text{Al}_{0.48}\text{As}$ Buffer layer (120). The device is built on a substrate (105) which is $i\text{-InP}$ or $i\text{-GaAs}$ with Si-atomic planarDoping. A Cap layer (140) and an $i\text{-In}_{0.52}\text{Al}_{0.48}\text{As}$ Spacer layer (110) are also shown. A blue box labeled 'Group III-V semiconductor device (150)' points to the barrier layer. A purple box labeled 'Gate electrode making Schottky contact (190)' points to the gate electrode. Figure 5 Sugimoto discloses the following, at 9:39-51: A gate electrode 44 (an example of an electrode) formed from a stacked structure of nickel (Ni) and gold (Au) is located at a center, relative to the page, of a top surface of the AlGa_N layer 34. The gate electrode 44 directly contacts with the top surface of the AlGa_N layer 34, and forms a Schottky contact with the AlGa_N layer 34. A drain electrode 42 and a source electrode 46, both formed from a stacked structure of titanium (Ti) and aluminum (Al), are disposed at left and right sides relative to the page, with the gate electrode 44 being located between the two. The drain electrode 42 and the source electrode 46 make ohmic contact with the top surface of the AlGa_N layer 34. The SI-GaN layer 62 is essentially formed from an intrinsic type semiconductor layer. Sugimoto discloses the following, at Fig. 1 (annotated):

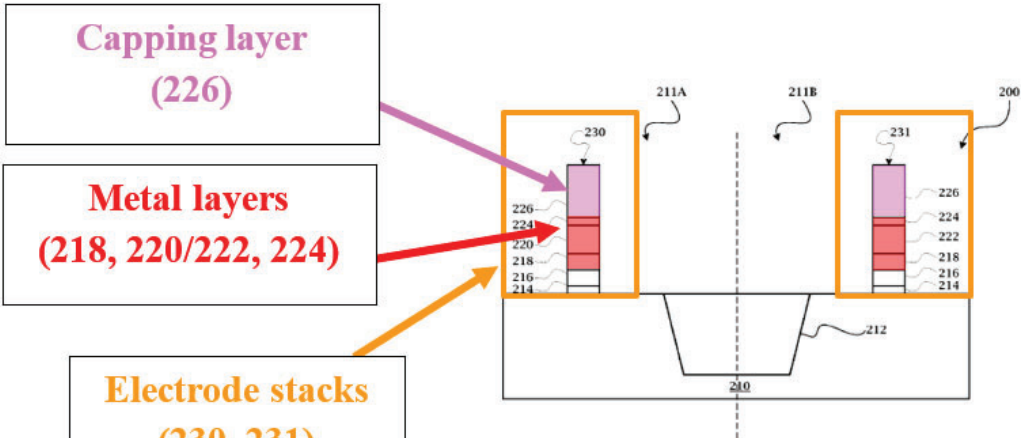
Claim 11	Exemplary Disclosure based on Yu and Related Combinations
	 See also Quay, 144; Krämer, 1, 2, 87; Mishra 2007, 219.

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
[13p] An electrical contact for use on a group III-V semiconductor device, said electrical contact comprising:	Yu, alone or in combination with one or more references, discloses and/or renders obvious an electrical contact for use on a group III-V semiconductor device, said electrical contact comprising. For example, Yu discloses the following, at [0040]: It is understood that the semiconductor device 200 may undergo further CMOS or MOS technology processing to form various features known in the art. For example, gate sidewall spacers may be formed on both sides of the metal gate stacks 230, 231 by a deposition and etching process. In some embodiments, lightly doped regions (referred to as LDD regions) may be formed in the substrate 210 using any suitable process, such as ion implantation, and any suitable dopants. In

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
	another example, source and drain regions (referred to as S/D regions) may be formed in the substrate 210 using ion implantation or diffusion with suitable dopants (depending on the configuration of the device such as NMOS and PMOS) and located proximate to each end of the metal gate stacks 230, 231 (the high-k gate dielectric and metal gate electrode), respectively. In still another example, various contacts/vias and multilayer interconnect features (e.g., metal layers and interlayer dielectrics) may be formed on the substrate 210 and configured to connect the various features or structures of the semiconductor device 200. Yu discloses the following, at Fig. 2E (annotated): Yu discloses the following, at [0023]: The semiconductor substrate 210 may comprise an elementary semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and GaInAsP; any other suitable material; and/or

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
	combinations thereof. In one embodiment, the alloy semiconductor substrate may have a gradient SiGe feature in which the Si and Ge composition change from one ratio at one location to another ratio at another location of the gradient SiGe feature. In another embodiment, the alloy SiGe is formed over a silicon substrate. In another embodiment, a SiGe substrate is strained. Furthermore, the semiconductor substrate may be a semiconductor on insulator, such as a silicon on insulator (SOI), or a thin film transistor (TFT). In some examples, the semiconductor substrate may include a doped epi layer or a buried layer. In other examples, the compound semiconductor substrate may have a multilayer structure, or the silicon substrate may include a multilayer compound semiconductor structure. In the present embodiment, the semiconductor substrate 210 comprises silicon, germanium, a group III-V material, or a group II-VI material. Yu discloses the following, at Fig. 2E (annotated): FIG. 2E
[13a] an electrode stack including a plurality of metal layers and a	Yu, alone or in combination with one or more references, discloses and/or renders obvious an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers.

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
capping layer formed over said plurality of metal layers;	For example, Yu discloses the following, at [0029]: In some embodiments, a diffusion barrier/protection layer 218 is formed over the high-k dielectric layer 216. The diffusion barrier/protection layer 218 may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present embodiment, the diffusion barrier/protection layer 218 comprises TiN, which is deposited by PVD to a thickness of approximately 20 Å. In alternate embodiments, the diffusion barrier/protection layer may be formed by any suitable process, such as CVD, PVD, ALD, thermal oxide, plating, and/or combinations thereof. Further, in alternate embodiments, the diffusion barrier layer 218 comprises any suitable thickness. It is understood that the diffusion barrier layer 218 may be omitted in alternate embodiments. Yu discloses the following, at [0035]: A diffusion barrier layer 224 may be formed over the semiconductor device 200, particularly, metal layers 220, 222 as illustrated in FIG. 2D. The diffusion barrier layer may comprise titanium, titanium nitride, tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present embodiment, the diffusion barrier layer 224 comprises TiN, which is deposited by PVD to a thickness of approximately 50 Å. In alternate embodiments, the diffusion barrier layer may be formed by any suitable process, such as CVD, PVD, ALD, thermal oxide, plating, and/or combinations thereof. Further, in alternate embodiments, the diffusion barrier layer 224 comprises any suitable thickness. It is understood that the diffusion barrier layer 224 may be omitted for alternate embodiments. Yu discloses the following, at [0036]: At step 110, referring to FIGS. 1 and 2D, a capping layer 226 is formed over the metal layers 220, 222, and in the present embodiment, over the diffusion barrier layer 224. The capping layer 226 may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
	the present embodiment, the capping layer 226 comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer 226 may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer 226 may comprise any suitable thickness. The capping layer 226 may be formed by CVD, PVD, ALD, thermal oxide, plating, other suitable processes, and/or combinations thereof. In some embodiments, the capping layer 226 comprises aluminum and/or tungsten. For example, in some embodiments, the capping layer 226 comprises aluminum formed by CVD. It is understood that, in alternate embodiments, the capping layer 226 may comprise multilayer structures. Yu discloses the following, at Fig. 2E (annotated):  The diagram illustrates a cross-sectional view of a semiconductor device. A substrate (200) is shown at the bottom. Two electrode stacks, 230 and 231, are formed on the substrate. Each electrode stack consists of a series of layers: 214, 216, 218, 220, 222, 224, and 226. A capping layer (226) is shown on top of the electrode stacks. A dashed line 212 indicates a vertical plane. Arrows point from labels 'Capping layer (226)', 'Metal layers (218, 220/222, 224)', and 'Electrode stacks (230, 231)' to the corresponding parts of the diagram. FIG. 2E

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
[13b] said capping layer consisting only of a metal selected from the group consisting of titanium nitride (TiN) and tantalum nitride (TaN),	Yu, alone or in combination with one or more references, discloses and/or renders obvious wherein said capping layer consisting only of a metal selected from the group consisting of titanium nitride (TiN) and tantalum nitride (TaN). For example, Yu discloses the following, at [0036]: At step 110, referring to FIGS. 1 and 2D, a capping layer 226 is formed over the metal layers 220, 222, and in the present embodiment, over the diffusion barrier layer 224. The capping layer 226 may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer 226 comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer 226 may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer 226 may comprise any suitable thickness. The capping layer 226 may be formed by CVD, PVD, ALD, thermal oxide, plating, other suitable processes, and/or combinations thereof. In some embodiments, the capping layer 226 comprises aluminum and/or tungsten. For example, in some embodiments, the capping layer 226 comprises aluminum formed by CVD. It is understood that, in alternate embodiments, the capping layer 226 may comprise multilayer structures. Yu discloses the following, at Fig. 2:

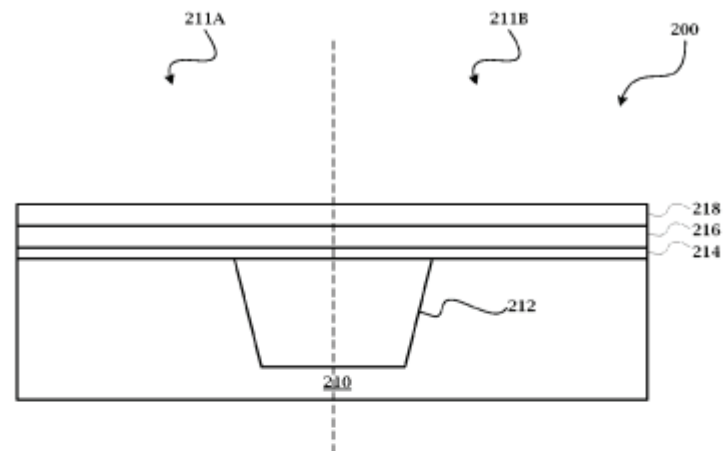


FIG. 2A

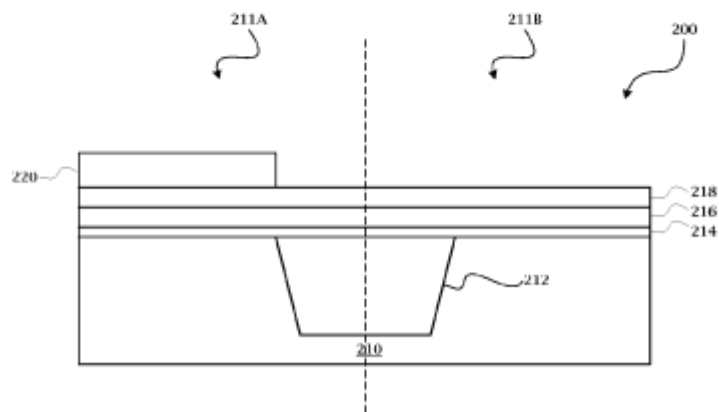


FIG. 2B

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
	This limitation is obvious in view of Yu and Usui. Usui discloses the following, at 5:49-65: Onto the aluminum-copper interconnect metallization 15 is then deposited about 50 to about 250 angstroms of a group IVA metal, preferably titanium, as layer 18 similar to the previously deposited metal layer 13 discussed above. Deposition and composition of layer 18 can be carried out in the same way as for layer 13. From FIG. 5, onto the metal layer 18 is then blanket deposited the suitable capping layer 19 to complete the interconnect metallurgy at this level. The capping layer is preferably titanium nitride and can be deposited in the same manner as the titanium nitride layer 14. The purpose of this layer is to limit the amount of light reflection during the subsequent photoresist steps and to act as a protective layer against corrosion during subsequent processing. Therefore, any layer which would similarly satisfy the requirements of reducing the amount of light reflection and provide protective anodic capping during subsequent processing would be usable for this layer. Usui discloses the following, at 1:5-14: The present invention is concerned with a method for fabricating a metallization structure and is especially concerned with producing a structure having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics. Moreover, the process of the present invention provides highly textured aluminum <111> layers. The structures fabricated by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure. Usui discloses the following, at 2:33-39: However, there still remains room for improvement of the electromigration characteristics. Accordingly, an objective of the present invention is to provide a structure that exhibits enhanced electromigration performance along with being hillock free and without a

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
	concomitant loss in the dry etchability characteristic and corrosion resistant characteristic of the structure. Usui discloses the following, at 3:22-37: FIG. 1 is a cross-sectional view of the preferred embodiment of an interconnect metallurgy structure according to the present invention. Referring to FIG. 1, the interconnect metallurgy preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 to make connection to a device substrate 6. The metallurgy structure includes an underlayer of a group IVA metal and preferably a layer of titanium. Critical to the success of the present invention is having the thickness of this underlayer 13 being between about 90 angstroms to about 110 angstroms. As will be demonstrated hereinbelow, by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention. <i>See also</i> Bauccio, 120; Cockeram, 1; Preuss, 2; Pierson, 156-157, 160; Kim, 46, 56; Suh, 3:39-43; Chen, Abstract, 1:58-61; Fair, Abstract, 1:29-34, 2:47-51.
[13c] said metal forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.	Yu, alone or in combination with one or more references, discloses and/or renders obvious said metal forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers. For example, Yu discloses the following, at [0029]: In some embodiments, a diffusion barrier/protection layer 218 is formed over the high-k dielectric layer 216. The diffusion barrier/protection layer 218 may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present embodiment, the diffusion barrier/protection layer 218 comprises TiN, which is deposited by PVD to a thickness of approximately 20 Å. In alternate embodiments, the diffusion barrier/protection layer

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
	may be formed by any suitable process, such as CVD, PVD, ALD, thermal oxide, plating, and/or combinations thereof. Further, in alternate embodiments, the diffusion barrier layer 218 comprises any suitable thickness. It is understood that the diffusion barrier layer 218 may be omitted in alternate embodiments. Yu discloses the following, at [0036]: At step 110, referring to FIGS. 1 and 2D, a capping layer 226 is formed over the metal layers 220, 222, and in the present embodiment, over the diffusion barrier layer 224. The capping layer 226 may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer 226 comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer 226 may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer 226 may comprise any suitable thickness. The capping layer 226 may be formed by CVD, PVD, ALD, thermal oxide, plating, other suitable processes, and/or combinations thereof. In some embodiments, the capping layer 226 comprises aluminum and/or tungsten. For example, in some embodiments, the capping layer 226 comprises aluminum formed by CVD. It is understood that, in alternate embodiments, the capping layer 226 may comprise multilayer structures. Yu discloses the following, at [0039]: In one example, for patterning the metal gate stacks 230, 231, a layer of photoresist is formed over the capping layer 226 by a suitable process, such as spin-on coating, and then patterned to form a patterned photoresist feature by a proper lithography patterning method. The pattern of the photoresist can then be transferred by a dry etching process to the underlying layers (i.e., the interfacial dielectric layer 214, the high-k dielectric layer 216, the diffusion barrier/protection layer 218, the first metal layer 220, the second metal layer 222, the diffusion barrier layer 224, and the capping layer 226) to form the metal gate stacks 230, 231 as shown in FIG. 2E. The photoresist layer may be stripped

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
	thereafter. In another example, a hard mask layer is formed over the capping layer 226; a patterned photoresist layer is formed on the hard mask layer; the pattern of the photoresist layer is transferred to the hard mask layer and then transferred to the electrode layers to form the electrode layers and dielectric layers of the gate structures. It is understood that the above examples do not limit the processing steps that may be utilized to form the metal gate stacks 230, 231. Yu discloses the following, at [0040]: It is understood that the semiconductor device 200 may undergo further CMOS or MOS technology processing to form various features known in the art. For example, gate sidewall spacers may be formed on both sides of the metal gate stacks 230, 231 by a deposition and etching process. In some embodiments, lightly doped regions (referred to as LDD regions) may be formed in the substrate 210 using any suitable process, such as ion implantation, and any suitable dopants. In another example, source and drain regions (referred to as S/D regions) may be formed in the substrate 210 using ion implantation or diffusion with suitable dopants (depending on the configuration of the device such as NMOS and PMOS) and located proximate to each end of the metal gate stacks 230, 231 (the high-k gate dielectric and metal gate electrode), respectively. In still another example, various contacts/vias and multilayer interconnect features (e.g., metal layers and interlayer dielectrics) may be formed on the substrate 210 and configured to connect the various features or structures of the semiconductor device 200. Yu discloses the following, at Fig. 2E (annotated):

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
	The diagram shows a cross-section of a substrate 200 with a trench 212. Two electrical contact stacks, 230 and 231, are formed in the trench. Each stack consists of a bottommost layer 218, a middle layer 216, and a capping layer 226. The diagram is labeled FIG. 2E. This limitation is obvious in view of Yu and Usui. Usui discloses the following, at 5:49-65: Onto the aluminum-copper interconnect metallization 15 is then deposited about 50 to about 250 angstroms of a group IVA metal, preferably titanium, as layer 18 similar to the previously deposited metal layer 13 discussed above. Deposition and composition of layer 18 can be carried out in the same way as for layer 13. From FIG. 5, onto the metal layer 18 is then blanket deposited the suitable capping layer 19 to complete the interconnect metallurgy at this level. The capping layer is preferably titanium nitride and can be deposited in the same manner as the titanium nitride layer 14. The purpose of this layer is to limit the amount of light reflection during the subsequent photoresist steps and to act as a protective layer against corrosion during subsequent processing. Therefore, any layer which would similarly satisfy the requirements of reducing the amount of light reflection and provide protective anodic capping during subsequent processing would be usable for this layer. Usui discloses the following, at Abstract:

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
	A metallization structure is fabricated by depositing an underlayer of a group IVA metal having a thickness of about 90 to about 110 angstroms, and depositing a layer of aluminum and/or an aluminum alloy. The metallization structure obtained exhibits enhanced electromigration and is highly textured and is especially suitable for forming electrical connections or wiring. Usui discloses the following, at 1:5-14: The present invention is concerned with a method for fabricating a metallization structure and is especially concerned with producing a structure having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics. Moreover, the process of the present invention provides highly textured aluminum <111> layers. The structures fabricated by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure. Usui discloses the following, at 2:33-39: However, there still remains room for improvement of the electromigration characteristics. Accordingly, an objective of the present invention is to provide a structure that exhibits enhanced electromigration performance along with being hillock free and without a concomitant loss in the dry etchability characteristic and corrosion resistant characteristic of the structure. Usui discloses the following, at 3:22-37: FIG. 1 is a cross-sectional view of the preferred embodiment of an interconnect metallurgy structure according to the present invention. Referring to FIG. 1, the interconnect metallurgy preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 to make connection to a device substrate 6. The metallurgy structure includes an underlayer of a group IVA metal and preferably a layer of titanium. Critical to the success of the present invention is having the thickness of this underlayer 13 being between about 90 angstroms to about 110 angstroms. As will be demonstrated hereinbelow, by limiting the thickness of this underlayer 13, the structure and texture

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
	of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention. Usui discloses the following, at 3:56-4:9: Also, although not required, according to preferred aspects of the present invention a capping layer is provided above layer 15. The capping layer when present, enhances the lithographic processing since it acts as an anti-reflective layer aiding in controlling line width. Preferred capping layers are titanium nitride and combinations of as layer 18 of a group IVA metal, preferably titanium with a titanium nitride layer 19. Typically the titanium nitride layer is about 150 to about 800 angstroms and more typically about 200 to about 500 angstroms. Typically, the titanium layer is about 50 angstroms to about 200 angstroms. Usui discloses the following, at 5:34-39: Referring now to FIG. 3, following the deposition of the layer 13, a titanium nitride layer 14 is formed by sputter deposition of titanium nitride to the desired thickness. Titanium nitride layer 14 may be formed in the same chamber used for deposition of the titanium layer 13 or in a different apparatus. Usui discloses the following, at 3:2-8: FIG. 1 is a cross-sectional view of a preferred embodiment of an interconnect metallurgy according to the present invention. FIGS. 2-8 are a cross-sectional view of the process for fabricating the preferred interconnect metallurgy of the present invention in a step-by-step fashion. Usui discloses the following, at Fig. 1:

Claim 13	Exemplary Disclosure based on Yu and Related Combinations
	FIG. 1 Usui discloses the following, at Fig. 8 (annotated): FIG. 8 <i>See also Chin, Abstract, Figs. 1a and 1b, [0020]-[0023]; Suh, 3:33-37; Chen, 3:9-15.</i>

Claim 14	Exemplary Disclosure based on Yu and Related Combinations
[14p] The electrical contact of claim 13,	Yu, alone or in combination with one or more references, discloses and/or renders obvious the electrical contact of claim 13. <i>See supra</i> claim 13.
[14a] wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).	Yu, alone or in combination with one or more references, discloses and/or renders obvious wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT). For example, Yu discloses the following, at [0023]: The semiconductor substrate 210 may comprise an elementary semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and GaInAsP; any other suitable material; and/or combinations thereof. In one embodiment, the alloy semiconductor substrate may have a gradient SiGe feature in which the Si and Ge composition change from one ratio at one location to another ratio at another location of the gradient SiGe feature. In another embodiment, the alloy SiGe is formed over a silicon substrate. In another embodiment, a SiGe substrate is strained. Furthermore, the semiconductor substrate may be a semiconductor on insulator, such as a silicon on insulator (SOI), or a thin film transistor (TFT). In some examples, the semiconductor substrate may include a doped epi layer or a buried layer. In other examples, the compound semiconductor substrate may have a multilayer structure, or the silicon substrate may include a multilayer compound semiconductor structure. In the present embodiment, the semiconductor substrate 210 comprises silicon, germanium, a group III-V material, or a group II-VI material. This limitation is obvious in view of Yu and Adesida; obvious in view of Yu, Usui, and Adesida; obvious in view of Yu and Sugimoto; and obvious in view of Yu, Usui, and Sugimoto. Usui discloses the following, at 1:5-14:

Claim 14	Exemplary Disclosure based on Yu and Related Combinations
	The present invention is concerned with a method for fabricating a metallization structure and is especially concerned with producing a structure having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics. Moreover, the process of the present invention provides highly textured aluminum <111> layers. The structures fabricated by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure. Adesida discloses the following, at [0031]: FIG. 5 shows, in cross-section, an example of a type of device that can be utilized in practicing a form of the invention. The device of FIG. 5 is a high electron mobility transistor (HEMT), which, in this example, is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT) on which is deposited an insulating $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer layer. In this diagram, there is shown an undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel layer 120, and, over this layer, a spacer layer 130 of undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$, a thin Si-atomic planar doping region, and an undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150, and, except in the notched central region, a heavily doped n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer 160. Spaced apart source 170 and drain 180 ohmic contacts are formed on the n⁺ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer 160, and the gate 190, which is shown as a T-gate in this example, is formed with a Schottky barrier contact of length L_g on the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150. Sugimoto discloses the following, at title: III-V HEMT DEVICES. Sugimoto discloses the following, at 1:55-58: The on-resistance here means a magnitude of resistance between the drain electrode and the source electrode while the predetermined gate voltage is applied to the gate electrode of HEMT.

Claim 14	Exemplary Disclosure based on Yu and Related Combinations
	<i>See also</i> Sheppard, [0004], [0044]; Mishra 2007, 375, 376, 393, 402-403; Mishra 2002, 1023-1024; Wu 2001, 586; Quay, 71; Pearton, 214.

Claim 15	Exemplary Disclosure based on Yu and Related Combinations
[15p] The electrical contact of claim 13,	Yu, alone or in combination with one or more references, discloses and/or renders obvious the electrical contact of claim 13. <i>See supra</i> claim 13.
[15a] wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.	Yu, alone or in combination with one or more references, discloses and/or renders obvious wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device. For example, Yu discloses the following, at [0023]: The semiconductor substrate 210 may comprise an elementary semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and GaInAsP; any other suitable material; and/or combinations thereof. In one embodiment, the alloy semiconductor substrate may have a gradient SiGe feature in which the Si and Ge composition change from one ratio at one location to another ratio at another location of the gradient SiGe feature. In another embodiment, the alloy SiGe is formed over a silicon substrate. In another embodiment, a SiGe substrate is strained. Furthermore, the semiconductor substrate may be a semiconductor on insulator, such as a silicon on insulator (SOI), or a thin film transistor (TFT). In some examples, the semiconductor substrate may include a doped epi layer or a buried layer. In other examples, the compound semiconductor substrate may have a multilayer structure, or the silicon substrate may include a multilayer compound semiconductor structure. In the present

Claim 15	Exemplary Disclosure based on Yu and Related Combinations
	embodiment, the semiconductor substrate 210 comprises silicon, germanium, a group III-V material, or a group II-VI material. This limitation is obvious in view of Yu and Adesida; obvious in view of Yu, Usui, and Adesida; obvious in view of Yu and Sugimoto; and obvious in view of Yu, Usui, and Sugimoto. Usui discloses the following, at 1:5-14: The present invention is concerned with a method for fabricating a metallization structure and is especially concerned with producing a structure having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics. Moreover, the process of the present invention provides highly textured aluminum <111> layers. The structures fabricated by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure. Sugimoto discloses the following, at 9:39-51: A gate electrode 44 (an example of an electrode) formed from a stacked structure of nickel (Ni) and gold (Au) is located at a center, relative to the page, of a top surface of the AlGaIn layer 34. The gate electrode 44 directly contacts with the top surface of the AlGaIn layer 34, and forms a Schottky contact with the AlGaIn layer 34. A drain electrode 42 and a source electrode 46, both formed from a stacked structure of titanium (Ti) and aluminum (Al), are disposed at left and right sides relative to the page, with the gate electrode 44 being located between the two. The drain electrode 42 and the source electrode 46 make ohmic contact with the top surface of the AlGaIn layer 34. The SI-GaN layer 62 is essentially formed from an intrinsic type semiconductor layer. Sugimoto discloses the following, at Fig. 1 (annotated):

Claim 15	Exemplary Disclosure based on Yu and Related Combinations
	The diagram shows a cross-section of a semiconductor device. The substrate is labeled 22 (Al₂O₃). Above it are layers 24 (GaN), 32 (p-GaN), 62 (Si-GaN), and 34 (AlGaN). A gate structure is formed on the surface, with a power electrode making ohmic contact (46, 44) and a source/drain contact (42). A cross-section line II-II is indicated. Adesida discloses the following, at [0031]: FIG. 5 shows, in cross-section, an example of a type of device that can be utilized in practicing a form of the invention. The device of FIG. 5 is a high electron mobility transistor (HEMT), which, in this example, is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT) on which is deposited an insulating In_{0.52}Al_{0.48}As buffer layer. In this diagram, there is shown an undoped In_{0.53}Ga_{0.47}As channel layer 120, and, over this layer, a spacer layer 130 of undoped In_{0.52}Al_{0.48}As, a thin Si-atomic planar doping region, and an undoped In_{0.52}Al_{0.48}As barrier layer 150, and, except in the notched central region, a heavily doped n-type In_{0.53}Ga_{0.47}As cap layer 160. Spaced apart source 170 and drain 180 ohmic contacts are formed on the n⁺ In_{0.53}Ga_{0.47}As cap layer 160, and the gate 190, which is shown as a T-gate in this example, is formed with a Schottky barrier contact of length L_g on the In_{0.52}Al_{0.48}As barrier layer 150. Adeseida discloses the following, at Fig. 5 (annotated):

Claim 15	Exemplary Disclosure based on Yu and Related Combinations
	Power electrode making ohmic contact (170, 180) Group III-V semiconductor device (105, 110, 120, 130, 150, 160) <i>Figure 5</i> See also Quay, 71, 144, 145; Voss, 22; Krämer, 1, 32; Neaman, 344; Pearton, 214; Sheppard, [0004], [0044]; Mishra 2007, 229, 375, 376, 393, 402-403; Wu 2001, 586; Mishra 2002 at 1023-1024.

Claim 16	Exemplary Disclosure based on Yu and Related Combinations
[16p] The electrical contact of claim 13,	Yu, alone or in combination with one or more references, discloses and/or renders obvious the electrical contact of claim 13. <i>See supra</i> claim 13.
[16a] wherein said electrical contact is implemented as a gate electrode making Schottky	Yu, alone or in combination with one or more reference,s discloses and/or renders obvious wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

Claim 16	Exemplary Disclosure based on Yu and Related Combinations
contact with said group III-V semiconductor device.	For example, Yu discloses the following, at [0023]: The semiconductor substrate 210 may comprise an elementary semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and GaInAsP; any other suitable material; and/or combinations thereof. In one embodiment, the alloy semiconductor substrate may have a gradient SiGe feature in which the Si and Ge composition change from one ratio at one location to another ratio at another location of the gradient SiGe feature. In another embodiment, the alloy SiGe is formed over a silicon substrate. In another embodiment, a SiGe substrate is strained. Furthermore, the semiconductor substrate may be a semiconductor on insulator, such as a silicon on insulator (SOI), or a thin film transistor (TFT). In some examples, the semiconductor substrate may include a doped epi layer or a buried layer. In other examples, the compound semiconductor substrate may have a multilayer structure, or the silicon substrate may include a multilayer compound semiconductor structure. In the present embodiment, the semiconductor substrate 210 comprises silicon, germanium, a group III-V material, or a group II-VI material. This limitation is obvious in view of Yu and Adesida; obvious in view of Yu, Usui, and Adesida; obvious in view of Yu and Sugimoto; and obvious in view of Yu, Usui, and Sugimoto. Usui discloses the following, at 1:5-14: The present invention is concerned with a method for fabricating a metallization structure and is especially concerned with producing a structure having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics. Moreover, the process of the present invention provides highly textured aluminum <111> layers. The structures fabricated

Claim 16	Exemplary Disclosure based on Yu and Related Combinations
	by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure. Adesida discloses the following, at [0016]: Another form of the invention is directed to a field-effect device, comprising: a layered semiconductor structure that includes a channel layer and at least one layer over the channel layer; spaced apart source and drain contacts disposed over said at least one layer and communicating with the channel layer; and an iridium gate, between the source and drain contacts, forming a Schottky barrier contact on said at least one layer. In an embodiment of this form of the invention, said at least one layer includes a layer of InAlAs, and the iridium gate is deposited on the InAlAs layer to form a Schottky barrier contact on the InAlAs layer. The gate can comprise at least one further metal layer disposed on the iridium gate. As one example, the iridium gate can further include titanium, platinum, and gold over the iridium, thereby comprising an Ir/Ti/Pt/Au gate. Adesida discloses the following, at [0031]: FIG. 5 shows, in cross-section, an example of a type of device that can be utilized in practicing a form of the invention. The device of FIG. 5 is a high electron mobility transistor (HEMT), which, in this example, is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate 105 (therefore commonly called an InP HEMT or GaAs metamorphic HEMT) on which is deposited an insulating $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer layer. In this diagram, there is shown an undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel layer 120, and, over this layer, a spacer layer 130 of undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$, a thin Si-atomic planar doping region, and an undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150, and, except in the notched central region, a heavily doped n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer 160. Spaced apart source 170 and drain 180 ohmic contacts are formed on the n+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer 160, and the gate 190, which is shown as a T-gate in this example, is formed with a Schontky barrier contact of length L_g on the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layer 150.

Claim 16	Exemplary Disclosure based on Yu and Related Combinations
	Adeseida discloses the following, at Fig. 5 (annotated): Figure 5 Sugimoto discloses the following, at 9:39-51: A gate electrode 44 (an example of an electrode) formed from a stacked structure of nickel (Ni) and gold (Au) is located at a center, relative to the page, of a top surface of the AlGaN layer 34. The gate electrode 44 directly contacts with the top surface of the AlGaN layer 34, and forms a Schottky contact with the AlGaN layer 34. A drain electrode 42 and a source electrode 46, both formed from a stacked structure of titanium (Ti) and aluminum (Al), are disposed at left and right sides relative to the page, with the gate electrode 44 being located between the two. The drain electrode 42 and the source electrode 46 make ohmic contact with the top surface of the AlGaN layer 34. The SI-GaN layer 62 is essentially formed from an intrinsic type semiconductor layer. Sugimoto discloses the following, at Fig. 1 (annotated):

Claim 16	Exemplary Disclosure based on Yu and Related Combinations
	Gate electrode making Schottky contact (44) Group III-V semiconductor device (34) 10 46 44 42 34 (AlGaN) 62 (SI-GaN) 32 (p-GaN) 24 (GaN) 22 (Al₂O₃) II II See also Quay, 144; Krämer, 1, 2, 87; Mishra 2007, 219.