

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AMERICAS CORP.,
Patent Owner.

Case No. IPR2025-00175
Patent No. 8,686,562

DECLARATION OF EDWIN PINER, Ph.D.

Infineon Exhibit 2024 Innoscence v. Infineon IPR2025-00175
--

TABLE OF CONTENTS

I.	PERSONAL AND PROFESSIONAL BACKGROUND	1
II.	MATERIALS REVIEWED AND CONSIDERED	4
III.	MY UNDERSTANDING OF PATENT LAW	5
	A. Anticipation	6
	B. Obviousness.....	7
IV.	PERSON OF ORDINARY SKILL IN THE ART (“POSA”).....	9
V.	OVERVIEW OF THE ’562 PATENT	12
VI.	RESPONSE TO DR. ZHAO’S TECHNOLOGY OVERVIEW	21
	A. Dr. Zhao Does Not Account for the Unpredictability Inherent in Ohmic Contact Design and Fabrication	22
	B. Dr. Zhao Never Addresses the Technical Constraints in Gate Contact Design	30
	C. Dr. Zhao Confuses Interconnects with Electrical Contacts.....	33
	1. Problems with Interconnects	35
	2. Electrical Contacts.....	38
	D. Dr. Zhao’s Mistakes Regarding Diffusion Barrier Layers.....	41
VII.	“ELECTRODE STACK” CLAIM CONSTRUCTION	45
	A. Intrinsic Evidence.....	50
	B. Extrinsic Evidence.....	57
VIII.	DISCUSSION OF THE PETITION’S REFERENCES	58
	A. Usui (U.S. Patent No. 5,943,601) (EX-1004)	58
	B. Yu (U.S. Patent App. Pub. No. 2010/0052066) (EX-1005).....	65
	C. Adesida (U.S. Patent App. Pub. No. 2008/0023726) (EX-1006)	72
	D. Sugimoto (U.S. Patent No. 7,777,252) (EX-1007)	76
IX.	RESPONSE TO THE PETITION’S GROUNDS	79
	A. Ground 1 – Usui Does Not Anticipate Claims 1, 2, and 4-7.....	80
	1. Neither Petitioner Nor Dr. Zhao Explains the Plain Meaning of “Electrode Stack”	83

2. No Evidence Supports the Assertion that Usui’s Interconnect Metallization Structure is an “Electrode Stack”.....	86
3. Usui’s Interconnect Metallization Structure is Not an Electrode Stack Under the Proper Construction.....	87
B. Grounds 2-4 Also Fail	95
1. Grounds 2-4 Fall with Ground 1	95
2. Ground 2 – The Petition and Dr. Zhao Fail to Establish Obviousness for Claims 12 And 17 for Additional Reasons	96
3. Ground 3 Fails for Additional Reasons.....	107
a. Claims 11 and 16.....	107
i. Petitioner Fails to Establish Any Reason to Have Modified Usui Based on Yu and Adesida in the Claimed Manner	108
ii. Petitioner Fails to Explain the Contemplated Workings of the Usui-Yu-Adesida Combination and How it Meets the Challenged Claims	115
iii. Petitioner Fails to Establish a Reasonable Expectation of Success	118
b. Claims 9 and 14.....	121
4. Ground 4 Fails for Additional Reasons.....	124
i. Dr. Zhao Fails to Explain the Contemplated Combination.....	125
ii. Petitioner Fails to Establish Any Reason to Modify Usui Based on Yu and Sugimoto in the Claimed Manner	129
iii. Dr. Zhao Fails to Establish a Reasonable Expectation of Success	135
C. Ground 5 (Obviousness over Yu and Usui) Fails	138
1. Petitioner Fails to Establish that Yu’s Diffusion Barrier/Protection Layer 218 is a Layer of Yu’s Electrode Stack	142
a. Petitioner’s Conclusion that Yu’s Diffusion Barrier Layer is Part of an Electrode Stack is Unsupported.....	143

b.	Neither Petitioner Nor Dr. Zhao Explain What the Term “Electrode Stack” Means	144
c.	No Evidence Supports the Assertion that Yu’s Entire Metal Gate Stack is an Electrode Stack as Claimed	145
d.	The Assertion that Yu’s Entire Metal Gate Stack is an “Electrode Stack” Contradicts the Intrinsic Evidence	146
e.	Ground 5 Fails Because Yu’s Diffusion Barrier/Protection Layer 218 is Not a Layer of Yu’s Electrode Stack	150
2.	Petitioner Also Fails to Show that Yu and Usui Render Obvious an Electrical Contact with a Capping Layer of a Refractory Metal Nitride that is Thicker Than Yu’s Alleged Bottommost Layer.....	150
a.	Yu Does Not Disclose a Refractory Metal Nitride Capping Layer Thicker Than Yu’s Alleged Bottommost Layer 218.....	152
b.	Petitioner’s Assertion that a POSA Would Have Used the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Capping Layer is Unsupported	153
i.	Petitioner Fails to Show There Was Any Reason to Choose the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Capping Layer	154
ii.	No Evidence Supports Petitioner’s Assertion that a POSA Would Have Chosen the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Capping Layer	155
iii.	Petitioner Does Not Identify the Thickness of Yu’s Diffusion Barrier/Protection Layer 218 When Made of Titanium as Alleged in the Yu-Usui Combination	157
c.	Petitioner’s Alternative Argument that Usui Would Have Motivated a POSA to Make Yu’s Refractory Metal Nitride Capping Layer Thicker Than Yu’s Diffusion Barrier/Protection Layer Fails.....	159
i.	A Capping Layer Thicker than the Bottommost Layer of the Electrode Stack’s Metal Layers is a Missing Limitation Not Taught by Yu or Usui	160

ii. Usui’s Interconnect Metallurgy Structure Would Not Have Motivated Any Change to Yu’s CMOS Gate Electrode	161
d. Petitioner’s “Known Techniques” Argument	164
D. Grounds 6-7 Also Fail	166
1. Ground 6-7 Fall with Ground 5	166
2. Ground 6 Fails for Claims 11 and 16 for Additional Reasons.....	166
3. Ground 7 Fails for Additional Reasons.....	169

I, Edwin Piner, declare:

1. I have been retained by Wolf, Greenfield & Sacks, P.C., counsel for Patent Owner Infineon Technologies Americas Corp., to provide my opinions concerning a Petition for *inter partes* review (IPR) filed by Petitioner Innoscience America, Inc. I am being compensated for my time at my standard rate of \$450 per hour. I am also being reimbursed for any expenses I incur on this matter. My compensation is not dependent in any way upon the outcome of the *inter partes* review of the '562 Patent, the opinions I express, or any other matter.

I. PERSONAL AND PROFESSIONAL BACKGROUND

2. My qualifications for forming the opinions in this Declaration are summarized below and are presented in more detail in my professional CV, which is attached as EX-2025.

3. I am a Professor of Physics at Texas State University. I also have appointments at Texas State University as Chair of the Department of Physics, Co-Director, Materials Application Research Center, and Director, NSF CREST Center for Ultrawide Bandgap Semiconductor Device Materials. I have experience in a number of areas that are related to the '562 Patent, and have particular expertise in research, development, and commercialization of semiconductor materials.

4. I received my bachelor's degree in Material Science and Engineering from North Carolina State University in 1993. Thereafter, I pursued a Ph.D. in Material Science and Engineering at North Carolina State University and received my Ph.D. in 1998.

5. From 1998 to 2000, I worked as a research engineer at ATMI Corporation/Epitronics, where I developed wide bandgap electronic materials for transistor devices.

6. From 2000 to 2009, I worked as director of advanced technology at Nitronex Corporation, where I conducted and directed research and development in III-nitride-on-silicon semiconductor materials, processing, and device design.

7. In 2010, I became an Associate Professor at Texas State University and attained tenure and promotion to Professor in 2013. I have continued to serve in that role through the present while also promoted to Chair, Department of Physics in 2023, Co-Director, Materials Application Research Center in 2024, and Director, NSF CREST Center for Ultrawide Bandgap Semiconductor Device Materials in 2025. In the role of Professor, I have taught courses such as Semiconductor Device Microfabrication, Semiconductor Device Physics, Electrical Characterization of Materials, Fundamentals of Materials Science & Engineering, and Advanced Concepts in Materials Science & Engineering. I have focused my research on technology development in the growth and

characterization of semiconductors, semiconductor fabrication, and performance optimization of wide and ultrawide bandgap materials for solid-state device applications.

8. My areas of research have included materials for light-emitting diodes, laser diodes and heterojunction field effect transistors. In particular, my research emphasis has been on semiconductor substrate nucleation processes, compositional inhomogeneities, and detailed interface science research. Thus, through my education, experience, and training, in academia and industry, I have expertise in the field of technology at issue.

9. I am a Fellow of the National Academy of Inventors, Senior Member of the Institutes of Electrical and Electronic Engineers, a member of the Materials Research Society, and international advisory committees for two annual conferences and workshops. I am the author or co-author of over one hundred published book chapters and papers, and over 30 U.S. patents relating to wide bandgap semiconductor materials and devices. I have received a number of honors and awards for my work and been invited to speak on several occasions regarding my research. A list of all publications that I have authored throughout my career is included in my professional CV attached as EX-2025.

II. MATERIALS REVIEWED AND CONSIDERED

10. My findings, as explained below, are based on my years of education, research, experience, and background in the field of semiconductor device fabrication, as well as my investigation and study of relevant materials for this declaration. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth in Section IV below. In addition to the Petition (Paper 1) and the Exhibits cited therein (EX-1001 through EX-1036), in forming my opinions, I have studied and considered the materials identified in the list below.

Exhibit	Description
2001	Excerpts from Merriam Webster's Collegiate Dictionary (10th ed.) (2001)
2002	U.S. Patent Application Publication No. 2008/0251828 A1 ("Meng")
2003	U.S. Patent Application Publication No. 2011/0247549 A1 ("Sachs")
2004	Quirk, M., & Serda, J. (2001) Semiconductor Manufacturing Technology. Prentice Hall.
2026	Transcript of Deposition of Yuji Zhao, Ph.D. (Sept. 5, 2025) ("Zhao Dep.")
2027	Larry Zhao, "All About Interconnects" Semiconductor Engineering, https://semiengineering.com/all-about-interconnects/ (Dec. 18, 2017)
2028	U.S. Patent No. 6,249,056 ("Kwon")
2029	U.S. Patent No. 4,017,890 ("Howard")
2030	Excerpts from JAEGER, INTRODUCTION TO MICROELECTRONIC FABRICATION (2nd Ed. 2002) ("Jaeger")
2031	Excerpts from OHRING, THE MATERIALS SCIENCE OF THIN FILMS (1992) ("Ohring")
2032	U.S. Patent No. 7,537,951 ("Gambino")
2033	U.S. Patent App. Pub. No. 2007/0007653 A1 ("Chen-653")

III. MY UNDERSTANDING OF PATENT LAW

11. In developing my opinions, I discussed various relevant legal principles with Patent Owner's attorneys. Though I do not purport to have prior knowledge of such principles, I understood them when they were explained to me and have relied upon such legal principles, as explained to me, in the course of forming the opinions set forth in this declaration. My understanding in this respect is as follows:

12. I understand that "*inter partes* review" (IPR) is a proceeding before the United States Patent & Trademark Office for evaluating the patentability of an issued patent's claims based on prior-art patents and printed publications.

13. I understand that, in this proceeding, Petitioner has the burden of proving that the challenged claims of the '562 Patent are unpatentable by a preponderance of the evidence. I understand that "preponderance of the evidence" means that a fact or conclusion is more likely true than not true.

14. I understand that, in IPR proceedings, claim terms in a patent are given their ordinary and customary meaning as understood by a person of ordinary skill in the art ("POSA") in the context of the entire patent and the prosecution history pertaining to the patent. If the specification provides a special definition for a claim term that differs from the meaning the term would otherwise possess, the specification's special definition controls.

15. I understand that determining whether a particular patent or printed publication constitutes prior art to a challenged patent claim can require determining the effective filing date (also known as the priority date) to which the challenged claim is entitled. I understand that for a patent claim to be entitled to the benefit of the filing date of an earlier application to which the patent claims priority, the earlier application must have described the claimed invention in sufficient detail to convey with reasonable clarity to the POSA that the inventor had possession of the claimed invention as of the earlier application's filing date. I understand that a disclosure that merely renders the claimed invention obvious is not sufficient written description for the claim to be entitled to the benefit of the filing date of the application containing that disclosure.

16. I understand that for an invention claimed in a patent to be patentable, it must be, among other things, new (novel – *i.e.*, not anticipated) and not obvious from the prior art. My understanding of these two legal standards is set forth below.

A. Anticipation

17. I understand that, for a patent claim to be “anticipated” by the prior art (and therefore not novel), each and every limitation of the claim must be found, expressly or inherently, in a single prior-art reference. I understand that a claim limitation is disclosed for the purpose of anticipation if a POSA would have

understood the reference to disclose the limitation based on inferences that a POSA would reasonably be expected to draw from the explicit teachings in the reference when read in light of the POSA's knowledge and experience.

18. I understand that a claim limitation is inherent in a prior art reference if that limitation is necessarily present when practicing the teachings of the reference, regardless of whether a person of ordinary skill recognized the presence of that limitation in the prior art.

B. Obviousness

19. I understand that a patent claim may be unpatentable if it would have been obvious in view of a single prior-art reference or a combination of prior-art references.

20. I understand that a patent claim is obvious if the differences between the subject matter of the claim and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the relevant field at the time the invention was made. Specifically, I understand that the obviousness question involves a consideration of:

- the scope and content of the prior art;
- the differences between the prior art and the claims at issue;
- the knowledge of a person of ordinary skill in the pertinent art; and

- if present, objective factors indicative of non-obviousness, sometimes referred to as “secondary considerations.”

21. I understand that in order for a claimed invention to be considered obvious, a POSA must have had a reason for combining teachings from multiple prior-art references (or for altering a single prior-art reference, in the case of obviousness in view of a single reference) in the fashion proposed.

22. I further understand that in determining whether a prior-art reference would have been combined with other prior art or with other information within the knowledge of a POSA, the following are examples of approaches and rationales that may be considered:

- combining prior-art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of a known technique to improve similar devices in the same way;
- applying a known technique to a known device ready for improvement to yield predictable results;
- applying a technique or approach that would have been “obvious to try,” *i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success.

- known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;
- some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior-art reference or to combine prior-art reference teachings to arrive at the claimed invention. I understand that this teaching, suggestion or motivation may come from a prior-art reference or from the knowledge or common sense of one of ordinary skill in the art.

23. I understand that for a single reference or a combination of references to render the claimed invention obvious, a POSA must have been able to arrive at the claimed invention by altering or combining the applied references.

IV. PERSON OF ORDINARY SKILL IN THE ART (“POSA”)

24. I have been informed and understand that for purposes of assessing whether prior-art references disclose every element of a patent claim (thus “anticipating” the claim) and/or would have rendered the claim obvious, the patent and the prior-art references must be assessed from the perspective of a person having ordinary skill in the art (“POSA”) to which the patent is related, based on the understanding of that person at the time of the patent claim’s priority date. I

have been informed and understand that a POSA is presumed to be aware of all pertinent prior art and the conventional wisdom in the art and is a person of ordinary creativity. I have applied this standard throughout my declaration.

25. It is my understanding that when interpreting the claims of a patent, I must do so based on the perspective of one of ordinary skill in the art at the time of invention. I discuss claim construction for purposes of the '562 Patent in Section VII below. I understand that when assessing the level of ordinary skill for a given patent, relevant factors include (1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.

26. Taking these factors into account, along with my personal experience working in the field and my knowledge of colleagues and others working in that field, and the specialized nature of semiconductor device processing, I believe that a person of ordinary skill in the art of the '562 Patent would be an individual who would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor design or fabrication. A person with less education but more relevant practical experience may also meet this standard

27. I understand that Petitioner and its expert, Dr. Yuji Zhao, contend that a POSA at the time of the purported invention would have possessed:

at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design. Additional education could substitute for professional experience and vice versa.

EX-1002 (Declaration of Yuji Zhao, Ph.D., “Zhao Dec.”), ¶81.

28. While Dr. Zhao’s position differs slightly from my own, the difference is insignificant in the context of my opinions in this report. For the sake of simplicity, I have based my opinions on the level of skill as Dr. Zhao defines it, but my opinions would be the same if I applied my own definition. As explained above in Section I (Personal and Profession Background), I possessed at least the above skill level as of August 25, 2009, the filing date of the ’562 Patent.

29. Whenever I offer an opinion in this declaration about the knowledge of a POSA, the manner in which a POSA would have understood the claims of the ’562 Patent or its description, the manner in which a POSA would have understood the prior art, or what a POSA would have been led to do based on the prior art, I am referencing the 2009 timeframe, even if not specifically mentioned in each case.

30. By 2009, I held a doctorate-level education and was a director of advanced technology in the field of semiconductor device fabrication, and I had a

decade of experience with semiconductor device fabrication. Therefore, I was a person exceeding ordinary skill in the art during the relevant timeframe. I also worked with many people who fit the characteristics of the POSA, and I am familiar with the ordinary level of skill fitting with the POSA definitions above. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth above.

V. OVERVIEW OF THE '562 PATENT

31. The '562 Patent relates to the field of semiconductor device fabrication and, more specifically, to “a refractory metal nitride capped electrical contact and a method for its fabrication.” EX-1001, 1:20–23, 2:19–24. The electrical contact of the '562 Patent is implemented as an electrode (*e.g.*, a source or drain electrode) on a group III-V semiconductor, such as a GaN-based device, as part of a semiconductor transistor. EX-1001, Abstract, 1:6–11, 2:19–24. For example, the '562 Patent describes a group III-V semiconductor high electron mobility transistor (HEMT) implemented in gallium nitride (GaN). EX-1001, 2:53-55, claim 9, claim 14.

32. III-nitride power semiconductor device fabrication typically includes forming electrical contacts (*e.g.*, ohmic contacts functioning as a source electrode or drain electrode), having a low Specific Linear Contact Resistivity (SCLR). EX-1001, 1:33-36; *see also* EX-1017 (Kramer), at *i* (Page 3 of 151). Previous

approaches to implement electrical contacts with suitably SCLR utilized gold to form a capping layer of an electrode stack – for example, a stack comprising pure films of titanium, aluminum, and nickel, capped with gold. *Id.*, at 1:33–43. It was recognized that, *e.g.*, high quality, low resistance ohmic contacts to p-GaN semiconductor devices were difficult to achieve. EX-1016 (Voss), 23; EX-1017 (Kramer), 31 (Page 38 of 151) (“The fabrication of Ohmic contacts is still more an art than a science.”).

33. This was due to several factors, including “the relative dearth of appropriate metal systems due to the large work function of GaN, low hole densities due to the difficulty in achieving a high doping concentration during growth, the presence of compensating hydrogen interstitials, and the presence of compensating nitrogen vacancies.” EX-1016 (Voss), 23-24. But more fundamentally, “[i]f a metal is placed into contact with such a semiconductor, the physics of the junction are not governed by the bulk properties of the metal and semiconductor material but by the properties of the surface boundaries and primarily those of the semiconductor surface.” EX-1017 (Kramer), 12 (Page 19 of 151).

34. Solutions typically involved electrical contacts with a stack of metals having a high work function metal such as Ni, Pd, or Pt with a capping layer of gold to achieve specific contact resistances desired. EX-1016 (Voss), 23-24, 27,

63; EX-1017 (Kramer), 31 (Page 38 of 151). The gold capping layer was used to prevent oxidation as well as to promote current spreading in the contact. EX-1016 (Voss), 21-22, 25.

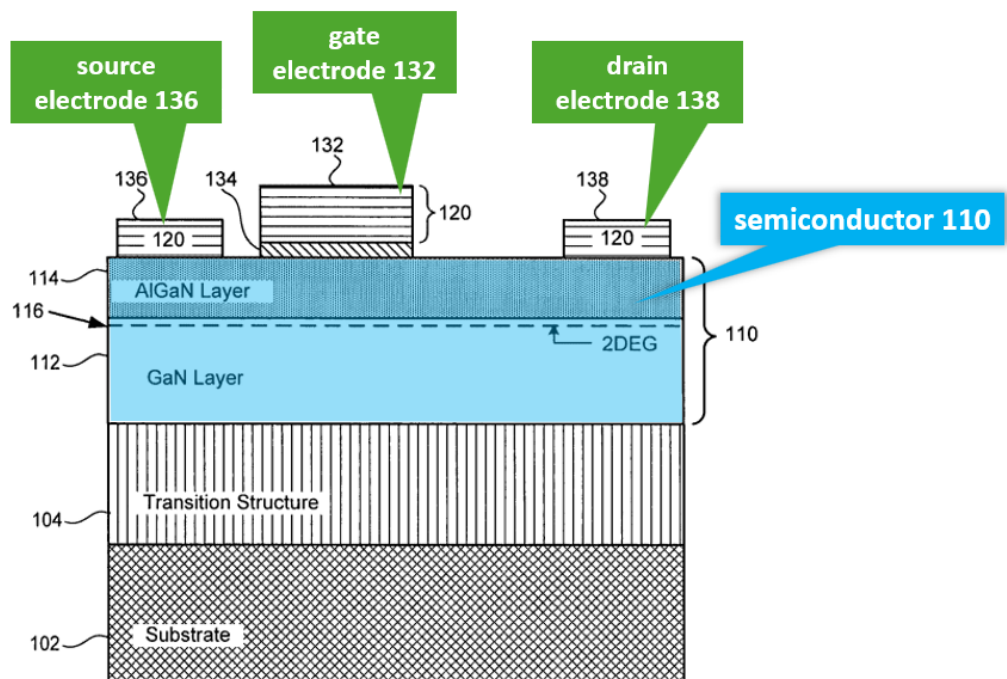
35. However, the inventor of the '562 Patent recognized multiple disadvantages to using gold (Au) as a capping layer – including gold's high cost and propensity to contaminate silicon fabrication process flows by diffusion through the electrode stack.¹ EX-1001, at 1:44–55. Such incompatibility with silicon-based semiconductor manufacturing made it difficult to integrate III-V semiconductor devices with silicon devices to benefit from the “energy efficiency and ease of fabrication of low power silicon.” *Id.*, at 1:25–29, 51–55.

36. The '562 Patent describes a new approach at the time to providing a gold-free electrical contact that is a silicon-compatible process and can be implemented on a III-V semiconductor device. The novel electrical contact for use on a semiconductor device comprises an electrode stack having a “capping layer” that is made up of a “refractory metal nitride.” EX-1001 at Abstract, 1:66–67, 2:19–21, 3:19–28. Capping the electrical contact with refractory metal nitride “presents significant advantages over the conventional art” and renders

¹ Gold was in common use as a capping layer of ohmic contacts. *See, e.g.*, EX-1013 (Quay), 147-49 (Page 174-76 of 492) (ohmic contacts with top Au (gold) layer); EX-1016 (Voss), 46 (describing convention ohmic contacts with Au top layer and that “Au is necessary to decrease the sheet resistance”).

“integration of group III-V ... semiconductor devices more efficient and cost effective by posing a reduced contamination risk to silicon.” *Id.* at 5:33–39.

37. The patent discloses three implementations of electrical contact, as a source electrode, drain electrode, and gate electrode, for use on a group III-V semiconductor device, specifically as a high electron mobility transistor (HEMT). EX-1001, FIG. 1, 2:53–65. For example, FIG. 1 shows “plurality of electrical contacts including source electrode 136, drain electrode 138, and insulated gate electrode 132.” *Id.*, 2:53–65. As shown in FIG. 1, source electrode 136, drain electrode 138, and insulated gate electrode 132 are in direct contact with semiconductor GaN body 110 which comprises GaN layer 112 and aluminum gallium nitride (AlGaN) layer 114. *Id.*



'562 Patent, FIG. 1 (annotated).

38. This overall arrangement of source, gate, and drain electrodes on a semiconductor illustrates the fundamental components of a field effect transistor (FET). The basic concept behind the transistor can be analogized to the flow of water through a channel. EX-1011 (Mishra), 246-248 (Page 270-272 of 583). The transistor has an active channel in the semiconductor through which charge carriers (electrons or holes) flow between from the source and the drain. EX-1011 (Mishra), 356-378 (Pages 380-402 of 583). The source and drain contacts are ohmic contacts. EX-1011 (Mishra), 356-358 (Pages 380-382 of 583). The conductivity of the channel is modulated by a potential applied to the gate, which is isolated from the channel. *Id.* This results in the modulation of the charge density flowing in the channel. *Id.*

39. In the '562 Patent, source/drain electrodes (such as source electrode 136 and drain electrode 138) are referred to as “power electrodes ohmically coupled to the heterojunction formed by GaN layer 112 and AlGaIn layer 114.” EX-1001, 3:19–21. *Id.* The drain and source are where current flow enters/exits the semiconductor in a transistor. A POSA understood the '562 Patent's description of ohmic coupling to be referring to ohmic contacts. An ohmic contact is a direct contact between a conductor and a semiconductor with certain ohmic electrical characteristics. An ohmic contact electrically behaves as a conductor

with a linear current-voltage (I-V) relationship under Ohm's law that has a much lower electrical resistance than a rectifying, non-ohmic contact. In the context of the '562 Patent, it is desirable for the ohmic contacts to have a low Specific Linear Contact Resistivity (SCLR). EX-1001, 1:33-43, 1:51-55. The source/drain electrode implementations of the electrical contact disclosed in the '562 Patent provide a direct contact between the electrical contact and the semiconductor.

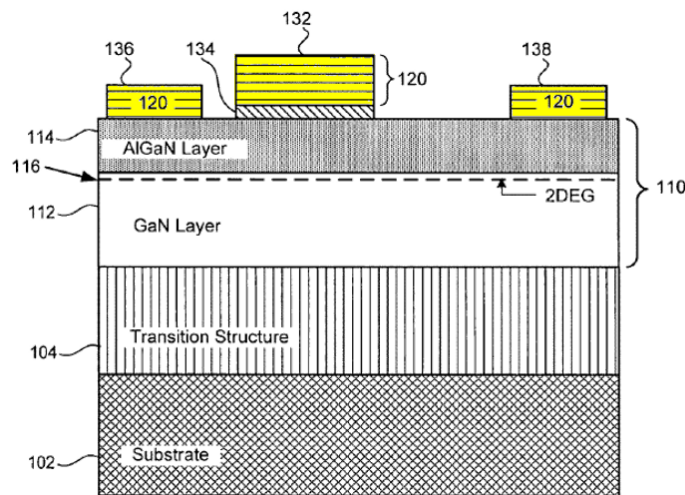
40. The '562 Patent also discloses two gate electrode implementations of its electrical contact: an insulated gate electrode and a Schottky gate electrode. EX-1001, 3:29-35, claims 11, 12, 16, 17. These are described further below.

41. FIG. 1 of the '562 Patent illustrates an example of an insulated gate electrode, in which "insulated gate electrode 132 includes gate insulator layer 134, such as a silicon nitride (Si_3N_4) or silicon dioxide (SiO_2) layer, for example, underlying electrode stack 120." '562 Patent, 3:29-31. In an insulated gate electrode for a transistor, the conductive gate electrode is capacitively coupled to the semiconductor underneath via a gate insulator layer, such that voltage on the gate electrode can modulate the charge carrier density inside the semiconductor and in turn, modulate the electron current flow through the semiconductor. In an insulated gate electrode the gate insulator layer makes direct contact with the semiconductor in order to provide the capacitive coupling between the conductive gate electrode and the semiconductor, because any air gap separating the gate

insulator and the semiconductor surface would significantly deteriorate the gate capacitive coupling due to air having the lowest dielectric constant compared to dielectric materials (a relative dielectric constant of ~ 1.0). Thus, the '562 Patent's insulated gate electrode implementation of the electrical contact (e.g., FIG. 1's insulated gate electrode 132, which includes gate insulator layer 134 underlying electrode stack 120), the electrical contact's gate insulator layer 134 makes direct contact with the GaN body 110 (i.e. a semiconductor). *See also* '562 Patent, Abstract ("forming ... a gate insulator layer between the electrode stack and the semiconductor device.").

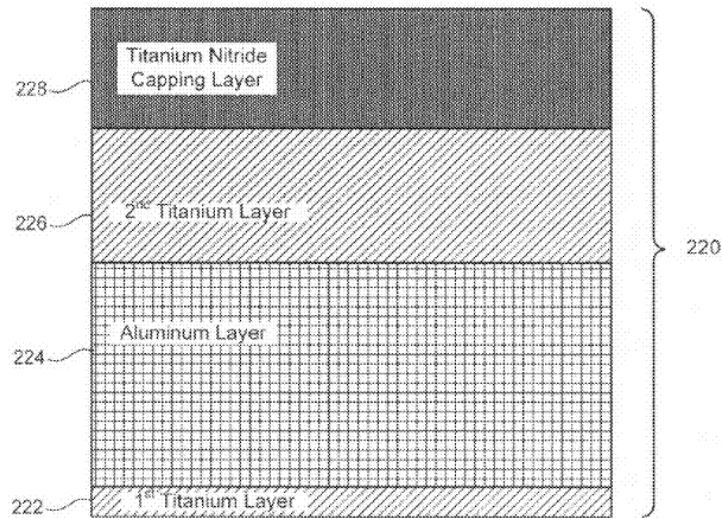
42. The '562 Patent also discloses a Schottky gate electrode implementation of the disclosed electrical contact in which "electrode stack 120 may make Schottky contact with GaN body 110." '562 Patent, 3:34-35, claims 11, 16, Abstract ("forming [] a Schottky metal layer ... between the electrode stack and the semiconductor device"). A Schottky contact is a junction between a metal conductor and a semiconductor that, unlike an ohmic contact, has a non-linear or rectifying I-V (current-voltage) electrical characteristics. A Schottky contact requires a direct contact between the metal conductor and the semiconductor. In the '562 Patent's Schottky gate electrode implementation of the electrical contact, the electrical contact makes direct contact with the GaN body 110 (*i.e.*, a semiconductor).

43. The '562 Patent also says that in the embodiment of the semiconductor device in FIG. 1, “each of source electrode 136, drain electrode 138, and insulated gate electrode 132 comprises electrode stack 120 [including] a refractory metal nitride capping layer (not explicitly shown in FIG. 1), such as a titanium nitride (TiN) capping layer.” *Id.* at 3:23–28. The electrode stack is highlighted in yellow in Figure 1 below.



'562 Patent, FIG. 1 (annotated).

44. FIG. 2 of the '562 Patent (shown below) illustrates an exemplary electrode stack 220 that includes a plurality of metal layers, such as first titanium (Ti) layer 222, an aluminum (Al) layer 224, a second titanium layer 226, and a titanium nitride (TiN) capping layer 228. '562 Patent, 3:36–45.



'562 Patent, FIG. 2.

45. According to one aspect of the claimed invention the capping layer made from refractory metal nitride has a thickness that is greater than that of a bottommost layer in the electrode stack. *Id.*, claim 1. For example, a titanium nitride (TiN) capping layer has a greater thickness than a thickness of a first titanium (Ti) layer (*i.e.*, the bottommost layer of the plurality of metal layers). *Id.* at 3:42–45, 4:25–27, 5:13–20.

46. The '562 Patent also describes the steps for fabricating a refractory metal nitride capped electrical contact according to some embodiments. *Id.* at Fig. 3, 4:4–5:32. For example, the patent describes that “first Ti layer 222 may be sputter deposited over GaN body 110” or “using a chemical vapor deposition (CVD) or electron beam deposition process,” and that “first Ti layer 222 is formed to a thickness of approximately 100 Å, plus or minus approximately ten percent

($\pm 10\%$).” *Id.* at 4:17–27. The patent also describes “depositing biased reactive TiN capping layer 228,” and that “TiN capping layer 228 may be formed to a thickness of approximately 600 Å, plus or minus approximately ten percent ($\pm 10\%$).” *Id.* at 5:1–22. Biased reactive TiN is “a species of TiN having a particularly high density” that is “also referred to in the art as ‘gold’ TiN.” *Id.* at 5:3–8. According to embodiments, the layers “may be patterned and plasma etched” and “annealed” “to produce one or more electrical contacts.” *Id.*, 5:23–32. The patent describes an anneal condition “at approximately 850 °C for approximately sixty seconds.” *Id.*

VI. RESPONSE TO DR. ZHAO’S TECHNOLOGY OVERVIEW

47. As I explained above in Section V, the technology at issue in this Investigation with regards to the ’562 Patent relates to electrical contacts for use on a semiconductor device. I have reviewed Dr. Zhao’s “Technology Overview” discussion. EX-1002 (Zhao Dec.), ¶¶48-73. Dr. Zhao’s Technology Overview omits or glosses over important technical details and does not accurately describe the relevant technology background that can reflect the state of the art in the August 2009 timeframe. Instead, Dr. Zhao’s description drastically oversimplifies the complex, unpredictable nature of the design and fabrication of electrical contacts, especially ohmic contacts. Dr. Zhao also glosses over and never addresses the technical constraints in gate contact design that are known to a

POSA. Further, Dr. Zhao's description confuses contact metal with interconnects, which refer to components that serve different functionalities and have different electrical characteristics in a semiconductor device.

A. Dr. Zhao Does Not Account for the Unpredictability Inherent in Ohmic Contact Design and Fabrication

48. An ohmic contact is a junction between a conductor and a semiconductor that is purposefully designed and intended to electrically behave as a conductor with a linear current-voltage (I-V) relationship under Ohm's law that has a much lower electrical resistance than a rectifying, non-ohmic contact. Designing ohmic contacts on a semiconductor device is a highly complex and interdisciplinary field, implicating both materials science and semiconductor physics. In August 2009, a POSA would have understood that designing an ohmic contact on a particular semiconductor involves practical considerations and selections of multiple materials properties of both the metal and the semiconductor.

49. The general principles of an ohmic contact design can initially be understood using an energy band diagram across the metal-semiconductor interface such as the one I reproduced below. Initially, a Schottky barrier forms at a metal-semiconductor junction that can impede electron flow across the junction and is generally non-ohmic. In principle, the height of the Schottky barrier is related to a work function of the metal relative to the position of the conduction band energy E_c for an n-type semiconductor (or valence band energy E_v for a p-type

semiconductor in which there will be holes, rather than electrons, that flow across the metal-semiconductor junction). Also generally speaking, narrowing the width of the Schottky barrier can allow electrons to more easily tunnel through the Schottky barrier across the interface. This can in principle be facilitated by heavily doping the semiconductor (such as the n^+ region below). *See, e.g.*, EX-1011 (Mishra) at 229–230. Theoretically, lowering the Schottky barrier height can facilitate a narrower barrier width, or additionally allow more electrons to climb over the top of the lowered barrier through processes such as thermionic emission. *See, e.g.*, EX-1016 (Voss) at 22, 23; EX-1013 (Quay) at 145.

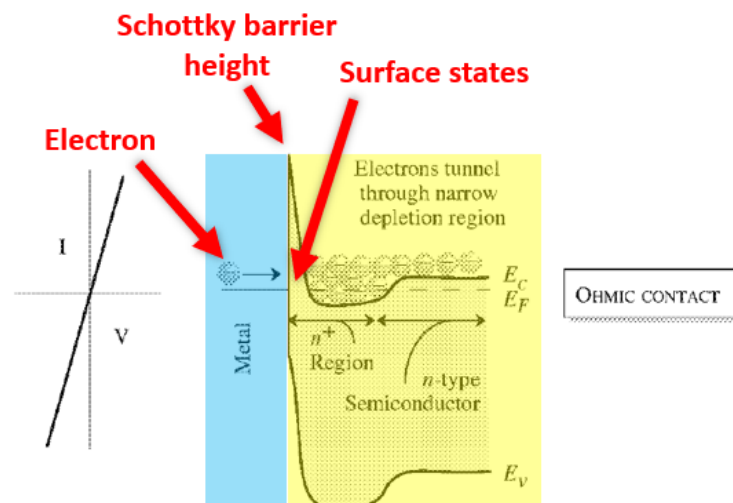


Figure 5.7: Current-voltage characteristics of an ohmic contact along with the band diagrams of metal $-n^+-n$ contact. The heavy doping reduces the depletion width to such an extent that the electrons can tunnel through the spiked barrier easily in either direction.

EX-1011 (Mishra) at 229 (annotated).

50. At the time of the filing of the '562 Patent (*i.e.*, August 2009), it was well known to a POSA that these general theoretical principles of Schottky

contacts and ohmic contacts are complicated in practice by the necessary interactions of multiple material properties that affect the performance of a designed ohmic contact, often in unpredictable ways that do not follow theoretical predictions. One source of uncertainty is the existence of interface states, also known as surface states at the surface of the semiconductor. The surface states are known to “make[] the prediction of barrier height using [theoretical equations] inaccurate.” EX-1016 (Voss), 25. The surface states are affected by the surface quality and processing steps (*e.g.*, surface pretreatment prior to metal deposition) of the semiconductor. EX-1011 (Mishra), at 228; EX-1013 (Quay) at 145. Surface states are also affected by metal diffusion, *e.g.*, through a thermal anneal which may cause the metal to diffuse or otherwise interact with atoms on the surface of the semiconductor. *See* EX-1013 (Quay) at 145. For example, the composition and thickness of the metal, especially the bottom layer of the metal making contact, as well as the composition (*e.g.*, containing atoms of Si or III-V materials) and doping (*e.g.*, amount and type of dopant atoms) of the semiconductor may impact how the atoms across the interface chemically react and alter the surface states. The metal work function varies by metal, and the semiconductor energy bands also vary based on the different doping type/level and different band gap of the semiconductor material. Different metal/semiconductor combinations are

therefore expected to have inherently different Schottky barrier characteristics and behave differently in terms of ohmic or non-ohmic behavior.

51. Thus, even a relatively small change to the composition of either the metal, the semiconductor, or to the processing conditions such as surface treatment and anneal condition, can impact the nature of the resulting Schottky barrier, and in turn whether or not the electrical characteristics of the junction behave as an ohmic contact. Some of these issues that affect ohmic contact formation are also summarized in EX-1013 (Quay), which include:

Issues of Ohmic Contact Formation

The issue include the following:

- The increase of the density of states at the interface for wide bandgap semiconductors with a bandgap of $\geq 3.4\text{eV}$
- The pretreat of the sensitive semiconductor surface prior to metal deposition
- The control of the metal morphology due to the high annealing temperatures of at least 600°C [4.163] necessary due to the wide bandgap, including:
 - The control of the vertical diffusion of metal by high temperature annealing [4.50]
 - The control of the lateral diffusion of contact metals to avoid surface and gate leakage
 - The control of the morphology for e-beam or optical pattern recognition

EX-1013 (Quay) at 145.

52. In my opinion, Dr. Zhao improperly relies on overgeneralizations and overlooks the widely prevalent teachings in the cited literature explaining the complex, unpredictable nature of the design and fabrication of electrical contacts. For example, Dr. Zhao cites a textbook EX-1015 (Neaman) for the proposition that “[a] POSITA knew about ... [t]he ideal nonrectifying barrier.” EX-1002 (Zhao

Dec.), ¶56. Yet Dr. Zhao neglects to mention that the same chapter he cited warns that “[t]he ideal energy bands shown [] do not take into account the effect of surface states... if we assume that donor surface state exists in the lower half of the band gap ... we may not necessarily form a good ohmic contact.” EX-1015 (Neaman) at 346.

53. Dr. Zhao also did not mention that EX-1021 (Kayali) teaches that:

The preceding description assumed ideal material conditions. Specifically, it was assumed that the semiconductor lattice structure was uniform and perfect, even at the surface of the material. In practical cases, this is not possible. The atoms on the exposed surface do not have the required neighboring atom to complete all of the covalent bonds. Therefore, these surface atoms may either give up an electron and become a positively charged donor ion, or accept an electron and become a negatively charged acceptor ion. Surface states and their associated charge cause the energy bands of the semiconductor to bend even before the metal is introduced, as shown in Figure 3-9. Furthermore, when the metal is brought into contact with the semiconductor, the surface states may be able to accommodate all of the charge movement required to equalize the free electrons between the two materials. When this occurs, the barrier potential is no longer dependent on the metal work function. Also, no additional band bending of the semiconductor occurs because of the metal-semiconductor contact. In other words, the junction characteristics are not dependent on the metal interface.

EX-1021 (Kayali), 27.

54. In my opinion, a POSA in August 2009, though aware of the general theoretical principles of Schottky contacts and ohmic contacts, was not able to reliably predict the resulting electrical performance of a contact as a result of depositing a particular metal to a particular semiconductor, or changing an aspect

of an existing ohmic contact design in the metal or in the semiconductor. Rather, as a result of complexities such as those I described above, a POSA would make a prototype to test the effects of design changes. In fact, it is known that “[i]n order to determine barrier height[], it is necessary to fabricate a specimen to test.” EX-1016 (Voss) at 25. This lack of a robust theoretical model to predict the effects of design changes has led artisans to deem the fabrication of ohmic contacts “more an art than a science.” EX-1017 (Kramer), 31 (Page 38 of 151).

55. As a result, every laboratory tended to have “its own favorite recipes which involve particular metal or alloy systems, particular deposition methods and particular forms of heat treatment.” EX-1017 (Kramer), 31 (Page 38 of 151). The number of factors in the material choice (of both the metal and semiconductor) and processing conditions that might be varied to change the ohmic vs. non-ohmic behavior of a metal-semiconductor contact, only some of which I have listed, inherently required a POSA to experiment with physical prototypes, in a trial and error process where each incremental change has to be tested and evaluated to determine whether the desired ohmic performance was met. Unsurprisingly, in August 2009 and still today, electrical contact design was a lengthy process that took months and sometimes years of significant experimentation. In my experience in the industry, and now in academia for the past 27 years, I have found that it typically takes over 12 months to create a new electric contact design, even

when working from existing or prior designs for inspiration and can often take up to three years. This was true in August 2009 as well. For example, when I was at Nitronex, it took me and a number of scientists about 3 years of diligent work, including design, testing, iteration and reliability validation to complete an ohmic contact and gate contact design on a GaN-based device. I note that this work at Nitronex is listed in p. 147 of EX-1013 (Quay) which Dr. Zhao cites.

56. In my opinion Dr. Zhao's report does not reflect the perspective of a POSA because he does not account for the complexities of electrical contact design, some of which are outlined above, and the resulting unpredictability. More importantly, Dr. Zhao neglected to consider the important context that Schottky or ohmic contacts are highly unique to one particular semiconductor and are not considered in a vacuum or with respect to any semiconductor. Rather, a POSA would understand that a specific semiconductor and related electric contact design is like a lock and key, with the electric contact design carefully tailored and validated experimentally to function as Schottky or ohmic contact only to the specific semiconductor.

57. Dr. Zhao also does not address the concerns that a POSA would have held that incorporating a metal structure from one device (sometimes not even intended to be an electrical contact at all as I will discuss below) into another would require multiple changes for that added structure to work as desired as an

electrical contact, which were generally appreciated only after extensive prototyping and measuring performance. Dr. Zhao offers another over-simplified statement that “[i]t was well-known by August 2009 that a variety of metals can be chosen to form either a Schottky contact or an ohmic contact GaN devices.” EX-1002 (Zhao Dec.), ¶65. In my opinion this statement ignores or glosses over the knowledge of a POSA that an electrical contact designed for a particular semiconductor device would not necessarily function as an electrical contact to another without significant experimentation. In fact, the two studies (Wu, Foresi) cited in EX-1002 (Zhao Dec.), ¶65 to purportedly support the above-quoted statement show the opposite. Even choosing the same metal may not always result in ohmic contact for the same semiconductor material. Foresi found that “as-deposited Al” contacts to n-GaN “are ohmic,” and that “annealing of Al contacts may result in the formation of a thin insulating AlN interlayer, which will increase its contact resistance.” EX-1020 (Foresi-1993), at 2861. On the other hand, Wu found that “Al/n-GaN” contacts have “rectifying behavior for the as-deposited diodes and for annealing temperatures up to 400 °C,” and the contact only becomes ohmic after annealing at 500 °C or above. EX-1012 (Wu-2001), 426. Therefore, based on Wu and Foresi a POSA would not understand Al can be chosen to form an ohmic contact to n-GaN without investigating further (e.g., to understand the specific n-doping level, and/or nature of the surface condition and surface states of

the particular n-GaN semiconductor), and these references do not support Dr. Zhao's generalized assertion.

B. Dr. Zhao Never Addresses the Technical Constraints in Gate Contact Design

58. In the section "Gate Contacts," Dr. Zhao merely offers generic statements such as "gate isolation is performed in a variety of ways, leading to many different devices," and "Schottky contacts serve as the gate contacts in HEMTs." EX-1002 (Zhao Dec.), ¶61. But Dr. Zhao's analysis fails to consider the technical constraints a POSA in August 2009 would have known in choosing a particular gate contact design for a particular semiconductor in a transistor.

59. A gate contact is a contact between a conductor and a semiconductor purposefully designed and intended to provide a voltage to modulate conduction of electrons in the semiconductor underneath the gate contact. Just like in an ohmic contact, it is well known by August 2009 that a gate contact design is uniquely suited to a specific semiconductor, and a gate contact for one type of semiconductor would not necessarily function when placed on a different semiconductor.

60. In an insulated-gate type transistor, the gate contact is capacitively coupled to the semiconductor via an insulating dielectric layer sometimes referred to as a gate dielectric. One common type of insulated-gate transistor is a metal-oxide semiconductor field effect transistor (MOSFET) which uses an oxide as gate

dielectric. Typically, in a transistor conduction in the semiconductor channel is off until a voltage applied on the gate electrode surpasses a threshold gate voltage V_T . In doing so, the gate voltage on the gate electrode in an insulated-gate transistor shifts the potential inside the semiconductor. By August 2009, it is well known that the work function of the metal in the gate contact would proportionally raise or lower the potential of the semiconductor underneath the gate dielectric even when no voltage is applied on the gate electrode. Therefore, it is well known in semiconductor device design that V_{th} of an insulated-gate transistor is dictated by the metal work function of the gate contact, as V_{th} is essentially how much extra voltage is needed to be applied in addition to the metal work function to modulate the potential inside the semiconductor. V_{th} has been an important design parameter for a transistor designer with tight constraints based on the available voltage range from a power supply or from a customer's requirements. Therefore, it is required that the metal in a gate contact to have a particular work function value. Moreover, because the potential of electrons in a semiconductor (sometimes refers to as Fermi energy E_F) also depends on factors such as the bandgap and doping type/concentration of the semiconductor, a POSA would understand that different types of semiconductor devices (e.g. n-type MOSFET vs. p-type MOSFET) require different work function value for their respective gate contacts. *See, e.g.*, EX-1005 (Yu), [0004].

61. In a Schottky-gate type transistor, the gate contact is a Schottky contact forming a Schottky barrier between a metal in the gate contact and the semiconductor surface. It is known to a POSA that the Schottky barrier height is an important practical aspect for a transistor utilizing a Schottky gate. *See, e.g.*, EX-1006 (Adesida), [0004]. For example, an enhancement-mode transistor (which is defined by the transistor being normally-off when no voltage is applied to the gate), relies chiefly on a high Schottky barrier height of the gate metal to deplete the channel and to obtain positive threshold voltage, V_{th} . *See id.*, [0005]. As I have discussed in Section VII.A, different metal/semiconductor combinations are known to a POSA to have inherently different Schottky barrier characteristics. Even a relatively small change to the composition of either the metal, the semiconductor, or to the processing conditions such as surface treatment and anneal condition, can impact the nature of the resulting Schottky barrier. *See, e.g.*, EX-1013 (Quay), 154–156 (discussing Schottky barrier height of various metal on various semiconductor materials of different doping type/concentrations, as well as the effect of surface pretreatment and annealing). A POSA by August 2009 would understand that a Schottky gate contact designed for a particular semiconductor device would not necessarily function as a Schottky gate contact to another without significant experimentation.

C. Dr. Zhao Confuses Interconnects with Electrical Contacts

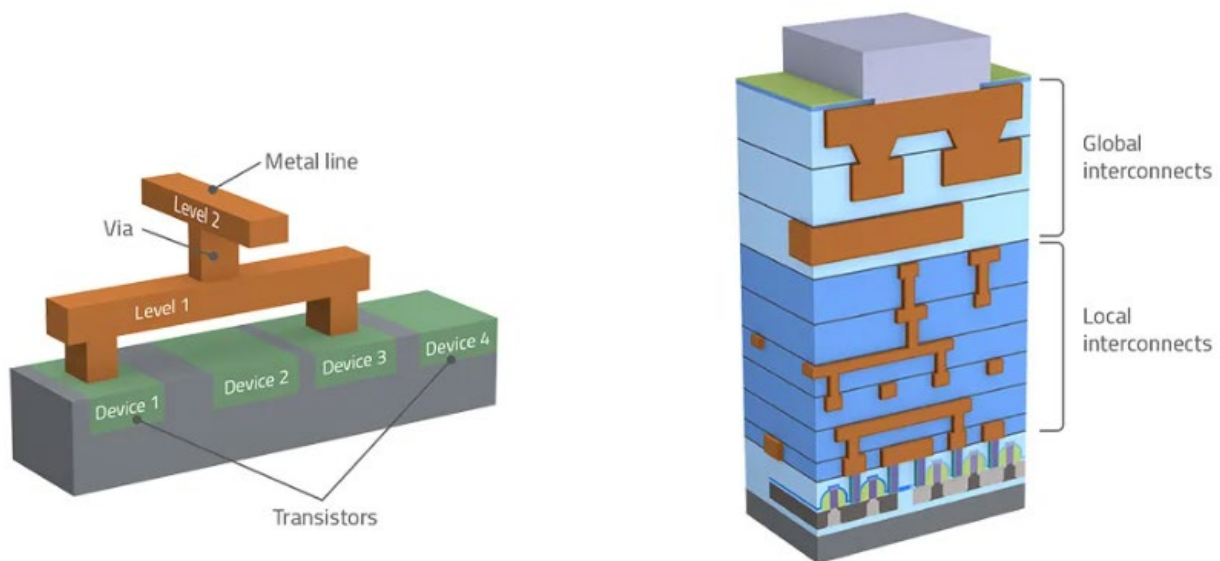
62. In the section “Contact Metals,” Dr. Zhao appears to classify “interconnects” as being in the same category as electrical contacts, such as “Schottky barriers,” “ohmic contacts,” and “gates in transistors.” EX-1002 (Zhao Dec.), ¶63. While I agree with Dr. Zhao that metals have been known for many decades to be used as interconnects connecting various semiconductor devices together, generally an interconnect does not have a metal – semiconductor junction like an ohmic contact or gate contact and therefore would not have been confused with an electrical contact.

63. An interconnect is a term of art since well before August 2009 to specifically refer to conductive strips (commonly aluminum or copper) or wiring that provide low resistance paths for current and *interconnect* various semiconductor devices. *See, e.g.*, EX-1004 (Usui), 1:5-2:38 (describing interconnects as “electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure”), 4:10-15 (interconnect layer in Fig. 8 is “repeated in a multiple level sequence to complete the interconnect circuit for the devices.”). One reference that Dr. Zhao relies upon describes interconnects in the following way:

In semiconductor circuits, **interconnects provide pathways through which charge travels from one point to another.** While these interconnects are obviously passive elements of the circuit they are

extremely important and play a role in circuit performance. The **metal strips making up the interconnect** must be able to carry adequate current and make good contact with the devices. Interconnects are **deposited on insulators and touch the active devices only through windows that are opened at select points.**

EX-1011 (Mishra), 261 (Page 240 of 583). For example, in the illustrations below interconnect structures are made multiple levels of metal lines and connecting vias are serve as the wiring between semiconductor devices, such as transistors.



EX-2027 (available at <https://semiengineering.com/all-about-interconnects/>).

64. This has been the understanding of a POSA for several decades as the excerpt from U.S. Patent No. 6,249,056 (Kwon) illustrates:

The metallization process provides interconnections between contacts within semiconductor devices and between devices and conductive pads. To make electrical connections in smaller and more complex

chips, multilevel metal interconnects are formed in the semiconductor process. The metal interconnect may be composed of Al, Ti, Cu, W, or other suitable conductive material or combination. A recess such as hole or via is bored through a dielectric covering a first level layer of metal, or a second level layer of metal. The recess is filled with a conductive material (i.e. Al, Ti, Cu, W). The conductive material in the via provides an electrical connection between the first metal layer and the second metal layer or between any two metal layers.

EX-2028 (Kwon), 1:20-34.

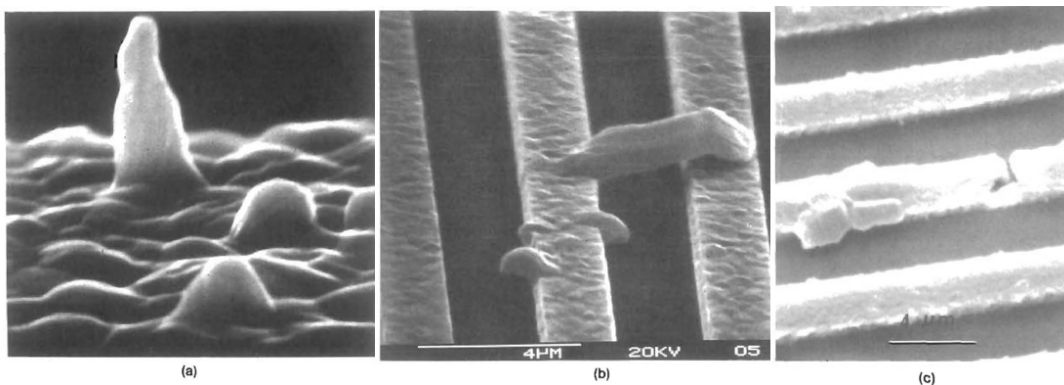
65. Thus, interconnects, typically formed in metal strips were generally understood as the wiring carrying the current *between* semiconductor devices. The connections of the interconnects were almost exclusively metal-to-metal junctions between horizontal lines and vertical vias. Any connection to the semiconductor material itself was generally separated from the process flow both because interconnect materials posed problems when they came into contact with the semiconductor. Instead, specialized electrical contacts have been used to form a metal – semiconductor junction and address the unique physics involved.

1. Problems with Interconnects

66. As greater numbers of devices are connected together, the interconnects must be able to handle the increased aggregated current and thus tend to be thicker at higher interconnect levels. One of the main challenges with designing smaller and smaller integrated circuits is the need for small interconnect

lines that can still carry suitable current. As the size of the wiring decreases, resistivity increases. This can lead to a phenomenon referred to as electromigration. “The term electromigration refers to the current induced mass transport which occurs in a conductive material maintained at an elevated temperature and through which current is passed wherein atoms of conductor material are displaced as a result of the combined effects of direct momentum exchange from the moving electrons and the influence of the applied electric field.” EX-2029 (U.S. Patent No. 4,017,890, “Howard”), 1:27-45.

67. Under high-current-density conditions, metal-atom migration can cause voids (open circuit) in some regions of the interconnect lines, or metal atoms can pileup to form hillocks that can degrade performance or even bridge separate interconnect lines causing short circuits. EX-2030 (Jaeger), 157; EX-2031 (Ohring), 380–381.



EX-2031 (Ohring), 380–381 (illustrating electromigration damage in Al films: (a) hillock growth; (b) whisker bridging two conductors; (c) nearby mass accumulation and depletion).

68. Furthermore, by August 2009 it is well known to form multiple-level interconnects in a transistor device to route signals both laterally, and vertically between different levels using conductive plugs and vias. One example of such a multilevel interconnect system is shown in the textbook by Jaeger, which I have reproduced below. *See* EX-2030 (Jaeger), FIG. 7.20(a). As shown below, FIG. 7.20(a) of Jaeger illustrates a cross-section of a device with six levels of metal interconnections, referred to as “Metal-1” to “Metal-6.” These interconnections run parallel to the surface of the semiconductor which is shown at the very bottom of FIG. 7.20(a) underneath Metal-1. The interconnections are formed on insulators such as silicon nitride or silicon oxide that provide electrical isolation between the different interconnection levels. These insulators were known as interlayer dielectrics or interlevel dielectrics (ILD). The multilevel interconnections provide conductive paths between different points in the device, which is better illustrated in the perspective view image in Jaeger’s FIG. 7.20(b) with the ILDs removed. In FIG. 7.20(a), the ohmic contact and gate contacts are made to the surface of the semiconductor as I have annotated.

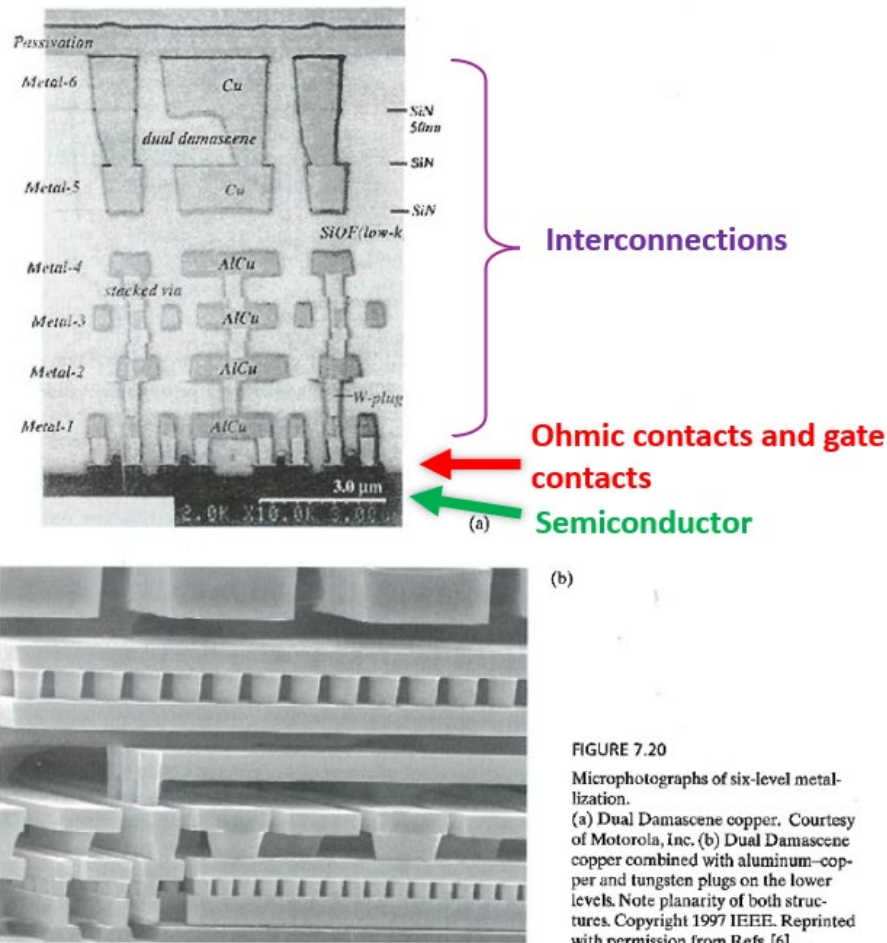


FIGURE 7.20
Microphotographs of six-level metalization.
(a) Dual Damascene copper. Courtesy of Motorola, Inc. (b) Dual Damascene copper combined with aluminum-copper and tungsten plugs on the lower levels. Note planarity of both structures. Copyright 1997 IEEE. Reprinted with permission from Refs. [6].

EX-2030 (Jaeger), 171 (annotations added). These interconnect structures (including those of Usui) would not have been mistaken for electrical contacts as described by the '562 Patent.

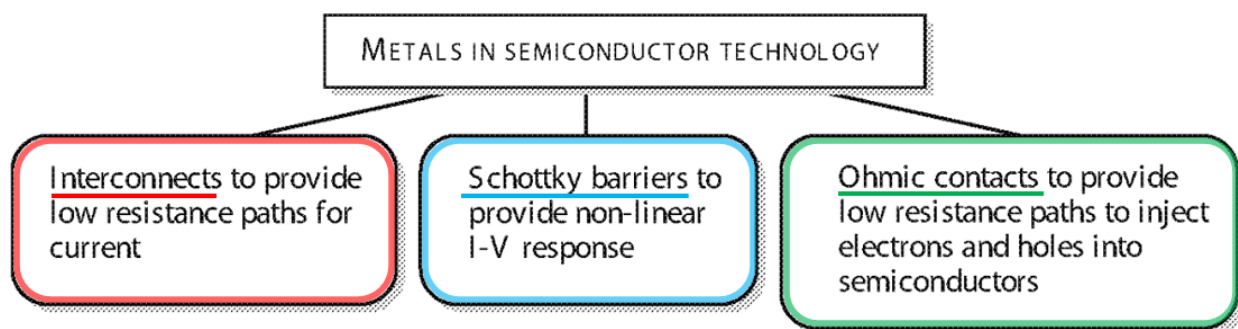
2. Electrical Contacts

69. Electric contacts have been the source of extensive semiconductor research for several decades. Dr. Zhao relies on EX-1016 (Voss) as representative of the state of the art, which explains that “[e]lectrical contacts to semiconductors are generally understood *as the junction between the semiconductor and a metal* or other contact material.” EX-1016 (Voss), 21. Several other references cited by

Dr. Zhao describe electrical contacts as metal–semiconductor junctions. *See, e.g.*, EX-1011 (Mishra), 229 (Pages 253 of 583) (“We have also seen from the previous section that at least in some cases a ***metal–semiconductor junction*** also provides a barrier to flow of electrons [Schottky barrier]. However, it is possible to create metal-semiconductor junctions that have a linear non-rectifying I-V characteristic, as shown in figure 5.7. Such junctions or contacts are called ohmic contacts.”); EX-1013 (Quay), 144 (Page 171 of 492) (“The formation of ***metal–semiconductor interfaces or contacts*** defines a second critical process step for any electronic device. Both ohmic and Schottky contacts are of critical importance with respect to device functionality, performance, and long-term reliability.”); EX-1017 (Kramer), 31 (Page 38 of 151) (“This chapter deals with the first of the two limiting cases of ***metal - semiconductor contacts***: the Ohmic contacts”), 87 (Page 93 of 151) (“This chapter is concerned with the second of the two limiting cases of ***metal–semiconductor contacts***: the Schottky contacts.”) 120 (Page 125 of 151) (“Chapter 4 showed that almost all practical Ohmic contacts are tunnel contacts that depend on the presence of a thin layer of highly doped (degenerate) semiconductor material near the ***metal–semiconductor interface***.”).

70. Electrical contacts could often be made from multiple very thin (nanometer scale) layers of conductive material in the form of a stack. It was typically necessary to anneal the contacts at elevated temperatures to achieve the

required properties such as a low specific contact resistance. This heat treatment causes the atoms of the layers to interact in often unpredictable ways and thus it was important to consider the layers above the junction itself as they would affect the performance of the contact. Electrical contacts, particularly for use in a transistor, generally embodied either power electrodes such as a source or drain electrode (requiring ohmic contact) and gate electrodes, such as a Schottky gate or insulating gate. Ohmic contacts provide low resistance paths to inject electrons and holes into semiconductors and (ideally) linear current-voltage (I-V) response, while a Schottky barrier provides non-linear I-V response, *e.g.*, to control the flow of current. *See, e.g.*, EX-1011 (Mishra) at 218. As illustrated below, although interconnects, Schottky barriers, and ohmic contacts were often all made from metals, their different usage demanded distinction and different investigations to determine suitable materials.



EX-1011 (Mishra), 218 (color added).

71. In other words, not all metals in a semiconductor device have the same purpose and could not be said to be interchangeable. By August 2009 it was

well known to a POSA how to discern if a metal component in a transistor is an interconnect or serves as an electrical contact such as gate contact or ohmic contact based on the structure and functionality of the metal component. For example, interconnects are made up of metal strips and are deposited on insulators. EX-1011 (Mishra) at 216. Interconnects are low resistance conductors that can carry very high current densities. *Id.*, 216, 217. Unlike Schottky contacts and ohmic contacts, interconnects do not provide non-linear IV response like Schottky contacts nor inject electrons and holes into semiconductors like ohmic contacts. *Id.*, 218. As many of the references cited by Dr. Zhao illustrate, electrical contacts had their own highly complex design challenges. EX-1008 (Pearson), 41-59 (Pages 53-71 of 383) (discussing electrical contacts); EX-1013 (Quay), 144-157 (Pages 171-184 of 492); EX-1016 (Voss), 21-27 (same); EX-1017 (Kramer), 11-126 (Pages 18-130 of 151) (same). And while Dr. Zhao cites these as supporting a POSA's knowledge of an electrical contact, none of these references describe electrical contacts as interconnects. And Dr. Zhao's failure to explain why he considers Usui's interconnect structure to be an electrical contact is telling in light of the contrary evidence.

D. Dr. Zhao's Mistakes Regarding Diffusion Barrier Layers

72. I also notice that Dr. Zhao mischaracterized certain teachings in the prior art regarding diffusion barrier layers, and made statements that are otherwise

unsupported. As one example, Dr. Zhao cites page 92 of EX-1021 (Kayali) as purported support for the assertion that “it was well-known that using a thin layer of titanium as the bottommost metal layer in a metallization structure ... provides a barrier for metal diffusion into the underlying semiconductor layer.” EX-1002 (Zhao Dec.), ¶67. However, this statement mischaracterizes EX-1021 (Kayali) and is otherwise unsupported. EX-1021 (Kayali) clearly states that it is a different layer (Pd or Pt) and not the layer of titanium that provides a barrier for metal diffusion. *See* EX-1021 (Kayali), at 92 (“The common gate metallization structure consists of three layers. The first layer contacting GaAs is a thin Ti layer used primarily for adhesion. The second layer is either Pd or Pt. This layer is used as a barrier to Au diffusion into GaAs. The last layer is thick Au used for conduction.”). In my opinion, it was well-known that a bottom metal layer would have been intended to have some diffusion into the underlying semiconductor layer to form an electrical contact on the semiconductor. As I explained above in Section VI.A, it was well known to a POSA by August 2009 to use a thermal anneal to cause the bottommost metal layer (*i.e.*, the metal layer that is deposited in contact with a semiconductor) to diffuse into or otherwise interact with atoms on the surface of the semiconductor to adjust the semiconductor surface states as part of the experimentation for a Schottky contact or ohmic contact design. In fact, in the very next page to what Dr. Zhao has cited, EX-1021 (Kayali) discloses it is

necessary to alloy a metal into GaAs to provide low contact resistance. EX-1021 (Kayali) at 93 (“The most common system for ohmic contacts is AuGe/Ni, which is alloyed into the GaAs at temperatures in excess of 400°C to provide the necessary low contact resistance (0.1 to 0.5 Ω /mm).”).

73. In the section “Diffusion Barrier Layers,” Dr. Zhao also generally states that “[d]iffusion barrier layers were known to be formed as a bottommost metal layer of a metallization structure.” EX-1002 (Zhao Dec.), ¶70. Dr. Zhao’s statement requires context as it appears to purport that it was known to form diffusion barrier layers in *any* kind of metallization structures. I disagree with this generalized notion. In my opinion, a POSA would consider this statement to be only applicable to metal interconnections, and not necessarily to other metal structures such as Schottky contacts or ohmic contacts. As I explained above, not all metal structures in a semiconductor device are equal. Metal interconnections are understood by a POSA as serving a different function from metal structures serving as Schottky contact and ohmic contacts, each with unique design constraints on the structure, composition and processing conditions. As I explained, it was well known to a POSA by August 2009 to use a thermal anneal to cause the bottommost metal layer to diffuse into or otherwise interact with the semiconductor in a Schottky contact or ohmic contact. A POSA therefore would

not consider using a diffusion barrier as a bottommost metal layer in a Schottky contact or ohmic contact with a semiconductor.

74. Further, in my opinion Dr. Zhao's statements in ¶70 of his declaration are more particularly limited to a specific type of interconnections, *i.e.*, copper interconnections, and Dr. Zhao has not cited any evidence such knowledge can be generalized outside the context of Cu interconnections. For example, all the documents Dr. Zhao relied in ¶70 are directed to copper interconnection and in particular, copper interconnection formed on insulating layers. *See, e.g.*, EX-1022 (Chin-2009) at ¶0005 ("traditional aluminum interconnection has failed to meet the requirements. Copper has been used to replace aluminum for deep sub-micron devices."); EX-1023 (Suh-590) at 1:27-33 ("multi-layered metal interconnects are preferably formed of a metal layer having low resistivity and high reliability, in order to improve the performance of the semiconductor device. A copper layer is generally used for the metal layer") and 1:62-66 ("it is necessary to form a diffusion barrier layer in order to limit diffusion of copper from the copper layer forming the metal plug and/or the upper interconnect. The diffusion barrier layer prevents the copper atoms from being diffused into the insulating layer."); EX-1024 (Chen-976) at Abstract ("A copper interconnect barrier layer structure includes a thin titanium nitride (TiN) (or tantalum nitride [TaN]) nucleation layer disposed directly on the dielectric substrate (e.g., a single or dual-damascene

copper interconnect dielectric substrate.”). Copper diffusion from a Cu interconnect into a silicon substrate has been known to a POSA well before August 2009, and in my opinion a POSA would understand that the teachings in these references cited by Dr. Zhao are limited to solving this particular problem. *See, e.g.,* EX-1023 (Suh-950) at 1:57-62; EX-1022 (Chin-2009) at ¶0005; EX-2030 (Jaeger), 168–171.

75. Where a diffusion barrier layer is used, a POSA would also have understood that a thicker barrier layer can provide better diffusion prevention performance, and that a thin barrier layer may not provide sufficient diffusion prevention. For example, Adesida teaches applying an iridium contact “at a thickness sufficient to prevent diffusion of [] further metal into the semiconductor surface below the iridium contact.” EX-1006 (Adesida), [0015].

VII. “ELECTRODE STACK” CLAIM CONSTRUCTION

76. I understand that the Board’s Decision Granting Institution of *Inter Partes* Review (Paper 10, “DI”) invited the parties to “take positions on the appropriate construction of” the term “electrode stack.” Paper 10 (DI), at 14.

77. I reviewed the Petition (Paper 1) and Dr. Zhao’s accompanying declaration (EX-1002) and was unable to locate anywhere where the Petitioner and Dr. Zhao explained what the claim term “electrode stack” means.

78. I also reviewed the transcript for the September 5, 2025 deposition of Dr. Zhao to see if he provided an explanation there of what the claim term “electrode stack” means. EX-2026 (Deposition of Dr. Zhao, “Zhao Dep.”). He was unable to provide any such explanation during the deposition. In fact, based on the transcript, it does not appear that Dr. Zhao gave the “electrode” part of the term “electrode stack” any weight at all. For example, when asked directly what he believed the meaning of the term “electrode stack” was, Dr. Zhao provided no definition or explanation, and instead said that his analysis “solely” focused on the “plurality of metal layers” and “capping layer” that the claimed “electrode stacks” includes.

Q. Can you tell me what an electrode stack is?

A. Again, at the very beginning, we went through this. For claim -- patent 562, claim 1, it clearly state[s] that electrode stack includes, includes metal layers and capping layer. And anything that is not a metal layer, or a capping layer of that electrode stack is unclaimed. So all -- **all my analysis, all discussion, solely focus on those metal layers and a capping layer.** And, you know, I been provided this description already. And so, yeah, these are my answer again.

EX-2026 (Zhao Dep.), 172:20-173:5. This statement, which indicates that Dr. Zhao did not consider whether the metal layers and capping layer were part of an *electrode* stack in the first place – and *solely* focused on the metal layers and capping layers regardless of whether they were part of an electrode stack – is

consistent with the absence of analysis regarding the term “electrode stack” in his declaration, and the testimony he provided a dozen or more times earlier during the deposition:

- EX-2026 (Zhao Dep.), 9:8-16 (“Anything outside this metal layers and the capping layer is unclaimed.”);
- *Id.*, 9:25-10:23 (“...anything that is outside this metal layer, or capping layer is unclaimed”);
- *Id.*, 11:18-12:7 (“All my analysis has been focused on those metal layers, the capping layers, because they include all the claim features.”);
- *Id.*, 30:8-33:6 (“...the electrode stack includes metal layers and the capping layer and everything outside, that everything is not a capping -- is not a metal layer or capping layer of the electrode stack is unclaimed”);
- *Id.*, 39:12-40:14 (“When I analyze 562 patent in claim one, it only -- it disclose the electrode stack as metal layers and the capping layer, and anything outside this is not a metal layer, or capping layer, regardless. It’s unclaimed.”);
- *Id.*, 42:2-17 (“...I focus my analysis on the capping layer, metal layers and bottom layer ... And if there are other part of electrode stack such as via, they are irrelevant here. They are irrelevant here.”);

- *Id.*, 42:18-43:3 (“I provide answers multiple times that on our matter discussing today, focusing on the metal layers and the capping layer, which are the claim features, includes all the claim features. And via, number 10, and whether it’s part of this broadly included electrode is irrelevant, because in the, in Usui, as well as in others. And then, in fact, it’s true as well, only those metal layers and capping layer are the claim features.”);
- *Id.*, 43:4-18 (“I already provide my opinion that whether this via 10 is part of electrode stack or not is irrelevant here for the reasons I provide many, many times. And in the end, of course the outside world will be electrically connected to the device 6 of Usui, the semiconductor device layer through this, this metal layers, and capping layer, and the via. And then, this depends on, you know, how you define this electrode stack. But our discussion, as well as when we look at fact 2 pattern, Usui and Yu are only focusing on the metal layers, which are 13, 14, 15, 18 and 19 in Usui’s 8 figure.”);
- *Id.*, 76:1-77:11 (“So I ask -- answer this question multiple, multiple times today and I can go from the very beginning, when we analyzed the -- when we look at 562 patent, and the claim one clearly state that electrode stack includes metal layers and the capping layer. Anything that is for this electrode stack that is not metal layer or capping layer is unclaimed and irrelevant.”);

- *Id.*, 77:12-78:2 (“And in reviewing this patent, we declared features that patent are the metal layers and the capping layer, via cut cross multiple layer. So it’s a filled hole. And it’s metal. But again, this is not part of the electrode stack that – it’s in the, in the, in the patent 562, or not in the -- does not include in the claim feature.”);
- *Id.*, 78:3-18 (“And I told you why our analysis will be some metal layers, and the capping layer, because they are claimed features. Because this is -- in the 562, this is in Usui, this in Yu and so forth. And via -- I also answered your question, via is a metal. But again, it’s not part of the claim feature, right? So we are not focusing on discussion on via.”);
- *Id.*, 93:16-94:19 (“...the electrode stack refers to the metal layers”).

79. Thus, Petitioner and Dr. Zhao appear to have interpreted the term “*electrode* stack” to be satisfied by *any* stack of metal layers that otherwise meets the claims’ limitations regarding the specific metal layers, regardless of whether or not those stack of metal layers are part of an *electrode* in the first place. I disagree with this interpretation, because it ignores the claim’s words. The word “*electrode*” is not “irrelevant” to the claims. The claims do not *only* recite a “stack” of metal layers. The claims recite an “*electrode* stack.” While the claims then set forth requirements regarding specific “layers” that the claimed “*electrode*

stack” “includes,” a POSA would not have understood the “includes” language to suggest that “electrode” should be given no weight.

80. My analysis regarding the term “electrode stack” below accounts for the teachings of the ’562 Patent, including its claims, drawings, written description, and prosecution history (EX-1034), *i.e.*, the *intrinsic* evidence. While my construction of the term “electrode stack” derives from the intrinsic evidence, it is also consistent with *extrinsic* evidence, as I explain in fuller detail below.

A. Intrinsic Evidence

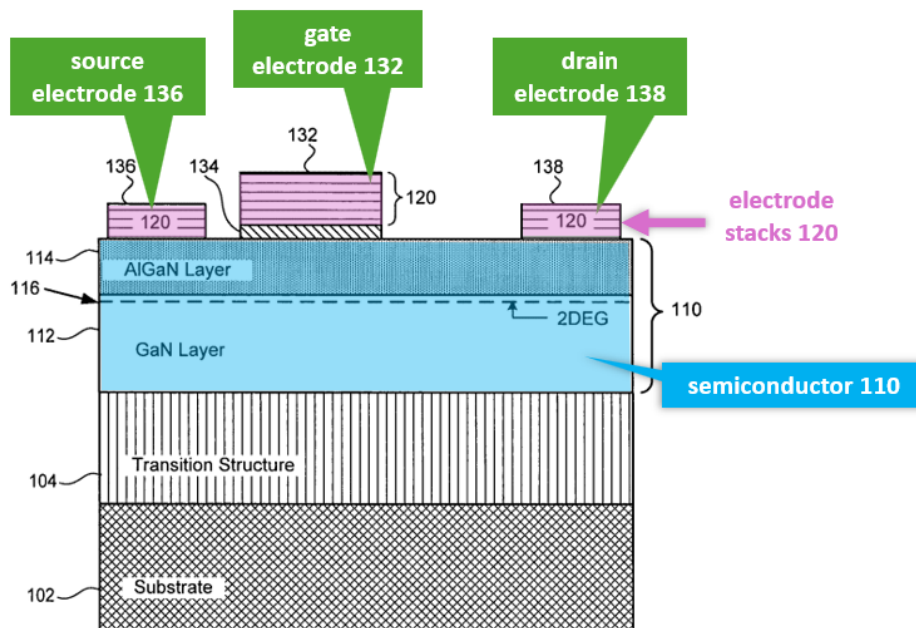
81. Beginning with the term itself, “electrode stack” has two important aspects: as an *electrode* and as a *stack* of materials. As to the “electrode” aspect, the surrounding claim language and the specification provides context. For example, independent claims 1 and 13 each recite, “[a]n electrical contact for use on a... semiconductor device, said electrical contact comprising an electrode stack.” EX-1001, 5:54–63. Hence, the electrode stack is at least a part of an *electrode* in the electrical contact for use on a semiconductor device.

82. Like the claims themselves, the ’562 Patent specification links the terms “electrical contact” and “electrode” by describing the electrical contact for use on a semiconductor device *as an electrode* of the device. EX-1001, 2:19-24 (“The present invention is directed to a refractory metal nitride capped *electrical contact* and a method for its fabrication. *More specifically*, the present invention

discloses *such a contact for implementation as an electrode on a semiconductor device*, such as a group III-V power semiconductor device, for example.”); *see also, e.g., id.*, 6:25-27 (further claiming that the “electrical contact is implemented as a power electrode”), 6:28-29 (further claiming that the “electrical contact is implemented as a gate electrode”). This is consistent with the specification’s implementation of an electrical contact as one of three electrode types: a source electrode and drain electrode (*i.e.*, power electrodes) and a gate electrode. EX-1001, 2:58-60 (“Structure 100 also includes a plurality of electrical contacts including source *electrode* 136, drain *electrode* 138, and insulated gate *electrode* 132), 3:23-25 (“As shown in FIG. 1, *each* of source *electrode* 136, drain *electrode* 138, and insulated gate *electrode* 132 comprises electrode stack 120.”), 3:40-42 (“Electrical contact 230 may be seen to correspond to any of source electrode 136, drain electrode 138, or insulated gate electrode 132, in FIG. 1.”). Thus, when the claims recite an “electrode stack,” it is in the context of the electrical contact implemented as an electrode of the semiconductor device.

83. The ’562 Patent specification describes source, drain, and gate electrodes for a transistor. EX-1001, Fig. 1 (below), 2:58-60 (“Structure 100 also includes a plurality of electrical contacts including source electrode 136, drain electrode 138, and insulated gate electrode 132.”), 3:19-35. Fig. 1 illustrates a

compound semiconductor formed from gallium nitride (GaN) layer 112 and aluminum gallium nitride (AlGaN) layer 114. EX-1001, 1:7-15, 2:53-65.



'562 Patent, Fig. 1 (annotated).

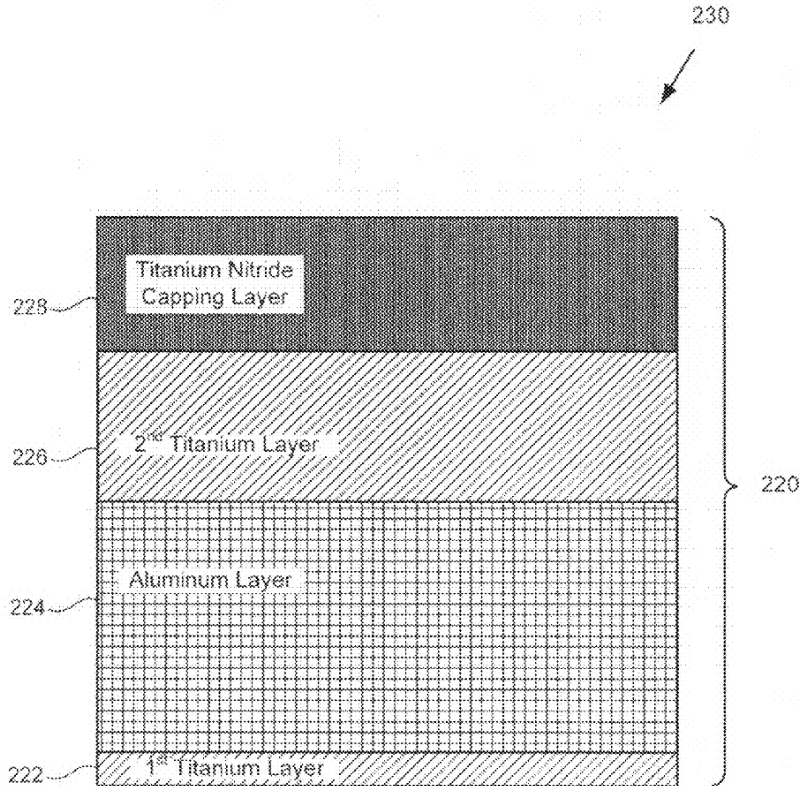
84. Above, “[s]ource electrode 136 and drain electrode 138” are each formed by an “electrode stack 120” and are described as “power electrodes” that are “*ohmically coupled*” to the semiconductor 110. EX-1001, 3:19-28, 1:33-43, Fig. 1. I agree with Dr. Zhao that an ohmic contact is a low-resistance metal-semiconductor junction having (ideally) linear, non-rectifying I-V (current-voltage) characteristics and providing conduction in both directions between the metal and the semiconductor. EX-1002 (Zhao Dec.), ¶56 (citing, EX-1011 (Mishra), 229).

85. Gate electrode 132 is “an insulated gate electrode” that is also formed by an electrode stack 120 but separated from the semiconductor by a thin

insulating oxide layer 134. *Id.*, 3:21-33. Although electrode stack 120 does not directly contact the semiconductor, the thin insulating oxide layer 134 that is part of gate electrode 132 does contact the semiconductor and, as a POSA would have appreciated, in gate electrode 132, electrode stack 120 must be in very close proximity to the semiconductor to allow for field-effect control of current flow in the 2DEG conduction layer.

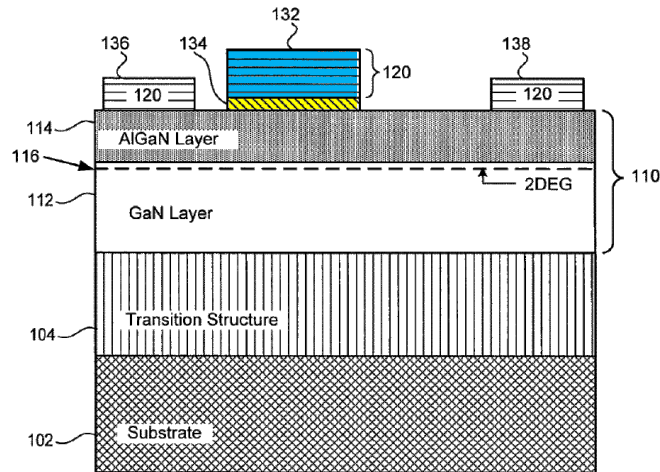
86. “In other embodiments... gate electrode 132 comprising electrode stack 120 may make Schottky contact with GaN body 110” with no insulating layer in between. EX-1001, 3:31-35. A “Schottky” barrier forms at the metal-semiconductor junction. *See, e.g.*, EX-1011 (Mishra), 219; EX-1002 (Zhao Dec.), ¶58.

87. The ’562 Patent specification discloses an embodiment of the inventive electrical contact comprising an electrode stack in Fig. 2 (reproduced below), which “may... correspond to *any* of source electrode 136, drain electrode 138, or insulated gate electrode 132, in FIG. 1.” EX-1001, 3:36-45.



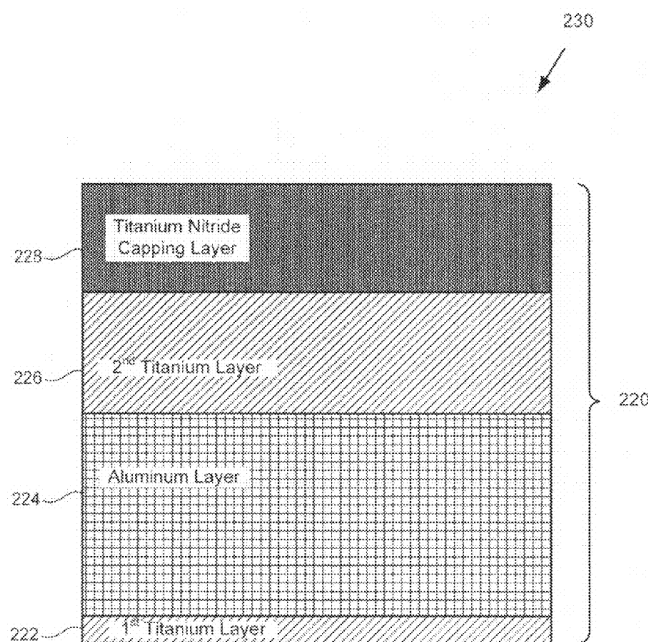
'562 Patent, Fig. 2.

88. In Fig. 1 (annotated below), insulated gate electrode 132 (highlighted blue below) is stacked over “gate insulating layer 134” (highlighted yellow below). EX-1001, 3:28-35. Gate electrode 132 is formed by the “electrode stack 120” and does not include gate insulating layer 134 which “underl[ies]” “electrode stack 120.” *Id.*, 3:28-31, Fig. 1 (the label for “electrode stack 120” does not include insulating layer 134). Indeed, the same “electrode stack 120” forms each of the source and drain electrodes 136 and 138 that have no insulating layer 134. *Id.*, 3:23-28, Fig. 1.



'562 Patent, Fig. 1 (annotated).

89. Fig. 2 is a more detailed illustration of an “[e]lectrode stack 220” that “corresponds to electrode stack 120 in FIG. 1.” EX-1001, 3:42-43. As seen from Fig. 2 (below), electrode stack 220 does not include an insulating layer. Fig. 2’s “[e]lectrical contact 230 may... correspond to any of source electrode 136, drain electrode 138, or insulated gate electrode 132 in FIG. 1.” *Id.*, 3:40-42.



'562 Patent, Fig. 2.

90. Thus, the '562 Patent specification uses “electrode stack” to refer to a stack of layers forming an electrode and describes three electrode types: (1) a “power electrode[]” that touches and is “*ohmically coupled* to” the nonmetallic semiconductor² (EX-1001, 3:19-28, 1:33-43); (2) a transistor gate electrode that controls the flow of electrons or holes through the transistor that touches and makes “Schottky contact” with the nonmetallic semiconductor (*id.*, 3:31-35); and (3) a transistor gate electrode that controls the flow of electrons or holes through the transistor but is “an insulated gate electrode” that is separated from the semiconductor by an insulating layer 134 (*id.*, 3:21-33). *See also id.*, claims 10-12 (reciting each electrode type). EX-1015, 503-505 (corroborating the functions of transistor source, drain, and gate electrodes).

91. The proper construction of the term “electrode stack” in view of the '562 Patent specification is a stack of conductive layers that forms an electrical contact that is part of a semiconductor device and used to (1) establish electrical contact with a nonmetallic part of the semiconductor device (like the source, drain, and Schottky gate electrodes in the '562 Patent) or (2) controls the operation of the semiconductor device (like the insulated or Schottky gate electrodes in the '562 Patent).

² This electrode type forms a transistor's source and drain electrodes.

B. Extrinsic Evidence

92. While I believe the specification is sufficient for a POSA to understand the plain meaning of the term “electrode stack,” my proposed construction is also consistent with dictionary definitions for electrode. For example, Merriam-Webster’s Collegiate Dictionary defines “electrode” as “1: a conductor used to establish electrical contact with a nonmetallic part of a circuit” and “2: an element in a semiconductor device (as a transistor) that emits or collects electrons or holes or controls their movements.” EX-2001, 371.

93. The first definition describes the ’562 Patent’s source and drain electrodes of the ’562 Patent that are “ohmically coupled” to the semiconductor, and the gate electrode embodiment that “make[s] Schottky contact with” the semiconductor, because a POSA understood that each of those electrodes is a conductor used to establish electrical contact with a nonmetallic part of a circuit in the ’562 Patent – namely, the semiconductor. EX-1001, 1:33-43, 3:19-21, 3:31-35.

94. The second definition also describes the electrodes in the ’562 Patent because each of the electrode types described in the ’562 Patent is “an element in a semiconductor... transistor,” and the source and drain electrodes “emit[.]” or “collect[.]” electrons or holes while the gate electrode “control[s] the movement of electrons or holes” between the transistor’s source and drain regions.

95. Thus, extrinsic evidence (*e.g.*, EX-2001) confirms my proposed construction of the term “electrode stack” based on the intrinsic evidence.

VIII. DISCUSSION OF THE PETITION’S REFERENCES

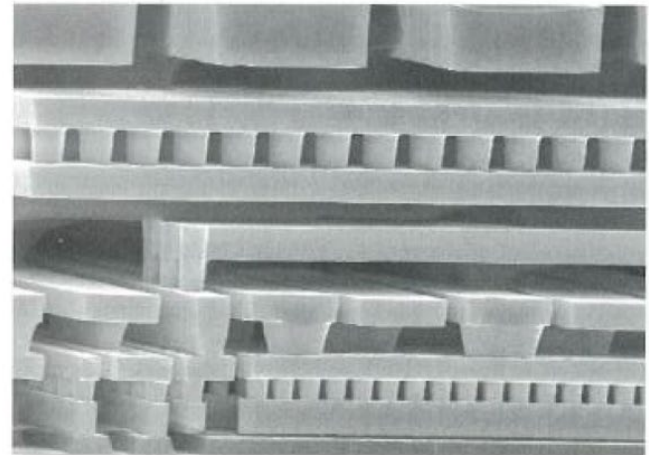
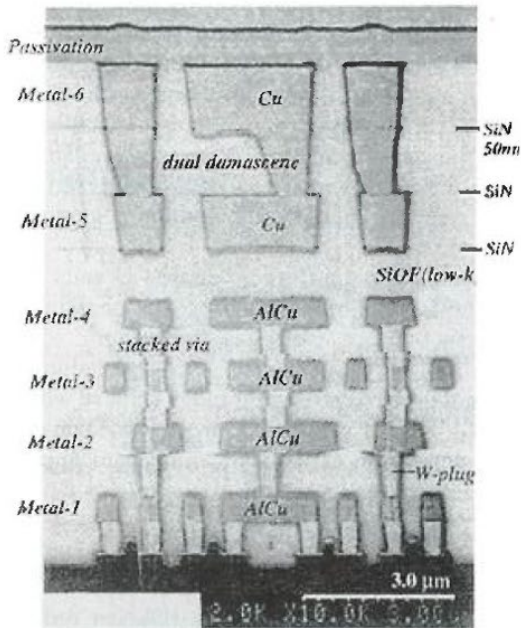
A. Usui (U.S. Patent No. 5,943,601) (EX-1004)

96. I have reviewed Usui and Dr. Zhao’s description of Usui’s teachings. I find Dr. Zhao’s description incomplete, because it omits important details regarding Usui’s disclosure and mistakes several of its teachings. Below I have elaborated with additional relevant details regarding Usui’s disclosures and have responded to certain of Dr. Zhao’s characterizations.

97. As discussed above in Section VI.C (Interconnections), thin metal lines or strips commonly interconnected various circuits and components within a semiconductor chip. These metal interconnections form the various wires between and among the integrated circuit. A single semiconductor chip could include hundreds of thousands of devices with interconnections between all of them. Aluminum and aluminum alloys were commonly used for forming various electrical connections or wiring in electronic devices, such as in integrated circuit structures. EX-1004 (Usui), 1:17–21.

98. To increase the numbers of integrated circuits for a given surface area of the semiconductor wafer, interconnects were devised with multilevel metal systems. EX-2030 (Jaeger), 166. For example, the first structure (a) below uses

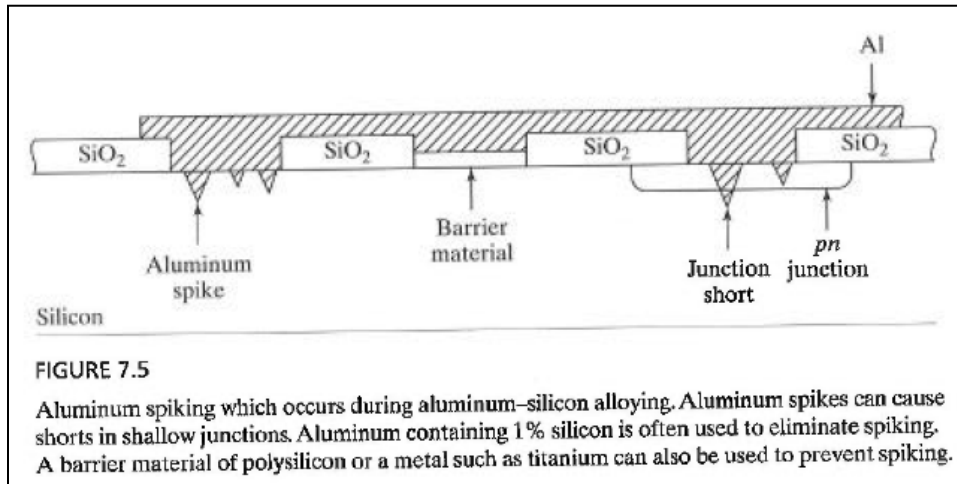
four layers of aluminum-copper interconnections with tungsten via plugs plus two levels of Damascene copper interconnections. EX-2030 (Jaeger), 171. The second structure (b) shows the use of six levels of copper wiring after interlayer dielectrics are removed.



EX-2030 (Jaeger), 171.

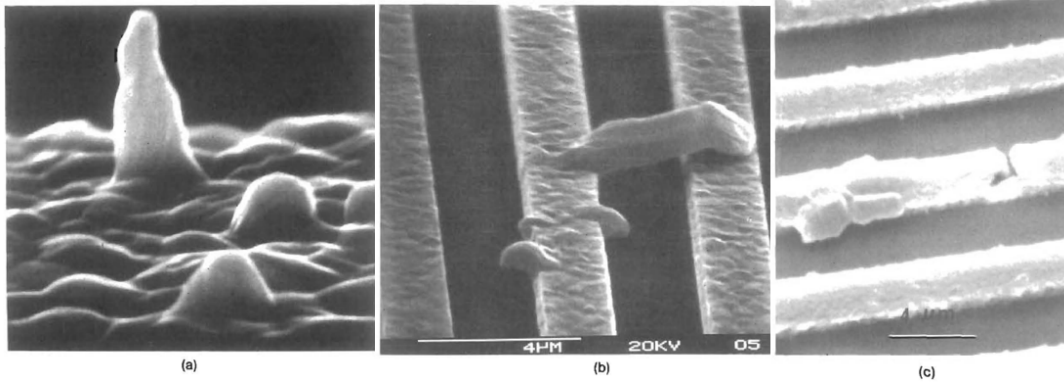
99. In the case of aluminum and aluminum alloy interconnections, a known problem was the electromigration of aluminum atoms into the underlying silicon (or spiking) if the aluminum were to come into direct contact with the silicon, which could interfere with the performance and reliability of the resulting integrated circuit structure. EX-1004 (Usui), 1:17–34, 2:9-16. The contact between aluminum and silicon would result in “spiking,” which would increase the surface area of the junction between silicon and the aluminum but could also cause

shorts in the shallow junctions. EX-2030 (Jaeger), 155–156; EX-2031 (Ohring), 387–389. Spiking is illustrated below.



EX-2030 (Jaeger), 156. To address the problem of spiking, a physical barrier material could be placed between the aluminum and the silicon semiconductor substrate. EX-1004 (Usui), 1:24–29, 2:9-16.

100. In addition to spiking, the problem of hillock growth could also occur between the very closely spaced metal interconnection lines, particularly at the submicron level. EX-1004 (Usui), 1:35–37. Electromigration is the movement of atoms in a metal film due to momentum transfer from the electrons carrying the current. EX-2030 (Jaeger), 157. Metal interconnections in integrated circuits were operated at relatively high current densities. EX-2030 (Jaeger), 157. Under high-current-density conditions, metal-atom migration could cause voids (open circuit) in some regions and metal pileup, or hillocks, in other regions, which could cause short circuits. EX-2030 (Jaeger), 157; EX-2031 (Ohring), 380–381.



EX-2031 (Ohring), 380–381 (electromigration damage in Al films: (a) hillock growth; (b) whisker bridging two conductors; (c) nearby mass accumulation and depletion).

101. As the demand increased for scaling down the dimensions of the interconnection lines and for increasing the current density, minimizing electromigration and hillock growth became important. EX-1004 (Usui), 1:37–41. Accordingly, Usui’s methods were intended to address this problem by providing an interconnect structure that having an aluminum and/or aluminum alloy layer exhibits enhanced electromigration performance along with being hillock free. EX-1004 (Usui), 1:5–9, 2:33–39.

102. I therefore do not agree with Dr. Zhao’s characterization of the field of the invention or the problem to be solved by the Usui patent. According to Dr. Zhao, a POSA allegedly would have considered Usui analogous art to the ’562 Patent,

because it is in the same field of endeavor, forming electrical contacts for semiconductor devices (Usui, Abstract; ’562, Abstract), and

addresses the same problem of providing enhanced or simplified semiconductor fabrication as the '562 Patent (Usui, 4:1-3; '562 Patent, 1:25-29, 1:56-62).

EX-1002 (Zhao Dec.), ¶87. I disagree. Usui does not address forming electrical contacts at all other than a contact metal 10,³ formed on the semiconductor wafer 6 prior to depositing the interconnect layers 13, 14, 15, 18, 19. EX-1004 (Usui), 5:10-65, Figs. 2-5. Usui instead describes problems and proposes a solution related to interconnections. Unlike electrical contacts of the '562 Patent which form a metal-semiconductor junction, interconnections function as metal-metal electrical connections much like conventional wires of a circuit. As Dr. Zhao seems to recognize, the distinct functions, distinct physics and chemistry at play, and unique problems/techniques differentiate these types of components. *See* EX-1002 (Zhao Dec.), ¶¶48–73.⁴ For example, Dr. Zhao states:

- “Ohmic contacts are formed from metal-semiconductor junctions or contacts that have a linear, non-rectifying I-V (current-voltage) characteristic.” EX-1002 (Zhao Dec.), ¶56;

³ Ex-1004 (Usui) refers to element 10 interchangeably as a “contact stud” (5:12) “contact metal” (5:18), “interplanar stud connection” (3:26), and “device contact metallization” (5:14–15, 5:25).

⁴ Dr. Zhao’s characterizations of the field of the '562 Patent are not consistent, describing it variously as “semiconductor devices featuring an electrode stack featuring a plurality of metal layers” (¶153), “forming electrical contacts for semiconductor devices” (¶¶87, 129).

- “[T]he formation of ohmic contacts at a semiconductor surface requires a high density of states near the interface to push the Fermi-level in the semiconductor close to the conduction band.” EX-1002 (Zhao Dec.), ¶57;
- “Schottky contacts are formed from metal-semiconductor junctions or contacts that have non-linear diode characteristics similar to those of the p-n diode...” EX-1002 (Zhao Dec.), ¶58;
- “Schottky contacts allow little or no current to flow through the contact until a critical voltage is reached...” EX-1002 (Zhao Dec.), ¶59;
- “Schottky contacts were known to have rectifying properties...” EX-1002 (Zhao Dec.), ¶59;
- “Schottky contacts should have a high breakdown voltage and a low reverse current.” EX-1002 (Zhao Dec.), ¶59;
- “Metals were known to be used as interconnects (i.e., low resistance conductors), to form Schottky barriers, to form ohmic contacts, and to form gates in transistors.” EX-1002 (Zhao Dec.), ¶63;

- “In semiconductor circuits, interconnects provide pathways through which charge travels from one point to another.” EX-1002 (Zhao Dec.), ¶64;
- “[I]nterconnects play an extremely important role in circuit performance.” EX-1002 (Zhao Dec.), ¶64;
- “The metal strips making up the interconnect must be able to carry adequate current and make adequate contact with the devices.” EX-1002 (Zhao Dec.), ¶64;

And although Usui mentions the spiking of the aluminum (where atoms of aluminum spikes form into the silicon substrate), Usui’s approach avoids this issue altogether by using a contact metal 10 (presumably of a barrier metal material) instead of aluminum metallization at the metal-semiconductor junction, as was known in the art. EX-1004 (Usui), 1:24–29, 2:9-16.

103. While Usui describes a “criticality of employing an underlayer of the group IVA metal having a thickness of 90 angstroms to 110 angstroms,” Usui clearly explains that this thickness of the underlayer is chosen because it uniquely produces “optimum Al<111> texture [] which has the lowest volume fraction of random components” and as such “electromigration data is also improved.” EX-1004 (Usui), 4:22-67, Abstract ([a]s a result of this invention, [] aluminum line electromigration characteristics are improved.”). Usui does not describe any

benefit or consideration outside of the context of improving electromigration in Al interconnects by optimizing Al texture.

104. Usui certainly does not address the same problems solved by the '562 Patent. For example, Usui does not discuss the problems associated with using gold in an electrical contact/electrode stack⁵; Usui does not mention gold whatsoever. Nor would a POSA understand the problems/solutions regarding electromigration in aluminum interconnectors to be reasonably pertinent to the problems addressed by the '562 Patent because as discussed in more detail above electromigration is a particular issue with metal interconnects relating to the combined currents from many devices, and not for electrical contacts for use on a semiconductor device.

105. Where relevant, I have discussed additional details regarding Usui's disclosures in my analysis below.

B. Yu (U.S. Patent App. Pub. No. 2010/0052066) (EX-1005)

106. I have reviewed Yu and Dr. Zhao's description of Yu's teachings. I find Dr. Zhao's description incomplete because it omits important details regarding Yu's disclosure and mistakes several of its teachings. Below I have elaborated

⁵ Gold was in common use as a capping layer of ohmic contacts—not interconnects. *See, e.g.*, EX-1013 (Quay), 147-49 (Page 174-76 of 492) (ohmic contacts with top Au (gold) layer); EX-1016 (Voss), 46 (describing convention ohmic contacts with Au top layer and that "Au is necessary to decrease the sheet resistance").

with additional relevant details regarding Yu's disclosures and have responded to certain of Dr. Zhao's characterizations.

107. Dr. Zhao does not provide much of a discussion of Yu so much as make repeatedly unsupported and erroneous assertions about the state of the art and the knowledge of a POSA. Yu is directed to a particular technique for forming a metal gate electrode for a complementary metal-oxide-semiconductor (CMOS) device. EX-1005 (Yu), [0004]. Yu explains that:

CMOS devices have typically been formed with a gate oxide and polysilicon gate electrode. There has been a desire to replace the gate oxide and *polysilicon gate electrode* with a high-k gate dielectric and *metal gate electrode* to improve device performance as feature sizes continue to decrease. Current processing utilizes metal, metal carbide, and/or metal nitride for the gate electrode. However, such materials provide insufficient work function values and present thermal stability issues, particularly when utilized in an n-type MOS device (NMOS) and a p-type MOS device (PMOS), which require different work functions for their respective gate electrode.

EX-1005 (Yu), [0004] (emphasis added). In particular, Yu notes that "metal, metal carbide, and/or metal nitride" used in metal gate structures "provide insufficient work function values and insufficient thermal stability." *Id.*, [0004], [0032].

108. Yu addresses the above-discussed problem by providing a CMOS device whose two transistors have metal gate electrodes formed from different metal layers made of "doped-conducting metal oxide (DCO)" in order to "provide desired work function values and thermal stability." EX-1005 (Yu), [0019], [0033]. A first gate electrode includes a "first metal layer 220 compris[ing] a

material with a first work function” and the second gate electrode includes a “second metal layer 222 compris[ing] a material with a second work function.” EX-1005 (Yu), [0029]; *see also id.*, Fig. 2E and [0033] (“metal layers 220, 222 [are provided with] correct work function values”). Yu’s goal of providing “different work functions for their respective gate electrode” is achieved by providing different work functions for the metal layers 220 and 222. EX-1005 (Yu), [0004], [0029], [0033].

109. Yu discloses a CMOS device with two metal gate stacks 230 and 231 as shown in Yu’s Fig. 2E annotated below. Yu refers to the entire stack 230 and 231 as a “metal gate stack.” EX-1005 (Yu), [0038]-[0040]. Metal gate stacks 230 and 231 have the different metal layers (220 and 222, respectively) with the different work functions as discussed above, but their structures are otherwise the same. Each metal gate stack includes two insulative dielectric layers 214, 216 (yellow) that sit atop the semiconductor (EX-1005 (Yu), [0028]-[0030]), a “diffusion barrier/protection layer” 218 that separates the metal layer (220 or 222, blue above) from the dielectric layers to prevent material from diffusing between the metal and dielectric layers (EX-1005 (Yu), [0029]), a capping layer 226 (EX-1005 (Yu), [0036]), and a diffusion barrier layer 224 that separates the capping layer from the metal layer (220 and 222) (EX-1005 (Yu), [0035]).

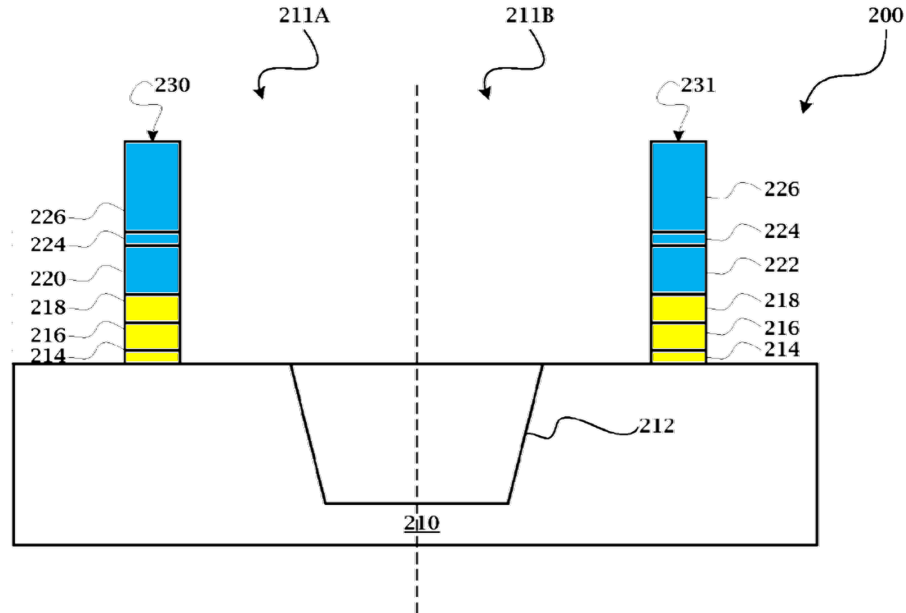


FIG. 2E

EX-1005 (Yu), FIG. 2E, annotation added.

110. Yu repeatedly uses a long list of potential materials to describe each component in Yu's semiconductor device. For example, as to the semiconductor substrate 210, Yu discloses an enormous number of possible materials including just about any common semiconductor material "and/or combinations thereof":

The semiconductor substrate 210 may comprise an elementary semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and GaInAsP; any other suitable material; and/or combinations thereof. In one embodiment, the alloy semiconductor substrate may have a gradient SiGe feature in which the Si and Ge composition change from one ratio at one location to another ratio at another location of the gradient SiGe feature. In

another embodiment, the alloy SiGe is formed over a silicon substrate. In another embodiment, a SiGe substrate is strained. Furthermore, the semiconductor substrate may be a semiconductor on insulator, such as a silicon on insulator (SOI), or a thin film transistor (TFT). In some examples, the semiconductor substrate may include a doped epi layer or a buried layer. In other examples, the compound semiconductor substrate may have a multilayer structure, or the silicon substrate may include a multilayer compound semiconductor structure. In the present embodiment, the semiconductor substrate 210 comprises silicon, germanium, a group III-V material, or a group II-VI material.

EX-1005 (Yu), [0023].

111. With respect to the “diffusion barrier/protection layer” 218, Yu again describes this layer as “may comprise” a list of different materials and “combinations thereof,” including metal, metal nitride, and even oxide (“may be formed by ... thermal oxide”):

The diffusion barrier/protection layer 218 may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present embodiment, the diffusion barrier/protection layer 218 comprises TiN, which is deposited by PVD to a thickness of approximately 20 Å. In alternate embodiments, the diffusion barrier/protection layer may be formed by any suitable process, such as CVD, PVD, ALD, thermal oxide, plating, and/or combinations thereof. Further, in alternate embodiments, the diffusion barrier layer 218 comprises any suitable thickness. It is understood that the diffusion barrier layer 218 may be omitted in alternate embodiments.

EX-1005 (Yu), [0029]. Yu discloses in one embodiment diffusion barrier/protection layer 218 “may comprise TiN” “deposited by PVD to a thickness of approximately 20 Å.” *Id.* Contrary to Dr. Zhao’s suggestion in ¶¶152 and 155 (contending this thickness is preferred along with a thicker capping layer), I do not find that Yu

describes this 20 Å thickness as a preferred embodiment. Nor is there guidance from Yu that this 20 Å thickness would apply to any of the other material choices that can be used to form Yu's layer 218. A POSA would know that the capability for a layer to sufficiently block diffusion across a layer depends on the material characteristics (e.g., diffusivity of the diffusing species) as well as geometry (e.g., layer thickness). There is no guidance to a POSA that if Yu's approximately 20 Å TiN is modified to be titanium or other materials, what would be a suitable thickness for the diffusion barrier layer to function for the purpose of Yu's device.

112. With respect to the "capping layer" 226, Yu again describes this layer as may comprise a long list of materials "and combinations thereof":

The capping layer 226 may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer 226 comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer 226 may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer 226 may comprise any suitable thickness. The capping layer 226 may be formed by CVD, PVD, ALD, thermal oxide, plating, other suitable processes, and/or combinations thereof. In some embodiments, the capping layer 226 comprises aluminum and/or tungsten. For example, in some embodiments, the capping layer 226 comprises aluminum formed by CVD. It is understood that, in alternate embodiments, the capping layer 226 may comprise multilayer structures.

EX-1005 (Yu), [0036]. In two specific embodiments, Yu discloses different thickness values for the capping layer given different material choices and manufacturing processes (e.g., “between about 200 Å and about 1,000 Å, preferably about 600 Å” when polysilicon is used, “between about 50 Å and about 1,000 Å, preferably about 200 Å” when “metal (e.g., an aluminum-based, tungsten, or copper material)” are used in “a gate last process.”). EX-1005 (Yu), [0036]. Neither of these embodiments for the capping layer uses a refractory metal nitride nor suggests any guidance for what would be the thickness if refractory metal nitride is used in Yu’s capping layer, which Dr. Zhao also appears to acknowledge. EX-1002 (Zhao Dec.), ¶¶152, 155 (“disclosure of [capping layer 226 being preferably 600 Å] is made with respect to the capping layer being polysilicon.”). On the other hand, Yu explicitly teaches a POSA that when TiN is used as a “protection layer,” the TiN is to be deposited to a thickness of approximately 20 Å. EX-1005 (Yu), [0036].

113. Yu recognizes that an electrode design such as gate electrode design cannot be simply substituted when the underlying semiconductor is different and instead must have compositions and electrical properties tailored to different semiconductor materials, as Yu emphasizes that p-type and n-type MOS devices “require different work functions for their respective gate electrode.” EX-1005 (Yu), [0004], [0033], [0037].

114. Where relevant, I have discussed additional details regarding Yu's disclosures in my analysis below.

C. Adesida (U.S. Patent App. Pub. No. 2008/0023726) (EX-1006)

115. I have reviewed Adesida and Dr. Zhao's description of Adesida's teachings. I find Dr. Zhao's description incomplete because it omits important details regarding Adesida's disclosure. Below I have elaborated with additional relevant details regarding Adesida's disclosures and have responded to certain of Dr. Zhao's characterizations.

116. Adesida concerns gate metallization of an InAlAs/InGaAs/InP high electron mobility transistor (HEMT) "for high speed digital circuits." EX-1006 (Adesida), [0004]-[0005]. In particular, Adesida explains that realization of a high performance enhancement-model HEMT (referred to as E-HEMT by Adesida) "relies chiefly on a high Schottky barrier height (ϕ_B) of the gate metals to deplete the channel and to obtain positive threshold voltage (V_{th}), as well as to reduce the gate leakage current." *Id.*, [0005].

117. Adesida explains that among several candidates for "metals on InAlAs," "Pt has the highest ϕ_B of over 800 meV after annealing and is frequently used as buried gate." *Id.*, ¶¶0005-0012. However, Pt presents "serious drawbacks to its use for Schottky contacts" because of its "low optimum annealing temperature, fast diffusivity, and thus low thermal stability." *Id.*, ¶0013. For

example, diffusion of Pt “during prolonged thermal treatment at a low temperature” causes formation of “a metastable amorphous interlayer” that “consumed up to 70% of the InAlAs barrier layer,” causing “substantial shortening in the gate-to-channel distance bring[ing] considerable changes to the operational parameters of the devices.” *Id.*, ¶0013.

118. Adesida describes extensive experimentation of an “Iridium contact” with the goal to provide “improved Schottky barrier contacts” and to “overcome problems and limitations of prior art approaches” using Pt. *Id.*, Abstract, ¶¶0014-0015. These experiments include fabricating Ir and Pt contacts on a lightly doped InAlAs layer as test structures (EX-1006 (Adesida), FIG. 1) and using current-voltage (I-V) measurements to obtain the Schottky barrier heights ϕ_B of as-deposited and annealed Ir contacts, which are repeated multiple times to obtain ϕ_B for Ir and Pt samples annealed at different temperatures. *Id.*, [0027]-[0029], FIG. 4. Adesida found that “Ir is more stable than Pt at higher temperatures,” and forms a maximum ϕ_B of 818 meV, comparable to the 800 meV from annealed Pt contact on InAlAs. *Id.*, [0029]-[0030]. From these experimentations, Adesida concludes that “Ir will form a thermally stable gate metal in InAlAs/InGaAs HEMTs.” *Id.*, ¶0030. Adesida attributes the observed results to the “interfacial reactions between the metals and InAlAs,” which were found to form “PtAs₂ and IrAs₂” as the

interfacial material that “may have higher work functions than the pure metals hence, the increase in Schottky barrier heights.” *Id.*, ¶0029.

119. FIG. 5 of Adesida shows a HEMT device that “practice[es] a form of the invention,” namely using the Ir gate contact. EX-1006 (Adesida), [0031]. In FIG. 5, gate 190 “is shown as a T-gate.” *Id.* By August 2009 it was known to a POSA that a T-gate structure is a requirement in a high speed HEMT such as the high speed InAlAs/InGaAs/InP HEMT disclosed by Adesida and is in fact “characteristic of all modern high speed FETs.” EX-1011 (Mishra) at 378. The use of a T-gate structure enables a very small intrinsic gate length while still maintaining a bulkier gate metal, which reduces the lateral gate resistance. *Id.* These characteristics are particularly important in a high-speed transistor design such as the embodiments disclosed in Adesida which concern frequencies up to 220 GHz. EX-1006 (Adesida), [0034].

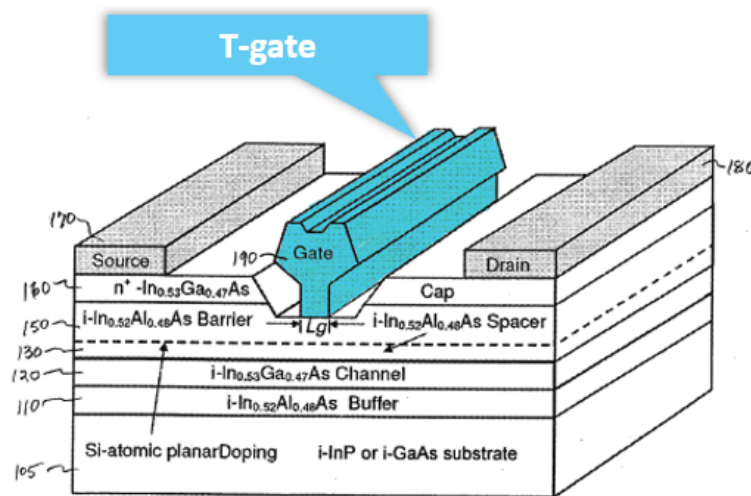
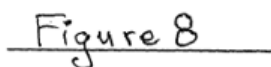


Figure 5

120. Adesida further describes an embodiment with “integration of enhancement- and depletion-mode (E/D) HEMT devices.” EX-1006 (Adesida), [0032]. This embodiment is shown in FIG. 8, which shows that both the E-HEMT and D-HEMT use a “T-gate” 190 that is “formed in PMMA/PMMA-MAA/PMMA trilayer resist.” *Id.* Separate devices using a T-gate metallization of Ir/Ti/Pt/Au and Pt/Ti/Pt/Au, respectively, are fabricated and the respective transistor characteristics for “Ir/Ti/Pt/Au gate HEMTs” and “Pt/Ti/Pt/Au gate eHEMTs” are compared in FIGs. 6a, 6b. EX-1006 (Adesida), FIGs. 6a, 6b, 8, [0032]-[0033].



121. Adesida also describes that in FIG. 8, “[a]lloyed AuGe/Ni/Au ohmic contacts” were used, which refer to the source/drain contacts 170/180 to the n+

InGaAs layer 165. This is consistent with POSA's knowledge by August 2009 that in a GaAs substrate "[t]ypically, the ohmic contacts are Au-Ge based." EX-1021 (Kayali), 34.

122. Where relevant, I have discussed additional details regarding Adesida's disclosures in my analysis below.

D. Sugimoto (U.S. Patent No. 7,777,252) (EX-1007)

123. I have reviewed Sugimoto and Dr. Zhao's description of Sugimoto's teachings. I find Dr. Zhao's description incomplete for it omits important details regarding Sugimoto's disclosure. Below I have elaborated with additional relevant details regarding Sugimoto's disclosures and have responded to certain of Dr. Zhao's characterizations.

124. Sugimoto "relates to normally-off type semiconductor devices comprising m-V semiconductors." EX-1007 (Sugimoto), 1:9–10. Sugimoto discloses an invention "that aims to present semiconductor devices in which stable normally-off operation can be guaranteed, and in which the on-resistance can be decreased." EX-1007 (Sugimoto), 2:4–7. Sugimoto explains that there is a problem that electrons in the 2DEG (2-Dimensional Electron Gas) scattered by impurities within the p-GaN layer cause an increase in a magnitude of resistance (on-resistance) between the drain electrode and the source electrode while the predetermined gate voltage is applied to the gate electrode of a HEMT (High

Electron Mobility Transistor). EX-1007 (Sugimoto), 1:49–58. Sugimoto also explains that reducing the impurities would cause the HEMT to become unstable. EX-1007 (Sugimoto), 1:59–67.

125. Sugimoto describes a stack of semiconductor layers to form semiconductor devices, capable of high temperature and high frequency operation and having the characteristics of high breakdown voltage with high output and low on-resistance. EX-1007 (Sugimoto), 9:7–17.

126. Sugimoto discloses three embodiments of a semiconductor device with slight variations in the semiconductor layers. *See, e.g.*, EX-1007 (Sugimoto), FIG. 1 and 9:19–51 (describing a first embodiment with a top AlGa_N layer 34 on an SI (Semi-Insulated) Ga_N layer 62, which is on a p-Ga_N layer 32 on a buffer layer 24 formed from Ga_N); FIG. 3 and 11:44–12:12 (describing a second embodiment with a top n-AlGa_N layer 134 on a Ga_N layer 132, which is on a buffer layer 124 formed from Ga_N); FIG. 5 and 14:13–48 (describing a third embodiment with a p-AlGa_N layer 235 on an n-AlGa_N layer 233 and p-Ga_N layer 232, which is on a buffer layer 224).

127. In each of the three embodiments, Sugimoto discloses essentially the same set of source/drain electrodes and a gate electrode at a top surface of the top AlGa_N layer. For example, with regard to the first embodiment in FIG. 1, Sugimoto describes a “gate electrode 44 directly contacts with the top surface of

the AlGaIn layer 34 and forms a Schottky contact with the AlGaIn layer 34,” and “drain electrode 42 and the source electrode 46 make ohmic contact with the top surface of the AlGaIn layer 34.” EX-1007 (Sugimoto), 9:39–51. Sugimoto further describes the process to form the electrodes:

First, titanium (Ti) and aluminum (Al) are vapor deposited in sequence on the AlGaIn layer 34. The lithography method and the etching method are then used to perform patterning of the drain electrode 42 and the source electrode 46. After patterning has been performed, heat treatment is performed at 550° C. for 30 seconds using the RTA (Rapid Thermal Anneal) method. The contact resistance of the drain electrode 42 and the source electrode 46 with respect to the AlGaIn layer 34 is thus reduced, and ohmic contact is realized.

Next, the gate electrode 44 is formed using the lift-off method. That is, a resist film is formed on areas other than where the gate electrode 44 is desired, and then nickel (Ni) and gold (Au) are vapor deposited in sequence. The resist film is then lifted off, removing the nickel (Ni) and gold (Au) formed on the resist film. The gate electrode 44 is thus formed with the desired positional relationship.

Id., 11:11–28.

128. Thus, Sugimoto discloses ohmic contacts for source and drain electrodes formed by annealing titanium and aluminum layers and a Schottky contact for a gate electrode formed from a nickel and gold layered stack. A POSA would have appreciated from this disclosure the titanium and aluminum are likely to alloy together.

129. Where relevant, I have discussed additional details regarding Sugimoto’s disclosures in my analysis below.

IX. RESPONSE TO THE PETITION’S GROUNDS

130. I understand that Petitioner and Dr. Zhao alleges that claims 1-17 of the '562 patent are anticipated or would have been obvious to a POSITA based on the following grounds:

Grounds	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	Usui
2	3, 8, 12, 13 and 17	§ 103	Usui and Yu
3	9, 11, 14 and 16	§ 103	Usui, Yu, and Adesida
4	10 and 15	§ 103	Usui, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	Yu and Usui
6	9, 11, 14, and 16	§ 103	Yu, Usui, and Adesida
7	10 and 15	§ 103	Yu, Usui, and Sugimoto

Petition, 3; EX-1002 (Zhao Dec.), ¶83. I disagree for the reasons stated herein.

131. The references that Dr. Zhao relies upon lacks critical features recited by the challenged claims. Further, contrary to Dr. Zhao’s opinions, the claims of the '562 Patent reflect a novel and inventive combination of features that was not disclosed in any prior art reference and a POSA would not have had a rationale to combine together the teachings of Yu, Adesida, or Sugimoto identified by Dr.

Zhao to form the claimed electrical contact with the requisite reasonable expectation of success.

132. Based on my review of Dr. Zhao's opinions, the materials that Dr. Zhao identified in his analysis, my understanding of how a POSA would view the asserted prior art, and my knowledge and considerable experience in the industry, the challenged claims are not anticipated by any reference that Dr. Zhao asserts and are not obvious over any purported combination that Dr. Zhao relies upon. In many instances, I have provided evidence of the knowledge of a POSA and discussed why those teachings are relevant to my analysis. I conclude that, in light of the totality of the evidence, Usui does not anticipate any of the challenged claims and a POSA would not have been motivated to combine any references in the manner that Dr. Zhao did so and would not have had a reasonable expectation of success in doing so.

A. Ground 1 – Usui Does Not Anticipate Claims 1, 2, and 4-7

133. I disagree with Dr. Zhao's conclusion that Usui anticipates claims 1, 2, and 4-7 of the '562 Patent. For convenience, I adopt Petitioner's claim limitation labeling when discussing limitations herein. Claim 1 is directed to an electrical contact for use on a semiconductor device. Limitation [1pre]. The electrical contact comprises "an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers." Limitation

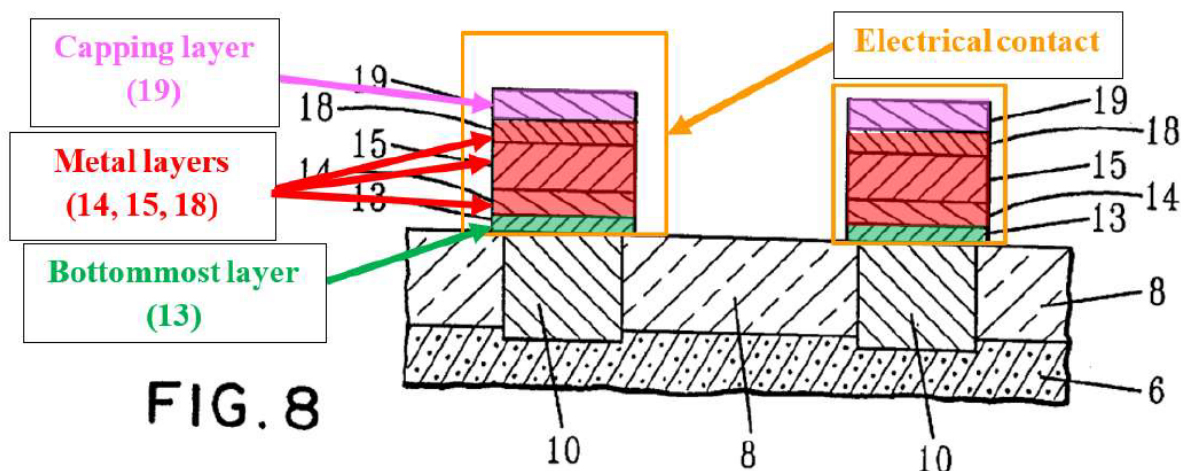
[1a]. The capping layer has “a thickness greater than that of a bottommost layer of said plurality of metal layers” of the electrode stack. Limitation [1c].

134. As discussed in Sections VI.C (Dr. Zhao Confuses Interconnects with Electrical Contacts) and VIII.A (Usui Summary), Usui’s interconnect is an *interconnection* (e.g., the wiring) *between* semiconductor devices – not an electrical contact comprising an electrode stack of the semiconductor device. Usui is directed to *interconnects* and addresses electromigration, a problem specifically associated with aluminum-based interconnects, and not associated with *electrical contacts having an electrode stack* as described and claimed by the ’562 Patent. An interconnect and an electrical contact having an electrode stack were understood to be fundamentally different structures facing different problems (including entirely different physics) and different approaches to addressing those problems. A POSA would have recognized the distinction.

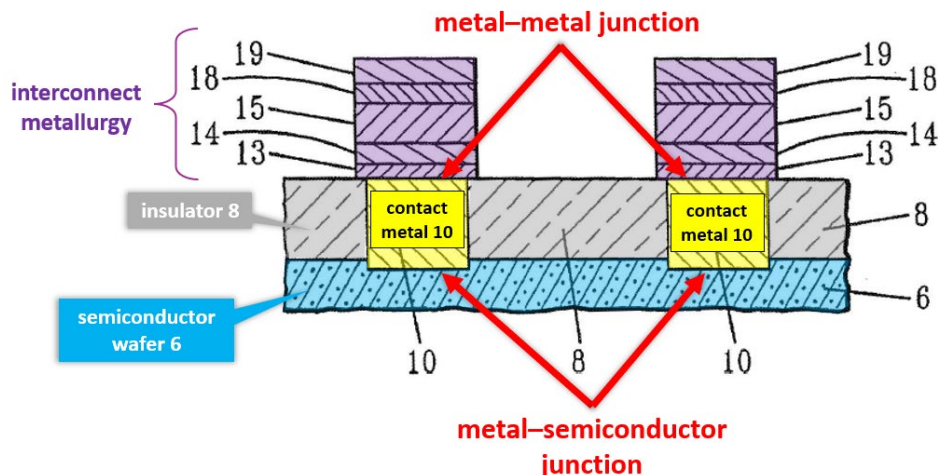
135. I discussed the ordinary meaning of “electrode stack” above in Section VII (including in ¶91) and explained (in ¶¶77-79) that Petitioner and Dr. Zhao gave no weight to the word “electrode” in that term. Petitioner and Dr. Zhao never construe “electrode stack” or ever explain what an “electrode” or “electrode stack” is. Petitioner and Dr. Zhao instead equate Usui’s interconnect metallurgy structure (layers 13-15 and 18-19) with an “electrode stack” without explanation,

even though Usui's interconnect metallurgy structure is not an "electrode stack" as used in the '562 Patent or even under a broad dictionary definition of an electrode.

136. As shown in Petitioner's annotations to Usui Fig. 8 below, Usui's interconnect metallurgy structure is deposited on an "interplanar stud connection 10" or "contact metal 10," which in turn "make[s] connection to a device substrate 6." EX-1004 (Usui), 3:24-27, 5:11-21.



Petition, 11 (Petitioner's Annotations to EX-1004 (Usui), Fig. 8). Usui's substrate 6 is a semiconductor. EX-1004 (Usui), 5:15 (referring to element 6 as "semiconductor wafer 6"). The Petitioner and Dr. Zhao never explain why, if there is an electrode in Usui FIG. 8 at all, the electrode is not the "device contact metallization 10" or "contact metal 10" that "make[s] connection to a device substrate 6," and forms a metal-semiconductor junction, as illustrated below.



EX-1004 (Usui), Figure 8 (annotated). By contrast, Usui’s interconnect metallurgy structure (layers 13-15 and 18-19) forms nothing more than a known metal-metal junction with contact metal 10. Petitioner and Dr. Zhao only identified a stack of metal layers, instead of an *electrode* stack.

1. Neither Petitioner Nor Dr. Zhao Explains the Plain Meaning of “Electrode Stack”

137. Neither the Petition nor Dr. Zhao explain what the plain meaning is for the term “electrode stack.” Petition, 7, 11; EX-1002 (Zhao Dec.), ¶¶79 (stating that he has “applied the ordinary and customary meaning that each claim term would have to a person of ordinary skill in the art in light of the ’562 patent’s specification and prosecution history” but not otherwise offering any constructions), 89 (stating that “Usui discloses an electrode stack,” without further explanation). For Ground 1, the Petition and Dr. Zhao simply *conclude* that Usui’s interconnect metallization structure (layers 13-15 and 18-19) constitutes the

claimed “electrode stack” without providing any explanation of how or why Usui’s interconnect metallurgy structure is allegedly an “electrode stack” and without providing any evidence in support. Petition, 11; EX-1002 (Zhao Dec.), ¶¶89-91 (contending that “Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers.”) (citing EX-1004 (Usui), Fig. 8).

138. This failure to provide any explanation of what an “electrode stack” is consistent with Petitioner’s (and Dr. Zhao’s) treatment of the preamble, which recites an “electrical contact.” Regarding the “electrical contact,” the *total* of Dr. Zhao’s analysis is an unsupported contention that Usui describes “a metallization structure, featuring group IVA metals for forming electrical connections” which can be equated with “contacts.” EX-1002 (Zhao Dec.), ¶88. To the extent Dr. Zhao is trying to argue that *any* metal structure for forming an electrical connection is an “electrical contact” in the context of the ’562 Patent, this is unsupported. Dr. Zhao cites only the abstract of *Usui*, which says nothing about electrodes or electrical contacts. Rather, Usui’s abstract explains that Usui’s “metallization structure... *exhibits enhanced electromigration* and is highly textured and is especially suitable *for forming electrical connections or wiring.*” EX-1004, abstract. This is consistent with Usui’s *interconnect*-related teachings more generally. *See, e.g.*, EX-1004 (Usui), 1:5-22 (“The structures fabricated by the

process of the present invention are especially useful for forming electrical connections or *wiring such as between active and/or passive devices* of an integrated circuit structure.”), 1:35-41 (“As the demand increases for scaling down the dimensions of the *interconnection lines* and for increasing the current density, overcoming, or at least minimizing, electromigration and hillock growth is essential.”), 1:48-60 (“In an effort to improve on the use of aluminum-copper as the *interconnection* metallurgy, aluminum-copper has been taught to be layered with a refractory metal such as in U.S. Pat. No. 4,017,890 (Howard). This patent suggests a method and resulting structure for *forming narrow intermetallic strips which carry high currents* on bodies such as semiconductors and integrated circuits,”), 1:61-2:32-38. But neither the reference to minimizing electromigration nor the structure of electrical wiring is suggestive of an electrical contact as described by the ’562 Patent. The electrical contacts of the ’562 Patent form a metal-semiconductor junction, either as source, drain or gate electrode. The interconnect metallurgy structure of Usui on which Petitioner relies does not form a metal-semiconductor junction. A POSA would not have mistaken such an interconnect structure for an electrode stack in an electrical contact, because they are different structures.

2. No Evidence Supports the Assertion that Usui's Interconnect Metallization Structure is an "Electrode Stack"

139. As noted above, Petitioner and Dr. Zhao say Usui's interconnect metallization structure (layers 13-15 and 18-19) is an "electrode stack" (Petition, 11) without providing an explanation of how or why Usui's interconnect metallurgy structure is allegedly an "electrode stack."

140. The evidence that the Petition cited in its mapping to Limitation [1A] for this proposition – "Usui, Fig. 8; Zhao, ¶89" – does not support Petitioner and Dr. Zhao's conclusion.

141. Usui's Fig. 8 *does not* label Usui's interconnect metallization structure (layers 13-15 and 18-19) an "electrode stack" or otherwise support Petitioner's assertion that Usui's layers 13-15 and 18-19 are an "electrode stack." As I have discussed, the interconnect metallization structure is instead an interconnect (e.g., wiring between semiconductor devices).

142. Paragraph 89 of EX-1002 (Zhao Dec.) repeats what the Petition says and does not add any analysis or evidence. As I discussed above in ¶¶76-79, Dr. Zhao never explains what the alleged plain meaning of "electrode stack" is and never explains how or why Usui's interconnect metallization structure (layers 13-15 and 18-19) is an electrode stack. By contrast, "all [of his] analysis," and "all [his] discussion" was "solely focus[ed] on" the "metal layers" and "capping layer"

that the claimed “electrode stack includes” – instead of what “electrode stack” means, or whether Usui discloses one in the first place. *E.g.*, Zhao-Dep., 172:20-175:5.

143. I note that the remainder of the Petition’s mapping to Limitation [1a] cites additional disclosures in Usui *only* for *other* reasons – for example, to allege that layers 13-15 and 18 are metal and that capping layer 19 is titanium nitride. Petition, 11 (citing Usui, Fig. 1, 3:38-41, 3:58-60, 4:4-5, 5:38, 5:52, 5:54-59). None of those disclosures cited by the Petition (or Dr. Zhao) characterize Usui’s interconnect metallization structure (layers 13-15 and 18-19) as an electrode stack.

3. Usui’s Interconnect Metallization Structure is Not an Electrode Stack Under the Proper Construction

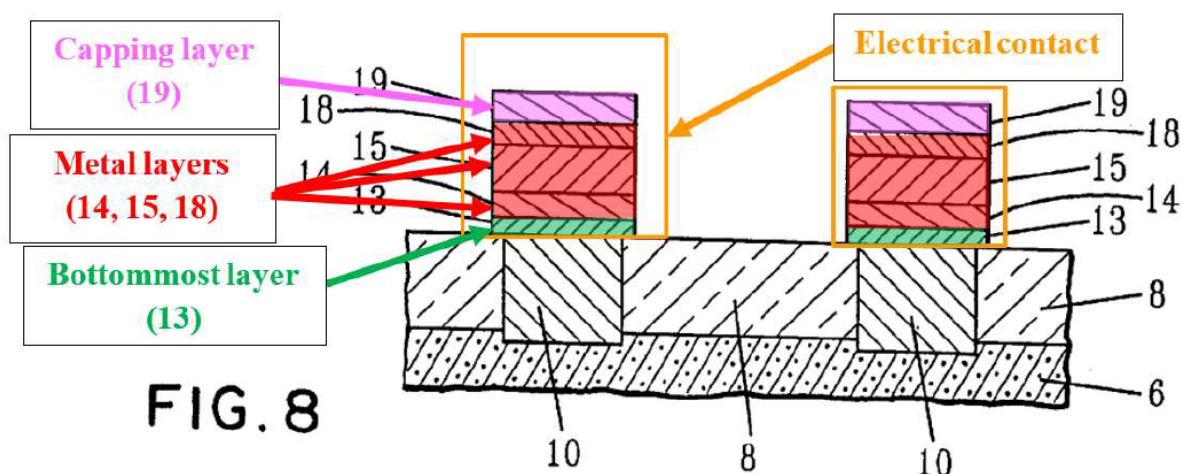
144. Other than repeating the claim language and alleging that Usui discloses an “electrode stack,” the Petition and Dr. Zhao entirely ignore the word “electrode” in the term “*electrode* stack.” Petition, 11-12; EX-1002 (Zhao Dec.), ¶¶89-91. As I discussed above in ¶¶76-79, Petitioner and Dr. Zhao appear to give no weight to the term “electrode,” and appear to contend that *any* stack “including a plurality of metal layers and a capping layer formed over said plurality of metal layers” constitutes an *electrode* stack. *See* Section VIII (noting that Dr. Zhao confirmed this more than a dozen times). I disagree with this approach.

145. As I discuss in Section VII, the ’562 specification uses “electrode stack” to refer to a stack of layers that form an electrode in a semiconductor

device, and describes three electrode types: (1) a “power electrode[]” that touches and is “ohmically coupled to” nonmetallic semiconductor material (EX-1001, 3:19-28, 1:33-43); (2) a transistor gate electrode that controls the flow of electrons or holes through the transistor and makes “Schottky contact” with nonmetallic semiconductor material (*id.*, 3:31-35); and (3) an insulated transistor gate electrode that controls the flow of electrons or holes through the transistor but is separated from the semiconductor by an insulating layer (*id.*, 3:21-33).

146. Usui’s interconnect metallurgy structure is not any of these structures and neither Petitioner nor Dr. Zhao even attempt to show that it is. *Compare, e.g.*, EX-1002 (Zhao Dec.), ¶¶55-61 (describing ohmic, Schottky, and gate contacts) *with* EX-1002 (Zhao Dec.), ¶¶88-91 (not contending that Usui’s structure is ohmic, Schottky, and gate contacts), ¶132 (conceding Usui does not disclose an electrical contact implemented as a gate electrode making Schottky contact), ¶140 (conceding Usui does not disclose a power electrode making ohmic contact).

147. The Usui structure that Petitioner and Dr. Zhao allege is an “electrode stack” is shown below.



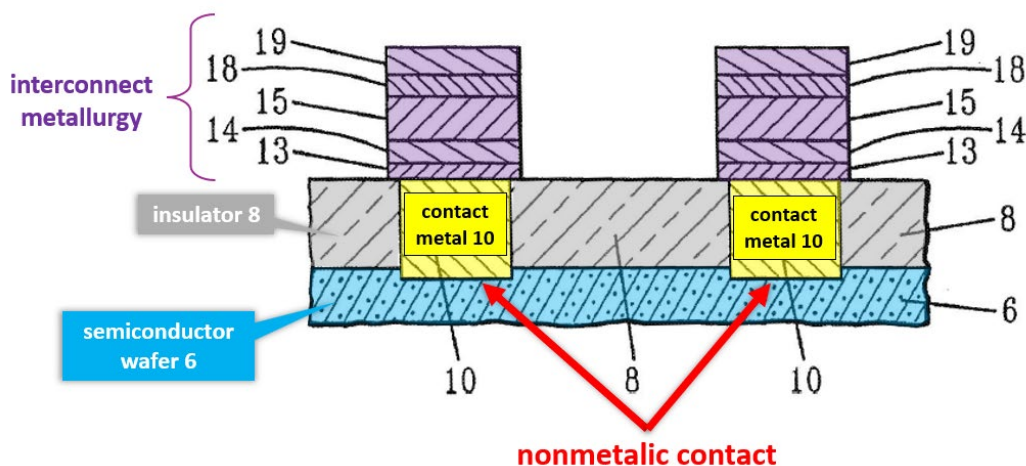
Petition, 11 (Petitioner’s Annotations to EX-1004 (Usui), Fig. 8). Usui uses several terms to refer to layers 13, 14, 15, 18, and 19 that Petitioner identifies above. For example, Usui (EX-1004) describes those layers as an “interconnect metallurgy” (1:22–27, 5:54–56), “metallization structure” (3:38–40, 7:53–54), “interconnect layer” (4:10–14), “interconnect metallization” (5:66–6:1), “metallurgy” (6:10–11), and “metallization stack” (6:26–33). Usui’s interconnect metallization structure “preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 to make connection to a device substrate 6.” EX-1002 (Usui), 3:24–27; *see also id.*, 5:14–15 (referring to the interplanar stud connection as “device contact metallization 10”), 3:2–8 (FIGs. 2–8 illustrate the process for making FIG. 1’s device).

148. Usui states that “[t]he structures fabricated by the process of the present invention are especially useful for forming *electrical connections or wiring* such as *between* active and/or passive *devices* of an integrated circuit structure.”

EX-1004 (Usui), 1:11–14. Usui’s interconnect metallurgy structure is thus, as I discuss above in Section VIII.A (e.g., ¶¶101-102), an *interconnect*. And, as I discussed in Section VI.C, interconnects are different from electrical contacts in numerous ways, and present different challenges, such as electromigration.

149. Usui *does not ever* use “electrical contact,” “electrode,” “electrode stack,” “source,” “gate,” “drain,” or any other terminology which would indicate to a POSA that Usui’s interconnect metallurgy (made up of layers 13, 14, 15, 18, and 19) is an “electrode” or forms an “electrode stack” of an electrical contact. And Usui’s interconnect metallization structure is not an electrode stack as disclosed in the ’562 Patent because it is not (1) a power electrode making ohmic contact with the nonmetallic semiconductor material (EX-1001, 3:19-27, 1:33-43); (2) a transistor gate electrode making “Schottky contact” with the nonmetallic semiconductor (*id.*, 3:31-35); or (3) an insulated transistor gate electrode (*id.*, 3:21-33). This is confirmed by the fact that Usui’s interconnect metallurgy is separated from underlying semiconductor material by Usui’s contact metal 10. Usui’s interconnect metallurgy thus does not form an ohmic contact (which requires direct contact with the semiconductor), or a Schottky contact (which also requires direct contact with the semiconductor), or an insulated gate electrode (which requires a very thin insulative material between the metal and semiconductor).

150. Usui's interconnect metallization structure is also not an "electrode stack" even under the broad dictionary definitions of electrode that I discussed above in Section VII (Claim Construction). As shown from Usui's annotated FIG. 8 below, Usui's interconnect metallization structure (layers 13-15 and 18-19) is not "a conductor used to establish electrical contact with a *nonmetallic* part of a circuit." EX-2001 (Merriam-Webster's), 371 (definition 1). Usui's interconnect metallization layer is instead connected to "interplanar stud connection 10." It is thus stud connection 10 that "make[s] connection to a device substrate 6" and establishes contact with a nonmetallic part of a circuit. EX-1002 (Usui), 3:24-27.



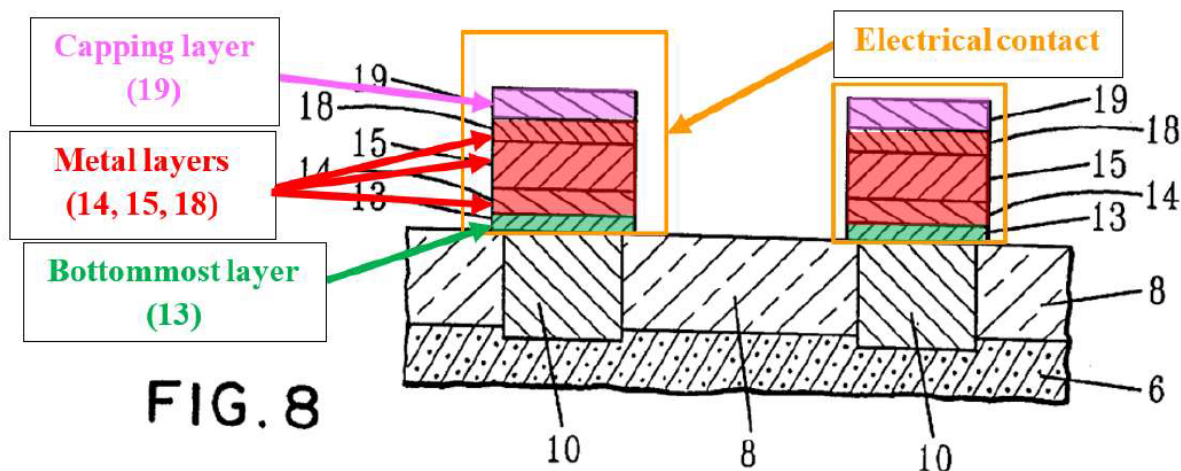
EX-1004 (Usui), Figure 8 (annotated). Above, stud connection 10 is *metal*. Usui, 5:14-15 ("device contact metallization 10"). Usui's interconnect metallization structure (layers 13-15 and 18-19) is therefore connected to *metal* stud connection 10, and is not "a conductor used to establish electrical contact with a nonmetallic

part of a circuit” – and, furthermore, is not an “electrode” under Merriam-Webster’s definition 1. EX-2001 (Merriam-Webster’s), 371.

151. Usui’s interconnect metallization structure also does not meet Merriam-Webster’s second definition of “electrode” specifically pertaining to a semiconductor device. Usui does not suggest that the interconnect metallization structure (layers 13-15 and 18-19) is “an element *in a semiconductor device* that *emits or collects electrons or holes or controls their movements.*” EX-2001 (Merriam-Webster’s), 371. As I have discussed (for example above in Section VIII.A), Usui’s interconnect metallization structure is not an element of a semiconductor device at all. Instead, as its “*interconnect* metallurgy” name indicates (EX-1004 (Usui), 3:23-27), Usui’s interconnect metallization structure is used to “form[] electrical connections or *wiring* such as *between* active and/or passive *devices* of an integrated circuit structure” (*id.*, 1:11-14). As Usui notes, Fig. 8’s single interconnect layer is “repeated in a multiple level sequence to complete the interconnect circuit for the devices.” Usui, 4:10-15.

152. The Petitioner and Dr. Zhao appear to mischaracterize Usui’s interconnect metallization structure (layers 13-15 and 18-19) as an electrode stack in order to meet claim 1’s requirement that the capping layer is thicker than the bottommost layer of the plurality of metal layers of the electrode stack. *See* Limitation [1c] (reciting, in relevant part, a “capping layer ... having a thickness

greater than that of a bottom most layer of said plurality of metal layers.”). The Petition and Dr. Zhao notably omit from their identification of an alleged electrode stack Usui’s “contact metal 10,” likely because it is depicted as significantly thicker than capping layer 19 in Usui’s Figure 8. EX-1004 (Usui), 5:11-21, Fig. 8.



Petition, 11 (Petitioner’s Annotations to EX-1004 (Usui), Fig. 8).

153. Dr. Zhao never explains why, if there is an electrode in Usui’s FIG. 8, “contact metal 10” would not have been considered to be the electrode – or part of the electrode – since contact metal 10 is the component that actually provides a “device contact” to Usui’s underlying nonmetallic semiconductor substrate 6. EX-1004 (Usui), 3:24-27, 5:14-15. Nothing in Usui or the ’562 Patent provides a basis to ignore Usui’s contact metal 10 when trying to identify an electrode stack in Usui. Moreover, *nothing* in Usui suggests that contact metal 10 is not itself a metal layer, or that contact metal 10 does not itself comprise metal layers. Instead, a POSA understood that structures like Usui’s contact metal 10 comprise a metal

layer or metal layers, which is corroborated by numerous references that illustrate how such structures are made. *E.g.*, EX-2032 (Gambino), 3:51-56 (“The field effect transistor[] T1... is located and fabricated within the semiconductor substrate 10...”), 6:8-19 (describing “contact studs 25” for “effecting optimal electrical contact and conduction to the first transistor T1...”), 7:9-22 (describing FIG. 4: “stud *layers* 25” and “dielectric layer[]...24” disposed underneath “interconnect layer[] 29”), 8:20-25 (describing “contact studs” as “conductor *layers*” that “are intended as electrically active *layers*.”), FIGs. 4-5; EX-2033 (Chen-653), [0014] (describing “interconnects in integrated circuits”), [0018] (describing FIG. 3: “via opening 14” over “semiconductor structure 10”), [0021]-[0023] (showing “diffusion barrier layer 18” and “conductive layer 20” in contact with semiconductor 10 within “via opening 14”), FIGs 3-4. A POSA also understood that Usui’s contact metal 10 comprises a metal “layer” or “layers,” as those words are used in the ’562 Patent, regardless of how contact metal 10 was formed – *e.g.*, by chemical vapor deposition (CVD), metal evaporation, or whether it is a “filled hole” as Dr. Zhao suggested during deposition (EX-2026 (Zhao Dep.), 10:10-13, 32:20, 32:24-25, 37:6-13, 37:19-25, 50:13-14, 51:11-23, 76:15-77:3, 77:17-24, 79:1-17). Petitioner or Dr. Zhao cannot show Usui has an “electrical *contact*” comprising an “electrode stack” as claimed simply by *ignoring* Usui’s “device *contact* metallization 10” (Usui, 5:14-15) which provides a “device

contact” to Usui’s nonmetallic semiconductor substrate. EX-2001 (Merriam Webster’s), 371.

B. Grounds 2-4 Also Fail

1. Grounds 2-4 Fall with Ground 1

154. Ground 2 challenges independent claim 13 and relies on EX-1005 (Yu) in addition to EX-1004 (Usui). For claim 13, the Petitioner and Dr. Zhao *only* rely on EX-1005 (Yu) to meet claim 13’s requirement for a Group III-V semiconductor device. Petition, 18-19; EX-1002 (Zhao Dec.), ¶¶110-111.

155. The Petitioner and Dr. Zhao rely on the *same* interconnect metallization structure from Usui that Ground 1 relies on to meet claim 13’s limitations reciting an electrical contact comprising an “electrode stack.” Petition, 18-19 (“A POSITA would have been motivated to implement *the electrical contacts as taught by Usui* in group III-V semiconductor devices, as taught by Yu”); EX-1002 (Zhao Dec.), ¶¶110-111. In fact, the Petition relies entirely on Ground 1’s showing for how Usui supposedly meets claim 1’s corresponding limitations to meet claim 13’s Limitations [13a] and 13[c]. Petition, 23 (arguing that “[13a] is identical to [1a]. [13a] is obvious as explained for [1a]” and that “[13c] is identical to [1c]. [13c] is obvious as explained for [1c]”). Ground 2’s argument regarding claim 13 therefore suffers from all of the same flaws I described above for Ground 1, in Section IX.A.

156. Grounds 2-4 also try to combine additional references to Ground 1's Usui reference to address certain dependent claims. Petition, 3; *see also* EX-1002 (Zhao Dec.), ¶83. For example, Ground 2 adds EX-1005 (Yu) to address claims 3, 8, 12, 13, and 17. Petition, 18-19. Ground 3 adds EX-1006 (Adesida) to address claims 9, 11, 14, and 16. Petition, 3. Ground 4 adds EX-1007 (Sugimoto) to address claims 10 and 15. *Id.* Because the dependent claims challenged in Grounds 2-4 depend from either independent claim 1 or independent claim 13, Ground 2-4 inherit the flaws regarding independent claims 1 and 13 that I discussed for Ground 1, above in Section IX.A.

157. I discuss additional flaws with each of Grounds 2-4, below.

2. Ground 2 – The Petition and Dr. Zhao Fail to Establish Obviousness for Claims 12 And 17 for Additional Reasons

158. I was asked to consider Ground 2's challenge to claims 12 and 17, which require that the independent claims' electrical contact is "implemented with a gate insulator," and have determined that Petitioner's challenge has additional glaring flaws.

159. As an initial matter, it appears that Petitioner alleges Yu motivates three disparate modifications to Usui (Petition, 16-17), but Petitioner never clearly identifies precisely what modifications to Usui that Petitioner proposes. Petitioner never illustrates the Usui-Yu combination. Petitioner never explains how the

supposed Usui-Yu combination works, and never maps any claim to a clearly-explained combination.

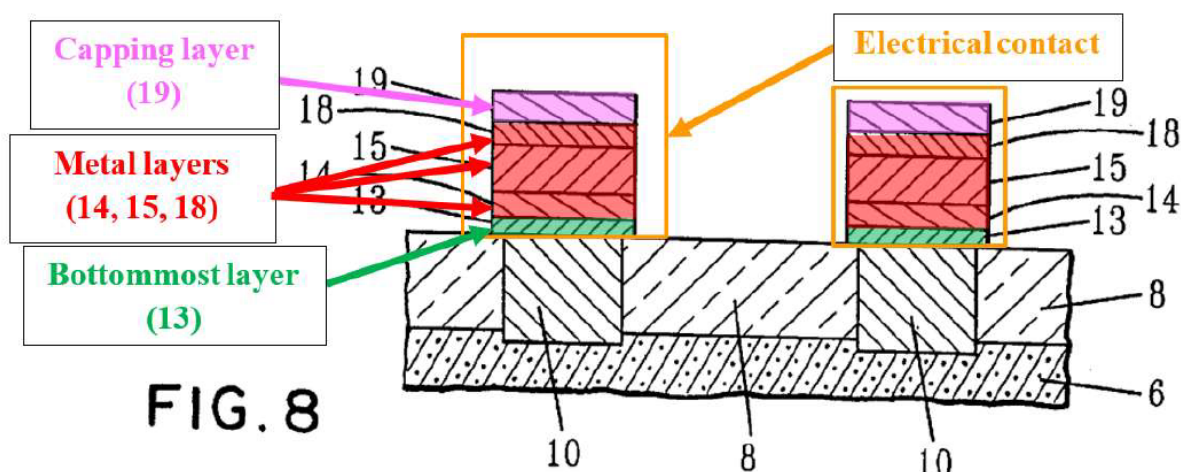
160. Setting that issue aside, at minimum, it is clear that Petitioner and Dr. Zhao concede that “Usui does not expressly disclose an electrical contact implemented with a gate insulator underlying a first metal layer to provide an insulated gate electrode.” Petition, 19; EX-1002 (Zhao Dec.), ¶112. And Petitioner and Dr. Zhao further allege that “Yu does.” Petition, 19; EX-1002 (Zhao Dec.), ¶112. I note Yu’s mere disclosure of an insulated gate electrode does not on its own articulate any non-hindsight reason to specifically select Yu’s gate insulator and add it to Usui’s interconnect metallization stack.

161. Petitioner and Dr. Zhao then make two disparate observations: first, that “Usui describes an electrical contact suitable to provide connections or wirings *between...devices* of an integrated circuit” and second, that it was “well-known” to isolate a gate from the channel in a thin film transistor. Petition, 19-20; EX-1002 (Zhao Dec.), ¶¶113-114. From these observations, Petitioner and Dr. Zhao somehow conclude: “it would have been obvious to implement the electrical contact of Usui with Yu’s gate insulator layer because Usui discloses the importance of improving electromigration characteristics and such [gate insulator] layers are commonly provided *under gate struct[ures]* to address gate leakage – combining prior art elements according to known techniques to a known device

ready for improvement to yield predictable results.” Petition, 20; EX-1002 (Zhao Dec.), ¶114. I disagree with Petitioner’s and Dr. Zhao’s conclusion.

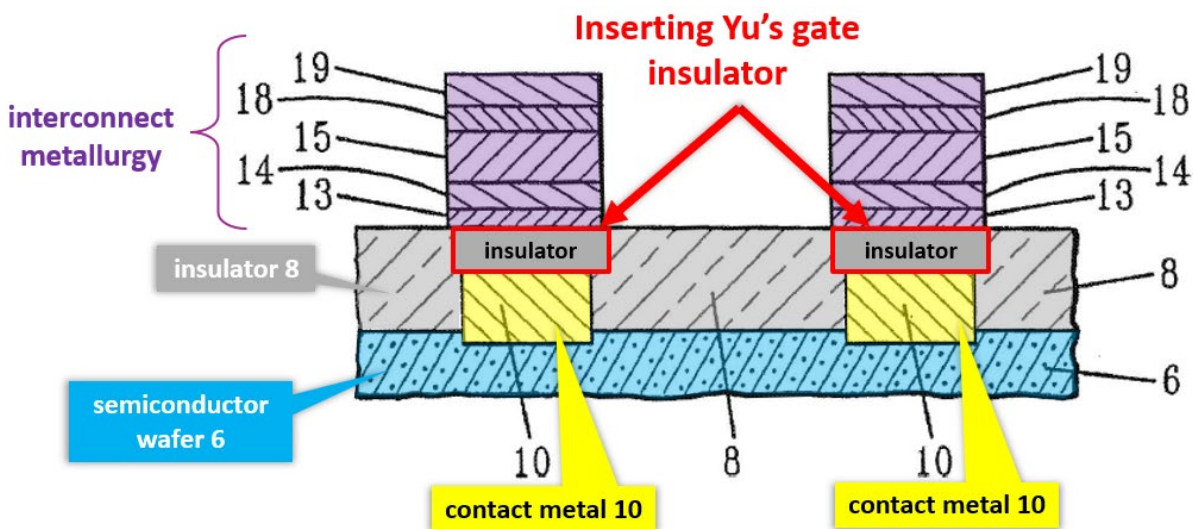
162. This modification is not one a POSA would have made. While Petitioner and Dr. Zhao provide very little detail regarding their proposed modification, at minimum it is clear that it includes “implement[ing] the electrical contact of Usui with Yu’s gate insulator layer.” Petition, 19; EX-1002 (Zhao Dec.), ¶114. As I discussed previously, Petitioner and Dr. Zhao repeatedly (and in my opinion wrongly) characterize Usui’s interconnect metallization structure (layers 13-15 and 18-19 in EX-1004 (Usui) FIG. 8) as the “electrical contact” of Usui. *E.g.*, Petition, 11; EX-1002 (Zhao Dec.), ¶91. Petitioner and Dr. Zhao also indicate that Yu’s interfacial dielectric layer 214 and high-k dielectric layer 216 are, together, Yu’s “gate insulator layer,” which Petitioner and Dr. Zhao say “underly[]” Yu’s “metal diffusion barrier/protection layer 218.” Petition, 19; EX-1002 (Zhao Dec.), ¶112.

163. Petitioner’s description, while scant, makes clear that Petitioner’s proposed modification involves adding an insulator from EX-1005 (Yu), Figure 2E to EX-1004 (Usui), Figure 8 that *underlies* Usui’s metal layer 13, which is the bottommost layer of the interconnect metallization structure that Petitioner alleges is Usui’s electrode stack. EX-1004 (Usui), Figure 8, with Petitioner’s annotations, is reproduced below for convenience:



Petition, 11 (Petitioner's Annotations to EX-1004 (Usui), Fig. 8).

164. I attempt to illustrate the modification below, based on Petitioner's and Dr. Zhao's description:



Usui, FIG. 8 (annotated to reflect Petitioner's modification in view of Yu). As can be seen above, Petitioner's modification entails *interrupting* the metal-to-metal junction of layer 13 and contact metal 10 using an insulator and thereby preventing the flow of current between them.

165. As an initial matter, *even if* the identified metal layers in Usui formed an electrode – they do not, as I discussed above in Section IX.A – there is no need to “isolat[e]” Usui’s alleged electrode “from the channel so that no current flows” to “address gate leakage” (Petition, 20) because Usui simply does not teach that its alleged electrode is a transistor *gate* electrode overlying a transistor channel in the semiconductor.

166. As I discussed above in Section VI.B, a gate electrode, or gate contact, is an electrode on a semiconductor purposefully designed and intended to provide a voltage to modulate conduction of electrons in the semiconductor underneath the gate contact. Usui does not use the words “gate” or “gate electrode,” and there is nothing in Usui to suggest that Usui’s metal interconnects would have been suitable for forming a gate electrode of a transistor. Usui also does not use the word “channel,” and there is nothing in Usui to suggest that Usui’s semiconductor wafer 6 is designed and intended to provide a voltage to modulate conduction of electrons through the semiconductor. The basic concept behind the field effect transistor in the context of an HEMT consists of an active channel (2DEG) in the semiconductor through which electrons flow from drain to source (or holes from the source to the drain). *See* EX-1011 (Mishra), 356 (Page 380 of 583). The conductivity of the channel is modulated by a potential applied (gate bias) to the gate. *Id.* This results in the modulation of the charge density

flowing in the channel. *Id.* Usui describes none of this. The only thing below Usui's interconnect structure is contact metal 10 (to allow the flow of current through the contact metal) and insulator 8 (to prevent the flow of current everywhere else). Placing an insulator between layer 13 and contact metal 10 would have prevented the flow of current but it would not have *created* a gate electrode – insulated or otherwise.

167. Indeed, EX-1004 (Usui) Fig. 8 *does not even disclose a transistor*, let alone that the alleged electrode overlies a transistor channel. This is undisputable, and Dr. Zhao agreed during deposition. EX-2026 (Zhao Dep.), 58:17-59:17 (“...in figure 8, there’s no information here I could, I could say whether it is or not a transistor...”), 59:18-60:1 (“...whether the, the device substrate layer 6 includes a transistor, or not a transistor, it’s not discussed in Usui.”). Because Usui does not disclose a transistor gate that would benefit from an insulating layer, the alleged motivation that Petitioner and Dr. Zhao articulate for modifying Usui to use a gate insulating layer simply makes no sense, and fails.

168. Petitioner and Dr. Zhao also fail to establish a reasonable expectation of success in implementing Usui to include Yu’s insulating layer. As noted above, Petitioner’s proposed modification entails *interrupting* the metal-to-metal junction of layer 13 and contact metal 10 using an insulator and thereby preventing the flow of current between them. This modification would prevent the flow of current,

created an open circuit, and caused Usui's device to cease functioning, as discussed in further detail below.

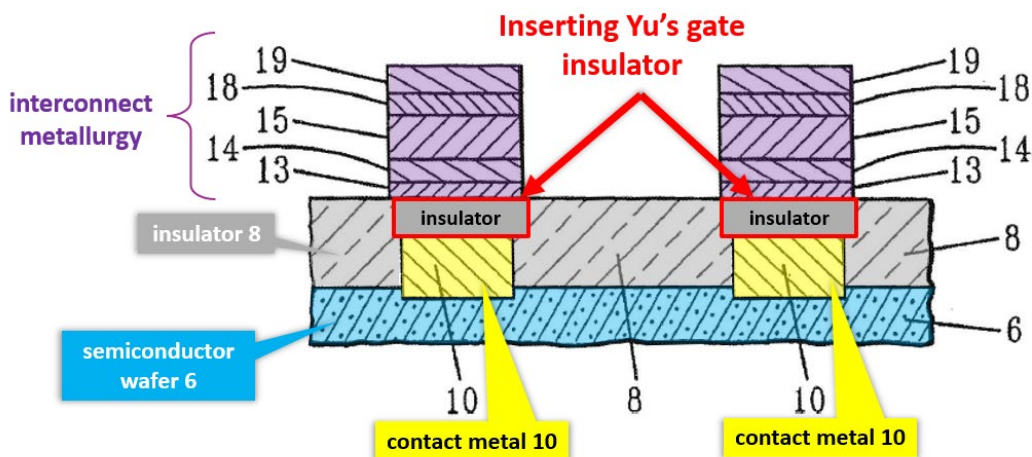
169. The *entire purpose* of Usui's metal layers 13-15 and 18-19 is to provide "electrical connections or wiring in electronic devices" (an interconnect) with improved "electromigration characteristics." EX-1004 (Usui), 1:17-23, 2:33-39; Petition, 19 (admitting same). That is, Usui's purpose is to provide an interconnect or wiring design in which electromigration is, as Dr. Zhao confirmed during deposition, *prevented*. EX-2026 (Zhao Dep.), 13:9-11 ("And in Usui, Usui provides a guidance to improve the electromigration by limiting the thickness of bottom layer."), 13:23-14:9 ("Q. What is your understanding of the phrase improve electromigration? A. To improve the electromigration by reducing some the negative effects. Q. And what negative effects are you referring to? A. In electromigration and what you see is metal, one the example of electromigration is the metal atom will diffuse into semiconductor layers, leading to reliability issues. One of the common way to, to mitigate, to improve the electromigration is to putting the diffusion barrier layer.").

170. In Usui's Fig. 8, metal layers 13-15, 18-19 – Usui's interconnect metallization structure between, e.g. semiconductor devices in a circuit – provide an electrical connection between "interplanar stud connection 10" – EX-1004 (Usui), 3:27 – and another layer of interconnect metal layers, with a "multiple level

sequence” of interconnect layers that “complete[s] the interconnect circuit” to another device, which is not shown in Fig. 8. EX-1004 (Usui), 4:10-15. Dr. Zhao agrees. EX-2026 (Zhao Dep.), 49:24-50:10 (“And eventually the outside world will be connected, in Usui’s case through the, you know, those metal layers, capping which are the claim features, and through the via, and to the semiconductor device level 6, I believe.”).

171. Yu’s gate insulator layer is undisputedly *not conductive*. EX-1005 (Yu), [0039]. Dr. Zhao agrees. EX-2026 (Zhao Dep.), 89:18-25 (“Q. ... Okay. Is layer 214 in Yu 19 figure 2E a conductive layer? A. Let me go to the reference. You are referring to 214, this layer, right? Q. That’s correct. A. Yeah, 214 layer, the 214 layer in Yu's reference is a dielectric layer. It is typically not conducting.”), 90:8 (“Yu 214 and 216, they are not conducting”).

172. Thus, placing Yu’s gate insulating layer under the alleged electrode in Usui, as Petitioner alleges (Petition, 19-20; EX-1002 (Zhao Dec.), ¶114), would place an insulator *between* Usui’s bottommost layer 13 and interplanar stud connection 10 and **break** the electrical connection therebetween. For convenience, this interruption is illustrated (again) below:

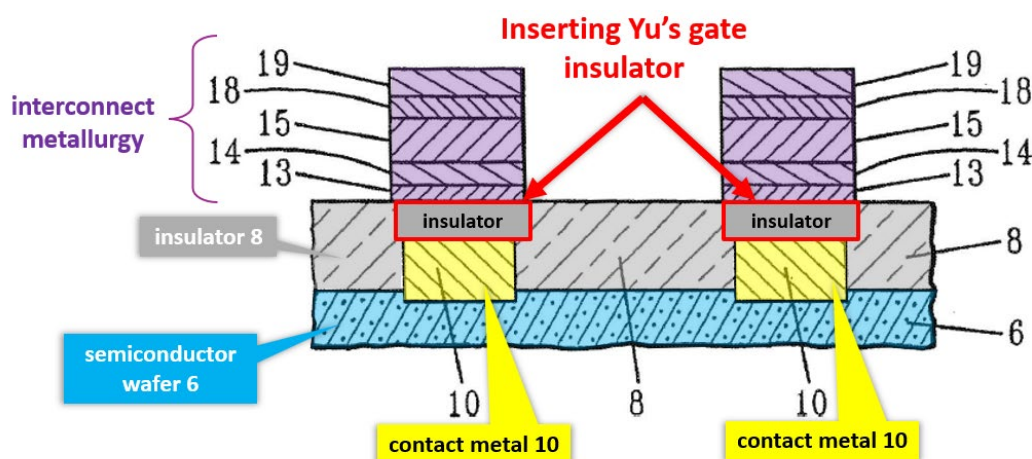


Usui, FIG. 8 (annotated to reflect Petitioner’s modification in view of Yu). As can be seen above, the modification would have rendered Usui inoperable for its intended purpose of providing improved “electrical connections or wiring” between devices of an integrated circuit. EX-1004 (Usui), 1:11-15.

173. Separately, Petitioner’s and Dr. Zhao’s assertion that its Usui-Yu combination “combin[es] prior elements according to known techniques to [yield] a known device ready for improvement” (Petition, 20; EX-1002 (Zhao Dec.), ¶114), is not technically sound. For example, I disagree with their unsupported conclusory assertion that Usui was “ready for improvement,” especially given the fact that neither Petitioner nor Dr. Zhao ever explains *how* Usui’s interconnect metallization structure allegedly would possibly have been improved by “implement[ing] the electrical contact of Usui with Yu’s gate insulating layer.” Petition, 20; EX-1002 (Zhao Dec.), ¶114. As I discussed above in ¶¶165-167, Usui does not even disclose a transistor gate electrode or a transistor channel, *and Dr.*

Zhao agrees. EX-2026 (Zhao Dep.), 58:17-60:1. Usui thus *certainly* does not disclose a transistor gate electrode that could be improved by being isolated from a transistor channel. Petitioner's and Dr. Zhao's premise of a device ready for improvement is simply wrong.

174. I was also asked by counsel to determine whether the elements of Usui and Yu, when combined, would have the same function before and after being combined. They do not. As I've discussed above, Petitioner's Usui-Yu combination renders Usui's interconnect inoperable. And the combination completely *changes* the function of Yu's gate insulating layer. Rather than being used to separate a gate electrode from a transistor channel as was taught in Yu, the gate insulating layer (Yu layers 214 and 216) in Usui-Yu would have an entirely new function: to separate two metal structures that Usui teaches should be in direct contact.



Usui, FIG. 8 (annotated to reflect Petitioner's modification in view of Yu).

175. I note that, based on my review of the Petition and EX-1002 (Zhao Dec.), that Petitioner and Dr. Zhao *do not allege* a POSA had any reason to replace Yu's gate electrode with Usui's metal layers. Petition, 20. They instead allege that a POSA would have implemented *Usui's* interconnect metallization structure (layers 13-15 and 18-19) with Yu's gate insulating layer. Petition, 20. I further note that, even if Petitioner had alleged in Ground 2 that a POSA would have *instead* replaced Yu's gate electrode with *Usui's* interconnect metallization structure (layers 13-15 and 18-19), that would likewise have resulted in dramatically changing the function of Usui's metal layers 13-15 and 18-19. In particular, Usui's interconnect metallization structure would change from functioning as a single interconnect layer that connects metal stud 10 to another interconnect level forming an interconnect circuit to another device (EX-1004 (Usui), 3:23-27, 4:10-15) – to functioning as a gate electrode. Moreover, a POSA would not have made such a modification because, as discussed above in Sections VI.C, Usui teaches a particular metal stack for wires to mitigate electromigration due to high current density (EX-1004 (Usui), 1:30-41, 2:33-39), which is not a concern for Yu's gate electrode, because it does not experience high current density. *See* also my discussion regarding current density and electromigration above in Section VIII.A and below in Section IX.B.3.a.iii. Additionally, as I discussed above in Section VIII.B (§§106-114), Yu's entire disclosure is about

using a *specific* metal stack (not Usui's) with a particular work function that is chosen to be compatible with a high-k dielectric. EX-1005 (Yu), [0004], [0029].

176. In sum, Ground 2 fails to establish any non-hindsight reason why a POSA would have combined Usui and Yu in the manner alleged to meet claims 12 and 17 with a reasonable expectation of success.

3. Ground 3 Fails for Additional Reasons

a. Claims 11 and 16

177. Claims 11 and 16 require that the electrical contact is “implemented as a gate electrode making Schottky contact with said...semiconductor device.” As I discussed above in Section VI.B (¶¶58-61) it was well-understood by POSAs that a gate electrode making Schottky contact (or Schottky barrier) is designed for a metal-semiconductor interface and does not have an insulating layer between the gate electrode and the semiconductor. EX-1001, 3:31-35; EX-1011 (Mishra), 219; EX-1013 (Quay), 151 (Page 178 of 492); EX-1002 (Zhao Dec.), ¶58.

178. In Ground 3, Petitioner and Dr. Zhao allege that claims 11 and 16 are obvious based on the combined teachings of Usui, Yu, and Adesida. Petitioner and Dr. Zhao admit that Usui and Yu do not disclose “an electrical contact implemented as a gate electrode making Schottky contact” but alleges “Adesida does.” Petition, 26; EX-1002 (Zhao Dec.), ¶132. But that does not establish obviousness, in part because neither Petitioner nor Dr. Zhao provides any logical

or credible reason why a POSA would have used Usui's interconnect metallurgy structure as a Schottky contact.

i. Petitioner Fails to Establish Any Reason to Have Modified Usui Based on Yu and Adesida in the Claimed Manner

179. Both Petitioner and Dr. Zhao allege that a "POSITA would have been motivated to implement the electrical contacts as taught by Usui-Yu as a gate electrode making Schottky contact, as taught by Adesida, because both Yu and Adesida disclose the use of III-V semiconductor devices." Petition, 16; EX-1002 (Zhao Dec.), ¶132. But just because Yu and Adesida *mention* III-V semiconductor devices does not mean that a POSA would have been motivated to modify Usui's interconnect structure to be used somehow as a Schottky contact, when Usui's interconnect was never intended to be used as an electrical contact – let alone a Schottky contact.

180. I reviewed the evidence cited by Petitioner at page 29 – Zhao ¶¶48-61, 137; Sections VII.C.1, VII.C.1.b – and was not able to find any reason to combine Usui's interconnect metallization structure with gate electrode teachings.

181. For example, Petitioner and Dr. Zhao allege that Adesida is analogous art, and that Schottky gate contacts were known in group III-V devices and were "well known for their suitability for high frequency applications and therefore enhanced electromigration." Petition, 26; EX-1002 (Zhao Dec.), ¶133.

182. However, I see no logical connection between the high-frequency applications of group III-V semiconductor devices and the electromigration issues discussed in Usui. Neither the Petitioner nor Dr. Zhao provided any evidence of any connection between the two. And Petitioner simply seems to be mistaken about electromigration in interconnects. As I discussed above in Section VI.C (¶¶62-71), hillock growth and other electromigration problems are caused when current through the limited cross-sectional area of the interconnect wiring is greater than the wiring can sufficiently handle. That has no logical connection to the frequency of the signal and, perhaps more importantly, no link to the use of Schottky contacts. Moreover, the general premise that Schottky contacts have been implemented in certain circumstances does not explain why a POSA would have modified Usui's specific interconnect structure (made from layers of titanium, aluminum, and titanium nitride) to be used as a Schottky contact nor that it could even work. *See, e.g.,* EX-1017 (Kramer), 30 (Page 37 of 151) (“[T]he major contribution to the Schottky barrier height is due to the difference in the metal and semiconductor work functions. Hence, metals with a low work function e.g. Titanium (Ti) and Aluminum (Al) are used for Ohmic contacts on *n* – type GaN – based materials systems. To obtain Schottky contacts on *n* – type GaN – based materials systems metals with a high work function e.g. Platinum (Pt), Nickel (Ni), Gold (Au), Iridium (Ir) and Palladium (Pd) are used.”), 2 (Page 10 of 151)

(reporting that, although Schottky contacts using Platinum (Pt), Ni, Au and Ni/Au were in use, testing of Pt and Au contacts “suffered from a very bad adhesion” to the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ semiconductor material).

183. Moreover, *even if* Petitioner’s and Dr. Zhao’s assertions regarding the benefits of Schottky gate electrodes were accepted as true, this does not establish any reason to modify Usui. As discussed above in Section IX.B.2, Usui does not disclose a transistor gate electrode, and Dr. Zhao agrees. EX-2026 (Zhao Dep.), 58:17-60:1.

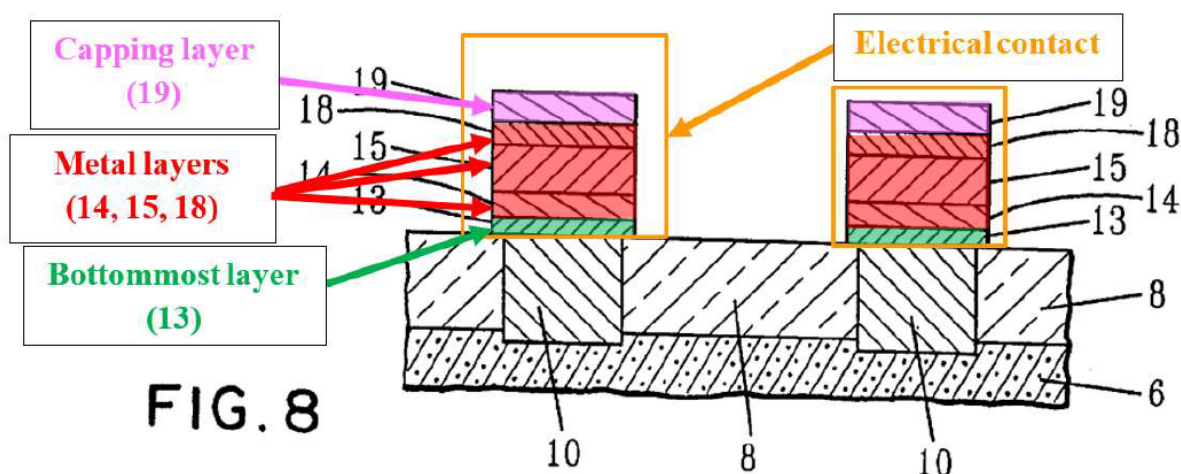
184. Petitioner and Dr. Zhao also state that “[i]t was well-known that Schottky contacts serve as gate contacts in group III-V devices.” Petition, 26-27; EX-1002 (Zhao Dec.), ¶132. But that does not mean it was well-known that any *interconnect* structure – such as the one taught in Usui – could serve as a Schottky contact. None of references that Petitioner and Dr. Zhao has cited which discuss Schottky contacts appear to indicate that a POSA would have even considered Usui’s interconnect structure relevant to Schottky gate design. As Dr. Zhao conceded during deposition, Usui does not even disclose a transistor – let alone a Schottky gate electrode. EX-2026 (Zhao Dep.), 58:17-60:1.

185. Despite there being no logical link between the teachings of Usui, Yu, and Adesida and no suggestion of the specific modification to Usui’s interconnect structure proposed, Petitioner and Dr. Zhao contend that “it was well-known at the

time that implementing the Usui-Yu contact as a Schottky contact, as taught by Adesida, constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications).” Petition, 26; EX-1002 (Zhao Dec.), ¶133. I do not agree. As I discussed above in Sections VI.A and VI.B, electrical contact design was anything but simple and nothing that Petitioner or Dr. Zhao cite indicates that anyone had ever modified an interconnect structure to be used as a Schottky gate in a transistor, to say nothing of modifying Usui’s specific structure. To the contrary, as one reference put it, fabrication of electrical contacts is “still more art than science.” EX-1017 (Kramer), 31 (Page 38 of 151); *see also* EX-1017 (Kramer), 51 (Page 58 of 151) (“Literature shows that the actual mechanism of Ohmic contact formation is still subject of discussion and yet to be understood.”). Although the author in EX-1016 specifically referred to ohmic contact fabrication, the statement about complexity also applies to Schottky contact fabrication – and in fact is still true today, a decade and half later.

186. Moreover, even if it *were* a “simple design choice” to choose between an insulated gate electrode and a Schottky gate electrode when implementing a transistor – which I do not concede – I note that this is irrelevant to Usui, because it would not have been a “simple design choice” to implement Usui specifically as a Schottky gate electrode, for numerous reasons. For example, as discussed, Usui’s interconnect metallization structure (metal layers 13-15, 18-19) is an

interconnect that provides wiring *between* devices and overlies contact metal 10. EX-1004 (Usui), 1:11-14 (“The structures fabricated by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure”), 3:23-27, 5:11-65. Moreover, as discussed, Usui does not disclose a transistor in the first place, let alone a transistor *gate* electrode, which Dr. Zhao concedes. EX-2026 (Zhao Dep.), 58:17-60:1. Moreover, Usui’s interconnect metallurgy structure (layers 13-15 and 18-19) does not make Schottky contact with Usui’s semiconductor wafer 6 because Usui’s interconnect metallurgy structure is separated from the semiconductor by insulator 8 – as Dr. Zhao himself appears to recognize. EX-1004 (Usui), 3:23-28, 5:11-33, Fig. 8; Zhao, ¶58; EX-2026 (Zhao Dep.), 123:19-124:3 (“...there are two types of commonly used gate structure, insulated gate *with* a[n] insulating or dielectric layer, or Schottky gate *without* the insulating or dielectric layers” – between which POSAs “*choose*.”). In view of above, a POSA understood that modifying Usui to have its interconnect metallization structure somehow make Schottky contact with a transistor channel would have been the furthest thing from a “simple design choice.”



Petition, 11 (Petitioner’s Annotations to EX-1004 (Usui), Fig. 8).

187. Petitioner and Dr. Zhao also contend that Usui-Yu-Adesida combination is merely “combining prior elements according to known techniques to a known device ready for improvement to yield predicable results.” Petition, 26-27; EX-1002 (Zhao Dec.), ¶133. Again, I do not agree. As an initial matter, there was nothing “known” about using Usui’s stack of metals for a completely unrelated purpose – particularly for something as challenging as a metal-semiconductor junction on a group III-V semiconductor material, when there was no way to predict how that stack would function (or not function) if deposited without modification on a group III-V semiconductor material. EX-1017 (Kramer), which Dr. Zhao relies on, reports that “[f]or the Schottky contacts several different metallization schemes were in use such as Platinum (Pt), Ni, Au and Ni/Au” – none of which are the metals suggested for use in Usui’s interconnect. *See* EX-1017 (Kramer), 2 (Page 10 of 151); EX-1004 (Usui), 5:11-

59. EX-1017 (Kramer) also indicated that “Schottky contacts should yield a: low reverse current density ($J_s \approx 10^{-5}$ A/cm² at breakdown); high breakdown voltage ($V_{break} > 100$ V); and unity approaching ideality factor (n).” EX-1017, 2 (Kramer), (Page 10 of 151). Dr. Zhao does not contend that Usui’s interconnect structure could meet any of these criteria.

188. I likewise disagree with Petitioner’s and Dr. Zhao’s assertion that Usui’s interconnect structure was “ready for improvement.” Neither Petitioner nor Dr. Zhao explain how Usui’s interconnect structure would have been improved by “implementing the Usui-Yu contact as a Schottky contact,” as alleged. Petition, 26-27; EX-1002 (Zhao Dec.), ¶133. Usui does not disclose a transistor gate electrode, as Dr. Zhao himself admitted. EX-2026 (Zhao Dep.), 58:17-60:1. Since Usui does not disclose a transistor gate electrode and instead discloses an interconnect, it is not clear how Usui’s interconnect could be improved by implementing it as an entirely different component – a Schottky gate electrode.

189. I was also asked by counsel to determine whether the elements of Usui, Yu, and Adesida, when combined, would have the same function before and after being combined. They would not. At minimum, the function of Usui’s interconnect structure would have dramatically changed in Petitioner’s and Dr. Zhao’s proposed combination. Instead of being an interconnect metallurgy structure that is part of an interconnect circuit that connects metal stud 10 to

another part of the circuit (Usui, 3:23-27, 4:10-15) while mitigating electromigration (Usui, 1:30-41, 2:33-39), Usui's metal layers 13-15 and 18-19 would somehow function as a Schottky gate electrode that does not experience high current density and thus would not even implicate any of the electromigration concerns that are the focus of Usui's disclosure. *See* also my discussion regarding current density and electromigration above in Section VIII.A and below in Section IX.B.3.a.iii.

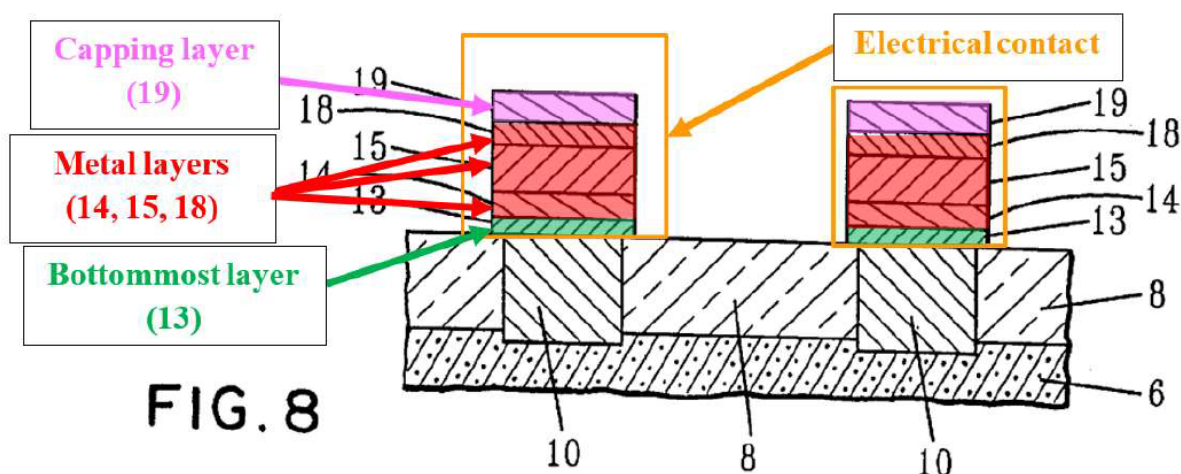
ii. Petitioner Fails to Explain the Contemplated Workings of the Usui-Yu-Adesida Combination and How it Meets the Challenged Claims

190. Petitioner and Dr. Zhao do not describe their Usui-Yu-Adesida combination in sufficient detail to establish obviousness. Petitioner and Dr. Zhao provide *no* details regarding which layers or specific components from which references (Usui, Yu, and Adesida) are incorporated into Petitioner's combination, where those layers or specific components would go in the combination, and what the thicknesses of the relevant layers would be after the references are combined. Petitioner's and Dr. Zhao's failure to reveal these *basic* details defeats any showing of obviousness, because, for example, those details are needed to confirm whether Usui-Yu-Adesida meets the thickness limitations in independent claims 1 and 13.

191. The closest that Petitioner and Dr. Zhao get to describing their actual combination is the contention is that "[i]t would have been obvious to implement

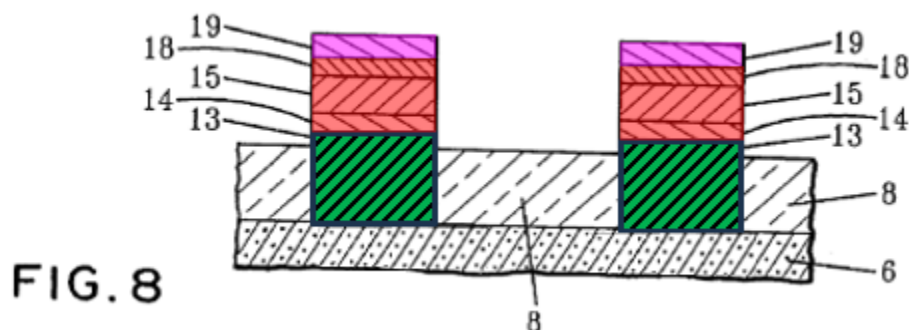
the electrical contact of Usui-Yu in a device with a gate electrode making Schottky contact, *as taught by Adesida.*” Petition, 29; EX-1002 (Zhao Dec.), ¶133. As an initial matter, this appears to be inconsistent with Petitioner’s and Dr. Zhao’s earlier description of “the electrical contact of Usui-Yu” that involves adding Yu’s insulator below Usui’s interconnect metallization structure (Petition, 19-20; EX-1002 (Zhao Dec.), ¶¶112-114), discussed above in Section IX.B.2. A gate electrode cannot have an insulating layer *and* make Schottky contact with the semiconductor device, as Dr. Zhao himself agrees. Zhao, ¶58; EX-2026 (Zhao Dep.), 123:19-124:3 (“...there are two types of commonly used gate structure, insulated gate *with* a[n] insulating or dielectric layer, or Schottky gate *without* the insulating or dielectric layers” – between which POSAs “*choose.*”).

192. Moreover, even assuming Yu’s gate insulator layer is *not* present in Usui-Yu-Adesida – which is impossible to confirm given Petitioner’s and Dr. Zhao’s silence regarding even the basic contours of their Usui-Yu-Adesida combination – Petitioner and Dr. Zhao completely fail to explain how Usui’s interconnect metallization structure (layers 13-15 and 18-19) *could* have been modified to make Schottky contact with Usui’s “semiconductor wafer 6” in the first place, given the presence of “insulator 8,” which separates layers 13-15 and 18-19 from semiconductor 6, as shown below.



Petition, 11 (Petitioner's Annotations to EX-1004 (Usui), Fig. 8).

193. To the extent Petitioner and Dr. Zhao are suggesting that a POSA would have increased the thickness of layer 13 to extend through the insulator 8 (as contact metal 10 does) to reach semiconductor 6 in order to achieve Schottky contact, that would not meet the requirement the capping layer have “a thickness greater than that of a bottommost layer of said plurality of metal layers,” as recited in claims 1 and 13. To illustrate, I have provided a modified version of Usui's Figure 8 that shows layer 13 extending through the insulator 8 to reach and contact semiconductor 6.



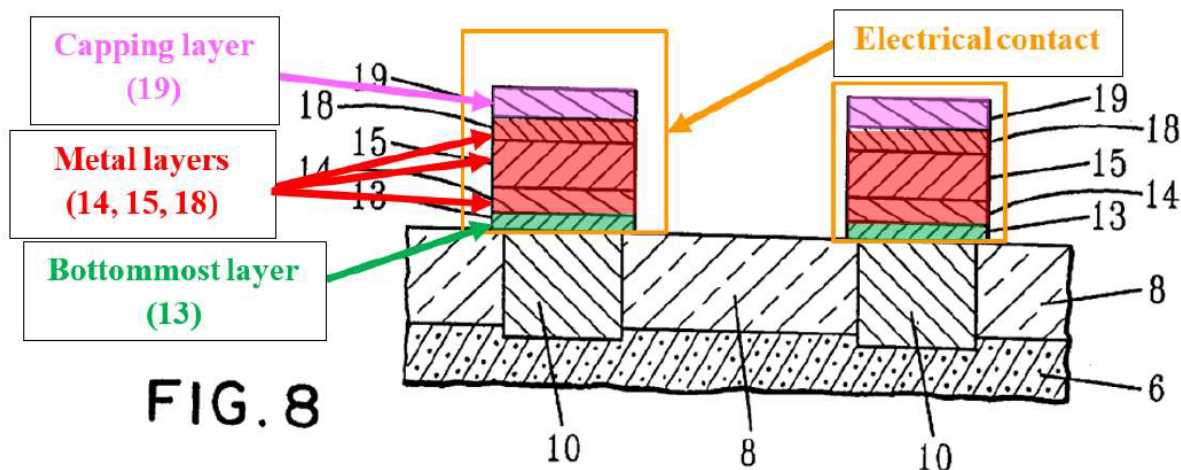
EX-1004 (Usui), Fig. 8 (annotated to reflect Petitioner's apparent modification in view of Yu and Adesida). As can be seen above, in this scenario, capping layer 19 (pink) would not have a thickness greater than layer 13 (green).

iii. Petitioner Fails to Establish a Reasonable Expectation of Success

194. Petitioner's Ground 3 also fails because neither Petitioner nor Dr. Zhao has established a reasonable expectation of success in arriving at the claimed combination. Indeed, as discussed below, Petitioner's proposed modification would have rendered Usui inoperable for its intended purpose.

195. Usui's interconnect metallization structure (layers 13-15 and 18-19) provides improved "electrical connections or wiring in electronic devices" with improved electromigration characteristics. EX-1004 (Usui), 1:17-23, 2:23-35; EX-2026 (Zhao Dep.), 13:9-11 ("And in Usui, Usui provides a guidance to improve the electromigration by limiting the thickness of bottom layer."), 13:23-14:9 ("Q. What is your understanding of the phrase improve electromigration? A. To improve the electromigration by reducing some the negative effects. Q. And what negative effects are you referring to? A. In electromigration and what you see is metal, one the example of electromigration is the metal atom will diffuse into semiconductor layers, leading to reliability issues. One of the common way to, to mitigate, to improve the electromigration is to putting the diffusion barrier layer.").

196. As a POSA would have appreciated, Usui's interconnect metallization structure readily allows current to pass through it. Usui's interconnect metallization structure (metal layers 13-15 and 18-19) is part of an "interconnect circuit" that provides an electrical connection between the contact metal 10 and a device that Usui does not illustrate in Fig. 8. EX-1004 (Usui), 3:27, 4:10-15; EX-2026 (Zhao Dep.), 49:24-50:10 ("And eventually the outside world will be connected, in Usui's case through the, you know, those metal layers, capping which are the claim features, and through the via, and to the semiconductor device level 6, I believe.").



Petition, 11 (Petitioner's Annotations to EX-1004 (Usui), Fig. 8).

197. It is unclear how Petitioner or Dr. Zhao proposes modifying Usui above to have Usui's alleged electrode (layers 13-15 and 18-19) somehow make Schottky contact with semiconductor material 6, because contact metal 10 is in between the alleged electrode (layers 13-15 and 18-19) and the semiconductor

material 6. But a POSA would understand that modifying Usui to have its alleged electrode (layers 13-15 and 18-19) somehow make Schottky contact with semiconductor material 6 would *at minimum* changed Usui's interconnect from operating as an "electrical connection[]" between contact metal 10 and another device, because instead of contacting metal stud 10 where it is pictured in Figure 8 above, Usui's interconnect metallization structure would have to directly contact the semiconductor. See my discussion above in Section VI.B (¶¶58-61), regarding Schottky contacts, and explaining that a gate electrode making Schottky contact (or Schottky barrier) is designed for a metal-semiconductor interface and does not have an insulating layer between the gate electrode and the semiconductor. EX-1001, 3:31-35; EX-1011 (Mishra), 219; EX-1013 (Quay), 151 (Page 178 of 492); EX-1002 (Zhao Dec.), ¶58.

198. Moreover, if Petitioner's modification involved removing *both* Usui's contact metal 10 and insulating layer 8 entirely – so that Usui's alleged electrode (metal layers 13-15 and 18-19) were simply placed in direct contact with the semiconductor, such that they contacted the semiconductor along their entire length and extent, without any insulator at all – that would also render Usui's device inoperable. A POSA would understand that such a modification would short the portions of the circuit not pictured in EX-1004 (Usui) Figure 8 that were previously isolated by insulating layer 8.

b. Claims 9 and 14

199. Claims 9 and 14 require that the electrical contact is configured for implementation on a “group III-V semiconductor device compris[ing] a high electron mobility transistor (HEMT).” As to claim 9, Petitioner and Dr. Zhao combine Usui in view of Yu and Adesida, contending that:

[i]t would have been obvious to implement the electrical contact of Usui-Yu on HEMTs, as taught by Adesida, because both Yu and Adesida disclose III-V semiconductor devices and as I further explained in Sections X.C.1, X.C.1.a, VI.A, VI.B.

Petition, 25; EX-1002 (Zhao Dec.), ¶¶134, 138. “Sections X.C.1, X.C.1.a” appears to refer to paragraphs 128-131 of the Zhao declaration, discussing an overview of the combination and motivations to combine. Sections “VI.A, VI.B” appear to refer to paragraphs 48-54 of the Zhao declaration, generally discussing Group III-V Material Devices and HEMTs.

200. Petitioner and Dr. Zhao generally describe purported advantages of HEMTs (“relatively high carrier concentration,” “relatively high carrier mobility,” “relatively large transconductance,” and “performance advantage over metal-semiconductor field effect transistors (MESFETS) for high-frequency applications” for their motivation to combine. Petition, 24-25; EX-1002 (Zhao Dec.), ¶130. None of these assertions explain why a POSA would have selected Usui’s interconnect structure for a group III-V semiconductor device having a

HEMT. As discussed in Sections VI.C and IX.A, Usui does not actually disclose an electrical contact comprising an electrode stack, contrary to Dr. Zhao's assertions. Thus, it is not clear how any of the purported advantages of HEMTs relate to the modification to Usui's interconnect structure.

201. Petitioner and Dr. Zhao also allege that "Usui discloses the importance of enhanced electromigration" and that a POSA would have been "motivated to implement" Usui-Yu's interconnect structure in group III-V semiconductor HEMT, as taught by Adesida, "because" this allegedly would have "enhanced electromigration." Petitioner, 25; EX-1002 (Zhao Dec.), ¶131. As discussed further below in the context of Ground 4, Petitioner misunderstands Usui's discussion of electromigration. Usui teaches that electromigration is a *problem* to be addressed and mitigated – not "*enhanced*" as Petitioner contends.

202. Further, there is no logical connection between the desire to provide relatively high carrier mobility and electromigration. To a POSA those concepts are unrelated. High carrier mobility refers to the mobility of *charge carriers within a semiconductor*. Electromigration refers to phenomenon of *atoms in a metal* physically migrating because of excessive electrical current. There is simply no rational link between them that would justify or even suggest Petitioner's proposed combination.

203. Petitioner and Dr. Zhao also contend that the Usui-Yu-Adesida combination would have allegedly constituted a “simple design choice depending on the application of the device.” Petition, 25; EX-1002 (Zhao Dec.), ¶131. But Petitioner and Dr. Zhao do not explain why certain applications of the device would cause a POSA to select Usui’s interconnect structure and implement it as an electrical contact in a group III-V semiconductor HEMT. Moreover, as I discussed previously in Section VI.B (¶¶58-61), there was nothing simple about *changing the type of transistor* associated with gate contact from Yu’s transistor to a HEMT. The design of electrical contacts in a group III-V semiconductor HEMT was – and remains – a challenging area of research because there is no verified way to predict how particular combinations of materials will perform when implemented in such devices without significant experimentation. *See, e.g.*, EX-1017 (Kramer), 79 (Page 86 of 151) (concluding that their proposed model for determining the optimal thickness ratio for two layers of an ohmic contact “fails completely” based on experimental data).

204. Further, the differences between Usui, Yu, and Adesida – and their respective description of materials, applications, and problems to be solved – do not lend themselves to any particular combination of a metal stack. Usui teaches a particular set of metal layers (Ti/TiN/Al/TiTiN) as an interconnect structure, designed to address problems associated with interconnects. Yu teaches

an insulated electrode using a conducting metal oxide to function as a gate electrode of a transistor. Adesida teaches use of Ir and Pt to form a Schottky gate on a lightly doped InAlAs layer. There is simply no connection between these very different materials, purposes, and implementations that would suggest the claimed combination of claims 9 and 14.

205. Beyond there being nothing in the cited prior art to suggest the combination, a POSA also would have understood that there would have been at the very least modifications to Usui's interconnect structure and its various layers in order for the interconnect structure to function as an electrical contact, if such an implementation were even possible. Petitioner and Dr. Zhao do not account for the changes that would have occurred to the metal layers – changes in materials or thicknesses – or the changes that would have occurred to the function of individual layers, and this failure to address the changes that would have needed to be made defeats Petitioner's obviousness showing as to claims 9 and 14.

4. Ground 4 Fails for Additional Reasons

206. In Ground 4, Petitioner and Dr. Zhao contend that claims 10 and 15 would have been obvious to a POSA based on a combination of EX-1004 (Usui), EX-1005 (Yu), and EX-1007 (Sugimoto). Claims 10 and 15 recites that the electrical contact is “implemented as a power electrode making ohmic contact with said group III-V semiconductor device.”

207. Petitioner and Dr. Zhao concede that Usui and Yu do not expressly disclose a power electrode making ohmic contact and relies exclusively on Sugimoto for this feature. Petition, 29; EX-1002 (Zhao Dec.), ¶140. Sugimoto – unlike Usui – is directed to addressing a problem of increase in resistance in the 2DEG (2-Dimensional Electron Gas) due to scattering of electrons caused by impurities within the p-GaN layer of a normally-off HEMT. EX-1007 (Sugimoto), 1:51-58. Sugimoto recognizes that lower impurities can cause instability in the normally-off operation of the HEMT and proposes alternative group III-V semiconductor layered structures with different band gaps to address the problem. EX-1007 (Sugimoto), 1:59-2:19; *see also* Section VIII.D (Sugimoto Discussion).

208. Ground 4 has several deficiencies as I discuss in more detail below.

i. Dr. Zhao Fails to Explain the Contemplated Combination

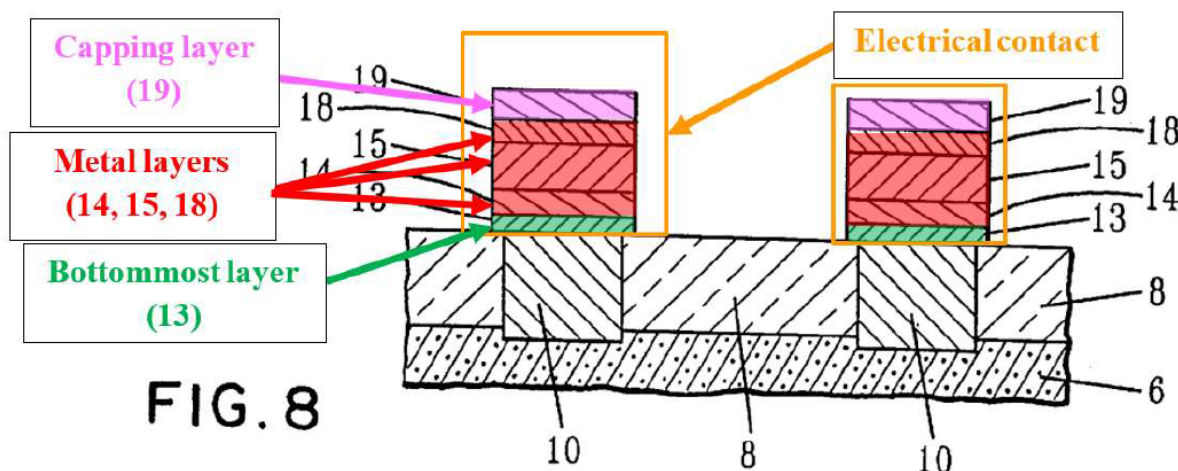
209. Petitioner and Dr. Zhao do not describe their Usui-Yu-Sugimoto combination in sufficient detail to establish obviousness. Petitioner and Dr. Zhao provide *no* details regarding which layers or specific components from which references (Usui, Yu, and Sugimoto) are incorporated into Petitioner's combination, where those layers or specific components would go in the combination, and what the thicknesses of the relevant layers would be after the references are combined. Petitioner's and Dr. Zhao's failure to reveal these *basic* details defeats any showing of obviousness, because, for example, those details are

needed to confirm whether Usui-Yu-Sugimoto meets the thickness limitations in independent claims 1 and 13.

210. The closest that Petitioner and Dr. Zhao get to describing their actual combination is the contention is that “[a] POSITA would have been motivated to implement the contact of Usui-Yu as a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide improved current flow (i.e., enhanced electromigration) and Sugimoto, like Yu, also teaches the use of III-V semiconductor devices.” Petition, 31; EX-1002 (Zhao Dec.), ¶144. As an initial matter, this appears to be inconsistent with Petitioner’s and Dr. Zhao’s earlier description of “the contact of Usui-Yu” that involves adding Yu’s insulator below Usui’s interconnect metallization structure (Petition, 19-20; EX-1002 (Zhao Dec.), ¶¶112-114), discussed above in Section IX.B.2. Dr. Zhao agrees that an insulating layer would prevent the metal layers from forming an ohmic contact, as Dr. Zhao would appear to concede. *See* EX-1002 (Zhao Dec.), ¶56.

211. Moreover, even assuming Yu’s gate insulator layer is *not* present in Usui-Yu-Sugimoto – which is impossible to confirm given Petitioner’s and Dr. Zhao’s silence regarding even the basic contours of their Usui-Yu-Sugimoto combination – Petitioner and Dr. Zhao completely fail to explain how Usui’s interconnect metallization structure (layers 13-15 and 18-19) *could* have been modified to make ohmic contact with Usui’s “semiconductor wafer” in the first

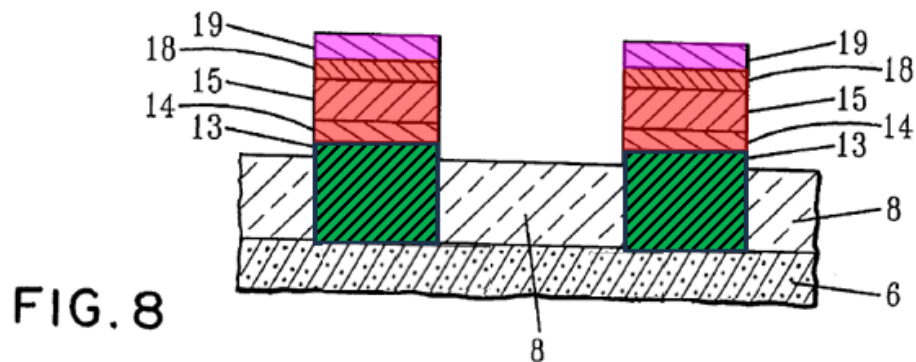
place, given the presence of “insulator 8,” which separates layers 13-15 and 18-19 from semiconductor 6, as shown below.



Petition, 11 (Petitioner’s Annotations to EX-1004 (Usui), Fig. 8).

212. This failure is particularly egregious because, as I discussed above in Section VI.A (§§48-57), forming an ohmic contact on a group III-V semiconductor device was not trivial when it involves a new contact “recipe,” as would be the case when attempting to use Usui’s interconnect metallization structure (layers 13-15, 18-19) for ohmic contact. Moreover, Usui does not teach the use of power electrodes, ohmic contacts, group III-V semiconductors, or even transistors – all of which Dr. Zhao readily admits. Thus, Petitioner’s argument appears to be that there was somehow reason to modify Usui in an unexplained manner, towards a specific purpose for which Usui’s interconnect metallization structure was never even intended.

213. To the extent Petitioner and Dr. Zhao are suggesting that a POSA would have modified Usui's layer 13 to be made thicker and replace contact metal 10, as shown below – so that layer 13 extended through the insulator 8 and directly contacted semiconductor 6 – that would not meet the requirement that the capping layer have “a thickness greater than that of a bottommost layer of said plurality of metal layers,” as recited in claims 1 and 13. To illustrate, I have provided a modified version of Usui's Figure 8 that shows layer 13 extending through the insulator 8 to reach and contact semiconductor 6.



Usui, Fig. 8 (Modified)

EX-1004 (Usui), Fig. 8 (annotated to reflect Petitioner's apparent modification in view of Yu and Sugimoto). As can be seen above, in this scenario, capping layer 19 (pink) would not have a thickness greater than layer 13 (green).

214. By not addressing precisely how a POSA would have modified Usui's teachings Petitioner and Dr. Zhao have not established that a POSA would have modified Usui's teachings in a way that would meet the claimed combinations.

ii. Petitioner Fails to Establish Any Reason to Modify Usui Based on Yu and Sugimoto in the Claimed Manner

215. Petitioner and Dr. Zhao allege that Sugimoto discloses a group III-V semiconductor device “[l]ike Yu,” Sugimoto is analogous to the ’562 Patent, and that ohmic contacts were well-known, important components of a semiconductor device. Petition, 29-31; EX-1002 (Zhao Dec.), ¶¶140-144. These are not reasons why a POSA would have modified Usui in the manner claimed.

216. Dr. Zhao trivializes a complex field. As I discuss in Section VI.A, the way in which particular materials would interact in the context of a metal-semiconductor junction was difficult to predict. As one reference put it, fabrication of ohmic contacts was “still more art than science.” EX-1017 (Kramer), 31 (Page 38 of 151); *see also* EX-1017 (Kramer), 51 (Page 58 of 151) (“Literature shows that the actual mechanism of Ohmic contact formation is still subject of discussion and yet to be understood.”). This is because, for example, “[i]f a metal is placed into contact with such a semiconductor, the physics of the junction are not governed by the bulk properties of the metal and semiconductor material but by the properties of the surface boundaries and primarily those of the semiconductor surface.” EX-1017 (Kramer), 12 (Page 19 of 151). Thus, by relying on “ohmic contacts” being “well-known, important components of a semiconductor device,” Petitioner and Dr. Zhao disregard the many well-

established challenges in finding suitable materials to function as an ohmic contact in a group III-V semiconductor device. Sugimoto does not offer any insight into those challenges other than to suggest an ohmic contact *different from* Petitioner's proposed combination. EX-1007 (Sugimoto), 11:12-20.

217. Petitioner and Dr. Zhao provide scant reasoning for combining the teachings of Usui, Yu, and Sugimoto in a manner that allegedly meets claims 10 and 15. Petition, 31; EX-1002 (Dr. Zhao Dec.), ¶144. Petitioner and Dr. Zhao only allege that a POSA “would have been motivated to implement the contact of Usui-Yu as a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide improved current flow (i.e., enhanced electromigration) and Sugimoto, like Yu, also teaches the use of III-V semiconductor devices.” Petition, 31; EX-1002 (Dr. Zhao Dec.), ¶144. I disagree.

218. As noted previously, Petitioner badly misunderstands Usui's reference to electromigration. Electromigration does not refer to enhancement of current flow (*i.e.*, the flow of charge carriers, such as electrons) as Petitioner assumes; electromigration instead has to do with the problem when excessive current displaces atoms of a conductive material, producing hillocks and other structural deformities in the materials. *See, e.g.*, EX-2029 (Howard), 1:27-45 (“The term electromigration refers to the current induced mass transport which occurs in a conductive material maintained at an elevated temperature and through which

current is passed wherein atoms of conductor material are displaced as a result of the combined effects of direct momentum exchange from the moving electrons and the influence of the applied electric field.”); EX-2026 (Zhao Dep.), 13:23-14:9, 53:18-54:25; EX-1004 (Usui), 1:30-34 (“Migration of aluminum atoms into the underlying silicon can interfere with the performance and reliability of the resulting integrated circuit.”), 1:35-41 (“As the demand increases for scaling down the dimensions of the interconnection lines and for increasing the current density, overcoming, or at least minimizing, electromigration and hillock growth is essential.”); EX-2030 (Jaeger), 157; EX-2031 (Ohring), 380–381. As discussed in Section VI.C, this problem is associated with interconnect structures, which are designed to carry current over distances to a large number of devices. As discussed, Ohmic contacts have very different challenges from interconnects. *See, e.g.*, EX-1017 (Kramer), 2-3 (Pages 9-10 of 151).

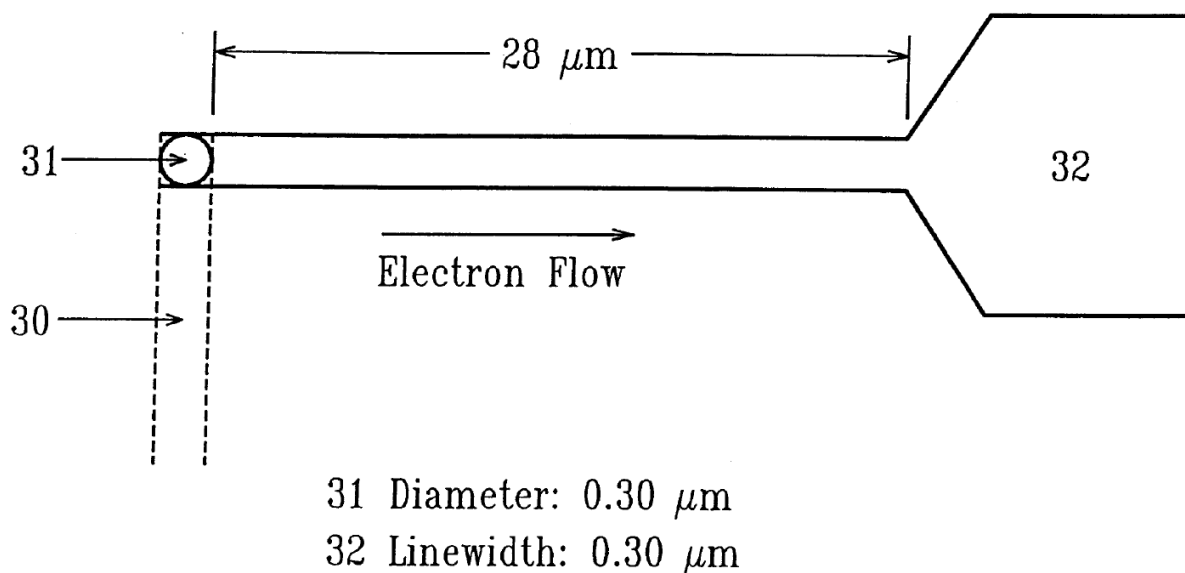
219. A POSA would not have sought to “enhance” electromigration as Petitioner alleges. Petition, 31. POSAs would have instead sought “improvement in the electromigration characteristics” of “electrical connections and wiring” by *reducing* electromigration. EX-1004 (Usui), 1:17-20, 2:33-39. Petitioner’s own expert, Dr. Zhao, agrees. EX-2026 (Zhao Dep.), 13:23-14:9 (a “common way to, to mitigate, to improve the electromigration is to putting the diffusion barrier

layer.”), 53:18-54:25 (“...it is very important to have this diffusion barrier layer” to “prevent the electromigration”).

220. Usui does not teach “improved current flow” “i.e., enhanced electromigration” as Petitioner alleges. Usui instead teaches, in the context of interconnects, the desire for “*overcoming, or at least minimizing*, electromigration and hillock growth.” EX-1004 (Usui), 1:35-41; *see also id.*, 1:17-20, 2:33-39; EX-2026 (Zhao Dep.), 13:23-14:9, 53:18-54:25; Section VI.C. POSAs were well-aware that electromigration was a concern for wiring of the type described by Usui, which can experience high current density.

221. Petitioner submits no evidence establishing that electromigration was even a concern for a transistor power electrode, let alone that any electromigration concerns for a power electrode would be solved by applying Usui’s teachings for wiring. Usui’s teachings are not directed to improving current flow that “flow[s] into and out of a semiconductor material” (Pet., 30; EX-1002 (Zhao Dec.), ¶¶57, 143)—i.e., the type of current flow that would occur in Sugimoto’s ohmic contacts. EX-1007 (Sugimoto), 9:48-50. Instead, Usui teaches that its interconnect metallurgy structure is directed to solving a problem associated with a current flow along the length of an interconnect (disposed, e.g., parallel to semiconductor material), as opposed to flowing into and out of the semiconductor. EX-1004

(Usui), 7:3-32, FIG. 11 (reproduced below, illustrating “electron flow” during electromigration tests of its disclosed metal film stack).



EX-1004 (Usui), FIG. 11. And to the extent relevant to the Usui-*Yu*-Sugimoto combination, a POSA would not have expected high current density in *Yu*’s gate electrode, because the gate in a MOS device (including in CMOS devices) controls the transistor through an electrical field across a gate insulator *without current flowing through the gate electrode*. *E.g.*, EX-1011 (Mishra), 356 (Page 380 of 583) (“It is important to isolate the gate from the channel so that no current flows into the gate.”); *see also id.*, 434-36 (Pages 458-60 of 583), 454-57 (Page 478-81 of 583). Thus, neither Petitioner nor Dr. Zhao establish that Usui’s approach to mitigating electromigration was applicable to transistor electrodes like the ones taught in *Yu* and Sugimoto.

222. Petitioner and Dr. Zhao further contend that the Usui-Yu-Sugimoto combination “is the result of combining prior elements according to known techniques to a known device ready for improvement.” Petition, 19; EX-1002 (Zhao Dec.), ¶144. Petitioner and Dr. Zhao have not established that there was anything “known” about attempting to convert Usui’s interconnect structure – which makes no contact with a silicon semiconductor – to become a power electrode making ohmic contact with a group III-V semiconductor. Petitioner and Dr. Zhao also never explain which device in Ground 4’s combination was allegedly “ready for improvement.” For example, Petitioner and Dr. Zhao fail to show that the proposed combination would have improved Sugimoto’s HEMT because there is no evidence Sugimoto’s HEMT source and drain electrodes suffer from an electromigration problem that would be solved using Usui’s techniques.

223. Further, Petitioner and Dr. Zhao never explain how *Usui’s* interconnect metallization structure would have been improved by “implement[ing] the contact of Usui-Yu as a power electrode” (Petition, 31; EX-1002 (Zhao Dec.), ¶144) particularly since Usui does not disclose any device having a power electrode. In fact, Dr. Zhao’s proposed combination does not “improve” Usui – it *changes* the function of Usui’s interconnect metallization structure to serve a very different purpose from what Usui intended: as wiring that

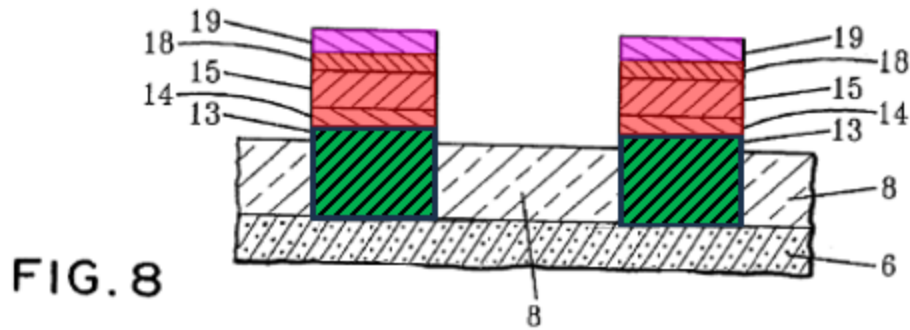
is part of an “interconnect circuit” connecting devices in a semiconductor circuit.

See EX-1004 (Usui), 1:5-12, 4:10-15.

iii. Dr. Zhao Fails to Establish a Reasonable Expectation of Success

224. For reasons similar to the ones I discussed for Ground 3 (see my analysis in Section IX.B.3.a.iii), Petitioner and Dr. Zhao fail to establish a reasonable expectation of success in modifying Usui, based on Yu and Sugimoto.

225. Petitioner’s proposed combination involves Usui’s interconnect metallization structure (layers 13-15 and 18-19) with a refractory metal nitride capping layer with “a thickness greater than that of a bottommost layer of said plurality of metal layers,” as required by Limitations [1c] and [13c]. Petitioner and Dr. Zhao then propose modifying Usui’s interconnect metallization structure to make ohmic contact with a III-V semiconductor as required by claims 10 and 15, without addressing whether Usui’s metal layers would have changed when attempting to repurpose Usui’s interconnect structure. See below for an example of what Petitioner’s modification may have looked like, where layer 13 is extended through insulating layer 8 in order to allow Usui’s interconnect metallization structure to directly contact the semiconductor:



EX-1004 (Usui), Fig. 8 (annotated to reflect Petitioner’s apparent modification in view of Yu and Sugimoto).

226. To the extent Dr. Zhao suggests that Usui-Yu’s alleged electrical contact could simply be used *without any changes* to form an ohmic contact on a semiconductor, no evidence supports that notion. Dr. Zhao trivializes a complex field. As I discuss in Section VI.A, the way in which particular materials would interact in the context of a metal-semiconductor junction was difficult to predict. As one reference put it, fabrication of ohmic contacts was “still more art than science.” EX-1017 (Kramer), 31 (Page 38 of 151); *see also* EX-1017 (Kramer), 51 (Page 58 of 151) (“Literature shows that the actual mechanism of Ohmic contact formation is still subject of discussion and yet to be understood.”). This is because, for example, “[i]f a metal is placed into contact with such a semiconductor, the physics of the junction are not governed by the bulk properties of the metal and semiconductor material but by the properties of the surface boundaries and primarily those of the semiconductor surface.” EX-1017 (Kramer), 12 (Page 19 of

151). Thus, by relying on “ohmic contacts” being “well-known, important components of a semiconductor device,” Petitioner and Dr. Zhao disregard the many well-established challenges in finding suitable materials to function as an ohmic contact in a group III-V semiconductor device.

227. Contrary to the plug-and-play view offered by Dr. Zhao, in reality, laboratories tended to have their own favorite recipes for ohmic contact formation which involve particular metal or alloy systems, particular deposition methods, and particular forms of heat treatment (anneal). EX-1017 (Kramer), 31 (Page 38 of 151). That is understandable because of the tremendous work that goes into finding a single suitable recipe. A POSA understood this work would have required significant changes to the layers – in their materials and thicknesses – because ohmic contacts are closely tailored to the semiconductor, like a lock and key. Petitioner fails to account for these changes, and fails to show that the alleged electrical contact of Usui-Yu-Sugimoto would meet claims 1 and 13 after making the necessary changes.

228. Sugimoto does not offer any insight into addressing the many challenges of ohmic contact formation other than to suggest an ohmic contact *different from* the proposed combination. EX-1007 (Sugimoto), 11:12-20. As discussed in EX-1017 (Kramer), “it should in principle be possible to obtain a contact with a negative barrier height (which should behave as an Ohmic contact)

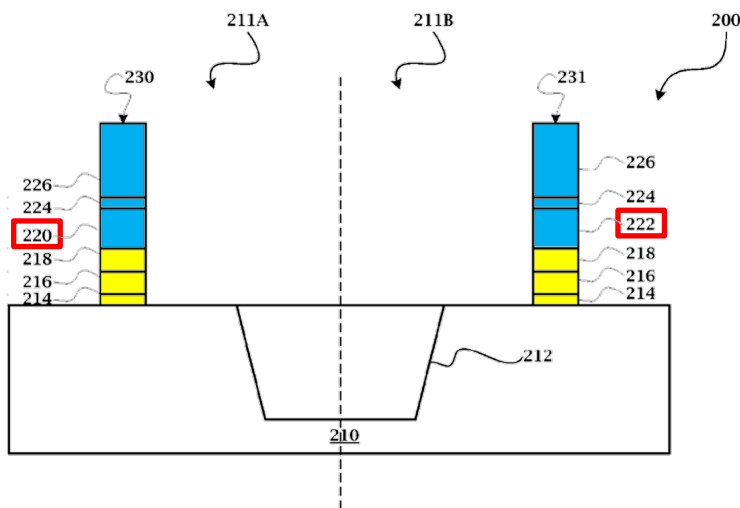
by finding a metal with a work function less than the work function of an n-type semiconductor or greater than the work function of a p - type semiconductor.” EX-1017 (Kramer), 32 (Page 39 of 151). Unfortunately for those in this field, it turns out that there are very few metal semiconductor combinations that have been proven to satisfy this condition. *Id.* Dr. Zhao seems to have given no consideration to whether Usui’s interconnect structure could prove suitable for making ohmic contact with a group III-V semiconductor device and he has not established that a POSA would have had a reasonable expectation of success (or any expectation of success) in arriving at the claimed combination.

C. Ground 5 (Obviousness over Yu and Usui) Fails

229. As I discussed above in Section VIII.B (§§106-114), Yu is directed to a particular technique for forming a metal gate electrode for a complementary metal-oxide-semiconductor. Yu was motivated by “a desire to replace the gate oxide and *polysilicon gate electrode* [in conventional CMOS devices] with a high-k gate dielectric and *metal gate electrode* to improve device performance as feature sizes continue to decrease.” EX-1005 (Yu), [0004]. Yu needed to address issues associated with “metal, metal carbide, and/or metal nitride...gate electrode...materials [that] provide insufficient work function values and present thermal stability issues...” *Id.* Yu addressed the above-discussed problems by

providing a CMOS device whose two transistors have metal gate electrodes formed from different metal layers. EX-1005 (Yu), [0030], [0033], Fig. 2E.

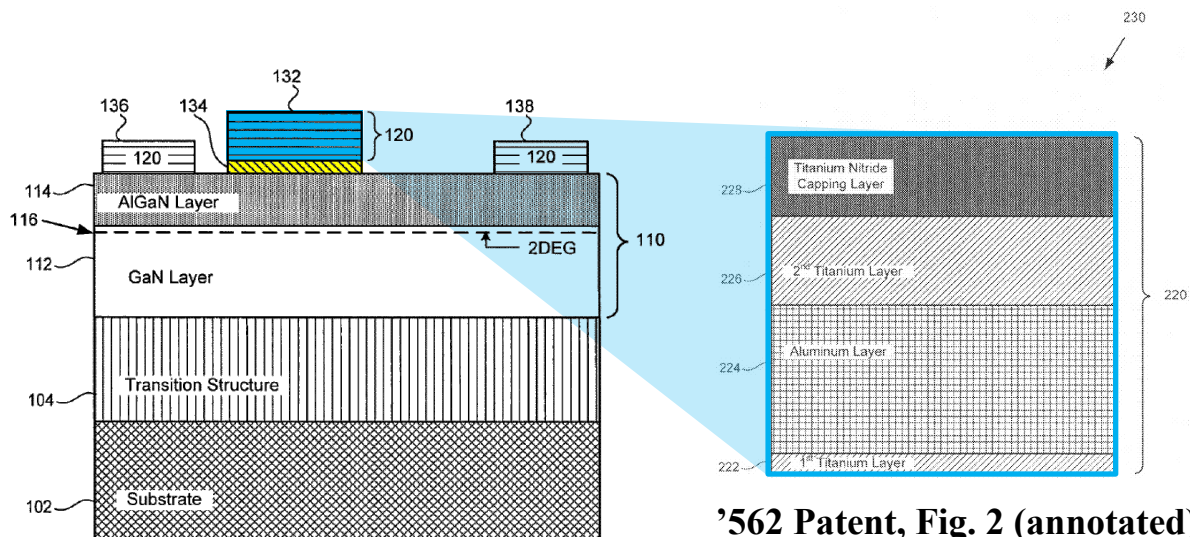
230. In particular, Yu discloses a first gate electrode that includes “first metal layer 220 compris[ing] a material with a first work function” and a second gate electrode that includes “second metal layer 222 compris[ing] a material with a second work function.” EX-1005 (Yu), [0030]; *see also id.*, [0033]. These layers can be seen in Figure 2E, annotated below:



Yu, Fig. 2E (annotated). As discussed, Yu provided “different work functions” for the two CMOS gate electrodes shown above by providing different work functions for metal layers 220 and 222. Yu, [0004], [0030], [0033].

231. Yu’s electrodes are insulated gate electrodes. As I discussed above in Section VII.A, the ’562 Patent discloses an insulated gate electrode in which gate

electrode 132 (blue) is stacked with insulating layer 134 (yellow) as shown in Fig. 1 (below left). EX-1001, 2:58-60 (“gate electrode 132”), 3:19-35 (same).

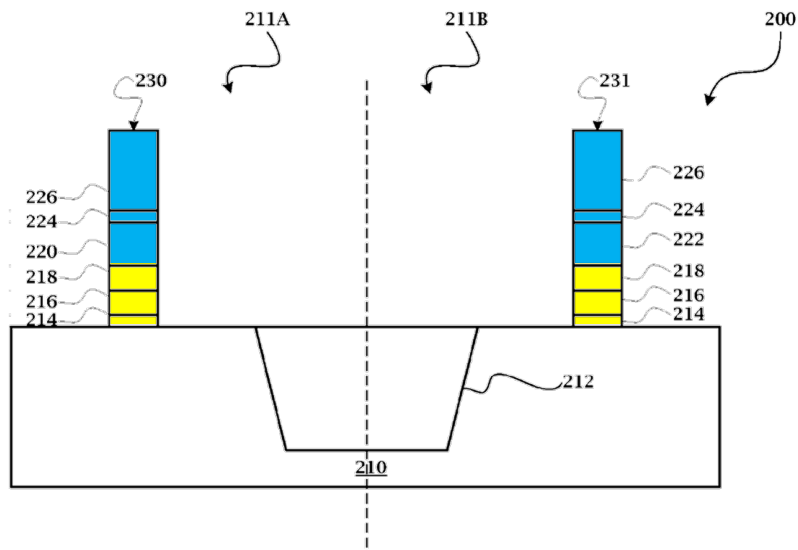


'562 Patent, Fig. 1 (annotated)

'562 Patent, Fig. 2 (annotated)

The electrode stack in Fig. 2 of the '562 Patent (above right) forms “gate electrode 132, in Fig. 1” (above left). EX-1001, 3:40-43 (Fig 2’s “[e]lectrode stack 220” “corresponds to electrode stack 120 in FIG. 1”). Thus, a POSA understood that “electrode stack” in the '562 Patent for a gate electrode *includes only* the metal layers forming the electrode and not other layers like insulating layer 134, which are stacked with, but are not part of, the gate electrode.

232. Like the '562 Patent’s insulated gate electrode (blue above), which is stacked with another layer (yellow above), Yu’s gate electrodes (blue below) are stacked with other layers (yellow below).



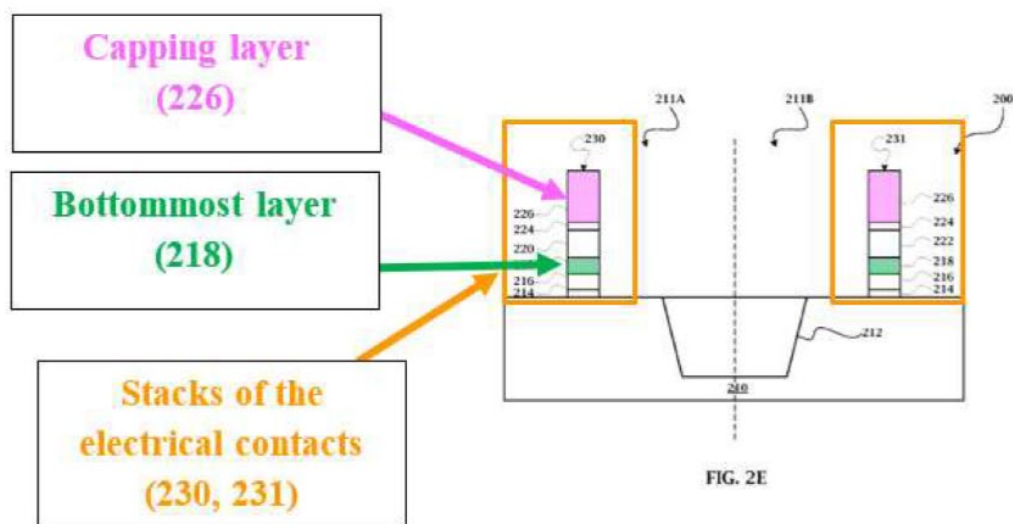
Yu (EX-1005), Fig. 2E (annotated).

233. Yu refers to the entire stack as a “metal gate stack.” Yu, [0038]-[0039]. As noted, Yu indicates that metal gate stacks 230 and 231 have different metal layers (220 and 222, respectively) with different work functions, but their structures are otherwise identical. Each stack includes two oxide layers 214, 216 (yellow above) atop the semiconductor (Yu, [0028]-[0030]), a “diffusion barrier layer” 218 separating the metal layer (220 or 222, blue above) from the oxide layers to prevent material from diffusing between the metal and oxide layers (Yu, [0029]), a capping layer 226 (Yu, [0036]), and a diffusion barrier layer 224 separating the capping layer from the metal layer (220 and 222) to prevent diffusion (Yu, [0035]).

1. Petitioner Fails to Establish that Yu’s Diffusion Barrier/Protection Layer 218 is a Layer of Yu’s Electrode Stack

234. The Challenged Claims all require an electrical contact comprising “an electrode stack including a plurality of metal layers and a capping layer,” where “the capping layer...is thicker than a *bottommost layer* of the plurality of metal layers of the electrode stack.” Limitations [1pre]-[1c] and [13pre]-[13c].

235. For Ground 5, Petitioner and Dr. Zhao say that Yu’s layer 218 meets the claimed “bottommost layer.” Petition, 35-37, 43-46; *id.*, 44 (annotating Yu’s Fig. 2E as reproduced below); Zhao, ¶152.



Petition, 44 (Petitioner’s Annotations to Yu, Fig. 2E); Zhao, ¶165. According to Yu, layer 218 is a “diffusion barrier/protection layer” that is “optional” and “may be omitted.” Yu, [0029].

a. Petitioner's Conclusion that Yu's Diffusion Barrier Layer is Part of an Electrode Stack is Unsupported

236. Diffusion barrier layers were well-known. *See e.g.*, EX-2002 (Meng), [0057] (“The gate electrode 629 is formed over the barrier layer 626. The barrier layer is adapted to prevent dopants, such as boron, in the gate electrode 629 from diffusing into the gate oxide layer 627, the source/drain 623 and the source/drain 625.”), [0058] (“In an embodiment, a further barrier layer 631 is formed... over the gate electrode 629.”), Fig. 6 (reproduced below).

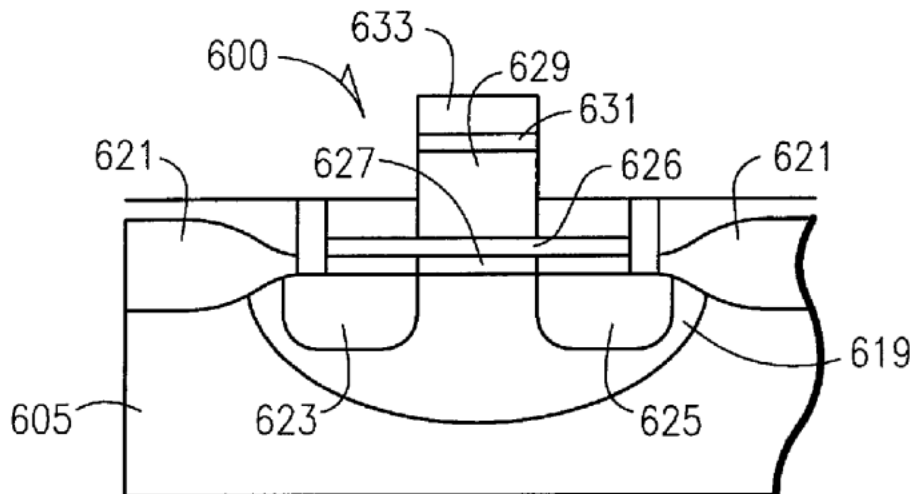


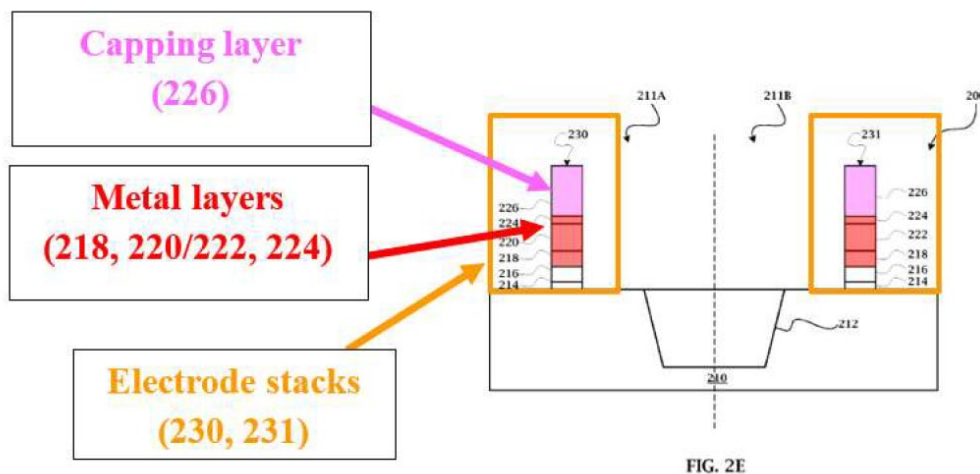
Fig. 6

EX-2002 (Meng), Fig. 6. As the above disclosures confirm, diffusion barrier layers were known to be disposed between two layers of material to prevent those materials (i.e., the materials separated by the diffusion barrier layer) from diffusing into one another. EX-2002 (Meng), [0057]-[0058], Fig. 6.

237. A POSA understood that diffusion barrier layers had been used to separate a gate electrode from an oxide layer, just like Yu's layer 218 does. EX-2002 (Meng), [0057]-[0058], Fig. 6. A POSA also understood that Yu's barrier layer is *not part of the gate electrode* – which is confirmed by the descriptions in, e.g., EX-2002 (Meng), which corroborate the understanding that gate electrodes are different from the diffusion barrier layers that separate the gate electrode from other elements. See EX-2002 (Meng), [0057]-[0058], Fig. 6. A POSA understood Yu's barrier layer separates Yu's gate electrode from Yu's oxide layer.

b. Neither Petitioner Nor Dr. Zhao Explain What the Term “Electrode Stack” Means

238. For Ground 5, the Petition and Dr. Zhao allege, without explanation, that Yu's entire “metal gate stack” (230 or 231) is an “electrode stack.” Petition, 42; EX-1002 (Zhao Dec.), ¶162. The Petition and Dr. Zhao's annotations to Yu Figure 2E illustrating this mapping is reproduced below:



Petition, 42 (Petitioner’s annotations to Yu, Fig. 2E); EX-1002 (Zhao Dec.), ¶162.

As I discussed above in ¶¶76-79, neither Petitioner nor Dr. Zhao ever explain the “plain meaning” of “electrode stack,” and based on my review of Dr. Zhao’s testimony, it appears that he gave no weight at all to the word “electrode” in the term “electrode stack.” As I have discussed, I disagree that this is the right way to interpret the term “electrode stack.” The word “electrode” should be given weight.

c. No Evidence Supports the Assertion that Yu’s Entire Metal Gate Stack is an Electrode Stack as Claimed

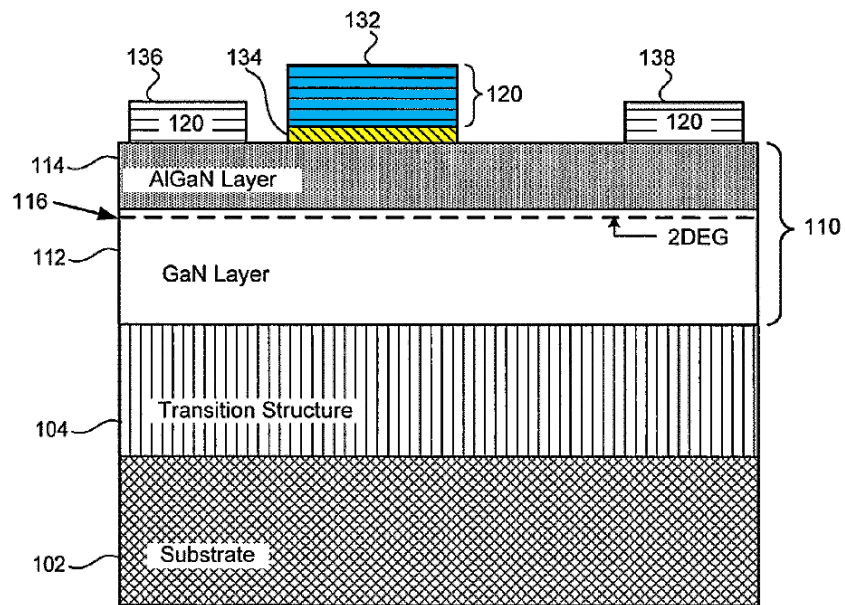
239. I also found no evidence supporting Petitioner’s and Dr. Zhao’s conclusion that Yu’s *entire* metal gate stack (230 or 231) is an electrode stack, as claimed. Petition, 42; EX-1002 (Zhao Dec.), ¶162.

240. For Limitation [1a], the Petition cites Yu, [0029] and [0035]-[0036]. Petition, 42. I reviewed those paragraphs, and found that none of those paragraphs characterizes Yu’s entire metal gate stack (230 or 231) as an *electrode* stack. The Petition also cites to “Zhao ¶162” (Petition, 42), where Dr. Zhao simply repeats the Petition’s Limitation [1a] argument and citations without adding any technical analysis or evidence. This approach is consistent with Dr. Zhao’s apparent belief (as I discussed above in ¶¶76-79), that he did not need to give weight to the word “electrode” or establish *why* Yu’s metal gate stacks 230 and 231 are “*electrode* stacks” in the first place.

241. Instead, Dr. Zhao and the Petition focused only on the characteristics of individual layers. For example, the Petitioner argues that (1) Yu's oxide layers 214 and 216 at the bottom of Yu's metal gate stacks 230 and 231 "cannot be the bottommost layer of '[said] plurality of metal layers' because they are dielectric layers not 'metal layers'" (Petition, 44-45; EX-1002 (Zhao Dec.), ¶166); and (2) Yu's diffusion barrier/protection layer 218 is metal. Petition, 42; EX-1002 (Zhao Dec.), ¶162. But even if those assertions were accepted as true, all that would show is that Yu's diffusion barrier layer 218 is metal, and that Yu's oxide layers 214 and 216 are not metal. That does not establish Yu's diffusion barrier layer 218 is specifically a layer of Yu's *electrode stack*, which is what is required by limitations [1a] and [1c]. See Limitation [1a] ("an *electrode stack* including a plurality of metal layers"); Limitation [1c] ("a bottommost layer of *said* plurality of metal layers"). A POSA understood that to meet Limitation [1c], the "bottommost layer of said plurality of metal layers" needs to be in Yu's "*electrode stack*," recited in limitation [1a].

d. The Assertion that Yu's Entire Metal Gate Stack is an "Electrode Stack" Contradicts the Intrinsic Evidence

242. As discussed above in ¶¶231-232, the '562 Patent discloses a metal gate stack sharing some similarities with Yu's metal gate stack. See '562 Patent Fig. 1 and EX-1005 (Yu) Fig. 2E Yu (both annotated below). Both stacks include a gate electrode (blue) and other layer(s) (yellow).



EX-1001, Fig. 1 (annotated).

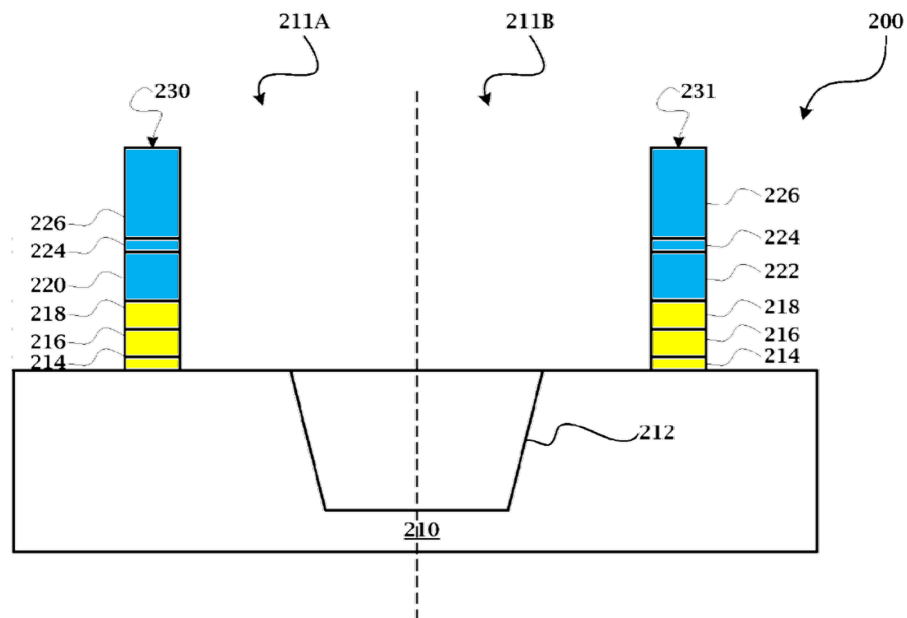
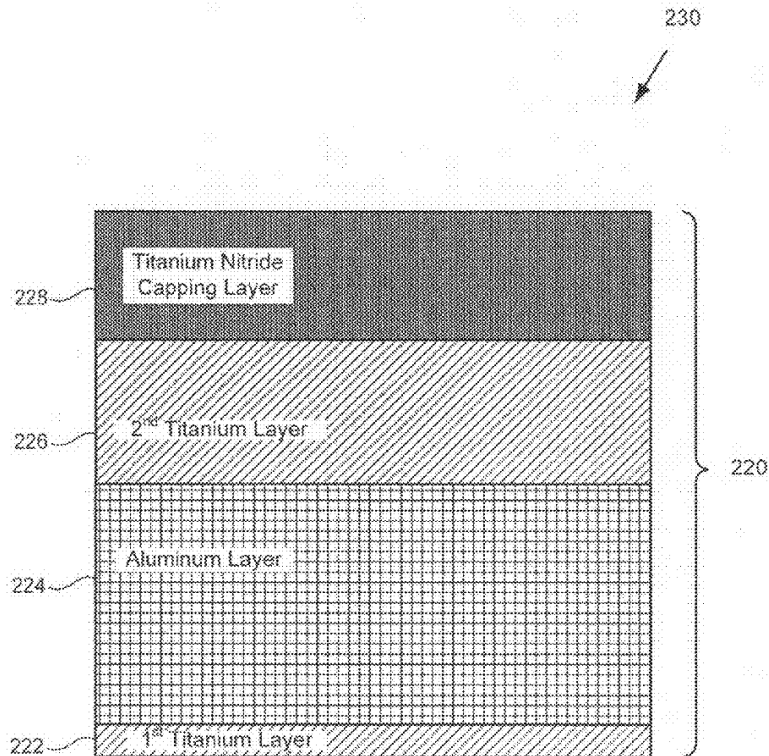


FIG. 2E

EX-1005 (Yu), Fig. 2E (annotated).

243. As I noted above in ¶231, the '562 Patent explains that Fig. 1 illustrates “gate electrode 132” stacked with “gate insulating layer 134.” EX-1001, 3:28-31. The '562 Patent specification is explicit that “electrode stack 120” for this gate electrode does *not* include gate insulating layer 134. *Id.* Fig. 1’s labelling of “electrode stack 120” makes clear that the electrode stack is comprised of the stacked metal layers that form the gate electrode 132 and does *not* include gate insulating layer 134. Indeed, the same “electrode stack 120” is used for source and drain electrodes 136 and 138, which have no insulating layer 134. *Id.*, 3:23-25, Fig. 1. Gate insulating layer 134 “underl[ies] the electrode stack 120” rather than being part of the electrode stack. *Id.*, 3:28-31. Furthermore, Fig. 2’s “[e]lectrode stack 220” “corresponds to electrode stack 120 in FIG. 1” (*id.*, 3:42-43) and does not include an insulating layer. *Id.*, Fig. 2 (reproduced below), 3:40-43 (Fig. 2’s “[e]lectrical contact 230 may...correspond to...[the] *insulated gate electrode* 132 in Fig. 1”).



EX-1001, Fig. 2. Thus, the '562 Patent specification is clear that the “electrode stack” includes only stacked layers that form the electrode. If the electrode is stacked with other layers, those other layers are not part of the electrode stack.

244. The above intrinsic evidence – which neither Petitioner nor Dr. Zhao address or discuss – directly refutes their conclusion that Yu’s *entire* metal gate stack is an “electrode stack” as claimed. Petition, 42. Yu’s entire metal gate stack (230 or 231) cannot be an “electrode stack” as claimed because it includes a dielectric layer (214 or 216) that performs the same insulating function as insulating layer 134 in the '562 Patent. EX-1005 (Yu), [0022], [0027]-[0028], [0039]. Indeed, the '562 Patent expressly discloses that its gate insulating layer 134 may be formed from silicon dioxide (SiO₂) (EX-1001, 3:28-31), which is a

“silicon oxide” – the same material referenced in Yu for dielectric layer 214. EX-1005 (Yu), [0027]; EX-2003 (Sachs), [0130] (confirming “silicon dioxide” is a “silicon oxide”); EX-2004 (Quirk), 225-230 (describing silicon oxide films). The intrinsic evidence therefore makes clear to a POSA that Yu’s oxide layer is distinct from and not part of the claimed “electrode stack.” Thus, Petitioner’s and Dr. Zhao’s assertion that Yu’s *entire* metal gate stack 230 or 231 is an “electrode stack” is wrong.

e. Ground 5 Fails Because Yu’s Diffusion Barrier/Protection Layer 218 is Not a Layer of Yu’s Electrode Stack

245. For the reasons I discussed above in ¶¶236-244, Petitioner and Dr. Zhao fail to identify Yu’s “electrode stack,” or establish that Yu’s diffusion barrier/protection layer 218 is even among the layers of Yu’s “electrode stack,” let alone its bottommost metal layer. Petitioner and Dr. Zhao thus do not (and cannot) establish that Yu discloses its capping layer having “a thickness greater than that of a bottommost layer of said plurality of metal layers” included in the “electrode stack,” as required in limitations [1a]-[1c] and [13a]-[13c].

2. Petitioner Also Fails to Show that Yu and Usui Render Obvious an Electrical Contact with a Capping Layer of a Refractory Metal Nitride that is Thicker Than Yu’s Alleged Bottommost Layer

246. The Challenged Claims all require a capping layer that is *both* (1) formed from a “refractory metal nitride” or from TiN or TaN (limitations [1b] and

[13b]); and (2) thicker than the electrode stack's bottommost metal layer (limitations [1c] and [13c]). Petitioner and Dr. Zhao fail to establish that Yu and Usui render obvious a capping layer of an electrical contact that meets both requirements.

247. As I discussed above in ¶112, Yu discloses numerous materials for forming a capping layer. However, Petitioner and Dr. Zhao both admit that Yu does not “expressly disclose[]” that capping layer 226 is thicker than the alleged bottommost metal layer (layer 218) when capping layer 226 is formed from a material meeting any Challenged Claim. Petition, 38 (“Yu expressly discloses every element of claims 1 and 13 except a *refractory metal nitride capping layer* having a thickness greater than that of a bottommost layer (claim element [1c]).”); EX-1002 (Zhao Dec.), ¶155.

248. Absent such a disclosure, Petitioner and Dr. Zhao point to Yu's thickness for the capping layer when formed from polysilicon, which Petitioner and Dr. Zhao concede is “*not* a refractory metal nitride as is stated in claims 1 and 13.” Petition, 38; EX-1002 (Zhao Dec.), ¶155.

249. Petitioner and Dr. Zhao then allege that the Challenged Claims are rendered obvious for two alternative reasons: (1) a POSA would have been motivated to make Yu's capping layer the same thickness when formed from a refractory metal nitride as when formed from polysilicon, and (2) Usui would have

motivated a POSA to make Yu's refractory metal nitride capping layer thicker than Yu's diffusion barrier/protection layer 218. Petition, 38-39; EX-1002 (Zhao Dec.), ¶¶155-158. As detailed below, neither of Petitioner's and Dr. Zhao's argument is supported by the evidence.

a. Yu Does Not Disclose a Refractory Metal Nitride Capping Layer Thicker Than Yu's Alleged Bottommost Layer 218

250. Yu describes many materials or "combinations thereof" that could form capping layer 226. EX-1005 (Yu), [0036]. Petitioner and Dr. Zhao cite Yu's disclosure that capping layer 226 can be titanium nitride or tantalum nitride because those are refractory metal nitrides. Petition, 42; EX-1002 (Zhao Dec.), ¶163. But, based on my review of Yu, Yu never discloses capping layer 226's thickness when it is formed from either of those materials. Neither Petitioner nor Dr. Zhao ever allege that Yu discloses this information.

251. Petitioner and Dr. Zhao both state that "[w]hile Yu discloses the **capping layer** is *preferably* 600Å and the **bottommost layer** 20Å (i.e., the **capping layer** is *preferably* thicker than the **bottommost layer**), this disclosure is made with respect to the **capping layer** being polysilicon (Yu, [0036], [0040]), which is not a **refractory metal nitride** as is stated in claims 1 and 13." Petition, 38 (emphasis original); EX-1002 (Zhao Dec.), ¶155. I note that the 600Å thickness described in Yu is the *only* capping layer thickness that Petitioner and Dr. Zhao

cite. That thickness is for polysilicon, which Petitioner and Dr. Zhao admit does not meet any Challenged Claim. Petition, 38 (emphasis original); EX-1002 (Zhao Dec.), ¶155; EX-1005 (Yu), [0036]. Petitioner and Dr. Zhao notably do not address or appear to consider Yu’s disclosure of a significantly different thickness (about 50-1,000 Å and “preferably about 200 Å”) when Yu’s capping layer 226 is an “aluminum-based, tungsten, or copper material.” EX-1005 (Yu), [0036].

b. Petitioner’s Assertion that a POSA Would Have Used the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Capping Layer is Unsupported

252. Petitioner alleges a POSA would have “replace[d] Yu’s polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed thicknesses because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation [*sic*].” Petition, 38 (highlighting added); EX-1002 (Zhao Dec.), ¶155. For ease of review, I have highlighted yellow and blue the two distinct assertions that Petitioner and Dr. Zhao make in this sentence.

253. For the purposes of this analysis, I do not dispute Petitioner’s assertion (highlighted yellow above) that a POSA had reason to use titanium nitride or tantalum nitride to form Yu’s capping layer, nor that these refractory metal nitrides had known benefits, given Yu’s disclosure that these materials can be used for capping layer 226. Yu, [0036]. But Petitioner’s and Dr. Zhao’s

assertion (highlighted blue above) that a POSA would have been motivated to “us[e] the same disclosed thickness” that Yu teaches for a polysilicon capping layer when making the capping layer from a refractory metal nitride is entirely unsupported, as discussed below.

i. Petitioner Fails to Show There Was Any Reason to Choose the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Capping Layer

254. The only reason Petitioner says that a POSA would have “been motivated to replace Yu’s polysilicon with either its disclosed titanium nitride or tantalum nitride” is highlighted yellow above, and reproduced here: “because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation [*sic*].” Petition, 38. Petitioner’s reference to “well-known” “benefits” of refractory metal nitrides does not address the question of *how thick* a capping layer using such materials should be. And my review of the Petition confirms that the Petition articulated no reason why a POSA would have chosen the “*same... thickness[]*” that Yu discloses for its polysilicon capping layer when the capping layer is instead formed from a refractory metal nitride.

255. The paragraphs to Dr. Zhao’s declaration that the Petition cites – EX-1002 (Zhao Dec.), ¶¶71-73, 155 – are also silent regarding reasons to choose the “same... thickness[]” that Yu discloses for its polysilicon capping layer. Of those paragraphs, only one paragraph – EX-1002 (Zhao Dec.) ¶155 – mentions anything

about layer thickness. And Dr. Zhao’s statement in that paragraph regarding layer thickness only repeats what the Petition says. Like the Petition, Dr. Zhao never articulates any specific *reason why* a POSA would have used the “*same... thickness[]*” that Yu discloses for its polysilicon capping layer when the capping layer is instead formed from a refractory metal nitride. The only reason Dr. Zhao offers is the general, unremarkable proposition that the “benefits of refractory metal nitrides are well-known.” EX-1002 (Zhao Dec.) ¶155.

256. The failure of Petitioner and Dr. Zhao to provide any reason to specifically choose the same thickness of the capping layer is especially problematic given that Yu expressly discloses that the material used to form the capping layer *significantly* impacts the thickness that should be used for the capping layer. EX-1002 (Yu), [0036]. For example, Yu discloses that when the capping layer is formed from “aluminum-based, tungsten, or copper material,” a very different “prefer[red]” thickness of “about 200 Å” should be used. 200Å is *one-third* of 600Å – the cited thickness for a polysilicon capping layer. EX-1002 (Yu), [0036]. If anything, Yu suggests that the same thickness would not be used.

ii. No Evidence Supports Petitioner’s Assertion that a POSA Would Have Chosen the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Capping Layer

257. Petitioner’s assertion that a “POSITA would have been motivated to replace Yu’s polysilicon with either its disclosed titanium nitride or tantalum

nitride using the same disclosed thicknesses” cites “Zhao ¶¶71-73, 155,” as well as EX-1025 (Bauccio), 120; EX-1026 (Preuss), 2; EX-1028 (Kim), 46, 56; EX-1023 (Suh-590), 3:39-43; EX-1024 (Chen-976), Abstract, 1:58-61; and EX-1029 (Fair), Abstract, 1:29-34, 2:47-51). Petition, 38 (highlighting added).

258. None of the cited paragraphs in Dr. Zhao’s declaration supports the assertion (highlighted blue above) that a POSA would have used Yu’s *same* thickness for a polysilicon capping layer, when the layer is formed from a refractory metal nitride. None of the paragraphs in EX-1002 (Zhao Dec.) ¶¶71-73 ever refer to the thickness of a refractory metal nitride capping layer. And EX-1002 (Zhao Dec.) ¶155 only repeats the Petition’s assertion from the first paragraph on page 38, but adds no analysis or evidence that supports the naked conclusion that a POSA would have used the “same...thickness[]” for a refractory metal nitride capping layer that Yu teaches is preferred for *polysilicon* capping layer.

259. Moreover, just like the Petition, Zhao ¶155 never explains any *reason why* POSA would have chosen Yu’s disclosed thickness for a polysilicon capping layer when using a refractory metal nitride capping layer even though Yu discloses vastly different thicknesses for the capping layer when formed from different materials. EX-1005 (Yu), [0036] cites a capping layer thickness of 200Å when the capping layer is formed from aluminum-based, tungsten, or copper material, which is *one-third* the 600Å thickness for a capping layer formed from polysilicon.

260. None of the additional references cited by the Petition or Dr. Zhao – EX-1025 (Bauccio), 120; EX-1026 (Preuss), 2; EX-1028 (Kim), 46, 56; EX-1023 (Suh-590), 3:39-43; EX-1024 (Chen-976), Abstract, 1:58-61; and EX-1029 (Fair), Abstract, 1:29-34, 2:47-51) – supports the assertion that a POSA had a reason to use the same thickness. None of those references appears to disclose a capping layer thickness for Yu’s gate electrode, and neither the Petition nor Dr. Zhao ever suggest that they do. Thus, neither Petition nor Dr. Zhao cites any credible evidence supporting the assertion that a POSA would have chosen the “same...thickness[]” that Yu discloses for its polysilicon capping layer when the capping layer is formed from a refractory metal nitride.

iii. Petitioner Does Not Identify the Thickness of Yu’s Diffusion Barrier/Protection Layer 218 When Made of Titanium as Alleged in the Yu-USui Combination

261. Petitioner and Dr. Zhao also allege that the thickness of Yu’s diffusion barrier/protection layer 218 is 20Å. Petition, 38; EX-1002 (Zhao Dec.), ¶155. I note that the 20Å thickness that Yu teaches is for a diffusion barrier/protection layer 218 formed from titanium *nitride* (TiN). EX-1005 (Yu), [0029].

262. The Yu-USui combination does *not* use a titanium *nitride* (TiN) diffusion barrier/protection layer 218. Instead, Petitioner and Dr. Zhao allege that a “POSITA would have been motivated to use *titanium* as **diffusion barrier/protection layer 218**... in Yu’s device.” Petition, 36; EX-1002 (Zhao

Dec.), ¶152. According to Dr. Zhao, “diffusion barrier layers made of titanium were well-known by August 2009 and constituted a simple design choice depending on the application of the device.” EX-1002 (Zhao Dec.), ¶152. But a POSA understood that titanium and titanium nitride are different materials. Titanium (Ti) is a metal element. Titanium nitride (TiN) is a material formed by reacting titanium with nitrogen. The presence of nitrogen in titanium nitride fundamentally changes, e.g., the diffusion behavior compared to pure titanium, resulting in a much lower rate of, e.g., Si diffusion. The two materials thus unsurprisingly have different properties that POSAs knew would have affected their implementation as layers in or with gate electrodes like those taught in Yu.

263. Neither Petitioner nor Dr. Zhao cites any teaching in Yu of a thickness for a *titanium* diffusion barrier/protection layer 218, like the one that Petitioner and Dr. Zhao selected for their Yu-USui combination. Petition, 36. The only thickness Petitioner cites is 20Å for a TiN “embodiment.” Yu, [0029]; EX-1002 (Zhao Dec.), ¶152. I reviewed Yu and confirmed that Yu never says the cited 20Å thickness applies for the diffusion barrier/protection layer 218 for *all* materials. Instead, Yu expressly teaches that “in alternate embodiments, the diffusion barrier layer 218 comprises any suitable thickness.” EX-1005 (Yu), [0029]. My review of Yu indicates that Yu provides no teaching of a “suitable thickness” for a

titanium diffusion barrier/protection layer 218, like the one used in Petitioner's and Dr. Zhao's Yu-Usui combination. Petition, 36; EX-1002 (Zhao Dec.), ¶152.

264. Petitioner's and Dr. Zhao's assertion that Yu teaches a capping layer 226 that is thicker than its diffusion barrier/protection layer 218 is thus based on thickness values that Yu reports for *different materials for both the capping layer and the alleged bottommost metal layer* in Petitioner's Yu-Usui combination. My review confirms that Yu teaches *nothing* about the thickness of these layers when formed from the *actual* materials that are used in Petitioner's Yu-Usui combination. Yu thus simply does not teach a refractory metal nitride capping layer 226 that is thicker than a titanium diffusion barrier layer 218 as Petitioner and Dr. Zhao allege.

c. Petitioner's Alternative Argument that Usui Would Have Motivated a POSA to Make Yu's Refractory Metal Nitride Capping Layer Thicker Than Yu's Diffusion Barrier/Protection Layer Fails

265. Petitioner argues, in the alternative, that “[t]o the extent Yu does not expressly disclose a **refractory metal nitride capping layer** having a thickness greater than that of a **bottommost layer**, Usui does.” Petition, 38-39 (citing Usui's statement, at 3:29-37, about “limiting the thickness of...underlayer 13”). I disagree with Petitioner, for the reasons discussed below.

i. A Capping Layer Thicker than the Bottommost Layer of the Electrode Stack's Metal Layers is a Missing Limitation Not Taught by Yu or Usui

266. As I discussed above in Section IX.A, Petitioner's assertion that Usui's underlayer 13 is the bottommost metal layer of an *electrode stack* fails because Petitioner fails to establish that Usui's interconnect metallization structure (Usui layers 13-15 and 18-19) is an electrode stack in the first place. Usui is an interconnect, not an electrical contact with an electrode stack. In view of that and the analysis provided above regarding Yu in Sections IX.C.1, IX.C.2.a, and IX.C.2.b, *neither* Yu nor Usui teaches an electrode stack having a capping layer thicker than the bottommost layer of the electrode stack's metal layers. This is a key limitation of every Challenged Claim – *see* Limitations [1a]-[1c] and [13a]-13[c] – which Petitioner and Dr. Zhao simply *fail to show* is in the prior art.

267. To the extent Petitioner and Dr. Zhao suggests that the technology is so simple and straightforward that a POSA's common sense can supply an electrode stack having a capping layer thicker than the bottommost layer of the electrode stack's metal layers – given that the prior art does not disclose it – I strongly disagree. As I discussed in depth above in ¶¶47-61 and 69-71, which include my discussions in Section VI.A (regarding the unpredictability inherent in ohmic contact design and fabrication), Section VI.B (regarding the technical constraints associated with gate contact design), and Section VI.C.2 (regarding the complexities unique to electrical

contact formation that are not present when forming interconnects) – the formation of electrical contacts for semiconductor devices is a far from simple or straightforward matter: it is more “art” than science, and subject to significant, complex technical constraints and unpredictability.

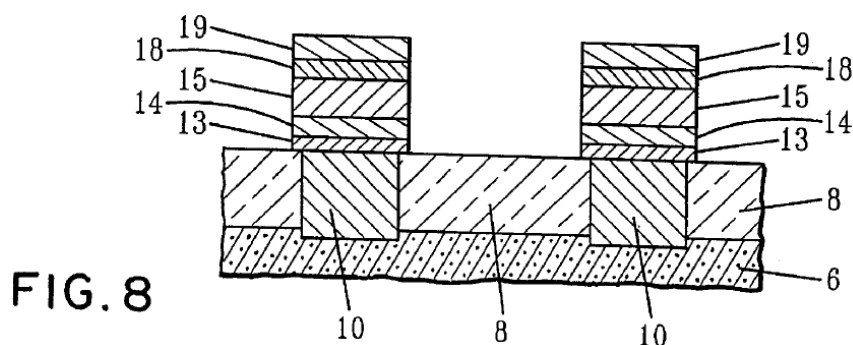
ii. Usui’s Interconnect Metallurgy Structure Would Not Have Motivated Any Change to Yu’s CMOS Gate Electrode

268. As discussed below, the motivations that Petitioner and Dr. Zhao appear to cite to support modifications to Yu’s CMOS device are not technically sound. In particular, Petitioner cites Usui’s teaching that “limiting the thickness of ... underlayer 13 ... is essential in achieving the necessary properties of the structure of *the present invention*.” Petition, 38-39 (quoting EX-1004 (Usui), 3:29-37).

269. Usui’s “present invention” is “an interconnect metallurgy structure” connected to an interplanar stud 10 that in turn contacts the device substrate. EX-1004 (Usui), 3:23-27. Yu, by contrast, has *nothing to do* with “interconnect metallurgy structure[s].” Instead, Yu is directed to gate electrodes for a CMOS device. EX-1005 (Yu), Title, [0004]-[0005], [0021]. As I discussed above in depth in Section VI.C (¶¶62-71), interconnects and electrical contacts with electrodes (such as gate electrodes) are fundamentally different and implicate fundamentally different design and implementation considerations. Petitioner and Dr. Zhao wholly fail to account for those differences, and thus fail to establish that Usui’s teachings about

how to improve interconnect metallurgy structures would have motivated a POSA to make any change to Yu's CMOS gate electrode.

270. I note also that Petitioner and Dr. Zhao rely on Usui's "underlayer 13." Petition, 38-39; EX-1002 (Zhao Dec.), ¶¶156-158. Underlayer 13 is the bottom layer of Usui's interconnect metallurgy structure and is "deposited" on "planar insulator 8 and contact stud 10." Usui, 5:11-14, Fig. 8 (below).



EX-1004 (Usui), Fig. 8. According to Usui, "by limiting the thickness of...underlayer 13, the structure and texture of" the interconnect metallurgy structure "is carefully controlled" to help limit electromigration. EX-1004 (Usui), 3:29-37, 2:33-39; Petition, 38-39; EX-1002 (Zhao Dec.), ¶156. As I discussed above in Section VI.C.1 (¶¶66-68), electromigration was a problem that POSAs understood to be applicable to interconnects, like the one in taught in Usui.

271. Petitioner's and Dr. Zhao's attempt to rely on teachings regarding Usui's interconnect "underlayer 13" to motivate changes to Yu's CMOS gate electrode diffusion barrier/protection layer 18 make little sense. In particular, Petitioner and Dr. Zhao allege that the claimed bottommost layer in the Yu-Usui

combination is met by Yu's diffusion barrier/protection layer 218. Petition, 39 ("A POSITA would have been motivated to apply known techniques of limiting the thickness of Usui underlayer 13 (bottommost metal layer) to diffusion barrier/protection layer 218 (bottommost layer) in Yu's known device..."); EX-1002 (Zhao Dec.), ¶158 (same).

272. Yu's layer 218 is *not* deposited on a contact stud and is *not* the underlayer of Yu's metal gate stack 230 or 231. Instead, the underlayer of Yu's metal gate stack is interfacial dielectric layer 214 "formed over the substrate 210." Yu, [0027], Fig. 2E (reproduced below).

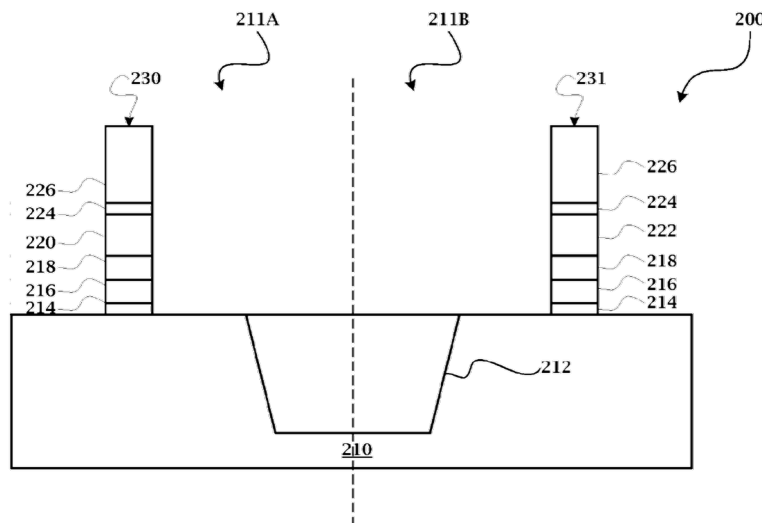


FIG. 2E

Yu (EX-1005), Fig. 2E

273. Usui's disclosure about how to "achiev[e] the necessary properties of the [interconnect metallurgy] structure of [Usui's] *present invention*" to help limit electromigration (Usui, 3:23-37, 2:33-39) would not have motivated a POSA to

make any change to Yu's CMOS gate electrode – a structure which a POSA would have understood did not implicate the same electromigration concerns that a POSA would have expected for an interconnect like the one taught in Usui. Petitioner's assertion that Usui would have motivated a POSA to make Yu's diffusion barrier/protection layer 218 thinner than Yu's capping layer 226 fails for this additional reason.

d. Petitioner's "Known Techniques" Argument

274. Petitioner asserts that Usui's teaching to limit the thickness of underlayer 13 in Usui's interconnect metallization structure would have motivated a POSA to limit the thickness of Yu's diffusion barrier/protection layer 218 because this would have been nothing more than "combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results." Petition, 39; *see also* Petition, 37; EX-1002 (Zhao Dec.), ¶58.

275. I was asked by counsel to determine whether the elements of Yu and Usui, when combined, would have the same function before and after being combined. While Petitioner's description of exactly what elements from Yu and Usui are respectively included in Petitioner's Yu-Usui combination is far from clear, I analyzed the elements that Petitioner and Dr. Zhao specifically identified – namely, Usui's underlayer 13 and Yu's diffusion barrier/protection layer 218.

276. The “function” of Usui’s underlayer 13 in Usui is to provide connection to interplanar stud connection 10. As I have discussed, according to Usui, when underlayer 13’s thickness is limited “the structure and texture of the subsequently to be applied metallic layers [of the interconnect metallurgy structure] is carefully controlled” to help mitigate electromigration. Usui, 3:29-37, 2:33-39, 5:11-14, Fig. 8; Petition, 38-39; EX-1002 (Zhao Dec.), ¶156.

277. The function of Usui’s underlayer 13 would have dramatically changed in Petitioner’s Yu-Usui combination, where the alleged bottommost metal layer is Yu’s diffusion barrier/protection layer 218. Petition, 39 (“A POSITA would have been motivated to apply known techniques of limiting the thickness of Usui underlayer 13 (bottommost metal layer) to diffusion barrier/protection layer 218 (bottommost layer) in Yu’s known device...”); EX-1002 (Zhao Dec.), ¶158 (same). Yu’s diffusion barrier/protection layer 218 does not connect to a metal stud, is not the bottommost layer of Yu’s metal gate stack, and its function is to prevent diffusion of materials between Yu’s metal layers (220, 221) and oxide layers (214, 216). EX-1005 (Yu), [0029]-[0030]; *see also* EX-2002 (Meng), [0057]-[0058], Fig. 6. A POSA would thus have understood the function of the elements combined in the Usui-Yu combination to have changed dramatically.

D. Grounds 6-7 Also Fail

1. Ground 6-7 Fall with Ground 5

278. I note that Grounds 6-7 add references to Ground 5's Yu-Usui combination to address certain dependent claims. Petition, 3; *see also* EX-1002 (Zhao Dec., ¶83). Ground 6 adds EX-1006 (Adesida) to address claims 9, 11, 14, and 16. Petition, 3. Ground 7 adds EX-1007 (Sugimoto) to address claims 10 and 15. *Id.* Neither Petitioner nor Dr. Zhao relies on either of the added references (Adesida and Sugimoto) to meet any limitation in the *independent* Challenged Claims, so I understand that Petitioner and Dr. Zhao to be relying on Ground 5's showing to meet independent claims 1 and 13. *See* Petition, 55-64 (not discussing independent claims 1 and 13); EX-1002 (Zhao Dec.), ¶¶188-201. For that reason, Grounds 6-7 fails for the same reasons that Ground 5 does, because they inherit the flaws I discussed for Ground 5, above in Section IX.C.

279. I discuss additional flaws with Grounds 6 and 7, below.

2. Ground 6 Fails for Claims 11 and 16 for Additional Reasons

280. Ground 6 alleges obviousness of claims 11 and 16 – which require that the recited electrical contact in the independent claims be implemented as a gate electrode that “mak[es] Schottky contact with” the semiconductor – over EX-1005 (Yu), EX-1004 (Usui), and EX-1006 (Adesida).

281. Petitioner and Dr. Zhao both admit that Yu “does not expressly teach an electrical contact implemented as a gate electrode making a Schottky contact”

with the semiconductor, but allege that a gate electrode in Adesida does. Petition, 58; EX-1002 (Zhao Dec.), ¶192. In particular, Ground 6 maps Adesida’s “**gate 190 (gate electrode)**” to the gate electrode in claims 11 and 15, using the annotated figure shown below. Petition, 60-61; EX-1002 (Zhao Dec.), ¶199.

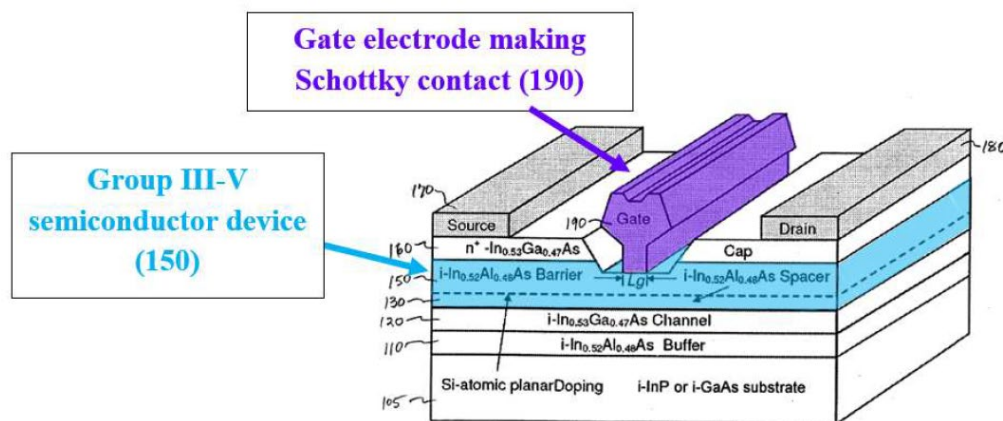


Figure 5

Petition, 61 (Petitioner’s Annotations to Adesida, Fig. 5).

282. Claims 11 and 16 limit “said electrical contact” in independent claims 1 and 13, respectively, but neither Petitioner nor Dr. Zhao even try to demonstrate that Adesida’s gate electrode meets claim 1 and 13. It does not. For example, neither Petitioner nor Dr. Zhao cites any evidence that Adesida’s gate electrode has a capping layer of a refractory metal nitride (limitation [1a]) or of TiN and/or TaN (limitation [13b]). Petitioner and Dr. Zhao also do not cite to any evidence showing that Adesida’s gate electrode has the required layer thicknesses recited in claims 1 and 13.

283. To the extent Petitioner and Dr. Zhao attempt to say in a future filing that the structure of the gate electrode in Yu-USUI-Adesida is *Yu's* gate electrode but modified to make Schottky contact, that argument would also fail. Neither Petitioner nor Dr. Zhao articulated this argument, and there is no evidence in the record supporting such a combination.

284. Moreover, as discussed above in, e.g., Section VIII.B (¶¶106-114), Yu's disclosure is *specifically* directed to implementing a CMOS device with "a *high-k gate dielectric* and metal gate electrode." EX-1005 (Yu), [0004]. As Petitioner and Dr. Zhao themselves admit, Yu's Fig. 2E – which Petitioner relies on for claims 1 and 13 (Petition, 41-44 and 54-55; EX-1002 (Zhao Dec.), ¶¶161-168, 183-186) – has dielectric "insulating" layers 214, 216 (Petition, 53-54; EX-1002 (Zhao Dec.), ¶182), and thus it illustrates an insulated gate electrode that does not form a Schottky contact with the semiconductor.

285. Petitioner does not cite any reference disclosing a Schottky gate electrode for a CMOS device like Yu's. That would be highly unconventional – the "O" in CMOS refers to the "oxide" between metal and semiconductor – and thus far from a "simple design choice" as Petitioner alleges (Petition, 59). Moreover, Petitioner's assertion that a POSA would have modified Yu to *remove* its high-k dielectric but *retain* Yu's gate structure – which is *specifically designed to work with that high-k dielectric* – is wholly unsupported and appears to be based on

improper hindsight. A POSA would not have used a Schottky gate electrode for Yu's CMOS device, and if interested in implementing a Schottky gate electrode, would not have used Yu's specific metal gate electrode, because Yu's metal gate electrode *is specifically designed for use with a high-k dielectric*.

286. Petitioner also fails to establish a reasonable expectation of success. To the extent Petitioner suggests that Yu-Usui's alleged electrical contact could simply be used unchanged to form a Schottky contact, no evidence supports that. A POSA understood this would require changes to the layers – in their materials and thicknesses – because, as I discussed above in Section VI.B (¶¶58-61), Schottky contacts, like ohmic contacts, are carefully designed and tailored to the semiconductor underneath the gate contact. Petitioner and Dr. Zhao fail to consider and account for the changes that would have been required when making such modifications, and fail to show that the alleged electrical contact of Yu-Usui-Adesida that resulted after such modifications would meet claims 1 and 13.

3. Ground 7 Fails for Additional Reasons

287. Ground 7 alleges obviousness of claims 10 and 15 – which require that the electrical contact is “implemented as a power electrode making ohmic contact with said ... semiconductor device” – over EX-1005 (Yu), EX-1004 (Usui), and EX-1007 (Sugimoto).

288. Petitioner and Dr. Zhao both admit that neither Yu nor Usui discloses a power electrode making ohmic contact with a semiconductor device. Petition, 62; EX-1002 (Zhao Dec.), ¶202. Petitioner and Dr. Zhao allege, however, that Sugimoto discloses a Group III-V semiconductor device, like Yu, and *source and drain* electrodes that are power electrodes making ohmic contact with a semiconductor. Petition, 62-63 (alleging ohmic contacts were well-known and important for implementing *source and drain* electrodes); EX-1002 (Zhao Dec.), ¶¶51-57, 203-206. Petitioner and Dr. Zhao conclude by alleging motivation “to implement the devices of Yu and Yu-Usui with a power electrode making an ohmic contact, as taught by Sugimoto” because this “would provide reduced internal heating of the contact and improved current flow (i.e., improved work function values).” Petition, 63 (citing EX-1006 (Adesida), [0031], Fig. 5; EX-1002 (Zhao Dec.) ¶¶51-57, 206); EX-1002 (Zhao Dec.), ¶206. Both Petitioner and Dr. Zhao again allege a rationale based on “known techniques known techniques to a known device ready for improvement to yield predicable results.” Petition, 63; EX-1002 (Zhao Dec.), ¶206.

289. For the purposes of this analysis, I do not dispute it would have been obvious to implement Yu’s CMOS device to have source and drain electrodes that are power electrodes making ohmic contact with a semiconductor. But I note that merely implementing a CMOS device to have source and drain electrodes would

not necessarily meet claim 10 or 15. This is because dependent claims 10 and 15 limit “said electrical contact” recited in independent claims 1 and 13, respectively, but neither Petitioner nor Dr. Zhao even try to demonstrate that Ground 7’s *Yu-Usui-Sugimoto combination* meets claim 1 or 13. Petition, 62-64; EX-1002 (Zhao Dec.), ¶¶202-209. For example, neither Petitioner nor Dr. Zhao cites any evidence that the resulting power electrode has the required layer thicknesses recited in claims 1 and 13.

290. Even if the argument articulated in the Petition and Dr. Zhao’s declaration were read to suggest that Ground 7’s Yu-Usui-Sugimoto combination somehow meets claims 1 and 13 in the same way that Ground 5’s Yu-Usui combination does, that is technically unsound. Ground 5 alleges that the claimed electrical contact comprising an electrode stack is met by Yu’s “metal *gate* stacks.” Petition, 41-44 and 54-55; EX-1002 (Zhao Dec.), ¶¶161-168, 183-186.

291. Yu’s gate stacks form *gate* electrodes – plural, because CMOS devices include two or more transistors (EX-2026 (Zhao Dep.), 60:15-17) – for a CMOS device that are undisputedly not *ohmic* contacts because they do not contact the semiconductor. Yu, Title, Abstract, [0004], Fig. 2E, [0027] (insulating “dielectric layer 214” is “formed over the substrate”); EX-1002 (Zhao Dec.), ¶¶56-57. See my discussion above regarding ohmic contacts, in Section VI.A (¶¶48-57).

292. Petitioner and Dr. Zhao allege that ohmic contacts were known to “serve as *source and drain* contacts in group III-V devices and allow current to flow into and out of a semiconductor material.” Petition, 62-63; EX-1002 (Zhao Dec.), ¶205. But a POSA understood well that current flow in and out of the semiconductor would not occur through Yu’s *gate* electrodes. Thus, even if a “POSITA would have been motivated to implement the devices of Yu and Yu-Usui with a power electrode making an ohmic contact” (Petition, 63), as Petitioner alleges, a POSA would have implemented the Yu device’s *source and drain* electrodes as power electrodes making ohmic contact. A POSA would not have touched Yu’s gate electrodes. That modification would not have met claim 10 or 15 because it would not have made any changes to Yu’s *gate* electrode, which is the electrode that Petitioner and Dr. Zhao allege meets “said electrical contact” in independent claims 1 and 13. Petition, 41-44 and 54-55; EX-1002 (Zhao Dec.), ¶¶161-168, 183-186.

293. I note that neither Petitioner nor Dr. Zhao alleges that a POSA would have implemented the Yu-Usui-Sugimoto combination by having its *source or drain* electrode have the same structure as either of the two Yu *gate* electrodes alleged to meet “said electrical contact” in independent claims 1 and 13 – let alone establish, with evidence, some reason for why this would have been done.

294. Yu is directed to CMOS devices. The “C” refers to the fact that CMOS devices included two complementary types of MOS devices (P-type and N-type), both of which have a gate oxide (“O” in MOS) isolating the metal gate electrode (“M” in MOS) from the semiconductor (“S” in MOS). EX-1005 (Yu), [0004]. It was well-known that a CMOS gate electrode is separated from the semiconductor by a dielectric layer and serves a different purpose than ohmic source and drain electrodes that contact the semiconductor and have current pass through them when the transistor is on. This is because a gate in a MOS device (including in CMOS devices) controls the transistor through an electrical field across the gate dielectric *without current flowing through the gate electrode*. E.g., EX-1011 (Mishra), 356 (Page 380 of 583) (“It is important to isolate the gate from the channel so that no current flows into the gate.”); *see also id.*, 434-36 (Pages 458-60 of 583), 454-57 (Page 478-81 of 583); Petition 63 (low contact resistance is critical for ohmic contacts for “improved current flow”). Thus, a POSA understood that MOSFET gate electrodes (including CMOS gate electrodes) were conventionally implemented using a *different structure formed from different materials* than MOSFET source and drain electrodes (including in the CMOS context), because a MOSFET must have a gate electrode with a metal composition with a correct work function for the MOSFET to function. E.g., EX-1005 (Yu), [0033]-[0034] (describing selection of n-type work function for NMOS, and p-type

work function for PMOS). A POSA would not simply use the identical metal composition used for forming ohmic contacts in the source and drain electrodes as a gate electrode without modification.

295. Neither Petitioner nor Dr. Zhao ever suggests a POSA would have had any reason to implement the Yu-Usui-Sugimoto combination by having the *source or drain* electrode have the same structure as either of the Yu *gate* electrodes⁶ that are alleged to meet “said electrical contact” comprising an electrode stack in independent claims 1 and 13. Petition, 41-44 and 54-55; EX-1002 (Zhao Dec.), ¶¶161-168, 183-186. Petitioner and Dr. Zhao thus point to one electrical contact comprising a gate electrode to allegedly meet the requirements in claims 1 and 13 but never allege that this *same* electrical contact comprising a gate electrode meets the additional requirements that claims 10 and 15 impose.

296. Petitioner also fails to establish a reasonable expectation of success. To the extent Petitioner suggests that Yu-Usui’s alleged electrical contact could simply be used unchanged to form an ohmic contact, no evidence supports that. A

⁶ As discussed above in Section VIII.B (¶¶106-114), Yu is directed to a particular CMOS *gate* electrode implementation using a high-k dielectric and metal *gate* electrodes with different work functions for the CMOS device’s NMOS and PMOS transistors. EX-1005 (Yu), Title, [0004], [0030].

POSA understood this would require significant changes to the layers – in their materials and thicknesses – because, as I discussed above in Section VI.A (¶¶48-57), ohmic contacts are carefully designed and closely tailored to the semiconductor underneath the contact, like a lock and key. Petitioner and Dr. Zhao fail to account for the changes that would have been required when making such modifications, and fail to show that the alleged electrical contact of Yu-Usui-Sugimoto that resulted after such modifications would meet claims 1 and 13.

* * *

I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

I declare under penalty of perjury that the foregoing is true and correct.

Dated: 9/30/2025

A handwritten signature in black ink, appearing to be 'Edwin Piner', written over a horizontal line.

Edwin Piner