

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.	) CASE NO.:
Petitioner,	) IPR2025-00175
	) PATENT NO.:
v.	) 8,686,562
	)
INFINEON TECHNOLOGIES AMERICAS	)
CORP.,	)
Patent Owner.	)
-----	)
	)

ORAL DEPOSITION OF

YUJI ZHAO, Ph.D.

SEPTEMBER 5, 2025

ORAL DEPOSITION OF YUJI ZHAO, Ph.D., produced as a witness at the instance of the Patent Owner, and duly sworn, was taken in the above-styled and numbered cause on September 5, 2025, from 9:00 a.m. to 5:11 p.m., before Kimberly Wheelis, CSR, RPR, CRR, in and for the State of Texas, reported by computerized stenotype machine, via Zoom, pursuant to the Texas Rules of Civil Procedure and the provisions stated on the record or attached hereto.

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1 YUJI ZHAO, Ph.D.,
2 having been first duly sworn, testified as follows:

3 MR. SARWAR: I'm Turhan Sarwar, I'm here
4 on behalf of Patent Owner, Infineon. I have with me
5 Mark Consilvio, also from Wolf Greenfield, also on
6 behalf of Patent Owner, Infineon.

7 MS. RODRIGUEZ: Hi, I'm Sarah Rodriguez.
8 I'm here on behalf of the Petitioner and I'm here with
9 Luke MacDonald and Lionel Lavenue.

10 EXAMINATION

11 BY MR. SARWAR:

12 Q. All right. If we're ready to begin, I'll get
13 started. Hi, Dr. Zhao.

14 A. Hi. Thank you.

15 Q. I will tell you that I'm likely to be somewhat
16 variable in my pronunciation of that, but I apologize in
17 advance.

18 Have you ever been deposed before?

19 A. Yes.

20 Q. How many times?

21 A. I deposed once in U.S. court and many times in
22 the Chinese courts.

23 Q. Is there anything preventing you from giving
24 your best testimony today?

25 A. No.

1 Q. Good. Here are some ground rules for today's
2 deposition. I'll ask you questions, you'll provide
3 verbal answers so that the court reporter can record the
4 answers. Petitioner's attorney might object to my
5 question, but you still have to answer the question
6 unless you are specifically instructed by Petitioner's
7 attorney not to answer.

8 Let's plan on taking a break every hour or
9 so. Though if you need to take a break before that, let
10 me know. Before we start any break, you should finish
11 providing your answer to any pending question on the
12 record.

13 Since we're conducting the deposition
14 remotely, I will ask, do you have any materials or notes
15 with you in the room where you are taking this
16 deposition?

17 A. I have all the declaration, my declaration,
18 all the exhibits, and the file history. There's no
19 notes or mark any of these copies.

20 Q. Okay, so they're clean copies of the filings
21 and the exhibits in this proceeding?

22 A. Correct.

23 Q. Okay. Thank you. I will plan on dropping
24 documents that I reference into the Zoom chat window so
25 that you can download them and review. But I suspect

1 you will have a paper copy in front of you of the
2 documents, at least most of the documents that I end up
3 using. So you should just let me know what document
4 you're referencing, you know, when you're referencing
5 documents for an answer, just so that we have a clean
6 record.

7 I'll be dropping the electronic copies for
8 the benefit of the court reporter.

9 Does that make sense?

10 A. Thank you.

11 Q. All right. And if you're consulting anything
12 other than the documents that I'm referencing and
13 providing to you, will you just let me know?

14 A. Thank you.

15 Q. All right. Okay, so how did you prepare for
16 this deposition?

17 A. I review the 562 patent, and the reference,
18 and my declaration.

19 Q. Did you review any materials that were not
20 as -- not submitted as papers or exhibits in these -- in
21 this proceeding?

22 A. The materials I refer to the materials that I
23 reviewed.

24 Q. I'm going to ask for a clarification on that.
25 When you say the materials you refer to, are you talking

1 about the materials that are cited in your declaration?

2 A. I am referring to my declaration and the
3 reference cited in declaration exhibits and file
4 histories.

5 Q. Okay. Did you conduct any research outside of
6 those documents and outside of the documents that were
7 submitted in this proceeding?

8 A. These materials are the ones that I reviewed
9 for this deposition.

10 Q. Okay, thank you. I am showing you Exhibit
11 1001. Let me know when you have it.

12 A. I have Exhibit 1001.

13 Q. Okay. And this is U.S. Patent Number
14 8,686,562, correct?

15 A. Correct.

16 Q. Will you understand me if I refer to this
17 patent as the 562 patent?

18 A. I understand.

19 Q. You reviewed the 562 patent, correct?

20 A. I reviewed 562 patent.

21 Q. All right. I'm also showing you Exhibit 1002.
22 Let me know when you have that.

23 A. I have it.

24 Q. This is the declaration that you prepared for
25 the IPR proceeding that challenges the 562 patent,

1 correct?

2 A. Correct.

3 Q. Did you write this declaration?

4 A. This declaration represents all my
5 professional opinions.

6 Q. Did you write this declaration?

7 A. I write a very big part of this declaration
8 and this declaration represents all my professional
9 opinions.

10 Q. What documents did you rely upon to prepare
11 this declaration?

12 A. I prepared the declaration using the
13 references that is cited in the declaration.

14 Q. All right. And when preparing the
15 declaration, did you review any documents and materials
16 that you did not cite in your declaration?

17 A. The materials cited in my declaration are the
18 ones I reviewed for the declaration.

19 Q. Okay. All right. Thank you so much.

20 I just thought of another ground rule, by
21 the way, that I should go over. Which is, as we sort of
22 start delving into the questions and answers, if you have
23 any questions or lack of clarity about the question that
24 I asked, you should feel free to just let me know and I
25 can try to clarify, okay?

1 A. Thank you.

2 Q. All right. You opined in your declaration
3 regarding ohmic contacts, correct?

4 A. Ohmic contact is included in my declaration.

5 Q. Can you explain to me what ohmic contact is?

6 A. Ohmic contact is a contact to achieve ohmic
7 behavior.

8 Q. What are the characteristics of the contact
9 that are needed in order to achieve ohmic behavior?

10 A. The contact needs to be -- to have a ohmic
11 behavior. In my analysis of this matter, I particularly
12 refer to 562, patent 1, which is about electrode stack
13 of metallic -- metal fumes -- or metal layers and
14 capping layer. Anything outside this metal layers and
15 the capping layer is unclaimed. These are the metals
16 that -- metal layers that I analyzed.

17 Q. What is ohmic behavior?

18 A. Ohmic behavior is a linear response in the IV
19 characteristic.

20 Q. Can you say the last part of that again? I
21 wasn't able to catch it on my audio, that's all.

22 A. Ohmic linear response in IV characteristics.

23 Q. You're saying IV?

24 A. Correct.

25 Q. In order to achieve ohmic behavior, do you

1 need to have direct contact between metal and
2 semiconductor?

3 A. There are different ways to make ohmic
4 contact. And as I previous state in my analysis of
5 declaration, the contact that I analyzed is in 562,
6 claim one, which is the electrode stack includes metal
7 layers and capping layer, and anything that is outside
8 this metal layer, or capping layer is unclaimed.

9 In my analysis I provided some of the
10 references such as Usui. In Usui's structure it has a
11 via; a via is not a layer. It's a filled hole. Usui's
12 via has to cut cross multiple layers, so it is not a
13 layer, it is a filled hole.

14 So in my analysis I focus on the contact.
15 The electro contact is on the metal layers and the
16 contacting layers because they included all the claimed
17 features. And whether this via is part of the electro
18 contact is irrelevant, and do not change my analysis.

19 And at the end of the day, if you want to
20 achieve ohmic contact then you can have multiple ways.
21 The outside way -- outside world will be connected to
22 this metal layer, electrode stack, and the via to the
23 semiconductor device layer 6 in Usui.

24 Q. Okay. So I'll have you turn to paragraph 55
25 of your declaration.

1 A. You say paragraph 55, correct?

2 Q. That's correct.

3 A. I have the paragraph 55 here.

4 Q. Okay. So you see here that paragraph 55 is --
5 looks like it's in a section entitled ohmic and shop key
6 contacts?

7 A. I see that.

8 Q. The question I'm asking you is, I'm trying to
9 learn a little bit more about what ohmic contacts are.
10 And so if you can turn to paragraph 57 of your
11 declaration, you see here --

12 A. Sorry, 57.

13 Q. Yeah, 57. I see here that you wrote, ohmic
14 contacts allow current to flow into and out of a
15 semiconductor material without distortion of the signal.

16 Do you see that?

17 A. I see this sentence.

18 Q. Okay. And the sentence after that says, the
19 most critical component of an ohmic contact is low
20 specific contact resistance, which minimizes the power
21 consumption of the contact and the internal heating of
22 the contact, thereby prolonging device operation with
23 predictable performance.

24 Do you see that?

25 A. I see this sentence, but just like I previous

1 noted, this is general description of ohmic contact.
2 The relevant part for my analysis and also declaration
3 is focus on claim one of 562 patent, which is electrode
4 stack, includes metal layers and capping layer. All my
5 analysis has been focused on those metal layers, the
6 capping layers, because they include all the claim
7 features.

8 Q. So is paragraph 57 of your declaration not
9 relevant to your analysis?

10 A. Page 57, this analysis is relevant to my
11 analysis. I want to highlight that the metal layers and
12 the capping layers in 562 patent could be widely applied
13 to wide range of structures. It could be in ohmic
14 contact. It could be in Schottky contact, it could be
15 in gate -- insulated gate, and we have seen those
16 applications in the reference such as Usui, such as Yu,
17 and Adesida and so forth.

18 Q. So can a metal layer and a semiconductor layer
19 be in ohmic contact if there's an insulating layer in
20 between them?

21 A. So, the metal layers in the -- there's many
22 ways to making contact to a semiconductor. And the
23 metal layers -- if we see Usui, for example, we have
24 those metal layers work as a interconnect.

25 And if we see Yu, we see similar metal

1 layers work as a gate structure. And it's very important
2 to know in Usui and Yu, they are metal layers, their
3 electrode stack is interchangeable, because those metal
4 layers are formed from the same type of materials. And
5 then, in Yu's case we have this metal layer and the
6 bottom layer is a diffusion barrier layer and one
7 important purpose for the diffusion barrier layer is to
8 improve electromigration.

9 And in Usui, Usui provides a guidance to
10 improve the electromigration by limiting the thickness of
11 bottom layer. So it is very obvious and predictably
12 successful for a POSITA at the time to combine Usui's
13 metal layers into Yu's gate to achieve this result.

14 So, it doesn't matter whether a metal
15 layer, or a metal layer in, you know, can form on
16 semiconductor or dielectric. It can form ohmic -- or not
17 ohmic behavior because Usui's teaching is broadly
18 applied.

19 Q. In your answer you used the phrase improve
20 electromigration; is that right?

21 A. I used improve electromigration as is stated
22 in some the references.

23 Q. What is your understanding of the phrase
24 improve electro migration?

25 A. To improve the electromigration by reducing

1 some the negative effects.

2 Q. And what negative effects are you referring
3 to?

4 A. In electromigration and what you see is metal,
5 one the example of electromigration is the metal atom
6 will diffuse into semiconductor layers, leading to
7 reliability issues. One of the common way to, to
8 mitigate, to improve the electromigration is to putting
9 the diffusion barrier layer.

10 And in 562 patent, it never distinguish
11 the diffusion barrier layer from the metal layers. As a
12 matter of fact, we see this layer everywhere. In 562
13 patent we see the bottom layer is titanium. In the
14 paragraph 29 of Yu, which I provided, it state that this
15 bottom layer of Yu's metal layer to be titanium. And
16 then in Usui's, the bottom layer again is titanium.

17 So this titanium base, the bottom metal
18 layer, is everywhere is the effective way to improve
19 electromigration. It's very well known, so as all my
20 combination shows.

21 Q. Okay. So I'm going to step back to an earlier
22 question, because I don't think I was able to get a
23 clear answer to it. And I'll try to rephrase in case it
24 was unclear.

25 So can a metal layer and a semiconductor

1 layer be an ohmic contact if there's an insulating layer
2 in between them?

3 A. The metal layers that we been focusing today,
4 according to 562 patent, is on the metal layers and the
5 capping layer, and they have all the claim features.
6 And from the -- as I previous stated, my analysis has
7 been focused on those metal layers and capping layers,
8 and these -- and from analysis of Usui and Yu, we see
9 that those metal layers and capping layer could be
10 widely applied to interconnect, to gate structures in
11 Yu, could be Schottky gate, could be insulate gate.

12 So even though the -- when you have a
13 dielectric layer, the contact could be characterized as
14 ohmic contact, which does not have a dielectric layer, or
15 gate -- a insulate gate, which has a dielectric layer.
16 The teaching in Usui and Yu could be widely applied to
17 both cases.

18 Q. I think you just said that the contact could
19 be characterized as ohmic contact, which does not have a
20 dielectric layer. Why did you say that?

21 MS. RODRIGUEZ: Objection, vague.

22 A. I provided the answer that because all the
23 reasoning that the metal layers and the capping layer,
24 which are the claim features that we analyze, it's in my
25 declaration, it's also the matter we discuss today.

1 These layers will be widely applied to achieve ohmic
2 contact, to achieve Schottky contact, to achieve
3 insulated gate structure, and of POSITA at the time is
4 very well known about this.

5 Q. (BY MR. SARWAR) So do you know whether a metal
6 layer and a semiconductor layer can be in ohmic contact
7 if there's an insulating layer in between them?

8 A. I --

9 MS. RODRIGUEZ: Objection, form.

10 A. I understand how to achieve ohmic contact in
11 semiconductors. Just, I lay out earlier if we see the
12 case such as Usui and Yu, Usui and Yu, they are electro
13 stat or the metal contact, as you refer to, they are
14 interchangeable, because they are formed from the
15 same -- from the metal layers of same type of materials.

16 And in Yu, in Yu, it cause the bottom
17 layer of its metal layers as diffusion barrier layer.
18 And again, this is the question you refer to earlier, one
19 purpose to -- for this diffusion barrier layer is to
20 improve electromigration. Usui's metal layers,
21 particular provides a important guidance to improve
22 electromigration by limiting the thickness of bottom
23 layer.

24 So it's perfectly predictable and obvious
25 for POSITA at the time to apply Usui's metal layers, and

1 metal structures to Yu's device, such as gate in
2 semiconductor. So you see that the matter we discuss,
3 focusing on the metal layers and capping layers, and from
4 this reference, we clearly see that they can be applied
5 to, to the ohmic contact, and to the insulated gate
6 structures, and these are the discussion today.

7 Q. (BY MR. SARWAR) So I, I have a pretty
8 straightforward question for you, and I still haven't
9 gotten a clean answer on it. Which is, I'm just trying
10 to find out if a metal layer and a semiconductor layer
11 can be in ohmic contact if there's an insulating layer
12 in between them?

13 MS. RODRIGUEZ: Objection, asked and
14 answered.

15 A. I answer the question multiple time. Again,
16 to our discussion today, it doesn't matter because we
17 are focusing on the nature of those metal layers, and
18 the capping layer, and I've answered they could be
19 broadly applied to achieve ohmic contact such as in the
20 interconnect, or source in the transistor, or drain in
21 the transistor, or in the gate in the transistor
22 structure. Could be insulating, or could be Schottky,
23 could be have a dielectric layer or could not -- or will
24 not have a dielectric layer, doesn't matter. The clear
25 features we focused on could be widely applied to all

1 those structures.

2 Q. (BY MR. SARWAR) Well, yes, I understand that
3 your analysis applies to different structures. I'm
4 going to ask you about ohmic contacts. I'm going to ask
5 you about Schottky contacts. I'll ask you about gated
6 electrodes. I'll ask you about all that.

7 The simple yes or no question that I'm
8 asking right now is: Can a metal layer and a
9 semiconductor layer be in ohmic contact if there's an
10 insulating layer in between them?

11 MS. RODRIGUEZ: Objection, asked and
12 answered.

13 A. Since you already understood that the teaching
14 here, that the metal layers, the capping layers could be
15 applied to both ohmic contact, Schottky contact, and the
16 insulating gate structure, and if we refer to general
17 question in my declaration, I provide very detailed
18 discussion on the ohmic contact and the ohmic contact
19 could be achieved by putting metal on semiconductor, of
20 course with some requirement of the semiconductor. They
21 are all very detail laid out in my declaration.

22 Q. (BY MR. SARWAR) Okay. So where in your
23 declaration is it laid out whether or not a metal layer
24 and a semiconductor layer can be in ohmic contact, if
25 there's an insulating layer in between them?

1 A. Counselor, could you repeat this question?

2 Because I think you have distorting what I just --

3 distorting what I just told you.

4 Q. Where in your declaration is it laid out,

5 about whether a metal layer and a semiconductor layer

6 can be in ohmic contact if there's an insulating layer

7 in between them?

8 A. Counselor, this is not what I just told you.

9 I want to put on record I provide very detailed

10 discussions on how to achieve ohmic contact, how to

11 achieve Schottky contact, and how to achieve insulated

12 gate in my declaration, and the counselor just confirm

13 that the teaching that -- about the metal layers, and

14 the capping layers could be broadly applied to all these

15 structures.

16 Q. So would an insulating layer between a metal

17 and semiconductor layer -- scratch that. I'm going to

18 try again.

19 Would an insulating layer that is in

20 between a metal layer and a semiconductor layer prevent

21 ohmic contact between the metal and the semiconductor?

22 MS. RODRIGUEZ: Objection, asked and

23 answered.

24 A. I answered these questions multiple times.

25 And in my declaration 62 -- paragraph 62, I lay out the

1 gate dielectrics, and it doesn't matter those -- whether
2 it's ohmic contact, or whether it's Schottky contact, or
3 whether it is gate insulated gate, the teaching here,
4 those metal layers and the capping layer, they could be
5 broadly applied to all these cases, and I see the
6 counselor is agree on this. That's the matter we focus
7 on.

8 Q. (BY MR. SARWAR) Well, you still actually have
9 to answer the questions that I'm asking. So, the
10 question I have, which I still haven't gotten a clear
11 answer on, because when you answered, you start bringing
12 into the scope of the answer Schottky contacts and
13 insulated gate electrodes, and all I'm really asking
14 is -- I'm just trying to get an understanding of whether
15 or not you can have an insulating layer, and still
16 achieve ohmic contact?

17 MS. RODRIGUEZ: Objection --

18 Q. (BY MR. SARWAR) Do you have an answer to that
19 question?

20 MS. RODRIGUEZ: Objection, asked and
21 answered.

22 MR. SARWAR: Oh, and actually before I
23 have you answer, I would just ask, Counselor, you
24 objected a few times now using improper objections for
25 this forum, should be limited to, like, one word, not

1 really coaching the witness, informing him about how he
2 should answer the question. You're definitely not
3 supposed to say objection, vague. And I think
4 objection, asked and answered, since it's resulting in
5 Dr. Zhao saying, oh, I've already answered this
6 question, even though he hasn't. I would ask that you
7 limit your objections to single word objections
8 regarding form or scope. Thank you.

9 Q. (BY MR. SARWAR) Dr. Zhao, you probably don't
10 remember my question; shall I repeat it?

11 A. Yeah, please repeat your question.

12 Q. Okay, yeah. So I'm trying to get an
13 understanding of whether or not you can have an
14 insulating layer in between a metal layer, and a
15 semiconductor layer and still achieve an ohmic contact;
16 yes or no?

17 A. I have again put on the record, I have provide
18 very comprehensive answers to the questions multiple
19 times. And in my declaration I lay out the ways to make
20 ohmic contact, to make Schottky contact, and to -- the
21 ways to make insulate gate structures.

22 And I have also provide my professional
23 opinions that they are not -- they are -- it doesn't
24 matter how we -- how we make those contacts in the
25 discussion of 562 patent, because, those metal layers and

1 the capping layer could be widely applied to the -- each
2 of the case.

3 Q. Let's turn to Exhibit 1001, column 3. And
4 I'll direct you to --

5 A. You are --

6 Q. -- specific --

7 A. 562 patent?

8 Q. Yes.

9 A. Okay, which paragraph you want me to go to?

10 Q. Okay, so in column 3, take a look at the
11 sentence that starts, as further shown in on line 28?

12 A. Would you let me know which sentence are you
13 referring to?

14 Q. Sure. The sentence begins -- or I guess I'm
15 going to ask you about a couple of sentences. As
16 further shown in figure one, insulated gate electrode
17 132 includes gate insulator layer 134, such as a silicon
18 nitride or silicon dioxide layer --

19 A. I didn't ask you this paragraph. You are
20 saying the 562 patent and on which page?

21 Q. This is the sixth page of the patent. This is
22 column 3.

23 A. Column 3, so what's the first sentence of that
24 paragraph?

25 Q. Of the whole paragraph.

1 A. Yeah, I could not find this, this sentence.

2 Q. Okay, that's fine. Do you know how to use the
3 line numbers in patents?

4 A. I do, but then the information you provided, I
5 just could not find it at this moment.

6 Q. It's okay. So if you look at column --

7 A. If you give me more time, I can find it.

8 Q. Sure.

9 A. You said page 6, page 6?

10 Q. Do you see that there are -- in the patent
11 there are column numbers up top?

12 A. Okay, I see column 3 now. In which line, 28?

13 Q. Yeah, let's start with 28.

14 A. Okay. Which sentence are you referring to?

15 Q. All right, so let's start with the sentence,
16 as further shown in figure 1, insulated gate electrode
17 132 includes.

18 A. I see this sentence now.

19 Q. Okay. And can you -- you don't have to read
20 it out loud, just read from that sentence to the end of
21 the paragraph and let me know when you're done.

22 A. Okay, so you want me to read through -- review
23 this paragraph at this time, okay, I will do that.

24 Okay, I reviewed these lines now.

25 Q. Okay. With those lines in mind, can you turn

1 to figure 1 of the 562 patent?

2 A. I have figure 1 of the 562 patent now.

3 Q. Excellent. And can you look at gate electrode
4 132?

5 A. I see 132 now.

6 Q. Do you know what layer 134 is?

7 A. 134 from the 562 patent, this is the gate
8 insulate layer.

9 Q. Gate insulator layer 134 can be silicon
10 dioxide, right?

11 A. There could be many combinations for the gate
12 dielectric layer. There are two very commonly seen gate
13 structures including the insulated gate, and the
14 Schottky gate, as the 562 patent shows that, and also
15 says in this paragraph these are two commonly seen
16 gates.

17 And in my analysis in the gate structure,
18 I, I, for example, combine Usui and Yu and Adesida. We
19 see that it's very clear the teaching of the metal layers
20 and the capping layer can be broadly applied to all these
21 gate structure because they can achieve the preferable
22 performance. So a POSITA at the time by looking at Usui
23 and Yu, and with Adesida, it's perfectly reasonable and
24 predictable and will be obvious for them to use the metal
25 layers, the capping layer for the insulated gate as shown

1 in the patent here, or remove the static gate to make
2 Schottky gate, because insulated gate and Schottky gate
3 are two commonly, most widely used and very well known
4 gate structures.

5 In my declaration I provide a lot of
6 detailed discussions on the benefits of achieving
7 Schottky gate, which is by removing this dielectric
8 layer, such as first response and non-linear IV
9 characteristic.

10 Q. So if I were to remove gate insulator 134 from
11 gate electrode 132, would that become a Schottky
12 contact?

13 MS. RODRIGUEZ: Objection, asked and
14 answered.

15 And I would just like to state that asked and
16 answered is appropriate, just as objection, foundation is
17 allowed. So unless you have a citation, I will continue
18 to use it.

19 As for objection, vague. I agree and with
20 apologies, I will not do that again. And I'd just like
21 to point out that Rule 1 is amended to emphasize that the
22 Court should construe and administer these rules to
23 secure just and speedy and extensive determination of
24 every action. So the parties share the responsibility to
25 employ the rules in the same way.

1 MR. SARWAR: Thank you --

2 MS. RODRIGUEZ: You're not allowed to
3 keep asking the same question unless you get the answer
4 you want, Counselor.

5 MR. SARWAR: Oh, thanks so much,
6 Counselor, I'll take that under advisement.

7 Q. (BY MR. SARWAR) So the question that I just
8 asked, which was not asked before, was, if I were to
9 remove gate insulator 134 from gate electrode 132, would
10 that become a Schottky contact?

11 A. I answer this question already, but let me
12 answer this question again. There are two commonly,
13 very widely known gate structure. One is insulating
14 gate which has a dielectric layer. The other is
15 Schottky gate which does not have this insulate gate.
16 By the effective date which is August 25th, 2009, both
17 of the gate structure are widely known, widely applied
18 to semiconductor device. And the POSITA at the time
19 very well known about these structures, and it is a very
20 obvious and motivated for a POSITA at the time by
21 removing a dielectric layer, such as in Yu's teaching.
22 And to achieve Schottky gate, which is in Adesida's
23 teaching.

24 So in both of those gate structure, very
25 well know. And the -- and then one is dielectric, and

1 one is not. One is without dielectric layer, very well
2 known. And again, our teaching here, this metal layer,
3 and the capping layer could be broadly applied to both
4 cases.

5 Q. If you removed that layer 134, why is it a
6 Schottky contact and not an ohmic contact?

7 A. Counselor, this, this is what I just already
8 answered, that if you, you can achieve ohmic contact,
9 you can achieve Schottky contact, and you can achieve
10 insulated gate and -- with a lot of combination. But
11 doesn't matter here because the metal layers, and the
12 capping layer can be broadly applied to all of these
13 applications as in the reference Usui, in Yu, and in a
14 Adesida with the combination I provided in the, in the
15 reference.

16 And I also want to note it that your
17 question -- the previous question is scientifically
18 incorrect. So I advise you to ask another question so I
19 can, I can answer.

20 Q. Now we're getting somewhere. This is good.

21 So, can you tell me why it's
22 scientifically incorrect? Why, why --

23 A. Ask the question again?

24 Q. Yeah, sure. So the question I had was, if you
25 remove 134 from 132, right, I think you've testified

1 that, you know, you could achieve a Schottky contact.

2 And I'm asking you whether you could, alternatively,

3 achieve an ohmic contact; is that possible?

4 MS. RODRIGUEZ: Objection, form.

5 A. Again, Counselor, I answer your question

6 multiple times. In my declaration I provide very

7 detailed discussions about ohmic contact, about Schottky

8 contact, about how to make a gate dielectric, which is

9 insulated gate, and Schottky gate, and I provide all

10 these details to you.

11 And even though there are ways to make all

12 those contact, the discussion today, you know, focus on

13 562 patent or the reference is about metal layers and the

14 capping layer, and these clear feature could be applied

15 broadly to all these, these, whether it's interconnect,

16 whether it's ohmic contact, whether it's insulated gate

17 or whether it's Schottky gate, could be all possible

18 here.

19 Q. (BY MR. SARWAR) Okay. In a Schottky contact

20 is the metal layer and the semiconductor layer directly

21 in contact with each other?

22 MS. RODRIGUEZ: Objection, form.

23 A. Again, I have repeatedly answer the questions

24 that there are multiple ways to making those contacts

25 and I would refer to my declaration. But at the end of

1 the day, they don't matter, because the clear features
2 that we discuss are the metal layers and the capping
3 layer, and they could be broadly applied to all these
4 structures including Schottky contact -- or Schottky
5 gate, insulated gate with a dielectric, or ohmic
6 contact, or interconnect. It could be broadly applied.

7 Q. (BY MR. SARWAR) Okay. So, the place in your
8 declaration where you answer these questions, can we
9 identify the paragraph so that I can look at them later?
10 I believe I'm going to provide where I think in your
11 declaration you've answered these questions. Is it
12 paragraphs 55 through 59, or is it somewhere else in
13 your declaration?

14 A. So you are asking me about the declaration.
15 So should we go to my declaration? Which paragraph are
16 you referring to?

17 Q. In your declaration, Exhibit 1002, paragraphs
18 55 through 59.

19 MS. RODRIGUEZ: Objection, form.

20 A. So paragraph 55 to 59 is entitled ohmic and
21 Schottky contacts.

22 Q. (BY MR. SARWAR) That's right. Is that where I
23 can look to find out whether or not -- or rather, is
24 that where I can look to find out how insulating layers
25 work in these -- the context of these contacts?

1 MS. RODRIGUEZ: Objection, form.

2 A. Counselor, I provide very detailed description
3 of ohmic and Schottky contacts in this -- in these
4 paragraph, you are free to read through them.

5 Q. (BY MR. SARWAR) Okay. I'm showing you Exhibit
6 1004.

7 A. Okay, I have 1004 here.

8 Q. Exhibit 1004 is the Usui reference, correct?

9 A. One -- Exhibit 1004 is Usui reference.

10 Q. Let's turn to Usui figure 8.

11 A. I see Usui figure 8 now.

12 Q. Can you tell me the relationship between
13 figure 1 and figure 8?

14 A. You are asking me figure 1 and figure 8, is
15 there a particular question that I need to answer here?

16 Q. Are figure 1 and figure 8 showing the same
17 structure?

18 A. Again, I will need more time to go to
19 paragraphs, but just by looking figure 1 and figure 8,
20 at this moment they appear to be same for me. But for
21 more details, I need to go over all the paragraphs to be
22 sure. Do you want me to do that now, or just give me a
23 few moments to review figure 1 -- let me see figure 1 --
24 yeah, I'm going over figure 1 and figure 8 now. It's
25 been a while. I want to -- I want to look at figure 1.

1 Okay. So, Counselor, so I reviewed,
2 again, just short period of time. So what is your
3 question again?

4 Q. Are they the same structure?

5 A. So in figure 1, again, I'm referring to the
6 column 3 of the Usui patent, it has descriptions of the
7 figure 1 and figure 2 through 8. Here I quote, figure 1
8 is a cross sectional view of a preferred embodiment of
9 interconnect metallurgy according to the present
10 invention, and here I quote figures 2 to 8, are a cross
11 sectional view of the process for fabricating the
12 preferred interconnect metallurgy of all the present
13 invention in the step by step fashion.

14 Q. Okay, is figure 8 the last step?

15 A. From the description I just read to you from
16 the reference, Usui reference, it appears the figure 8
17 may present one the final steps.

18 Q. And you rely on figure 8, correct?

19 A. I -- when I using Usui as a reference, I rely
20 on everything in Usui, all the paragraphs, all the
21 figures, everything --

22 Q. Okay.

23 A. -- in my analysis and understanding.

24 Q. In the annotations you provided of the Usui
25 figures are of figure 8, correct?

1 A. Are you referring to my declaration?

2 Q. Yes.

3 A. Can you, can you -- which page are you
4 referring to?

5 Q. Say page 36 of your declaration.

6 A. Okay, I see this figure 8, Usui. This is in
7 my declaration, I want to highlight here that in my
8 analysis of the matter today, I rely on patent 2
9 pattern, claim one, which is the electrode stack
10 includes metal layers and the capping layer and
11 everything outside, that everything is not a capping --
12 is not a metal layer or capping layer of the electrode
13 stack is unclaimed.

14 And in my declaration I provided Usui as a
15 reference. And in this figure 8 as we are looking at, we
16 are -- I can focus on my analysis on colored layers,
17 which are metal layers, a capping layer and the bottom
18 layer. I want to highlight that the via structure in
19 Usui on number 10 here is not the metal layers that we
20 analyze here. It's a filled hole, and all my analysis --
21 all my discussion will be focused on the patent -- on the
22 metallization, which is the colored, the metal layer,
23 capping layer, and the bottom layer, because they have
24 all the claim features. Here is a filled hole. It's not
25 a layer. Usui has to cut cross multiple layers.

1 So whether this is part of this electrode
2 stack or so, it doesn't change my analysis here, because
3 it's irrelevant for our discussion on Usui. Figure 8 as
4 we are looking at now will be focusing on the metal
5 layers, capping layers, bottommost layer and colored
6 here.

7 Q. What is layer 6 in figure 8?

8 A. Layer 6 is a device layer.

9 Q. Is that silicon?

10 A. I will have to go to the Usui patent to see
11 what eventually this device layer refer to.

12 Q. I can point you to a column and line number,
13 if that would help you.

14 A. Oh, please.

15 Q. So I'm referring again to the columns at the
16 top of the -- so column 3, line 23. And I believe that
17 that passage goes until line 37.

18 A. So I'm reading this sentence, referring to
19 figure 1 here, I quote, in Usui, the interconnect
20 metallurgy preferable comprise the four or five layer
21 structure over interplanar stud connection, and so
22 forth, that it ended to make connection to a device
23 substrate number 6.

24 So again, you are asking me this number 6,
25 it's a device substrate, and it's a device, so it's

1 likely a semiconductor material. And at the end of the
2 day, the, the outside world could be connected to round
3 the patent feature, those metal layers and capping layer,
4 through the via to the semiconductor device. But again,
5 all our discussion on the matter here is the metal
6 layers, and the capping layer; these are the clear
7 features. These are all the discussion has been focused
8 on.

9 Q. So the device substrate, you called it a
10 semiconductor, correct?

11 A. In the patent Usui, it calls -- the sentence I
12 just referred to, it says it's a device substrate. And
13 in semiconductor technology a device typically means a
14 semiconductor material. And it could be broadly applied
15 to, for example, silicon or sulfite materials and so
16 forth.

17 And in the reference I provided, such as
18 Yu, Adesida, and we see that, you know, although we are
19 looking at Usui, the metal layer, the capping in Usui is
20 not limited to the broad application. And by combining
21 Usui to Yu, we can go to other semiconductor device, and
22 adding other reference that -- Adesida, this broadly
23 covers the silicon, broadly covers the III-V, broadly
24 covers the nitrite, broadly covers the ten devices. So
25 all this combination renders the fact that obvious

1 because it's all laid out here.

2 Q. So device substrate 6, is that non-metallic?

3 A. A device substrate 6, there's no information
4 provide on this device substrate. It could be, you
5 know, again, this is what we -- I emphasize again, it
6 doesn't matter how eventually this, this connection
7 goes. We talk about Schottky contact, we talk about the
8 ohmic contact. I talk about the insulated gate
9 structure, and we talk about -- so, we talk about many
10 of those.

11 The teaching here from Usui in other
12 combination could be broadly applied to each of those
13 cases, and in the outside world will be electrically
14 connected to, in this case -- in this case this is a
15 device substrate, a 6, a semiconductor through the metal
16 layer and the capping layer, which are claimed features
17 and the via, and the nature of this device substrate, the
18 patent did not provide information, but it doesn't matter
19 here.

20 Q. What is layer 8?

21 A. Well, I need time to go through this
22 paragraph, just give me one second. Are we referring to
23 figure 1?

24 Q. I'm looking at figure 8.

25 A. Okay.

1 Q. But, --

2 MS. RODRIGUEZ: Is this a good time for a
3 break? We're past 11:00.

4 MR. SARWAR: Yeah, if, if the expert
5 would like to take a break, that's fine with me.

6 THE WITNESS: I would like to take a
7 break.

8 MR. SARWAR: Okay. Take five minutes,
9 ten minutes, what would you like?

10 MS. RODRIGUEZ: Ten minutes.

11 MR. SARWAR: All right. Thank you.

12 (Recess.)

13 Q. (BY MR. SARWAR) Did you discuss your testimony
14 with counsel at all during the break?

15 A. No.

16 Q. In figure 8 of Usui, can you tell me what
17 layer 8 is?

18 A. Here being figure 1, in the first paragraph I
19 refer to -- it says, this insulating -- un-insulator 8.
20 So if this is, you know, if this layer 8 is seen in
21 figure 1 and figure 8, then this layer 8 appear to be an
22 insulator as stated in the Usui.

23 Q. Okay. The insulator is not metal, right?

24 A. Insulator is not a metal.

25 Q. What is stud connection 10?

1 A. Okay, I found number 10 in figure 8, and just
2 I have multiple times repeated structure number 10 is a
3 via, and it is not the metal layers or the capping
4 layer. So all our discussion, all my analysis has been
5 focused on the metal layers, the capping layer, which
6 are the claim features, in claim features. And number
7 10 is a via, it's a filled hole. It's not a layer. Has
8 to cut across multiple layers.

9 So number 10, I identify as via, as shown
10 in Usui. It's irrelevant to our discussion to the 562
11 patent, irrelevant to our declaration. Whether this via
12 is part of this electrode stack or not, it doesn't
13 matter, it won't change my analysis here, and I have --
14 talk about this multiple times now.

15 Q. Is this element 10, is it metal?

16 A. Again, I repeatedly, you know, this via
17 structure in number 10 is irrelevant to our discussion
18 because it -- it's not included in the claim feature.
19 The claim feature about the facet 2 pattern is metal
20 layers, and the capping layer. This via is a filled
21 hole. It cut across multiple layer. It's not a layer.
22 So this via could be forming metal, but it's irrelevant
23 because it's not a cap in the features. It's not --
24 it's irrelevant, it won't change our discussion, won't
25 change my opinion on the matter.

1 Q. I understand. So that was a yes or no
2 question. Is the via a metal?

3 A. I answered question already. It doesn't
4 matter, because all my discussions is on the feature,
5 the patent, the feature here, the patent 2, claim 1,
6 only claims the metal layers and the capping layer.
7 Anything outside is unclaimed.

8 So my analysis, everything is on the metal
9 layer, the capping layer. The via is typically made of
10 metal, but it doesn't matter here. It won't change my
11 professional opinion. It won't change any of the
12 analysis here.

13 Q. I understand that it won't change your
14 opinion. I also understand that in your opinion it does
15 not matter. But, let me ask the question a slightly
16 different way.

17 Is the via a semiconductor?

18 MS. RODRIGUEZ: Objection, asked and
19 answered.

20 A. Counsel, I have answered multiple times.

21 Q. (BY MR. SARWAR) Well, no, I'm going to pause
22 for just a second. I asked you previously whether or
23 not the via was metal, and you gave an answer that it
24 didn't matter. And now I'm asking you if the via is a
25 semiconductor. This is a simple yes or no question.

1 It's a different question from before. And I think, if
2 you're a person of ordinary skill in the art, you should
3 be able to answer. So is the via a semiconductor?

4 A. Counsel, you want to rephrase your question?

5 Q. Yeah. Is the via filled with the
6 semiconductor?

7 A. I have answered it multiple times and I will
8 answer it again, whether this via is not irrelevant
9 because our discussion focus on the metal layers and
10 capping layers; these are claimed features. The via is
11 not a semiconductor.

12 Q. I got the answer at the end there, okay, good.

13 The via is typically metal. It's not a
14 semiconductor. And in your opinion the -- this element
15 10 is not part of the electrode stack, correct?

16 A. Counselor, I have provide this answer
17 extensively. When I analyze 562 patent in claim one, it
18 only -- it disclose the electrode stack as metal layers
19 and the capping layer, and anything outside this is not
20 a metal layer, or capping layer, regardless. It's
21 unclaimed. So -- and this via, as we all agree here, is
22 not a metal layer, is not a capping layer, is not a
23 claimed patent feature, it's not, is not part of that.
24 And I have answered this question multiple times.

25 My analysis has been focused on the

1 claimed features. Which are the metal layers, and the
2 capping layer, not the via. And whether via is part of
3 this interconnect, or anything is irrelevant. It won't
4 change our discussion here. I also have extensively
5 provided those metal layers, the capping layer can be
6 broadly applied to various structure. It can be broadly
7 applied to the gate structure, insulated gate, Schottky
8 gate. Could be applied to interconnect, could be applied
9 to source and drain.

10 Our discussion is focusing on the metal
11 layers, and the, and the capping layer. This is, after
12 all, how 562 claims its electrode stack. It claims its
13 electrode stack includes metal layer and the capping
14 layer, and anything else unclaimed in 562 of claim one.

15 Q. So with respect, you have been referring over
16 the course of your answers about what is relevant and
17 what is not relevant to the discussion at hand. I'm
18 asking you straightforward questions, often yes or no
19 questions, and receiving extremely long paragraphs about
20 all manner of other things that are not pertinent to the
21 actual questions that I'm asking.

22 So, if you could listen carefully to the
23 questions that I ask and answer them to the best of your
24 ability, and try to answer the actual question that I'm
25 asking, I would very much appreciate it.

1 Layers 13 through 15 and 18 through 19 are
2 the layers that you rely upon as the claimed electrode
3 stack, correct?

4 A. Can you refer to -- are we talking about
5 figure 8 in paragraph 36 in my declaration?

6 Q. We are not referring to paragraph 36 of your
7 declaration.

8 A. I'm sorry, page 36, and are you referring to
9 the Usui figure 8?

10 Q. I am referring to your declaration, and
11 paragraph 90 in your declaration.

12 A. Okay, I'm at the paragraph 90 now, let me go
13 through this paragraph. Okay, I see that paragraph 90.

14 Q. Okay. Can you also look at paragraph 89, and
15 review it?

16 A. I will review paragraph 89 now. I see
17 paragraph 89 now.

18 Q. In your opinion, layers 14, 15, 18 and 19 are
19 an electrode stack, correct?

20 A. Again, I provide this answer repeatedly when
21 we --

22 Q. And you -- just provide the answer now --

23 A. And -- Counsel, do you want me to answer your
24 question?

25 Q. Yes, please. In your opinion --

1 A. I'm trying --

2 Q. In your opinion, layers 13, 14, 15, 18 and 19
3 are an electrode stack, correct?

4 A. Again, so when we analyze the matter today in
5 562 patent, claim 1, shows the electrode stack includes
6 those metal layers and the capping layer. And
7 electrostatically include after -- but it's unclaimed.

8 So the claim features that the discussion
9 we focus today are the metal layers and the capping
10 layer. And in the case of Usui, I focus my analysis on
11 the capping layer, metal layers and bottom layer. They
12 are labeled 13, 14, 15, 18 and 19, and these includes all
13 the claim features in -- and then so these are the --
14 these are the -- part of the electrode stack that I
15 analyzed. And if there are other part of electrode stack
16 such as via, they are irrelevant here. They are
17 irrelevant here. So it won't change my analysis.

18 Q. Okay. So do you have an opinion on whether or
19 not element 10 is part of an electrode stack?

20 A. Again, Counselor, I provide answers multiple
21 times that on our matter discussing today, focusing on
22 the metal layers and the capping layer, which are the
23 claim features, includes all the claim features. And
24 via, number 10, and whether it's part of this broadly
25 included electrode is irrelevant, because in the, in

1 Usui, as well as in others. And then, in fact, it's
2 true as well, only those metal layers and capping layer
3 are the claim features.

4 Q. Okay. So you don't have an opinion on whether
5 or not element 10 is part of an electrode stack,
6 correct?

7 A. I already provide my opinion that whether this
8 via 10 is part of electrode stack or not is irrelevant
9 here for the reasons I provide many, many times. And in
10 the end, of course the outside world will be
11 electrically connected to the device 6 of Usui, the
12 semiconductor device layer through this, this metal
13 layers, and capping layer, and the via. And then, this
14 depends on, you know, how you define this electrode
15 stack. But our discussion, as well as when we look at
16 fact 2 pattern, Usui and Yu are only focusing on the
17 metal layers, which are 13, 14, 15, 18 and 19 in Usui's
18 figure.

19 Q. All right. So layer 18 is titanium, right?

20 A. Are you referring to -- are you referring to
21 figure 8 in Usui?

22 Q. I'm referring to layer 18 in Usui.

23 A. Okay, so let me review this so I can give you
24 a correct answer.

25 Q. And I'm referring to your words in paragraph

1 90 of your declaration.

2 A. So let me review this as well, in -- which
3 paragraph are you referring to?

4 Q. Still on paragraph 90.

5 A. Okay, let me review this. I see in paragraph
6 90, it says, Usui disclose the plurality of metal
7 layers. Usui layer 18 comprises titanium.

8 Q. All right. Layer 15 is aluminum or aluminum
9 alloy, correct?

10 A. Here I quote, layer 15 comprises aluminum or
11 aluminum alloy.

12 Q. Layer 14 is titanium nitride, correct?

13 A. Layer 14, again, here I quote on my
14 declaration, layer 14 comprises titanium nitride metal
15 layer.

16 Q. All right. Layer 13 is titanium, correct?

17 A. And continue -- this sentence in my
18 declaration, under layer 13 comprise titanium, both in
19 both the metal layer.

20 Q. And layer 19 is titanium nitride, correct?

21 A. Here I quote, Usui's capping layer 19 is
22 titanium nitride.

23 Q. Is there a difference between titanium and
24 titanium nitride?

25 A. So, in the declaration that I provide very

1 extensive descriptions of titanium and titanium nitride.
2 And then there's a -- they have very, very good
3 performance, and both of them are widely used in
4 semiconductor technology, and to achieve similar
5 results.

6 As a matter of fact, if we go to some of
7 the reference for them in Yu, it shows that, you know,
8 you can -- sometimes you can use titanium, sometimes you
9 can use titanium nitride. So they are very largely
10 interchangeable.

11 Q. Okay. You mentioned discussing the -- or
12 providing very extensive descriptions of titanium and
13 titanium nitride. Can you point to me where in your
14 declaration you provide these extensive descriptions?

15 A. So, here, in page 27, paragraph 26, I discuss
16 titanium as metal layers. And then on page 29,
17 paragraph 71, I provide refractory metal nitrides, which
18 including titanium nitride.

19 I also want to highlight here, I provide a
20 lot of references in exhibits, discuss those metals,
21 including titanium, and titanium nitride, and tantalum
22 nitride, and how they are widely used in semiconductor
23 technology by the effective date of POSITA at the time,
24 who very well understood the characteristics of those
25 metals, including titanium -- titanium, titanium nitride,

1 or tantalum nitride.

2 Q. Okay. In your answer you mentioned page 27,
3 paragraph 26. You might have misspoken there, can you
4 let me know what paragraph on page 27 you're talking
5 about?

6 A. So again, from page 27 to 28, to 29, to 30 of
7 my declaration, as well as, you know, the background, if
8 we go further of previously being -- starting page 22,
9 23, 24, 25, I provide a lot of discussions on these,
10 these metals, including titanium, including titanium
11 nitride, including the tantalum nitrides, as well as
12 how, you know, making contacts. And these are all in my
13 declaration, and I also provide very extensive reference
14 in exhibits above the characteristic, performance of
15 those metals. And these materials are very well
16 known -- widely accepted by the effective date of POSITA
17 at the time, simply a choice that available to them for
18 the, for the -- when they choose metals.

19 Q. You characterize titanium and titanium nitride
20 as very largely interchangeable. Is tantalum nitride
21 also very largely interchangeable with titanium nitride
22 and titanium?

23 A. So you are asking tantalum nitride, TAN, and
24 titanium nitride, TIN?

25 Q. Correct.

1 A. Okay. So let me give you an example from the
2 reference -- from the Yu's reference, Yu's reference
3 number -- paragraph 36 renders it very obvious that the
4 claim 1C is very obvious, because in paragraph 36 of the
5 Yu, it discuss, for example, the capping layer of, of,
6 of this metal layers, and this shows that this capping
7 layer could be a metal. And it provides examples,
8 including titanium.

9 And while not expressing, a POSITA at the
10 time would have understood that these metal layers refer
11 to the list of refractory metal nitrides also in
12 paragraph 36 of Yu, which include titanium nitride, TIN,
13 and tantalum nitride, TAN. So it's -- and later on, in
14 my declaration as well as in paragraph 36 of Yu, it
15 provides thickness, including 600 Angstrom, which is in
16 my declaration, and 200 Angstrom preferably. This, this
17 also in the, in the Yu renders 1C obvious. Although it
18 is all that takes, I further -- all that takes that Yu
19 alone renders 1C obvious.

20 In my analysis I further found Usui that
21 further confirms a POSITA at the time would choose a
22 capping layer that is thicker than the bottom layer, and
23 from all this analysis, especially from the paragraph 36
24 of Yu, you clearly see that titanium nitride, TIN, and
25 tantalum nitride, TAN, are interchangeable.

1 Q. Okay. So can you turn to the Usui reference
2 column 1. This is Exhibit 1004.

3 A. Okay, so you are looking at -- you are talking
4 about Usui reference column 1?

5 Q. That's right. Line 11 to 14.

6 A. So column 1, 11, to 14, let me go through
7 that. I see this here.

8 Q. Okay. So it says that structures fabricated
9 by the process of the present invention are especially
10 useful for forming electrical connections or wiring,
11 such as between active and/or passive devices of
12 integrated circuit structure.

13 Do you see that?

14 A. I see this sentence.

15 Q. Okay. And Usui's talking about structures
16 fabricated by the process of the present invention, Usui
17 is talking about the metal layers that we've been
18 talking about, layers 13 through 15 and 18 through 19,
19 right?

20 A. So, are you -- do you want me to talk about
21 this sentence, or what's your question here?

22 Q. I'm asking --

23 A. Because I see this sentence, but your question
24 is not related to this sentence.

25 Q. So, I'll ask that you listen to the question

1 again.

2 When Usui is talking about the structures
3 fabricated by the process of the present invention, which
4 are literally words that are from the sentence that we're
5 discussing, I'm just confirming with you --

6 A. Wait, wait, wait. Which -- so the sentence
7 you refer to, here I quote it: The structures
8 fabricated by the process of the presenting invention
9 are especially useful for forming electrical connections
10 or wiring such as between active and/or passive device
11 of integrated circuit structure.

12 By reading this sentence, it's clearly
13 that -- very clear that there's no limitation of the
14 metal layers, or the capping layer. Those structures --
15 there's no limitation on how they can apply. They can
16 broadly apply. They just say this structure are
17 especially useful for connections in wiring, but there is
18 no limitation, it could be -- again, I emphasize again,
19 this teaching could be applied to connections, as stated
20 here. Could be applied to the gate structure, as Usui
21 teaches that. It could be in the source, in the drain.
22 Could be in the form of insulated gate, or as in the
23 structure gate, as all in my analysis here.

24 Q. Okay. Are layers 13 through 15 and 18 through
25 19 being used to form an electrical connection between

1 element 10, and some other part of the circuit that's
2 not shown in figure 8?

3 A. So again, in my analysis I've been focused on
4 the metal layers, and the capping layer which are the
5 claim features, which has all the claim feature here.
6 And eventually the outside world will be connected, in
7 Usui's case through the, you know, those metal layers,
8 capping layers, which are the claim features, and
9 through the via, and to the semiconductor device level
10 6, I believe.

11 But then, all our discussion is, you know,
12 all the claim features is the metal layers, and the --
13 and the capping layer. The via itself is a filled hole.
14 It's not a layer. It's not part of the claim features
15 here. And in the end, the outside world could be
16 connected through, you know, those metal layers, via, to
17 semiconductor device, but then the via and everything
18 else is unclaimed, they are not relevant.

19 Q. Okay. Are layers 13 through 15 and 18 through
20 19 in Schottky contact with substrate layer 6? And this
21 is just a yes or no question.

22 A. Layers 13 and -- to layer 19 are not directly
23 connected to semiconductor device layer 6.

24 Q. Okay. So they're not in Schottky contact,
25 correct?

1 A. They are not contact, Counselor.

2 Q. Not in contact, period?

3 A. Not contact.

4 Q. So not in ohmic contact, not in Schottky
5 contact, correct?

6 A. So the layers 13 and 19 -- layers 13 through
7 19 -- this is the layer 13, layer 14, layer 15, layer 18
8 and 19, which are the claim features that we been
9 focusing this discussion on, those are the metal layers
10 and the capping layer. They connect to the device layer
11 6 through a via structure number 10. And the via
12 structure is not a layer. It's a filled hole. So they
13 are not in the claim features. We will not consider --
14 the via 10 will not be on the analysis here, because
15 they are not relevant.

16 And how layer 10, via 10 is connected to,
17 to device level -- to the device 6 is also not discussed
18 in the patent. But they are all not relevant. And
19 eventually the outside world, outside circuit, or other
20 component will be electrically connected to device 6
21 through the 13, the 14, 15, 18, 19 layers, which are
22 layers through the via, which is a hole, filled hole, to
23 device 6.

24 So, if you asking me how the 13 -- layers
25 13, 14, 15, 18, 19 connected to layers 6, it is through

1 via number 10.

2 Q. And is that connection a Schottky contact?

3 A. Can you be more specific? Which, which
4 connection are you referring to?

5 Q. You stated in your answer at the end that
6 layers 13, 14, 15, 18 and 19 connected to layers 6 is
7 through via number 10?

8 A. Yeah.

9 Q. All right. So I'm asking if that --

10 A. So, let me rephrase -- so, let me clear your
11 answer.

12 You are asking me because via number 10 is
13 connected to semiconductor device layer 6, and what is
14 nature of via number 10 connected to semiconductor 6?

15 Q. Yes. Is that a Schottky contact?

16 A. So, again, this contact is irrelevant, because
17 all our discussion, again -- and Counselor, you agree,
18 the patent feature, the claim feature from the patent,
19 claim one is on the metal layers. And it's 13 to 19.

20 But yes, I will answer your question, the
21 via 10 to semiconductor device 6, the nature of this
22 contact is not disclosed, not discussed at all in the, in
23 this patent. It could be many, many different ways. But
24 then again, the teaching -- those metal layers on top, of
25 our claimed feature here, could be broadly applied. And

1 this is another example, it could be broadly applied to
2 whether it's Schottky contact, whether it's ohmic
3 contact, whether it's in gate, insulated gate or so
4 forth. And here this just further confirms this, because
5 in the patent it did not discuss the via, and the nature
6 of the via and the semiconductor device 6. There's no
7 information here.

8 Q. I understand. So let's turn to column 1 of
9 Usui; this is Exhibit 1004. Starting around line 29.

10 A. So --

11 Q. Lines 28, 29. This is column 1, Usui Exhibit
12 1004.

13 A. So column 1 in Usui, and which line?

14 Q. Around lines 28 to 29. Do you see where Usui
15 discusses providing a physical or metallurgical barrier
16 between the silicon and aluminum?

17 A. So I see the sentence here you referring to.

18 Q. Okay. And around line 30, you see that Usui
19 says, or discusses, preventing electro migration and the
20 spiking of the aluminum into the silicon.

21 Do you see that?

22 A. I see this sentence.

23 Q. Okay. And then around line 32, do you see
24 where it discusses migration of aluminum atoms into the
25 underlying silicon?

1 A. I see this sentence.

2 Q. Okay. So earlier you talked a little bit
3 about electro migration. Is this what that's referring
4 to?

5 A. Electro migration is a defined phenomenon. By
6 reading here, it appears -- here I quote, the migration
7 of aluminum atoms into underlying silicon, and, you
8 know, the rest of sentence is giving example of part of
9 the electromigration.

10 Q. So is electro migration like the movement of
11 metal atoms from a conductor into a semiconductor?

12 A. The electromigration is a very complicated
13 process. And atom moving, diffusing into semiconductor
14 is one possible phenomenon.

15 Q. Okay. This is a very, sort of general
16 question. What is causing this?

17 A. You are asking me the cause of
18 electromigration?

19 Q. Yeah.

20 A. So in electron -- in the electromigration, it
21 is very important to have this diffusion barrier layer,
22 and to, to stop this. And then we see that in this
23 titanium layer is everywhere, it's in Yu, in Usui, and
24 the -- affects this pattern as a very effective way to
25 prevent the electromigration.

1 So in 562 patent, you have the bottom
2 layer of this metal layer, which is the titanium, and
3 Usui has this bottom layer as -- the bottom metal layer,
4 which is titanium, and if we go to reference Yu, because
5 this bottom metal layer is titanium, in paragraph,
6 actually, 29 of Yu, in paragraph 29 of Yu, it states this
7 bottom metal layer could be titanium.

8 So those metal layer are everywhere. As
9 you see, it's widely accepted that this titanium bottom
10 layer is effective diffusion barrier layer to provide
11 electromigration. And it, just like I discussed in
12 operation of semiconductor device, you may encounter
13 electromigration under different bias operations. And
14 you also discuss how the atom can move, can diffuse, and
15 that's why it's very important to have diffusion barrier
16 layer. And this layer is practically everywhere in Usui,
17 in Yu, in 562 patent, and using titanium, and it's very
18 well accepted -- it's very obvious for the POSITA at the
19 time, so as in all the combination I analyze.

20 Q. Okay, so is it caused by electrons flowing
21 through the conductor?

22 A. Can you -- you are asking me the -- what, what
23 is your question again?

24 Q. Is the movement of these metal atoms, you
25 know, sorry. I'm going oh rephrase it, rephrase it more

1 clearly.

2 The movement of these metal atoms away
3 from the conductor, is that being caused by electrons
4 flowing through the conductor?

5 A. So, again, you are asking me the general --
6 general thing about electromigration. Electromigration
7 is a very complicated process. A lot of things could
8 trigger it. It could be electrical issues. And it's a
9 very important topic in both semiconductor technology.
10 That's why we need diffusion barrier layer.

11 And if you go to, you know, a patent, it
12 does not -- in fact, it does not distinguish the
13 diffusion barrier layer from its metal layer, and the
14 fact that we see this titanium bottom layer exists
15 everywhere, exists in Yu, exists in Usui, exist in the
16 patent, it renders it very obvious. And the POSITA at
17 the time would very well -- well understood -- would have
18 very well understood to use titanium as a bottom layer,
19 as effective diffusion barrier layer to improve the
20 electromigration.

21 Q. And when you say improve electromigration,
22 what do you mean?

23 A. Counsel, at the very beginning I answer this
24 question already. We -- I already answered this
25 question.

1 Q. Okay, I just dropped into the chat window
2 Exhibit 1005.

3 A. So Exhibit 1005, which is Yu patent.

4 Q. Yeah. I just wanted to do that, because I
5 think we've been discussing Yu and I wanted to make sure
6 that you had it in front of you so you could reference
7 it.

8 Sort of stepping back, just to -- before
9 we move onto Yu, just a quick question about Exhibit 1004
10 and Usui.

11 A. So you want to go back to Usui --

12 Q. Yeah.

13 A. -- Exhibit 1004, okay.

14 Q. That's correct.

15 Usui doesn't expressly discuss
16 transistors, correct?

17 A. There's no limitation on Usui's application.
18 And again, I have been emphasized today, again, again,
19 the Usui's teaching could be, could be broadly applied.
20 Could be applied to interconnect, could be applied to
21 the gate structure as Usui shows it. Could be applied
22 to, you know, a source and drain contact. I provide
23 very extensive analysis in my reference. Usui --
24 there's no limitation of Usui's metal layer, the capping
25 layer, and there's no limitation on their applications

1 in, in, in Usui's patent. It could be widely applied.

2 And a POSITA at the time will understand
3 Usui's teaching could be broadly applied to, to the gate
4 structure, whether it's insulate gate, or Schottky gate,
5 could be source, could be drain, could be interconnect,
6 and so forth.

7 Q. Right. I understand that. Would you say
8 figure 8 of Usui shows a transistor?

9 A. Again, like I state earlier, that Usui's
10 claim, there's no limitation on Usui's metal layers, and
11 they can be widely applied. And, Counsel, you also
12 agree with me they could be applied to the gate, such as
13 Usui structure. It could be applied in the source, in
14 drain, in transistor, in the, in the other semiconductor
15 device. It could be broadly applied.

16 And in my declaration, I provide, you
17 know, all this combination. I show this. But in figure
18 8, there's no information here I could, I could say
19 whether it is or not a transistor, because there's no
20 information just by looking at figure 8, because it did
21 not disclose what the device layer 6, what the structure
22 is for the detail of device structure 6 is.

23 Q. Right. So in the context of transistors, you
24 know what a channel is, correct?

25 A. I understand what channel is.

1 Q. What is a channel in the context of a
2 transistor?

3 A. Channel is to provide electron flow in a
4 transistor.

5 Q. And does, does Usui figure 8 illustrate a
6 channel?

7 A. Again, Counselor, I have answered this
8 question multiple times. There's no information about
9 this -- such a device layer 6. And just by looking at
10 this figure, because all our discussion, everything, and
11 the claim feature is of the metal layers, and capping
12 layer, which is layers 13, 14, 15, 18, and 19.

13 And the device layer 6, I do not find the
14 information on Usui. So based on this, I could not tell
15 you what, what it has, or does not have. This figure, I
16 could not tell you, because it does not show whether
17 there's a channel in this device or not.

18 Q. Okay. Okay. And I -- figure 8 obviously
19 doesn't show enough information to tell whether or not
20 it's illustrating like a transistor gate electrode,
21 correct?

22 A. Again, like I answer many, many times, that in
23 figure 6, there's -- it could be there, you know,
24 whether the, the device substrate layer 6 includes a
25 transistor, or not a transistor, it's not discussed in

1 Usui.

2 Q. All right. Let's turn to Exhibit 1005 now,
3 which I provided earlier. This is the Yu reference.
4 And I apologize to the court reporter on this. This
5 part of the discussion might get slightly confusing
6 because the word Yu is spelled Y-U, and it's referencing
7 this actual reference. It's the last name of the
8 inventor of this -- or at least the invention on this
9 application. So I will try to use the phrase Yu
10 reference in order to distinguish from the word Y-O-U.

11 Okay. The Yu reference is entitled
12 structure and method for a CMOS device with doped
13 conducting metal oxide as the gate electrode, correct?

14 A. I'm reading the title, it seems right.

15 Q. What is a CMOS device?

16 A. CMOS device is a particular semiconductor
17 device composed with two type of MOS transistor. And
18 again, they are not relevant to our analysis here,
19 because I emphasize again and again the claimed features
20 are the metal layers, and the capping layer. And they
21 can be broadly applied to all kinds of a transistor
22 type. Could be applied to source, drain, gate. It
23 could be applied in connection interconnect. It could
24 be ohmic. It could be Schottky. It could be insulated
25 gate structure. It can be certainly applied to the CMOS

1 structure as we see in Yu's title.

2 Q. So at the beginning of your answer you
3 mentioned that the CMOS device is a particular
4 semiconductor device composed of two types of MOS
5 transistors, right?

6 A. The CMOS device typically requires two MOS
7 transistors. And again, our discussion today, the
8 claimed feature metal layers and the capping layer could
9 be broadly applied and it could be applied to contact,
10 could be applied to, you know, Schottky, ohmic, gate --
11 insulated gate, Schottky gate and it could be
12 interconnect and certainly be applied to the CMOS as we
13 discuss today.

14 Q. Do you know whether CMOS devices typically
15 have electrodes that are in Schottky contact with the
16 semiconductor?

17 A. There are many ways to make a CMOS structure.
18 And the MOS, this term refers to the insulated gate, but
19 the Schottky gate is also widely used in the -- it's the
20 C-type structure. As a matter of fact, there are CMOS
21 structure that using Schottky -- two of the Schottky
22 gate structure. And then people, for the benefits of
23 convenience do call it CMOS.

24 So there's two widely used gate structure.
25 One is insulated gate with, with insulated dielectric

1 layer. The other is Schottky gate which has not
2 insulated gate. Both of this gate structure widely used.
3 And the POSITA at the time, by looking at Yu, and in my
4 declaration I also show, by -- goes to POSITA, it's very
5 obvious and motivated for the POSITA at the time that
6 remove the dielectric layer in Yu from -- and they change
7 this gate from insulated gate structure to a Schottky
8 gate structure. And it's a very well accepted and
9 predictably to be successful.

10 So in -- and in my declaration, again, I
11 discuss the Schottky gate and the insulate gate and I
12 discuss the benefits of Schottky gate, such as passive
13 response, nonlinear behavior and so forth.

14 Q. Did CMOS devices have source, drain and gate
15 electrodes?

16 A. CMOS device will have source, drain and gate
17 electrodes. And the teaching in Usui, and in Yu can be
18 broadly applied. The metal layers, and the capping
19 layer, and how they improve electromigration, you know,
20 by limiting the bottom layer. This could be broadly
21 applied to source, drain and the gate of the transistor,
22 of the CMOS.

23 Q. Would you use the same materials to make
24 source and drain electrodes in a CMOS context?

25 A. It is possible to make source and drain using

1 the same material.

2 Q. Would you use the same materials to make gate
3 electrodes and power electrodes in the context of CMOS
4 devices?

5 A. Again, there are many options for the POSITA
6 at the time of the materials they choose to make source
7 and drain, and power electrodes and gate. And by
8 reviewing the Yu and Usui, we see that it's perfectly
9 reasonable and obvious a POSITA of the time to use the
10 metal, thin metal layer, which we, is a claimed feature
11 to use either gate or interconnect and we can also put
12 the POSITA and we can see it's very obvious for them to
13 use the, use the, the same -- the metal layers.

14 And because those -- if you look at Yu and
15 Usui, we see those metal layers, they are
16 interchangeable. They are formed from the electrodes in Yu and
17 Usui. They are interchangeable because the metal layers
18 are formed from the same type of material.

19 And in Yu -- we are discussing Yu here,
20 and in Yu, it causes the bottom layer, a diffusion barrier
21 layer, and this ties back to our discussion of
22 electromigration. And one important purpose of this
23 bottom layer of the metal layer in Yu is to improve the
24 electromigration, a topic that we discussed, and Usui
25 provides guidance limiting the thickness of the

1 bottommost layer that we can include the
2 electromigration.

3 So it's very obvious, and particularly
4 successful for POSITA at the time to combine Usui to Yu's
5 device and use it as a gate in Yu as we see here. So,
6 again, I emphasize this again, the teacher of the Usui
7 can be broadly applied to Schottky gate, to insulate the
8 gate, to ohmic contact, to the source or drain because
9 universally we want to improve electromigration for any
10 of those contacts.

11 Q. Out of curiosity, do you recall what my
12 question was?

13 A. I answered your question very clearly,
14 Counselor. I told you that those metal layers, those
15 contact, the teaching here can be broadly applied. You
16 can use it for source, drain, and gate.

17 Q. But do you recall what my question was?

18 A. I do recall your question here, and I provide
19 very comprehensive answers to your question.

20 Q. I don't mean to quiz you, but what do you
21 think my question was?

22 A. Your question is about whether I can use the
23 metal layers for source, drain and gate, and provide
24 very clear reasoning why it is possible, and why POSITA
25 at the time will do so.

1 Q. Okay, so the -- I think I might -- I maybe
2 have an understanding of why I got sort of a long answer
3 though. It kind of delved into obviousness and so
4 forth.

5 The specific question I had was: Can you
6 use the same materials to make the gate electrode and the
7 power electrodes, specifically in the context of CMOS
8 devices?

9 MS. RODRIGUEZ: Objection, asked and
10 answered.

11 A. Counselor, I provide -- this is the same
12 question I answered. I provide very detailed analysis,
13 and why it is possible. I provide you that by Usui and
14 Yu, their electrode stack is interchangeable. They are
15 from the same metal layers, same type of material.

16 And in Yu's structure, it's a gate
17 structure. And it requires the improvement
18 electromigration. And Usui provides this important
19 guidance to improve this electromigration by limiting the
20 bottommost layer of thickness. And, so it's very
21 reasonable for a POSITA at the time to use Usui's metal
22 layer in Yu's structure, which is a gate, to achieve --
23 improve the electromigration.

24 So I further, just telling you, you know,
25 it's perfectly reasonable and it's the choice for POSITA

1 at the time. They can use those metal layers to use a
2 source, use a drain, use gate. And there are many other
3 references that I provided for that. I provide Adesida
4 which is III-V transistor. I provide very detailed,
5 analysis there. All these combinations that I provided
6 renders this very obvious.

7 Q. (BY MR. SARWAR) So in, in Yu, specifically in
8 the Yu reference, the power electrodes and the gate
9 electrodes are interchangeable; is that your testimony?

10 A. Just -- Counselor, I don't think you are, you
11 are quoting my words correctly. Could you repeat?

12 Q. Sure. In your opinion -- or I will rephrase
13 for you. I won't repeat it.

14 In your opinion, specifically in Yu, not
15 in Usui, not in Adesida, not in any of the other
16 references; in Yu, are the gate electrodes and the power
17 electrodes interchangeable?

18 A. So, can you refer me to which part of the Yu
19 is describing the power electrodes and I will review
20 this paragraph and get back to you?

21 Q. Well, this is the question I had. I was
22 asking you whether or not you would use the same
23 materials to make gate electrodes as you would power
24 electrodes, specifically in the context of CMOS devices
25 in Yu and --

1 A. No, no. Counselor, you are trying to distort
2 it here. I answer your question repeatedly and very
3 clearly. I provide a reasoning why it is perfectly
4 obvious, and perfectly successful for the POSITA of the
5 time to use metal layers, and to use the teachings in
6 Usui and Yu's device, including the variety of the gate
7 structure, insulated gate, Schottky gate. It could be
8 in source and drain, and generally, you know, it's all
9 fine, because there's -- this is already --

10 Q. Dr. Zhao --

11 A. -- POSITA at the time, but if you want me to
12 ask particularly a power electrode in Yu structure, you
13 need to show me this power structure -- power electrode
14 structure and I will go through the paragraph and I will
15 get back to you. You cannot tell me, oh, there's a
16 power electrode, and then, you know -- I need to review
17 this.

18 Q. Okay, so do you know whether or not there is a
19 power electrode in Yu?

20 MS. RODRIGUEZ: Can I just ask that you
21 don't talk over the witness, please.

22 A. What is your question?

23 Q. (BY MR. SARWAR) Do you know whether or not
24 there is a power electrode in Yu?

25 A. I need to go through the reference, but right

1 now, I have been looking at the reference Yu and it is
2 talking about this gate, gate structure, so could you
3 point me to the right direction where you talk about
4 power electrodes so I can review the material and get
5 back to you?

6 Q. The question I have is: Do you know, based
7 off of your review of Yu, whether or not Yu discusses
8 power electrodes?

9 A. Counselor, I answered your question. So this
10 is an expensive material, and I think whether you
11 mention power electrode or not is irrelevant. As I
12 discuss many time, because the metal layer can be
13 broadly applied. But if you want me to discuss the
14 power electrode in Yu, you need to show me the paragraph
15 here so I can review it once again. These are many,
16 many pages. I can't remember everything.

17 Q. I mean, that's fine, if you don't recall
18 whether or not Yu discusses power electrodes, that's,
19 that's a perfectly reasonable answer. And one, by the
20 way, that could be given briefly.

21 Let's turn to paragraph four.

22 MS. RODRIGUEZ: Is now a good time for a
23 lunch break?

24 THE WITNESS: Yes, I would like to have a
25 lunch break.

1 MR. SARWAR: I think that would work
2 great, yes. When would you like to resume?

3 MS. RODRIGUEZ: An hour.

4 MR. SARWAR: Sounds good.

5 MS. RODRIGUEZ: Thirty minutes.

6 MR. SARWAR: Thirty minutes. That would
7 be even better.

8 MS. RODRIGUEZ: Great.

9 MR. SARWAR: See you guys soon.

10 (Recess.)

11 Q. (BY MR. SARWAR) Welcome back. Let's turn to
12 paragraph 4 of the Yu reference, Exhibit 1005.

13 A. So paragraph four.

14 Q. Yes. So it says here that CMOS devices were
15 typically formed with a gate oxide and a poly silicon
16 gate electrode. What is the gate oxide here?

17 A. So we are referring this sentence in paragraph
18 4 of Yu, in that it's generally talking about, you know,
19 the general idea of CMOS device. And it states one way
20 to make CMOS device is to use a gate oxide. And a gate
21 oxide could be many combinations, in Yu it shows it's an
22 oxide material.

23 Q. So, is it -- the gate dielectric?

24 A. Gate oxide could be referring to the gate
25 dielectric.

1 Q. Okay. So in this context, is that what it's
2 referring to? That's my question.

3 A. In the contact, you mean this sentence?

4 Q. Yes.

5 A. In this sentence, again, just by reading, it
6 just tell you this gate oxide, this sentence.

7 Q. Okay. So in the paragraph can you tell
8 whether or not you're talking about the gate dielectric?

9 A. So paragraph 4.

10 Q. Yes.

11 A. Let me review this. In paragraph 4, again, a
12 general discussion about the background of Yu, it
13 discuss gate dielectric, mentions gate dielectric.

14 Q. But you don't know whether or not the gate
15 oxide that Yu was referring to here is referring to the
16 gate dielectric, correct?

17 A. The gate oxide, typically could be used as
18 gate dielectric, but Counselor, you are asking me just
19 one sentence, and one sentence, it just reads gate
20 oxide.

21 Q. Okay. It says here that there has been a
22 desire to replace the gate oxide and poly silicon gate
23 electrode with a high-k gate dielectric and a metal gate
24 electrode, right?

25 A. It sounds generally right, I'm reading this

1 sentence now.

2 Q. Okay. What is a high-k gate dielectric?

3 A. High-k gate is a group of materials, can
4 improve the, the gate performance in the transistor. I
5 want to highlight here, this in the background story and
6 it's irrelevant to, you know, the matter we discuss
7 today, which is metal layers and capping layers.

8 Q. Okay. So the background of Yu discusses this
9 high-k gate dielectric. Yu's disclosure relates to ways
10 of replacing conventional poly silicon gate electrodes
11 and gate oxides with a metal gate electrode and high-k
12 dielectrics, correct?

13 A. Again, in Yu, it tells the, you know, using
14 metal layers, and the capping layers, to use as a -- for
15 example, gate, gate structure here. And again, those
16 metal layers and those -- the capping layer, we see that
17 they are interchangeable with Usui's teaching. And they
18 are forming at the same -- they are forming as metal
19 layers with the same type of materials.

20 So again, you know, I mean, when we see
21 Usui and Yu, it's perfectly obvious for POSITA at the
22 time to combine and to choose that this metal layer, the
23 capping layer to be used in gate structure, in
24 interconnect, in source, and in drain, as well as showed
25 in other combination I analyzed.

1 Q. Okay. Do you think the, the sort of
2 description of Yu's efforts to replace conventional poly
3 silicon gate electrodes is irrelevant to the Yu
4 disclosure as a whole?

5 A. So, again, we are talking about a background
6 story about this patent, Yu's patent, and in background
7 story, the patents can discuss many broad range of
8 topics.

9 Q. So in this context, specifically for Yu, this
10 is irrelevant to your analysis, right?

11 A. Can you repeat the question again?

12 Q. This context that's set forth in the
13 background of Yu is irrelevant to your analysis,
14 correct?

15 A. You mean relevant or irrelevant?

16 Q. Irrelevant.

17 A. So, again, in my analysis, for the whole
18 matter today, we been focusing on the metal layers and
19 the capping layer, as shown in 562 patent, claim 1. And
20 in all my analysis, I discuss, you know, those metal
21 layers and capping layer. And one of the analysis in
22 Yu, which we're discussing right now, I show that by
23 combining Usui and Yu, it is very obvious, because Usui
24 and Yu shares the same electrode stack, which features
25 the -- which is formed from the metal layers of the same

1 type of materials, and, you know, and in -- and I
2 already discussed, it's very obvious that motivated --
3 it would be very motivated for a POSITA at the time to
4 combine Usui's -- those metal layer, the capping layer,
5 to Yu's structures such as gate.

6 And as we see here, those teachings can be
7 broadly applied. And so, you know, it's the -- my
8 analysis for the whole matter will be focused on the
9 metal layers and the metal -- and the capping layers,
10 because these are the claim features, okay.

11 And the others, you know, they are not
12 important to our analysis.

13 Q. When you say the others, what are you
14 referring to?

15 A. So, let me just -- let me give you a little
16 bit more clear discussions. It's that if we look at
17 the -- look at this gate structure in Yu, we are looking
18 at the metal layers on top with the oxide dielectric
19 layer, and metal layers, which are the claim features in
20 562 patent, as well as Usui and so forth. Those metal
21 layers are conducting, while the dielectric layer is not
22 conducting.

23 So for a POSITA at the time when they do
24 their analysis, and combination, they would never have
25 understood that the -- that the dielectric layer is part

1 of this -- of that feature, or of the electrode stack,
2 because it is not. It is not conducting. As a matter of
3 fact, if you go to 562 patent, it shows the same thing as
4 Yu, that the metal layers over a dielectric.

5 Q. What is your understanding of the term metal
6 layers?

7 A. Metal layers -- you want me to refer to the
8 562 pattern or Usui or Yu here?

9 Q. Are you -- you use the word metal layers in
10 your previous answer --

11 A. Okay.

12 Q. -- I'm just trying to get a sense of what your
13 understanding of the term is.

14 A. Okay, here, here we are discussing Yu here,
15 and I would say that the metal layer, I would love to go
16 to my declaration and we have one the figures that --
17 with color -- or let's see -- give me one second.

18 So I may not be able to get to that, but
19 just give me one second, let me go to a clear figure and
20 then in the context of Yu patent I will tell you what the
21 metal layers that I refer to.

22 Q. Well, the question I have is actually --

23 A. Okay, I have it now. Do you want me to go
24 through the metal layers in Yu's contact, or?

25 Q. No, the question I have is what is your

1 understanding of the term metal layers?

2 A. Yeah, the metal layers are layers from the
3 metal, and I want to highlight that in our discussions
4 and we have very clearly seen those metal layers in 562
5 patent, that's very clear, with multiple layers, and
6 with the bottom layer and the cap layer.

7 And in Usui, again, we have went through
8 very extensively in Usui, again, we have very clear that
9 the metal layers, right -- and that we very strongly
10 discuss that via is not top of the metal layer. And that
11 in terms of what the -- in terms of the -- in Yu's
12 contact, the metal layers are formed by metals. Metals
13 are refer to metal nitride, as discussed in Yu. And we
14 can refer to capping layer 226, as well as the metal
15 layers 218, 220, 222, and 224, and these are the metal
16 layers that referred in Yu.

17 Q. In Usui why is element 10 not a metal layer?

18 A. You are going back to Usui?

19 MS. RODRIGUEZ: Object --

20 Q. (BY MR. SARWAR) That's right.

21 A. Okay, so be specific, because we are looking
22 at Yu and now you want me to go back to Usui.

23 Q. That's fine, so the question I asked was in
24 Usui --

25 A. Okay, and you want me to go back to Usui?

1 Q. Correct. In Usui, why is element 10 not an
2 element layer -- sorry. Why is element 10 not a metal
3 layer?

4 A. So, so --

5 MS. RODRIGUEZ: Objection, asked and
6 answered.

7 A. So I ask -- answer this question multiple,
8 multiple times today and I can go from the very
9 beginning, when we analyzed the -- when we look at 562
10 patent, and the claim one clearly state that electrode
11 stack includes metal layers and the capping layer.
12 Anything that is for this electrode stack that is not
13 metal layer or capping layer is unclaimed and
14 irrelevant.

15 And in the Usui, I provide a reference to
16 Usui. Usui has a via structure which is number 10 that
17 you are asking about. And in previous answers I already
18 provided via is a filled hole. So it is cutting across
19 multiple layers. So it is not the metal layers that we
20 discuss.

21 And whether -- your question, whether via
22 is metal, whether via is part of electrode, it doesn't
23 matter. It's irrelevant to us because the claim feature,
24 all my analysis has been focused on the claim features,
25 which are the metal layers and the capping layer, and the

1 via is not a layer. And I have provide very extensive
2 discussion and, you know, the number 10, the fact that
3 you have this -- number 10 does not change my analysis.

4 At end of the day, you know, outside world
5 will be connected through the metal layers, the capping
6 layer, which are features to the via which is metal and
7 to the semiconductor device which is number 6 in Usui,
8 but we been through this. But again, we focus only on
9 the metal layers and the capping layers -- those are the
10 claim features. Those are the, you know, the -- my
11 analysis has been focused on.

12 Q. (BY MR. SARWAR) So in Usui, this is, you know,
13 Exhibit 1004, element 10 is not a metal layer because it
14 spans multiple layers?

15 A. I already answer this question very
16 extensively. Counselor, you are changing concepts here.
17 I already told you that via is not part of -- not a
18 metal layer. And in reviewing this patent, we declared
19 features that patent are the metal layers and the
20 capping layer, via cut cross multiple layer. So it's a
21 filled hole. And it's metal. But again, this is not
22 part of the electrode stack that -- it's in the, in the,
23 in the patent 562, or not in the -- does not include in
24 the claim feature.

25 So whether -- I already answer your

1 question, but again, whether this via, this via is not
2 part of the analysis here. It doesn't matter.

3 Q. Now, I understand your conclusion that the via
4 doesn't matter. I'm trying to figure out why the via is
5 not a metal layer, and this is sort of where my
6 questions are trying to go. From your answers, it seems
7 like a metal layer can't cross -- can't cut across
8 multiple layers. Is that fair?

9 A. Counselor, we don't need to play this game. I
10 gave you very clear answer multiple times. And I told
11 you why our analysis will be some metal layers, and the
12 capping layer, because they are claimed features.
13 Because this is -- in the 562, this is in Usui, this in
14 Yu and so forth. And via -- I also answered your
15 question, via is a metal. But again, it's not part of
16 the claim feature, right? So we are not focusing on
17 discussion on via. And then you are intentionally
18 distort my answer.

19 Q. Okay.

20 A. And I hope, you know, we just move on,
21 because, you know.

22 Q. I don't intend to distort your answer.

23 MS. RODRIGUEZ: Don't interrupt the
24 witness.

25 Q. (BY MR. SARWAR) I don't intend to distort your

1 answer at all. All I'm trying to do is figure out why
2 the via is not a metal layer?

3 Now, is it not a metal layer because it's
4 a hole that has been drilled into layers and then filled
5 in? Is that why it's not a metal layer?

6 MS. RODRIGUEZ: Objection, asked and
7 answered.

8 A. Counselor, I answered it multiple, multiple
9 times now. And the 562 -- let's go back to 562 patent,
10 claim one. It clearly state electrode stack includes
11 multiple -- includes metal layers and capping layer.
12 That's, that's the, the central part that we discuss.
13 And via is not a layer. It's a filled hole. It's not a
14 metal layer. It's a filled hole. I answer your
15 question. The via is not a metal layer, it's a filled
16 hole. It cut cross multiple layer. It's very obvious
17 via is not a metal layer.

18 Q. (BY MR. SARWAR) I actually appreciate the
19 clarity of that answer. Now I completely understand
20 your position.

21 Does the 562 patent discuss vias?

22 A. 562 patent does not include vias. But then in
23 the reference Usui, we have vias, but these -- that's
24 why via is irrelevant, right, because 562 patent has
25 been focused -- the focus on the metal layer, the cap

1 layer. So that's why the via is not -- nowhere, not in
2 the claim features. The via is irrelevant in our
3 discussion. Irrelevant to 562 patent, and so forth,
4 because we have been going through multiple times this
5 claim feature, which are the metal layers, the capping
6 layer could be broadly applied to gate structure,
7 insulated gate, could be Schottky the gate, could be
8 ohmic contact, could be source and drain, could be
9 interconnect.

10 Q. Okay. I'm going to ask you to now move to
11 Exhibit 1005. Now we're -- this is the Yu reference.
12 We're away from Usui. We're away from the 562 patent.
13 We're now Yu reference.

14 So can you turn to paragraph 29? And here
15 in paragraph 29 of Yu, you see that there's a description
16 of the diffusion barrier slash protection layer 218,
17 correct?

18 A. I'm reviewing the paragraph now. Correct, I
19 see this sentence that paragraph 29 and some
20 embodiments, diffusion barrier, protecting layer 218 is
21 form over the high-k dielectric 216. And again, this is
22 the point I made earlier that this diffusion barrier
23 layer, as the bottom layer of the metal layers, and we
24 see it everywhere. We see it in Usui. And we see it in
25 Yu here, and then we see it in the patent 562.

1 And I believe in paragraph 29, it disclose
2 that it could be taking in, you know, and in 562, the
3 bottom layer of this metal layer is -- metal layer is the
4 titanium. And in here in Yu, it says that it's bottom
5 diffusion barrier layer is titanium. And in Usui, also
6 shows that this bottom layer of the metal layer, which
7 are the claim features, is titanium.

8 So again, we see this titanium over all
9 the place, and the Usui clearly state this titanium is a
10 diffusion barrier layer. So it's all in the combination
11 I analyzed. It's obvious here.

12 Q. Okay. So the question I asked was whether or
13 not you saw the discussion of, you know, the diffusion
14 barrier slash protection layer 218; the answer to that
15 question is yes, correct?

16 A. I answered. I see this sentence. I think 218
17 is the barrier diffusion layer, and I provide --

18 Q. Additional context?

19 A. And that's all in my declaration.

20 Q. Okay, so what is the purpose of layer 218?

21 A. So 218 is a diffusion barrier layer, and it
22 helps to, helps to mitigate the electromigration and we
23 have extensive discussion electromigration, and that's
24 why I provided my analysis that when Usui provides a
25 guidance to improve electromigration, and Yu, it's

1 perfectly obvious and perfectly acceptable POSITA at the
2 time will combine Usui and Yu and use Usui's teaching of
3 limiting this bottom layer, diffusion barrier layer
4 thickness to include the electromigration.

5 So it's perfectly fine and reasonable and
6 perfectly acceptable for POSITA at the time to use Usui's
7 idea of this -- of the, of the metal layers and include
8 electromigration to the Yu's device, such as use as a
9 gate structure we discuss here.

10 Q. And in your view, you'd still need layer 218
11 if Yu had nothing to do with high-k dielectrics, right?

12 A. Well, layer 218 for -- what's your question
13 again?

14 Q. I understand your opinion to be that layer 218
15 is useful in the context of Yu, even if Yu had nothing
16 to do with high-k dielectrics; is that correct?

17 A. So let me -- so again, we been focusing on
18 those metal layers today. And those metal layers, these
19 are the claim features. If I see Yu and I see Usui, and
20 then anything it is a true of POSITA of the time that
21 chose these materials, those layers, to their -- to the
22 problem they have, and I already get very extensive --
23 because Usui and Yu see those metal layer, they are
24 interchangeable. They are from the same type of
25 material. And this is a POSITA of the time, they can

1 make those combinations and in my analysis provide a lot
2 of examples. And then, this is -- POSITA at the time,
3 he will -- it's very obvious, and very predictable,
4 successful for him for making those combinations, making
5 those metal layers to achieve their result.

6 Q. So in the context of Yu, if you didn't have
7 layer 216, would you still need the diffusion barrier
8 slash protection layer 218?

9 A. Again, we have been focusing on, discussing on
10 those metal layers, and we already discuss from Usui and
11 Yu, you know, you know, from Usui's structure and Yu
12 structure electrode stack, we are formed with metal
13 layer of similar type of materials. And then Yu, here
14 in this paragraph calls this bottom metal layer as
15 diffusion barrier layer to improve electromigration.

16 Usui has provided guidance to improve the
17 electromigration. So it's perfectly fine to -- it's a
18 choice for the POSITA at the time to make those
19 combinations to achieve this goal. And you are asking me
20 that if Yu, a POSITA of time, remove this diffusion
21 barrier layer -- it's their choice. But if they remove
22 this diffusion barrier layer they are not achieving the
23 improving the electromigration.

24 Q. Sorry --

25 A. One purpose for this diffusion barrier is to

1 improve electromigration.

2 Q. Dr. Zhao, I don't want to talk over you. But
3 the problem is sometimes I'll ask a question, and you
4 will answer sort of a different question, right.

5 So here we're not talking about removing
6 layer 218. I'm asking about in the context of Yu -- and
7 I'm going to try to say this slowly so you can listen to
8 all the parts. In the context of Yu, the Yu reference,
9 if you removed layer 216, 216, would you still need 218?
10 And again, forgive me, I did not mean to try to talk over
11 you or anything like that, but when you started talking
12 about the removal of the 218, I wanted to step in and say
13 actually I had a separate question. This is the question
14 I'm asking.

15 A. So can you repeat your question again?
16 Because you are now referring to different type. So can
17 you go to the figure and tell me your question and if
18 you are removing a particular layer, you let me know
19 which layer you are removing.

20 Q. One hundred percent.

21 MS. RODRIGUEZ: Let him finish when he
22 talks, please. Please try not to interrupt.

23 MR. SARWAR: Sorry, are you referring to
24 him or me at this point?

25 MS. RODRIGUEZ: To you, counselor.

1 MR. SARWAR: Sorry, I'm trying not to
2 interrupt him.

3 Q. (BY MR. SARWAR) So figure 2E?

4 A. Okay, I have figure 2E, yes.

5 Q. Okay. The layer I'm talking about removing is
6 layer 216.

7 A. So you want me to change the structure in Yu
8 by removing one layer?

9 Q. Correct.

10 A. So you want me to change, change Yu's
11 structure?

12 Q. Correct.

13 A. Okay.

14 Q. So --

15 A. And what's your question here?

16 Q. The question is, would you still need
17 diffusion barrier slash protection layer 218?

18 A. Again, as I stated multiple times, there's a
19 need to improve electromigration. In Yu's structure, in
20 source, drain, and gate, transistor, interconnect, it's
21 very important problem. And then the multiple times I
22 emphasize that in, in Usui, has provided that guidance.
23 Okay. So it's very important for any of the contact
24 that form, and the teaching in Usui can be generally
25 applied to Schottky gate, to dielectric gate, or to

1 ohmic contact, so forth.

2 So the question you are asking is, for
3 example, if we remove the dielectrics, right, and then,
4 again, it will be benefit from the teaching, because
5 those metal layers, and the way to improve
6 electromigration, it's a universal need and benefit to
7 all those contacts. That's why it is obvious to make
8 those combination. And that is why a POSITA at the time
9 will be motivated to making those combinations and to
10 solve the problem they face, as I extensively discussed
11 in my declaration.

12 Q. Okay. If you replaced layer 216 with a
13 conventional gate oxide dielectric, like the one
14 described in Yu, does this universal benefit of the
15 diffusion barrier slash protection layer 218 still
16 apply?

17 A. So you need to give me more content here. So
18 you want to remove 216, and then there is a 214 layer
19 there, is that still there?

20 You also need to put into -- if you're
21 removing 213, are you adding another layer? And what's
22 the nature of that layer? And if 214 is there, is 214
23 there? And then if, you know, you are a semiconductor or
24 not. You need to provide me detailed description because
25 you are changing the figure from Yu. I need to see what

1 the picture is, and then provide you answer.

2 Q. I completely appreciate that. And this is
3 really helpful. So, for this particular hypothetical,
4 we're replacing layer 216 with a conventional gate oxide
5 dielectric layer. No other changes. So, no change to
6 layer 214 --

7 A. So, so --

8 Q. And -- I'm sorry, did you have a question?

9 A. Yeah, because this is not clear to me. 216 is
10 also a dielectric. You are saying replace the
11 dielectric with another dielectric. Then the structure
12 stays the same.

13 And again -- but I say -- but again, the
14 benefits here are -- and the idea is the same. This
15 teaching Usui has that with those metal layers and
16 capping layer, and the fact Yu calls this bottom layer
17 diffusion barrier layer to improve electromigration, it
18 is a well known issue.

19 And this structure at this, you know, the
20 enhancement, teach of the improve electromigration can be
21 broadly applied to gate, to the source, to the drain, to
22 the interconnect. There's no limit in this metal layer
23 in this structure, and the importance of improved
24 electromigration here, because it's important in all
25 those contacts. And I already answered this question

1 multiple times, and I answer you again, but you are still
2 working on your, you know, the removing dielectric, but
3 again, I'm answering the question again for you.

4 Q. Okay, I appreciate that. So, I believe I have
5 the answer to the previous hypothetical. This next one,
6 this next question I have is again focused on figure 2E
7 of Yu. If you removed, did not replace, just removed,
8 both layers 214 and 216, so both dielectric layers,
9 would you still need the barrier slash protection layer
10 218?

11 MS. RODRIGUEZ: Objection, form.

12 A. I answer this question multiple times now, but
13 I want to, you know, answer again.

14 First of all, this teaching of those metal
15 layers, capping layer thicker than the -- thicker than
16 the bottom layer, this teaching is universal. And it
17 could be in the interconnect, the source, drain, gate.
18 If we discuss the gate case, which Yu's case is
19 discussing right now, they are two commonly used -- the
20 gate structure, one is insulated gate, as Yu has, which
21 has a dielectric layer. One is Schottky gate, which
22 is -- we saw those dielectrics, we saw those oxide
23 Schottky gate.

24 And in my analysis I have provided
25 reference of Adesida, that is clearly shown that a POSITA

1 at the time would be clearly motivated to remove the
2 dielectric layer to achieve the Schottky contact.
3 Because this is both the insulated gate structure and
4 Schottky gate structure are very well known that they
5 inform the POSITA at the time. They are very well and
6 familiar and competent to make those changes, the choice
7 that they make.

8 And in my declaration I discuss very
9 detailed benefits of a Schottky gate and so forth. So
10 those metal layer, the teachings, including those --
11 limiting the bottommost thickness and improve the
12 electromigration, could be very well applied to, in Yu's
13 case here, as well as in your case removing the
14 dielectrics to make Schottky gate because these are all
15 very well accepted ideas, and the POSITA at the time well
16 understood this, would have understood this. And they
17 were very motivated -- and it's obvious for them.

18 Q. (BY MR. SARWAR) Okay. Is layer 214 in Yu
19 figure 2E a conductive layer?

20 A. Let me go to the reference. You are referring
21 to 214, this layer, right?

22 Q. That's correct.

23 A. Yeah, 214 layer, the 214 layer in Yu's
24 reference is a dielectric layer. It is typically not
25 conducting.

1 Q. Okay. Is -- I'm going to ask the same
2 question about layer 216. Is layer 216 in Yu figure 2E
3 a conductive layer?

4 A. Well, I have answered this question also
5 previously. So, and in my analysis we've been focusing
6 on the metal layers of the electro, electro part. And
7 the metal layers, they are conducting. And they're from
8 Yu 214 and 216, they are not conducting. So they are
9 not in the claim features of patent 562. They are
10 not -- they are not in my analysis.

11 So the fact that you have 214 and 216,
12 they will be not relevant and won't change my analysis
13 here, because all the claim features are the metal
14 layers. And the POSITA at the time, by looking at this,
15 they will have very well understood that the 214, 216,
16 they are not the metal layers, they are not part of the
17 electrode stack. They are not -- they are not that the
18 claim features.

19 As a matter of fact, if you go to 562
20 patent, you see the same thing, that the metal layers,
21 those electrode stack formed by metal layers will be on
22 the dielectric layers. The same thing in 562. The fact
23 that we see Yu here disclose this, renders the 562 patent
24 obvious.

25 Q. All right. So elements 230 and 231 in figure

1 2E of Yu, those are gate stacks, correct?

2 A. I draw the yellow box on 230, 231 just to
3 highlight this component of Yu as important. But then
4 again, the analysis has been focusing on the metal
5 layers, of this electrode stack, because metal layers
6 conducting. Dielectric or oxide does not conduct. So
7 it's very clear.

8 And then for the, for the POSITA at the
9 time, when looking at this, Yu, 230, 231, it's very clear
10 to them that the features are the -- that the features
11 are the 2 -- are the metal layers and the capping layer,
12 they would never, would never have understood that the
13 oxide layers or dielectric layer are part of these
14 electrodes. And so, it is, again, obvious to them. And
15 then, and then the combination of Yu and Usui, again, as
16 many of the combinations I provided renders the 562
17 obvious.

18 Q. All right. The electrodes that you can see in
19 Yu figure 2E don't make ohmic contact with the
20 semiconductor, right?

21 A. You are referring to -- what are you referring
22 to in Yu's figure?

23 Q. Elements 230 and 231.

24 A. Again, I draw this yellow box to call
25 attention for those -- and again, I emphasize again and

1 again our discussion 562 patent, Usui and Yu, the claim
2 features are the metal layers, and at the time were not
3 considered the dielectric layer as part of the metal
4 layer.

5 And for this particular structure, you can
6 call it whatever, of course, but our discussion will be,
7 will be on the metal layers, and in this particular case,
8 you can put the whole thing of 230 on the semiconductor.
9 But again, this will be the choice for a POSITA at the
10 time, you know. The teaching here is universal. They
11 can be on the insulated gate. Could be on Schottky gate.
12 Could be on, you know, the source and drain. It could be
13 on interconnect, as the combination I showed.

14 Q. The question I had was whether -- what figure
15 2E is showing. Is it showing electrodes making ohmic
16 contact with the semiconductor material? This is a
17 simple yes or no question.

18 A. Again, you need to be more specific. So which
19 part of 2E are you referring to? And I can answer. But
20 again, I answered multiple times now.

21 Q. I'll -- so Yu calls, the Yu reference calls
22 element 230 and 231 metal gate stacks, correct?

23 A. So which part are you referring to in Yu? Let
24 me review this.

25 Q. Yeah, elements 230 and 231.

1 A. Can you direct me to the right -- so I can --

2 Q. Yes. Paragraph 37 of Yu.

3 A. I'm reviewing this now.

4 Q. Thank you.

5 A. Okay, I have this paragraph. What's your
6 question again?

7 Q. The question is, I'm going to break it down
8 into two different questions to make it easier, more
9 concrete.

10 The first metal gate stack, 230, is that
11 making ohmic contact with semiconductor material?

12 A. I'm confused here, because it says the second
13 metal gate stack 231, so you talk about 230, right, the
14 first metal stack. What are you referring to, 230? Or
15 231?

16 Q. I'll repeat the question again. The first
17 metal gate stack, 230, is that metal gate stack making
18 ohmic contact with semiconductor?

19 A. Again, I've been answering this question many,
20 many times that the teaching Usui has, the -- in form of
21 those metal layers, and the capping layers, and the
22 benefits of electromigration could be broadly applied to
23 gate, to source, to drain, to interconnect, and, and
24 then the, you know, the metal gate in Yu can -- I draw
25 the yellow box to highlight this 230, which Yu

1 highlights here.

2 But the POSITA at the time will be very
3 well understood that what is metal gate, which is --
4 you're asking now, and they will very well understood
5 that the teaching from Usui and everything, the electrode
6 stack refers to the metal layers. Because the oxide is
7 not part of the metal layer. Oxide is not conducting and
8 I have answered this many, many times.

9 And in terms of a gate, I also answered
10 you many, many times. They are two commonly ways to make
11 gate; they are insulated gate, and they're Schottky gate.
12 Insulated gate has a dielectric. Schottky gate, we saw
13 that (indiscernible) contact semiconductor. It's a very
14 well widely known structure by the fact that a POSITA
15 can -- very freely they can choose what structure they
16 work on. So, it's very well accepted concepts here. And
17 you know, that's all -- again, in my declaration I
18 provide all detail, everything here in my declaration.
19 And I answered your question several times now.

20 Q. So the answer is, just so that I am clear,
21 these are insulated gate electrics; is that correct?

22 A. So are you referring to the figure 2E -- which
23 figure are you referring to?

24 Q. Figure 2E.

25 A. Okay. So, again, in figure 2E, you may have

1 used an insulated gate as example, but like I
2 extensively explain, that it's a choice, it's a matter
3 of choice for the POSITA at the time to change from the
4 insulated gate by, by choose the other gate, by simply
5 removing the insulating dielectric layers. And the
6 later I provide reference, Adesida, for example, to show
7 that it's a very common practice, a very well known, by
8 the time of POSITA, they can make those changes.

9 So even though Yu shows that insulated
10 gate in their figure, that doesn't matter here, because
11 POSITA can choose what they want to do when they see
12 those references.

13 Q. Understood. Okay. Let's turn to ground 2 of
14 your arguments. Paragraph 112 of your declaration?

15 A. I'm trying to find this, so, if we're on
16 ground 2, which paragraph are you referring to?

17 Q. I'm looking at paragraph 112 of your
18 declaration, it's Exhibit 1002.

19 A. 112, okay. So you are referring to paragraph
20 112, just give me a few minutes, go over this.

21 Okay, so I have -- I'm at paragraph 112
22 here.

23 Q. Okay. Here you're analyzing claims 12 and 17
24 of the 562 patent, correct?

25 A. Correct.

1 Q. And you discuss the Yu references interfacial
2 dielectric layer 214, and high-k dielectric layer 216,
3 correct?

4 A. I'm generating this whole section, I'm
5 discussing that a POSITA would be -- have been motivated
6 to implement Yu's device as a III-V device with a gate
7 insulator, as taught by Yu. So combination of Usui or
8 Yu will render claims 12 and 17 obvious and whole
9 paragraph 112, 113, 114 as giving details about claim 12
10 and claim 17 obvious.

11 Q. Okay. So you say that layers 214 and 216 in
12 Yu -- sorry, try that again.

13 You say that layers 214 and 216 in the Yu
14 reference underlie this metal diffusion barrier slash
15 protection layer 218, correct?

16 A. So you are referring to my, paragraph 112 on
17 my declaration. I say here, you expose multilayer
18 active III-V semiconductor device, transistor featuring
19 a interface dielectric layer 214 and a high-k barrier
20 216 underlying a metal diffusion barrier, protection
21 layer 218.

22 Q. Right. So layers 214 and 216 underlie layer
23 218, correct?

24 A. I just read the sentence to you.

25 Q. So do you agree with my statement?

1 A. I read the sentence to you, so the sentence I
2 already provided. It's in my declaration.

3 Q. Okay, so you don't agree with my statement?

4 A. What is your statement? Because I provide --
5 you want me to refer to my sentence in my paragraph. I
6 read through this paragraph to you. I did not get a
7 specific question here. You first asking me, you agree
8 with me. And then later say, you do not -- you do not
9 agree with me. So I don't know what you are referring
10 to here, Counselor. Can you be specific so I can answer
11 it -- your question.

12 Q. Sure, I'll try to be specific. This is a yes
13 or no question. Layers 214 and 216, in your opinion,
14 underlie layer 218? This is a yes or no question.

15 A. Again, in my declaration, I have provided
16 previously and noted, Yu disclose a multilayer active
17 III-V basin semiconductor device, featuring interfacial
18 dielectric 214 and a high-k dielectric layer 216,
19 underlying a metal diffusion barrier protecting layer
20 218. I believe I answered your question.

21 Q. Okay. In paragraph 114, you explain that it
22 would have been obvious to implement the electrical
23 contact of Usui with Yu's gate insulator layer, correct?

24 A. In this whole section, I discuss that why a
25 POSITA at the time will be motivated to implement Usui's

1 device as a III-V device with a gate insulated layer as
2 taught by Yu.

3 Q. When you refer to Yu's gate insulator layer,
4 you're referring to both layer 216 and 218, correct?

5 A. I'm referring in this whole section. Again, I
6 been telling -- I been showing that for the reasons I
7 already discussed extensively, I won't go there, but it
8 is very obvious for a POSITA at the time to use Usui's
9 structure in Yu's device such as gate.

10 As I many, many times I explain today,
11 because Usui's teaching is universal, these metal layers,
12 the capping layer to enhance electromigration. Benefit
13 can be applied to interconnect, can be applied to the
14 gate structure, which includes Schottky gate, or
15 insulated gate. Can be applied to source or drain. It
16 doesn't matter what these -- this contacts are. This
17 whole idea, this could be broadly applied. And here in
18 claim -- in this whole section as well as in 114, I am
19 talking about these points.

20 Q. To be clear, here you are describing a
21 specific combination, are you not?

22 A. I'm talking about the combination of Usui and
23 Yu, and I answered very clearly previously how, you
24 know, this Usui and Yu combination make it obvious for
25 claim 12 and 17. And in paragraph 112, 113 and 114 we

1 discussed all these points.

2 Q. Okay. So in paragraph 114, you used the
3 phrase Yu's gate insulator layer, correct?

4 A. So which part are you referring to? I need to
5 see --

6 Q. Second line on page 47.

7 A. Forty-seven, here I told in my declaration to
8 a POSITA it would have been obvious to implement the
9 electro contact Usui with Yu's gate insulating layer
10 because Usui disclose the importance of improving
11 electromigration characteristics and such layers are
12 commonly provided under gate structure to address gate
13 leakage and so forth. This is in my declaration and in
14 the previous few, you know, answers I stated that this
15 whole section, everything here is discussed, the
16 combination of Usui and Yu that renders claim 12 and 17
17 obvious.

18 Q. Right. So when you use the phrase, Yu's gate
19 insulated layer in the sentence that you just read, I'm
20 confirming that you were referring to both layer 216 and
21 218 of Yu?

22 MS. RODRIGUEZ: Objection, asked and
23 answered.

24 Q. (BY MR. SARWAR) Is that correct?

25 A. I have answered the question multiple times.

1 The whole section is about -- and also I explain,
2 explained this extensively, is that using Usui's
3 electrode stack to the Yu structure, such as a gate,
4 which includes dielectric layer and it's perfectly fine
5 and reasonable, because a POSITA of the time would use
6 Usui's teaching because the benefit of improved
7 electromigration and so forth -- we went through
8 multiple runs now.

9 And then the Usui's teaching here is
10 universally broad. It could be applied to interconnect.
11 It could be applied to gate structure. It could be
12 insulated gate or Schottky gate. It could be source and
13 drain. And again, in here, I provide very detailed
14 discussions why combining Usui and Yu made the claim 12
15 and 17 obvious, and I have answered your question
16 repeatedly, why it is obvious, and why we made this
17 combination, yeah.

18 Q. Did you provide a drawing of what you call the
19 combination of Usui and Yu?

20 A. You want me to refer to a particular figure or
21 you want -- you want to see that in this paragraph C,
22 whether it -- in paragraph C of, of my declaration? I
23 need to go through this, but just by looking at page 46
24 and page 47 of my declaration, I do not see a figure
25 here.

1 Q. When you say paragraph C, what are you
2 referring to?

3 A. I'm referring to C, in my section here, on
4 page 46, it's claims 12 and 17, a POSITA would have been
5 motivated to implement, use this device as III-V device
6 with a gate insulated layer as taught by Yu.

7 Q. Okay, got it. So let's turn to Usui, that's
8 Exhibit 1004, figure 8?

9 A. Okay, so we go back to Usui and figure 8.

10 Q. So is this the embodiment of Usui that you're
11 modifying in view of Yu?

12 A. So again, I want to emphasize that I have
13 spent plenty of time to discuss that we can very broadly
14 to apply Usui's teaching, which are the metal layers in
15 how to include electromigration by limiting the bottom
16 layer of those metal layers to the benefit of Yu's
17 device, such as gate structure. In figure 8 in Usui is
18 one embodiment that discussed in Yu -- in Usui's patent.
19 And it's also, has been referred in my declaration.

20 Q. Okay. Okay, what I'm trying to do is
21 concretely determine what your combination is. In
22 paragraph 114 you say that, it would have been obvious
23 to implement the electrical contact of Usui with Yu's
24 gate insulator layer. In paragraph 112 you say that,
25 Yu's gate insulator layer is layer 214, and 216. I'm

1 now looking at Usui, and trying to find out where you're
2 putting Yu's layers 214 and 216.

3 Do you know where in figure 8 of Usui you
4 are putting layers 214 and 216 from Yu?

5 A. Again, Counselor, I've been answered this
6 question multiple times, and when we looking at the
7 patent features of 562, the claimed features, these are
8 metal layers. These are the -- which are conducting,
9 and then if we look at Yu's patent, which including --
10 Yu's patent, Yu's structure, the dielectric layers.
11 Dielectric layers or oxide layers, they're insulating.
12 They're not conducting.

13 So a POSITA of the time when making their
14 changes, when, when having their problem, they would have
15 understood that -- be focusing on the metal layers,
16 because they would never have understood that the
17 dielectric layer is part of this metal layer, and a
18 POSITA at the time, when making changes, and it is --
19 freely they can choose whether you have a metal on your
20 outside layer there to form a insulated gate, as Yu
21 shows, or, removing this dielectric layer to make
22 Schottky gate as in other reference I showed. It's
23 simple choice that they can make.

24 And again, discussing that in -- here in
25 paragraph 112, one point I very clearly lay out those

1 discussions, and their focusing is on the metal layers
2 and the capping layer, which are the claimed features in
3 562. Okay. The 562 patent does not have claim feature
4 of oxide layer or insulating layer. And we focus on the
5 discussion on the patent features, claim features, which
6 are the metal layers and the capping.

7 Q. So, in Usui figure 8, are you putting layers
8 214 and 216 from Yu between the titanium layer 13 and
9 the metal stud 10?

10 A. Again, when we looking at this claim in 12 and
11 17, it's, you know, you have Usui and Yu, both POSITA at
12 the time, it's their choice to make their combinations.
13 And POSITA of the time for level CA transistor and CA
14 gate structure, and for them, but they say oh, we want
15 to improve electromigration, let me use Usui's structure
16 2 here, and there could be other cases. This their
17 choice. The POSITA of time have their choice to make.
18 And I discuss extensively here.

19 Q. So you haven't picked a specific spot where
20 those layers are going in to Usui; is that right?

21 A. I disagree. I --

22 Q. What is --

23 A. So, I provide very extensive discussions.
24 There are three paragraphs, very detailed, of how we
25 combine Usui's, you know, and Yu to render claim 12 and

1 17 are obvious. A lot of details here, as well as I
2 provide very lengthy answers to your question. I
3 provide all these. It's all very clear.

4 Q. Okay. Since it is so clear, take a look at
5 figure 8 of Usui, and tell me exactly where clearly
6 layers 214 and 216 go?

7 A. Again, Counselor, I have answered this
8 question multiple times. For a POSITA of time, if they
9 are facing a problem, it's their choice to combine the
10 reference. If POSITA of time see a transistor with
11 insulated gate, such as the Yu case, it's their choice.
12 They have, and the reference provide, Usui is there,
13 they will just take the claimed features, the patent
14 claim features, which are the metal layers, and to put
15 on the gate structure. And whether this gate is
16 insulating gate, or whether this is gate is, is Schottky
17 gate, it doesn't matter. Because the benefits are
18 all -- apply to both.

19 And let's go bolder than that, the Usui
20 teaching can be applied in everywhere. Can be applied in
21 interconnect, can be applied to gate, whether Schottky
22 gate or insulate gate, can be applied to source and
23 drain. And I answer this question many, many times now.

24 And again, in the page 46 and 47, I
25 provided very detailed discussion from paragraph 112,

1 113, 114, how we are making this argument, how -- very
2 detailed, all the details here. And again, I answer this
3 question a lot of times now.

4 Q. Okay. So, it's not between titanium layer 13
5 and metal stud 10, correct?

6 A. I have answered multiple times. POSITA of
7 time, if they are dealing with a transistor, they are --
8 it's perfectly their choice to making a -- making their,
9 you know, the changes for POSITA at the time. And here
10 I just provide, you know, examples. And one example,
11 this combination will render claims 12, 17 obvious.

12 Q. Right. The example is what I'm trying to
13 figure out your description of. There's no detail here
14 regarding where those two layers go, correct?

15 A. I'm very confused, Counselor. I have two
16 pages in front of me, paragraph 112, 113 and 114, as
17 long as -- also all the answers, very lengthy answers I
18 provide to you and you just tell me all those
19 paragraphs, as well as my lengthy answers to you, no
20 detail. I, I, I respectfully disagree. I provide a lot
21 of details to you already. You cannot answer -- ask me
22 the same question if you can -- if you do not get answer
23 you want. I provide a lot of detail answers to you
24 already.

25 Q. Right, so it's not that I'm not getting the

1 answer that I want. It's that I'm not really getting an
2 answer here.

3 In paragraph 112, do you tell us where you
4 would place layers 214 and 216 into Usui?

5 A. Again, it's a, it's a choice of the POSITA,
6 how they making those changes. And in here a POSITA
7 would be using the metal layers from Usui, the teaching
8 from Usui, and to the Yu's gate dielectric -- the gate
9 structure which has a dielectric, that to achieve
10 result.

11 But again, it's not limiting to here,
12 because these teachings, Usui can be widely applied to,
13 you know, insulated gate, to Schottky gate, to be source
14 and drain. And whether the, you know, how you make
15 insulate gate, how to make a Schottky gate, how you make
16 a interconnect, how make a source or drain is irrelevant
17 here. Because these are not -- because those metal can
18 both be applied here. And this is a choice of POSITA.
19 They can do -- they can do the combination they want to
20 solve their problems.

21 Q. Okay.

22 MS. RODRIGUEZ: Is now a good time for a
23 break?

24 MR. SARWAR: Now is a good time for a
25 break.

1 (Recess.)

2 Q. (BY MR. SARWAR) Couple of, just sort of last
3 questions about this last line that we had just almost
4 finished, regarding, you know, where a POSA might choose
5 to place the layers 214 and 216 from Yu into Usui.

6 So, is it fair to say that a POSA might
7 have chosen to place it between the titanium layer 13 and
8 metal stud 10?

9 A. So which figure are you referring to? Figure
10 8?

11 Q. Yeah, figure 8 of Usui.

12 A. So, what is your question again?

13 Q. So I'm keying my question off of implementing
14 the electrical contact of Usui with Yu's gate insulator
15 layer, which is how you describe the combination in
16 paragraph 114. And I'm trying to figure out, okay,
17 where do we put Yu's gate insulator layer in the
18 electrical contact of Usui.

19 And so the thought here is based off of
20 Yu's teachings, which says, you know, -- I'm reading off
21 of paragraph 112 of your declaration, you know,
22 dielectric layer 214 and 216, they underlie this
23 diffusion barrier, right, and it's a metal diffusion
24 barrier. So maybe one of the places you could put 214
25 and 216, when you're trying to implement Usui in view of

1 those layers, is underneath figure 8, Usui's titanium
2 layer 13, but above stud 10.

3 That's a really long wind-up, but the
4 question was: Is it fair to say that a POSITA might have
5 chosen to place layers 214 and 216 from Yu into that
6 location in Usui figure 8, which is between titanium
7 layer 13, and metal stud 10?

8 A. So, let me just rephrase your question in a
9 way -- we've been discuss this for a while now, and you
10 want to know how a POSITA of time to make the
11 combination Usui and Yu. And I already answered, but
12 let me -- from very beginning to go over this.

13 As laid out in my declaration, is if we
14 look at Usui and Yu, we see that the electro stacks are
15 generally interchangeable because they are form at the
16 same type of -- at the metal layers with same type of
17 materials. And in Yu, it has a bottom metal layer that
18 is diffusion barrier layer. One purpose of this bottom
19 diffusion barrier layer is to improve electromigration.
20 Usui provides guidance to achieve this goal, improving
21 electro migration, by limiting the thickness of the
22 bottom layer thickness.

23 So, as you see, a POSITA at the time, by
24 looking at this problem, very obvious. They're very
25 motivated for him to use Usui's metal layers, electrode

1 stack, to apply to Yu's gate structure, which is showing
2 here. And because this is obvious, and this is
3 predictable and successful for them at the time. And I
4 have provided detailed discussion here. And again, I
5 went over this, you know, how I made the combination here
6 to you, and it is very clear now.

7 Q. So, are you saying that your -- maybe I was
8 misunderstanding what the combination was before. Are
9 you saying that this combination here that you're
10 describing in paragraphs 112 through 114, involves
11 replacing the gate electrode that's shown in Yu with the
12 metal layers that are in Usui?

13 A. Again, I have provide very detailed
14 discussion. We will be focusing on the metal layers,
15 and the capping layer. And again, I provide this, all
16 the rationale about, you know, they're interchangeable.
17 Yu use electrode stack of the metal layers. And there's
18 a desire for Yu to improve the electromigration.

19 And a POSITA would take the metal layers
20 from Usui to apply to replace the metal layers in Yu to
21 achieve, you know, for the gate structure to achieve that
22 goal. But again, whether this gate structure has metal
23 and dielectric, or this gate structure has metal without
24 dielectric, it doesn't matter because both insulated gate
25 and Schottky gate are widely known concept. Why do they

1 use the concept for the transistors. And POSITA can, can
2 choose what the structure they want to work on, but this
3 teaching of Usui of those metal layers, and this limiting
4 the bottom metal layer, this bottom diffusion layer is
5 universal. Could be applied to gate, Schottky gate,
6 insulating gate. Could be applied to source, drain,
7 could be applied to interconnect.

8 Q. I see. Okay. So the combination then is, is
9 replacing the metal layers in the Yu reference with the
10 metal layers in the Usui reference. And so, the way
11 this combination would look is, it would look like, I
12 guess, figure 2E of Yu. It would have interfacial
13 dielectric layer 214, high-k dielectric layer 216. And
14 then on top of that, instead of Yu's metal layers, it
15 would have Usui's metal layers. Is that a fair summary?
16 Am I understanding the combination correctly?

17 A. Again, I have provided very detailed answer to
18 you. And in my paragraph, if we, you know, 114, to a
19 POSITA it would have been obvious to implement electric
20 contact Usui with Yu's gate insulated layer because Usui
21 disclosed the importance of improving electromigration
22 characteristic, as such layers are commonly provided
23 under gate -- to address gate leakage, so on, so forth.

24 So again, I have provide multiple times,
25 you know, the -- how I made the combination. And at the

1 end of the day, POSITA at the time have their choice,
2 when placing their province, you know, when making, you
3 know, Usui and Yu, that combination, they can do what
4 they want, but it's all obvious.

5 Q. All right. So in this combination, the
6 motivation is to address gate leakage, correct?

7 A. So again, I have go through a lot of lengthy
8 details here that Yu has this bottom layer of the metal
9 layers that cause diffusion barrier layer, and one
10 purpose of this diffusion barrier layer is to improve
11 electromigration.

12 And Usui provides guidance to achieve this
13 goal, improve electronmigration. And leakage -- gate
14 leakage is one of the outcome from the electronmigration.
15 And by combining Usui and Yu, a POSITA, it's very obvious
16 for him to solve this gate leakage problem. If they
17 choose -- if the problem they are facing is gate leakage
18 problem.

19 Q. Okay. Why don't we -- why don't I -- going to
20 turn to ground 3 now. Might revisit this afterwards, if
21 it isn't -- if it's still not clear to me, but might be
22 a good idea to just move on.

23 I'm putting into the chat Exhibit 1006.
24 I'm providing this because we're moving onto ground 3.
25 You might not end up needing it. But based on my line of

1 questions, you recognize Exhibit 1006, right?

2 A. I just have 1666 (sic) to me, it's the Adesida
3 patent.

4 Q. That's right. 1006 is the Adesida patent,
5 that's exactly right. So, please go to exhibit, -our
6 declaration, Exhibit 1002, paragraph 128, and 129. And
7 when you're done reading --

8 A. Yes, I'm reading the 128 and 129 of my
9 declaration. Okay.

10 Q. All right. I'm going to try asking some
11 pretty straightforward yes, no questions. So hopefully,
12 we can move quickly through them.

13 If I'm understanding correctly, your
14 argument here is that you modify the electrical contact
15 that you get from combining Usui and Yu in view of
16 Adesida; is that right?

17 A. In this ground 3, I'm, I'm basically described
18 that Usui gives Yu, and further in view of Adesida
19 renders claim 9, 11, 14 and 16 obvious.

20 Q. Okay, so that electrical content that you get
21 from combining those three references would meet all of
22 claims 9, 11, 14 and 16, correct?

23 A. The combination I provided, which is Yu --
24 Usui, Yu and Adesida will render claim 9, 11, 14 and 16
25 obvious.

1 Q. Okay. And this electrical contact would be
2 implemented as a gate electrode as required by claim 16,
3 right?

4 A. Let me go to claim 16. So you are referring
5 to claim 16, right? So let me, let me go to claim 16.

6 So I have reviewed the claim 16 of the 562
7 patent, and as I discussed it earlier and multiple times,
8 they are two commonly ways to make gate structure. One
9 is the insulate gate as shown in Yu, with a dielectric
10 layer, and the other -- dielectric layers. And the other
11 is a Schottky gate, which resolve the dielectric layers.

12 By looking -- by combining Usui and Yu, it
13 would be very obvious for a POSITA at the time to remove
14 the dielectric layer in Yu to make Schottky gate. And
15 because this is predictably successful and very obvious
16 for the POSITA at the time, because this insulated gate
17 structure is in Yu, and the Schottky gate structure in
18 Adesida. Both of them very well known by the effective
19 date. And in my declaration I discuss that the, the
20 preferable feature of subject gate, such as fast response
21 and so forth. So, all this combination, Usui, Yu, and
22 Adesida will render claim 16 obvious.

23 Q. So for this combination, are you -- you're
24 starting with Usui, or are you starting with Yu?

25 A. So let me go through the logic with you. So

1 Usui and Yu disclose transistor. And then if we look at
2 Adesida, Adesida is talking about HEMT device. By the
3 effective date, HEMT devices, particular III-V HEMT
4 devices, are very widely known as a type of transistor
5 that Usui and Yu discloses.

6 So a POSITA at the time would be very
7 motivated, and it's obvious for a POSITA at the time to
8 apply the III-V material of Adesida to achieve the
9 benefit of HEMT for high frequency, high power
10 applications. And Yu already disclose in Yu's patent the
11 application in III-V materials. So by combining these,
12 we clearly see that it will -- it renders claim 9, 11, 14
13 and 16 obvious. And also I discuss this in the ground 3.

14 Q. So what's the difference between your agent
15 for ground 3, which is Usui in view of Yu, and further
16 in view of Adesida -- sorry, Adesida, and your argument
17 for ground 6, which is Yu, in view of Usui, and Adesida?

18 A. So you are asking me ground 6 now, right.

19 Q. Yeah, I'm asking about what --

20 MS. RODRIGUEZ: Objection --

21 Q. (BY MR. SARWAR) -- about the difference
22 between grounds between 3 and 6 are?

23 MR. SARWAR: I apologize, Sarah.

24 A. What's your question again? I need to review,
25 but please tell me what's your question again.

1 Q. (BY MR. SARWAR) Yeah, what's the difference
2 between ground 3 and ground 6?

3 MS. RODRIGUEZ: Objection, form.

4 A. Again, so when we have POSITA at the time they
5 have many choices. I provide Usui, Yu, Adesida, and
6 Usui, Yu, and Adesida, it's referred to POSITA of time
7 to make those combinations. They can make any
8 combinations they want to solve the -- solve the problem
9 they have. And in my declaration, you know, I show some
10 of the examples that -- how to combine those reference.
11 But again, for a POSITA of time, they can choose what
12 they want to do. And there are many, many options here.

13 Q. (BY MR. SARWAR) Yeah. But my understanding is
14 that you chose two options, right? You chose an option
15 for ground 3 and an option for ground 6, correct?

16 A. Correct. These are in my declaration. I have
17 ground 1, 2, 3, 4, 5, 6, 7.

18 Q. Right. And so, for ground 3, the way you
19 describe ground 3, sounded like you were starting with
20 the Yu reference, modifying it in view of Usui. And
21 then modifying that in view of Adesida. I'm getting it
22 wrong; is that right?

23 A. Again --

24 Q. Sorry, you were shaking your head, that's why
25 I --

1 A. I clearly provided each description of
2 ground -- ground 3 and ground 6, very detailed
3 discussion there. So I will refer to my declaration of
4 ground 3 and ground 6. If you have, you know, you have
5 general question about ground 3 and ground 6.

6 Q. Okay, sure. So let's start with ground 3, all
7 right.

8 A. All right, ground 3, so let me get to ground 3
9 first. Okay, ground 3, paragraph 128 now.

10 Q. Yeah, so ground 3, my understanding, based off
11 of the rest of your declaration is that you're starting
12 with Usui figure 8, and you're arguing that the
13 electrical contact, disclosed by Usui, is on a group
14 III-V semiconductor device because of Yu's teachings.
15 And the place where it looks like you describe that is
16 Exhibit 1002 at paragraphs 110 through 111. That's
17 where you describe combining --

18 A. Wait, wait, wait. Counselor, you're confusing
19 me. You are referring to another paragraph? So we are
20 under 128, which is ground 3, but you are referring to
21 110 or something? So it's --

22 Q. No, I apologize. I did not design your
23 declaration. No, I -- look, I'm doing the best I can to
24 sort of untangle it, and like -- bear with me, right.

25 A. Yeah, so --

1 Q. Like, the --

2 A. Which are you covering right now, and which
3 paragraph are you referring to? And if you're referring
4 to ground 3, I previously already answer your question,
5 how I make the combination very clearly. So what is
6 your question? Is that on ground 3, or previous --

7 Q. Yeah. The question remains on ground 3.

8 A. Okay.

9 Q. And what was strange about your answer
10 regarding ground 3 is the description of why you were
11 combining Usui and Yu in the first place.

12 I believe your description for why you
13 were combining Usui and Yu in the first place was set
14 forth earlier in paragraphs 110 through 111, right? So
15 this is before we're getting to Adesida. This is --
16 we're sort of, you know, like before Adesida enters the
17 picture, we're doing something with Usui and Yu. So I
18 thought you had described that in paragraphs 110 through
19 111. If that's not true, you should let me know.

20 A. I'm waiting for your question, because what
21 you say is very confusing to me. You want me to focus
22 on ground 3, which starts paragraph 128, and then you
23 want to -- you refer to page -- paragraph 110, which is
24 the previous ground. So I'm very confused here.
25 Counselor, like, what is your question? And you want to

1 discuss ground 3 or ground 2? And again, ground 2, I
2 have give very extensive answers already. Ground 3, I
3 also answered extensively on how we get to ground 3. So
4 what is your question here?

5 Q. All right. So what is your starting point for
6 ground 3?

7 A. I have -- let me go through this whole thing
8 together with you. I already provided this answer to
9 you previously, but let me go there, so --

10 Q. Well --

11 A. Usui and Yu provides Usui and Yu combination
12 disclose transistor.

13 Q. Can I --

14 A. And (indiscernible) -- revises -- is a, is a
15 widely known type of transistor due to its benefiting
16 high frequency and high power applications. So, a
17 POSITA at the time will be very motivated to, to use
18 III-V material of Adesida to achieve the benefit of
19 HEMT, because that's all very well known. And that
20 Yu -- this reference of Yu further disclose to using
21 III-V materials.

22 Q. Okay. So, let's take it a little slower so
23 that you don't do the full combination without actually
24 getting to the details of what the combination is.

25 So, for the first part of this

1 combination, Usui, in view of Yu, right? What is --

2 A. What is your question here?

3 Q. Okay.

4 A. I'm waiting for the question.

5 Q. Okay. So -- here's --

6 A. You're asking me how I get to ground 3, I
7 provided twice now how I get to ground 3 in very
8 details.

9 Q. Okay, so --

10 A. And then you -- now you say don't want me to
11 provide details.

12 Q. Previously you testified today that Usui
13 was -- did not describe any specific transistors, right?

14 A. I have to go back to the record. Do you want
15 me to go back to the record?

16 Q. I mean, if you decide to change your answer --

17 A. If you have a specific question that I can
18 answer, we can move forward.

19 Q. Sure. So I asked you if the figure 8 of Usui
20 gave you enough information to conclude that it was a
21 transistor; do you recall what your answer to that
22 question was?

23 A. Okay, so I recall now. So you want to go back
24 to Usui again. Okay. So I want to go back to Usui
25 again, and I want to note here I answered this question

1 clearly in previous, in previous answers.

2 And then my answer here is, again, whether
3 Usui has a transistor or not, it's not discussed in
4 figure 8. And again, the application of Usui's teaching
5 is not limited anywhere in Usui. It could be broadly
6 applied and I have emphasized again and again those claim
7 features, those metal layers and the capping layer and
8 the limited thickness of the bottom layer can be applied
9 to interconnect, can be applied to the gate, such as
10 insulating gate in Yu, can be applied in a Schottky gate
11 such as in Adesida's case, can be applied in contact such
12 as ohmic contact for source and drain. It's broadly
13 applied. So, I have answered this question previously.
14 I'm now provide another -- repeat of my answer again.

15 Q. That's great. So, then just now, when you
16 were trying to describe what you did for ground 3, you
17 said that Usui discloses the transistor, right? You
18 said Usui and Yu both disclose transistor?

19 A. I said, I -- Counselor, you are again
20 distorting what I said. I never say something like you
21 just phrased.

22 Q. So --

23 A. I provide very clear answer. We can go to the
24 record here. I provide --

25 Q. Yes --

1 A. -- very clear answers to you.

2 Q. -- let's do that.

3 A. I respectfully request you do not distort what
4 I say. We have a record, called the record here, very
5 clear record.

6 Q. Absolutely. One hundred percent. Let's pause
7 for a second and look up at the record and see if you
8 have ever said, that Usui and Yu disclosed transistors?

9 A. Counselor, I want to again point out what you
10 are saying, the last part is different from what you are
11 saying previous part.

12 Q. You can look back at the record at that as
13 well and see if I am now changing my words. I --

14 A. You are changing your words.

15 Q. -- will tell you that I am not.

16 A. Again, if we move on, you can ask me question,
17 we can move on.

18 Q. So the previous question I asked you, just
19 before this was: You said Usui and Yu both disclosed
20 transistors. You're telling me now that, oh, no, that's
21 not something I said before. I was proposing that we go
22 back and look up at the transcript and see if that
23 was --

24 A. The record -- see the record written and we
25 will have those copies in record. We don't need to

1 argue that. And if you have another question, I'm ready
2 to answer.

3 Q. Yeah, I'll just pause for a second now, and
4 just look to see if, you know, I'm misremembering your
5 testimony. And then we can move on from there.

6 MR. MACDONALD: So, Counsel, are you
7 proposing that the witness reviews the transcript right
8 now? We can show it to him.

9 MR. SARWAR: No, that's not my proposal.
10 I'm just looking --

11 THE WITNESS: I propose a break for five
12 minutes, and I want to use the restroom.

13 MR. SARWAR: That will be great. Thank
14 you so much.

15 (Recess.)

16 Q. (BY MR. SARWAR) We were trying to clear up
17 confusion earlier about what your argument for ground 3
18 was. There was testimony previously that I'll just read
19 to you, and this is a rough transcript, of course, to
20 sort of give you a general idea, to give you a sense of
21 why I got confused.

22 Regarding ground 3, I asked: So for this
23 combination, are you starting with Usui, or are you
24 starting with Yu?

25 And you said: So let me go through the

1 logic with Yu, the Yu reference. So Usui and Yu disclose
2 the transistor, and if we look add Adesida, Adesida is
3 talking about a HEMT device, by the effective date HEMT
4 devices were very widely known as a type of transistor
5 that Usui and Yu discloses.

6 So for that reason, I got a little turned
7 around about what your argument for ground 3 is. Should
8 we try that one again? Like, are you starting with Usui
9 or Yu?

10 A. So I can start again. First of all, Usui and
11 Yu combination disclose a transistor, and the Adesida
12 HEMT devices by the effective date. It's a very widely
13 known type of a transistor, and with the benefiting high
14 power, high frequency application, a POSITA of the time
15 will be very motivated to use the III-V materials in
16 Adesida to achieve the benefit of a HEMT. And it is
17 predictable to be successful and obvious because Yu
18 already disclose application in count III-V materials.

19 Further, a POSITA at the time won't be
20 motivated to change the insulated gate structure in Yu by
21 removing the oxide dielectric layers to achieve the
22 Schottky contact as in Adesida, because it is very widely
23 known, well-accepted that there are two types of commonly
24 used gate structure, insulated gate with a insulating or
25 dielectric layer, or Schottky gate without the insulating

1 or dielectric layers. And a POSITA of time are freely to
2 choose. It's a matter of choice to go with which gate
3 structure they use.

4 And in my declaration I go over the
5 benefits of Schottky gate, including fast response and
6 non-linear behavior. And therefore, in ground 3, using
7 Usui, Yu and Adesida combination, making claim 9, 11, 14
8 and 16 obvious, and being -- I provide, again, another
9 detail answer to your question. And the paragraph 1
10 through 8 goes on, and provide, again, more details
11 again, here.

12 Q. Okay. That was very helpful. I understand
13 where the misunderstanding comes from, right, because
14 you were talking about Usui and Yu after they had been
15 combined, as disclosing a transistor, which now makes a
16 lot more sense to me.

17 So, that initial combination of Usui and
18 Yu, is it fair to say you described that in your
19 declaration in paragraphs 110 and 111?

20 A. So again, in my declaration ground 3, I
21 provide very detailed discussion how to make a
22 combination with Usui, Yu and Adesida that renders claim
23 9, 11, 14 and 16 obvious. It's all in the declaration.

24 Q. Will you indulge me and let me know where you
25 describe in -- let me step back.

1 In paragraph 128 you say, Usui -- Usui and
2 Yu do not expressly disclose its electrical contact being
3 configured for implementation on HEMT, or its electrical
4 contact being implemented as a gate electrode making
5 Schottky contact.

6 Unless I'm mistaken, in paragraph 128,
7 we're already starting to refer to a combination of Usui
8 and Yu that you have described previously; is that
9 correct? Am I reading paragraph 128 correctly?

10 A. Again, Counselor, I'm very confused here. In
11 ground 3, I have so many paragraphs, go all the way --
12 all the way to discuss why this is. And in paragraph
13 128, it's just one sentence. And it's in the overview
14 of the combination and the motivation to combine. So,
15 is there a question here? Because this is just one
16 sentence here. But if you want to go to the detail, how
17 I make those combination, I have answered your question
18 twice. And that's all in the detail of these
19 paragraphs.

20 Q. Okay, so are you telling me that in ground 3 I
21 don't need to go back and look at ground 2 for any
22 information regarding the combination of Usui and Yu?

23 A. Counselor, this is not what I just tell you.
24 I gave you very detailed discussions on, you know, how
25 I, how I come to ground 3. And, you know, multiple

1 times now. And also, these are all in my declaration.
 2 And why, you know, the combination of Usui, Yu and
 3 Adesida renders claim 9, 11, 14 and 16 obvious. It's
 4 all here.

5 Q. Let's move onto ground 6. So ground 6 is
 6 different from ground 3, correct?

7 A. Are you referring to -- what page? So I can
 8 go there and review first.

9 Q. Paragraph 188, it's on page --

10 A. 188.

11 Q. -- 81.

12 A. Okay, so we are at the 188 now.

13 Q. You'll agree with me that this is using the
 14 same three references that you use for ground 3?

15 A. Again, in my declaration I provide very
 16 detailed descriptions from ground 3 and ground 6, how
 17 is, you know, Usui, Yu and Adesida. And here is Yu in
 18 view of Usui and the Adesida. And again, in my
 19 declaration, I provide some examples here.

20 But the POSITA at the time, they can --
 21 when they see those reference, it's their choice to make
 22 those combinations, and they will -- regardless, there
 23 are many combinations the POSITA at the time can choose.
 24 But they will reach the same conclusion as I put out here
 25 that, you know, these claims are obvious.

1 Q. So for this ground, unlike in ground 3, you
2 started with the Yu reference, correct?

3 A. So again, I will refer to my declaration. And
4 in declaration ground 3, as Usui, Yu and Adesida, and
5 here we have Yu in view -- in ground 6 is Yu in view of
6 Usui and Adesida. So, these are all clearly state in
7 the declaration, and yeah.

8 Q. So when we were talking about ground 2
9 earlier, we discussed starting with the Yu reference,
10 which has two dielectric layers and a series of metal
11 layers stacked on top of it, and switching out the metal
12 layers in Yu with the metal layers that were found in
13 Usui; this is what we discussed for ground 2, and I
14 think you characterized that as --

15 A. So, do you have a question here? So if, you
16 know, we have been go through very lengthy ground 2, and
17 I explain multiple times how we can -- you know, why
18 it's perfectly obvious to use Usui structure on Yu to
19 solve the electromigration, and then, you know, Usui
20 structure can be on Yu's gate, and so forth. So we can
21 go through that very extensively.

22 So, I want to see, do you want to go back
23 to ground 2, and, you know, start again? But I think we
24 answer that very extensively.

25 Q. You know what, I believe everything you just

1 said about ground 2 is consistent with what my memory of
2 the testimony was. Which is that, it was obvious to use
3 Usui's structure on Yu to solve electromigration
4 problems. And you explained to me how ground 6 differs
5 specifically for that Yu and Usui component, how it
6 differs from what you described for ground two --

7 A. So your question -- let me repeat. Your
8 question is how my ground 6 is different from ground 2?

9 Q. Specifically as it pertains to Yu in view of
10 Usui.

11 A. So again, so let me first go through why
12 ground 6 -- ground 2. Because, you know, if you see
13 ground 2 -- again, we have a table here, in the ground
14 2, first of all, combination in Usui and Yu, and talk
15 about challenging claims in 3, 8, 12, 13 and 17. And
16 ground 6 is Usui and Adesida covers challenging claims
17 9, 11, 14 and 16.

18 So just by looking here, it's very clear,
19 and it's all in my declaration. These are two grounds.
20 And -- but again, a POSITA of time, you know, can -- when
21 they see those reference, it's their choice. They can
22 make the combination they want to solve the problem they
23 have. And over all my grounds, 1, 2, 3, 4, 5, 6, 7, I
24 provide very extensive detail to show that all the
25 challenge claims are obvious. It's all in the details in

1 my declaration.

2 Q. Okay. So you gave me a comparison just now
3 with grounds 6 and 2, and you pointed out that they
4 cover different claims. Can you go through the same
5 exercise for grounds 3 and 6?

6 A. So is there a question here?

7 Q. Yes. I'm trying to figure out what the
8 substantive difference is between ground 3, which is
9 Usui in view of Yu and Adesida, and ground 6, which is
10 Yu in view of Usui and Adesida. What is the substantive
11 difference between ground 3 and ground 6? And --

12 A. Yeah, I, I don't understand your question,
13 because, you know, ground 3 and ground 6 are discussed
14 in detail in my declaration. And there are many, many
15 pages here. And you -- what is your question? You want
16 me to really go through all those pages and tell you if
17 the words are different or --

18 Again, I said, you know, this is a choice
19 of POSITA. When they have the reference in hand, it's
20 their choice to make combinations to solve the problem
21 they have. And here, I'm just providing examples here,
22 and with all this ground. But overall, all these grounds
23 I provided in my declaration very strongly, clearly show
24 all the challenge of claims are obvious.

25 Q. Are you able to provide a summary of grounds 3

1 and 6 that would illustrate for me verbally the
2 differences between those two grounds, or do I have to
3 go back and look back at the declaration to try sifting
4 through these paragraphs?

5 A. So I, I, I will repeat to you that the title
6 of ground 3 and ground -- you are talking about ground 3
7 and ground 6, right?

8 Q. Yes.

9 A. Yeah. So ground 3, Usui in view of Yu and
10 further in view of Adesida renders obvious claims 9, 11,
11 14, and 16. And ground 6, Yu in view of Usui and
12 Adesida renders obvious claims 9, 11, 14 and 16.

13 And I have answered your question
14 repeatedly, for the details are all in my declaration.
15 There are many, many paragraphs to discuss ground 3 and
16 ground 6 and how we get there.

17 The second thing I emphasize, again, I'm
18 providing examples here, but POSITA at the time, it's
19 their choice, they can make the combination they want.
20 But at the end of the day, when we look all these grounds
21 that I provided, which are very extensive, you can come
22 to the conclusion very strongly that all the challenging
23 claims are obvious.

24 Q. Okay. Is it fair to say that ground 3 starts
25 with Usui?

1 A. So again, Counselor, I would strongly -- if
2 you have not read my declaration, I would strongly go
3 advise you to go to the declaration, and from ground 3,
4 I provide multiple answers to you, how, you know, we get
5 to that. So, you know, it's, it's Usui and the Yu
6 combination disclose a transistor, and the Adesida HEMT,
7 I provide this to you already multiple times.

8 And then I also say, all the details are
9 in ground 3 from 128, 129, all the way multiple pages.
10 So I provide all those details, how we make the
11 combination and how they render claims 9, 11, 14 and 16
12 obvious, I answer this question multiple times.

13 So is there another question regarding
14 ground 3 you are not clear?

15 Q. Yeah, sure. Why don't we do it this way:
16 We'll start going into ground 6. And through our
17 questioning and answering, I'm sure you'll be able to
18 clarify how it is different from ground 3, and you won't
19 be saying the same arguments that you said for ground 3.
20 So let's turn to ground 6. Paragraph 188. And going
21 onto paragraph 189.

22 Here you're starting with the Yu
23 reference, instead of Usui, correct?

24 A. Well, let me, let me go through. So you want
25 me to read through 188 and 189, so let me take some time

1 to read.

2 Okay. So again, I can go over the logic
3 with you, but, you know, it's again, it's the choice of
4 POSITA. And in this case POSITA say, oh, I see a gate
5 structure in Yu, and I want to improve electromigration,
6 I'm going it take Usui's teaching here, and again, I see
7 the Adesida which is talking about apply application in
8 the III-V device in the HEMTs, so I will combine with
9 these, and then I will solve the problems. And then, you
10 know, these are all, you know, discussed detail in ground
11 6 that Yu in view of Usui and Adesida renders claim 9,
12 11, 14 and 16 obvious.

13 So, you know, the POSITA -- I emphasize a
14 lot now the POSITA of the time, it's their choice.
15 Because yes, these are all very well known. And it's
16 their choice to, to choose how they want to solve the
17 problems.

18 Q. Okay. So in your opinion, what you just said
19 in terms of your summary for ground 6 is different from
20 what you said from ground 3, correct?

21 A. So, again, being it's a POSITA choice, that
22 they make a combination that they want, to, to solve the
23 problems that they have.

24 Q. And you understand that you are -- you
25 articulated two of those choices for grounds 3 and 6,

1 correct?

2 A. Again, I have also this question many times.
3 It's -- comes to time. They can do what they want, they
4 can choose the reference. They can, they can, you know,
5 solve the problems. And I'm just showing some examples
6 here. But again, there's many, many possibilities.
7 POSITA of time, they can do whatever they want to solve
8 the problems they have.

9 Q. Did you articulate concrete possibilities, or,
10 in your declaration did you really emphasize that
11 POSITAs had a lot of choices here?

12 A. POSITA -- again, I answered this question
13 multiple times now.

14 POSITA -- it's up to POSITA. POSITA have
15 their choice. And I see, you know, there could be many,
16 many choice, many, many possibilities that they -- how
17 they use reference and to solve the problems, they have.

18 Q. Okay. And that's what you described in your
19 declaration, right?

20 A. My declaration can provide some of the
21 examples, some of the possibilities, but again, there
22 are many, many possibilities that POSITA can go.

23 Q. Okay. So in paragraph 199 of your declaration
24 --

25 A. 199, I have paragraph 199 now.

1 Q. All right. That's on page 86 of your
2 declaration, right?

3 A. On page 86 of declaration, paragraph 199, I
4 have it now.

5 Q. All right. If you peek back at the previous
6 page, you'll see that you're discussing claim 11 here.

7 A. Which page are you referring to?

8 Q. Page 85.

9 A. Page 85, okay.

10 Q. You're discussing claim 11 here.

11 A. I see page 5 (sic) and claim 11, the electro
12 contact, claim 8, electro contact is implemented as gate
13 electro making Schottky contact with III-V semiconductor
14 device.

15 Q. Right. So in paragraph 199, you point out
16 that Adesida discloses gate 190, which you say is the
17 claimed gate electrode, right?

18 A. So, in paragraph 199, I -- in my declaration
19 paragraph 199 I quote, consistent with the 562 patent,
20 Adesida disclose gate 190, gate electrode, formed as a
21 Schottky barrier contact, Schottky contact on the group
22 III-V device.

23 Q. Okay. And that gate, from Adesida is the one
24 that you're relying on for your mapping for claim 11,
25 correct?

1 A. Can you repeat the question again?

2 Q. That gate from Adesida is the one that you're
3 relying on for your mapping for claim 11 in this ground,
4 correct?

5 A. As I discuss very extensively, there are two
6 widely used gate structure. One is insulated gate with
7 a dielectric layer. One is the Schottky gate, as shown
8 Adesida or here, and it's, it's for the POSITA at the
9 time, both of the gate structure very well known and
10 widely used. And POSITA will be very -- really obvious
11 for them, and they'll be motivated to, you know, change
12 the dielectric -- remove the dielectric in Yu, and to
13 make, to make a Schottky contact as seen in Adesida so
14 there, there -- it's very obvious. And they will be
15 motivated to do so, because there are benefits of a
16 Schottky gate, as I emphasized in my declaration,
17 including passive response and non-linear behavior.

18 Q. All right. And you mentioned here that this
19 gate 190 is formed as a Schottky barrier contact, or
20 Schottky contact on the group III-V device, correct?

21 A. Again, I -- in this paragraph, I talk about,
22 you know, gate 190 in Adesida is the Schottky contact.
23 And at the end of the day, I emphasize many times now
24 the claim feature from 562, the claim feature which are
25 the metal layer, the capping layer. They can be broadly

1 applied. They can be applied to interconnect. They can
2 be applied to Schottky, contact. Can be applied to the
3 gate insulating.

4 And also, I already provide very extensive
5 discussion that the -- why it is obvious. It is obvious
6 for POSITA at the time to, to make the motivation to go
7 from a insulated gate in Yu to the Schottky gate in
8 Adesida, because all they need to do is just remove the
9 dielectric layers. It's a very simple, obvious and very
10 well known at the effective time, and the POSITA will be
11 very motivated to do so.

12 Q. So does Adesida's gate 190 have layers?

13 A. So, in the figure 5, that the gate structure,
14 the Adesida does not disclose whether it has layer, or
15 not. It could be have layers.

16 Q. What would the layers be?

17 A. Again, there are many choice that a POSITA can
18 choose for the layers in the gate structure in the
19 Adesida. And again, like we discussed, in Yu's
20 teaching, it teaches those metal layers, and the, and
21 the capping layer with the benefits of improving the --
22 improving the electromigration. And it is perfectly
23 fine for POSITA of time to, you know, make the
24 combination of those metal layers in Usui and Yu, and
25 eventually to use in the Schottky gate. These are

1 perfectly fine and predictably successful. These are
2 all very well known -- and were well known structures at
3 the time.

4 Q. Okay. What is the structure of the gate
5 electrode that you're relying on for your specific
6 argument?

7 A. What's the question?

8 Q. What is the structure of the gate electrode
9 that you're relying on for your specific argument?

10 A. Which argument are you referring to?

11 Q. I'm referring to ground 6.

12 A. So you are asking me what is the gate
13 structure in ground 6?

14 Q. That's right.

15 A. Again, I have provide many times now that, you
16 know, there are two commonly used gate. One is
17 insulated gate. One is the Schottky gate. And they are
18 very commonly known at the effective date. And POSITA
19 of time, they can freely choose what gate they can use.
20 And they can just simply remove the dielectric layer,
21 which is shown in Yu, Yu's patent.

22 And to make Schottky gate, which is in
23 the -- Adesida's, Adesida's figure here, it's just
24 simple -- it's so -- it will be -- would have been so
25 obvious for POSITA of time to make those modifications,

1 and to make those changes.

2 Q. So if I wanted to understand what layers are
3 in the gate electrode that you've proposed here for
4 ground 6, I can't just rely on Adesida, can I?

5 A. We are -- again, in ground 6 here, let's go
6 back to ground 6. It is Yu in view of Usui and Adesida.
7 We make those combinations and to render the claim 9,
8 11, 14 and 16 obvious. And at the end of the day,
9 POSITA can have many choices. They can see all these
10 references and they can make their choice by their own.

11 And, you know, again, I have repeated
12 answered your question and also in ground 6, very
13 detailed discussion why in Yu in view of Usui and Adesida
14 this combinations make claim 9, 11, 14 and 16 obvious.

15 Q. Where do you discuss the layers of gate
16 electrode 190 in ground 6?

17 A. What's your question again?

18 Q. Where do you discuss the layers of gate
19 electrode 190 in ground 6?

20 A. Again, Counselor, I have answered this
21 question repeatedly. In ground 6 we rely on Yu, Usui
22 and Adesida, this combination. And those metal layers
23 that we already see in Usui. We already see in Yu. And
24 we understand they are benefits, including improving
25 electromigration and so forth.

1 And, Adesida, it's very obvious for a
2 POSITA of time to use those metal layers as a gate in the
3 Adesida case. As I discussed, first of all, those metal
4 layers, those patent features, those claim features of
5 metal layers, they can broadly apply to interconnect, to
6 insulate gate, to Schottky gate, and to, and to
7 contact -- you know, to source and drain, so forth.

8 And also, second, the POSITA of time, they
9 can make choices. They can do the combination they want
10 because either insulated gate, or the Schottky gate are
11 very well known. And those metal layers, they want to
12 choose -- it's a choice for them they can make. This
13 is -- everything here, you know, claim 9, 11, 14, 16,
14 very well known, you know, at the time. So that's why,
15 you know, in Yu, in Usui and Adesida will render these
16 claim very obvious.

17 Q. Can you identify the paragraphs in which you
18 discuss the layers of gate electrode 190 in ground 6?

19 A. Your question again, please?

20 Q. Can you identify the paragraphs in which you
21 discuss the layers of electrode 190 -- gate electrode
22 190 in ground 6?

23 A. The metal layers -- again, Counselor, I have
24 repeatedly answered your question.

25 In here, we rely on combination Yu, Usui,

1 and Adesida. And we apply the metal layers Yu, Usui to
2 the benefit of Adesida here, and I answer this question
3 multiple times now.

4 And again, for our discussion, for the
5 whole declaration it's about metal layers. And this
6 metal layers can be applied to gate structure, can be
7 applied to Schottky gate, can be applied to insulated
8 gate, can be applied to source and drain and so forth.

9 Q. So if I go back and look at the transcript,
10 I'll find citations to specific paragraphs in which you
11 discuss the layers of gate electrode 190, and ground 6?

12 A. Can you give me a more specific question here?

13 Q. I've asked you if you could identify the
14 paragraphs in which you discuss the layers of gate
15 electrode 190 and ground 6, and I received the answer
16 that you've repeatedly answered this. So I'm asking you
17 if I were to go back and look at the transcript of our
18 deposition today, would I find those paragraph numbers
19 that you already testified to?

20 A. So, Counselor, again, I have go over all the
21 logic with you. I don't have to provide this, because
22 we are making combination here, because we are not rely
23 on Adesida for ground 6. We rely on Yu, Usui and
24 Adesida.

25 And then the metal layer has been the

1 essential part of the discussion today. And it's
2 everywhere. It's everywhere in, you know, in this metal
3 layers, because they're benefit -- they can be applied to
4 gate, Schottky gate, or insulate gate and so forth. I
5 very extensively go over how we come to ground 6 by
6 combination Yu, Usui and Adesida. And it's also in
7 detailed discussion in paragraph 188 and all the way to
8 paragraph 199, it's all there.

9 Again, I have answered your question
10 repeatedly.

11 Q. Okay. How many layers are in that gate
12 electrode in ground 6?

13 A. Again, I have answered this very repeatedly,
14 that we are rely on three patent; Yu, Usui and Adesida.
15 And a POSITA of the time will be very motivated to use
16 those metal layers in Yu and Usui's teaching to the
17 Adesida's gate structure to achieve the benefits that
18 lay out and whether or not such layer are showing in
19 figure 1, figure 5 in Adesida is irrelevant here. It's
20 not important, because ground 6, I have answered this
21 multiple times now, and also in detailed discussion in
22 ground 6, in multiple paragraph have discussed this
23 combination of Yu, Usui, and Adesida render claims 9,
24 11, 14, 16 obvious.

25 Q. So is the number of layers in the gate

1 electrode in ground 6 irrelevant to your analysis?

2 A. Can you repeat your question again?

3 Q. Is the number of layers that are in the gate
4 electrode in ground 6 irrelevant to your analysis?

5 A. So you mean the number of the layers in, in
6 which --

7 Q. In the gate electrode that you identify for
8 ground 6.

9 A. Figure -- which? Counselor, can you speak up
10 louder? I'm sorry, it's difficult for me to hear.

11 Q. I'm sorry, is my audio going out? How's it
12 now? Is it okay now.

13 A. It's better, but can you speak louder?

14 Q. Yeah, sorry about that. I had no idea what
15 was happening. Maybe I'll switch out my headphones or
16 something at some point if it keeps getting worse.

17 Okay. Is the number of layers that are in
18 the gate electrode in ground 6 irrelevant to your
19 analysis?

20 A. Again, we are talking about the metal layers
21 that Yu and Usui teaches, and again, goes through their
22 many benefits to use those metal layers in the gate
23 structure that Adesida shows. And, you know, I have go
24 through this many, many times.

25 So there is perfectly motivation obvious

1 for the, for the POSITA to use those metal layers in the
2 Adesida's gate structure. And as well as to those
3 layered construction of those metal layers, you know,
4 Usui and Yu discuss very extensively for -- in Usui, it
5 discuss, you know, the bottom layer, the bottommost
6 layer, this metal layer cannot be very thick, right? The
7 cap layer should be thicker. So those are all discussed
8 extensively in Usui and so forth. So these are all
9 relevant information as I already, you know, went over.

10 Q. Right. So if I wanted to identify and
11 evaluate the merits of your argument, and examine the
12 metal layers that you have incorporated into your
13 combination for ground 6, where would I look?

14 A. Okay, so, if you try to understand ground 6,
15 again, it's very clear to see we have Yu in view of
16 Usui, and the Adesida. So both Yu and Usui provide a
17 lot of discussion on those metal layers. And how those
18 metal layers, especially the, you know, can, can benefit
19 and so forth. And, you know, there's, again, in my
20 declaration, I also provide a lot of discussion here.

21 So, it's perfectly fine to, you know, for
22 a POSITA of the time to see, oh, I see this metal layers,
23 and I'm going to just use, you know, Yu have this gate
24 structure, right, and Usui has metal layers, it's going
25 to improve electromigration. And again I have a

1 transistor, a HEMT transistor, let me use those metal
2 layers, that combination, to use in III-V HEMT devices.
3 I went through multiple times, again, in the ground 6,
4 it's a very detailed discussion here.

5 Q. Okay. And for this ground, ground 6, do you
6 know how many layers, metal layers were incorporated
7 from the Usui reference?

8 A. Again, when I have emphasized many times now
9 that the metal layers, which are the patent features
10 here -- claim features here, we been focusing on,
11 discussing those metal layers. And Usui, and Yu,
12 provide the very detailed discussions of those metal
13 layers in the -- for example, in paragraph 36 of Yu,
14 provide a wide range of materials, including the metal
15 nitride they can choose from to further provide the
16 thickness and so forth. All the information are there.

17 So here, for ground 6, we are making a
18 combination of Yu, Usui and Adesida. And Yu and Usui,
19 they have very detail information about the metal layers,
20 about their thickness, you know, in paragraph 36 and so
21 forth. So all the information are there. We are making,
22 you know, again, for POSITA, when they see those, they
23 can make their choice, they can do what they want. But
24 in my, in my declaration, you know, ground 6, I lay out,
25 you know, how we can get here, and how, how combination

1 of Yu, Usui and Adesida make claims 9, 11, 14 and 16
2 obvious.

3 Q. For ground 6 do you know which of the metal
4 layers from Usui are incorporated in your combination?

5 A. Again, just -- Counselor, I'm answering the
6 same question, again, again. I have give you very clear
7 information on the, on, you know, how we come to here,
8 and the metal layers, and information here. I have
9 give -- answered this question multiple times now.

10 Q. Okay. I'll ask a slightly different question.
11 Before ground 6, do you know which of the metal layers
12 from Yu are incorporated into your combination?

13 A. Again, in ground 6, we are combining Yu, Usui,
14 and the Adesida. And Yu and Usui provides metal layers.
15 And in Yu it provides, you know, many other choices,
16 including, you know, the titanium nitride, tantalum
17 nitride, and many other metals, and so forth. It will
18 be a choice for the POSITA of time to, to make those
19 combinations.

20 But we have been once over again, again,
21 those metal layers, because the benefit of improving
22 electromigration could be broadly applied to gate
23 structure, insulating gate, Schottky, source and drain,
24 and so forth. And then, you know, it's all -- I answer
25 this question many, many times now. And you know, Yu and

1 Usui provides detailed information on the metal layers.
2 And Yu provides thickness. So you can just refer to
3 those document and the combination Yu, Usui and Adesida
4 will render claims 9, 11, 14 and 16 obvious.

5 Q. Okay. And in your declaration, you know, when
6 I go back and read it again, I will find clear
7 identifications of which layers you took from Usui and
8 which layers you took from Yu for ground 6, correct?

9 A. Again, I have answered this question same --
10 this is the same question repeat and repeat. And I
11 answered it already many, many times. That when we make
12 those combination -- again, I don't need to give, you
13 know, those metal layers and others, because the whole
14 declaration is about those metal layers. It's about
15 these, and they can be -- how they can be broadly
16 applied. And the fact that Yu and Usui, you know,
17 provides details in their patents about those metal
18 layers, I don't have to copy every word from Yu or Usui
19 to my declaration.

20 Q. Okay. And this is also true for the other
21 grounds in your declaration, correct? Namely that, when
22 you made the combinations, you didn't need to provide
23 for us the metal layers that were included in the
24 respective combinations, correct?

25 A. Throughout my declaration I provide a lot of

1 details about metal layers, what their components, their
2 thickness and so forth. And, again, a lot of details in
3 my declaration. And, for example, page 64 I talk about,
4 you know, those layer. I talk about thickness. And
5 there's many places I talk about titanium, titanium
6 nitride, tantalum, tantalum nitride, you know, whole
7 declaration is about those metal layers and provide
8 thickness, so as in reference Usui and Yu, there's a lot
9 of information in my declaration, and the -- about those
10 metal layers, they are the type of metals can be choosen
11 (sic), as well as thickness. And again, this
12 information all in the declaration.

13 Q. Okay. But the specific details I'm asking
14 about, namely the number of layers that you've taken
15 from Yu and Usui, and which layers you've taken from Yu
16 and Usui. You did not set that out in your declaration,
17 or any of your grounds, because it wasn't necessary for
18 your analysis, correct?

19 MS. RODRIGUEZ: Objection, form.

20 A. No, Counselor, this is not what I just said.
21 I provide the opposite. I provide -- I just said I
22 provide a lot of information about those metal layers.
23 They are the type of material can be choose from,
24 including titanium nitride and tantalum nitride and
25 titanium, about their thickness. A lot of information

1 about those metal layers in the declaration. I
2 provided. As well as those information are in
3 references.

4 Q. (BY MR. SARWAR) Okay. So you're telling me
5 that you did identify in your declaration the number of
6 metal layers you take from Yu and Usui for each of the
7 combinations and which of the mental healths you take
8 from Yu and Usui from each of your combinations,
9 correct?

10 A. Again, I refer to my previous question. I
11 provide a lot of information about those metal layers,
12 their thickness, the type of materials. And then at the
13 end of the day, it's the choice of POSITA at the time to
14 make those changes as they see fit, when they see a
15 problem. In my declaration I provide a lot of
16 information about those metal layers. I provide all
17 this -- again, POSITA at the time they have their choice
18 to making changes and to get to their desired results.

19 Q. Okay. I'm going to show you Exhibit 1007.
20 Hold on, I'm going to try to show you Exhibit 1007. I
21 feel like somehow --

22 A. Okay, I have 1007 now.

23 Q. Okay. I'm showing you Exhibit 1007 in case
24 you need it. You recognize Exhibit 1007 as Sugimoto,
25 right?

1 MS. RODRIGUEZ: Is it time for a break
2 or?

3 THE WITNESS: Yeah, let's do a break.

4 MR. SARWAR: Sure, yeah, now's fine.

5 (Recess.)

6 Q. (BY MR. SARWAR) Dr. Zhao, have you been
7 talking with counsel at all about your testimony during
8 the breaks?

9 A. No.

10 Q. Just checking. Every now and then, you know,
11 have to check.

12 Okay. Did I already give you -- I already
13 showed you Exhibit 1007, correct? It's the Sugimoto
14 reference, I think I may have just --

15 A. Sugimoto, I have it now.

16 Q. All right, excellent. I'm just giving it to
17 you in case it is helpful for our next sort of set of
18 questions.

19 So Exhibit 1007 is Sugimoto, right?

20 A. I see Sugimoto patent as 1007 exhibit.

21 Q. And, you know, for ground 7, from your
22 declaration, I understand that you're again starting
23 with the Yu reference as your starting point. So let's
24 turn to figure 2E of the Yu reference. This is Exhibit
25 1005.

1 A. So you want to go to 100 -- 1005, you want to
2 go to Yu?

3 Q. Correct.

4 A. And you are referring to -- which one are you
5 referring to?

6 Q. I'm referring to ground 7, which is --

7 A. It's combination, right? Let me go to -- so
8 ground 7, combination, Yu, Usui, and Sugimoto, okay.

9 Q. Exactly. Okay. All right. So we've turned
10 to figure 2E and if I'm understanding your argument in
11 ground 7 correctly, you're saying that would have been
12 obvious to use the electrode stacks shown here in figure
13 2E as power electrodes, right?

14 A. So, Counselor, you are asking me about ground
15 7, which is the combination with Yu in view of Usui and
16 Sugimoto to render the claim 10 and 15 obvious. And I
17 will go through this how we get there.

18 So, again, at the very beginning, we have
19 discussed that Yu and Usui had those electrostatic metal
20 layers that are interchangeable, and we have agreed that
21 a POSITA at the time will, will make those combinations
22 of, you know, of those metal layers, which are the claim
23 features in the 562 patent.

24 And here we see clearly that with those
25 metal layers, because they are benefit in improving

1 electromigration and so forth, those metal layers, again,
2 not dielectric layer. We're only referring to those
3 metal layers. They could be -- it's perfectly fine for
4 the POSITA at the time to use those metal layers to
5 achieve ohmic contact and to use those metal layers to
6 achieve power electrode, as discussed in Sugimoto.

7 So, it also goes back to what I discussed
8 early earlier, the teaching here in Usui and Yu can be
9 broadly applied to gate structure, but as well as source
10 and drain structure. And to -- and for the ohmic
11 contact -- and for power electrode, which are disclosed
12 here, because it is overall a benefit to improve the
13 electromigration and to all those cases a POSITA of time
14 would make -- it's their choice to make those choices, to
15 make those modifications. Therefore in ground 7, Yu in
16 view of Usui and Sugimoto will render claims 10 and 15
17 obvious.

18 Q. All right. And in Yu, figure 2E, you can see
19 two gate electrodes, correct?

20 A. Again, we been discussed previously in Yu,
21 when we talk about the electrode, which are relevant to
22 the 562 patent here, we are referring to the metal
23 layers, the dielectric layer, they are not metal, they
24 are irrelevant to our discussion here.

25 And particularly we're talking about

1 ground 7 here, and what we see is a POSITA who takes a
2 look at the figure 2E that we are discussing, and sees
3 those metal layer, not dielectric layer. Those metal
4 layers, it's perfectly obvious for him to combine, okay,
5 Usui teaches way to improve electromigration, so let me
6 combine. So those metal layers can improve
7 electronmigration, it's very good metal layer, and for
8 the -- Sugimoto use those metals for power electrode and
9 use for ohmic contact, which are claims 15 and 10.

10 So with this combination, Yu, Usui and
11 Sugimoto, a POSITA of time, it's obvious for them that
12 the claim 10, 15 in the 562 patent are obvious.

13 Q. Do you have a sense of which of the two gate
14 electrodes disclosed in Yu figure 2E would be
15 appropriate for interchanging as a power electrode?

16 A. Again, Counselor, for ground 7, we are making
17 combination Yu, Usui and Sugimoto. And I have
18 emphasized again, again we are talking about those metal
19 layers. Those metal layers are in figure 2E of Yu.
20 Those metal layers are in Usui. And we use those metal
21 layers to improve the electromigration, for example;
22 there are many other benefits there.

23 And we use those metal layers -- again,
24 those metal layers are in figure 2E, we use those metal
25 layers and we do the combination, and it's the POSITA of

1 time -- it's their choice. They pick this Yu and they
2 pick this from Usui. It's their choice that they can be
3 applied to Sugimoto, because Sugimoto already disclosed,
4 you can make ohmic contact, you can make power electron.
5 So with these combinations, Yu, Usui and Sugimoto, again,
6 POSITA of time, he can make those choices, he can -- and
7 it will be obvious for them.

8 Q. Okay. Your analysis for ground 7 is -- spans
9 from paragraphs 200 to 209 in your declaration, correct?

10 A. Yes, for ground 7 in my declaration is
11 paragraph 202, and 209.

12 Q. Okay. And if I were to look for the details
13 regarding which of the metal layers were taken from Yu
14 and which of the metal layers were taken from Usui to
15 form the combination described in ground 7, it's in
16 those paragraphs, right?

17 A. Again, Counselor, I think I answer this
18 question in the same fashion previously already.

19 In my declaration, throughout declaration
20 I provide a lot of information about those metal layers,
21 their thickness, the metal that can be choose from, so as
22 in Yu and Usui.

23 And in this ground 7 here, in those
24 paragraphs, I'm basically lay out why we are making the
25 combinations so that claim 10 and 15 are obvious. I do

1 not need to copy every word, provide every information
2 that already in my declaration or the reference to this
3 section, because all this information are already
4 provided. A lot of information is there. I don't need
5 to copy every word, you know, in this sections.

6 Q. I understand. What we should do is, I would
7 like to give you the opportunity to look through your
8 declaration and identify for me the paragraphs in which
9 you identify which metal layers from Yu and Usui you
10 select and use for each of the combinations so that you
11 can provide that for me on the record, if possible. So
12 can we go ahead and do that now?

13 A. So, Counselor, again, you know, all the metal
14 layers, in terms of metal layers, their thickness and so
15 forth are in Yu and Usui. In my declaration it's not
16 the purpose of declaration to copy every word and copy
17 every information about Yu and Usui and put every word
18 in my declaration.

19 I have cited these references in my
20 declaration all over the place. I cited them. That's,
21 that's enough and that's all the information is there,
22 it's in my declaration as well as in the reference. So
23 again, I emphasize here, I don't need to put all the
24 words of those metal layers, and thickness in every
25 section of my declaration.

1 Q. Yeah, I don't mean to suggest that you needed
2 to copy and paste material from the references and put
3 it in your declaration. Instead, I'm -- I'd like you to
4 provide me a catalog of the paragraphs that are relevant
5 to the specific questions of which, which metal layers
6 from Yu you are selecting for your combinations, and
7 which metal layers from Usui you are selecting for your
8 combinations, and, you know, I understand that the
9 language from the references will not be there, and it
10 will instead be citations. But the specific paragraphs
11 where that analysis is, I would like an indication of
12 where that is in your declaration?

13 A. So this is a very vague request here,
14 because -- I want to put on note, as stated that
15 information about the -- those metal layers and their
16 thickness and so forth, a lot of information about those
17 metal layers are presented in the -- very detailed in
18 the references, and I cited those reference in --
19 throughout the discussion of declaration. And there
20 many place when we go through ground 1 to ground 7,
21 there many place where I cite those reference and talk
22 about those metal layers. And now you are asking me to
23 find each of the place that those metal layers are
24 cited. Is that your request here?

25 Q. No. The specific request I have is where in

1 your declaration you identify which specific layers you
2 are using from the Usui reference, and which specific
3 layers you're using for the -- from the Yu reference,
4 and show me where in the declaration you did that. It's
5 a very focused request.

6 And if it makes it easier for you to be
7 able to comply with this request, we can do it on a
8 ground by ground basis, if that helps. Because I'm sure
9 with each of the combinations, there might be some
10 variance regarding which layers from Yu you chose to rely
11 on, and which layers from Usui you chose to rely on?

12 A. Again, you just rephrased my previous request.
13 If you want me to point out every place that I mention
14 metal layers, and that every place I cited Yu and Usui
15 throughout my declaration, which is almost 100 pages,
16 and you say we can go from ground to ground, which we
17 have nine grounds, and then we have almost, you know,
18 tens of pages and you want me to go through those pages
19 and point to you all this information about those metal
20 layers and those thickness and all that information,
21 even though this information are found in the references
22 and it was scattered all in my reference -- in my
23 declaration.

24 I do not understand here that you want me
25 to start ground 1, which is, I don't know which page, all

1 the way to 100 page, you want me to go through one by
2 one. Again, I will comply. So, again, you want me to
3 find everywhere in my declaration about those metal
4 layers, their component, and their thickness, and from,
5 you know, ground 1 to ground 7, and point out to you.

6 Is that the request? Because what you
7 just repeat, it sounds the same thing, because you said
8 Usui and Yu, all those metal layers, where are they in
9 all the declaration and point out to you, to you -- is
10 that your request?

11 Q. It is not my request. I'll, I'll articulate
12 the request again. And I'm going to use a specific
13 example for you so that you understand what the request
14 is.

15 So in ground 2, please identify for me
16 where in your declaration you identify which specific
17 metal layers from Usui have been included in your
18 combination and where you identify --

19 A. And I -- go over ground 2, right, go to ground
20 2 first.

21 Q. Dr. Zhao --

22 A. I have ground 2.

23 Q. Dr. Zhao, if -- so the request will become
24 very clearly narrow if you allow me to finish it. If
25 you don't mind.

1 A. I'm waiting for your instruction here, I'm
2 waiting for a question here. Do you want me to go to
3 ground 2? I'm at ground 2 now.

4 Q. Okay. Yes. So in ground 2, please identify
5 for me where in your declaration you identify which
6 specific metal layers in Usui you've included in your
7 combination?

8 A. Again, this goes back to what I said
9 repeatedly. When I refer to Yu and Usui, all those
10 metal layer in Yu and Usui, the information are in the
11 reference. And I do not need to copy every word from Yu
12 and Usui of those extensive list of material -- the
13 metals and refractory metals and the refractory nitride
14 metals and their thickness. I don't need to copy every
15 word in the declaration.

16 And here I already provide you the
17 description there that, you know, how we make those
18 combination, how, you know, Usui and Yu, their metal
19 layers are formed -- they are, they are electrode stack
20 of Usui and Yu. They are interchangeable. They are
21 formed at the same -- they are formed as a metal layer of
22 same type of materials and these materials are listed in
23 Yu and Usui.

24 I don't need to copy -- there's no need
25 for me to copy those, you know, those layers, those

1 materials to you because they are described in Yu and
2 Usui.

3 And my ground 2 here is to talk about
4 how -- the way I combine for POSITA at the time, they can
5 do many choice, but then in ground 2 I provide example
6 that Usui combine Yu and makes claims 3, 8, 12, 13, 17
7 obvious. I don't need to copy all the list of the metals
8 and their components, and the thickness from the
9 reference, because when I say Yu and Usui, you know,
10 everybody understands what I refer to.

11 Q. So do you understand my request as demanding
12 that you copy disclosures from the references into your
13 declaration?

14 A. My understanding I have been talking about
15 multiple times now. I provide very detailed discussion
16 in ground 2, and throughout my declaration I refer to
17 the reference. I provide a lot of information of metal
18 layers and fumes and so forth. And those information
19 can be found in Yu and Usui in this reference. As long
20 as we can find them, that's fine.

21 My declaration, again, all those grounds
22 are particularly talking about we combine those
23 referenced and then making those claims, you know,
24 obvious. It's not the purpose of declaration to copy
25 every word from the reference, which I already did, we

1 can find them, which are cited in my declaration. You
 2 know, copy every word, including every word, every -- you
 3 know, those material list to each section of the ground.
 4 It's not useful here. And as long as we have those
 5 materials in the reference, it's enough.

6 Q. With respect, Dr. Zhao, no matter how many
 7 times you characterize what I'm asking you as copying
 8 something, I'm not asking you to do that.

9 A. Okay, so I --

10 Q. I can, I can try to -- I can try to give you
 11 --

12 A. How about we go to the reference Yu and I give
 13 you the list of the materials and their thickness.
 14 Let's go to your paragraph 36, in paragraph 36, you give
 15 a list of the materials that a capping layer, for
 16 example, is that a capping layer can be --

17 Q. Sorry, Dr. Zhao --

18 A. (Indiscernible).

19 COURT REPORTER: One at a time, please.
 20 One at a time. I can only take one at a time.

21 Q. (BY MR. SARWAR) I'm going to ask you to stop
 22 because I'm not asking you to read from the reference.
 23 I'm asking something different.

24 MS. RODRIGUEZ: Please stop interrupting
 25 the witness.

1 A. Yeah, Counselor, I understand we have a job to
2 do; we work together. I answer your question multiple
3 times.

4 The information of those metal layer,
5 their thickness and so forth, can find reference -- can
6 find in the declaration; we can find them there. And I
7 don't think this is a reasonable request for me, without
8 each of the -- those metal layer in my declaration, which
9 are 100 pages to find each of them. I want to show that
10 I already provide enough information on the adequate
11 information about those metal layers in my declaration,
12 and then I provide the reference. Reference has all list
13 of those metal layers, and the thickness and so forth.
14 And this is already enough information for us to get to
15 where we are discussing today.

16 And again, if you want to detail the metal
17 layers, here on page -- column four of Yu, for example,
18 it give very extensive information of those metal layers.
19 And at the end of day for POSITA at the time, it's their
20 choice. They can see all these metal choices in Yu and
21 Usui, and so forth. It's their choice to make those
22 information. POSITA of time have this choice here. They
23 see all those information of metal layers and the fumes.
24 My declaration is to provide some the examples and
25 some -- we have made very clear. And again, if you want

1 me to provide a list of the material layers and their
2 component and so forth, we can find them in the, you
3 know, declaration and the reference.

4 Q. (BY MR. SARWAR) I will narrow the request down
5 so that we can at least try to find it for one of the
6 grounds. For ground 2, please tell me where you
7 identified which specific layers from Usui are in the
8 combination of Usui in view of Yu?

9 A. Again, Counselor, I have answered the question
10 multiple times.

11 When I say Usui, we will refer to the
12 metal layer in Usui, and when we say Yu, we will see the
13 metal layers in Yu. And then the metal layers, you know
14 those electrode stack in Usui and Yu, they are
15 interchangeable. And, you know, they are formed -- you
16 know, they are, they are formed of the same type of
17 materials. And in Yu and Usui provide a lot of
18 information on those metal layers. I cited Yu, Usui
19 already here. There's no need for me to list all the
20 metal layers in Usui and Yu into my declaration because
21 they are all in the reference and I cited reference in
22 the description for ground 2 here.

23 Q. Okay. For ground 2, turn to Usui figure 8.

24 A. Which page are you referring to?

25 Q. In Exhibit 1004.

1 A. Okay.

2 Q. There are a series of figures in the Usui
3 patent.

4 A. Okay, so I have Usui 1004 in front of me.

5 Q. Excellent. And then, if you could turn to
6 figure 8.

7 A. I have figure 8 of Usui in front of me.

8 Q. And you recognize figure 8 of Usui, correct?

9 A. I see figure 8 of Usui in front of me.

10 Q. Okay. And do you recognize the figure?

11 A. Is this a question? Because I told you I just
12 see -- I already see figure 8 of Usui in front of me.

13 Q. It is, in fact, a separate question. The
14 question that I originally asked was whether you
15 recognized it, instead of whether you saw it.

16 So my question is: Do you recognize
17 figure 8?

18 A. Okay. So I, I see either 8 of Usui in front
19 of me, and I recognize this figure.

20 Q. Excellent. Okay. So in your combination for
21 ground 2, which combines Usui and Yu, which of the metal
22 layers in figure 8 are in your combination?

23 A. Again, I have been answer this question
24 multiple times. So let me just go over ground 2 with
25 you, again. I already been answer this many, many times

1 now.

2 When we have Usui and Yu, we see that the
3 electrode stack of Usui and Yu, they are interchangeable,
4 because they are form -- they are form of, of the metal
5 layers of same type of materials as referenced in Usui
6 and Yu. And in Yu, it cause the bottom layer of its
7 metal layers as a diffusion barrier layer.

8 One purpose of the diffusion barrier layer
9 in Yu is to improve electromigration; also something we
10 discuss extensively. Usui provides a guidance to improve
11 electromigration by limiting the thickness of the bottom
12 layer in the metal layers. So it is very obvious, and
13 predictably successful for POSITA of the time, to use
14 Usui's metal layers to Yu's gate structure to achieve,
15 improve electromigration and other benefits. And I
16 being -- went through this logic and these are all laid
17 out in ground 2.

18 Q. Okay. So is layer 19 in the resulting
19 combination?

20 A. You are referring to layer 19, figure 8 of
21 Usui?

22 Q. Yes.

23 A. So what is your question about layer 19?

24 Q. Is layer 19 included in your combination of
25 Usui and Yu?

1 A. Layer 19 is a layer in Usui, and in Yu. As I
2 lay out in paragraph 36 of Yu, it discuss very
3 extensively about the capping layer of the metal layers
4 and it give examples that this layer could be metal,
5 which in Yu, it could be metal, and it goes onto give
6 examples, and POSITA at the time would go to paragraph
7 36 of Yu and to see the list of metals as well as
8 infractive (sic) metal nitride, such as titanium nitride
9 and tantalum nitride, TIN and TAN.

10 In paragraph 36 of Yu also provide
11 extensive details in the thickness of those capping
12 layer, including the, including the 600 angstrom that's
13 in my declaration, as well as 200 angstrom, and this will
14 render claim 1C obvious. So, although it is obvious by
15 Yu alone, I provide Usui here. That confirms the POSITA
16 of time that will use a capping layer that is thicker
17 than the bottom layer to achieve the -- to achieve the,
18 the result.

19 So I, again, went through all the, you
20 know, analysis here.

21 Q. The question I asked was a yes or no question.
22 Is layer 19 included in your combination of Usui and Yu?
23 Are you able to answer that question --

24 A. I, I --

25 Q. -- with a yes or a no?

1 A. I (indiscernible) a lot of details, and then
2 both Usui and Yu have, having this capping layer, and
3 the paragraph 36 of Yu discusses capping layer and in
4 Usui also we have capping layer.

5 Q. Is layer 18 of figure 8 of Usui in your
6 combination of Usui and Yu?

7 A. So again, we been focusing on the metal
8 layers, and particularly the claimed features about 562
9 patent, it's about metal layers and a capping layer.
10 And these are the claimed features. In, in the -- we
11 can have different metal layers. And then in Usui, we
12 see those layers, we see metal layers 13, 14, 15, as
13 well as the 18 you're referring to, and the capping
14 layer 19.

15 Q. Is layer 15 from Usui in your combination of
16 Usui and Yu?

17 A. Again, we are talking -- the 562 patent
18 everything is focusing on metal layers, and then by
19 looking at figure 8 we see different metal layers, and
20 there are metal layers 14 and 15.

21 Q. Is layer 14 from Usui in your combination of
22 Usui and Yu?

23 A. So again, we are seeing different layers in
24 Usui, and we have multiple layers in Usui, and
25 eventually, you know, these multiple layers. And to

1 achieve -- they work together to achieve
2 electronmigration, you know, Usui is to limiting the
3 bottom layer thickness, and so forth. We been through
4 all this, but then the claimed features and all we
5 discuss is focus on those metal layers.

6 Q. Is layer 13 from Usui in your combination of
7 Usui and Yu?

8 A. Again, we see the metal layer 13 as the bottom
9 layer of the claimed feature metal layers here.

10 Q. Okay. Where in your description of the
11 combination of Usui and Yu do you identify whether
12 layers 13 through 15 and 18 through 19 are in the
13 combination of Usui and Yu?

14 A. So again, in my declaration, are you referring
15 to ground 2?

16 Q. Still in ground 2, yes.

17 A. Okay. So, again, I have been -- went through
18 all the details of ground 2 that talk about multiple
19 layers, all the metal layers and so forth; I go through
20 these with you already. Again, I do not need to point
21 out each of those layers in my ground 2 analysis as long
22 as you know Usui provides this. And I refer Usui
23 already, so.

24 Q. Okay. Let's turn to Exhibit 1005.

25 A. I have Exhibit 1005 in front of me.

1 Q. Thank you. Sorry for interrupting. Go ahead
2 and turn to figure 2E.

3 A. I have figure 2E.

4 Q. Is layer 26 figure 2E of Yu?

5 A. Twenty-six?

6 Q. Yeah, sorry, layer 226.

7 A. You mean layer 26 in figure 2E? There's no
8 layer 26.

9 Q. Is layer 226 from --

10 A. Oh, you're referring to layer 226, okay. I
11 see layer 226 in figure 2E of Yu.

12 Q. Very good. Is layer 226 from figure 2E of Yu
13 in your combination of Usui and Yu?

14 A. Again, we -- in Yu we discuss extensively
15 about this capping layer 226 in Yu, paragraph 36,
16 provide a lot of detailed information about this capping
17 layer 226 and how it could be made as metal, and how it
18 could be made as the, the refractory metal nitrides,
19 including titanium nitride and tantalum nitride. So
20 these are all in the discussion Yu, as well as in my
21 declaration.

22 Q. Where in your declaration do you identify
23 layer 226 from figure 2E of Yu as being part of your
24 combination of Usui and Yu?

25 A. So, again, when I -- in ground 2 when we talk

1 about Usui and Yu, we are obviously referring to those
2 metal layers here. And like I said again and again, I
3 don't need to print out each of the layers and their
4 component, or the thickness in my declaration. I
5 provide the reference in my declaration, refer to Yu and
6 so forth. And again, I also, multiple times now, went
7 through the ground 2, how combine Usui and Yu, multiple
8 times now.

9 And are you saying that I did not mention
10 Yu, those metal layers in ground 2? Because that's not
11 true.

12 Q. Is layer 224 from figure 2E of Yu in your
13 combination of Usui and Yu?

14 A. Counselor, we are, again, just same question.
15 You are asking me each layer and there are multiple
16 layers here. And again, we been discuss that there --
17 there are multiple layers, and we been focusing on those
18 layers. And they are, they are the, you know, in Usui
19 and Yu, they are interchangeable, and Yu, the option of
20 those layers, thickness, wide range of thickness and
21 wide range of material to choose from.

22 It's POSITA of time -- it's their choice
23 to make, you know, what material they want to use, what
24 thickness they want to use, and so forth. And if we go
25 to the matter today, the claimed feature, about 562

1 patent, it's about those metal layers. Plurality of
2 those metal layers, including one of 562, this many
3 layers. It's not putting any limitation of, you know, of
4 those layers.

5 So, you know, I, I think I provided a lot
6 of useful information already, and, and at the end of the
7 day, it's POSITA of time to choose the metal of layers,
8 to choose the thickness, to choose the metal they want to
9 solve the problem they are facing. Yu and Usui clearly
10 provide very useful guidance here, which will render the
11 claims obvious.

12 Q. I understand your answer. We're almost done,
13 though, so we'll just get through this.

14 Is layer 220 from figure 2E of Yu in your
15 combination of Usui and Yu?

16 A. I refer to my previous response that I gave
17 extensive response and you are just asking me the same
18 question in nature.

19 Q. Is layer 218 from figure 2E of Yu in your
20 combination of Usui and Yu?

21 A. Again, I want to state here, that I consider
22 the metal layers, that metal layers in Yu -- it's in my
23 discussion -- the metal layers, they are conducting, and
24 for the layers such as 214 or 216 that are not metal,
25 they are oxide or they're dielectric, they are not part

1 of the electrode that, that we discuss today. Because
2 in 562 patent, focus on those metal layers, a POSITA at
3 the time by looking at those patterns, by looking at
4 Usui and Yu, they would never have understood that the
5 dielectric layers are part of the metal layer, because
6 they are not. So we been focusing on those metal layers
7 in all the discussion. And other discussion, for
8 example, for the oxide, they are irrelevant. And they
9 are not part of, you know, they won't change my analysis
10 today.

11 Q. Is layer 216 from figure 2E of Yu in your
12 combination of Usui and Yu?

13 A. Again, I answer this question in the previous
14 answer already, that we focus on the metal layers, okay,
15 so I answered that already. You can go onto 214, but
16 doesn't matter, I answered this multiple times now.

17 Q. Okay, I'll ask about 214 as well.

18 A. Okay, I answered already. I will refer to the
19 previous answers that I gave you.

20 Q. Sounds good. In order to have a clean record,
21 I just want to make sure it's on there.

22 A. I answer that already.

23 Q. So, is layer 214 from figure 2E of Yu in your
24 combination of Usui and Yu?

25 A. I answer this question already. I'll refer to

1 my previous answers.

2 Q. And should also ask about layer 222. Is layer
3 222 from figure 2E of Yu in your combination of Usui and
4 Yu?

5 A. Let me see, I will generally refer to my
6 previous answer. I think, you know, we don't need to go
7 each layer by layer. I think I provide very clear
8 answers to your question, and you can just refer to my
9 previous answers.

10 Q. Okay. Thank you so much.

11 And then, where in your declaration do you
12 identify layers 226, 224 -- sorry. Let me back up and
13 rephrase that question, I apologize.

14 Where in your declaration to you identify
15 whether or not layers 226, 224, 220, 218, 216, 214, and
16 222 as being part of your combination of Usui and Yu?

17 A. Again, I answer -- this is the same question.
18 I answer multiple times now. I will refer to my
19 previous answer.

20 Q. Can you tell me what an electrode stack is?

21 A. Again, at the very beginning, we went through
22 this. For claim -- patent 562, claim 1, it clearly
23 state that electrode stack includes, includes metal
24 layers and capping layer. And anything that is not a
25 metal layer, or a capping layer of that electrode stack

1 is unclaimed. So all -- all my analysis, all
2 discussion, solely focus on those metal layers and a
3 capping layer. And, you know, I been provided this
4 description already. And so, yeah, these are my answer
5 again.

6 Q. Thank you. Can you tell me your impression of
7 the meaning of the term electrode stack?

8 A. Again, I just answer your question about
9 electrode stack. With respect to our -- today's, you
10 know, matter, with respect to 562 patent, with respect
11 to my declaration, and I answer this many, many times
12 now.

13 Q. So where in your declaration did you discuss
14 the meaning of the term electrode stack?

15 A. It is -- again, it is the same question over
16 and over. In my declaration I focus on those metal
17 layers and the capping layer, and this is the
18 emphasized -- this is in 562 patent, claim 1. And when
19 I analyze Usui and, for example, I focus on those metal
20 layer because they have all the claimed features, okay.
21 So, you know, I, I -- my declaration center around those
22 metal layers, and capping layer, and you will find all
23 those information in declaration as well as in
24 references. And again, I won't -- if it's the same
25 question, I won't answer again.

1 Q. Can you tell me as a, a person of ordinary
2 skill in the art what an electrode is?

3 MS. RODRIGUEZ: Objection, form.

4 A. Again, when we analyzed this, we assume person
5 -- POSITA. This -- the thing I just describe,
6 everything by description, in my declaration and
7 everything we discuss today is for POSITA. And it won't
8 be -- it is the POSITA at the time, they would
9 understand what I just said. It is the same definition
10 that I provided.

11 Q. (BY MR. SARWAR) Can you indulge me and remind
12 me what definition of electrode you provided?

13 A. I answer the question --

14 MS. RODRIGUEZ: Objection, form.

15 A. -- many times. I will not answer this
16 question again. I provide multiple times answers to
17 this question.

18 Q. (BY MR. SARWAR) So you're under the impression
19 that I asked you about the meaning of the term electrode
20 during the deposition today, and that you've provided an
21 answer to it, correct?

22 A. I provided multiple times about electrode,
23 about -- and multiple times now, and I will refer to the
24 previous answers I provided.

25 Q. Okay. And can you identify for me where in

1 your declaration you previously discussed the meaning of
2 the term electrode?

3 A. I answer -- this is the same question couple,
4 you know, couple minutes ago. I answer that already.
5 I'll refer to the previous answer I gave you.

6 Q. Okay. Can you talk to me about the general
7 approach you used when you first started analyzing
8 whether or not the claims of the 562 patent were
9 anticipated or obvious?

10 A. Okay, so, if we go to the declaration, I
11 provide a lot of -- you know, description on this. And,
12 you know, these are all in the, in the declaration, so
13 page 12, 8, I talk about level of ordinary skill. B, I
14 talk about prior art. C, I talk about anticipation. D,
15 I talk about obviousness and along the way. And, you
16 know, page 10, all the way to page 18 -- as well as the
17 previous pages provide a lot of descriptions on your
18 answers --

19 Q. So -- so in your declaration you sort of
20 describe the process you went through in order to
21 analyze the claims of the 562 patent?

22 A. Again, I answer this question already.

23 Q. Okay. Did you conduct prior art searching for
24 your analysis?

25 A. Again, I believe I answer this question

1 already. And there is a prior art section in my
2 declarations and I refer to that section if you want
3 to -- more information.

4 Q. Are you referring to paragraph 36 of your
5 declaration?

6 A. Paragraph 35, okay, yeah, I have paragraph 35
7 here.

8 Q. And this paragraph summarizes your, I guess,
9 process for looking for prior art?

10 A. Paragraph 35 about prior art here, I quote, I
11 have been advised and understand that information used
12 to evaluate whether an invention was new and not obvious
13 when made is generally referred to as prior art. I
14 understand that prior art includes patents and printed
15 publications that existed before the earliest prior art
16 date, or the earliest applying date of the patent, which
17 I have been informed is also called effective bidding
18 day.

19 I have been informed and understand that a
20 patent or population of patent application is prior art
21 if it was filed before the effective bidding day of the
22 claim mentioned and the printed publication is prior art
23 if that -- it was publicly available before the effective
24 bidding day of the claim mentioned.

25 I believe this whole paragraph will, will

1 answer all your -- answer your previous question very
2 adequately.

3 Q. Does your analysis in your declaration provide
4 any specific opinion regarding the field of endeavor of
5 the 562 patent?

6 A. Is there a specific question you're asking me?

7 Q. Yes. I'm asking whether there's any location
8 or paragraph in your declaration where you provide an
9 opinion about what field the 562 patent is in.

10 A. Well, the 562 patent, if you want to find
11 out -- you go to 562 patent and the reference there.

12 And my declaration, again, provides all
13 these all these and by combination of those references
14 talk about why all the claims of 562 patent are obvious
15 for POSITA at the time.

16 Q. Are you familiar with the term interconnect?

17 A. I'm familiar with the term interconnect.

18 Q. Do you consider the term interconnect a term
19 of art?

20 A. Again, I gave very detailed discussion today
21 about interconnect, about gate, about OHMIC, Schottky,
22 source and drain, and I won't go through them again.

23 But Usui's teaching about those metal
24 layers and technical layer, they could be widely applied
25 to all those cases. It could be in interconnect, it

1 could be in -- it could be in Schottky gate, insulate
2 gate, could be in source, and drain and power electrode.
3 And I provide very detailed discussion in all the grounds
4 when I combine, you know, those references. And, you
5 know, these I have answered, you know, very extensively.

6 Q. Is a wire a type of interconnect?

7 A. Wire can be many, many things. I don't know
8 what wire are you referring to.

9 Q. Is the term interconnect the same thing as
10 interconnection?

11 A. I don't know what you mean.

12 Q. Are they synonyms? Are the terms interconnect
13 and interconnection synonyms?

14 A. I don't know what you mean. You're giving me
15 two words, one is interconnect and one is
16 interconnection, so they are two words. So what is your
17 question here?

18 Q. Do they mean the same thing?

19 A. The two words can mean very different things,
20 or mean the same thing. We have to put them in the
21 context and understand what they refer to. So again,
22 what's your question -- specific question here,
23 Counselor?

24 Q. Just trying to get a sense of whether or not
25 you view the term interconnect as being interchangeable

1 with the term interconnection?

2 A. Again, Counselor, I'm very well understand and
3 familiar with the term interconnect and interconnection,
4 and I understand those terms. But then, if you are
5 asking whether those two terms are interchangeable, we
6 need to see the content of paragraph, a sentence, or
7 something that we can, we can refer to.

8 Q. Are you familiar with the term metallization?

9 A. I'm familiar with the term metallization.

10 Q. Do you have any opinion about what that term
11 means?

12 A. Metallization of the metal structures, and
13 again, in our discussions today, focusing on the metal
14 in 562 patent, claim 1, it shows us electro stacks of
15 metal includes metal layer and capping layer. I focus
16 my analysis on those metal layers and we talk the
17 metallization structure, one type of metallization
18 structure, and those metal layers, having all the
19 claimed features.

20 Q. Do you have an opinion of the customary
21 meaning of the term interconnect?

22 MS. RODRIGUEZ: Objection, asked and
23 answered.

24 A. I answer this question multiple times now.

25 Q. (BY MR. SARWAR) What is an electrical

1 junction?

2 MS. RODRIGUEZ: Objection, asked and
3 answered.

4 A. I answered question already. You know, we
5 been talking about, you know, ohmic contact, Schottky
6 contact, gate, dielectric and so forth. These can all
7 be found in my declaration. And we went through all
8 these already. It's all in my declaration.

9 Q. (BY MR. SARWAR) So you think that if we look
10 at the transcript you will find a question from me
11 asking you what the meaning of electrical junction is,
12 and that you've provided an answer?

13 A. I provide answers to Schottky, Schottky
14 contact, ohmic contact, in my declaration has Schottky
15 contact, metal contact, has the information of the gate,
16 insulated gate and so forth, and then -- so, this
17 question has been answered.

18 Q. Are those examples of electrical junctions?

19 MS. RODRIGUEZ: Objection, asked and
20 answered.

21 A. Again, I answered the question already.

22 Q. (BY MR. SARWAR) Do you think when we look back
23 at the transcript you will see a question in which I
24 asked you whether the things that you just listed were
25 examples of electrical junctions?

1 MS. RODRIGUEZ: Objection, asked and
2 answered.

3 A. The question I already answered; I refer to
4 the previous answer.

5 Q. (BY MR. SARWAR) Turn to paragraph 8 of your
6 declaration, please?

7 A. Okay, I have paragraph 8.

8 Q. Do you see where you reference your standard
9 rate?

10 A. You mean, I'm being compensated for my time at
11 my normal hourly rate, this sentence?

12 Q. Yeah.

13 A. So what's your question here?

14 Q. What is your normal hourly rate?

15 A. It is irrelevant to my declaration and my
16 analysis, and I don't want to disclose to you. It's a
17 normal hourly rate.

18 Q. All right. Are you suggesting this is a
19 privileged communication or something like that?

20 A. No, I just simply think it does not concern
21 the declaration, does not concern my professional
22 opinion. It's a normal activity in those IT cases, and
23 I don't want to provide numbers to you. And again, this
24 sentence has all the information you need. I'm being
25 compensated for my time at my normal, normal hourly

1 rate, and you will find this in all the declarations for
2 all the experts.

3 MS. RODRIGUEZ: This is not privileged
4 information. You can answer that question.

5 A. What about if I don't want to? Is that -- you
6 can note it that the witness does not want to disclose
7 hourly rate to the counsel -- counselor.

8 Q. (BY MR. SARWAR) I'll move onto the next
9 question. You have a Bachelor of Science, correct?

10 A. I have a Bachelor of Science degree.

11 Q. When did you earn that?

12 A. I have my Bachelor degree in 2008.

13 Q. And then after that, you studied under
14 professor Shuji Nakamura for your Ph.D., right?

15 A. So I got my degree, my Bachelor degree in 2008
16 and by the time 2008 I already have one year of training
17 in the undergraduate research lab, doing engineering
18 work closely related to the field. I start my graduate
19 work in 2008, in University California, with Professor
20 Shuji Nakamura. And by the effective day of 2009, I am
21 effectively POSITA because I have four years of
22 undergraduate study and effectively two years of
23 engineering work.

24 But most importantly, I know many POSITA
25 at the time. I work with POSITA, such as engineer in the

1 lab from companies. I know how they think. I know how
2 they behave. I use their thinking at the time, at the
3 effective date, 2008, and throughout all my analysis
4 here.

5 Q. You mentioned in your answer that you, by the
6 time of 2008, had already had one year of training, in
7 an undergraduate research lab doing engineering work
8 closely related to the field. What is your
9 understanding of the field of the 562 patent?

10 A. Again, we are talking about electrical
11 engineering, and this is also in my definition of
12 POSITA, that it's a Bachelor degree in electrical
13 engineering or related field.

14 Q. So your undergraduate research lab was in
15 electrical engineering?

16 A. Correct.

17 Q. When, when did you start working on
18 semiconductor device design?

19 A. Again, like I just said, by the time 2008 when
20 I graduated, I already work a year of experience in an
21 engineer lab and on this work.

22 Q. So your work in the undergraduate lab involved
23 semiconductor device design?

24 A. I work at the research lab as a undergraduate
25 student, and I have one year of engineering experience

1 by the time 2008.

2 Q. And the engineering experience was related to
3 semiconductor device design?

4 A. Yes.

5 Q. When did you start working on gallium nitride
6 for semiconductor device design?

7 A. So I started gallium nitride as an
8 undergraduate student, as well as through my graduate
9 studies.

10 Q. Under Professor Nakamura?

11 A. I worked as a undergraduate student in the
12 undergraduate lab, already exposed to their nitride
13 work, and continue my graduate study at the -- with
14 Shuji Nakamura on gallium nitride.

15 MR. SARWAR: Okay. I think we should
16 take a break right now and I'd like to sort of look
17 through my notes and see if there's anything else I want
18 to tackle. But if I could have like 15 minutes to sort
19 of gather thoughts. If that works for you guys? I know
20 that your flight has been moved to --

21 THE WITNESS: Yeah.

22 MR. SARWAR: The ship has -- well, I
23 don't know what the -- the plane has flown. But if you
24 give me 15 minutes, I can try to wrap this up.

25 (Recess.)

1 MR. SARWAR: I have good news. No
2 further questions at this time.

3 MS. RODRIGUEZ: Can we just have five
4 minutes?

5 MR. SARWAR: Yeah.

6 MS. RODRIGUEZ: Thank you.

7 (Recess.)

8 EXAMINATION

9 BY MS. RODRIGUEZ:

10 Q. So, Dr. Zhao, I'm just going to ask you a few
11 questions.

12 A. Okay.

13 Q. Dr. Zhao, do you recall that Mr. Sarwar asked
14 you many questions about how you combined references for
15 grounds 2, 3, 4, 5, 6 and 7?

16 A. Yes.

17 Q. Let's look at your declaration for ground 2.
18 Specifically claim 8, which is a combination of Usui and
19 Yu. Can you go to paragraphs 110 and 111; do you see
20 that?

21 A. Paragraph 110 and 111, yes.

22 Q. This discusses claim 8, correct?

23 A. Correct.

24 Q. Here you write: A POSITA would have been
25 motivated to implement the electrical contacts as taught

1 by Usui in group III-V semiconductor devices, as taught
2 by Yu. Do you see that?

3 A. Yes.

4 Q. What is a resulting device of the combination
5 of Usui and Yu that you have described for claim 8?

6 A. The -- here we are using Usui's natural
7 contact to, to -- for the III-V semiconductor device as
8 taught by Yu.

9 Q. So are you saying that we're using Usui's
10 metal layers?

11 A. Yes.

12 MR. SARWAR: Objection, leading.

13 Q. (BY MS. RODRIGUEZ) Okay. So next I have a
14 question on claim 12. Can you please go to Exhibit 1001
15 and read claim 12?

16 A. Which, which --

17 Q. This is the 562 patent.

18 A. 562 patent. I have 562 patent now.

19 Q. Please read claim 12.

20 A. Claim 12?

21 Q. Claim 12.

22 A. Okay. I will read claim 12. The electrical
23 contact, claim A, within said electrical contact is
24 implemented with a gate to a layer and line set for
25 metal layer of electro stack to provide insulate gate --

1 electro stack in III-V semiconductor electric device.

2 Q. Does claim 12 depend from claim 8?

3 A. Yes.

4 Q. Please return to your declaration. I have
5 some questions on the combination of ground 2 for claim
6 12.

7 A. Okay.

8 Q. Will you please go to paragraphs 112 through
9 114.

10 A. Okay.

11 Q. Do you see those?

12 A. Yes.

13 Q. Do these paragraphs discuss the combination of
14 ground 2 for claim 12?

15 A. Yes.

16 MR. SARWAR: Objection, form.

17 Q. (BY MS. RODRIGUEZ) Is the resulting device of
18 the Usui, Yu combination that you have described for
19 claim 12 the same as it is for claim 8, or is it
20 different?

21 A. Yes.

22 MR. SARWAR: Objection, form.

23 Q. (BY MS. RODRIGUEZ) Okay. Let's talk about
24 ground 3. This is a combination of Usui, Yu, and
25 Adesida, can you please go to paragraphs 130 through

1 131. Do you see those?

2 A. Yes.

3 Q. Do these paragraphs discuss the combination
4 for ground 3 for claims 9 and 14?

5 A. Yes.

6 MR. SARWAR: Objection, form.

7 Q. (BY MS. RODRIGUEZ) In paragraph 131, you
8 write: A POSITA would have been motivated to implement
9 the electrical contacts as taught by Usui, and Yu, in
10 group III-V semiconductor HEMP as taught by Adesida?

11 A. Yes.

12 MR. SARWAR: Objection, form.

13 Q. (BY MS. RODRIGUEZ) What is the resulting
14 device of the combination of the Usui, Yu and Adesida
15 that you have described for claims 9 and 14?

16 MR. SARWAR: Objection, form.

17 A. III-V semiconductor HEMT.

18 Q. (BY MS. RODRIGUEZ) And how are you using the
19 III-V materials in the combination?

20 A. So, at the effective date, the HEMT structure
21 is very well known, and typically made of III-V
22 materials and a POSITA of the time will be very well
23 understood to take Usui and Yu's teaching to be used,
24 being III-V semiconductor, to achieve the benefit of the
25 HEMT. Also in Yu disclose the application of -- on the

1 III-V materials.

2 Q. In the combination where are the III-V
3 materials of Adesida used?

4 A. The III-V material will be used as the
5 material for the HEMT structure.

6 Q. And what device?

7 A. It's a HEMT device, it's called high electron
8 mobility transistors.

9 Q. But in this specific combination, where are
10 the III-V materials used?

11 A. The III-V material is well known for providing
12 very high carrier mobilities, and to use, for example,
13 to make channel of the HEMT device.

14 MS. RODRIGUEZ: Can we go off the record.

15 (Recess.)

16 Q. (BY MS. RODRIGUEZ) So let's go back to what we
17 were discussing before. We were on paragraph 131, we
18 were discussing ground 3 and we were discussing claim 9.
19 We were discussing the combination of Usui, Yu, and
20 Adesida?

21 A. Yes.

22 Q. In paragraph 131, you write: A POSITA would
23 have been motivated to implement the electrical contacts
24 as taught by Usui and Yu?

25 A. Correct.

1 MR. SARWAR: Objection, form.

2 Q. (BY MS. RODRIGUEZ) In the combined device of
3 Usui, Yu, and Adesida, how are the Usui and Yu teachings
4 applied?

5 A. Correct.

6 MR. SARWAR: Objection, form.

7 Q. (BY MS. RODRIGUEZ) How are the teachings of
8 Usui and Yu applied in that combination?

9 A. So in this combination, we will see that Usui
10 disclose those metal layers and it can be used as gate
11 structure for transistors. And those metal layers could
12 be applied to use the gate structure for the transistor.
13 And by combining to Adesida we see that, first of all,
14 the Adesida III-V semiconductor HEMT is very well known
15 at the time. So a POSITA at the time will be very
16 motivated to use this Usui and Yu combination to achieve
17 the benefit of HEMT using the III-V material in the
18 Adesida. It's predictable to be successful, because in
19 Yu already disclose the -- using, using application
20 III-V materials.

21 Furthermore, because there are two
22 commonly used gate structure, Schottky gate, and the
23 dielectric, and the insulated gate. A POSITA at the time
24 will be further motivated to remove the dielectric in the
25 Yu's gate to form a Schottky gate as showing POSITA. And

1 I also discuss extensively the benefits of HEMT devices,
2 III-V material, as well as the Schottky gate in the
3 declaration.

4 Q. Okay. So now I would like to ask you some
5 questions on claims 11 and 16. Please go to paragraphs
6 132 through 133. Do you see those?

7 A. Yes.

8 Q. Do these paragraphs discuss the combination of
9 ground 3 for claims 11 and 16?

10 A. Yes.

11 MR. SARWAR: Objection to form.

12 Q. (BY MS. RODRIGUEZ) Here you write: A POSITA
13 would have been motivated to implement the electrical
14 contacts as taught by Usui, Yu, as a gates electrode
15 making Schottky contact?

16 A. Correct.

17 MR. SARWAR: Objection, form.

18 Q. (BY MS. RODRIGUEZ) What is the resulting
19 device of a combination of Usui, Yu, and Adesida that
20 you have described for claims 11 and 16?

21 A. So for --

22 MR. SARWAR: Objection form.

23 A. So for claim 11 and 16, we are making Schottky
24 gate structure on III-V semiconductor HEMT device, and
25 we are using the metal layers that taught by Usui and

1 Yu.

2 Q. (BY MS. RODRIGUEZ) Okay. Next, I have some
3 questions on ground 4. Which is a combination of Usui,
4 Yu, and Sugimoto. Can you please go to paragraphs 140
5 through 144. Do you see those?

6 A. 140 and 144, I see these paragraphs.

7 Q. Do these paragraphs discuss the combination of
8 ground 4?

9 A. Yes.

10 MR. SARWAR: Objection, form.

11 Q. (BY MS. RODRIGUEZ) In paragraph 143 you write:
12 It is well known that ohmic contact serve as a source
13 and drain contact in group III-V devices, and allow
14 current to flow into and out of a semiconductor material
15 without distortion of the signal?

16 A. Correct.

17 Q. Do you see that?

18 MR. SARWAR: Objection, form.

19 A. I see that.

20 Q. (BY MS. RODRIGUEZ) Moving to paragraph 144,
21 you write: A POSITA would have been motivated to
22 implement the contact of Usui, Yu, as a power electrode,
23 making an ohmic contact as taught by Sugimoto. Do you
24 see that?

25 A. Yes, correct.

1 MR. SARWAR: Objection, form.

2 Q. (BY MS. RODRIGUEZ) What is the resulting
3 device of a combination of Usui, Yu, and Sugimoto you
4 have described for ground 4?

5 A. So for ground 4, we are using Usui and Yu's
6 teaching of those metal layers to form ohmic contact,
7 and that ohmic contact will serve as power electrode on
8 a III-V semiconductor device, as laid out in Sugimoto.
9 And furthermore, Sugimoto further disclose this III-V
10 device is a HEMT.

11 Q. Do you, do you see -- do the combination of
12 Usui and Yu -- sorry, scratch that.

13 Does the combination have ohmic source and
14 drain electrodes?

15 MR. SARWAR: Form.

16 A. Yes.

17 Q. (BY MS. RODRIGUEZ) Next I would like to
18 discuss ground 5. Ground 5 is a combination of Yu and
19 Usui. Correct?

20 A. Yes.

21 MR. SARWAR: Scope.

22 Q. (BY MS. RODRIGUEZ) Please go to paragraphs 155
23 through 158. Do you see those?

24 A. I have paragraph 155 and 156.

25 MR. SARWAR: Scope.

1 Q. (BY MS. RODRIGUEZ) Do these paragraphs discuss
2 the combination of claims 1 and 13?

3 A. Yes.

4 MR. SARWAR: Scope.

5 Q. (BY MS. RODRIGUEZ) Paragraph 158 states: A
6 POSITA would have been motivated to apply known
7 techniques of limiting the thickness of Usui under layer
8 13, the bottommost metal layer, to diffusion barrier
9 layer, barrier protection layer 218, bottommost layer in
10 Yu's known device. Correct?

11 A. Yes.

12 MR. SARWAR: Scope and form.

13 Q. (BY MS. RODRIGUEZ) Do you see that?

14 A. Yes.

15 Q. What is the resulting device of a combination
16 of Yu and Usui you have described for ground 5, claims 1
17 and 13?

18 A. So claim 1 is saying here, we are making the
19 combination so that we have a capping layer that
20 refractory metal nitride that is thicker than the
21 bottommost metal layer.

22 MR. SARWAR: There was a scope and form
23 objection to that last question.

24 Q. (BY MS. RODRIGUEZ) How are Usui's teachings
25 applied in this combination?

1 MR. SARWAR: Scope and form.

2 A. So in here in Usui's teaching, Usui disclose
3 many layers, metal layers. And Usui discuss that the --
4 this capping layer needs to be thicker than the bottom
5 layer, and, and this is applied here.

6 Q. (BY MS. RODRIGUEZ) Next I would like to ask
7 some questions on ground 6, which is a combination of
8 Yu, Usui, and Adesida. Will you please go to paragraphs
9 190 to 191. Do you see them?

10 A. 190 and 191, I see this.

11 Q. Do these paragraphs discuss the combination of
12 ground 6 for claims 9 and 14?

13 A. Yes.

14 MR. SARWAR: Form.

15 Q. (BY MS. RODRIGUEZ) In paragraph 191, you
16 write: A POSITA would have been motivated to implement
17 Yu's device as a HEMT as taught by Adesida. Do you see
18 that?

19 A. Yes.

20 MR. SARWAR: Form.

21 Q. (BY MS. RODRIGUEZ) What is the resulting
22 device of the combination of Yu -- sorry, Yu, Usui and
23 Adesida you have described for claims 9 and 14?

24 A. A result a HEMT device with the metal layers
25 taught by Yu and Usui as the gate.

1 MR. SARWAR: Form objection to that last
2 one.

3 Q. (BY MS. RODRIGUEZ) And how are Adesida's
4 materials used in the combination?

5 A. So Adesida's material is III-V materials, they
6 will be used, the base materials, semiconductors for the
7 HEMT structure, HEMT device.

8 Q. Next I have some questions on ground 5, claims
9 11 and 16. Can you please go to paragraphs 192 through
10 193; do you see that?

11 A. I need to do 193.

12 Q. Do these paragraphs discuss the combination
13 for claim 11 and 16?

14 A. Yes.

15 Q. Here you write: A POSITA would have been
16 motivated to implement Yu's device as a gate electrode
17 making a Schottky contact as taught by Adesida. Do you
18 see that?

19 A. Yes.

20 MR. SARWAR: Scope and form.

21 Q. (BY MS. RODRIGUEZ) What is the resulting
22 device of a combination of Yu, Usui, and Adesida as you
23 have described for claims 11 and 16?

24 MR. SARWAR: Scope and form.

25 A. So here we are having a III-V HEMT devices

1 with the metal layers from Usui and Yu as the Schottky
2 gate contact, or Schottky gate electrode on these III-V
3 HEMT device.

4 Q. (BY MS. RODRIGUEZ) Next I'd like to ask you
5 about ground 7. This is a combination of Yu, Usui, and
6 Sugimoto. Please go to paragraphs 202 through 206. Do
7 you see that?

8 A. Yes.

9 MR. SARWAR: Scope and form.

10 Q. (BY MS. RODRIGUEZ) In paragraph 205 you write:
11 It was well known that ohmic contact serve as a source
12 and drain contact in group III-V devices and allow
13 current to flow into and out of a semiconductor material
14 without distortion of the signal. Do you see that?

15 A. Yes.

16 MR. SARWAR: Objection, form.

17 Q. (BY MS. RODRIGUEZ) And in paragraph 206 you
18 write: A POSITA would have been motivated to implement
19 the devices of Yu, and Yu and Usui with the power
20 electrode, making ohmic contact as taught by Sugimoto.
21 Do you see that?

22 A. Yes.

23 MR. SARWAR: Form.

24 Q. (BY MS. RODRIGUEZ) What is the resulting
25 device of the combination?

1 A. So the --

2 MR. SARWAR: Form.

3 A. -- the resulting device is group III-V
4 semiconductor device with aluminum and nitride top
5 layer. So III-V nitride HEMT device with the metal
6 layer from Usui as the power electrode here, which is
7 source and drain, and this metal layer is ohmic contact
8 for the source and drain.

9 Q. (BY MS. RODRIGUEZ) Next I'd like to turn to
10 ground 2, here we're discussing claim 3. Please go to
11 paragraphs 106 to 109. Do you see those?

12 A. Yes.

13 MR. SARWAR: Form.

14 Q. (BY MS. RODRIGUEZ) In paragraph 108, it
15 states: It is my opinion that a POSITA would have
16 appreciated that replacing the titanium nitride of Usui
17 with the tantalum (sic) nitride of Yu is merely a
18 suitable design alternative, because Yu discloses both
19 titanium nitride, the material expressly disclosed in
20 Usui as the second metal layer, and tantalum nitride
21 may be employed?

22 A. Yes.

23 MR. SARWAR: Scope and form.

24 Q. (BY MS. RODRIGUEZ) What is the resulting
25 device of the combination of Usui and Yu you have

1 described for ground 2, claim 3?

2 MR. SARWAR: Scope, form.

3 A. So these are the metal layers from Usui, but
4 the capping layer is tantalum nitrate, TAN, as told by
5 Yu.

6 Q. (BY MS. RODRIGUEZ) Does the modification
7 include Usui's device modified by Yu's TAN?

8 MR. SARWAR: Scope and form.

9 A. Correct.

10 Q. (BY MS. RODRIGUEZ) Do you recall Usui figure
11 8, your discussion with Mr. Sarwar?

12 A. Correct.

13 Q. Can you please go to figure 8 in Usui?

14 A. Yes.

15 Q. Is it your understanding that figure 8's an
16 interconnect, a transistor, is it your -- sorry, excuse
17 me.

18 Is it your understanding that figure 8 is
19 an interconnect, a transistor, or some other structure?

20 A. It's an interconnect.

21 MR. SARWAR: There was a form objection
22 to that one, sorry.

23 MS. RODRIGUEZ: We have no further
24 questions.

25 FURTHER EXAMINATION

1 BY MR. SARWAR:

2 Q. Hello again, Dr. Zhao. Did you talk with
3 counsel regarding the testimony you provided on
4 redirect?

5 A. No.

6 Q. Did you meet with counsel or discuss your
7 testimony in any way?

8 A. We did not discuss anything related to the
9 matter.

10 MR. SARWAR: Nothing further.

11

12 (Deposition concluded.)

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25 YUJI ZHAO, Ph.D.

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SEPTEMBER 5, 2025

CHANGES AND SIGNATURE

PAGE	LINE	CHANGE	REASON
------	------	--------	--------

1 I, YUJI ZHAO, Ph.D., have read the foregoing
 2 deposition and hereby affix my signature that same is
 3 true and correct, except as noted above.

4

5 YUJI ZHAO, Ph.D.

6

7 THE STATE OF)

8 COUNTY OF)

9 Before me, , on this day

10 personally appeared YUJI ZHAO, Ph.D., known to me or

11 proved to me on the oath of or through

12 ----- (description of identity card or

13 other document) to be the person whose name is subscribed

14 to the foregoing instrument and acknowledged to me that

15 he/she executed the same for the purpose and

16 consideration therein expressed.

17 Given under my hand and seal of office on this

18 day of , .

19

20

21 NOTARY PUBLIC IN AND FOR

22 THE STATE OF

23 My Commission Expires:

24

25

1 UNITED STATES PATENT AND TRADEMARK OFFICE
 2 BEFORE THE PATENT TRIAL AND APPEAL BOARD
 3 INNOSCIENCE AMERICA, INC.) CASE NO.:
)
) Petitioner,) IPR2025-00175
 4) PATENT NO.:
)
) v.) 8,686,562
 5)
) INFINEON TECHNOLOGIES AMERICAS)
 6 CORP.,)
)
) Patent Owner.)
 7 -----)
)

8

9

10

REPORTER'S CERTIFICATE

11

ORAL VIDEOTAPED DEPOSITION OF

12

YUJI ZHAO, Ph.D.

13

SEPTEMBER 5, 2025

14

15

I, Kimberly Wheelis, Certified Shorthand Reporter in

16

and for the State of Texas, hereby certify to the

17

following:

18

That the witness, YUJI ZHAO, Ph.D., was duly sworn

19

and that the transcript of the deposition is a true

20

record of the testimony given by the witness;

21

That the deposition transcript was duly submitted on

22

to the witness or to the attorney for

23

the witness for examination, signature, and return to me

24

by

25

That pursuant to information given to the deposition

1 officer at the time said testimony was taken, the
2 following includes all parties of record and the amount
3 of time used by each party at the time of the deposition:

4 Mr. Sarwar - 6 hours, 39 minutes

5 Ms. Rodriguez - 38 minutes

6 That a copy of this certificate was served on all
7 parties shown herein on and filed
8 with the Clerk.

9 I further certify that I am neither counsel for,
10 related to, nor employed by any of the parties in the
11 action in which this proceeding was taken, and further
12 that I am not financially or otherwise interested in the
13 outcome of this action.

14 Further certification requirements pursuant to
15 Rule 203 of the Texas Code of Civil Procedure will be
16 complied with after they have occurred.

17 Certified to by me on this day of

18 , .

19 *Kimberly Wheelis*
20 /S/ Kimberly Wheelis

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