

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AMERICAS CORP.,
Patent Owner.

Case No. IPR2025-00175
Patent No. 8,686,562

PATENT OWNER'S RESPONSE

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LISTING OF EXHIBITS

Exhibit	Description
2001	Excerpts from Merriam Webster’s Collegiate Dictionary (10th ed.) (2001)
2002	U.S. Patent Application Publication No. 2008/0251828 A1 (“Meng”)
2003	U.S. Patent Application Publication No. 2011/0247549 A1 (“Sachs”)
2004	Quirk, M., & Serda, J. (2001) Semiconductor Manufacturing Technology. Prentice Hall.
2005	Stewart, C.M., “Interim Processes for PTAB Workload Management,” Memorandum dated March 26, 2025
2006	United States Patent Office, “Guidance on USPTO’s rescission of ‘Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation’ (March 24, 2025), available at https://www.uspto.gov/sites/default/files/documents/guidance_memo_on_interim_procedure_rescission_20250324.pdf .
2007	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Order No. 5, Initial Determination Setting an 18-Month Target Date and Order Setting Preliminary Conference (ITC Sept. 18, 2024)
2008	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Order No. 6, Setting the Procedural Schedule (ITC Sept. 27, 2024)
2009	RESERVED
2010	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Order No. 25, Amending the Procedural Schedule (ITC Feb. 27, 2025)
2011	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Order No. 32, Amending the Procedural Schedule (ITC Apr. 8, 2025)
2012	Email from Niemeyer, Elizabeth, RE: Inv. No 337-TA-1414 Innoscience’s Invalidity Contentions (Feb. 3, 2025)
2013	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Respondents’ Invalidity Contentions (ITC Jan. 24, 2025)
2014	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Respondents’ Invalidity Contentions Appendix B-2 (ITC Jan. 24, 2025)

Exhibit	Description
2015	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Respondents’ Invalidity Contentions Appendix B-3 (ITC Jan. 24, 2025)
2016	Email from Green, Alissa, RE: Inv. No. 337-TA-1414 Infineon's Case Narrowing Disclosure (Apr. 1, 2025)
2017	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Joint Proposed Claim Construction Chart (ITC Jan. 17, 2025)
2018	United States Patent Office, “USPTO rescinds memorandum addressing discretionary denial procedures” (Feb. 28, 2025) available at https://www.uspto.gov/about-us/news-updates/uspto-rescinds-memorandum-addressing-discretionary-denial-procedures .
2019	Vidal, K., “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings With Parallel District Court Litigation,” Memorandum dated Jun. 21, 2022
2020	Email from Lavenue, Lionel RE: Stay, Infineon v. Innoscience – NDCA (Aug. 27, 2024)
2021	<i>Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al.</i> ; Case No. 4:24-cv-01553-YGR, Dkt. No. 55, Joint Stipulation to Stay Pending ITC Proceeding; [Proposed] Order (N.D. Cal. Aug. 30, 2024)
2022	<i>Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al.</i> ; Case No. 4:24-cv-01553-YGR, Dkt. No. 56, Order Staying and Conditionally Closing Case for Statistical Purposes (N.D. Cal. Aug. 30, 2024)
2023	Declaration of Turhan F. Sarwar in Support of Admission <i>Pro Hac Vice</i>
2024	Declaration of Edwin Piner, Ph.D. (“Piner”)
2025	Curriculum Vitae of Edwin Piner, Ph.D.
2026	Transcript of Deposition of Yuji Zhao, Ph.D. (Sept. 5, 2025) (“Zhao-Dep.”)
2027	Larry Zhao, “All About Interconnects” Semiconductor Engineering, https://semiengineering.com/all-about-interconnects/ (Dec. 18, 2017)
2028	U.S. Patent No. 6,249,056 (“Kwon”)
2029	U.S. Patent No. 4,017,890 (“Howard”)
2030	Excerpts from JAEGER, INTRODUCTION TO MICROELECTRONIC FABRICATION (2nd Ed. 2002) (“Jaeger”)
2031	Excerpts from OHRING, THE MATERIALS SCIENCE OF THIN FILMS (1992) (“Ohring”)

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2032	U.S. Patent No. 7,537,951 (“Gambino”)
2033	U.S. Patent App. Pub. No. 2007/0007653 A1 (“Chen-653”)
2034	Stewart, C.M., “Enforcement and Non-Waiver of 37 C.F.R. § 42.104(B)(4) and Permissible Uses of General Knowledge in Inter <i>Partes</i> Reviews,” Memorandum dated July 31, 2025

I. INTRODUCTION

Petitioner fails to carry its burden to demonstrate any Challenged Claim (claims 1-17) in Patent No. 8,686,562 (“562 Patent”) unpatentable.

Every Challenged Claim is directed to an electrical contact for use on a semiconductor device. The electrical contact comprises “an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers.” The capping layer consists only of a refractory metal nitride and has “a thickness greater than that of a bottommost layer of said plurality of metal layers” of the electrode stack. To purportedly meet the above-discussed electrode stack limitations, Grounds 1-4 (“Usui-based grounds”) rely on Usui (EX-1004), and Grounds 5-7 (“Yu-based grounds”) rely on Yu (EX-1005).

In its decision on institution (Paper, 10 “DI”), the Board correctly found that Petitioner’s Yu-based grounds did not meet the claimed capping layer that consists only of a *refractory metal nitride and is thicker than a bottommost layer* of said plurality of metal layers” of the electrode stack. DI, 18-19. The Board should reach the same conclusion at Final Written Decision. The Yu-based grounds fail for this and additional reasons explained below.

For the Usui-based grounds, the POPR explained that Petitioner failed to establish that Usui’s alleged “electrode stack” meets that term under any reasonable claim construction. The Board cited Usui’s interconnect metallurgy

“useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure” and, for purposes of institution, found this “sufficient, on this record, to establish that” Usui’s metallurgy is an “electrode stack.” DI, 11-12. The Board found that “neither party ha[d] taken an explicit position on the appropriate construction of ‘electrode stack’” and “direct[ed] the parties to take specific positions during the trial on the appropriate construction of ‘electrode stack’ and whether the claims are unpatentable...under such a specific construction.” DI, 14.

Below, Patent Owner (“Infineon”) explains the appropriate construction of “electrode stack.” Infineon also explains that every ground fails if the Board gives “electrode stack” its proper construction. Infineon’s arguments are supported by testimony from Edwin Piner, Ph.D., who has substantial experience in the technology area – Piner (EX-2024), ¶¶2-10, 24-46; EX-2025 – and admissions from Petitioner’s expert, Yuji Zhao, Ph.D.

The POPR focused only on deficiencies in the Petition’s showing for the independent claims. This POR identifies additional deficiencies in the Petition’s showing for many of the dependent claims. Time and again, the Petition simply alleges that claimed features were “known” because they are taught in disparate prior art references and then alleges that *KSR*’s known elements/predictable results rationale supports obviousness. That *KSR* rationale does not support Petitioner’s

combinations, which dramatically change the functions of the components that Petitioner cobbles together in a hindsight attempt to reconstruct the dependent claims. Petitioner's challenges to the dependent claims are internally inconsistent and combine prior art teachings in ways a POSA¹ never would have. The Petition separately fails for many of the dependent claims as discussed below.

II. "ELECTRODE STACK" CLAIM CONSTRUCTION

Every Challenged Claim recites "[a]n electrical contact for use on a...semiconductor device, said electrical contact comprising an *electrode stack*."²

At institution, the Board preliminarily suggested that any metallurgy forming "electrical connections or wiring such as *between* active and/or passive *devices* of an integrated circuit structure" is an "electrode stack." DI, 12. Respectfully, that preliminary finding cannot be maintained because it is inconsistent with the evidence.

As detailed below, an electrode is part of a semiconductor device (e.g., a transistor) used to establish electrical contact with a nonmetallic part of the semiconductor device or control the operation of the semiconductor device. Metal forming "connections or wiring...*between*...*devices* of an integrated circuit" (DI,

¹ Infineon does not challenge Petitioner's POSA definition (Petition, 6) because the Petition fails even if that definition is adopted.

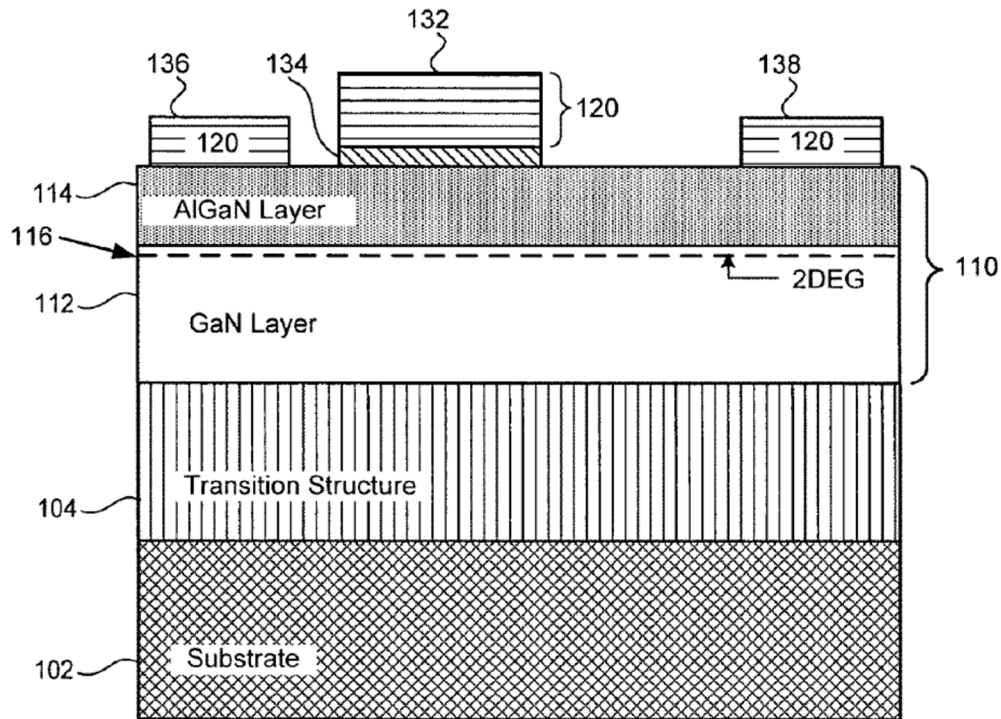
² All emphasis is added unless otherwise indicated.

12) – i.e., an *interconnect* between devices – is not part of any semiconductor device and not an electrode.

A. Intrinsic Evidence

“[T]he specification ‘is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (*en banc*).

The '562 Patent specification describes source, drain, and gate electrodes for a transistor. EX-1001, Fig. 1 (below), 2:58-60 (“Structure 100 also includes a plurality of electrical contacts including source electrode 136, drain electrode 138, and insulated gate electrode 132.”), 3:19-35. Fig. 1 illustrates a compound semiconductor formed from gallium nitride (GaN) layer 112 and aluminum gallium nitride (AlGaN) layer 114. EX-1001, 1:7-15, 2:53-65.

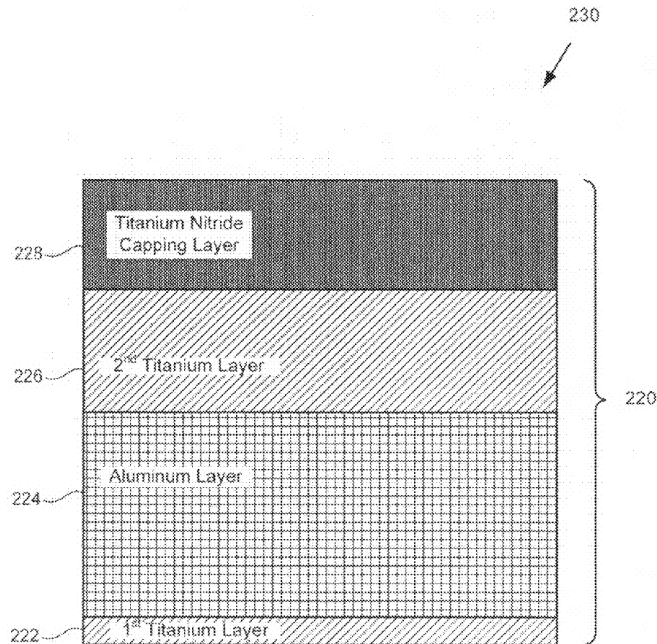


'562 Patent, Fig. 1

“Source electrode 136 and drain electrode 138” – each formed by an “electrode stack 120” – are “power electrodes” that touch, and are “*ohmically coupled* to[,] the semiconductor.” EX-1001, 3:19-28, 1:33-43.

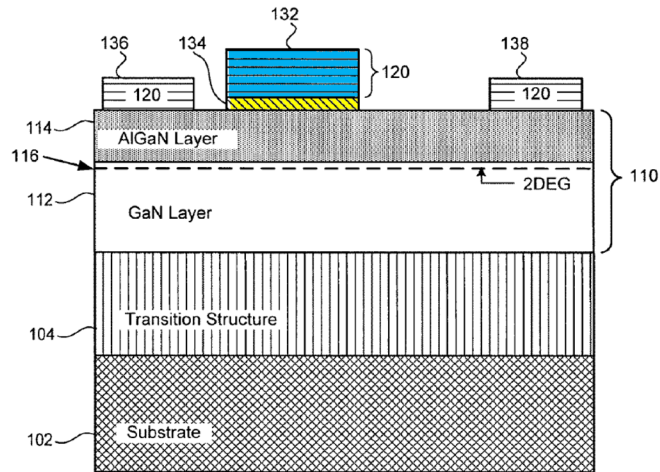
Gate electrode 132 is “an insulated gate electrode” formed by the same electrode stack 120 but separated from the semiconductor by an insulating oxide layer 134. *Id.*, 3:21-33. “In other embodiments...gate electrode 132 comprising electrode stack 120 may make Schottky contact with GaN body 110” with no insulating layer in between. EX-1001, 3:31-35. Thus, a “Schottky” barrier forms at the metal-semiconductor junction. EX-1011, 219; Piner, ¶86; Zhao (EX-1002), ¶58.

The '562 Patent specification discloses an embodiment of the inventive electrical contact comprising an electrode stack in Fig. 2 (reproduced below), which “may...correspond to *any* of source electrode 136, drain electrode 138, or insulated gate electrode 132, in FIG. 1.” EX-1001, 3:36-45.



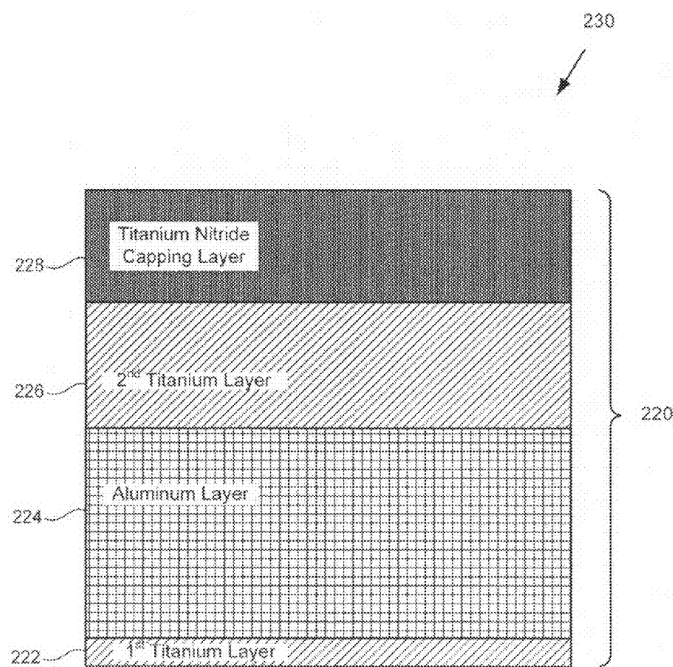
'562 Patent, Fig. 2

In Fig. 1 (annotated below), insulated gate electrode 132 (blue) is stacked over “gate insulating layer 34” (yellow). EX-1001, 3:28-35. Gate electrode 132 is formed by “electrode stack 120” and does not include gate insulating layer 134 which “underl[ies]” “electrode stack 120.” *Id.*, 3:28-31, Fig. 1 (the labelled “electrode stack 120” does not include insulating layer 134). Indeed, the same “electrode stack 120” forms each of the source and drain electrodes 136 and 138 that have no insulating layer 134. *Id.*, 3:23-28, Fig. 1.



'562 Patent, Fig. 1 (annotated)

Fig. 2 (below) is a more detailed illustration of an “[e]lectrode stack 220” that “corresponds to electrode stack 120 in FIG. 1.” EX-1001, 3:42-43. As seen in Fig. 2, electrode stack 220 does not include an insulating layer. Fig. 2’s “[e]lectrical contact 230 may...correspond to any of source electrode 136, drain electrode 138, or *insulated gate electrode* 132 in FIG. 1.” *Id.*, 3:40-42.



'562 Patent, Fig. 2

Thus, the '562 Patent specification uses “electrode stack” to refer to a stack of layers forming an electrode and describes three electrode types: (1) a “power electrode[]” touching (“*ohmically coupled* to”) the nonmetallic semiconductor³ (EX-1001, 3:19-28, 1:33-43); (2) a transistor gate electrode that controls the flow of electrons or holes through the transistor and touches (makes “Schottky contact” with) the nonmetallic semiconductor (*id.*, 3:31-35); and (3) a transistor gate electrode that controls the flow of electrons or holes through the transistor but is “an insulated gate electrode” separated from the semiconductor by an insulating layer 134 (*id.*, 3:21-33). *See also id.*, claims 10-12; EX-1015, 503-505 (corroborating the functions of transistor source, drain, and gate electrodes).

The Board need not reach an outer boundary construction for “electrode stack” to reject the Usui-based grounds (*infra* §§III-IV) or the Yu-based grounds (*infra* §§V-VI). *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (the Board need only construe terms to the extent necessary to resolve the parties’ dispute). If the Board reaches an outer boundary construction for “electrode stack,” the proper construction in view of the specification is a stack of conductive layers that form an electrical contact that is a part of a semiconductor device and used to (1) establish electrical contact with a

³ This electrode type forms a transistor’s source and drain electrodes.

nonmetallic part of the semiconductor device (like the source, drain and Schottky gate electrodes in the '562 Patent specification) or (2) control the operation of the semiconductor device (like the insulated or Schottky gate electrodes in the '562 Patent Specification). Piner, ¶¶80-91.

B. Extrinsic Evidence

Petitioner never explains the plain meaning of “electrode stack” that the Petition purportedly applied. Petition, 7; DI, 14 (Petitioner took no “explicit position on the appropriate construction of ‘electrode stack’”). Any meaning divorced from the specification would be inappropriate. *Supra* §II.A (discussing *Phillips*). Without conceding that dictionary definitions are the appropriate way to interpret “electrode stack,” Infineon notes that the Usui structure Petitioner relies upon (*infra* §III) is not an “electrode” even under a broad dictionary definition.

Merriam-Webster’s Collegiate Dictionary defines “electrode” as “1: a conductor used to establish electrical contact with a ***nonmetallic*** part of a circuit” and “2: an element in a semiconductor device (as a transistor) that emits or collects electrons or holes or controls their movements.” EX-2001, 371. The '562 Patent’s electrodes meet these definitions.

Definition 1 is met by Fig. 1’s source and drain electrodes that are “ohmically coupled” to the semiconductor, and by the Schottky gate electrode embodiment because each of those electrodes is a conductor used to

establish electrical contact with a nonmetallic (semiconductor) part of a circuit. EX-1001, 1:33-43, 3:19-21, 3:31-35; Piner, ¶¶92-93. The electrodes in the '562 Patent also all meet definition 2, because each is “an element in a semiconductor...transistor” and the source and drain electrodes “emit[]” or “collect[]” electrons or holes while the gate electrode “control[s] the movement of” electrons or holes between the transistor’s source and drain regions. Piner, ¶¶94-95. Thus, the extrinsic evidence is consistent with the '562 Patent specification’s explanation of an “electrode.”

III. GROUND 1 FAILS BECAUSE PETITIONER FAILS TO ESTABLISH THAT USUI’S INTERCONNECT METALLIZATION STRUCTURE IS AN ELECTRODE STACK AS CLAIMED

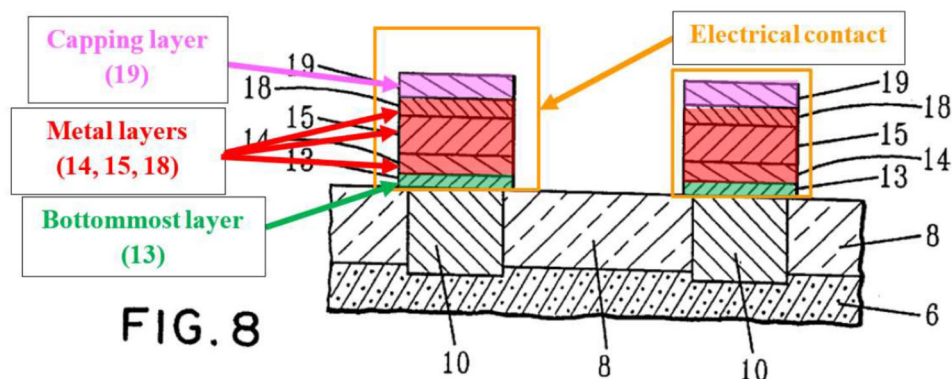
Ground 1 alleges that claims 1-2 and 4-7 are anticipated by Usui. Petition, 3, 8-16. Claim 1 is directed to an electrical contact for use on a semiconductor device. Limitation [1pre].⁴ The electrical contact comprises “an *electrode stack* including a plurality of metal layers and a capping layer formed over said plurality of metal layers.” Limitation [1a]. The capping layer has “a thickness greater than that of a bottommost layer of said plurality of metal layers” of the electrode stack. Limitation [1c].

⁴ Infineon herein adopts the Petition’s claim limitation labelling.

Other than repeating the claim language and alleging that Usui “discloses” what Limitation [1a] requires, *the Petition entirely ignores the “electrode stack” requirement.* Petition, 11-12. The Petition never construes “electrode stack,” never explains what an “electrode” or “electrode stack” is, and presents no evidence or argument establishing that the Usui structure Petitioner identifies as meeting Limitation [1a] – layers 13-15 and 18-19 (Petition, 11), which Usui calls a “interconnect metallurgy structure” (Usui, 3:23) – is an “*electrode* stack.” Piner, ¶¶133-138. For that reason alone, Ground 1 fails.

Worse yet, Usui’s interconnect metallurgy structure is not an “electrode stack” as used in the ’562 Patent or even under a broad dictionary definition. As shown from the Petition’s annotated FIG. 8 (reproduced below from Petition, 11), Usui’s interconnect metallurgy structure is connected to “interplanar stud connection 10,” which is a “device contact metallization” that “make[s] connection to a device substrate 6.” Usui, 3:24-27, 5:14-15.⁵ Petitioner never explains why, if there is an electrode in Usui FIG. 8, the electrode is not the “device contact metallization 10” that “make[s] connection to” the semiconductor “device substrate 6.” Usui, 3:24-27, 5:14-15; Piner, ¶136.

⁵ Usui’s FIGs. 1 and 8 are identical. Usui, 3:2-8 (FIG. 8 is the last of FIGs. 2-8, illustrating the process for making FIG. 1’s device).



Petitioner's Annotated Usui, Fig. 8

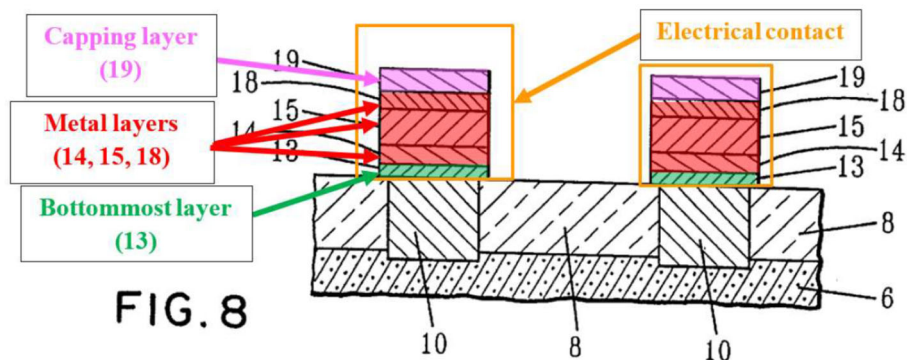
As detailed below, Ground 1 fails because Petitioner fails to establish that Usui's interconnect metallurgy structure is an electrode stack as claimed.

A. Petitioner Fails to Explain its Alleged Plain Meaning Construction of "Electrode Stack"

The Board's rules specify "Content" the Petition "must" have. *See* 37 C.F.R. §§ 42.22 and 42.104. The Petition "**must**" identify "how the challenged claim is to be construed" and "[h]ow the **construed** claim is unpatentable." 37 C.F.R. § 42.104(b)(3)-(4).

The Board preliminarily found Petitioner's assertion that "the plain meaning of each term can be applied" (Petition, 7) meets this requirement. DI, 13. But as the Board noted, the Petition never explains what the alleged "plain meaning" is for "electrode" or "electrode stack." DI, 14 (Petitioner takes no "explicit position on the appropriate construction of 'electrode stack.'"). The Petition just alleges in conclusory fashion that "Usui discloses an electrode stack in Figure 8 with a

plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metals.” Petition, 11.



Petitioner’s Annotated Usui, Fig. 8

Because Petitioner never explained its alleged plain meaning of “electrode stack,” the Board cannot evaluate if Petitioner’s alleged plain meaning is correct, let alone whether Usui meets that unstated plain meaning. It was Petitioner’s burden to explain *in the Petition* the alleged “plain meaning” of “electrode stack” (Petition, 7 and 11) and how and why Usui’s interconnect metallization structure meets that plain meaning. 37 C.F.R. § 42.104(b)(3)-(4). Petitioner did not meet that burden. The Usui-based grounds fail for this reason alone.

B. No Evidence Supports Petitioner’s Assertion that Usui’s Interconnect Metallization Structure is an “Electrode Stack”

The Petition “must include” a “detailed explanation of the significance of the evidence.” 37 C.F.R. § 42.22(a)(2). Petitioner alleges Usui’s interconnect metallization structure (layers 13-15 and 18-19) is an “electrode stack” (Petition, 11) but provides *no* explanation (“detailed” or otherwise) of *how or why* Usui’s

interconnect metallurgy structure is allegedly an “electrode stack” and cites no *evidence* to support that conclusory assertion.

The Petition’s mapping of Limitation [1a] to Usui alleges that Usui’s interconnect metallization structure (layers 13-15 and 18-19) is an “electrode stack” only in its opening sentence, which *only cites “Usui, Fig. 8; Zhao ¶89.”* Petition, 11.⁶ The only disclosure in Usui that Petitioner cites – Fig. 8 – does not label Usui’s interconnect metallization structure an “electrode stack” or otherwise support Petitioner’s assertion that Usui’s layers 13-15 and 18-19 are an “electrode stack.”

Dr. Zhao’s declaration cannot save Petitioner from the Petition’s failures to explain how “electrode stack” is construed, and how and why Usui’s interconnect metallization structure (layers 13-15 and 18-19) is allegedly an “electrode stack” as claimed. This is “content” the *Petition* must have, and arguments cannot be

⁶ The remainder of Petitioner’s Limitation [1a] mapping cites additional disclosures in Usui for other reasons, e.g., to allege that layers 13-15 and 18 are metal and capping layer 19 is titanium nitride. Petition, 11 (citing Usui, Fig. 1, 3:38-41, 3:58-60, 4:4-5, 5:38, 5:52, 5:54-59). None of those disclosures characterize Usui’s interconnect metallization structure (layers 13-15 and 18-19) as an electrode stack and Petitioner never alleges that they do.

incorporated by reference from the expert declaration. 37 CFR §§ 42.22, 42.104(b)(3)-(4), and 42.6(a)(3).

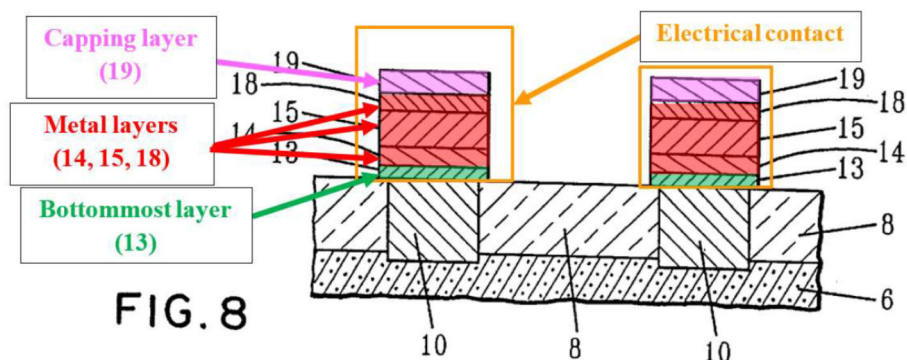
Even if the Board were to wade into Dr. Zhao's declaration, it does not remedy the Petition's failures. The Petition's mapping of Limitation [1a] to Usui cites Zhao ¶¶89-91. Petition, 11-12. Those paragraphs do ***nothing but repeat the Petition's unsupported assertions word-for-word.*** Compare Zhao ¶¶89-91 with Petition, 11-12. Dr. Zhao never explains what the alleged plain meaning of "electrode stack" is and never explains how or ***why*** Usui's interconnect metallization structure (layers 13-15 and 18-19) is an electrode stack. Dr. Zhao's conclusory assertion that Usui's metallization structure is an "electrode stack" is unsupported by any reasoned analysis or corroborating evidence, so it warrants no weight. *Xerox v. Bytemark*, IPR2022-00624, Paper 9, 15 (Aug. 24, 2022) (precedential) ("[T]he cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight."); *see also id.* (quoting 37 C.F.R. § 42.65(a): "Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

Because the Petition cites no ***evidence*** establishing that Usui's interconnect metallurgy structure is an electrode stack, Ground 1 fails. Piner, ¶¶139-143.

C. Usui's Interconnect Metallization Structure is Not an Electrode Stack Under the Proper Construction

As discussed *infra* §II, the '562 specification uses “electrode stack” to refer to a stack of layers that form an electrode in a semiconductor device, and describes three electrode types: (1) a “power electrode[]” that touches and is “*ohmically coupled* to” nonmetallic semiconductor material (EX-1001, 3:19-28, 1:33-43); (2) a transistor gate electrode that controls the flow of electrons or holes through the transistor and makes “Schottky contact” with nonmetallic semiconductor material (*id.*, 3:31-35); and (3) an insulated transistor gate electrode that controls the flow of electrons or holes through the transistor and is separated from the semiconductor by an insulating layer (*id.*, 3:21-33). Piner, ¶¶144-145.

Petitioner does not even *try* to establish that the Usui structure that Petitioner purports to be an “electrode stack” is an electrode stack as described in the '562 Patent.



Petitioner's Annotated Usui, Fig. 8

The identified Usui structure is instead an “interconnect metallurgy structure”⁷ – an *interconnect* (Piner, ¶¶146-148, 62-68, 96-105; EX-2027; EX-2028) – that “preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 to make connection to a device substrate 6.” Usui, 3:24-27; *see also id.*, 5:14-15 (referring to the interplanar stud connection as “*device* contact metallization 10”), 3:2-8 (FIGs. 2-8 illustrate the process for making FIG. 1’s device).⁸

Usui never says that its interconnect metallization structure (layers 13-15 and 18-19) is an “electrode” or forms an “electrode stack.”⁹ Usui’s interconnect metallization structure is manifestly not an electrode stack as disclosed in the ’562 Patent because it is not (1) a power electrode making ohmic contact with the nonmetallic semiconductor material (EX-1001, 3:19-27, 1:33-43); (2) a transistor

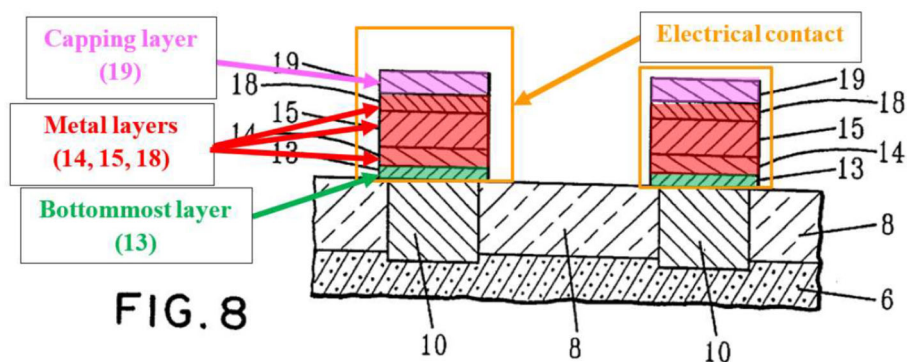
⁷ Usui also calls this a “metallization structure.” Usui, 3:38.

⁸ Usui’s FIGs. 1 and 8 are identical.

⁹ Dr. Zhao testified that he only focused on whether the prior art had a stack of metal layers and a capping layer as claimed without regard to whether the stack was an “*electrode* stack.” *E.g.*, Zhao-Dep., 172:20-175:5. That improperly reads “electrode” out of the claims. Piner, ¶¶76-79.

gate electrode making “Schottky contact” with the nonmetallic semiconductor (*id.*, 3:31-35); or (3) an insulated transistor gate electrode (*id.*, 3:21-33). Piner, ¶149.

Infineon does not concede that a meaning divorced from the specification would be appropriate (*supra* §II), but notes that the Usui structure Petitioner relies on is not an “electrode” even under the broad dictionary definitions discussed *supra* §II.B. Usui’s interconnect metallization structure (layers 13-15 and 18-19) is not “a conductor used to establish electrical contact with a nonmetallic part of a circuit.” EX-2001, 371 (definition 1). As shown below, Usui’s interconnect metallization layer is connected to “interplanar stud connection 10” – it is *stud connection 10* that “make[s] connection to a device substrate 6.” Usui, 3:24-27.



Petitioner’s Annotated Usui, Fig. 8

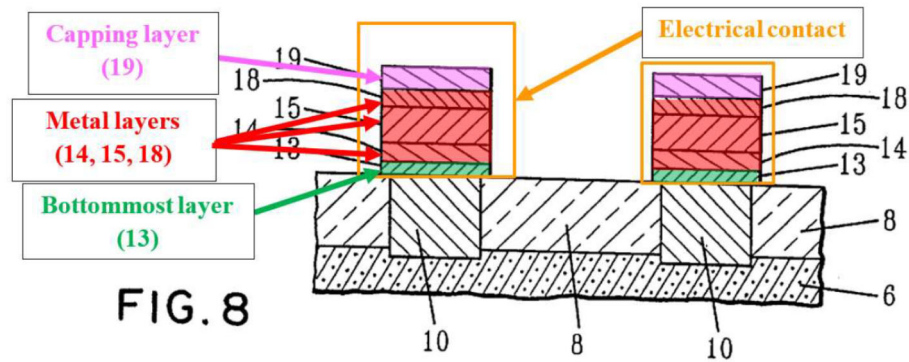
Stud connection 10 is *metal*. Usui, 5:14-15 (“device contact *metallization* 10”).

Thus, Usui’s interconnect metallization structure is connected to *metal* stud connection 10. Usui’s interconnect metallization structure (layers 13-15 and 18-19) is not “a conductor used to establish electrical contact with a nonmetallic part

of a circuit” and is thus not an “electrode” under Merriam-Webster’s definition 1. EX-2001, 371; Piner, ¶150.

Usui’s interconnect metallization structure also does not meet Merriam-Webster’s definition 2. Piner, ¶151. Usui never teaches that its interconnect metallization structure (layers 13-15 and 18-19) is “an element *in a semiconductor device* that emits or collects electrons or holes or controls their movements.” EX-2001, 371. Usui’s interconnect metallization structure is not an element of a semiconductor device at all – it is used to connect two devices. As its name signifies, Usui’s “*interconnect* metallurgy” (Usui, 3:23-27) “form[s] electrical connections or *wiring* such as *between* active and/or passive *devices* of an integrated circuit structure” (Usui, 1:11-14). Fig. 8’s single interconnect layer is “repeated in a multiple level sequence to complete the *interconnect circuit for the devices*.” Usui, 4:10-15.

Petitioner mischaracterizes Usui’s *interconnect* metallization structure (layers 13-15 and 18-19) as an electrode stack to try meeting claim 1’s requirement that the capping layer is thicker than the bottommost layer of the plurality of metal layers of the electrode stack. *See* Limitation [1c]. Petitioner ignores Usui’s “*device contact* metallization 10” (Usui, 5:14-15), which Fig. 8 illustrates as thicker than capping layer 19. Piner, ¶¶152-153.



Petitioner's Annotated Usui, Fig. 8

Petitioner cannot meet its burden to show Usui has an “electrical *contact*” comprising an “electrode stack” as claimed by ignoring Usui’s “device *contact* metallization 10” (Usui, 5:14-15) which provides a “device *contact*” to Usui’s *nonmetallic* semiconductor substrate 6. EX-2001, 371; Piner, ¶153 (citing EX-2032; EX-2033).

D. Ground 1 Conclusion

Ground 1 fails for the following independent reasons: (1) Petitioner fails to meet its burden to explain how “electrode stack” is construed under Petitioner’s alleged “plain meaning”; (2) Petitioner fails to meet its burden to explain how or why Usui’s interconnect metallization structure is an electrode stack as claimed; (3) Petitioner submits no evidence supporting Petitioner’s assertion that Usui’s interconnect metallization structure is an “electrode stack”; and (4) Petitioner ignores that Usui’s interconnect metallization structure is connected to device contact metallization 10 that provides a device contact to the nonmetallic semiconductor substrate.

IV. GROUNDS 2-4 FAIL

A. Grounds 2-4 Fall with Ground 1

Ground 2 challenges independent claim 13 which recites an electrical contact (for use on a semiconductor device) comprising “an *electrode stack* including a plurality of metal layers and a capping layer formed over said plurality of metal layers,” where the capping layer forms a top of the electrical contact and is thicker than a “bottommost layer of said plurality of metal layers” of the electrode stack. Limitations [13pre]-[13a] and [13c].

Ground 2 relies on Yu to address claim 13’s requirement for a Ground III-V semiconductor device. Ground 2 relies on Usui’s same interconnect metallization structure that Ground 1 relies on to meet claim 13’s limitations reciting an electrical contact comprising an “electrode stack.” Petition, 18-19 (“A POSITA would have been motivated to implement the *electrical contacts as taught by Usui* in group III-V semiconductor devices, as taught by Yu”). Indeed, Petitioner relies entirely on Ground 1’s showing for how Usui purportedly meets claim 1’s corresponding limitations to meet claim 13’s Limitations [13a] and 13[c] that require an “*electrode* stack including a plurality of metal layers and a capping layer,” where the capping layer forms a top of the electrical contact and is thicker than a “bottommost layer of said plurality of metal layers” of the electrode stack. Petition, 23 (alleging that “[13a] is identical to [1a]. [13a] is obvious as explained

for [1a]” and that “[13c] is identical to [1c]. [13c] is obvious as explained for [1c]”). Thus, Ground 2’s showing for independent claim 13 inherits Ground 1’s above-identified flaws. Piner, ¶¶154-155.

Grounds 2-4 address certain dependent claims. Petition, 3. The Petition’s showing in Grounds 2-4 for each dependent claim inherits the Petition’s failures for the independent claim from which it depends.

Thus, Grounds 2-4 inherit all Ground 1’s above-discussed flaws and fail for the same reasons. Piner, ¶156.

B. Ground 2 Fails for Claims 12 and 17 for Additional Reasons

Claims 12 and 17 require that the electrical contact is “implemented with a gate insulator” under the electrode stack “to provide an insulated gate electrode.”

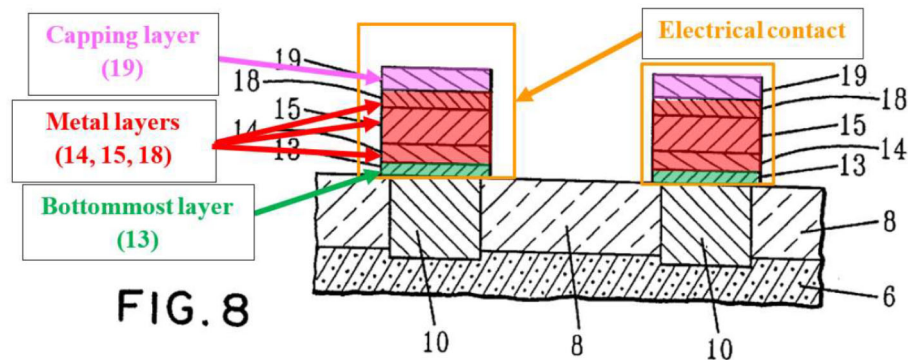
Ground 2 alleges obviousness over Usui and Yu. Petitioner alleges that Yu motivates three disparate modifications to Usui. Petition, 16-17. But the Petition fatally fails to explain the contemplated workings of its Usui-Yu combination and never maps any claim to a clearly-explained combination. *Personal Web Techs. v. Apple*, 848 F.3d 987, 994 (Fed. Cir. 2017) (“[A] clear, evidence-supported account of the contemplated workings of the combination is a *prerequisite* to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination and reasonably expect success in doing so.”).

Petitioner admits Usui lacks a gate insulator layer but alleges “Yu does.” Petition, 19. That does not establish obviousness. To demonstrate obviousness, Petitioner needed to establish some supportable, non-hindsight *reason* why a POSA “would have selected and combined [the] prior art elements” *in a manner “yield[ing] the claimed invention.”* *Unigene Labs. v. Apotex*, 655 F.3d 1352, 1360 (Fed. Cir. 2011); *see also KSR v. Teleflex*, 550 U.S. 398, 418 (2007) (obviousness requires establishing some “*reason* for combining” the prior art “*in the manner claimed*”); *TQ Delta v. Cisco*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) (reversing obviousness determination because Board “fail[ed] to identify any actual *reason why* a skilled artisan would have combined the elements *in the manner claimed.*”) (citations omitted).

Petitioner alleges “Usui describes an electrical contact suitable to provide connections or wirings *between...devices* of an integrated circuit” and that it was known to isolate the gate from the channel in a thin film transistor. Petition, 19-20. From this, Petitioner concludes: “it would have been obvious to implement the electrical contact of Usui with Yu’s gate insulator layer because Usui discloses the importance of improving electromigration characteristics and such [gate insulator] layers are commonly provided *under gate structs to address gate leakage*—combining prior art elements according to known techniques to a known device

ready for improvement to yield predictable results.” Petition, 20 (citing *KSR* and Zhao ¶¶62, 114).

Petitioner’s proposed modification is not one POSAs would have made. Piner, ¶¶158-162. While Petitioner does not illustrate it, Petitioner’s proposed modification inserts insulating layers (Yu layers 214 and 216) under Usui’s alleged electrode (Usui’s layers 13-15 and 18-19). Petition, 11.



Petitioner’s Annotated Usui, Fig. 8

Even if Usui’s identified metal layers formed an electrode – they do not, *supra* §III – there is no need to “isolat[e]” Usui’s alleged electrode “from the channel so that no current flows” to “address gate leakage” (Petition, 20) because Usui does not teach that its alleged electrode is a transistor gate electrode overlying a transistor channel. Piner, ¶¶163-166. Usui Fig. 8 does not even disclose a transistor, let alone that the alleged electrode overlies a transistor channel. Piner, ¶167; Zhao-Dep. (EX-2026), 58:17-59:17 (“...in figure 8, there’s no information here I could, I could say whether it is or not a transistor...”), 59:18-60:1 (“...whether the...device

substrate layer 6 includes a transistor, or not a transistor, it's not discussed in Usui.”). Because Usui does not disclose a transistor gate that would benefit from an insulating layer, Petitioner's alleged motivation for modifying Usui to use a gate insulating layer fails.

Petitioner also fails to establish a reasonable expectation of success. *Eli Lilly & Co. v. Teva Pharms. Int'l*, 8 F.4th 1331, 1344 (Fed. Cir. 2021) (reasonable expectation of success is required to establish obviousness). Indeed, Petitioner's proposed modification would have rendered Usui inoperable for its intended purpose. That defeats obviousness. *In re Gordon*, 733 F.2d 900, 902 (Fed.Cir.1984).

Usui's metal layers 13-15 and 18-19 provide “electrical connections or wiring in electronic devices” with improved “electromigration characteristics.” Usui, 1:17-23, 2:33-39; Petition, 19 (admitting same); Piner, ¶¶168-169; Zhao-Dep., 13:9-11, 13:23-14:9. Interconnect metal layers 13-15, 18-19 provide an electrical connection between “interplanar stud connection 10” (Usui, 3:27) and another layer of interconnect metal layers, with a “multiple level sequence” of interconnect layers “complet[ing] the interconnect circuit” to another device not shown in Fig. 8. Usui, 4:10-15; Piner, ¶170; Zhao-Dep., 49:24-50:10.

Yu's gate insulator layer is not conductive. Yu, [0039]; Piner, ¶171; Zhao-Dep., 89:18-25, 90:8. Thus, placing Yu's gate insulating layer under the alleged

electrode in Usui, as Petitioner alleges (Petition, 19-20), would place an insulator ***between*** Usui’s bottommost layer 13 and interplanar stud connection 10 and ***break*** the electrical connection therebetween. Piner, ¶172. This would have rendered Usui inoperable for its intended purpose of providing improved “electrical connections or wiring” between devices of an integrated circuit. *Id.*; Usui, 1:11-15.

Petitioner’s assertion that its Usui-Yu combination “combin[es] prior elements according to known techniques to [yield] a known device ready for improvement” (Petition, 20) likewise fails. Petitioner’s invoked *KSR* rationale only applies when elements are combined “***with no change in their respective functions.***” *KSR*, 550 U.S. at 415-416. Petitioner’s conclusory assertion that Usui was “ready for improvement” never explains how Usui allegedly would have been improved by “implement[ing] the electrical contact of Usui with Yu’s gate insulating layer” (Petition, 20) despite Usui not disclosing a transistor gate electrode that would be improved by being isolated from a likewise-undisclosed transistor channel. Piner, ¶173; Zhao-Dep., 58:17-60:1. Petitioner’s combination also ***changes*** the function of both Usui’s interconnect (which would be inoperable

as an interconnect as discussed above) and Yu's gate insulating layer¹⁰ (which would no longer separate a gate electrode from a transistor channel as in Yu). Piner, ¶174. Because Petitioner's combination changes component functions, Petitioner's invoked *KSR* rationale does not apply.

¹⁰ Petitioner does not allege that a POSA had reason to replace *Yu*'s gate electrode with Usui's metal layers and instead alleges a POSA would have implemented *Usui* with a gate insulating layer. Petition, 20. If Petitioner belatedly were to allege that a POSA would have replaced Yu's gate electrode with Usui's metal stack, that would fail for multiple reasons. First, it would preclude application of the *KSR* rationale Petitioner invokes (Petition, 20) because it would change the function of *Usui*'s metal layers from a single interconnect layer – connecting metal stud 10 to another interconnect level forming an interconnect circuit to another device (Usui, 3:23-27, 4:10-15) – to a gate electrode. Piner, ¶175. Second, POSAs would not have made such a modification. Usui teaches a particular metal stack for wires to mitigate electromigration due to high current density (Usui, 1:30-41, 2:33-39; *infra* §IV.D.2) which is not a concern for Yu's gate electrode which does not experience high current density. Piner, ¶175. Conversely, Yu teaches a specific metal stack with a particular work function chosen to be compatible with a *high-K dielectric* gate insulator. *Id.*; Yu, [0004], [0029]; *infra* §V.A.

Ground 2 fails to establish any non-hindsight reason why a POSA would have combined Usui and Yu in the manner alleged to meet claims 12 and 17 with a reasonable expectation of success.

C. Ground 3 Fails for Additional Reasons

1. Claims 11 and 16

Claims 11 and 16 require that the electrical contact is “a gate electrode making Schottky contact with said...semiconductor device.” A gate electrode making Schottky contact has no insulating layer between the gate electrode and the semiconductor. EX-1001, 3:31-35; EX-1011, 219; Piner, ¶¶177-178; Zhao, ¶58; *supra* §II.A.

Ground 3 alleges obviousness over Usui, Yu, and Adesida (EX-1006). Petitioner admits Usui and Yu do not disclose “an electrical contact implemented as a gate electrode making Schottky contact” but alleges “Adesida does.” Petition, 26; *see* Piner, ¶¶115-122 (describing Adesida). That does not establish obviousness. Petitioner needed to establish some supportable, non-hindsight reason why a POSA would have combined Usui, Yu, and Adesida in the manner claimed, with a reasonable expectation of success. *Supra* §IV.B (citing authority).

a. Petitioner Fails to Establish Any Reason to Have Modified Usui Based on Yu and Adesida in the Claimed Manner

Petitioner alleges “[i]t would have been *obvious to* implement the electrical contact of Usui-Yu in a device with a gate electrode making Schottky contact, as

taught by Adesida. Zhao ¶¶48-61, 137; Sections VII.C.1, VII.C.1.b.” Petition, 29. Obviousness is a legal conclusion that must be demonstrated by establishing some *reason* why a POSA would have combined the prior art elements in the manner claimed with a reasonable expectation of success. *Supra* §IV.B. Petitioner’s conclusory assertion provides no such reason.

Petitioner cites “Sections VIII.C.1, VIII.C.1.b” (Petition, 29) but no supportable reason to combine is found there. Section VIII.C.1 merely alleges that Adesida is analogous art. Petition, 24. Section VIII.C.1.b says that Schottky gate contacts were known in group III-V devices, like Yu’s and Adesida’s, and were “well known for their suitability for high frequency applications and therefore enhanced electromigration.”¹¹ Petition, 26. Even if Petitioner’s assertions that a Schottky gate electrode was known to have benefits over insulated gate electrodes are accepted as true, they establish no reason why a POSA would have modified *Usui* because *Usui does not disclose a transistor gate electrode*. *Supra* §IV.B; Piner, ¶¶179-183; Zhao-Dep., 58:17-60:1.

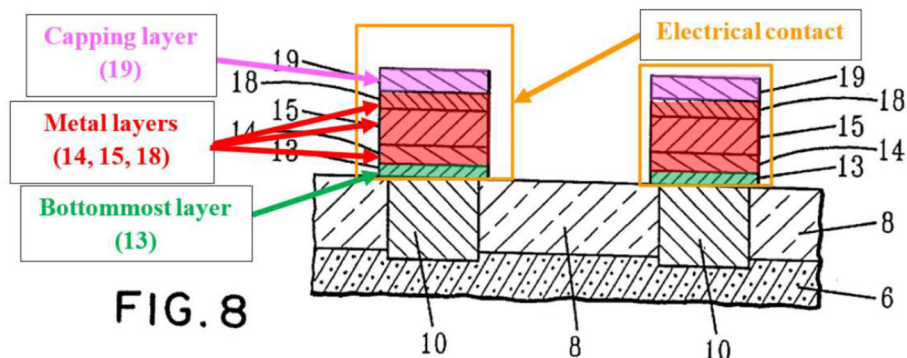
Petitioner’s only argument that mentions modifying *Usui* states in conclusory fashion that “it was well-known...that implementing the *Usui*-Yu

¹¹ Petitioner misunderstands “electromigration” which *Usui* teaches should be reduced – not enhanced. *Infra* §IV.D.2.

contact as a Schottky contact, as taught by Adesida, constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications)—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results.” Petition, 26-27 (citing *KSR* and Zhao ¶¶48-59, 133).

Even if it were a “simple design choice” to choose between an insulated gate electrode and a Schottky gate electrode when implementing a transistor (which Infineon does not concede), that is irrelevant to Usui. Usui’s alleged electrode (metal layers 13-15, 18-19) provides “connections or wirings between...devices” (Petition, 19) and overlies metal stud connection 10. Usui, 3:23-27; Piner, ¶¶184-186. Usui does not disclose a transistor, let alone a transistor gate electrode. Piner, ¶186; Zhao-Dep., 58:17-60:1. Additionally, Usui’s alleged electrode cannot make Schottky contact with “semiconductor wafer 6” because Usui’s alleged electrode is separated from the semiconductor by “insulator 8.” Usui, 3:23-28, 5:15; Piner, ¶186; Zhao, ¶58; Zhao-Dep., 123:19-124:3 (“...there are two types of commonly used gate structure, insulated gate *with* a insulating or dielectric layer, or Schottky gate *without* the insulating or dielectric layers”). Modifying Usui to have its alleged electrode somehow make Schottky contact with a transistor channel would have been the furthest thing from a “simple design choice” because Usui’s alleged

electrode is not a transistor gate electrode and it is separated from the semiconductor by insulator 8. Piner, ¶186; Zhao-Dep., 58:17-60:1.



Petitioner's Annotated Usui, Fig. 8

For similar reasons, Petitioner's assertion that its Usui-Yu-Adesida combination "combin[es] prior elements according to known techniques to a known device ready for improvement" (Petition, 26-27) fails. That *KSR* rationale only applies when elements are combined "with no change in their respective functions." *KSR*, 550 U.S. at 415-416. Petitioner's conclusory assertion that Usui was "ready for improvement" never even explains how Usui allegedly would have been improved by "implementing the Usui-Yu contact as a Schottky contact" (Petition, 26) despite Usui not disclosing a transistor gate electrode that could be improved by implementing it as a Schottky gate electrode. Piner, ¶¶187-188; Zhao-Dep., 58:17-60:1. Because the function of Usui's alleged electrode is dramatically changed in Petitioner's combination – from being an "interconnect metallurgy structure" that is part of an interconnect circuit connecting metal stud

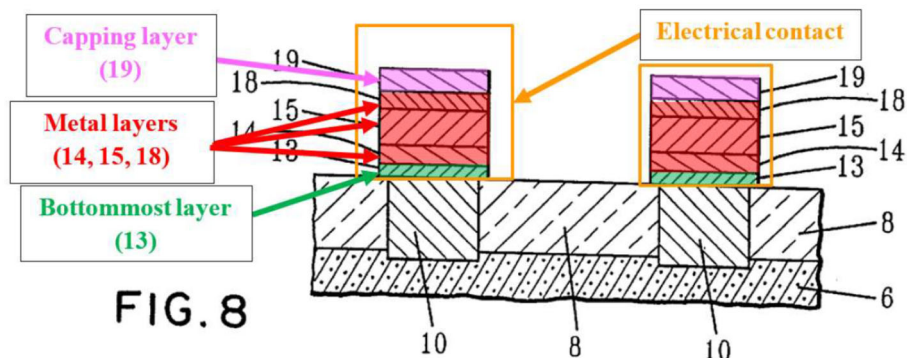
10 to another part of the circuit (Usui, 3:23-27, 4:10-15) while mitigating electromigration (Usui, 1:30-41, 2:33-39; *infra* §IV.D.2) to being a Schottky gate electrode that does not experience high current density and thus has no electromigration concerns (Piner, ¶189) – Petitioner’s invoked *KSR* rationale does not apply.

b. Petitioner Fails to Explain the Contemplated Workings of the Usui-Yu-Adesida Combination and How it Meets the Challenged Claims

Petitioner alleges “[i]t would have been obvious to implement the electrical contact of Usui-Yu in a device with a gate electrode making Schottky contact, as taught by Adesida.” Petition, 29. That is inconsistent with Petitioner’s explanation of what “the electrical contact of Usui-Yu” is (Petition, 29), because Petitioner’s “electrical contact of Usui-Yu” is a gate electrode with an insulating layer (Petition, 19-20). A gate electrode cannot have an insulating layer *and* make Schottky contact with the semiconductor device. Piner, ¶191; Zhao, ¶58; Zhao-Dep., 123:19-124:3.

Moreover, Petitioner never explains the contemplated workings of its Usui-Yu-Adesida combination and how Usui’s alleged electrode (layers 13-15, 18-19) *could* make Schottky contact with Usui’s “semiconductor wafer 6” when it is *separated therefrom by “insulator 8.”* Usui, 3:23-28, 5:15; Piner, ¶¶190-192; Zhao, ¶58; Zhao-Dep., 123:19-124:3. Explaining the contemplated workings of

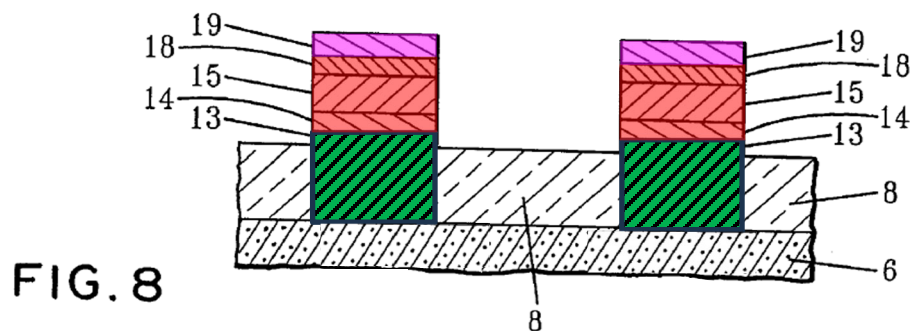
the combination is a “prerequisite” to establishing obviousness. *Personal Web*, 848 F.3d at 994. Petitioner’s failure to do so is fatal.



Petitioner’s Annotated Usui, Fig. 8

Petitioner’s failure to explain the contemplated workings of its Usui-Yu-Adesida combination and how its alleged electrode (Usui’s layers 13-15, 18-19) makes Schottky contact with Usui’s semiconductor 6 is significant. To the extent Petitioner suggests that Usui’s alleged “bottommost layer 13” would be made thicker to extend through insulator 8 and reach semiconductor 6, that would not meet any claim challenged in Ground 3 because it would not meet either independent claim (claim 1 or 13) from which the claims challenged in Ground 3 depend. Piner, ¶193; Zhao-Dep., 112:20-25 (confirming Ground 3 describes one “combination” allegedly “render[ing] claim 9, 11, 14, and 16 obvious”). Those independent claims require that the metal forming the top of the electrical contact have “a thickness greater than that of a bottommost layer of said plurality of metal layers” of the electrical contact (*see* Limitations [1c] and [13c]), which would not

be true if Usui's layer 13 had its thickness increased to extend through insulator 8 as shown in the figure below in which Infineon has modified Petitioner's annotated Usui Fig. 8 to show such a modification. Petitioner fails to even allege, let alone establish, that Usui-Yu-Adesida would meet Limitation [1c] or [13c] if Usui's alleged electrode (Usui's layers 13-15, 18-19) were modified to make Schottky contact with Usui's semiconductor 6.



Usui, Fig. 8 (Modified)

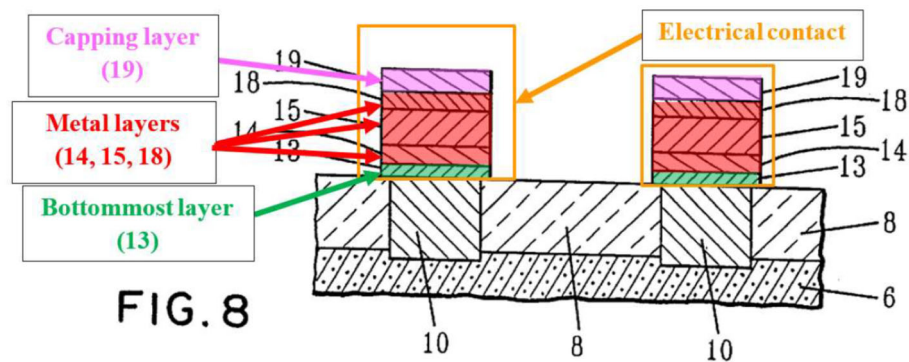
c. Petitioner Fails to Establish a Reasonable Expectation of Success

Ground 3 also fails because Petitioner fails to establish a reasonable expectation of success. *Eli Lilly*, 8 F.4th 1331 at 1344. Indeed, Petitioner's proposed modification would have rendered Usui inoperable for its intended purpose. *Gordon*, 733 F.2d at 902.

Usui's metal layers 13-15 and 18-19 – which Petitioner (mis)characterizes as an electrode – provide improved “electrical connections or wiring in electronic

devices.” Usui, 1:17-23, 2:23-35; Piner, ¶¶194-195; Petition, 19 (admitting same); Zhao-Dep., 13:9-11, 13:23-14:9.

Usui’s metal layers 13-15 and 18-19 are part of an “interconnect circuit” providing an electrical connection between interplanar stud 10 and a device Usui does not illustrate. Usui, 3:27, 4:10-15; Piner, ¶196; Zhao-Dep., 49:24-50:10. Modifying Usui to have its alleged electrode somehow make Schottky contact with semiconductor material 6 would have rendered Usui inoperable for its intended purpose of providing an “electrical connection[]” between metal stud 10 and another device, because Usui’s alleged electrode would no longer contact metal stud 10. Piner, ¶197.



Petitioner’s Annotated Usui, Fig. 8

Moreover, if Usui’s insulating layer 8 were eliminated so the alleged electrode were in direct contact with the semiconductor everywhere, that would render the device inoperable because it would short circuit every part of the semiconductor

device contacted by the metal layers (13-15 and 18-19) that form Usui’s alleged electrode. Piner, ¶198.

2. Claims 9 and 14

Claims 9 and 14 require that the electrical contact is configured for implementation on a “group III-V semiconductor device compris[ing] a high electron mobility transistor (HEMT).” Petitioner alleges “Usui discloses the importance of enhanced electromigration” and that a POSA was “motivated to implement” Usui-Yu’s electrical contact in group III-V semiconductor HEMT, as taught by Adesida, “because” this would have “enhanced electromigration.” Petition, 25. Petitioner misunderstands electromigration; Usui teaches that it should be mitigated – not “*enhanced*.” *Infra* §IV.D.2; Piner, ¶¶199-202. Petitioner’s alleged motivation for making the combination fails.

Petitioner’s “*simple design choice*” rationale fails because Petitioner ignores that Usui does not disclose a transistor and because there would have been substantial complexities in *changing the transistor type* from Yu’s transistor to a HEMT. Piner, ¶¶56-59, 203-204. Petitioner fails to establish there would have been no change to the functions of Usui-Yu’s metal layers. Piner, ¶205. That is fatal because Petitioner’s invoked *KSR* rationale only applies when prior art elements are combined “with no change in their respective functions.” *KSR*, 550 U.S. at 415-416.

D. Ground 4 Fails for Additional Reasons

Ground 4 alleges obviousness of claims 10 and 15 – which require that the electrical contact is “implemented as a power electrode making ohmic contact with said...semiconductor device” – over Usui, Yu, and Sugimoto (EX-1007).

Petitioner admits neither Usui nor Yu discloses a power electrode making ohmic contact but alleges “Sugimoto does.” Petition, 29; *see* Piner, ¶¶206-207, 123-129 (describing Sugimoto).

Ground 4 fails for numerous independent reasons detailed below.

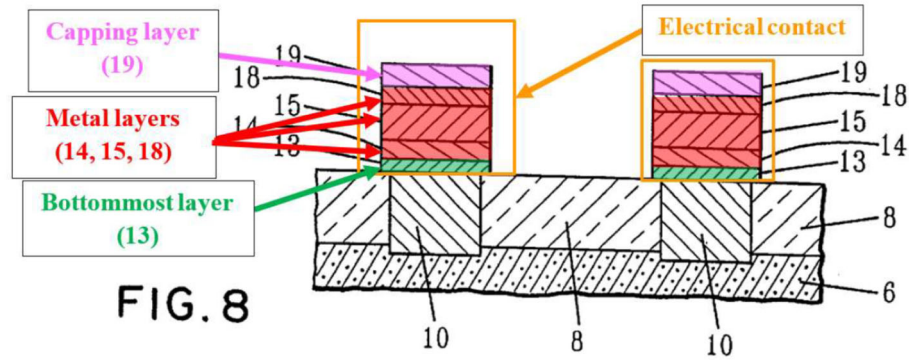
1. Petitioner Fails to Explain the Contemplated Workings of Ground 4’s Combination

The Petition neither explains the contemplated workings of its Usui-Yu-Sugimoto combination nor maps any claim to an explained combination. Doing so was a “prerequisite” to establishing obviousness. *Personal Web*, 848 F.3d at 994.

Petitioner’s assertion that a POSA would have used “the contact of Usui-Yu as a power electrode making ohmic contact” ignores that “the contact of Usui-Yu” is “implement[ed] ...with Yu’s gate insulating layer.” Petition, 20 (Ground 2 describing Usui-Yu). An insulating layer prevents ohmic contact. Piner, ¶¶209-210; Zhao, ¶56.

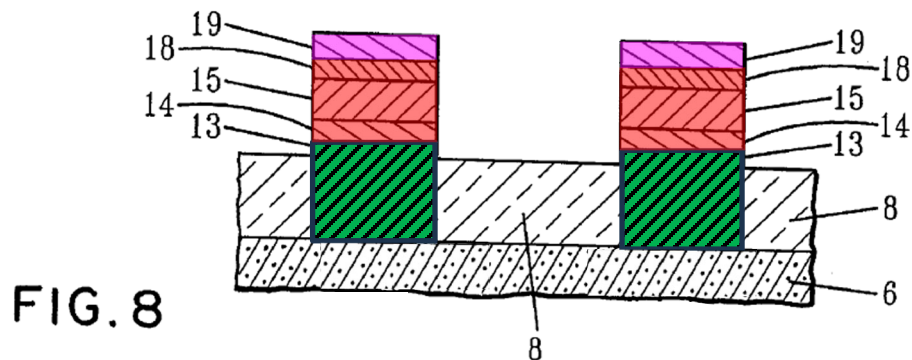
Even if “the electrical contact of Usui-Yu” is considered to not include Yu’s gate insulating layer, Petitioner never explains the contemplated workings of its Usui-Yu-Sugimoto combination, what Yu teachings are used in the combination,

nor how Usui's alleged electrode (layers 13-15, 18-19) could make ohmic contact with Usui's "semiconductor wafer 6" when it is *separated therefrom by "insulator 8."* Usui, 3:23-28, 5:15; Piner, ¶¶211-212; Zhao, ¶¶56-57.



Petitioner's Annotated Usui, Fig. 8

To the extent Petitioner suggests that Usui's bottommost layer 13 would be made thicker, as shown below, to extend through insulator 8 and reach semiconductor 6 to make ohmic contact, that would not meet any claim challenged in Ground 4 because it would not meet either independent claim (claim 1 or 13) from which those claims depend. Piner, ¶213.



Usui, Fig. 8 (Modified)

Claims 1 and 13 require that the capping layer have “a thickness greater than that of a bottommost layer of said plurality of metal layers” of the electrical contact. *See* Limitations [1c] and [13c]. Petitioner fails to explain what the thickness of the bottommost metal layer in Usui-Yu-Sugimoto’s alleged electrode stack is, let alone establish that the combination has a capping layer with a greater thickness than the bottommost metal layer as required by every Challenged Claim. *See* Limitations [1c] and [13c]; Piner, ¶¶213-214.

Petitioner’s failure to explain the “contemplated workings” of its Usui-Yu-Sugimoto combination, or how that combination meets any Challenged Claim, is fatal to Ground 4. *Personal Web*, 848 F.3d at 994.

2. Petitioner Fails to Establish Any Reason to Modify Usui Based on Yu and Sugimoto in the Claimed Manner

Petitioner alleges that Sugimoto discloses a group III-V semiconductor device “[l]ike Yu,” Sugimoto is analogous to the ’562 Patent, and that ohmic contacts were well-known, important components of a semiconductor device. Petition, 29-31. None of these assertions establishes any reason why a POSA would have modified Usui in the manner claimed.

Petitioner offers one conclusory paragraph purporting to establish some reason to combine Usui, Yu, and Sugimoto in a manner meeting claims 10 and 15. Petition, 31. Petitioner alleges a POSA “would have been motivated to implement the contact of Usui-Yu as a power electrode making an ohmic contact, as taught by

Sugimoto *because such a combination would provide improved current flow (i.e., enhanced electromigration)* and Sugimoto, like Yu, also teaches the use of III-V semiconductor devices.” *Id.* This assertion fails.

Petitioner badly misunderstands “electromigration.” Electromigration does not refer to “current flow” as Petitioner suggests via its parenthetical equating the terms. *Id.* Both experts agree that electromigration refers to electron-flow-induced movement of *metal atoms* in a conductor which can cause reliability and performance issues for the conductor. Piner, ¶¶215-218 (citing EX-2029, EX-2030, EX-2031), 66-67, 99-101; Zhao-Dep., 13:23-14:9, 53:18-54:25; Usui, 1:30-41 (“Migration of *aluminum atoms* into the underlying silicon can interfere with the performance and reliability of the resulting integrated circuit...”).

POSAs would not have sought “*enhanced* electromigration” as Petitioner alleges (Petition, 31) and would have instead sought “improvement in the electromigration characteristics” of “*electrical connections and wiring*” by *reducing* electromigration. Usui, 1:17-20, 2:33-39; Zhao-Dep., 13:23-14:9 (admitting electromigration was “improve[d]” by “*mitigat[ing]*” electromigration), 53:18-54:25 (“...it is very important to have this diffusion barrier layer” to “*prevent* the electromigration”); Piner, ¶219.

Usui does not teach “improved current flow” “i.e., enhanced electromigration” as Petitioner erroneously alleges (Petition, 31) – it teaches

improved electromigration characteristics which means *reduced* electromigration. Usui, 1:17-20, 2:33-39; Piner, ¶220; Zhao-Dep., 13:23-14:9, 53:18-54:25. It was well-known that electromigration was a concern for wiring of the type described by Usui. Piner, ¶¶220-221. Petitioner submits no evidence establishing that electromigration was a concern for a transistor power electrode, let alone that any electromigration concerns for a power electrode would be solved by applying Usui’s teachings used in wiring. *Id.*

Petitioner’s assertion that its Usui-Yu-Sugimoto combination “combin[es] prior elements according to known techniques to a known device ready for improvement” (Petition, 19) fails. As discussed *supra* §IV.B, that *KSR* rationale only applies when elements are combined without “change in their respective functions.” *KSR*, 550 U.S. at 415-416.

Petitioner never even explains what device in Ground 4’s combination was allegedly “ready for improvement.” Petitioner never establishes that Ground 4’s modification would have improved *Sugimoto* because Petitioner fails to establish that Sugimoto’s electrode suffers from electromigration that would be solved using Usui’s techniques. Piner, ¶222. And Petitioner never explains how *Usui* would have been improved by “implement[ing] the contact of Usui-Yu as a power electrode” (Petition, 31) given that Usui does not disclose any device having a power electrode. Piner, ¶223. Petitioner’s combination does not “improve” Usui –

it *changes* the function of Usui's metal layer stack to serve as a power electrode rather than as wiring that is part of an "interconnect circuit" connecting devices in a semiconductor circuit. *Id.*; Usui, 1:5-12, 4:10-15. Because the functions of the components are changed in Petitioner's combination, the *KSR* rationale Petitioner invokes does not apply.

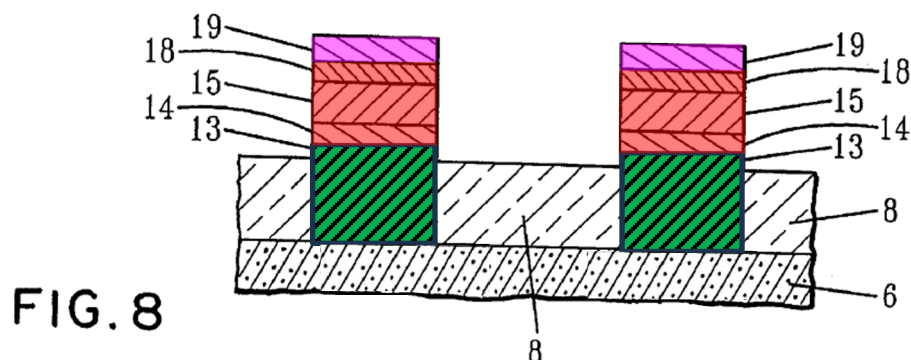
The Petition's sole alleged motivation for the combination ("improved current flow (i.e., enhanced electromigration)") is unsupported and based on a fundamental misunderstanding of Usui's teachings about electromigration. *KSR* cannot save Petitioner because the invoked *KSR* rationale does not apply.

Petitioner's failure to establish any supportable, non-hindsight reason to combine the references in the manner claimed is fatal to Ground 4. *Supra* §IV.B (citing authority).

3. Petitioner Fails to Establish a Reasonable Expectation of Success

For the same reasons discussed *supra* §IV.D.1, Petitioner fails to establish a reasonable expectation of success in modifying Usui, based on Yu and Sugimoto, so that Usui's alleged electrode (layers 13-15 and 18-19) has a capping layer with "a thickness greater than that of a bottommost layer of said plurality of metal layers" of the electrical contact, as required by Limitations [1c] and [13c], despite Usui's alleged bottommost layer 13 being modified to somehow make ohmic

contact with Usui's semiconductor 6 as required to meet claims 10 and 15. Piner, ¶¶224-225.



Usui, Fig. 8 (Modified)

To the extent Petitioner suggests that Usui-Yu's alleged electrical contact could be used unchanged to form an ohmic contact, no evidence supports that. POSAs understood this would require significant changes to the layers – in their materials and thicknesses – because ohmic contacts are closely tailored to the semiconductor, like a lock and key. Piner, ¶¶226-228, 48-57. Petitioner fails to account for these changes, and fails to show that the alleged electrical contact of Usui-Yu-Sugimoto would meet claims 1 and 13 after making the necessary changes. Piner, ¶227.

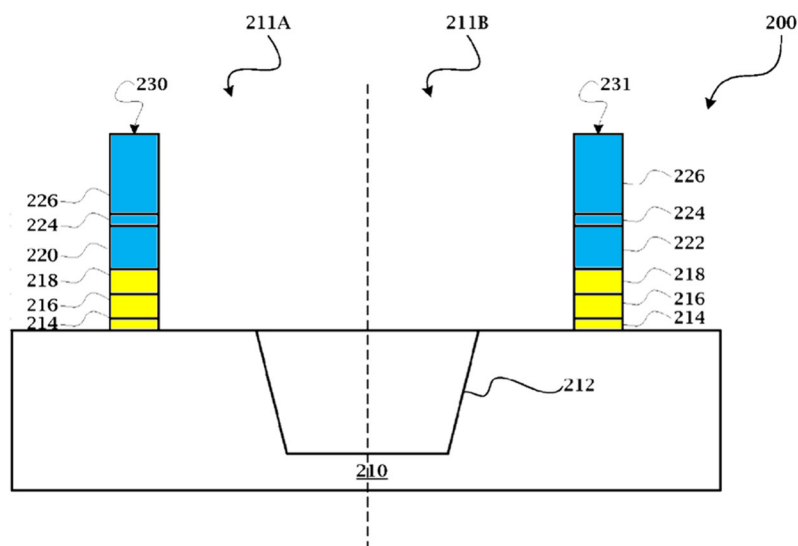
V. GROUND 5 (OBVIOUSNESS OVER YU AND USUI) FAILS

The Board did not address “this ground in full” at institution, but found “merit” to Infineon's argument that Ground 5 fails because Petitioner failed to establish that the Yu-based grounds meet the claimed capping layer that consists

only of a refractory metal nitride *and* is thicker than a bottommost layer of said plurality of metal layers of the electrode stack. DI, 15 and 18-19 (finding that the allegedly-supporting testimony of Petitioner’s expert warranted no weight because it merely parroted the Petition’s conclusory assertions). The Board should reach the same conclusion at Final Written Decision. The Yu-based grounds also fail for additional reasons detailed below.

A. Yu Overview

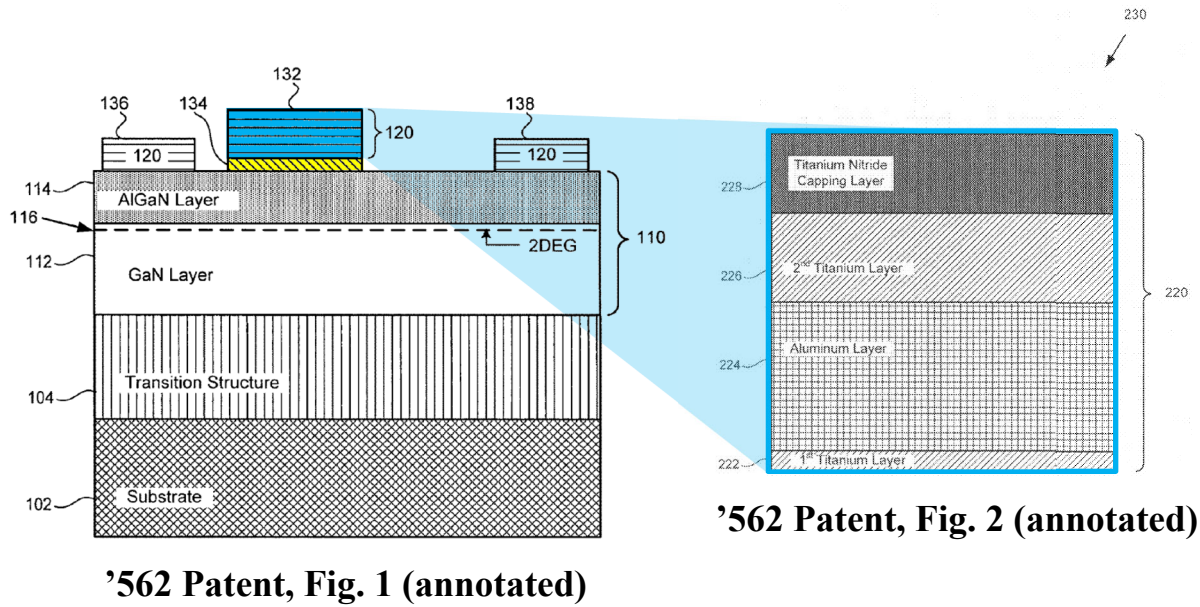
Yu is directed to a particular technique for forming a metal gate electrode for a CMOS device. Piner, ¶¶106-114, 229-233. Yu was motivated by “a desire to replace the gate oxide and *polysilicon gate electrode* [in conventional CMOS devices] with a high-k gate dielectric and *metal gate electrode* to improve device performance as feature sizes continue to decrease.” Yu, [0004]. Yu needed to address issues associated with “metal, metal carbide, and/or metal nitride...gate electrode...materials [that] provide insufficient work function values and present thermal stability issues...” *Id.* Yu addresses those problems by providing a CMOS device whose two transistors have metal gate electrodes formed from different metal layers. A first gate electrode includes “first metal layer 220 compris[ing] a material with a first work function” and the second gate electrode includes “second metal layer 222 compris[ing] a material with a second work function.” Yu, [0030]; *see also* Yu, Fig. 2E (annotated below), [0033].



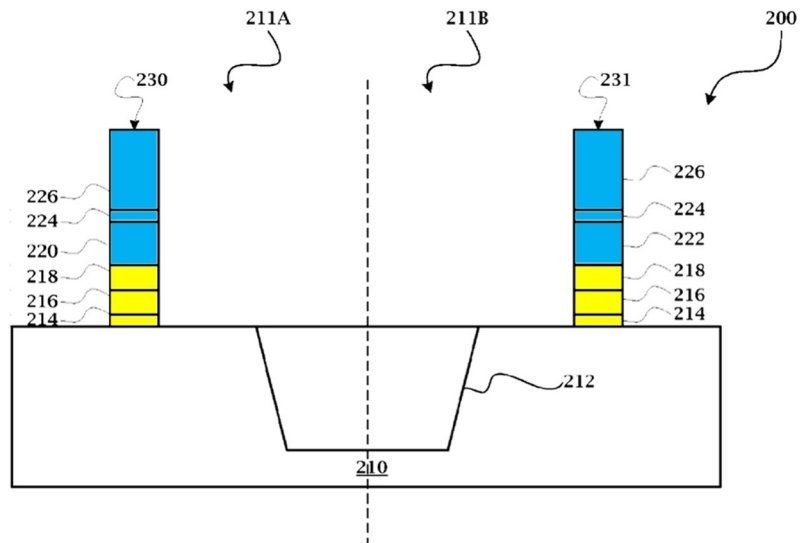
Yu, Fig. 2E (annotated)

Yu provided “different work functions” for the two CMOS gate electrodes by providing different work functions for metal layers 220 and 222. Yu, [0004], [0030], [0033].

Yu’s electrodes are insulated gate electrodes. As discussed *supra* §II.A, the ’562 Patent discloses an insulated gate electrode in which gate electrode 132 (blue) is stacked with insulating layer 134 (yellow) as shown in Fig. 1 (below left). EX-1001, 2:58-60 (“gate electrode 132”), 3:19-35 (same). The electrode stack in Fig. 2 (below right) forms “gate electrode 132, in Fig. 1.” *Id.*, 3:40-43 (Fig 2’s “[e]lectrode stack 220” “corresponds to electrode stack 120 in FIG. 1”). Thus, the ’562 Patent is clear that the “electrode stack” for a gate electrode includes only the metal layers forming the electrode and not other layers like insulating layer 134 that are stacked with, but are not part of, the gate electrode.



Like the '562 Patent's insulated gate electrode (blue above) is stacked with another layer (yellow above), Yu's gate electrodes (blue below) are stacked with other layers (yellow below).

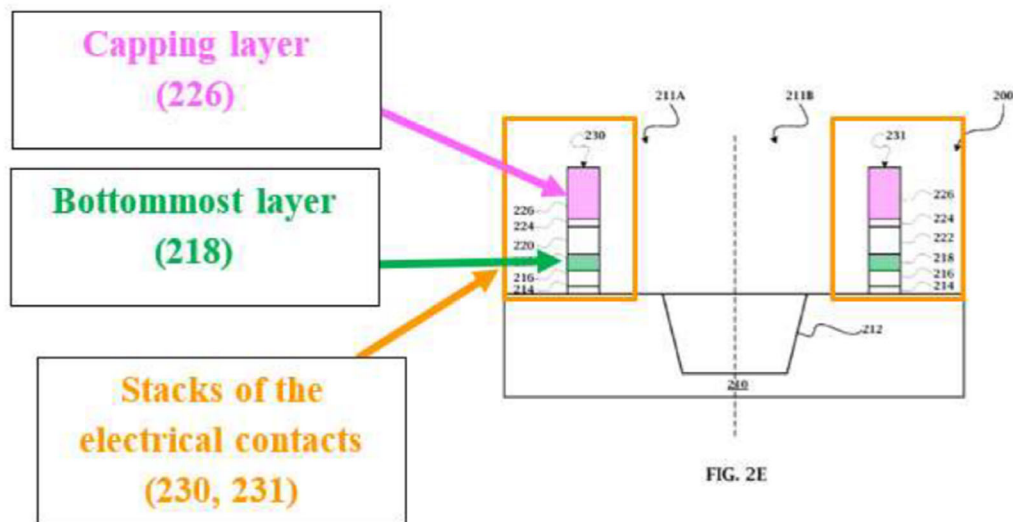


Yu calls the entire stack a “metal gate stack.” Yu, [0038]-[0039]. Metal gate stacks 230 and 231 have different metal layers (220 and 222, respectively) with different work functions, but their structures are otherwise identical. Each stack includes two oxide layers 214, 216 (yellow above) atop the semiconductor (Yu, [0028]-[0030]), a “diffusion barrier layer” 218 separating the metal layer (220 or 222, blue above) from the oxide layers to prevent material from diffusing between the metal and oxide layers (Yu, [0029]), a capping layer 226 (Yu, [0036]), and a diffusion barrier layer 224 separating the capping layer from the metal layer (220 and 222) to prevent diffusion (Yu, [0035]).

B. Petitioner Fails to Establish that Yu’s Diffusion Barrier/Protection Layer 218 is a Layer of Yu’s Electrode Stack

Every Challenged Claim recites an electrical contact comprising “an electrode stack including a plurality of metal layers and a capping layer,” where the capping layer is thicker than “a *bottommost layer*” of the “plurality of metal layers” of the electrode stack. Limitations [1pre]-[1c] and [13pre]-[13c].

Petitioner alleges Yu’s layer 218 meets the claimed “bottommost layer.” Petition, 35-37, 43-46.



Petitioner's Annotated Yu, Fig. 2E

Layer 218 is an “optional” “diffusion barrier/protection layer” that “may be omitted.” Yu, [0029]; Petition, 43; Piner, ¶¶234-235.

Diffusion barrier layers were well-known. Piner, ¶¶236-237; *see also id.*, ¶¶72-75. They are disposed between two layers of material to prevent the separated materials from diffusing into each other. EX-2002, [0057]-[0058], Fig. 6. Diffusion barrier layers had been used to separate a gate electrode from an oxide layer, like Yu’s layer 218 does. *Id.* Yu’s barrier layer is not part of the gate electrode; it separates the gate electrode from the oxide layer. *Id.*; Piner, ¶237.

1. Petitioner Fails to Construe “Electrode Stack”

Petitioner alleges in conclusory fashion that Yu’s entire “metal gate stack” (230 or 231) is an “electrode stack” as claimed. Petition, 42. The Petition never explains the “plain meaning” of “electrode stack.” Petition, 7; Zhao-Dep., 172:20-

175:5; Piner, ¶238. That fails to carry Petitioner’s burden (“*must*”) to identify “how the challenged claim is to be construed” and “[h]ow the *construed* claim is unpatentable.” 37 C.F.R. § 42.104(b)(3)-(4). That is reason enough why Ground 5 fails.

2. No Evidence Supports Petitioner’s Assertion that Yu’s Entire Metal Gate Stack is an Electrode Stack

The Petition cites no intrinsic or extrinsic *evidence* supporting Petitioner’s conclusory assertion that Yu’s *entire* metal gate stack (230 or 231) is an electrode stack. Petition, 42.

Petitioner alleges that oxide layers 214 and 216 at the bottom of Yu’s metal gate stacks 230 and 231 cannot be the claimed “bottommost layer of said plurality of metal layers” because they are not metal (Petition, 44-45) and that Yu’s diffusion barrier/protection layer 218 can be metal (Petition, 42). Even if accepted as true, those assertions do not establish that Yu’s diffusion barrier/protection layer 218 is a layer of Yu’s *electrode stack*.

Limitation [1c] recites “a bottommost layer of said plurality of metal layers.” The antecedent for “*said* plurality of metal layers” is in Limitation [1a], which recites “an *electrode stack* including a plurality of metal layers.” Thus, to meet Limitation [1c], Petitioner needed to identify a “bottommost layer of said plurality

of metal layers” in Yu’s “*electrode stack*.” See Limitations [1a] and [1c].¹²

Petitioner makes no such showing.

Petitioner alleges Yu’s diffusion barrier/protection layer is the “*bottommost layer of plurality of metal layers*” in Yu’s metal gate stacks 230 and 231. Petition, 43-44. Petitioner parenthetically equates Yu’s *entire* metal gate stack (230 or 231) with the claimed “electrode stack.” Petition, 42 (“Yu discloses [1a] because it discloses **metal gate stacks 230, 231 (electrode stacks)**”) (coloring original). The Petition provides *no* explanation – let alone the required “detailed explanation” – of how or why the cited evidence purportedly establishes that Yu’s *entire* gate metal stack is an electrode stack as claimed. 37 C.F.R. § 42.22(a)(2).

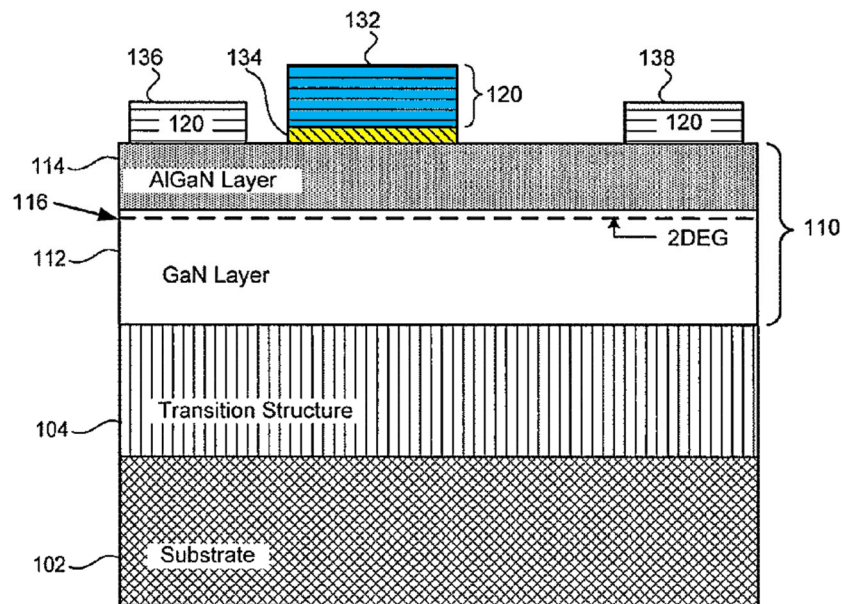
No evidence supports Petitioner’s conclusory assertion that Yu’s entire metal gate stack is an electrode stack. Piner, ¶¶239-241. For Limitation [1a], the Petition cites Yu, [0029] and [0035]-[0036]. Petition, 42. None of those paragraphs characterizes Yu’s entire metal gate stack as an electrode stack. The only other evidence Petitioner cites is “Zhao ¶162” (Petition, 42) in which Dr. Zhao parrots the Petition’s Limitation [1a] argument *word-for-word*. This conclusory testimony is devoid of analysis or evidence supporting Petitioner’s

¹² Ground 5 relies on Petitioner’s showing for Limitation [1c] to meet Limitation [13c]. Petition, 55.

assertion that Yu's *entire* metal gate stack is an "electrode stack," so it warrants no weight. *Xerox*, IPR2022-00624, Paper 9, 15; DI, 18-19 (finding other similarly-unsupported Dr. Zhao testimony to warrant no weight).

3. Petitioner's Assertion that Yu's Entire Metal Gate Stack is an "Electrode Stack" is Refuted by the Intrinsic Evidence

The '562 Patent discloses a metal gate stack sharing similarities with Yu's metal gate stack. *See* '562 Patent Fig. 1 and Yu Fig. 2E (both annotated below). Both stacks include a gate electrode (blue) and other layer(s) (yellow).



'562 Patent, Fig. 1 (annotated)

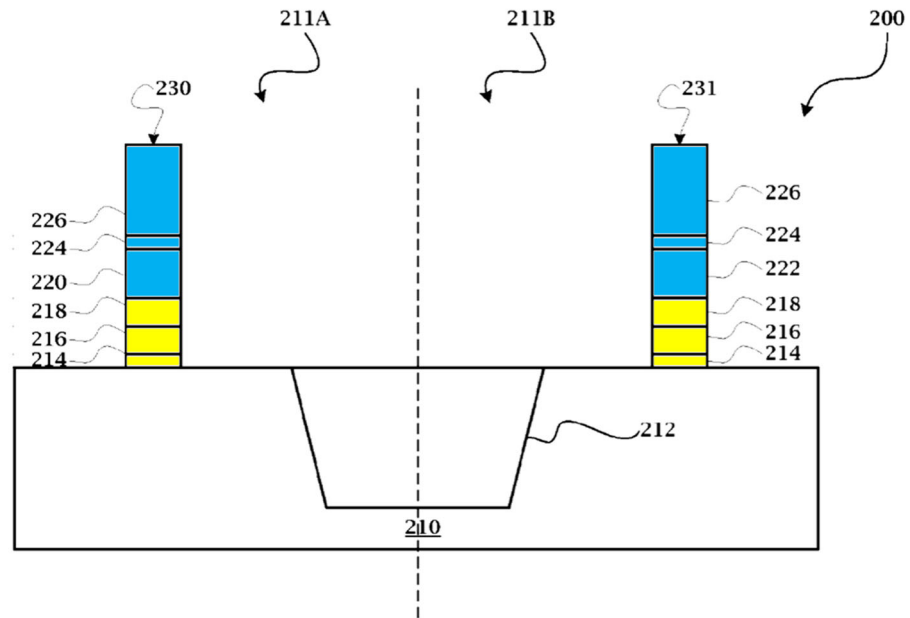
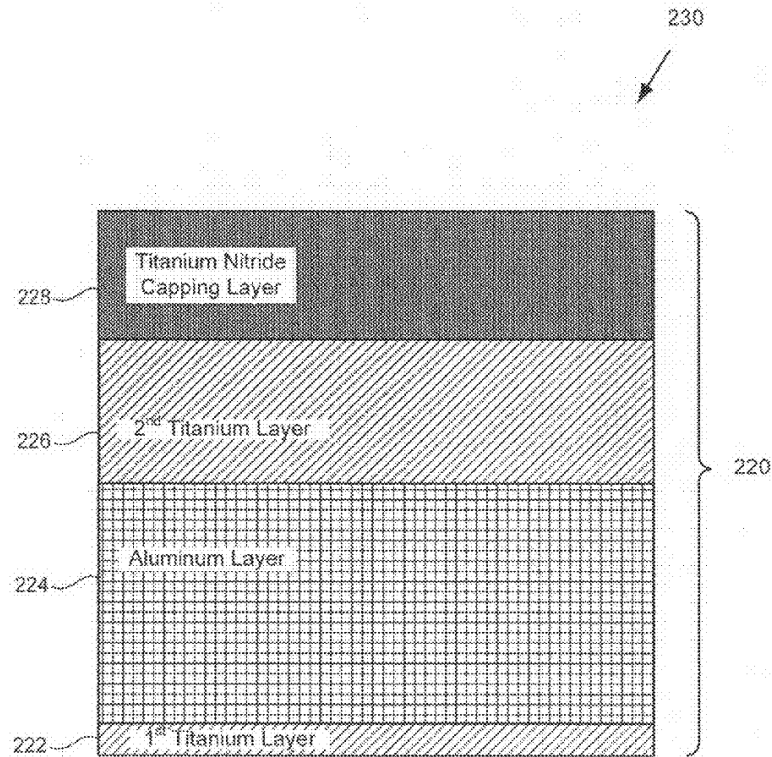


FIG. 2E

Yu, Fig. 2E (annotated)

The '562 Patent explains that Fig. 1 illustrates “gate electrode 132” stacked with “gate insulating layer 134.” EX-1001, 3:28-31. The '562 Patent is explicit that the “electrode stack 120” for this gate electrode does *not* include gate insulating layer 134. *Id.* Fig. 1’s labelling of “electrode stack 120” makes clear that the electrode stack is comprised of the stacked metal layers forming the gate electrode 132 and does *not* include gate insulating layer 134. Indeed, the same “electrode stack 120” is used for source and drain electrodes 136 and 138, which have no insulating layer 134. *Id.*, 3:23-25, Fig. 1. Gate insulating layer 134 “underl[ies] the electrode stack 120” rather than being part of the electrode stack.

Id., 3:28-31. Furthermore, Fig. 2’s “[e]lectrode stack 220” “corresponds to electrode stack 120 in FIG. 1” (*id.*, 3:42-43) and does not include an insulating layer. *Id.*, Fig. 2 (reproduced below), 3:40-43 (Fig. 2’s “[e]lectrical contact 230 may...correspond to...[the] **insulated gate electrode** 132 in Fig. 1”).



'562 Patent, Fig. 2

Thus, the '562 Patent specification is clear that the “electrode stack” includes only stacked layers that form the electrode; if the electrode is stacked with other layers, those other layers are not part of the electrode stack. Piner, ¶¶242-244; *Phillips*, 415 F.3d at 1315 (“[T]he specification ‘is... the single best guide to the meaning of a disputed term.’”).

The above-identified intrinsic evidence – ignored by Petitioner – directly refutes Petitioner’s conclusory assertion that Yu’s entire metal gate stack is an “electrode stack.” Petition, 42. Yu’s entire metal gate stack (230 or 231) cannot be an “electrode stack” as claimed because it includes a dielectric layer (214 or 216) that performs the same insulating function as insulating layer 134 in the ’562 Patent.¹³ Yu, [0022], [0027]-[0028], [0039]. The intrinsic evidence makes clear that such an oxide layer is not part of the claimed “electrode stack.” Thus, Petitioner’s conclusory assertion that Yu’s entire metal gate stack 230 or 231 is an “electrode stack” is wrong.

4. Petitioner’s Failure to Correctly Identify an “Electrode Stack” in Yu is Fatal to Ground 5

Limitations [1c] and [13c] require that the capping layer have “a thickness greater than that of a bottommost layer of *said* plurality of metal layers” that are included in the “electrode stack” per Limitations [1a] and [13a].

The *only* argument Petitioner advances to purportedly meet Limitations [1c] and [13c] is that each of Yu’s *entire* metal gate stacks 230, 231 is an electrode

¹³ The ’562 Patent’s gate insulating layer 134 can be silicon dioxide (SiO₂) (EX-1001, 3:28-31) which is a “silicon oxide,” the material referenced in Yu for dielectric layer 214. Yu, [0027]; EX-2003, [0130]; EX-2004, 225-230; Piner, ¶244.

stack, diffusion barrier/protection layer 218 is the bottommost metal layer of that alleged electrode stack, and capping layer 226 is purportedly thicker than diffusion barrier/protection layer 218. Petition, 43-46. But Petitioner fails to establish that Yu's diffusion barrier/protection layer 218 is even among the layers of Yu's "electrode stack," let alone its bottommost metal layer. *Supra* §§V.B.2-V.B.3; Piner, ¶245. Thus, Ground 5 fails for all Challenged Claims because Petitioner fails to establish that Yu's capping layer has "a thickness greater than that of a bottommost layer of *said* plurality of metal layers" included in the "electrode stack." Limitations [1a]-[1c] and [13a]-[13c].

C. As the Board Already Found, Petitioner Fails to Show that Yu and Usui Render Obvious an Electrical Contact with a Capping Layer of a Refractory Metal Nitride that is Thicker Than Yu's Alleged Bottommost Layer

Every Challenged Claim requires a capping layer that is *both* (1) formed from a "refractory metal nitride" or from TiN or TaN¹⁴ and (2) thicker than the electrode stack's bottommost metal layer. Petitioner fails to establish that Yu and Usui render obvious a capping layer meeting both requirements.

Yu discloses various materials for forming its capping layer. Petitioner admits Yu does not "expressly disclose[]" that capping layer 226 is thicker than the alleged bottommost metal layer (layer 218) when capping layer 226 is formed from

¹⁴ Limitations [1b] and [13b].

a material meeting any Challenged Claim. Petition, 38 (“Yu expressly discloses every element of claims 1 and 13 except a *refractory metal nitride capping layer* having a thickness greater than that of a bottommost layer (claim element [1c]).”).

Petitioner points to Yu’s thickness for the capping layer when formed from polysilicon, which Petitioner concedes is “*not* a refractory metal nitride as is stated in claims 1 and 13.” Petition, 38. Petitioner then alleges that the Challenged Claims are rendered obvious for two alternative reasons: (1) a POSA would have been motivated to make Yu’s capping layer the same thickness when formed from a refractory metal nitride as when formed from polysilicon, and (2) Usui would have motivated a POSA to make Yu’s refractory metal nitride capping layer thicker than Yu’s diffusion barrier/protection layer 218. Petition, 38-39. As detailed below, neither assertion is supported by the evidence. Piner, ¶¶246-249.

1. Yu Does Not Disclose a Refractory Metal Nitride Capping Layer Thicker Than Yu’s Alleged Bottommost Layer 218

Yu describes many materials or “combinations thereof” that could form capping layer 226. Yu, [0036]. The Petition seizes on Yu’s disclosure that capping layer 226 can be titanium nitride or tantalum nitride because those are refractory metal nitrides. Petition, 42. But Yu *never* discloses capping layer 226’s thickness when formed from those materials; Petitioner never alleges otherwise.

Petitioner states that “[w]hile Yu discloses the *capping layer* is *preferably* 600Å and the *bottommost layer* 20Å (i.e., the *capping layer* is *preferably* thicker

than the **bottommost layer**), this disclosure is made with respect to the **capping layer** being polysilicon (Yu, [0036], [0040]), which is not a **refractory metal nitride** as is stated in claims 1 and 13.” Petition, 38 (emphasis original). The 600Å thickness is the only capping layer thickness Petitioner cites and it is for polysilicon,¹⁵ which Petitioner admits does not meet any Challenged Claim. *Id.*; Yu, [0036]; Piner, ¶¶250-251.

2. As the Board Already Found, Petitioner’s Assertion that a POSA Would Have Used the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Capping Layer is Unsupported

Petitioner alleges a POSA would have “replace[d] Yu’s polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed thicknesses because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation.” Petition, 38 (highlighting added). Petitioner makes two distinct assertions, highlighted yellow and blue.

Infineon does not dispute Petitioner’s assertion (highlighted yellow) that a POSA had reason to use titanium nitride or tantalum nitride for Yu’s capping layer, nor that these refractory metal nitrides had known benefits, as Yu discloses that these materials can be used for capping layer 226. Yu, [0036].

¹⁵ Yu discloses a different thickness (about 50-1,000 Å and “preferably about 200 Å”) when capping layer 226 is an “aluminum-based, tungsten, or copper material.”

But *as the Board already found*, Petitioner’s separate assertion (highlighted blue) that a POSA would have been motivated to “us[e] the same disclosed thickness” that Yu teaches for a polysilicon capping layer when making the capping layer from a refractory metal nitride is entirely unsupported. Petition, 38; DI, 18-19; Piner, ¶¶252-253.

a. Petitioner Alleges No Reason to Choose the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Capping Layer

Establishing obviousness requires a supportable, evidence-based *reason why* a POSA would have combined prior art teachings in the art in the manner claimed. *KSR*, 550 U.S. at 418; *TQ Delta*, 942 F.3d at 1359 (reversing obviousness determination: “‘a conclusory assertion with no explanation is inadequate to support a finding that there would have been a motivation to combine’ because ‘[t]his type of finding, without more, tracks the *ex post* reasoning *KSR* warned of and fails to identify any actual *reason why* a skilled artisan would have combined the elements in the manner claimed.’”) (internal citation omitted).

The only reason Petitioner alleges a POSA would have “been motivated to replace Yu’s polysilicon with either its disclosed titanium nitride or tantalum nitride” is highlighted yellow above. Petition, 38 (“because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation [*sic*] as explained by Dr. Zhao,” citing Zhao ¶¶71-73, 155).

Petitioner does not even allege, let alone establish with evidence, any reason why a POSA would have chosen the “same...thickness[]” that Yu discloses for its polysilicon capping layer when the capping layer is instead formed from a refractory metal nitride. Petition, 38. Dr. Zhao also never alleges, let alone establishes, any reason to use the same thickness Yu discloses for a polysilicon capping layer when the capping layer is formed from a refractory metal nitride. In §V.C.2.b below, Infineon walks through the cited paragraphs from Dr. Zhao. Most say nothing about any layer “thickness.” Only Zhao ¶155 mentions thickness. But as the Board found, it “mirrors the statements in the Petition without providing technical explanation or additional evidence in support thereof so it warrants no weight.” DI, 19 (*citing Xerox*). Like the Petition, Dr. Zhao never alleges any ***reason why*** a POSA would have used the “same...thickness[]” that Yu discloses for its polysilicon capping layer when the capping layer is instead formed from a refractory metal nitride.

Petitioner’s failure to provide a supportable reason why a POSA would have chosen the “same...thickness[]” that Yu discloses for its polysilicon capping layer when the capping layer is formed from a different material – a refractory metal nitride (Petition, 38) – is egregious given that Yu discloses that the capping layer material significantly impacts the capping layer’s thickness. Yu, [0036]; Piner, ¶¶254-256. When the capping layer is formed from other materials (“aluminum-

based, tungsten, or copper material”), Yu discloses a very different “prefer[red]” thickness of “about 200 Å” – less than *one-third* the preferred thickness (600Å) for a polysilicon capping layer. Yu. [0036].

Petitioner’s failure to allege any reason to choose the “*same*...thickness[]” that Yu discloses for its polysilicon capping layer when the capping layer is formed from a refractory metal nitride is fatal to Petitioner’s assertion that Yu alone suggests to a POSA the use of a capping layer of a refractory metal nitride thicker than Yu’s alleged bottommost layer 218 (Petition, 38). *KSR*, 550 U.S. at 418; *TQ Delta*, 942 F.3d at 1359 (a “reason” is required); DI, 18-19.

b. No Evidence Supports Petitioner’s Assertion that a POSA Would Have Chosen the Same Thickness for a Refractory Metal Nitride Capping Layer as for a Polysilicon Capping Layer

Petitioner’s assertion that a “POSITA would have been motivated to replace Yu’s polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed thicknesses” cites “Zhao ¶¶71-73, 155.” Petition, 38 (highlighting added). None of these cited paragraphs supports the assertion (blue above) that a POSA would have used Yu’s same thickness for a polysilicon capping layer when the layer is instead formed from a refractory metal nitride. Piner, ¶¶257-260 (discussing EX-1023; EX-1024; EX-1025; EX-1026; EX-1028; EX-1029).

Zhao ¶¶71-73 never refer to thickness of a refractor metal nitride capping layer and Zhao ¶155 does nothing but parrot the argument in the first paragraph on page 38 of the Petition *word-for-word*. Compare Petition, 38 with Zhao ¶155. As the Board already found, Dr. Zhao’s naked conclusory assertion that a POSA would have used the “same...thickness[]” for a refractory metal nitride capping layer that Yu teaches is preferred for *polysilicon* capping layer warrants no weight. DI, 18-19; *Xerox*, IPR2022-00624, Paper 9, 15.

Moreover, just like the Petition, Zhao ¶155 never explains any *reason why* a POSA would have chosen Yu’s disclosed thickness for a polysilicon capping layer when using a refractory metal nitride capping layer despite Yu’s disclosure of different thicknesses for the capping layer when formed from different materials. Yu, [0036]; *supra* §V.C.2.a (Yu’s preferred thickness for the capping layer when formed from other materials is less than *one-third* of that for a polysilicon capping layer).

The Petition cites no credible *evidence* supporting its assertion that a POSA would have chosen the “same...thickness[]” that Yu discloses for its polysilicon capping layer when the capping layer is formed from a refractory metal nitride. Petition, 38. That is fatal to Ground 5.

**c. Petitioner Does Not Identify the Thickness of Yu’s
Diffusion Barrier/Protection Layer 218 When Made
of Titanium as Alleged in the Yu-USui Combination**

Petitioner alleges that the thickness of Yu’s diffusion barrier/protection layer 218 is 20Å. Petition, 38. The 20Å thickness Yu teaches is for a diffusion barrier/protection layer 218 formed from titanium *nitride* (TiN). Yu, [0029]. But Petitioner’s Yu-USui combination does *not* use a *TiN* diffusion barrier/protection layer 218. Instead, Petitioner alleges a “POSITA would have been motivated to use *titanium* as **diffusion barrier/protection layer 218**...in Yu’s device.” Petition, 36. Titanium nitride and titanium are different materials. Piner, ¶¶261-263.

Petitioner cites no teaching in Yu of a thickness for a *titanium* diffusion barrier/protection layer 218 as in Petitioner’s Yu-USui combination. Petition, 36. The only thickness Petitioner cites is 20Å for a TiN “embodiment.” Yu, [0029]. Yu never says this thickness applies for the diffusion barrier/protection layer 218 for all materials. Instead, Yu says that “in alternate embodiments, the diffusion barrier layer 218 comprises any suitable thickness.” Yu, [0029]. Yu provides no teaching of a “suitable thickness” for the *titanium* diffusion barrier/protection layer 218 used in Petitioner’s Yu-USui combination. Petition, 36.

* * *

Petitioner’s assertion that Yu teaches a capping layer 226 that is thicker than its diffusion barrier/protection layer 218 is thus based on thickness values that Yu reports for *different materials for both layers* than are used in Petitioner’s Yu-Usui combination. Yu teaches nothing about the thickness of these layers when formed from the materials in Petitioner’s Yu-Usui combination. Yu simply does not teach a refractory metal nitride capping layer 226 that is thicker than a titanium diffusion barrier layer 218 as Petitioner alleges. Piner, ¶264.

3. As the Board Already Found, Petitioner’s Alternative Argument that Usui Would Have Motivated a POSA to Make Yu’s Refractory Metal Nitride Capping Layer Thicker Than Yu’s Diffusion Barrier/Protection Layer Also Fails

Petitioner alternatively argues that “[t]o the extent Yu does not expressly disclose a **refractory metal nitride capping layer** having a thickness greater than that of a **bottommost layer**, Usui does.” Petition, 38-39 (citing Usui’s statement, at 3:29-37, about “limiting the thickness of...underlayer 13”). The Board already rejected this argument (DI, 19) for good reason. Petitioner’s assertion fails as detailed below.

a. A Capping Layer Thicker than the Bottommost Layer of the Electrode Stack’s Metal Layers is a Missing Limitation Not Taught by Yu or Usui

Petitioner’s assertion that Usui’s underlayer 13 is the bottommost metal layer of an *electrode stack* fails because Petitioner fails to establish that Usui’s interconnect

metallization structure (Usui layers 13-15 and 18-19) is an electrode stack. *Supra* §III (Ground 1). Thus, neither Yu nor Usui teaches an electrode stack having a capping layer thicker than the bottommost layer of the electrode stack's metal layers. This is a limitation of every Challenged Claim. *See* Limitations [1a]-[1c] and [13a]-13[c]. The Petition fails to identify where this "element...is found in the prior art patents or printed publications relied upon" which is a requirement ("must") in 37 C.F.R. § 42.104(b)(4). Petitioner does not rely on applicant admitted prior art (AAPA) so there is no justification for waiving Rule 104(b)(4) even for this Petition filed before September 1, 2025 (EX-2034).

Moreover, the Federal Circuit has repeatedly held that for "common sense" or expert testimony alone to supply a claim limitation missing from the prior art, "the limitation in question [must be] unusually simple and the technology particularly straightforward." *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016); *see also DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1374 (Fed. Cir. 2018). That is not the case here. *Piner*, ¶¶265-267, 47-61, 69-71; *see also* EX-1008; EX-1011; EX-1012; EX-1013; EX-1015; EX-1016; EX-1017; EX-1020; EX-1021. Petitioner does not even attempt to establish that its reliance on expert testimony to supply the thickness limitation missing from Petitioner's prior art references (Yu and Usui) is consistent with Federal Circuit precedent. It is not. *Piner*, ¶267. Petitioner's

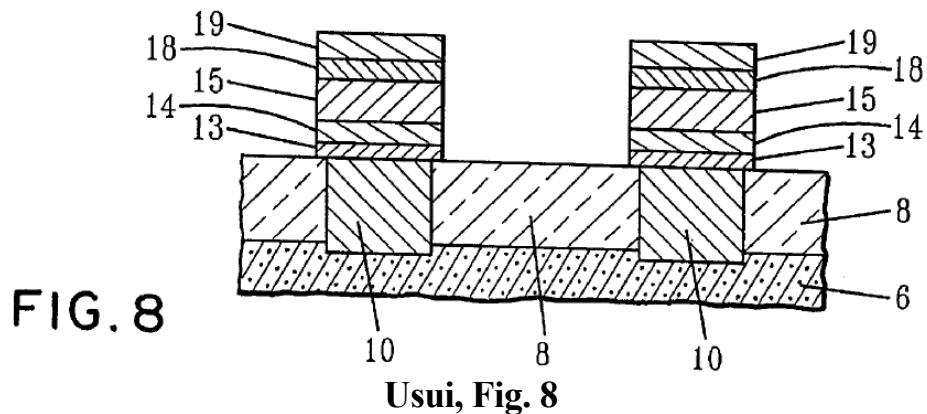
attempt to meet a missing claim limitation with expert testimony alone is another reason why Ground 5 fails.

b. Usui's Interconnect Metallurgy Structure Would Not Have Motivated Any Change to Yu's CMOS Gate Electrode

Petitioner cites Usui's teaching that "limiting the thickness of...underlayer 13...is essential in achieving the necessary properties of the *structure of the present invention*." Petition, 38-39 (quoting Usui, 3:29-37). Usui's "present invention" is "an interconnect metallurgy structure" to form an "interconnect circuit" for semiconductor devices. Usui, 3:23-27, 4:10-15; Piner, ¶268.

Yu has nothing to do with "interconnect metallurgy structure[s]." Yu is directed to gate electrodes for a CMOS device. Yu, Title, [0004]-[0005], [0021]. Petitioner fails to establish that Usui's teachings about how to improve interconnect metallurgy structures would have motivated a POSA to make any change to Yu's CMOS gate electrodes. Piner, ¶269.

Petitioner relies on Usui's "underlayer 13." Petition, 38-39. Underlayer 13 is the bottom layer of Usui's interconnect metallurgy structure and is "deposited" on "planar insulator 8 and contact stud 10." Usui, 5:11-14, Fig. 8 (below).



“[B]y limiting the thickness of...underlayer 13, the structure and texture of” the interconnect metallurgy structure “is carefully controlled” to help limit electromigration. Usui, 3:29-37, 2:33-39; Petition, 38-39; Piner, ¶¶270-271.

Petitioner alleges that the claimed bottommost layer in Yu-Usui is met by Yu’s diffusion barrier/protection layer 218. Petition, 39. Yu’s layer 218 is *not* deposited on a contact stud and is *not* the underlayer of Yu’s metal gate stack 230 or 231. Piner, ¶272. Instead, the underlayer of Yu’s metal gate stack is dielectric layer 214 “formed over the substrate 210.” Yu, [0027], Fig. 2E.

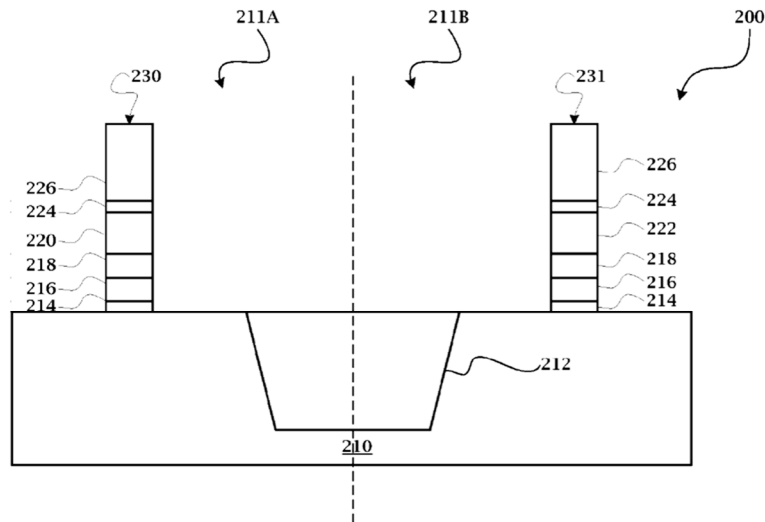


FIG. 2E

Yu, Fig. 2E

Usui's disclosure about "achiev[ing] the necessary properties of the [interconnect metallurgy] structure of [Usui's] *present invention*" to mitigate electromigration (Usui, 3:23-37, 2:33-39) would not have motivated a POSA to make any change to Yu's CMOS gate electrode which does not experience high current density and thus has no electromigration concerns. Piner, ¶273. Petitioner's assertion that Usui would have motivated a POSA to make Yu's diffusion barrier/protection layer 218 thinner than Yu's capping layer 226 fails for this additional reason.

4. Petitioner's Reliance on *KSR*'s Known Techniques/Predictable Results Rationale Fails

Petitioner asserts that Usui's teaching to limit the thickness of underlayer 13 in Usui's interconnect metallization structure would have motivated a POSA to limit the thickness of Yu's diffusion barrier/protection layer 218 because this

would have been nothing more than “combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results.” Petition, 39 (citing *KSR*); *see also* Petition, 37.

The invoked *KSR* rationale only applies when the elements are combined without “change in their respective functions.” *KSR*, 550 U.S. at 415-416. The “function” of Usui’s underlayer 13 is to provide connection to interplanar stud connection 10 and when its thickness is limited “the structure and texture of the subsequently to be applied metallic layers [of the interconnect metallurgy structure] is carefully controlled” to mitigate electromigration. Usui, 3:29-37, 2:33-39, 5:11-14, Fig. 8; Petition, 38-39; Piner, ¶¶274-277.

The function of Usui’s underlayer 13 is dramatically changed in Petitioner’s Yu-Usui combination, where the alleged bottommost metal layer is Yu’s diffusion barrier/protection layer 218. Diffusion barrier/protection layer 218 does not connect to a metal stud, is not the bottommost layer of Yu’s metal gate stack, and its function is to prevent diffusion of materials between Yu’s metal layers (220, 221) and oxide layers (214, 216). Yu, [0029]-[0030]; *see also* EX-2002, [0057]-[0058], Fig. 6. Thus, Petitioner’s invoked *KSR* rationale (Petition, 39) does not support Petitioner’s Yu-Usui combination. Nothing does. That is an additional reason why Ground 5 fails.

VI. GROUNDS 6-7 FAIL

A. Grounds 6-7 Fail with Ground 5

Grounds 6-7 add references to Ground 5's Yu-Usui combination to address certain dependent claims. Petition, 3. Petitioner does not rely on these references to meet any limitation in the independent claims, so Petitioner could only rely on Ground 5's showing to meet independent claims 1 and 13. Petition, 55-64. Thus, Grounds 6-7 inherit Ground 5's above-discussed flaws and fail for the same reasons.

B. Ground 6 Fails for Claims 11 and 16 for Additional Reasons

Ground 6 alleges obviousness of claims 11 and 16 – which require that the gate electrode make Schottky contact with the semiconductor – over Yu, Usui, and Adesida. Ground 6 is facially deficient.

Petitioner admits Yu's gate electrode does not make Schottky contact with the semiconductor but alleges Adesida's does. Petition, 58. Ground 6 maps Adesida's "**gate 190 (gate electrode)**" to the gate electrode in claims 11 and 16, using the annotated figure below. Petition, 60-61. That fails to demonstrate obviousness because claims 11 and 16 limit "said electrical contact" in claims 1 and 13, respectively, and Petitioner never even alleges that Adesida's gate

electrode meets claim 1 or 13. It does not.¹⁶ Piner, ¶¶278-282. That is fatal to Ground 6.

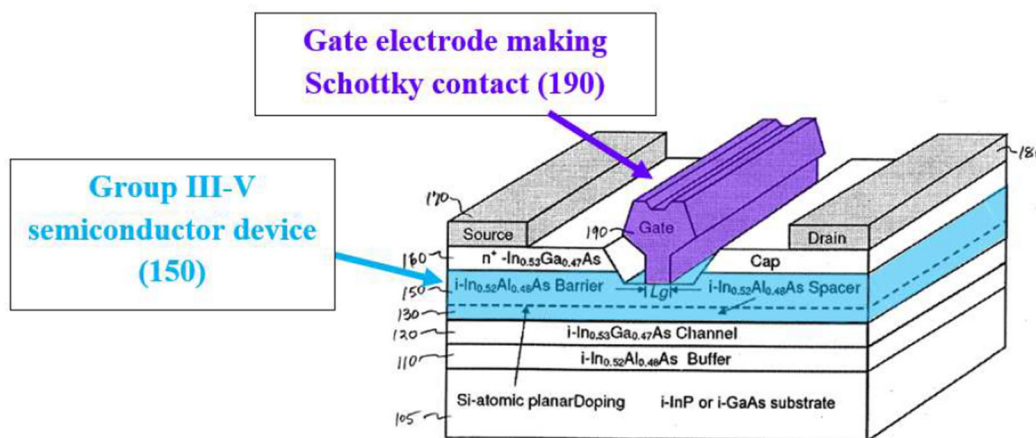


Figure 5

Petitioner's Annotated Adesida, Fig. 5

To the extent Petitioner alleges in Reply that the gate electrode in Yu-Usui-Adesida is not Adesida's gate electrode, that would fail. The Petition was required to specify its grounds with particularity and provide a "detailed explanation" thereof. 35 U.S.C. § 312; 37 C.F.R. § 42.104(b)(4). Moreover, a "prerequisite" to establishing obviousness is to explain the "contemplated workings" of the Yu-Usui-Adesida combination. *Personal Web*, 848 F.3d at 994. The Petition fails to do so. Ground 6 fails for that reason as well.

¹⁶ For example, Petitioner does not establish that Adesida's gate electrode has a capping layer of a refractory metal nitride (limitation [1a]) or of TiN and/or TaN (limitation [13b]).

Finally, to the extent Petitioner alleges in Reply that the structure of the gate electrode in Yu-USUI-Adesida is **Yu's** gate electrode but modified to make Schottky contact, that would fail because the Petition *never alleges this* and cites *no evidence* in support. Piner, ¶¶283-286. Yu discloses a CMOS device with “a **high-k gate dielectric** and metal gate electrode.” Yu, [0004]. Petitioner admits that Yu's Fig. 2E – which Petitioner relies on for claims 1 and 13 (Petition, 41-44 and 54-55) – has dielectric “insulating” layers 214, 216 (Petition, 53-54), so it is an insulated gate electrode that does not make Schottky contact. Piner, ¶284.

Petitioner cites no reference disclosing a Schottky gate electrode for a CMOS device like Yu's. That would be highly unconventional and is the furthest thing from a “simple design choice” as Petitioner erroneously alleges. Petition, 59; Piner, ¶285. Moreover, Petitioner's assertion that a POSA would have modified Yu to *remove* its high-k dielectric but *retain* Yu's gate structure – which is *specifically designed to work with that high-k dielectric* – is unsupported and based on nothing but improper hindsight. *Id.* POSAs would not have used a Schottky gate electrode for Yu's CMOS device, and if interested in implementing a Schottky gate electrode, would not have used Yu's metal gate electrode specifically designed for use with a high-k dielectric insulator. *Id.*

Moreover, Petitioner fails to establish a reasonable expectation of success. To the extent Petitioner suggests that Yu-USUI's alleged electrical contact could

simply be used unchanged to form a Schottky contact, no evidence supports that. POSAs understood this would require changes to the layers – in their materials and thicknesses – because Schottky contacts, like ohmic contacts, are tailored to the semiconductor. Piner, ¶286. Petitioner fails to account for the changes that would be required and fails to show that the alleged electrical contact of Yu-USui-Adesida would meet claim 1 or 13 after such changes. *Id.*

C. Ground 7 Fails for Additional Reasons

Ground 7 alleges obviousness of claims 10 and 15 – requiring that the electrical contact is “implemented as a power electrode making ohmic contact with said...semiconductor device” – over Yu, Usui, and Sugimoto.

Ground 7 is facially deficient. To demonstrate obviousness, Petitioner needed to establish some supportable non-hindsight *reason why* a POSA “would have selected and combined [the] prior art elements” in a manner “*yield[ing] the claimed invention.*” *Unigene Labs*, 655 F.3d at 1360; *see also KSR*, 550 U.S. at 418; *TQ Delta*, 942 F.3d at 359. The Petition did not even try to make the legally required showing.

Even if everything Ground 7 alleges were accepted as true, it fails to demonstrate obviousness of claim 10 or 15. Petitioner admits that neither Yu nor Usui discloses a power electrode making ohmic contact. Petition, 62. Petitioner alleges that Sugimoto discloses a Group III-V semiconductor device, like Yu, and

source and drain electrodes that are power electrodes making ohmic contact. *Id.*, 62-63 (alleging ohmic contacts were well-known and important for implementing *source and drain* electrodes). Petitioner concludes by alleging motivation “to implement the devices of Yu and Yu-Usui with a power electrode making an ohmic contact, as taught by Sugimoto” because this “would provide reduced internal heating of the contact and improved current flow (i.e., improved work function values).” Petition, 63 (citing Adesida, [0031], Fig. 5; Zhao ¶¶51-57, 206). Petitioner also again invokes *KSR*’s known techniques rationale. *Id.*

Infineon does not dispute it would have been obvious to implement Yu’s CMOS device to have source and drain electrodes that are power electrodes making ohmic contact. But that does not meet claim 10 or 15. Piner, ¶¶287-289. Those dependent claims limit “said electrical contact” recited in independent claims 1 and 13, respectively. Ground 7 does not even purport to show how Ground 7’s *Yu-Usui-Sugimoto combination* allegedly meets claim 1 or 13. Petition, 62-64. For that reason alone, Ground 7 fails.

If the Petition is read to implicitly suggest that Ground 7’s Yu-Usui-Sugimoto combination meets claims 1 and 13 in the same way that Ground 5’s Yu-Usui combination does, that fails. Ground 5 alleges that the claimed electrical contact comprising an electrode stack is met by Yu’s “metal *gate* stacks.” Petition, 41-44 and 54-55. Yu’s gate stacks form CMOS *gate*

electrodes¹⁷ that are undisputedly not ohmic contacts because they do not contact the semiconductor. Yu, Title, Abstract, [0004], Fig. 2E, [0027] (insulating “dielectric layer 214” is “formed over the substrate”); Piner, ¶¶287-291; Zhao, ¶¶56-57.

Petitioner alleges that ohmic contacts were known to “serve as *source and drain* contacts in group III-V devices and allow current to flow into and out of a semiconductor material.” Petition, 62-63. Current flow in and out of the semiconductor does not occur through Yu’s *gate* electrodes; thus, even if a “POSITA would have been motivated to implement the devices of Yu and Yu-Usui with a power electrode making an ohmic contact” (Petition, 63), a POSA would have implemented the device’s *source and drain* electrodes as power electrodes making ohmic contact. Piner, ¶292. That does not meet claim 10 or 15 because it makes no change to Yu’s *gate* electrode which is alleged to meet “said electrical contact” in independent claims 1 and 13. Petition, 41-44 and 54-55.

Petitioner does not even allege that a POSA would have implemented the Yu-Usui-Sugimoto combination by having its *source or drain* electrode have the same structure as either Yu *gate* electrode alleged to meet “said electrical

¹⁷ CMOS devices include two or more transistors. Piner, ¶291; Zhao-Dep., 60:15-17.

contact” in independent claims 1 and 13, let alone establish with evidence some supportable reason why this allegedly would have been so. Piner, ¶293.

It was well-known that a CMOS gate electrode is separated from the semiconductor by a dielectric layer and serves a different purpose than ohmic source and drain electrodes that contact the semiconductor and have current pass through them when the transistor is on. Piner, ¶294 (a CMOS gate controls the transistor through an electrical field across the gate dielectric without current flowing through the gate); EX-1011, 356, 434-36, 454-57; Petition 63 (low contact resistance is critical for ohmic contacts for “improved current flow”). Thus, CMOS gate electrodes were conventionally implemented using a *different structure formed from different materials* than CMOS source and drain electrodes. Piner, ¶294.

Petitioner never alleges that a POSA had any reason to implement the Yu-Usui-Sugimoto combination by having the *source or drain* electrode have the same structure as either Yu *gate* electrode¹⁸ alleged to meet “said electrical contact” comprising an electrode stack in independent claims 1 and 13. Petition,

¹⁸ Yu is directed to a particular CMOS *gate* electrode implementation using a high-k dielectric and metal *gate* electrodes with different work functions for the device’s NMOS and PMOS transistors. Yu, Title, [0004], [0030]; Piner, ¶¶295, 106-114.

41-44 and 54-55. Petitioner thus points to an electrical contact comprising a gate electrode to allegedly meet the requirements in claims 1 and 13, but never alleges that this same electrical contact comprising a gate electrode meets the additional requirements that claims 10 and 15 impose. That is fatal to Ground 7 because Petitioner fails to establish some supportable non-hindsight reason why a POSA would have combined the prior art elements in a manner that “yield[s] the claimed invention” in claim 10 or 15. *Unigene Labs*, 655 F.3d at 1360; *see also KSR*, 550 U.S. at 418; *TQ Delta*, 942 F.3d at 359.

Moreover, Petitioner fails to establish a reasonable expectation of success. To the extent Petitioner suggests that Yu-Usui’s alleged electrical contact could simply be used unchanged to form an ohmic contact, no evidence supports that. POSAs understood this would require significant changes to the layers – in their materials and thicknesses – because ohmic contacts are closely tailored to the semiconductor, like a lock and key. *Piner*, ¶¶48-57. Petitioner fails to account for the changes that would be required and fails to show that the alleged Yu-Usui-Sugimoto electrical contact would meet claims 1 and 13 after such changes. *Piner*, ¶296.

Respectfully submitted,

Date: September 30, 2025

/Richard Giunta/

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing **PATENT OWNER'S RESPONSE** contains 13,998 words excluding; a table of contents, a table of authorities, a certificate of service or word count, or appendix of exhibits or claim listing. Patent Owner has relied on the word count feature of the word processing system used to create this paper in making this certification.

Date: September 30, 2025

/MacAulay Rush/

MacAulay Rush

Paralegal

WOLF, GREENFIELD & SACKS, P.C.

CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.6 (e)(4)

I certify that on September 30, 2025, a copy of the foregoing document, including any exhibits filed therewith, is being served via electronic mail, as previously consented to by Petitioner, upon the following:

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