



US 20070108585A1

(19) **United States**

(12) **Patent Application Publication**
Pavier et al.

(10) **Pub. No.: US 2007/0108585 A1**

(43) **Pub. Date: May 17, 2007**

(54) **SEMICONDUCTOR PACKAGE INCLUDING
A SEMICONDUCTOR DIE HAVING
REDISTRIBUTED PADS**

Related U.S. Application Data

(60) Provisional application No. 60/736,003, filed on Nov. 10, 2005.

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Publication Classification

(51) **Int. Cl.**
H01L 23/48 (2006.01)

(52) **U.S. Cl.** **257/690**

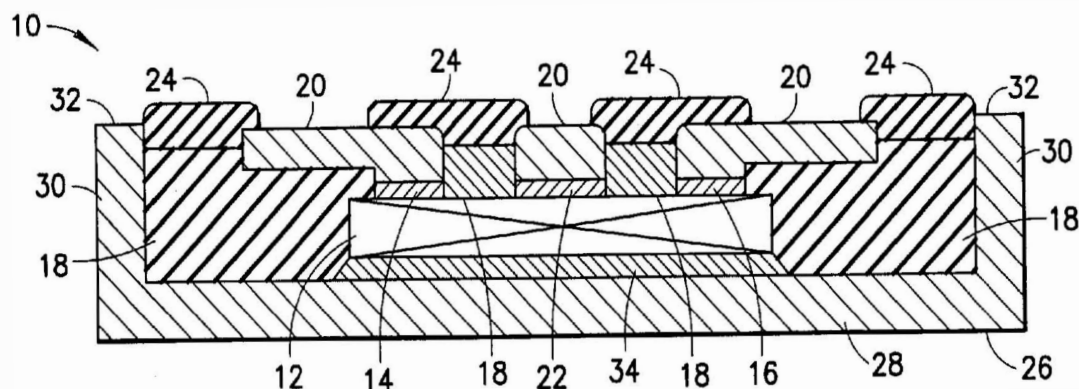
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(57) **ABSTRACT**

(21) Appl. No.: **11/595,206**

A semiconductor package that includes a semiconductor die, an insulation around the die, and a conforming conductive pad coupled to an electrode of the die.

(22) Filed: **Nov. 10, 2006**



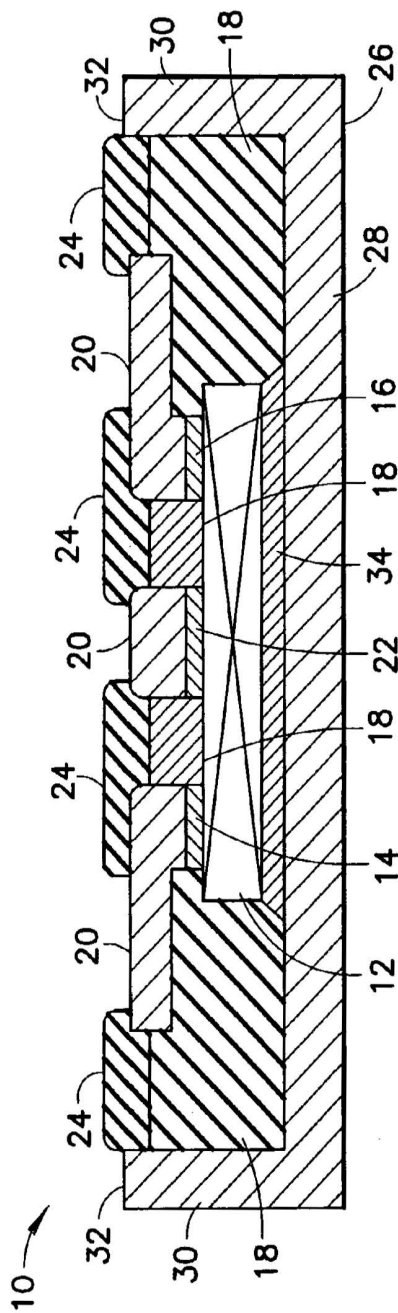


FIG. 1

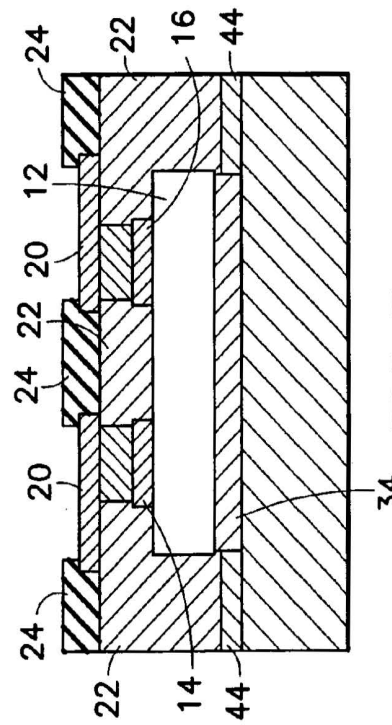


FIG. 3

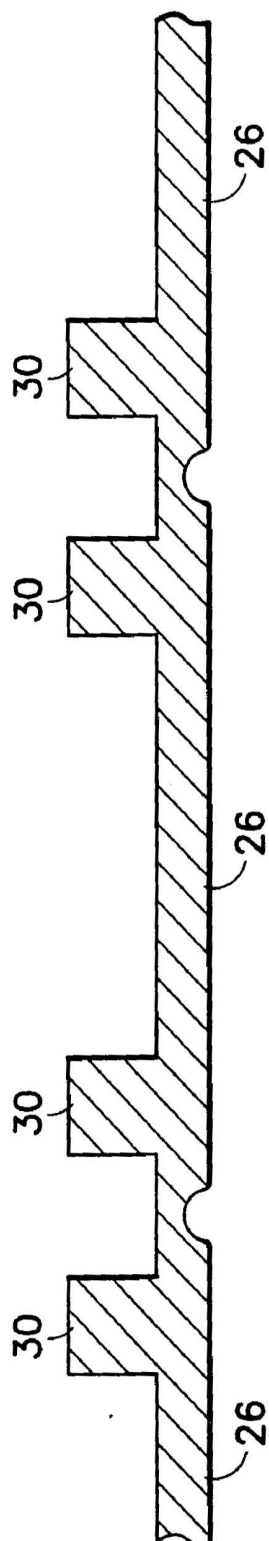


FIG. 2A

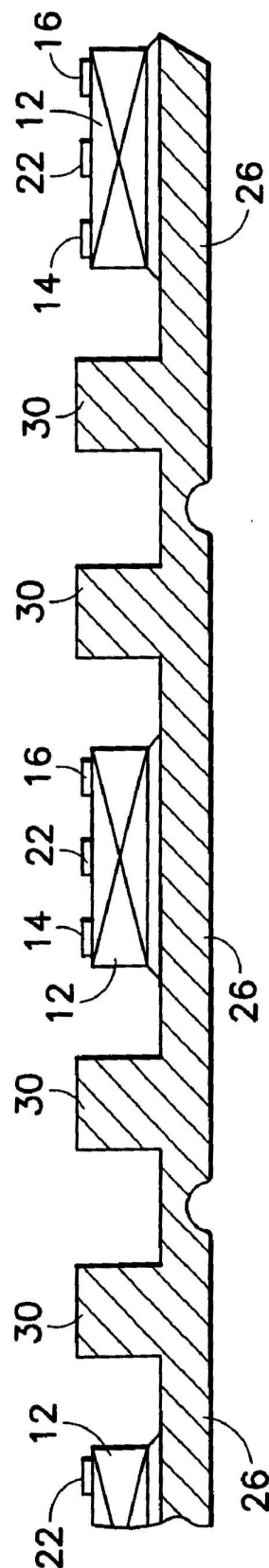


FIG. 2B

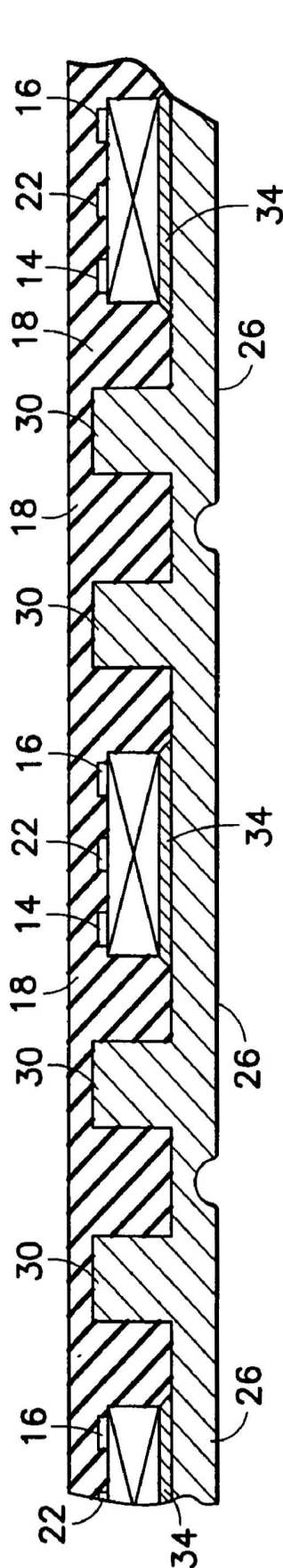


FIG. 2C

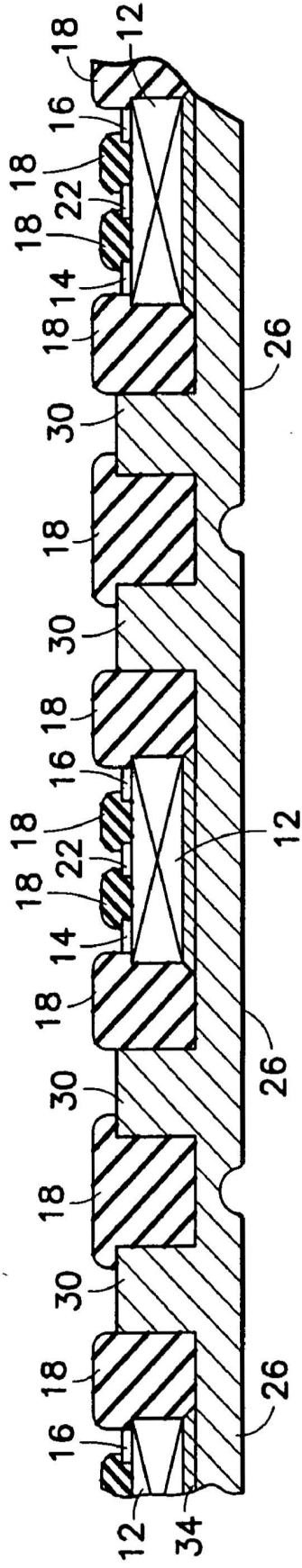


FIG. 2D

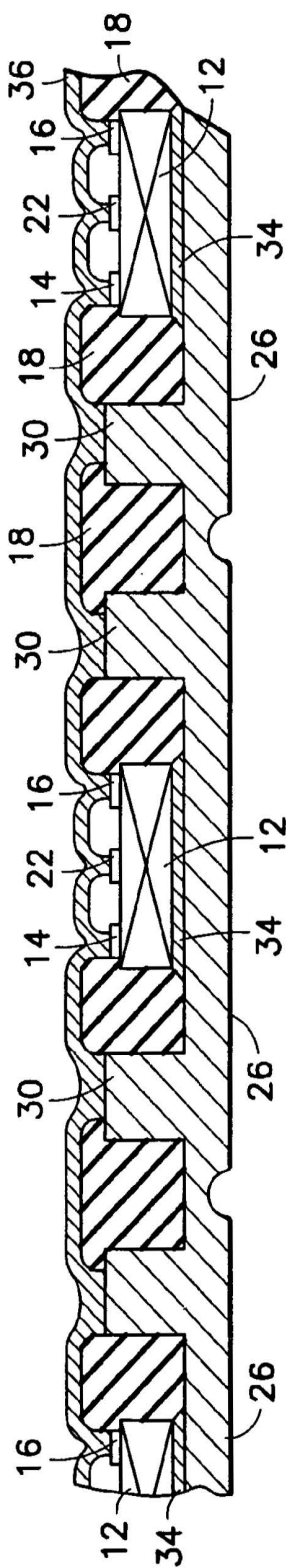


FIG. 2E

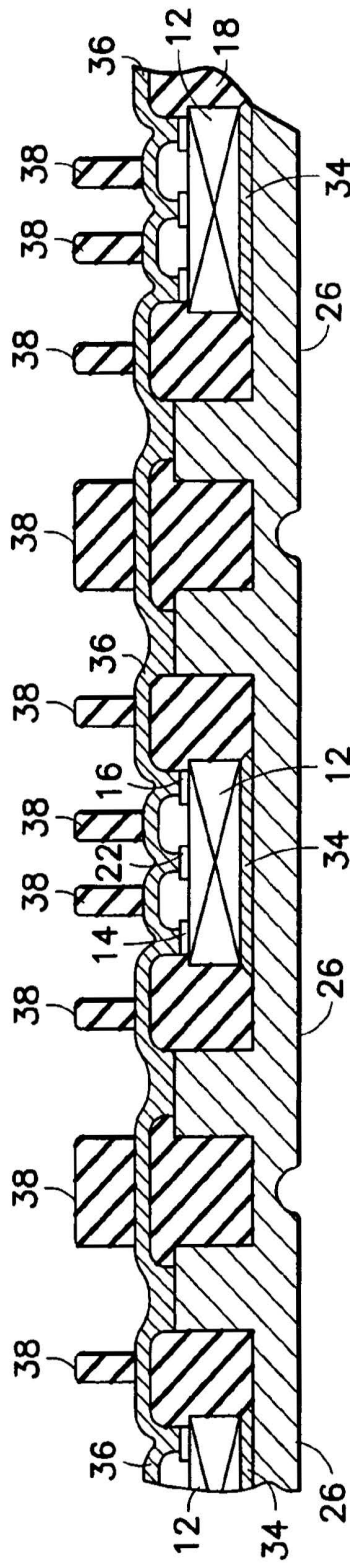


FIG. 2F

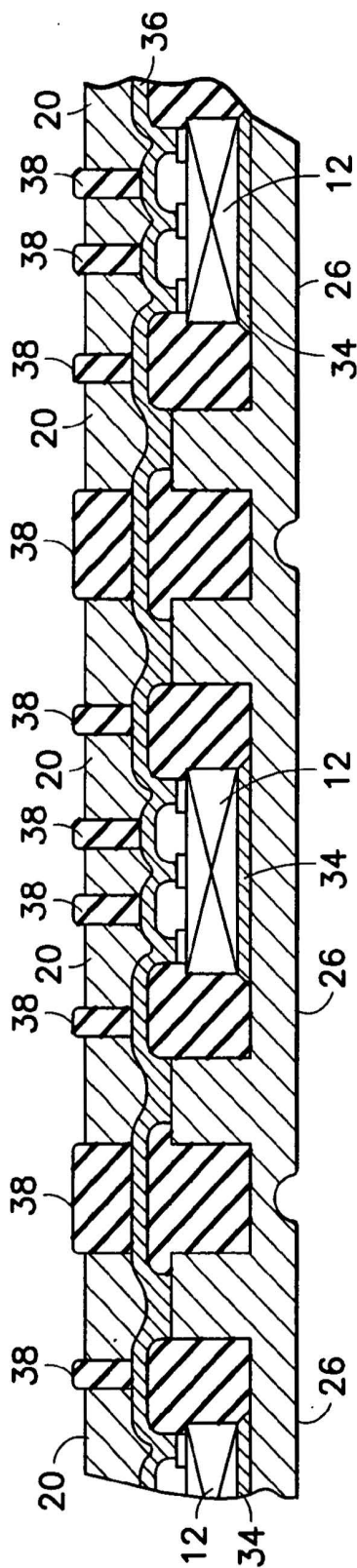


FIG. 2G

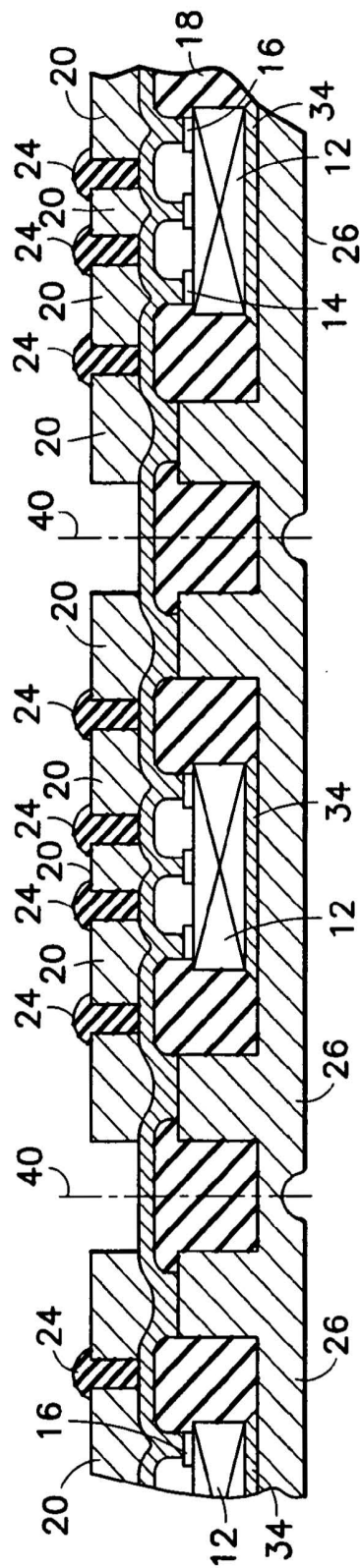


FIG. 2H

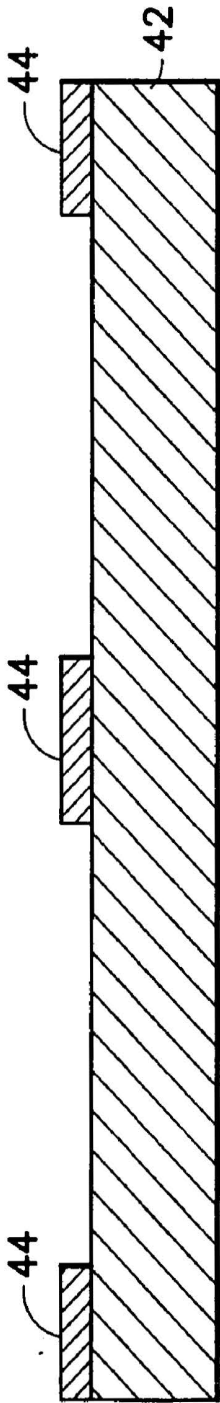


FIG. 4A

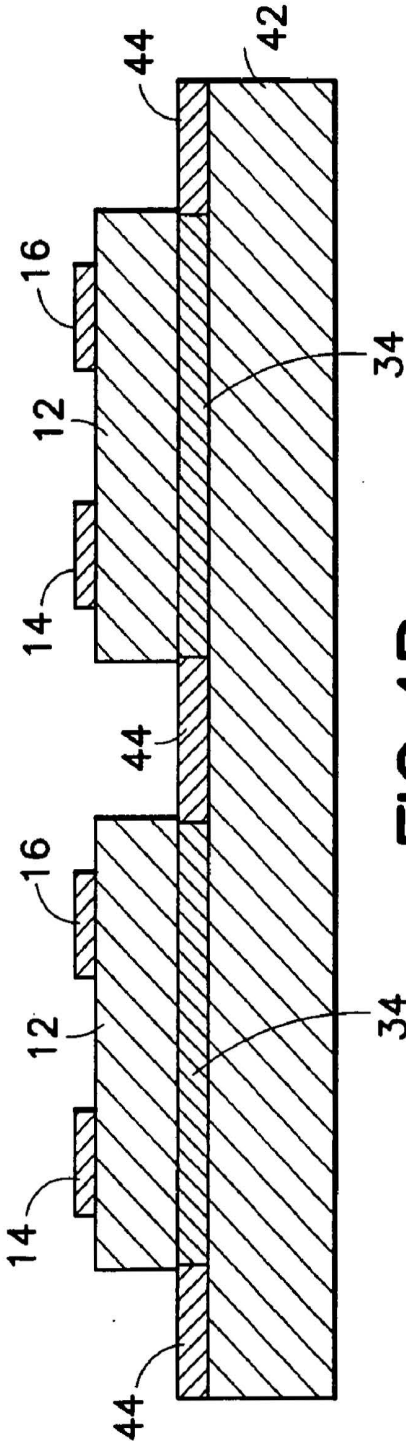


FIG. 4B

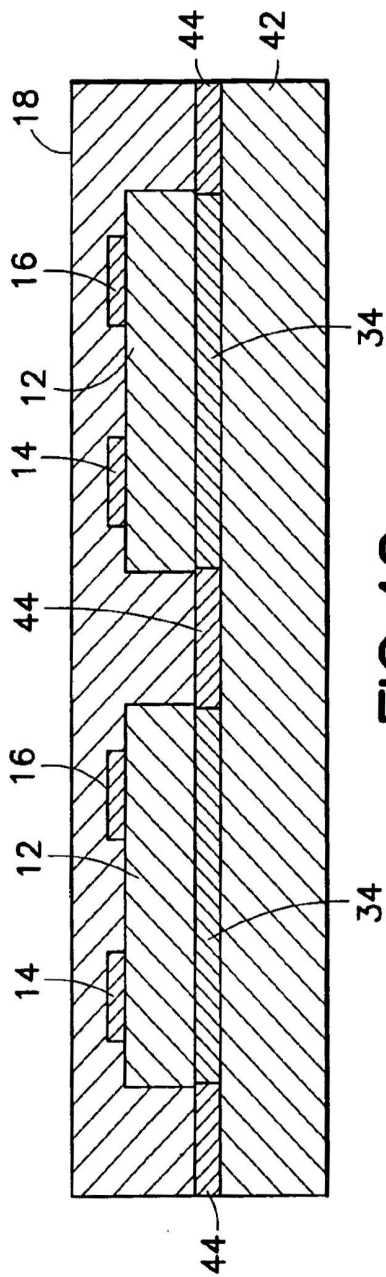


FIG. 4C

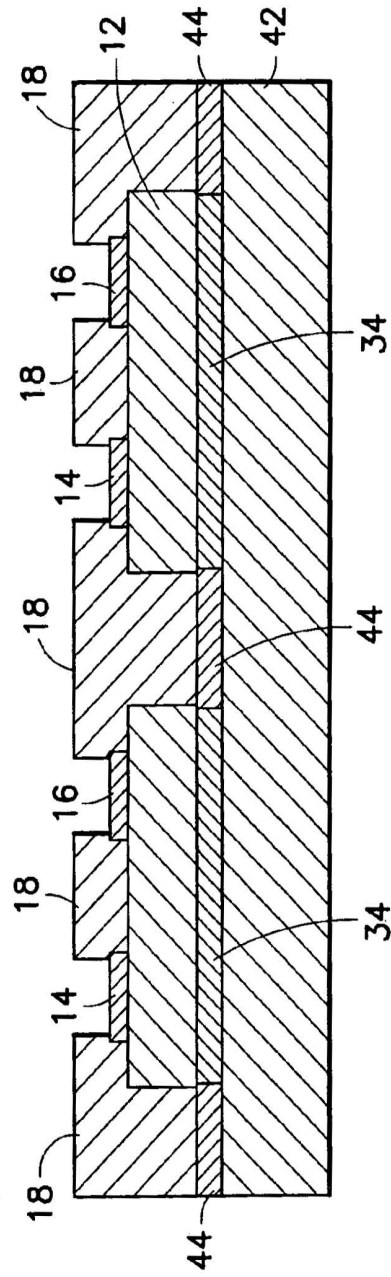


FIG. 4D

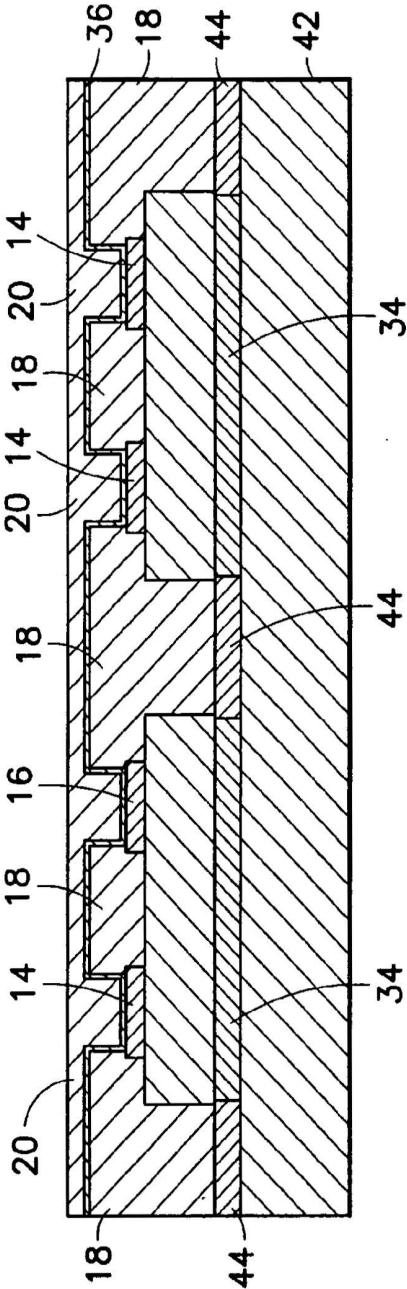


FIG. 4E

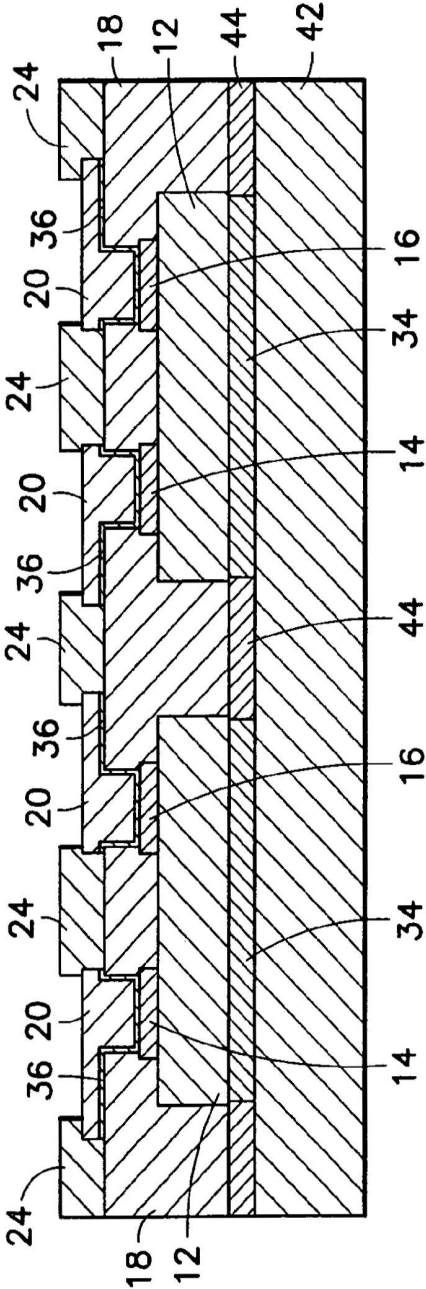


FIG. 4F

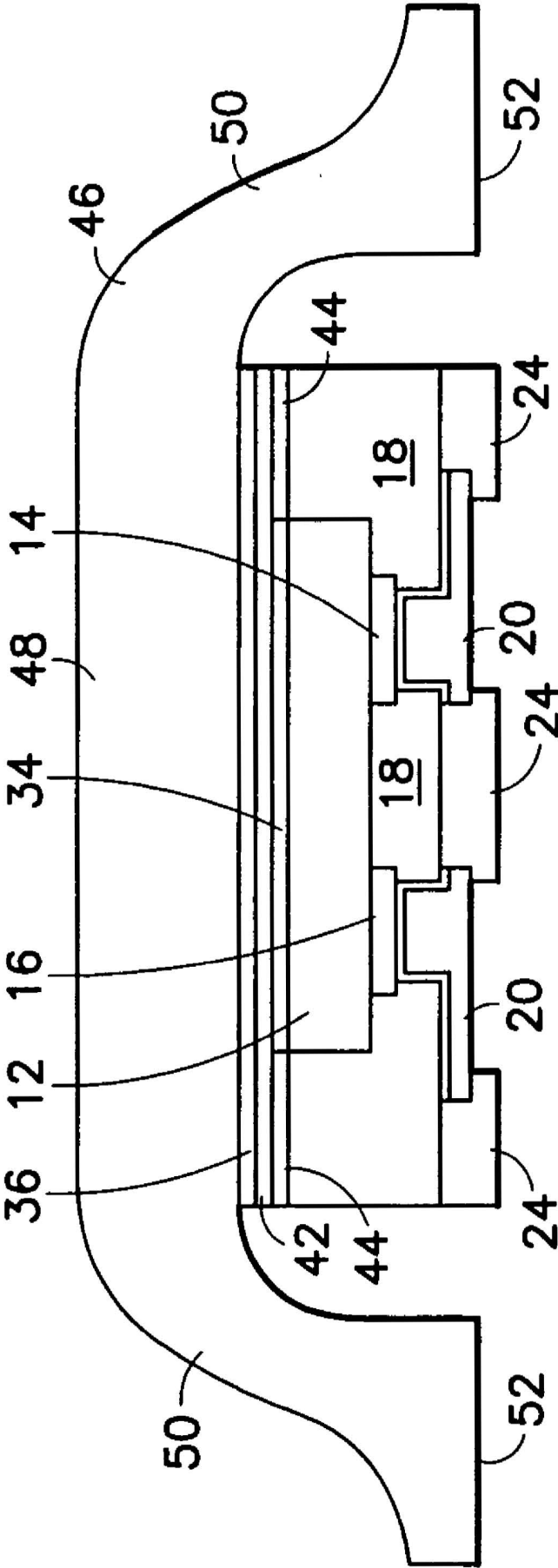


FIG. 5

SEMICONDUCTOR PACKAGE INCLUDING A SEMICONDUCTOR DIE HAVING REDISTRIBUTED PADS

RELATED APPLICATION

[0001] This application is based on and claims benefit of U.S. Provisional Application Ser. No. 60/736,003, filed on Nov. 10, 2005, entitled Power Semiconductor Die with Redistributed Contact Pads, to which a claim of priority is hereby made and the disclosure of which is incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to semiconductor packages and methods of fabricating semiconductor packages.

[0003] As demand for improved performance and reduction in the cost of semiconductor devices such as power semiconductor devices increases, the size of semiconductor devices decreases while the performance thereof increases. Specifically, it is anticipated that to reduce the cost of manufacturing more die must be fabricated out of a single wafer, while each die must provide better characteristics, such as more current carrying capability per unit area. Consequently, it is expected that as the die size decreases the electrodes thereof that make external connection via, for example, a solder body will also decrease in size while the current passed therethrough will increase.

[0004] It is believed that the reduction in the size of the electrodes combined with an increase in the current load passing through the electrode and its solder connection, particularly in the presence of high switching frequencies, may result in a higher than desirable failure rate in the solder connection due, for example, to electromigration or the like phenomenon.

[0005] Furthermore, it may become difficult for the end users of semiconductor die to adapt to connecting semiconductor die to conductive pads or the like of circuit boards if the electrodes are made small.

SUMMARY OF THE INVENTION

[0006] A semiconductor package according to the present invention includes a semiconductor die, the die including an electrode having an area, a conductive pad directly connected to the electrode, the pad having an area that is larger than the area of the electrode of the die, whereby the electrode of the die is redistributed to a larger connection surface for external connection.

[0007] A semiconductor package according to the present invention includes a semiconductor die including at least one electrode disposed on one major surface thereof, the electrode having a first area, an insulation body disposed around the semiconductor die, and a conforming conductive pad being coupled to the at least one electrode and extending over and conforming to a portion of the insulation body, the conforming pad having an area that is larger than the area of the electrode.

[0008] In a package according to one preferred embodiment, the conductive pad may include a solderable surface, and/or a passivation body, which may have solder resist

characteristics, disposed over the semiconductor die, the passivation body including at least one opening over the conforming conductive pad.

[0009] According to one embodiment of the present invention, the web portion of a conductive clip is coupled to another major surface of the semiconductor die opposite the one major surface thereof. The clip may include at least one lead extending from an edge of the web portion, the lead including a connection surface generally coplanar with the conforming conductive pad.

[0010] In another embodiment of the present invention a conductive plate is coupled to another major surface of the semiconductor die opposite the one major surface.

[0011] A method for fabricating a semiconductor package includes coupling a first major surface of a semiconductor die to a metallic body, depositing an insulation body over the semiconductor die, removing a portion of the insulation body to expose at least one electrode of the semiconductor die on a second major surface of the semiconductor die opposite the first surface, the one electrode having an area, and forming a conductive pad having an area larger than the area of the one electrode and extending over the insulation body.

[0012] Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 illustrates a cross-section view of a package according to the first embodiment of the present invention.

[0014] FIGS. 2A-2H illustrate a method for fabricating a package according to the first embodiment.

[0015] FIG. 3 illustrates a package according to the second embodiment of the present invention.

[0016] FIGS. 4A-4F illustrate a method for fabricating a package according to the second embodiment.

[0017] FIG. 5 illustrates an enhanced package according to the second embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0018] Referring to FIG. 1, a semiconductor package 10 according to the first embodiment of the present invention includes a semiconductor die 12, which may be a power semiconductor device, such as a power MOSFET or an IGBT, having preferably two electrodes 14, 16 on one surface thereof. Electrodes 14, 16 may be power electrode 14 (e.g. source electrode or emitter electrode) and control electrode 16 (e.g. gate electrode) respectively. An insulation body 18 is disposed around die 12 but includes openings leading to and exposing at least a portion of each electrode 14, 16. According to an aspect of the present invention a conforming conductive pad 20 (made, for example, from copper or the like metal) is coupled to each electrode 14, 16 and extends through a respective opening in and over a portion of insulation body 18. To obtain the desired distribution, each contouring conductive pad 20 has a larger free surface area available for external connection than the surface area of the electrode to which it is coupled. Note that

each pad conforms to (i.e. follows the contours of) the portion of insulation body 18 over which it lies. Further note that each pad 20 is directly coupled to respective electrode 14, 16 without the solder or the like conductive adhesive.

[0019] Semiconductor die 12 may be a lateral condition device and thus may include another power electrode 22 (e.g. drain electrode or collector electrode) arranged generally coplanar with electrodes 14, 16. Note that a conforming conductive pad 20 is coupled to electrode 22 and redistributes electrode 22 in the same manner as the other electrodes 14, 16. Conductive pads 20 are preferably rendered solderable with a solderable body such as a Ni/Ag or Ni/Au stack.

[0020] A package according to the present invention preferably includes a passivation body 24. Passivation body 24 preferably includes solder resist characteristics, and as shown is disposed between pads 20 to prevent shorting due to solder encroachment during solder reflow when package 10 is being mounted onto an end user's circuit board or assembly.

[0021] Package 20 may further include a conductive clip 26 (formed, for example, from copper or a copper alloy). Clip 26 includes a web portion 28, and lead portion 30 each having a connection surface 32 which is generally coplanar with pads 20. Web portion 28 of clip 26 may be thermally coupled to a surface of die 12 opposite pads 20 with a thermally conductive adhesive, such as, solder or a thermally conductive adhesive 34. Note that a die in a package according to the invention may be a vertical conduction device, in which case an active electrode (e.g. power electrode) may be disposed opposite to pads 20. In such a case, the active electrode so arranged may be electrically and mechanically coupled to clip 26 with solder, and clip 26 may be used as a lead frame as well as a thermal dissipater (i.e. heatsink, or heat spreader).

[0022] Referring to FIGS. 2A-2H, a package 10 according to the first embodiment of the present invention is fabricated by first providing a plurality of clips 26 interconnected to form a matrix (FIG. 2A) so that a number of packages can be fabricated simultaneously. Thereafter, solder 34 is deposited (e.g. in paste form) in the interior of each clip 26, die 12 is disposed over solder 34, and solder 34 is then reflowed. Next, insulation 18, which is preferably photoimageable, is deposited over die 12 preferably encapsulating the same as shown in FIG. 2C. Portions of insulation 18 are then removed, through photolithography, to provide openings to expose electrodes 14, 16, 22. Thereafter, a copper seed layer 36 is applied by sputtering or the like on the arrangement shown by FIG. 2D as illustrated by FIG. 2E. Thereafter, a mask 38 is formed over seed layer 36. Note that mask 38 will define portions of seed layer 36 to be removed (as explained below).

[0023] It should be noted that insulation 18 need not be photoimageable but can be patterned using other techniques, for example, laser ablation. For example, when insulation 18 is thicker than a few tens of microns an alternate material containing fillers such as silica may be required. Photoimaging of such materials is not always possible as the exposure beam is not able to pass through the fillers or is blocked by the increased thickness of the passivation. Where this is the case a more suitable process for selectively removing passivation over contacts 14, 16 may be laser ablation. A suitable laser such as a Nd:YAG, CO₂ or excimer laser may be used to pattern the contact openings in insulation 18.

[0024] There are several other options available to create seed layer 20. For example, an electroless copper plating process can be used to deposit anywhere between 1 and 10 μm of copper over the surface of the assembly. The electroless plated seed layer can then be patterned through appropriate photolithography, and then electrolytic plating can be used to create thick conductive tracks. Any remaining photoresist from the photolithography step can be then stripped and the unwanted seed layer can be etched away.

[0025] Alternatively, a seed layer can be deposited using drop-on-demand deposition. In this case, ink containing a suspension of nano particulate (e.g. Ag or Cu) may be drop-on-demand deposited to create a silver or copper seed layer on the assembly. The assembly containing the ink is then cured to 'sinter' the metal nano-particles together and create a metallic film in the region of 0.2 to 3 μs thick. Where this process is used it is possible to place the seed layer in pre-defined regions on the assembly and remove the requirement for the subsequent application of photoresist materials/pattern plating. Additional metal may also be deposited onto the seed layer using electroless or electrolytic copper deposition. Drop-on-demand deposition is disclosed in U.S. patent application Ser. No. 11/367,725, assigned to the assignee of the present application, and incorporated herein by this reference.

[0026] Next, pads 20 are formed over portions of seed layer 36 not covered by mask 38 through, for example, electroplating or electroless plating. Thereafter, mask 38 and portions of seed layer 36 below mask 38 are removed through appropriate etching or the like whereby isolated pads 20 are left remaining. Passivation body 24 is then applied and packages 10 are cut out along scribe lines 40 from the clip matrix.

[0027] Referring next to FIG. 3, in which like numerals identify like features, a semiconductor package 41 according to the second embodiment of the present invention includes flat conductive plate 42 (formed, for example, from copper or a copper alloy) instead of a clip as shown. In all other respects package 41 according to the second embodiment is similar to package 10.

[0028] Referring to FIGS. 4A-4F, a package 41 according to the second embodiment is fabricated by first formed solder mask 44 over a surface of a large copper plate 42, solder mask 44 including openings therein to expose selected portions of plate 42 (see FIGS. 4A). Solder paste 34 is then disposed inside each opening in mask 44, and after a respective die is disposed on each body of paste 34, paste 34 is reflowed (see FIG. 4B). Thereafter, insulation 18 is deposited over die 12 to encapsulate the same (see FIG. 4C). Portions of insulation 18 are then removed to expose electrodes 14, 16 of die 12 (FIG. 4D), a copper seed layer 36 is formed as previously described, and then copper is plated on seed layer 36. Plated copper 20 is then patterned to form pads 20, passivation body 24 is then applied, and packages 41 are cut out along scribe line 40, for example, to obtain packages according to the second embodiment. Note that solder mask 44 may not be required if the conductive adhesive contains epoxy or a similar polymeric adhesive such as a conductive epoxy (e.g. Ablestik 84-I) or an insulating polymer (e.g. Ablestik 84-3J).

[0029] In an alternative embodiment copper plate 42 can be replaced with a patterned substrate that includes insulated

die pads (each pad for receiving a semiconductor die in the same manner described above) and traces. Such an alternative embodiment may allow for fabrication of multi-chip packages for, for example, half-bridge circuits or full bridge circuits.

[0030] Referring to FIG. 5, a conductive clip 46 (formed from, for example, copper or a copper alloy) having a web portion 48 and leads 50 can be coupled at least thermally and mechanically, or electrically and mechanically (when die 12 includes an active electrode opposite electrodes 14, 16) to plate 42 with a layer of thermally conductive adhesive, such as solder 34 conductive epoxy, or the like. Note that each lead 50 may include a connection surface 52, which is generally coplanar with pads 20. When die 12 includes an active electrode opposite pads 20, clip 46 can serve as a lead frame used for external electrical connection as well as a thermal dissipater for package 41. Otherwise, clip 46 can serve to dissipate heat from package 41, only.

[0031] In cases where die 12 includes a major electrode disposed on the back thereof (opposite electrodes 14, 16 on the front), it is possible to create a hole or via through insulation 18 to redistribute the back electrode to pads on the front side of the package that are co-planar with pads 20. In such a case the via sidewalls may be coated with metal using the seed/plating processes described above in order to electrically couple the back electrode that is electrically connected to the plate to the redistributed pad on the front surface of the package coplanar with pads 20.

[0032] In addition to pads 20, tracks may also be formed for interconnection while pads 20 are being processed. The tracks may be formed from Ag/Cu with Ni/Au solderable finish, or electroless/electrolytic copper and a solderable finish.

[0033] The present invention should not be understood to be limited to silicon-based semiconductor devices. Other semiconductor devices such as E-nitride based semiconductor devices can be used without deviating from the scope and spirit of the present invention.

[0034] In addition, the present invention is not limited to one semiconductor die per package. Rather, multiple die may be thermally and mechanically coupled to the lead frame in the manner described above before overmolding and other steps are carried out to obtain a package that includes more than one die. Furthermore, a package according to the present invention may include passive components (e.g. capacitors, resistors, inductors) which may be accessible through vias or the like access features in the clip or the metallic plate.

[0035] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A semiconductor package, comprising:

a semiconductor die including at least one electrode disposed on one major surface thereof, said electrode having a first area;

an insulation body disposed around said semiconductor die; and

a conforming conductive pad being coupled to said at least one electrode and extending over and conforming to a portion of said insulation body, said conforming pad having an area that is larger than said area of said electrode.

2. The package of claim 1, wherein said conductive pad includes a solderable surface.

3. The package of claim 1, further comprising a passivation body disposed over said semiconductor die, said passivation body including at least one opening over said conforming conductive pad.

4. The package of claim 1, wherein said passivation body includes solder resist characteristics.

5. The package of claim 1, further comprising a conductive clip having a web portion coupled to another major surface of said semiconductor die opposite said one major surface.

6. The package of claim 5, wherein said clip includes at least one lead extending from an edge of said web portion and including a connection surface generally coplanar with said conforming conductive pad.

7. The package of claim 6, wherein said web portion is coupled to said another major surface by a conductive adhesive body.

8. The package of claim 7, wherein said conductive adhesive body is comprised of solder or a conductive epoxy.

9. The package of claim 1, further comprising a conductive plate coupled to another major surface of said semiconductor die opposite said one major surface.

10. The package of claim 9, wherein said conductive plate is coupled to said another major surface with a conductive adhesive body.

11. The package of claim 10, wherein said conductive adhesive body is comprised of either solder or a conductive epoxy.

12. The package of claim 9, further comprising a conductive clip having a web portion coupled to said conductive plate.

13. The package of claim 12, wherein said conductive clip includes at least one lead extending from an edge of said web portion and including a connection surface generally coplanar with said conforming conductive pad.

14. The package of claim 6, wherein said web portion is coupled to said conductive plate by a conductive adhesive body.

15. The package of claim 14, wherein said conductive adhesive body is comprised of solder or a conductive epoxy.

16. The package of claim 1, wherein said semiconductor die is a IE-nitride semiconductor device.

17. The package of claim 1, further comprising another semiconductor die.

18. The package of claim 1, further comprising at least one passive component.

19. The package of claim 1, further comprising a patterned substrate that include at least one die pad coupled to another major surface of said semiconductor die opposite said one major surface.

20. The package of claim 19, wherein said patterned substrate includes another die pad coupled to another semiconductor die to obtain a multi-chip package.

21. The package of claim 20, wherein said package constitutes a half-bridge.

22. The package of claim 20, wherein said package constitutes a full-bridge.

23. The package of claim 1, further comprising a track.

24. The package of claim 23, wherein said track is comprised of Ag/Cu, which includes a solderable finish.

25. The package of claim 23, wherein said track is comprised of electroless or electrolytic copper and includes a solderable finish.

26. A method for fabricating a semiconductor package, comprising:

coupling a first major surface of a semiconductor die to a metallic body;

depositing an insulation body over said semiconductor die;

removing a portion of said insulation body to expose at least one electrode of said semiconductor die on a second major surface of said semiconductor die opposite said first surface, said one electrode having an area; and

forming a conductive pad having an area larger than said area of said one electrode on said one electrode and extending over said insulation body.

27. The method of claim 26, wherein said insulation body is photoimageable.

28. The method of claim 26, wherein said conductive pad is formed by forming a seed layer of a conductive material on said one electrode and plating a conductive body on said seed layer.

29. The method of claim 26, wherein said conductive pad is comprised of copper.

30. The method of claim 26, wherein said metallic body is a metallic plate.

31. The method of claim 26, wherein said metallic body is a metallic clip.

32. The method of claim 31, wherein said clip includes a connection surface that is generally coplanar with said conductive pad.

33. The method of claim 31, wherein said metallic clip is cup-shaped.

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