

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INNOSCIENCE AMERICA, INC.,  
PETITIONER,

V.

INFINEON TECHNOLOGIES AUSTRIA AG,  
PATENT OWNER.

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IPR2025-00175  
U.S. Patent 8,686,562

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**SUPPLEMENTAL DECLARATION OF YUJI ZHAO, Ph.D.**

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## **I. INTRODUCTION**

1. I have been retained by Innoscience America, Inc. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office.

2. I am over 21 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

3. I understand that this proceeding involves U.S. Patent No. 8,686,562 (“the ’562 patent,” Ex-1001).

4. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of any proceedings.

5. I previously provided a declaration in this proceedings as Ex. 1002. My CV was previously submitted as Ex. 1003.

6. I have been asked by Petitioner to provide my opinion on the meaning of the term ‘electrode stack’ as used in the claims of the ’562 patent according to a person of ordinary skill in the art at the time of the earliest possible priority date of the ’562 patent and to respond to Dr. Piner’s construction and analysis of the prior art under that construction. In performing my analysis, I have been asked to assume that the priority date of the ’562 patent is August 25, 2009, and my opinions are set forth below.

7. Throughout this declaration, I refer to specific pages, figures, and/or line numbers of various exhibits. These citations are illustrative and are not intended to suggest that they are the only support for the propositions for which they are cited.

## II. QUALIFICATIONS

8. My qualifications have been provided in my prior declaration. Ex. 1002; Ex. 1003.

## III. MATERIALS CONSIDERED

9. In forming my opinions, I have reviewed and considered the declaration of Dr. Piner (Ex. 2024), as well as all associated exhibits, the following documents, and any other document cited in my first declaration (Ex. 1002).

| Exhibit | Description                                                                                                                       |
|---------|-----------------------------------------------------------------------------------------------------------------------------------|
| Ex-1038 | U.S. Patent Publication No. 2006/0124954 A1 to Akaishi (Published June 15, 2006)                                                  |
| Ex-1039 | Songyuan Dai et al., <i>Design of DSC panel with efficiency more than 6%</i> , 85 Solar Energy Materials & Solar Cells 447 (2005) |
| Ex-1040 | U.S. Patent No. 5,940,732 to Zhang (Issued August 17, 1999)                                                                       |
| Ex-1041 | U.S. Patent Publication No. 2007/0210350 A1 to Omura et al. (Published September 13, 2007)                                        |
| Ex-1042 | U.S. Patent No. 7,381,993 B2 to Uchida et al. (Published June 3, 2008)                                                            |
| Ex-1043 | U.S. Patent Publication No. 2007/108585 A1 to Pavier, et al. (Published May 17, 2007)                                             |
| Ex-1044 | U.S. Patent Publication No. 2006/0258143 A1 to Kuo (Published November 16, 2006)                                                  |
| Ex-1045 | U.S. Patent Publication No. 2007/0190803 A1 to Singh (Published August 16, 2007)                                                  |

| <b>Exhibit</b> | <b>Description</b>                                                                                         |
|----------------|------------------------------------------------------------------------------------------------------------|
| Ex-1046        | Steven M. Kaplan, Wiley Electrical and Electronics Engineering Dictionary (John Wiley & Sons, Inc. (2004)) |

10. I have also relied on my education, experience, research, training, and knowledge in the relevant art, and my understanding of any applicable legal principles described in this declaration.

11. All the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my understanding of how a person of ordinary skill in the art would have understood the claims of the '562 patent at the time of the invention.

12. I reserve the right to supplement and amend any of my opinions in this declaration based on documents, testimony, and other information that becomes available to me after the date of this declaration.

#### **IV. LEGAL STANDARDS**

13. My understanding of the relevant legal standards is set forth in my previous declaration. Ex. 1002, ¶¶ 27-47, 76-79.

#### **V. LEVEL OF ORDINARY SKILL**

14. My understanding of the level of ordinary skill in the art is set forth in my previous declaration. Ex. 1002, ¶¶ 33-34, 80-82. I have applied the same level of ordinary skill in considering my opinions in this declaration.

**VI. THE PLAIN AND ORDINARY MEANING APPLIES TO THE CLAIMED “ELECTRODE STACK”**

15. My previous declaration articulates the legal standards on which I rely, including for claim construction. Ex. 1002, ¶¶ 27-47, 76-79.

**A. The Claims Do Not Limit the Term “Electrode Stack” Beyond Its Plain and Ordinary Meaning**

16. Nothing in the claims limits the term “electrode stack” beyond its plain meaning. Independent claims 1 and 13 recite an “electrical contact comprising: an electrode stack including plurality of metal layers and a capping layer formed over said plurality of metal layers.” Ex. 1001 at claims 1, 13. Thus, as Dr. Piner agrees, “the electrode stack is at least a part of an electrode in the electrical contact for use on a semiconductor device.” Ex. 2024 at ¶ 81. The claimed “electrode stack” includes metal layers and a capping layer. Ex. 1001 at claims 1, 13. These requirements describe particular aspects of the “electrode stack” that do not limit or otherwise alter its plain meaning. Moreover, a POSITA would have understood that the open-ended terms “comprising” and “including” means that the claimed “electrical contact” has other components besides the “electrode stack”, and the “electrode stack” may include other features not expressly claimed.

17. The independent claims also require certain materials in the capping layer and that the capping layer “thickness greater than that of a bottom most layer of said plurality of metal layers.” Ex. 1001 at claims 1, 13. But a POSITA would

have understood that those materials and thickness relationships do not change the meaning of “electrode stack.” Likewise, while the “electrical contact” of independent claim 1 is “for use on a semiconductor device” and the “electrical contact” of claim 13 is “for use on a group III-V semiconductor,” these requirements convey the context in which the electrode is implemented, but a POSITA would have understood that these different requirements do not alter the meaning of “electrode stack.”

18. The dependent claims also do not limit the term “electrode stack.” Dependent claims 2-3 require certain materials in the capping layer of the electrode stack. Claim 4 requires a particular arrangement of metal and capping layers of the electrode stack. Claims 5-7 require certain materials in the metal layers of the electrode stack. The dependent claims’ requirements for certain materials and layer arrangements do not alter the plain meaning of “electrode stack.”

19. The meaning of “electrode stack” is also not changed by the requirements in claims 8-11 or 14-16. Dependent claim 8 specifies that the “electrical contact is configured for implementation on a group III-V semiconductor device,” but this provides the context in which the “electrode stack” is implemented and does not alter its plain meaning. Claims 9 and 14 specify that the claimed III-V semiconductor device comprises a HEMT, which again describes the context and likewise does not alter the meaning of “electrode stack.” And claims 10-11 and 15-

16 implements the *electrical contact* as a particular type of electrode, namely “a power electrode making ohmic contact with said group III-V semiconductor device” (claims 10, 15), or “a gate electrode making Schottky contact with said group III-V semiconductor device” (claims 11, 16).

20. The remaining dependent claims recite “wherein said electrical contact is implemented with a gate insulator layer underlying [said/a] first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.” Ex. 1001 at claims 12, 17. This shows that the “electrode stack” of the independent claims is broader than an insulated gate electrode, which is just one example.

21. Accordingly, a POSITA would not have understood that the claims alter the plain and ordinary of “electrode stack.”

**B. The Specification Does Not Define the Term “Electrode Stack” or Disavow Its Full Scope**

22. A POSITA reading the '562 patent would not have understood it provided any special definition of the term “electrode stack” that differs from its ordinary meaning. For example, the patent uses the term “electrode” fifty-nine times. Ex. 1001 at Abstract, Fig. 3, 1:36-40, 1:46-49, 2:21-24, 2:58-60, 3:19-36, 3:40-49, 3:60-62, 4:17-20, 4:45-47, 4:56-58, 5:8-12, 5:20-32, claims 1, 5-7, 10-13, 15-17, Fig. 3. And it uses the term “electrode” in conjunction with “stack” twenty-nine times. Ex. 1001 at Abstract, 1:36-40, 1:46-49, 3:21-35, 3:40-49, 3:60-62, 4:17-20,

4:45-47, 4:56-58, 5:8-12, 5:20-22, claims 1, 5-7, 12, 13 and 17. Yet the '562 patent never once offers a definition for the term “electrode” or “electrode stack” that limits the scope of these terms.

23. Instead, when the patent describes the “electrode stack,” it uses non-limiting language that does not define the term with any precision and does not disavow scope. The patent puts no boundaries or constraints on the meaning of “electrode” or “stack” beyond their ordinary meaning. For example, the patent repeatedly describes the electrode stack as “*including* a plurality of metal layers and a capping layer formed over the plurality of metal layers.” *E.g.*, Ex. 1001 at Abstract (emphasis added), 3:46-48. It claims the “electrode stack” the same way—as “including” metal layers and a capping layer. Ex. 1001 at claims 1, 13. A POSITA reading the specification would have understood that the open-ended claim term “including” means that the electrode stack may include other features not expressly described. Thus, the specification provides no statements that alter the plain meaning of “electrode stack.”

24. Embodiments and drawings of the '562 patent are presented as examples that do not limit the meaning of “electrode stack.” The patent states Figure 1 is “an *example* group III-V semiconductor device.” Ex. 1001 at 2:43-46 (emphasis added). Likewise, Figure 2 is “a more detailed block diagram showing a refractory metal nitride capped electrical contact, according to one embodiment of

the present invention,” i.e. it refers to an example embodiment. Ex. 1001, 3:36-39, 60-62. The patent does not limit the number or type of metal layers in the electrode stack of Figures 1 and 2, instead stating “[m]oreover, the number and character of the plurality of metal layers 222, 224, and 226 of electrode stack 220 are merely exemplary.” Ex. 1001, 3:36-39, 60-62.

25. The process of Figure 3 similarly only refers to an example. Figure 3 is a flow chart “describ[ing] the steps, according to one embodiment of the present invention, of a method for fabricating a refractory metal nitride capped electrical contact.” Ex. 1001 at 4:4-8. And “[w]hile steps 310 though 360 indicated in flowchart 300 are sufficient to describe one embodiment of the present invention, other embodiments of the invention may utilize steps different from those shown in flowchart 300.” Ex. 1001, at 4:12-16. The patent is not limited to this method of fabrication, and the claimed electrical contacts could be made with other methods known to a POSITA.

26. Moreover, the ’562 patent broadly states: “[a]lthough the present inventive concepts are described with respect to specific embodiments, the principals of the invention, as defined by the claims appended herein, can obviously be applied beyond the specifically described embodiments of the invention described herein.” Ex. 1001, at 2:25-28. And the patent confirms that “[i]t should be understood that particular details such as ... the semiconductor device represented

by structure 100, for example, are provided for conceptual clarity and should not be interpreted as limitations.” Ex. 1001, at 3:46-52. This means that, in addition to the specific examples of “electrode stacks” provided in the specification and figures, other types of electrode stacks fall within the scope of the disclosure.

27. For at least these reasons, a POSITA would have understood that the drawings and description do not confine the claimed term “electrode stack” do not alter its plain meaning.

## **VII. DR. PINER PROPOSES AN UNJUSTIFIED, OVERLY NARROW DEFINITION OF ELECTRODE STACK**

28. I disagree with Dr. Piner’s opinion that an “electrode stack” is:

“a stack of conductive layers that forms an electrical contact that is part of a semiconductor device and used to (1) establish contact with a nonmetallic part of the semiconductor device (like the source, drain and Schottky gate electrodes in the ’562 Patent Specification) or (2) controls the operation of the semiconductor device (like the insulated or Schottky gate electrodes in the ’562 Patent Specification).”

Ex. 2024 at ¶ 91. He purports to rely on (1) intrinsic evidence from the claims, specification, and figures and (2) an extrinsic dictionary definition. Ex. 2024 at ¶¶ 81-95. But the evidence does not support his opinion. I address the intrinsic and extrinsic evidence in turn, below.

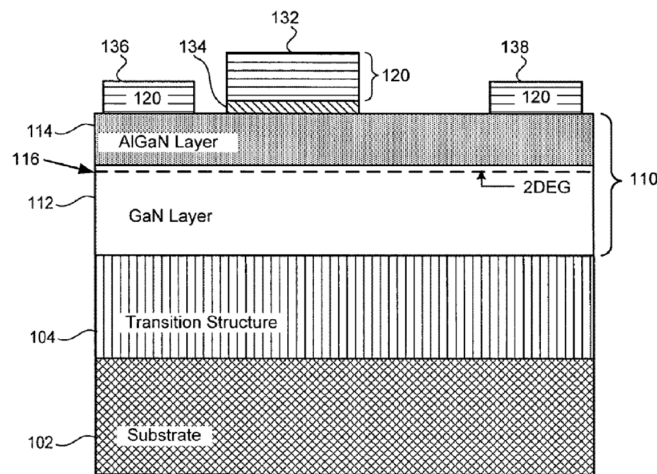
**A. Dr. Piner Imports Examples From the Specification Into the Claims to Narrowly Construe “Electrode Stack”**

29. Dr. Piner’s construction inappropriately adds limitations to the claims that only appear in example embodiments from the specification. Ex. 2024 at ¶¶ 81-91. As I explained above, the specification gives no definition and makes no disclaimer which would alter the plain and ordinary meaning of an “electrode” or “electrode stack” as understood by a POSITA. Section VI.

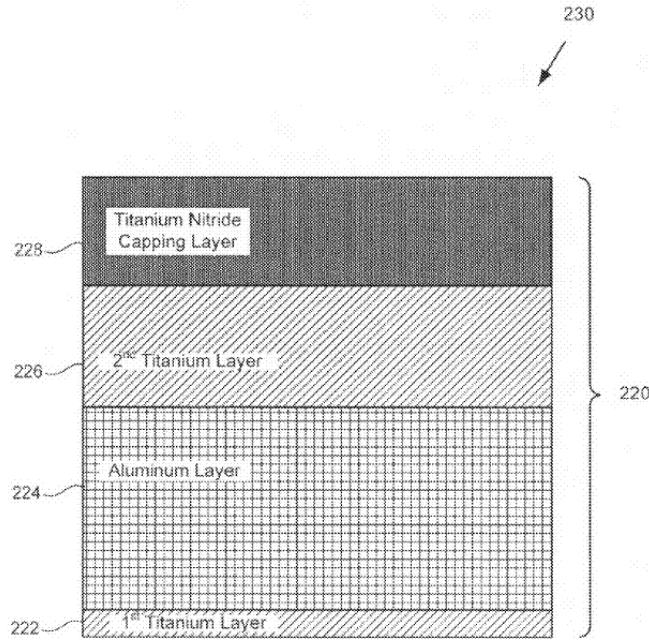
30. Dr. Piner apparently roots his construction on the mistaken premise that the claimed “electrical contact” is the “electrode stack.” Ex. 2024 at ¶ 82. He states the patent “links the terms ‘electrical contact’ and ‘electrode’, by describing the electrical contact for use on a semiconductor device *as an electrode of the device.*” Ex. 2024 at ¶ 82 (emphasis original). He contends that “when the claims recite an ‘electrode stack,’ it is in the context of the electrical contact implemented as an electrode of the semiconductor device.” Ex. 2024 at ¶ 82. Dr. Piner inaccurately conflates the terms “electrical contact” and “electrode stack” because he believes the “electrical contact” is only ever “implemented” as an “electrode.” Ex. 2024 at ¶ 82, *see, e.g.*, Ex. 2024 at ¶¶ 39 (“source/drain electrode implementations of the electrical contact”), 40 (“gate electrode implementations of [the patent’s] electrical contact”), 41 (“insulated gate electrode implementation of the electrical contact”), 42 (“Schottky gate electrode implementation of the disclosed electrical contact”).

31. But neither the claims nor the specification equate “electrical contact” and “electrode stack,” as Dr. Piner suggests. It is my understanding that different terms have different meanings. Dr. Piner’s analysis overlooks that independent claims 1 and 13 use the open-ended language “electrical contact *comprising*: an electrode stack,” so the electrical contact may include other components and is not simply “implemented” as an “electrode stack.” *See* Section VI.A.

32. Dr. Piner relies on the examples of Figures 1 and 2 to attempt to (i) limit the scope of the term “electrode stack” to just three types of electrodes and (ii) to require either direct contact between a metal layer and a semiconductor or a thin insulating material between a metal layer and a semiconductor. The claims are not limited by these examples. Section VI.



'562 Patent, Fig. 1.



'562 Patent, Fig. 2.

33. Dr. Piner refers to those example figures and their accompanying description in the specification to contend the claimed “electrode stack” must only be one of three specific “electrode types”: “(1) a ‘power electrode []’ that touches and is ‘*ohmically coupled*’ to the nonmetallic semiconductor (EX – 1001, 3:19-28, 1:33-43), (2) a transistor gate electrode that controls the flow of electrons or holes through the transistor that touches and makes ‘Schottky contact’ with the nonmetallic semiconductor (*id.*, 3:31-35), and (3) a transistor gate electrode that controls the flow of electrons or holes through the transistor but is ‘an insulated gate electrode’ that is separated from the semiconductor by an insulating layer 134 (*id.*, 3:21-33).” Ex. 2024 at ¶ 90 (emphasis original), *see* Ex. 2024 ¶¶ 83-90 (analyzing Figures 1 and 2). This analysis imports limitations from the specification into the

term “electrode stack” by limiting it to an ohmic contact, a Schottky gate, or an insulated gate. He also imports the examples of Figures 1 and 2 and accompanying text into the claims to contend the “electrode stack” must either (1) “touch” (i.e., make direct contact with) the nonmetallic portion of the semiconductor device (*see* Ex. 2024 at ¶¶ 69, 90, 145, 149), or (2) have thin insulative material between metal and semiconductor as in an insulated gate (*see* Ex. 2024 at ¶¶ 85, 88, 90, 149).

34. I disagree with Dr. Piner. The claims and specification do not alter the ordinary meaning of “electrode stack.” *See* Section VI. Figures 1 and 2 are only examples that do not compel Dr. Piner’s construction. *E.g.*, Ex. 1001 at 2:6-9 (stating Figure 1 shows “one embodiment”), 2:10-12 (stating Figure 2 shows “one embodiment”), 2:43-46 (Figure 1 is an “embodiment”), 3:1-3 (“the present embodiment” of Figure 1), 3:36-38 (Figure 2 is “an embodiment”), *see* Section VI.B. Regarding Figure 1, the patent expressly states that “particular details such as the materials used to form structure 100 and the semiconductor device represented by structure 100, for example, are provided for conceptual clarity and should not be interpreted as limitations.” Ex. 1001 at 3:46-52. And the electrode stack of Figure 2 “corresponds” to Figure 1. Ex. 1001 at 3:36-45.

35. Thus, contrary to Dr. Piner’s assertions, a POSITA would have understood that the term “electrode stack” does not only refer to the structures

specifically depicted in Figures 1 and 2. Ex. 2024 at ¶¶ 81-91. It is broader and should be afforded the full scope of its plain meaning.

**B. The Extrinsic Record Does Not Support Dr. Piner's Narrow Interpretation of "Electrode Stack"**

36. Dr. Piner argues that he articulates the proper construction of "electrode stack" because he believes it is "consistent with" a definition from a general-purpose Merriam-Webster's Collegiate Dictionary that he provides. Ex. 2024 at ¶¶ 92-96. That dictionary defines an "electrode" as:

1: a conductor used to establish electrical contact with a nonmetallic part of a circuit

2: an element in a semiconductor device (as a transistor) that emits or collects electrons or holes or controls their movements

Ex. 2001 at 371. I disagree that this definition is the appropriate definition of electrode. It does not show Dr. Piner's construction of "electrode stack" is correct.

37. Dr. Piner's carefully curated definition is incomplete and does not limit the scope of the claimed "electrode stack." Dr. Piner does not explain why this specific, general-purpose definition should be accorded any weight. As I explained above, the intrinsic evidence does not support Dr. Piner's narrow construction, and it is my understanding that a dictionary is extrinsic evidence, which carries less weight for claim construction than the intrinsic evidence. Section VI. Yet Dr. Piner attempts to use this dictionary definition to narrow the plain meaning of "electrode stack" when the patent itself does not require such narrowing.

38. Moreover, a POSITA would have understood that Dr. Piner's general-purpose English definition is incomplete. A technical definition from the relevant time, for example, does not comport to the narrow confines of that definition. The Wiley Electrical Electronics Engineering Dictionary defines "electrode" as:

A conductor which serves to deliver, receive, collect, emit, deflect or control electric charge carriers. An electrode provides the path for current entering or leaving a medium such as a dielectric, electrolytic solution, semiconductor, gas, or vacuum. ... It is often a metal, and may consist for instance, of a wire, grid, plate or region.

Ex. 1046 at 237. This does not limit an electrode to "establish[ing] electrical contact with a nonmetallic part of a circuit," as Dr. Piner's definition requires. *Compare* Ex. 1046 at 237 *with* Ex. 2001 at 371. It does not require a metal-semiconductor junction. Ex. 1046 at 237. And it does not limit "electrode" to an "element in a semiconductor device (as a transistor) that emits or collects electrons or holes or controls their movements" *Compare* Ex. 1046 at 237 *with* Ex. 2001 at 371. Instead, the Wiley technical definition more broadly describes that electrodes "deliver, receive, collect, emit, deflect or control electric charge carriers" and provide a current path, which is consistent with how a POSTIA would have understood the term "electrode."

39. Further, there are other examples extrinsic to the '562 patent that contradict Dr. Piner's construction. A POSITA would have understood that not every electrode is a source contact, drain contact, Schottky gate, or insulated gate.

For example, many references from the relevant time describe “interconnect electrodes” in semiconductor devices. Ex. 1038 at [0013], [0026], [0084], [0085], [107], Figs. 1-2, 10-11, Ex. 1039 at 449, Ex. 1040 at 1:42-45, 2:1-4, 2:9-19, 2:28-34, Ex-1041 at [0233], Fig. 45, Ex-1042 at 7:44, 9:47-50, Fig. 1B. Thus, the extrinsic evidence does not support Dr. Piner’s narrow construction.

### **VIII. USUI’S STRUCTURE IS AN ELECTRODE STACK UNDER THE PLAIN AND ORDINARY MEANING AND UNDER DR. PINER’S CONSTRUCTION**

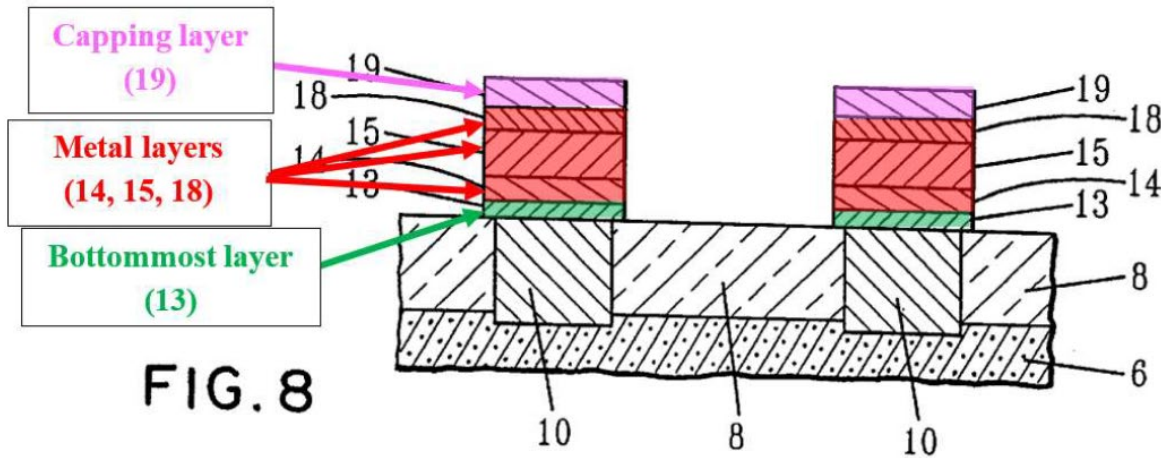
40. As I previously opined, Usui (Ex-1004) discloses an “interconnect” that is an “electrode stack” under its plain meaning (Ex-1002 at ¶¶ 89-91), and it is my opinion that this structure meets even Dr. Piner’s narrow construction. Dr. Piner’s contrary arguments fail. Ex. 2024 at ¶¶ 144-153.

#### **A. Usui Discloses an Electrode Stack that is Part of a Semiconductor Device and used to (1) Establish Contact with a Nonmetallic Part of the Semiconductor Device**

41. As shown below, Usui’s interconnect includes a stack of conductive layers that contacts a nonmetallic part of the semiconductor device in two ways—physically and electrically.

42. First, Usui’s figures plainly show *physical contact* between the underlayer 13 and insulator 8, consistent with Dr. Piner’s construction of “electrode stack.” Usui, Figs. 1-8. The interconnect includes the capping layer (19), metal layers (14, 15, and 18) and underlayer (13) which form an electrode stack under Dr.

Piner's construction. Usui, 3:23-4:15. Underlayer 13 is a metal layer that may be sputter deposited on insulator 8, which is a non-metallic part of the semiconductor device. Usui, 5:11-33, 5:49-52, Figs. 1-8.



Usui, Fig. 8 (annotated).

43. Usui's structure has a substantial area of physical contact between underlayer 13 and insulator 8. This is because "contact stud 10" is not a layer, it is an interplanar conductive via that cuts across device layers, which I explained during my deposition. Usui at 3:24-27, 5:11-13, Figs. 1-8; Ex. 2026 at 10:6-8,12:2-7, 32:6-13, 33:1-6, 34:1-8, 37:9-14, 40:10-14, 42:4-10, 43:7-18, 76:17-20, 76:23-77:1, 77:16-18, 79:15-17, 79:22-80:9. A conductive via is a filled hole, which is typically a much smaller structure than the surrounding layers and structures. Ex. 2026 at 50:13-14, 51:11-12, 51:18-23, 10:6-8,12:2-7, 32:6-13, 33:1-6, 34:1-8, 37:9-14, 40:10-14, 42:4-10, 76:16-18, 77:18-21, 79:13-15. As shown in Figures 1 and 8 of

Usui, stud 10 comprises a total cross-sectional length which is less than a total cross-sectional length of the electrode stack.

44. Second, Usui's interconnect metallization structure meets Dr. Piner's construction of "electrode stack" because it establishes *electrical contact* with the nonmetallic semiconductor wafer layer 6. Dr. Piner does not dispute that an interconnect provides electrical connections between semiconductor components. Ex. 2024 at ¶¶ 63, 147-148. Dr. Piner notes "[i]nterconnects are **deposited on insulators and touch the active devices**" and are made [of] multiple levels of metal lines and connecting vias "serve as the wiring between semiconductor devices, such as transistors." Ex. 2024 at ¶ 63 (quoting Ex. 1011 (emphasis original)). There, Dr. Piner shows he understands that interconnects electrically connect to semiconductor layers. Indeed, Usui explicitly makes this point, stating that its metallization structure "preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 *to make connection to* a device substrate 6." Usui at 3:24-27 (emphasis added).

45. Dr. Piner nevertheless contends that the metallization structure does not establish contact with the semiconductor layer 6 because the electrical connection between the metallization structure and semiconductor is *indirect* through stud layer 10. Ex. 2024 at ¶¶ 149-151. Here, Dr. Piner inappropriately construes his own construction to impose further requirements—an electrode stack needs *direct* contact

with a nonmetallic part of the device. A construction should add clarity, not create confusion by requiring further interpretation of its terms.

46. In support of his further construction to require *direct* contact between an electrode stack and non-metallic component, Dr. Piner again advances his flawed contention that the claims require an ohmic contact, Schottky contact, or insulated gate contact. Ex. 2024 at ¶¶ 149-150. But as I have already shown, the intrinsic record does not support that position. *See* Sections VI, VII.A. The word “direct” is nowhere found in the patent, and there are no statements requiring the electrode stack to make direct electrical contact with a non-metallic part of the semiconductor. Ex. 1001.

47. Although Dr. Piner references his curated, general purpose dictionary definition of “electrode” for support (Ex. 2024 ¶¶ 150-151), this is misplaced. *See* Section VI.B. Nothing in the first part of the definition, the requirement to make electrical contact with a nonmetallic part of the circuit, states or suggests an electrode must make *direct* electrical contact. Ex. 2001 at 371. The word “direct” is not present in that definition. Ex. 2001 at 371. The definition only says an electrode “*establish[es]* electrical contact with a nonmetallic part of the circuit,” and a POSITA would have understood this to include establishing indirect and direct forms of electrical contact. Ex. 2001 at 371. Indeed, a POSITA would have understood that electrical connections include indirect connections, as was found in

the prior art. Usui's metallization structure "make[s] connection to" semiconductor layer 6 through the conductive via (i.e., stud 10). Usui at 3:24-27. Yu (Ex-1005), another prior art reference, similarly describes indirect electrical contacts that include interconnects. Yu, ¶ [0087] ("various contacts/vias and multilayer interconnect features (e.g., metal layers and interlayer dielectrics) may be formed on the substrate 610 and configured to connect the various features or structures of the semiconductor device 600."), [0111] (same).

48. Regarding the second part of the general-purpose definition, as I have already explained, this definition is incomplete. Section VI.B. Dr. Piner's contention that Usui's device is not an electrode because it does not emit or collect electrons or holes or control their movements is wrong. Ex. 2024 at ¶ 151. Instead, Usui's interconnect is "[a] conductor which serves to deliver, receive, collect, emit, deflect, or control electric charge carries" and "provides the path for current entering or leaving a medium," consistent with the technical definition of "electrode" that I provided. Ex. 1046 at 237.

**B. Usui's Electrode Stack (2) Controls the Operation of the Semiconductor Device**

49. Dr. Piner does not explain what he means by "control," when he construes electrode stack as something that "controls the operation of the semiconductor device." Ex. 2024 at ¶¶ 81-91. The word "control" is not a claim term and does not appear anywhere in the '562 patent. Ex. 1001. Dr. Piner's construction

thus creates further confusion by requiring further interpretation of its terms. Nevertheless, it is my opinion that a POSITA would have understood “controls the operation” to involve at least enabling or influencing current flow.

50. In my opinion, Usui’s interconnect controls the operation of the semiconductor device and therefore satisfies Dr. Piner’s construction. As Dr. Piner himself acknowledges, an interconnect provides electrical connections between devices. Ex. 2024 at ¶¶ 63-65, 147-148. Such functionality controls the operation of a semiconductor device by enabling and influencing current flow through the semiconductor. Interconnects “provide low resistance paths for current.” Ex-1011 at 218. It would not be possible for an integrated circuit to function without the use of interconnects.

51. Furthermore, Usui discloses its interconnect metallization improves electromigration performance, which results in longer times to failure. Ex. 1004 at Abstract, 3:54-57, 4:57-5:10, Figs. 9-10. This is another way the metallization structure “controls” Usui’s semiconductor device. Usui describes electromigration as the migration of atoms into a semiconductor surface, a problem that impairs operation of the device because it “can interfere with the performance and reliability of the resulting integrated circuit structure.” Ex. 1004 at 1:30-35. Dr. Piner recognizes that electromigration was caused by “[a] current induced mass transport... wherein atoms of [a] conductor material are displaced as a result of the

combined effects of direct momentum exchange from the moving electrons and the influence of the applied electric field.” Ex. 2024 at ¶ 66, *see* Ex. 1024 at ¶¶ 100, 218. Because Usui’s metallization structure improves electromigration, it shapes current characteristics, so it controls operation of the semiconductor device.

**C. While Applying his Construction of “Electrode Stack” to Usui, Dr. Piner Also Incorrectly Construes “Semiconductor Device” And “Electrical Contact”**

**1. Without support, Dr. Piner attempts to exclude structures that electrically connect other devices from the claimed “semiconductor device”**

52. To argue that Usui’s metallization structure does not meet the proper construction of “electrode stack,” Dr. Piner attempts to construe “semiconductor device” to exclude interconnect metallization structures based on their function. He incorrectly asserts that “Usui’s interconnect metallization structure is not an element of the semiconductor device at all” because it connects two devices. Ex. 2024 at ¶ 151. But he cites no evidence in the ’562 patent that a semiconductor device cannot include such metallization structures merely because they electrically contact other devices. The patent claims a “semiconductor device” (claims 1, 13) without altering its meaning and does not limit the “electrical contact” or “electrode” to exclude structures connect to other devices. *See* Section VI.

53. Dr. Piner cannot find support because prior art contradicts his position. Prior art references described interconnects as part of a semiconductor device. For

example, a prior art patent publication describes an interconnect structure is part of an IC chip (semiconductor device) and claims a “semiconductor device structure comprising: a substrate ... [and] a metal line,” where the substrate can be a semiconductor and the metal line is part of an interconnect. Ex.1044 at ¶¶ [0009], [0029], claim 11. Another is directed to “manufacturing interconnects *in* a semiconductor device,” which shows the interconnect is a component of the semiconductor device. Ex. 1045 at ¶ [0007] (emphasis added). It discusses “semiconductor device interconnect” as part of a semiconductor device and which includes semiconductor substrate layer. Ex. 1045 at ¶¶ [0003]-[0010], [0016], [0020], [0031], claims 1-8. Yu (Ex-1005) similarly explains interconnects connect internal features of a semiconductor device. Yu, [0040], [0063] (same), [0087] (same). A relevant textbook similarly discusses interconnects “in semiconductor technology.” Ex-1011 at 217-218 (emphasis added).

54. Moreover, Dr. Piner’s argument that the interconnect is separate from the semiconductor device contradicts Usui’s disclosure. Usui describes a semiconductor device that includes the “interconnect metallurgy structure” (layers 13-15, 18, and 19) and “semiconductor wafer 6,” which are formed as one device through a sequence of deposition, masking, and etching steps. Usui, 3:23-4:10, Figs. 1-8. That device has a semiconductor layer, so it is a semiconductor device.

**2. Dr. Piner implausibly construes “electrical contact” to require a metal-semiconductor junction**

55. Dr. Piner repeatedly contends electrical contacts of the '562 patent require a metal-semiconductor junction, not a metal-metal connection. Ex. 2024 at ¶¶ 62-71, 100, 102, 136. Although Dr. Piner recognizes that “metal-metal electrical connections” were “conventional” and “known,” he contends they are not within the scope of the '562 patent’s “electrical contact.” Ex. 2024 at ¶¶ 62, 102, 136. In support, he advances the same flawed argument I have already addressed, alleging that “generally an interconnect does not have a metal-semiconductor junction like an ohmic contact or gate contact and therefore would not have been confused with an electrical contact.” Ex. 2024 at ¶ 62, *see* Section VI-VII.

56. This is incorrect for two reasons. First, as I already demonstrated, the claimed “electrode stack” does not require a metal-semiconductor junction, so the broader “electrical contact comprising: an electrode stack” does not require a metal-semiconductor junction either. Sections VI-VII. Second, this argument inexplicably excludes metal-metal junctions without support from the patent itself. Dr. Piner recognizes that metal-metal contacts are electrical contacts, but nonetheless seeks to exclude them from the claimed electrical contact. Ex. 2024 at ¶¶ 62, 102, 136. He has no support to do so. The patent does not provide a definition of “electrical contact” that excludes metal-metal contacts. *See generally* Ex. 1001. Instead, the patent

provides non-limiting examples of electrical contacts. Ex. 1001 at 2:43-46, 3:36-39, 60-62, Figs. 1-2. It never indicates metal-metal contacts are not “electrical contacts.”

**3. Dr. Piner inappropriately contends the claimed “electrical contact” cannot include an interconnect because he incorrectly alleges the claims exclude components that experience electromigration**

57. Dr. Piner incorrectly construes “electrical contact” and “electrode” as recited in the claims to exclude interconnects. For example, he argues “electromigration [is] a problem specifically associated with aluminum-based interconnects, and not associated with *electrical contacts having an electrode stack* as described and claimed by the ’562 Patent.” Ex. 2024 at ¶ 134. He contends “a POSA [would not] understand the problems/solutions regarding electromigration in aluminum interconnects be reasonably pertinent to problems addressed by the ’562 patent because ... electromigration is a particular issue with metal interconnects relating to the combined currents from many devices, and not for electrical contacts for use on a semiconductor device.” Ex. 2024 at ¶ 104; *see* Ex. 2024 at ¶¶ 66-68 (discussing electromigration in interconnects), 99-105 (discussing electromigration in Usui’s device). 158-176. This inaccurate analysis leads him to wrongly conclude that “electrodes” of the ’562 patent do not implicate electromigration concerns so he implicitly construes “electrical contact” and “electrode” to exclude an interconnect. Ex. 2024 at ¶¶ 99-105, 134, 138, 148, 161, 169-176, 181-182, 189, 195, 201-202, 210, 217-222, 270-273. I disagree for several reasons.

58. First, Dr. Piner once again imposes limitations on the claims that are not there. The claims do not recite that its “electrical contact” or “electrode stack” is a component that does not experience electromigration. And the specification nowhere states that an electrode stack cannot experience electromigration—it does not discuss electromigration at all.

59. Second, a POSITA would have understood the ’562 patent’s device to experience electromigration, which generally arises at high current density. As one reference describes:

Metal migration [electromigration] is the physical movement of metal in a conductor caused by current flow. Electron scattering from metallic atoms literally pushes these atoms in the direction of current flow. Metal can be depleted from one part of the conductor and accumulate at a nearby part. At the depletion site, the cross-sectional area of the conductor is reduced. This increases the current density, which increases the effect even more and can lead to the burnout at the thin portion of the conductor.

Ex. 1021 at 7-8. As this reference explains, current flow causes electromigration, meaning that higher current densities lead to more electromigration. Dr. Piner agrees that electromigration typically occurs at relatively high current densities. Ex. 2024 at ¶100. A POSITA would therefore expect at least some electromigration in the devices of the ’562 patent, including HEMT power transistors.

60. Dr. Piner's statements to the contrary are incorrect. In fact, a prior art Infineon patent identifies that electrodes of semiconductor transistors experience electromigration. Ex.1043 (U.S. Patent No. 9,633,951 (B2) ("Pavier"))<sup>1</sup>. It states:

As a demand for improved performance and reduction in the cost of semiconductor devices such as power semiconductor devices increases, the size of semiconductor devices decreases while the performance thereof increases. . . . Consequently, it is expected that as the die size decreases the electrodes thereof that make external connection via, for example, a solder body will also decrease in size while *the current passed therethrough will increase*.

It is believed that the reduction in the size of the electrodes combined with an increase in the current load passing through the electrode and its solder connection, particularly in the presence of high switching frequencies, may result in high than desirable failure rate in the solder connection due, for example, to *electromigration* or the like phenomenon."

Ex. 1043 at 1:17-36 (emphases added). This passage describes electromigration between electrodes of a semiconductor power transistor and its external connections due to high current through the electrodes. And the electrodes described in this Infineon patent, which purportedly benefit from the improved electromigration characteristics it seeks, include "power electrode 14 (e.g., source electrode or emitter

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<sup>1</sup> I understand that U.S. 9,633,951 (B2) as filed November 10, 2006, making it prior art to the '562 Patent, which has an earliest claimed priority date of August 25, 2009. This patent is assigned to Infineon Technologies Americas Corp., which, by its name, appears to be related to Patent Owner (Infineon Technologies Austria AG).

electrode) and control electrode 16 (e.g., gate electrode), respectively.” Ex. 1043 at 2:39-61, Fig. 1. As this Infineon patent shows, Dr. Piner is simply wrong that Usui’s interconnect is not an “electrode stack” because it experiences electromigration. Instead, as this patent shows, a POSITA would have understood that electrodes would receive the electromigration benefits that Usui describes, as I discussed in my first declaration and deposition. Ex. 1002 at ¶¶ 73, 84, 101, 113-114, 118-119, 121-122, 131, 133, 144, 176, 179; Ex. 2025 at 12:18-14:20, 16:5-17:6, 54:2-56:25. A POSITA would have understood that one purpose of the barrier layer described in the patent is to improve electromigration. Ex. 2025 at 54:2-56:25.

61. The ’562 patent claims and describes a HEMT power transistor, which often has high current flows and current densities, including in their ohmic contacts. Ex. 1001 at 2:53-65, claims 9, 14. Dr. Piner fails to explain why the HEMT power devices of the ’562 patent would not experience electromigration. As I explained above, a POSITA would have appreciated electromigration is indeed a concern for such devices, and the electrical contact of the ’562 patent would have experienced electromigration.

62. Furthermore, it was known that gate leakage can cause electromigration in gate electrodes. Leakage turns the gate from a voltage only node into a current-carrying conductor. Ex. 1018 at 937. Once sufficiently high current flows in the gate metal, the basic conditions for electromigration are met. This is especially

problematic for gate electrode forming a Schottky connection because Schottky gates do not feature an insulating oxide to block current, and leakage increases exponentially with voltage and temperature. Ex. 1015 at 353-354. Thus, it is common and well known to make fabrication decisions preventing gate leakage as well as minimizing the effects of electromigration.

63. A POSITA would have recognized the problem of electromigration was not limited to interconnects and would have arisen in devices of the '562 patent. The claimed "electrical contact" and "electrode" do not exclude components that experience electromigration.

## **IX. CONCLUSION**

64. For the reasons set forth above, it is my opinion that one skilled in the art would have found the '562 patent to adequately and clearly define the plain and ordinary meaning of the term 'electrode' and 'electrode stack' without the need to import additional limitations from the specification as filed or the use of extrinsic evidence.

65. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the

United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

66. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: December 21, 2025

Respectfully submitted,

A handwritten signature in cursive script, appearing to read 'Yuji Zhao', is written above a horizontal line.

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Yuji Zhao, PhD