

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AUSTRIA AG,
Patent Owner.

IPR2025-00175
U.S. Patent 8,686,562

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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TABLE OF EXHIBITS

Exhibit	Description
Ex-1001	U.S. Patent No. 8,686,562 (“the ’562 patent”)
Ex-1002	Expert Declaration of Dr. Yuji Zhao (“Zhao”)
Ex-1003	Curriculum Vitae of Dr. Yuji Zhao
Ex-1004	U.S. Patent No. 5,943,601 to Usui et al. (“Usui”)
Ex-1005	U.S. Patent Publication No. 2010/0052066 to Yu et al. (“Yu”)
Ex-1006	U.S. Patent Publication No. 2008/0023726 to Adesida et al. (“Adesida”)
Ex-1007	U.S. Patent No. 7,777,252 to Sugimoto et al. (“Sugimoto”)
Ex-1008	Pearton et al., <i>Gallium Nitride Processing for Electronics, Sensors and Spintronics</i> , Springer, 10.1007/1-84628-359-0. (2006)
Ex-1009	Adachi, <i>Properties of Group-IV, III–V and II–VI Semiconductors</i> , John Wiley & Sons, Ltd, 10.1002/0470090340 (2005)
Ex-1010	U.S. Patent Publication No. 2007/0164321 to Sheppard et al. (“Sheppard”)
Ex-1011	Mishra et al., <i>Semiconductor Device Physics and Design</i> , Springer (2008)
Ex-1012	Wu et al., <i>Very-High Power Density AlGaIn/GaN HEMTs</i> , IEEE Transactions on Electronic Devices, Vol. 48, No. 3, March 2001
Ex-1013	Quay, <i>Gallium Nitride Electronics</i> , Springer, 10.1007/978-3-540-71892-5. (2008)
Ex-1014	Mishra et al., <i>AlGaIn/GaN HEMTs—An Overview of Device Operation and Applications</i> , Proceedings of the IEEE, Vol. 90, No. 6, June 2002
Ex-1015	Neaman, <i>Semiconductor Physics and Devices</i> , 3 rd edition (2002)

Exhibit	Description
Ex-1016	Voss, <i>Thermally Stable Ohmic and Schottky Contacts to GaN</i> , University of Florida, 2008
Ex-1017	Krämer, <i>Fabrication and characterization of metal-semiconductor contacts for application in $Al_xGa_{1-x}N/GaN$ HEMTs</i> , (Oct. 31, 2000)
Ex-1018	Kuzmick et al., <i>Technology and Performance of InAlN/AlN/GaN HEMTs With Gate Insulation and Current Collapse Suppression Using ZrO_2 or HfO_2</i> , IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 55, No. 3, Mar. 2008
Ex-1019	Wu et al., <i>Aluminum, magnesium, and gold contacts to contamination free n-GaN surfaces</i> , Journal of Applied Physics, Vol. 89, No. 1, Jan. 1, 2001
Ex-1020	Foresi et al., <i>Metal contacts to gallium nitride</i> , Appl. Phys. Lett., Vol. 62, No. 22, May. 31, 1993
Ex-1021	Kayali et al., <i>GaAs MMIC Reliability Assurance Guideline for Space Applications</i> , JPL Publication 96-25, Dec. 15, 1996
Ex-1022	U.S. Patent Publication No. 2009/0250816 to Chin et al. (“Chin”)
Ex-1023	U.S. Patent No. 7,335,590 to Suh et al. (“Suh”)
Ex-1024	U.S. Patent No. 6,607,976 to Chen et al. (“Chen”)
Ex-1025	Excerpts from Bauccio, Michael, <i>Refractory Metals</i> , ASM Metals Reference Book, ASM International, American Society for Metals, ISBN 978-0-87170-478-8, (1993)
Ex-1026	Preuss, <i>Finer Copper Wires Make for Faster Integrated Circuits</i> , Berkeley Lab, https://www2.lbl.gov/Science-Articles/Archive/integrated-circuits-copper.html , Apr. 5, 1999
Ex-1027	Cockeram, <i>The Diffusion Bonding of Silicon Carbide and Boron Carbide Using Refractory Metals</i> , USDOE Contract No. DE-AC11-98PN38206, Nov. 22, 1999

Exhibit	Description
Ex-1028	Kim, <i>Atomic Layer Deposition of Metal and Nitride Thin films: Current Research Efforts and Applications for Semiconductor Device Processing</i> , RC22737 (W0303-012), Mar. 5, 2003
Ex-1029	U.S. Patent No. 6,844,258 to Fair et al. (“Fair”)
Ex-1030	U.S. Patent No. 4,980,752 to Jones, Jr. (“Jones”)
Ex-1031	U.S. Patent No. 5,635,763 to Inoue et al. (“Inoue”)
Ex-1032	U.S. Patent No. 6,646,352 to Ohmi et al. (“Ohmi”)
Ex-1033	Order Staying and Conditionally Closing Case, 4-24-cv-01553
Ex-1034	Excerpts from Prosecution History of the ’562 Patent
Ex-1035	Excerpts from Rooy, Introduction to Aluminum and Aluminum Alloys
Ex-1036	Pierson, The Refractory Nitrides
Ex-1037	Order Construing Certain Claim Terms, Inv. No. 337-TA-1414
Ex-1038	U.S. Patent Application Publication No. 2006/0124954 to Akaishi (“Akaishi”)
Ex-1039	Songyuan Dai et al., <i>Design of DSC panel with efficiency more than 6%</i> , Solar Energy Materials & Solar Cells 85 (2005) 447–455
Ex-1040	U.S. Patent No. 5,940,732 to Zhang (“Zhang”)
Ex-1041	U.S. Patent Application Publication No. 2007/0210350 to Omura et al. (“Omura”)
Ex-1042	U.S. Patent No. 7,381,993 to Uchida et al. (“Uchida”)
Ex-1043	U.S. Patent Application Publication No. 2007/0108585 to Pavier et al. (“Pavier”)
Ex-1044	U.S. Patent Application Publication No. 2006/0258143 to Kuo (“Kuo”)

Exhibit	Description
Ex-1045	U.S. Patent Application Publication No. 2007/0190803 to Singh et al. (“Singh”)
Ex-1046	<i>Wiley Electrical and Electronics Engineering Dictionary</i> (excerpt) 2004
Ex-1047	Supplemental Declaration of Yuji Zhao, Ph.D.

*Emphasis added unless otherwise noted.

I. Introduction

Patent Owner's theory of nonobviousness for Grounds 1-4 hinges on an unsupported claim construction of "electrode stack." In an attempt to exclude Usui's metallization structure, Patent Owner relies on examples in the specification to propose an unjustified, overly narrow definition when the plain and ordinary meaning of the term applies. *Laitram Corp. v. NEC Corp.*, 163 F.3d 1342, 1347 (Fed. Cir. 1998). Regardless, Usui (Ex-1004) meets that narrow construction, and Patent Owner's defense fails.

Patent Owner repeatedly mischaracterizes the Petition's combinations of Grounds 2-4 in its attempts to save the claims, mixing the teachings of the references in ways never described by Petitioner. Paper 17 (POR), 31-34, 42-43. Those nonresponsive arguments do not rebut the Petition. Any further rebuttal is forfeited. *Google LLC v. UNILOC 2017 LLC*, IPR2020-00447, Paper 24, at 8 (P.T.A.B. May 11, 2021).

Regarding the Yu Grounds, Patent Owner cannot save the claims when Yu at [0036] discloses or at least rendered obvious a refractory metal capping layer with a thickness from 50-1000Å, thicker than the 20Å bottommost metal layer (Ground 5). And Patent Owner again mischaracterizes the combinations of Grounds 6-7.

Patent Owner's legally and factually

II. The Plain and Ordinary Meaning of an Electrode Stack Applies

Patent Owner's nonobviousness defense for Grounds 1-4 hinges on an unsupported claim construction. POR, 11, 21-22. Although it is a "well-established principle that a court may not import limitations from the written description into the claims," that is exactly what Patent Owner does. POR, 4-9; Ex-1047, ¶¶28-35; *Laitram*, 163 F.3d at 1347 ("[C]laims are not to be interpreted by adding limitations appearing only in the specification"); *Rex Med., L.P. v. Intuitive Surgical, Inc.*, 156 F.4th 1289, 1302 (Fed. Cir. 2025) ("This court will not countenance the importation of claim limitations from a few specification statements or figures into the claims"). Patent Owner seeks to limit the meaning of "electrode stack" to three example electrodes given in the specification: an ohmic contact, a Schottky contact, or an insulated gate. POR, 8-9. Neither the claims nor the specification support that construction. The plain meaning of "electrode stack" applies.

A. The Claims Do Not Limit the Term "Electrode Stack" Beyond Its Plain and Ordinary Meaning

Nothing in the claims limits the term "electrode stack" beyond its plain meaning. Ex-1047, ¶¶15-27. Independent claims 1 and 13 recite an "electrical contact comprising: an electrode stack including plurality of metal layers and a capping layer." Ex-1001. As Dr. Piner agrees, "the electrode stack is at least a part of an electrode in the electrical contact for use on a semiconductor device." Ex-2024, ¶ 81. Nothing here limits or otherwise alter the plain meaning of "electrode stack,"

and the open-ended terms “comprising” and “including” means other components may be part of the “electrical contact” and “electrode stack.”

The independent claims also require certain materials and cap dimensions, and they call for “use on a [group III-V] semiconductor,” but none of those requirements alter the meaning of “electrode stack.” Ex-1047, 17; Ex-1001, claims 1, 13. Likewise, the dependent claims specific requirements for certain materials and layer arrangements in the electrode stack, for implementation as particular types of contacts and devices, do not limit the plain meaning of “electrode stack.” Ex-1047, ¶18. In fact, the dependent claims implement the broader term “*electrical contact* as” an ohmic contact (claims 10, 14) or Schottky contact (claims 11, 15), which does not specifically require the “electrode stack” makes ohmic or Schottky contact much less limit its the plain meaning. Ex-1047, ¶19; *see SimpleAir, Inc. v. Sony Ericsson Mobile Commc’ns AB*, 820 F.3d 419, 431 (Fed. Cir. 2016) (“Different claim terms are presumed to have different meanings.” (citation omitted)). Similarly, claims 12 and 17 implement the electrical contact with a gate insulator layer under the first metal layer “to provide an insulated gate electrode,” which demonstrates the “electrode stack” of the independent claims is broader than an insulated gate electrode. Ex-1047, 20.

B. The Specification Does Not Define the Term “Electrode Stack” or Disavow Its Full Scope

The '562 patent provides no special definition of the term “electrode stack” that differs from its ordinary meaning. *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1367 (Fed. Cir. 2012) (held that claim term has its plain and ordinary meaning unless the patentee explicitly redefines the term or disavows its full scope); Ex-1047, ¶¶16-27. The term “electrode” appears fifty-nine times, including twenty-nine times with “stack.” *See* Ex-1001; Ex-1047, ¶22. Yet the '562 patent never once offers a precise definition that limits the scope of these terms. *Id.*; *Thorner*, 669 F.3d at 1367.

Instead, the patent uses non-limiting language and does not disavow scope. *See* Ex-1047, ¶¶23-26. For example, the patent repeatedly describes and claims the electrode stack as “**including** a plurality of metal layers and a capping layer,” so it may include other features not expressly described. *E.g.*, Ex-1001, Abstract (emphasis added), 3:46-48, claims 1, 13. Figure 1 is “an **example** group III-V semiconductor device,” for which Figure 2 provides “more detail[.]” Ex-1001, 2:43-46 (emphasis added), 3:36-39, 3:60-62. The “number and character” of metal layers in the electrode stack of Figures 1 and 2 “are merely exemplary.” Ex-1001, 3:36-39, 3:60-62. And Figure 3 similarly only refers to an example fabrication method. Ex-1001, 4:4-8, 4:12-16; Ex-1047, ¶25.

Moreover, the '562 patent broadly states: “[a]lthough the present inventive concepts are described with respect to specific embodiments, the principals of the

invention, as defined by the claims appended herein, can obviously be applied beyond the specifically described embodiments of the invention described herein.” Ex-1001, 2:25-28. And it confirms “particular details” of the structure of Figure 1 “are provided for conceptual clarity and should not be interpreted as limitations.” Ex-1001, 3:46-52. Other types of electrode stacks not depicted fall within the scope of the disclosure. Ex-1047, ¶¶26-27.

III. Patent Owner Proposes an Unjustified, Overly Narrow Definition of “Electrode Stack”

Patent Owner asserts an “electrode stack” is:

“a stack of conductive layers that forms an electrical contact that is part of a semiconductor device and used to (1) establish contact with a nonmetallic part of the semiconductor device (like the source, drain and Schottky gate electrodes in the ’562 Patent Specification) or (2) controls the operation of the semiconductor device (like the insulated or Schottky gate electrodes in the ’562 Patent Specification).”

POR, 8-9; Ex-2024, ¶91. They purport to rely on (1) intrinsic evidence from the claims, specification, and figures and (2) an extrinsic dictionary definition. POR, 3-10; Ex-2024, ¶¶81-95. But the specification does not limit the claims, *Thorner*, 669 F.3d at 1367, and extrinsic evidence cannot override the patent, *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005).

A. Patent Owner Imports Examples From the Specification Into the Claims to Narrowly Construe “Electrode Stack”

Patent Owner inappropriately adds limitations that from examples in the specification. POR, 4-9; Ex-2024, ¶¶81-91; *Haddad v. U.S.*, 164 Fed. Cl. 28, 50-51 (2023) (“Limitations from preferred embodiments are not read ‘into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited.’”). As explained above, the intrinsic record does not alter the meaning of “electrode stack.” Section II.

Although the law is clear that different terms mean different things, Patent Owner roots its construction on expert opinion that conflates “electrical contact” with “electrode stack.” *SimpleAir*, 820 F.3d at 431 (different terms mean different things); POR, 8-9 (citing Ex-2024, ¶¶80-91); Ex-1047, ¶¶29-35. Patent Owner’s expert Dr. Piner states contends the patent “links” the “electrical contact” and “electrode” and only ever implements the electrical contact as an electrode. Ex-2024, ¶¶86-91. But neither the claims nor the specification equate “electrical contact” and “electrode stack.” Section II; Ex-1047, ¶¶16-27. The claims open-endedly recite “electrical contact **comprising**: an electrode stack,” so these terms differ, and the electrical contact may include other components and is not simply “implemented” as an “electrode stack.” Ex-1047, ¶¶16-21.

Patent Owner and Dr. Piner rely on the examples of Figures 1 and 2 to attempt to (i) limit the scope of the term “electrode stack” to just three types of electrodes and (ii) to require either direct contact between a metal layer and a semiconductor

or a thin insulating material between a metal layer and a semiconductor. POR, 4-9; Ex-2024, ¶¶81-91(citing Ex-1001, 3:19-28, 1:33-43, 3:31-35, 3:21-33). As explained, the claims are not only limited to Ohmic, Schottky, or insulated contacts. Section II; Ex-1047, ¶¶28-35. For the same reasons, any examples showing either direct contact with a semiconductor or a contacted insulated by a thin material do not limit the “electrode stack.” *Id.* This term should be afforded the full scope of its plain meaning.

B. The Extrinsic Record Does Not Support Patent Owner’s Narrow Interpretation of “Electrode Stack”

Patent Owner’s curated, general-purpose definition of “electrode” does not limit the claims, and it cannot override the intrinsic evidence. Ex-1047, ¶¶36-39; POR 9-10; Ex-2024, ¶¶92-95; *Phillips*, 415 F.3d at 1317; *see* Section II. Patent Owner’s definition requires a component that (1) “establish[es] electrical contact with a nonmetallic component” or (2) “emits or collects electrons or holes or controls their movements.” Ex-2001 at 371. But that definition is incomplete, and Patent Owner fails to explain why it should be accorded any weight. Ex-1047, ¶¶37-38; POR, 9-10.

A technical definition from the relevant time shows the term is not limited to the narrow confines of Patent Owner’s incomplete definition. Ex-1047, ¶38. The Wiley Electrical Electronics Engineering Dictionary defines “electrode” as:

A conductor which serves to **deliver, receive, collect, emit, deflect or control electric charge carriers**. An electrode **provides the path for current entering or leaving a medium** such as a dielectric, electrolytic solution, semiconductor, gas, or vacuum. ... It is often a metal, and may consist for instance, of a wire, grid, plate or region.

Ex-1046, 237 (emphasis added). This definition broadly describes that electrodes “deliver, receive, collect, emit, deflect or control electric charge carriers” and provide a current path, which is consistent with how a POSTIA would have understood the term “electrode.” Ex-1047, ¶¶38-39.

Other extrinsic evidence contradicts Patent Owner’s construction. Ex-1047, ¶39. A POSITA would have understood that not every electrode is a source contact, drain contact, Schottky gate, or insulated gate. *Id.* For example, many references from the relevant time describe “interconnect electrodes” in semiconductor devices. *Id.*; Ex-1038, [0013], [0026], [0084], [0085], [107], Figs. 1-2, 10-11; Ex-1039, 449; Ex-1040, 1:42-45, 2:1-4, 2:9-19, 2:28-34; Ex-1041, [0233], Fig. 45; Ex-1042, 7:44, 9:47-50, Fig. 1B.

IV. Usui’s Structure is an Electrode Stack Under the Plain and Ordinary Meaning and Under Patent Owner’s Construction (Ground 1)

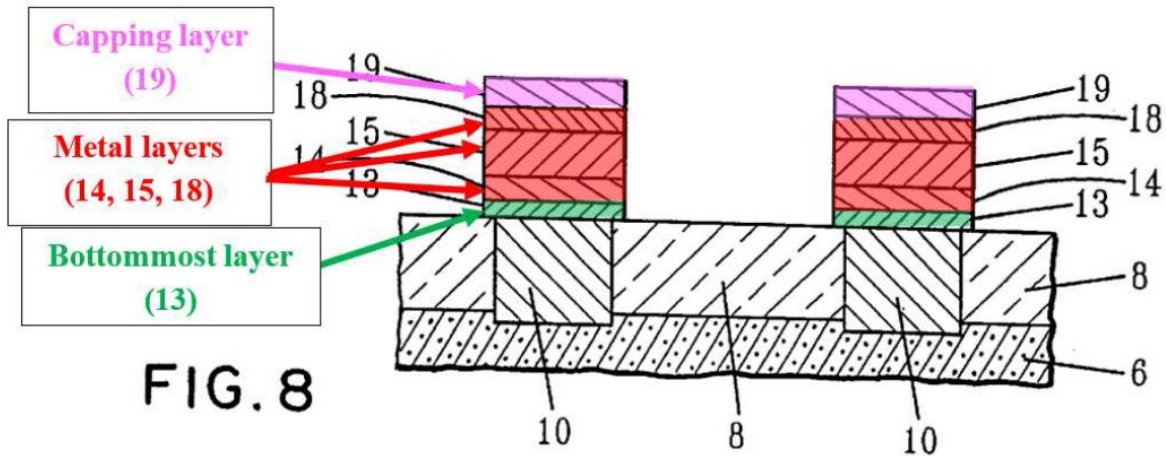
Patent Owner’s entire defense to Ground 1 rests on an improper, narrow construction of “electrode stack.” POR, 10-20; *supra* Sections II-III. Patent Owner asserts “electrode stack” excludes interconnects. Patent Owner even implausibly

contends Usui's layers of stacked metals is no evidence of a "stack." POR, 13-15. But as already shown, Usui discloses an interconnect that is an “electrode stack” under its plain meaning (Ex-1002, ¶¶89-91), and its interconnect meets even Patent Owner’s narrow construction (Ex-1047, ¶¶40-63).

A. Usui Discloses an Electrode Stack that is Part of a Semiconductor Device and Used to Establish Contact with a Nonmetallic Part of the Semiconductor Device

Usui meets the first part of Patent Owner’s alternative construction. POR, 4-9. Its interconnect includes a stack of conductive layers that contacts a nonmetallic part of the semiconductor device in two ways—physically and electrically. Ex-1047, ¶¶40-48.

First, Usui’s figures plainly show *physical contact* between the underlayer 13 and insulator 8, consistent with Patent Owner’s construction of “electrode stack.” Ex-1047, ¶42; Usui, Figs. 1-8. The interconnect includes the capping layer (19), metal layers (14, 15, and 18) and underlayer (13) which form an electrode stack. Ex-1004, 3:23-4:15. Underlayer 13 is a metal layer that may be sputter deposited on insulator 8, which is a non-metallic part of the semiconductor device. Ex-1004, 5:11-33, 5:49-52, Figs. 1-8.



Usui, Fig. 8 (annotated).

Usui's structure has a substantial area of physical contact between underlayer 13 and insulator 8. Ex-1047, ¶43. This is because "contact stud 10" is not a layer, it is an interplanar conductive via that cuts across device layers. Ex-1004, 3:24-27, 5:11-13, Figs. 1-8, Ex-1047, ¶43 (citing Ex-2026 (e.g., 10:9-13, 32:14-25, 37:6-14, 37:20-25, 50:11-18, 51:11-52:1, 76:16-20, 77:15-78:2, 79:8-17)). A conductive via is a filled hole, which is typically a much smaller structure than the surrounding layers and structures. Ex-1047, ¶43; Ex-2026, 10:9-13, 32:14-25, 37:6-14, 37:20-25, 50:11-18, 51:11-52:1, 76:16-20, 77:15-78:2, 79:8-17.

Second, Usui's interconnect establishes *electrical contact* with nonmetallic semiconductor wafer layer 6. Ex-1047, ¶¶44-47. The parties agree an interconnect provides electrical connections between semiconductor components. Ex-1047, ¶44; POR, 19; Ex-2024, ¶¶ 63, 147-148. And Patent Owner's expert concurs that interconnects electrically connect to semiconductor layers: "[i]nterconnects are

deposited on insulators and touch the active devices” and are made [of] multiple levels of metal lines and connecting vias “serve as the wiring between semiconductor devices, such as transistors.” Ex-2024, ¶63 (quoting Ex-1011 (emphasis original)); Ex-1047, ¶44. Usui makes the same point—its metallization structure “preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 *to make connection to* a device substrate 6.” Usui at 3:24-27 (emphasis added).

Patent Owner nevertheless contends the metallization structure does not establish contact with the semiconductor layer 6 because it *indirectly* connects the semiconductor through stud layer 10. POR, 18-19; Ex-2024 at ¶¶149-151; Ex-1047, ¶45. This inappropriately construes the construction to impose further requirements—an electrode stack needs *direct* electrical contact with a nonmetallic component. Ex-1047, ¶46. But the purpose of claim construction is to clarify the meaning of claim terms, not to create confusion or ambiguity, by requiring further interpretation. *O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008).

Patent Owner looks to the specification and their dictionary definition to assert an electrode requires “direct” electrical contact with a nonmetal. POR, 17-19; Ex-2024, ¶¶149-151. But, as explained, the intrinsic and extrinsic record do not limit “electrode stack.” See Sections II-III; Ex-1047, ¶¶15-39. And neither the

specification nor Patent Owner’s dictionary definition use the term “direct” in any context. *See generally* Ex-1001; Ex-2001, 371; Ex-1047, ¶¶36-39. Regardless, Patent Owner’s definition that is incomplete. Section III.B. Usui’s interconnect is “[a] conductor which serves to deliver, receive, collect, emit, deflect, or control electric charge carries” and “provides the path for current entering or leaving a medium,” consistent with the technical definition of “electrode.” Ex-1047, ¶38; Ex-1037, 237.

A POSITA would have understood that electrical connections include indirect connections, in accord with the prior art. Ex-1047, ¶¶44-48. For example, Usui’s metallization structure connects to semiconductor layer 6 through a conductive via. Ex-1004, 3:24-27. Yu (Ex-1005) also makes indirect electrical contacts with interconnects. Yu, ¶¶[0087], [0111].

B. Usui’s Electrode Stack Controls the Operation of the Semiconductor Device

Usui meets the second of Patent Owner’s alternative constructions—it controls the operation of the semiconductor device. POR, 4-9; Ex-1047, ¶¶49-51.

“Control” is not a claim term and does not appear anywhere in the ’562 patent. Ex-1001. Patent Owner’s construction thus creates further confusion by requiring interpretation of “control.” POR, 4-10; Ex-2024, ¶¶81-91; Ex-1047, ¶49. This is another reason the construction is incorrect. *O2 Micro*, 521 F.3d at 1362.

Nevertheless, Petitioner understands “controls the operation” to involve at least enabling or influencing current flow. Ex-1047, ¶49. Usui satisfies this condition two ways. *First*, an interconnect undisputedly provides electrical connections between devices (e.g. Ex-2024, ¶¶63-65, 147-148), which controls the operation of a semiconductor device by enabling and influencing current flow. Ex-1047, ¶50. An integrated circuit cannot function without an interconnect. Ex-1047, ¶50. *Second*, Usui’s interconnect metallization reduces electromigration, resulting in longer failure times, which is another way it “controls” the semiconductor device. Usui, Abstract, 1:30-35, 3:54-57, 4:57-5:10, Figs. 9-10; Ex-1037, 237; *see* Ex-2024, ¶66, Ex-1024, ¶¶100, 218. By improving electromigration, the metallization structure shapes current characteristics, so it controls operation. Ex-1047, ¶51.

C. While Applying Patent Owner’s Construction of “Electrode Stack” to Usui, Patent Owner Incorrectly Construes “Semiconductor Device” and “Electrical Contact”

1. Without support, Patent Owner attempts to exclude structures that electrically connect other devices from the claimed “semiconductor device”

Patent Owner construes “semiconductor device” to exclude interconnect metallization structures based on their function, because it connects two devices. POR, 10-20; Ex-2024, ¶151. But Patent Owner cites no intrinsic evidence in support. POR, 10-20; Ex-2024, ¶¶144-153. The patent claims a “semiconductor device”

(claims 1, 13) without altering its meaning and does not limit the “electrical contact” or “electrode.” *See* Section II; Ex-1047, ¶¶28-39; *Phillips*, 415 F.3d at 1313.

Usui’s interconnect was part of its semiconductor device, consistent with Usui’s description and other prior art. Ex-1047 ¶¶52-54. Usui’s “interconnect metallurgy structure” and “semiconductor wafer 6” are formed as one device through a sequence of deposition, masking, and etching steps. Usui, 3:23-4:10, Figs. 1-8. Other prior art agrees. Ex-1044, [0009], [0029], claim 11; Ex-1045, ¶¶[0003]-[0010], [0016], [0020], [0031], claims 1-8; *see* Ex-1011, 217-218; Yu, [0040], [0063], [0087]; Ex-1047 ¶¶52-54.

2. Patent Owner implausibly construes “electrical contact” to require a metal-semiconductor junction

Patent Owner relies on an expert opinion that construes an “*electrical contact*” to require a metal-semiconductor junction, not a metal-metal connection. POR, 5, 11, 18-19; Ex-2024 at ¶¶62-71, 100, 102, 136; Ex-1047, ¶¶55-56. Dr. Piner recognizes that “metal-metal electrical connections” were “conventional” and “known,” but he contends they are not within the scope of the ’562 patent’s “electrical contact.” Ex-2024 at ¶¶62, 102, 136. In support, he advances the same flawed argument as with “electrode stack,” alleging that “generally an interconnect does not have a metal-semiconductor junction like an ohmic contact or gate contact and therefore would not have been confused with an electrical contact.” Ex-2024 at ¶62; Ex-1047, ¶55; *see* Section II-III.

This is incorrect for two reasons. Ex-1047, ¶56. First, the claimed “electrode stack” does not require a metal-semiconductor junction, so the broader “electrical contact comprising: an electrode stack” does not require a metal-semiconductor junction either. Sections II-III. Second, this argument inexplicably excludes metal-metal junctions without support from the patent itself. Ex-2024, ¶¶62, 102, 136; Ex-1047, ¶56. The patent provides only non-limiting examples of electrical contacts. Ex-1001, 2:43-46, 3:36-39, 60-62, Figs. 1-2.

3. Patent Owner inappropriately contends the claimed “electrical contact” cannot be an interconnect because Dr. Piner incorrectly alleges the claims exclude components that experience electromigration

Patent Owner incorrectly construes “electrical contact” and “electrode” to exclude interconnects. POR, 11 (citing Ex-2024, ¶¶133-138); Ex-1047, ¶¶57-63. It bases this position on expert opinion that excludes devices electrodes cannot experience “electromigration, a problem specifically associated with aluminum-based interconnects, and not associated with *electrical contacts having an electrode stack* as described and claimed by the ’562 Patent.” Ex-2024, ¶134; Ex-1047, ¶57; *see* Ex-2024, ¶¶99-105, 134, 138, 148, 161, 169-176, 181-182, 189, 195, 201-202, 210, 217-222, 270-273. This once again imposes limitations on the claims that are not there. Ex-1047, ¶58.

The ’562 patent’s electrodes would have experienced electromigration, which generally arises at high current density. Ex-1047, ¶59 (citing Ex-1021, 7-8). In fact,

Dr. Piner agrees electromigration typically occurs at relatively high current densities. Ex-2024, ¶100. So does a prior Infineon patent. Ex-1043, 1:17-36;¹ Ex-1047, ¶60. Thus, electrodes would benefit from improved (reduced) electromigration. Ex-1047, ¶¶57-63; Ex-1002 at ¶¶73, 84, 101, 113-122, 131-133, 144, 176, 179; Ex-2026 at 12:18-14:20, 16:5-17:6, 54:2-56:25. That is one purpose of the barrier layer described in the patent. Ex-2026 at 54:2-56:25.

The electrical contact of the '562 patent would have experienced electromigration. Ex-1047, ¶¶60-63. HEMT power transistors often have high current flows and densities, including in ohmic contacts, which can cause electromigration. Ex-1047, ¶61; Ex-1001, 2:53-65, claims 9, 14. Gate leakage can also cause electromigration in gate electrodes. Ex-1047, ¶62; Ex-1018 at 937. This is especially problematic for Schottky connections, where leakage increases exponentially with voltage and temperature. Ex-1047, ¶62, Ex-1015, 353-354.

¹ Assigned to Infineon Technologies Americas Corp., which, appears to relate to Patent Owner (Infineon Technologies Austria AG).

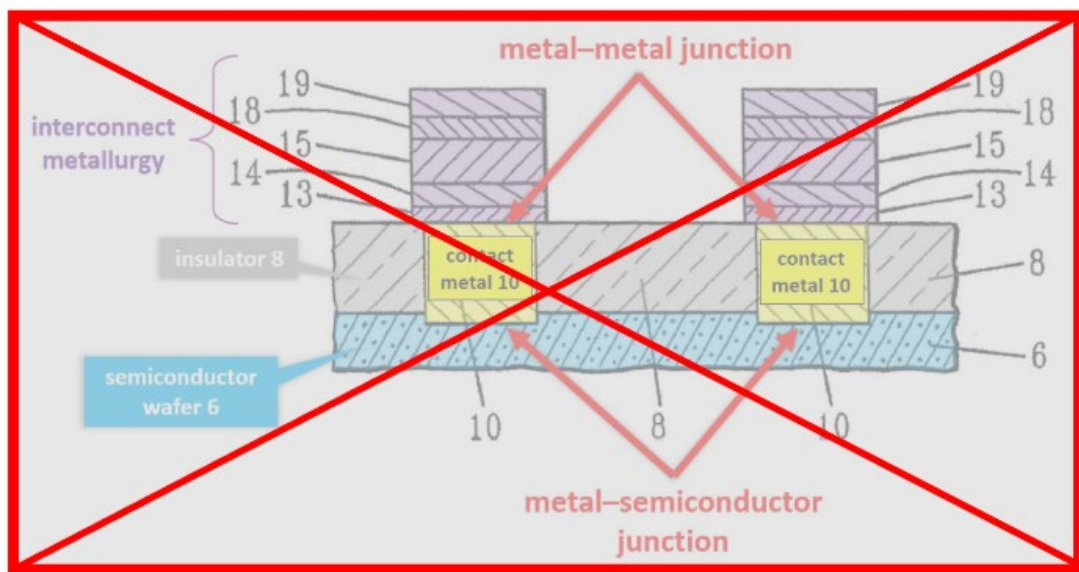
V. Patent Owner Mischaracterizes the Combination of Usui and Yu for Claims 12 and 17 and the Petition’s Position on Electromigration (Ground 2)

A. The Petition Implemented Usui’s electrode stack in Yu’s device

The combination for claims 12 and 17 implements Usui’s electrode stack in Yu’s device. Petition, 18-19 (claim 8), 19-20 (claims 12 and 17).² Claim 12 depends from claim 8. Regarding claim 8, the Petition reasons a POSTIA would have “implement[ed] the electrical contacts as taught by Usui in group III-V semiconductor devices, as taught by Yu.” (emphasis added). Petition, 19. Dr. Zhao reiterated this point: “here we are using Usui’s natural contact . . . for the III-V semiconductor device as taught by Yu.” Ex-2026, 186:4-11. Claim 12 makes the same combination: “it would have been obvious for the POSITA to *place the Usui contact in the transistor of Yu* and to further include the gate insulator layer.” Petition, 22 (emphasis added). There is nothing “belated” about this combination. See POR, 27 at n.10.

² For claim 3, the Petition described another obvious way to combine Usui and Yu by using Yu’s TaN in Usui’s device. Petition, 17-18; see Ex-2026, 198:9-199:9. Patent Owner does not dispute that combination besides its challenge to Ground 1. POR, 21-22.

Rather than addressing Petitioner’s actual position, Patent Owner invents their own, contending Ground 2 involves incorporating Yu’s dielectric into Usui’s device. POR, 22-28. Even though Patent Owner acknowledges the Petition “does not illustrate” this fabricated position, Dr. Piner provides an illustration, shown below, POR, 24; Ex-2024, ¶164. All arguments on this made-up combination are non-responsive and further argument on this issue combination not in the Patent Owner Response is forfeited. *Google LLC v. UNILOC 2017 LLC*, IPR2020-00447, Paper 24, at 8 (P.T.A.B. May 11, 2021).



Ex-2024, ¶164 (annotated by Petitioner).

B. A POSITA Would Have Used Usui’s Metallization Stack in Yu’s Device to Improve Electromigration

Patent Owner can hardly support its contention that Dr. Zhao misunderstands electromigration when describing “enhanced electromigration.” POR, 29, 36, 40-42; Ex-2024, ¶¶182, 201, 218, 219. Usui itself describes its benefits in precisely this

way, discussing “enhanced electromigration performance” (Usui, 2:33-39), “enhanced electromagnetic characteristics” (Usui, 2:50-53), “greatly improved electromigration performance” (Usui, 3:54-57), “optimum electromigration performance [and] significantly improved electromigration performance” (Usui, 6:34-42),; “maximiz[ing] the electromigration performance” (Usui, 6:64-67). This plainly describes reducing the negative effects of electromigration. *See* Ex-2026, 13:23-14:9.

Drs. Zhao and Piner share the same general understanding. As Dr. Zhao explained, electromigration is the physical transport of metal in a conductor caused by current flow. Ex-2026, 14:4-9, Ex-100, Ex-1021, 7-8; Ex-2026, 13:25-14:1. Dr. Piner concurs. Ex-2025, ¶66. Dr. Zhao displays no “fundamental” misunderstanding of this phenomenon. POR, 40.

Moreover, Patent Owner and Dr. Piner, not Petitioner, apparently misapply electromigration principles to contend it cannot be found in electrodes, only in interconnects. *See* Section IV.C.3; Ex-2024, ¶¶104, 134; Ex-1047, ¶¶57-63. Even an Infineon patent disagrees, identifying electromigration as a problem for gate electrodes. Ex-1043, 1:17-36, 2:39-61, Fig. 1.

Accordingly, a POSITA would have used Usui’s principles to improve electromigration characteristics in Yu’s device. Petition, 19-20. Patent Owner’s contention that this would “change the function” of Usui’s invention (POR, 27 n.10)

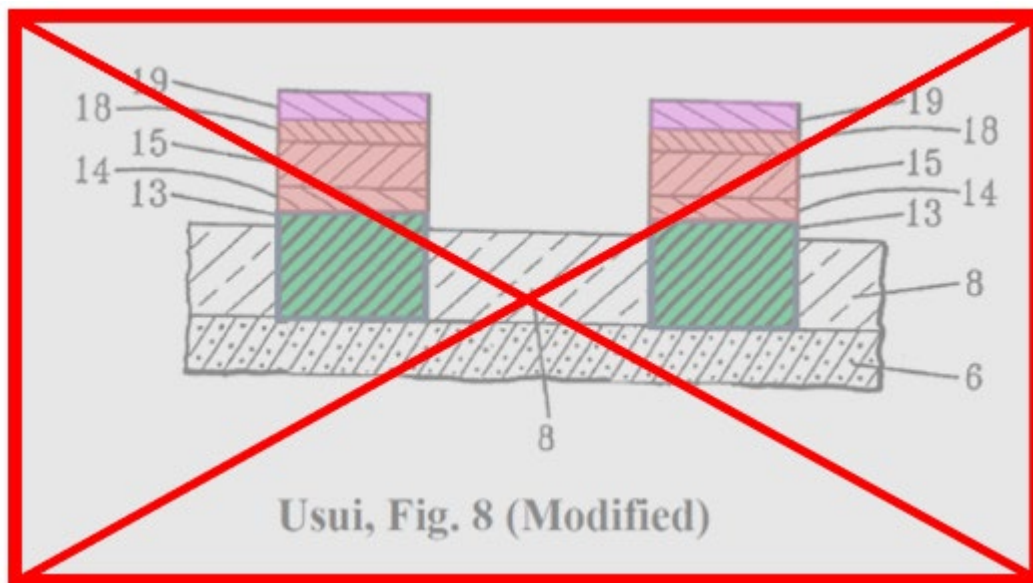
misunderstands the reference, which would benefit electromigration in the context of Yu. *Supra*. Metal and capping layers of Usui and Yu are interchangeable and may be widely applied because the layers are formed from the same type of materials. See Section V.B. Thus a POSTIA would have expected success. *Eli Lilly & Co. v. Teva Pharms. Int'l*, 8 F.4th 1331, 1344 (Fed. Cir. 2021). Yu's insulating layers further reduce electromigration because a diffusion barrier is known for "excellent barrier characteristics for inhibiting" unwanted metal migration. Petition, 19-20; Ex-1031 at 5:39-41; Ex-2026, 13:4-13, 14:4-20, 16:11-17:6, 54:20-55:19, 56:5-20, 63:14-64:2, 81:21-9, 83:9-84:1, 85:18-86:11, 100:1-8, 103:10-18, 108:13-109:6, 109:13-110:7, 111:7-18, 164:2-17. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2005).

VI. For Ground 3, Patent Owner Fabricates Its Own Combination, Which Fails to Address the Actual Ground in the Petition

For Ground 3, Patent Owner and Dr. Piner make the same mistake as for Ground 2 and fabricate a different combination than the one presented in the Petition. POR, 28-36. For claims 11 and 16, a POSITA would have "implement[ed] the Usui-Yu contact as a *Schottky contact*, as taught by Adesida." Petition, 25-27 (emphasis added). Dr. Zhao reiterated this position at his deposition: "So for claim 11 and 16, we are making Schottky gate structure on III-V semiconductor HEMT device, and we are using the metal layers that taught be Usui and Yu." Ex-2026, 191:23-192:1. For claims 9 and 14, a POSTIA would have implemented the

electrical contact of Usui-Yu on **HEMTs**, as taught by Adesida. Petition, 27 (emphasis added). The combination “result[ed] [in] a HEMT device with the metal layers taught by Yu and Usui as the gate.” Ex-2026, 195:21-25.

Patent Owner ignores that evidence to fabricate a strawman combination, as shown below. POR, 33-34; Ex-2024, ¶193. No such combination is depicted or described in the Petition. Patent Owner’s arguments are thus nonresponsive and it forfeits argument against the correct combination. *Google LLC v. UNILOC 2017 LLC*, IPR2020-00447, Paper 24, at 8 (P.T.A.B. May 11, 2021).



Piner, ¶193 (annotated)

Those nonresponsive arguments lack merit. Usui’s electrode is not “dramatically changed” in combination with Yu. POR, 31-32, Ex-2024, ¶189. This misunderstand the interchangeability of such materials and fails to appreciate a

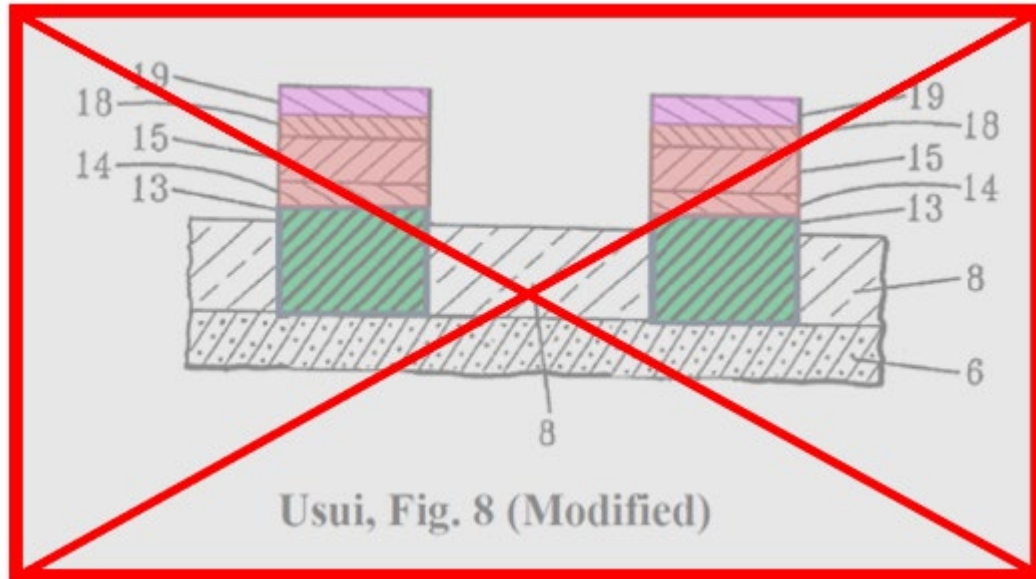
POSITA would have recognized the benefits of Usui's electromigration protections in Yu's system, as discussed for Ground 2. Section V.B.

The motivation to reduce electromigration is even greater in the Schottky electrode, especially at high frequencies, where leakage increases exponentially with voltage and temperature. Ex-1047, ¶¶57-63, Ex-1015, 353-354. And a POSTIA would have used Adesida's Schottky approach for high frequency applications. Petition, 26. The combination was "predictable and will be obvious . . . because insulated gate and Schottky gate are two commonly, most widely used and very well known gate structures." Ex-2026, 24:9-25:9, 26:12-23, 61:24-62:13, 88:24-89:17, 102:5-103:6, 113:6-22, 135:5-17, 135-21-136:11, 136:17-137-3, 137:15-138:1, 139:1-16, and 190:9-191:3.

VII. For Ground 4, Patent Owner Fabricates Its Own Combination, Which Fails to Address the Actual Ground in the Petition

Yet again, for Ground 4, Patent Owner and Dr. Piner fabricate a different combination than the one presented in the Petition. POR, 37-43; Ex-2024, ¶¶206-228. For claims 10 and 15, a POSITA would have "implement[ed] the contact of Usui-Yu as a power electrode making an ohmic contact as taught by Sugimoto" to improve current flow. Petition, 31. Dr Zhao confirmed: "for ground 4, we are using Usui and Yu's teaching of those metal layers to form ohmic contact, and that ohmic contact will serve a power electrode on a III-V semiconductor device, as laid out in Sugimoto," which "is a HEMT" with ohmic source and drain electrodes. Ex-2026,

¶¶193:2-16. Patent Owner and Dr. Piner create their own combination. POR, 38-39, Ex-2024 at ¶213.



Piner, ¶213 (annotated)

Those nonresponsive arguments lack merit and are irrelevant. POR, 42-43, Ex-2024 at ¶¶224-228; *see* Section VI. And Patent Owner's repeat argument that Dr. Zhao misunderstands electromigration (POR, 41), fails as previously explained (Section VI; Ex-1014, 1024; Ex-1043, 1:17-36, 2:39-61; Ex-1047, ¶60).

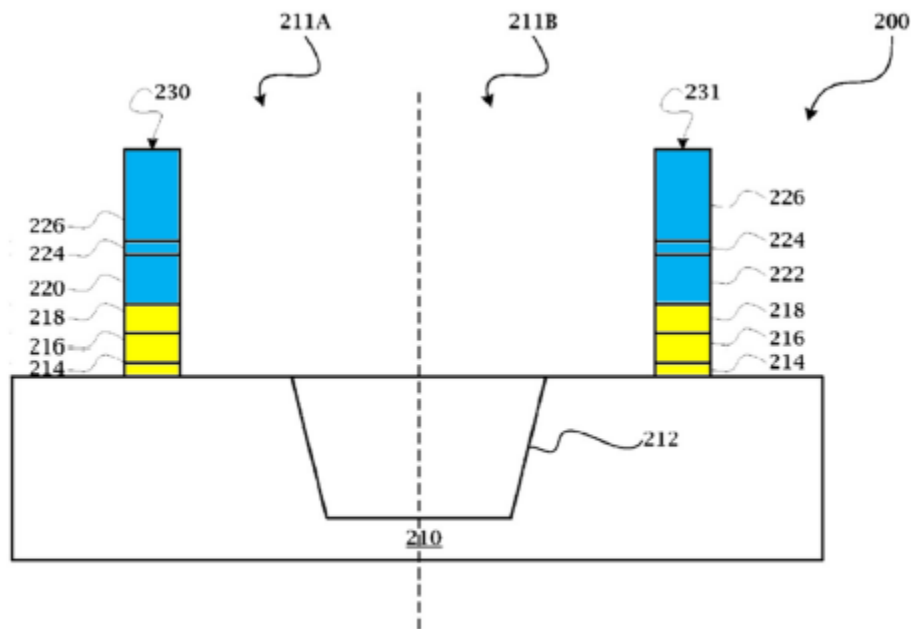
A POSITA would have implemented Usui-Yu's contact as a power electrode with an ohmic contact, as taught by Sugimoto, to improve current flow due to reduced electromigration. Petition, 31. A HEMT device was a design alternative within the level of skill of the POSITA. Petition, 29-31. And ohmic contacts minimize power consumption and heating, which prolongs device operation with

predictable performance. Ex-2026, 11:18-23. This would have been an obvious design choice. *See* Section V.B.

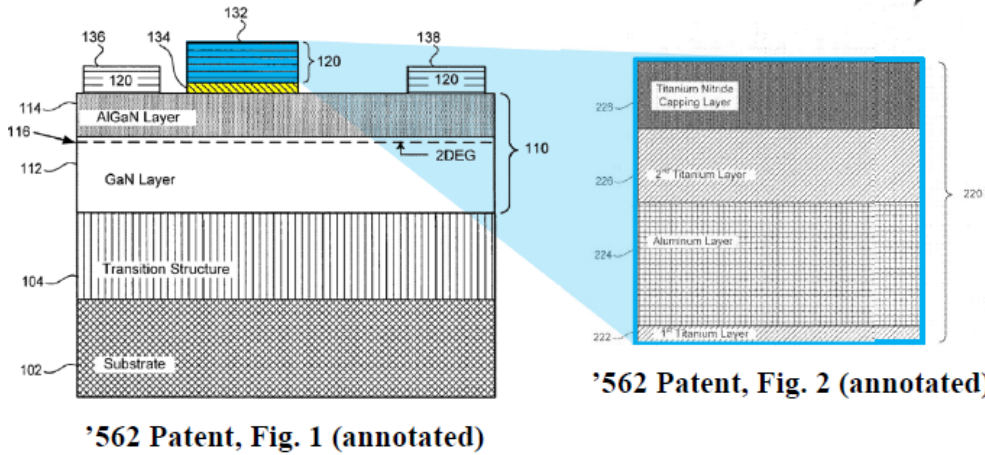
VIII. Yu Has the Same Layer Arrangement as the Claimed “Electrode Stack,” and it Expressly Provides the Refractory Metal Nitride Capping Layer Thickness of Presented in the Petition (Ground 5)

A. Patent Owner Agrees that Yu’s Metal Gate Stacks Have the Same Arrangement of Layers as the Claimed “Electrode Stack” But Draws Arbitrary Boundaries in Defense

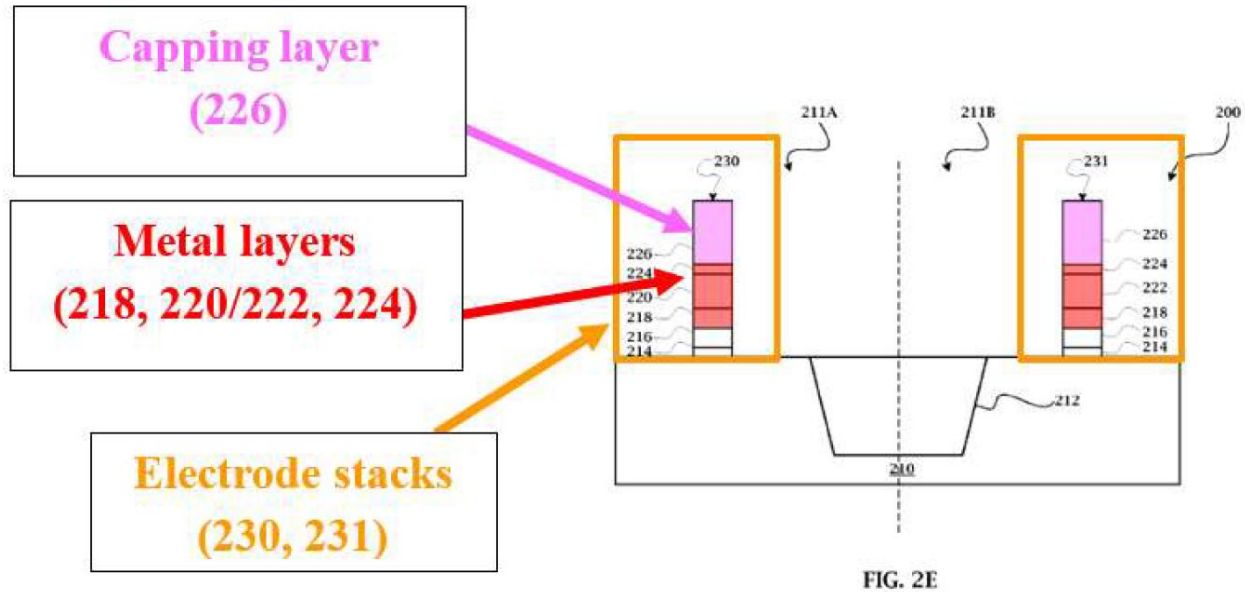
Patent Owner agrees that Yu discloses the same insulated gate electrodes stacked above other layers, just like the Patent, and even highlights these similarities (blue and yellow). POR, 46.



Yu, Fig. 2E (annotated)



While Patent Owner divides structures 230 and 231 into the above blue and yellow portions, that is not the mapping in the Petition. Instead, the Petition identifies capping layer 226 (pink), and metal layers (red) 218, 220/222, and 224. Petition, 42. Barrier layer 218 is the claimed “bottommost layer” of the plurality of metal layers. Petition, 42; Ex-2026, 14:10-20, 44:25-45:10, 45:19-46:1, 54:20-55:19, 56:13-20, 81:1-11. It is undisputed that layers 216 and 214 (unhighlighted) are dielectrics. Yu, [0027].



Petition, 42.

Claims 1 and 13 recite an “electrical contact comprising: an electrode stack *including* plurality of metal layers and a capping layer.” Ex-1001. Patent Owner’s semantic critique that “Yu *calls* the entire stack a ‘metal gate stack,’” fails. POR, 47 (citing Yu, [0038]-[0039]) (emphasis added). So does Patent Owner contention that the Petition boxes the “entire” structures 230 and 231 to identify the claimed “electrode stack.” POR, 49-51. The claims open-ended use of “including” does not preclude other structures in the stack. And as the Patent Owner admits, both Yu and the ’562 patent show a stack of metal layers above dielectrics. POR, 46.

Yu thus discloses the claimed “electrode stack,” whether its boundaries are drawn to include the dielectrics or not. Dr. Zhao clarified that he drew the “yellow box on 230, 231 just to highlight this component of Yu as important.” Ex-2026,

90:25-91:17. But the analysis as presented in the declaration and the Petition focused on the claimed features—the metal layers and capping layers—not the non-conducting dielectric. Petition, 33-55; Ex-1002, ¶¶149-187; Ex-2026, 90:25-91:17.

In another failed defense, Patent Owner contradicts itself by contending Yu’s barrier layer 218 is “not part of the gate electrode, it separates the gate electrode from the oxide layer.” POR, 48. Yet on the preceding page, Patent Owner argues the opposite, that “Yu calls the entire stack”—including barrier 218—“a “metal gate stack.” POR, 47. And Patent Owner does not dispute that barrier 218 is a metal layer stacked along with the other metal layers. POR, 47-49. Patent Owner cannot exclude it from the “electrode stack’s plurality of metal layers with expert opinion when the intrinsic record does not. *Phillips*, 415 F.3d at 1317. The plain meaning applies. Section II.

B. Yu at [0036] discloses or at least rendered obvious a refractory metal capping layer with a thickness from 50-1000Å, thicker than the 20Å bottommost metal layer

While Yu does not expressly disclose the claimed thickness of [1.C], it renders it obvious. Petition, 33-55 (citing Yu, [0036]); Ex-1002, 149-187 (same). Barrier layer 218 comprises metals, including TiN, which may have a thickness of 20Å. Petition, 38; Yu, [0029]. This is the claimed bottommost layer. Petition, 43-44.

When Yu’s capping layer is polysilicon, it measures 200-1,000Å, preferably 600Å, thicker than the bottommost layer, as required in [1c]. Yu, [0036]; Petition,

42-43. When the cap layer comprises metal, its thickness ranges from 50Å to 1,000Å, which includes 600Å. Yu, [0036]; Ex-2026, 46:19-47:25 (discussing this passage), 164:23-165:23 (same). This applies to Yu’s refractory metals, such as TiN and TaN. Petition, 38-39; Ex-1002, ¶¶165-168; Ex-2026, 46:19-47:25, 164:23-165:23. It would have been obvious that the capping layer would have had a thickness of 600. Pet, 33-55; Ex-2026, 46:19-47:25 (discussing this passage), 164:23-165:23 (same).

Yu provides the exact rational the Board questioned: whether a POSITA would have replaced the polysilicon cap with TiN or TaN at 600Å thick. Paper 10, 17-19. Yu’s metal based capping layer is thicker than the bottommost metal layer (20Å) for the *entire range* 50-1,000Å. A polysilicon thickness of 600Å would have been a suitable choice for a capping layer *including metal*. Ex-2026, ,47:1-25, 144:11-145:2, 161:16-162:3, 165:1-20, 168: 14-21.

The Petition looked to Usui to confirm the relationship of capping layer to bottommost layer—already disclosed by Yu—was known and obvious. Petition, 45-46.

IX. The Combination of Yu, Usui and Adesida Discloses all the Features of Claims 9, 11, 14 and 16 (Ground 6)

As with the earlier Grounds, Patent Owner attacks the Petition for positions it did not take then alleges the Reply cannot argue “the structure of the gate electrode

in Yu-Usui-Adesida is ***Yu***’s gate electrode.” POR, 70-71. But that is precisely what the Petition did.

For claims 9 and 14, “it would have been obvious to implement Yu-Usui’s group III-V semiconductor devices as HEMTs.” Petition, 59. This meant Adesida’s “HEMT device with the metal layers taught by Yu and Usui as the gate.” Ex-2026, 195:21-196:7. Similarly, for claims 11 and 16, “would have been obvious to implement Yu or Yu-Usui’s group III-V semiconductor devices with gate electrodes making Schottky contacts.” Petition, 60. The result is “a III-V HEMT device with the metal layers from Usui and Yu as the Schottky gate contact, or Schottky gate electrode on these III-V HEMT device.” *Id.* at 196:25-197:3. The Petition gave detailed motivation, and a POSITA would have expected success. Petition, 55-59; *see* Sections V.B, VII.

X. The Combination of Yu, Usui and Sugimoto Discloses all the Features of Claims 10 and 15 (Ground 7)

Yet again, for Ground 7, Patent Owner fabricates a different combination than the one presented in the Petition alleging it implements Sugimoto’s source and drain as gate electrodes. POR, 74. Not true. It “implement the devices [i.e., the electrode stacks] of Yu and Yu-Usui with a power electrode making an ohmic” which uses Usui’s metal layer as the power electrode in ohmic contact with the underlying layer. Petition, 63; Ex-2026, 197:4-198:8. The Petition provided a rationale for doing so, despite Patent Owner’s assertions none was given. Petition, 62-64; POR, 72-76.

XI. Conclusion

The Board should find all claims of the '562 patent unpatentable.

Dated: December 23, 2025

/Lionel M. Lavenue/

Lionel Lavenue

Reg. No. 46,859

37 C.F.R. § 42.24(D) CERTIFICATION

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), Petitioner certifies that this petition complies with the requirements of 37 C.F.R. § 42.24. Excluding parts of this Petition exempted under § 42.24(a), this Petition contains 5,584 words, as measured by the word-processing system used to prepare this paper.

Dated: December 23, 2025

/Lionel M. Lavenue/
Lionel Lavenue
Reg. No. 46,859

CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing **Petitioner's Reply to Patent Owner's Response and Exhibits 1038-1047** were served on December 23, 2025, via email directed to counsel of record for the Patent Owner at the following:

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