

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AMERICAS CORP.,
Patent Owner.

Case No. IPR2025-00175
Patent No. 8,686,562

PATENT OWNER'S SUR-REPLY TO PETITIONER'S REPLY

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LISTING OF EXHIBITS

Exhibit	Description
2001	Excerpts from Merriam Webster’s Collegiate Dictionary (10th ed.) (2001)
2002	U.S. Patent Application Publication No. 2008/0251828 A1 (“Meng”)
2003	U.S. Patent Application Publication No. 2011/0247549 A1 (“Sachs”)
2004	Quirk, M., & Serda, J. (2001) Semiconductor Manufacturing Technology. Prentice Hall.
2005	Stewart, C.M., “Interim Processes for PTAB Workload Management,” Memorandum dated March 26, 2025
2006	United States Patent Office, “Guidance on USPTO’s rescission of ‘Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation’ (March 24, 2025), available at https://www.uspto.gov/sites/default/files/documents/guidance_memo_on_interim_procedure_rescission_20250324.pdf .
2007	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Order No. 5, Initial Determination Setting an 18-Month Target Date and Order Setting Preliminary Conference (ITC Sept. 18, 2024)
2008	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Order No. 6, Setting the Procedural Schedule (ITC Sept. 27, 2024)
2009	RESERVED
2010	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Order No. 25, Amending the Procedural Schedule (ITC Feb. 27, 2025)
2011	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Order No. 32, Amending the Procedural Schedule (ITC Apr. 8, 2025)
2012	Email from Niemeyer, Elizabeth, RE: Inv. No 337-TA-1414 Innoscience’s Invalidity Contentions (Feb. 3, 2025)
2013	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Respondents’ Invalidity Contentions (ITC Jan. 24, 2025)
2014	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Respondents’ Invalidity Contentions Appendix B-2 (ITC Jan. 24, 2025)

Exhibit	Description
2015	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Respondents’ Invalidity Contentions Appendix B-3 (ITC Jan. 24, 2025)
2016	Email from Green, Alissa, RE: Inv. No. 337-TA-1414 Infineon's Case Narrowing Disclosure (Apr. 1, 2025)
2017	<i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; Inv. No. 337-TA-1414. Joint Proposed Claim Construction Chart (ITC Jan. 17, 2025)
2018	United States Patent Office, “USPTO rescinds memorandum addressing discretionary denial procedures” (Feb. 28, 2025) available at https://www.uspto.gov/about-us/news-updates/uspto-rescinds-memorandum-addressing-discretionary-denial-procedures .
2019	Vidal, K., “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings With Parallel District Court Litigation,” Memorandum dated Jun. 21, 2022
2020	Email from Lavenue, Lionel RE: Stay, Infineon v. Innoscience – NDCA (Aug. 27, 2024)
2021	<i>Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al.</i> ; Case No. 4:24-cv-01553-YGR, Dkt. No. 55, Joint Stipulation to Stay Pending ITC Proceeding; [Proposed] Order (N.D. Cal. Aug. 30, 2024)
2022	<i>Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al.</i> ; Case No. 4:24-cv-01553-YGR, Dkt. No. 56, Order Staying and Conditionally Closing Case for Statistical Purposes (N.D. Cal. Aug. 30, 2024)
2023	Declaration of Turhan F. Sarwar in Support of Admission <i>Pro Hac Vice</i>
2024	Declaration of Edwin Piner, Ph.D. (“Piner”)
2025	Curriculum Vitae of Edwin Piner, Ph.D.
2026	Transcript of Deposition of Yuji Zhao, Ph.D. (Sept. 5, 2025) (“Zhao-Dep.”)
2027	Larry Zhao, “All About Interconnects” Semiconductor Engineering, https://semiengineering.com/all-about-interconnects/ (Dec. 18, 2017)
2028	U.S. Patent No. 6,249,056 (“Kwon”)
2029	U.S. Patent No. 4,017,890 (“Howard”)
2030	Excerpts from JAEGER, INTRODUCTION TO MICROELECTRONIC FABRICATION (2nd Ed. 2002) (“Jaeger”)
2031	Excerpts from OHRING, THE MATERIALS SCIENCE OF THIN FILMS (1992) (“Ohring”)

Exhibit	Description
2032	U.S. Patent No. 7,537,951 (“Gambino”)
2033	U.S. Patent App. Pub. No. 2007/0007653 A1 (“Chen-653”)
2034	Stewart, C.M., “Enforcement and Non-Waiver of 37 C.F.R. § 42.104(B)(4) and Permissible Uses of General Knowledge in Inter <i>Partes</i> Reviews,” Memorandum dated July 31, 2025

I. USUI-BASED GROUNDS 1-4 FAIL

A. “Electrode Stack” Construction

1. Infineon’s Construction

“[T]he proper construction in view of the specification is a stack of conductive layers that form an electrical contact that is a part of a semiconductor device and used to (1) establish electrical contact with a nonmetallic part of the semiconductor device (like the source, drain and Schottky gate electrodes in the ’562 Patent specification) or (2) control the operation of the semiconductor device (like the insulated or Schottky gate electrodes in the ’562 Patent Specification).” POR, 8-9.

2. Petitioner’s Construction

Unable to refute that both the intrinsic and extrinsic evidence support Infineon’s construction, Petitioner twists itself into knots. Petitioner asks the Board to ignore the intrinsic evidence because “the specification does not limit the claims,” then inconsistently says the Board should ignore the extrinsic evidence because it “cannot override the patent.” Reply, 5. Petitioner criticizes use of a dictionary definition (Reply, 7), then offers its own:

A conductor which serves to deliver, receive, collect, emit, deflect or control electric charge carriers. An electrode provides *the path for current entering or leaving a medium such as a dielectric,*

electrolytic solution, *semiconductor*, gas, or vacuum... It is often a metal, and may consist for instance, of a wire, grid, plate or region.¹

Reply, 7-8 (citing EX-1046).

Petitioner’s definition limiting an electrode to “provid[ing] the path for current *entering or leaving* a medium, such as *a... semiconductor*” (Reply, 7-8) is largely consistent with Infineon’s construction.² Petitioner would have the Board believe that *any* wire *anywhere* in a connection path between a semiconductor device and another circuit component is an “electrode.” That is inconsistent with the claims (which recite the electrical contact comprising the electrode stack as being “on” a semiconductor device), the specification, and both parties’ dictionary definitions.

3. Petitioner Attacks Strawmen

Infineon never argued that “Usui’s layers of stacked metals is no evidence of a ‘stack.’” Reply, 8-9. Infineon explained that Petitioner failed to establish that Usui’s layers 13-15 and 18-19 are an “electrode stack” (POR, 13-15) because Petitioner “improperly read[] ‘electrode’ out of the claims”—not “stack.” POR, 17 n.9.

¹ All emphasis is added unless otherwise indicated.

² Petitioner’s critique that Infineon’s construction uses the word “control” (Reply, 12) ignores that Petitioner’s definition does too.

Infineon never argued that “an electrode requires ‘direct’ electrical contact with a nonmetal.” Reply, 11; *see also* Reply, 14-15 (“Patent Owner implausibly construes ‘electrical contact’ to require a metal-semiconductor junction”). Infineon’s construction encompasses the ’562 Patent’s “insulated” gate electrodes “separated from the semiconductor by an insulating oxide layer.” POR, 5.

Dr. Piner never “allege[d] the claims exclude components that experience electromigration.” Reply, 15-16. He merely explained why (Piner, ¶¶62-68, 134-135) Usui’s electromigration teachings support Infineon’s explanation that Usui relates to interconnects rather than electrodes. Piner, ¶134.

B. Petitioner Fails to Demonstrate that Usui’s Interconnect is an Electrode Under Any Reasonable Construction

1. ’562 Patent

Petitioner never disputes that Usui’s interconnect is unlike any of the ’562 Patent’s electrodes. POR, 16 (it is not a Schottky or insulated gate electrode or a power electrode ohmically coupled to a semiconductor).

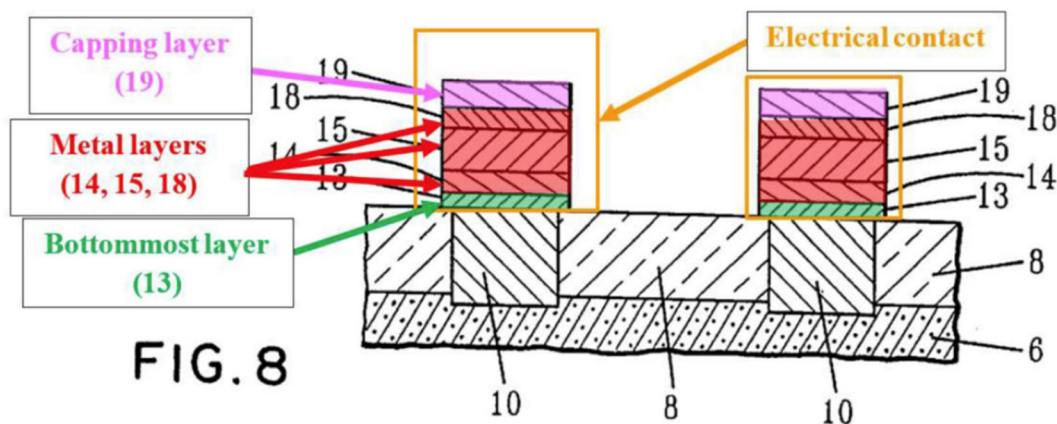
2. Usui’s Interconnect Does Not Meet the Plain Meaning of Electrode Stack Under Either Dictionary Definition

Usui’s interconnect – Fig. 8’s layers 13-15 and 18-19 (Petition, 11) – does not meet the plain meaning of “electrode stack.” POR, 3-4, 16-20.

a. **Usui's Interconnect Does Not Establish Contact with the Semiconductor or Provide the Current Path for Entering/Leaving the Semiconductor**

Merriam-Webster says “a conductor used to establish *electrical* contact with a nonmetallic part of a circuit” is an electrode. EX-2001, 371; POR, 9. Petitioner's assertion that Usui's interconnect meets this because it makes “*physical* contact” with insulator 8 fails. Reply, 9. **Insulator** 8 does not make “electrical contact” with anything. Piner, ¶¶150, 166 (“insulator 8... prevent[s] the flow of current everywhere else[.]”), 171.

Petitioner's assertion that “Usui's interconnect establishes *electrical contact*” with semiconductor 6 (Reply, 10 (emphasis original)) is directly refuted by Usui. Usui is explicit that it is **stud connection 10** that “make[s] connection to a device substrate 6.” Usui, 3:24-27.



Petitioner's Annotated Usui, Fig. 8

Usui's “interconnect” *interconnects* stud connection 10 to another part of a circuit not shown in Fig. 8. Petitioner's assertion that Usui's interconnect

“indirectly connect[ing] the semiconductor *through stud layer 10*” (Reply, 11) meets Merriam-Webster’s first definition fails. Merriam-Webster’s first definition does not encompass every “conductor” – it refers only to “a conductor used *to establish electrical contact* with a nonmetallic part of a circuit.” EX-2001, 371; POR, 18. As shown below, an “interconnect” (red) atop an “electrode” (blue) is distinct from the electrode. EX-2002, [0058], Fig. 6 (annotated below).

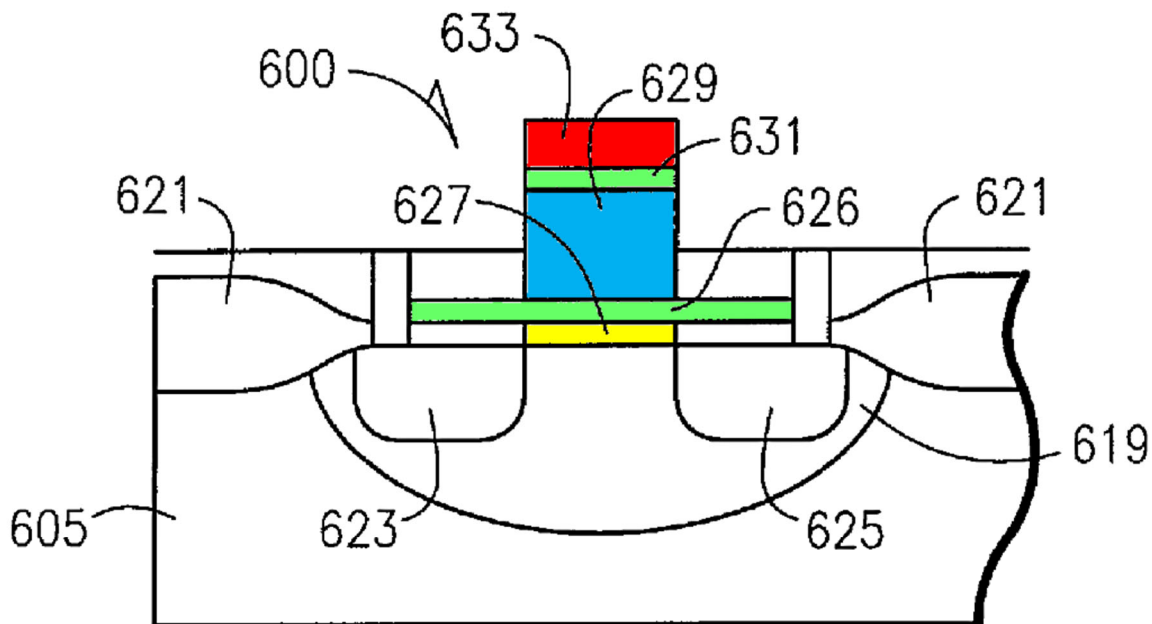


Fig. 6

Petitioner’s assertion that Usui’s interconnect meets Wiley’s dictionary definition fails for similar reasons. Reply, 8-9. Wiley’s definition does not “broadly describe[]” an electrode as *any* conductor. Reply, 8. Only a conductor

that “provides the path for current *entering or leaving* a medium” like a semiconductor meets Wiley’s definition. EX-1046, 237. Usui’s *stud connection 10* is the conductor that provides “the path for current entering or leaving” Usui’s semiconductor 6. Usui, 3:24-27, 5:14-15; Reply, 12 (admitting Usui’s interconnect “connects to semiconductor layer 6 *through a conductive via*” 10).³

If there is an electrode in Usui Fig. 8, *it is – or at least includes – stud connection 10 under either party’s dictionary definition.*

**b. Usui’s Interconnect Does Not Control
Electron/Hole Movement in a Semiconductor**

Merriam-Webster’s second definition says an electrode is “an element in a semiconductor device (*as a transistor*) that emits or collects electrons or holes or controls their movements.” EX-2001, 371. “[C]ontrols” encompasses a transistor gate electrode which controls electron/hole movement through the transistor by turning the transistor on/off. Piner, ¶¶38, 90, 94, 166.

Petitioner’s assertion that Usui’s interconnect “controls the operation of a semiconductor device” by “enabling... current flow” in an integrated circuit fails.

³ Zhao’s conclusory assertion that Usui meets Wiley’s definition (EX-1047, ¶48) warrants no weight because Zhao again merely parrots Petitioner’s assertion. DI, 18-19 (giving no weight to similarly-unsupported Zhao testimony); *Xerox v. Bytemark*, IPR2022-00624, Paper 9, 15 (Aug. 24, 2022).

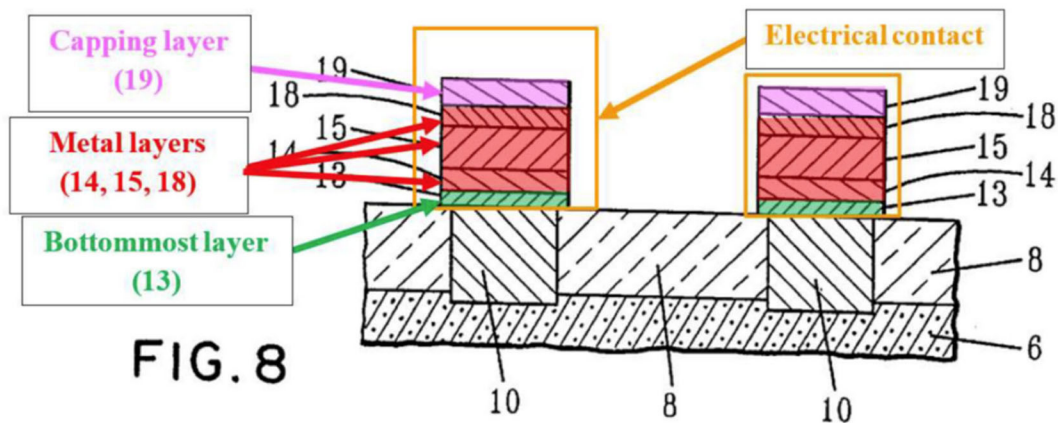
Reply, 13. Usui never says its interconnect somehow controls an (unidentified) device in semiconductor 6. As for an entire “integrated circuit” (*id.*) formed from interconnected semiconductor devices (which Usui nowhere describes), Petitioner never explains how or why Usui’s interconnect that is interconnecting two parts of such a circuit somehow controls the entire circuit.

Finally, even if “controls” were as broad as Petitioner alleges (it is not), without stud connection 10, Usui’s interconnect does not “provide[] electrical connections between” any “devices” or “enabl[e] and influenc[e] current flow.”

Reply, 13. Again, if there is an electrode in Usui Fig. 8, *it is – or at least includes – stud connection 10.*

C. Petitioner’s Exclusion of Usui’s Stud 10 Connection 10 from Any Usui Electrode is Fatal

Petitioner says the claimed “electrical contact” comprising an electrode stack is met by Usui’s interconnect *without* stud connection 10. Petition, 11 (annotating Fig. 8 to identify the alleged “Electrical contact”); Reply, 9-12 (same).



Petitioner's Annotated Usui, Fig. 8

Petitioner took that untenable position because if stud connection 10 is Usui's electrode, or even *part* of Usui's electrode along with the interconnect, Petitioner's Usui-based grounds fail. POR, 11, 19-20. The claims require a capping layer thicker than the *bottommost* metal layer of the electrode stack. POR, 10 (Limitation [1c]). If stud connection 10 is part of Usui's electrode, it is the bottommost metal layer and Usui fails to meet the claims because stud connection 10 is thicker than Usui's alleged capping layer 19. POR, 19-20.

Petitioner says “‘contact stud 10’ is not a layer.” Reply, 10. Even if that were true (it is not), it fails to show that stud connection 10 is not an electrode. POR, 11, 19-20. Petitioner does not even allege that an electrode must be a “layer” and none of the evidence establishing the plain meaning of “electrode” requires that.

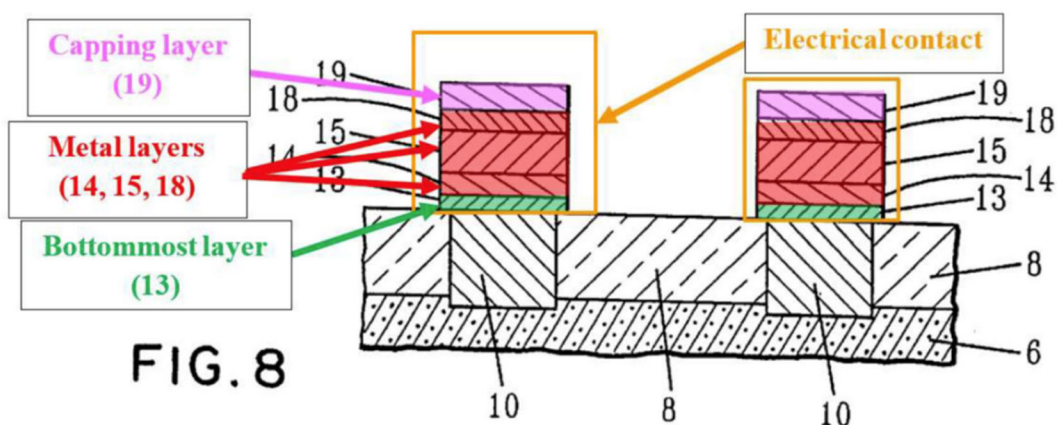
Petitioner's assertion that stud connection 10 is not a “layer” fails to refute Infineon's argument *and evidence* showing that if Usui Fig. 8 discloses an

electrode, then metal contact is that electrode or is at least part of that electrode. *Id.*

That is fatal to Usui-based Grounds 1-4.

D. If the Reply is Read as Arguing that Usui’s Electrode Includes Stud Connection 10 But Still Meets the Claims, that Fails

The Petition never argued that stud connection 10 is part of Usui’s electrode but not the bottommost metal *layer* because stud connection 10 is not a layer. Petitioner was foreclosed from advancing that new argument in Reply. Petition, 11 (annotating Fig. 8 as shown below to identify Usui’s alleged “Electrical contact” comprising an electrode). If the Reply is read as alleging that stud connection 10 is part of Usui’s electrode, that is a new argument belatedly advanced in an attempt to establish *prima facie* obviousness and should not be considered. TPG, §II.I; *Wasica v. Cont’l Auto*, 853 F.3d 1272, 1286-87 (Fed. Cir. 2017).



Petitioner’s Annotated Usui, Fig. 8

Moreover, Petitioner’s assertion that stud connection 10 is “not a layer” (Reply, 10) fails. Usui Fig. 8 shows that stud connection 10 is as much a “layer” as layers 13-15 and 18-19. “[N]othing in Usui suggests that contact metal 10 is not itself a metal layer, or... comprise[s] metal layers.” Piner, ¶153. POSAs “understood that structures like Usui’s contact metal 10 comprise a metal layer or metal layers, which is corroborated by numerous references that illustrate how such structures are made.” *Id.* (citing EX-2032, EX-2033).

Petitioner never explains why “an interplanar conductive via” (Reply, 10) is not a “layer” and no evidence supports that. Usui never says metal stud connection 10 is not a layer. Zhao’s testimony (Reply, 10) merely parrots the Reply and warrants no weight. *Xerox*, IPR2022-00624, Paper 9, at 15. Unlike Zhao, Dr. Piner cited ***corroborating evidence*** supporting his explanation that interplanar vias are formed using metal layer(s). Piner, ¶153. Zhao’s Reply declaration (EX-1047) did not even acknowledge, let alone rebut, Dr. Piner’s testimony or corroborating evidence. Petitioner’s assertion that Usui’s stud connection 10 does not comprise a metal layer fails.

II. GROUNDS 2-4 FAIL FOR ADDITIONAL REASONS

Petitioner never disputes that the law required Petitioner to establish some reason to combine the prior art teachings in the manner claimed and explain the “contemplated workings” of each combination. POR, 22-23. Infineon

demonstrated that the combinations – as alleged in the Petition – for Grounds 2-4 were unworkable. POR, 21-43. Petitioner says Infineon misunderstood its combinations and points to *deposition* testimony of its expert. Reply, 17-18, 20-23. That cannot save Petitioner. The *Petition* needed to state its grounds “with particularity” and provide a “detailed explanation” thereof. POR, 70. The Petition never explained the contemplated workings of its combinations in the manner the Reply belatedly alleges. That is fatal to Grounds 2-4. If the Board considers the combinations as proposed in Reply, they fail as detailed below.

A. Ground 2

1. The Reply Improperly Changes the Petition’s Combination

The Petition said Ground 2 modifies “Usui in view of Yu” (Petition, 16) as opposed to Ground 5 which modifies “Yu in view of Usui” (*id.*, 33). The Petition’s Ground 2 motivation-to-combine argument alleged POSAs would have “implement[ed] the electrical contact *of Usui* with Yu’s gate insulator layer.” Petition, 20. That would have rendered Usui inoperable. POR, 23-26. Petitioner never disputes that. Instead, Petitioner says that is not what its combination was. Reply, 17-18.

The Reply alleges that Ground 2’s “Usui in view of Yu” combination challenging claims 12 and 17 is different from Ground 2’s combination challenging claim 3 which Petitioner admits modified “*Usui’s device*.” Reply, 17

n.2. Petitioner says the challenge to claims 12 and 17 “implements Usui’s” alleged “electrode stack *in Yu’s device.*” *Id.*, 17. The Board should hold Petitioner to the *Petition’s* Ground 2 – “Usui in view of Yu” (*id.*, 16) which indisputably fails for claims 12 and 17. POR, 23-28.

2. Petitioner Fails to Establish Motivation to Combine Usui and Yu in the Manner the Reply Alleges

Petitioner did not demonstrate a supportable reason to combine Usui and Yu in the manner the Reply alleges.

a. KSR’s Rationale Does Not Apply

Ground 2’s motivation-to-combine argument for claims 12 and 17 relied on *KSR’s* known elements/techniques rationale. *Petition*, 20. Petitioner does not dispute that this rationale does not apply to the *Reply’s* combination which changes the function of Usui’s metal layers from being an interconnect to being a transistor electrode. POR, 27 n.10; *Piner*, ¶175; *KSR*, 550 U.S. at 415-416 (rationale *only applies* when prior art elements are combined “with no change in their respective functions.”).

b. Petitioner Does Not Establish that Usui’s Metal Stack Meets Yu’s Gate Electrode Requirements

Yu modified conventional CMOS transistors to replace the materials used for the gate electrodes and insulating layers. Yu, [0004]-[0005]. Yu uses a high-K dielectric gate insulator and metal gate electrodes with “doped-conducting metal oxide (DCO)[s]” chosen to have *sufficiently high work functions and thermal*

stability compatible with the high-K gate insulator. Yu, [0004], [0029]-[0030], [0032]-[0033]; Piner, ¶175; POR, §V.A and 27 n.10. Petitioner never disputes this.

Yu's *two* gate electrodes use *different* metal stacks with different work functions. Yu, [0029]-[0030]. POSAs never would have replaced *both* Yu gate electrodes with Usui's metal stack because that would have yielded the same work function for both gate electrodes. Indeed, Petitioner ignores Yu's work function teachings entirely.

Petitioner says POSAs would have "place[d] the Usui contact in the transistor of Yu" and "include[d] the gate insulator layer." Reply, 17. Some metals "provide *insufficient* work function values and insufficient thermal stability" to work with Yu's high-K gate insulator. Yu, [0032]. Yu used a "doped-conducting metal oxide (DCO)" to "achieve[]" the necessary work function and thermal stability. Yu, [0033]. Usui's metal stack is not a DCO and Petitioner never alleges that Usui's metal stack had a sufficient work function and thermal stability to be compatible with Yu's high-K gate insulator, let alone submit evidence proving it.

Petitioner's failure to establish that Usui's metal layers meet the requirements Yu imposed on its metal gate electrodes to be compatible with Yu's high-K gate insulator is fatal to Petitioner's assertion that POSAs would have

replaced Yu’s carefully-selected DCO metal electrodes with Usui’s metal stack. That is fatal to Ground 2’s challenge to claims 12 and 17.

c. Petitioner Fails to Prove that Electromigration Concerns Would Have Motivated POSAs to Replace Yu’s DCO Metal Gate Electrodes

The Petition alleges POSAs would have used Usui’s metal stack in Yu to “improv[e] electromigration characteristics” Petition, 20. The Petition equated “electromigration” with “current flow” and alleged POSAs wanted to increase it. Petition, 31 (“improved current flow (i.e., enhanced electromigration)”). Both experts agree electromigration is not “current flow” and is something POSAs sought to *reduce*. POR, 29 n.11, 36, 40. The *Petition*’s motivation-to-combine argument fails.

The Reply attempts to gaslight the Board by saying both experts agree that electromigration is what *Infineon*’s *POR* explained. Reply, 18-19. That confirms that the *Petition*’s assertion that electromigration equates to current flow was wrong. Petition, 31.

i. The Reply’s New Electromigration Argument Fails

The Reply’s new argument that POSAs would have replaced Yu’s carefully-chosen DCO metal gate electrodes to use Usui’s metal stack to *reduce* electromigration fails. Petitioner does not dispute that Usui teaches a metal stack for *interconnect wires* to mitigate electromigration due to high current density.

Usui, 1:30-41, 2:33-39; POR, §IV.D.2. That was not a concern for Yu’s *gate* electrode which does not experience high current density. Piner, ¶175. Petitioner’s assertion that “HEMT power transistors often have high current flows and densities, including in ohmic contacts, which can cause electromigration” (Reply, 16) does not help Petitioner because Yu is a CMOS (not HEMT) device and its gate electrodes are *insulated* so they do not make ohmic contact with the semiconductor. Piner, ¶¶291, 210, 284-285; EX-1002 (Zhao-Dec.), ¶¶56-57. Petitioner’s assertion that “an Infineon patent” “identif[ies] electromigration as a problem for *gate* electrodes” fails. Reply, 19. EX-1043 is published application with numbered paragraphs, so Petitioner’s column:line citations make no sense. Reply, 19. Moreover, “electromigration” appears once in EX-1043 ([0004]) and never in connection with a gate electrode like Yu’s.

The Reply’s new argument that “[*g*] *ate leakage* can also cause electromigration in gate electrodes” (Reply, 16 (citing EX-1015)) should not be considered. TPG, §II.I; *Wasica*, 853 F.3d at 1286-87. If considered, Petitioner’s argument that electromigration from “gate leakage” is a concern for Yu’s *insulated* gate electrode fails.⁴ EX-1018 never mentions “electromigration” let alone teach

⁴ Gate leakage being “problematic for Schottky connections” (Reply, 16, 22) is irrelevant because Yu’s *insulated* gate electrode has no Schottky connection.

that gate leakage causes electromigration. Worse yet, EX-1018 says gate leakage is addressed by using a *gate insulator*, including a “(high-k)” insulator like Yu’s. EX-1018, 1; Yu, [0006], [0028]; Petition, 4 (admitting insulators “address gate leakage”). This proves *Infineon’s* point that there was no electromigration concern for Yu’s *insulated* gate electrode. EX-1018, 1; Yu, [0004]; POR, 27, 44, 71.

d. Conclusion

Petitioner fails to establish any supportable reason why POSA’s would have replaced the DCO metal gate electrodes Yu specifically chose to have work functions and thermal stability compatible with Yu’s high-K gate dielectric.

B. Ground 3

1. Claims 11 and 16

The POR explained that Ground 3 (“Usui in View of Yu and... Adesida,” Petition, 24) fails because the Petition never explained the contemplated workings of the combination, Adesida’s Schottky gate electrode established no reason to modify Usui, and having Usui’s alleged electrode make Schottky contact with Usui’s semiconductor would have rendered Usui inoperable. POR, 28-36.

Petitioner criticizes Infineon’s understanding of the *Petition’s* Usui-Yu-Adesida combination – alleging “[n]o such combination is depicted or described in the Petition.” Reply, 21. But Petitioner identifies no *other* Usui-Yu-Adesida combination “depicted or described in the Petition.” That is fatal. POR, 32-34 (the

Petition needed to explain the “contemplated workings” of this combination to establish obviousness).

Zhao’s deposition and the Reply (Reply, 20-21) are too late to explain the combination. TPG, §II.I. The Reply says the combination is a “Schottky gate structure on III-V semiconductor HEMT *device*” ***as taught by Adesida*** “with the metal layers taught by Yu and Usui as the gate.” Reply, 20-21. This new argument that makes Adesida the primary reference should not be considered. TPG, §II.I.

If considered, Petitioner’s new Reply combination fails. Petition again fails to describe the contemplated workings of its Usui-Yu-Adesida combination.

Petitioner says “***metal layers taught by Yu and Usui [are used] as the gate***” (Reply, 20-21) but ***never identifies*** which Yu layers and which Usui layers are in the Usui-Yu-Adesida combination. POR, 32-34. Nor has Petitioner explained “where those [unidentified] layers... would go in the combination, and what the thicknesses of the relevant layers would be after the references are combined.” Piner, ¶190. Petitioner’s failure to explain the “contemplated workings” of the Reply’s new Usui-Yu-Adesida combination is fatal. POR, 32-33 (citing *Personal Web*).

Petitioner also failed to establish any ***reason*** to combine Usui, Yu, and Adesida in the claimed manner. POR, 28-32. Petitioner says Infineon “misunderst[ood] the interchangeability of ***such*** materials” but never even explains

what Yu and Usui materials were allegedly “interchangeab[le],” let alone provide *evidence* proving interchangeability. Reply, 21-22.

Petitioner’s assertion that POSAs “would have recognized the benefits of Usui’s electromigration protections in Yu’s system, as discussed for Ground 2” (Reply, 21-22) fails for the reason discussed *supra* §II.A.2.c. That argument also fails because Petitioner never identifies what aspect of “Yu’s system” is even present in the Usui-Yu-Adesida combination. Yu discloses a Complementary Metal ***Oxide*** Semiconductor (“CMOS”) transistor (Yu, title) where the oxide insulates the gate electrode. Yu, [0028], Fig. 2E. POSAs never would have eliminated the insulator from Yu’s gates electrodes to make Schottky contact.

Finally, Petitioner’s Reply cannot keep its story straight. Petitioner’s sole alleged basis for modifying Yu’s transistor based on Usui is to *reduce* electromigration (Reply, 19-20) which Petitioner alleges is caused by gate leakage that is “especially problematic for Schottky connections” (Reply, 16). Petitioner’s assertion that POSAs would have then modified Petitioner’s Usui-Yu combination to use a Schottky gate electrode – that Petitioner says would exacerbate

electromigration (Reply, 16) – is based on nothing but hindsight.⁵ Petitioner’s nonsensical Ground 3 Reply arguments should be rejected.

2. Claims 9 and 14

The Petition’s motivation-to-combine arguments for these claims fail. POR, 36. Petitioner never refutes that its “simple design choice” and *KSR* “known elements” rationales fail because there would have been substantial complexities in converting Yu’s transistor into a HEMT. *Id.*

C. Ground 4

The Petition fatally never explained what Yu teachings are used in its Usui-Yu-Sugimoto combination nor how the Usui-Yu electrode allegedly would have been modified to make ohmic contact with Usui’s semiconductor. POR, 37-39. Petitioner again criticizes Infineon’s understanding of the combination and then seeks to change the *Petition’s* Ground 4 combination through expert deposition testimony. Reply, 22-23. That fails for the same reasons discussed *supra* §II.B.1.

If Petitioner’s Reply arguments are considered, they still fail to explain the contemplated workings of the Usui-Yu-Sugimoto combination. Petitioner says “we are using Usui and *Yu’s teaching of those metal layers* to form ohmic contact”

⁵ Petitioner’s assertion that POSAs would have eliminated Yu’s gate insulator fails because Yu’s entire disclosure is about improving CMOS transistors by using a high-K gate insulator. Yu, Abstract, [0004]-[0006].

(Reply, 22) and that “*Usui-Yu’s* contact [is used] as a power electrode” (*id.*, 23). Petitioner does not identify what Yu “metal layers” are used in the combination, what Usui “metal layers” are used in the combination, and how they are used together. Even after Reply, Petitioner provides “no details regarding which layers... from which references (Usui, Yu, and Sugimoto) are incorporated into Petitioner’s combination, where those layers... would go in the combination, and what the thicknesses of the relevant layers would be after the references are combined.” Piner, ¶209. That is fatal to Ground 4. POR, 39 (*Personal Web* requires an explanation of the contemplated workings of the combination).

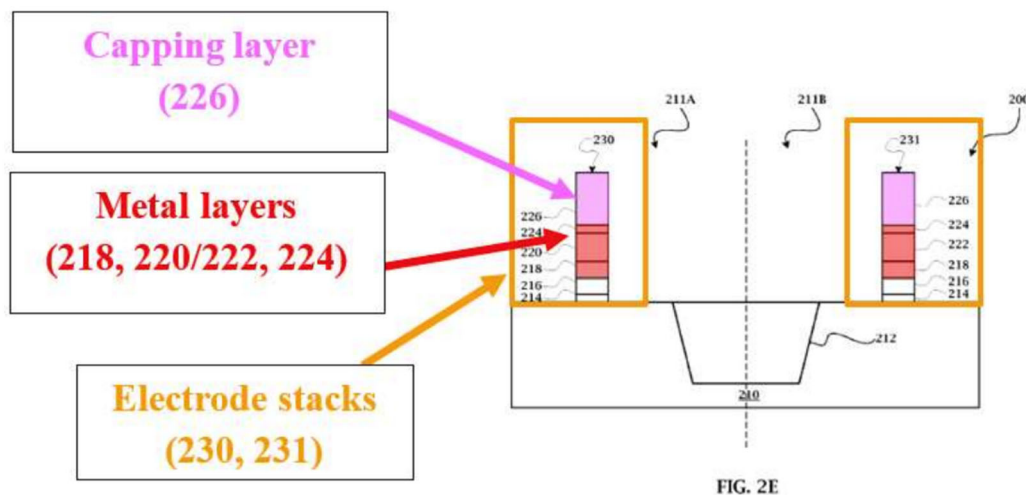
Moreover, the Petition’s single conclusory paragraph purporting to establish a motivation to combine fails. POR, 39-42. Petitioner fails to meet the factual predicate for *KSR’s* “known elements” rationale (Petition, 31) that there is no change in the function of any of the combined elements. POR, 41-42. Indeed, the combination changes the function of Usui’s metal stack from being used for an interconnect to being an electrode making ohmic contact to create a transistor power electrode. *Id.* Lauding the benefits of ohmic contacts (Reply, 23-24) does not help Petitioner because it establishes no reason to use *Usui’s* metal stack (modified in some unexplained way by Yu’s *gate* electrode stack) as an ohmic contact.

The Petition's only other motivation-to-combine argument says the combination provides "improved current flow (*i.e.*, enhanced electromigration)." Petition, 31. The Reply does not refute that enhanced electromigration is not the same thing as "improved current flow." POR, 39-41. The Petition's motivation-to-combine argument fails and the Reply offers no alternative motivation-to-combine argument for Ground 4.

III. YU-BASED GROUNDS 5-7 FAIL

On the pre-institution record, the Board found that Grounds 5-7 fail. DI, 18-19. The same conclusion is compelled on the fully-developed record. Ground 5 fails for multiple reasons that are all inherited by Grounds 6-7. POR, 43-69.

The Petition's identification of Yu's alleged electrode stack (Petition, 42) is reproduced below:



Petitioner's Annotated Yu, Fig. 2E

Petitioner alleged that diffusion barrier/protection layer 218 is the bottommost metal layer of Yu's electrode stack and is thinner than capping layer 226. Petition, 43-44. The POR explained that (1) Petitioner failed to establish that barrier layer 218 is a layer of Yu's electrode stack (POR, 48-55) and (2) even if it is, Petitioner failed to demonstrate that POSAs would have made Yu's capping layer 226 thicker than barrier layer 218 when formed from the materials Petitioner relies on to purportedly meet the claims (POR, 55-68). The Board did not comment on argument (1) but credited argument (2). DI, 18-19.

A. The Board Correctly Found that Petitioner Fails to Establish that POSAs Would Have Made Yu's Capping Layer Thicker than Yu's Alleged Bottommost Metal Layer When Formed from the Materials Petitioner Relies On

1. Petitioner Fails to Support Its Alleged Thickness for a Refractory Metal Nitride Capping Layer

Limitation [1c] requires a refractory metal nitride capping layer thicker than the electrode stack's bottommost metal layer. Petitioner admits "Yu does not expressly disclose the claimed thickness of [1.C]." Reply, 27; *see also* POR, 56.

a. Yu Does Not Say the Same Thickness Used for Polysilicon is Used for a Refractory Metal Nitride

The Petition cited Yu's disclosure of a *polysilicon* capping layer thickness of 600Å and alleged POSAs would have used the same thickness for a refractory metal nitride capping layer (Petition, 38) because "these thicknesses apply to Yu's capping... layer regardless of whether Yu's capping layer is comprised of

polysilicon or titanium nitride or tantalum nitride” (*id.*, 43). The Petition’s assertion that “these [same] thicknesses apply” was unsupported and wrong. POR, 58. As the Board found: “Petitioner [did] not adequately explain why a POSITA would have replaced Yu’s polysilicon capping layer with a titanium nitride or tantalum nitride layer *with the same thickness* as the polysilicon layer.” DI, 18 (emphasis original). The Board gave no weight to Zhao’s testimony that “mirror[ed] the statements in the Petition without providing further technical explanation or additional evidence in support thereof.” DI, 19 (citing *Xerox*).

The only proper Reply would have been to demonstrate where the ***Petition*** provided evidence and argument supporting its assertion that “these [same] thicknesses apply.” Petition, 43. That was required to establish *prima facie* obviousness. Petitioner cannot present new argument and evidence in Reply in an attempt to belatedly establish *prima facie* obviousness. TPG, §II.I; *Wasica*, 853 F.3d at 1286-87 (changing arguments in Reply after the Petition’s argument is shown to fail is “foreclosed by statute, our precedent, and Board guidelines”). The Board’s invitation to “develop these arguments further at trial” was limited “***to the extent permitted under our rules.***” DI, 19. Petitioner’s new Reply arguments and evidence are not permitted and should not be considered. If considered, these arguments fail.

Petitioner does not dispute that Yu says its preferred capping layer thickness varies for different materials and never discloses a capping layer thickness for the refractory metal nitrides Petitioner relies upon. POR, 56; Yu, [0036]. That is fatal to the Petition’s argument that “these [same] thicknesses apply.” Petition, 43.

The Reply newly alleges that Yu’s disclosure of a range of thickness for some metals “includes 600Å” – the preferred polysilicon thickness. Based on this, the Reply states in conclusory fashion that “it would have been obvious that the capping layer would have had a thickness of 600” which is “suitable” for a refractory metal nitride capping layer. Reply, 28. This new argument should not be considered. If considered, this argument fails because the Reply never even attempts to explain how or why 600Å is a “suitable” or “obvious” thickness for a refractory metal nitride capping layer and no such explanation can be incorporated by reference from Zhao’s deposition testimony. 37 C.F.R. §42.6(a)(3). Moreover, Zhao’s deposition testimony is uncorroborated and warrants no weight. No *credible evidence* supports the Reply’s new argument.

b. Usui Would Not Have Motivated POSAs to Make Yu’s Refractory Metal Nitride Capping Layer Thicker Than Yu’s Barrier Layer

Petitioner alternatively argued that Usui would have motivated POSAs to make Yu’s capping layer thicker than its barrier layer 218. Petition, 39. The Board correctly rejected this too: “Petitioner does not explain, on this record, why

limiting the thickness of Yu's diffusion barrier/protection layer 218 would result in a titanium nitride or tantalum nitride capping layer 226 in Yu having a greater thickness than diffusion barrier/protection layer 218 if the thickness of the titanium nitride or tantalum nitride capping layer is not known." DI, 19. The POR cited extensive evidence showing that Usui's teachings have no bearing on the thicknesses of Yu's layers. POR, 63-68. The Reply fails to refute any of this evidence.

2. Petitioner Did Not Establish the Thickness of a Titanium Bottommost Metal Layer

The Petition relied on a *titanium* barrier layer 218. Petition, 36 (POSAs were "motivated to use *titanium* as **diffusion barrier/protection layer 218**"); POR, 62. Yet, the thickness Petitioner relied on (20Å) is for a *titanium nitride* layer 218 and Yu never says a *titanium* layer 218 would have the same thickness. POR, 62. The Reply does not dispute any of this. That is fatal to the *Petition's* Grounds 5-7. POR, 62-63.

In Reply, Petitioner changes its argument and alleges that a *titanium nitride* "TiN" barrier layer 218 of 20Å "is the claimed bottommost layer." Reply, 27. That is improper and should not be considered. TPG, §II.I; *Wasica*, 853 F.3d at 1286-87.

B. Petitioner Failed to Establish that Yu's Barrier Layer is Part of Yu's Electrode

The Petition alleged Yu's barrier layer 218 is the bottommost metal layer of Yu's electrode stack but failed to prove that the barrier layer is part of Yu's "electrode stack." POR, 49-54. The Petition's *only* argument was that barrier layer 218 is part of Yu's electrode stack because it is part of Yu's "metal gate stack" (230, 231), which Petitioner equated to the claimed electrode stack. Petition, 42, 44-45 (annotating Yu Fig. 2E as shown below). The intrinsic evidence is clear that for an insulated gate electrode like Yu's, the "electrode stack" is *not* the entire gate stack. POR, 49-54. That is fatal to Grounds 5-7 because the Petition failed to establish that the layer 218 it mapped to the claimed bottommost metal layer of the *electrode stack* is even part of Yu's electrode stack in the first place. POR, 55.

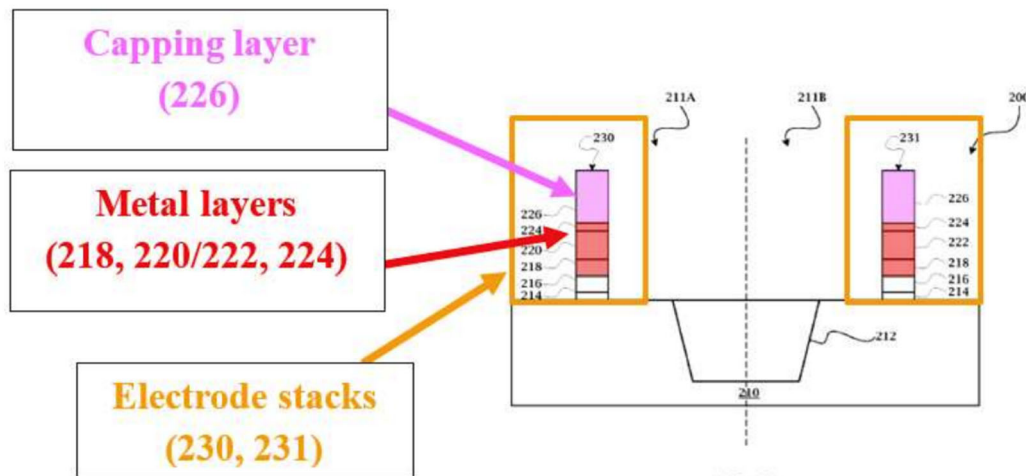


FIG. 2E

Petitioner's Annotated Yu, Fig. 2E

The Reply's assertion that barrier layer 218 is the "bottommost layer of the plurality of metal layers" (Reply, 28) is non-responsive because it ignores that the

claimed bottommost layer is of “*said* plurality of metal layers” in the *electrode stack*. POR, 55. Petitioner equating Yu’s *entire* “metal gate stack” (POR, 47; Yu, [0038]-[0039]) with the claimed “electrode stack” was far more than a “semantic” error (Reply, 26) – it demonstrates that the Petition’s *sole* argument for why barrier layer 218 is part of Yu’s electrode stack failed.

Petitioner seeks to change its argument in Reply by now alleging that Yu’s electrode stack is everything other than the dielectrics. Reply, 26-27. Petitioner’s assertion that “Dr. Zhao clarified” during deposition “that he drew the ‘yellow box on 230, 231 just to highlight this component of Yu as important’” is irrelevant and not credible. *Id.* The *Petition* unambiguously identified Yu’s entire metal gate stacks (230, 231) as the claimed “electrode stacks.” Petition, 42 (“metal gate stacks 230, 231 (electrode stacks)” and “Electrode stacks (230, 231)”). The *statutory* requirement that the Petition state its grounds “with particularity” forecloses Petitioner from shifting its argument in Reply, based on an expert’s alleged “clarification” at deposition, after the Petition’s argument was shown to fail. *Wasica*, 853 F.3d at 1286-87.

If considered, Petitioner’s new argument fails. Petitioner’s assertion that barrier layer 218 is part of Yu’s electrode ignores that “barrier layer 218 may be omitted.” Yu, [0029]. Barrier layer 218 sits *between* Yu’s electrode and insulating layers and prevents their materials from diffusing into each other. Yu, [0029].

*Petitioner does not dispute the evidence establishing that this is what Yu’s diffusion barrier layer does, and that such a “barrier layer 626” (green) in an insulated gate stack is **distinct** from a “gate electrode 629” (blue) and “gate oxide layer 627” (yellow). EX-2002, [0057]-[0058], Fig. 6 (annotated below); Piner, ¶¶236-237; POR, 47-48.*

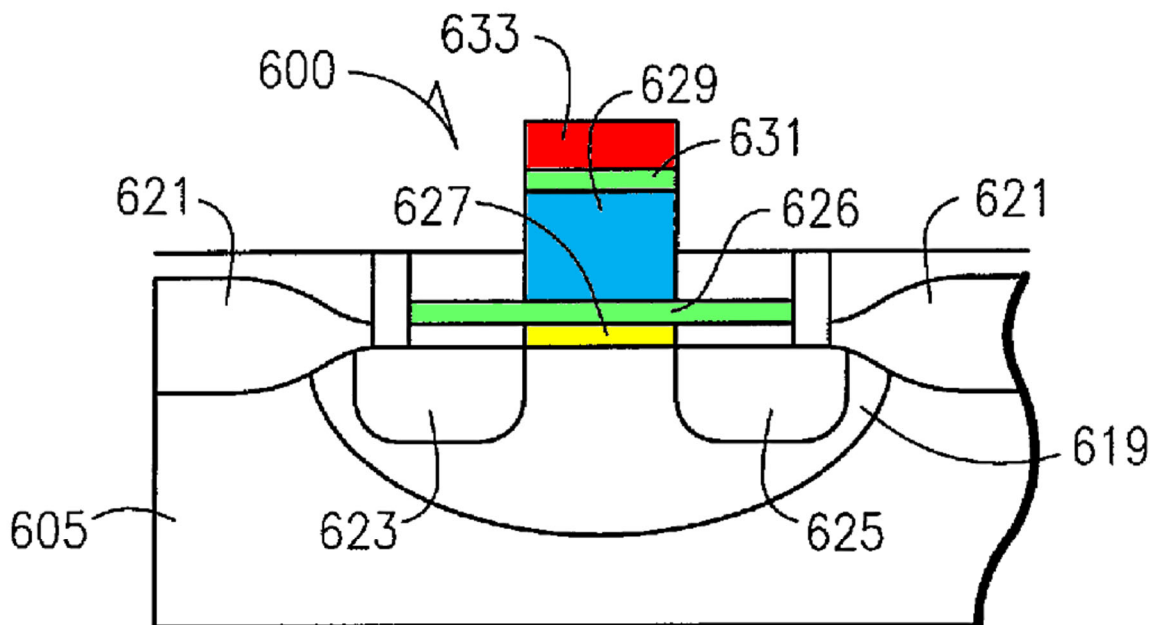


Fig. 6

Petitioner obfuscates. There is no “contradict[ion]” in explaining that Yu’s entire metal gate stack includes layers that are not part of the electrode. Reply, 27. Petitioner concedes as much by not disputing that insulating layers 214, 216 are not part of Yu’s electrode stack. Petitioner’s assertion that the intrinsic record does

not explicitly “exclude” a diffusion barrier layer from the electrode stack is irrelevant because the specification does not disclose a diffusion barrier layer. *Id.*

Petitioner failed to carry its burden to show that Yu’s barrier layer 218 is part of Yu’s “electrode stack.” This is fatal to Yu-based Grounds 5-7.

C. Grounds 6-7 Fail for Additional Reasons

Ground 6 is facially deficient for claims 11 and 16 because the Petition mapped the “gate electrode” in those dependent claims to Adesida’s gate electrode rather than the electrode the Petition mapped to the independent claims from which claims 11 and 16 depend. POR, 69-72. Petitioner again asks the Board to discard the Petition’s annotations (to Adesida Fig. 5) and arguments (Petition, 60-61) and accept the explanation of its expert at deposition of what Petitioner “meant” to allege. Reply, 29. The Reply’s new assertion that the gate electrode in claims 11 and 16 is met by an electrode with unidentified “metal layers from Usui and Yu” (Reply, 28-29) should not be considered. TPG, §II.I. Petitioner also has no answer for evidence showing that “a Schottky gate electrode for a CMOS device like Yu’s... would be highly unconventional and is the furthest thing from a ‘simple design choice.’” POR, 71; Piner, ¶¶284-285.

Even if everything Ground 7 alleged was true, the Petition failed to demonstrate that its Yu-Usui-Sugimoto combination meets both independent claims 1 and 13 and claims 10 and 15 (which Ground 7 challenges) depending

therefrom. POR, 72-76. The Reply fabricates a new combination based on deposition testimony from Petitioner's expert. Reply, 29. The Board should hold Petitioner to the ***Petition's*** failed Ground 7. If considered, the Reply's new Ground 7 fails. Petitioner fails to rebut Dr. Piner's explanation that if the electrode stacks of Yu or Yu-USUI were used as a power electrode making ohmic contact (Reply, 29), the electrode materials and thicknesses would have to change "because ohmic contacts are closely tailored to the semiconductor." POR, 76 (citing Piner, ¶¶48-57).

Respectfully submitted,

Date: February 3, 2026

/Richard Giunta/

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing **PATENT OWNER'S SUR-REPLY TO PETITIONER'S REPLY** contains 5,599 words excluding; a table of contents, a table of authorities, a certificate of service or word count, or appendix of exhibits or claim listing. Patent Owner has relied on the word count feature of the word processing system used to create this paper in making this certification.

Date: February 3, 2026

/MacAulay Rush/
MacAulay Rush
Paralegal
WOLF, GREENFIELD & SACKS, P.C.

CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.6 (e)(4)

I certify that on February 3, 2026, a copy of the foregoing document, including any exhibits filed therewith, is being served via electronic mail, as previously consented to by Petitioner, upon the following:

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