Innoscience

Case No: IPR2025-00175
Patent No. 8,686,562

Petitioner's Demonstrative Exhibits

Innoscience America, Inc.
v. Infineon Technologies Austria AG

April 9, 2026

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

INNOSCIENCE EXHIBIT 1048
INNOSCIENCE v. INFINEON
IPR2025-00175

Table of Contents

Innoscience

All claims challenged

1. Usui Grounds

2. Yu Grounds

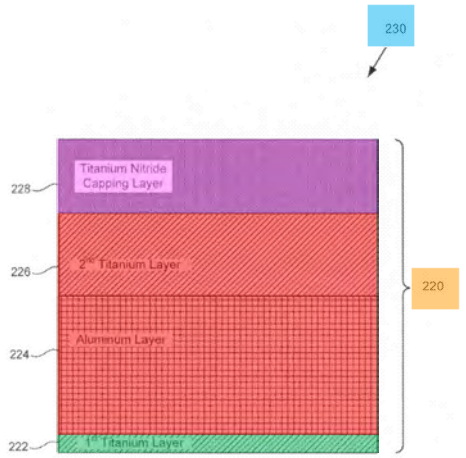
Petition	Slides
Overview of the ’562 Patent	3-7
Claim Construction	8-22
Invalidity Grounds	23-29
Ground 1: **Usui** anticipates claims 1, 2, and 4-7	30-70
Ground 2: **Usui**, Yu discloses claims 3, 8, 12, 13, and 17	71-93
Ground 3: **Usui**, Yu, Adesida discloses claims 9, 11, 14, and 16	94-104
Ground 4: **Usui**, Yu, Sugimoto discloses claims 10 and 15	105-114
Ground 5: **Yu**, Usui discloses claims 1-8, 12, 13, and 17	115-142
Ground 6: **Yu**, Usui, Adesida discloses claims 9, 11, 14, and 16	143-152
Ground 7: **Yu**, Usui, Sugimoto discloses claims 10 and 15	153-163
Summary	164-166

Pet., 1-8; *see generally* Reply.

Overview of the ’562 Patent

The ’562 patent

Claim 1: Electrical contact



[1p] An **electrical contact** for use on a semiconductor device, said electrical contact comprising:

[1a] an **electrode stack** including a **plurality of metal layers** and a **capping layer** formed over said plurality of metal layers;

[1b] said **capping layer** consisting only of a refractory metal nitride,

[1c] said **refractory metal nitride** forming a top of said **electrical contact** and having a thickness greater than that of a **bottommost layer** of said plurality of metal layers.

17 claims total

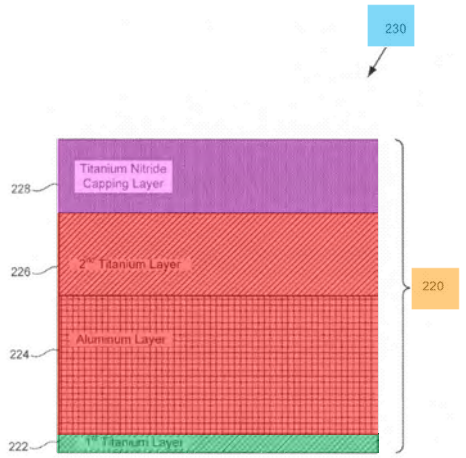
Four claim elements:

1. Electrical contact — Undisputed
2. Electrode stack of metal layers — Disputed
3. Refractory metal nitride capping layer — Undisputed
4. Capping layer is thicker than bottommost metal layer — Disputed

’562 patent, claim 1, Fig. 2 (annotated); Pet., 5-8; Reply, 2-16, 24-28.

The ’562 patent

Claim 1: Electrical contact



[1p] An **electrical contact** for use on a semiconductor device, said electrical contact comprising:

[1a] an **electrode stack** including a **plurality of metal layers** and a **capping layer** formed over said plurality of metal layers;

[1b] said **capping layer** consisting only of a refractory metal nitride,

[1c] said **refractory metal nitride** forming a top of said **electrical contact** and having a thickness greater than that of a **bottommost layer** of said plurality of metal layers.

Usui dispute:

Claim construction of “electrode stack”.

“Electrode stack” is more than just a source, drain, Schottky gate, or insulated gate electrode. If the Board agrees, then Usui discloses all limitations of claim 1.

Yu dispute:

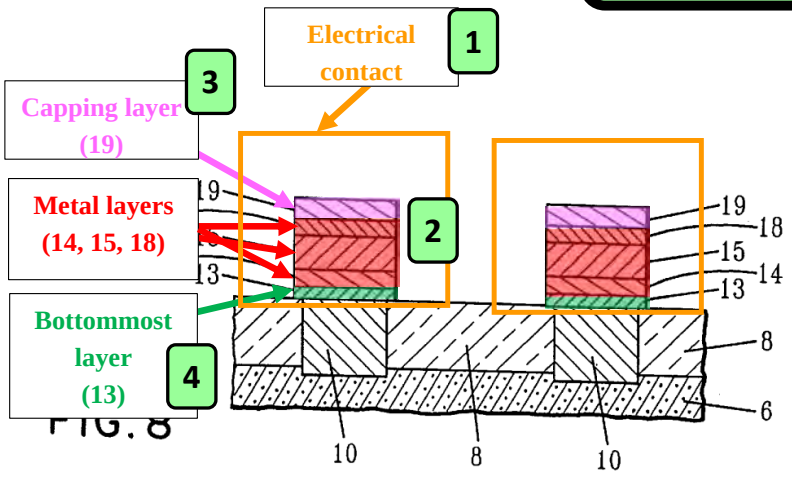
Obviousness of Yu.

Patent Owner misinterprets Yu’s explicit disclosure of claim limitation [1c] in ¶36. If the Board agrees, then Yu discloses all limitations of claims 1 and 13.`

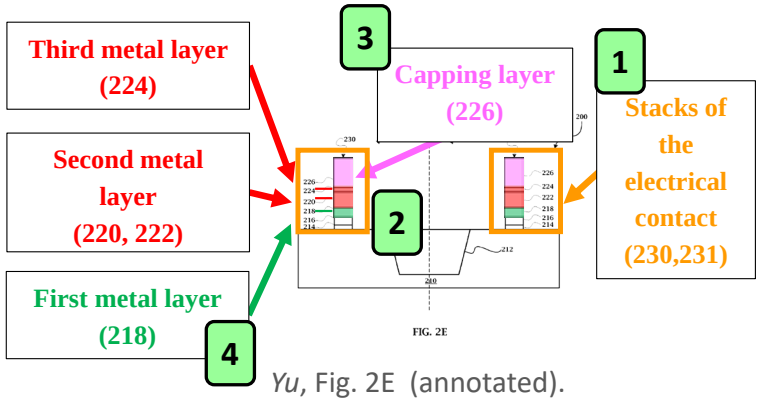
’562 patent, claim 1, Fig. 2 (annotated); Reply, 2-16, 27-28.

Usui and Yu

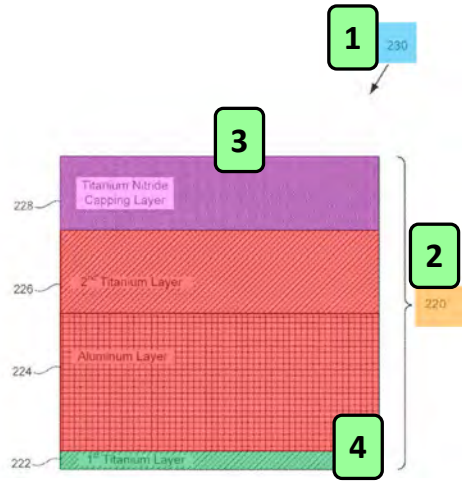
Usui and Yu disclose all 4 claim elements



Usui, Fig. 8 (annotated).



Yu, Fig. 2E (annotated).



'562 patent, Fig. 2 (annotated).

Pet., 5-6, 8-13, 33-39, 41-46.

Usui and Yu

Patent Owner argues:	But Patent Owner's arguments fail because:
☒ "Electrode stack" is only source, drain, Schottky gate, or insulated gate electrode.	✓ The patent does not limit "electrode stack" to those examples. Usui discloses an electrical contact and an electrode stack.
☒ No motivation to combine Usui and other references because Usui does not disclose a transistor gate electrode and its metal stack is separated from semiconductor wafer 6.	✓ Patent Owner gets combination backwards. Petitioner's true combination is using the capping and metal layers of Usui to modify secondary references.
☒ Yu does not disclose a refractory metal nitride capping layer that is thicker than the bottommost metal layer.	✓ Yu discloses "capping layer 226 may comprise … titanium nitride, tantalum nitride … and comprise a thickness between about 50 Å and about 1,000 Å" (Yu, ¶36) and "the diffusion barrier/protection layer 218 [bottommost metal layer] comprises TiN, which is deposited by PVD to a thickness of approximately 20 Å" (Yu, ¶29).
☒ No motivation to combine Yu and other references because POSITA would not have combined Yu's insulating layers with other references and because Yu discloses a gate.	✓ Patent Owner gets combination backwards. Petitioner's true combination is using the capping and metal layers of Yu, not its insulating layers.

See generally Pet.; *see, e.g.,* Pet., 8-12, 16-39, 43-46, 55-64; Reply, 2-18, 20-23, 27-29; POR, 3-10, 23-27, 29, 37-38, 43-47, 55-76.

Innoscience

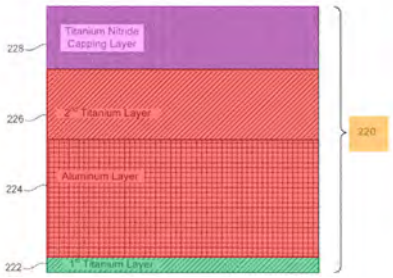
Claim Construction

The intrinsic and extrinsic records show that the plain and ordinary meaning of "electrode stack" prevails

Innoscience

Claims 1, 5-7, 12, 13, and 17: "electrode stack"

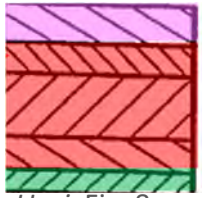
Patent Owner's Proposed Construction	Petitioner's Proposed Construction
a stack of conductive layers that forms an electrical contact that is part of a semiconductor device and used to (1) establish contact with a nonmetallic part of the semiconductor device (like the source, drain and Schottky gate electrodes in the '562 Patent Specification) or (2) controls the operation of the semiconductor device (like the insulated or Schottky gate electrodes in the '562 Patent Specification)	Plain and ordinary meaning



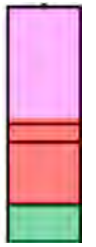
'562 patent, Fig. 2 (annotated).

Patent Owner contends the "electrode stack" *must* be used as a Schottky gate, ohmic, or gate; it cannot be an interconnect

Petitioner showed the claims, specification, and extrinsic evidence do not limit "electrode stack"; it includes an interconnect



Usui, Fig. 8 (annotated).



Yu, Fig. 2E (annotated).

Pet., 6, 9, 11, 35; Reply, 2-13; POR, 8-9.

The intrinsic and extrinsic records show that the plain and ordinary meaning of "electrode stack" prevails

Innoscience

Plain and Ordinary Meaning of "electrode stack" Prevails Because:

1A
The claims do not limit the term "electrode stack" beyond its plain and ordinary meaning.

1B
The specification does not define the term "electrode stack" or disavow its full scope.

1C
The extrinsic record does not support Patent Owner's narrow interpretation of "electrode stack".

Reply, 2-8.

Patent Owner inappropriately equates "electrode stack" to "electrical contact"

Innoscience

1. The claims never require the "electrode stack" to make ohmic (source/drain) or Schottky contact.

2. Instead, dependent claims require the "electrical contact" to be ohmic (source/drain) or Schottky.

10. The electrical contact of claim **8**, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.

11. The electrical contact of claim **8**, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

'562 Pat., claims 10, 11 (annotated).

15. The electrical contact of claim **13**, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.

16. The electrical contact of claim **13**, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

'562 Pat., claims 15, 16 (annotated).

1A
The claims do not limit the term "electrode stack" beyond its plain and ordinary meaning.

Reply, 2-7; Ex-1047, ¶¶16-21; POR, 4-9;
'562 Pat., claims 1, 10, 11, 13, 15, 16.

Patent Owner's construction of "electrode stack": stack of conductive layers that forms an electrical contact that is part of a semiconductor device and used to (1) establish contact with a nonmetallic part of the semiconductor device (like the source, drain and Schottky gate electrodes in the '562 Patent Specification)

The claims do not limit "electrode stack"

Innoscience

1. An electrical contact for use on a semiconductor device, said electrical contact comprising:
an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;

5. The electrical contact of claim 4, wherein said first metal layer and said third metal layer of said electrode stack comprise titanium (Ti).
6. The electrical contact of claim 4, wherein said second metal layer of said electrode stack comprises aluminum (Al).
7. The electrical contact of claim 6, wherein said second metal layer of said electrode stack further comprises silicon (Si).

12. The electrical contact of claim 8, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

13. An electrical contact for use on a group III-V semiconductor device, said electrical contact comprising:
an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;

17. The electrical contact of claim 13, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

Nothing in the claims limits or alters the plain meaning of "electrode stack."

The claims use open-ended language "comprises" or "includes."

1A
The claims do not limit the term "electrode stack" beyond its plain and ordinary meaning.

Reply 2-5; Ex-1047, ¶¶16-21;'562 Pat., claims 1, 5-7, 12, 13, 17 (annotated).

The claims do not limit "electrode stack"

Innoscience

"electrode stack" of the independent claims is *broader* than an insulated gate electrode.

12. The electrical contact of claim 8, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

17. The electrical contact of claim 13, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

Patent Owner's construction of "electrode stack": stack of conductive layers that forms an electrical contact that is part of a semiconductor device and used to (2) controls the operation of the semiconductor device (like the insulated or Schottky gate electrodes in the '562 Patent Specification)

1A
The claims do not limit the term "electrode stack" beyond its plain and ordinary meaning.

Reply 2-5; Ex-1047, ¶¶16-21; POR, 8-9; '562 Pat., claims 1, 12, 17 (annotated).

Patent Owner inappropriately equates "electrode stack" to "electrical contact"

Innoscience

"electrical contact" is broader than "electrode stack"

1. An electrical contact for use on a semiconductor device, said electrical contact comprising:
an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;

'562 Pat., claim 1 (annotated).

Patent Owner's construction of "electrode stack": stack of conductive layers that forms an electrical contact that is part of a semiconductor device …

POR, 4-9.

Dr. Zhao says "electrical contact" is broader than "electrode stack"

A. There are different ways to make ohmic contact. And as I previous state in my analysis of declaration, the contact that I analyzed is in 562, claim one, which is the electrode stack includes metal layers and capping layer, and anything that is outside this metal layer, or capping layer is unclaimed.

Ex-2026, 10:3-8 (annotated).

1A
The claims do not limit the term "electrode stack" beyond its plain and ordinary meaning.

Reply, 2-7; Ex-1047, ¶¶16-21.

Patent Owner's expert Dr. Piner agrees!

stack." EX-1001, 5:54–63. Hence, the electrode stack is at least a part of an *electrode* in the electrical contact for use on a semiconductor device.

Ex-2024, ¶81 (Dr. Piner) (annotated).

The intrinsic and extrinsic records show that the plain and ordinary meaning of "electrode stack" prevails

Innoscience

Plain and Ordinary Meaning of "electrode stack" Prevails Because:

1A
The claims do not limit the term "electrode stack" beyond its plain and ordinary meaning.

1B
The specification does not define the term "electrode stack" or disavow its full scope.

1C
The extrinsic record does not support Patent Owner's narrow interpretation of "electrode stack".

Reply, 2-3; Ex-1047, ¶¶16-21.

The intrinsic and extrinsic records show that the plain and ordinary meaning of "electrode stack" prevails

Innoscience

Plain and Ordinary Meaning of "electrode stack" Prevails Because:

1A
The claims do not limit the term "electrode stack" beyond its plain and ordinary meaning.

1B
The specification does not define the term "electrode stack" or disavow its full scope.

1C
The extrinsic record does not support Patent Owner's narrow interpretation of "electrode stack".

Reply, 3-7; Ex-1047, ¶¶22-35.

The ’562 patent does not provide a special definition of “electrode stack” that differs from its ordinary meaning

Innoscience

More generally, electrode stack **220** corresponds to an electrode stack including a plurality metal layers, e.g., first Ti layer **222**, Al layer **224**, and second Ti layer **226**, and a

’562 Pat., 3:46-48 (annotated).

for example. Although the present inventive concepts are described with respect to specific embodiments, the principles of the invention, as defined by the claims appended herein, can obviously be applied beyond the specifically described embodiments of the invention described herein.

’562 Pat., 2:24-28 (annotated).

Moreover, the number and character of the plurality of metal layers **222**, **224**, and **226** of electrode stack **220** are merely exemplary. As a result, in other embodiments, elec-

’562 Pat., 3:60-62 (annotated).

FIG. **1** is a block diagram showing an example group III-V semiconductor device including a plurality of refractory metal nitride capped electrical contacts, according to one embodiment of the present invention. Structure **100**, in FIG. **1**, shows a specific implementation of the present inventive concepts. It should be understood that particular details such as the materials used to form structure **100** and the semiconductor device represented by structure **100**, for example, are provided for conceptual clarity, and should not be interpreted as limitations.

’562 Pat., 2:43-52 (annotated).

The ’562 patent never offers a precise definition of “electrode stack” that limits the scope of the term or disavows its full scope.

1B
The specification does not define the term “electrode stack” or disavow its full scope.

Reply, 3-7; Ex-1047, ¶¶22-35.

Patent Owner’s construction of “electrode stack”: stack of conductive layers that forms an electrical contact that is part of a semiconductor device and used to (1) establish contact with a nonmetallic part of the semiconductor device (like the source, drain and Schottky gate electrodes in the ’562 Patent Specification) or (2) controls the operation of the semiconductor device (like the insulated or Schottky gate electrodes in the ’562 Patent Specification)

POR, 8-9 (annotated).

Patent Owner inappropriately adds examples of electrodes from the specification to limit "electrode stack" in the claims

Innoscience

Patent Owner incorrectly limits the "electrode stack" to power electrodes, Schottky contacts, and insulated gate electrodes

Thus, the '562 Patent specification uses "electrode stack" to refer to a stack of layers forming an electrode and describes three electrode types: (1) a "power electrode[]" touching ("***ohmically coupled*** to") the nonmetallic semiconductor[3] (EX-1001, 3:19-28, 1:33-43); (2) a transistor gate electrode that controls the flow of electrons or holes through the transistor and touches (makes "Schottky contact" with) the nonmetallic semiconductor (*id.*, 3:31-35); and (3) a transistor gate electrode that controls the flow of electrons or holes through the transistor but is "an insulated gate electrode" separated from the semiconductor by an insulating layer 134 (*id.*, 3:21-33).

POR, 8 (annotated).

1B
The specification does not define the term "electrode stack" or disavow its full scope.

Reply, 3-7; Ex-1047, ¶¶22-35.

The '562 patent says the described contacts are examples

For example, III-nitride power semiconductor device fabrication typically includes forming electrical contacts, such as ohmic source/drain contacts, having a low Specific Linear

'562 pat., 1:33-35 (annotated).

The intrinsic and extrinsic records show that the plain and ordinary meaning of "electrode stack" prevails

Innoscience

Plain and Ordinary Meaning of "electrode stack" Prevails Because:

1A
The claims do not limit the term "electrode stack" beyond its plain and ordinary meaning.

1B
The specification does not define the term "electrode stack" or disavow its full scope.

1C
The extrinsic record does not support Patent Owner's narrow interpretation of "electrode stack".

Reply, 2-7; Ex-1047, ¶¶16-35.

The intrinsic and extrinsic records show that the plain and ordinary meaning of "electrode stack" prevails

Innoscience

Plain and Ordinary Meaning of "electrode stack" Prevails Because:

1A
The claims do not limit the term "electrode stack" beyond its plain and ordinary meaning.

1B
The specification does not define the term "electrode stack" or disavow its full scope.

1C
The extrinsic record does not support Patent Owner's narrow interpretation of "electrode stack".

Reply, 7-8; Ex-1046, 237; Ex-1047, ¶¶36-39.

Patent Owner's curated definition of "electrode" does not limit "electrode stack"

Patent Owner's incomplete definition of "electrode" (lay dictionary):

Merriam-Webster's Collegiate Dictionary defines "electrode" as "1: a conductor used to establish electrical contact with a ***nonmetallic*** part of a circuit" and "2: an element in a semiconductor device (as a transistor) that emits or collects electrons or holes or controls their movements." EX-2001, 371. The '562 Patent's electrodes meet these definitions.

POR, 9.

Technical Dictionary definition of "electrode" is broader:

A conductor which serves to **deliver, receive, collect, emit, deflect or control electric charge carriers**. An electrode **provides the path for current entering or leaving a medium** such as a dielectric, electrolytic solution, semiconductor, gas, or vacuum. … It is often a metal, and may consist for instance, of a wire, grid, plate or region.

Reply, 8; Ex-1046, 237 (emphasis added).

Technical Dictionary never mentions a source contact, a drain contact, Schottky gate, or insulated gate.
It never mentions contact with non-metallic part of a circuit.

1C
The extrinsic record does not support Patent Owner's narrow interpretation of "electrode stack."

Reply, 7-8; Ex-1047, ¶¶36-39.

The intrinsic and extrinsic records show that the plain and ordinary meaning of "electrode stack" prevails

Innoscience

Plain and Ordinary Meaning of "electrode stack" Prevails Because:

1A
The claims do not limit the term "electrode stack" beyond its plain and ordinary meaning.

1B
The specification does not define the term "electrode stack" or disavow its full scope.

1C
The extrinsic record does not support Patent Owner's narrow interpretation of "electrode stack".

Reply, 2-8; Ex-1047, ¶¶16-39; Ex-1046, 237.

Invalidity Grounds

Invalidity Grounds

Innoscience

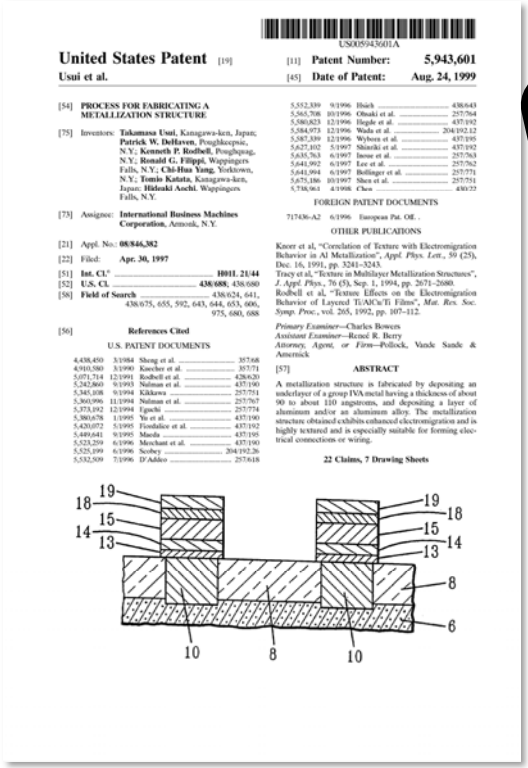
Usui Grounds

Yu Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	**Usui**
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu
3	9, 11, 14, and 16	§ 103	**Usui**, Yu, and Adesida
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	**Yu** and Usui
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida
7	10 and 15	§ 103	**Yu**, Usui, and Sugimoto

Pet., 3.

Usui Discloses or Renders the Claims Obvious: Grounds 1-4



US005943601A

United States Patent [19]
Usui et al.

[11] **Patent Number: 5,943,601**
[45] **Date of Patent: Aug. 24, 1999**

[54] **PROCESS FOR FABRICATING A METALLIZATION STRUCTURE**

[75] Inventors: **Takamasa Usui**, Kanagawa-ken, Japan; **Patrick W. DeHaven**, Poughkeepsie, N.Y.; **Kenneth P. Rodbell**, Poughquag, N.Y.; **Ronald G. Filippi**, Wappingers Falls, N.Y.; **Chi-Hua Yang**, Yorktown, N.Y.; **Tomio Katata**, Kanagawa-ken, Japan; **Hideaki Aochi**, Wappingers Falls, N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **08/846,382**

[22] Filed: **Apr. 30, 1997**

[51] **Int. Cl.**[6] **H01L 21/44**

[52] **U.S. Cl.** **438/688**; 438/680

[58] **Field of Search** 438/624, 641, 438/675, 655, 592, 643, 644, 653, 606, 975, 680, 688

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,438,450	3/1984	Sheng et al.	357/68
4,910,580	3/1990	Koscher et al.	357/71
5,071,714	12/1991	Rodbell et al.	428/620
5,242,860	9/1993	Nulman et al.	437/190
5,345,108	9/1994	Kikkawa	257/751
5,360,996	11/1994	Nulman et al.	257/767
5,373,192	12/1994	Eguchi	257/774
5,380,678	1/1995	Yu et al.	437/190
5,420,072	5/1995	Fiordalice et al.	437/192
5,449,641	9/1995	Maeda	437/195
5,523,259	6/1996	Merchant et al.	437/190
5,525,199	6/1996	Seeley	204/192.26
5,532,509	7/1996	D'Addeo	257/618
5,552,339	9/1996	Hsieh	438/643
5,565,708	10/1996	Ohsaki et al.	257/764
5,580,823	12/1996	Hegde et al.	437/192
5,584,973	12/1996	Wada et al.	204/192.12
5,587,339	12/1996	Wyborn et al.	437/195
5,627,102	5/1997	Shinohi et al.	437/192
5,635,763	6/1997	Inoue et al.	257/763
5,641,992	6/1997	Lee et al.	257/762
5,641,994	6/1997	Bollinger et al.	257/771
5,675,186	10/1997	Shen et al.	257/751
5,738,961	4/1998	Chen	430/22

FOREIGN PATENT DOCUMENTS

717436-A2 6/1996 European Pat. Off. .

OTHER PUBLICATIONS

Knorr et al, "Correlation of Texture with Electromigration Behavior in Al Metallization", *Appl. Phys. Lett.*, 59 (25), Dec. 16, 1991, pp. 3241–3243.
Tracy et al, "Texture in Multilayer Metallization Structures", *J. Appl. Phys.*, 76 (5), Sep. 1, 1994, pp. 2671–2680.
Rodbell et al, "Texture Effects on the Electromigration Behavior of Layered Ti/AlCu/Ti Films", *Mat. Res. Soc. Symp. Proc.*, vol. 265, 1992, pp. 107–112.

Primary Examiner—Charles Bowers
Assistant Examiner—Reneé R. Berry
Attorney, Agent, or Firm—Pollock, Vande Sande & Amernick

[57] **ABSTRACT**

A metallization structure is fabricated by depositing an underlayer of a group IVA metal having a thickness of about 90 to about 110 angstroms, and depositing a layer of aluminum and/or an aluminum alloy. The metallization structure obtained exhibits enhanced electromigration and is highly textured and is especially suitable for forming electrical connections or wiring.

22 Claims, 7 Drawing Sheets

Ex. 1004, Cover.

35 U.S.C. §102(b) Prior Art (published August 24, 1999).

At Institution, the Board found Petitioner established Usui discloses all limitations of claims 1, 2, and 4-7, including "electrode stack." ID, 11-14.

Usui discloses an electrode stack with metal layers and a capping layer, as claimed

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

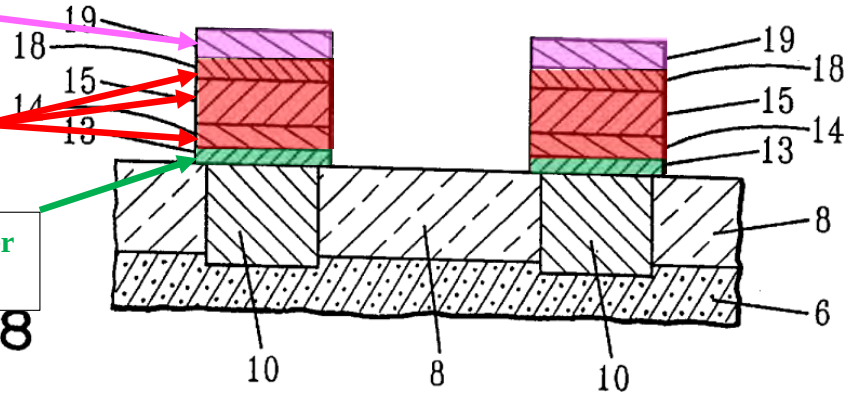


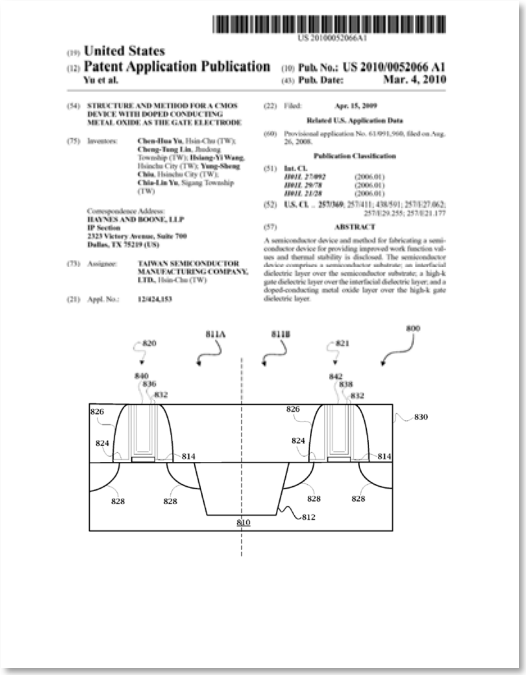
FIG. 8

Usui, Fig. 8 (annotated).

If the Board agrees on claim construction, claims 1, 2, and 4-7 are anticipated by Usui (Ground 1) because the only dispute is the construction of "electrode stack."

Pet., 1-33.

Yu Discloses or Renders the Claims Obvious: Grounds 5-7



(19) United States
(12) Patent Application Publication
Yu et al.
(10) Pub. No.: US 2010/0052066 A1
(43) Pub. Date: Mar. 4, 2010

(54) STRUCTURE AND METHOD FOR A CMOS DEVICE WITH DOPED CONDUCTING METAL OXIDE AS THE GATE ELECTRODE

(75) Inventors: Chen-Hua Yu, Hsin-Chu (TW); Cheng-Tung Lin, Jhudong Township (TW); Hsiang-Yi Wang, Hsinchu City (TW); Yung-Sheng Chin, Hsinchu City (TW); Chia-Lin Yu, Sigang Township (TW)

Correspondence Address: HAYNES AND BOONE, LLP IP Section 2323 Victory Avenue, Suite 700 Dallas, TX 75219 (US)

(73) Assignee: TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD., Hsin-Chu (TW)

(21) Appl. No.: 12/424,153

(22) Filed: Apr. 15, 2009

Related U.S. Application Data

(60) Provisional application No. 61/091,960, filed on Aug. 26, 2008.

Publication Classification

(51) Int. Cl.
H01L 27/092 (2006.01)
H01L 29/78 (2006.01)
H01L 21/28 (2006.01)

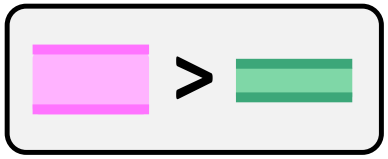
(52) U.S. Cl. 257/369; 257/411; 438/591; 257/E27.062; 257/E29.255; 257/E21.177

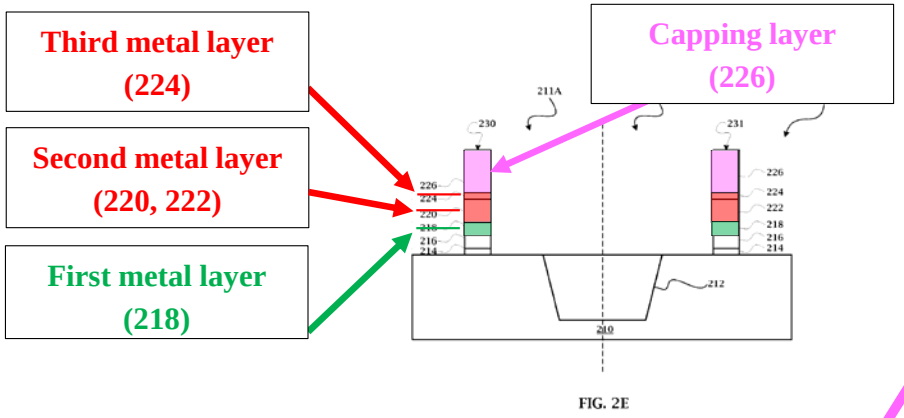
(57) ABSTRACT

A semiconductor device and method for fabricating a semiconductor device for providing improved work function values and thermal stability is disclosed. The semiconductor device comprises a semiconductor substrate; an interfacial dielectric layer over the semiconductor substrate; a high-k gate dielectric layer over the interfacial dielectric layer; and a doped-conducting metal oxide layer over the high-k gate dielectric layer.

Ex. 1005, Cover.
35 U.S.C. §102(e) Prior Art (filed April 15, 2009).

Yu discloses an electrode stack with a TiN or TaN capping layer that is thicker than the bottommost metal layer





Yu, Fig. 2E (annotated).

[0036] At step **110**, referring to FIGS. **1** and **2**D, a capping layer **226** is formed over the metal layers **220**, **222**, and in the present embodiment, over the diffusion barrier layer **224**. The capping layer **226** may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer **226** comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer **226** may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer **226** may

Yu, ¶[0036] (annotated).

If the Board agrees Yu at paragraph 36 discloses a TiN or TaN capping layer thicker than its bottommost layer, claims 1-8, 12, 13, and 17 invalid over Yu and Usui (Ground 5)

Pet., 1-8, 33-64.

Just Two Claim Features Disputed: Grounds 1-7

Innoscience

Patent Owner only disputes the prior art shows *two* features for claims 1 and 13 for grounds 1-7 and the motivations to combine the references for grounds 2-7

- ✓ [1a], [13a] an **electrode stack** (Usui grounds)
- ✓ [1c], [13c] said **refractory metal nitride / metal … having a thickness greater than that of a bottommost layer of said plurality of metal layers** (Yu grounds)
- ✓ Motivations to combine (grounds 2-7)

Ground 1:
At Institution, the Board agreed Usui discloses all limitations of claims 1, 2, and 4-7, including "electrode stack." ID, 11-14.

Ground 5:
At Institution, the Board did not reach a decision. ID, 18-19.

Grounds 2-4:
At Institution, the Board agreed the combinations of Usui, Yu, Adesida, and Sugimoto had a reasonable likelihood of showing that the claims would have been obvious. ID, 14.

Reply, 2-16, 27-28.

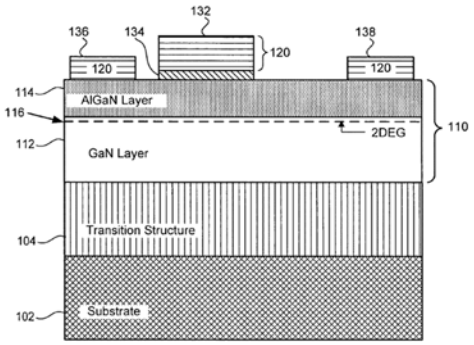
Just Two Claim Features Disputed: Grounds 1-7

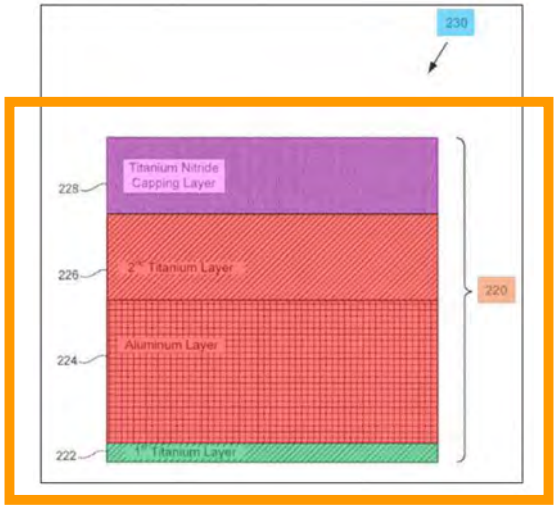
Innoscience

Patent Owner only disputes the prior art shows *two* features for claims 1 and 13

Disputed limitations claims 1 and 13:

- ✓ [1a/13a] an **electrode stack** (Usui grounds)
- ✓ [1c/13c] said **refractory metal nitride [metal] … having a thickness greater than that of a bottommost layer of said plurality of metal layers** (Yu grounds)





[1p] An **electrical contact** for use on a semiconductor device, said electrical contact comprising:

[1a] an **electrode stack** including a plurality of metal layers and a **capping layer** formed over said plurality of metal layers;

[1b] said **capping layer** consisting only of a refractory metal nitride,

[1c] said **refractory metal nitride** forming a top of said **electrical contact** and **having a thickness greater than that of** a **bottommost layer** of said plurality of metal layers.

Disputed

Disputed

'562 pat., Fig. 1, Fig. 2 (annotated), claim 1 (annotated).

Reply, 2-16, 27-28; Pet., 6; '562 pat., Fig. 1, claims 1, 13, Fig. 2 (annotated).

Motivations to Combine Disputed: Grounds 2-7

Innoscience

Patent Owner disputes the motivations to combine for grounds 2-7

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	**Usui**
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu
3	9, 11, 14, and 16	§ 103	**Usui**, Yu, and Adesida
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	**Yu** and Usui
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida
7	10 and 15	§ 103	**Yu**, Usui, and Sugimoto

Reply, 17-29; Pet., 3.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Usui Grounds

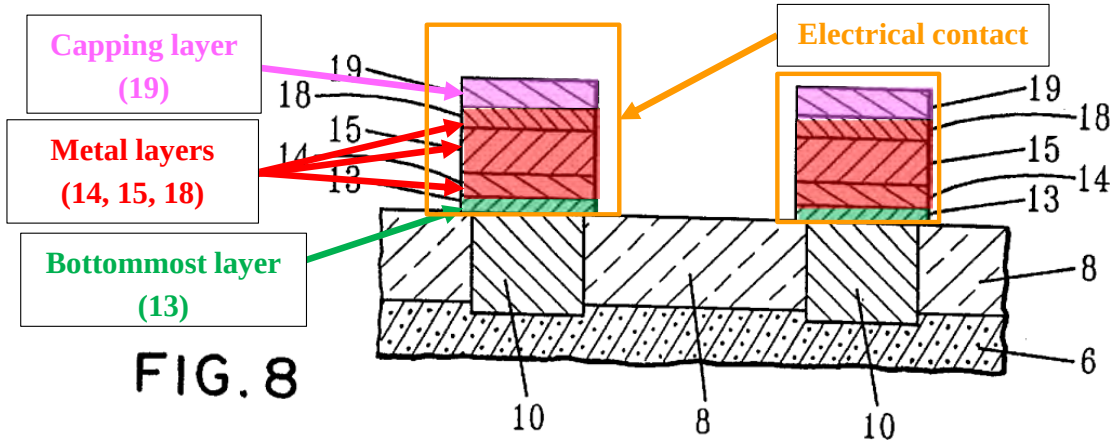
Yu Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	**Usui**
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu
3	9, 11, 14, and 16	§ 103	**Usui**, Yu, and Adesida
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	**Yu** and Usui
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida
7	10 and 15	§ 103	**Yu**, Usui, and Sugimoto

If the Board agrees on claim construction, claims 1, 2, and 4-7 are anticipated by Usui (Ground 1) because the only dispute is the construction of "electrode stack."

Pet., 3.

Ground 1: Usui anticipates claims 1, 2, and 4-7



Usui, Fig. 8 (annotated).

Usui	Limitation	
✓	**[1p]** An **electrical contact** for use on a semiconductor device, said electrical contact comprising:	Undisputed
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;	
✓	**[1b]** said **capping layer** consisting only of a refractory metal nitride,	Undisputed
✓	**[1c]** said **refractory metal nitride** forming a top of said **electrical contact** and having a thickness greater than that of a **bottommost layer** of said plurality of metal layers.	Undisputed

Claim construction dispute

'562 pat., Claim 1;

Pet., 8-13; Reply, 2-16.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Patent Owner relies on its construction to argue Usui's interconnect is not the claimed "electrode stack"

✓ [1a] an **electrode stack** (Usui grounds)

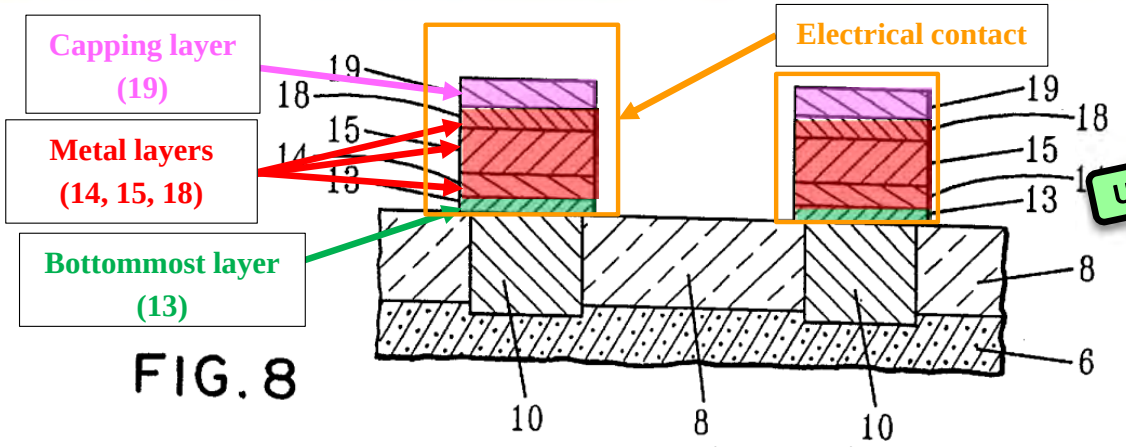
Usui discloses "electrode stack":

i. **under the plain and ordinary meaning; and**

ii. **under Patent Owner's construction.**

Pet., 8-13; Reply, 2-16; '562 pat., Claim 1.

Ground 1: Usui anticipates claims 1, 2, and 4-7



Usui, Fig. 8 (annotated).

Usui	Limitation
✓ Undisputed	**[1p]** An **electrical contact** for use on a semiconductor device, said electrical contact comprising:

'562 pat., Claim 1.

[57] **ABSTRACT**

A metallization structure is fabricated by depositing an underlayer of a group IVA metal having a thickness of about 90 to about 110 angstroms, and depositing a layer of aluminum and/or an aluminum alloy. The metallization structure obtained exhibits enhanced electromigration and is highly textured and is especially suitable for forming electrical connections or wiring.

Usui, Abstract (annotated).

Pet., 8-13; Reply, 8-16.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

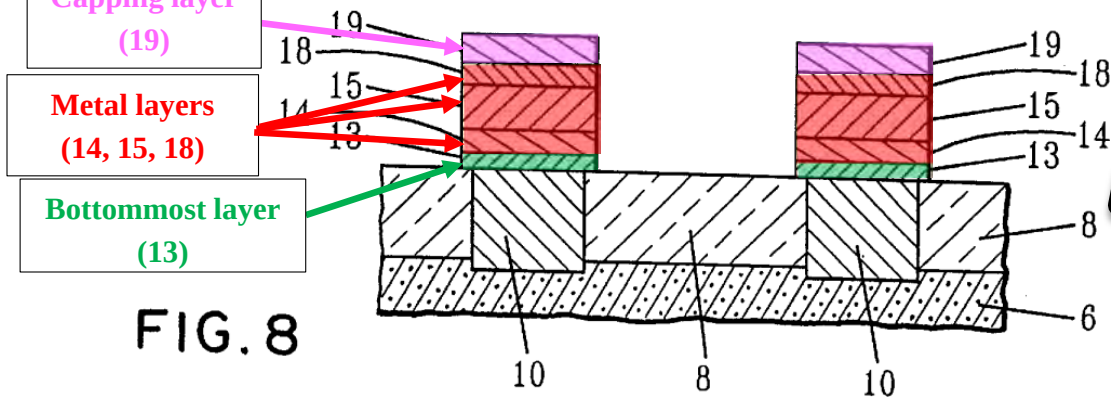


FIG. 8

Usui, Fig. 8 (annotated).

Usui discloses "electrode stack" under its plain meaning, including a plurality of metal layers and a capping layer formed over the plurality of metal layers

Pet., 8-13; Reply, 8-16.

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Capping layer (19)

18 is then blanket deposited the suitable capping layer **19** to complete the interconnect metallurgy at this level. The capping layer is preferably titanium nitride and can be

Usui, 5:55-57 (annotated).

Metal layer (18)

layers are titanium nitride and combinations of as layer **18** of a group IVA metal, preferably titanium with a titanium

Usui, 4:4-5 (annotated).

Metal layer (14, 15)

with underlayer **13**. Layer **15** is aluminum or an aluminum alloy. Typical aluminum alloys include alloying metal such as copper, magnesium, silicon, lanthanides such as vanadium and yttrium; and palladium. Preferably, the amount of

Usui, 3:38-41 (annotated).

Although not required, it is preferred that a titanium nitride layer **14** be located intermediate the group IVA layer

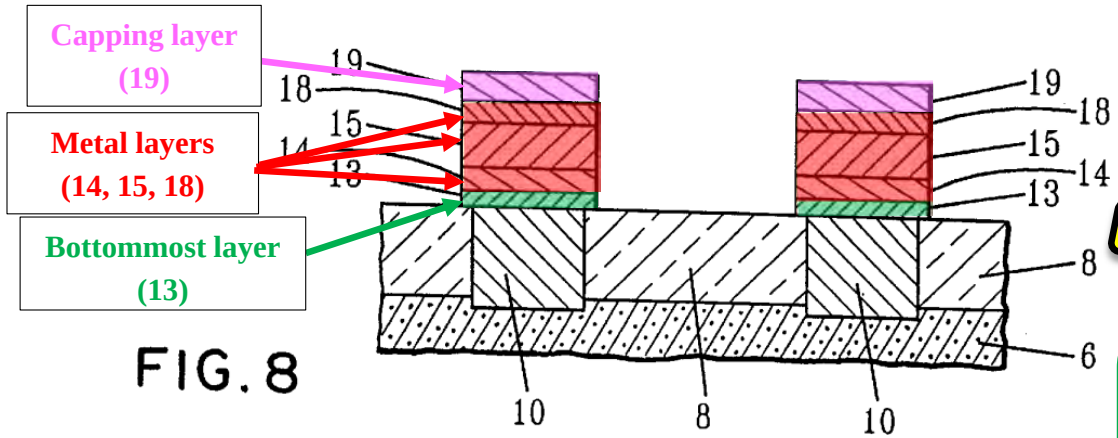
Usui, 3:58-59 (annotated).

Metal layer (13)

used for deposition of the titanium layer **13** or in a different

Usui, 5:38 (annotated).

Ground 1: Usui anticipates claims 1, 2, and 4-7



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Usui discloses an electrode stack under Patent Owner's construction.

1A
Usui discloses an "electrode stack" under Patent Owner's (incorrect) first construction: requiring contact with a nonmetallic part of the semiconductor device. Reply, 8-12; EX-1047, ¶¶40-48.

1B
Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device. Reply, 12-13; EX-1047, ¶¶49-51.

1C
A "semiconductor device" includes interconnect metallization structures. Reply, 13-16; EX-1047, ¶¶52-63.

Pet., 8-13; Reply, 8-16.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

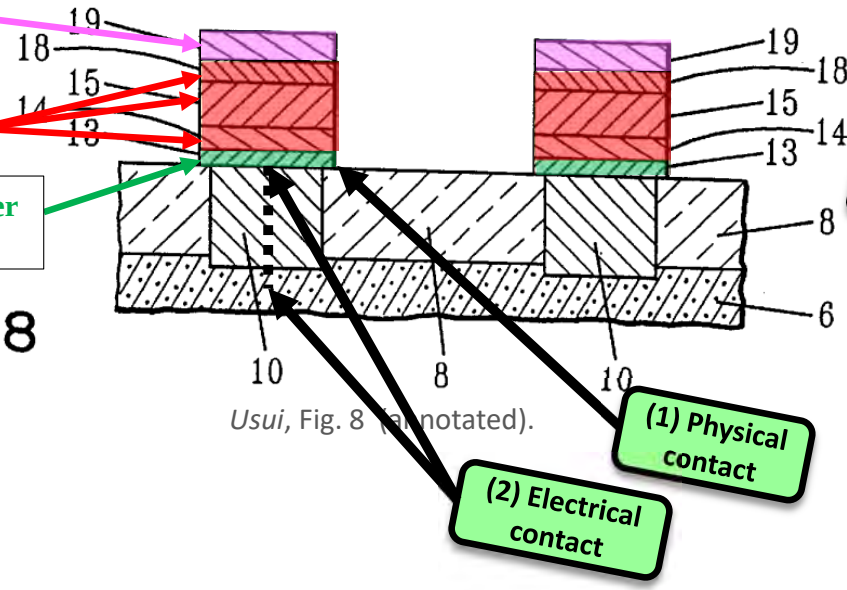


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Patent Owner's construction of "electrode stack": stack of conductive layers that forms an electrical contact that is part of a semiconductor device and used to (1) establish contact with a nonmetallic part of the semiconductor device (like the source, drain and Schottky gate electrodes in the '562 Patent Specification).

1A
Usui discloses an "electrode stack" under Patent Owner's (incorrect) first construction: requiring contact with a nonmetallic part of the semiconductor device.

Layers 14, 15, 18, 19, and underlayer 13 meet Patent Owner's Construction of "electrode stack" by contacting nonmetallic layers:
(1) physically contacts insulator 8
(2) electrically contacts semiconductor wafer 6

Pet., 8-13; Reply, 8-12; EX-1047, ¶¶40-48; POR, 8-9.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

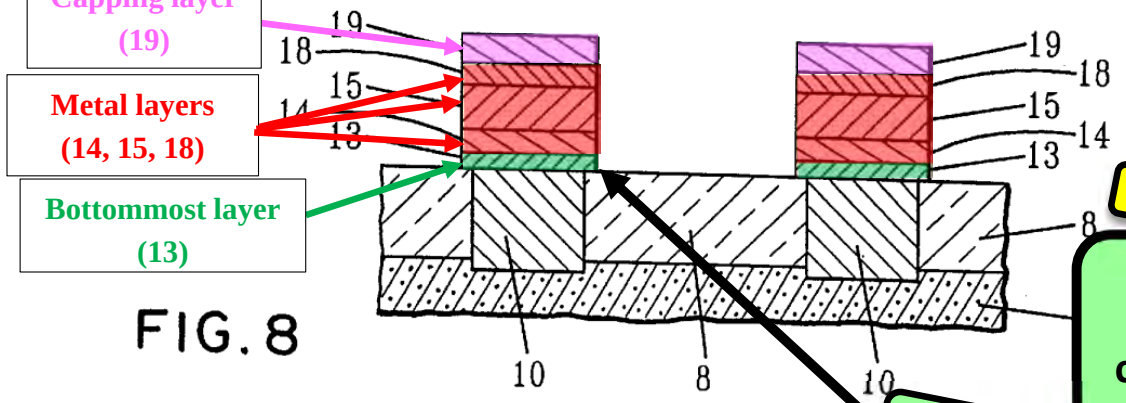


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

(1) Physical Contact:
Underlayer 13 and insulator 8 have a substantial contact area because contact stud 10 is not a layer, it is a conductive via that cuts across device layers

(1) Physical contact

43. Usui's structure has a substantial area of physical contact between underlayer 13 and insulator 8. This is because "contact stud 10" is not a layer, it is an interplanar conductive via that cuts across device layers, which I explained during my deposition. Usui at 3:24-27, 5:11-13, Figs. 1-8; Ex. 2026 at 10:6-8,12:2-7, 32:6-77:16-18, 79:15-17, 79:22-80:9. A conductive via is a filled hole, which is typically a much smaller structure than the surrounding layers and structures. Ex. 2026 at

Ex-1047, ¶43.

Ex-1047, ¶43.

As Dr. Zhao explained, contact stud is not a layer

1A
Usui discloses an "electrode stack" under Patent Owner's (incorrect) first construction: requiring contact with a nonmetallic part of the semiconductor device.

Pet., 8-13; Pet., 8-13; Reply, 8-12; EX-1047, ¶¶40-48.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

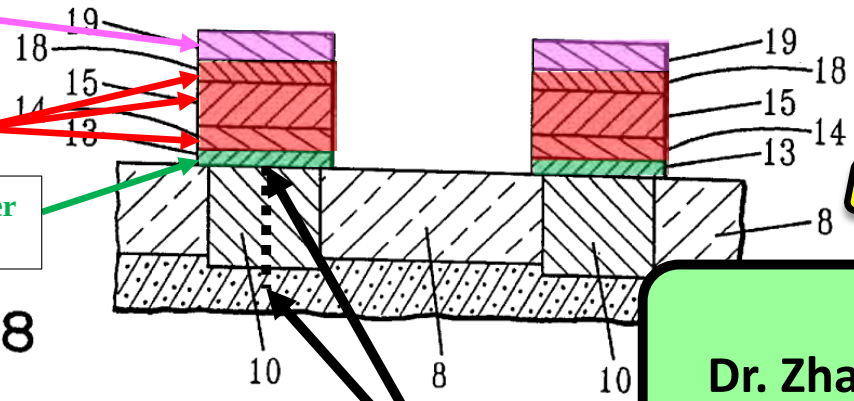


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

(2) Electrical Contact:
Dr. Zhao and Dr. Piner agree that interconnects electrically connect to semiconductor layers.

(2) Electrical contact

1A
Usui discloses an "electrode stack" under Patent Owner's (incorrect) first construction: requiring contact with a nonmetallic part of the semiconductor device.

Dr. Zhao's supplemental declaration

Ex. 2024 at ¶¶ 63, 147-148. Dr. Piner notes "[i]nterconnects are **deposited on insulators and touch the active devices**" and are made [of] multiple levels of metal lines and connecting vias "serve as the wiring between semiconductor devices, such as transistors." Ex. 2024 at ¶ 63 (quoting Ex. 1011 (emphasis original)). There, Dr. Piner shows he understands that interconnects electrically connect to semiconductor layers. Indeed, Usui explicitly makes this point, stating that its metallization

Ex-1047, ¶44 (emphasis added); Ex-2024, ¶63.

Pet., 8-13; Reply, 8-12; EX-1047, ¶¶40-48; POR, 8-9.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

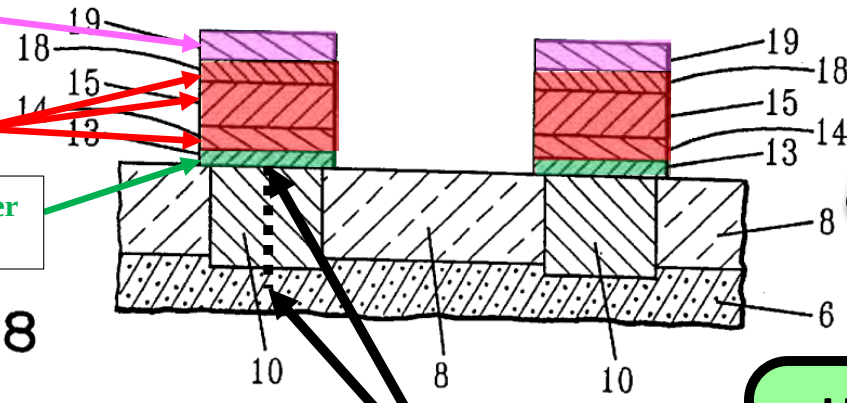


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

(2) Electrical contact

Usui's interconnect establishes *electrical contact* with nonmetallic semiconductor wafer 6

1A
Usui discloses an "electrode stack" under Patent Owner's (incorrect) first construction: requiring contact with a nonmetallic part of the semiconductor device.

the present invention. Referring to FIG. **1**, the interconnect metallurgy preferably comprises a **4** or **5** layer structure over an interplanar stud connection **10** surrounded by an insulator **8** to make connection to a device substrate **6**. The metallurgy

Usui, 3:24-27 (annotated); Figs. 1, 8.

Pet., 8-13; Reply, 8-12; EX-1047, ¶¶40-48.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

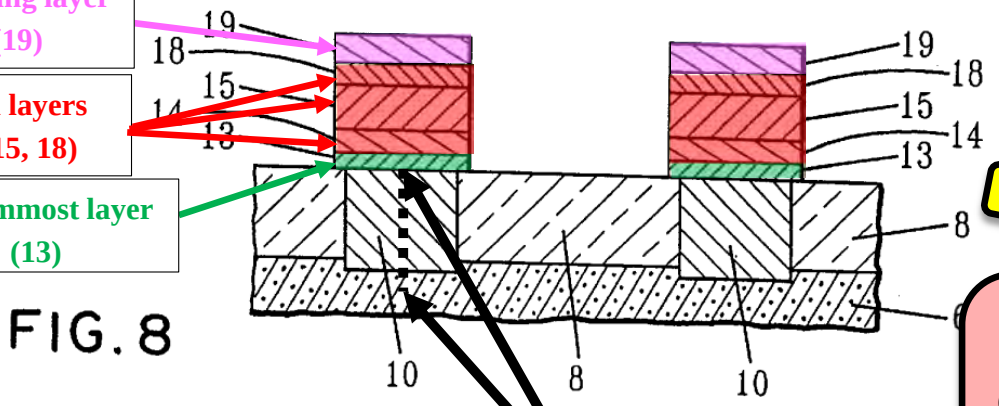


FIG. 8

Usui, Fig. 8 (annotated).

(2) Electrical contact

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Patent Owner inappropriately construes its construction to impose further requirements—an electrode stack needs *direct* electrical contact with a nonmetallic component

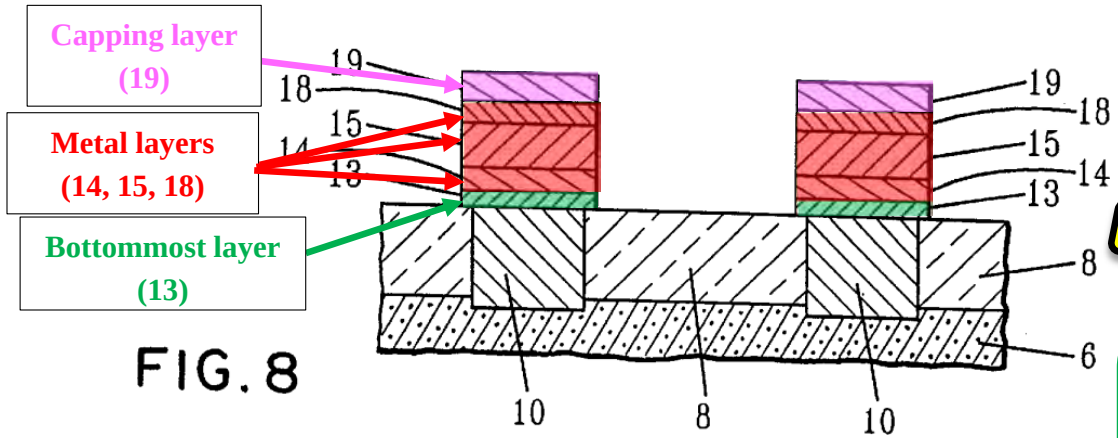
1A
Usui discloses an "electrode stack" under Patent Owner's (incorrect) first construction: requiring contact with a nonmetallic part of the semiconductor device.

Pet., 8-13; Reply, 8-12; EX-1047, ¶¶40-48.

~~Thus, Usui's interconnect metallization structure is connected to ***metal*** stud connection 10. Usui's interconnect metallization structure (layers 13-15 and 18-19) is not "a conductor used to establish electrical contact with a ***nonmetallic part of a circuit***" and is thus not an "electrode" under Merriam-Webster's definition 1.~~

POR, 18-19.

Ground 1: Usui anticipates claims 1, 2, and 4-7



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Usui discloses an electrode stack under Patent Owner's construction.

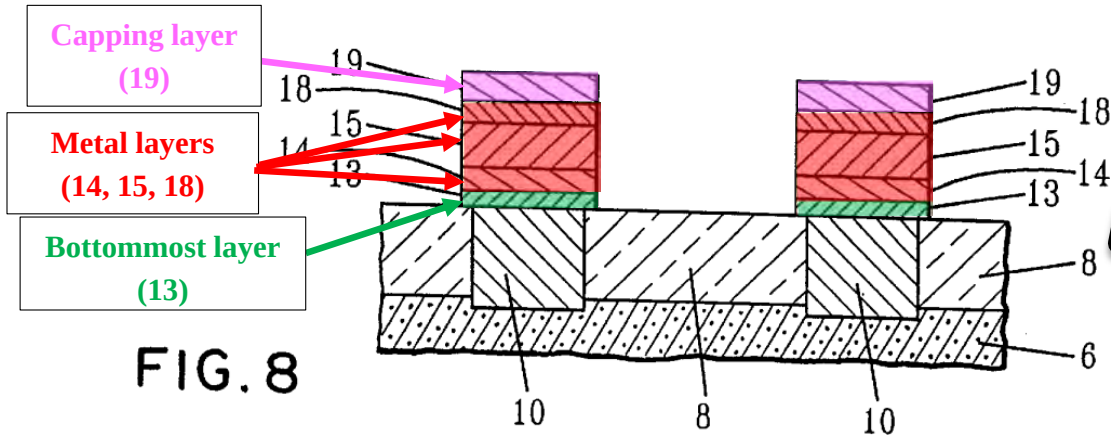
1A
Usui discloses an "electrode stack" under Patent Owner's (incorrect) first construction: requiring contact with a nonmetallic part of the semiconductor device. Reply, 8-12; EX-1047, ¶¶40-48.

1B
Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device. Reply, 12-13; EX-1047, ¶¶49-51.

1C
A "semiconductor device" includes interconnect metallization structures. Reply, 13-16; EX-1047, ¶¶52-63.

Pet. at 8-13; Reply, 8-16.

Ground 1: Usui anticipates claims 1, 2, and 4-7



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Usui discloses an electrode stack under Patent Owner's construction.

✓

1A
Usui discloses an "electrode stack" under Patent Owner's (incorrect) first construction: requiring contact with a nonmetallic part of the semiconductor device. Reply, 8-12; EX-1047, ¶¶40-48.

1B
Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device. Reply, 12-13; EX-1047, ¶¶49-51.

1C
A "semiconductor device" includes interconnect metallization structures. Reply, 13-16; EX-1047, ¶¶52-63.

Pet., 8-13; Reply, 8-16.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

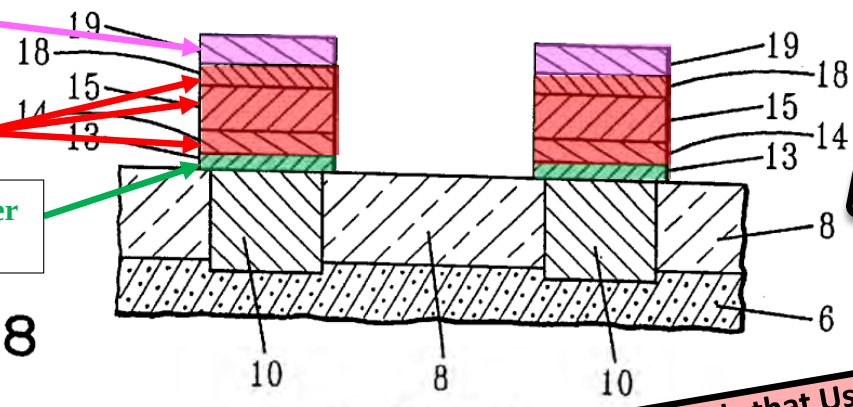


FIG. 8

Usui, Fig. 8 (annotated)

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Patent Owner's construction of "electrode stack": stack of conductive layers that forms an electrical contact that is part of a semiconductor device and used to (2) controls the operation of the semiconductor device (like the insulated or Schottky gate electrodes in the '562 Patent Specification)

Patent Owner incorrectly contends that Usui's interconnect:

(1) Is not an element in a semiconductor device

(2) Does not control operation of the semiconductor device

1B

Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device.

Usui's interconnect metallization structure also does not meet Merriam-Webster's definition 2. Piner, ¶151. Usui never teaches that its interconnect metallization structure (layers 13-15 and 18-19) is "an element ***in a semiconductor device*** that emits or collects electrons or holes or controls their movements." EX-

POR, 19 (annotated).

Pet., 8-13; Reply, 12-13; EX-1047, ¶¶49-51; POR, 8-9.

Ground 1: Usui anticipates claims 1, 2, and 4-7

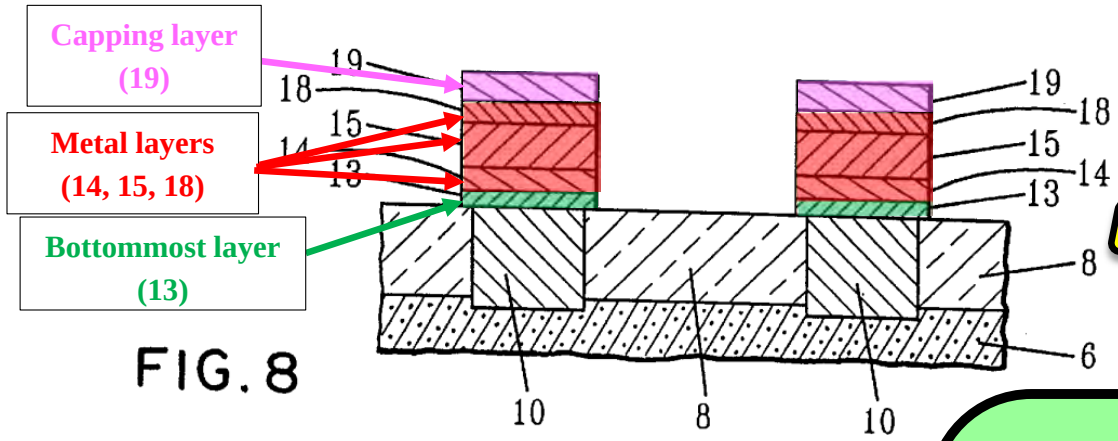


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

1B
Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device.

Usui's interconnect satisfies Patent Owner's construction because:

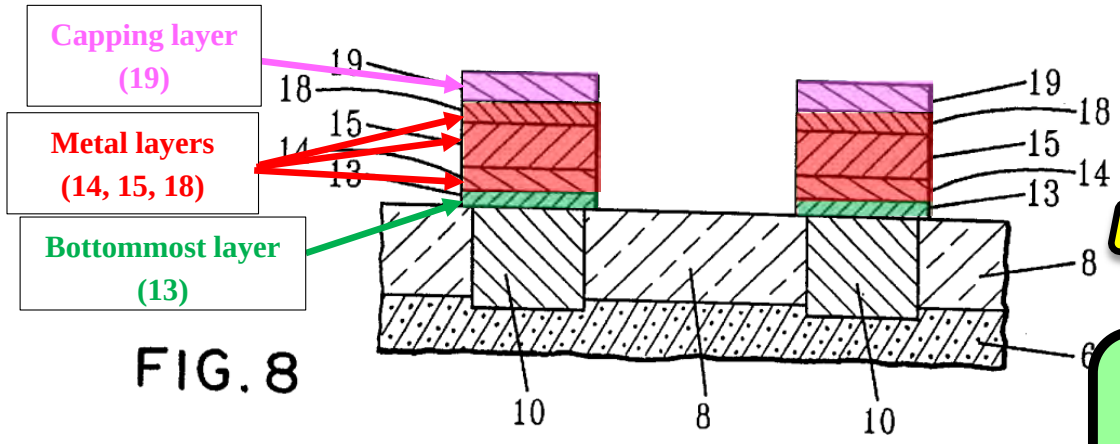
(1) It is part of the semiconductor device
- **Usui's interconnect is formed as one device with semiconductor wafer 6**

(2) It controls operation of the semiconductor device
- **Usui's interconnect enables or influences current flow**

Pet. at 8-13; Reply, 12-13; EX-1047, ¶¶49-51.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Usui's interconnect:
(1) It is part of the semiconductor device

Usui's metallurgy structure and semiconductor wafer 6 are formed as one device

FIG. **1** is a cross-sectional view of the preferred embodiment of an interconnect metallurgy structure according to the present invention. Referring to FIG. **1**, the interconnect metallurgy preferably comprises a **4** or **5** layer structure over an interplanar stud connection **10** surrounded by an insulator **8** to make connection to a device substrate **6**. The metallurgy

Usui, 3:23-28; *see also Usui*, 3:28-4:10.

1B
Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device.

Pet., 8-13; Reply, 12-13; EX-1047, ¶¶49-51.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

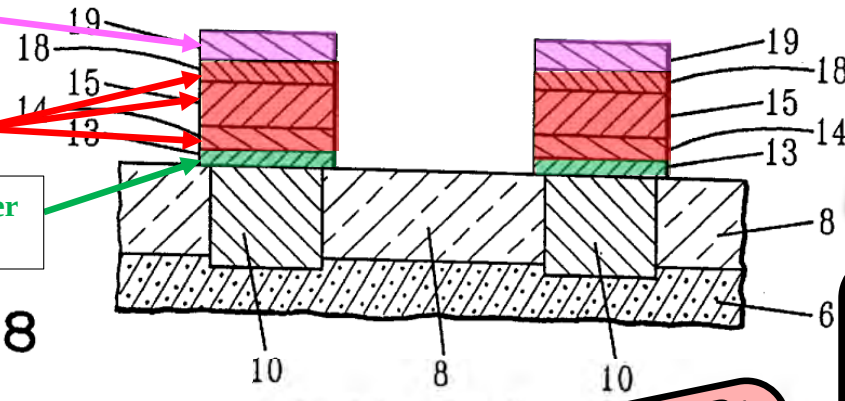


FIG. 8

Usui, Fig. 8 (annotated)

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Usui's electrode stack:
(2) Controls operation of the semiconductor device because it involves enabling or influencing current flow

As Patent Owner's expert Dr. Piner notes, interconnections provide electrical connections within and between devices

64. This has been the understanding of a POSA for several decades as the excerpt from U.S. Patent No. 6,249,056 (Kwon) illustrates:

The metallization process provides interconnections between contacts within semiconductor devices and between devices and conductive pads. To make electrical connections in smaller and more complex

Ex-2024, ¶64 (Dr. Piner) (annotated).

1B
Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device.

Pet., 8-13; Reply, 12-13; EX-1047, ¶¶49-51.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

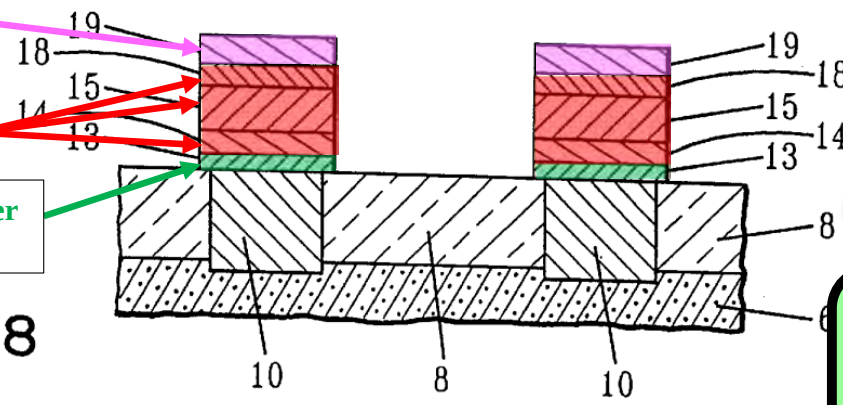


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Usui's electrode stack:
(2) Controls operation of the semiconductor device because it involves enabling or influencing current flow

Usui's interconnect metallization reduces electromigration, resulting in longer failure times

aluminum and/or an aluminum alloy. The metallization structure obtained exhibits enhanced electromigration and is highly textured and is especially suitable for forming electrical connections or wiring.

Usui, Abstract; *see also Usui*, 1:30-35, 3:54-57, 4:57-5:10; Ex-1047, ¶51.

1B
Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device.

Pet., 8-13; Reply, 12-13; EX-1047, ¶¶49-51.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

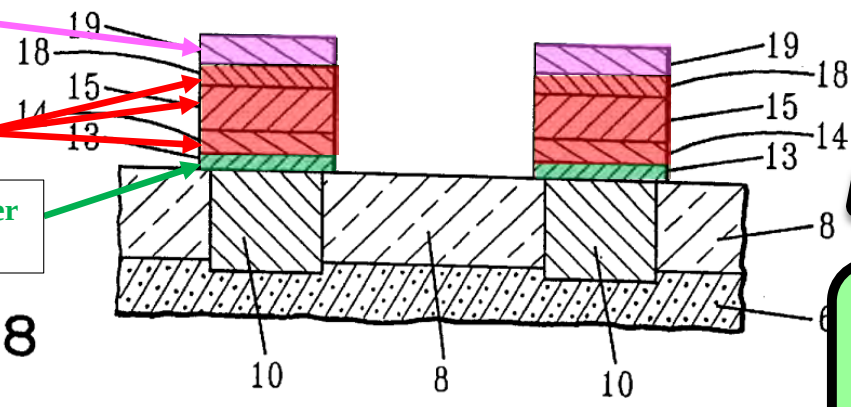


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Usui's electrode stack:
(2) Controls operation of the semiconductor device because it involves enabling or influencing current flow

Dr. Zhao notes an integrated circuit cannot function without an interconnect

semiconductor. Interconnects "provide low resistance paths for current." Ex-1011 at 218. It would not be possible for an integrated circuit to function without the use of interconnects.

Ex-1047, ¶50.

1B
Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device.

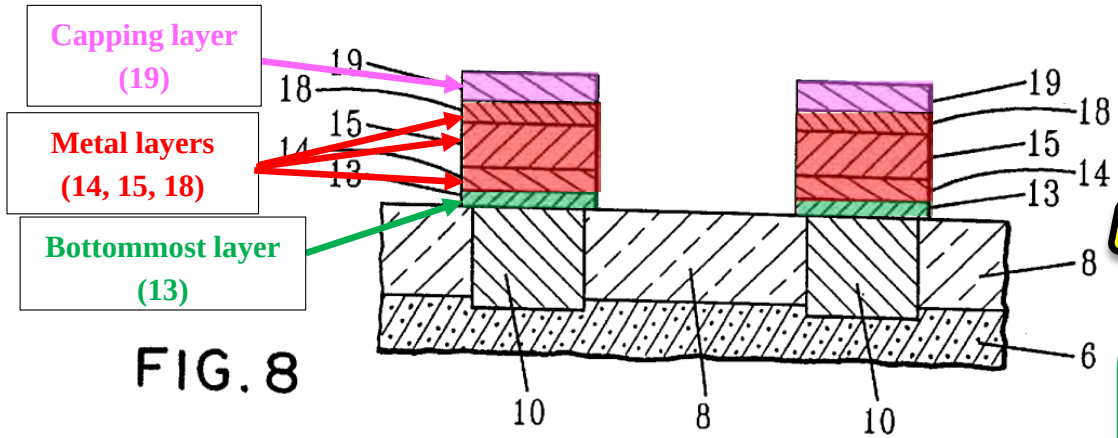
Dr. Zhao also notes that by improving electromigration, the metallization structure shapes current characteristics, thereby controlling operation

Because Usui's metallization structure improves electromigration, it shapes current characteristics, so it controls operation of the semiconductor device.

Ex-1047, ¶51.

Pet., 8-13; Reply, 12-13; EX-1047, ¶¶49-51.

Ground 1: Usui anticipates claims 1, 2, and 4-7



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Usui discloses an electrode stack under Patent Owner's construction.

1A
Usui discloses an "electrode stack" under Patent Owner's (incorrect) first construction: requiring contact with a nonmetallic part of the semiconductor device. Reply, 8-12; EX-1047, ¶¶40-48.

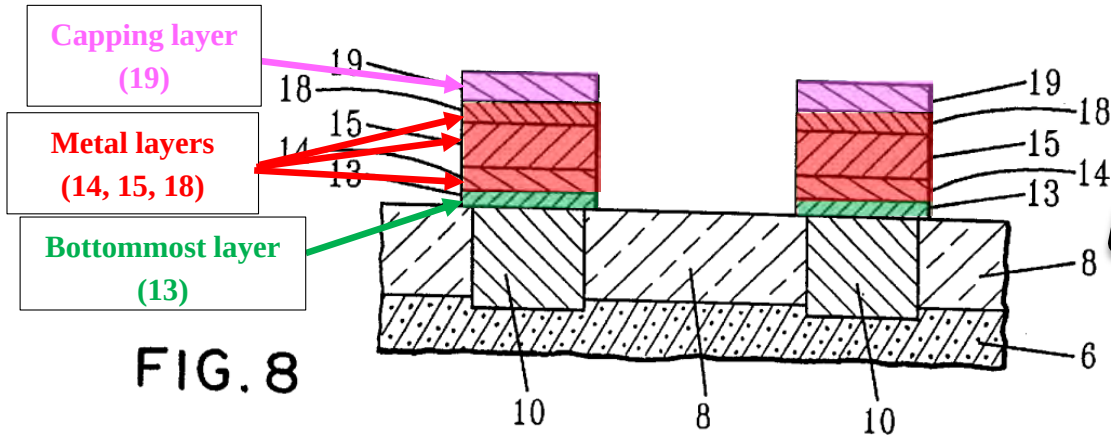
1B
Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device. Reply, 12-13; EX-1047, ¶¶49-51.

1C
A "semiconductor device" includes interconnect metallization structures. Reply, 13-16; EX-1047, ¶¶52-63.

Pet., 8-13; Reply, 8-16.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Usui discloses an electrode stack under Patent Owner's construction.

1A
Usui discloses an "electrode stack" under Patent Owner's (incorrect) first construction: requiring contact with a nonmetallic part of the semiconductor device. Reply, 8-12; EX-1047, ¶¶40-48.

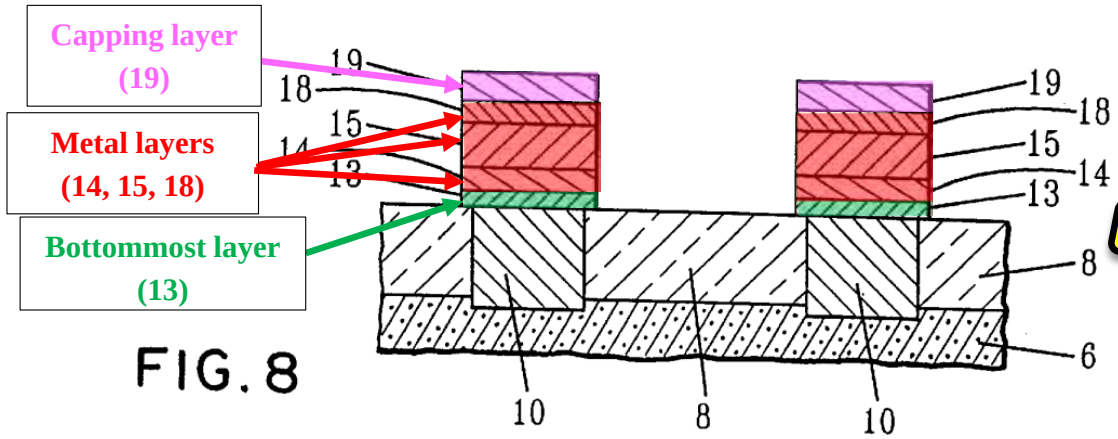
1B
Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device. Reply, 12-13; EX-1047, ¶¶49-51.

1C
A "semiconductor device" includes interconnect metallization structures. Reply, 13-16; EX-1047, ¶¶52-63.

Pet., 8-13; Reply, 8-16.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Patent Owner incorrectly construes "semiconductor device" to exclude interconnect metallization structures based on their function

1C
A "semiconductor device" includes interconnect metallization structures.

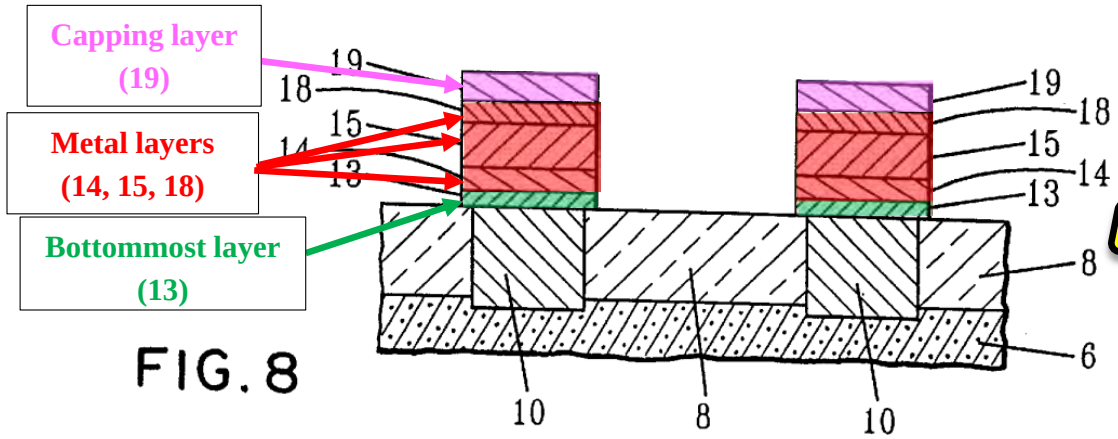
~~2001, 371. Usui's interconnect metallization structure is not an element of a semiconductor device at all – it is used to connect two devices. As its name~~

POR, 19.

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Semiconductors do not exclude interconnects: Usui's interconnect is formed as one device that includes the metallurgy and semiconductor wafer 6

1C
A "semiconductor device" includes interconnect metallization structures.

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

FIG. 1 is a cross-sectional view of the preferred embodiment of an interconnect metallurgy structure according to the present invention. Referring to FIG. 1, the interconnect metallurgy preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 to make connection to a device substrate 6. The metallurgy

Usui, 3:23-28 (annotated); *see also Usui*, 3:28-4:10.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

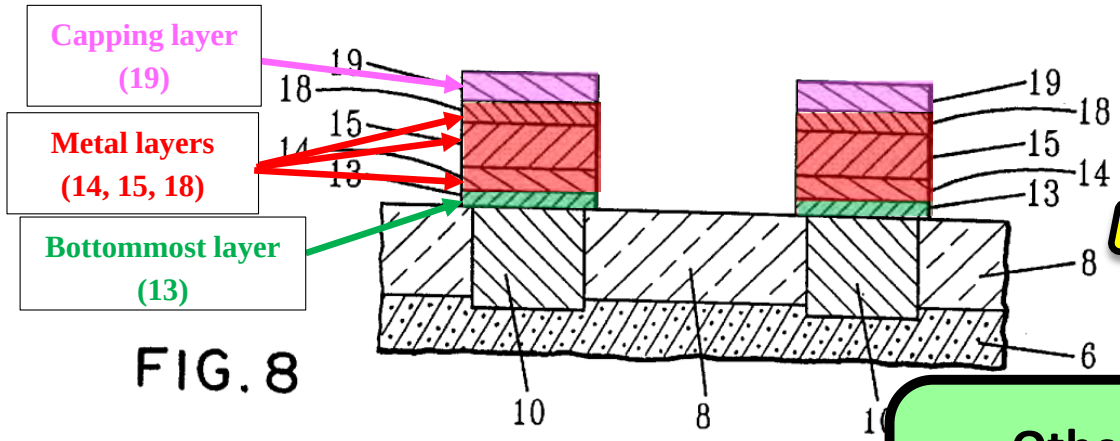


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Other prior art describes interconnect structures as a part of a semiconductor device

1C
A "semiconductor device" includes interconnect metallization structures.

electrode), respectively. In still another example, various contacts/vias and multilayer interconnect features (e.g., metal layers and interlayer dielectrics) may be formed on the substrate **210** and configured to connect the various features or structures of the semiconductor device **200**.

Yu, ¶[0040] (annotated).

[0009] Packaging follows in which an IC chip (not shown) of which the interconnect structure **10** is a part is assembled into a higher-order electronic structure. This involves the wire bonding of an internal lead (not shown) of a leadframe to the aluminum pad **26**. The leadframes are electrically attached to components in the electronic structure.

Ex-1044, ¶[0009] (annotated).

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

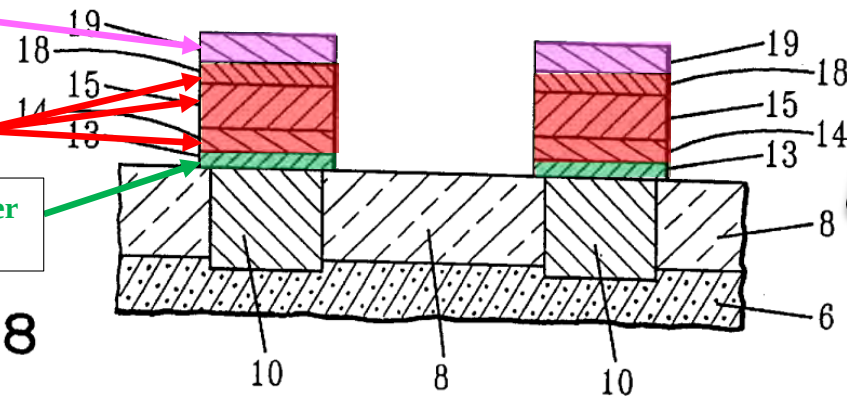


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Other prior art describes interconnect structures as a part of a semiconductor device

Prior art describes forming interconnects in a semiconductor device

[0007] Accordingly, what is needed in the art is a process for manufacturing interconnects in a semiconductor device that does not exhibit the limitations of the prior art.

Ex-1045, ¶[0007] (annotated).

Prior art describes a semiconductor device interconnect, which includes a semiconductor substrate layer

[0008] To address the above-discussed deficiencies of the prior art, the present invention provides, in one embodiment, a process for forming a semiconductor device interconnect. The process includes, forming a dielectric layer over a metal line located on a substrate, forming an opening in the

Ex-1045, ¶[0008] (annotated).

1C
A "semiconductor device" includes interconnect metallization structures.

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

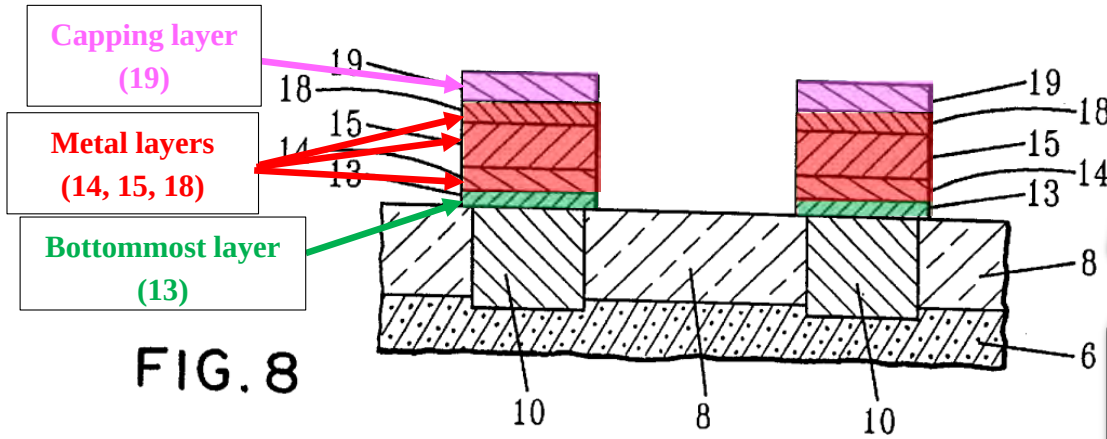


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

The '562 patent does not exclude interconnect metallization structures from "semiconductor device"

1C
A "semiconductor device" includes interconnect metallization structures.

The '562 patent does not alter limit the meaning of "semiconductor device," "electrical contact," or "electrode"

1. An electrical contact for use on a semiconductor device, said electrical contact comprising:
an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;
said capping layer consisting only of a refractory metal nitride, said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

See, e.g., '562 pat., Claim 1.

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

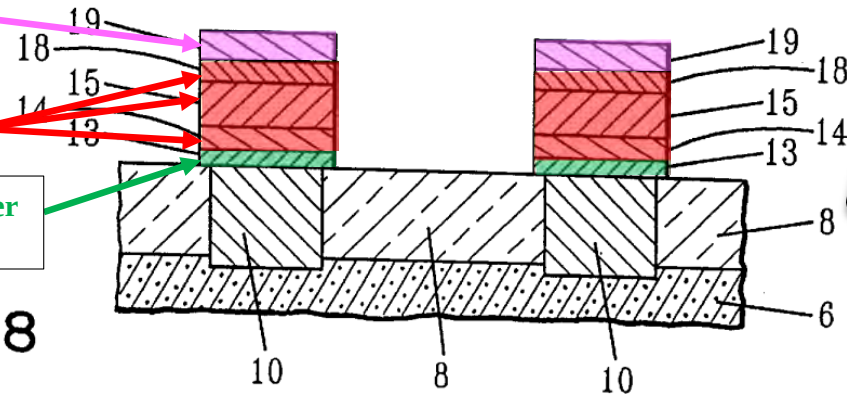


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Patent Owner implausibly construes "electrical contact" to require a metal-semiconductor junction

Ex-1047, ¶¶ 55-56.

1C
A "semiconductor device" includes interconnect metallization structures.

Patent Owner tries to use its distorted construction to exclude Usui's interconnect metallization structure (e.g., layers 13-15 and 18-19), which shows a metal-metal connection to stud connection 10

~~*circuit*." EX-2001, 371 (definition 1). As shown below, Usui's interconnect metallization layer is connected to "interplanar stud connection 10" – it is *stud connection 10* that "make[s] connection to a device substrate 6." Usui, 3:24-27.~~

POR, 18.

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

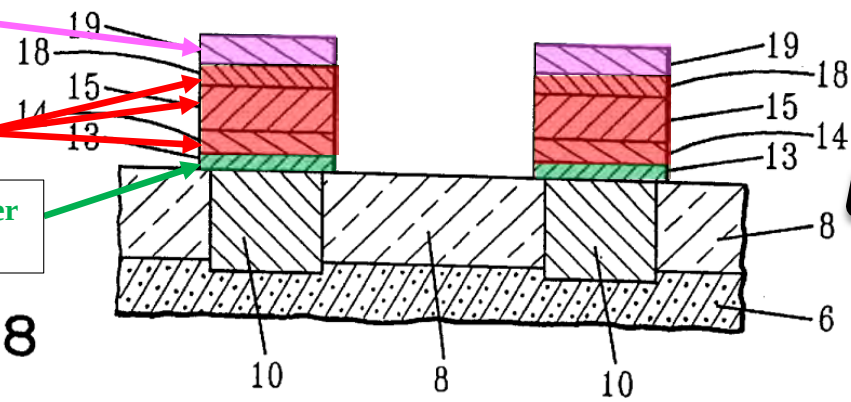


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Even Patent Owner's expert Dr. Piner admits that "metal-metal electrical connections" were "conventional" and "known"

Ex-1047, ¶55.

related to interconnections. Unlike electrical contacts of the '562 Patent which form a metal-semiconductor junction, interconnections function as metal-metal electrical connections much like conventional wires of a circuit. As Dr. Zhao

Ex-2024, ¶102 (Dr. Piner) (annotated).

EX-1004 (Usui), Figure 8 (annotated). By contrast, Usui's interconnect metallurgy structure (layers 13-15 and 18-19) forms nothing more than a known metal-metal junction with contact metal 10. Petitioner and Dr. Zhao only identified a stack of

Ex-2024, ¶136 (Dr. Piner) (annotated).

1C
A "semiconductor device" includes interconnect metallization structures.

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

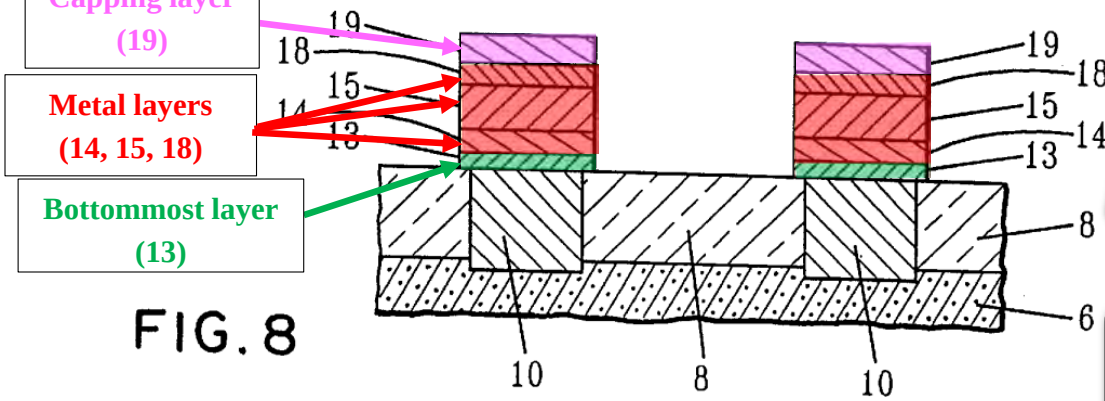


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

The claims do not require an "electrical contact" to be a metal-semiconductor junction

1. The "electrode stack" does not require metal-semiconductor junction, so broader "electrical contact comprising: an electrode stack" does not either

2. The '562 patent disclosure does not exclude metal-metal junctions from its electrical contact

1C
A "semiconductor device" includes interconnect metallization structures.

1. An electrical contact for use on a semiconductor device, said electrical contact comprising:
an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;
said capping layer consisting only of a refractory metal nitride, said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

See, e.g., 562 pat., Claim 1 (annotated).

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Capping layer (19)

Metal layers (14, 15, 18)

Bottommost layer (13)

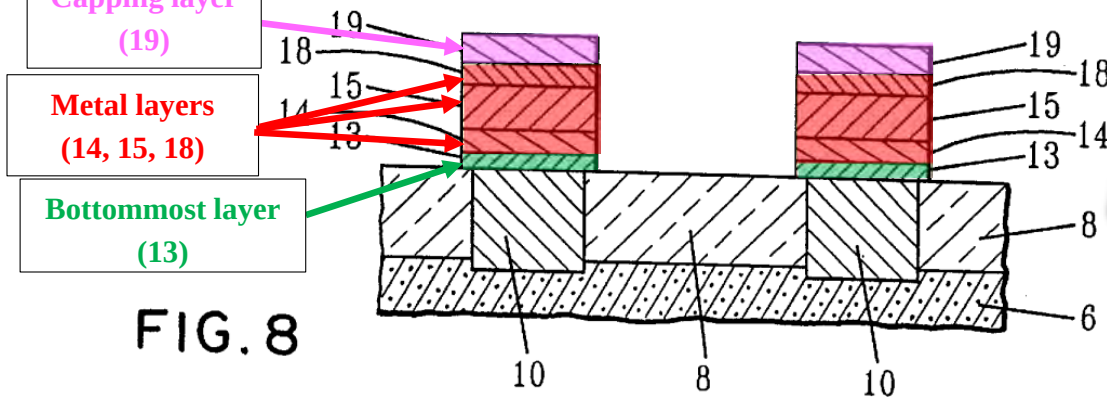


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

No electromigration?

Patent Owner inappropriately contends the claimed "electrical contact" comprising an "electrode stack" cannot be an interconnect because Dr. Piner incorrectly alleges the claims exclude components that experience electromigration.

1C
A "semiconductor device" includes interconnect metallization structures.

Patent Owner imposes even more limitations on the claims that are not there

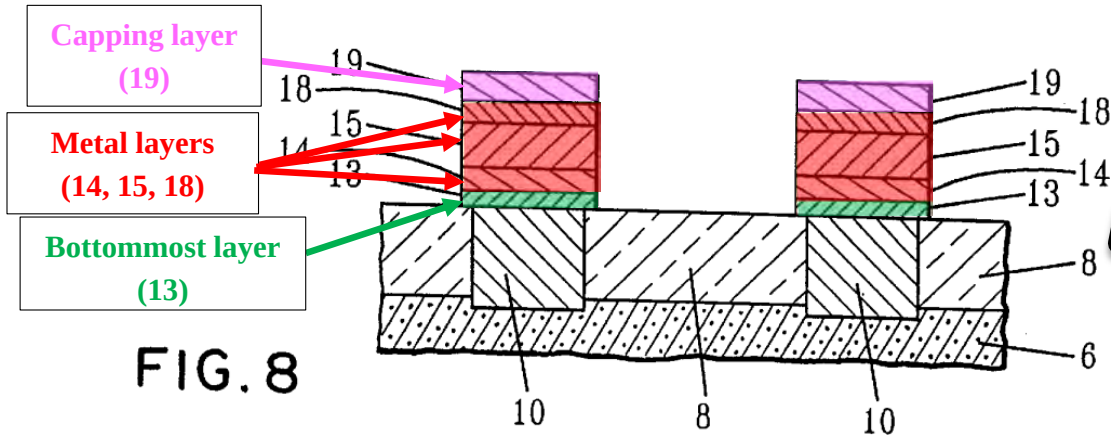
~~electrical contact comprising an electrode stack of the semiconductor device. Usui is directed to *interconnects* and addresses electromigration, a problem specifically associated with aluminum-based interconnects, and not associated with *electrical contacts having an electrode stack* as described and claimed by the '562 Patent.~~

Ex-2024, ¶134 (Dr. Piner) (annotated).

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

No electromigration?
Patent Owner contends the claimed "electrical contact" comprising an "electrode stack" cannot experience electromigration.

1C
A "semiconductor device" includes interconnect metallization structures.

Dr. Zhao explains that HEMT power transistors (disclosed in the '562 patent) often have high current flows and densities, including in ohmic contacts, which can cause electromigration

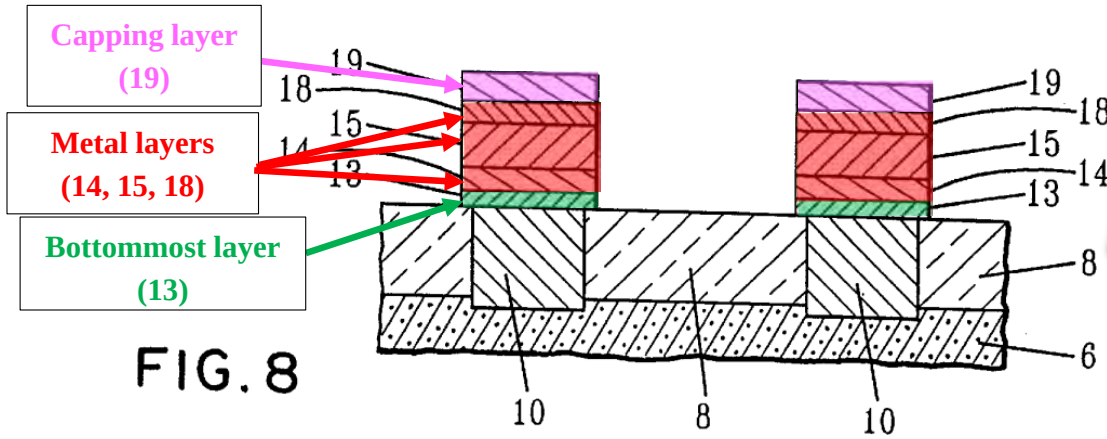
61. The '562 patent claims and describes a HEMT power transistor, which often has high current flows and current densities, including in their ohmic contacts. Ex. 1001 at 2:53-65, claims 9, 14. Dr. Piner fails to explain why the HEMT power devices of the '562 patent would not experience electromigration. As I explained above, a POSITA would have appreciated electromigration is indeed a concern for such devices, and the electrical contact of the '562 patent would have experienced electromigration.

Ex-1047, ¶61 (annotated).

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

No electromigration?
Patent Owner contends the claimed "electrical contact" comprising an "electrode stack" cannot experience electromigration.

1C
A "semiconductor device" includes interconnect metallization structures.

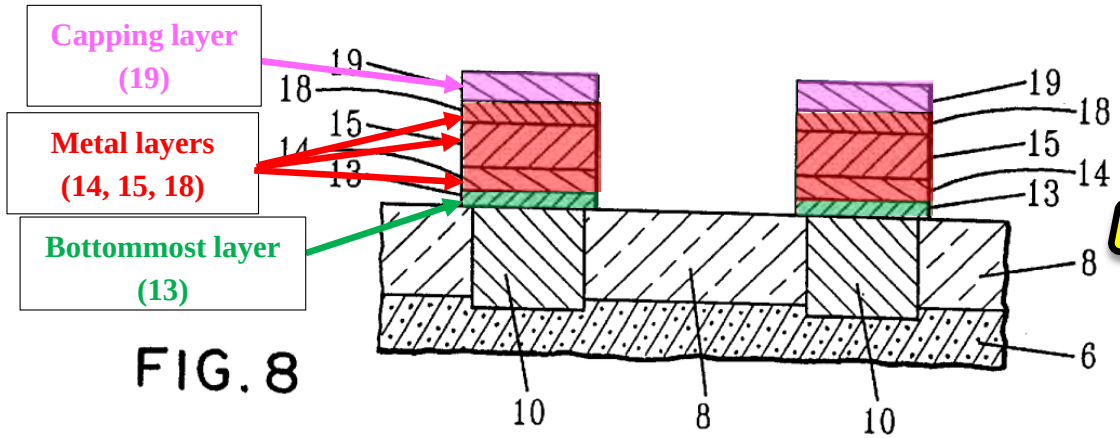
Dr. Zhao explains that gate leakage can also cause electromigration in gate electrodes, which is especially problematic for Schottky connections.

62. Furthermore, it was known that gate leakage can cause electromigration in gate electrodes. Leakage turns the gate from a voltage only node into a current-carrying conductor. Ex. 1018 at 937. Once sufficiently high current flows in the gate metal, the basic conditions for electromigration are met. This is especially problematic for gate electrode forming a Schottky connection because Schottky gates do not feature an insulating oxide to block current, and leakage increases exponentially with voltage and temperature. Ex. 1015 at 353-354. Thus, it is common and well known to make fabrication decisions preventing gate leakage as well as minimizing the effects of electromigration. Ex-1047, ¶62(annotated).

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

No electromigration?
Patent Owner contends the claimed "electrical contact" comprising an "electrode stack" cannot experience electromigration.

1C
A "semiconductor device" includes interconnect metallization structures.

Even Patent Owner's expert Dr. Piner agrees electromigration typically occurs at relatively high current densities

submicron level. EX-1004 (Usui), 1:35–37. Electromigration is the movement of atoms in a metal film due to momentum transfer from the electrons carrying the current. EX-2030 (Jaeger), 157. Metal interconnections in integrated circuits were operated at relatively high current densities. EX-2030 (Jaeger), 157. Under high-current-density conditions, metal-atom migration could cause voids (open circuit) in some regions and metal pileup, or hillocks, in other regions, which could cause short circuits. EX-2030 (Jaeger), 157; EX-2031 (Ohring), 380–381.

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ex-2024, ¶100 (Dr. Piner) (annotated).

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

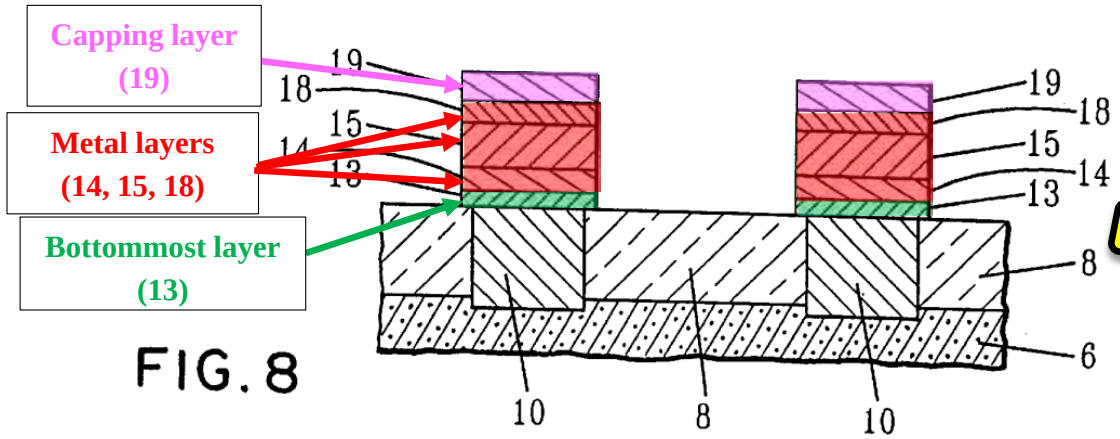


FIG. 8

Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

No electromigration?
Patent Owner contends the claimed "electrical contact" comprising an "electrode stack" cannot experience electromigration.

1C
A "semiconductor device" includes interconnect metallization structures.

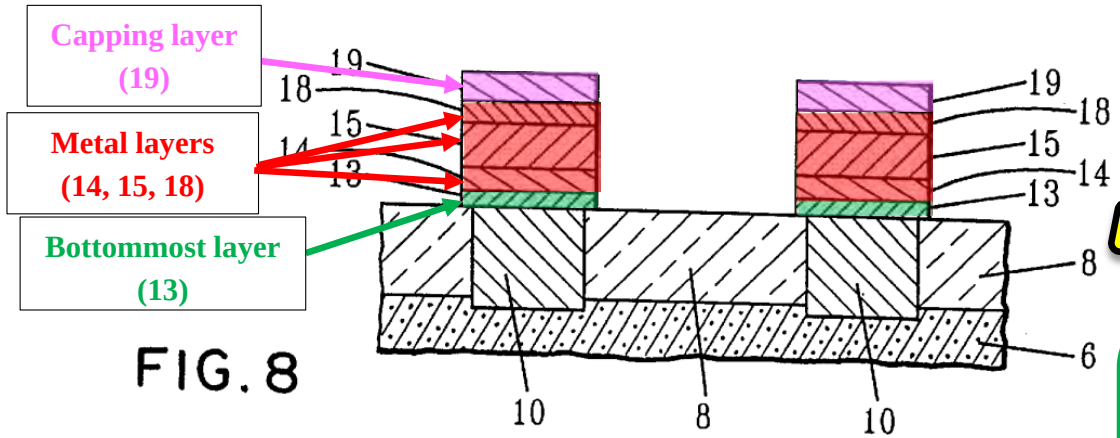
Prior Infineon (Patent Owner) patent agrees that electromigration typically occurs at relatively high current densities.

[0004] It is believed that the reduction in the size of the electrodes combined with an increase in the current load passing through the electrode and its solder connection, particularly in the presence of high switching frequencies, may result in a higher than desirable failure rate in the solder connection due, for example, to electromigration or the like phenomenon.

Ex-1043, ¶[0004], (US patent, 1:17-36) (annotated).

Pet., 8-13; Reply, 13-16; EX-1047, ¶¶52-63.

Ground 1: Usui anticipates claims 1, 2, and 4-7



Usui, Fig. 8 (annotated).

Usui	Limitation
✓	**[1a]** an **electrode stack** including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;

'562 pat., Claim 1.

Disputed

Usui discloses an electrode stack under Patent Owner's construction.

1A
Usui discloses an "electrode stack" under Patent Owner's (incorrect) first construction: requiring contact with a nonmetallic part of the semiconductor device. Reply, 8-12; EX-1047, ¶¶40-48.

1B
Usui discloses an "electrode stack" under Patent Owner's (incorrect) second construction: requiring control of the semiconductor device. Reply, 12-13; EX-1047, ¶¶49-51.

1C
A "semiconductor device" includes interconnect metallization structures. Reply, 13-16; EX-1047, ¶¶52-63.

Pet., 8-13; Reply, 8-16.

Ground 1: Usui anticipates claims 1, 2, and 4-7

Innoscience

Patent Owner relies on its construction to argue Usui's interconnect is not the claimed "electrode stack"

✓ [1a] an **electrode stack** (Usui grounds)

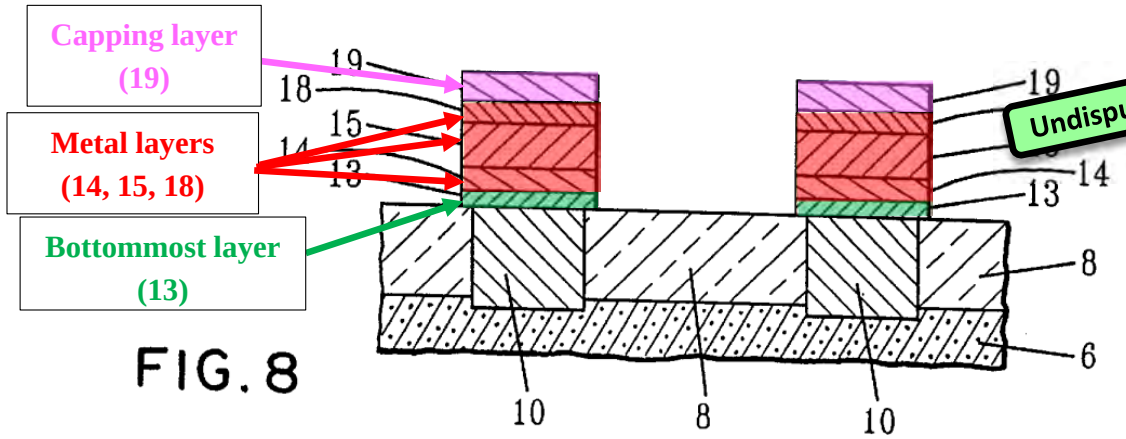
Usui discloses "electrode stack":

i. **under the plain and ordinary meaning; and**

ii. **under Patent Owner's construction.**

Pet., 8-13; Reply, 2-16; '562 pat., Claim 1.

Ground 1: Usui anticipates claims 1, 2, and 4-7



Usui, Fig. 8 (annotated).

Undisputed:
✓ **Usui discloses a capping layer consisting only of a refractory metal nitride (TiN)**

Usui	Limitation
✓ Undisputed	**[1b]** said capping layer consisting only of a refractory metal nitride,

'562 pat., Claim 1.

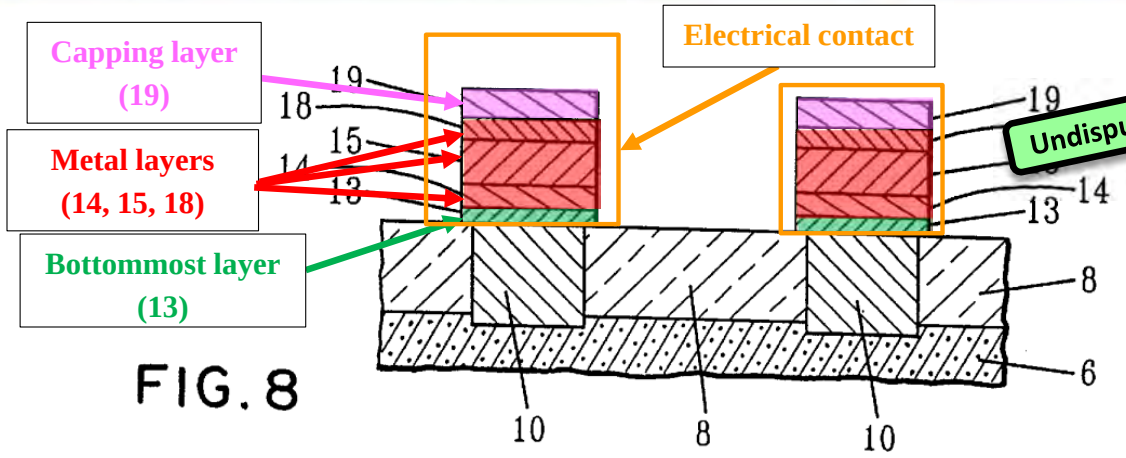
Capping layer (19)

same way as for layer **13**. From FIG. **5**, onto the metal layer **18** is then blanket deposited the suitable capping layer **19** to complete the interconnect metallurgy at this level. The capping layer is preferably titanium nitride and can be deposited in the same manner as the titanium nitride layer **14**. The purpose of this layer is to limit the amount of light

Usui, 5:54-59 (annotated).

Pet., 8-13; Reply, 8-16.

Ground 1: Usui anticipates claims 1, 2, and 4-7



Usui, Fig. 8 (annotated).

Undisputed:

✓ **Usui discloses a refractory metal nitride forming a top of the electrical contact and having a thickness greater than that of a bottommost layer of the metal layers**

Usui	Limitation
✓ Undisputed	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

'562 pat., Claim 1.

Capping layer (19)

of a group IVA metal, preferably titanium with a titanium nitride layer **19**. Typically the titanium nitride layer is about 150 to about 800 angstroms and more typically about 200 to about 500 angstroms. Typically, the titanium layer is about

Usui, 4:5-8 (annotated).

preferably a layer of titanium. Critical to the success of the present invention is having the thickness of this underlayer **13** being between about 90 angstroms to about 110 angstroms. As will be demonstrated hereinbelow, by limiting the

Usui, 3:29-32 (annotated).

Pet., 8-13; Reply, 8-16.

Ground 1: Usui anticipates claims 1, 2, and 4-7

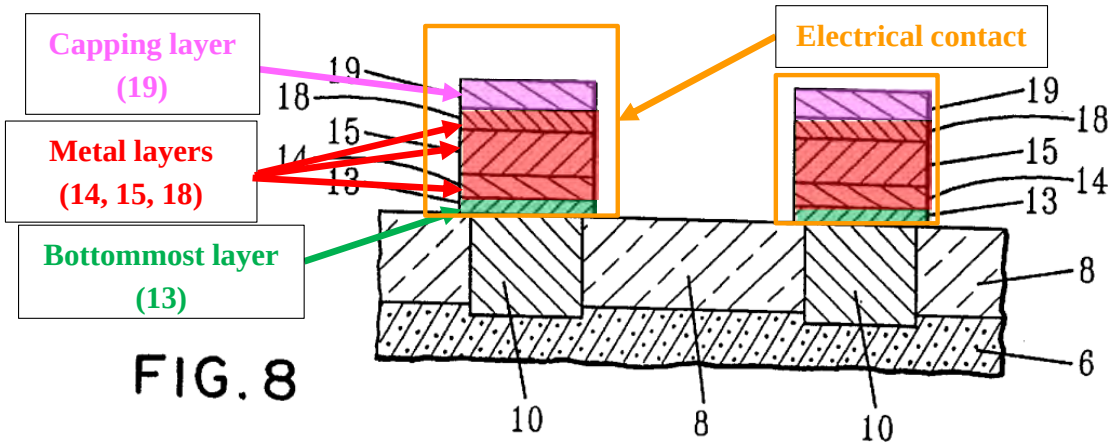


FIG. 8

Usui, Fig. 8 (annotated).

Undisputed:
✓ Usui discloses a capping layer comprising TiN

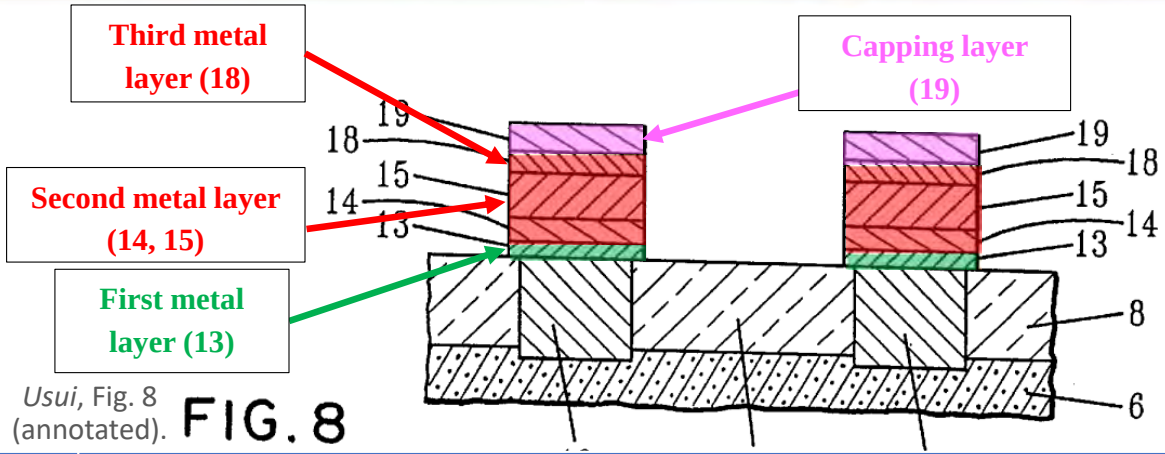
18 is then blanket deposited the suitable capping layer **19** to complete the interconnect metallurgy at this level. The capping layer is preferably titanium nitride and can be

Usui, 5:55-57 (annotated).

Usui	Limitation
✓ Undisputed	**[2]** The electrical contact of claim 1, wherein said capping layer comprises titanium nitride (TiN).

Pet., 11, 13; '562 Pat., Claim 2.

Ground 1: Usui anticipates claims 1, 2, and 4-7



Usui, Fig. 8 (annotated). FIG. 8

Usui	Limitation
✓	**[4]** The electrical contact of claim 1, wherein said plurality of **metal layers** includes respective **first**, **second (14, 15)**, and **third (18)** metal layers, wherein said second metal layer is formed between said first metal layer and said third metal layer, and said **capping layer** is formed on said third metal layer.
✓	**[5]** The electrical contact of claim 4, wherein said **first metal layer** and said **third metal layer (18)** of said electrode stack comprise titanium (Ti).
✓	**[6]** The electrical contact of claim 4, wherein said **second metal layer (14, 15)** of said electrode stack comprises aluminum (Al).
✓	**[7]** The electrical contact of claim 6, wherein said **second metal layer (14, 15)** of said electrode stack further comprises silicon (Si).

Pet., 13-16; '562 Pat., Claims 4-7.

Third metal layer (18)

layers are titanium nitride and combinations of as layer **18** of a group IVA metal, preferably titanium with a titanium

Usui, 4:4-5 (annotated).

Second metal layer (14, 15)

with underlayer **13**. Layer **15** is aluminum or an aluminum alloy. Typical aluminum alloys include alloying metal such as copper, magnesium, silicon, lanthanides such as vanadium and yttrium; and palladium. Preferably, the amount of

Usui, 3:38-41 (annotated).

Although not required, it is preferred that a titanium nitride layer **14** be located intermediate the group IVA layer

Usui, 3:58-59 (annotated).

First metal layer (13)

used for deposition of the titanium layer **13** or in a different

Usui, 5:38 (annotated).

Undisputed

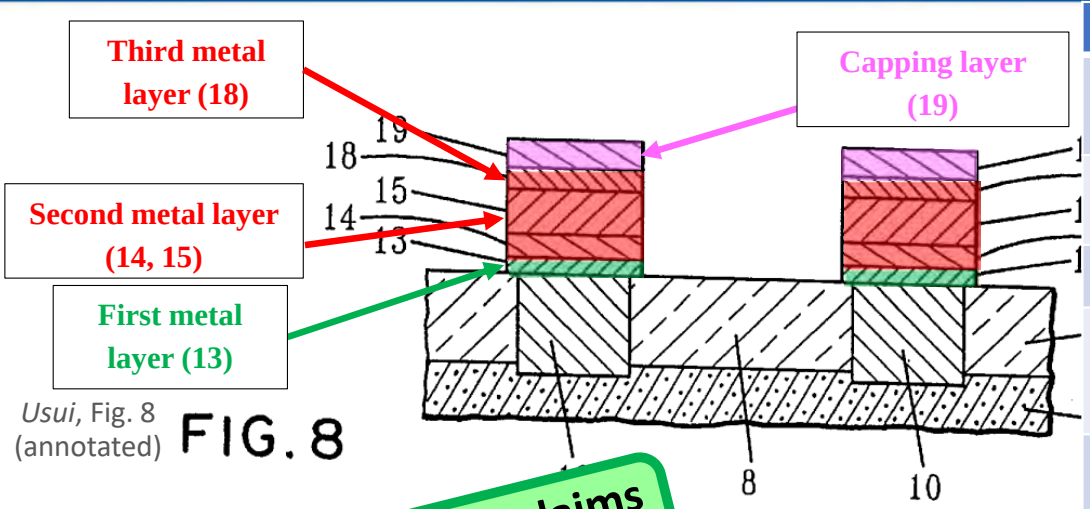
Undisputed

Undisputed

Undisputed

Undisputed:
✓ **Usui discloses claimed arrangement and composition of metal layers and capping layer**

Ground 1: Usui anticipates claims 1, 2, and 4-7



Usui, Fig. 8 (annotated) FIG. 8

Petitioner has shown the claims are anticipated by Usui

All of Patent Owner's Arguments Fail

Pet., 8-16; Reply, 2-16; '562 Pat., Claims 1, 2, 4-7.

Usui	Limitation
✓	**[1p]** An **electrical contact** for use on a semiconductor device, said electrical contact comprising:
✓	**[1a]** an electrode stack including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;
✓	**[1b]** said **capping layer** consisting only of a refractory metal nitride,
✓	**[1c]** said **refractory metal nitride** forming a top of said **electrical contact** and having a thickness greater than that of a **bottommost layer** of said plurality of metal layers.
✓	**[2]** The electrical contact of claim 1, wherein said **capping layer** comprises titanium nitride (TiN).
✓	**[4]** The electrical contact of claim 1, wherein said plurality of **metal layers** includes respective **first**, **second (14, 15)**, and **third (18)** metal layers, wherein said second metal layer is formed between said first metal layer and said third metal layer, and said **capping layer** is formed on said third metal layer.
✓	**[5]** The electrical contact of claim 4, wherein said **first metal layer** and said **third metal layer (18)** of said electrode stack comprise titanium (Ti).
✓	**[6]** The electrical contact of claim 4, wherein said **second metal layer (14, 15)** of said electrode stack comprises aluminum (Al).
✓	**[7]** The electrical contact of claim 6, wherein said **second metal layer (14, 15)** of said electrode stack further comprises silicon (Si).

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience

Usui Grounds

Yu Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	Usui
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu
3	9, 11, 14, and 16	§ 103	Usui, Yu, and Adesida
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	Yu and Usui
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida
7	10 and 15	§ 103	**Yu**, Usui, and Sugimoto

To find claims 3, 8, 12, 13, and 17 invalid over Usui and Yu (Ground 2), the Board need only agree that implementing Usui's electrode stack in Yu's device would have been obvious.

Pet., 3.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience

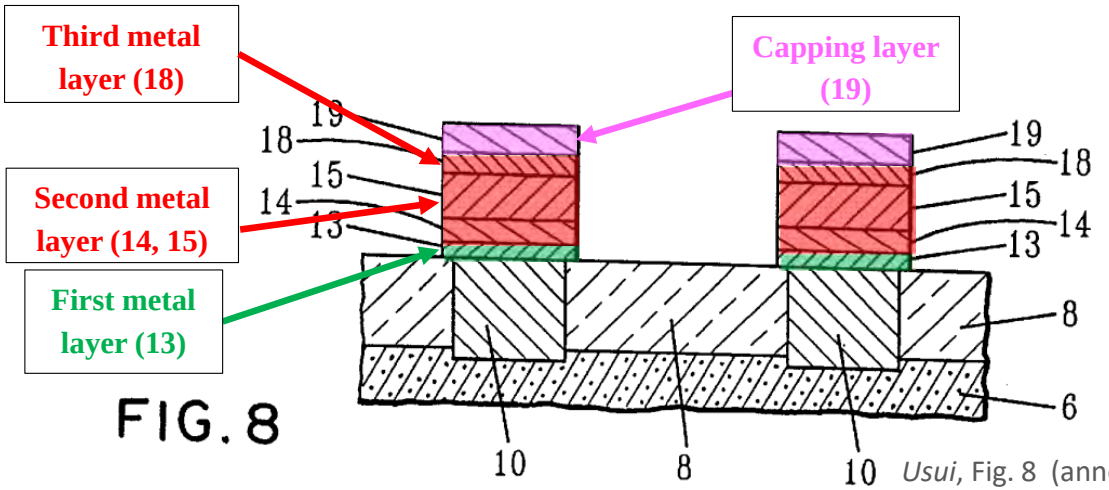


FIG. 8

Usui, Fig. 8 (annotated).

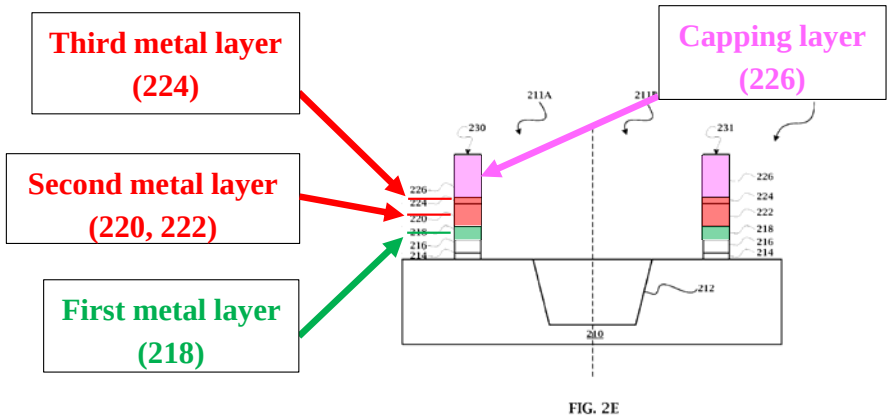


FIG. 2E

Yu, Fig. 2E (annotated).

Usui-Yu	Limitation
✓	**[3]** The electrical contact of claim 1, wherein said capping layer comprises tantalum nitride (TaN).
✓	**[8]** The electrical contact of claim 1, wherein said electrical contact is configured for implementation on a group III-V semiconductor device.
✓	**[12]** The electrical contact of claim 8, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.
✓	**[13p]** An electrical contact for use on a group III-V semiconductor device … [Usui discloses body of claim 13, as explained for claim 1].
✓	**[17]** The electrical contact of claim 13, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

Undisputed

Undisputed

Motivation to Combine (MTC) Disputed

Undisputed

Pet., 15-23, 35; Reply, 17-20; '562 Pat., Claims 3, 8, 12, 13, 17.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience

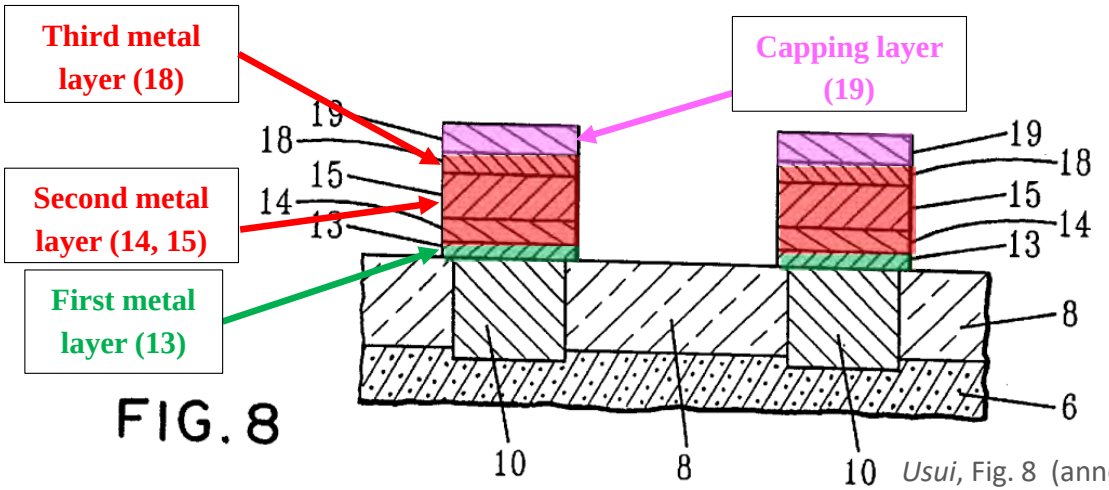


FIG. 8

Usui, Fig. 8 (annotated).

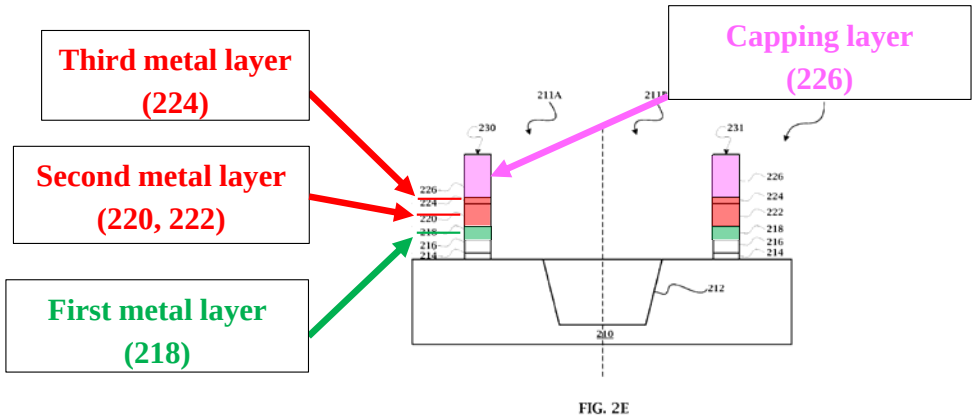


FIG. 2E

Yu, Fig. 2E (annotated).

Undisputed:

✓ **It would have been obvious to combine Usui and Yu to disclose a capping layer comprising TaN**

present embodiment, over the diffusion barrier layer **224**. The capping layer **226** may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantulum, titanium nitride, tantalum nitride, nickel silicide, cobalt

Yu, ¶[0036] (annotated).

Usui-Yu	Limitation
✓	**[3]** The electrical contact of claim 1, wherein said capping layer comprises tantalum nitride (TaN).

Undisputed

Pet., 15-18, 20-21, 35; Reply, 17-20; '562 Pat., Claim 3.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience

Patent Owner only disputes the motivation to combine Usui with Yu for claims 12 and 17

✓ Motivation to combine Usui with secondary references (grounds 2-4)

Petition shows it would have been obvious to implement Usui's electrical contact in Yu's device

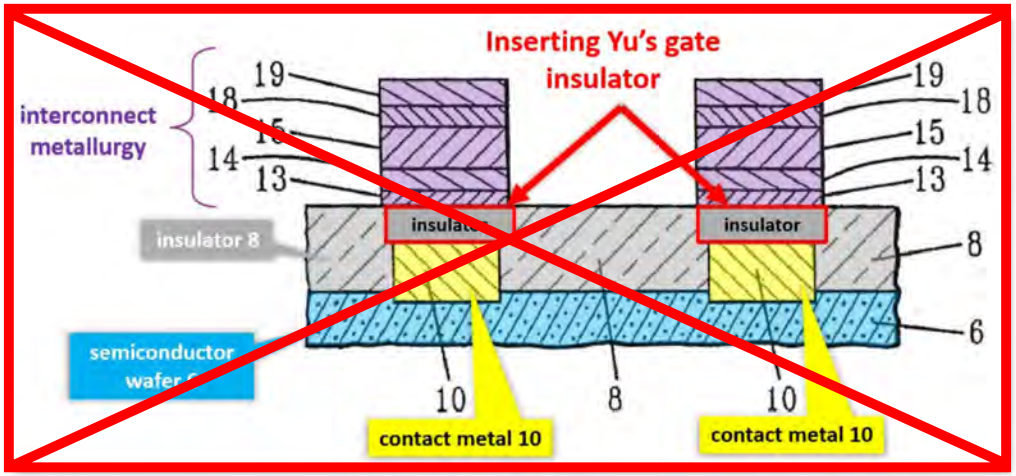
Pet., 16-23; Reply, 17-20.

Ground 2: Patent Owner invents their own combination of Usui and Yu

Innoscience

The Petition never included this combination or figure.

Patent Owner's made-up combination: Incorporating Yu's dielectric into Usui's device. This was not the Petition's combination.



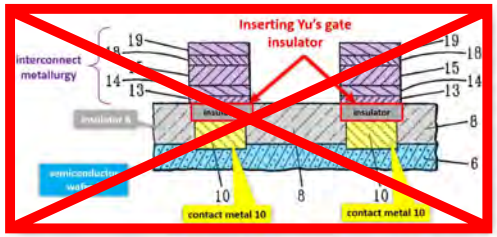
Ex-2024, ¶164 (adding red X to Patent Owner's figure).

- ✓ **Patent Owner's arguments on this made-up combination are non-responsive.**
- ✓ **Further argument not in the Patent Owner's response is forfeited.**

Pet., 16-23; Reply, 17-20.

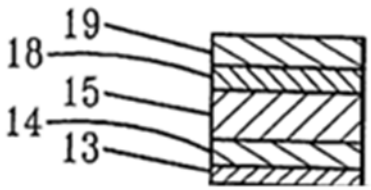
Ground 2: Patent Owner invents their own combination of Usui and Yu

Patent Owner's made-up combination:

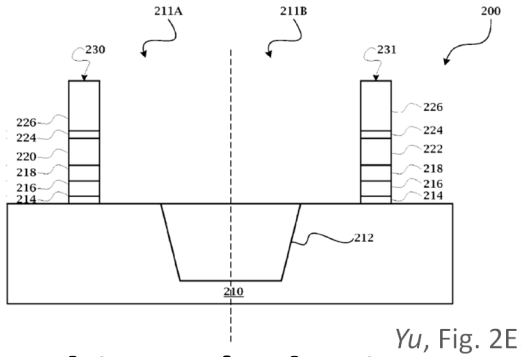


Ex-2024, ¶164 (adding red X to Patent Owner's figure).

Petitioner's real combination:



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Usui's metallurgy implemented in Yu's device

> **b.** **Claims 8 and 13 – A POSITA would have been motivated to implement Usui's electrical contact in a group III-V semiconductor device as taught by Yu.**

Pet., 18.

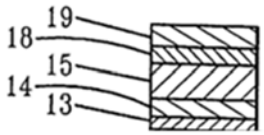
> **c.** **Claims 12 and 17 – A POSITA would have been motivated to implement Usui's device as a III-V device with a gate insulator layer, as taught by Yu.**

Pet., 19.

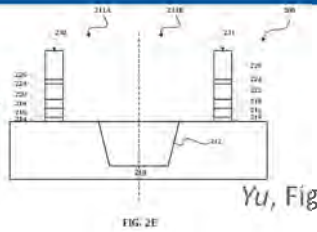
Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

✓ **Would have been obvious to use Usui's contact in Yu's device to improve electromigration characteristics**

GaN (III-V semiconductor) were known to have good electron transport properties

Pet., 18.

transistor of Yu. Because Usui's device provides improved electromigration characteristics, it would have been obvious for the POSITA to place the Usui contact in the III-V semiconductor transistor of Yu as such materials (i.e., III-V materials) are commonplace within the field and was known in the art, as evidenced by Section VII.B.1.b. Zhao ¶¶48-50, 60-61, 119.

Pet., 21 (annotated).

Additionally, GaN was known to have excellent electron transport properties, including good mobility, and high saturated drift velocity. Ex-1008, 4. These

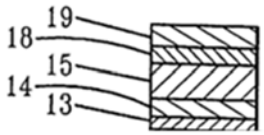
Ex-1002, ¶49 (Decl. of Dr. Zhao) (annotated).

However, there still remains room for improvement of the electromigration characteristics. Accordingly, an objective of the present invention is to provide a structure that exhibits enhanced electromigration performance along with being

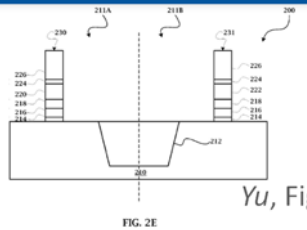
Usui, 2:33-36 (annotated).

Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Patent Owner relies on a misapplication of electromigration to argue Usui-Yu lacks a motivation to combine

Usui solves the problem of electromigration that would have been present in Yu.

2A
"enhanced electromigration" is less electromigration. Reply, 18-20.

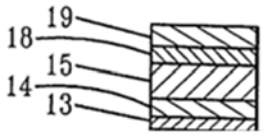
2B
Electromigration can be found in electrodes. Reply, 19.

2C
Usui's principles to improve electromigration characteristics in Yu's device would improve the Usui-Yu contact. Pet., 19-20; Reply, 19-20.

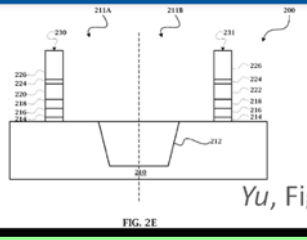
Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Usui solves the problem of electromigration

> [57] **ABSTRACT**
>
> A metallization structure is fabricated by depositing an underlayer of a group IVA metal having a thickness of about 90 to about 110 angstroms, and depositing a layer of aluminum and/or an aluminum alloy. The metallization structure obtained exhibits enhanced electromigration and is highly textured and is especially suitable for forming electrical connections or wiring.

Usui, Abstract.

1. Usui uses the phrase "enhanced migration" to describe reducing electromigration.

2. The Board should reject Patent Owner's argument that a POSA would not have sought "enhanced electromigration" because Usui repeatedly describes enhanced electromigration.

Both parties agree that Usui teaches reducing electromigration

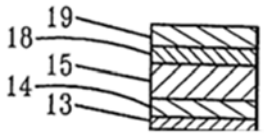
Patent Owner agrees POSITAs would have sought "'improvement in the electromigration characteristics' of 'electrical connections and wiring' by reducing electromigration."	POR, 40 (citing Usui, 1:17-20, 2:33-39; Ex-2026 (Zhao-Dep.), 13:23-14:9, 53:8-54:25; Piner, ¶219).
Usui discloses "forming various electrical connections or wiring in electronic devices such as in integrated circuit structures" and "an objective of the present invention is to provide a structure that exhibits enhanced electromigration performance."	Usui, 1:17-20, 2:33-39.
Dr. Zhao agrees that improving electromigration is reducing its negative effects.	Ex-2026, 13:23-14:9 (Zhao Deposition).

2A
"enhanced electromigration" is less electromigration. Reply, 18-20.

Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience



Usui, Fig. 8 (modified).

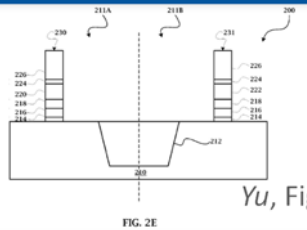


FIG. 2E

Yu, Fig. 2E.

According to preferred aspects of the present invention, at least the titanium and, when employed, titanium nitride layers are coherently deposited by collimation or "long throw" in order to achieve optimum electromigration performance. Structures prepared with a collimated or long throw deposition for the titanium and, if present, titanium nitride layers demonstrate a significantly improved electromigration performance as compared to those deposited

Usui, 6:34-42 (annotated).

electromigration characteristics. Accordingly, an objective of the present invention is to provide a structure that exhibits enhanced electromigration performance along with being

Usui, 2:33-35 (annotated).

2A
"enhanced electromigration" is less electromigration. Reply, 18-20.

Usui plainly describes "enhanced," "optimum," and "improved" electromigration by reducing its negative effects

the group IVA metal. The process of the present invention provides a metallization structure that exhibits enhanced electromigration characteristics along with

Usui, 2:50-52 (annotated).

volume fraction (e.g. <20 percent) of random grains. This textured structure is significant in achieving the greatly improved electromigration performance obtained pursuant to the present invention.

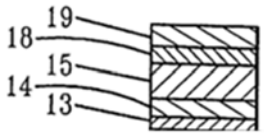
Usui, 3:54-57 (annotated).

purity titanium film being deposited. This is especially important for the top titanium layer, which needs to be of the highest purity in order to maximize the electromigration performance.

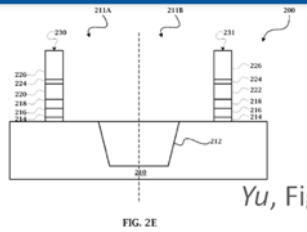
Usui, 6:64-67 (annotated).

Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Dr. Piner and Dr. Zhao share the same general understanding of electromigration.

Dr. Piner

electromigration. "The term electromigration refers to the current induced mass transport which occurs in a conductive material maintained at an elevated temperature and through which current is passed wherein atoms of conductor material are displaced as a result of the combined effects of direct momentum exchange from the moving electrons and the influence of the applied electric field." EX-2029 (U.S. Patent No. 4,017,890, "Howard"), 1:27-45.

Ex-2024, ¶66 (Dr. Piner) (annotated).

Dr. Zhao

Q. What is your understanding of the phrase improve electro migration?

A. To improve the electromigration by reducing some the negative effects.

Q. And what negative effects are you referring to?

A. In electromigration and what you see is metal, one the example of electromigration is the metal atom will diffuse into semiconductor layers, leading to reliability issues. One of the common way to, to mitigate, to improve the electromigration is to putting the diffusion barrier layer.

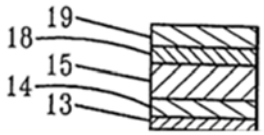
Ex-2026, 13:23-14:9 (Dr. Zhao Deposition) (annotated).

2A
"enhanced electromigration" is less electromigration. Reply, 18-20.

Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience



Usui, Fig. 8 (modified).

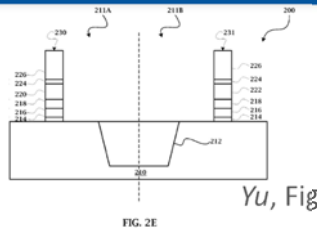


FIG. 2E

Yu, Fig. 2E.

Patent Owner relies on a misapplication of electromigration to argue Usui-Yu lacks a motivation to combine

Usui solves the problem of electromigration that would have been present in Yu.

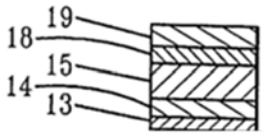
2A
"enhanced electromigration" is less electromigration. Reply, 18-20.

2B
Electromigration can be found in electrodes. Reply, 19.

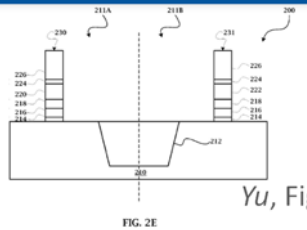
2C
Usui's principles to improve electromigration characteristics in Yu's device would improve the Usui-Yu contact. Pet., 19-20; Reply, 19-20.

Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Patent Owner relies on a misapplication of electromigration to argue Usui-Yu lacks a motivation to combine

Usui solves the problem of electromigration that would have been present in Yu.

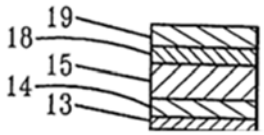
2A
"enhanced electromigration" is less electromigration. Reply, 18-20.

2B
Electromigration can be found in electrodes. Reply, 19.

2C
Usui's principles to improve electromigration characteristics in Yu's device would improve the Usui-Yu contact. Pet. 19-20; Reply, 19-20.

Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17



Usui, Fig. 8 (modified).

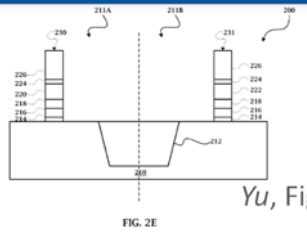


FIG. 2E

Yu, Fig. 2E.

Dr. Zhao and an Infineon patent publication (Patent Owner) explain that electromigration principles can be found in electrodes.

Infineon (Patent Owner) patent publication

[0004] It is believed that the reduction in the size of the electrodes combined with an increase in the current load passing through the electrode and its solder connection, particularly in the presence of high switching frequencies, may result in a higher than desirable failure rate in the solder connection due, for example, to electromigration or the like phenomenon.

Ex-1043, ¶[0004] (annotated).

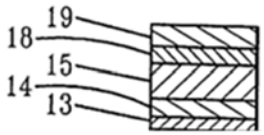
Ex. 1043 at 1:17-36 (emphases added). This passage describes electromigration between electrodes of a semiconductor power transistor and its external connections due to high current through the electrodes. And the electrodes described in this Infineon patent, which purportedly benefit from the improved electromigration characteristics it seeks, include "power electrode 14 (e.g., source electrode or emitter electrode) and control electrode 16 (e.g., gate electrode), respectively." Ex. 1043 at 2:39-61, Fig. 1. As this Infineon patent shows, Dr. Piner is simply wrong that Usui's interconnect is not an "electrode stack" because it experiences electromigration. Instead, as this patent shows, a POSITA would have understood that electrodes would receive the electromigration benefits that Usui describes, as I discussed in my first declaration and deposition. Ex. 1002 at ¶¶ 73, 84, 101, 113-114, 118-119, 121-

Ex-1047, ¶60 (annotated); *see also* Ex-1047, ¶¶57-59, 61-63.

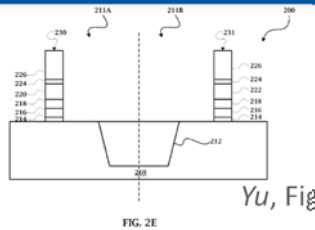
2B
Electromigration can be found in electrodes. Reply, 19.

Pet., 16-23; Reply, 15-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Patent Owner relies on a misapplication of electromigration to argue Usui-Yu lacks a motivation to combine

Usui solves the problem of electromigration that would have been present in Yu.

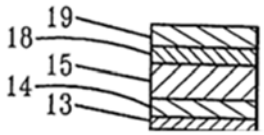
2A
"enhanced electromigration" is less electromigration. Reply, 18-20.

2B
Electromigration can be found in electrodes. Reply, 19.

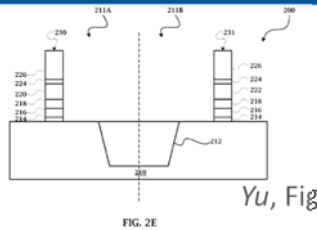
2C
Usui's principles to improve electromigration characteristics in Yu's device would improve the Usui-Yu contact. Pet., 19-20; Reply, 19-20.

Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Patent Owner relies on a misapplication of electromigration to argue Usui-Yu lacks a motivation to combine

Usui solves the problem of electromigration that would have been present in Yu.

2A
"enhanced electromigration" is less electromigration. Reply, 18-20.

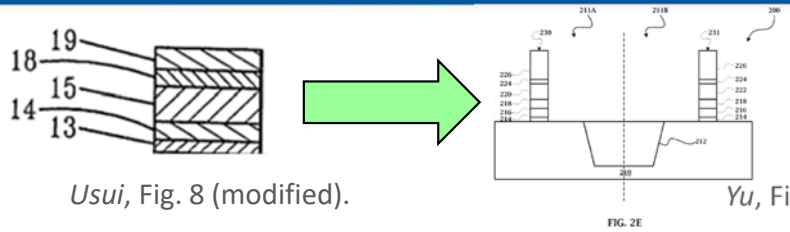
2B
Electromigration can be found in electrodes. Reply, 19.

2C
Usui's principles to improve electromigration characteristics in Yu's device would improve the Usui-Yu contact. Pet., 19-20; Reply, 19-20.

Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience



Usui, Fig. 8 (modified). *Yu*, Fig. 2E.

Usui would have solved the electromigration problems in Yu:

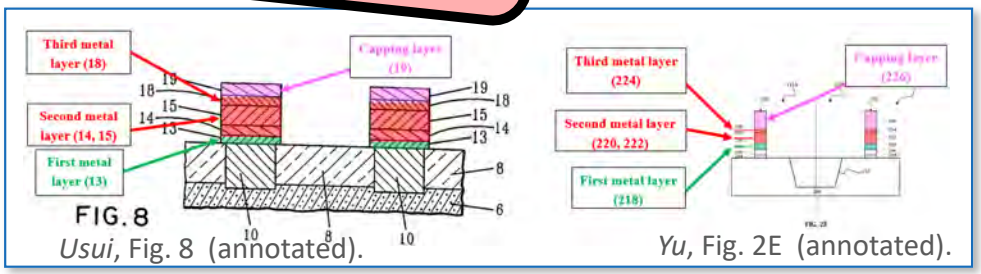
Usui and Yu have the same capping and metal layers, so Usui's layers would function like Yu's layers.

Usui with a gate insulating layer. Petition, 20. If Petitioner belatedly were to allege that a POSA would have replaced Yu's gate electrode with Usui's metal stack, that would fail for multiple reasons. First, it would preclude application of the *KSR* rationale Petitioner invokes (Petition, 20) because it would change the function of *Usui's* metal layers from a single interconnect layer – connecting metal stud 10 to another interconnect level forming an interconnect circuit to another device (Usui, 3:23-27, 4:10-15) – to a gate electrode. Piner, ¶175. Second, POSAs

POR, 27 n.10 (annotated).

Patent Owner mistakenly contends that the function of Usui's metal layers would be changed in Yu's device

2C
Usui's principles to improve electromigration characteristics in Yu's device would improve the Usui-Yu contact. Pet., 19-20; Reply, 19-20.

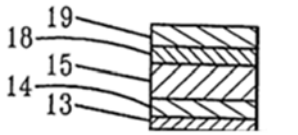


Usui, Fig. 8 (annotated). *Yu*, Fig. 2E (annotated).

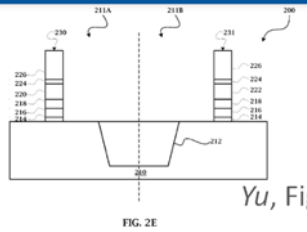
Pet., 14-23, 35.

Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

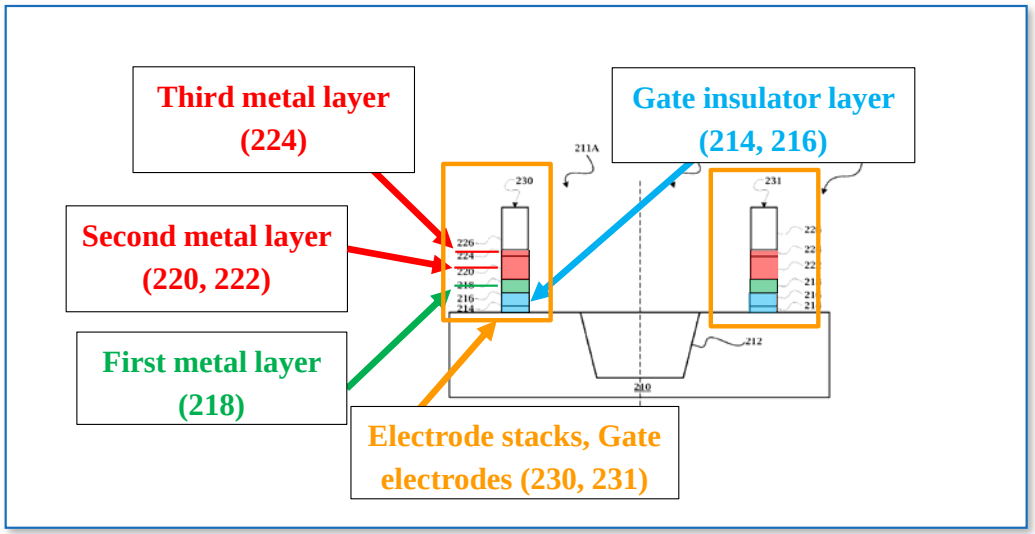


Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Yu's insulating layers further reduce electromigration due to its diffusion barrier, which is known for inhibiting unwanted metal migration



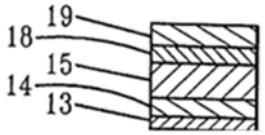
Yu, Fig. 2E (annotated); Pet., 54.

2C
Usui's principles to improve electromigration characteristics in Yu's device would improve the Usui-Yu contact. Pet., 19-20; Reply, 19-20.

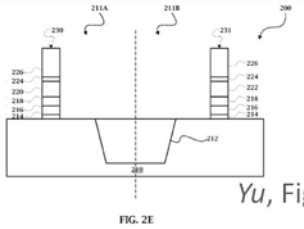
Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Patent Owner relies on a misapplication of electromigration to argue Usui-Yu lacks a motivation to combine

Usui solves the problem of electromigration that would have been present in Yu.

2A
"enhanced electromigration" is less electromigration. Reply, 18-20.

2B
Electromigration can be found in electrodes. Reply, 19.

2C
Usui's principles to improve electromigration characteristics in Yu's device would improve the Usui-Yu contact. Pet., 19-20; Reply, 19-20.

Pet., 16-23; Reply, 17-20.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience

Patent Owner only disputes the motivation to combine Usui with Yu for claims 12 and 17

REJECTED

✓ Motivation to combine Usui with secondary references (grounds 2-4)

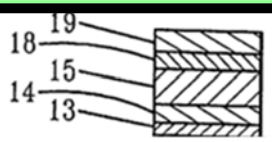
Petition shows it would have been obvious to implement Usui's electrical contact in Yu's device

Pet., 16-23; Reply, 17-20.

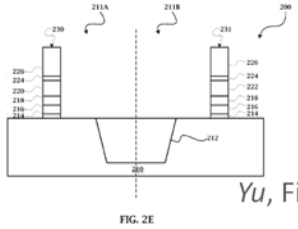
Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17

Innoscience

Usui-Yu renders obvious claims 8 and 13



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

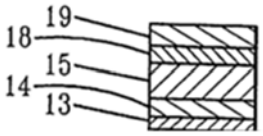
structure. In the present embodiment, the semiconductor substrate **210** comprises silicon, germanium, a group III-V material, or a group II-VI material.

Yu, ¶[0023] (annotated).

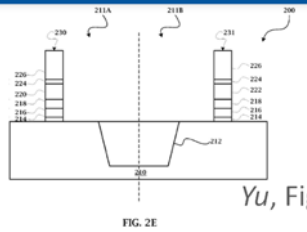
Usui-Yu	Limitation
Undisputed ✓	**[8]** The electrical contact of claim 1, wherein said electrical contact is configured for implementation on a **group III-V semiconductor device**.
Undisputed ✓	**[13p]** An electrical contact for use on a **group III-V semiconductor device** … [Usui discloses body of claim 13, as explained for claim 1].

Pet., 18-23; '562 pat., Claims 8, 13.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17



Usui, Fig. 8 (modified).



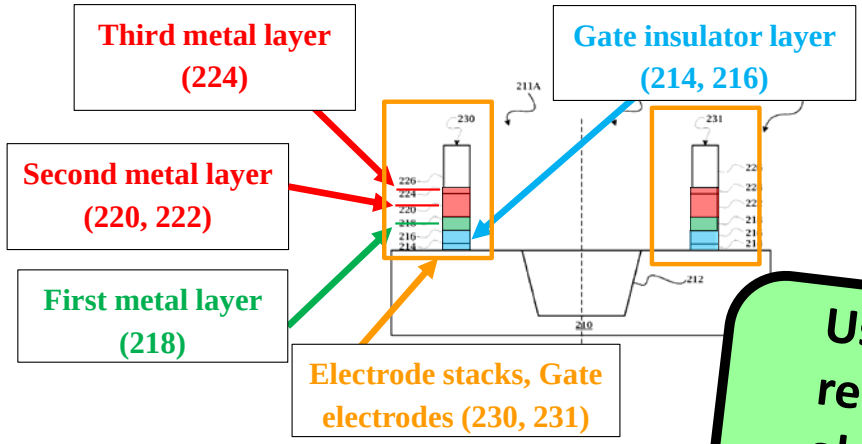
Yu, Fig. 2E.

the underlying layers (i.e., the interfacial dielectric layer **214**, the high-k dielectric layer **216**, the diffusion barrier/protec-

Yu, ¶[0039] (annotated).

The diffusion barrier/protection layer **218** may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present

Yu, ¶[0029] (annotated).



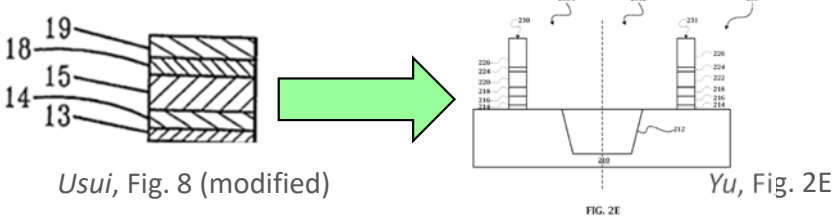
Yu, Fig. 2E (annotated); Pet., 54.

Usui-Yu renders obvious claims 12 and 17

Usui-Yu	Limitation
✓	**[12]** The electrical contact of claim 8, wherein said electrical contact is implemented with a **gate insulator layer** underlying said **first metal layer** of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.
✓	**[17]** The electrical contact of claim 13, wherein said electrical contact is implemented with a **gate insulator layer** underlying a **first metal layer** of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

Pet., 19-23, 54; Reply 17-20; '562 pat., Claims 12, 17.

Ground 2: Usui-Yu renders obvious claims 3, 8, 12, 13, and 17



Usui, Fig. 8 (modified)

Yu, Fig. 2E

Petitioner has shown the claims are rendered obvious by Usui-Yu

All of Patent Owner's Arguments Fail

Usui-Yu	Limitation
✓	**[3]** The electrical contact of claim 1, wherein said capping layer comprises tantalum nitride (TaN).
✓	**[8]** The electrical contact of claim 1, wherein said electrical contact is configured for implementation on a group III-V semiconductor device.
✓	**[12]** The electrical contact of claim 8, wherein said electrical contact is implemented with a **gate insulator layer** underlying said **first metal layer** of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.
✓	**[13p]** An electrical contact for use on a group III-V semiconductor device … [Usui discloses body of claim 13, as explained for claim 1].
✓	**[17]** The electrical contact of claim 13, wherein said electrical contact is implemented with a **gate insulator layer** underlying a **first metal layer** of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

Pet., 16-23; Reply, 17-20; '562 pat., Claims 3, 8, 12, 13, 17.

Ground 3: Usui-Yu-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience

Usui Grounds

Yu Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	Usui
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu
3	9, 11, 14, and 16	§ 103	**Usui**, Yu, and Adesida
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	Yu and Usui
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida
7	10 and 15	§ 103	**Yu**, Usui, and Sugimoto

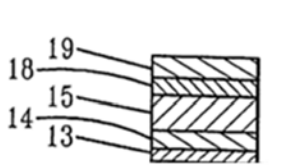
To find claims 9, 11, 14, and 16 invalid over Usui, Yu, and Adesida (Ground 3), the Board need only agree that implementing Usui-Yu's contact as a Schottky contact in a HEMT using the teachings of Adesida would have been obvious.

Pet., 3.

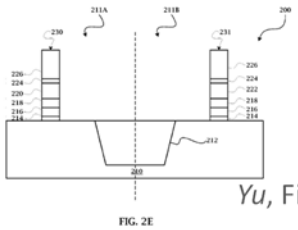
Ground 3: Usui-Yu-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience

Usui-Yu



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

HEMT

Schottky

Adesida's teachings

invention. The device of FIG. **5** is a high electron mobility transistor (HEMT), which, in this example, is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate **105** (therefore commonly called an InP HEMT or GaAs metamorphic HEMT) on which is deposited

$In_{0.53}Ga_{0.47}As$ cap layer **160**. Spaced apart source **170** and drain **180** ohmic contacts are formed on the n+ $In_{0.53}Ga_{0.47}As$ cap layer **160**, and the gate **190**, which is shown as a T-gate in this example, is formed with a Schottky barrier contact of length L_g on the $In_{0.52}Al_{0.48}As$ barrier layer **150**.

Adesida, ¶[0031] (annotated).

Motivation to Combine (MTC) Disputed

Usui-Yu-Adesida	Limitation
✓	**[9]** The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a **high electron mobility transistor (HEMT)**.
✓	**[11]** The electrical contact of claim 8, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.
✓	**[14]** The electrical contact of claim 13, wherein said group III-V semiconductor device comprises a **high electron mobility transistor (HEMT)**.
✓	**[16]** The electrical contact of claim 13, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

Pet., 24-29;
Reply, 20-22.

Ground 3: Usui-Yu-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience

Patent Owner only disputes the motivation to combine Usui-Yu with Adesida for claims 9, 11, 14, and 16

✓ Motivation to combine Usui with secondary references (grounds 2-4)

Petition shows it would have been obvious to implement Usui-Yu's contact as a Schottky contact in a HEMT using the teachings of Adesida

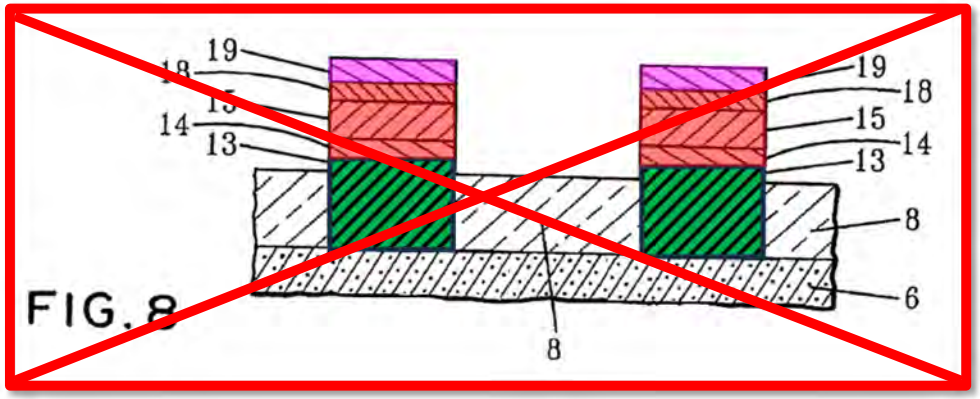
Pet., 24-29; Reply, 20-22.

Ground 3: Patent Owner invents their own combination of Usui, Yu, and Adesida

Innoscience

Patent Owner's made-up combination: Modifying Usui's device to have Adesida's Schottky contact.

The Petition never included this combination or figure.



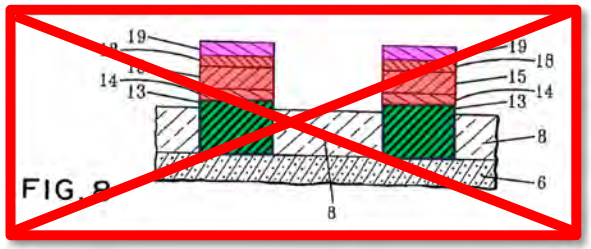
Reply, 21 (adding red "X" to Patent Owner's figure).

- ✓ **Patent Owner's arguments on this made-up combination are non-responsive.**
- ✓ **Further argument not in the Patent Owner's response is forfeited.**

Pet., 24-29; Reply, 20-22.

Ground 3: Patent Owner invents their own combination of Usui, Yu, and Adesida

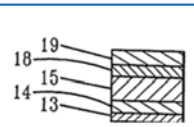
Patent Owner's made-up combination:



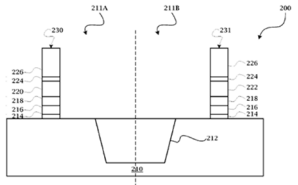
Reply, 21
(adding red "X" to Patent Owner's figure).

Petitioner's real combination:

Usui-Yu



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Adesida's teachings

HEMT

Schottky

Adesida, ¶[0031].

a. **Claims 9 and 14 - A POSITA would have been motivated to implement Usui's electrical contact on a group III-V semiconductor device, as taught by Yu, comprises a high electron mobility transistor (HEMT) as taught by Adesida**

Pet., 24.

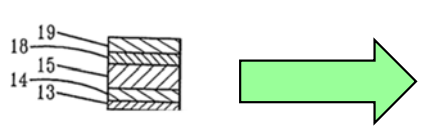
b. **Claims 11 and 16 - A POSITA would have been motivated to implement Usui's electrical contact as a gate electrode making Schottky contact, as taught by Adesida, with said group III-V semiconductor device as taught by Yu**

Pet., 25-26.

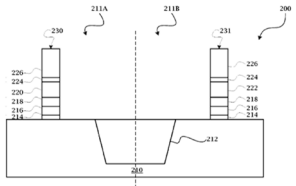
Pet., 24-29; Reply, 20-22.

Ground 3: Usui-Yu-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

HEMT

Schottky

Adesida, ¶[0031].

✓ **Would have been obvious to implement Usui-Yu's contact as a Schottky contact in a HEMT using the teachings of Adesida to improve electromigration characteristics**

Motivation to reduce electromigration in Schottky electrodes, especially at high frequencies, where leakage increases exponentially with voltage and temperature

Reply, 22.

carrying conductor. Ex. 1018 at 937. Once sufficiently high current flows in the gate metal, the basic conditions for electromigration are met. This is especially problematic for gate electrode forming a Schottky connection because Schottky gates do not feature an insulating oxide to block current, and leakage increases exponentially with voltage and temperature. Ex. 1015 at 353-354. Thus, it is common and well known to make fabrication decisions preventing gate leakage as well as minimizing the effects of electromigration.

Ex-1047, ¶62 (annotated).

POSITA would have used Adesida's Schottky approach for high frequency applications

Reply, 22.

Yu and Adesida disclose III-V semiconductor material devices

Yu, ¶[0023]; *Adesida*, ¶[0031].

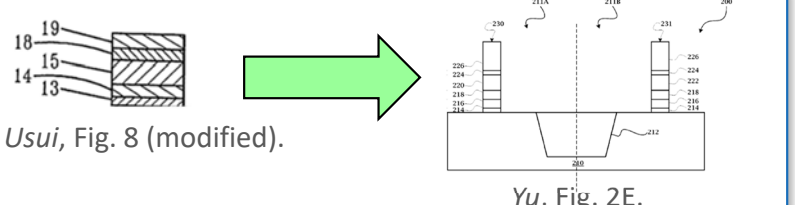
(citing Ex-1013, 144). It was well-known that Schottky contacts serve as gate contacts in group III-V devices and have excellent rectifying properties, which make them suitable for high frequency applications. Zhao ¶¶59, 132.

Pet., 26 (annotated).

Pet., 24-29; Reply, 20-22; Ex. 1002, ¶¶59, 132.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 3: Usui-Yu-Adesida renders obvious claims 9, 11, 14, and 16



Usui, Fig. 8 (modified).

Yu, Fig. 2E.

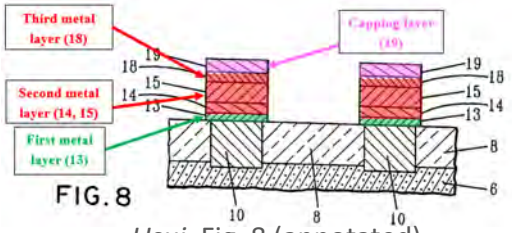
HEMT

Schottky

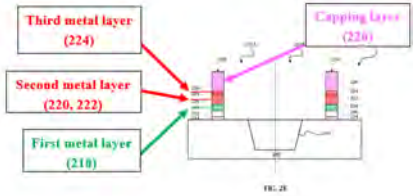
Adesida, ¶[0031].

Usui's and Yu's metal and capping layers are formed from the same type of materials

See, e.g., Pet. 15-23, 35; Ex-1002, ¶49.



Usui, Fig. 8 (annotated).



Yu, Fig. 2E (annotated).

Usui enhancing electromigration by reducing its negative effects

Pet., 16-23; Reply, 17-20.

electromigration characteristics. Accordingly, an objective of the present invention is to provide a structure that exhibits enhanced electromigration performance along with being

Usui, 2:33-35 (annotated).

Patent Owner incorrectly contends Usui's electrode is "dramatically changed" in combination with Yu

Pet., 24-29; Reply, 20-22.

Zhao-Dep., 58:17-60:1. Because the function of Usui's alleged electrode is dramatically changed in Petitioner's combination – from being an "interconnect

Reply, 21.

POR, 31 (annotated).

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 3: Usui-Yu-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience

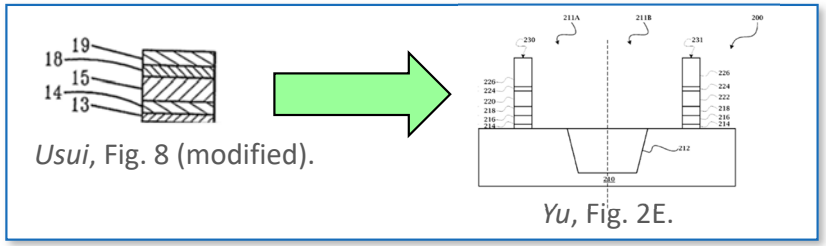
Patent Owner only disputes the motivation to combine Usui-Yu with Adesida for claims 9, 11, 14, and 16

✓ Motivation to combine Usui with secondary references (grounds 2-4)

Petition shows it would have been obvious to implement Usui-Yu's contact as a Schottky contact in a HEMT using the teachings of Adesida

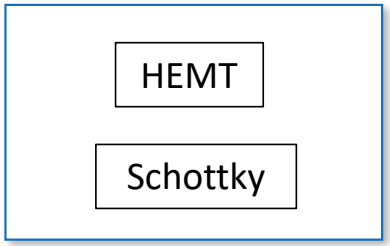
Pet., 24-29; Reply, 20-22.

Usui-Yu-Adesida renders obvious claims 9 and 14



Usui, Fig. 8 (modified).

Yu, Fig. 2E.



Adesida, ¶[0031].

Pet., 24-25.

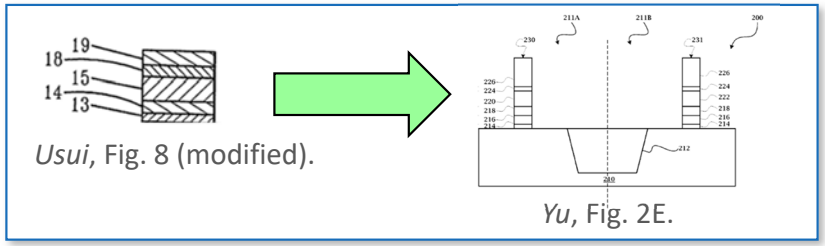
invention. The device of FIG. **5** is a high electron mobility transistor (HEMT), which, in this example, is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate **105** (therefore commonly called an InP HEMT or GaAs metamorphic HEMT) on which is deposited

Adesida, ¶[0031] (annotated).

Usui-Yu-Adesida	Limitation
✓	**[9]** The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a **high electron mobility transistor (HEMT)**.
✓	**[14]** The electrical contact of claim 13, wherein said group III-V semiconductor device comprises a **high electron mobility transistor (HEMT)**.

Pet., 24-29; Reply 20-22; '562 pat., Claims 9, 14.

Usui-Yu-Adesida renders obvious claims 11 and 16



Usui, Fig. 8 (modified).

Yu, Fig. 2E.

HEMT

Schottky

Pet., 25-27.

Adesida, ¶[0031].

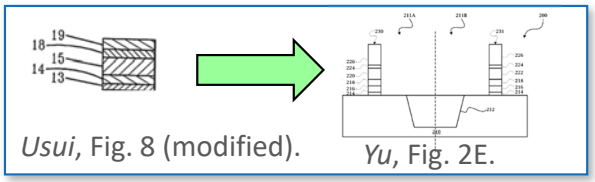
$In_{0.53}Ga_{0.47}As$ cap layer **160**. Spaced apart source **170** and drain **180** ohmic contacts are formed on the n+ $In_{0.53}Ga_{0.47}As$ cap layer **160**, and the gate **190**, which is shown as a T-gate in this example, is formed with a Schontky barrier contact of length L_g on the $In_{0.52}Al_{0.48}As$ barrier layer **150**.

Adesida, ¶[0031] (annotated).

Usui-Yu-Adesida	Limitation
✓	**[11]** The electrical contact of claim 8, wherein said electrical contact is implemented as a **gate electrode making Schottky contact** with said **group III-V semiconductor device**.
✓	**[16]** The electrical contact of claim 13, wherein said electrical contact is implemented as a **gate electrode making Schottky contact** with said **group III-V semiconductor device**.

Pet., 24-29; Reply, 20-22; '562 pat., Claims 11, 16.

Ground 3: Usui-Yu-Adesida renders obvious claims 9, 11, 14, and 16



Usui, Fig. 8 (modified).

Yu, Fig. 2E.

HEMT

Schottky

Adesida, ¶[0031].

Petitioner has shown the claims are rendered obvious by Usui-Yu-Adesida

All of Patent Owner's Arguments Fail

Usui-Yu-Adesida	Limitation
✓	**[9]** The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).
✓	**[11]** The electrical contact of claim 8, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.
✓	**[14]** The electrical contact of claim 13, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).
✓	**[16]** The electrical contact of claim 13, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

Pet., 24-29; Reply, 20-22; '562 Pat., Claims 9, 11, 14, 16.

Ground 4: Usui-Yu-Sugimoto renders obvious claims 10 and 15

Innoscience

Usui Grounds

Yu Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	Usui
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu
3	9, 11, 14, and 16	§ 103	Usui, Yu, and Adesida
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	Yu and Usui
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida
7	10 and 15	§ 103	Yu, Usui, and Sugimoto

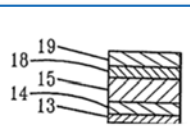
For Ground 4, the Board need only agree that it would have been obvious to make one change to Usui-Yu's power electrode:
Make ohmic contact following Sugimoto.

Pet., 3.

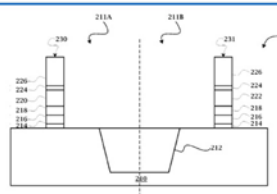
Ground 4: Usui-Yu-Sugimoto renders obvious claims 10 and 15

Innoscience

Usui-Yu's power electrode



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Sugimoto's teachings of ohmic contact

ohmic

located between the two. The drain electrode **42** and the source electrode **46** make ohmic contact with the top surface of the AlGaN layer **34**. The SI-GaN layer **62** is essentially

Sugimoto, 9:48-50 (annotated).

Motivation to Combine (MTC) Disputed

Usui-Yu-Sugimoto	Limitation
✓	**[10]** The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.
✓	**[15]** The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.

Pet., 29-33; Reply, 19, 22-24; '562 pat., Claims 10, 15.

Dr. Zhao explained that:

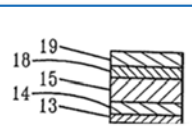
1. Enhanced electromigration is reduced electromigration;
2. ohmic contacts were known to be critical to device functionality, performance, and long-term reliability; and
3. ohmic contacts were known to minimize power consumption and internal heating and prolong device operation with predictable performance.

Ex-1002, ¶¶55-57 (Decl. of Dr. Zhao); Ex-2026, 13:23-14:9 (Dr. Zhao Deposition).

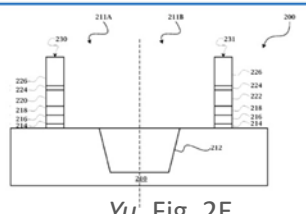
Ground 4: Usui-Yu-Sugimoto renders obvious claims 10 and 15

Innoscience

Usui-Yu's power electrode



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Sugimoto's teachings of ohmic contact

ohmic

located between the two. The drain electrode **42** and the source electrode **46** make ohmic contact with the top surface of the AlGaN layer **34**. The SI-GaN layer **62** is essentially

Sugimoto, 9:48-50 (annotated).

Patent Owner does not dispute obviousness of Yu as an ohmic contact

Infineon does not dispute it would have been obvious to implement Yu's CMOS device to have source and drain electrodes that are power electrodes making ohmic contact.

POR, 73.

Petitioner showed:

1. Usui discloses an electrical contact.
   (Ground 1, claim 1)

2. It would have been obvious to implement Usui's electrical contact in a group III-V semiconductor device as taught by Yu.
   (Ground 2, claims 8 and 13)

3. It would have been obvious to make Usui-Yu's power electrode make ohmic contact following Sugimoto.
   (Ground 4, claims 10 and 15)

Pet., 8-13, 18-19, 21, 23, 29-33.

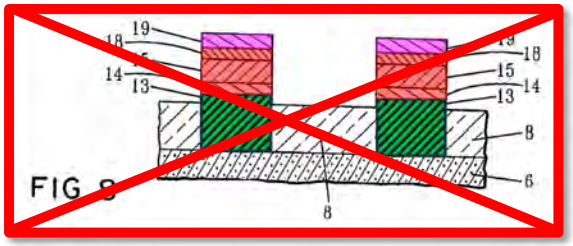
Pet., 29-33; Reply, 22-24.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 4: Patent Owner invents their own combination of Usui, Yu, and Sugimoto

Innoscience

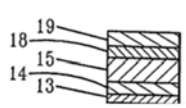
Patent Owner's made-up combination:



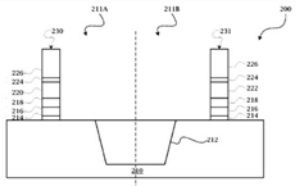
Reply, 23 (adding red X to Patent Owner's figure).

Petitioner's real combination:

Usui-Yu



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

Sugimoto's teachings

ohmic

Sugimoto, 9:48-50.

- ✓ **Patent Owner's arguments on this made-up combination are non-responsive.**
- ✓ **Further argument not in the Patent Owner's response is forfeited.**

A POSITA would have been motivated to implement the contact of Usui-Yu as a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide improved current flow (i.e., enhanced electromigration) and Sugimoto, like Yu, also teaches the use of III-V semiconductor devices. Furthermore, such a combination is the result of combining

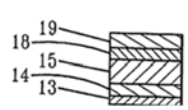
Pet., 31 (annotated).

A. So for ground 4, we are using Usui and Yu's teaching of those metal layers to form ohmic contact, and that ohmic contact will serve as power electrode on a III-V semiconductor device, as laid out in Sugimoto. And furthermore, Sugimoto further disclose this III-V device is a HEMT.

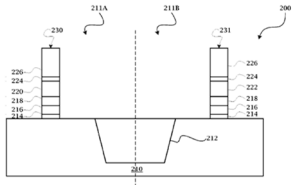
Ex-2026, 193:5-10 (Dr. Zhao) (annotated).

Pet. at 29-33; Reply, 22-24.

Ground 4: Usui-Yu-Sugimoto renders obvious claims 10 and 15



Usui, Fig. 8 (modified).



Yu, Fig. 2E.

ohmic

Sugimoto, 9:48-50.

Motivation to combine: Usui solves the problem of electromigration

Enhanced electromigration = reduced electromigration

Reply, 19, 22-23.

[57] **ABSTRACT**

A metallization structure is fabricated by depositing an underlayer of a group IVA metal having a thickness of about 90 to about 110 angstroms, and depositing a layer of aluminum and/or an aluminum alloy. The metallization structure obtained exhibits enhanced electromigration and is highly textured and is especially suitable for forming electrical connections or wiring.

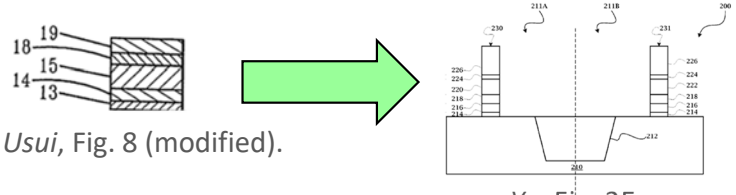
Usui, Abstract.

Patent Owner agrees POSAs would have sought "'improvement in the electromigration characteristics' of 'electrical connections and wiring' by reducing electromigration."	POR, 40 (citing Usui, 1:17-20, 2:33-39; Zhao-Dep., 13:23-14:9, 53:8-54:25; Piner, ¶219).
Usui discloses "forming various electrical connections or wiring in electronic devices such as in integrated circuit structures" and "an objective of the present invention is to provide a structure that exhibits enhanced electromigration performance."	Usui, 1:17-20, 2:33-39.
Dr. Zhao agrees that improving electromigration is reducing its negative effects.	Ex-2026, 13:23-14:9 (Dr. Zhao Deposition).

Pet. at 29-33; Reply, 19, 22-24.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 4: Usui-Yu-Sugimoto renders obvious claims 10 and 15



Usui, Fig. 8 (modified).

Yu, Fig. 2E.

ohmic

Sugimoto, 9:48-50.

Dr. Zhao explained the importance of ohmic contacts:

1. **Functionality**
2. **Performance**
3. **Long-term reliability**

Ex-1002, ¶55.

55. The interface between the metal and the semiconductor material can comprise either an ohmic contact or a Schottky contact, and both "ohmic and Schottky contacts" were known to be of "critical importance with respect to device functionality, performance, and long-term reliability" by the time of the alleged invention (August 25, 2009). Ex-1013, 144.

Ex-1002, ¶55 (Decl. of Dr. Zhao) (annotated).

Dr. Zhao explained the motivation for using an ohmic contact:

1. **Minimize power consumption**
2. **Minimize internal heating**
3. **Prolong device operation with predictable performance**

Ex-1002, ¶57.

material without distortion of the signal. Ex-1016, 22. The most critical component of an ohmic contact is low specific contact resistance, which minimizes the power consumption of the contact and the internal heating of the contact, thereby prolonging device operation with predictable performance. Ex-1016, 22. The

Ex-1002, ¶57 (Decl. of Dr. Zhao) (annotated); Ex-2026, 11:18-23.

Pet. at 29-33; Reply, 22-24.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 4: Usui-Yu-Sugimoto renders obvious claims 10 and 15

Innoscience

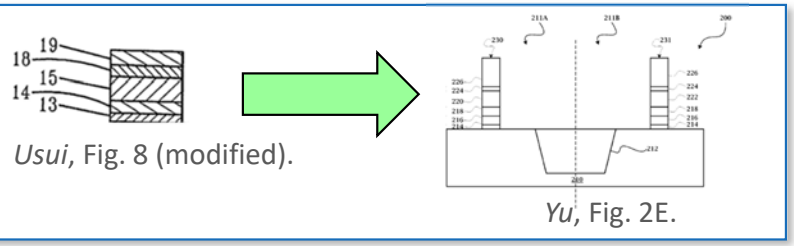
Patent Owner only disputes the motivation to combine Usui-Yu with Sugimoto for claims 10 and 15

✓ Motivation to combine Usui with secondary references (grounds 2-4)

Petition shows it would have been obvious to implement Usui-Yu's power electrode as an ohmic contact using the teachings of Sugimoto

Pet., 29-33; Reply, 22-24.

Usui-Yu-Sugimoto renders obvious claims 10 and 15



Usui, Fig. 8 (modified).

Yu, Fig. 2E.

ohmic

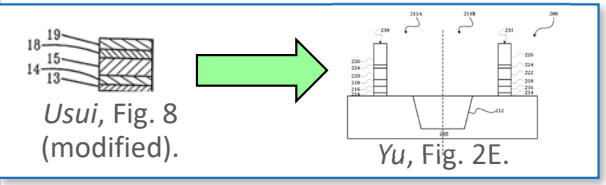
located between the two. The drain electrode **42** and the source electrode **46** make ohmic contact with the top surface of the AlGaN layer **34**. The SI-GaN layer **62** is essentially

Sugimoto, 9:48-50 (annotated).

Usui-Yu-Sugimoto	Limitation
✓	**[10]** The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.
✓	**[15]** The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.

Pet., 29-33; Reply, 22-24; '562 pat., Claims 10, 15.

Ground 4: Usui-Yu-Sugimoto renders obvious claims 10 and 15



Usui, Fig. 8 (modified).

Yu, Fig. 2E.

ohmic

Sugimoto, 9:48-50.

Usui-Yu-Sugimoto	Limitation
✓	**[10]** The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.
✓	**[15]** The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.

Petitioner has shown the claims are rendered obvious by Sugimoto

All of Patent Owner's Arguments Fail

Pet., 29-33; Reply, 22-24; '562 pat., Claims 10, 15.

Usui grounds: All claims invalid

Innoscience

Usui Grounds

Yu Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	**Usui**
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu
3	9, 11, 14, and 16	§ 103	**Usui**, Yu, and Adesida
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	Yu and Usui
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida
7	10 and 15	§ 103	Yu, Usui, and Sugimoto

All Claims Invalid

All Claims Invalid

All Claims Invalid

All Claims Invalid

Pet., 3.

Ground 5: Yu or Yu-Usui disclose claims 1-8, 12, 13, and 17

Innoscience

Usui Grounds

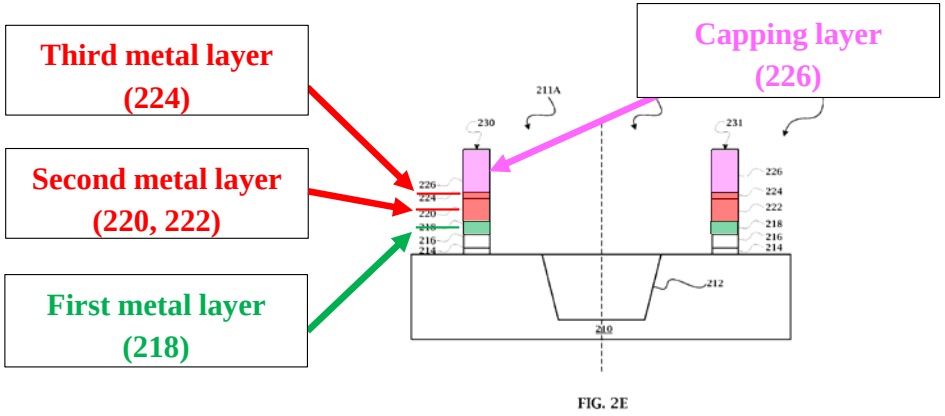
Yu Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	Usui
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu
3	9, 11, 14, and 16	§ 103	**Usui**, Yu, and Adesida
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	**Yu** and Usui
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida
7	10 and 15	§ 103	**Yu**, Usui, and Sugimoto

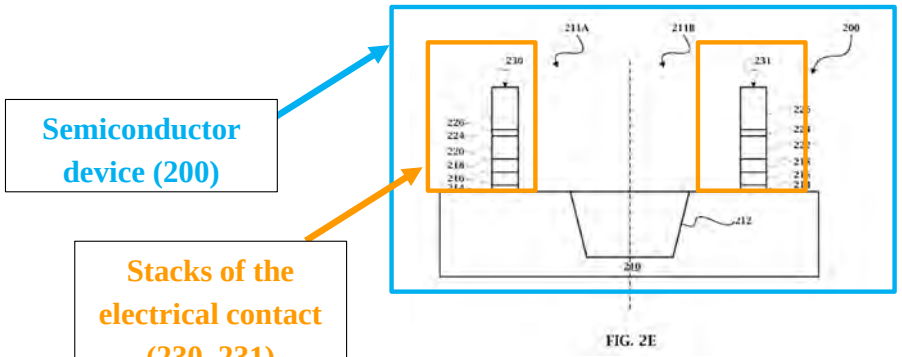
For Ground 5, the Board need only agree that Yu discloses a refractory metal nitride capping layer thicker than the bottommost layer.

Pet., 3.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17



Yu, Fig. 2E (annotated).



Yu, Fig. 2E (annotated).

Yu	Limitation	
✓	**[1p]** An **electrical contact** for use on a semiconductor device, said electrical contact comprising:	Undisputed
✓	**[1a]** an electrode stack including a plurality of **metal layers** and a **capping layer** formed over said plurality of metal layers;	Undisputed
✓	**[1b]** said **capping layer** consisting only of a refractory metal nitride,	Undisputed
✓	**[1c]** said **refractory metal nitride** forming a top of said **electrical contact** and having a thickness greater than that of a **bottommost layer** of said plurality of metal layers.	Disputed

Pet., 33-46; Reply, 24-28; '562 pat., Claim 1.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Patent Owner only disputes Yu shows *one* feature for claims 1 and 13

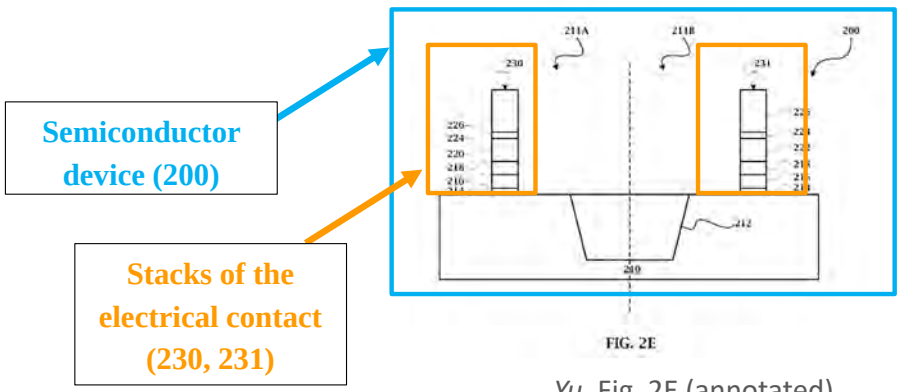
- ✓ [1c], [13c] said **refractory metal nitride / metal** … having a thickness greater than that of a **bottommost layer** of said plurality of metal layers (Yu grounds)

Yu expressly discloses a "refractory metal nitride … having a thickness greater than that of a bottommost layer of said plurality of metal layers"

Pet., 33-46, 54-55; Reply, 24-28; '562 pat., Claims 1, 13.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience



Yu, Fig. 2E (annotated).

Yu	Limitation
Undisputed ✓	**[1p]** An electrical contact for use on a semiconductor device, said electrical contact comprising:

Pet., 41; '562 pat., Claim 1.

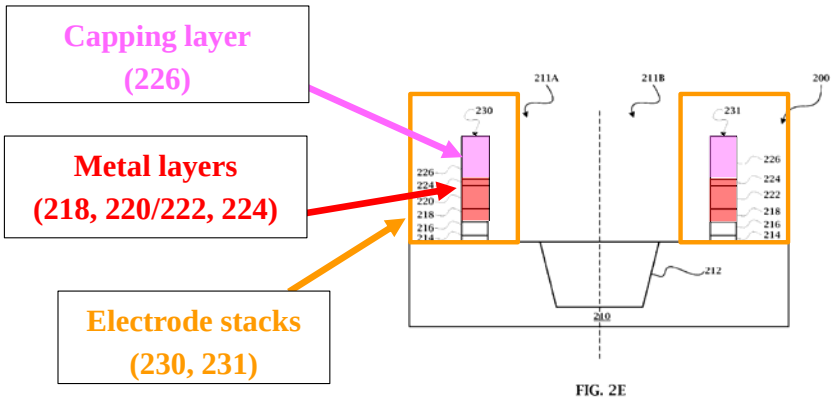
electrode), respectively. In still another example, various contacts/vias and multilayer interconnect features (e.g., metal layers and interlayer dielectrics) may be formed on the substrate **210** and configured to connect the various features or structures of the semiconductor device **200**.

Yu, ¶[0040] (annotated).

Pet., 33-46; Reply, 24-28.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience



Yu, Fig. 2E (annotated).

Yu	Limitation
Undisputed ✓	**[1a]** an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;

Pet., 42; '562 pat., Claim 1.

Electrode stack (230/231)

[0037] Referring to FIGS. **1** and **2**E, at step **112**, a first metal gate stack **230** with a first work function in the active/NMOS region **211**A and a second metal gate stack **231** with a second work function in the active/PMOS region **211**B are formed. In

Yu, ¶[0037] (annotated).

Capping layer (226)

[0036] At step **110**, referring to FIGS. **1** and **2**D, a capping layer **226** is formed over the metal layers **220**, **222**, and in the present embodiment, over the diffusion barrier layer **224**. The

Yu, ¶[0036] (annotated).

Metal layers (220/222, 224)

[0035] A diffusion barrier layer **224** may be formed over the semiconductor device **200**, particularly, metal layers **220**, **222** as illustrated in FIG. **2**D. The diffusion barrier layer may comprise titanium, titanium nitride, tantalum, tantalum nitride, other suitable material, and/or combinations thereof.

Yu, ¶[0035] (annotated).

Metal layer (218)

[0029] In some embodiments, a diffusion barrier/protection layer **218** is formed over the high-k dielectric layer **216**. The diffusion barrier/protection layer **218** may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present

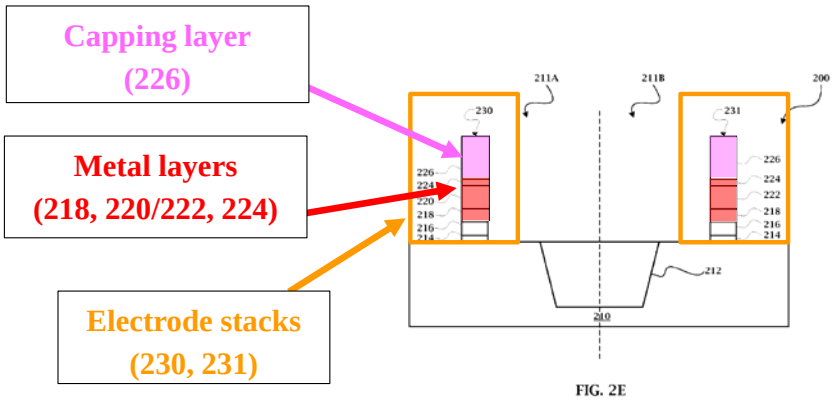
Yu, ¶[0029] (annotated).

The Petition shows:
✓ Yu discloses an "electrode stack" including a plurality of metal layers and a capping layer formed over the plurality of metal layers

Pet., 33-46; Reply, 24-28.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience



Yu, Fig. 2E (annotated).

Yu	Limitation
✓ Undisputed	**[1b]** said capping layer consisting only of a refractory metal nitride,

Pet., 42-43; '562 pat., Claim 1.

Capping layer (226)

present embodiment, over the diffusion barrier layer **224**. The capping layer **226** may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantulum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer **226**

Yu, ¶[0036] (annotated).

The Petition shows:

✓ **Yu discloses a capping layer consisting only of a refractory metal nitride (e.g., TiN, TaN)**

Pet., 33-46; Reply, 24-28.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Capping layer (226)

Bottommost layer (218)

Stacks of the electrical contacts (230, 231)

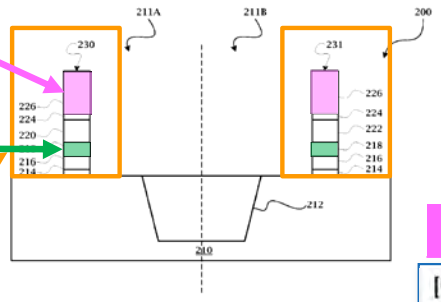
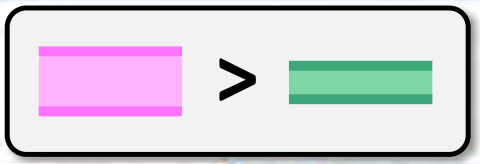


FIG. 2E

Yu, Fig. 2E (annotated).

Yu	Limitation
✓ Disputed	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

Pet., 43-46; Reply, 27-28; '562 pat., Claim 1.



Capping layer (226)

[0036] At step **110**, referring to FIGS. **1** and **2**D, a capping layer **226** is formed over the metal layers **220**, **222**, and in the present embodiment, over the diffusion barrier layer **224**. The capping layer **226** may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantulum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer **226** comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer **226** may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer **226** may comprise any suitable thickness. The capping layer **226** may

Yu, ¶[0036] (annotated).

Bottommost layer (218)

The diffusion barrier/protection layer **218** may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present embodiment, the diffusion barrier/protection layer **218** comprises TiN, which is deposited by PVD to a thickness of approximately 20 Å. In alternate embodiments, the diffusion barrier/protection layer may be formed by any suitable process, such as CVD, PVD, ALD, thermal oxide, plating, and/or combinations thereof. Further, in alternate embodiments, the diffusion barrier layer **218** comprises any suitable thickness.

Yu, ¶[0029] (annotated).

The Petition shows:

✓ **Yu discloses a refractory metal nitride capping layer forming a top of the electrical contact with a thickness greater than the bottommost layer**

Pet., 33-46; Reply, 24-28.

Capping layer metal (e.g., TiN, TaN) is 50-1000Å thick > **Bottommost layer: 20Å thick**

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Capping layer (226)

Bottommost layer (218)

Stacks of the electrical contacts (230, 231)

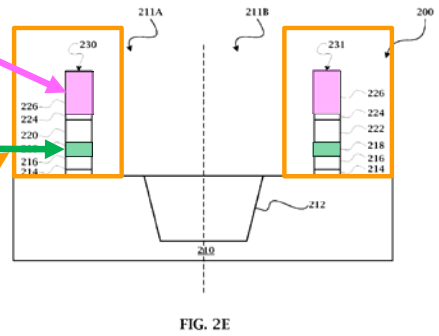


FIG. 2E

Yu, Fig. 2E (annotated).

Yu	Limitation
Disputed ✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

Pet., 42-43; Reply, 24-28; '562 pat., Claim 1.

Yu expressly discloses a refractory metal nitride capping layer thicker than a bottommost metal layer.

5A
The parties agree that Yu's metal gate stacks have the same arrangement of layers as the claimed "electrode stack". Pet., 33-46; Reply, 24-27.

5B
Paragraph 36 of Yu shows the obviousness of a refractory metal nitride capping layer being thicker than a bottommost metal layer. Pet., 33-46; Reply, 27-28.

Pet., 33-46; Reply, 24-28.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Capping layer (226)

Bottommost layer (218)

Stacks of the electrical contacts (230, 231)

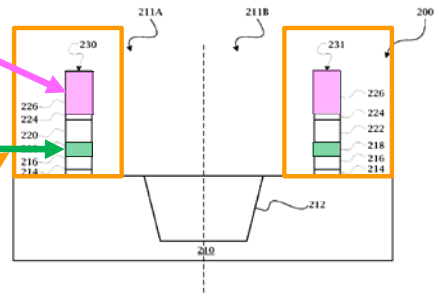


FIG. 2E

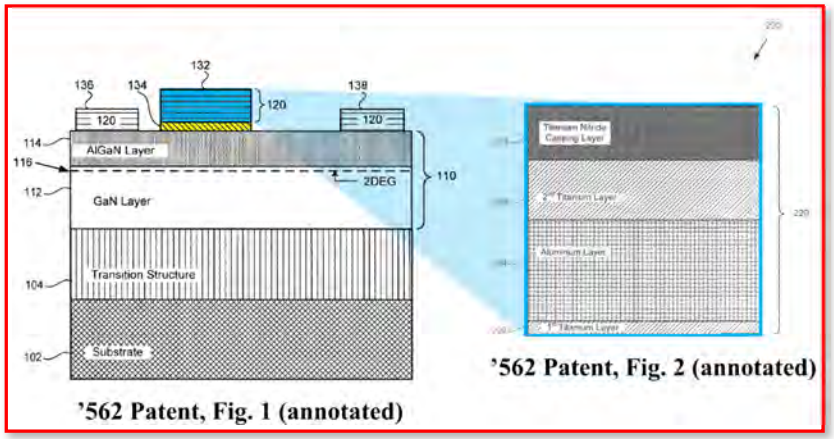
Yu, Fig. 2E (annotated); Pet., 44.

Yu	Limitation
Disputed ✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

Patent Owner highlights the similarities between Yu and the ’562 patent

Patent Owner agrees that Yu discloses the same insulated gate electrodes stacked above other layers as the ’562 patent

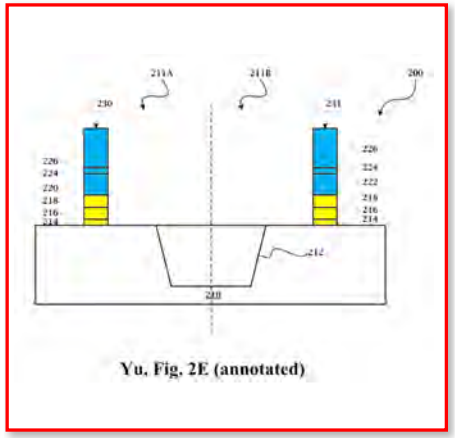
POR, 46.



’562 Patent, Fig. 1 (annotated)

’562 Patent, Fig. 2 (annotated)

POR, 46.



Yu, Fig. 2E (annotated)

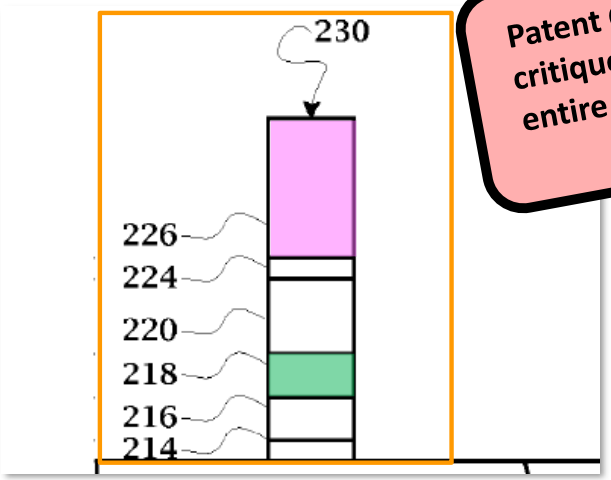
POR, 46.

5A

The parties agree that Yu’s metal gate stacks have the same arrangement of layers as the claimed “electrode stack”.

Pet., 33-46; Reply, 24-28; ’562 pat., Claim 1.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17



Yu, Fig. 2E (annotated); Pet., 44.

Patent Owner's semantic critique that "Yu calls the entire stack a 'metal gate stack,'" fails.

Reply, 24-26.

Disputed

Yu	Limitation
✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

Dr. Zhao clarified that he drew the box on 230, 231 of Yu to highlight its importance

Ex-1002, ¶165.

> A. I draw the yellow box on 230, 231 just to highlight this component of Yu as important. But then again, the analysis has been focusing on the metal layers, of this electrode stack, because metal layers

Ex-2026, 90:25-91:17 (annotated)

5A
The parties agree that Yu's metal gate stacks have the same arrangement of layers as the claimed "electrode stack".

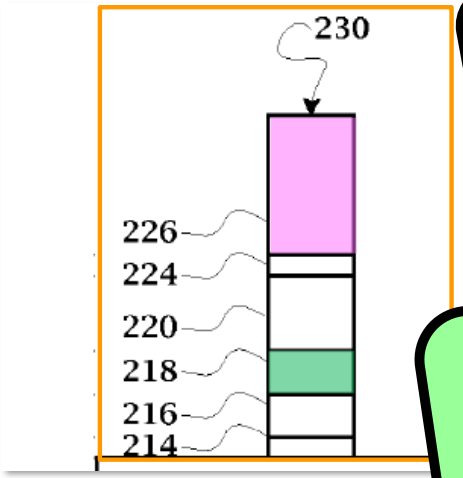
Pet., 33-46; Reply, 24-28; '562 pat., Claim 1.

- **Petition shows that Yu discloses the claimed electrode stack, including a bottommost metal layer 218**
- **Both Yu and the '562 patent show a stack of metal layers above dielectrics.**
- **The claims open-ended use of "including" does not preclude other structures in the stack.**

Pet., 43-46; Reply, 24-26.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience



Yu, Fig. 2E (annotated); Pet., 44.

Patent Owner's semantic critique that "Yu calls the entire stack a 'metal gate stack,'" fails.

Reply, 24-26.

Disputed

Yu's metal gate stack 230 includes layers 216 and 214, which the parties agree are dielectrics

Reply, 25.

Yu	Limitation
✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

'562 pat., Claim 1.

> Layer 214 and 216 cannot be the bottommost layer of the "plurality of **metal layers**" because they are dielectric layers not "metal layers." Layer 214 is an

Pet. at 44.

> with different work functions, but their structures are otherwise identical. Each stack includes two oxide layers 214, 216 (yellow above) atop the semiconductor

POR, 47.

5A
The parties agree that Yu's metal gate stacks have the same arrangement of layers as the claimed "electrode stack".

Pet., 33-46; Reply, 24-28.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Capping layer (226)

Metal layers (218, 220/222, 224)

Electrode stacks (230, 231)

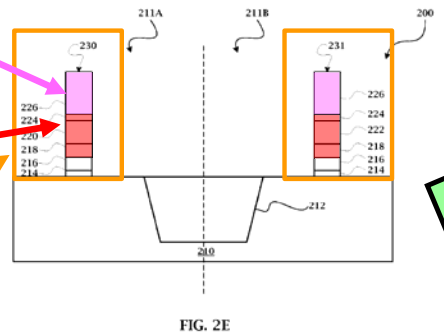


FIG. 2E

Yu, Fig. 2E (annotated); Pet., 42

Yu	Limitation
Disputed ✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

'562 pat., Claim 1.

Mapping of Yu in the Petition

Patent Owner's annotation of Yu is not the mapping in the Petition

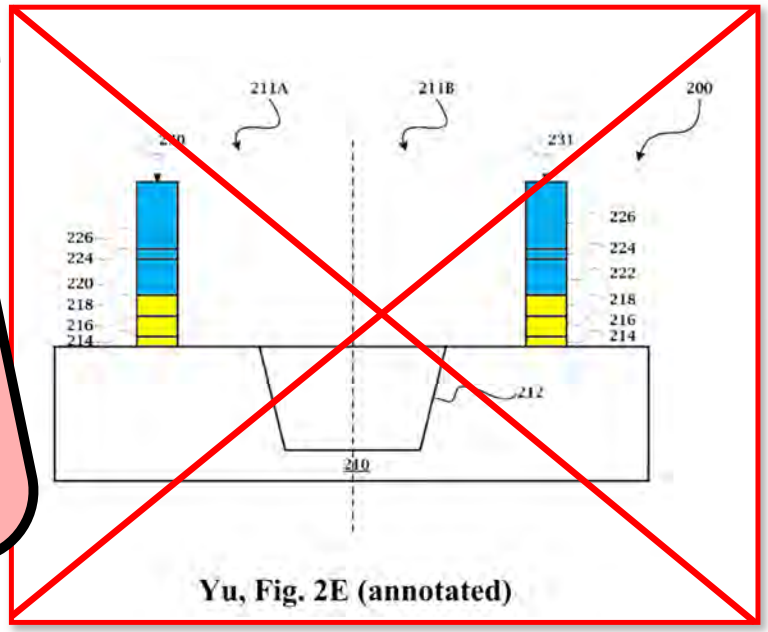
Reply, 24-26.

5A
The parties agree that Yu's metal gate stacks have the same arrangement of layers as the claimed "electrode stack".

Pet., 33-46; Reply, 24-28.

Patent Owner draws arbitrary boundaries to exclude metal layer 218 from the claimed "electrode stack" because it separates the other layers from the dielectrics

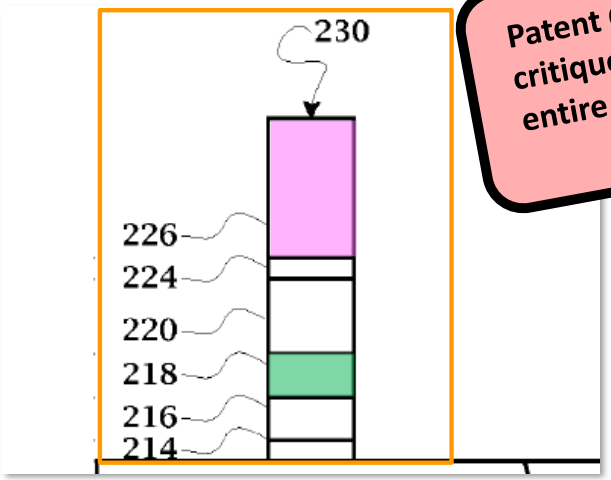
Reply, 24-26.



Yu, Fig. 2E (annotated)

POR, 46 (adding red X to Patent Owner's figure).

Ground 5: Yu discloses claims 1-8, 12, 13, and 17



Yu, Fig. 2E (annotated); Pet., 44.

Patent Owner's semantic critique that "Yu calls the entire stack a 'metal gate stack,'" fails.

Reply, 24-26.

Disputed

Yu	Limitation
✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

'562 pat., Claim 1.

"electrode stack" is open-ended in the claims – it does not exclude dielectrics

Reply, 26.

an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;

'562 pat., claim limitations [1a] and [13a] (annotated).

Patent Owner admits both Yu and the '562 patent show a stack of metal layers above dielectrics

Like the '562 Patent's insulated gate electrode (blue above) is stacked with another layer (yellow above), Yu's gate electrodes (blue below) are stacked with other layers (yellow below).

POR, 46.

5A
The parties agree that Yu's metal gate stacks have the same arrangement of layers as the claimed "electrode stack".

Pet., 33-46; Reply, 24-28.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Capping layer (226)

Bottommost layer (218)

Stacks of the electrical contacts (230, 231)

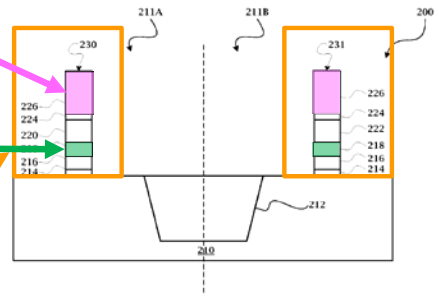


FIG. 2E

Yu, Fig. 2E (annotated); Pet., 44

Yu	Limitation
Disputed ✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

'562 pat., Claim 1.

oxide layer, like Yu's layer 218 does. *Id.* Yu's barrier layer is not part of the gate electrode; it separates the gate electrode from the oxide layer. *Id.*; Piner, ¶237.

POR, 48.

Patent Owner contradicts itself by contending that Yu calls the entire stack a metal gate stack and that Yu's barrier layer 218 is not part of the gate electrode

Yu calls the entire stack a "metal gate stack." Yu, [0038]-[0039]. Metal

POR, 47.

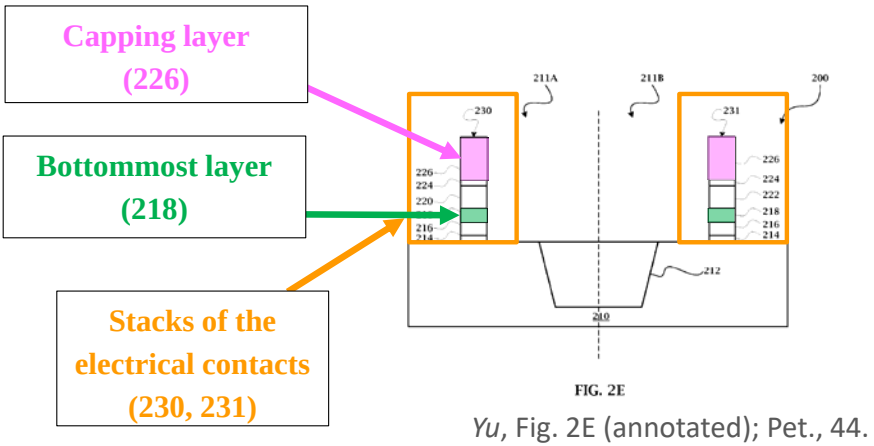
Reply, 27.

5A
The parties agree that Yu's metal gate stacks have the same arrangement of layers as the claimed "electrode stack".

Pet., 33-46; Reply, 24-28.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience



Yu, Fig. 2E (annotated); Pet., 44.

Patent Owner does not dispute that barrier layer 218 is a metal layer stacked with other metal layers

Reply, 27.

5A
The parties agree that Yu's metal gate stacks have the same arrangement of layers as the claimed "electrode stack".

Pet., 33-46; Reply, 24-28.

Yu	Limitation
Disputed ✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

'562 pat., Claim 1.

Yu expressly discloses layer 218 is a metal layer

[0029] In some embodiments, a diffusion barrier/protection layer **218** is formed over the high-k dielectric layer **216**. The diffusion barrier/protection layer **218** may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present

Yu, ¶[0029] (annotated).

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Capping layer (226)

Bottommost layer (218)

Stacks of the electrical contacts (230, 231)

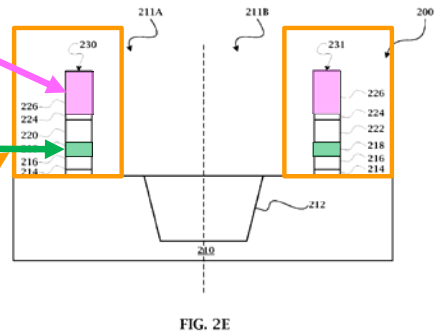


FIG. 2E

Yu, Fig. 2E (annotated).

Yu	Limitation
Disputed ✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

'562 pat., Claim 1.

Yu expressly discloses a refractory metal nitride capping layer thicker than a bottommost metal layer.

5A

The parties agree that Yu's metal gate stacks have the same arrangement of layers as the claimed "electrode stack". Pet., 33-46; Reply, 24-27.

5B

Paragraph 36 of Yu shows the obviousness of a refractory metal nitride capping layer being thicker than a bottommost metal layer. Pet., 33-46; Reply, 27-28.

Pet., 33-46; Reply, 24-28.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Capping layer (226)

Bottommost layer (218)

Stacks of the electrical contacts (230, 231)

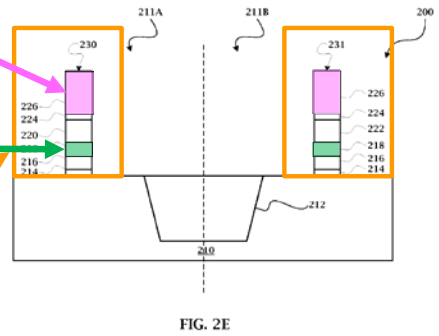


FIG. 2E

Yu, Fig. 2E (annotated).

Yu	Limitation
Disputed ✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

'562 Pat., Claim 1.

Yu expressly discloses a refractory metal nitride capping layer thicker than a bottommost metal layer.

5A

The parties agree that Yu's metal gate stacks have the same arrangement of layers as the claimed "electrode stack". Pet., 33-46; Reply, 24-27.

5B

Paragraph 36 of Yu shows the obviousness of a refractory metal nitride capping layer being thicker than a bottommost metal layer. Pet., 33-46; Reply, 27-28.

Pet., 33-46; Reply, 24-28.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Capping layer (226)

Bottommost layer (218)

Stacks of the electrical contacts (230, 231)

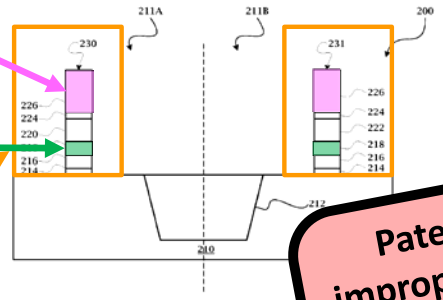


FIG. 2E

Yu, Fig. 2E (annotated).

Yu	Limitation
✓ Disputed	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers. '562 pat., Claim 1.

Yu discloses or at least rendered obvious a refractory metal nitride capping layer thicker than the bottommost metal layer

5B
Paragraph 36 of Yu shows the obviousness of a refractory metal nitride capping layer being thicker than a bottommost metal layer.

Pet., 33-46; Reply, 24-28.

Patent Owner improperly limits Yu to a polysilicon capping layer embodiment

Yu discloses a metal capping layer thickness 50-1000Å, which includes 600Å, thicker than the 20Å bottommost metal layer

Pet., 43-44; Reply, 27-28.

Yu's metals include TiN and TaN

Pet., 43-44; Reply, 28.

~~blue) that a POSA would have been motivated to "us[e] the same disclosed thickness" that Yu teaches for a polysilicon capping layer when making the capping layer from a refractory metal nitride is entirely unsupported. Petition, 38;~~

POR, 58 (annotated).

Capping layer (226)

[0036] At step **110**, referring to FIGS. **1** and **2**D, a capping layer **226** is formed over the metal layers **220**, **222**, and in the present embodiment, over the diffusion barrier layer **224**. The capping layer **226** may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer **226** comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer **226** may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer **226** may comprise any suitable thickness. The capping layer **226** may

Yu, ¶[0036] (annotated).

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Capping layer (226)

Bottommost layer (218)

Stacks of the electrical contacts (230, 231)

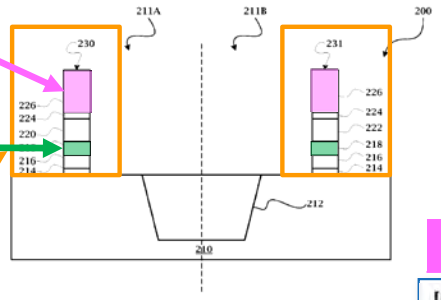


FIG. 2E

Yu, Fig. 2E (annotated).

Yu	Limitation
Disputed ✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

'562 pat., Claim 1.

Yu's rationale for replacing polysilicon capping layer with TiN or TaN at 600Å: Yu's metal based capping layer is thicker than the bottommost metal layer for entire range 50-1000Å

Reply, 27-28.

5B

Paragraph 36 of Yu shows the obviousness of a refractory metal nitride capping layer being thicker than a bottommost metal layer.

Pet., 33-46; Reply, 24-28.

Capping layer (226)

[0036] At step **110**, referring to FIGS. **1** and **2**D, a capping layer **226** is formed over the metal layers **220**, **222**, and in the present embodiment, over the diffusion barrier layer **224**. The capping layer **226** may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantulum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer **226** comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer **226** may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer **226** may comprise any suitable thickness. The capping layer **226** may

Yu, ¶[0036] (annotated).

Bottommost layer (218)

The diffusion barrier/protection layer **218** may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present embodiment, the diffusion barrier/protection layer **218** comprises TiN, which is deposited by PVD to a thickness of approximately 20 Å. In alternate embodiments, the diffusion barrier/protection layer may be formed by any suitable process, such as CVD, PVD, ALD, thermal oxide, plating, and/or combinations thereof. Further, in alternate embodiments, the diffusion barrier layer **218** comprises any suitable thickness.

Yu, ¶[0029] (annotated).

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Yu discloses the disputed element in a single embodiment: a metal capping layer (TiN or TaN) with a thickness between 50 Å and 1,000 Å, which includes 600 Å, which is thicker than the bottommost layer (20 Å)

No motivation to combine or modify is required.

Capping layer (226)

[0036] At step **110**, referring to FIGS. **1** and **2**D, a capping layer **226** is formed over the metal layers **220**, **222**, and in the present embodiment, over the diffusion barrier layer **224**. The capping layer **226** may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantulum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer **226** comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer **226** may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer **226** may comprise any suitable thickness. The capping layer **226** may

Yu, ¶[0036] (annotated).

Pet., 33-46; Reply 24-28.

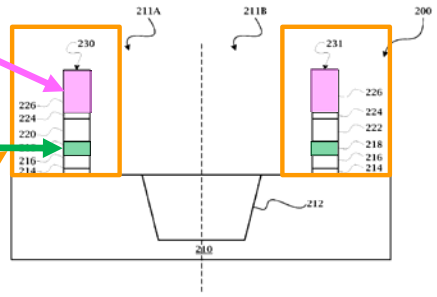
Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Capping layer (226)

Bottommost layer (218)

Stacks of the electrical contacts (230, 231)



Yu, Fig. 2E (annotated).

Yu	Limitation
Disputed ✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers. ’562 pat., Claim 1.

Petition looked to Usui to confirm relationship between capping layer and bottommost layer, already disclosed by Yu, was known and obvious

Usui confirms that a refractory metal nitride capping layer thicker than the bottommost layer was known and obvious

preferably a layer of titanium. Critical to the success of the present invention is having the thickness of this underlayer **13** being between about 90 angstroms to about 110 angstroms. As will be demonstrated hereinbelow, by limiting the thickness of this underlayer **13**, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention.

Usui, 3:29-33 (annotated).

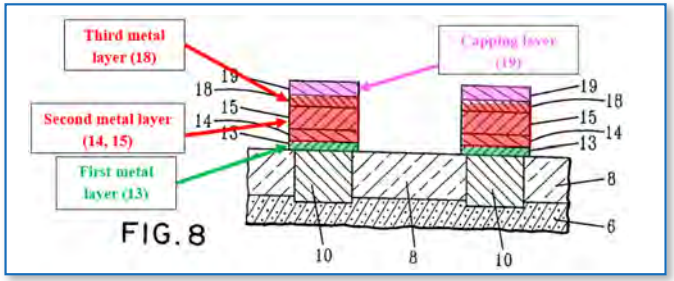
of a group IVA metal, preferably titanium with a titanium nitride layer **19**. Typically the titanium nitride layer is about 150 to about 800 angstroms and more typically about 200 to about 500 angstroms. Typically, the titanium layer is about

Usui, 4:5-8 (annotated).

5B

Paragraph 36 of Yu shows the obviousness of a refractory metal nitride capping layer being thicker than a bottommost metal layer.

Pet., 33-46; Reply, 24-28.



Usui, Fig. 8 (annotated).

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Capping layer (226)

Bottommost layer (218)

Stacks of the electrical contacts (230, 231)

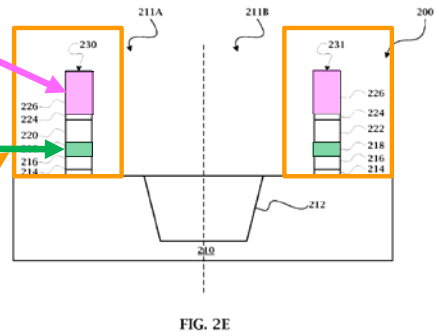


FIG. 2E

Yu, Fig. 2E (annotated).

Yu	Limitation
Disputed ✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

'562 pat., Claim 1.

Yu expressly discloses a refractory metal nitride capping layer thicker than a bottommost metal layer.

5A
The parties agree that Yu's metal gate stacks have the same arrangement of layers as the claimed "electrode stack". Pet., 33-46; Reply, 24-27.

5B
Paragraph 36 of Yu shows the obviousness of a refractory metal nitride capping layer being thicker than a bottommost metal layer. Pet., 33-46; Reply, 27-28.

Pet., 33-46; Reply, 24-28.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

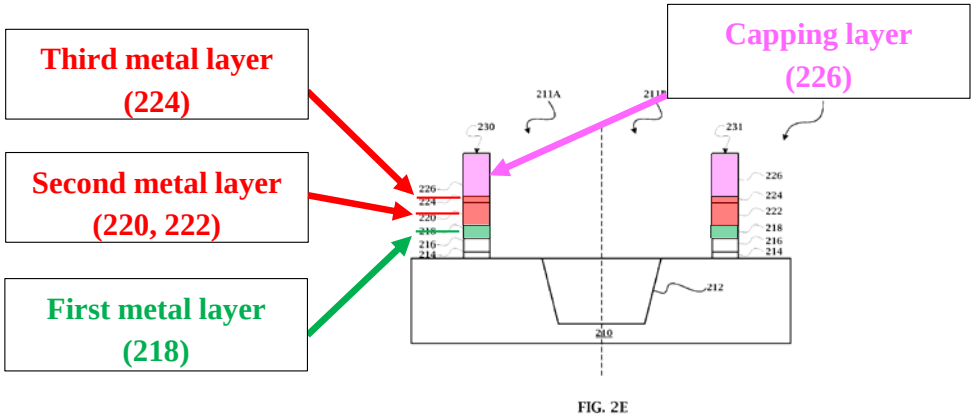
Patent Owner only disputes Yu shows *one* feature for claims 1 and 13

✓ [1c], [13c] said **refractory metal nitride / metal** … having a thickness greater than that of a **bottommost layer** of said plurality of metal layers (Yu grounds)

Yu expressly discloses a "refractory metal nitride … having a thickness greater than that of a bottommost layer of said plurality of metal layers"

Pet., 33-46, 54-55; Reply, 24-28; '562 pat., Claims 1, 13.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17



Yu, Fig. 2E (annotated).

The Petition shows:
✓ Yu discloses a capping layer comprising TiN or TaN

Pet., 46-48.

present embodiment, over the diffusion barrier layer **224**. The capping layer **226** may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantulum, titanium nitride, tantalum nitride, nickel silicide, cobalt

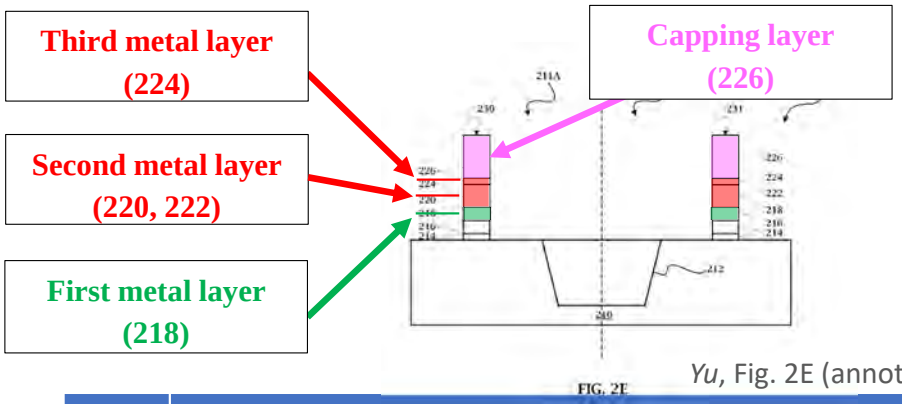
Yu, ¶[0036] (annotated).

Yu	Limitation
Undisputed ✓	**[2]** The electrical contact of claim 1, wherein said capping layer comprises titanium nitride (TiN).
Undisputed ✓	**[3]** The electrical contact of claim 1, wherein said capping layer comprises tantalum nitride (TaN).

Pet., 33-39, 46-48; '562 pat., Claims 2, 3.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience



Yu, Fig. 2E (annotated).

Yu	Limitation
Undisputed ✓	**[4]** The electrical contact of claim 1, wherein said plurality of **metal layers** includes respective **first**, **second (220,222)**, and **third (224)** metal layers, wherein said second metal layer is formed between said first metal layer and said third metal layer, and said **capping layer** is formed on said third metal layer.
Undisputed ✓	**[5]** The electrical contact of claim 4, wherein said **first metal layer** and said **third metal layer (224)** of said electrode stack comprise titanium (Ti).
Undisputed ✓	**[6]** The electrical contact of claim 4, wherein said **second metal layer (220,222)** of said electrode stack comprises aluminum (Al).
Undisputed ✓	**[7]** The electrical contact of claim 6, wherein said **second metal layer (220,222)** of said electrode stack further comprises silicon (Si).

Third metal layer (224)

[0035] A diffusion barrier layer **224** may be formed over the semiconductor device **200**, particularly, metal layers **220**, **222** as illustrated in FIG. **2**D. The diffusion barrier layer may comprise titanium, titanium nitride, tantalum, tantalum nitride, other suitable material, and/or combinations thereof.

Yu, ¶[0035] (annotated).

Second metal layer (220,222)

stability. Such improved work function values and thermal stability is achieved by the metal layers **220**, **222** comprising a doped-conducting metal oxide (DCO). The DCO may comprise SnO_2, In_2O_3, ZnO, CdO, and/or combinations thereof; SnO_2 doped with Sb, F, As, Nb, Ta, and/or combinations thereof; In_2O_3 doped with Zn, Ge, Mo, F, Ti, Zr, Hf, Nb, Ta, W, Te, Ga, Mg, Sn, and/or combinations thereof; ZnO doped with Al, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf, and/or combinations thereof; CdO doped with In, Sn, and/or com-

Yu, ¶[0033] (annotated).

First metal layer

The diffusion barrier/protection layer **218** may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present

Yu, ¶[0029] (annotated).

The Petition shows:
✓ **Yu discloses claimed arrangement and composition of metal layers and capping layer**

Pet., 33-37, 40-41, 48-53; '562 pat., Claims 4-7.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17

Innoscience

Group III-V semiconductor device (210)

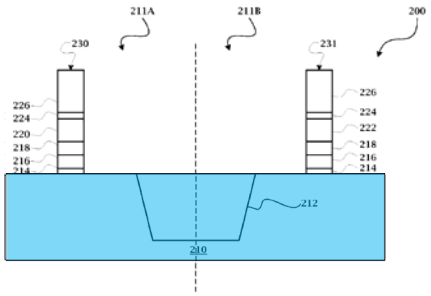


FIG. 2E

Yu, Fig. 2E (annotated).

The Petition shows:
✓ **Yu discloses an electrical contact configured for implementation on a group III-V semiconductor device**

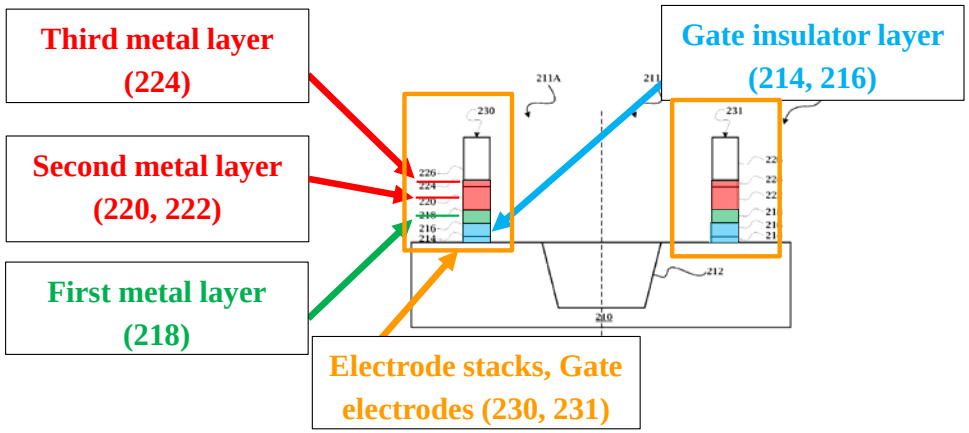
structure. In the present embodiment, the semiconductor substrate **210** comprises silicon, germanium, a group III-V material, or a group II-VI material.

Yu, ¶[0023] (annotated).

	Yu	Limitation
Undisputed	✓	**[8]** The electrical contact of claim 1, wherein said electrical contact is configured for implementation on a group III-V semiconductor device.
Undisputed	✓	**[13]** An electrical contact for use on a group III-V semiconductor device … [Yu discloses body of claim 13, as explained for claim 1].

Pet., 33-46, 53-55; '562 pat., Claims 8, 13.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17



Yu, Fig. 2E (annotated).

The Petition shows:

✓ **Yu discloses an electrical contact implemented with a gate insulator underlying the first metal layer to provide an insulated gate electrode**

the underlying layers (i.e., the interfacial dielectric layer **214**, the high-k dielectric layer **216**, the diffusion barrier/protec-

Yu, ¶[0039] (annotated).

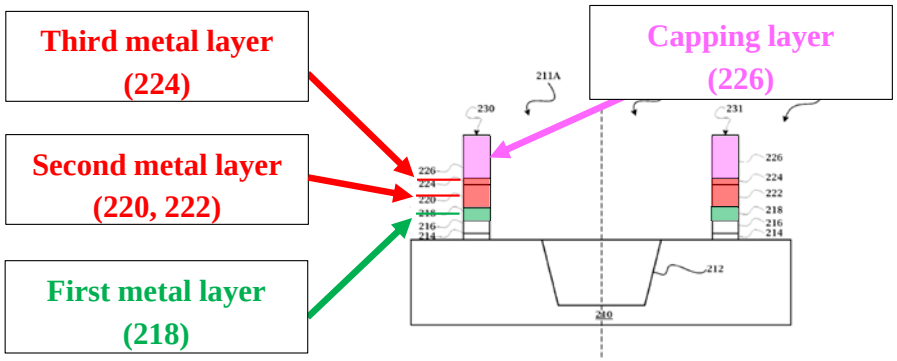
The diffusion barrier/protection layer **218** may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present

Yu, ¶[0029] (annotated).

Yu	Limitation
Undisputed ✓	**[12]** The electrical contact of claim 8, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.
Undisputed ✓	**[17]** The electrical contact of claim 13, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

Pet., 33-37, 53-55; '562 pat., Claims 12, 17.

Ground 5: Yu discloses claims 1-8, 12, 13, and 17



Yu, Fig. 2E (annotated). FIG. 2E

Petitioner has shown the claims are disclosed by Yu or Yu-Usui

All of Patent Owner's Arguments Fail

Pet., 33-55; Reply, 24-28; '562 pat., Claims 1-8, 12, 13, 17.

Yu	Limitation
✓	**[1p]** An electrical contact for use on a semiconductor device, said electrical contact comprising:
✓	**[1a]** an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;
✓	**[1b]** said capping layer consisting only of a refractory metal nitride,
✓	**[1c]** said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.
✓	**[2]** The electrical contact of claim 1, wherein said capping layer comprises titanium nitride (TiN).
✓	**[3]** The electrical contact of claim 1, wherein said capping layer comprises tantalum nitride (TaN).
✓	**[4]** The electrical contact of claim 1, wherein said plurality of metal layers includes respective first, second (220,222), and third (224) metal layers, wherein said second metal layer is formed between said first metal layer and said third metal layer, and said capping layer is formed on said third metal layer.
✓	**[5]** The electrical contact of claim 4, wherein said first metal layer and said third metal layer (224) of said electrode stack comprise titanium (Ti).
✓	**[6]** The electrical contact of claim 4, wherein said second metal layer (220,222) of said electrode stack comprises aluminum (Al).
✓	**[7]** The electrical contact of claim 6, wherein said second metal layer (220,222) of said electrode stack further comprises silicon (Si).
✓	**[8]** The electrical contact of claim 1, wherein said electrical contact is configured for implementation on a group III-V semiconductor device.
✓	**[12]** The electrical contact of claim 8, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.
✓	**[13]** An electrical contact for use on a group III-V semiconductor device … [Yu discloses body of claim 13, as explained for claim 1]
✓	**[17]** The electrical contact of claim 13, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

Ground 6: Yu-Usui-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience

Usui Grounds

Yu Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	Usui
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu
3	9, 11, 14, and 16	§ 103	Usui, Yu, and Adesida
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	Yu and Usui
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida
7	10 and 15	§ 103	Yu, Usui, and Sugimoto

To find claims 9, 11, 14, and 16 invalid over Yu, Usui, and Adesida (Ground 6), the Board need only agree that implementing Yu-Usui's contact as a Schottky contact in a HEMT using the teachings of Adesida would have been obvious.

Pet., 3.

Ground 6: Yu-Usui-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience

Yu-Usui

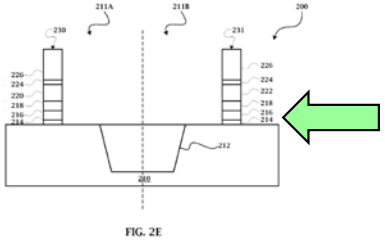


FIG. 2E

Yu, Fig. 2E.

Metal layers

preferably a layer of titanium. Critical to the success of the present invention is having the thickness of this underlayer **13** being between about 90 angstroms to about 110 angstroms. As will be demonstrated hereinbelow, by limiting the thickness of this underlayer **13**, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention.

Usui, 3:29-37 (annotated).

of a group IVA metal, preferably titanium with a titanium nitride layer **19**. Typically the titanium nitride layer is about 150 to about 800 angstroms and more typically about 200 to about 500 angstroms. Typically, the titanium layer is about

Usui, 4:5-8 (annotated).

Adesida's teachings

HEMT

invention. The device of FIG. **5** is a high electron mobility transistor (HEMT), which, in this example, is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate **105** (therefore commonly called an InP HEMT or GaAs metamorphic HEMT) on which is deposited

Schottky

$In_{0.53}Ga_{0.47}As$ cap layer **160**. Spaced apart source **170** and drain **180** ohmic contacts are formed on the n+ $In_{0.53}Ga_{0.47}As$ cap layer **160**, and the gate **190**, which is shown as a T-gate in this example, is formed with a Schottky barrier contact of length L_g on the $In_{0.52}Al_{0.48}As$ barrier layer **150**.

Adesida, ¶[0031] (annotated).

Motivation to Combine (MTC) Disputed

Pet., 37-39, 45-46, 55-61; Reply, 28-29; '562 pat., Claims 9, 11, 14, 16.

Yu-Usui-Adesida	Limitation
✓	**[9]** The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a **high electron mobility transistor (HEMT)**.
✓	**[11]** The electrical contact of claim 8, wherein said electrical contact is implemented as a **gate electrode making Schottky contact** with said group III-V semiconductor device.
✓	**[14]** The electrical contact of claim 13, wherein said group III-V semiconductor device comprises a **high electron mobility transistor (HEMT)**.
✓	**[16]** The electrical contact of claim 13, wherein said electrical contact is implemented as a **gate electrode making Schottky contact** with said group III-V semiconductor device.

Ground 6: Yu-Usui-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience

Patent Owner only disputes the motivation to combine Yu-Usui with Adesida for claims 9, 11, 14, and 16

✓ Motivation to combine Yu with secondary references (grounds 6-7)

Petition shows it would have been obvious to implement Yu-Usui's contact as a Schottky contact in a HEMT using the teachings of Adesida

Pet., 55-61; Reply, 28-29.

Ground 6: Yu-Usui-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience

Patent Owner wrongly contends that Petitioner never modified Yu's gate electrode to make Schottky contact

Finally, to the extent Petitioner alleges in Reply that the structure of the gate electrode in Yu-Usui-Adesida is ***Yu's*** gate electrode but modified to make Schottky contact, that would fail because the Petition ***never alleges this*** and cites ***no evidence*** in support. Piner, ¶¶283-286. Yu discloses a CMOS device with "a

POR, 71 (annotated).

Yu in view of Usui and Adesida renders obvious claim 9 because Adesida discloses a HEMT, and it would have been obvious to implement Yu-Usui's group III-V semiconductor devices as HEMTs (explained in VII.F.1, VII.F.1.a). Zhao ¶¶51-54, 194.

Pet., 59 (annotated).

Yu in view of Usui and Adesida renders obvious claim 11 because Adesida discloses a group III-V device with a gate electrode making a Schottky contact with the group III-V device, and it would have been obvious to implement Yu or Yu-Usui's group III-V semiconductor devices with gate electrodes making Schottky contacts (explained in Sections VII.F.1, VII.F.1.b). Zhao ¶¶48-55, 58-61,

Pet., 55-61; Reply, 28-29.

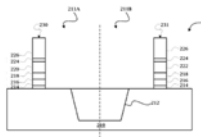
Pet., 59-60 (annotated).

Petition's combination

Dr. Zhao confirmed the combination in his deposition

Petitioner's real combination: Yu-Usui's contact as a Schottky contact in a HEMT using the teachings of Adesida

Yu-Usui



Yu, Fig. 2E.

Metal layers

Usui, 3:29-37, 4:5-8.

Adesida's teachings

HEMT

Schottky

Adesida, ¶[0031].

A. So here we are having a III-V HEMT devices with the metal layers from Usui and Yu as the Schottky gate contact, or Schottky gate electrode on these III-V HEMT device.

Ex-2026, 196:25-197:3.

Ground 6: Yu-Usui-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience

Petition's combination

discloses a HEMT, and it would have been obvious to implement Yu-Usui's group III-V semiconductor devices as HEMTs (explained in VII.F.1, VII.F.1.a). Zhao

Pet., 59.

with the group III-V device, and it would have been obvious to implement Yu or Yu-Usui's group III-V semiconductor devices with gate electrodes making Schottky contacts (explained in Sections VII.F.1, VII.F.1.b). Zhao ¶¶48-55, 58-61,

Pet., 60.

Q. (BY MS. RODRIGUEZ) What is the resulting device of the combination of Yu -- sorry, Yu, Usui and Adesida you have described for claims 9 and 14?

A. A result a HEMT device with the metal layers taught by Yu and Usui as the gate.

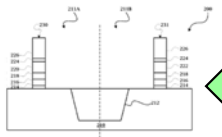
Ex-2026, 195:21-25.

A. So Adesida's material is III-V materials, they will be used, the base materials, semiconductors for the HEMT structure, HEMT device.

Ex-2026, 196:5-7.

Petitioner's real combination: Yu-Usui's contact as a Schottky contact in a HEMT using the teachings of Adesida

Yu-Usui



Yu, Fig. 2E.

Metal layers

Usui, 3:29-37, 4:5-8.

Adesida's teachings

HEMT

Schottky

Adesida, ¶[0031].

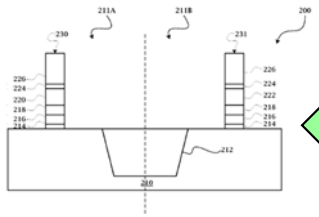
Dr. Zhao confirmed the combination

A. So here we are having a III-V HEMT devices with the metal layers from Usui and Yu as the Schottky gate contact, or Schottky gate electrode on these III-V HEMT device.

Ex-2026, 196:25-197:3.

Pet., 55-61; Reply, 28-29.

Ground 6: Yu-Usui-Adesida renders obvious claims 9, 11, 14, and 16



Yu, Fig. 2E.

Metal layers

Usui, 3:29-37, 4:5-8.

HEMT

Schottky

Adesida, ¶[0031].

¶55 (citing Ex-1013, 144). It was well-known that Schottky contacts serve as gate contacts in group III-V devices, have a fast response for many applications due to their unipolar carrier transport, and have excellent rectifying properties, which make them suitable for high frequency applications. Zhao ¶¶58-59, 192 (citing Ex-1011, 219; Ex-1017, 1, 87).

Pet., 58 (annotated).

✓ **Motivation from petition**

Pet., 55-61.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 6: Yu-Usui-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience

Patent Owner only disputes the motivation to combine Yu-Usui with Adesida for claims 9, 11, 14, and 16

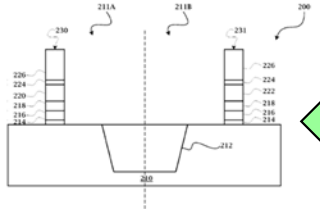
Petition shows it would have been obvious to implement Yu-Usui's contact as a Schottky contact in a HEMT using the teachings of Adesida

✓ Motivation to combine Yu with secondary references (grounds 6-7)

Pet., 55-61; Reply, 28-29.

Innoscience

Yu-Usui-Adesida renders obvious claims 9 and 14



Yu, Fig. 2E.

Metal layers

Usui, 3:29-37, 4:5-8.

HEMT

Schottky

Adesida, ¶[0031].

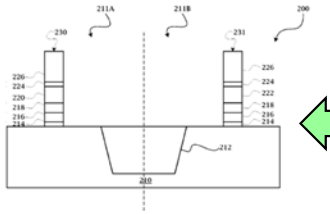
invention. The device of FIG. **5** is a high electron mobility transistor (HEMT), which, in this example, is a field-effect HEMT formed on an indium phosphide substrate or gallium arsenide substrate **105** (therefore commonly called an InP HEMT or GaAs metamorphic HEMT) on which is deposited

Adesida, ¶[0031] (annotated).

Yu-Usui-Adesida	Limitation
✓	**[9]** The electrical contact of claim 8, wherein said **group III-V semiconductor device** comprises a **high electron mobility transistor (HEMT)**.
✓	**[14]** The electrical contact of claim 13, wherein said **group III-V semiconductor device** comprises a **high electron mobility transistor (HEMT)**.

Pet., 55-61; Reply, 28-29; '562 pat., Claims 9, 14.

Yu-Usui-Adesida renders obvious claims 11 and 16



Yu, Fig. 2E.

Metal layers

Usui, 3:29-37, 4:5-8.

HEMT

Schottky

Adesida, ¶[0031].

$In_{0.53}Ga_{0.47}As$ cap layer **160**. Spaced apart source **170** and drain **180** ohmic contacts are formed on the n+ $In_{0.53}Ga_{0.47}As$ cap layer **160**, and the gate **190**, which is shown as a T-gate in this example, is formed with a Schottky barrier contact of length L_g on the $In_{0.52}Al_{0.48}As$ barrier layer **150**.

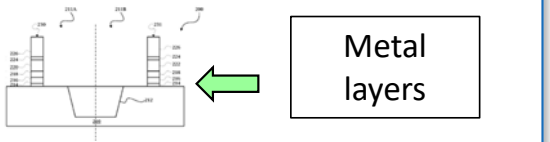
Adesida, ¶[0031] (annotated).

Yu-Usui-Adesida	Limitation
✓	**[11]** The electrical contact of claim 8, wherein said electrical contact is implemented as a **gate electrode making Schottky contact** with said **group III-V semiconductor device**.
✓	**[16]** The electrical contact of claim 13, wherein said electrical contact is implemented as a **gate electrode making Schottky contact** with said **group III-V semiconductor device**.

Pet., 55-61; Reply, 28-29; '562 pat., Claims 11, 16.

Ground 6: Yu-Usui-Adesida renders obvious claims 9, 11, 14, and 16

Innoscience



Yu, Fig. 2E. *Usui*, 3:29-37, 4:5-8.

HEMT

Schottky

Adesida, ¶[0031].

Petitioner has shown the claims are rendered obvious by Yu-Usui-Adesida

All of Patent Owner's Arguments Fail

Yu-Usui-Adesida	Limitation
✓	**[9]** The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a **high electron mobility transistor (HEMT)**.
✓	**[11]** The electrical contact of claim 8, wherein said electrical contact is implemented as a **gate electrode making Schottky contact** with said group III-V semiconductor device.
✓	**[14]** The electrical contact of claim 13, wherein said group III-V semiconductor device comprises a **high electron mobility transistor (HEMT)**.
✓	**[16]** The electrical contact of claim 13, wherein said electrical contact is implemented as a **gate electrode making Schottky contact** with said group III-V semiconductor device.

Pet., 55-61; Reply, 28-29;
'562 pat., Claims 9, 11, 14, 16.

Ground 7: Yu-Usui-Sugimoto renders obvious claims 10 and 15

Innoscience

Usui Grounds

Yu Grounds

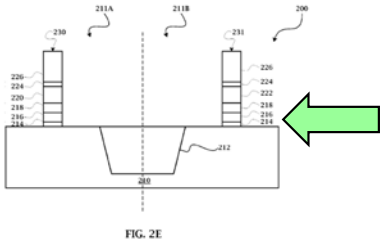
Ground	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	Usui
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu
3	9, 11, 14, and 16	§ 103	POR, 73. Usui, Yu, and Adesida
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	Yu and Usui
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida
7	10 and 15	§ 103	**Yu**, Usui, and Sugimoto

For Ground 7, the Board need only agree that it would have been obvious to make one change to Yu-Usui's power electrode:
Mae ohmic contact following Sugimoto.

Pet., 3.

Ground 7: Yu-Usui-Sugimoto renders obvious claims 10 and 15

Yu-Usui's power electrode



Yu, Fig. 2E.

Metal layers

preferably a layer of titanium. Critical to the success of the present invention is having the thickness of this underlayer **13** being between about 90 angstroms to about 110 angstroms. As will be demonstrated hereinbelow, by limiting the thickness of this underlayer **13**, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention.

Usui, 3:29-37 (annotated).

of a group IVA metal, preferably titanium with a titanium nitride layer **19**. Typically the titanium nitride layer is about 150 to about 800 angstroms and more typically about 200 to about 500 angstroms. Typically, the titanium layer is about

Usui, 4:5-8 (annotated).

Sugimoto's teachings of ohmic contact

ohmic

located between the two. The drain electrode **42** and the source electrode **46** make ohmic contact with the top surface of the AlGaN layer **34**. The SI-GaN layer **62** is essentially

Sugimoto, 9:48-50 (annotated).

Motivation to Combine (MTC) Disputed

Yu-Usui-Sugimoto	Limitation
✓	**[10]** The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.
✓	**[15]** The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.

Pet., 62-64; Reply, 29; '562 pat., Claims 10, 15.

Ground 7: Yu-Usui-Sugimoto renders obvious claims 10 and 15

Patent Owner only disputes the motivation to combine Yu-Usui with Sugimoto for claims 10 and 15

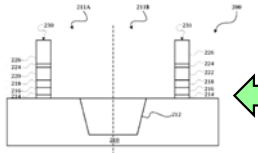
✓ Motivation to combine Yu with secondary references (grounds 6-7)

Petition shows it would have been obvious to implement Yu-Usui contact as an ohmic contact using the teachings of Sugimoto

Pet., 62-64; Reply, 29.

Ground 7: Patent Owner invents their own combination of Yu, Usui, and Sugimoto

Yu-Usui's power electrode



Metal layers

Yu, Fig. 2E. *Usui*, 3:29-37, 4:5-8.

Sugimoto's teachings of ohmic contact

ohmic

located between the two. The drain electrode **42** and the source electrode **46** make ohmic contact with the top surface of the AlGaN layer **34**. The SI-GaN layer **62** is essentially

Sugimoto, 9:48-50 (annotated).

Patent Owner does not dispute obviousness of Yu as an ohmic contact

Infineon does not dispute it would have been obvious to implement Yu's CMOS device to have source and drain electrodes that are power electrodes making ohmic contact.

POR, 73 (annotated).

Petitioner showed:

1. Yu discloses an electrical contact in group III-V device; Usui confirms obviousness of capping layer and bottommost layer thicknesses.
   (Ground 5, claims 1, 8, and 13)

2. It would have been obvious to make Yu-Usui's power electrode make ohmic contact following Sugimoto.
   (Ground 7, claims 10 and 15)

Pet., 33-39, 41-46, 53-55, 62-64.

Pet., 62-64; Reply, 29.

Ground 7: Patent Owner invents their own combination of Yu, Usui, and Sugimoto

Innoscience

Patent Owner's made-up combination:

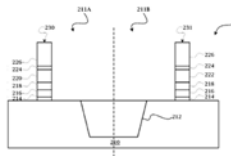
Petitioner alleges that ohmic contacts were known to "serve as ***source and drain*** contacts in group III-V devices and allow current to flow into and out of a semiconductor material." Petition, 62-63. Current flow in and out of the semiconductor does not occur through Yu's ***gate*** electrodes; thus, even if a

POR, 74 (annotated).

- ✓ **Patent Owner's arguments are non-responsive because they address the wrong combination.**

Reply, 29.

Petitioner's real combination: Yu-Usui's power electrode + Sugimoto's ohmic teaching



Yu, Fig. 2E

Metal layers

Usui, 3:29-37, 4:5-8

+

ohmic

Sugimoto, 9:48-50.

stability. Yu, Abstract. A POSITA would have been motivated to implement the devices of Yu and Yu-Usui with a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide reduced internal

Pet., 63.

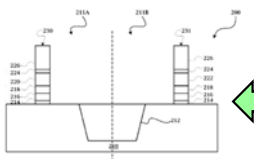
Dr. Zhao confirmed the combination

A. -- the resulting device is group III-V semiconductor device with aluminum and nitrite top layer. So III-V nitride HEMT device with the metal layer from Usui as the power electrode here, which is source and drain, and this metal layer is ohmic contact for the source and drain.

Ex-2026, 198:3-8.

Pet., 62-64; Reply, 29.

Ground 7: Patent Owner invents their own combination of Yu, Usui, and Sugimoto



Yu, Fig. 2E.

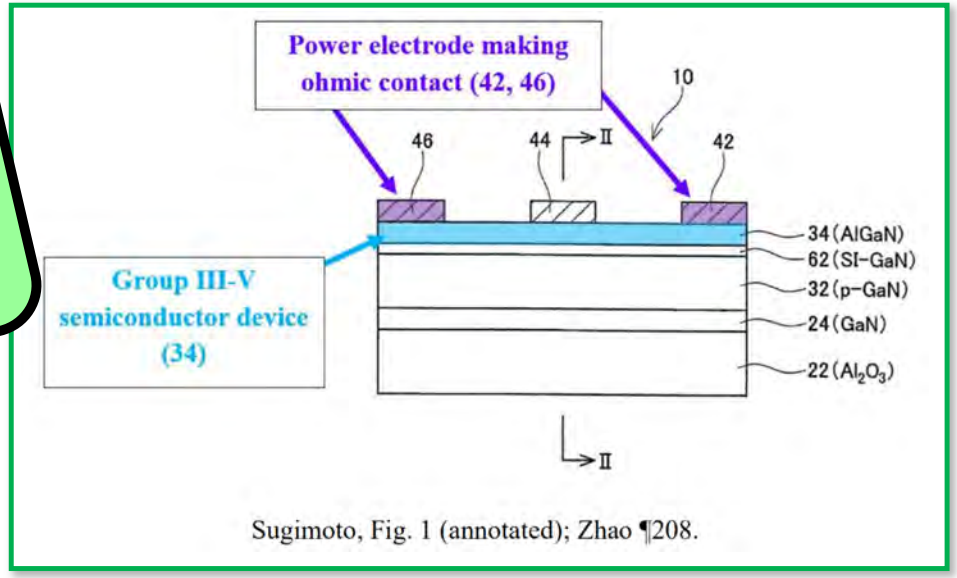
Metal layers

Usui, 3:29-37, 4:5-8.

ohmic

Sugimoto, 9:48-50.

Petition showed Sugimoto's teachings of ohmic contact

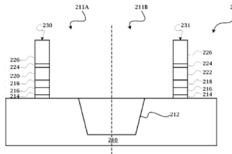


Sugimoto, Fig. 1 (annotated); Zhao ¶208.

Pet., 64.

Pet., 62-64; Reply, 29.

Ground 7: Yu-Usui-Sugimoto renders obvious claims 10 and 15



Yu, Fig. 2E.

Metal layers

Usui, 3:29-37, 4:5-8.

ohmic

Sugimoto, 9:48-50.

Dr. Zhao explained the importance of ohmic contacts:

1. **Functionality**
2. **Performance**
3. **Long-term reliability**

Ex-1002, ¶55.

55. The interface between the metal and the semiconductor material can comprise either an ohmic contact or a Schottky contact, and both "ohmic and Schottky contacts" were known to be of "critical importance with respect to device functionality, performance, and long-term reliability" by the time of the alleged invention (August 25, 2009). Ex-1013, 144.

Ex-1002, ¶55 (Decl. of Dr. Zhao) (annotated).

Dr. Zhao explained the motivation for using an ohmic contact:

1. **Minimize power consumption**
2. **Minimize internal heating**
3. **Prolong device operation with predictable performance**

Ex-1002, ¶57.

material without distortion of the signal. Ex-1016, 22. The most critical component of an ohmic contact is low specific contact resistance, which minimizes the power consumption of the contact and the internal heating of the contact, thereby prolonging device operation with predictable performance. Ex-1016, 22. The

Ex-1002, ¶57 (Decl. of Dr. Zhao) (annotated); Ex-2026, 11:18-23.

Pet., 62-64; Reply, 29.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 7: Yu-Usui-Sugimoto renders obvious claims 10 and 15

Innoscience

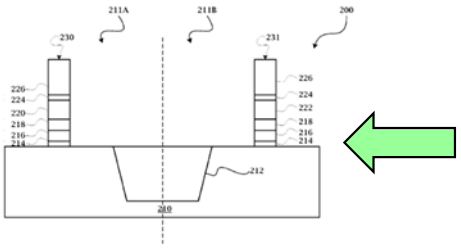
Patent Owner only disputes the motivation to combine Yu-Usui with Sugimoto for claims 10 and 15

✓ Motivation to combine Yu with secondary references (grounds 6-7)

Petition shows it would have been obvious to implement Yu-Usui contact as an ohmic contact using the teachings of Sugimoto

Pet., 62-64; Reply, 29.

Yu-Usui-Sugimoto renders obvious claims 10 and 15



Yu, Fig. 2E.

Metal layers

Usui, 3:29-37, 4:5-8.

ohmic

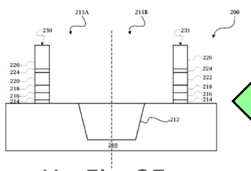
located between the two. The drain electrode **42** and the source electrode **46** make ohmic contact with the top surface of the AlGaN layer **34**. The SI-GaN layer **62** is essentially

Sugimoto, 9:48-50 (annotated).

Yu-Usui-Sugimoto	Limitation
✓	**[10]** The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.
✓	**[15]** The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.

Pet., 62-64; Reply, 29;
'562 pat., Claims 10, 15.

Ground 7: Yu-Usui-Sugimoto renders obvious claims 10 and 15



Yu, Fig. 2E.

Metal layers

Usui, 3:29-37, 4:5-8.

ohmic

Yu-Usui-Sugimoto	Limitation
✓	**[10]** The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.
✓	**[15]** The electrical contact of claim 13, wherein said electrical contact is implemented as a power electrode making **ohmic contact** with said group III-V semiconductor device.

Petitioner has shown the claims are rendered obvious by Yu-Usui-Sugimoto

All of Patent Owner's Arguments Fail

Pet., 62-64; Reply, 29; '562 pat., Claims 10, 15.

Yu grounds: All claims invalid

Innoscience

Usui Grounds

Yu Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, and 4-7	§ 102	Usui
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu
3	9, 11, 14, and 16	§ 103	Usui, Yu, and Adesida
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto
5	1-8, 12, 13, and 17	§ 103	**Yu** and Usui
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida
7	10 and 15	§ 103	**Yu**, Usui, and Sugimoto

All Claims Invalid

All Claims Invalid

All Claims Invalid

Pet., 3.

Summary

All claims invalid

Innoscience

Usui Grounds

Yu Grounds

Ground	Challenged Claims	Basis	Prior Art	
1	1, 2, and 4-7	§ 102	**Usui**	All Claims Invalid
2	3, 8, 12, 13, and 17	§ 103	**Usui** and Yu	All Claims Invalid
3	9, 11, 14, and 16	§ 103	**Usui**, Yu, and Adesida	All Claims Invalid
4	10 and 15	§ 103	**Usui**, Yu, and Sugimoto	All Claims Invalid
5	1-8, 12, 13, and 17	§ 103	**Yu** and Usui	All Claims Invalid
6	9, 11, 14, and 16	§ 103	**Yu**, Usui, and Adesida	All Claims Invalid
7	10 and 15	§ 103	**Yu**, Usui, and Sugimoto	All Claims Invalid

Pet., 3.

Unrebutted Arguments

Innoscience

Petitioner's Argument:	
Patent Owner seeks to limit the meaning of "electrode stack" to three example electrodes given in the specification: an ohmic contact, a Schottky contact, or an insulated gate.	Unrebutted
The open-ended terms "comprising" and "including" means other components may be part of the "electrical contact" and "electrode stack."	Unrebutted
The dependent claims' specific requirements for certain materials and layer arrangements in the electrode stack, for implementation as particular types of contacts and devices, do not limit the plain meaning of "electrode stack."	Unrebutted
The dependent claims implement the broader term "electrical contact" as an ohmic contact or Schottky contact, which does not specifically require the "electrode stack" make ohmic or Schottky contact.	Unrebutted
"electrode stack" of the independent claims is broader than an insulated gate electrode.	Unrebutted
The 562 specification does not define the term "electrode stack" or disavow its full scope.	Unrebutted
Neither the claims nor the specification equate "electrical contact" and "electrode stack."	Unrebutted
The parties agree an interconnect provides electrical connections between semiconductor components.	Unrebutted
Patent Owner construes "electrode stack" to require ***direct*** electrical contact with a nonmetallic component.	Unrebutted
The patent claims a "semiconductor device" (claims 1, 13) without altering its meaning and does not limit the "electrical contact" or "electrode."	Unrebutted
Patent Owner does not dispute that Yu's barrier 218 is a metal layer stacked along with the other metal layers.	Unrebutted

Reply, 2-7, 10-14, 27; *see generally* Sur-Reply.