

United States Patent and Trademark Office
Before the Patent Trial and Appeal Board

Innoscence America Inc.

(Petitioner)

v.

Infineon Technologies America Corp.

(Patent Owner)

IPR2025-00175 | **U.S. Patent No. 8,686,562**

Infineon Exhibit 2035
Innoscence v. Infineon
IPR2025-00175

April 9, 2026

- **Grounds 1-4 (based on Usui) fail**
 - Construction of “electrode stack”
 - Usui’s interconnect is not an “electrode stack” under any reasonable construction
 - Petitioner cannot ignore Usui’s stud connection 10
 - Grounds 2-4 fail for additional reasons
- **Grounds 5-7 (based on Yu) fail**
 - The Board was correct about Petitioner’s failure to justify modifications to Yu’s layers
 - Petitioner failed to establish Yu’s barrier layer is part of Yu’s electrode
 - Ground 6-7 fail for additional reasons

'562 Patent

1. An electrical contact for use on a semiconductor device, said electrical contact comprising:
an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;
said capping layer consisting only of a refractory metal nitride, said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

EX-1001, Claim 1

Institution Decision

In an effort to guide the parties, we note that, on the current record, neither party has taken an explicit position on the appropriate construction of “electrode stack,” and it appears that such a construction may impact the ultimate determination of whether Usui teaches the limitation. We accordingly direct the parties to take specific positions during the trial on the appropriate construction of “electrode stack” and whether the claims are unpatentable for anticipation or obviousness under such a specific construction.

Institution, 14

Patent Owner also argues that the Petition does not include a detailed explanation of how Usui’s interconnect metallurgy structure is the claimed electrode stack, and, in any event, Petitioner’s assertion that Usui’s interconnect metallurgy structure is an electrode stack is inconsistent with how a POSITA would have understood the term. Prelim. Resp. 14–26. We find that Patent Owner’s arguments in this regard raise issues of fact that are best resolved on a full trial record.

We invite the parties to develop these arguments further at trial, to the extent permitted by our rules.

Institution, 13

The Petition Needed to Explain the Plain Meaning of “Electrode Stack”

POR, 12-13

Patent Owner's Response

A. Petitioner Fails to Explain its Alleged Plain Meaning Construction of “Electrode Stack”

The Board’s rules specify “Content” the Petition “must” have. *See* 37

C.F.R. §§ 42.22 and 42.104. The Petition “*must*” identify “how the challenged claim is to be construed” and “[h]ow the *construed* claim is unpatentable.” 37

C.F.R. § 42.104(b)(3)-(4).

POR, 12

Because Petitioner never explained its alleged plain meaning of “electrode stack,” the Board cannot evaluate if Petitioner’s alleged plain meaning is correct, let alone whether Usui meets that unstated plain meaning. It was Petitioner’s burden to explain *in the Petition* the alleged “plain meaning” of “electrode stack” (Petition, 7 and 11) and how and why Usui’s interconnect metallization structure meets that plain meaning. 37 C.F.R. § 42.104(b)(3)-(4). Petitioner did not meet that burden. The Usui-based grounds fail for this reason alone.

POR, 13



32 C.F.R. § 42.104

§ 42.104 Content of petition.

In addition to the requirements of §§ 42.6, 42.8, 42.22, and 42.24, the petition must set forth:

- (b) *Identification of challenge.* Provide a statement of the precise relief requested for each claim challenged. The statement must identify the following:
 - (1) The claim;
 - (2) The specific statutory grounds under 35 U.S.C. 102 or 103 on which the challenge to the claim is based and the patents or printed publications relied upon for each ground;
 - (3) How the challenged claim is to be construed. Where the claim to be construed contains a means-plus-function or step-plus-function limitation as permitted under 35 U.S.C. 112(f), the construction of the claim must identify the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function;
 - (4) How the construed claim is unpatentable under the statutory grounds identified in paragraph (b)(2) of this section. The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon; and

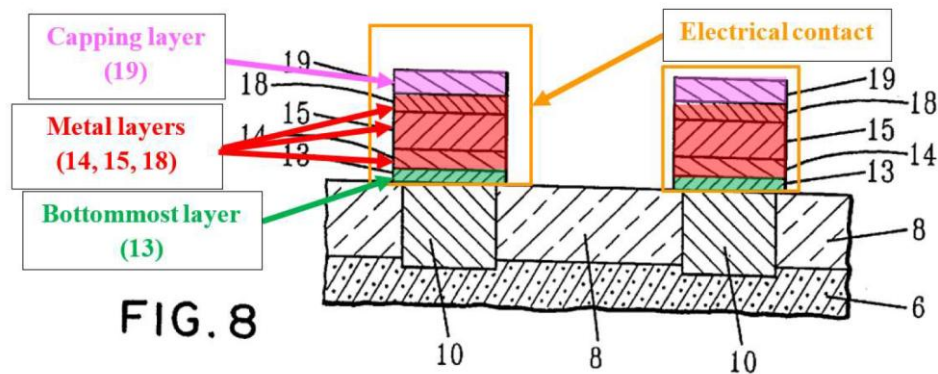
Petition

- b. [1a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;

Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8; Zhao ¶89.

Usui discloses a plurality of metal layers. Usui’s **layer 18** comprises titanium (**metal layer**) (Usui, 4:4-5, Figs. 1 and 8), **layer 15** comprises aluminum or aluminum alloy (**metal layer**) (*id.*, 3:38-41, Figs. 1 and 8), **layer 14** comprises titanium nitride (**metal layer**) (*id.* 3:58-60, Figs. 1 and 8) and **underlayer 13** comprises titanium (**bottommost metal layer**) (collectively, a plurality of metal layers). *Id.*, 5:38, 52, Figs. 1 and 8; Zhao ¶90.

Usui discloses a capping layer. Usui’s **capping layer 19** is **titanium nitride** and is formed above the plurality of **metal layers** (Usui, 5:54-59) forming a top of the **metallization structure (electrical contact)**. *Id.*, Abstract, 3:2-8, Figs. 1 and 8.



Usui, Fig. 8 (annotated); Zhao ¶91.

Usui (EX-1004)

PROCESS FOR FABRICATING A METALLIZATION STRUCTURE

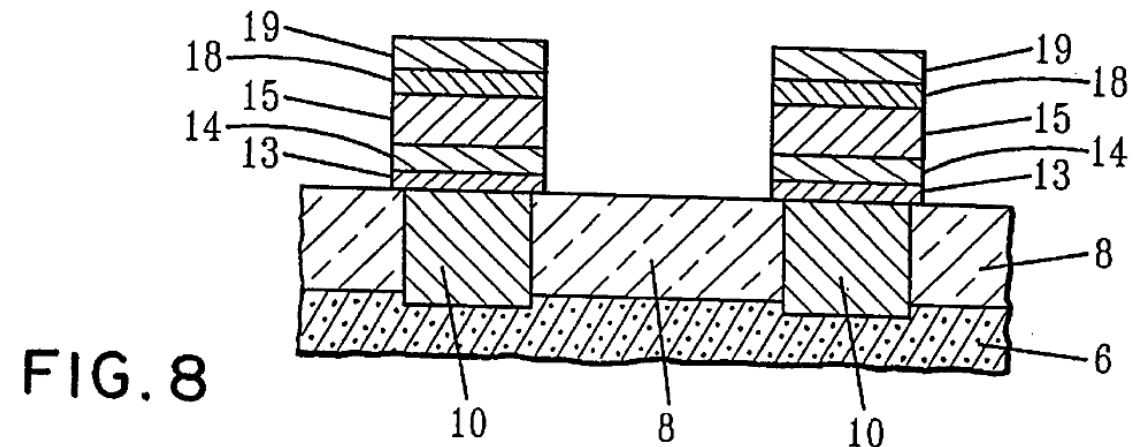
TECHNICAL FIELD

The present invention is concerned with a method for fabricating a metallization structure and is especially concerned with producing a structure having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics. Moreover, the process of the present invention provides highly textured aluminum <111> layers. The structures fabricated by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure.

Usui (EX-1004), 1:11-14

FIGS. 2–8 are a cross-sectional view of the process for fabricating the preferred interconnect metallurgy of the present invention in a step-by-step fashion.

Usui (EX-1004), 3:2-8



Usui (EX-1004), FIG. 8

Piner (EX-2024)

C. Dr. Zhao Confuses Interconnects with Electrical Contacts

62. In the section “Contact Metals,” Dr. Zhao appears to classify “interconnects” as being in the same category as electrical contacts, such as “Schottky barriers,” “ohmic contacts,” and “gates in transistors.” EX-1002 (Zhao Dec.), ¶63. While I agree with Dr. Zhao that metals have been known for many decades to be used as interconnects connecting various semiconductor devices together, generally an interconnect does not have a metal – semiconductor junction like an ohmic contact or gate contact and therefore would not have been confused with an electrical contact.

EX-2024, ¶ 62

63. An interconnect is a term of art since well before August 2009 to specifically refer to conductive strips (commonly aluminum or copper) or wiring that provide low resistance paths for current and *interconnect* various semiconductor devices. *See, e.g.*, EX-1004 (Usui), 1:5-2:38 (describing interconnects as “electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure”), 4:10-15 (interconnect layer in Fig. 8 is “repeated in a multiple level sequence to complete the interconnect circuit for the devices.”). One reference that Dr. Zhao relies upon describes interconnects

EX-2024, ¶ 63; *see also* EX-2024, ¶¶ 64-65

97. As discussed above in Section VI.C (Interconnections), thin metal lines or strips commonly interconnected various circuits and components within a semiconductor chip. These metal interconnections form the various wires between and among the integrated circuit. A single semiconductor chip could include hundreds of thousands of devices with interconnections between all of them. Aluminum and aluminum alloys were commonly used for forming various electrical connections or wiring in electronic devices, such as in integrated circuit structures. EX-1004 (Usui), 1:17–21.

EX-2024, ¶ 97

Patent Owner's Response

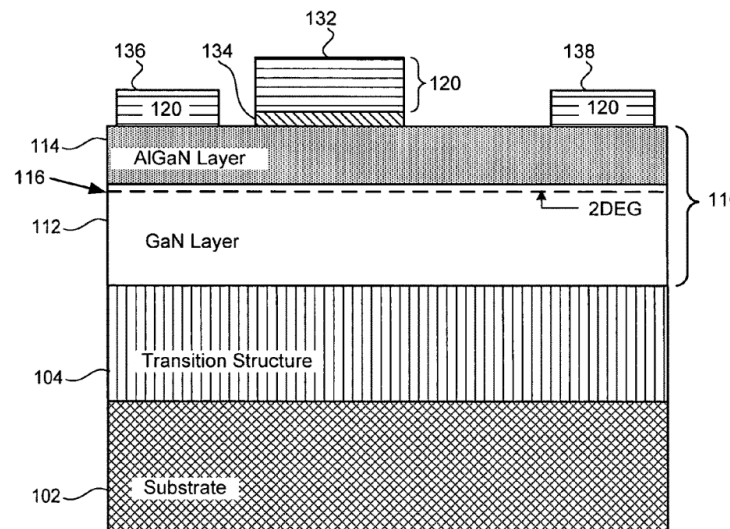
necessary to resolve the parties' dispute). If the Board reaches an outer boundary construction for "electrode stack," the proper construction in view of the specification is a stack of conductive layers that form an electrical contact that is a part of a semiconductor device and used to (1) establish electrical contact with a nonmetallic part of the semiconductor device (like the source, drain and Schottky gate electrodes in the '562 Patent specification) or (2) control the operation of the semiconductor device (like the insulated or Schottky gate electrodes in the '562 Patent Specification). Piner, ¶¶80-91.

POR, 8-9

'562 Patent

Source electrode 136 and drain electrode 138 are power electrodes ohmically coupled to the heterojunction formed by GaN layer 112 and AlGaN layer 114. Moreover, insulated gate electrode 132 is situated between source electrode 136 and drain electrode 138, on GaN body 110. As shown in FIG. 1, each of source electrode 136, drain electrode 138, and insulated gate electrode 132 comprises electrode stack 120. Electrode stack 120 includes a refractory metal nitride capping layer (not explicitly shown in FIG. 1), such as a titanium nitride (TiN) capping layer, for example. As further shown in FIG. 1, insulated gate electrode 132 includes gate insulator layer 134, such as a silicon nitride (Si₃N₄) or silicon dioxide (SiO₂) layer, for example, underlying electrode stack 120. It is noted that although in the embodiment of FIG. 1, gate electrode 132 is shown as an insulated gate electrode, in other embodiments, gate electrode 132 comprising electrode stack 120 may make Schottky contact with GaN body 110.

EX-1001, 3:19-35



EX-1001, FIG. 1

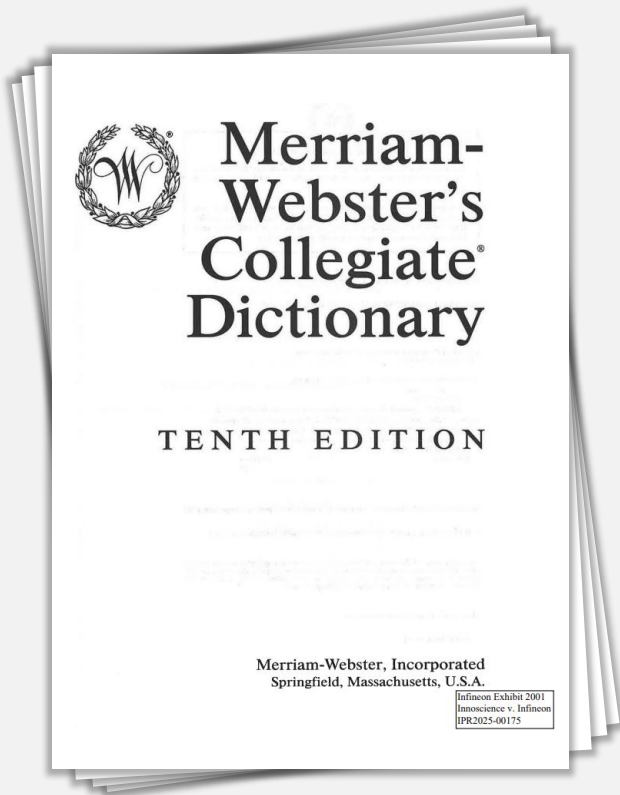


PHILLIPS v. AWH CORP.

Cite as 415 F.3d 1303 (Fed. Cir. 2005)

[7, 8] The claims, of course, do not stand alone. Rather, they are part of “a fully integrated written instrument,” *Markman*, 52 F.3d at 978, consisting principally of a specification that concludes with the claims. For that reason, claims “must be read in view of the specification, of which they are a part.” *Id.* at 979. As we stated in *Vitronics*, the specification “is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.” 90 F.3d at 1582.

Phillips v. AWH Corp., 415 F.3d 1303, 1315 (Fed. Cir. 2005) (cited at POR, 4)



EX-2001

Patent Owner's Response

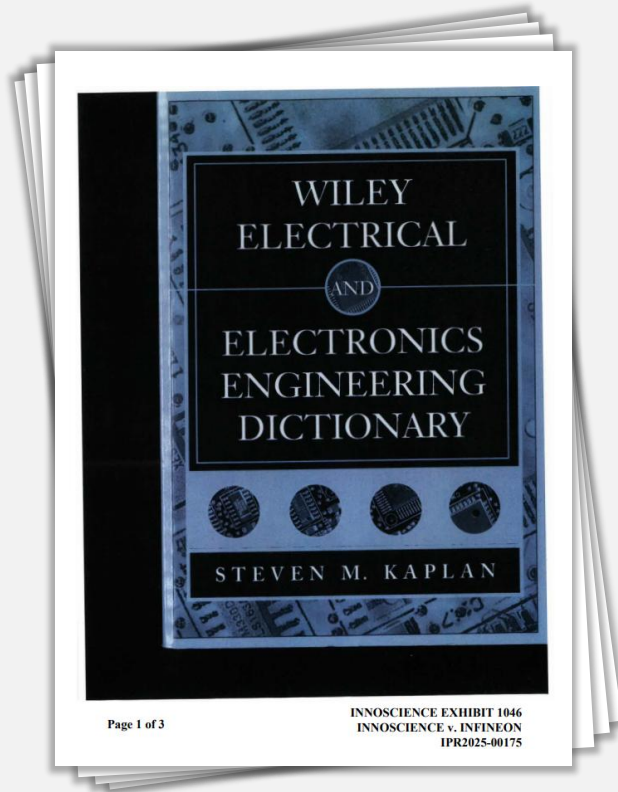
Merriam-Webster's Collegiate Dictionary defines "electrode" as "1: a conductor used to establish electrical contact with a *nonmetallic* part of a circuit" and "2: an element in a semiconductor device (as a transistor) that emits or collects electrons or holes or controls their movements." EX-2001, 371. The '562 Patent's electrodes meet these definitions.

POR, 9 (quoting EX-2001)

Petitioner's Reply

POR, 8-9; Ex-2024, ¶¶91. They purport to rely on (1) intrinsic evidence from the claims, specification, and figures and (2) an extrinsic dictionary definition. POR, 3-10; Ex-2024, ¶¶81-95. But the specification does not limit the claims, *Thorner*, 669 F.3d at 1367, and extrinsic evidence cannot override the patent, *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005).

Reply, 5



EX-1046

Petitioner's Reply

A conductor which serves to deliver, receive, collect, emit, deflect or control electric charge carriers. An electrode provides the path for current entering or leaving a medium such as a dielectric, electrolytic solution, semiconductor, gas, or vacuum. ... It is often a metal, and may consist for instance, of a wire, grid, plate or region.

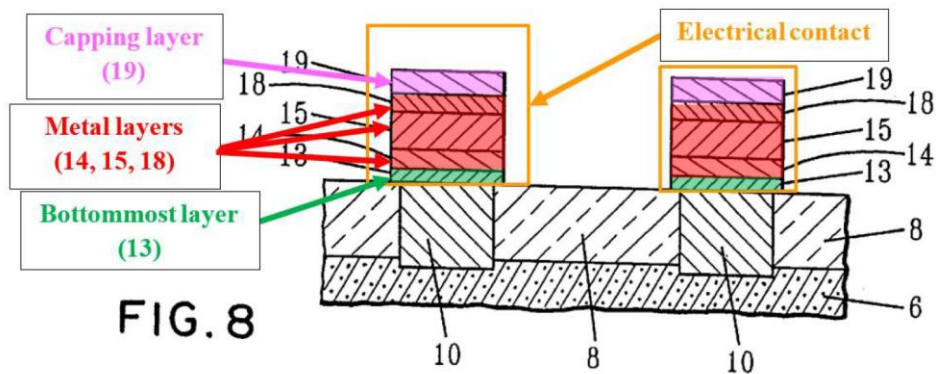
Ex-1046, 237 (emphasis added). This definition broadly describes that electrodes “deliver, receive, collect, emit, deflect or control electric charge carriers” and provide a current path, which is consistent with how a POSTIA would have understood the term “electrode.” Ex-1047, ¶¶38-39.

Reply, 8 (quoting EX-1046)

- **Usui's interconnect (layers 13-15 and 18-19) is not an “electrode” stack under any reasonable construction**
 - Usui's interconnect is unlike any of the '562 patent's electrodes
 - Usui's interconnect does not meet the plain meaning of “electrode stack” under either parties' dictionary definition
 - Usui's interconnect does not establish contact with the semiconductor or provide the current path for entering or leaving the semiconductor
 - Usui's interconnect is not an element in a semiconductor device that controls electron or hole movement
- **Petitioner cannot ignore Usui's stud connection 10**
 - Petitioner's exclusion of Usui's stud connection 10 is fatal
 - If Petitioner's Reply is read as arguing that Usui's alleged electrode stack includes stud connection 10 and still meets the claims, that fails

Petition

Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8; Zhao ¶89.



Petition, 11

'562 Patent

1. An electrical contact for use on a semiconductor device, said electrical contact comprising:
an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;
said capping layer consisting only of a refractory metal nitride, said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

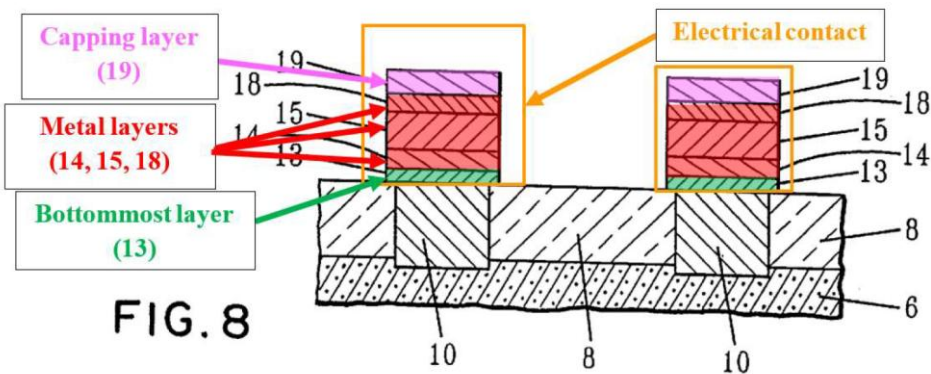
EX-1001, Claim 1

The Petition's Failure to Address Usui's Stud Connection 10 Is Fatal

POR, 11, 18-20;
Sur-Reply, 7-9

Petition

Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8; Zhao ¶89.



Petition, 11

Patent Owner's Response

Usui's interconnect metallurgy structure is connected to "interplanar stud connection 10," which is a "device contact metallization" that "make[s] connection to a device substrate 6." Usui, 3:24-27, 5:14-15.⁵ Petitioner never explains why, if there is an electrode in Usui FIG. 8, the electrode is not the "device contact metallization 10" that "make[s] connection to" the semiconductor "device substrate 6." Usui, 3:24-27, 5:14-15; Piner, ¶136.

POR, 11

Petitioner mischaracterizes Usui's *interconnect* metallization structure (layers 13-15 and 18-19) as an electrode stack to try meeting claim 1's requirement that the capping layer is thicker than the bottommost layer of the plurality of metal layers of the electrode stack. See Limitation [1c]. Petitioner ignores Usui's "device contact metallization 10" (Usui, 5:14-15), which Fig. 8 illustrates as thicker than capping layer 19. Piner, ¶¶152-153.

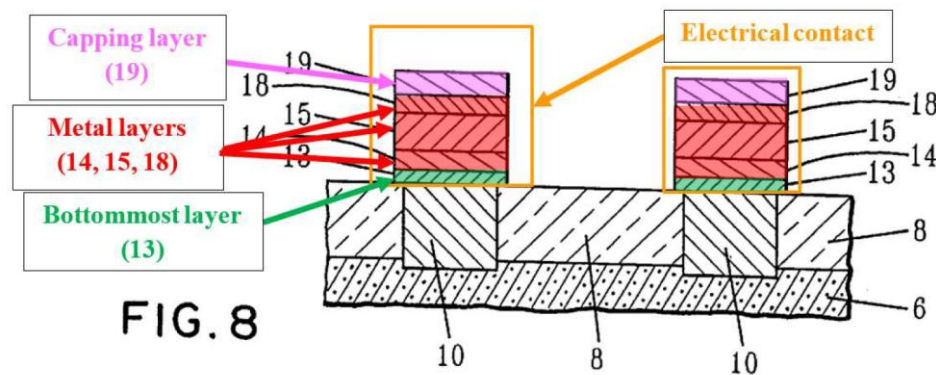
POR, 19

Usui's Stud Connection 10 Establishes Electrical Contact With Nonmetal

POR, 11, 18-20;
Sur-Reply, 4-6

Petition

Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8; Zhao ¶89.



Petition, 11

Usui (EX-1004)

the present invention. Referring to FIG. 1, the interconnect metallurgy preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 to make connection to a device substrate 6. The metallurgy

Usui (EX-1004), 3:24-27

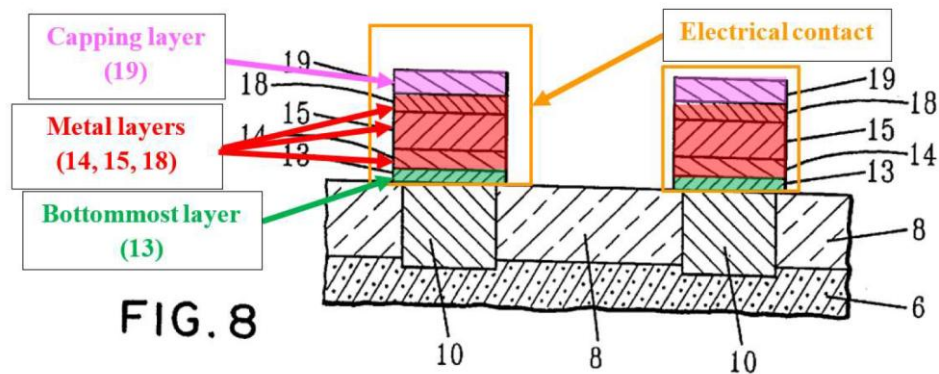
Patent Owner's Sur-Reply

semiconductor meets Wiley's definition. EX-1046, 237. Usui's *stud connection 10* is the conductor that provides "the path for current entering or leaving" Usui's semiconductor 6. Usui, 3:24-27, 5:14-15; Reply, 12 (admitting Usui's interconnect "connects to semiconductor layer 6 *through a conductive via*" 10).³

If there is an electrode in Usui Fig. 8, *it is – or at least includes – stud connection 10 under either party's dictionary definition.*

Sur-Reply, 6; see also POR, 11, 18-20

Petition



Petition, 11

Petitioner's Reply

Nevertheless, Petitioner understands “controls the operation” to involve at least enabling or influencing current flow. Ex-1047, ¶49. Usui satisfies this condition

Reply, 13

Patent Owner's Sur-Reply

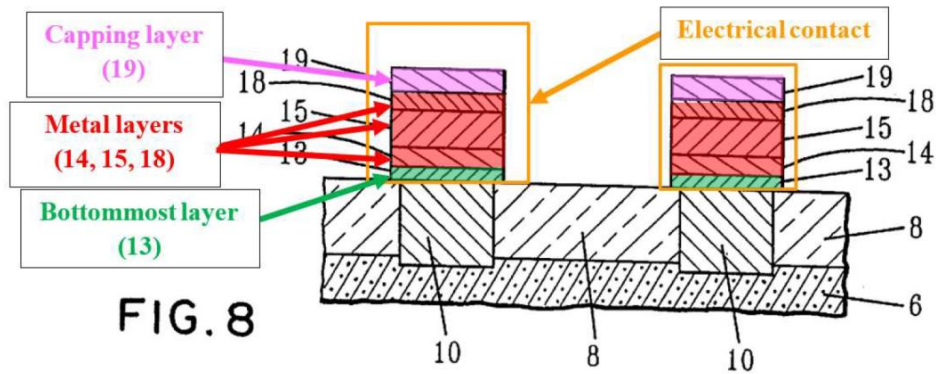
Finally, even if “controls” were as broad as Petitioner alleges (it is not), without stud connection 10, Usui's interconnect does not “provide[] electrical connections between” any “devices” or “enabl[e] and influenc[e] current flow.”

Reply, 13. Again, if there is an electrode in Usui Fig. 8, *it is – or at least includes – stud connection 10.*

Sur-Reply, 7

Petition

Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8; Zhao ¶89.



Petition, 11

'562 Patent

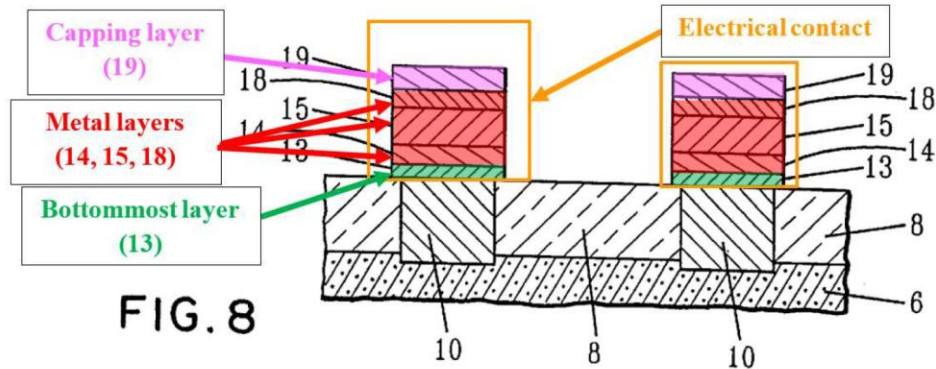
1. An electrical contact for use on a semiconductor device, said electrical contact comprising:
an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;
said capping layer consisting only of a refractory metal nitride, said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

EX-1001, Claim 1

Petitioner's Reply Argument That Stud Connection 10 Is "Not a Layer" Is Nonresponsive

Reply, 10;
Sur-Reply, 8

Petition



Petition, 11

Petitioner's Reply

underlayer 13 and insulator 8. Ex-1047, ¶43. This is because “contact stud 10” is not a layer, it is an interplanar conductive via that cuts across device layers. Ex-1004, 3:24-27, 5:11-13, Figs. 1-8, Ex-1047, ¶43 (citing Ex-2026 (e.g., 10:9-13, 32:14-25, 37:6-14, 37:20-25, 50:11-18, 51:11-52:1, 76:16-20, 77:15-78:2, 79:8-17)). A conductive via is a filled hole, which is typically a much smaller structure than the surrounding layers and structures. Ex-1047, ¶43; Ex-2026, 10:9-13, 32:14-25, 37:6-14, 37:20-25, 50:11-18, 51:11-52:1, 76:16-20, 77:15-78:2, 79:8-17.

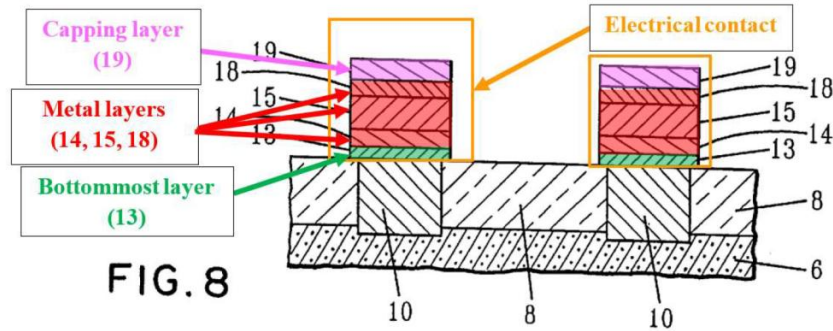
Reply, 10

Patent Owner's Sur-Reply

Petitioner says “‘contact stud 10’ is not a layer.” Reply, 10. Even if that were true (it is not), it fails to show that stud connection 10 is not an electrode. POR, 11, 19-20. Petitioner does not even allege that an electrode must be a “layer” and none of the evidence establishing the plain meaning of “electrode” requires that.

Sur-Reply, 8

Petition



Petition, 11

Patent Owner's Sur-Reply

comprising an electrode). If the Reply is read as alleging that stud connection 10 is part of Usui's electrode, that is a new argument belatedly advanced in an attempt to establish *prima facie* obviousness and should not be considered. TPG, §II.I; *Wasica v. Cont'l Auto*, 853 F.3d 1272, 1286-87 (Fed. Cir. 2017).

Sur-Reply, 9



WASICA FINANCE GMBH v. CONTINENTAL AUTO. SYSTEMS

Cite as 853 F.3d 1272 (Fed. Cir. 2017)

Continental Response Br. 49–59. Rather than explaining how its original petition was correct, Continental's subsequent arguments amount to an entirely new theory of *prima facie* obviousness absent from the petition. Shifting arguments in this fashion is foreclosed by statute, our precedent, and Board guidelines. See 35 U.S.C. § 312(a)(3) (requiring petitions to identify "with particularity ... the grounds on which the challenge to each claim is

based"); *Illumina*, 821 F.3d at 1369–70; *Dell Inc. v. Accelaron, LLC*, 818 F.3d 1293, 1301 (Fed. Cir. 2016) (vacating a finding of unpatentability when the Board relied on an argument first made during oral hearing); *Trial Practice Guide*, 77 Fed. Reg. 48,756, 48,767 (Aug. 14, 2012) (prohibiting parties from submitting evidence necessary for a *prima facie* showing of obviousness in a reply). We therefore see no error in the Board declining to engage such an argument here.

Wasica Finance GmbH v. Cont'l Auto. Sys., 853 F.3d 1272, 1286-87 (Fed. Cir. 2017) (cited at Sur-Reply, 9)

Petitioner's Reply Argument That Stud Connection 10 Is "Not a Layer" Fails

POR, 19-20;
Sur-Reply, 10

Patent Owner's Sur-Reply

Moreover, Petitioner's assertion that stud connection 10 is "not a layer" (Reply, 10) fails. Usui Fig. 8 shows that stud connection 10 is as much a "layer" as layers 13-15 and 18-19. "[N]othing in Usui suggests that contact metal 10 is not itself a metal layer, or... comprise[s] metal layers." Piner, ¶153. POSAs "understood that structures like Usui's contact metal 10 comprise a metal layer or metal layers, which is corroborated by numerous references that illustrate how such structures are made." *Id.* (citing EX-2032, EX-2033).

Sur-Reply, 10; see also POR, 19-20 (citing Piner, ¶ 153; EX-2032; EX-2033)

Piner (EX-2024)

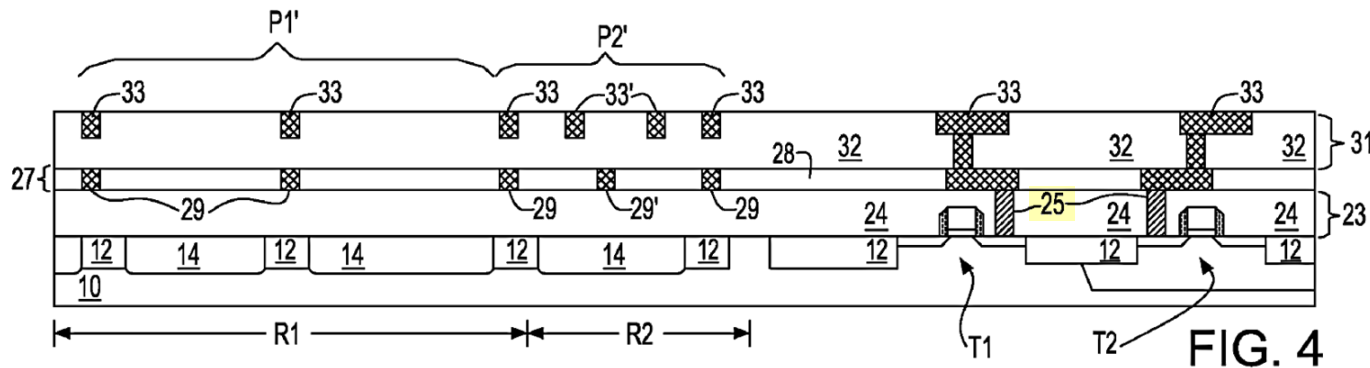
how such structures are made. *E.g.*, EX-2032 (Gambino), 3:51-56 ("The field effect transistor[] T1... is located and fabricated within the semiconductor substrate 10..."), 6:8-19 (describing "contact studs 25" for "effecting optimal electrical contact and conduction to the first transistor T1..."), 7:9-22 (describing FIG. 4: "stud layers 25" and "dielectric layer[]...24" disposed underneath "interconnect layer[] 29"), 8:20-25 (describing "contact studs" as "conductor layers" that "are intended as electrically active layers."), FIGs. 4-5; EX-2033 (Chen-653), [0014] (describing "interconnects in integrated circuits"), [0018] (describing FIG. 3: "via opening 14" over "semiconductor structure 10"), [0021]-[0023] (showing "diffusion barrier layer 18" and "conductive layer 20" in contact with semiconductor 10 within "via opening 14"), FIGs 3-4. A POSA also understood that Usui's contact metal 10 comprises a metal "layer" or "layers," as those words are used in the '562 Patent, regardless of how contact metal 10 was formed – e.g., by chemical vapor deposition (CVD), metal evaporation, or whether it is a "filled hole" as Dr. Zhao suggested during deposition (EX-2026 (Zhao

EX-2024, ¶ 153 (discussing EX-2032, EX-2033)

Petitioner's Reply Argument That Stud Connection 10 Is "Not a Layer" Fails

POR, 19-20;
Sur-Reply, 10

Gambino (EX-2032)



Gambino (EX-2032), FIG. 4

FIG. 4 shows a dielectric/stud-interconnect layer 31 located upon the dielectric/interconnect layer 27 illustrated within the schematic cross-sectional diagram of FIG. 3. The dielectric/stud-interconnect layer 31 comprises dielectric layer 32 and stud-interconnect layers 33 and 33', some of which are not of appropriate cross-section to illustrate stud portions of stud-interconnect layers 33 and 33'. The dielectric layer 32 may comprise materials and be formed using methods generally analogous to the materials and methods used for forming the dielectric layers 28 and 24. The stud-interconnect layers 33 and 33' may comprise materials and be formed using methods generally analogous to the materials and methods used for forming the interconnect layers 29 and 29' or the stud layers 25.

Gambino (EX-2032), 7:9-22

Chen-653 (EX-2033)

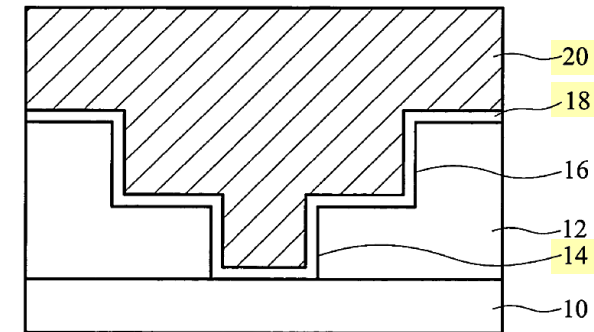


FIG. 4

Chen-653 (EX-2033), FIG. 4

[0021] Referring to FIG. 4, a conformal diffusion barrier layer 18 can be deposited on the sidewalls and bottom of the via opening 14 and the trench 16. The diffusion barrier layer 18 can be deposited by CVD, plasma enhanced CVD, or atomic layer deposition (ALD). The diffusion barrier 18 may include Ta, TaN, Ti, TiN, TaSiN, W, or WN, or a composite layer of two or more of the aforementioned materials. Next, a conductive layer 20, that may be tungsten (W), silver (Ag), or gold (Au) and preferably copper (Cu) or copper alloys, is then deposited over the barrier layer 18, completely filling the trench 16 and via opening 14. The conductive layer 20 may be formed by electroless deposition, CVD methods, or more preferably by electrochemical deposition (ECD).

Chen-653 (EX-2033), [0021]

No Evidence Supports Petitioner's Reply Argument That Stud 10 Is "Not a Layer"

Reply, 10;
Sur-Reply, 10

Petitioner's Reply

underlayer 13 and insulator 8. Ex-1047, ¶43. This is because "contact stud 10" is not a layer, it is an interplanar conductive via that cuts across device layers. Ex-1004, 3:24-27, 5:11-13, Figs. 1-8, Ex-1047, ¶43 (citing Ex-2026 (e.g., 10:9-13, 32:14-25, 37:6-14, 37:20-25, 50:11-18, 51:11-52:1, 76:16-20, 77:15-78:2, 79:8-17)). A conductive via is a filled hole, which is typically a much smaller structure than the surrounding layers and structures. Ex-1047, ¶43; Ex-2026, 10:9-13, 32:14-25, 37:6-14, 37:20-25, 50:11-18, 51:11-52:1, 76:16-20, 77:15-78:2, 79:8-17.

Reply, 10

Patent Owner's Sur-Reply

Petitioner never explains why "an interplanar conductive via" (Reply, 10) is not a "layer" and no evidence supports that. Usui never says metal stud connection 10 is not a layer. Zhao's testimony (Reply, 10) merely parrots the Reply and warrants no weight. *Xerox*, IPR2022-00624, Paper 9, at 15. Unlike Zhao, Dr. Piner cited *corroborating evidence* supporting his explanation that interplanar vias are formed using metal layer(s). Piner, ¶153. Zhao's Reply declaration (EX-1047) did not even acknowledge, let alone rebut, Dr. Piner's testimony or corroborating evidence. Petitioner's assertion that Usui's stud connection 10 does not comprise a metal layer fails.

Sur-Reply, 10

Petitioner’s Reply

Usui’s structure has a substantial area of physical contact between underlayer 13 and insulator 8. Ex-1047, ¶43. This is because “contact stud 10” is not a layer, it is an interplanar conductive via that cuts across device layers. Ex-1004, 3:24-27, 5:11-13, Figs. 1-8, Ex-1047, ¶43 (citing Ex-2026 (e.g., 10:9-13, 32:14-25, 37:6-14, 37:20-25, 50:11-18, 51:11-52:1, 76:16-20, 77:15-78:2, 79:8-17)). A conductive via is a filled hole, which is typically a much smaller structure than the surrounding layers and structures. Ex-1047, ¶43; Ex-2026, 10:9-13, 32:14-25, 37:6-

Reply, 10

Zhao Supp. Dec. (EX-1047)

43. Usui’s structure has a substantial area of physical contact between underlayer 13 and insulator 8. This is because “contact stud 10” is not a layer, it is an interplanar conductive via that cuts across device layers, which I explained during my deposition. Usui at 3:24-27, 5:11-13, Figs. 1-8; Ex. 2026 at 10:6-8,12:2-7, 32:6-13, 33:1-6, 34:1-8, 37:9-14, 40:10-14, 42:4-10, 43:7-18, 76:17-20, 76:23-77:1, 77:16-18, 79:15-17, 79:22-80:9. A conductive via is a filled hole, which is typically a much smaller structure than the surrounding layers and structures. Ex. 2026 at

EX-1047, ¶ 43



XEROX v. BYTEMARK

Patent Trial and Appeal Board

PRECEDENTIAL

Designated: 2/10/2023

in a data record associated with that user’s account.”). Dr. Jones does not cite to any additional supporting evidence or provide any technical reasoning to support his statement. Thus, the cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight. See 37 C.F.R. § 42.65(a)

Xerox Corp. v. Bytemark, Inc., IPR2022-00624, Paper 9, at 15 (Aug. 24, 2022) (precedential) (cited at Sur-Reply, 10)

TITLE 35—PATENTS

§ 312. Petitions

(a) REQUIREMENTS OF PETITION.—A petition filed under section 311 may be considered only if—

(1) the petition is accompanied by payment of the fee established by the Director under section 311;

(2) the petition identifies all real parties in interest;

(3) the petition identifies, in writing and with particularity, each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim, including—

(A) copies of patents and printed publications that the petitioner relies upon in support of the petition; and

(B) affidavits or declarations of supporting evidence and opinions, if the petitioner relies on expert opinions;



37 C.F.R. § 42.22

§ 42.22 Content of petitions and motions.

(a) Each petition or motion must be filed as a separate paper and must include:

(1) A statement of the precise relief requested; and

(2) A full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent.



PERSONAL WEB TECHNOLOGIES, LLC v. APPLE, INC.

Cite as 848 F.3d 987 (Fed. Cir. 2017)

If the Board's statement were read more broadly, it would not be adequately explained and grounded in evidence. Indeed, the Board nowhere clearly explained, or cited evidence showing, *how* the combination of the two references was supposed to work. At least in this case, such a clear,

evidence-supported account of the contemplated workings of the combination is a prerequisite to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination and reasonably expect success in doing so.

Personal Web Techs., LLC v. Apple, Inc., 848 F.3d 987, 994 (Fed. Cir. 2017) (cited at POR, 22)

- **Ground 2**
 - The Petition failed to establish obviousness for claims 12 and 17
 - No motivation to implement Usui with a gate insulator layer
 - Implementing Usui with Yu's gate insulator layer would have rendered Usui inoperable for its intended purpose
 - The Petition's *KSR* rationale fails
 - The Reply improperly attempts to change the Petition's combination
 - Petitioner fails to establish motivation for the Reply's new combination
 - The Reply's *KSR* rationale fails
 - The Reply fails to establish Usui's metal layers could replace Yu DCO metal layers
 - The Reply's new electromigration arguments fail

'562 Patent

12. The electrical contact of claim **8**, wherein said electrical contact is implemented with a gate insulator layer underlying said first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

EX-1001, Claim 12

17. The electrical contact of claim **13**, wherein said electrical contact is implemented with a gate insulator layer underlying a first metal layer of said electrode stack to provide an insulated gate electrode for said group III-V semiconductor device.

EX-1001, Claim 17

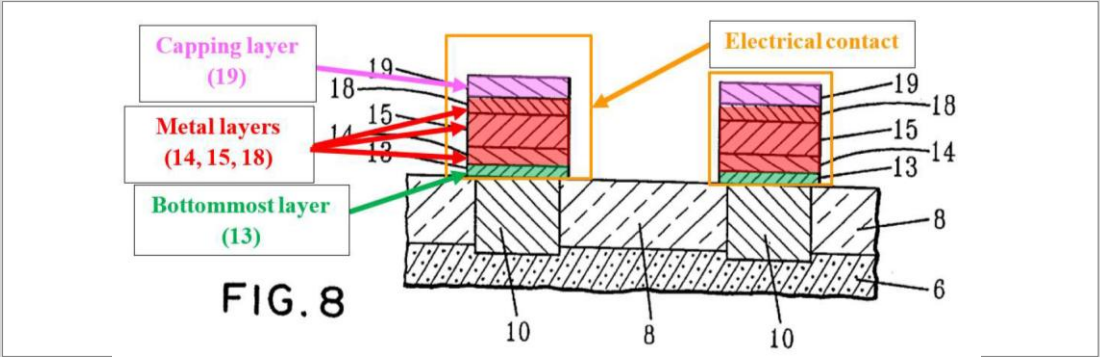
Ground 2: The Petition Says It Would Have Been Obvious to Implement Usui With Yu's Gate Insulator Layer

Petition, 19-20;
POR, 23-25

Petition

114 (citing Ex-1008, 3). Further, Dr. Zhao explains that it was well-known that an important design aspect in thin film transistors is isolating the gate from the channel so that no current flows. Zhao ¶¶60, 114 (citing Ex-1011, 356). To a POSITA it would have been obvious to implement the electrical contact of Usui with Yu's gate insulator layer because Usui discloses the importance of improving electromigration characteristics and such layers are commonly provided under gate structures to address gate leakage—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 401, 416-17; Zhao ¶¶62, 114.

Petition, 20



Petition, 11

Zhao Dec. (EX-1002)

60. FETs, including HEMTs (also known as MODFETs), were known to be made from a wide variety of materials, including group III-V materials by the time of the alleged invention (August 25, 2009). Ex-1011, 356; *see* Zhao ¶¶53-54. The basic concept of a FET is that electrons (or holes) flow from the source to the drain through an active channel of the device. Ex-1011, 356. The conductivity of the channel is modulated by a potential applied to the gate. Ex-1011, 356. This results in the modulation of the charge density flowing in the channel. Ex-1011, 356. It is important to isolate the gate from the channel so that no current flows into the gate. Ex-1011, 356.

EX-1002, ¶ 60

Further, as I explained in Section VI.D, it was well-known that an important design aspect in thin film transistors is isolating the gate from the channel so that no current flows. To a POSITA it would have been obvious to implement the electrical contact

EX-1002, ¶ 114

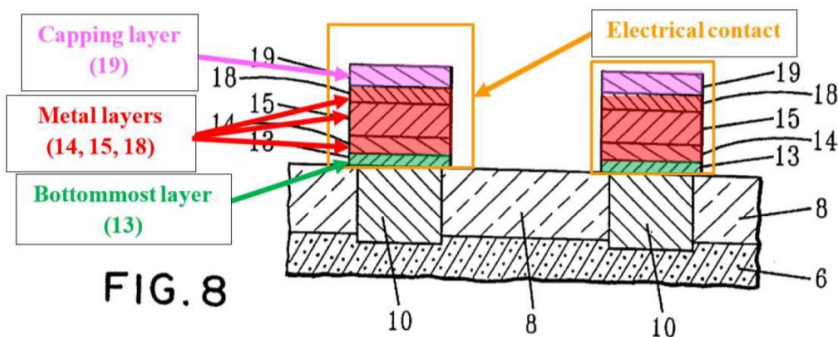
Ground 2 Fails: POSAs Would Not Have Implemented Usui With Yu's Gate Insulator Layer Because Usui Undisputedly Does Not Disclose a Transistor Gate Electrode

Petition, 19-20;
POR, 23-25

Petition

114 (citing Ex-1008, 3). Further, Dr. Zhao explains that it was well-known that an important design aspect in thin film transistors is isolating the gate from the channel so that no current flows. Zhao ¶¶60, 114 (citing Ex-1011, 356). To a POSITA it would have been obvious to implement the electrical contact of Usui with Yu's gate insulator layer because Usui discloses the importance of improving electromigration characteristics and such layers are commonly provided under gate structures to address gate leakage—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 401, 416-17; Zhao ¶¶62, 114.

Petition, 20



Petition, 11

Patent Owner's Response

Even if Usui's identified metal layers formed an electrode – they do not, *supra* §III – there is no need to “isolat[e]” Usui's alleged electrode “from the channel so that no current flows” to “address gate leakage” (Petition, 20) because Usui does not teach that its alleged electrode is a transistor gate electrode overlying a transistor channel. Piner, ¶¶163-166. Usui Fig. 8 does not even disclose a transistor, let alone that the alleged electrode overlies a transistor channel. Piner, ¶167; Zhao-Dep. (EX-2026), 58:17-59:17 (“...in figure 8, there's no information here I could, I could say whether it is or not a transistor...”), 59:18-60:1 (“...whether the...device substrate layer 6 includes a transistor, or not a transistor, it's not discussed in Usui.”). Because Usui does not disclose a transistor gate that would benefit from an insulating layer, Petitioner's alleged motivation for modifying Usui to use a gate insulating layer fails.

POR, 24-25

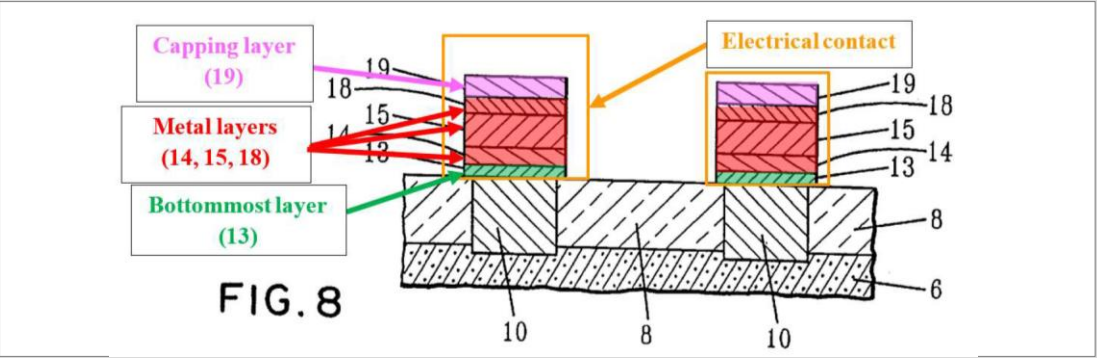
Ground 2 Fails: The Petition’s Modification Would Have Rendered Usui Inoperable for Its Intended Purpose

Petition, 19-20;
POR, 25-26

Petition

114 (citing Ex-1008, 3). Further, Dr. Zhao explains that it was well-known that an important design aspect in thin film transistors is isolating the gate from the channel so that no current flows. Zhao ¶¶60, 114 (citing Ex-1011, 356). To a POSITA it would have been obvious to implement the electrical contact of Usui with Yu’s gate insulator layer because Usui discloses the importance of improving electromigration characteristics and such layers are commonly provided under gate structures to address gate leakage—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int’l Co.*, 550 U.S. at 401, 416-17; Zhao ¶¶62, 114.

Petition, 20



Petition, 11

Patent Owner’s Response

Dep., 13:9-11, 13:23-14:9. Interconnect metal layers 13-15, 18-19 provide an electrical connection between “interplanar stud connection 10” (Usui, 3:27) and another layer of interconnect metal layers, with a “multiple level sequence” of interconnect layers “complet[ing] the interconnect circuit” to another device not shown in Fig. 8. Usui, 4:10-15; Piner, ¶170; Zhao-Dep., 49:24-50:10.

Yu’s gate insulator layer is not conductive. Yu, [0039]; Piner, ¶171; Zhao-Dep., 89:18-25, 90:8. Thus, placing Yu’s gate insulating layer under the alleged electrode in Usui, as Petitioner alleges (Petition, 19-20), would place an insulator **between** Usui’s bottommost layer 13 and interplanar stud connection 10 and **break** the electrical connection therebetween. Piner, ¶172. This would have rendered Usui inoperable for its intended purpose of providing improved “electrical connections or wiring” between devices of an integrated circuit. *Id.*; Usui, 1:11-15.

POR, 25-26

Ground 2 Fails: The Petition's *KSR* Rationale Fails

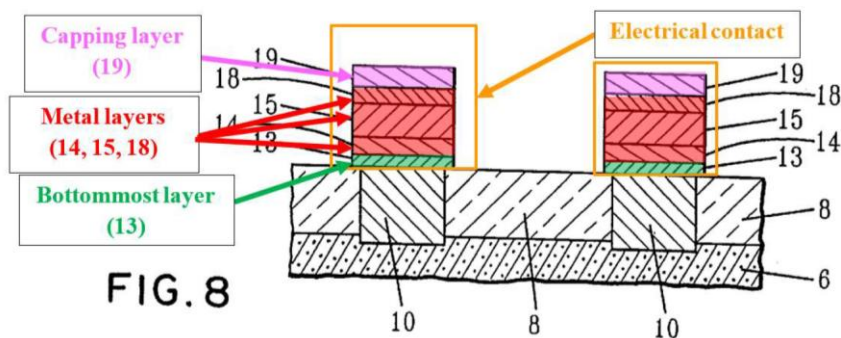
Petition, 19-20;
POR, 26-27

Petition

114 (citing Ex-1008, 3). Further, Dr. Zhao explains that it was well-known that an important design aspect in thin film transistors is isolating the gate from the channel so that no current flows. Zhao ¶¶60, 114 (citing Ex-1011, 356). To a POSITA it would have been obvious to implement the electrical contact of Usui with Yu's gate insulator layer because Usui discloses the importance of improving electromigration characteristics and such layers are commonly provided under gate structures to address gate leakage—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results.

KSR Int'l Co., 550 U.S. at 401, 416-17; Zhao ¶¶62, 114.

Petition, 20



Petition, 11

Patent Owner's Response

improvement” (Petition, 20) likewise fails. Petitioner’s invoked *KSR* rationale only applies when elements are combined “*with no change in their respective functions.*” *KSR*, 550 U.S. at 415-416. Petitioner’s conclusory assertion that Usui was “ready for improvement” never explains how Usui allegedly would have been improved by “implement[ing] the electrical contact of Usui with Yu’s gate insulating layer” (Petition, 20) despite Usui not disclosing a transistor gate electrode that would be improved by being isolated from a likewise-undisclosed transistor channel. Piner, ¶173; Zhao-Dep., 58:17-60:1. Petitioner’s combination also *changes* the function of both Usui’s interconnect (which would be inoperable as an interconnect as discussed above) and Yu’s gate insulating layer¹⁰ (which would no longer separate a gate electrode from a transistor channel as in Yu). Piner, ¶174. Because Petitioner’s combination changes component functions, Petitioner’s invoked *KSR* rationale does not apply.

POR, 26-27

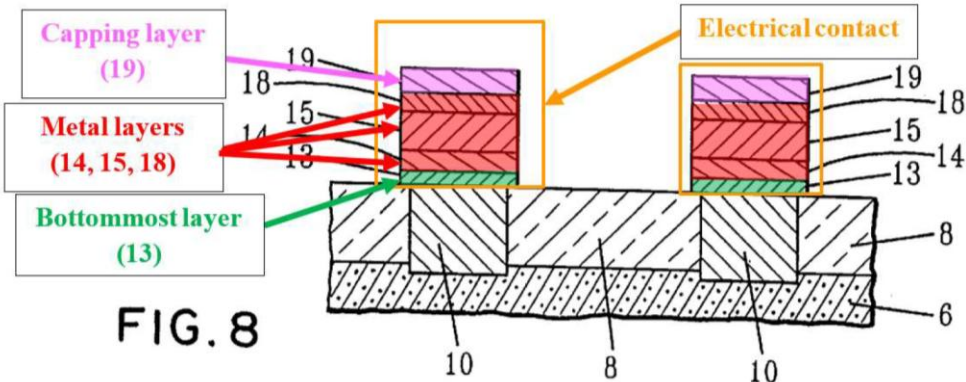
Petitioner's Reply Tries to Change Ground 2 to Yu's Device in View of Usui (Except for Claim 3)

Reply, 17;
Sur-Reply, 12

Petition

channel so that no current flows. Zhao ¶¶60, 114 (citing Ex-1011, 356). To a POSITA it would have been obvious to implement the electrical contact of Usui with Yu's gate insulator layer because Usui discloses the importance of improving electromigration characteristics and such layers are commonly provided under gate structs to address gate leakage— combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 401, 416-17; Zhao ¶¶62, 114.

Petition, 20



Petition, 11

Petitioner's Reply

The combination for claims 12 and 17 implements Usui's electrode stack in Yu's device. Petition, 18-19 (claim 8), 19-20 (claims 12 and 17).² Claim 12 depends

² For claim 3, the Petition described another obvious way to combine Usui and Yu by using Yu's TaN in Usui's device. Petition, 17-18; see Ex-2026, 198:9-199:9.

Reply, 17

Patent Owner's Sur-Reply

"electrode stack in Yu's device." *Id.*, 17. The Board should hold Petitioner to the Petition's Ground 2 – "Usui in view of Yu" (*id.*, 16) which indisputably fails for claims 12 and 17. POR, 23-28.

Sur-Reply, 12

Ground 2 in Petitioner's Reply Fails: *KSR* Still Does Not Apply

POR, 27;
Sur-Reply, 12

Patent Owner's Sur-Reply

a. *KSR*'s Rationale Does Not Apply

Ground 2's motivation-to-combine argument for claims 12 and 17 relied on *KSR*'s known elements/techniques rationale. Petition, 20. Petitioner does not dispute that this rationale does not apply to the *Reply*'s combination which changes the function of Usui's metal layers from being an interconnect to being a transistor electrode. POR, 27 n.10; Piner, ¶175; *KSR*, 550 U.S. at 415-416 (rationale *only applies* when prior art elements are combined "with no change in their respective functions.").

Sur-Reply, 12

Patent Owner's Response

Usui with a gate insulating layer. Petition, 20. If Petitioner belatedly were to allege that a POSA would have replaced Yu's gate electrode with Usui's metal stack, that would fail for multiple reasons. First, it would preclude application of the *KSR* rationale Petitioner invokes (Petition, 20) because it would change the function of *Usui*'s metal layers from a single interconnect layer – connecting metal stud 10 to another interconnect level forming an interconnect circuit to another device (Usui, 3:23-27, 4:10-15) – to a gate electrode. Piner, ¶175. Second, POSAs would not have made such a modification. Usui teaches a particular metal stack for wires to mitigate electromigration due to high current density (Usui, 1:30-41, 2:33-39; *infra* §IV.D.2) which is not a concern for Yu's gate electrode which does not experience high current density. Piner, ¶175. Conversely, Yu teaches a specific metal stack with a particular work function chosen to be compatible with a *high-K dielectric* gate insulator. *Id.*; Yu, [0004], [0029]; *infra* §V.A.

POR, 27 n.10

Ground 2 in Petitioner's Reply Fails: Yu Teaches Exacting Requirements for Its Gate Electrodes

POR, 44;
Sur-Reply, 12-14

Piner (EX-2024)

and the knowledge of a POSA. Yu is directed to a particular technique for forming a metal gate electrode for a complementary metal-oxide-semiconductor (CMOS) device. EX-1005 (Yu), [0004]. Yu explains that:

CMOS devices have typically been formed with a gate oxide and polysilicon gate electrode. There has been a desire to replace the gate oxide and *polysilicon gate electrode* with a high-k gate dielectric and *metal gate electrode* to improve device performance as feature sizes continue to decrease. Current processing utilizes metal, metal carbide, and/or metal nitride for the gate electrode. However, such materials provide insufficient work function values and present thermal stability issues, particularly when utilized in an n-type MOS device (NMOS) and a p-type MOS device (PMOS), which require different work functions for their respective gate electrode.

EX-1005 (Yu), [0004] (emphasis added). In particular, Yu notes that “metal, metal carbide, and/or metal nitride” used in metal gate structures “provide insufficient work function values and insufficient thermal stability.” *Id.*, [0004], [0032].

EX-2024, ¶¶ 107-108 (discussing Yu (EX-1005)); see also EX-2024, ¶ 175

108. Yu addresses the above-discussed problem by providing a CMOS device whose two transistors have metal gate electrodes formed from different metal layers made of “doped-conducting metal oxide (DCO)” in order to “provide desired work function values and thermal stability.” EX-1005 (Yu), [0019], [0033]. A first gate electrode includes a “first metal layer 220 compris[ing] a material with a first work function” and the second gate electrode includes a “second metal layer 222 compris[ing] a material with a second work function.” EX-1005 (Yu), [0029]; see also *id.*, Fig. 2E and [0033] (“metal layers 220, 222 [are provided with] correct work function values”). Yu’s goal of providing “different work functions for their respective gate electrode” is achieved by providing different work functions for the metal layers 220 and 222. EX-1005 (Yu), [0004], [0029], [0033].

Ground 2 in Petitioner's Reply Fails: POSAs Never Would Have Replaced Yu's Gate Electrodes With Usui's Metal Stack

POR, 44-45;
Sur-Reply, 12-14

Patent Owner's Sur-Reply

Yu's *two* gate electrodes use *different* metal stacks with different work functions. Yu, [0029]-[0030]. POSAs never would have replaced *both* Yu gate electrodes with Usui's metal stack because that would have yielded the same work function for both gate electrodes. Indeed, Petitioner ignores Yu's work function teachings entirely.

Petitioner says POSAs would have “place[d] the Usui contact in the transistor of Yu” and “include[d] the gate insulator layer.” Reply, 17. Some metals “provide *insufficient* work function values and insufficient thermal stability” to work with Yu's high-K gate insulator. Yu, [0032]. Yu used a “doped-conducting metal oxide (DCO)” to “achieve[.]” the necessary work function and thermal stability. Yu, [0033]. Usui's metal stack is not a DCO and Petitioner never alleges that Usui's metal stack had a sufficient work function and thermal stability to be compatible with Yu's high-K gate insulator, let alone submit evidence proving it.

Sur-Reply, 12-13

Yu (EX-1005)

[0032] Conventional metal layers utilized in metal gate structures comprise metal, metal carbide, and/or metal nitride. For example, conventional metal layer 220 would comprise metal carbide (e.g., TaC) in the active/NMOS region 211A, and conventional metal layer 222 would comprise metal nitride (e.g., Mo₂N) in the active/PMOS region 211B. However, these conventional metal layers provide insufficient work function values and insufficient thermal stability.

[0033] The present embodiment provides metal layers 220, 222 with correct work function values (e.g., more band-edge work function for doped-channel device, mid-gap work function for depleted channel device, etc.) and better thermal stability. Such improved work function values and thermal stability is achieved by the metal layers 220, 222 comprising a doped-conducting metal oxide (DCO). The DCO may comprise SnO₂, In₂O₃, ZnO, CdO, and/or combinations thereof; SnO₂ doped with Sb, F, As, Nb, Ta, and/or combinations thereof; In₂O₃ doped with Zn, Ge, Mo, F, Ti, Zr, Hf, Nb, Ta, W, Te, Ga, Mg, Sn, and/or combinations thereof; ZnO doped with Al, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf, and/or combinations thereof; CdO doped with In, Sn, and/or combinations thereof; CdSb₂O₆ doped with Y; other suitable materials; and/or combinations thereof (e.g., ZnO doped with SnO₂; ZnO doped with In₂O₃; ZnO doped with In₂O₃ doped with SnO₂). The DCO may comprise a transparent conducting oxide (TCO), which may include SnO₂, In₂O₃, ZnO, CdO, and/or combinations thereof. TCOs are widely utilized

Yu (EX-1005), [0032]-[0033]

The Petition Wrongly Equated Electromigration With Current Flow

Petition, 20, 31;
POR, 29, 36, 40

Petition

channel so that no current flows. Zhao ¶¶60, 114 (citing Ex-1011, 356). To a POSITA it would have been obvious to implement the electrical contact of Usui with Yu's gate insulator layer because Usui discloses the importance of improving electromigration characteristics and such layers are commonly provided under gate structs to address gate leakage— combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 401, 416-17; Zhao ¶¶62, 114.

Petition, 20

Usui disclosed the importance of enhanced electromigration. Usui, Abstract. A POSITA would have been motivated to implement the contact of Usui-Yu as a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide improved current flow (i.e., enhanced electromigration) and Sugimoto, like Yu, also teaches the use of III-V semiconductor devices. Furthermore, such a combination is the result of combining

Petition, 31

Patent Owner's Response

Petitioner badly misunderstands “electromigration.” Electromigration does not refer to “current flow” as Petitioner suggests via its parenthetical equating the terms. *Id.* Both experts agree that electromigration refers to electron-flow-induced movement of *metal atoms* in a conductor which can cause reliability and performance issues for the conductor. Piner, ¶¶215-218 (citing EX-2029, EX-2030, EX-2031), 66-67, 99-101; Zhao-Dep., 13:23-14:9, 53:18-54:25; Usui, 1:30-41 (“Migration of *aluminum atoms* into the underlying silicon can interfere with the performance and reliability of the resulting integrated circuit...”).

POR, 40

Ground 2 in Petitioner's Reply Fails: Electromigration Would Not Have Motivated Change to Yu's Gate Electrodes

POR, 25, 27;
Sur-Reply, 14-16

Patent Owner's Sur-Reply

The Reply's new argument that POSAs would have replaced Yu's carefully-chosen DCO metal gate electrodes to use Usui's metal stack to *reduce* electromigration fails. Petitioner does not dispute that Usui teaches a metal stack for *interconnect wires* to mitigate electromigration due to high current density. Usui, 1:30-41, 2:33-39; POR, §IV.D.2. That was not a concern for Yu's *gate* electrode which does not experience high current density. Piner, ¶175. Petitioner's

Sur-Reply, 14-15

Patent Owner's Response

Usui's metal layers 13-15 and 18-19 provide "electrical connections or wiring in electronic devices" with improved "electromigration characteristics." Usui, 1:17-23, 2:33-39; Petition, 19 (admitting same); Piner, ¶¶168-169; Zhao-Dep., 13:9-11, 13:23-14:9. Interconnect metal layers 13-15, 18-19 provide an

POR, 25

Usui (EX-1004)

Aluminum and aluminum alloys are used for forming various electrical connections or wiring in electronic devices such as in integrated circuit structures. The aluminum or aluminum alloys are used for forming the electrical connections between active and/or passive devices of the integrated circuit structure. It has been the practice to use aluminum or an alloy electrically connected to an underlying substrate such as silicon. While the aluminum and silicon are electrically connected together, it has become the practice to use intermediate electrically conductive layers interposed between the silicon and aluminum to provide better electrical connection to the silicon, and to provide a physical (metallurgical) barrier between the silicon and aluminum. This is for the purpose of preventing electromigration and spiking of the aluminum into the silicon. Migration of aluminum atoms into the underlying silicon can interfere with the performance and reliability of the resulting integrated circuit structure.

In addition to electromigration, the problem of hillock growth also occurs. These problems are especially pronounced at the submicron level. As the demand increases for scaling down the dimensions of the interconnection lines and for increasing the current density, overcoming, or at least minimizing, electromigration and hillock growth is essential.

Usui (EX-1004), 1:17-23, 1:30-41

Ground 2 in Petitioner's Reply Fails: Electromigration Would Not Have Motivated Change to Yu's Gate Electrodes

POR, 24, 27;
Sur-Reply, 14-16

Piner (EX-2024)

(Usui), 3:23-27, 4:10-15) – to functioning as a gate electrode. Moreover, a POSA would not have made such a modification because, as discussed above in Sections VI.C, Usui teaches a particular metal stack for wires to mitigate electromigration due to high current density (EX-1004 (Usui), 1:30-41, 2:33-39), which is not a concern for Yu's gate electrode, because it does not experience high current density. See also my discussion regarding current density and electromigration above in Section VIII.A and below in Section IX.B.3.a.iii. Additionally, as I

EX-2024, ¶ 175 (cited at POR, 27 n.10 & Sur-Reply, 15)

166. As I discussed above in Section VI.B, a gate electrode, or gate contact, is an electrode on a semiconductor purposefully designed and intended to provide a voltage to modulate conduction of electrons in the semiconductor underneath the gate contact. Usui does not use the words “gate” or “gate

EX-2024, ¶ 166 (cited at POR, 24 & Sur-Reply, 6); see also EX-2024, ¶¶ 59-60

38. This overall arrangement of source, gate, and drain electrodes on a semiconductor illustrates the fundamental components of a field effect transistor (FET). The basic concept behind the transistor can be analogized to the flow of water through a channel. EX-1011 (Mishra), 246-248 (Page 270-272 of 583). The transistor has an active channel in the semiconductor through which charge carriers (electrons or holes) flow between from the source and the drain. EX-1011 (Mishra), 356-378 (Pages 380-402 of 583). The source and drain contacts are ohmic contacts. EX-1011 (Mishra), 356-358 (Pages 380-382 of 583). The conductivity of the channel is modulated by a potential applied to the gate, which is isolated from the channel. *Id.* This results in the modulation of the charge density flowing in the channel. *Id.*

EX-2024, ¶ 38 (cited at Sur-Reply, 6)

Ground 2 in Petitioner’s Reply Fails: Petitioner’s New Electromigration Evidence Does Not Apply to Yu’s Insulated CMOS Gate Electrodes

Reply, 19;
Sur-Reply, 15

Petitioner’s Reply

interconnects. See Section IV.C.3; Ex-2024, ¶¶104, 134; Ex-1047, ¶¶57-63. Even an Infineon patent disagrees, identifying electromigration as a problem for gate electrodes. Ex-1043, 1:17-36, 2:39-61, Fig. 1.

Reply, 19



Patent Owner’s Sur-Reply

Petitioner’s assertion that “an Infineon patent” “identif[ies] electromigration as a problem for *gate* electrodes” fails. Reply, 19. EX-1043 is published application with numbered paragraphs, so Petitioner’s column:line citations make no sense. Reply, 19. Moreover, “electromigration” appears once in EX-1043 ([0004]) and never in connection with a gate electrode like Yu’s.

Sur-Reply, 15

Pavier (EX-1043)

(19) **United States**
(12) **Patent Application Publication**
Pavier et al.

(10) **Pub. No.: US 2007/0108585 A1**

INNOSCIENCE EXHIBIT 1043

[0004] It is believed that the reduction in the size of the electrodes combined with an increase in the current load passing through the electrode and its solder connection, particularly in the presence of high switching frequencies, may result in a higher than desirable failure rate in the solder connection due, for example, to electromigration or the like phenomenon.

EX-1043, [0004]

Ground 2 in Petitioner’s Reply Fails: Petitioner’s New Electromigration Evidence Regarding HEMT Does Not Apply to Yu’s Insulated CMOS Gate Electrodes

Reply, 16;
Sur-Reply, 15

Petitioner’s Reply

The electrical contact of the ’562 patent would have experienced electromigration. Ex-1047, ¶¶60-63. HEMT power transistors often have high current flows and densities, including in ohmic contacts, which can cause electromigration. Ex-1047, ¶61; Ex-1001, 2:53-65, claims 9, 14. Gate leakage can

Reply, 16

Patent Owner’s Sur-Reply

electrode which does not experience high current density. Piner, ¶175. Petitioner’s assertion that “HEMT power transistors often have high current flows and densities, including in ohmic contacts, which can cause electromigration” (Reply, 16) does not help Petitioner because Yu is a CMOS (not HEMT) device and its gate electrodes are *insulated* so they do not make ohmic contact with the semiconductor. Piner, ¶¶291, 210, 284-285; EX-1002 (Zhao-Dec.), ¶¶56-57.

Sur-Reply, 15

Piner (EX-2024)

291. Yu’s gate stacks form *gate electrodes*— plural, because CMOS devices include two or more transistors (EX-2026 (Zhao Dep.), 60:15-17) – *for a CMOS device that* are undisputedly not *ohmic* contacts because they do not contact the semiconductor. Yu, Title, Abstract, [0004], Fig. 2E, [0027] (insulating “dielectric layer 214” is “formed over the substrate”); EX-1002 (Zhao Dec.), ¶¶56-57. See my discussion above regarding ohmic contacts, in Section VI.A (¶¶48-57).

EX-2024, ¶ 291

Yu (EX-1005)

(54) **STRUCTURE AND METHOD FOR A CMOS DEVICE WITH DOPED CONDUCTING METAL OXIDE AS THE GATE ELECTRODE**

Yu (EX-1005), Title

Ground 2 in Petitioner's Reply Fails: Petitioner's Purported Evidence That Gate Leakage Causes Electromigration Does Not Apply to Yu's Insulated CMOS Gate Electrodes

Reply, 16;
Sur-Reply, 15-16

Petitioner's Reply

electromigration. Ex-1047, ¶61; Ex-1001, 2:53-65, claims 9, 14. Gate leakage can also cause electromigration in gate electrodes. Ex-1047, ¶62; Ex-1018 at 937. This

Reply, 16

Patent Owner's Sur-Reply

considered. TPG, §II.I; *Wasica*, 853 F.3d at 1286-87. If considered, Petitioner's argument that electromigration from "gate leakage" is a concern for Yu's *insulated* gate electrode fails.⁴ EX-1018 never mentions "electromigration" let alone teach that gate leakage causes electromigration. Worse yet, EX-1018 says gate leakage is addressed by using a *gate insulator*, including a "(high-k)" insulator like Yu's. EX-1018, 1; Yu, [0006], [0028]; Petition, 4 (admitting insulators "address gate leakage"). This proves *Infineon's* point that there was no electromigration concern for Yu's *insulated* gate electrode. EX-1018, 1; Yu, [0004]; POR, 27, 44, 71.

Sur-Reply, 15-16

Kuzmik (EX-1018)

Gate leakage current is an important factor that limits the performance and reliability of conventional high-power AlGaIn/GaN HEMTs [9]. Thus, a thin dielectric oxide layer is often inserted between the gate metal and the AlGaIn barrier layer leading to the approach of the MOS HEMT [9]–[14]. The dielectric was also used to cover the bare surface between the HEMT contacts [10], [13]. Consequently, the AlGaIn surface traps were passivated and the current collapse reduction was obtained simultaneously with the gate insulation [10], [13]. On the other hand, by applying the gate insulation, the gate to channel separation increases, and a shift of V_T due to a gate-to-source capacitance C_{GS} decrease can be observed [9]–[13], [14]. Furthermore, if we adopt $g_m = v_{sat} C_{GS} / L_G$ [11] where g_m is the device intrinsic transconductance, v_{sat} the electron saturation velocity, and L_G the gate length, g_m is supposed to decrease proportionally to C_{GS} . The use of high-permittivity (high- k) insulating materials such as already reported for AlGaIn/GaN (Al_2O_3 ($k_{ox} \sim 9$) [12], HfO_2 ($k_{ox} \sim 20$ –25) [10] or ZrO_2 ($k_{ox} \sim 23$ –30) [13]–[15]) has eliminated these drawbacks. Despite high k , ZrO_2 and HfO_2 materials provide

Kuzmik (EX-1018), page 1 of 5

- **Ground 3**
 - Claims 11 and 16:
 - The Petition did not explain contemplated workings of Usui-Yu-Adesida
 - Adesida's Schottky gate electrode provided no reason to modify Usui
 - Modifying Usui to include a Schottky contact would have rendered Usui inoperable for its intended purpose
 - The Reply's attempts to change the combination should be rejected
 - The Reply fails to explain contemplated workings of the new combination
 - The Reply fails to identify reason to combine or explain what materials are interchangeable
 - The Reply's new combination includes nothing from Yu
 - The Reply's new electromigration arguments fail
 - Claims 9 and 14:
 - The Petition badly misunderstood electromigration
 - The Petition's *KSR* rationales fail

Ground 3 (Claims 11 & 16) Fails: No Explanation of Contemplated Workings of Combination

Petition, 26-27;
POR, 32-34

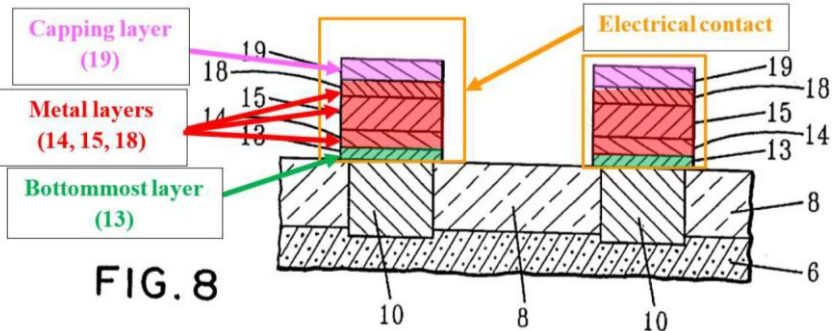
Petition

Claims 11 and 16 - A POSITA would have been motivated to implement Usui's electrical contact as a gate electrode making Schottky contact, as taught by Adesida, with said group III-V semiconductor device as taught by Yu

Petition, 26-27

It would have been obvious to implement the electrical contact of Usui-Yu in a device with a gate electrode making Schottky contact, as taught by Adesida. Zhao ¶¶48-61, 137; Sections VII.C.1, VII.C.1.b.

Petition, 29



Petition, 11

'562 Patent

11. The electrical contact of claim 8, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

EX-1001, Claim 11; see also EX-1001, claim 16



PERSONAL WEB TECHNOLOGIES, LLC v. APPLE, INC.
Cite as 848 F.3d 987 (Fed. Cir. 2017)

If the Board's statement were read more broadly, it would not be adequately explained and grounded in evidence. Indeed, the Board nowhere clearly explained, or cited evidence showing, *how* the combination of the two references was supposed to work. At least in this case, such a clear,

evidence-supported account of the contemplated workings of the combination is a prerequisite to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination and reasonably expect success in doing so.

Personal Web Techs., LLC v. Apple, Inc., 848 F.3d 987, 994 (Fed. Cir. 2017) (cited at POR, 33)

Ground 3 (Claims 11 & 16) Fails: No Reason to Implement Usui as a Schottky Gate Contact

Petition, 24, 26;
POR, 28-32

Petition

Adesida is analogous to the '562 patent because it is in the same field of endeavor, forming electrical contacts for semiconductor devices (Adesida, Abstract; '562, Abstract), and addresses the same problem of providing enhanced or simplified fabrication as the '562 patent (Adesida, [0015]-[0017], [0032]-[0034]). Consistent with the '562 patent, Adesida discloses a gate electrode making Schottky contact and power electrodes (source and drain electrodes) making ohmic contact. Adesida, [0031]. Similar to Yu, Adesida also discloses a III-V semiconductor device (*id.*) Zhao ¶129.

Petition, 24

Usui and Yu do not expressly disclose an electrical contact implemented as a gate electrode making Schottky contact. But Adesida does. Like Yu, Adesida teaches the use of a III-V semiconductor device. By August 2009, Dr. Zhao explains it was well-known that Schottky contacts are of critical importance with respect to device functionality, performance, and long-term reliability. Zhao ¶55 (citing Ex-1013, 144). It was well-known that Schottky contacts serve as gate contacts in group III-V devices and have excellent rectifying properties, which make them suitable for high frequency applications. Zhao ¶¶59, 132.

Petition, 26

Patent Owner's Response

Petitioner cites “Sections VIII.C.1, VIII.C.1.b” (Petition, 29) but no supportable reason to combine is found there. Section VIII.C.1 merely alleges that Adesida is analogous art. Petition, 24. Section VIII.C.1.b says that Schottky gate contacts were known in group III-V devices, like Yu’s and Adesida’s, and were “well known for their suitability for high frequency applications and therefore enhanced electromigration.”¹¹ Petition, 26. Even if Petitioner’s assertions that a Schottky gate electrode was known to have benefits over insulated gate electrodes are accepted as true, they establish no reason why a POSA would have modified *Usui* because Usui **does not disclose a transistor gate electrode**. *Supra* §IV.B; Piner, ¶¶179-183; Zhao-Dep., 58:17-60:1.

POR, 29

Ground 3 (Claims 11 & 16) Fails: “Simple Design Choice” and KSR Rationales Fail

Petition, 26-27;
POR, 30-32

Petition

Usui discloses the importance of enhanced electromigration. Usui, Abstract. A POSITA would have been motivated to implement the electrical contacts as taught by Usui-Yu as a gate electrode making Schottky contact, as taught by Adesida, because both Yu and Adesida disclose the use of III-V semiconductor devices. Furthermore, Schottky contacts are well known for their suitability for high frequency applications and therefore enhanced electromigration. Furthermore, it was well-known at the time that implementing the Usui-Yu contact as a Schottky contact, as taught by Adesida, constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications)—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int’l Co.*, 550 U.S. at 416-17; Zhao ¶¶48-59, 133.

Petition, 26-27

Patent Owner’s Response

¶186; Zhao, ¶58; Zhao-Dep., 123:19-124:3 (“...there are two types of commonly used gate structure, insulated gate **with** a insulating or dielectric layer, or Schottky gate **without** the insulating or dielectric layers”). Modifying Usui to have its alleged electrode somehow make Schottky contact with a transistor channel would have been the furthest thing from a “simple design choice” because Usui’s alleged electrode is not a transistor gate electrode and it is separated from the semiconductor by insulator 8. Piner, ¶186; Zhao-Dep., 58:17-60:1.

POR, 30-31

known device ready for improvement” (Petition, 26-27) fails. That KSR rationale only applies when elements are combined “with no change in their respective functions.” *KSR*, 550 U.S. at 415-416. Petitioner’s conclusory assertion that Usui was “ready for improvement” never even explains how Usui allegedly would have been improved by “implementing the Usui-Yu contact as a Schottky contact” (Petition, 26) despite Usui not disclosing a transistor gate electrode that could be improved by implementing it as a Schottky gate electrode. Piner, ¶¶187-188;

POR, 31

Piner (EX-2024)

1002 (Zhao Dec.), ¶133. I do not agree. As I discussed above in Sections VI.A and VI.B, electrical contact design was anything but simple and nothing that Petitioner or Dr. Zhao cite indicates that anyone had ever modified an interconnect structure to be used as a Schottky gate in a transistor, to say nothing of modifying Usui's specific structure. To the contrary, as one reference put it, fabrication of electrical contacts is "still more art than science." EX-1017 (Kramer), 31 (Page 38 of 151); *see also* EX-1017 (Kramer), 51 (Page 58 of 151) ("Literature shows that the actual mechanism of Ohmic contact formation is still subject of discussion and yet to be understood."). Although the author in EX-1016 specifically referred to ohmic contact fabrication, the statement about complexity also applies to Schottky contact fabrication – and in fact is still true today, a decade and half later.

186. Moreover, even if it *were* a "simple design choice" to choose between an insulated gate electrode and a Schottky gate electrode when implementing a transistor – which I do not concede – I note that this is irrelevant to Usui, because it would not have been a "simple design choice" to implement Usui specifically as a Schottky gate electrode, for numerous reasons. For example, as discussed, Usui's interconnect metallization structure (metal layers 13-15, 18-19) is an

interconnect that provides wiring *between* devices and overlies contact metal 10.

EX-1004 (Usui), 1:11-14 ("The structures fabricated by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure"), 3:23-27, 5:11-65. Moreover, as discussed, Usui does not disclose a transistor in the first place, let alone a transistor *gate* electrode, which Dr. Zhao concedes. EX-2026 (Zhao Dep.), 58:17-60:1. Moreover, Usui's interconnect metallurgy structure (layers 13-15 and 18-19) does not make Schottky contact with Usui's semiconductor wafer 6 because Usui's interconnect metallurgy structure is separated from the semiconductor by insulator 8 – as Dr. Zhao himself appears to recognize. EX-1004 (Usui), 3:23-28, 5:11-33, Fig. 8; Zhao, ¶58; EX-2026 (Zhao Dep.), 123:19-124:3 ("...there are two types of commonly used gate structure, insulated gate *with* a[n] insulating or dielectric layer, or Schottky gate *without* the insulating or dielectric layers" – between which POSAs "*choose*."). In view of above, a POSA understood that modifying Usui to have its interconnect metallization structure somehow make Schottky contact with a transistor channel would have been the furthest thing from a "simple design choice."

Piner (EX-2024)

187. Petitioner and Dr. Zhao also contend that Usui-Yu-Adesida combination is merely “combining prior elements according to known techniques to a known device ready for improvement to yield predictable results.” Petition, 26-27; EX-1002 (Zhao Dec.), ¶133. Again, I do not agree. As an initial matter, there was nothing “known” about using Usui’s stack of metals for a completely unrelated purpose – particularly for something as challenging as a metal-semiconductor junction on a group III-V semiconductor material, when there was no way to predict how that stack would function (or not function) if deposited without modification on a group III-V semiconductor material. EX-1017 (Kramer), which Dr. Zhao relies on, reports that “[f]or the Schottky contacts several different metallization schemes were in use such as Platinum (Pt), Ni, Au and Ni/Au” – none of which are the metals suggested for use in Usui’s interconnect. See EX-1017 (Kramer), 2 (Page 10 of 151); EX-1004 (Usui), 5:11-

59. EX-1017 (Kramer) also indicated that “Schottky contacts should yield a: low reverse current density ($J_s \approx 10^{-5}$ A/cm² at breakdown); high breakdown voltage ($V_{break} > 100$ V); and unity approaching ideality factor (n).” EX-1017, 2 (Kramer), (Page 10 of 151). Dr. Zhao does not contend that Usui’s interconnect structure could meet any of these criteria.

188. I likewise disagree with Petitioner’s and Dr. Zhao’s assertion that Usui’s interconnect structure was “ready for improvement.” Neither Petitioner nor Dr. Zhao explain how Usui’s interconnect structure would have been improved by “implementing the Usui-Yu contact as a Schottky contact,” as alleged. Petition, 26-27; EX-1002 (Zhao Dec.), ¶133. Usui does not disclose a transistor gate electrode, as Dr. Zhao himself admitted. EX-2026 (Zhao Dep.), 58:17-60:1. Since Usui does not disclose a transistor gate electrode and instead discloses an interconnect, it is not clear how Usui’s interconnect could be improved by implementing it as an entirely different component – a Schottky gate electrode.

EX-2024, ¶¶ 187-188

Ground 3 (Claims 11 & 16) Fails: The Modification Would Have Rendered Usui Inoperable

Petition, 24, 26;
POR, 34-36

Piner (EX-2024)

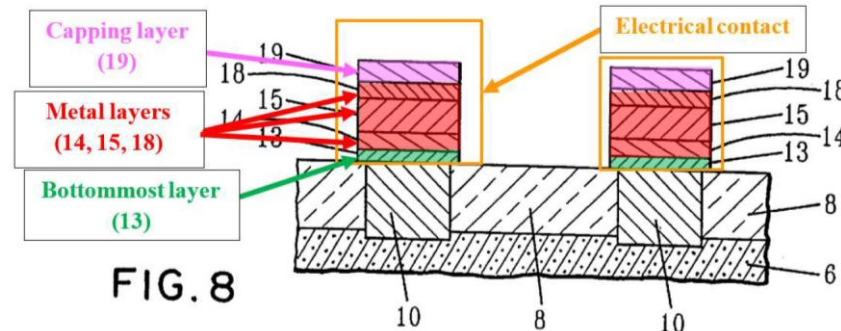
material 6. But a POSA would understand that modifying Usui to have its alleged electrode (layers 13-15 and 18-19) somehow make Schottky contact with semiconductor material 6 would *at minimum* changed Usui's interconnect from operating as an "electrical connection[]" between contact metal 10 and another device, because instead of contacting metal stud 10 where it is pictured in Figure 8 above, Usui's interconnect metallization structure would have to directly contact the semiconductor. See my discussion above in Section VI.B (§§58-61), regarding Schottky contacts, and explaining that a gate electrode making Schottky contact (or Schottky barrier) is designed for a metal-semiconductor interface and does not have an insulating layer between the gate electrode and the semiconductor. EX-1001, 3:31-35; EX-1011 (Mishra), 219; EX-1013 (Quay), 151 (Page 178 of 492); EX-1002 (Zhao Dec.), ¶58.

EX-2024, ¶ 197 (cited at POR, 35)

198. Moreover, if Petitioner's modification involved removing *both* Usui's contact metal 10 and insulating layer 8 entirely – so that Usui's alleged electrode (metal layers 13-15 and 18-19) were simply placed in direct contact with the semiconductor, such that they contacted the semiconductor along their entire length and extent, without any insulator at all – that would also render Usui's device inoperable. A POSA would understand that such a modification would short the portions of the circuit not pictured in EX-1004 (Usui) Figure 8 that were previously isolated by insulating layer 8.

EX-2024, ¶ 198 (cited at POR, 35-36)

Petition



Petition, 11

Petitioner's Reply Tries to Change Ground 3 (for Claims 11 & 16) to Start With Adesida and Add Layers From Usui and Yu

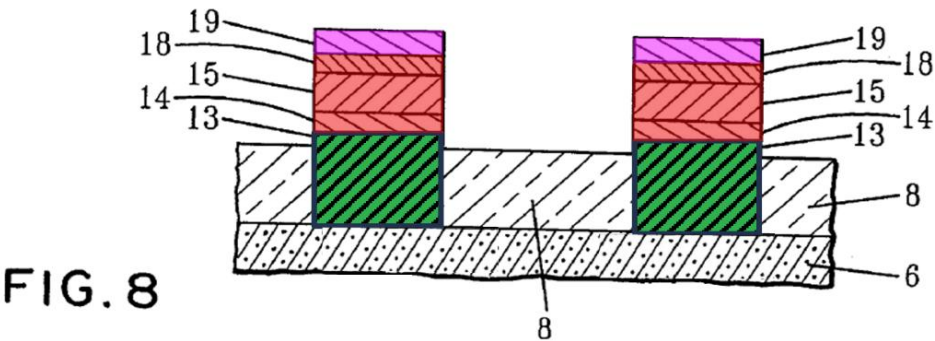
Reply, 20-21;
Sur-Reply, 17-19

Petition

Claims 11 and 16 - A POSITA would have been motivated to implement **Usui's electrical contact as a gate electrode making Schottky contact, as taught by Adesida, with said group III-V semiconductor device as taught by Yu**

Petition, 26

Patent Owner's Response



Usui, Fig. 8 (Modified)

POR, 34

Petitioner's Reply

shown below. POR, 33-34; Ex-2024, ¶193. No such combination is depicted or described in the Petition. Patent Owner's arguments are thus nonresponsive and it

Reply, 21

(emphasis added). Dr. Zhao reiterated this position at his deposition: “So for claim 11 and 16, **we are making Schottky gate structure on III-V semiconductor HEMT device, and we are using the metal layers that taught be Usui and Yu.**” Ex-2026, 191:23-192:1. For claims 9 and 14, a POSTIA would have implemented the

Reply, 20

Patent Owner's Sur-Reply

Zhao's deposition and the Reply (Reply, 20-21) are **too late to explain the combination.** TPG, §II.I. The Reply says the combination is a “Schottky gate structure on III-V semiconductor HEMT *device*” **as taught by Adesida** “with the metal layers taught by Yu and Usui as the gate.” Reply, 20-21. This **new argument that makes Adesida the primary reference should not be considered.** TPG, §II.I.

Sur-Reply, 17

Ground 3 in Petitioner’s Reply (for Claims 11 & 16) Fails: Petitioner Still Does Not Describe Combination

Reply, 20-21;
Sur-Reply, 17-19

Patent Owner’s Sur-Reply

If considered, Petitioner’s new Reply combination fails. Petition again fails to describe the contemplated workings of its Usui-Yu-Adesida combination.

Petitioner says “*metal layers taught by Yu and Usui [are used] as the gate*”

(Reply, 20-21) but *never identifies* which Yu layers and which Usui layers are in

the Usui-Yu-Adesida combination. POR, 32-34. Nor has Petitioner explained

“where those [unidentified] layers... would go in the combination, and what the

thicknesses of the relevant layers would be after the references are combined.”

Piner, ¶190. Petitioner’s failure to explain the “contemplated workings” of the Reply’s new Usui-Yu-Adesida combination is fatal. POR, 32-33 (citing *Personal Web*).

Sur-Reply, 17



PERSONAL WEB TECHNOLOGIES, LLC v. APPLE, INC.

Cite as 848 F.3d 987 (Fed. Cir. 2017)

If the Board’s statement were read more broadly, it would not be adequately explained and grounded in evidence. Indeed, the Board nowhere clearly explained, or cited evidence showing, *how* the combination of the two references was supposed to work. At least in this case, such a clear,

evidence-supported account of the contemplated workings of the combination is a prerequisite to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination and reasonably expect success in doing so.

Personal Web Techs., LLC v. Apple, Inc., 848 F.3d 987, 994 (Fed. Cir. 2017) (cited at POR, 33 & Sur-Reply, 17)

Ground 3 in Petitioner's Reply (for Claims 11 & 16) Fails: Petitioner Still Does Not Identify a Reason to Combine

Reply, 20-21;
Sur-Reply, 17-19

Petitioner's Reply

B. A POSITA Would Have Used Usui's Metallization Stack in Yu's Device to Improve Electromigration

of Yu. *Supra*. Metal and capping layers of Usui and Yu are interchangeable and may be widely applied because the layers are formed from the same type of materials. See Section V.B. Thus a POSTIA would have expected success. *Eli Lilly & Co. v.*

Reply, 20 (citing only itself)

Patent Owner's Sur-Reply

Petitioner also failed to establish any *reason* to combine Usui, Yu, and Adesida in the claimed manner. POR, 28-32. Petitioner says Infineon “misunderst[ood] the interchangeability of *such* materials” but never even explains what Yu and Usui materials were allegedly “interchangeab[le],” let alone provide *evidence* proving interchangeability. Reply, 21-22.

Sur-Reply, 17-18

Ground 3 in Petitioner's Reply (for Claims 11 & 16) Fails: Yu Is Missing

Reply, 20-21;
Sur-Reply, 17-19

Patent Owner's Sur-Reply

Petitioner's assertion that POSAs "would have recognized the benefits of Usui's electromigration protections in Yu's system, as discussed for Ground 2" (Reply, 21-22) fails for the reason discussed *supra* §II.A.2.c. That argument also fails because Petitioner never identifies what aspect of "Yu's system" is even present in the Usui-Yu-Adesida combination. Yu discloses a Complementary Metal **Oxide** Semiconductor ("CMOS") transistor (Yu, title) where the oxide insulates the gate electrode. Yu, [0028], Fig. 2E. POSAs never would have eliminated the insulator from Yu's gates electrodes to make Schottky contact.

Sur-Reply, 18

⁵ Petitioner's assertion that POSAs would have eliminated Yu's gate insulator fails because Yu's entire disclosure is about improving CMOS transistors by using a high-K gate insulator. Yu, Abstract, [0004]-[0006].

Sur-Reply, 19

Yu (EX-1005)

(54) **STRUCTURE AND METHOD FOR A CMOS DEVICE WITH DOPED CONDUCTING METAL OXIDE AS THE GATE ELECTRODE**

Yu (EX-1005), Title

[0004] During the scaling trend, various materials have been implemented for the gate electrode and gate dielectric for CMOS devices. CMOS devices have typically been formed with a gate oxide and polysilicon gate electrode. There has been a desire to replace the gate oxide and polysilicon gate electrode with a high-k gate dielectric and metal gate electrode to improve device performance as feature sizes continue to decrease. Current processing utilizes metal, metal carbide, and/or metal nitride for the gate electrode. However, such materials provide insufficient work function values and present thermal stability issues, particularly when utilized in an n-type MOS device (NMOS) and a p-type MOS device (PMOS), which require different work functions for their respective gate electrode.

[0005] Accordingly, what is needed is a semiconductor device that addresses the above stated issues, and a method for making such semiconductor device.

Yu (EX-1005), [0004]-[0005]

Ground 3 (Claims 9 & 14) Fails: The Petition's Electromigration Motivation Fails

Petition, 25;
POR, 36

'562 Patent

9. The electrical contact of claim 8, wherein said group III-V semiconductor device comprises a high electron mobility transistor (HEMT).

EX-1001, Claim 9; see also EX-1001, claim 14

Petition

Usui discloses the importance of enhanced electromigration. Usui, Abstract. A POSITA would have been motivated to implement the electrical contacts as taught by Usui and Yu in group III-V semiconductor HEMT, as taught by Adesida, because group III-V material HEMTs were well-known at the time for providing relatively high carrier mobility (Zhao ¶51) and thus enhanced electromigration and both Yu and Adesida are directed towards the use of III-V semiconductor devices.

Petition, 25

Patent Owner's Response

Petition, 25. Petitioner misunderstands electromigration; Usui teaches that it should be mitigated – not “*enhanced*.” *Infra* §IV.D.2; Piner, ¶¶199-202.

Petitioner's alleged motivation for making the combination fails.

POR, 36

Ground 3 (Claims 9 & 14) Fails: Changing Yu’s CMOS Into an HEMT Was Not Simple

Petition

Furthermore, it was well-known at the time that including the Usui-Yu device on a HEMT, as taught by Adesida, and constituted a simple design choice depending on the application of the device (e.g., high power and/or high frequency applications)—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int’l Co.*, at 416-17; Zhao ¶¶48-54, 131.

Petition, 25

Patent Owner’s Response

Petitioner’s “*simple design choice*” rationale fails because Petitioner ignores that Usui does not disclose a transistor and because there would have been substantial complexities in *changing the transistor type* from Yu’s transistor to a HEMT. Piner, ¶¶56-59, 203-204. Petitioner fails to establish there would have been no change to the functions of Usui-Yu’s metal layers. Piner, ¶205. That is fatal because Petitioner’s invoked *KSR* rationale only applies when prior art elements are combined “with no change in their respective functions.” *KSR*, 550

POR, 36

Piner (EX-2024)

electrical contact in a group III-V semiconductor HEMT. Moreover, as I discussed previously in Section VI.B (¶¶58-61), there was nothing simple about *changing the type of transistor* associated with gate contact from Yu’s transistor to a HEMT. The design of electrical contacts in a group III-V semiconductor HEMT was – and remains – a challenging area of research because there is no verified way to predict how particular combinations of materials will perform when implemented in such devices without significant experimentation. See, e.g., EX-1017 (Kramer), 79

EX-2024, ¶ 203

- **Ground 4**
 - The Petition did not explain contemplated workings of Usui-Yu-Sugimoto
 - The Petition badly misunderstood electromigration and otherwise failed to establish motivation to modify Usui based on Yu and Sugimoto
 - No reasonable expectation of success
 - The Petition did not show that Usui's layers, after being modified to include an ohmic contact, would still meet the claims' thickness requirements
 - The Petition did not show Usui could be used unchanged to form an ohmic contact
 - The Reply's attempts to change the combination should be rejected
 - No explanation of the contemplated workings of the Reply's Usui-Yu-Sugimoto combination
 - The Reply's discussion of the benefits of ohmic contacts does not establish any reason to use Usui's metal stack as an ohmic contact
 - The Reply offers no alternative motivation-to-combine

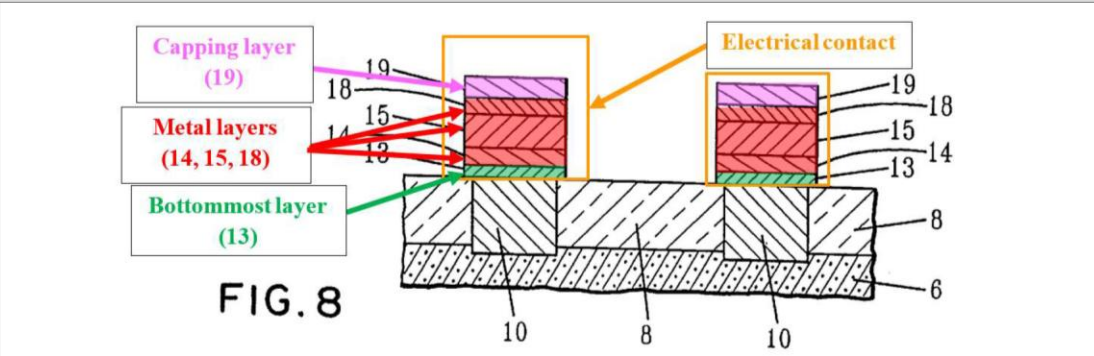
Ground 4 Fails: No Explanation of Contemplated Workings of Combination

Petition, 29-33;
POR, 37-39

Petition

A POSITA would have been motivated to implement the contact of Usui-Yu as a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide improved current flow (i.e., enhanced electromigration) and Sugimoto, like Yu, also teaches the use of III-V semiconductor devices. Furthermore, such a combination is the result of combining

Petition, 31



Petition, 11

'562 Patent

10. The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.

EX-1001, Claim 10; see also EX-1001, claim 15



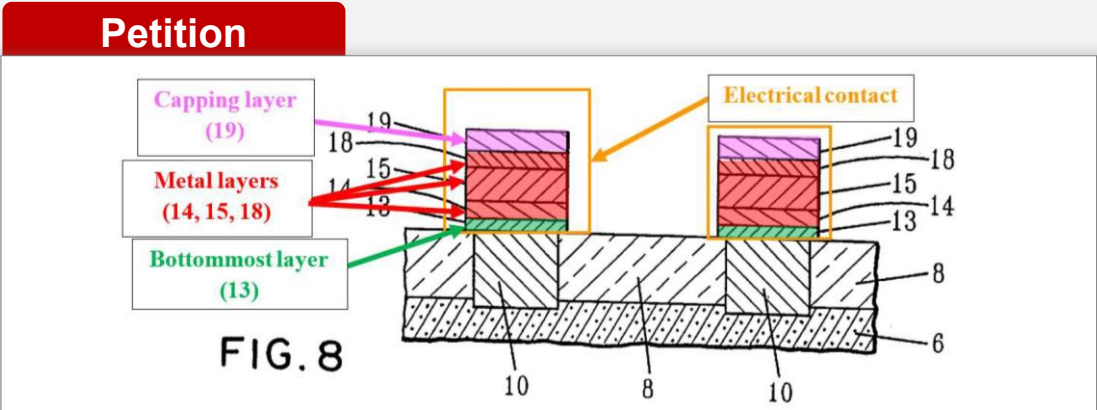
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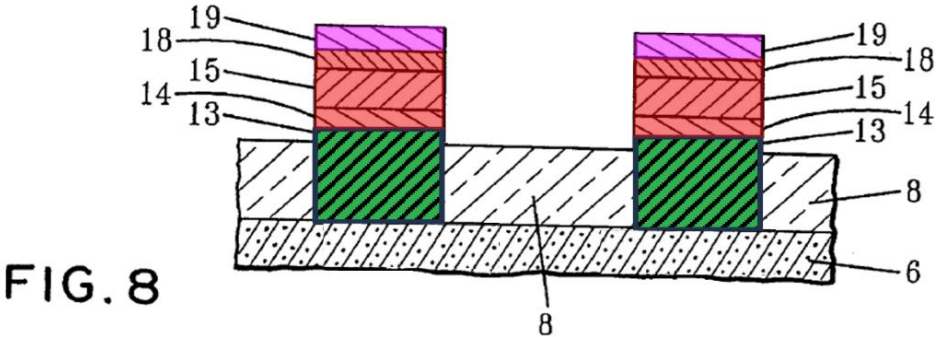
Personal Web Techs., LLC v. Apple, Inc., 848 F.3d 987, 994 (Fed. Cir. 2017) (cited at POR, 37)



Petition, 11

Patent Owner's Response

To the extent Petitioner suggests that Usui's bottommost layer 13 would be made thicker, as shown below, to extend through insulator 8 and reach semiconductor 6 to make ohmic contact, that would not meet any claim challenged in Ground 4 because it would not meet either independent claim (claim 1 or 13) from which those claims depend. Piner, ¶213.



Usui, Fig. 8 (Modified)

POR, 38

Ground 4 Fails: The Petition's Motivation to Combine Was Based On Conflating Current Flow and Electromigration

Petition, 31;
POR, 40

Petition

A POSITA would have been motivated to implement the contact of Usui-Yu as a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide improved current flow (i.e., enhanced electromigration) and Sugimoto, like Yu, also teaches the use of III-V semiconductor devices. Furthermore, such a combination is the result of combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, at 416-17; *Adesida*, [0031], Fig. 5; Zhao ¶¶51-57, 144.

Petition, 31

Patent Owner's Response

Petitioner badly misunderstands “electromigration.” Electromigration does not refer to “current flow” as Petitioner suggests via its parenthetical equating the terms. *Id.* Both experts agree that electromigration refers to electron-flow-induced movement of *metal atoms* in a conductor which can cause reliability and performance issues for the conductor. Piner, ¶¶215-218 (citing EX-2029, EX-2030, EX-2031), 66-67, 99-101; Zhao-Dep., 13:23-14:9, 53:18-54:25; Usui, 1:30-41 (“Migration of *aluminum atoms* into the underlying silicon can interfere with the performance and reliability of the resulting integrated circuit...”).

POR, 40

Petition

A POSITA would have been motivated to implement the contact of Usui-Yu as a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide improved current flow (i.e., enhanced electromigration) and Sugimoto, like Yu, also teaches the use of III-V semiconductor devices. Furthermore, such a combination is the result of combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, at 416-17; *Adesida*, [0031], Fig. 5; Zhao ¶¶51-57, 144.

Petition, 31

Patent Owner's Response

Petitioner never even explains what device in Ground 4's combination was allegedly "ready for improvement." Petitioner never establishes that Ground 4's modification would have improved *Sugimoto* because Petitioner fails to establish that Sugimoto's electrode suffers from electromigration that would be solved using Usui's techniques. Piner, ¶222. And Petitioner never explains how *Usui* would have been improved by "implement[ing] the contact of Usui-Yu as a power electrode" (Petition, 31) given that Usui does not disclose any device having a power electrode. Piner, ¶223. Petitioner's combination does not "improve" Usui – it *changes* the function of Usui's metal layer stack to serve as a power electrode rather than as wiring that is part of an "interconnect circuit" connecting devices in a semiconductor circuit. *Id.*; Usui, 1:5-12, 4:10-15. Because the functions of the components are changed in Petitioner's combination, the *KSR* rationale Petitioner invokes does not apply.

POR, 41-42

Ground 4 Fails: No Reasonable Expectation of Success

Petition, 31;
POR, 42-43

Patent Owner's Response

For the same reasons discussed *supra* §IV.D.1, Petitioner fails to establish a reasonable expectation of success in modifying Usui, based on Yu and Sugimoto, so that Usui's alleged electrode (layers 13-15 and 18-19) has a capping layer with "a thickness greater than that of a bottommost layer of said plurality of metal layers" of the electrical contact, as required by Limitations [1c] and [13c], despite

To the extent Petitioner suggests that Usui-Yu's alleged electrical contact could be used unchanged to form an ohmic contact, no evidence supports that. POSAs understood this would require significant changes to the layers – in their materials and thicknesses – because ohmic contacts are closely tailored to the semiconductor, like a lock and key. Piner, ¶¶226-228, 48-57. Petitioner fails to account for these changes, and fails to show that the alleged electrical contact of Usui-Yu-Sugimoto would meet claims 1 and 13 after making the necessary changes. Piner, ¶227.

POR, 42-43

Piner (EX-2024)

226. To the extent Dr. Zhao suggests that Usui-Yu's alleged electrical contact could simply be used *without any changes* to form an ohmic contact on a semiconductor, no evidence supports that notion. Dr. Zhao trivializes a complex field. As I discuss in Section VI.A, the way in which particular materials would interact in the context of a metal-semiconductor junction was difficult to predict. As one reference put it, fabrication of ohmic contacts was "still more art than science." EX-1017 (Kramer), 31 (Page 38 of 151); *see also* EX-1017 (Kramer), 51 (Page 58 of 151) ("Literature shows that the actual mechanism of Ohmic contact formation is still subject of discussion and yet to be understood."). This is because, for example, "[i]f a metal is placed into contact with such a semiconductor, the physics of the junction are not governed by the bulk properties of the metal and semiconductor material but by the properties of the surface boundaries and primarily those of the semiconductor surface." EX-1017 (Kramer), 12 (Page 19 of

EX-2024, ¶ 226

Ground 4 in Petitioner’s Reply Fails: Petitioner Again Tries to Change Combination But Does Not Describe It

Reply, 22-24;
Sur-Reply, 19-21

Patent Owner’s Sur-Reply

Petitioner again criticizes Infineon’s understanding of the combination and then seeks to change the *Petition’s* Ground 4 combination through expert deposition testimony. Reply, 22-23. That fails for the same reasons discussed *supra* §II.B.1.

Sur-Reply, 19

Petitioner does not identify what Yu “metal layers” are used in the combination, what Usui “metal layers” are used in the combination, and how they are used together. Even after Reply, Petitioner provides “no details regarding which layers... from which references (Usui, Yu, and Sugimoto) are incorporated into Petitioner’s combination, where those layers... would go in the combination, and what the thicknesses of the relevant layers would be after the references are combined.” Piner, ¶209. That is fatal to Ground 4. POR, 39 (*Personal Web* requires an explanation of the contemplated workings of the combination).

Sur-Reply, 20

Petitioner’s Reply

improve currently flow. *Petition*, 31. Dr Zhao confirmed: “for ground 4, we are using Usui and Yu’s teaching of those metal layers to form ohmic contact, and that ohmic contact will serve a power electrode on a III-V semiconductor device, as laid out in Sugimoto,” which “is a HEMT” with ohmic source and drain electrodes. *Ex-2026*,

Reply, 22-23



PERSONAL WEB TECHNOLOGIES, LLC v. APPLE, INC.

Cite as 848 F.3d 987 (Fed. Cir. 2017)

If the Board’s statement were read more broadly, it would not be adequately explained and grounded in evidence. Indeed, the Board nowhere clearly explained, or cited evidence showing, *how* the combination of the two references was supposed to work. At least in this case, such a clear,

evidence-supported account of the contemplated workings of the combination is a prerequisite to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination and reasonably expect success in doing so.

Personal Web Techs., LLC v. Apple, Inc., 848 F.3d 987, 994 (Fed. Cir. 2017) (cited at POR, 37)

Ground 4 in Petitioner's Reply Fails: Petitioner Still Does Not Identify Reason to Combine

Reply, 22-24;
Sur-Reply, 20-21

Patent Owner's Sur-Reply

a motivation to combine fails. POR, 39-42. Petitioner fails to meet the factual predicate for *KSR*'s "known elements" rationale (Petition, 31) that there is no change in the function of any of the combined elements. POR, 41-42. Indeed, the combination changes the function of Usui's metal stack from being used for an interconnect to being an electrode making ohmic contact to create a transistor power electrode. *Id.* Lauding the benefits of ohmic contacts (Reply, 23-24) does not help Petitioner because it establishes no reason to use *Usui's* metal stack (modified in some unexplained way by Yu's *gate* electrode stack) as an ohmic contact.

Sur-Reply, 20

The Petition's only other motivation-to-combine argument says the combination provides "improved current flow (*i.e.*, enhanced electromigration)." Petition, 31. The Reply does not refute that enhanced electromigration is not the same thing as "improved current flow." POR, 39-41. The Petition's motivation-to-combine argument fails and the Reply offers no alternative motivation-to-combine argument for Ground 4.

Sur-Reply, 21

- **The Board correctly found that Petitioner failed to establish reason to implement Yu's layers with the claimed relative thicknesses when formed from the materials Petitioner relied on**
 - Petitioner fails to support alleged thickness for a refractory metal nitride capping layer
 - Yu does not say the same thickness used for polysilicon is used for a refractory metal nitride
 - Usui does not teach making Yu's refractory metal nitride capping layer thicker than Yu's barrier layer
 - Petitioner did not establish thickness of a titanium bottommost layer
- **Petitioner failed to establish Yu's barrier layer is part of Yu's electrode**

Grounds 5-7: Petitioner Failed to Explain POSA's Motivation for Choosing the Claimed Layer Thicknesses When Using the Materials Selected by the Petitioner

Institution, 18-19

Institution Decision

Based on the current record, we find that Patent Owner's arguments regarding the "said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers" limitation of claim 1 have merit. Petitioner does not adequately explain why a POSITA would have replaced Yu's polysilicon capping layer with a titanium nitride or tantalum nitride layer *with the same thickness* as the polysilicon layer. Petitioner points to Dr. Zhao's testimony with respect to the benefits of using refractory metal nitrides in general, and of refractory metal nitride capping layers in particular, but this testimony does not address the thickness of the beneficial refractory metal nitride capping layers.⁷ Pet. 38 (citing Ex. 1002 ¶¶ 71–73). And Dr. Zhao's testimony that a titanium nitride or tantalum nitride capping layer in Yu would have the same thickness as Yu's polysilicon capping layer mirrors the statements in the Petition without providing further technical explanation or additional evidence in support thereof. Ex. 1002 ¶ 155; *see also Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential) (expert declaration that "merely repeats, *verbatim*, the conclusory assertion for which it is offered to support" is entitled to little weight).

Petitioner alternatively argues that Usui would have motivated a POSITA "to apply known techniques of limiting the thickness of Usui underlayer 13 (bottommost metal layer) to diffusion barrier/protection layer 218 (bottommost layer) in Yu's known device." Pet. 39. Petitioner does not explain, on this record, why limiting the thickness of Yu's diffusion barrier/protection layer 218 would result in a titanium nitride or tantalum nitride capping layer 226 in Yu having a greater thickness than diffusion barrier/protection layer 218 if the thickness of the titanium nitride or tantalum nitride capping layer is not known.

We invite the parties to develop these arguments further at trial, to the extent permitted under our rules.

Institution, 18-19

The Claims Require a Refractory Metal Nitride Capping Layer That Is Thicker Than a Bottommost Metal Layer

Petition, 43;
POR, 55

'562 Patent

1. An electrical contact for use on a semiconductor device, said electrical contact comprising:
an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;
said capping layer consisting only of a refractory metal nitride, said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

EX-1001, Claim 1

Petition

[1c]: said refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers.

Petition, 43

Yu Undisputedly Does Not Disclose Thickness Requirement of Element [1C]

Petition, 36, 38;
Reply, 27

Petition

Yu's device also includes **capping layer 226** (**capping layer**) is preferably 600Å and **diffusion barrier/protection layer 218** (**bottommost layer**) is preferably 20Å (i.e., the **capping layer** is *preferably* thicker than the **bottommost layer**). This disclosure is made with respect to the **capping layer** being polysilicon (Yu, [0036], [0040]), which is not a **refractory metal nitride** as is stated in claims 1 and 13. However, Yu teaches the **capping layer** may be titanium nitride and tantalum nitride, which are **refractory metal nitrides**. Zhao ¶152.

Petition, 36

Yu expressly discloses every element of claims 1 and 13 except a **refractory metal nitride capping layer** having a thickness greater than that of a **bottommost layer** (claim element [1c]). While Yu discloses the **capping layer** is *preferably*

Petition, 38

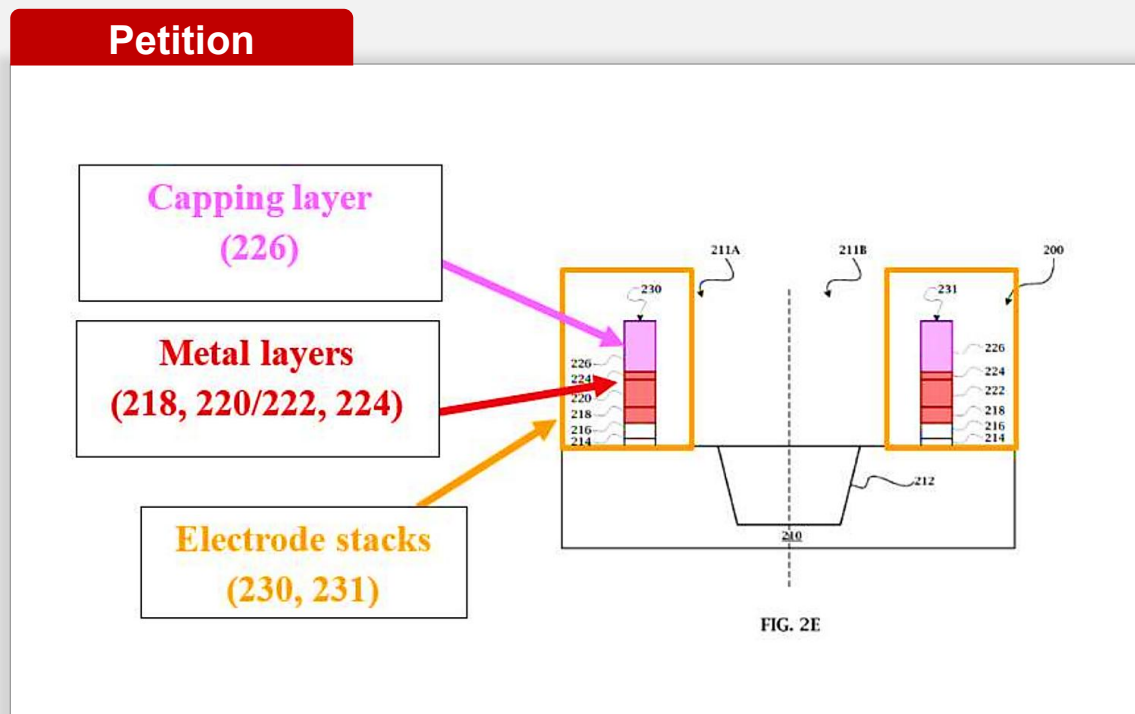
Petitioner's Reply

While Yu does not expressly disclose the claimed thickness of [1.C], it renders it obvious. Petition, 33-55 (citing Yu, [0036]); Ex-1002, 149-187 (same). Barrier layer 218 comprises metals, including TiN, which may have a thickness of 20Å. Petition, 38; Yu, [0029]. This is the claimed bottommost layer. Petition, 43-44.

Reply, 27

The Petition Relies on Yu's Capping Layer 226 and Diffusion Barrier/Protection Layer 218 in Metal Gate Stacks 230 and 231

Petition, 36, 38, 42-43



Petition, 42

Yu (EX-1005)

[0036] At step 110, referring to FIGS. 1 and 2D, a capping layer 226 is formed over the metal layers 220, 222, and in the present embodiment, over the diffusion barrier layer 224. The capping layer 226 may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer 226 comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some

Yu (EX-1005), [0036]

[0029] In some embodiments, a diffusion barrier/protection layer 218 is formed over the high-k dielectric layer 216. The diffusion barrier/protection layer 218 may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present embodiment, the diffusion barrier/protection layer 218 comprises TiN, which is deposited by PVD to a thickness of approximately 20 Å. In alternate embodiments, the diffusion

Yu (EX-1005), [0028]

Patent Owner's Response

Petitioner's assertion that Yu teaches a capping layer 226 that is thicker than its diffusion barrier/protection layer 218 is thus based on thickness values that Yu reports for *different materials for both layers* than are used in Petitioner's Yu-Usui combination. Yu teaches nothing about the thickness of these layers when formed from the materials in Petitioner's Yu-Usui combination. Yu simply does not teach a refractory metal nitride capping layer 226 that is thicker than a titanium diffusion barrier layer 218 as Petitioner alleges. Piner, ¶264.

POR, 63

Yu Never Discloses Thickness of Capping Layer 226 When Formed From TaN or TiN

Petition, 36, 38;
POR, 56-57

Petition

layer (claim element [1c]). While Yu discloses the **capping layer** is *preferably* 600Å and the **bottommost layer** 20Å (i.e., the **capping layer** is *preferably* thicker than the **bottommost layer**), this disclosure is made with respect to the **capping layer** being polysilicon (Yu, [0036], [0040]), which is not a **refractory metal nitride** as is stated in claims 1 and 13. However, Yu teaches the **capping layer** may

Petition, 38; see also Petition, 36

Patent Owner's Response

Yu describes many materials or “combinations thereof” that could form capping layer 226. Yu, [0036]. The Petition seizes on Yu’s disclosure that capping layer 226 can be titanium nitride or tantalum nitride because those are refractory metal nitrides. Petition, 42. But Yu *never* discloses capping layer 226’s thickness when formed from those materials; Petitioner never alleges otherwise.

¹⁵ Yu discloses a different thickness (about 50-1,000 Å and “preferably about 200 Å”) when capping layer 226 is an “aluminum-based, tungsten, or copper material.”

POR, 56-57

Yu (EX-1005)

[0036] At step 110, referring to FIGS. 1 and 2D, a **capping layer 226** is formed over the metal layers 220, 222, and in the present embodiment, over the diffusion barrier layer 224. The capping layer 226 may comprise polycrystalline silicon; silicon-containing materials; germanium-containing materials; metal, such as aluminum, copper, tungsten, titanium, tantalum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide; other proper conductive materials; and combinations thereof. In the present embodiment, the capping layer 226 comprises polysilicon having a thickness between about 200 Å and about 1,000 Å, preferably about 600 Å. In some embodiments, the capping layer 226 may include metal (e.g., an aluminum-based, tungsten, or copper material), which may be used in a gate last-process and comprise a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å. In alternate embodiments, the capping layer 226 may comprise any suitable thickness. The capping layer 226 may

Yu (EX-1005), [0036]

The Petition Says a POSA Would Have Been Motivated to Replace Yu's Polysilicon Capping Layer 226 With TaN or TiN, Using the Same Thickness

Petition, 36, 38, 43-44;
POR, 57-61

Petition

be titanium nitride and tantalum nitride, which are **refractory metal nitrides**. A POSITA would have been motivated to replace Yu's polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed thicknesses because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation as explained by Dr. Zhao. Zhao ¶¶71-73, 155 (citing Ex-1025, 120; Ex-1026, 2; Ex-1028, 46, 56; Ex-1023, 3:39-43; Ex-1024, Abstract, 1:58-61; Ex-1029, Abstract, 1:29-34, 2:47-51).

Petition, 38

[0029], Fig. 2E), which is 20 Å (*id.*, [0029]). As explained in Sections VII.E.2 and VII.E.2.a, a POSITA would have understood these thicknesses apply to Yu's capping and bottommost layer regardless of whether Yu's capping layer is comprised of polysilicon or titanium nitride or tantalum nitride.

Petition, 43

Institution Decision

said plurality of metal layers" limitation of claim 1 have merit. Petitioner does not adequately explain why a POSITA would have replaced Yu's polysilicon capping layer with a titanium nitride or tantalum nitride layer *with the same thickness* as the polysilicon layer. Petitioner points to Dr. Zhao's testimony with respect to the benefits of using refractory metal nitrides in general, and of refractory metal nitride capping layers in particular, but this testimony does not address the thickness of the beneficial refractory metal nitride capping layers.⁷ Pet. 38 (citing Ex. 1002 ¶¶ 71-73). And Dr. Zhao's testimony that a titanium nitride or tantalum nitride capping layer in Yu would have the same thickness as Yu's polysilicon capping layer mirrors the statements in the Petition without providing further technical explanation or additional evidence in support thereof. Ex. 1002 ¶ 155; *see also Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential) (expert declaration that "merely repeats, *verbatim*, the conclusory assertion for which it is offered to support" is entitled to little weight).

Institution, 18-19

Ground 5 Fails Because the Petition's Assertion Regarding Thickness of Capping Layer 226 When Formed From TaN or TiN Is Unsupported

Petition, 38;
POR, 57-61

Petition

Yu expressly discloses every element of claims 1 and 13 except a **refractory metal nitride capping layer** having a thickness greater than that of a **bottommost layer** (claim element [1c]). While Yu discloses the **capping layer** is *preferably* 600Å and the **bottommost layer** 20Å (i.e., the **capping layer** is *preferably* thicker than the **bottommost layer**), this disclosure is made with respect to the **capping layer** being polysilicon (Yu, [0036], [0040]), which is not a **refractory metal nitride** as is stated in claims 1 and 13. However, Yu teaches the **capping layer** may be titanium nitride and tantalum nitride, which are **refractory metal nitrides**. A POSITA would have been motivated to replace Yu's polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed thicknesses because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation as explained by Dr. Zhao. Zhao ¶¶71-73, 155 (citing Ex-1025, 120; Ex-1026, 2; Ex-1028, 46, 56; Ex-1023, 3:39-43; Ex-1024, Abstract, 1:58-61; Ex-1029, Abstract, 1:29-34, 2:47-51).

Petition, 38

Zhao Dec. (EX-1002)

155. Yu expressly discloses every element of claims 1 and 13 except a **refractory metal nitride capping layer** having a thickness greater than that of a **bottommost layer** (claim element [1c]). While Yu discloses the **capping layer** is *preferably* 600Å and the **bottommost layer** 20Å (i.e., the **capping layer** is *preferably* thicker than the **bottommost layer**), this disclosure is made with respect to the **capping layer** being polysilicon (Yu, [0036], [0040]), which is not a **refractory metal nitride** as is stated in claims 1 and 13. However, Yu teaches the **capping layer** may be titanium nitride and tantalum nitride, which are **refractory metal nitrides**. A POSITA would have been motivated to replace Yu's polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed thicknesses because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternation as I explained in Section VI.G.

EX-1002, ¶ 155

Petitioner's Expert Offers No Testimony Regarding Thickness of Capping Layer 226 When Formed From TaN or TiN

Petition, 38;
POR, 57-61

Zhao Dec. (EX-1002)

G. Refractory Metal Nitrides

71. Refractory metals are a class of metals that were known for resistance to heat and wear by the time of the alleged invention (August 25, 2009). Ex-1025, 120. The most common definition of refractory metals were metals comprising a melting point above 2,204°C, such as niobium, molybdenum, tantalum, tungsten and rhenium. *Id.* A wider definition of refractory metals included metals such as titanium. Ex-1027, 1.

72. By August 25, 2009, refractory metals had been known to be chemically bound with nitrogen to form refractory metal nitrides, such as TiN and TaN. Ex-1026, 2. Titanium nitride and tantalum nitride were well-known and widely used refractory metal nitrides (Ex-1026, 2) which possess a combination of useful mechanical and chemical properties such as hardness and heat resistance (Ex-1036, 156-157, 160). By August 2009, it was common and well-known to use titanium nitride as a diffusion barrier, conducting electrode, and antireflection coating layer in interconnect stacks due to its good thermal and mechanical properties and low

resistivity. Ex-1028, 46. By August 25, 2009, it was common and well-known to use tantalum nitride in interconnect structures (e.g., as a diffusion barrier) due to its high thermal, mechanical, and chemical stability. Ex-1028, 56. It was well-known that titanium nitride and tantalum nitride could be used interchangeably as a diffusion barrier in semiconductor devices. Ex-1026, 2; Ex-1023, 3:39-43; Ex-1024, Abstract, 1:58-61.

73. By August 25, 2009, it was also well-known that refractory metal nitride capping layers are effective for reducing metal electromigration and diffusion, such as copper electromigration and copper diffusion. Ex-1029, Abstract. It was well-known that metals, such as copper, can readily diffuse into surrounding materials, leading to line-to-line leakages and eventual device failure. Ex-1029, 1:29-34. Refractory metal nitride capping layers were known to be effective in preventing copper electromigration and diffusion in semiconductor devices. Ex-1029, 2:47-51.

EX-1002, ¶¶ 71-73

Petitioner Introduces New “Suitable Choice” Argument in Petitioner’s Reply

Reply, 28;
Sur-Reply, 23

Petitioner’s Reply

165:23. It would have been obvious that the capping layer would have had a thickness of 600. Pet, 33-55; Ex-2026, 46:19-47:25 (discussing this passage), 164:23-165:23 (same).

Yu provides the exact rational the Board questioned: whether a POSITA would have replaced the polysilicon cap with TiN or TaN at 600Å thick. Paper 10, 17-19. Yu’s metal based capping layer is thicker than the bottommost metal layer (20Å) for the *entire range* 50-1,000Å. A polysilicon thickness of 600Å would have been a suitable choice for a capping layer *including metal*. Ex-2026, 47:1-25, 144:11-145:2, 161:16-162:3, 165:1-20, 168: 14-21.

Reply, 28

Institution Decision

We invite the parties to develop these arguments further at trial, to the extent permitted under our rules.

Institution, 19

Patent Owner’s Sur-Reply

The only proper Reply would have been to demonstrate where the *Petition* provided evidence and argument supporting its assertion that “these [same] thicknesses apply.” *Petition*, 43. That was required to establish *prima facie* obviousness. Petitioner cannot present new argument and evidence in Reply in an attempt to belatedly establish *prima facie* obviousness. TPG, §II.I; *Wasica*, 853 F.3d at 1286-87 (changing arguments in Reply after the *Petition*’s argument is shown to fail is “foreclosed by statute, our precedent, and Board guidelines”). The

Sur-Reply, 23



Trial Practice Guide § II.I

petitioner's reply. Petitioner may not submit new evidence or argument in reply that it could have presented earlier, e.g. to make out a prima facie case of unpatentability. A party also may submit



WASICA FINANCE GMBH v. CONTINENTAL AUTO. SYSTEMS

Cite as 853 F.3d 1272 (Fed. Cir. 2017)

Continental Response Br. 49–59. Rather than explaining how its original petition was correct, Continental's subsequent arguments amount to an entirely new theory of *prima facie* obviousness absent from the petition. Shifting arguments in this fashion is foreclosed by statute, our precedent, and Board guidelines. See 35 U.S.C. § 312(a)(3) (requiring petitions to identify “with particularity . . . the grounds on which the challenge to each claim is

based”); *Illumina*, 821 F.3d at 1369–70; *Dell Inc. v. Acceleron, LLC*, 818 F.3d 1293, 1301 (Fed. Cir. 2016) (vacating a finding of unpatentability when the Board relied on an argument first made during oral hearing); *Trial Practice Guide*, 77 Fed. Reg. 48,756, 48,767 (Aug. 14, 2012) (prohibiting parties from submitting evidence necessary for a *prima facie* showing of obviousness in a reply). We therefore see no error in the Board declining to engage such an argument here.

Wasica Finance GmbH v. Cont'l Auto. Sys., 853 F.3d 1272, 1286–87 (Fed. Cir. 2017) (cited at Sur-Reply, 23)

Ground 5 in Petitioner's Reply Fails Because Petitioner Provides No Explanation of Why 600Å Is a "Suitable" Thickness for TiN or TaN

Reply, 28;
Sur-Reply, 24

Petitioner's Reply

165:23. It would have been obvious that the capping layer would have had a thickness of 600. Pet, 33-55; Ex-2026, 46:19-47:25 (discussing this passage), 164:23-165:23 (same).

Yu provides the exact rationale the Board questioned: whether a POSITA would have replaced the polysilicon cap with TiN or TaN at 600Å thick. Paper 10, 17-19. Yu's metal based capping layer is thicker than the bottommost metal layer (20Å) for the *entire range* 50-1,000Å. A polysilicon thickness of 600Å would have been a suitable choice for a capping layer *including metal*. Ex-2026, 47:1-25, 144:11-145:2, 161:16-162:3, 165:1-20, 168: 14-21.

Reply, 28

Patent Owner's Sur-Reply

Petitioner does not dispute that Yu says its preferred capping layer thickness varies for different materials and never discloses a capping layer thickness for the refractory metal nitrides Petitioner relies upon. POR, 56; Yu, [0036]. That is fatal to the Petition's argument that "these [same] thicknesses apply." Petition, 43.

The Reply newly alleges that Yu's disclosure of a range of thickness for some metals "includes 600Å" – the preferred polysilicon thickness. Based on this, the Reply states in conclusory fashion that "it would have been obvious that the capping layer would have had a thickness of 600" which is "suitable" for a refractory metal nitride capping layer. Reply, 28. This new argument should not be considered. If considered, this argument fails because the Reply never even attempts to explain how or why 600Å is a "suitable" or "obvious" thickness for a refractory metal nitride capping layer and no such explanation can be incorporated by reference from Zhao's deposition testimony. 37 C.F.R. §42.6(a)(3). Moreover, Zhao's deposition testimony is uncorroborated and warrants no weight. No *credible evidence* supports the Reply's new argument.

Sur-Reply, 24

Ground 5 in Petitioner's Reply Fails Because Dr. Zhao's Uncorroborated Deposition Testimony Warrants No Weight

Reply, 28;
Sur-Reply, 24

Zhao Dep. (EX-2026)

A. Okay. So let me give you an example from the reference -- from the Yu's reference, Yu's reference number -- paragraph 36 renders it very obvious that the claim 1C is very obvious, because in paragraph 36 of the Yu, it discuss, for example, the capping layer of, of, of this metal layers, and this shows that this capping layer could be a metal. And it provides examples, including titanium.

EX-2026, 47:1-19; see also 144:11-145:2, 161:16-162:3, 165:1-20, 168:14-21

And while not expressing, a POSITA at the time would have understood that these metal layers refer to the list of refractory metal nitrides also in paragraph 36 of Yu, which include titanium nitride, TIN, and tantalum nitride, TAN. So it's -- and later on, in my declaration as well as in paragraph 36 of Yu, it provides thickness, including 600 Angstrom, which is in my declaration, and 200 Angstrom preferably. This, this also in the, in the Yu renders 1C obvious. Although it is all that takes, I further -- all that takes that Yu alone renders 1C obvious.

Ground 5 Also Fails Because Usui Would Not Have Motivated POSAs to Make Yu's Refractory Metal Nitride Capping Layer Thicker Than Yu's Barrier Layer

Petition, 38-39;
POR, 63-68

Petition

does. As Usui recognizes, “by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention.” Usui, 3:29-37. This benefit of limiting the bottommost metal layer of an electrode stack was well-known by August 2009, as explained by Dr. Zhao. Zhao ¶¶70, 156 (citing Ex-1022, Abstract; Ex-1023, 3:33-37; Ex-1024,

A POSITA would have been motivated to apply known techniques of limiting the thickness of Usui **underlayer 13 (bottommost metal layer)** to **diffusion barrier/protection layer 218 (bottommost layer)** in Yu's known device ready for improvement to yield predictable results and would have expected success because limiting the thickness of the bottommost metal layer had known benefits and was known in the art—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 401, 416-17; Zhao ¶¶66-67, 70, 158.

Petition, 38-39

Institution Decision

Petitioner alternatively argues that Usui would have motivated a POSITA “to apply known techniques of limiting the thickness of Usui underlayer 13 (bottommost metal layer) to diffusion barrier/protection layer 218 (bottommost layer) in Yu's known device.” Pet. 39. Petitioner does not explain, on this record, why limiting the thickness of Yu's diffusion barrier/protection layer 218 would result in a titanium nitride or tantalum nitride capping layer 226 in Yu having a greater thickness than diffusion barrier/protection layer 218 if the thickness of the titanium nitride or tantalum nitride capping layer is not known.

We invite the parties to develop these arguments further at trial, to the extent permitted under our rules.

Institution, 18-19

Ground 5 Also Fails Because Usui Would Not Have Motivated POSAs to Make Yu's Refractory Metal Nitride Capping Layer Thicker Than Yu's Barrier Layer

Petition, 38-39;
POR, 63-68

Petition

does. As Usui recognizes, “by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention.” Usui, 3:29-37. This benefit of limiting the bottommost metal layer of an electrode stack was well-known by August 2009, as explained by Dr. Zhao. Zhao ¶¶70, 156 (citing Ex-1022, Abstract; Ex-1023, 3:33-37; Ex-1024,

A POSITA would have been motivated to apply known techniques of limiting the thickness of Usui **underlayer 13 (bottommost metal layer)** to **diffusion barrier/protection layer 218 (bottommost layer)** in Yu's known device ready for improvement to yield predictable results and would have expected success because limiting the thickness of the bottommost metal layer had known benefits and was known in the art—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 401, 416-17; Zhao ¶¶66-67, 70, 158.

Petition, 38-39

Patent Owner's Response

A Capping Layer Thicker than the Bottommost Layer of the Electrode Stack's Metal Layers is a Missing Limitation Not Taught by Yu or Usui

POR, 63-65

Usui's Interconnect Metallurgy Structure Would Not Have Motivated Any Change to Yu's CMOS Gate Electrode

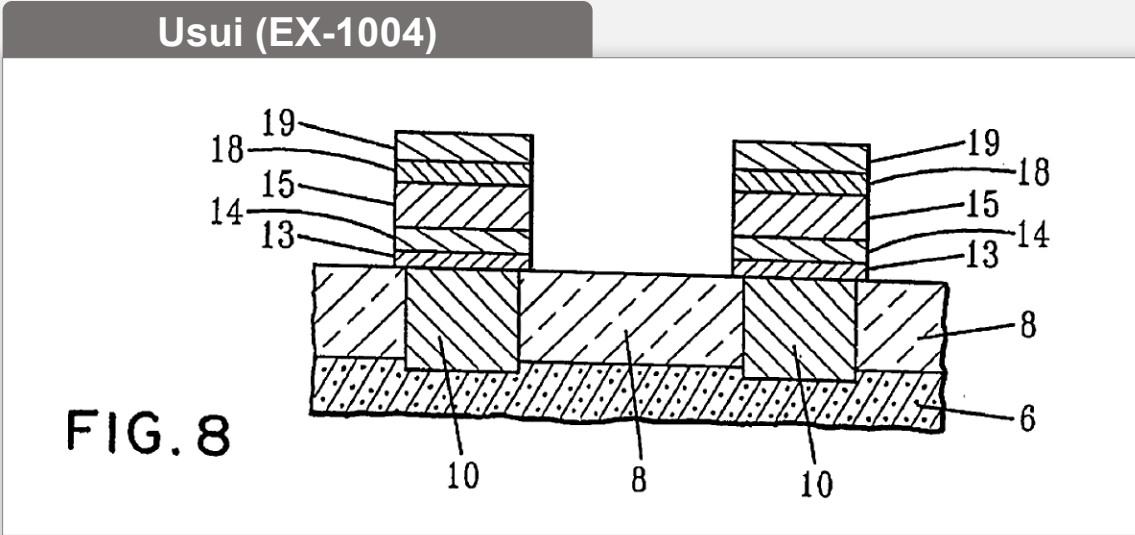
POR, 65-67

Petitioner's Reliance on *KSR*'s Known Techniques/Predictable Results Rationale Fails

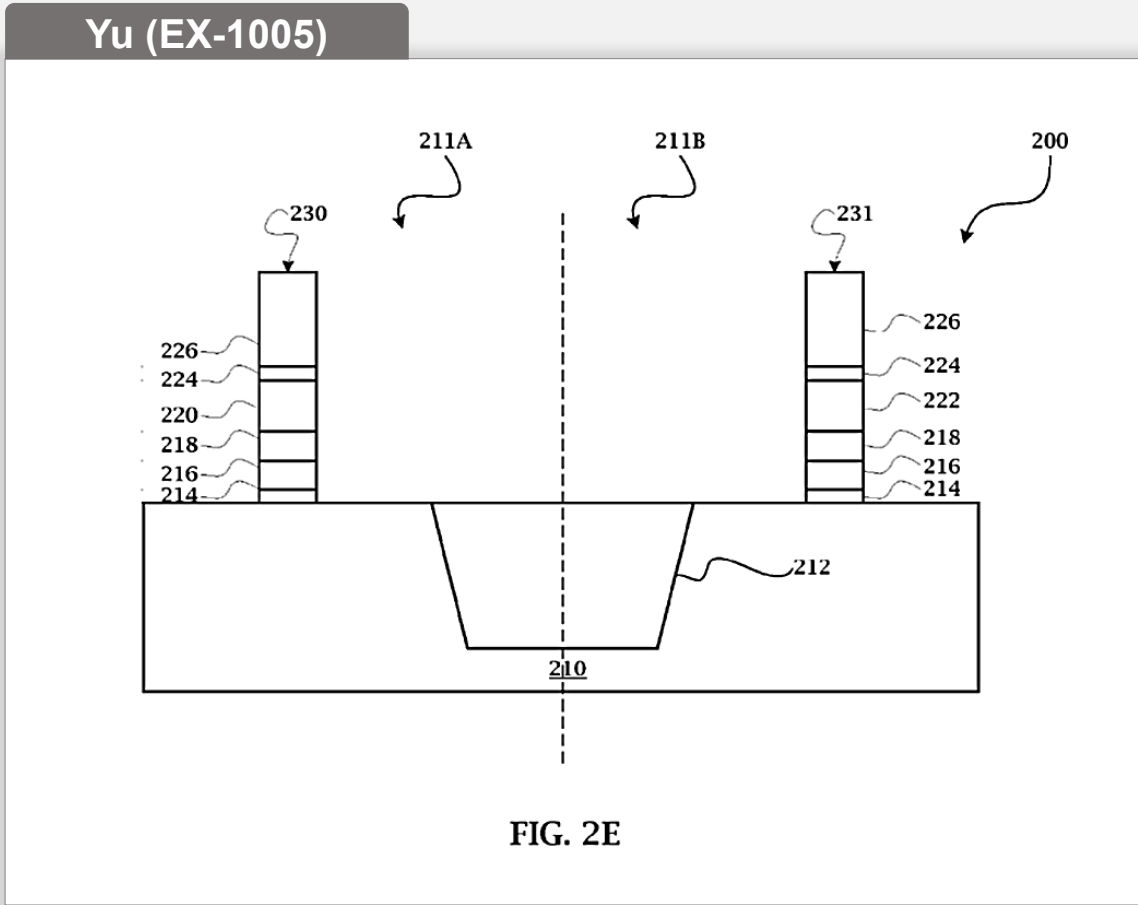
POR, 67-68

Ground 5 Also Fails Because the Petition’s *KSR* Rationale Does Not Apply: Usui’s Underlayer 13 Has a Different Function Than Yu’s Diffusion Barrier Layer 218

POR, 67-68



Usui (EX-1004), FIG. 8



Yu (EX-1005), FIG. 2E

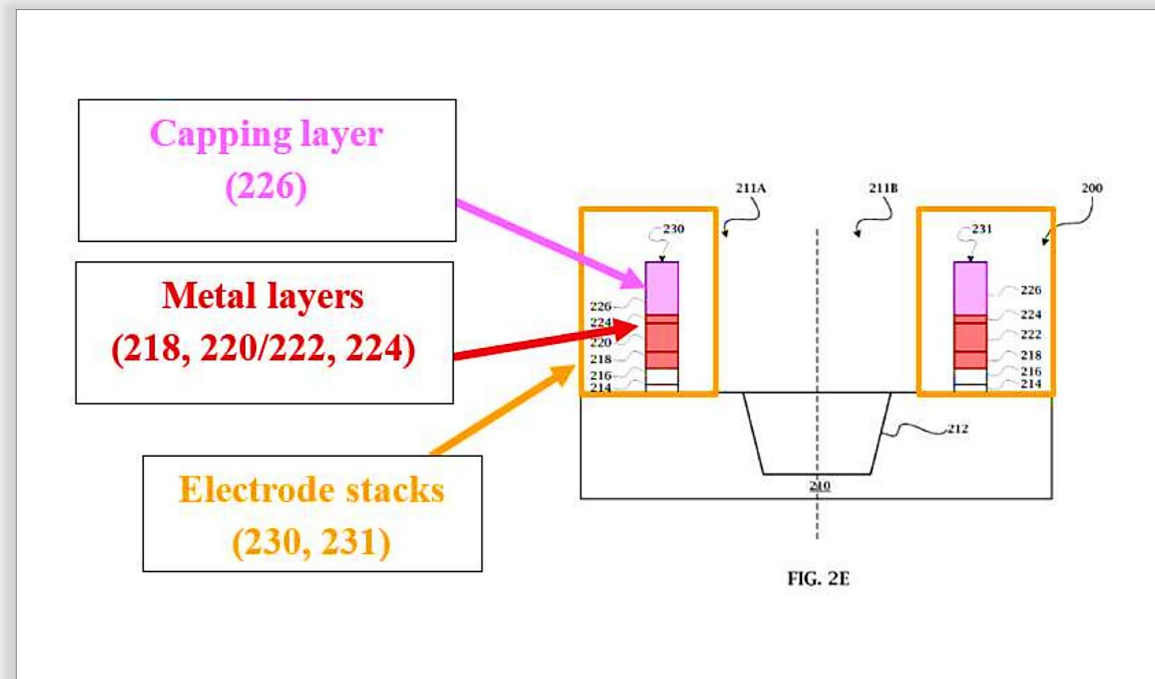
The Petition Also Argues That a POSA Would Use Titanium for Barrier/Protection Layer 218

Petition, 35-36;
POR, 62-63

Petition

A POSITA would have been motivated to use titanium as diffusion barrier/protection layer 218 and diffusion barrier layer 224 in Yu's device, as Yu discloses, because diffusion barrier layers made of titanium were well-known by August 2009 and constituted a simple design choice depending on the application of the device. Zhao ¶¶66-67, 70, 152.

Petition, 36



Petition, 42

Ground 5 Separately Fails Because Yu Never Discloses Thickness of Diffusion Barrier Layer 218 When Formed From Titanium

POR, 62-63

Patent Owner's Response

Petitioner alleges that the thickness of Yu's diffusion barrier/protection layer 218 is 20Å. Petition, 38. The 20Å thickness Yu teaches is for a diffusion barrier/protection layer 218 formed from titanium *nitride* (TiN). Yu, [0029]. But Petitioner's Yu-USui combination does *not* use a *TiN* diffusion barrier/protection layer 218. Instead, Petitioner alleges a "POSITA would have been motivated to use *titanium* as **diffusion barrier/protection layer 218**...in Yu's device." Petition, 36. Titanium nitride and titanium are different materials. Piner, ¶¶261-263.

Petitioner cites no teaching in Yu of a thickness for a *titanium* diffusion barrier/protection layer 218 as in Petitioner's Yu-USui combination. Petition, 36. The only thickness Petitioner cites is 20Å for a TiN "embodiment." Yu, [0029]. Yu never says this thickness applies for the diffusion barrier/protection layer 218 for all materials. Instead, Yu says that "in alternate embodiments, the diffusion barrier layer 218 comprises any suitable thickness." Yu, [0029]. Yu provides no teaching of a "suitable thickness" for the *titanium* diffusion barrier/protection layer 218 used in Petitioner's Yu-USui combination. Petition, 36.

POR, 62

Yu (EX-1005)

[0029] In some embodiments, a diffusion barrier/protection layer 218 is formed over the high-k dielectric layer 216. The diffusion barrier/protection layer 218 may comprise titanium, titanium nitride (TiN), tantalum, tantalum nitride, other suitable material, and/or combinations thereof. In the present embodiment, the diffusion barrier/protection layer 218 comprises TiN, which is deposited by PVD to a thickness of approximately 20 Å. In alternate embodiments, the diffusion

Yu (EX-1005), [0029]

Petitioner Improperly Tries to Change Argument to Use Titanium Nitride for Barrier/Protection Layer 218 in Petitioner's Reply, Which is Foreclosed

Reply, 27;
Sur-Reply, 25

Petition

A POSITA would have been motivated to use titanium as diffusion barrier/protection layer 218 and diffusion barrier layer 224 in Yu's device, as Yu discloses, because diffusion barrier layers made of titanium were well-known by August 2009 and constituted a simple design choice depending on the application of the device. Zhao ¶¶66-67, 70, 152.

Petition, 36

Petitioner's Reply

While Yu does not expressly disclose the claimed thickness of [1.C], it renders it obvious. Petition, 33-55 (citing Yu, [0036]); Ex-1002, 149-187 (same). Barrier layer 218 comprises metals, including TiN, which may have a thickness of 20Å. Petition, 38; Yu, [0029]. This is the claimed bottommost layer. Petition, 43-44.

Reply, 27

Patent Owner's Sur-Reply

In Reply, Petitioner changes its argument and alleges that a *titanium nitride* "TiN" barrier layer 218 of 20Å "is the claimed bottommost layer." Reply, 27. That is improper and should not be considered. TPG, §II.I; *Wasica*, 853 F.3d at 1286-87.

Sur-Reply, 25

Ground 5 Separately Fails Because the Petition Failed to Establish Yu's Barrier Layer Is Part of Electrode Stack

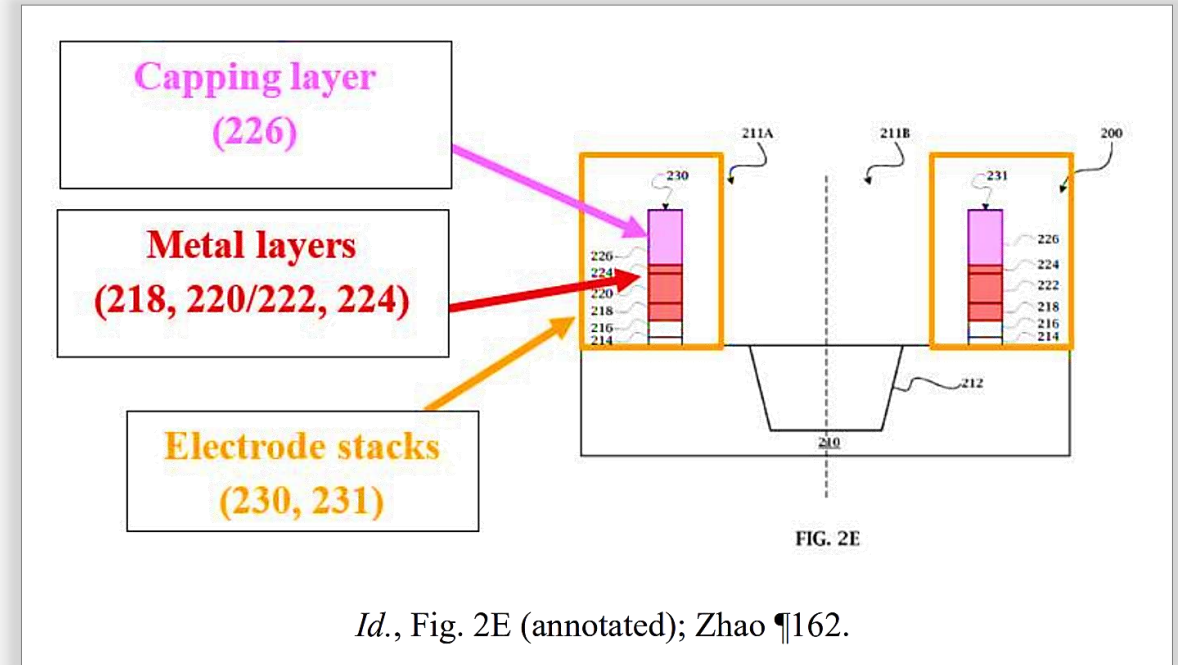
Petition, 42

Petition

- b. [1a]: an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers;

Yu discloses [1a] because it discloses **metal gate stacks 230, 231** (electrode stacks) each including a metal **diffusion barrier/protection layer 218** (first metal layer) (*id.*, [0029]), **metal layers 220, 222** (*id.*, [0035]) (second metal layer), a metal **diffusion barrier layer 224** (*id.*, [0035]) (third metal layer), and a **capping layer 226** (*id.*, [0036]) (capping layer) formed over the metal layers.

Petition, 42

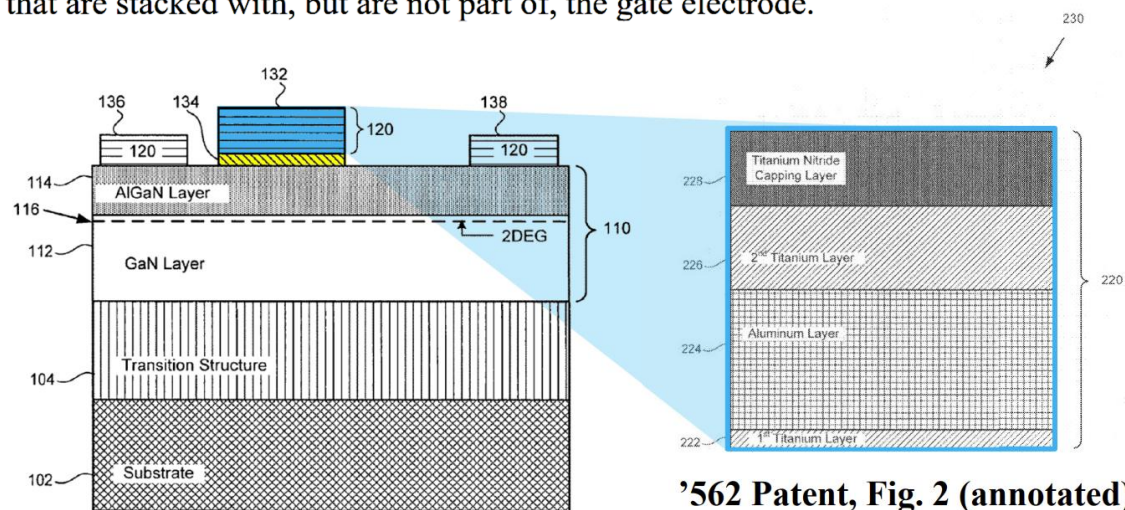


The Specification Explains that an “Electrode Stack” in an Insulated Gate Electrode Only Includes the Metal Layers Forming the Electrode

POR, 45-46

Patent Owner's Response

1001, 2:58-60 (“gate electrode 132”), 3:19-35 (same). The electrode stack in Fig. 2 (below right) forms “gate electrode 132, in Fig. 1.” *Id.*, 3:40-43 (Fig 2’s “[e]lectrode stack 220” “corresponds to electrode stack 120 in FIG. 1”). Thus, the ’562 Patent is clear that the “electrode stack” for a gate electrode includes only the metal layers forming the electrode and not other layers like insulating layer 134 that are stacked with, but are not part of, the gate electrode.



’562 Patent, Fig. 1 (annotated)

’562 Patent, Fig. 2 (annotated)

’562 Patent

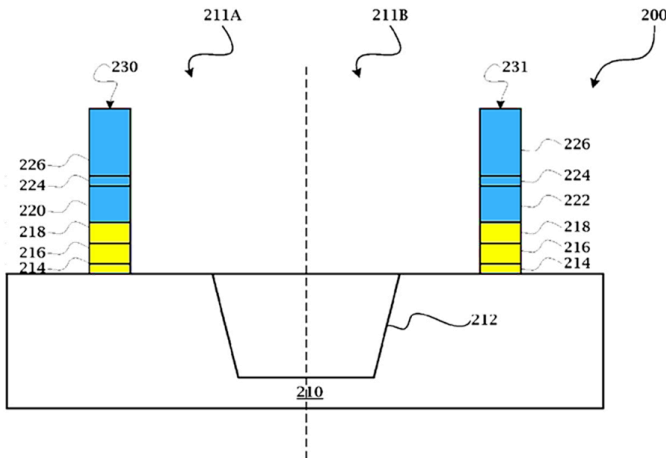
Source electrode 136 and drain electrode 138 are power electrodes ohmically coupled to the heterojunction formed by GaN layer 112 and AlGaIn layer 114. Moreover, insulated gate electrode 132 is situated between source electrode 136 and drain electrode 138, on GaN body 110. As shown in FIG. 1, each of source electrode 136, drain electrode 138, and insulated gate electrode 132 comprises electrode stack 120. Electrode stack 120 includes a refractory metal nitride capping layer (not explicitly shown in FIG. 1), such as a titanium nitride (TiN) capping layer, for example. As further shown in FIG. 1, insulated gate electrode 132 includes gate insulator layer 134, such as a silicon nitride (Si₃N₄) or silicon dioxide (SiO₂) layer, for example, underlying electrode stack 120. It is noted that although in the embodiment of FIG. 1, gate electrode 132 is shown as an insulated gate electrode, in other embodiments, gate electrode 132 comprising electrode stack 120 may make Schottky contact with GaN body 110.

EX-1001, 3:19-35

POR, 45-46

Patent Owner's Response

Like the '562 Patent's insulated gate electrode (blue above) is stacked with another layer (yellow above), Yu's gate electrodes (blue below) are stacked with other layers (yellow below).



Yu, Fig. 2E (annotated)

Yu calls the entire stack a “metal gate stack.” Yu, [0038]-[0039]. Metal gate stacks 230 and 231 have different metal layers (220 and 222, respectively) with different work functions, but their structures are otherwise identical. Each stack includes two oxide layers 214, 216 (yellow above) atop the semiconductor (Yu, [0028]-[0030]), a “diffusion barrier layer” 218 separating the metal layer (220 or 222, blue above) from the oxide layers to prevent material from diffusing between the metal and oxide layers (Yu, [0029]), a capping layer 226 (Yu, [0036]), and a diffusion barrier layer 224 separating the capping layer from the metal layer (220 and 222) to prevent diffusion (Yu, [0035]).

Patent Owner's Response

Layer 218 is an “optional” “diffusion barrier/protection layer” that “may be omitted.” Yu, [0029]; Petition, 43; Piner, ¶¶234-235.

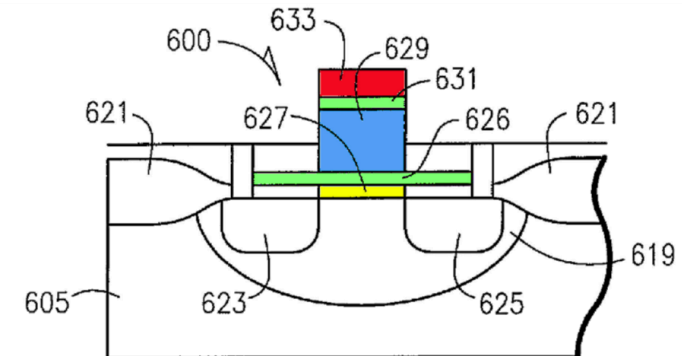
Diffusion barrier layers were well-known. Piner, ¶¶236-237; *see also id.*, ¶¶72-75. They are disposed between two layers of material to prevent the separated materials from diffusing into each other. EX-2002, [0057]-[0058], Fig. 6. Diffusion barrier layers had been used to separate a gate electrode from an oxide layer, like Yu's layer 218 does. *Id.* Yu's barrier layer is not part of the gate electrode; it separates the gate electrode from the oxide layer. *Id.*; Piner, ¶237.

POR, 48

Meng (EX-2002)

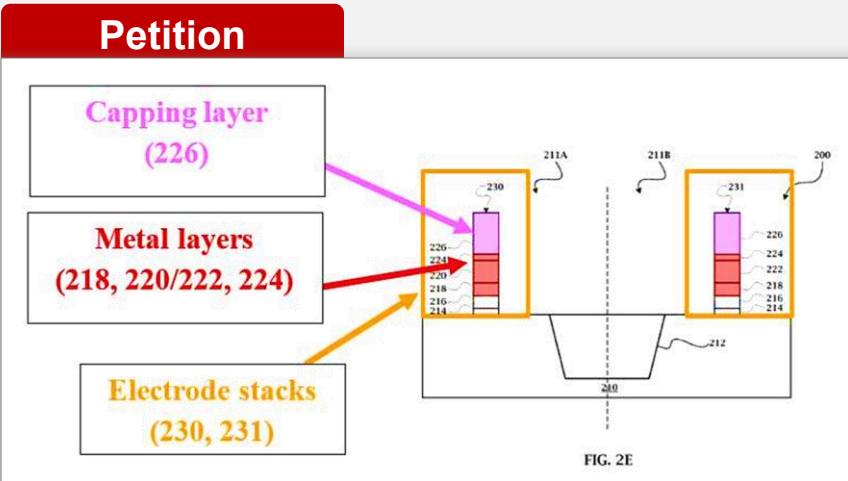
[0057] FIG. 6 shows a transistor 600 including an ALD layer according to the present invention. In an embodiment, the transistor 600 is used as an access transistor to the memory cell 500. Transistor 600 is formed on a substrate 605 in an active area including a doped well 619 covered by a field oxide region 621. The field oxide region 621 has a thin center

region of the well 619. In an embodiment, a barrier layer 626 is formed according to the present invention over the gate oxide 627. The gate electrode 629 is formed over the barrier layer 626. The barrier layer 626 is adapted to prevent dopants, such as boron, in the gate electrode 629 from diffusing into the gate oxide layer 627, the source/drain 623 and the source/drain 625. The barrier layer 626 also prevents reactions between the gate electrode 629 and the gate oxide layer 627, prevents migration of dopants from the gate electrode 629 to other areas of the semiconductor device, prevents oxidation of the gate electrode 629 and prevents the formation of silicides on the gate electrode.



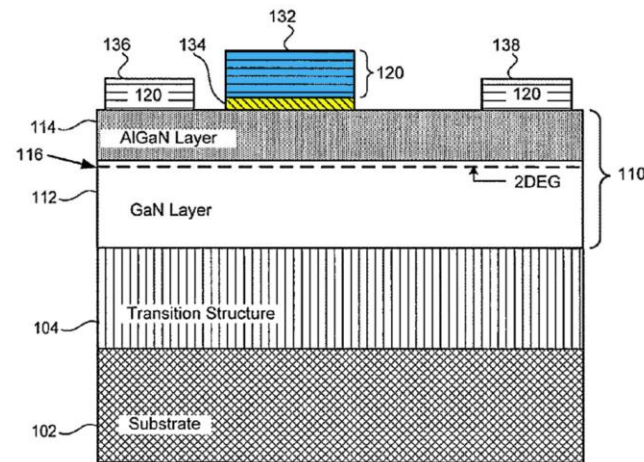
Meng (EX-2002), [0057], FIG. 6

Petition



Petition, 42

Patent Owner's Response



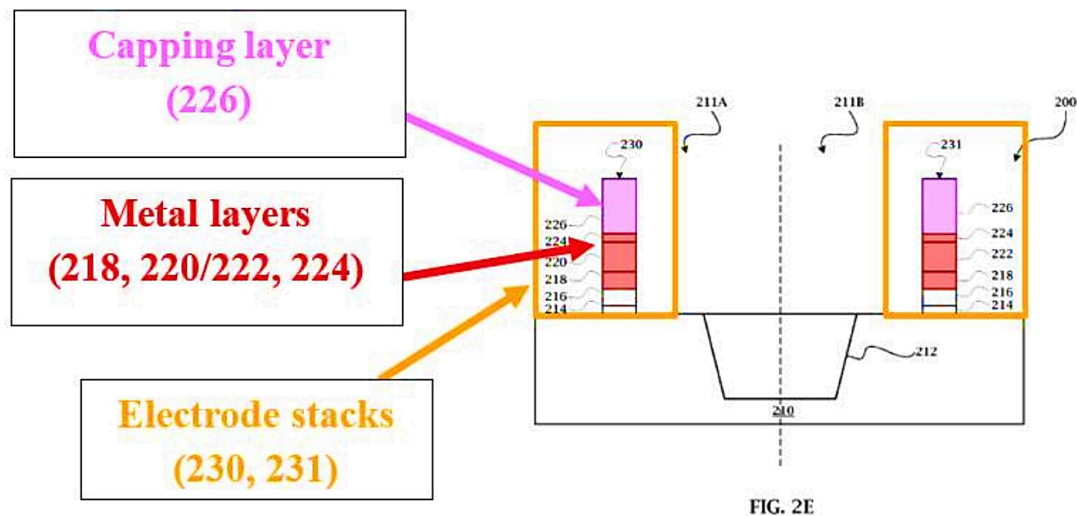
'562 Patent, Fig. 1 (annotated)

The above-identified intrinsic evidence – ignored by Petitioner – directly refutes Petitioner's conclusory assertion that Yu's entire metal gate stack is an "electrode stack." Petition, 42. Yu's entire metal gate stack (230 or 231) cannot be an "electrode stack" as claimed because it includes a dielectric layer (214 or 216) that performs the same insulating function as insulating layer 134 in the '562 Patent.¹³ Yu, [0022], [0027]-[0028], [0039]. The intrinsic evidence makes clear that such an oxide layer is not part of the claimed "electrode stack." Thus, Petitioner's conclusory assertion that Yu's entire metal gate stack 230 or 231 is an "electrode stack" is wrong.

Petitioner Improperly Tries to Change Argument to Say Yu's Electrode Stack May Not Include Dielectrics in Petitioner's Reply, Which is Foreclosed

Reply, 26-27;
Sur-Reply, 27

Petition



Id., Fig. 2E (annotated); Zhao ¶162.

Petition, 42

Petitioner's Reply

Yu thus discloses the claimed “electrode stack,” whether its boundaries are drawn to include the dielectrics or not. Dr. Zhao clarified that he drew the “yellow box on 230, 231 just to highlight this component of Yu as important.” Ex-2026,

Reply, 26-27

Patent Owner's Sur-Reply

Petitioner seeks to change its argument in Reply by now alleging that Yu's electrode stack is everything other than the dielectrics. Reply, 26-27. Petitioner's assertion that “Dr. Zhao clarified” during deposition “that he drew the ‘yellow box on 230, 231 just to highlight this component of Yu as important’” is irrelevant and not credible. *Id.* The **Petition** unambiguously identified Yu's entire metal gate stacks (230, 231) as the claimed “electrode stacks.” Petition, 42 (“metal gate stacks 230, 231 (electrode stacks)” and “Electrode stacks (230, 231)”). The **statutory** requirement that the Petition state its grounds “with particularity” forecloses Petitioner from shifting its argument in Reply, based on an expert's alleged “clarification” at deposition, after the Petition's argument was shown to fail. *Wasica*, 853 F.3d at 1286-87.

Sur-Reply, 27

POR, 48;
Sur-Reply, 28

Fig. 6

Petitioner Tries to Obfuscate Its Failure to Provide Evidence Establishing That Diffusion Barrier Layers Are Part of a Gate Electrode

Reply, 27;
Sur-Reply, 28-29

Petitioner's Reply

In another failed defense, Patent Owner contradicts itself by contending Yu's barrier layer 218 is "not part of the gate electrode, it separates the gate electrode from the oxide layer." POR, 48. Yet on the preceding page, Patent Owner argues the opposite, that "Yu calls the entire stack"—including barrier 218—"a "metal gate stack." POR, 47. And Patent Owner does not dispute that barrier 218 is a metal layer stacked along with the other metal layers. POR, 47-49. Patent Owner cannot exclude it from the "electrode stack's plurality of metal layers with expert opinion when the intrinsic record does not. *Phillips*, 415 F.3d at 1317. The plain meaning applies.

Reply, 27

Patent Owner's Sur-Reply

Petitioner obfuscates. There is no "contradict[ion]" in explaining that Yu's entire metal gate stack includes layers that are not part of the electrode. Reply, 27. Petitioner concedes as much by not disputing that insulating layers 214, 216 are not part of Yu's electrode stack. Petitioner's assertion that the intrinsic record does not explicitly "exclude" a diffusion barrier layer from the electrode stack is irrelevant because the specification does not disclose a diffusion barrier layer. *Id.*

Sur-Reply, 28-29

Yu-Based Grounds 6-7 Fail for Additional Reasons

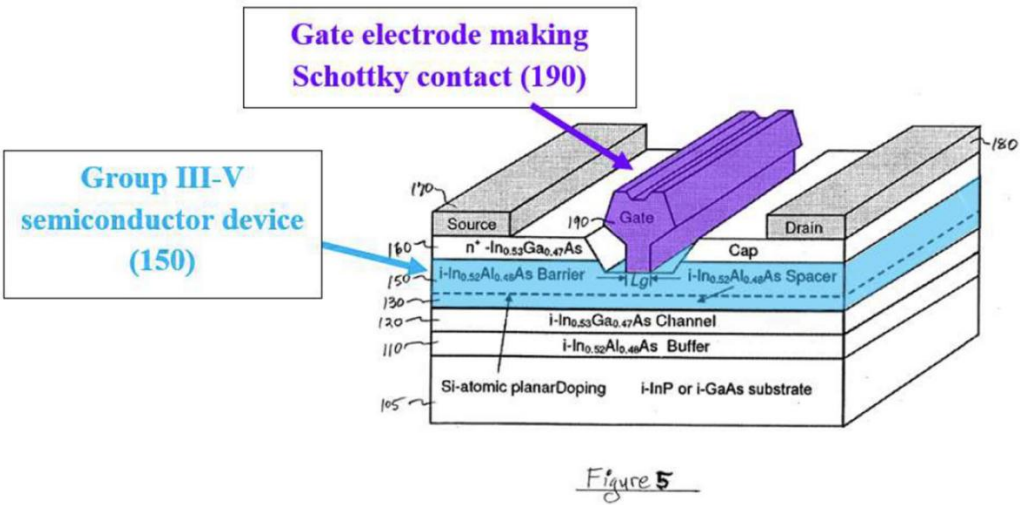
- **Ground 6**
 - The Petition did not explain contemplated workings of Yu-Usui-Adesida
 - The Petition maps Adesida's "gate 190 (gate electrode)" to the gate electrode in claims 11 and 16 but fails to allege or establish that gate 190 meets claim 1 or 13
 - The Reply's attempts to change the combination should be rejected
 - No explanation of the contemplated workings of the Reply's Yu-Usui-Adesida combination
 - Petitioner cites no reference disclosing a Schottky gate electrode for a CMOS device
 - No supported reason to remove Yu's high-k dielectric while retaining Yu's gate structure which is specifically designed for that dielectric
 - No reasonable expectation of success using Yu-Usui's alleged electrical contact unchanged as a Schottky contact

Ground 6 Fails: The Petition Provides No Evidence that Adesida's Gate Electrode Meets Claims 1 and 13

Petition, 60-61
POR, 69-70

Petition

Consistent with the '562 patent, Adesida discloses **gate 190 (gate electrode)** formed as a **Schottky barrier contact (Schottky contact)** on the group III-V device and **source 170** and **drain 180 (power electrodes)** making ohmic contact with the group III-V device. Adesida, Fig. 5 and [0031].



Petition, 60-61

'562 Patent

11. The electrical contact of claim 8, wherein said electrical contact is implemented as a gate electrode making Schottky contact with said group III-V semiconductor device.

EX-1001, Claim 11; see also EX-1001, claim 16

Patent Owner's Response

Petitioner admits Yu's gate electrode does not make Schottky contact with the semiconductor but alleges Adesida's does. Petition, 58. Ground 6 maps Adesida's "**gate 190 (gate electrode)**" to the gate electrode in claims 11 and 16, using the annotated figure below. Petition, 60-61. That fails to demonstrate obviousness because claims 11 and 16 limit "said electrical contact" in claims 1 and 13, respectively, and Petitioner never even alleges that Adesida's gate electrode meets claim 1 or 13. It does not.¹⁶ Piner, ¶¶278-282. That is fatal to Ground 6.

POR, 69-70

Ground 6 in Petitioner's Reply: Modify Yu's Gate Electrode Instead of Adesida's Gate

POR, 70-71;
Reply, 28-29

Patent Owner's Response

To the extent Petitioner alleges in Reply that the gate electrode in Yu-Usui-Adesida is not Adesida's gate electrode, that would fail. The Petition was required to specify its grounds with particularity and provide a "detailed explanation" thereof. 35 U.S.C. § 312; 37 C.F.R. § 42.104(b)(4). Moreover, a "prerequisite" to establishing obviousness is to explain the "contemplated workings" of the Yu-Usui-Adesida combination. *Personal Web*, 848 F.3d at 994. The Petition fails to do so. Ground 6 fails for that reason as well.

Finally, to the extent Petitioner alleges in Reply that the structure of the gate electrode in Yu-Usui-Adesida is Yu's gate electrode but modified to make Schottky contact, that would fail because the Petition *never alleges this* and cites *no evidence* in support. Piner, ¶¶283-286. Yu discloses a CMOS device with "a *high-k gate dielectric* and metal gate electrode." Yu, [0004]. Petitioner admits that Yu's Fig. 2E – which Petitioner relies on for claims 1 and 13 (Petition, 41-44 and 54-55) – has dielectric "insulating" layers 214, 216 (Petition, 53-54), so it is an insulated gate electrode that does not make Schottky contact. Piner, ¶284.

Petitioner's Reply

For claims 9 and 14, "it would have been obvious to implement Yu-Usui's group III-V semiconductor devices as HEMTs." Petition, 59. This meant Adesida's "HEMT device with the metal layers taught by Yu and Usui as the gate." Ex-2026, 195:21-196:7. Similarly, for claims 11 and 16, "would have been obvious to implement Yu or Yu-Usui's group III-V semiconductor devices with gate electrodes making Schottky contacts." Petition, 60. The result is "a III-V HEMT device with the metal layers from Usui and Yu as the Schottky gate contact, or Schottky gate electrode on these III-V HEMT device." *Id.* at 196:25-197:3. The Petition gave

Reply, 29

Patent Owner's Sur-Reply

claims 11 and 16 depend. POR, 69-72. Petitioner again asks the Board to discard the Petition's annotations (to Adesida Fig. 5) and arguments (Petition, 60-61) and accept the explanation of its expert at deposition of what Petitioner "meant" to allege. Reply, 29. The Reply's new assertion that the gate electrode in claims 11 and 16 is met by an electrode with unidentified "metal layers from Usui and Yu" (Reply, 28-29) should not be considered. TPG, §II.I. Petitioner also has no answer

Sur-Reply, 29

POR, 70-71

Ground 6 in Petitioner’s Reply Fails: No Evidence Schottky Gate Electrodes Ever Used in CMOS Devices

POR, 71-72

Piner (EX-2024)

285. Petitioner does not cite any reference disclosing a Schottky gate electrode for a CMOS device like Yu’s. That would be highly unconventional – the “O” in CMOS refers to the “oxide” between metal and semiconductor – and thus far from a “simple design choice” as Petitioner alleges (Petition, 59). Moreover,

EX-2024, ¶ 285; see also EX-2024, ¶ 284.

Yu (EX-1005)

PMOS). It is understood that the semiconductor device 200 may be formed by complementary metal-oxide-semiconductor (CMOS) technology processing, and thus some processes are not described in detail herein.

Yu (EX-1005), [0025]

Patent Owner’s Response

Piner, ¶285. Moreover, Petitioner’s assertion that a POSA would have modified Yu to *remove* its high-k dielectric but *retain* Yu’s gate structure – which is *specifically designed to work with that high-k dielectric* – is unsupported and based on nothing but improper hindsight. *Id.* POSAs would not have used a Schottky gate electrode for Yu’s CMOS device, and if interested in implementing a Schottky gate electrode, would not have used Yu’s metal gate electrode specifically designed for use with a high-k dielectric insulator. *Id.*

Moreover, Petitioner fails to establish a reasonable expectation of success. To the extent Petitioner suggests that Yu-Usui’s alleged electrical contact could simply be used unchanged to form a Schottky contact, no evidence supports that. POSAs understood this would require changes to the layers – in their materials and thicknesses – because Schottky contacts, like ohmic contacts, are tailored to the semiconductor. Piner, ¶286. Petitioner fails to account for the changes that would be required and fails to show that the alleged electrical contact of Yu-Usui-Adesida would meet claim 1 or 13 after such changes. *Id.*

POR, 71-72

Yu-Based Grounds 6-7 Fail for Additional Reasons

- **Ground 7**
 - Even if everything in Ground 7 were accepted as true, Ground 7 fails as to claims 10 and 15 because the Petition did not establish any non-hindsight reason to implement a CMOS gate electrode as a power electrode making ohmic contact
 - Yu's (or Yu-Usui's) gate electrode does not meet claims 10 and 15
 - Sugimoto's disclosure of source and drain electrodes would not have motivated a POSA to modify Yu's (or Yu-Usui's) gate electrodes
 - The Petition's allegations regarding current flow in and out of a semiconductor do not apply to Yu's (or Yu-Usui's) gate electrodes
 - The Petition does not allege (or support) implementing Yu-Usui-Sugimoto's source or drain electrodes to have the same structure as (or Yu-Usui's) gate electrodes
 - CMOS gate electrodes were insulated and served a different purpose than source/drain electrodes
 - No reasonable expectation of success using Yu's (or Yu-Usui's) gate electrodes unchanged as an ohmic contact

Ground 7: The Petition Describes Reasons That Power Electrodes Use Ohmic Contacts

Petition, 62-63;
POR, 72-74

'562 Patent

10. The electrical contact of claim 8, wherein said electrical contact is implemented as a power electrode making ohmic contact with said group III-V semiconductor device.

EX-1001, Claim 10; see *also* EX-1001, claim 15

Petition

Yu and Usui do not expressly disclose that their group III-V devices have a power electrode making an ohmic electrical contact. Zhao ¶202.

By August 2009, Dr. Zhao explains that it was well-known that ohmic contacts are of critical importance with respect to device functionality, performance, and long-term reliability. Zhao ¶55 (citing Ex-1013, 144). It was well-known that ohmic contacts serve as source and drain contacts in group III-V devices and allow current to flow into and out of a semiconductor material without distortion of the signal. Zhao ¶57 (citing Ex-1016, 22; Ex-1017, 1). It was well-known that the most critical component of an ohmic contact is its low specific contact resistance, which minimizes the power consumption of the contact and the

internal heating of the contact, thereby prolonging device operation with predictable performance. Zhao ¶57, 205 (citing Ex-1016, 22).

Yu disclosed the importance of an improved work function and thermal stability. Yu, Abstract. A POSITA would have been motivated to implement the devices of Yu and Yu-Usui with a power electrode making an ohmic contact, as taught by Sugimoto because such a combination would provide reduced internal heating of the contact and improved current flow (i.e., improved work function values). Furthermore, such a combination is the result of combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 416-17; *Adesida*, [0031], Fig. 5; Zhao ¶¶51-57, 206).

Petition, 62-63

Ground 7 Fails: No Evidence that Yu-Usui-Sugimoto's Alleged Power Electrode Can Meet Claims 1 and 13 In the Same Way Yu-Usui's Alleged Insulated Gate Electrode Would

POR, 72-74

Patent Owner's Response

If the Petition is read to implicitly suggest that Ground 7's Yu-Usui-Sugimoto combination meets claims 1 and 13 in the same way that Ground 5's Yu-Usui combination does, that fails. Ground 5 alleges that the claimed electrical contact comprising an electrode stack is met by Yu's "metal *gate* stacks." Petition, 41-44 and 54-55. Yu's gate stacks form CMOS *gate* electrodes¹⁷ that are undisputedly not ohmic contacts because they do not contact the semiconductor. Yu, Title, Abstract, [0004], Fig. 2E, [0027] (insulating "dielectric layer 214" is "formed over the substrate"); Piner, ¶¶287-291; Zhao, ¶¶56-57.

POR, 73-74

Ground 7 Fails: No Reason Why a POSA Would Have Modified Yu's / Yu-Usui's Gate Electrode in View of Knowledge Related to Ohmic Contacts

POR, 74

Patent Owner's Response

Petitioner alleges that ohmic contacts were known to “serve as *source and drain* contacts in group III-V devices and allow current to flow into and out of a semiconductor material.” Petition, 62-63. Current flow in and out of the semiconductor does not occur through Yu's *gate* electrodes; thus, even if a “POSITA would have been motivated to implement the devices of Yu and Yu-Usui with a power electrode making an ohmic contact” (Petition, 63), a POSA would have implemented the device's *source and drain* electrodes as power electrodes making ohmic contact. Piner, ¶292. That does not meet claim 10 or 15 because it makes no change to Yu's *gate* electrode which is alleged to meet “said electrical contact” in independent claims 1 and 13. Petition, 41-44 and 54-55.

POR, 74

Ground 7 Fails: A POSA Would Not Have Reasonably Expected Success Using Yu's / Yu-Usui's Gate Electrode As An Ohmic Contact Without Any Changes

POR, 74-76

Patent Owner's Response

Petitioner does not even allege that a POSA would have implemented the Yu-Usui-Sugimoto combination by having its *source or drain* electrode have the same structure as either Yu *gate* electrode alleged to meet “said electrical contact” in independent claims 1 and 13, let alone establish with evidence some supportable reason why this allegedly would have been so. Piner, ¶293.

It was well-known that a CMOS gate electrode is separated from the semiconductor by a dielectric layer and serves a different purpose than ohmic source and drain electrodes that contact the semiconductor and have current pass through them when the transistor is on. Piner, ¶294 (a CMOS gate controls the transistor through an electrical field across the gate dielectric without current flowing through the gate); EX-1011, 356, 434-36, 454-57; Petition 63 (low contact resistance is critical for ohmic contacts for “improved current flow”).

Thus, CMOS gate electrodes were conventionally implemented using a *different structure formed from different materials* than CMOS source and drain electrodes. Piner, ¶294.

POR, 74-75

Moreover, Petitioner fails to establish a reasonable expectation of success.

To the extent Petitioner suggests that Yu-Usui's alleged electrical contact could simply be used unchanged to form an ohmic contact, no evidence supports that. POSAs understood this would require significant changes to the layers – in their materials and thicknesses – because ohmic contacts are closely tailored to the semiconductor, like a lock and key. Piner, ¶¶48-57. Petitioner fails to account for the changes that would be required and fails to show that the alleged Yu-Usui-Sugimoto electrical contact would meet claims 1 and 13 after such changes. Piner, ¶296.

POR, 76

Piner (EX-2024)

54. In my opinion, a POSA in August 2009, though aware of the general theoretical principles of Schottky contacts and ohmic contacts, was not able to reliably predict the resulting electrical performance of a contact as a result of depositing a particular metal to a particular semiconductor, or changing an aspect of an existing ohmic contact design in the metal or in the semiconductor. Rather, as a result of complexities such as those I described above, a POSA would make a prototype to test the effects of design changes. In fact, it is known that “[i]n order to determine barrier height[], it is necessary to fabricate a specimen to test.” EX-1016 (Voss) at 25. This lack of a robust theoretical model to predict the effects of design changes has led artisans to deem the fabrication of ohmic contacts “more an art than a science.” EX-1017 (Kramer), 31 (Page 38 of 151).

EX-2024, ¶¶ 54-55; *see also generally*, EX-2024, ¶¶ 48-47.

55. As a result, every laboratory tended to have “its own favorite recipes which involve particular metal or alloy systems, particular deposition methods and particular forms of heat treatment.” EX-1017 (Kramer), 31 (Page 38 of 151). The number of factors in the material choice (of both the metal and semiconductor) and processing conditions that might be varied to change the ohmic vs. non-ohmic behavior of a metal-semiconductor contact, only some of which I have listed, inherently required a POSA to experiment with physical prototypes, in a trial and error process where each incremental change has to be tested and evaluated to determine whether the desired ohmic performance was met. Unsurprisingly, in August 2009 and still today, electrical contact design was a lengthy process that took months and sometimes years of significant experimentation. In my experience in the industry, and now in academia for the past 27 years, I have found that it typically takes over 12 months to create a new electric contact design, even when working from existing or prior designs for inspiration and can often take up to three years. This was true in August 2009 as well. For example, when I was at

Patent Owner's Sur-Reply

Even if everything Ground 7 alleged was true, the Petition failed to demonstrate that its Yu-USui-Sugimoto combination meets both independent claims 1 and 13 and claims 10 and 15 (which Ground 7 challenges) depending therefrom. POR, 72-76. The Reply fabricates a new combination based on deposition testimony from Petitioner's expert. Reply, 29. The Board should hold Petitioner to the *Petition's* failed Ground 7. If considered, the Reply's new Ground 7 fails. Petitioner fails to rebut Dr. Piner's explanation that if the electrode stacks of Yu or Yu-USui were used as a power electrode making ohmic contact (Reply, 29), the electrode materials and thicknesses would have to change "because ohmic contacts are closely tailored to the semiconductor." POR, 76 (citing Piner, ¶¶48-57).

Sur-Reply, 29-30

Additional Slides

Conclusion of Petitioner’s Expert About “Electrode Stack” Is Entitled to No Weight

Petition, 11;
POR, 15

Petition

Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8; Zhao ¶89.

Petition, 11

Zhao Dec. (EX-1002)

89. Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8.

EX-1002, ¶ 89

XEROX v. BYTEMARK



Patent Trial and Appeal Board
PRECEDENTIAL
Designated: 2/10/2023

in a data record associated with that user’s account.”). Dr. Jones does not cite to any additional supporting evidence or provide any technical reasoning to support his statement. Thus, the cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight. See 37 C.F.R. § 42.65(a)

Xerox Corp. v. Bytemark, Inc., IPR2022-00624, Paper 9, at 15 (Aug. 24, 2022) (precedential) (cited at POR, 15)

Zhao Dep. (EX-2026)

Q. Can you tell me what an electrode stack is?

A. Again, at the very beginning, we went through this. For claim -- patent 562, claim 1, it clearly state that electrode stack includes, includes metal layers and capping layer. And anything that is not a metal layer, or a capping layer of that electrode stack is unclaimed. So all -- all my analysis, all discussion, solely focus on those metal layers and a capping layer. And, you know, I been provided this description already. And so, yeah, these are my answer again.

EX-2026, 172:20-173:5

Patent Owner's Response

⁹ Dr. Zhao testified that he only focused on whether the prior art had a stack of metal layers and a capping layer as claimed without regard to whether the stack was an “*electrode* stack.” *E.g.*, Zhao-Dep., 172:20-175:5. That improperly reads “electrode” out of the claims. Piner, ¶¶76-79.

POR, 17

Piner (EX-2024)

EX-2026 (Zhao Dep.), 172:20-173:5. This statement, which indicates that Dr. Zhao did not consider whether the metal layers and capping layer were part of an electrode stack in the first place – and *solely* focused on the metal layers and capping layers regardless of whether they were part of an electrode stack – is consistent with the absence of analysis regarding the term “electrode stack” in his declaration, and the testimony he provided a dozen or more times earlier during the deposition:

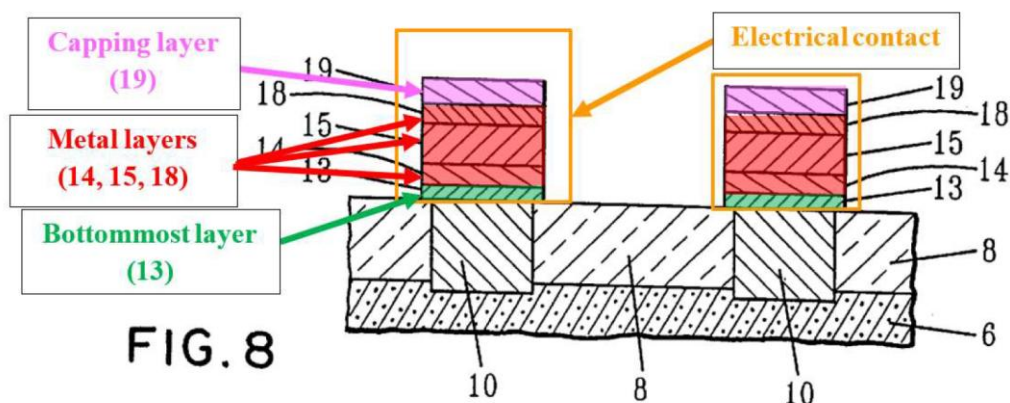
- EX-2026 (Zhao Dep.), 9:8-16 (“Anything outside this metal layers and the capping layer is unclaimed.”);
- *Id.*, 9:25-10:23 (“...anything that is outside this metal layer, or capping layer is unclaimed”);
- *Id.*, 11:18-12:7 (“All my analysis has been focused on those metal layers, the capping layers, because they include all the claim features.”);

EX-2024, ¶ 78 (discussing EX-2026, 9:8-16, 9:25-10:23, 11:8-12:7, 30:8-33:6, 39:12-40:14, 42:2-43:18, 76:1-78:18, 93:16-94:19)

The Petition Cited No Evidence About What an “Electrode Stack” Is

Petition, 11; POR, 17

Petition



Petition, 11

Zhao Dep. (EX-2026)

A. I already provide my opinion that whether this via 10 is part of electrode stack or not is irrelevant here for the reasons I provide many, many times. And in the end, of course the outside world will be electrically connected to the device 6 of Usui, the semiconductor device layer through this, this metal layers, and capping layer, and the via. And then, this depends on, you know, how you define this electrode stack. But our discussion, as well as when we look at fact 2 pattern, Usui and Yu are only focusing on the metal layers, which are 13, 14, 15, 18 and 19 in Usui's figure.

EX-2026, 43:7-18 (discussed at EX-2024, ¶ 78)

Usui (EX-1004)

1

PROCESS FOR FABRICATING A METALLIZATION STRUCTURE

TECHNICAL FIELD

The present invention is concerned with a method for fabricating a metallization structure and is especially concerned with producing a structure having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics. Moreover, the process of the present invention provides highly textured aluminum <111> layers. The structures fabricated by the process of the present invention are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure.

Usui (EX-1004), 1:11-14

Aluminum and aluminum alloys are used for forming various electrical connections or wiring in electronic devices such as in integrated circuit structures. The aluminum or aluminum alloys are used for forming the electrical connections between active and/or passive devices of the integrated circuit structure. It has been the practice to use aluminum or an alloy electrically connected to an underlying substrate such as silicon. While the aluminum and silicon are electrically connected together, it has become the practice to use intermediate electrically conductive layers interposed between the silicon and aluminum to provide better electrical connection to the silicon, and to provide a physical (metallurgical) barrier between the silicon and aluminum. This is for the purpose of preventing electromigration and spiking of the aluminum into the silicon. Migration of aluminum atoms into the underlying silicon can interfere with the performance and reliability of the resulting integrated circuit structure.

In addition to electromigration, the problem of hillock growth also occurs. These problems are especially pronounced at the submicron level. As the demand increases for scaling down the dimensions of the interconnection lines and for increasing the current density, overcoming, or at least minimizing, electromigration and hillock growth is essential.

Usui (EX-1004), 1:17-23, 1:30-41

Usui (EX-1004)

FIG. 1 is a cross-sectional view of the preferred embodiment of an interconnect metallurgy structure according to the present invention. Referring to FIG. 1, the interconnect metallurgy preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 to make connection to a device substrate 6. The metallurgy structure includes an underlayer of a group IVA metal and preferably a layer of titanium. Critical to the success of the present invention is having the thickness of this underlayer 13 being between about 90 angstroms to about 110 angstroms. As will be demonstrated hereinbelow, by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled. This is essential in achieving the necessary properties of the structure of the present invention.

Usui (EX-1004), 3:23-37

deposited thereon. The layer 13 is deposited by the following process. After formation of the device contact metallization 10, the semiconductor wafer 6 would be loaded into a sputtering tool which has been pumped to a low pressure. An in-situ sputter clean is then performed to remove any oxide from the contact metal 10 formed on the wafer at this time. This in-situ sputter clean typically is a mild sputter clean, run, for example, at about 5 minutes at low power (approximately 1000 watt) in a high-pressure argon ambient.

Following the sputter cleaning, the first layer of metallization 13 is then deposited. This first level metallization 13

Usui (EX-1004), 5:14-15

FIGS. 2-8 are a cross-sectional view of the process for fabricating the preferred interconnect metallurgy of the present invention in a step-by-step fashion.

Usui (EX-1004), 3:6-8

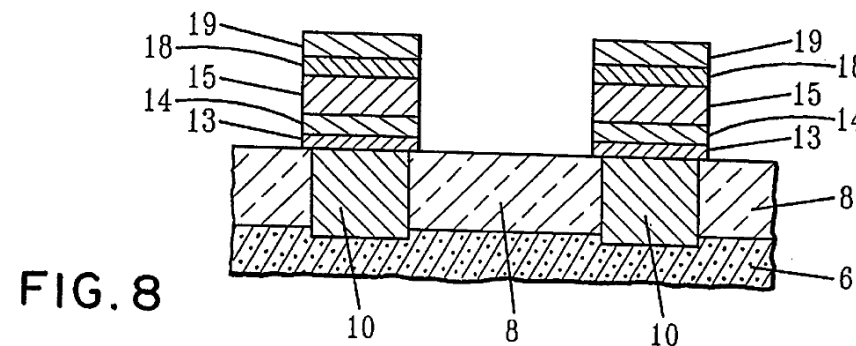


FIG. 8

Usui (EX-1004), FIG. 8; see also FIG. 1

While this completes the structure for a single interconnect layer according to the present invention, it should be recognized by those skilled in the art that these layers can then be repeated in a multiple level sequence to complete the interconnect circuit for the devices.

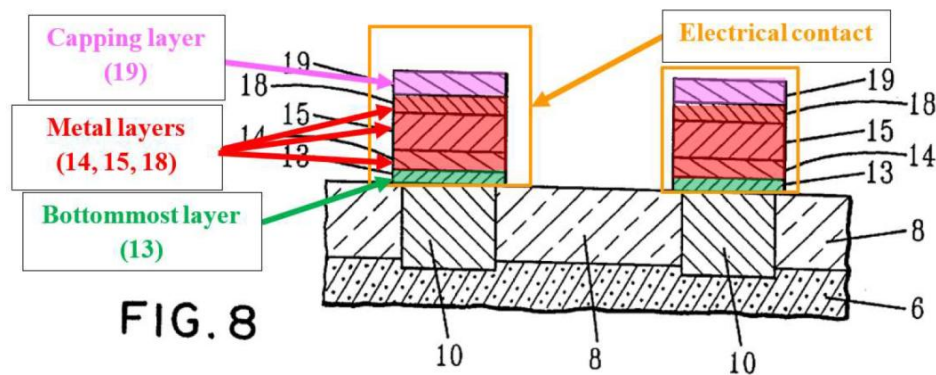
Usui (EX-1004), 4:10-14

Usui's Interconnect Is Not Like Any Electrode Described in the '562 Patent

POR, 16;
Sur-Reply, 3

Petition

Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8; Zhao ¶89.



Petition, 11

'562 Patent

Source electrode 136 and drain electrode 138 are power electrodes ohmically coupled to the heterojunction formed by GaN layer 112 and AlGaIn layer 114. Moreover, insulated gate electrode 132 is situated between source electrode 136 and drain electrode 138, on GaN body 110. As shown in FIG. 1, each of source electrode 136, drain electrode 138, and insulated gate electrode 132 comprises electrode stack 120. Electrode stack 120 includes a refractory metal nitride capping layer (not explicitly shown in FIG. 1), such as a titanium nitride (TiN) capping layer, for example. As further shown in FIG. 1, insulated gate electrode 132 includes gate insulator layer 134, such as a silicon nitride (Si_3N_4) or silicon dioxide (SiO_2) layer, for example, underlying electrode stack 120. It is noted that although in the embodiment of FIG. 1, gate electrode 132 is shown as an insulated gate electrode, in other embodiments, gate electrode 132 comprising electrode stack 120 may make Schottky contact with GaN body 110.

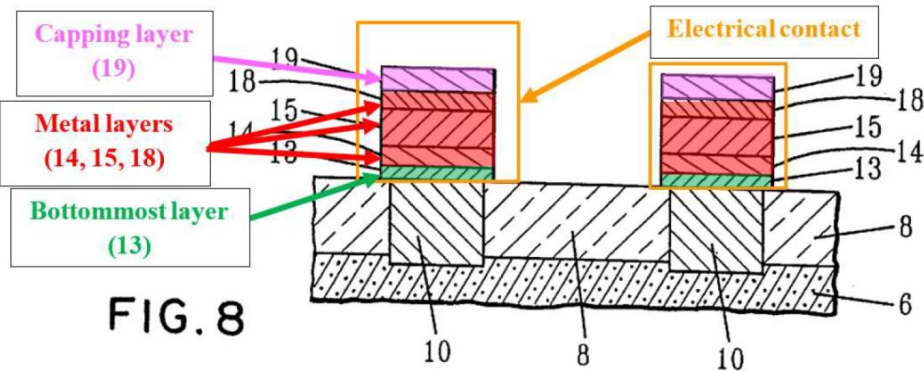
EX-1001, 3:19-35

Usui's Interconnect Does Not Establish Electrical Contact With Nonmetal/Medium as in the Parties' Dictionary Definitions

POR, 18;
Sur-Reply, 4-6

Petition

Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8; Zhao ¶89.



Petition, 11

Patent Owner's Response

supra §II.B. Usui's interconnect metallization structure (layers 13-15 and 18-19) is not "a conductor used to establish electrical contact with a nonmetallic part of a circuit." EX-2001, 371 (definition 1). As shown below, Usui's interconnect metallization layer is connected to "interplanar stud connection 10" – it is *stud connection 10* that "make[s] connection to a device substrate 6." Usui, 3:24-27.

POR, 18 (quoting EX-2001)

Petitioner's Reply

A conductor which serves to deliver, receive, collect, emit, deflect or control electric charge carriers. An electrode provides the path for current entering or leaving a medium such as a dielectric, electrolytic solution, semiconductor, gas, or vacuum. ... It is often a metal, and may consist for instance, of a wire, grid, plate or region.

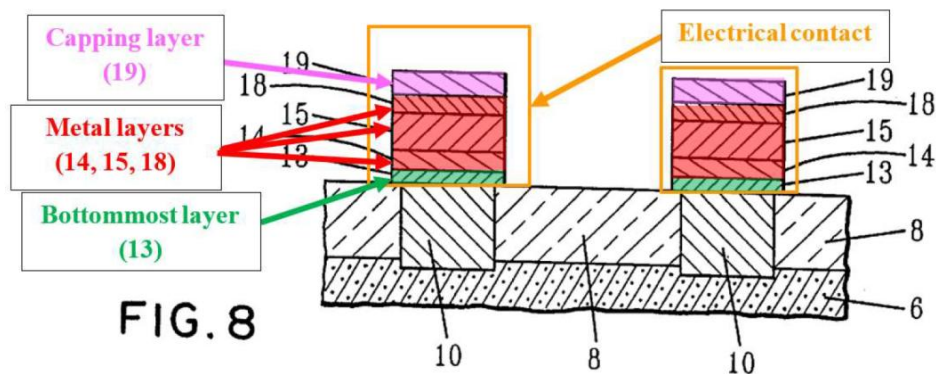
Reply, 8 (quoting EX-1046)

Usui's Interconnect Is Not a Semiconductor Device Element that Controls Electron Movement Under Patent Owner's Dictionary Definition

POR, 19

Petition

Usui discloses [1a] because Usui discloses an electrode stack in Figure 8 with a plurality of metal layers (metal layers 13, 14, 15, and 18) and capping layer 19 over the metal layers. Usui, Fig. 8; Zhao ¶89.



Petition, 11

Patent Owner's Response

Usui's interconnect metallization structure also does not meet Merriam-Webster's definition 2. Piner, ¶151. Usui never teaches that its interconnect metallization structure (layers 13-15 and 18-19) is "an element *in a semiconductor device* that emits or collects electrons or holes or controls their movements." EX-2001, 371. Usui's interconnect metallization structure is not an element of a semiconductor device at all – it is used to connect two devices. As its name signifies, Usui's "*interconnect* metallurgy" (Usui, 3:23-27) "form[s] electrical connections or *wiring* such as *between* active and/or passive *devices* of an integrated circuit structure" (Usui, 1:11-14). Fig. 8's single interconnect layer is "repeated in a multiple level sequence to complete the *interconnect circuit for the devices*." Usui, 4:10-15.

POR, 19

Usui's Interconnect Does Not Control Device Operation

Reply, 12;
Sur-Reply, 6-7

Petitioner's Reply

"Control" is not a claim term and does not appear anywhere in the '562 patent. Ex-1001. Patent Owner's construction thus creates further confusion by requiring interpretation of "control." POR, 4-10; Ex-2024, ¶¶81-91; Ex-1047, ¶49. This is another reason the construction is incorrect. *O2 Micro*, 521 F.3d at 1362.

Reply, 12

A conductor which serves to deliver, receive, collect, emit, deflect or control electric charge carriers. An electrode provides the path for current entering or leaving a medium such as a dielectric, electrolytic solution, semiconductor, gas, or vacuum. ... It is often a metal, and may consist for instance, of a wire, grid, plate or region.

Reply, 8 (quoting EX-1046)

Patent Owner's Sur-Reply

controls their movements." EX-2001, 371. "[C]ontrols" encompasses a transistor gate electrode which controls electron/hole movement through the transistor by turning the transistor on/off. Piner, ¶¶38, 90, 94, 166.

Petitioner's assertion that Usui's interconnect "controls the operation of a semiconductor device" by "enabling... current flow" in an integrated circuit fails. Reply, 13. Usui never says its interconnect somehow controls an (unidentified) device in semiconductor 6. As for an entire "integrated circuit" (*id.*) formed from interconnected semiconductor devices (which Usui nowhere describes), Petitioner never explains how or why Usui's interconnect that is interconnecting two parts of such a circuit somehow controls the entire circuit.

Sur-Reply, 6-7

Patent Owner's Sur-Reply

POR, 18. As shown below, an “interconnect” (red) atop an “electrode” (blue) is distinct from the electrode. EX-2002, [0058], Fig. 6 (annotated below).

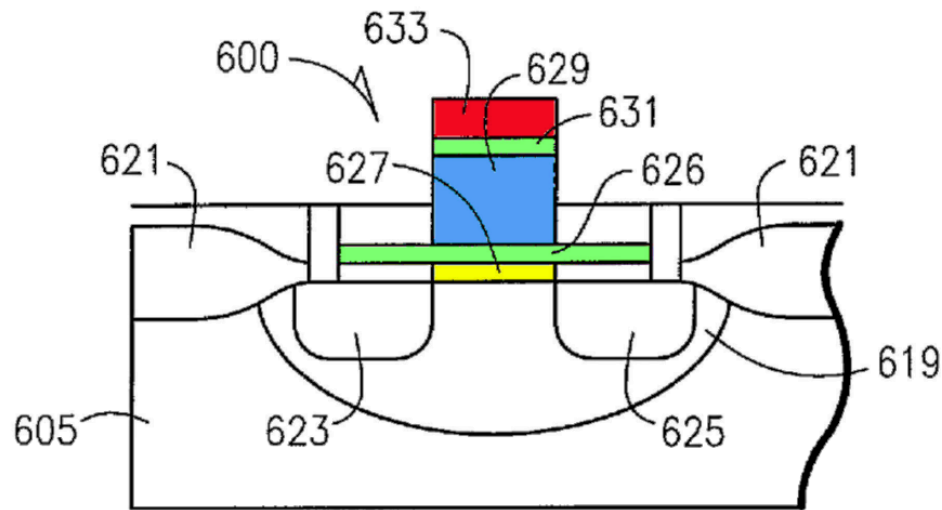


Fig. 6

Sur-Reply, 5 (annotating EX-2002)

Meng (EX-2002)

[0058] In an embodiment, a further barrier layer 631 is formed according to the present invention over the gate electrode 629. A line or interconnect 633 is formed on the barrier layer 631. The line 633 is adapted to control the gate electrode 629 and hence operation of the transistor 600 by conducting a control signal from a control circuit (not shown) to the gate. Barrier layer 631 is adapted to prevent diffusion of elements from either the line 633 or gate electrode 629 to the other of the line 633 and gate electrode 629.

Meng (EX-2002), [0058]

Petition, 11

Usui, Fig. 8 (Modified)

Ground 3 in Petitioner's Reply (for Claims 11 & 16) Also Fails Because It Is Based on Hindsight

Reply, 16, 19-21;
Sur-Reply, 17-19

Petitioner's Reply

Accordingly, a POSITA would have used Usui's principles to improve electromigration characteristics in Yu's device. Petition, 19-20. Patent Owner's

Reply, 19

electromigration. Ex-1047, ¶61; Ex-1001, 2:53-65, claims 9, 14. Gate leakage can also cause electromigration in gate electrodes. Ex-1047, ¶62; Ex-1018 at 937. This is especially problematic for Schottky connections, where leakage increases exponentially with voltage and temperature. Ex-1047, ¶62, Ex-1015, 353-354.

Reply, 16

Petition. POR, 28-36. For claims 11 and 16, a POSITA would have "implement[ed] the Usui-Yu contact as a *Schottky contact*, as taught by Adesida." Petition, 25-27

Reply, 20

Patent Owner's Sur-Reply

Finally, Petitioner's Reply cannot keep its story straight. Petitioner's sole alleged basis for modifying Yu's transistor based on Usui is to reduce electromigration (Reply, 19-20) which Petitioner alleges is caused by gate leakage that is "especially problematic for Schottky connections" (Reply, 16). Petitioner's assertion that POSAs would have then modified Petitioner's Usui-Yu combination to use a Schottky gate electrode – that Petitioner says would exacerbate electromigration (Reply, 16) – is based on nothing but hindsight.⁵ Petitioner's nonsensical Ground 3 Reply arguments should be rejected.

Sur-Reply, 18-19