

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AMERICAS CORP.,
Patent Owner.

IPR2025-00175
Patent 8,686,562 B2

Before JO-ANNE M. KOKOSKI, CHRISTOPHER M. KAISER, and
LISA A. MURRAY, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We have jurisdiction to conduct this *inter partes* review under 35 U.S.C. § 6, and issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Innoscience America, Inc. (“Petitioner”) does not show by a preponderance of the evidence that claims 1–17 (the “challenged claims”) of U.S. Patent No. 8,868,562 B2 (“the ’562 patent,” Ex. 1001) are unpatentable.

A. Procedural Background

Petitioner filed a Petition to institute an *inter partes* review of claims 1–17 of the ’562 patent. Paper 1 (“Pet.”). Infineon Technologies Americas Corp. (“Patent Owner”) filed a Preliminary Response. Paper 6. Patent Owner did not “file a brief requesting discretionary denial of institution,” so the case was referred to us “to consider the merits and non-discretionary considerations.” Paper 9, 1–2.

Pursuant to 35 U.S.C. § 314(a), we instituted an *inter partes* review of claims 1–17 on the grounds advanced in the Petition on July 10, 2025. Paper 10 (“Dec.”). Patent Owner filed a Patent Owner Response (“PO Resp.,” Paper 17), Petitioner filed a Reply (“Pet. Reply,” Paper 18), and Patent Owner filed a Sur-reply (“PO Sur-reply,” Paper 20).

We held an oral hearing on April 9, 2026, and a transcript is included in the record. Paper 26 (“Tr.”). After the oral hearing, we invited the parties to submit supplemental briefing regarding an argument raised by Petitioner during the oral hearing. Paper 27. Petitioner and Patent Owner subsequently filed Supplemental Briefs. Paper 28; Paper 29.

B. Real Parties-in-Interest

Petitioner identifies itself, Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience (Suzhou) Technology Holding Company, Ltd. as real parties-in-interest. Pet. 67. Patent Owner identifies itself as the real party-in-interest. Paper 3, 1.

C. Related Matters

The parties indicate that the '562 patent is asserted in *Infineon Technologies Austria AG v. Innoscience (Suzhou) Tech. Co., Ltd.*, Case No. 3:24-cv-01553 (N.D. Cal.) and U.S. International Trade Commission Investigation No. 337-TA-1414, *In re Certain Semiconductor Devices and Products Containing the Same*, filed on July 26, 2024. Pet. 67; Paper 3, 1.

D. The '562 Patent

The '562 patent, titled “Refractory Metal Nitride Capped Electrical Contact and Method for Fabricating Same,” is directed to “a contact for implementation as an electrode on a semiconductor device, such as a group III-V power semiconductor device.” Ex. 1001, code (54), 2:19–23. The '562 patent explains that “‘group III-V semiconductor’ refers to a compound semiconductor that includes at least one group III element and at least one group V element, such as, but not limited to, gallium nitride (GaN), gallium arsenide (GaAs), aluminum gallium arsenide (AlGaAs), indium gallium nitride (InGaN) and the like.” *Id.* at 1:6–11. “Analogously, ‘III-nitride semiconductor’ refers to a compound semiconductor that includes nitrogen and at least one group III element, such as, but not limited to, GaN, AlGaN, InN, AlN, InGaN, InAlGaN and the like.” *Id.* at 1:11–15.

Figure 1 is reproduced below.

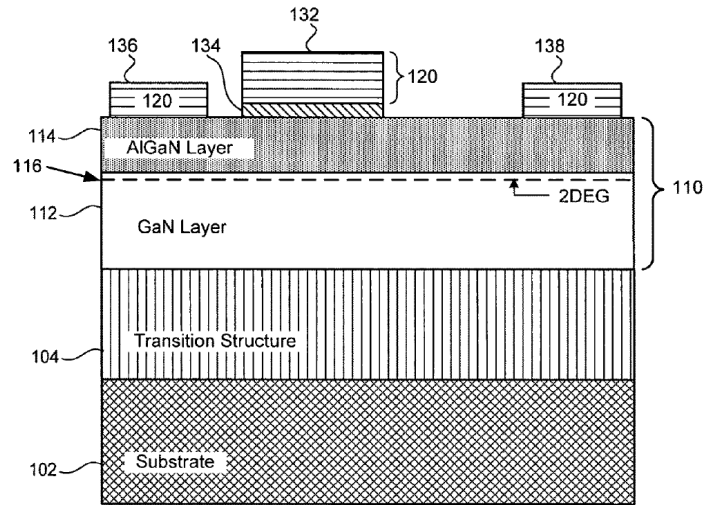


Figure 1 is a block diagram showing a group III-V semiconductor high electron mobility transistor (HEMT) implemented in gallium nitride (GaN). Ex. 1001, 2:53–55. The semiconductor structure includes substrate 102, transition structure 104, and GaN body 110 comprising GaN layer 112 and AlGaN layer 114. *Id.* at 2:55–58. Electrode stack 120 comprises source electrode 136, drain electrode 138, and insulated gate electrode 132. *Id.* at 3:23–25. Insulated gate electrode layer 132 includes gate insulator layer 134. *Id.* at 3:28–31. Electrode stack 120 also includes a refractory metal nitride capping layer (not shown), such as a titanium nitride (TiN) capping layer. *Id.* at 3:26–28.

Figure 2 is reproduced below.

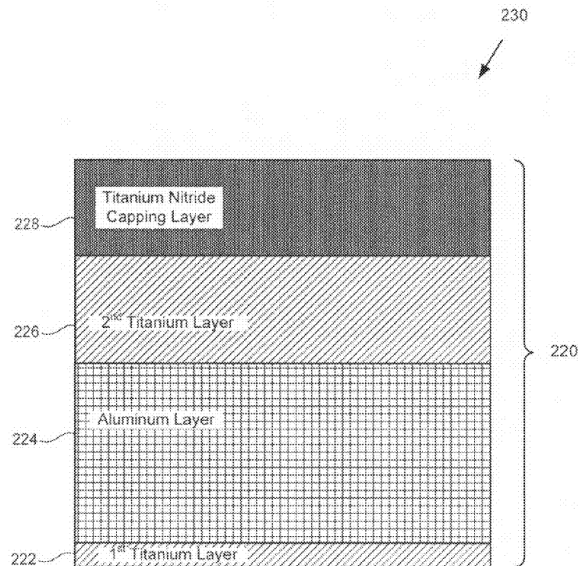


Figure 2 is a block diagram showing one embodiment of a refractory metal nitride capped electrical contact described in the '562 patent.

Ex. 1001, 2:10–13. Electrical contact 230, which corresponds to any of source electrode 136, drain electrode 138, or insulated gate electrode 132 shown in Figure 1, comprises electrode stack 220, which corresponds to electrode stack 120 in Figure 1. *Id.* at 3:39–43. Electrode stack 220 comprises a plurality of metal layers (first titanium (Ti) layer 222, aluminum (Al) layer 224, and second Ti layer 226), and a capping layer comprising a refractory metal nitride (TiN capping layer 228). *Id.* at 3:43–49.

The '562 patent explains that “refractory metal” includes Ti, zirconium, vanadium, niobium, molybdenum, tantalum, and tungsten. Ex. 1001, 3:51–56. The '562 patent also teaches that first Ti layer 222 is approximately 100 Å thick, and Al layer 224 is approximately 1300 Å thick, and second Ti layer 228 is approximately 680 Å thick. *Id.* at 4:25–27, 4:51–55, 4:61–67. TiN capping layer 228 has a thickness of approximately 600 Å. *Id.* at 5:13–17. According to the '562 patent, the

disclosed refractory metal nitride capped electrical contact “presents significant advantages over the conventional art, such as rendering integration of group III-V and group IV semiconductor devices more efficient and cost effective by posing a reduced contamination risk to silicon, or other group IV semiconductor fabrication process flows.” *Id.* at 5:33–39.

E. Illustrative Claim

Petitioner challenges claims 1–17 of the ’562 patent. Claims 1 and 13 are independent. Claim 1 is illustrative; it is reproduced below.

1. An electrical contact for use on a semiconductor device, said electrical contact comprising:

an electrode stack including a plurality of metal layers
and a capping layer formed over said plurality of
metal layers;

said capping layer consisting only of a refractory metal
nitride, said refractory metal nitride forming a top of
said electrical contact and having a thickness greater
than that of a bottommost layer of said plurality of
metal layers.

Ex. 1001, 5:54–63.

F. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–17 are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1, 2, 4–7	102	Usui ²
3, 8, 12, 19, 17	103	Usui, Yu ³
9, 11, 14, 16	103	Usui, Yu, Adesida ⁴
10, 15	103	Usui, Yu, Sugimoto ⁵
1–8, 12, 13, 17	103	Yu, Usui
9, 11, 14, 16	103	Yu, Usui, Adesida
10, 15	103	Yu, Usui, Sugimoto

Pet. 3. Petitioner relies on the Declaration of Yuji Zhao, Ph.D. (Ex. 1002) and the Supplemental Declaration of Yuji Zhao, Ph.D. (Ex. 1047) (collectively, the “Zhao Declarations”) to support its contentions. Patent Owner relies on the Declaration of Edwin Piner, Ph.D. (the “Piner Declaration,” Ex. 2024).

II. ANALYSIS

A. Legal Standards

A claim is anticipated if a single prior art reference either expressly or inherently discloses every limitation of the claim. *Orion IP, LLC v. Hyundai Motor Am.*, 605 F.3d 967, 975 (Fed. Cir. 2010). Although the elements must be arranged or combined the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not

¹ Amendments to 35 U.S.C. §§ 102 and 103 enacted by the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), took effect on March 16, 2013. The ’562 patent issued from an application filed on August 25, 2009. *See* Ex. 1001, code (22). Therefore, we apply the pre-AIA versions of §§ 102 and 103. Neither party, however, argues that the outcome of this case would differ based on applying the post-AIA versions of these laws.

² US 5,943,601, issued Aug. 24, 1999 (Ex. 1004).

³ US 2010/0052066 A1, published Mar. 4, 2010 (Ex. 1005).

⁴ US 2008/0023726 A1, published Jan. 31, 2008 (Ex. 1006).

⁵ US 7,777,252 B2, issued Aug. 17, 2010 (Ex. 1007).

required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2019) (citing *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990)).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and “the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). “While the sequence of these questions might be reordered in any particular case,” *KSR*, 550 U.S. at 407, the U.S. Court of Appeals for the Federal Circuit has repeatedly emphasized that “it is error to reach a conclusion of obviousness until all those factors are considered,” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1328 (Fed. Cir. 2016).

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in an *inter partes* review).

We analyze the asserted grounds with the above-noted principles in mind.

B. Level of Ordinary Skill in the Art

The level of ordinary skill in the pertinent art at the time of the invention is a factor in how we construe patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). It is also one of the factors we consider when determining whether a patent claim is obvious over the prior art. *See Graham*, 383 U.S. at 17–18.

Factors pertinent to a determination of the level of ordinary skill in the art include “(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.” *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). “Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case.” *Id.*

Petitioner contends that a person of ordinary skill in the art (“POSITA” or “POSA”) would have had “at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design,” and “[a]dditional education could substitute for professional experience and vice versa.” Pet. 6 (citing Ex. 1002 ¶¶ 80–82). Patent Owner does not dispute Petitioner’s proposed level of ordinary skill. PO Resp. 1–76. Neither party explains why the

outcome of this case would be affected by the adoption of the proffered definition of a person of ordinary skill in the art.

In the Institution Decision, we adopted the assessment offered by Petitioner. Dec. 6–7. Because Petitioner’s definition of the level of skill in the art is consistent with the ’562 patent and the asserted prior art, we maintain Petitioner’s definition for purposes of this Final Written Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir 2001).

C. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

Based on our review of the complete trial record and the arguments raised by the parties, we determine that it is necessary to address the claim term “electrode stack.”

Claims 1 and 13 recite “an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers.” Ex. 1001, 5:56–58, 6:39. Patent Owner proposes that “electrode stack” be construed as

a stack of conductive layers that form an electrical contact that is part of a semiconductor device and used to (1) establish electrical

contact with a nonmetallic part of the semiconductor device (like the source, drain and Schottky gate electrodes in the '562 Patent specification) or (2) control the operation of the semiconductor device (like the insulated or Schottky gate electrodes in the '562 Patent Specification).

PO Resp. 8–9 (citing Ex. 2024 ¶¶ 80–91). Referring to Figure 1 of the '562 patent (reproduced above in § I.D), Patent Owner argues that source electrode 136 and drain electrode 138, which are formed by electrode stack 120, “are ‘power electrodes’ that touch, and are ‘*ohmically coupled* to[,] the semiconductor.” *Id.* at 5 (citing Ex. 1001, 3:19–28, 1:33–43) (alteration in original). Patent Owner asserts that “[g]ate electrode 132 is ‘an insulated gate electrode’ formed by the same electrode stack 120 but separated from the semiconductor by an insulating oxide layer 134.” *Id.* (citing Ex. 1001, 3:21–33). Patent Owner also asserts that “[i]n other embodiments...gate electrode 132 comprising electrode stack 120 may make Schottky contact with GaN body 110’ with no insulating layer in between.” *Id.* (citing Ex. 1011, 219; Ex. 2024 ¶ 86; Ex. 1002 ¶ 58) (second alteration in original); *see also id.* at 7 (“Fig. 2’s ‘[e]lectrical contact 230 may...correspond to any of source electrode 136, drain electrode 138, or *insulated gate electrode* 132 in FIG. 1.” (second alteration in original)).

Thus, Patent Owner concludes:

[T]he '562 Patent specification uses “electrode stack” to refer to a stack of layers forming an electrode and describes three electrode types: (1) a “power electrode[]” touching (“*ohmically coupled* to”) the nonmetallic semiconductor (EX-1001, 3:19–28, 1:33–43); (2) a transistor gate electrode that controls the flow of electrons or holes through the transistor and touches (make[s] “Schottky contact” with) the nonmetallic semiconductor (*id.*, 3:31–35); and (3) a transistor gate electrode that controls the flow of electrons or holes through the transistor but it is “an insulated gate electrode” separated from the semiconductor by an

insulating layer 134 (*id.*, 3:21–33). *See also id.*, claims 10–12; Ex-1015, 503–505.

Id. at 8 (internal footnote omitted) (second alteration in original).

Petitioner argues that “Patent Owner seeks to limit the meaning of ‘electrode stack’ to three example electrodes given in the specification: an ohmic contact, a Schottky contact, or an insulated gate,” but “[n]either the claims nor the specification support that construction.” Pet. Reply 2 (citing PO Resp. 8–9). Petitioner argues that the Specification does not provide a special definition of “electrode stack” that differs from the ordinary meaning, but instead “uses non-limiting language and does not disavow scope.” *Id.* at 4 (citing Ex. 1047 ¶¶ 23–26). Petitioner points to the Specification’s description of “electrode stack as ‘*including* a plurality of metal layers and a capping layer,’ so it may include other features not expressly described.” *Id.* (citing Ex. 1001, code (57), 3:46–48, Claims 1, 13). Petitioner asserts that “Figure 1 is ‘an *example* group III-V semiconductor device,’ for which Figure 2 provides ‘more detail[,],’” and “[t]he ‘number and character’ of metal layers in the electrode stack of Figures 1 and 2 ‘are merely exemplary.’” *Id.* (citing Ex. 1001, 2:43–46, 3:36–39, 3:60–62).

Petitioner also argues that Patent Owner is adding limitations from examples in the Specification into the claims, and that Patent Owner conflates “electrical contact” with “electrode stack” when neither the claims nor the Specification equate the terms. Pet. Reply 6 (citing Ex. 1047 ¶¶ 16–27). In particular, Petitioner argues that Patent Owner relies on “Figures 1 and 2 to attempt to (i) limit the scope of the term ‘electrode stack’ to just three types of electrodes and (ii) to require either direct contact between a metal layer and a semiconductor or a thin insulating material between a

metal layer and a semiconductor.” *Id.* at 6–7 (citing PO Resp. 4–9; Ex. 2024 ¶¶ 81–91).

Petitioner argues that “electrode stack” should be given its plain and ordinary meaning, and that “electrodes ‘deliver, receive, collect, emit, deflect or control electric charge carriers’ and provide a current path,” and “[a] POSITA would have understood that not every electrode is a source contact, drain contact, Schottky gate, or insulated gate.” *Id.* at 8 (citing Ex. 1047 ¶¶ 38–39); *see also* Tr. 9 (Petitioner’s counsel stating that “the electrode part” of the electrode stack “is the part that the parties are arguing about,” and “a POSITA would interpret the plain meaning that it requires—that it just provides a path for current entering and leaving a medium, that it’s something that could deliver, receive, collect, emit, deflect or control electric charge carriers.”). Patent Owner responds that “Petitioner’s definition limiting an electrode to ‘provid[ing] the path for current **entering or leaving** a medium, such as *a . . . semiconductor*’ is largely consistent with Infineon’s construction.” PO Sur-reply 2 (citing Pet. Reply 7–8) (alterations in original).

Having reviewed the claim language, the Specification, and the evidence from the complete record now before us, we determine that an “electrode stack” is “a conductor that provides a path for current entering or leaving a medium such as a semiconductor device.”

We begin our analysis with the language of the claims. *Phillips*, 415 F.3d at 1312; *see also SuperGuide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 874–875 (Fed. Cir. 2004) (“There is a ‘heavy presumption’ that the terms used in the claims ‘mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the

relevant art.”). The language of claims 1 and 13 requires that the “electrode stack” of the “electrical contact” include “a plurality of metal layers” and “a capping layer” formed thereover. Ex. 1001, 5:54–58, 6:37–41. Claims 1 and 13 also recite that the capping layer consists only “of a refractory metal nitride” (claim 1) or “a metal selected from the group consisting of titanium nitride (TiN) and tantalum nitride (TaN)” (claim 13) that forms “a top of said electrical contact” and has “a thickness greater than that of a bottommost layer of said plurality of metal layers.” *Id.* at 5:59–63, 6:42–47. A plain reading of the claim text reveals that that the recited “electrode stack” includes a plurality of metal layers and a capping layer that includes the recited metals and has the recited thickness.

We turn next to the Specification. *Phillips*, 415 F.3d at 1315; *see also SuperGuide*, 358 F.3d at 875 (“We review the patent’s written description and drawings to confirm that the patentee’s use of the disputed term is consistent with the meaning given to it by the court.”); *Brown v. 3M*, 265 F.3d 1349, 1352 (Fed. Cir. 2001) (finding that the plain reading of the claim text is sufficient to construe terms that “are not technical terms of art” and, therefore, “do not require elaborate interpretation.”).

The “Background of the Invention” section of the Specification states that “conventional approaches” to forming electrical contacts in group III-V semiconductor devices such as III-nitride power transistors “utilized aluminum as part of an *electrode stack*, and a noble metal, such as gold to form a capping layer of the stack. As a specific example, an electrical contact stack comprising pure films of titanium, aluminum, and nickel, capped with gold, has been widely used.” Ex. 1001, 1:36–43 (emphasis added). The Specification states that drawbacks of this approach include

“that gold has been found to diffuse through the electrode stack, as well as capping it, so that some gold undesirably appears at the interface of the electrical contact and the III-nitride semiconductor body” and that gold as a capping layer has the “propensity to contaminate a silicon fabrication process flow.” *Id.* at 1:46–52. The inventors sought to overcome these drawbacks “by providing an electrical contact for use on a group III-V semiconductor device that renders integration of group III-V and group IV semiconductors more efficient and cost effective by posing a reduced contamination risk to silicon, or other group IV semiconductor fabrication process flows.” *Id.* at 1:56–62.

The Specification consistently describes the electrode stack as metal layers stacked on another with a capping layer on top. Figures 1 and 2 of the '562 patent are reproduced again below:

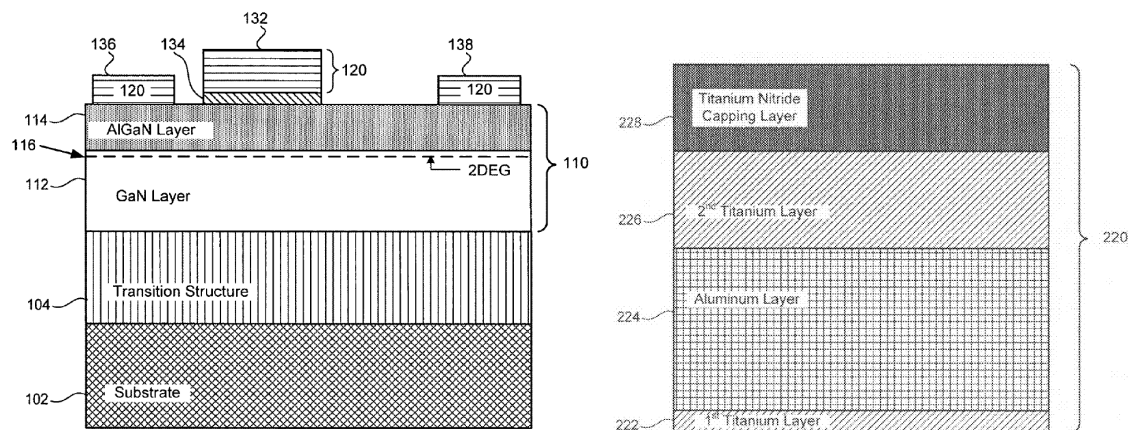


Figure 1 (on the left) is a block diagram of a group III-V semiconductor device including a plurality of refractor metal nitride capped electrical contacts, and Figure 2 (on the right) is a more detailed block diagram of a refractory metal nitride capped electrical contact, according to one embodiment described in the '562 patent. Ex. 1001, 2:6–12. Figure 1 includes source electrode 136, drain electrode 138, and insulated gate

electrode 132, each of which comprises electrode stack 120. *Id.* at 2:58–60, 3:23–25. The Specification explains that “[e]lectrode stack 120 includes a refractory metal nitride capping layer (not explicitly shown in FIG. 1), such as a titanium nitride (TiN) capping layer, for example.” *Id.* at 3:26–28. Electrode stack 220 (shown in Figure 2) “corresponds to electrode stack 120 in FIG. 1” and “includes first titanium (Ti) layer 222, aluminum (Al) layer 224, second Ti layer 226, and TiN capping layer 228.” *Id.* at 3:42–45. The Specification explains that, “[m]ore generally, electrode stack 220 corresponds to an electrode stack including a plurality of metal layers, e.g., first Ti layer 222, Al layer 224, and second Ti layer 226, and a capping layer comprising a refractory metal nitride.” *Id.* at 3:46–49.

The Specification teaches that “the number and character of the plurality of metal layers 222, 224, and 226 of electrode stack 220 are merely exemplary, and, in other embodiments, “electrode stack 220 may comprise more, or fewer, metal layers underlying the refractory metal nitride capping layer, e.g., TiN capping layer 228, and the plurality of metal layers may be different from those shown in FIG. 2.” Ex. 1001, 3:60–66. The Specification also describes the steps of a method of fabricating a refractory metal nitride capped electrical contact according to one embodiment, in which first Ti layer 222 of electrode stack 120 is deposited over GaN body 110 formed over substrate 102, followed by the formation of Al layer 224 over Ti layer 222, second Ti layer 226 over Al layer 224, and TiN capping layer 228 over second Ti layer 226. *Id.* at 4:4–5:22. The described method includes deposition techniques and layer thicknesses. *Id.*

Read as a whole, the Specification supports the conclusion that an “electrode stack” includes a stack of metal layers with a capping layer that

comprises the recited metals and has the recited thickness, which forms an electrical contact for use on a semiconductor device generally or a group III-V semiconductor in particular. This is consistent with our determination that “electrode stack” is a conductor that provides a path for current entering or leaving a medium such as a semiconductor device

We disagree with Patent Owner that “electrode stack” as used in the challenged claims should be limited to the specific electrodes shown in the embodiments described in the Specification. *See* PO Resp. 4–9. Although the Specification describes embodiments using source, drain, and Schottky gate electrodes as electrical contacts, we see no reason to construe the term “electrode stack” itself to be limited to these components as Patent Owner proposes. Claims 1 and 13 expressly recite that electrode stacks comprise the claimed “electrical contact,” without expressly including or precluding any specific type of electrode. Ex. 1001, 5:54–63, 6:37–47. The Federal Circuit advises that the Specification “is not a substitute for, nor can it be used to rewrite, the chosen claim language. ‘Specifications teach. Claims claim.’” *SuperGuide*, 358 F.3d at 875 (quoting *SRI Int’l v. Matsushita Elec. Corp. of Am.*, 775 F.2d 1107, 1121 n.14 (Fed. Cir. 1985) (en banc)). The Specification does teach electrical contacts that include source, drain, and Schottky gate electrodes, but claims 1 and 13 are directed to electrical contacts that are not expressly so limited. Patent Owner’s proposed construction would effectively rewrite the claim by adding limitations, which we decline to do under the guise of claim construction. *See id.* (“Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not a part of the claim.”).

In view of the foregoing, we construe the claim term “electrode stack” to mean “a conductor that provides a path for current entering or leaving a medium such as a semiconductor device.”

D. Ground 1: Asserted Anticipation by Usui

Petitioner asserts that claims 1, 2, and 4–7 are anticipated by Usui, and relies on the Zhao Declarations to support its assertions. Pet. 10–16; Pet. Reply 8–16. Patent Owner disagrees with Petitioner’s assertions and relies on the Piner Declaration. PO Resp. 10–20; PO Sur-reply 3–11.

1. Overview of Usui

Usui is directed to a method of fabricating a metallization structure “having an aluminum and/or aluminum alloy layer that exhibits enhanced electromigration characteristics.” Ex. 1004, 1:5–9. Usui seeks “to provide a structure that exhibits enhanced electromigration performance along with being hillock free and without a concomitant loss in the dry etchability characteristic and corrosion resistant characteristic of the structure.” *Id.* at 2:34–39. According to Usui, the fabricated metallization structures “are especially useful for forming electrical connections or wiring such as between active and/or passive devices of an integrated circuit structure.” *Id.* at 1:11–14.

Figure 1 of Usui is reproduced below.

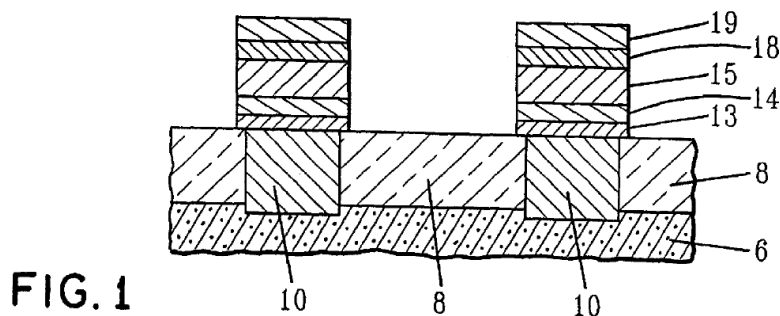


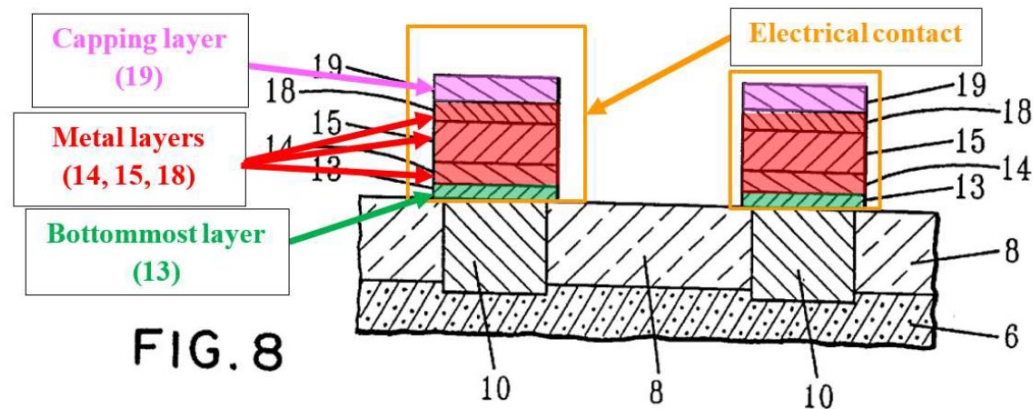
Figure 1 is a cross-sectional view of an embodiment of an interconnect metallurgy structure disclosed in Usui. Ex. 1004, 3:2–4. The interconnect metallurgy structure “preferably comprises a 4 or 5 layer structure over an interplanar stud connection 10 surrounded by an insulator 8 to make connection to a device substrate 6.” *Id.* at 3:24–27. Underlayer 13 is composed of a group IVA metal, preferably titanium, and is about 90 to about 110 Å thick. *Id.* at 3:27–32. Layer 15 is an aluminum or aluminum alloy that is in electrical contact with underlayer 13, and typically has a thickness of about 2000 to about 6000 Å. *Id.* at 3:38–40, 3:47–49. Titanium nitride layer 14 is located between underlayer 13 and aluminum or aluminum alloy layer 15, and has a thickness of about 50 to about 500 Å. *Id.* at 3:58–65. Above aluminum or aluminum alloy layer 15 is titanium layer 18 and capping layer 19. *Id.* at 3:67–4:6. Titanium layer 18 is about 50 to about 200 Å thick, and capping layer 19 is typically about 150 to about 800 Å thick. *Id.* at 4:6–9.

Usui teaches that “[c]ritical to the success of the present invention is having the thickness of this underlayer 13 being between about 90 angstroms to about 110 angstroms” because “by limiting the thickness of this underlayer 13, the structure and texture of the subsequently to be applied metallic layers is carefully controlled.” Ex. 1004, 3:29–35. Usui further teaches that controlling the thickness of underlayer 13 is “essential in achieving” the properties of the structure. *Id.* at 3:35–36.

2. Claim 1

Petitioner contends that Usui discloses all of the limitations of claim 1. Pet. 10–13.

Petitioner provides an annotated version of Usui's Figure 8, reproduced below, to illustrate its contentions.



Usui's Figure 8, as annotated by Petitioner, is a cross-sectional view of a step of the fabrication process of the preferred interconnect metallurgy structure described in Usui, with Petitioner's addition of colored shading and labels identifying different components of the structure. Pet. 11; Ex. 1004, 3:5–7, Fig. 8.

Referring to annotated Figure 8, Petitioner contends that Usui discloses the “an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers” limitation of claim 1. Pet. 11. Petitioner contends that Usui's titanium layer 18, aluminum or aluminum alloy layer 15, and titanium nitride layer 14 (all shaded red), and titanium underlayer 13 (shaded green) together form the claimed “plurality of metal layers.” *Id.* (citing Ex. 1004, 3:38–41, 3:58–60, 4:4–5, 5:38, 5:52, Figs. 1, 8; Ex. 1002 ¶ 90). Petitioner then identifies layer 19 (shaded pink) that forms the top of the metallization structure (orange box labelled “Electrical contact”) as the claimed “capping layer formed over said plurality of metal layers.” *Id.* (citing Ex. 1004, Abs., 3:2–8, 5:54–59, Figs. 1, 8; Ex. 1002 ¶ 91).

Petitioner also contends that Usui discloses the “said capping layer consisting only of a refractory metal nitride forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers” limitation of claim 1. Pet. 12–13. In particular, Petitioner contends that “capping layer 19 is formed only of titanium nitride,” which a POSITA would have known is a refractory metal nitride, and “forms a top of the metallization structure (electrical contact).” *Id.* at 12 (citing Ex. 1004, 5:54–59; Ex. 1002 ¶¶ 71–73, 92). Petitioner identifies underlayer 13 (shaded green) comprising a thickness of about 90–110 Å as the recited “bottommost layer of said plurality of metal layers.” *Id.* at 12–13 (citing Ex. 1004, 3:29–35). Petitioner further contends that capping layer 19 “has a thickness of about 150–800 Å . . . which is greater than the thickness of underlayer 13 (bottommost layer of plurality of metal layers).” *Id.* at 13 (citing Ex. 1004, 5:38, 5:52, Figs. 1, 8; Ex. 1002 ¶ 94).

As set forth above, we construe “electrode stack” to mean “a conductor that provides a path for current entering or leaving a medium such as a semiconductor device.” Thus, Petitioner must show that Usui’s layers 13–15, 18, and 19 provide a path for current entering or leaving a medium such as a semiconductor device. After reviewing the complete trial record, we are not persuaded that Petitioner has done so.

Petitioner relies on the testimony of Dr. Zhao to support its contention that the identified layers in Usui’s interconnect metallurgy structure form an “electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers” as recited in claim 1. *See* Pet. 11–12 (citing Ex. 1002 ¶¶ 89–91). Neither Petitioner nor Dr. Zhao, however, provide adequate explanation or evidence as to why Usui’s

interconnect metallurgy structure forms an “electrode stack,” i.e., a conductor that provides a path for current entering or leaving a medium such as a semiconductor device. Dr. Zhao’s testimony merely repeats the disclosures in Usui and concludes, without further technical detail, explanation, or reference to objective evidence, that Usui’s Figure 8 discloses an electrode stack. Ex. 1002 ¶¶ 89–91. Dr. Zhao’s testimony sets forth Petitioner’s conclusory assertions as though they are facts, rather than setting forth facts and evidence in support of those assertions. *Compare id. with* Pet. 11–12. Absent underlying facts or evidence to support Dr. Zhao’s opinion, the cited testimony “adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight.” *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential).

In contrast, Patent Owner’s declarant Dr. Piner testifies, with evidentiary support, that interconnects (such as Usui’s interconnect metallurgy structure) and electrical contacts (such as that claimed in the ’562 patent) are not the same thing. *See* Ex. 2024 ¶¶ 63–70. For example, Dr. Piner explains:

In other words, not all metals in a semiconductor device have the same purpose and could not be said to be interchangeable. By August 2009 it was well known to a POSA how to discern if a metal component in a transistor is an interconnect or serves as an electrical contact such as a gate contact or ohmic contact, based on the structure and functionality of the metal component. For example, interconnects are made up of metal strips and are deposited on insulators. EX-1011 (Mishra) at 216. Interconnects are low resistance conductors that can carry very high current densities. *Id.*, 216, 217. Unlike Schottky contacts and ohmic contacts, interconnects do not provide non-linear IV response like Schottky contacts nor inject

electrons and holes into semiconductors like ohmic contacts. *Id.*, 218. As many of the references cited by Dr. Zhao illustrate, electrical contacts had their own highly complex design challenges. EX-1008 (Pearton), 41-59 (Pages 53-71 of 383) (discussing electrical contacts); EX-1017 (Kramer), 11-126 (Pages 18-130 of 151) (same). And while Dr. Zhao cites these as supporting a POSA's knowledge of an electrical contact, none of these references describe electrical contacts as interconnects.

Id. ¶ 71. Dr. Piner further testifies that Usui's interconnect metallurgy structure is an interconnect, and not an electrical contact, because "Usui states that '[t]he structures fabricated by the process of the present invention are especially useful for forming *electrical connections or wiring* such as *between* active and/or passive *devices* of an integrated circuit structure.'" *Id.* ¶ 148 (citing Ex. 1004, 1:11–14) (alteration in original); *see also id.* ¶¶ 150–151 (Dr. Piner testifying that Usui's interconnect metallization structure is not an "electrode stack" under a broad definition of electrode). Dr. Piner's testimony in this regard rebuts Petitioner's and Dr. Zhao's conclusory assertions to the contrary.

We note that in the Reply, Petitioner argues that Usui's interconnect metallurgy structure "meets even Patent Owner's narrow construction" of "electrode stack." Pet. Reply 9 (citing Ex. 1047 ¶¶ 40–63). Because we do not adopt Patent Owner's construction of "electrode stack," we are not persuaded that Petitioner's arguments in this regard sufficiently show that Usui discloses an "electrode stack" as recited in claim 1. *See id.* at 9–16.

For these reasons, after considering the parties' arguments and evidence, we determine that Petitioner does not meet its burden of establishing, by a preponderance of the evidence, that Usui discloses "an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers" as recited in claim 1.

Accordingly, we find that Petitioner has not established by a preponderance of the evidence that claim 1 is anticipated by Usui.

3. *Claims 2 and 4–7*

Claims 2 and 4–7 depend, directly or indirectly, from claim 1. Ex. 1001, 6:1–2, 6:5–17. Because, as discussed above, Petitioner does not show that claim 1 is anticipated by Usui, Petitioner has not shown that claims 2 and 4–7 are anticipated by Usui.

E. Grounds 2–4: Asserted Obviousness over Usui and Yu; Usui, Yu and Adesida; and Usui, Yu and Sugimoto

Petitioner contends that (1) claims 3, 8, 12, 13, and 17 would have been obvious over the combined teachings of Usui and Yu (Pet. 16–23; Pet. Reply 17–20); (2) claims 9, 11, 14, and 16 would have been obvious over the combined teachings of Usui, Yu, and Adesida (Pet. 24–29; Pet. Reply 20–22); and (3) claims 10 and 15 would have been obvious over the combined teachings of Usui, Yu, and Sugimoto (Pet. 29–33; Pet. Reply 22–24).

Claims 3 and 8–12 depend, directly or indirectly, from claim 1. Ex. 1001, 6:3–35. Petitioner does not rely on Yu, Adesida, or Sugimoto to remedy the deficiencies identified above with respect Petitioner’s challenge to claim 1. *See* Pet. 16–33; Pet. Reply 17–24. Because Petitioner does not show that Usui discloses all of the limitations of claim 1, for the same reasons Petitioner does not show that (1) claims 3, 8, and 12 would have been obvious over the combined teachings of Usui and Yu; (2) claims 9 and 11 would have been obvious over the combined teachings of Usui, Yu, and Adesida; or (3) claim 10 would have been obvious over the combined teachings of Usui, Yu, and Sugimoto. *See* § II.D.2, *supra*.

Independent claim 13, like claim 1, recites “an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers.” Ex. 1001, 6:36–47. Petitioner contends that Usui discloses this limitation of claim 13 for the same reasons set forth above with respect to Petitioner’s contention that claim 1 is anticipated by Usui. Pet. 23 (citing Ex. 1002 ¶ 124). Because Petitioner does not show that claim 1 is anticipated by Usui, Petitioner has not shown that claim 13 would have been obvious over the combined teachings of Usui and Yu. *See* § II.D.2, *supra*.

Claims 14–17 depend from claim 13. Ex. 1001, 6:48–61. Petitioner does not rely on Yu, Adesida, or Sugimoto to remedy the deficiencies identified above with respect to Petitioner’s challenge to claim 13. *See* Pet. 16–33; Pet. Reply 17–24. Because Petitioner does not show that the combined teachings of Usui and Yu discloses all of the limitations of claim 13, for the same reasons Petitioner does not show that (1) claim 17 would have been obvious over the combined teachings of Usui and Yu; (2) claims 14 and 16 would have been obvious over the combined teachings of Usui, Yu, and Adesida; or (3) claim 15 would have been obvious over the combined teachings of Usui, Yu, and Sugimoto.

F. Ground 5: Asserted Obviousness over Yu and Usui

Petitioner asserts that claims 1–8, 12, 13, and 14 would have been obvious over the combined teachings of Yu and Usui, and relies on the Zhao Declarations to support its assertions. Pet. 33–55; Pet. Reply 24–28. Patent Owner disagrees with Petitioner’s assertions and relies on the Piner Declaration. PO Resp. 43–68; PO Sur-reply 21–29.

1. Overview of Yu

Yu relates to “semiconductor devices having doped-conducting metal oxide and methods for forming such semiconductor devices.” Ex. 1005 ¶ 6. Yu explains that “[t]he doped-conducting metal oxide can provide desired work function values and thermal stability.” *Id.*

Figure 2E is reproduced below.

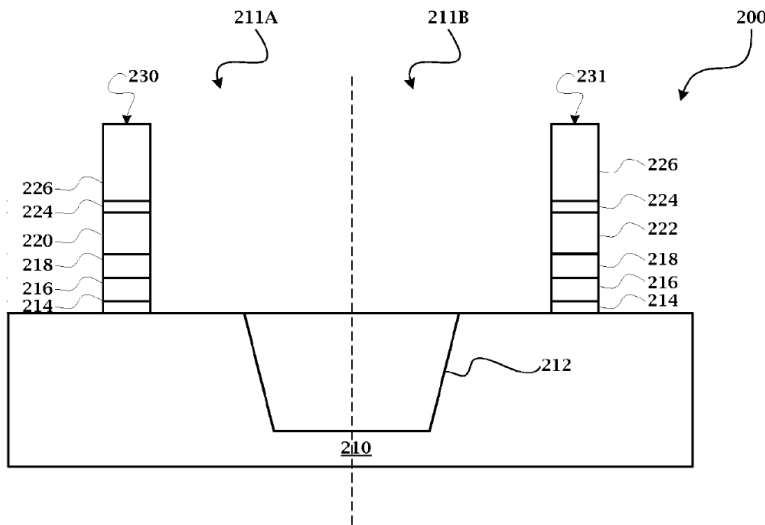


FIG. 2E

Figure 2E is a cross-sectional view of one embodiment of a semiconductor device described in Yu during a fabrication stage. Ex. 1005 ¶ 8.

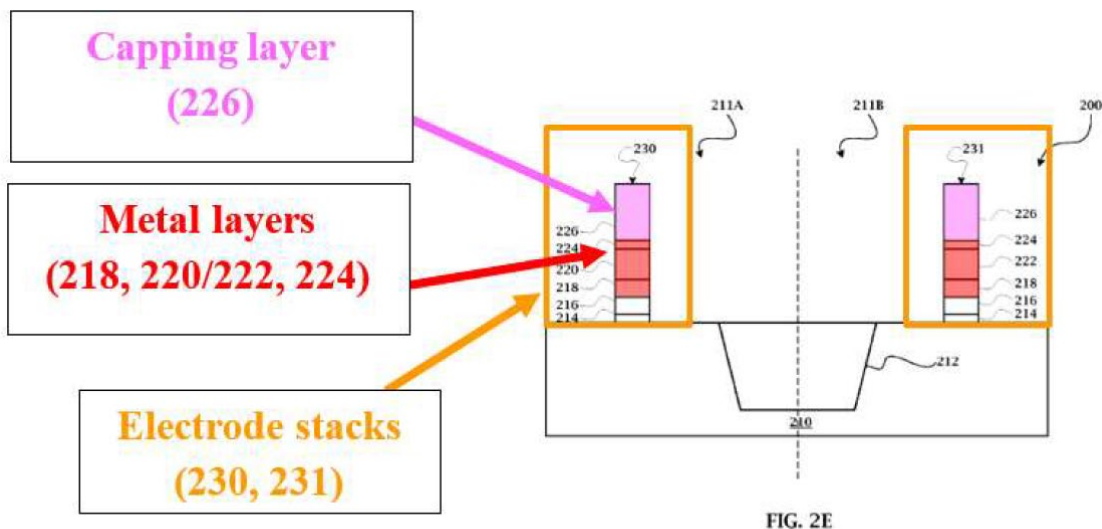
Semiconductor device 200 includes semiconductor substrate 210, isolation region 212, first metal gate stack 230 in active/NMOS region 211A, and second metal gate stack 231 in active/PMOS region 211B. *Id.* ¶¶ 22, 37. Metal gate stacks 231, 232 comprise interfacial dielectric layer 214, high-k dielectric layer 216, diffusion barrier/protection layer 218, first metal layer 220 (in first metal gate stack 230), second metal layer 222 (in second metal gate stack 231), diffusion barrier layer 224, and capping layer 226. *Id.* ¶¶ 38–39.

Yu teaches that “capping layer 226 may include metal (e.g., an aluminum-based, tungsten, or copper material)” that “comprise[s] a thickness between about 50 Å and about 1,000 Å, preferably about 200 Å.” Ex. 1005 ¶ 36. Yu further teaches that, “[i]n alternate embodiments, the capping layer 226 may comprise any suitable thickness.” *Id.* Yu further teaches that diffusion barrier/protection layer 218 may comprise titanium, titanium nitride, tantalum, tantalum nitride and/or combinations thereof. *Id.* ¶ 29. Yu describes an embodiment wherein diffusion barrier/protection layer 218 comprises titanium nitride at a thickness of approximately 20 Å. *Id.* According to Yu, “in alternate embodiments, the diffusion barrier layer 218 comprises any suitable thickness.” *Id.*

2. Claims 1 and 13

Petitioner contends that the combined teachings of Yu and Usui teach all of the limitations of claims 1 and 13. Pet. 10–13, 54–55.

Petitioner provides an annotated version of Yu’s Figure 2E, reproduced below, to illustrate its contentions.



Pet. 42. Yu's Figure 2E is a cross-sectional view of an embodiment of a semiconductor device during fabrication according to the method described in Yu. Ex. 1005 ¶ 10. Petitioner's annotations include identifying the capping layer with pink shading, the metal layers with red shading, and the electrode stacks with an orange box. Pet. 42.

With respect to the limitation “an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers” in claims 1 and 13, Petitioner points to Yu's metal gate stacks 230, 231. Pet. 42, 55. Specifically, Petitioner contends that metal gate stacks 230, 231 are “electrode stacks” that include a “plurality of metal layers” diffusion barrier/protection layer 218, metal layers 220, 222, diffusion barrier layer 224, and capping layer 226 formed over the metal layers. *Id.* at 42 (citing Ex. 1005 ¶¶ 29, 35, 36, Fig. 2E; Ex. 1002 ¶ 162). Petitioner also contends that Yu teaches “said capping layer consisting only of a refractory metal nitride” because it discloses that capping layer 26 is titanium nitride or tantalum nitride, which a POSITA would have known “are each a ‘refractory metal nitride.’” *Id.* at 42–43 (citing Ex. 1005 ¶ 36; Ex. 1002 ¶¶ 71–73, 163).

With respect to the “said refractory metal nitride/metal forming a top of said electrical contact and having a thickness greater than that of a bottommost layer of said plurality of metal layers” limitation of claims 1 and 13, Petitioner contends that capping layer 226 comprising titanium nitride or tantalum nitride forms a top of metal gate stacks 230, 231. Pet. 43 (citing Ex. 1005 ¶¶ 36, 40, Fig. 2E), 55 (citing Ex. 1002 ¶ 186). Petitioner identifies diffusion barrier/protection layer 218 as the recited “bottommost

layer of said plurality of metal layers.” *Id.* at 43 (citing Ex. 1005 ¶ 29, Fig. 2E). Petitioner contends:

While Yu discloses the capping layer is *preferably* 600 Å and the bottommost layer 20 Å (i.e., the capping layer is *preferably* thicker than the bottommost layer), this disclosure is made with respect to the capping layer being polysilicon, which is not a refractory metal nitride as stated in claims 1 and 13. However, Yu teaches the capping layer may be titanium nitride and tantalum nitride, which are refractory metal nitrides. A POSITA would have been motivated to replace Yu’s polysilicon with either its disclosed titanium nitride or tantalum nitride using the same disclosed thickness because the benefits of refractory metal nitrides are well-known and this would have been an obvious design alternative as explained by Dr. Zhao.

Id. at 38 (citing Ex. 1005 ¶¶ 36, 40; Ex. 1002 ¶¶ 71–73, 155) (internal citations omitted).

Patent Owner argues that Petitioner does not establish that “Yu’s diffusion barrier/protection layer 218 is a layer of Yu’s *electrode stack*.” PO Resp. 49. Patent Owner also argues that there is no support for Petitioner’s assertion that Yu’s metal gate stacks 230, 231 are electrode stacks. *Id.* at 50–55. Patent Owner further argues that Petitioner does not establish that the combined teachings of Yu and Usui teach a capping layer “having a thickness greater than that of a bottommost layer of said plurality of metal layers.” *Id.* at 55–65.

As set forth above, we construe “electrode stack” to mean “a conductor that provides a path for current entering or leaving a medium such as a semiconductor device.” Thus, Petitioner must show that Yu’s metal gate stacks 230, 231 provide a path for current entering or leaving a medium such as a semiconductor device. After reviewing the complete trial record, we are not persuaded that Petitioner has done so.

As shown above in Petitioner’s annotated version of Yu’s Figure 2E, Yu’s metal gate stacks 230, 231 include dielectric layers 214 and 216 in addition to what Petitioner identifies as “a plurality of metal layers” (layers 218, 220, 222, 224) and “a capping layer formed over said plurality of metal layers” (layer 226). Ex. 1005 ¶¶ 27–30, 35, 36, Fig. 2E. Petitioner points to Dr. Zhao’s testimony to support its conclusory assertion that metal gate stacks 230, 231 are “electrode stacks” as recited in claim 1. Pet. 42 (citing Ex. 1002 ¶ 162). But neither Petitioner nor Dr. Zhao provide an adequate explanation of why or how dielectric layers 214 and 216 are part of the “electrode stack,” i.e., a conductor that provides a path for current entering or leaving a medium such as a semiconductor device. Dr. Zhao’s testimony repeats, *verbatim*, Petitioner’s conclusory arguments, and does not provide any explanation or statements supporting why Dr. Zhao determines that Yu’s metal gate stacks 230, 231 (including dielectric layers 214 and 216) are the recited “electrode stack.” Compare Ex. 1002 ¶ 167, with Pet. 42. Absent underlying facts or evidence to support Dr. Zhao’s opinion, the cited testimony “adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight.” *Xerox*, Paper 9 at 15.

Additionally, Petitioner argues that “the analysis as presented in the declaration and the Petition focused on the claimed features—the metal layers and capping layers—not the non-conducting dielectric.” Pet. Reply 27 (citing Pet. 33–55; Ex. 1002 ¶¶ 149–187; Ex. 2026, 90:25–91:17). “Electrode stack,” however, is also an element of the claim, and Petitioner explicitly states that Yu “discloses metal gate stacks 230, 231 (electrode stacks).” Pet. 42, 55; *see also Harmonic*, 815 F.3d at 1363 (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify

“with particularity . . . the evidence that supports the grounds for the challenge to each claim.”)). Because Petitioner identified Yu’s metal gate stacks 230, 231 in their entirety as the recited “electrode stack,” Petitioner must show that all of the layers in metal gate stacks 230, 231, including dielectric layers 214 and 216, together form a conductor that provides a path for current entering or leaving a medium such as a semiconductor device. Petitioner’s acknowledgment that dielectrics are nonconductors undercuts its arguments in this regard. *See* Pet. Reply 27.

After considering the complete record, and for the reasons set forth above, we are not persuaded that Petitioner adequately establishes that Yu teaches “an electrode stack including a plurality of metal layers and a capping layer formed over said plurality of metal layers” as recited in claims 1 and 13.⁶ Accordingly, we determine that Petitioner does not establish by a preponderance of the evidence that claims 1 and 13 would have been obvious over the combined teachings of Yu and Usui.

3. *Claims 2–8, 12, and 17*

Claims 2–8 and 12 depend, directly or indirectly, from claim 1. Ex. 1001, 6:1–21, 6:31–35. Claim 17 directly depends from claim 13. *Id.* at 6:57–61. Because, as discussed above, Petitioner does not show that claims 1 and 13 would have been obvious over the combined teachings of Yu and Usui, Petitioner has not shown that claims 2–8, 12, and 17 would have been obvious over the combined teachings of Yu and Usui.

⁶ Petitioner does not rely on Usui with respect to this limitation. *See* Pet. 38 (“Yu expressly discloses every element of claims 1 and 13 except a refractory metal nitride capping layer having a thickness greater than that of a bottommost layer (claim element [1c]).”), 42.

G. Grounds 6 and 7: Asserted Obviousness over Yu, Usui, and Adesida or Sugimoto

Petitioner contends that claims 9, 11, 14, and 16 would have been obvious over the combined teachings of Yu, Usui, and Adesida, and claims 10 and 15 would have been obvious over the combined teachings of Yu, Usui, and Sugimoto. Pet. 55–64. Claims 9–11 indirectly depend from claim 1, and claims 14–16 directly depend from claim 13. Ex. 1001, 6:22–30, 6:48–56. Petitioner does not rely on Adesida or Sugimoto to remedy the deficiencies identified above with respect to Petitioner’s contention that claims 1 and 13 would have been obvious over the combination of Yu and Usui. See Pet. 55–64. Accordingly, for the reasons set forth above with respect to Ground 5, we determine that Petitioner does not establish by a preponderance of the evidence that claims 9, 11, 14, and 16 would have been obvious over the combined teachings of Yu, Usui, and Adesida, or that claims 10 and 15 would have been obvious over the combined teachings of Yu, Usui, and Sugimoto. See § II.F.2, *supra*.

III. CONCLUSION⁷

After considering the briefs, evidence, and oral arguments in this case, we determine that Petitioner has not proven by a preponderance of the evidence that any of claims 1–17 of the ’562 patent is unpatentable.

⁷ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

The following table summarizes the outcome for the challenged claims of this Final Written Decision:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1, 2, 4–7	102	Usui		1, 2, 4–7
3, 8, 12, 13, 17	103(a)	Usui, Yu		3, 8, 12, 13, 17
9, 11, 14, 16	103(a)	Usui, Yu, Adesida		9, 11, 14, 16
10, 15	103(a)	Usui, Yu, Sugimoto		10, 15
1–8, 12, 13, 17	103(a)	Yu, Usui		1–8, 12, 13, 17
9, 11, 14, 16	103(a)	Yu, Usui, Adesida		9, 11, 14, 16
10, 15	103(a)	Yu, Usui, Sugimoto		10, 15
Overall Outcome				1–17

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has not demonstrated by a preponderance of the evidence that any of claims 1–17 of the '562 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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