

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

COMCAST CABLE COMMUNICATIONS, LLC,
Petitioner,

v.

ENTROPIC COMMUNICATIONS, LLC,
Patent Owner.

Patent No. 11,785,275
Filing Date: September 30, 2022
Issue Date: October 10, 2023
Title: SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL

Inter Partes Review No.: IPR2025-00181

DECLARATION OF DAVID B. LETT

**IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.***

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I, David B. Lett, declare that I have personal knowledge of the facts set forth in this declaration and, if called to testify as a witness, could and would do so competently.

1. INTRODUCTION

1. I have been retained as an expert witness on behalf of the Petitioner, Comcast Cable Communications, LLC, for the above-referenced *inter partes* review proceeding.

2. I have been asked to provide a declaration regarding certain matters pertaining to U.S. Patent No. 11,785,275 (“the ’275 patent”) (Ex. 1101) and the unpatentability grounds set forth in the Petition for this proceeding. My experience with television distribution systems, Set Top Boxes (STBs), modulation schemes, radio frequency systems, Video on Demand (VOD), and content delivery systems provides me with an understanding of the subject matter described and claimed in the ’275 patent.

3. I am being compensated at my usual consulting rate or testimony rate of \$385 per hour. My compensation is in no way dependent upon my opinions or testimony or the outcome of this proceeding. I have no financial interest in the party or in the outcome of this proceeding.

2. PROFESSIONAL BACKGROUND AND QUALIFICATIONS

4. I am a technical consultant and product development industry veteran with expertise in electronics, software, hardware, video, audio, and data communications, having led product development organizations in cable, satellite, consumer electronics, home automation, asset tracking, remote tank logistics, and alarm industries. My current curriculum vitae is attached as Ex. 1103 and some highlights follow.

5. I earned my B.S. in Electrical Engineering (1982) with high honors from the University of Tennessee in Knoxville, Tennessee. I also attended the Georgia Institute of Technology from 1986 to 1987, completing 40% of the required degree hours for the M.S. Electrical Engineering program.

6. From 1982 to 1985, I worked at Scientific Atlanta as an Electrical Engineer designing video, audio, and data communications equipment for the cable television industry. I designed software and hardware including addressable data transmitters, video sync suppression scramblers, transaction format converters, and data channel monitors for addressable Cable Television systems and Set Top Boxes.

7. From 1983 to 1985, while working at Scientific Atlanta, I also worked as an Assistant Professor at DeVry Institute of Technology, teaching courses in electronics and microprocessor hardware/software.

8. From 1985 to 1990, I worked at Wegener Communications as a Senior Electrical Engineer, designing satellite communications equipment including forward error correction (FEC) coding systems, PSK modems, and analog control systems for RF modulators and PSK demodulators. I was promoted to the Hardware Engineering Manager, where I managed product development of video, audio, and data satellite receivers, modulators, graphics display systems, DSP-based companders, FSK and PSK satellite modems, multiplexers, forward error correction (FEC) codecs, RF upconverters and downconverters, and baseband analog and digital processing components.

9. In 1990, I returned to Scientific Atlanta, which was acquired by Cisco in 2006. I worked as Engineering Manager running the set top box engineering group where I was promoted to Director and Vice President during my tenure until 2011. I led the design of many cable set top boxes and systems through the evolution of analog video, addressability, downloadable software, electronic program guides, digital video, VOD, software applications, high-definition TV, DVR, DOCSIS, full spectrum tuners, and multiroom DVR. These systems implemented various technologies including DOCSIS 1/2/3 and hybrid gateways, 802.11, IPTV, DVR, cable modems, ADSL, VDSL, DVB-T/C/S, bootloaders, factory diagnostics, application frameworks, Nagra, DRMs, conditional access, secure microprocessors, device management, Android, Adobe Flash, Linux, DVD play/record, MPEG-4,

MPEG-2, H.264, NTSC, PAL, DAVIC, MoCA, high-performance CPUs, cablecards, network processors, HDMI, multiple video/audio display interfaces, 2D/3D graphics, multiple RF tuners, and full spectrum tuners.

10. From 2011 to 2016, I worked for EchoStar Technologies, which served as the product development organization for sister company DISH Network. I served as Vice President of Engineering and was the Head of the Atlanta research and development center. I led the development of satellite set top boxes, consumer electronic equipment, and a home automation and security system. Technologies used included video/audio, IoT, H.265, HEVC, 3D, Satellite, wireless, MoCA, transcoding, embedded C Linux applications, mobile applications (IOS and Android), SaaS, web applications (JavaScript, HTML), BSS/OSS, AWS cloud storage, 2-way video/audio streaming, authentication, and VoIP.

11. In 2016, I started an independent consulting business in technology and intellectual property projects. I have consulted in various technology areas and industries including consumer electronics, Internet of Things (IoT), cable, satellite, television, media, and cryptocurrency.

12. From 2019 to 2022, I worked as Chief Technology Officer for Telular, an Ametek company. I was responsible for the development of Industrial Internet of Things (IIoT) recurring revenue solutions, combining wireless technologies,

purpose-built hardware, and SaaS in the commercial telematics, security and home automation markets and sold under the SkyBitz and Telguard brands.

13. My record of professional service includes awards on products I designed and developed from several organizations in my field of expertise, including Best of Show, Technology Emmy, and Best of Innovations.

14. I am a named inventor on at least 117 patents and published patent applications corresponding to the areas of my professional work. The patents and published applications involving video and audio technologies include:

- U.S. Patent No. 9,882,736 titled “Remote Sound Generation for a Home Automation System”
- U.S. Patent No. 9,615,139 titled “Determining Device That Performs Processing of Output Pictures”
- U.S. Patent No. 8,549,567 titled “Media Content Sharing Over a Home Network”
- U.S. Patent No. 8,161,388 titled “Interactive Discovery of Display Device Characteristics”
- U.S. Patent Nos. 8,120,924, 7,240,217, 6,785,817, 6,564,324, 6,212,278, and 5,440,632 titled “Reprogrammable Subscriber Terminal”
- U.S. Patent No. 7,908,625 titled “Networked Multimedia System”

- U.S. Patent Nos. 7,861,272 and 7,849,486 titled “Networked Subscriber Television Distribution”
- U.S. Patent Nos. 7,774,820 and 7,069,578 titled “Settop Cable Television Control Device and Method Including Bootloader Software and Code Version Table for Maintaining and Updating Settop Receiver Operating System Software”
- U.S. Patent No. 5,771,064 titled “Home Communications Terminal having an Applications Module”
- U.S. Patent No. 5,715,515 titled “Method and Apparatus for Downloading On-Screen Graphics and Captions to a Television Terminal”
- U.S. Patent No. 5,657,414 titled “Auxiliary Device Control for a Subscriber Terminal”
- U.S. Patent No. 5,592,551 titled “Method and Apparatus for Providing Interactive Electronic Programming Guide”
- U.S. Patent No. 5,539,822 titled “System and Method for Subscriber Interactivity in a Television System”
- U.S. Patent No. 5,357,276 titled “Method of Providing Video On Demand with VCR Like Functions”
- U.S. Patent Application Publication Nos. 2004/0068753 and 2008/0072272 titled “Video Transmission Systems and Methods for a Home Network”

- U.S. Patent Application Publication No. 2004/0133911 titled “Subscriber Network in a Satellite System”

15. I have a general understanding of the U.S. patent prosecution process and of the novelty and non-obviousness requirements for patentability.

16. I believe that my extensive industry experience and educational background qualify me as an expert in the relevant field of digital signal processing (DSP) and radio frequency (RF) tuning systems for satellite and/or cable communications. I am knowledgeable of the relevant skill set that would have been possessed by a hypothetical person of ordinary skill in the art at the time of the invention of the '275 patent, which I (as I discuss below) understand is early 2009 or early 2010.

3. MATERIALS CONSIDERED

17. In formulating my opinion, I reviewed and considered the '275 patent (U.S. Pat. No. 11,785,275 to Reddy, et al.) (Ex. 1101), as to which I am offering my opinion regarding the validity of certain claims, as discussed herein.

18. In preparing this declaration, I also reviewed and considered the Petition and the file history of the '275 patent (included in Ex. 1104) as well as the following references:

Ex. 1101: U.S. Patent No. 11,785,275 (“the '275 patent”)

Ex. 1103: Curriculum Vitae of David B. Lett

- Ex. 1104: Certified Prosecution History of the '275 patent
- Ex. 1105: Certified Prosecution History of U.S. Patent No. 11,490,152 (“the parent”)
- Ex. 1107: Certified Prosecution History of U.S. Provisional App. No. 61/170,526 (“’526 provisional”)
- Ex. 1108: U.S. Pub. No. 2009/0290659 (“Petrovic”)
- Ex. 1109: Specification and drawings of U.S. Provisional App. No. 61/054,886 (“Petrovic ’886”)
- Ex. 1110: U.S.P.T.O Assignment Record for U.S. Application No. 12/414,892
- Ex. 1112: U.S. Patent No. 7,783,958 (“Eidson”)
- Ex. 1114: U.S. Patent No. 7,237,214 (“Pandey”)
- Ex. 1115: Excerpts of “IEEE Std 100-2000, The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition” (IEEE Press. 2000) (“IEEE Std 100”)
- Ex. 1116: Excerpts of Jan M Rabaey, “Digital Integrated Circuits: A Design Perspective” (Pearson, 2nd ed. 2002) (“Rabaey”)
- Ex. 1117: A. P. Chandrakasan, “Ultra low power digital signal processing,” Proceedings of 9th International Conference on VLSI Design, Bangalore, India, 1996, pp. 352-357 (“Chandrakasan”)

- Ex. 1118: S. Mirabbasi and K. Martin, “Classical and Modern Receiver Architectures,” IEEE Communications Magazine, vol. 38, no. 11, pp. 132-139, November 2000 (“Mirabbasi”)
- Ex. 1119: U.S. Patent No. 6,061,406 (“Carson”)
- Ex. 1121: Data-Over-Cable Service Interface Specifications, DOCSIS 2.0, Radio Frequency Interface Specification CM-SP-RFIV2.0-I11-060602
- Ex. 1125: J. Crols and M. S. J. Steyaert, “Low-IF topologies for high-performance analog front ends of fully integrated receivers,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998 (“Crols”)
- Ex. 1127: U.S. Patents and Patent Applications Family Tree for U.S. Pat. No. 11,785,275
- Ex. 1133: Excerpts of W. Ciciora, J. Farmer, D. Large, and M. Adams, “Modern Cable Television Technology: Video, Voice, and Data Communications” (2nd ed. 2004) (“Ciciora”)
- Ex. 1134: Excerpts of J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design” (1997)
- Ex. 1135: U.S. Patent No. 7,340,230 (“Khoini-Poorfard”)
- Ex. 1136: U.S. Pub. No. 2003/0217362 (“Summers”)
- Ex. 1137: U.S. Pub. No. 2006/0256799 (“Eng”)

- Ex. 1138: U.S. Pub. No. 2006/0083335 (“Seendripu”)
- Ex. 1139: Excerpts of Chris Bowick, “RF Circuit Design” (2nd ed. 2008)
- Ex. 1140: U.S. Pub. No. 2006/0031894 (“Petruzzelli”)
- Ex. 1141: Excerpts of Roland Priemer, “Introductory Signal Processing” (1991)
- Ex. 1142: U.S. Patent No. 7,272,375 (“Tuttle”)
- Ex. 1143: U.S. Patent No. 7,130,576 (“Gurantz”)
- Ex. 1144: U.S. Patent No. 5,278,837 (“Kelley”)
- Ex. 1145: Jeffrey Hugh Reed, “Software Radio: A Modern Approach to Radio Engineering” (2002)
- Ex. 1146: U.S. Patent No. 7,213,042 (“Cannon”)
- Ex. 1148: Excerpts of William Buchanan, “Computer Busses” (2000)
- Ex. 1149: U.S. Patent No. 7,079,528 (“Ziegler”)
- Ex. 1150: Excerpts of “Software Defined Radio: Enabling Technologies” (Walter H.W. Tuttlebee ed., 2003)
- Ex. 1153: U.S. Pub. No. 2008/0039036 (“Lee”)
- Ex. 1154: U.S. Pub. No. 2003/0220072 (“Coffin”)
- Ex. 1155: U.S. Patent No. 6,493,873 (“Williams”)

- Ex. 1156: U.S. Pub. No. 2007/0053314 (“Gat”)
- Ex. 1158: U.S. Pub. No. 2010/0020794 (“Cholas”)
- Ex. 1160: U.S. Patent No. 6,160,443 (“Maalej”)
- Ex. 1161: U.S. Pub. No. 2006/0256216 (“Takahiko”)
- Ex. 1170: U.S.P.T.O Assignment Record for U.S. Patent No. 8,526,898
- Ex. 1171: U.S.P.T.O Assignment Record for U.S. Patent No. 7,783,958 (“Eidson”)
- Ex. 1173: Expert Declaration of Dr. Sylvia Hall-Ellis
- Ex. 1175: U.S. Patent No. 6,791,995 (“Azenkot”)
- Ex. 1176: U.S. Patent No. 6,542,203 (“Shadwell”)
- Ex. 1180: Certified Copy of U.S. Pat. App. No. 11/681,774, filed March 03, 2007
- Ex. 1181: U.S. Pub. No. 2007/0250864 (“Diaz Perez”)
- Ex. 1182: U.S. Pub. No. 2007/0180485 (“Dua”)
- Ex. 1183: U.S. Pub. No. 2005/0114904 (“Monk”)
- Ex. 1184: U.S. Patent No. 5,317,391 (“Banker”)

4. UNDERSTANDING OF APPLICABLE LEGAL STANDARDS

19. Although I am not an attorney, I have a general understanding of the applicable legal standards pertaining to the patentability issues presented in this proceeding. I understand that the Petitioner is challenging the patentability of the claims of the '275 patent based on the following grounds:

- (A) claims 1, 4, 7-9, 11, 14, and 17-19 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Petrovic in view of Eidson;
- (B) claims 2-3 and 12-13 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Petrovic in view of Eidson and Rabaey;
- (C) claims 11, 14, and 17-19 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Petrovic in view of Eidson and Takahiko;
- (D) claims 12 and 13 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Petrovic in view of Eidson, Takahiko, and Rabaey;
- (E) claims 1, 4-5, 7-8, 10-11, 14-15, 17-18, and 20 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Cholas in view of Petrovic and Maalej;
- (F) claims 2-3 and 12-13 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Cholas in view of Petrovic, Maalej, and Rabaey;
- (G) claims 6 and 16 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Cholas in view of Petrovic, Maalej, and Lee;

- (H) claims 11, 14-15, 17-18, and 20 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Cholas in view of Petrovic, Maalej, and Takahiko;
- (I) claims 12 and 13 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Cholas in view of Petrovic, Maalej, Takahiko, and Rabaey; and
- (J) claim 16 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Cholas in view of Petrovic, Maalej, Takahiko, and Lee.

20. I understand that, in this *inter partes* review, Petitioner has the burden of proving that each challenged claim is unpatentable by a preponderance of the evidence.

21. I understand that to be valid, a patent claim must be “novel,” and is invalid if “anticipated” by a single prior art reference. I further understand a reference anticipates if it discloses each and every element as arranged in the claim so as to enable a person of ordinary skill in the art to make and use the claimed invention without undue experimentation.

22. I understand that a patent claim is unpatentable if, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of the prior art to yield the patent claim. It is my understanding that this determination is made after weighing the following factors: (1) the level of ordinary skill in the pertinent art; (2) the scope and content of the prior art; (3) the

differences between the prior art as a whole and the claim at issue; and (4) as appropriate, other objective considerations identified below.

23. It is my understanding that the prior art and claimed invention should be viewed through the knowledge and understanding of a person of ordinary skill in the art – one should not use his or her own insight or hindsight in deciding whether a claim is obvious. I further understand that a claim may be rendered obvious if a person of ordinary skill in the art can implement the claimed invention as a predictable variation of a known product. I further understand that a person of ordinary skill in the art is presumed to have knowledge of the relevant prior art at the time of the claimed invention, which comprises any prior art that was reasonably pertinent to the particular problems the inventor faced.

24. I understand that a showing of obviousness requires some articulated reasoning with a rational underpinning to support the combination of the references. I understand that in consideration of the issue of obviousness it is important to identify whether a reason existed at the time of the invention that would have led a person of ordinary skill in the pertinent art to combine elements of the references in a way that yields the claimed invention.

25. I understand that a claim may be considered unpatentable for obviousness for various reasons. I have been informed that the following exemplary rationales may support a finding of obviousness:

- (A) combining prior art elements according to known methods to yield predictable results;
- (B) substituting one known element for another to obtain predictable results;
- (C) use of a known technique to improve similar devices in the same way;
- (D) applying a known technique to a known device ready for improvement to yield predictable results;
- (E) choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- (F) known work in a field that prompts variations in the work in the same or a different field that leads to predictable results; and
- (G) some teaching, suggestion, or motivation in the prior art that would have led a person of ordinary skill in the art to modify a prior art reference or combine multiple prior art references or teachings to arrive at the claimed invention.

26. I understand that various objective or “real world” factors may be indicative of non-obviousness. I understand that such factors include:

- (A) the commercial success of the claimed invention;
- (B) the existence of a long-felt, unresolved need for a solution to the problem solved by the claimed invention;
- (C) failed attempts to solve the problem solved by the claimed invention;

- (D) copying of the claimed invention;
- (E) unexpected results of the claimed invention;
- (F) praise for the claimed invention by others in the relevant field; and
- (G) willingness of others to accept a license under the patent because of the merits of the claimed invention.

27. It is my understanding that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the link may be based on the common sense of the person of ordinary skill in the pertinent art. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and market demand is sufficient motivation to combine references.

28. It is my understanding that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. For example, common sense is a good reason for a person of ordinary skill to pursue known options when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions.

29. I further understand that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, it is my understanding that any need or problem known in

the field at the time of invention and addressed by the patent can provide a reason for combining the limitations in the manner claimed.

5. THE RELEVANT ART AND LEVEL OF ORDINARY SKILL IN THE RELEVANT ART

30. I understand that obviousness is determined from the vantage point of a person of ordinary skill in the relevant art at the time of the alleged invention (“POSITA”). The ’275 patent is directed to a wideband receiver system 200 “capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum.” Ex. 1101, 1:36-39. I understand that a person of ordinary skill in the art is one who is presumed to be aware of all pertinent art, thinks along conventional wisdom in the art, and is a person of ordinary creativity.

31. I believe that a person of ordinary skill in the art of the ’275 patent, at the time of the alleged invention of the ’275 patent, would have a degree in electrical engineering or a similar discipline, along with three-to-four years of experience with digital signal processing (DSP) and radio frequency (RF) tuning systems for satellite and/or cable communications. Additional education may substitute for professional experience, and significant work experience may substitute for formal education. I worked in the relevant field with such persons at, and leading up to, the time of the alleged invention of the ’275 patent, and thus, I am familiar with the knowledge that

such persons had at the time (*i.e.*, early 2009 or early 2010). At that time, I had a skill level that was at least as high as the skill level I describe above for a person of ordinary skill in the art of the '275 patent.

32. All of my statements in this declaration regarding what a person of ordinary skill in the art would have known, understood, appreciated, been motivated to do, etc., refer to a person of ordinary skill in the art in early 2009 to early 2010, before the earliest claimed priority date of the '275 patent.

6. CLAIM CONSTRUCTION

33. I understand that my analysis requires an understanding of the scope of the claims of the '275 patent. I understand that claim terms subject to *inter partes* review, absent some other definition provided in the patent, are given their ordinary meaning to a person of ordinary skill in the art in light of the patent specification. Therefore, in my analyses given below, I have assumed that all claim terms are given their ordinary interpretation as would have been understood by a POSITA reading the patent specification as of the priority date. I further understand that certain claim terms may be means plus function limitations. In particular, I understand that a “means plus function” limitation should be interpreted to cover only the corresponding structure described in the specification that performs the recited function, and equivalents thereof. I also understand that a limitation will be presumed to be a means plus function limitation if (a) the claim limitation uses the

phrase “means for”; (b) the “means for” is modified by functional language; and (c) the phrase “means for” is not modified by sufficient structure for achieving the specified function. I understand that a structure will be considered structurally equivalent to the corresponding structure identified in the specification only if the differences between them are insubstantial. For example, a structure may be deemed to be a structural equivalent to the corresponding structure where the structure performs the same function in substantially the same way to achieve substantially the same result.

34. Though no claims in the '275 patent include “means for” language, I have been asked to consider a potential construction of “radio front end” in claim 11 as a means-plus-function limitation. Should this term be construed as such, the corresponding structure that performs the recited function for this limitation (which is the function of “process the input signal” recited in claim 11) is the radio front end 210 illustrated in Figure 2 or the radio front end 410 illustrated in Figure 4. Ex. 1101, Figs. 2, 4. I note that the internal components of the radio front end 210 and the radio front end 410 are the same. Specifically, each includes a low noise amplifier (LNA) (e.g., LNA 202 in Figure 2 and LNA1 in Figure 4), two mixers (e.g., mixers 211 and 221 in Figure 2 and mixers 411 and 421 in Figure 4), two more amplifiers (e.g., amplifiers 213 and 223 in Figure 2 and amplifiers 413 and 423 in Figure 4) and two filters (e.g., filters 215 and 225 in Figure 2 and filters 415 and 425 in Figure 4). Ex.

1101, 4:43-5:47, 7:31-46, Figs. 2, 4. A POSITA would have understood that any one of these components processes the RF input signal that is input to the radio front end 210 or radio front end 410. Lastly, as I discuss in my detail analysis below, the prior art discloses the “radio front end” limitation whether or not it is construed as a means-plus-function limitation.

35. I have also been asked to consider a potential construction of “digital frontend (DFE)” in claims 11, 12, and 13 as a means-plus-function limitation. Should this term be construed as such, the corresponding structure that performs the recited functions for this limitation (which are the functions of “select the plurality of desired channels from the digitized signal and output the selected plurality of desired channels to at least one demodulator as a digital datastream” recited in Elements [11E]-[11F], “output the digital datastream via a serial interface” recited in claim 12, and “output the digital datastream via a parallel interface” recited in claim 13) is the digital front end 230 illustrated in Figure 2. Ex. 1101, 5:56-7:20, Figs. 2, 3. The digital front end 230 in Figure 2, for example, shows a bank of N complex mixers 250, a bank of filters 260, and a bank of decimators 270. Ex. 1101, 5:56-6:20, Fig. 2. One of the paths through the digital front end 230 is shown in more detail in Figure 3. Ex. 1101, 6:21-23. Therefore, Figure 3 shows that the digital front end 230 from Figure 2 includes a mixer 300 that includes four multipliers 313, 315, 323, and 325 and two adders 317 and 327. Ex. 1101, 6:21-7:2. The ’275 patent also

discloses that the multipliers receive the $\cos(\omega_{ci}t)$ and $\sin(\omega_{ci}t)$ signals from numerically controlled oscillators (NCOs). Ex. 1101, 6:35-7:2. Figure 3 also shows that the two outputs of the mixer 300 are then filtered by filters 330 and 340 and decimated by decimator 350. Ex. 1101, 7:3-15. I note that the '275 patent indicates that decimators are optional. Ex. 1101, 3:8-10, 6:11-19. Indeed, a POSITA would have understood that the recited functions of the claims (identified above) do not require decimating and could be performed by the mixers/multipliers and filters alone. Lastly, as I discuss in my detailed analysis below, the prior art discloses the “digital frontend (DFE)” limitation whether or not it is construed as a means-plus-function limitation.

7. OVERVIEW OF THE '275 PATENT

36. The '275 patent describes a wideband receiver system 200 “capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum.” Ex. 1101, 1:33-35.

37. The '275 patent states that the system groups the desired channels that extend over non-contiguous portions of the frequency spectrum “into a contiguous, or substantially-contiguous, frequency spectrum” to “increase the dynamic range without requiring expensive data conversion, filtering, and channel selection at the demodulator.” Ex. 1101, 1:35-40, 2:44-46. According to the '275 patent, a receiver is “wideband” if it is “designed to concurrently receive several TV channels.” *Id.*,

1:42-43. Figure 2 is a “block diagram of a wideband receiver system 200.” *Id.*, 4:40-41.

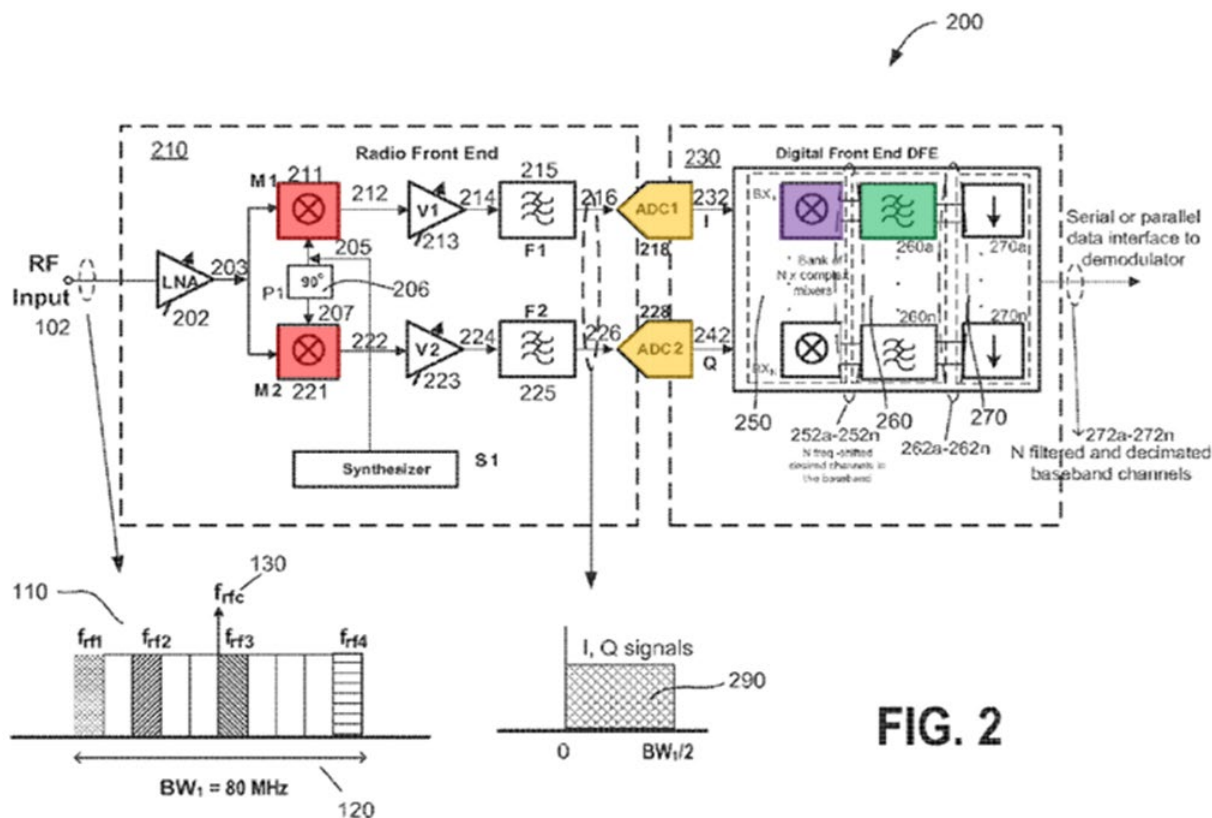


FIG. 2

Ex. 1101, Fig. 2 (annotated)

38. The wideband receiver system 200 receives both desired and undesired television channels as frequencies dispersed within a frequency bandwidth BW_1 . Ex. 1101, Abstract, 1:35-40. Mixers “M1” and “M2,” which are shown in **red** above, “generate an in-phase signal 212 and a quadrature signal 222 that have a phase shift of 90 degree between them” and that have been downconverted to “the baseband or low intermediate frequency (IF) band.” Ex. 1101, 2:64-3:1, 4:65-5:4, *see also* 2:10-12. “[U]nwanted frequency components” are filtered from the in-phase signal and

the quadrature signal by respective filters 215 and 225. Ex. 1101, 5:22-29. The filtered signals are then individually digitized by wideband analog-to-digital converters ADC1 and ADC2 (**gold**) to generate a digital in-phase (I) signal 232 and a digital quadrature (Q) signal 242. Ex. 1101, 3:1-3, 5:53-56. U.S. Provisional App. No. 61/170,526 (“the ’526 provisional”), which the ’275 patent incorporates by reference, admits that the left side of Figure 2 (up to and including ADC1 and ADC2) “is similar to conventional tuners.” Ex. 1107 at 5; Ex. 1101, 1:6-28.

39. The digital I and Q signals 232 and 242 are input to a bank of N complex mixers 250 (one of which is shown above in **purple**) in a digital front end 230, where “N is an integer value corresponding to the number of desired RF channels.” Ex. 1101, 5:56-60. “Each of the N complex mixers ... extract[s] a different one of the desired channels” from the I and Q signals 232 and 242 and “frequency-shifts the extracted signals to the baseband frequency.” Ex. 1101, 6:8-11. An associated filter module of filters 260a-260n (one of which is shown above in **green**) filters the frequency-shifted desired channel. Ex. 1101, 6:11-13.

40. Figure 3 “is a simplified circuit diagram of one of the signal paths 272a to 272n of digital front end 230” and shows elements in one of the rows of digital front end 230 in Figure 2. Ex. 1101, 6:21-23.

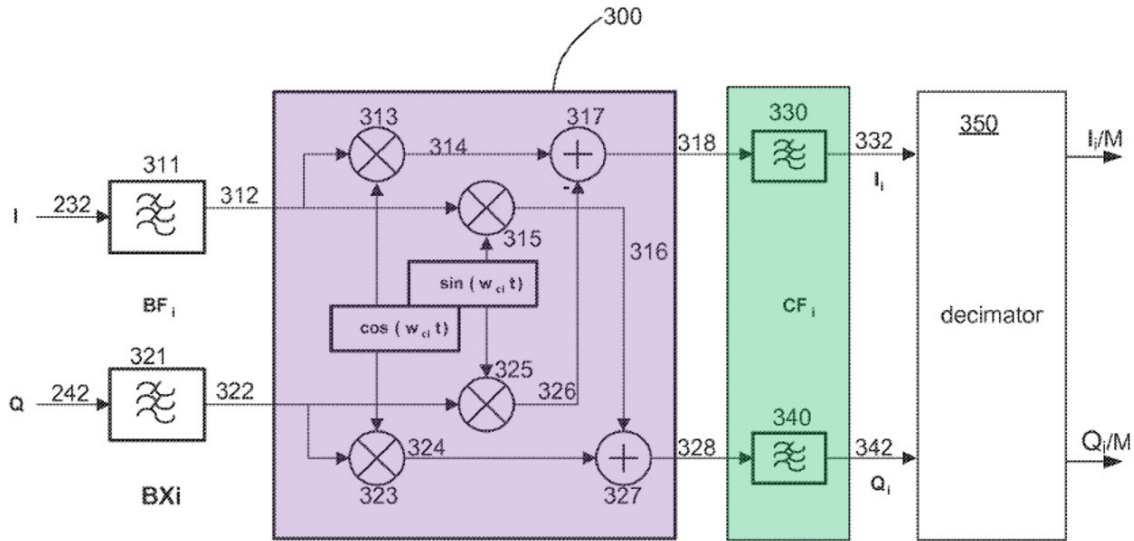


FIG. 3

Ex. 1101, Fig. 3 (annotated)

41. Mixer 300 (**purple**) represents one of the complex mixers 250 and has multipliers 313, 315, 323, and 325 and adders 317 and 327. Ex. 1101, 6:33-43. “[C]omplex mixer 300 causes a frequency shift of the filtered components 312 and 322 to respective baseband signals 318 and 328 in the digital domain” by using a frequency ω_{ci} that is chosen such that “each one of the desired channels embedded in the digital signals I 232 and Q 242 will be downshifted to the baseband.” Ex. 1101, 6:43-62. The baseband signals 318 and 328 are filtered by filters 330 and 340 (**green**) that are “one of the filters 260a-n” shown in Figure 2. Ex. 1101, 7:3-5.

42. After decimation, “the N desired baseband channels will be sent as a serial or parallel digital data stream to a demodulator using a serial or parallel data interface according to commonly known methods.” Ex. 1101, 7:16-20. The ’275

patent does not provide any details of how $N \times 2$ signals (N channels, with an I and a Q signal for each channel) might be manipulated, combined, and/or otherwise processed between the decimators 270 and a demodulator. Rather, the '275 patent admits that this is performed “according to commonly known methods.” *Id.*

7.1. Prosecution History

43. The '275 patent claims priority to a number of applications. In particular, it is a direct continuation of U.S. Application No. 17/862,946, which became U.S. Patent No. 11,490,152 (“the parent”), which has very similar claims. The main difference is that the '275 patent claims add “the plurality of desired channels are non-contiguous.” Thus, below I have addressed the prosecution history of the parent and then the prosecution history of the '275 patent.

7.1.1. Prosecution History of the Parent

44. The parent was filed on July 12, 2022, with original claims 1-18 and a preliminary amendment removing the original claims and adding new claims 19-38. Ex. 1105 at 2, 5-8. In a first office action issued on September 7, 2022, the examiner only examined the original claims 1-18 by mistake and provided double patenting and 35 U.S.C. § 112 rejections. Ex. 1105 at 119-123. The applicant requested examination on the new claims 19-38 on September 12, 2022. Ex. 1105 at 143-148. The examiner allowed claims 19-38 on September 28, 2022 based on the prior art not teaching “selecting, by a digital frontend (DFE) coupled to the ADC, *a plurality*

of desired channels from the digitized signal and outputting by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream.” Ex. 1105 at 153-159. None of Petrovic, Takahiko, Rabaey, Cholas, Maalej, or Lee were cited or considered during the prosecution of the parent. Eidson was similarly not cited during prosecution of the parent. Although Eidson was cited during prosecution of related U.S. Patent No. 11,399,206, the parent of the parent (i.e., the grandparent of the ’275 patent), there is no indication in the file history of the parent that Eidson was considered during prosecution of the parent.

7.1.2. Prosecution History of the ’275 Patent

45. It is my understanding that U.S. Application No. 17/956,889 (“’889 application”), which issued as the ’275 patent, was filed on September 30, 2022. Ex. 1104 at 44. The ’889 application was filed with 18 claims including independent claims 1 and 10. Ex. 1104 at 91-95. On November 17, 2022, the applicant filed a preliminary amendment to remove the original 18 claims and to add new claims 19-38. Ex. 1104 at 110-117. The main difference from the parent’s claims is that the ’275 patent claims add “the plurality of desired channels are non-contiguous.” *Compare* Ex. 1104 at 91-95, 113-116, 3385-3387 *with* Ex. 1101, claims 1-20. The first Office Action, issued on May 1, 2023, rejected all claims on the basis of nonstatutory double patenting over claims 1-20 of U.S. Patent No. 11,490,152. Ex. 1104 at 3352-3357. Applicant then filed a terminal disclaimer on July 25, 2023. Ex.

1104 at 3390-3393. On August 14, 2023, a Notice of Allowance was mailed that stated that the prior art failed to teach “selecting, by a digital frontend (DFE) coupled to the ADC, a plurality of desired channels from the digitized signal and outputting by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream.” Ex. 1104 at 3400-3406. This was the same statement as the reasons for allowance in the parent. *Compare* Ex. 1104 at 3405 *with* Ex. 1105 at 158.

46. Instead of paying the issue fee, Applicant filed a Request for Continued Examination (RCE) and an Information Disclosure Statement (IDS) on August 16, 2023. Ex. 1104 at 3415-3421. A second notice of allowance was sent and the '275 patent was issued. In the second Notice of Allowance, the examiner indicated that “[t]he prior art comprising Information Disclosure Statements filed 16 August 2023 and 18 August 2023” was “from the applicant’s other patents, i.e., US 8[,]223,775, as part of the Entropic Communications, LLC, the applicant, v. Charter communications, Inc. Civil Action and Entropic Communications, LLC v. DirectTV, LLC and Dish Network Corp., Civil Action.” Ex. 1104 at 4829. Then, the examiner simply repeated the same reason for allowance given in the previous notice of allowance and in the parent. *Compare* Ex. 1104 at 4830 *with* Ex. 1105 at 158. Specifically, the second Notice of Allowance stated that:

The following is a statement of reasons for the indication of allowable subject matter: the prior art made of record teach a receiver for a wireless telecommunication system teach all of the adjacent frequency bands in the IF signal passed by a band pass filter in the radio frontend are converted to a digital signal by an ADC and then separated into their respective frequency bands by a channelizer where the separated frequency bands are processed in the normal manner by subsequent DSP devices, see Claxton et al. US 6,735,421. The prior art made of record do not teach selecting, by a digital frontend (DFE) coupled to the ADC, a plurality of desired channels from the digitized signal and outputting by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream.

Ex. 1104 at 4830. The application issued as the '275 patent on October 10, 2023.

Ex. 1104 at 4857-4858. None of Cholas, Rabaey, Maalej, Lee, or Takahiko were cited or considered during prosecution. Ex. 1104 at 4824-4831; Ex. 1101 at 1-3. No IDS or Office Action cites or mentions Petrovic. Ex. 1104 at 4-11, 125-130, 3352-3357, 3418-3420, 4820-22. The patent number of U.S. Patent No. 8,345,798 (Petrovic '798), which issued based on Petrovic, appears twice—without analysis or discussion—in over 4500 pages of NPL documents that the applicant submitted. Ex. 1104 at 2309, 2839. The “Petrovic” mentioned in the claim charts and other analyses included in those NPLs is a different patent with a disclosure different from that of Petrovic '798. *E.g.*, Ex. 1104 at 2333. Moreover, Petrovic '798 is only identified in NPL documents addressing U.S. Patent No. 8,792,008, which is unrelated to the '275 patent. Ex. 1104 at 2293, 2308-2309, 2823, 2838-2839. The patent number for Eidson appears in one place in the file history of the '275 patent. Ex. 1104, at 3411.

7.2. Earliest Priority Date for the Claims

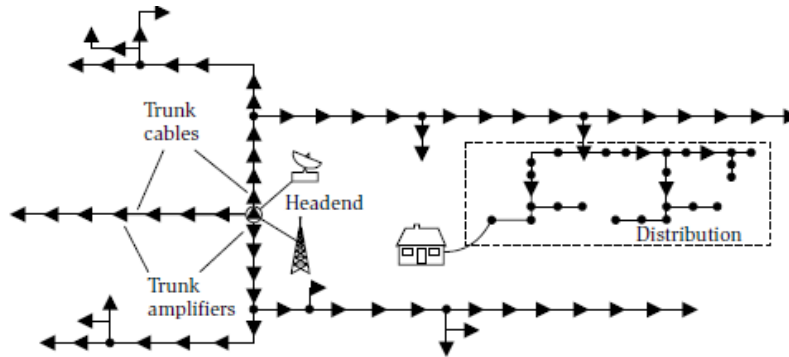
47. I understand that Application No. 17/956,889 (“the ’889 application”), which eventually became the ’275 patent, was filed on September 30, 2022. It is further my understanding that the ’889 Application claims priority to a chain of applications that claim priority to the ’526 provisional filed on April 17, 2009. It is my understanding that the ’275 patent asserts to be entitled to a priority date of the filing date of the earliest application from which the ’275 patent claims priority, *i.e.*, April 17, 2009, which is the filing date of the ’526 provisional. Thus, the earliest possible effective filing date for the claims of the ’275 patent is April 17, 2009. I understand that all of the references that I rely on in this Declaration were published or filed before April 17, 2009, and are prior art to that date.

8. OVERVIEW OF THE PRIOR ART

8.1. Cable and Satellite Television Networks

48. The origins of the cable and satellite television networks long predate the earliest claimed priority date (April 17, 2009) of the ’275 patent. Cable television networks are entertainment distribution systems that allow consumers to access and enjoy various television channels. Ex. 1133 at 22. The cable television networks include one or more headends that are designed to broadcast and distribute, via coaxial cables, the data for the television channels as modulated radio frequency (RF) signals to multiple terminal equipment belonging to the consumers (e.g.,

television receivers, set-top boxes, data modems, digital video recorders, personal video recorders, and other terminal equipment). *Id.* at 22, 29-30, 40, 352; Ex. 1134 at 20-21. This is illustrated in Figure 1.1 of Ex. 1133.

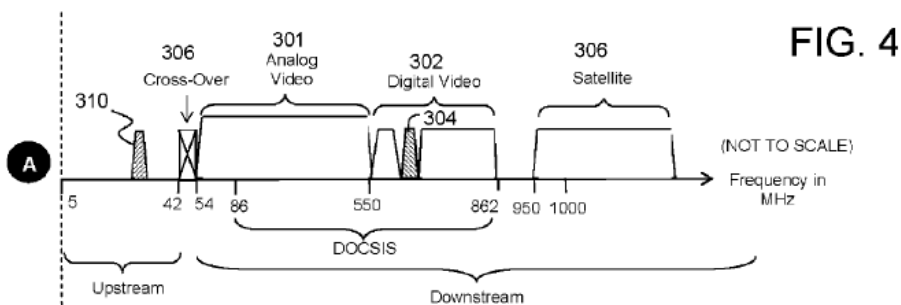


Ex. 1133, Fig. 1.1 (Excerpted) at 34

RF is the frequency range starting from 10 kHz to 100,000 MHz in the electromagnetic spectrum; signals having frequencies from this RF range are used for data transmission (wired or wireless) between devices. *See* Ex. 1115 at 9. The transmissions between the headends and the terminal equipment are governed by various well-known industry standards, including Data Over Cable Systems Interface Specification (DOCSIS). Ex. 1121 at 2-5, Figs. 1-2; Ex. 1133 at 27, 211-212.

49. Consumers can also access television channels from satellites via conventional home satellite television systems. Ex. 1135, 1:30-31; Ex. 1136, [0006]. Such home satellite television systems typically include a fixed dish antenna that receives television channels in modulated RF signals, as well as a satellite receiver

or set-top box designed to process and demodulate the modulated RF signals. Ex. 1135, 1:31-35; Ex. 1136, [0013]. Satellites may also be used to distribute the television channels to headends of cable television networks, which are then redistributed to the consumers. Ex. 1133 at 262, 280-282; Ex. 1136, [0009].



Ex. 1137, Fig. 4 (Excerpted)

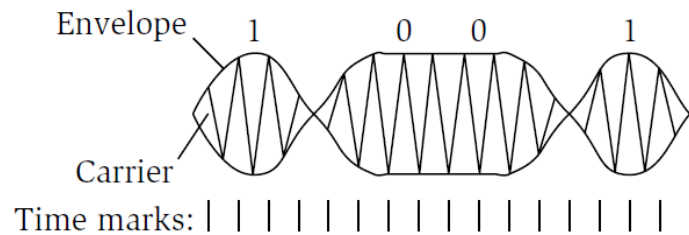
50. Figure 4 of Exhibit 1137 (partially reproduced above) illustrates the RF spectrum usage of television channels from cable and satellite television networks. Ex. 1137, [0079]-[0080]. In North America, television channels from cable television networks occupy the RF spectrum from 54 to 864 MHz, with digital channels occupying the RF spectrum above 550 MHz. Ex. 1133 at 413, 503; Ex. 1137, [0079]-[0080]. In 1941, the National Television System Committee, established by the United States Federal Communications Commission, set a standard that each television channel should be allocated 6 MHz of RF bandwidth and that the set of allocated television channels should occupy the RF spectrum in a contiguous manner. Ex. 1121 at 1, 23-24; Ex. 1133 at 45, 413, 515-520.

51. Television channels from satellite networks occupy various bands in frequencies greater than 950 MHz. Ex. 1135, 1:37-48; Ex. 1137, [0079]-[0080]. Signals in satellite bands are sent to a satellite receiver or set-top box, with the satellite bands carrying multiple transponder channels and each transponder channel carrying a number of different television channels. Ex. 1135, 1:37-48.

8.2. Modulated RF Signals

52. Modulation is a method where an RF carrier signal is varied (e.g., in amplitude, frequency, and/or phase) with information to be transmitted. Ex. 1133 at 155. The information to be transmitted can be digital data comprising of bits “1” and “0,” such as the digital data of television channels for transmission from headends of cable television networks or subscriber locations. *Id.* One of the main goals of modulation is to squeeze as much data into the allocated RF bandwidth as possible, and that objective, known as spectral efficiency, measures how quickly data can be transmitted in an assigned RF bandwidth. *Id.* at 156. The unit of measurement of spectral efficiency is bits per second per Hz (b/s/Hz). *Id.* As I discuss below, multiple modulation techniques facilitating high spectral efficiencies were known to a POSITA by the earliest claimed priority date of the '275 patent.

8.2.1. Biphase Shift Keying



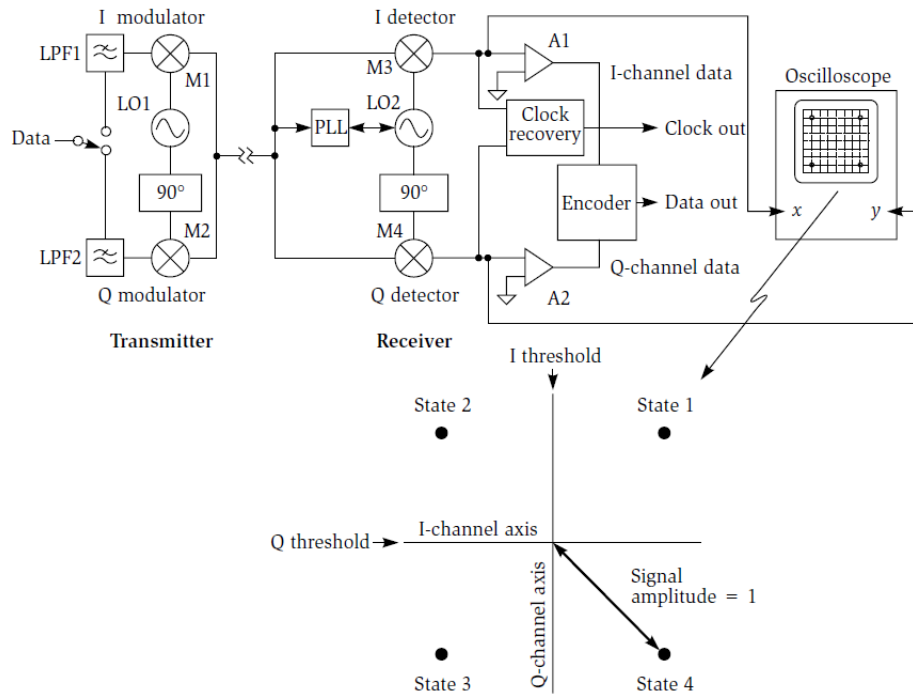
Ex. 1133, Fig. 4.3 (Excerpted) (at 161)

53. Biphase shift keying (BPSK) is a simple form of modulation that can be used in digital cable and satellite television networks, where the phase of an RF signal is shifted 180° in phase between transmission of bit “0” and bit “1.” Ex. 1133 at 160-161, Fig. 4.3 (partially reproduced above). The spectral efficiency of BPSK modulation is 1 bit/s/Hz. *Id.* at 156.

8.2.2. Quadrature Phase Shift Keying (QPSK)

54. In Quadrature Phase Shift Keying (also called 4-Quadrature Amplitude Modulation (4-QAM)), digital data is split into two components, an I (in-phase) component and a Q (quadrature) component. Ex. 1133 at 163-164, Fig. 4.4 (reproduced below). The same RF carrier signal is used for each component, but the phases of the two signals in the two components are 90° apart or in quadrature. *Id.* Signals in quadrature are orthogonal and do not interfere with one another. *Id.* Quadrature modulation takes advantage of this principal by combining two signals in quadrature for a combined output signal. *Id.* In quadrature modulation, digital data are broken into a discrete number of symbols, which are used to convey information.

Id. at 164-165. These symbols are mapped to a discrete set of magnitude and phase values on an I/Q constellation, which are referred to as constellation points. *Id.* For example, in BPSK, each symbol can only represent a bit “0” or a bit “1” because the constellation of BPSK modulation has just two possible constellation points representing two possible states, or symbols, where each symbol represents a single bit of information. The constellation of QPSK modulation has four constellation points representing four different states, or symbols: state 1 (bits “00”), state 2 (bits “01”), state 3 (bits “10”), and state 4 (bits “11”). *Id.* QPSK can, therefore, transmit 2 bits per symbol. *Id.* The RF carrier signals in each of the I and Q components are encoded with one of the two bits of the symbol. *Id.* at 163. Therefore, QPSK can transmit twice as much data using the same amount of bandwidth as BPSK, or it could transmit the same amount of data using half the bandwidth. *Id.* at 156.



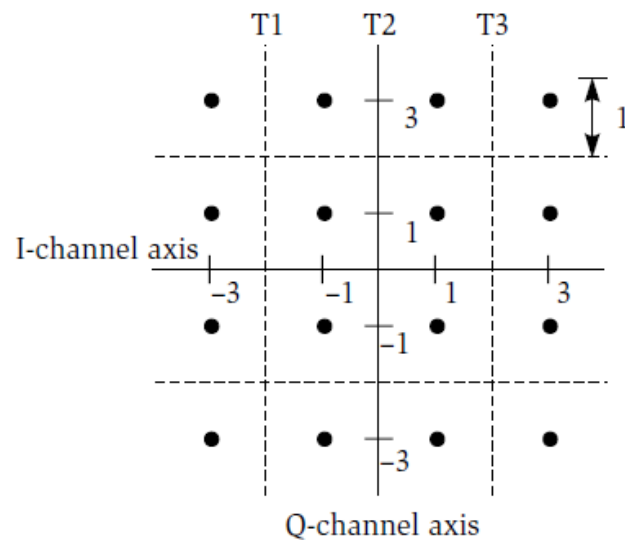
Ex. 1133, Fig. 4.4 (at 164)

55. After the two RF carrier signals from the two components I and Q are modulated, the RF carrier signals are combined for transmission to the receiver. Ex. 1133 at 163. At the receiver, the received combined signal is split back into the I-component and the Q-component by two mixers, M3 and M4. *Id.* The separation back into I/Q components allows the encoder inside the receiver to map the two components onto the QPSK I/Q constellation and interpret which of the four possible symbols are encoded in the components. *Id.* at 164.

56. A POSITA would have been well aware that satellite television networks primarily used QPSK modulation. Ex. 1133 at 280; Ex. 1136, [0071], [0075]. Satellite transponders that transmit RF signals to headends and dish antennas are simply a frequency translator and a power amplifier, and for the sake of

efficiency, it was preferred to use modulation formats that do not depend on amplitude changes to communicate information. Ex. 1133 at 280. QPSK modulation met this requirement of satellite transponders. *Id.*

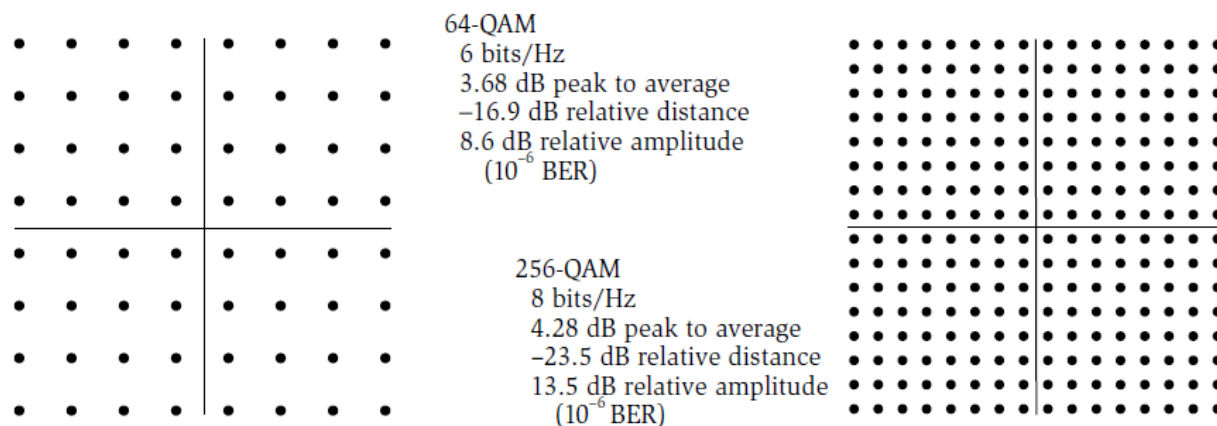
8.2.3. 16-Quadrature Amplitude Modulation (QAM), 64-QAM, and 256-QAM



Ex. 1133, Fig. 4.5 (Partial Excerpt) (at 167)

57. Modulation schemes with greater numbers of constellation points are able to transmit more information per symbol. Ex. 1133 at 166-169. The next denser known modulation format after QPSK was 16-QAM, where data is split into I and Q components and carried by two RF signals in quadrature. *Id.* at 166. However, the 16-QAM I/Q constellation has sixteen different states (as illustrated by the sixteen dots in Figure 4.5 of Ex. 1133, partially reproduced above), where each state is a symbol that contains one of 16 different combinations of amplitude and phase levels. *Id.* Each symbol contains up to 4 bits and, therefore, can represent values from

“0000” to “1111.” *Id.* The spectral efficiency of 16-QAM is 4 bit/s/Hz. *Id.* at 168, Fig. 4.6.



Ex. 1133, Fig. 4.6 (Partial Excerpt) (at 168)

58. Similarly, the I/Q constellation of 64-QAM (illustrated by Figure 4.6 of Ex. 1133, partially reproduced above) has sixty-four different states, where each state is a symbol that contains one of 64 different combinations of amplitude and phase levels. *Id.* Each symbol contains up to 6 bits (representing values from “000000” to “111111”), and the spectral efficiency of 64-QAM is 6 bit/s/Hz. *Id.* The I/Q constellation of 256-QAM has 256 different states, where each state is a symbol that contains one of 256 different combinations of amplitude and phase levels. *Id.* Each symbol contains up to 8 bits (representing values from “00000000” to “11111111”), and the spectral efficiency of 256-QAM is 8 bit/s/Hz. *Id.*

59. DOCSIS (finalized in 1997), DOCSIS 1.1 (finalized in 2001), and DOCSIS 2.0 (finalized in 2002) mandate the use of either 64-QAM or 256-QAM for downstream data transmission from headends to consumers’ terminal equipment.

Ex. 1133 at 168, 213-214. Therefore, a POSITA would have known that terminal equipment receiving signals from headends of cable television networks were required to demodulate signals that have been modulated using 64-QAM or 256-QAM. Moreover, a POSITA would have understood the relative benefits of using 64-QAM or 256-QAM versus BPSK, as 64-QAM and 256-QAM offer higher rates of spectral efficiencies than BPSK. *Id.* at 156.

8.3. Radio Receivers or Tuners for Cable and Satellite Television Networks

60. As discussed in Section 8.1, it was well-known to a POSITA that consumer terminal equipment (e.g., television receivers, cable set-top boxes, satellite set-top boxes, digital video recorders, personal video recorders, and other terminal equipment) receive modulated RF signals from headends and satellites. Ex. 1133 at 22, 30, 40, 352; Ex. 1135, 1:30-35; Ex. 1136, [0006]. A POSITA was also aware that consumer terminal equipment included a radio receiver (also known as a tuner) that received the RF signals and processed them in such a way that a demodulator could demodulate the RF signals to recover the digital data encoded in the RF signals. Ex. 1133 at 408-411, Fig. 22.1; Ex. 1135, 1:35-37, 1:49-52; Ex. 1136, [0018], [0020]-[0021].

61. Cable television RF receivers concurrently receive RF signals for multiple digital television channels allocated in the RF frequency spectrum of 550

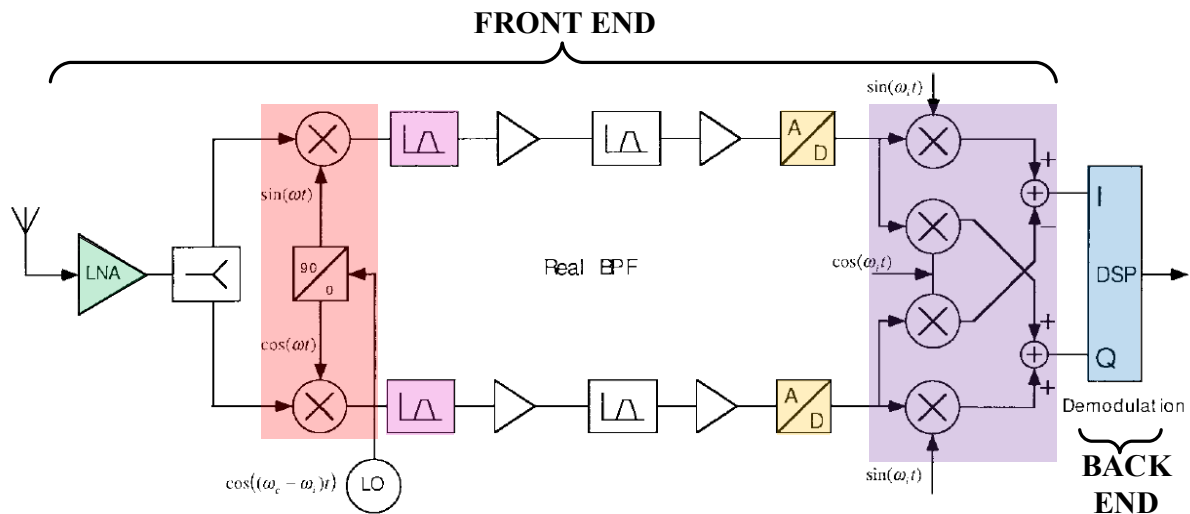
to 864 MHz. Ex. 1133 at 413, 503; Ex. 1137, [0079]-[0080], Fig. 4. Satellite RF receivers concurrently receive RF signals for multiple television channels allocated in the RF frequency spectrum above 950 MHz. Ex. 1135, 1:37-47; Ex. 1137, [0080]. Furthermore, the POSITA was aware that cable and satellite television radio receivers could tune (i.e., select and extract) signals for certain desired television channels (e.g., channels selected for viewing by a consumer) from the received RF frequency spectrum. Ex. 1133 at 299; Ex. 1136, [0020]-[0021]; Ex. 1142, 4:10-36; Ex. 1144, 1:51-58.

62. One type of receiver is known as an IF (intermediate frequency) receiver, and in particular, a type of receiver known as a low-IF receiver. By the earliest claimed priority date of the '275 patent, IF receivers, including low-IF receivers, were well-known in wireless communication systems for their high performance and low power consumption. Ex. 1125 at 270, 272; Ex. 1134 at 17, 65-74. It was also known to a POSITA, by the earliest claimed priority date of the '275 patent, that low-IF receivers were conventionally used for receiving RF signals from cable television networks and satellite television networks. Ex. 1135, 1:49-61; Ex. 1138, [0022]-[0023], [0029]-[0030], [0042].

63. IF receivers have been used for a long time, and their way of operating is very well known. Ex. 1125 at 270. In general, IF receivers operate by initially downconverting RF signals, which may comprise multiple RF sub-bands each

carrying one or more separate signals, from its RF carrier frequency to an intermediate frequency (IF). *Id.* The downconverted signals can be demodulated at the IF or further downconverted to baseband before being demodulated. *Id.* at 270, 279. When a band of signals is at baseband, the low end of the band is near zero frequency in the frequency spectrum or includes zero frequency. Ex. 1115 at 4. Intermediate frequency falls below the frequency of the RF signals but above the baseband frequency. Ex. 1134 at 22. Low-IF receivers initially downconvert to an IF that is at a relatively low frequency, such as a few hundred kilohertz. Ex. 1125 at 269.

8.3.1. Architecture of Low-IF receivers



Ex. 1125, Fig. 22(a) (annotated)

64. Low-IF receivers (illustrated by Figure 22(a) of Ex. 1125, reproduced and annotated above) comprise two main portions: a front end that performs

frequency downconversion of the RF signals, and a back end including a digital signal processor (DSP) that performs the actual demodulation of the RF signals. Ex. 1134 at 22-23. The demodulation technique that will be used in the DSP depends on the modulation technique used to modulate the incoming RF signals, and therefore, if the incoming RF signals are modulated using QPSK or QAM techniques (which modulate I and Q components), then demodulation is typically performed to extract the I and Q components of the incoming RF signals. *Id.* at 23. DSPs typically perform demodulation on baseband signals. *Id.*; Ex. 1139 at 11; Ex. 1125 at 269, 279. However, the received RF signals are at much higher (non-baseband) frequencies. *Id.* Therefore, the front end must produce baseband quadrature I and Q components of the incoming RF signals to be usable by the DSP. Ex. 1134 at 23.

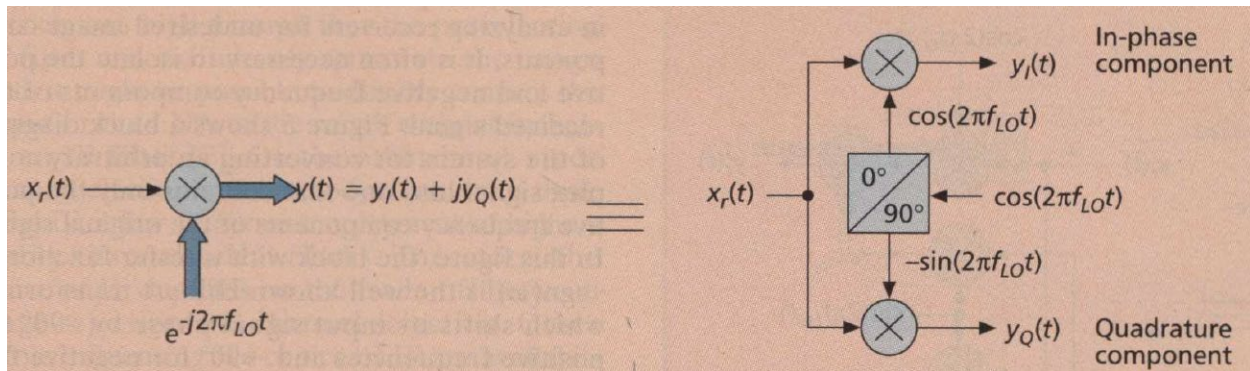
65. Still referring to Figure 22(a) of Ex. 1125 (reproduced and annotated above), in the front end of a low-IF receiver, the incoming RF signals are first amplified by a front-end low noise amplifier (LNA) (**green**) to provide enough gain to boost the received RF signal levels to an acceptable level such that further signal processing can be performed on the received RF signals; the LNA compensates for the attenuations of the RF signals during the transmission of the RF signals from another device. Ex. 1134 at 41; Ex. 1139 at 16. The RF signals are downconverted to baseband signals in two steps, where the first step (**red**) converts the RF signals to Intermediate Frequency (IF) signals before one or more analog-to-digital

converters (ADCs) (gold) convert IF signals to digital signals, and the second step (purple) converts the digital signals of IF to baseband signals. Ex. 1125 at 270, 272; Ex. 1134 at 23.

66. In the first downconversion step, from RF to IF, the incoming RF signals are split and then down-converted by a quadrature downconverter (red), also referred to as a complex mixer or complex multiplier, which comprises two real mixers to produce I and Q components of the signals in IF. Ex. 1134 at 65-72; Ex. 1139 at 11 (“Two mixers are needed to retain both the amplitude and phase of the original modulated signal: one for the in-phase (I) and another for a quadrature (Q) baseband output.”); Ex. 1118 at 133-134. For example, as explained in an article by Shahriar Mirabbasi and Ken Martin in IEEE Communications Magazine in November 2000:

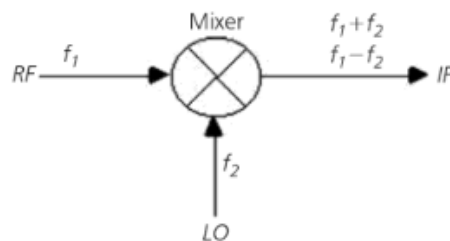
The realization of a multiplier for mixing a real signal with a complex exponential *requires two real multipliers*, as illustrated in Fig. 2. *The real and imaginary parts of the mixer output are called the in-phase (I) and quadrature (Q) components* of the downconverted signal (since cosine and sine are in quadrature). In Fig. 2 the frequency of the complex exponential is chosen to be the same as the center frequency of the passband signal, for comparison with case 2 in Fig. 1. In this case there is no image problem associated with the *complex mixer*.

Ex. 1118 at 134 (emphasis added).



Ex. 1118, Fig. 2

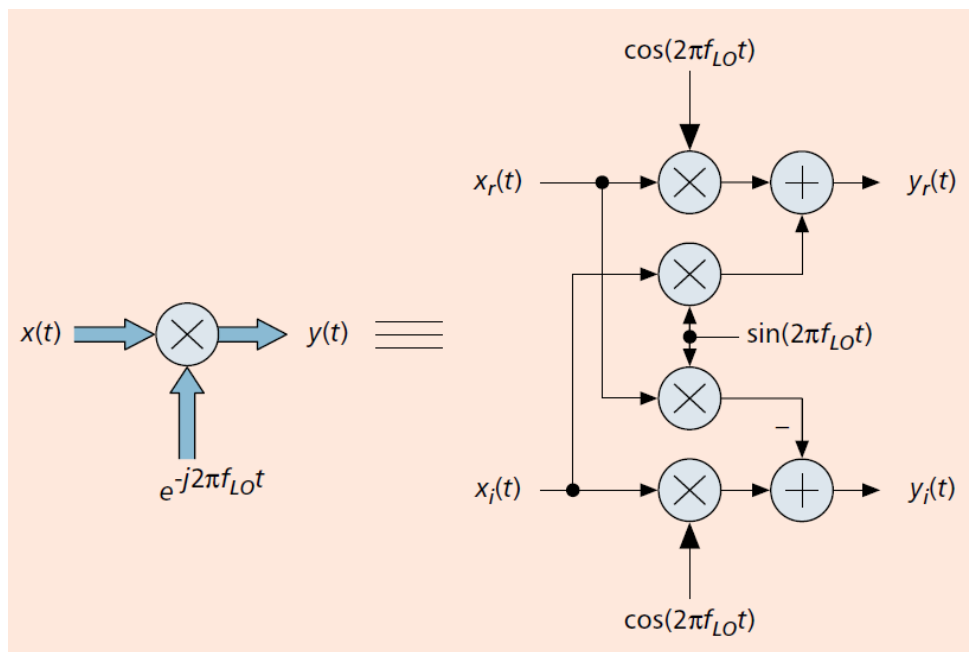
The term “mixer” and “multiplier” are often used interchangeably to refer to an analog or digital electrical circuit (represented by the symbol $\otimes$) that multiplies a modulated input signal (e.g., an RF signal) at frequency f_1 and a reference signal (e.g., from a local oscillator LO) at frequency f_2 , which produces new signals at the sum and difference of the input frequencies, f_1+f_2 and f_1-f_2 . Ex. 1139 at 12-13. This is illustrated in Figure 8-9 from Ex. 1139.



Ex. 1139, Figs. 8-9

By filtering out the signal with the sum (f_1+f_2), and passing only the signal with difference (f_1-f_2), the center frequency of the modulated input signal is reduced, or down-converted. A mixer/multiplier is “complex,” if it multiplies the input signal by

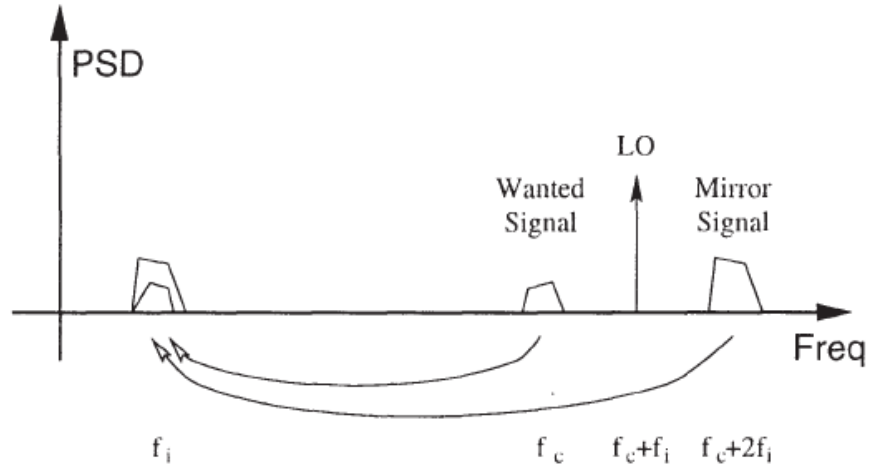
a complex signal, having real and imaginary parts, to produce in-phase and quadrature signals. Ex. 1118 at 133. A complex mixer/multiplier can include two real mixers/multipliers when the input signal is real and the reference signal is complex as shown in Figure 22(a) of Ex. 1125 above, or it can include four real mixers/multipliers if both the input signal and reference signal are complex as shown below. Ex. 1118 at 133-134, Fig. 3. As shown in the figure below, the symbol $\otimes$ is used interchangeably to refer to a complex mixer (left) or individual real multiplier/mixers (right) that make up a complex mixer.



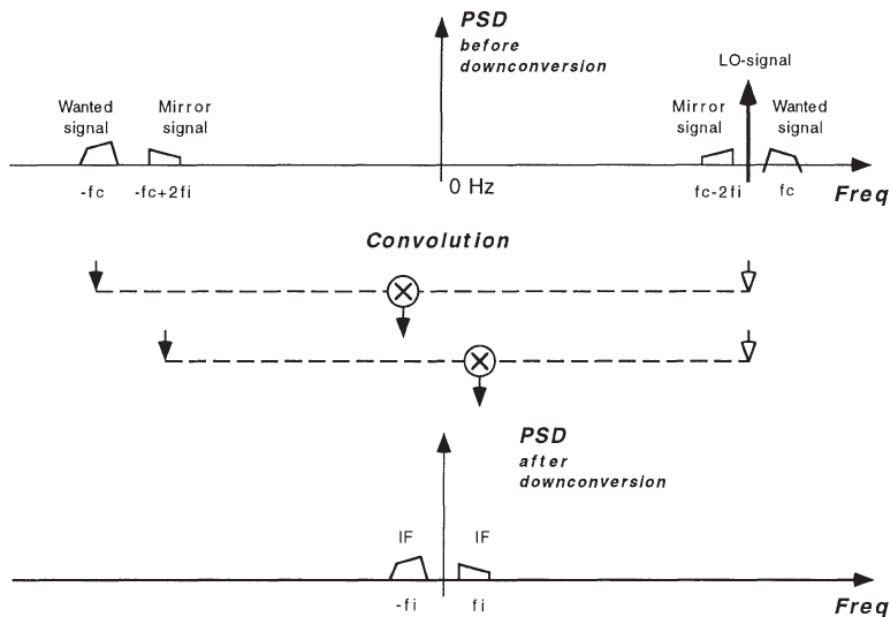
Ex. 1118, Fig. 3

Referring back to Figure 22(a) of Ex. 1125, the RF signals could also be downconverted using a single mixer and a sinusoidal signal (as shown by Figure 2.6 of Ex. 1134, reproduced below); however, the main disadvantage of mixing an RF signal of frequency f_c with just a single sinusoidal signal $\cos(2\pi f_{LO}t)$ to downconvert

to intermediate frequency f_i is that a second mirror signal of frequency f_c+2f_i is also downconverted to frequency f_i . Ex. 1134 at 24.



Ex. 1134, Fig. 2.6



Ex. 1134, Fig. 3.23

67. It was known that the mirror signal problem could be avoided by mixing the incoming RF signals with a complex signal, $\cos(2\pi f_i t) + j\sin(2\pi f_i t)$. Ex.

1134 at 28, 43; Ex. 1139 at 13. Mixing with such complex signals shifts a wanted RF signal at frequency f_c to frequency f_i while the unwanted mirror (or image) frequency signal at f_c+2f_i is shifted to frequency f_i . *Id.* Furthermore, separately mixing the RF signals with the signal $\sin(2\pi f_i t)$ produces the I-components of the RF signals, while mixing with $\cos(2\pi f_i t)$ produces the Q-components for the RF signals, and both of these components are needed for the DSP at the back end to ultimately demodulate the incoming RF signals. Ex. 1134 at 23. Filters can be used after the first stage of downconversion to filter out unwanted mirror signals. *Id.* at 28; Ex. 1139 at 17.

68. One could directly downconvert the incoming RF signal to baseband in the analog part of the RF receivers by using quadrature downconverters such that a second downconversion stage is not needed before the signals are forwarded to a demodulator; for example, zero-IF receivers perform such direct conversion. Ex. 1134 at 28; Ex. 1150 at 13-14. However, a significant problem in direct downconversion is the introduction of parasitic baseband signals at baseband, known as DC-offset, in the output of the quadrature downconverters. Ex. 1118 at 136; Ex. 1134 at 29; Ex. 1150 at 14-15. This DC-offset is mainly the result of the crosstalk between the incoming RF signals and the complex signal of the quadrature downconverters, the self-mixing phenomenon of the local oscillator producing the complex signal, the leakage of the complex signals to the input of the LNA, and/or

capacitive/inductive bondings between the different components of the RF receivers. Ex. 1118 at 136; Ex. 1134 at 29, 55-62; Ex. 1150 at 14-15. Such DC-offset issues are not present in low-IF receivers as the output of the first stage of mixing is at IF and not at baseband, and the downconversion at the second step is digitally performed. Ex. 1118 at 137-138; Ex. 1134 at 18. Furthermore, in the analog part of the RF receivers, mismatches between the two components of the complex signal and differences along the two branches of quadrature mixers and any following amplifiers and filters can cause the corruption of the I/Q components of the downconverted signals. Ex. 1118 at 138; Ex. 1134 at 29, 42, 55. However, such mismatches are not an issue in the second digital downconversion step. Ex. 1118 at 137; Ex. 1134 at 74, 76.

69. Analog-to-digital converters (ADCs) were commonly used in RF receivers for either IF or baseband signal sampling. Ex. 1139 at 18. Therefore, referring again to Figure 22(a) of Ex. 1125 (reproduced and annotated above), the quadrature downconverter (**red**) downconverts the incoming RF signals to produce I and Q components in IF before two ADCs (**gold**) separately digitize the IF I and Q components. *See* Ex. 1134 at 42. The digitized I and Q components are further downconverted to baseband by a digital complex mixer (**purple**) (comprising four digital mixers represented by the symbol $\otimes$ and two summers) before being forwarded to the DSP (**blue**).

8.3.2. Channel Selection based on Digital Filters

70. RF receivers receive RF signals for multiple television channels from cable and satellite television networks. Ex. 1135, 1:37-47. An important function for RF receivers is the ability to tune or filter out the signals for a desired television channel from the received RF signals such that only the signals of the desired television channels are demodulated. Ex. 1133 at 510. A POSITA would have known that digital filters based on digital signal processing are far superior to analog filters as digital filters do not suffer from manufacturing variations or aging, are easily programmable and tunable, have low power consumption, are unaffected by environmental influences, and have a superior performance-to-cost ratio. Ex. 1141 at 43. Digital filters, such as low pass filters and band pass filters, were known to select signals of desired television channels in RF receivers. Ex. 1135, 11:13-23, Fig. 7A; Ex. 1142, 6:5-8, Fig. 1B; Ex. 1143, 5:13-29, 5:46-53; Ex. 1150 at 44, 48.

- Low pass filter: A low-pass filter is a filter that passes signals with a frequency lower than a selected cutoff frequency (ω_c) and attenuates signals with frequencies higher than the cutoff frequency. Ex. 1141 at 14.

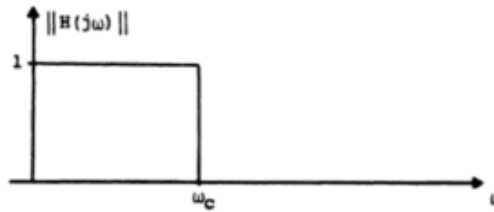


Fig. 1.23. Ideal LP filter magnitude frequency response.

Ex. 1141, Fig. 1.23

- Bandpass filter: A bandpass filter allows a specific range of frequencies (ω_1 to ω_2) to pass through while attenuating frequencies outside that range.

Ex. 1141 at 21.

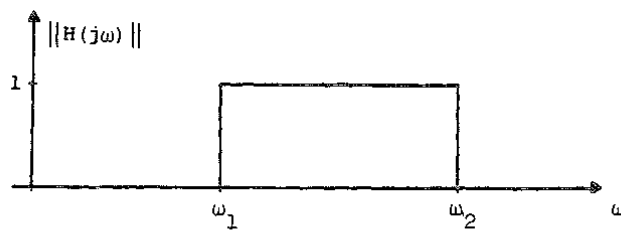


Fig. 1.27. Ideal BP filter.

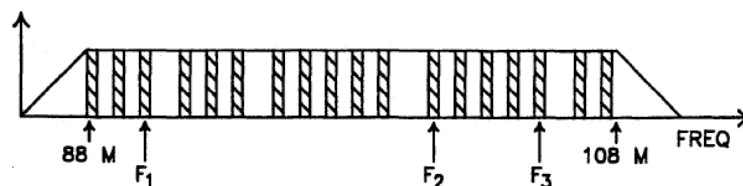
Ex. 1141, Fig. 1.27

A bandpass filter allows signals within a selected frequency range (e.g., signals for a selected television channel) to be isolated from undesired signals from outside the range. Ex. 1143, 5:13-15; Ex. 1150 at 44. Signals for a desired television channel can also be isolated from signals of undesired television channels by downconverting all the signals such that the signals for the desired television frequency are placed at baseband and then applying a low pass filter function to isolate the signals of the desired television channel. Ex. 1143, 5:46-50; Ex. 1150 at 48. However, low pass filters are preferred over bandpass filters as low pass filters

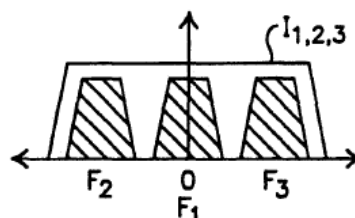
require fewer computational steps and, therefore, less computational power than bandpass filters. Ex. 1150 at 33, 48-49. It was also known to a POSITA that low pass filters and bandpass filters use well-known digital architectures of Finite Impulse Response (FIR) filters. Ex. 1141 at 24-63; Ex. 1143, 5:15-17; Ex. 1150 at 44.

71. Some receivers may allow signals of two or more desired channels to be filtered out such that consumers may enjoy a feature called picture-in-picture, where a small window showing one of the desired television channels is inserted into a larger window showing another one of the desired television channels. Ex. 1133 at 467; Ex. 1135, 4:37-43. For example, Khoini-Poorfard (Ex. 1135) describes using two RF receivers to filter and demodulate two television channels such that the filtered television channels can be used in the picture-in-picture feature. Ex. 1135, 4:37-43, 11:13-23, Fig. 7A.

8.3.3. Stacking of Desired Channels before Demodulation



Ex. 1144, Fig. 1



Ex. 1144, Fig. 6

72. Khoini-Poorfard (Ex. 1135) describes using two RF receivers that individually filter and demodulate two television channels. Ex. 1135, 4:37-43, 11:13-23, Fig. 7A. Kelly (Ex. 1144) describes an RF receiver that demodulates multiple desired channel bands without expensive hardware requirements and hardware duplications. Ex. 1144, 2:42-50. The RF receiver in Kelly digitizes RF signals comprising multiple desired RF bands in an RF spectrum (e.g., bands F_1 , F_2 , and F_3 in Figure 1 of Ex. 1144 reproduced above) and subjects the digitized signals to multiple frequency translations such that the desired bands are adjacent to each other (e.g., bands F_1 , F_2 , and F_3 are adjacent to each other in Figure 6 of Ex. 1144 reproduced above). *Id.*, 2:51-58, 4:38-40, 4:54-5:9. The desired frequency bands are then digitally separated, demodulated and processed to provide multiple outputs from the single receiver. *Id.*, 2:58-60.

8.3.4. Decimation

73. ADCs in RF receivers convert incoming RF signals to digital signals by sampling the RF signals at a rate that is at least twice the highest frequency of the RF signals. Ex. 1145 at 70. The reason for the high sampling rate is to prevent information loss during digitization; the Nyquist theorem specifies that a sinusoidal function in time or distance can be regenerated with no loss of information as long as it is sampled at a frequency greater than or equal to twice per cycle. *Id.*; Ex. 1133 at 98. That is, if you digitize an analog signal by sampling the signal at two or more

times the highest frequency contained in the signal, that signal can be theoretically converted back to the exact same analog signal by passing the signal through a low pass filter. The Nyquist theorem is a fundamental principle that enables us to digital signal process (DSP) analog signals (radio waves, sound waves, vibrations, etc.) that exist in the real world. Ex. 1133 at 98-101. Because the sample rate of the resulting signal from an ADC may be too high for subsequent DSP processing, decimation is typically performed on the sampled signals at baseband to lower the sampling rate. Ex. 1134 at 104; Ex. 1145 at 70. Decimation is a well-known process that reduces the original sample rate of a signal to a lower rate. Ex. 1145 at 14-15. A decimation filter can be implemented in a digital signal processing block of an RF receiver after the second downconverting step. Ex. 1134 at 104; Ex. 1145, Fig. 3.57; Ex. 1146, 2:51-57.

8.3.5. Demodulation of Multiple Channels

74. A POSITA would have been well aware that either a single demodulator or multiple demodulators can perform demodulation of signals for multiple selected television channels. Ex. 1119, 1:67-2:7, 2:32-35, 2:61-63, 3:50-52; Ex. 1144, 7:53:57. For example, Carson (Ex. 1119) describes a multichannel time-shared demodulator that demodulates the signals of multiple channels concurrently using time division multiple access (TDMA) techniques. Ex. 1119, 1:67-2:7, 2:32-35, 2:61-63, 3:50-52. Another example is shown in Azenkot

(Ex. 1175), which describes a single shared demodulator for demodulating multiple time-division multiplexed QAM channels in a cable modem termination system (CMTS) in a hybrid fiber-cable (HFC) network. Ex. 1175, Abstract, 1:6-14, 6:14-22, 6:30-37, 7:15-20, 32:53-33:14. As another example, Shadwell (Ex. 1176) discloses the system shown below, which receives multiple digitized downconverted channels (**green**), which are time-multiplexed together (**purple**) into a data stream (**orange**) that is output to a single demodulator (**brown**), which then provides a demodulated time-multiplexed output (**light blue**).

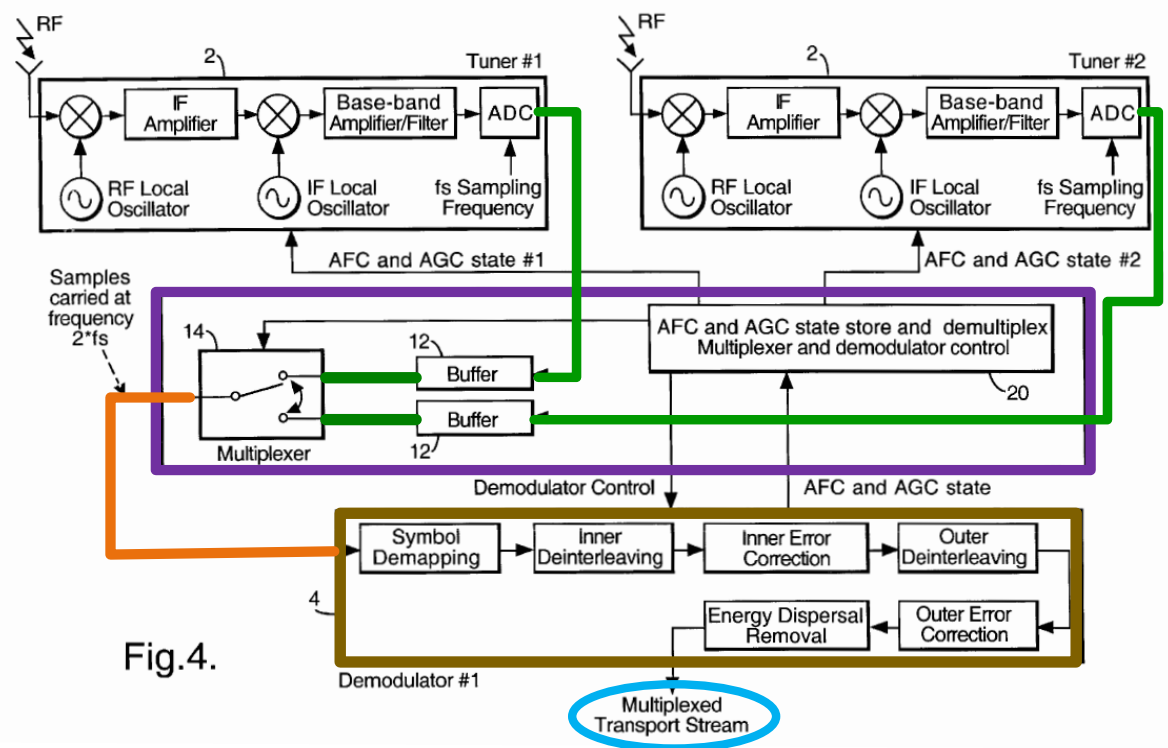


Fig.4.

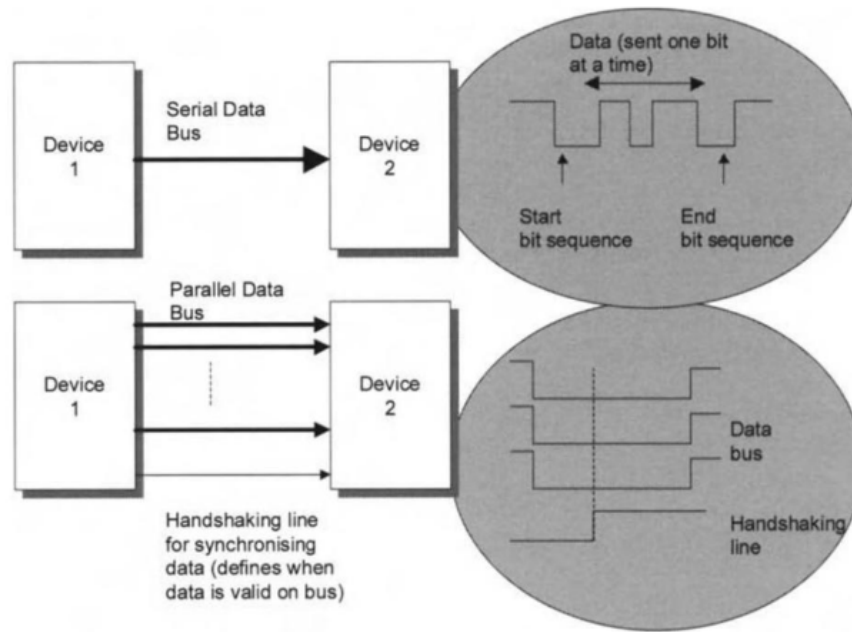
Ex. 1176, Fig. 4 (annotated)

A POSITA would have been well aware that single demodulator at the time, such as those disclosed in Carson, Azenkot, and Shadwell, were capable of demodulating

multiple selected channels. Ex. 1176, Abstract, 2:28-52, 3:6-17, 4:21-32, 6:19-37, Figs. 1a, 1b, 2, 4. The use of a single demodulator would reduce cost of the system, and enable certain functionality, such as providing a transport stream including two demodulated television channels, for example, for decoding a picture-in-picture stream. Ex. 1176, 2:13-26, 2:53-59.

8.4. Serial vs. Parallel Data Communication

75. As described throughout subsection 8.3.1 above, the different components of an IF receiver, including a low-IF receiver, were known to a POSITA prior to the '275 patent. It was also known to the POSITA by the earliest claimed priority date (April 17, 2009) of the '275 patent that the different components of low-IF receivers, such as the front end and the back end, could be fabricated on the same chipset or as different chipsets, and different types of buses could later connect the chipsets. Ex. 1134 at 23, 183; Ex. 1148 at 16. Data buses were known to pass data between electronic components. Ex. 1148 at 16. The data could be either passed in a serial manner by passing one bit at a time in a single bus, or in a parallel manner where several bits are transmitted simultaneously and each along its own separate channel. *Id.*; Ex. 1149, 1:10-28.



Ex. 1148, Fig. 2.3 (at 17)

76. A POSITA would have known that data transmission using parallel data buses offers a much higher data transmission rate than data transmission using a serial data bus. Ex. 1148 at 16. However, the parallel bus structure requires a larger number of conductors and more space on the chip. Ex. 1149, 1:32-40. Furthermore, due to natural aberrations in the structure of each bus (e.g., resistance), signals in parallel data buses do not arrive at the same time, creating a problem known as “skew.” *Id.* at 1:24-40. This problem becomes more severe as the distances between chipsets increase. *Id.*

77. Therefore, it was well known before the claimed priority date of the ’275 patent to use technologies such as those described above in Sections 8.2-8.4 to broadcast data for television channels using QPSK and QAM modulated RF signals,

and to use radio frequency receivers and tuners, such as low-IF receivers, to receive and process the RF signals to select one or more desired television channels. As also discussed above, such processing was well-known to include channel stacking, downconversion, channel selection (e.g., filtering), demodulation, and decimation, as well as parallel and serial bussing between receiver components.

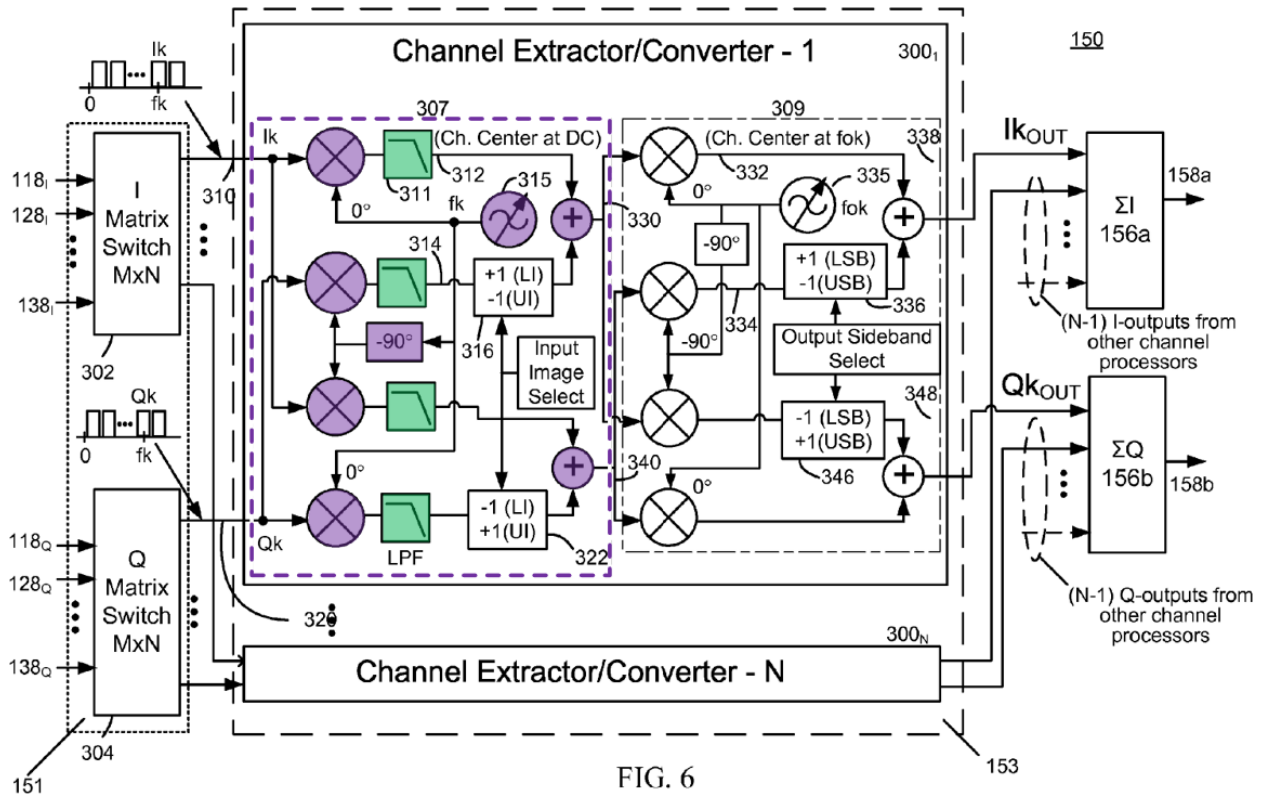
8.5. Petrovic (Ex. 1108)

78. U.S. Patent Application Publication No. 2009/0290659 (“Petrovic”) (Ex. 1108) is a publication of U.S. Patent Application No. 12/414,892 (“the ’892 Application”), which claims priority to, and incorporates by reference, U.S. Provisional Patent Application No. 61/054,886 to Petrovic et al. (“Petrovic ’886”, Ex. 1109), which was filed May 21, 2008. Ex. 1108, cover, [0001]. In my analysis below, I provide parallel citations where appropriate to both the figures and paragraph numbers of Petrovic ’886 (Ex. 1109) and the figures and paragraph numbers of Petrovic (Ex. 1108). I refer to Petrovic ’886 using paragraph numbers and figure numbers from the specification and drawings of Petrovic ’886, which are at pages 6-61 of Ex. 1109.

79. As I show below in Section 8.5.1 of this Declaration, it is my opinion that Petrovic ’886 provides written description support for at least independent claim 14 of Petrovic and provides written description support for the relied-on disclosure of Petrovic. Petrovic ’886 was filed on May 21, 2008. Ex. 1108, cover. Thus, I

downconversion (APD) stages 107_{I-M}” (two marked in **red** broken lines). Ex. 1108, [0032], Fig. 4; Ex. 1109, [0010], [0013], [0020], Fig. 1. Those APD stages downconvert RF signals into in-phase (I) and quadrature (Q) intermediate frequency (IF) components that are, after filtering, converted to digital form (i.e., digitized) by analog-to-digital converters 108_{I-M} (**gold**). Ex. 1108, [0032]-[0039], [0050]-[0052], Figs. 4-6; Ex. 1109, [0010], [0013], [0018]-[0024], [0031]-[0032], Figs. 1-3A.

82. Digital signal switching and pre-processing stage (DSSP) 150 (**blue**) receives the digitized signals and “extract[s] the channels of interest ... (i.e., remove[s] all the channels that are not of interest).” Ex. 1108, [0040], [0042], Fig. 4; Ex. 1109, [0015], [0025], [0033], Fig. 1. Figure 6 of Petrovic shows additional details of the DSSP 150, including “channel extractor/converter circuit 300.” Ex. 1108, [0058]; Ex. 1109, [0033], Fig. 3A.



Ex. 1108, Fig. 6 (annotated)

83. Also similar to the '275 patent, a channel is extracted from the digitized I, Q components corresponding to one of the RF sources 102-106 by downconverting those components in a complex mixer (**purple** and/or **purple** broken-line box) of a stage 307 so that the desired channel is at baseband, and filtering using low pass filters (LPFs) 311 (**green**), to create I, Q components 330, 340 for an extracted channel. Ex. 1108, [0060]-[0077]; Ex. 1109, [0037]-[0054]. The frequency f_k used for the downconversion to baseband is selected based on a frequency corresponding to a desired channel. Ex. 1108, [0066]; Ex. 1109, [0045].

84. The I and Q signals 330 and 340 of the extracted channel are upconverted to a desired output frequency in the stage 309, and then summed with other upconverted channels (from stages 309 of other channel/extractor converters) in combiners 156a and 156b to result in the I and Q components 158a and 158b. Ex. 1108, [0078]-[0086]; Ex. 1109 [0055]-[0061].

85. In my opinion, Petrovic is in the same field of endeavor as the '275 patent and reasonably pertinent to problems with which the '275 patent is concerned, and is thus analogous art. Petrovic describes a system and method for receiving wideband RF signals comprising multiple channels, as well as selecting individual channels (in the same way as the '275 patent) by conversion to baseband and filtering. Ex. 1101, 6:21-7:15, Fig. 3; Ex. 1108, Abstract, [0029]-[0030], [0042], [0047], [0050], [0058]-[0077], Figs. 4, 6; Ex. 1109, [0010]-[0011], [0013], [0015]-[0016], [0020], [0023], [0033], [0037]-[0054], Figs. 1, 3A.

8.5.1. Petrovic is Entitled to a Priority date of May 21, 2008

86. It is my understand that, regardless of whether Petrovic is entitled to the priority of Petrovic '886, Petrovic is prior art to the '275 patent under pre-AIA 35 U.S.C. § 102(e) because the application of which Petrovic is a publication was filed on March 31, 2009, which is before the earliest possible priority date of the '275 patent (April 17, 2009). It is my understanding that a reference patent or printed publication (such as Petrovic) is entitled to claim the benefit of the filing date of an

earlier-filed provisional application (such as Petrovic '886) if the disclosure of the earlier-filed provisional application provides support for one or more claims in the reference patent/publication, and if the relied-on portions of the reference patent/publication are supported by the earlier-filed provisional application.

87. As shown in the table below, Petrovic '886 provides support for at least claim 14 of Petrovic. Moreover, and as shown by the parallel citations to Petrovic and Petrovic '886 provided in this declaration, the relied-on portions of Petrovic are supported by Petrovic '886. Thus, Petrovic is entitled to the May 21, 2008 priority date of Petrovic '886, and is also prior art to the '275 patent under pre-AIA 35 U.S.C. § 102(e) as of May 21, 2008.

Petrovic – Claim 14 (Ex. 1108)	Petrovic '886 (Ex. 1109)
14. A method for assembling channels in a composite signal, the method comprising:	[0001], [0004], [0008], Claim 16.
a) downconverting, in a single frequency translation process, a first input signal comprising a first plurality of channels to a first IF signal comprising said plurality of first channels;	[0005], [0010], [0014], [0029], [0031], [0032], Claim 16, Figs. 1 and 2
b) converting the first IF signal into a first digital IF signal;	[0010], Claim 16, Fig. 1
c) downconverting, in a single frequency translation process, a second input signal	[0005], [0013], [0014], [0023], [0029], [0031], [0032], Claim 16, Figs. 1, 2

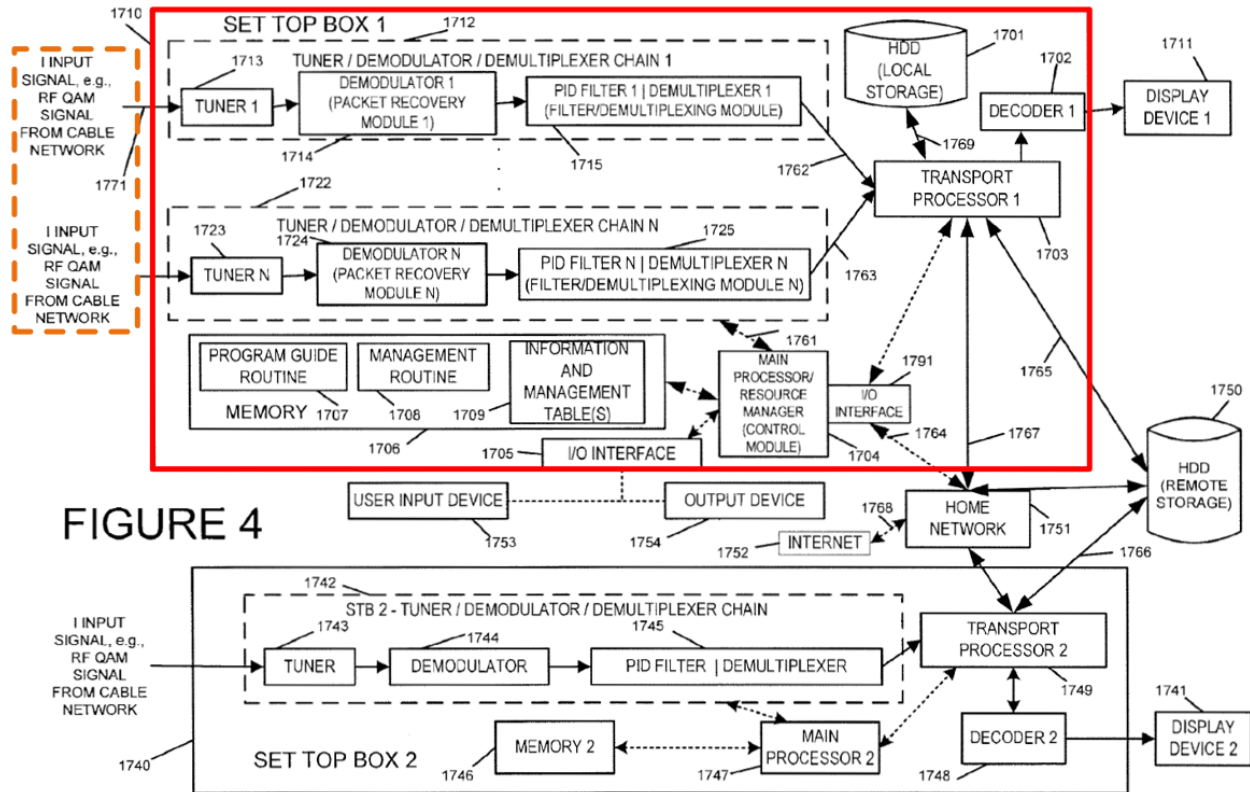
Petrovic – Claim 14 (Ex. 1108)	Petrovic '886 (Ex. 1109)
comprising a plurality of second channels to a second IF signal comprising said plurality of second channels;	
d) converting the second IF signal into a second digital IF signal; and	[0005], [0013], [0024], Claim 16, Fig.1
e) assembling, in the digital domain, at least one of the first channels and at least one of the second channels into a digital composite signal.	[0015], [0025], [0036]-[0068], [0080], Claim 16, Figs. 3A, 3B

8.6. Cholas (Ex. 1158)

88. U.S. Patent Application Publication No. 2010/0020794 (“Cholas”) (Ex. 1158) is a publication of U.S. Patent Application No. 11/754,714 that was filed May 29, 2007. Ex. 1158, cover. Thus, I understand that Cholas is prior art under pre-AIA 35 U.S.C. § 102(e), because the application on which Cholas is based was filed before the earliest possible priority date of the '275 patent (i.e., before April 17, 2009).

89. Cholas describes a set-top box (STB) 1710 (red) with tuner/demodulator/demultiplexer chains 1-N that receive “input signal[s] [orange]

... from the cable network.” *Id.*, [0044], [0010]-[0011], [0024], [0059]-[0071], Figs. 4, 6.



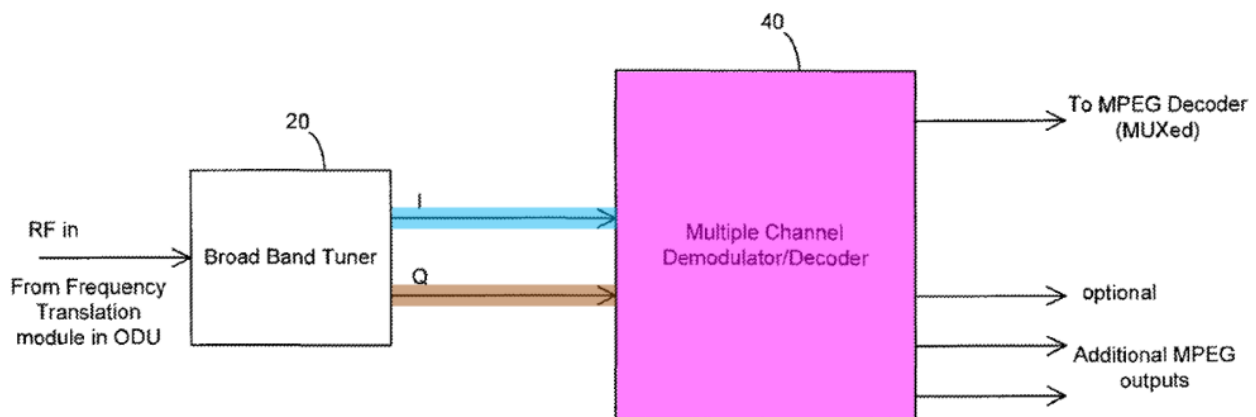
Ex. 1158, Fig. 4 (annotated)

90. In my opinion, Cholas is analogous art, as it is in the same field of endeavor as the '275 patent and reasonably pertinent to problems with which the '275 patent is concerned. Like the '275 patent, Cholas “relates to wideband receiver systems that are capable of receiving multiple desired television channels.” Ex. 1101, 1:36-37; Ex. 1158, [0001], [0043]-[0045], [0052]-[0057], Figs. 4-5. Cholas also relates to cable network STBs, an expected environment for the wideband receiver system of the '275 patent. Ex. 1101, 1:52-54, 5:12-16, claims 9, 10; Ex. 1158, [0043]-[0045], Fig. 4.

8.7. Eidson (Ex. 1112)

91. U.S. Patent No. 7,783,958 to Eidson (“Eidson”) indicates on its face that it issued on August 24, 2010. Ex. 1112, cover. I understand that Eidson qualifies as prior art to the ’275 patent. As indicated above, the patent number for Eidson appears in one place in the file history of the ’275 patent, but the extent to which Eidson might have been considered is unclear. Ex. 1101 at 1-3 (Eidson not included in “References Cited”); Ex. 1104, at 3411.

92. Eidson describes a multiple-channel receiver that demodulates multiple channels using a multiple channel demodulation and error correction decoding engine. Ex. 1112, Abstract, 8:27-30. Eidson’s Figure 8 “shows a broadband tuner and multi-channel demodulator and decoder” according to the Eidson invention. Ex. 1112, 7:58-59.



Ex. 1112, Fig. 8 (annotated)

93. A frequency translation module located in an outdoor unit selects desired satellite transponder channels and translates those selected channels to a contiguous section of bandwidth that is received by a broad band tuner 20. Ex. 1112, 8:43-57. The digital outputs of the tuner 20 are I (**light blue**) and Q (**brown**) signals that represent multiple selected transponder channels. Ex. 1112, 8:54-57, 9:5-25, Figs. 9-10. As discussed in more detail below, these I and Q signals input to the multiple channel demodulator/decoder 40 (**pink**) are functionally the same as the summed I signal 158a and the summed Q signal 158b output by the Petrovic DSSP 150. In Eidson, the digital I and Q output of the broadband tuner 20 “is processed by a multiple channel demodulator and decoder 40 to produce one or more MPEG streams comprising multiple video programs derived from the selected transponder channels.” Ex. 1112, 8:65-9:2.

94. In my opinion, Eidson is reasonably pertinent to problems with which the '275 patent is concerned, and is analogous art to the '275 patent on at least that basis. For example, the '275 patent indicates that signals recovered from received RF signals may be output to a demodulator, but leaves the particulars to “commonly known methods.” Ex. 1101, 7:16-19, Fig. 2. A POSITA would consider Eidson, which relates to demodulation of signals for multiple channels, as a pertinent example of those “commonly known methods.” Moreover, a POSITA would have

similarly considered Eidson pertinent to Petrovic, which generates multichannel digital I and Q signals that are functionally the same as signals described in Eidson.

8.8. Rabaey (Ex. 1116)

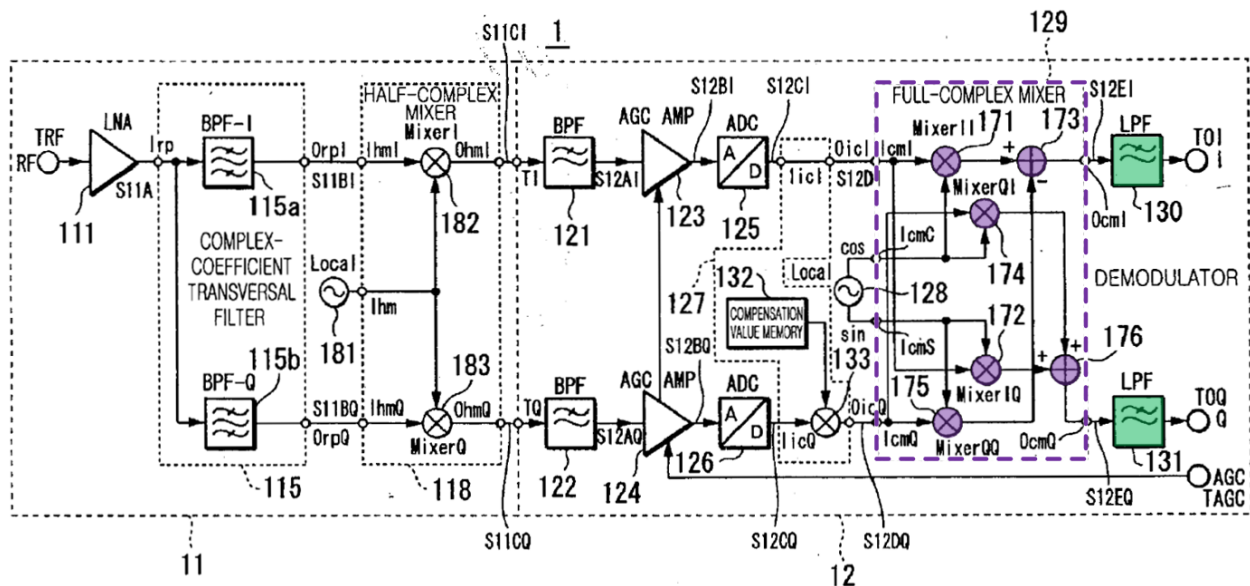
95. Rabaey is a textbook on digital integrated circuit design (Ex. 1116) (“Digital Integrated Circuits[;] A Design Perspective”). It is my understanding that Rabaey was publicly available more than one year before the earliest possible priority date of the ’275 patent, and that Rabaey is thus prior art to the ’275 patent under pre-AIA 35 U.S.C. § 102(b). Ex. 1173, ¶¶ 47-54. In my opinion, Rabaey is reasonably pertinent to problems with which the ’275 is concerned, and is analogous art. The ’275 patent describes at length how signals may be processed in digital form. Ex. 1101, 5:56-7:15, Figs. 2-3. Integrated circuits were a well-known and widely-used way to implement digital processing in electronics. Ex. 1116 at 17 (recognizing “continuous trend towards digital solutions in all other areas of electronics”), 28 (“The purpose of this book is to provide a bridge between the abstract vision of digital design and the underlying digital circuit and its peculiarities”). In my opinion, a POSITA would have known that Rabaey describes the “commonly known methods” of sending “a serial or parallel digital data stream to a demodulator using a serial or parallel data interface” that the ’275 patent also refers to. Ex. 1101, 7:16-20.

8.9. Lee (Ex. 1153)

96. U.S. Patent Application Publication No. 2008/0039036 (“Lee”) was published February 14, 2008. Ex. 1153, cover. Lee is prior art to the ’275 patent under pre-AIA 35 U.S.C. § 102(b), because Lee published more than one year before the earliest possible priority date of the ’275 patent. Lee describes a STB that receives cable broadcasting signals. Ex. 1153, [0035]. In my opinion, Lee is analogous art, as it is in the same field of endeavor as the ’275 patent (e.g., receiving cable signals) and reasonably pertinent to problems with which the ’275 patent is concerned. For example, Lee describes an STB having claimed features (picture-in-picture display). Ex. 1101, claims 6, 16; Ex. 1153, [0007], [0031].

8.10. Takahiko (Ex. 1161)

97. U.S. Patent Application Publication No. 2006/0256216 (“Takahiko”) was published November 16, 2006. Ex. 1161, cover. Takahiko is prior art to the ’275 patent under pre-AIA 35 U.S.C. § 102(b), because Takahiko published more than one year before the earliest possible priority date of the ’275 patent. Referring to the annotated figure below, Takahiko discloses a downconverter of a radio receiver that includes a digital baseband complex mixer (**purple**) and low pass filters (**green**) similar to those of the ’275 patent. Ex. 1161, [0143], [0153], [0156].



98. In my opinion, Takahiko is reasonably pertinent to problems with which the '275 patent is concerned, and is analogous art to the '275 patent on at least that basis. For example, Takahiko describes circuits, very similar to those described by the '275 patent, used for similar purposes (reception and tuning of RF signals). Ex. 1161, [0143]-[0156], Fig. 1.

8.11. Maalej (Ex. 1160)

99. U.S. Patent No. 6,160,443 (“Maalej”) was issued December 12, 2000. Ex. 1160, cover. Maalej is prior art to the ’275 patent under pre-AIA 35 U.S.C. § 102(b), because Maalej published more than one year before the earliest possible priority date of the ’275 patent. Maalej discloses a QAM demodulator for, e.g., demodulating 6 MHz CATV channels. Ex. 1160, 1:6-8, 1:28-33, 3:47-52. In my opinion, Maalej is reasonably pertinent to problems with which the ’275 patent is

concerned, and is analogous art to the '275 patent on at least that basis. For example, Maalej describes demodulators that can be used for a claimed feature (“at least one demodulator”). Ex. 1101, claims 1, 11; Ex. 1160, 1:6-8, 1:28-32, 3:47-52.

9. OPINIONS WITH RESPECT TO THE '275 PATENT

9.1. Petrovic in View of Eidson Renders Claims 1, 4, 7-9, 11, 14, and 17-19 Obvious

100. In the following, I provide a limitation-by-limitation analysis showing how Petrovic in view of Eidson renders claims 1, 4, 7-9, 11, 14, and 17-19 obvious. To help illustrate how the disclosures of these references map to the claim limitations, I have color coded some of my remarks and some figures in the noted art below. Also, in my analysis throughout this declaration, I will sometimes refer to combinations of references with dashes between them. For example, I will refer to a combination of Petrovic and Eidson as “Petrovic-Eidson.”

9.1.1. Independent Claim 1

101. The limitations of claim 1 appear below and in the Claims Listing Appendix, labeled as limitations [1A]-[1F]. For the following reasons, it is my opinion that claim 1 is rendered obvious over Petrovic-Eidson.

a. [1A]: “A method for operating a television receiver, comprising:”

102. It is my opinion that Petrovic discloses “[a] method for operating a television receiver, comprising:” as claimed.

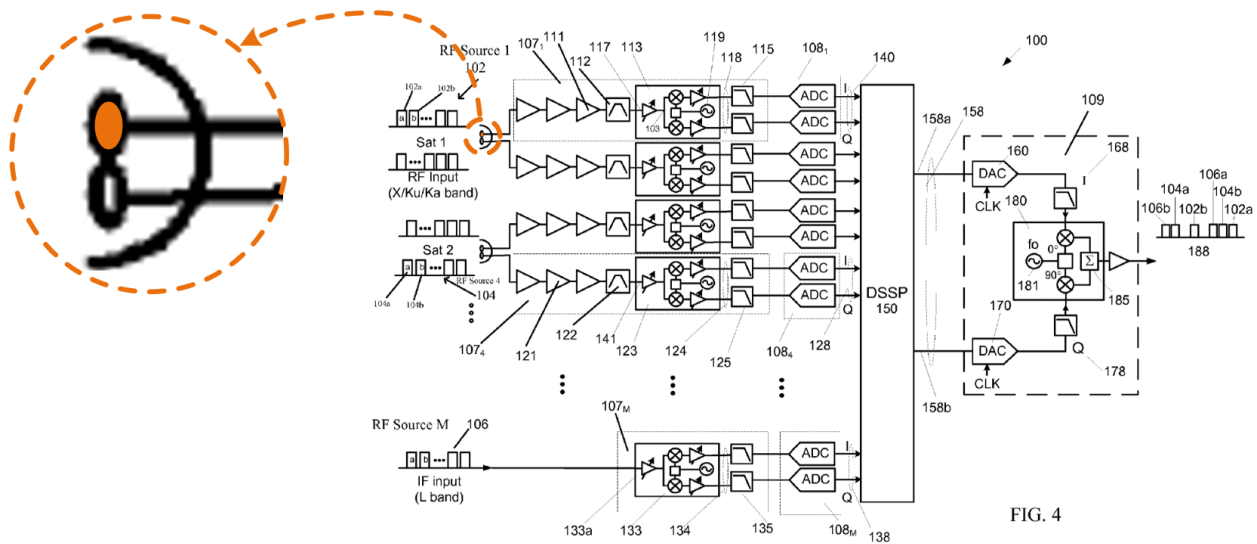
103. In my opinion, preamble [1A] simply refers to claim 1 being a method claim and does not impose any particular limitations on the claim. Nevertheless, to the extent the preamble is considered limiting, it is my opinion that Petrovic teaches preamble [1A]. Petrovic describes a method of operating a channel stacking system 100. Ex. 1108, Title, [0008], [0028]-[0096]; Ex. 1109, Title, [0008]-[0069]. That system—including the APD stage 107₁, ADC pair 108₁, and DSSP 150 discussed below—receives satellite signals 102 and is thus a “receiver.” Ex. 1108, [0028]-[0029]; Ex. 1109, [0010]-[0013]. As explained in Section 9.1.1.b for limitation [1B], those signals comprise multiple channels.

104. In my opinion, a POSITA would have understood those channels to include television channels. For example, Petrovic discloses outputting signals from the system 100 “to a rendering device, such as a set-top box, or other receiver/tuner,” which are devices associated with output of television programming to users. Ex. 1108, [0028], [0054]; Ex. 1109, [0008], [0030]. Moreover, and as a POSITA would have understood, satellite communication had long been used for transmission of television programming channels to end users. For example, Coffin discloses that video content received by home satellite receiving systems includes television programs Ex. 1154, [0011], *see also* [0017], [0020]-[0022]; Ex. 1155, 3:13-19 (satellite transmission of QPSK-modulated television channels). In fact, “[s]atellite television and data broadcast services from Direct Broadcast Satellites (DBS)

operating in the Broadcast Satellite Service (BSS) to homes with stationary antennas comprises well known art.” Ex. 1156, [0005]. Because satellite communication was so commonly used for transmission of television programming to end users, in my opinion a POSITA would have been motivated to use the Petrovic channel stacking system 100 in a home satellite reception system for obtaining and outputting television programming via television channels. Doing so would have involved merely combining known prior art elements (Petrovic’s channel stacking system that receives channels that were transmitted by satellite, and the fact that it was well-known to receive television programming channels that were transmitted by satellite) according to known methods (by using the channel stacking system 100 in the manner Petrovic discloses to receive the channels) to yield predictable results (the channels of Petrovic being television channels that could be transmitted via satellite and received by the channel stacking system 100 of Petrovic).

- b. [1B]: “receiving by an input terminal, an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels, wherein the plurality of desired channels are non-contiguous;”**

105. It is my opinion that Petrovic discloses limitation [1B]. Petrovic Figure 4 shows an input terminal (**orange**) of the system 100. Ex. 1108, [0029], Fig. 4; Ex. 1109, [0010], [0019], Fig. 1.



Ex. 1108, Fig. 4 (annotated)

106. Referring to annotated Figure 4 of Petrovic above, the channel stacking system 100 receives a signal 102 that comprises “4, 6, 8, 16, 24, 28, 32, 40, 48, 60, 120 or more” satellite channels. Ex. 1108, [0028]-[0029], Fig. 4; Ex. 1109, [0005], [0010]-[0011], [0016], Fig. 1. A POSITA would have understood that the Petrovic satellite channels are “broadcast channels.” The ’275 patent acknowledges that satellite channels are a type of broadcast channel. Ex. 1101, 12:60-61.

107. Petrovic also discloses that the channels in the RF signal 102 may include “a plurality of desired channels” and a “plurality of undesired channels.” Ex. 1108, [0042], [0053], [0055], [0058], Figs. 4, 6; Ex. 1109, [0004]-[0005], [0015], [0025], [0033], [0036], Figs. 1, 3A, 3B. As explained in detail in Section 9.1.1.e for limitation [1E], Petrovic discloses extracting, or selecting, less than all of the channels included in a received RF signal. Ex. 1108, [0042], [0053], [0055], [0058]; Ex. 1109, [0004]-[0005], [0015], [0025], [0033], [0036], Figs. 1, 3A, 3B. Consistent

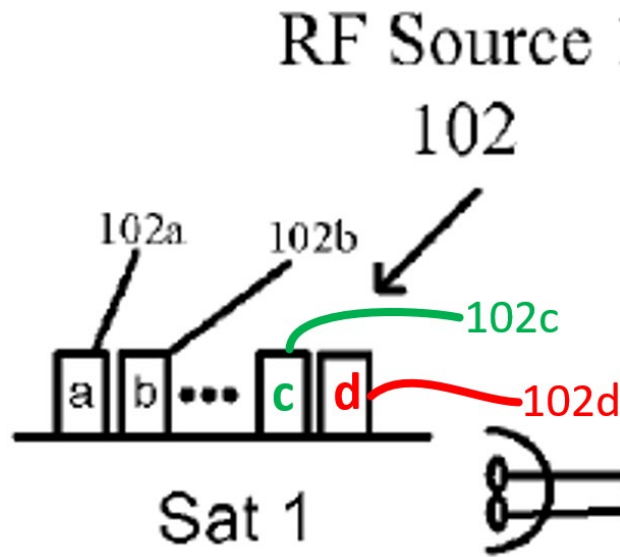
with the use of “desired” and “undesired” in the ’275 patent, a selected Petrovic channel is desired and an unselected Petrovic channel is undesired. Ex. 1101, Abstract, 1:46-51, 3:29-60, 4:43-58, 5:66-6:3, 6:8-20, 6:59-7:2, 7:16-25.

108. In my opinion, a POSITA would have understood that the Petrovic system would be operated so as to receive noncontiguous desired channels. For example, the Petrovic system 100 “‘stack[s]’ or assemble[s] channels resident within an RF signal into a composite signal in which the received channels are placed (or sequenced) in desired channel slots for output to a rendering device, such as a set-top box, or other receiver/tuner.” Ex. 1108, [0028]; Ex. 1109, [0008]. Petrovic discloses that the number of available slots in that composite signal may be much less than the total number of channels received by the system 100 in the RF signal 102. Ex. 1108, [0029] (received signal 102 may have 120 or more channels), [0055] (output signal 158 may have as few as four channel slots); Ex. 1109, [0016], [0033]. A POSITA would thus have understood from Petrovic that, in order for the system 100 to stack four channels selected from 120 channels in an input signal, the system 100 would need to be able to select at least two channels that are not contiguous in the received RF signal.

109. Moreover, as a matter of common experience, and as a POSITA would have understood, users of a satellite system such as in Petrovic would select channels according to their individual desires to watch content carried via those channels, and

without regard to underlying frequencies used to carry the content channels in the signal 102. For example, and as explained in Eidson, a typical STB would “select[] the specific satellite signal it needs to view a desired program by monitoring an internal look-up table guide that lists the specific satellite, polarization and transponder required for reception of the program.... A satellite transponder signal is also called a channel.” Ex. 1112, 1:40-45. In other words, a human user selecting programs would normally not be aware of the channel on which those programs were carried. Thus, a POSITA would have expected that, inevitably, a user would select content channels within non-contiguous RF channels. Indeed, the '275 patent recognizes that it was known that, inevitably, users would select (i.e., “desire”) channels that are non-contiguous in a received RF bandwidth. Ex. 1101, 1:44-48, 1:55-58, 2:16-18.

110. Moreover, and because the output signal 158 may have 4 or more channel slots, a POSITA would have understood that the Petrovic system 100 would be operated so as to select at least 3 channels from a signal 102. Ex. 1108, [0055]; Ex. 1109, [0033]. When at least 3 channels from a signal 102 were selected, at least 2 of those channels (a “plurality”) would necessarily be separated by a third of those channels, with those 2 channels thus being “non-contiguous” to each other. For example, consider the upper left portion of Petrovic Figure 4:



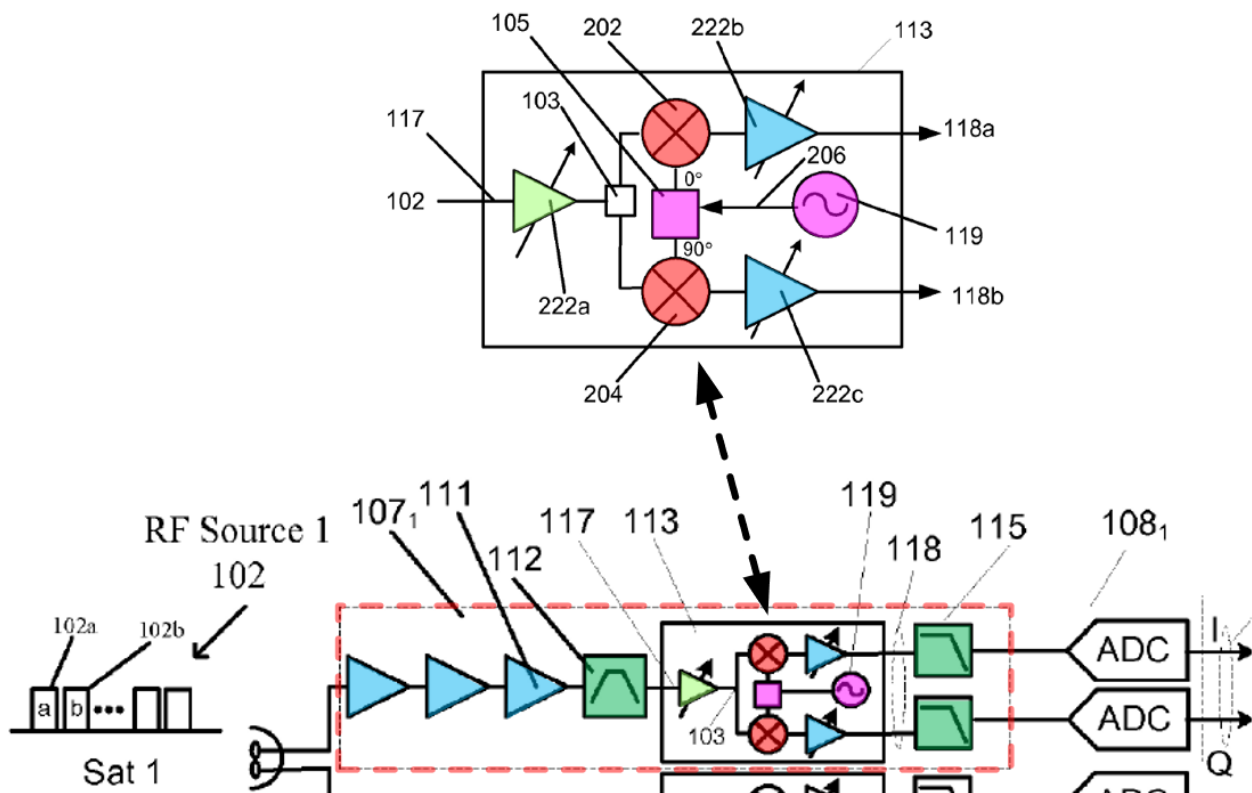
Ex. 1108, Fig. 4 (excerpted and annotated)

Petrovic Figure 4 shows that RF signal 102 comprises channels 102a, 102b, 102c (indicated by **green** annotation), 102d (indicated by **red** annotation), and some unspecified number of channels, between channels 102b and 102c, indicated by 3 dots. Ex. 1108, [0029], [0033], [0036], Fig. 4; Ex. 1109, [0010], [0016], Fig. 1. If channels 102a, 102b, and 102c are selected/desired, channels 102a and 102c are non-contiguous because they are separated from each other at least by channel 102b. Similarly, if channels 102b, 102c, and 102d are selected/desired, channels 102b and 102d are non-contiguous because they are separated from each other at least by channel 102c.

111. In sum, Petrovic discloses receiving, by an input terminal of system 100, an RF signal 102 that comprises a plurality of desired and undesired satellite channels, and that the plurality of channels includes both desired and undesired channels. Thus, it is my opinion that Petrovic discloses Element [1B].

c. [1C]: “processing, by a radio front end coupled to the input terminal, the input signal to generate a processed input signal;”

112. It is my opinion that Petrovic discloses limitation [1C]. The Petrovic system 100 comprises a “radio front end” (**red** broken line), which Petrovic calls an analog preprocessing and downconversion (APD) stage 107₁, coupled to the input terminal and that generates a processed input signal. Ex. 1108, [0032]-[0039], Figs. 4-5; Ex. 1109, [0010], [0017], [0031], Figs. 1-2.



Ex. 1108, Fig. 5 (excerpted and annotated) (top)
Ex. 1108, Fig. 4 (excerpted and annotated) (bottom)

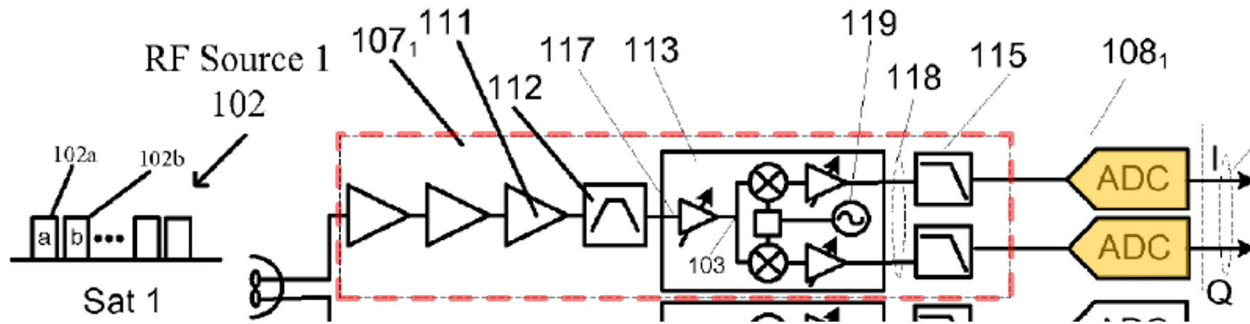
113. In my opinion, the Petrovic APD stage 107₁ performs processing that includes amplifying by amplifiers 111 (**light blue**), filtering by filter 112 (**green**), amplifying by amplifier 222a (**light green**), mixing by mixers 202 and 204 (**red**)

using 90° phase-shifted oscillator signals from a synthesizer/frequency source 119 (pink) and a phase shifter 105 (pink), amplifying by amplifiers 222b and 222c (light blue), and filtering by low pass filters 115 (green). Ex. 1108, [0032]-[0039], Figs. 4-5; Ex. 1109, [0010], [0017], [0031], Figs. 1-2. The processing by the Petrovic APD stage 107₁ includes the same type of processing performed by the radio front end 210 of the '275 patent, and generates the same type of processed input signal - downconverted and filtered in-phase and quadrature components of an input signal. Ex. 1101, 4:40-5:25, Fig. 2; Ex. 1108, [0032]-[0039], Figs. 4-5; Ex. 1109, [0010], [0017], [0031], Figs. 1-2.

114. In sum, Petrovic discloses performing processing, by the Petrovic APD stage 107₁ coupled to the input terminal, the input signal 102 and generating, by the Petrovic APD stage 107₁, a processed input signal. Thus, it is my opinion that Petrovic discloses Element [1C].

d. [1D]: “digitizing, by an analog-to-digital converter (ADC) coupled to the radio front end, the processed input signal to generate a digitized signal;”

115. It is my opinion that Petrovic discloses limitation [1D]. Petrovic system 100 includes an ADC pair 108₁ (gold) that is coupled to the radio front end 107₁ (red broken line). Ex. 1108, [0039], Fig. 4; Ex. 1109, [0005], [0010], [0022], Fig. 1.



Ex. 1108, Fig. 4 (excerpted and annotated)

116. The ADC pair 108₁ digitizes the processed input signal, received from the APD stage 107₁, to generate a digitized signal. Ex. 1108, [0039], [0051]-[0052], Fig. 4; Ex. 1109, [0005], [0010], [0018], [0019], [0022], Fig. 1.

117. In sum, Petrovic discloses digitizing, by the ADC pair 108₁ coupled to the Petrovic APD stage 107₁, the processed input signal to generate a digitized signal. Thus, it is my opinion that Petrovic discloses Element [1D].

e. [1E]: “selecting, by a digital frontend (DFE) coupled to the ADC, the plurality of desired channels from the digitized signal; and”

118. It is my opinion that Petrovic discloses limitation [1E]. The Petrovic DSSP 150 (blue) is a DFE that selects desired television channels from the digitized signals received from the ADC pair 108₁. Ex. 1108, [0042], [0053], [0058]-[0077], Figs. 4, 6; Ex. 1109, [0004] (“[t]he present invention provides for a channel stacking system ... which processes channel selection ... within the digital domain”), [0005], [0015], [0025], [0033], [0037]-[0054], Fig. 1.

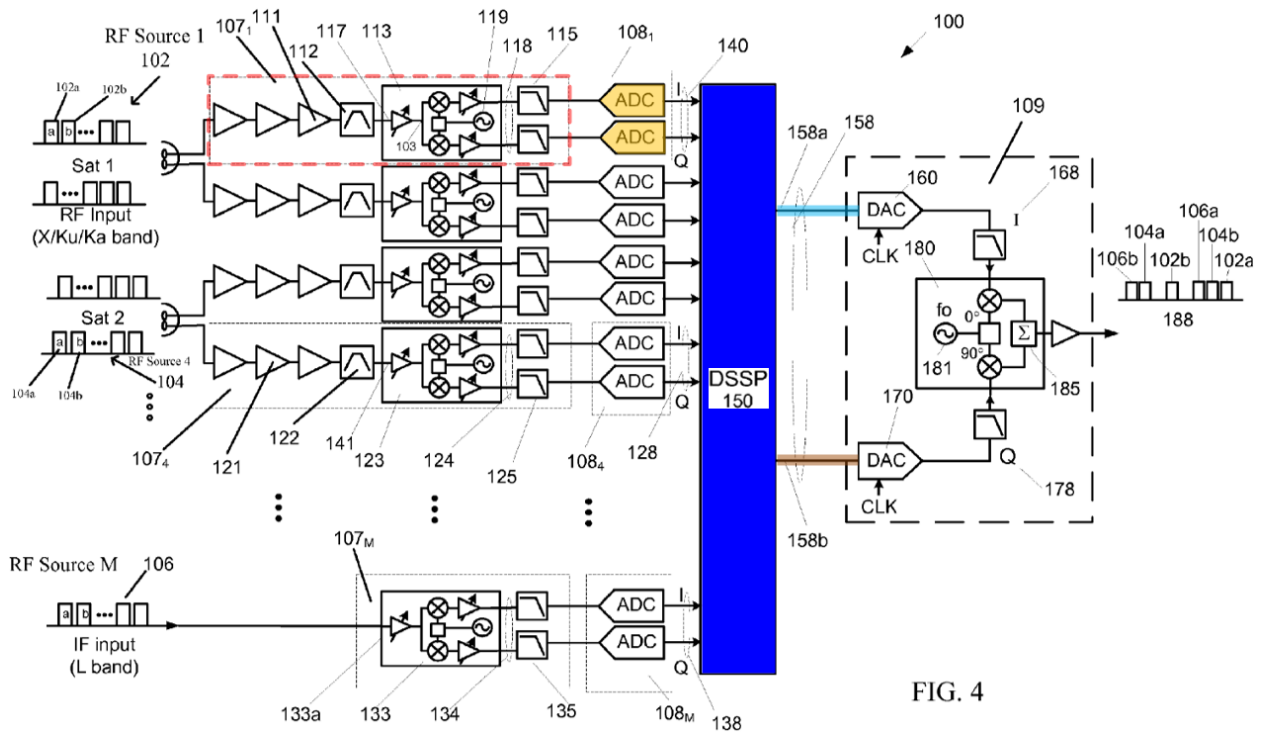
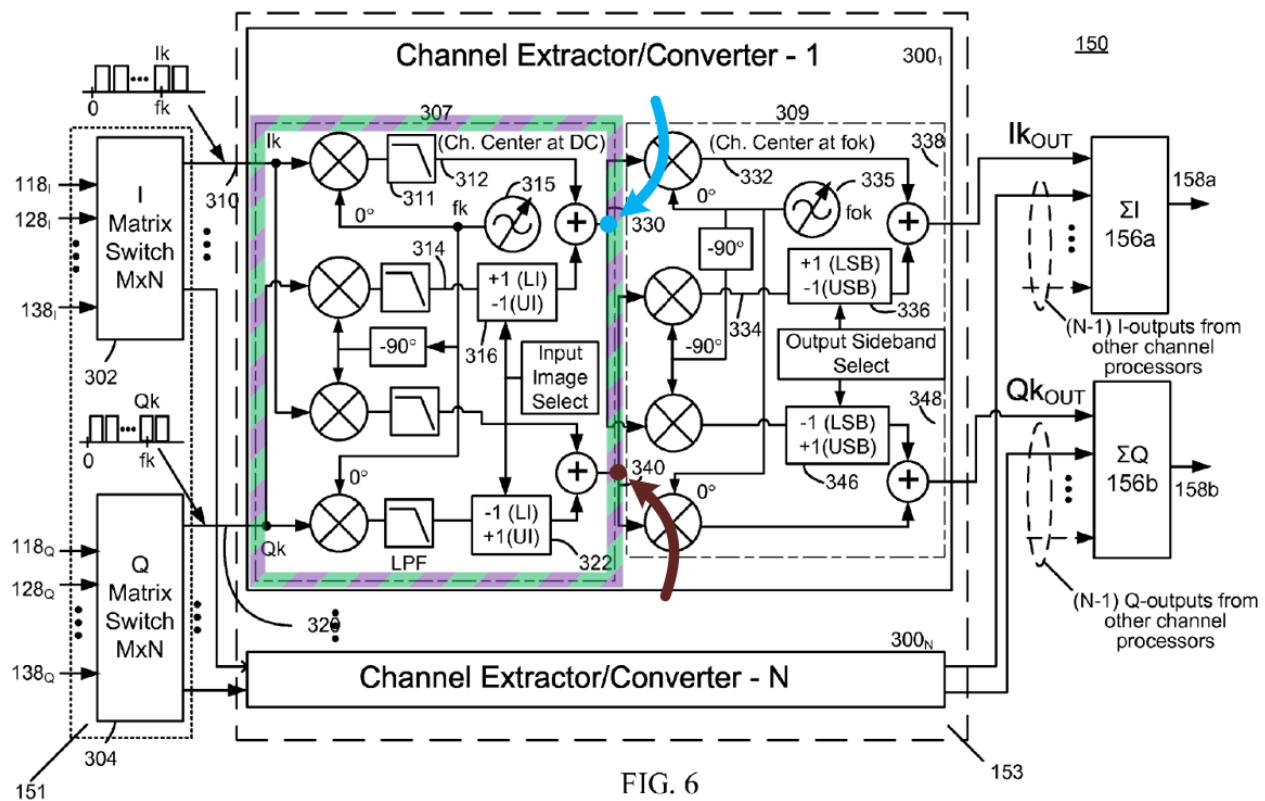


FIG. 4

Ex. 1108, Fig. 4 (annotated)

119. As explained in Section 9.1.1.d for limitation [1D], and as can be seen in Figure 4, the ADC pair 108₁ digitizes I,Q components of a signal that include channels (desired and undesired) from a received RF input signal 102. Petrovic Figure 6 shows additional details of the DSSP 150. Ex. 1108, [0016], [0055]; Ex. 1109, [0007], [0033].



Ex. 1108, Fig. 6 (annotated)

120. The DSSP 150 includes multiple circuits 300, that are shown in Figure 6 as circuits 300₁ (“Channel Extractor/Converter – 1”) through 300_N (“Channel Extractor/Converter – N”), with each circuit 300 comprising a channel extraction stage 307 (purple/green), and with each of those stages 307 able to select a different channel. Ex. 1108, [0055], [0059]-[0077], Fig. 6; Ex. 1109, [0033], [0037]-[0054], Fig. 3A. The stages 307 “extract [i.e., select] the channels of interest [i.e., desired channels]” from the signals received from the ADC pair 108₁ and “remove all of the channels that are not of interest,” i.e., the claimed “undesired channels.” Ex. 1108, [0042], [0053], [0055], [0058], Figs. 4, 6; Ex. 1109, [0003], [0004] (“[t]he present invention provides for a channel stacking system ... which processes channel

selection ... within the digital domain”), [0005], [0015], [0025] (digital signal processor 150 “assemble[s] a composite signal 158 having the desired channels”), [0033] (channel extractor/converter circuits of digital signal processor 150 “extract a desired channel”), [0036], Fig. 1. A stage 307 extracts a desired channel from the digitized I, Q components, corresponding to the RF source 102, received from ADC pair 108₁ and outputs an I component 330 (**light blue** dot and arrow) and a Q component 340 (**brown** dot and arrow) corresponding to a selected/desired channel. Ex. 1108, [0051], [0053], [0060]-[0077], Figs. 4, 6; Ex. 1109, [0018]-[0019], [0022], [0025], [0037]-[0054], Figs. 1, 3A.

121. In fact, Petrovic describes the same selection technique that is described by the '275 patent. For example, the '275 patent discusses frequency shifting to baseband and filtering of the baseband signal, while Petrovic explains that desired channels are digitally translated to baseband and “[t]he translated channels are then digitally lowpass filtered ..., leaving only the channel of interest.” Ex. 1101, 6:21-7:15, Fig. 3; Ex. 1108, [0042], [0058]-[0077], Fig. 6. Petrovic '886 also describes the same selection technique that is described by the '275 patent. For example, Petrovic '886 explains that “channel extraction ... is performed by direct digital conversion to zero IF, followed by channel filters.” Ex. 1109, [0025], *see also* [0036]-[0054], Fig. 3A. Petrovic '886 further explains that digital signal processor 150 is operable to “extract and order at least one *of* the first plurality of channels ...

into the desired channel slot positions,” thus indicating that not all of the channels need to be selected. Ex. 1109, [0015]. *See also* Ex. 1109, [0025] (“The digital signal processors 150 is operable to assemble at least one of the first channels 102a, 102b ... into a composite signal 158....”). Consistent with the above-cited discussion in Petrovic ’886 of selecting fewer than all of the channels, Petrovic ’886 further explains that the number of extractor/converter circuits can be fewer than the total number of channels in the received RF signals, thus indicating that some undesired channels are not selected. Ex. 1109, [0033] (“the channel extractor/converter circuits 300, 350 are operable to extract a desired channel and to locate or place it in the desired channel slot of the output signal 158. Exemplary, the number of parallel-connect channel extractor/converter circuits will be equal to the number of available channels (i.e., channel slots) in the output signal 158..., although in other embodiments a larger or smaller number of channel extractor/converter circuits may be employed within the signal processors 150 as well.”).

122. The DSSP 150 upconverts the baseband I, Q components of selected channels output by the stages 307 in corresponding stages 309, sums the upconverted I, Q components to create a combined signal 158 having digital I component 158a (**light blue**) and digital Q component 158b (**brown**), and outputs those summed components 158a and 158b. Ex. 1108, [0018]-[0024], [0043], [0053]-[0054], [0078]-[0096], [0098]-[0122], Figs. 4, 6, 9-15; Ex. 1109, [0005], [0007], [0015],

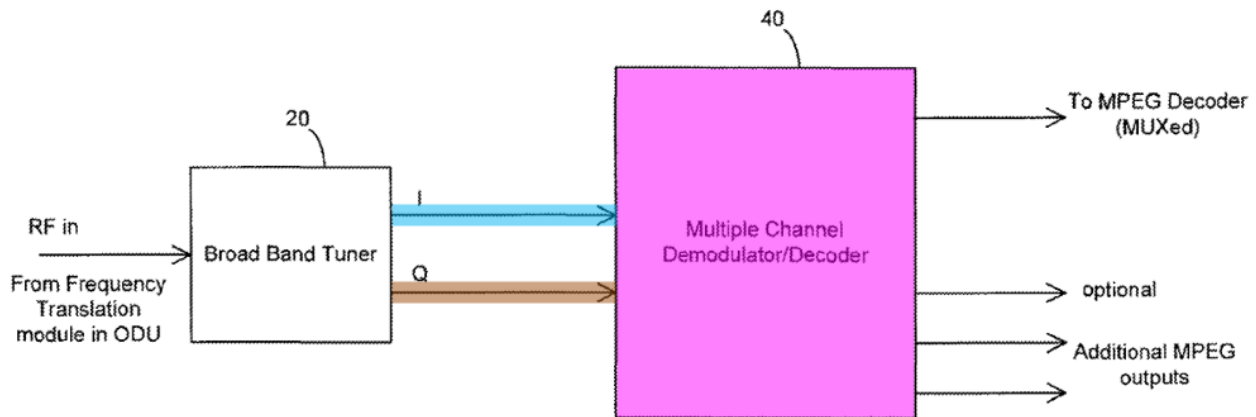
[0025], [0055]-[0069], [0071]-[0095], Figs. 1, 3A, 5-11. The components 158a, 158b are a digital datastream that contains the selected channels. Ex. 1108, [0009], [0043], [0046] (referring to “digital composite signal 158”), [0054], [0055] (circuits of the DSSP 150 “extract a desired channel and locate or place the channel in the desired channel slot of the output signal 158”), Figs. 4, 6; Ex. 1109, [0005], [0015], [0025], [0030], [0033], Figs. 1, 3A.

123. In sum, Petrovic discloses selecting, by the Petrovic DSSP 150 coupled to the ADC pair 108₁, desired channels from the digitized signal received from the ADC pair 108₁. Thus, it is my opinion that Petrovic discloses Element [1E].

f. [1F]: “outputting, by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator extracts information encoded in the digital datastream.”

124. It is my opinion that Petrovic-Eidson discloses limitation [1F]. As I explain below, a POSITA would have output the Petrovic components 158a and 158b to a demodulator as taught by Eidson.

125. Eidson Figure 8 discloses “a broadband tuner and multi-channel demodulator and decoder [pink]” that can be used as a multiple channel receiver of a set top box. Ex. 1112, 1:48-50, 2:8-10, 2:25-33, 2:42-51, 5:59-60, 7:58-59, 8:27-9:2.



Ex. 1112, Fig. 8 (annotated)

126. The multiple channel demodulator and decoder (“demodulator/decoder”) 40 receives digital I (**light blue**) and Q (**brown**) signals from a front end that comprises a broadband tuner 20 and a frequency translation module (FTM) of a satellite outdoor unit (ODU). Ex. 1112, 8:29-9:2, Fig. 8. The FTM portion of the front end selects multiple channels, translates those selected channels to contiguous portions of a bandwidth, and sends an RF signal with those translated channels to the tuner 20. Ex. 1112, 8:30-47, 9:5-25, Figs. 8-10. The tuner 20 (like the RFE and DFE of Petrovic) downconverts the received RF signal, generates I and Q components of that downconverted signal, and digitizes those I and Q components to create digital I, Q components. Ex. 1112, 8:43-47, 9:5-25, Figs. 8-10. Those digital I, Q components are output to the demodulator/decoder 40, which demodulates multiple channels in those components. Ex. 1112, 8:65-9:2, 11:44-12:28, Figs. 8, 15-16. Eidson clearly states that the output (I, Q) of the broadband tuner is digital, and shows in Figure 9 an example implementation of a

broadband tuner that has analog-to-digital (A/D) converters that provide digital I and Q signals to the demodulator/decoder. Ex. 1112, 7:61-62 (“FIG. 9 shows a broadband tuner”), 8:65-9:2, 9:5, Fig. 9. Thus, it is my opinion that Eidson teaches a demodulator to which a “selected plurality of desired channels” is being output “as a digital datastream.”

127. Eidson further teaches “wherein the demodulator extracts information encoded in the digital datastream.” For example, Eidson states that “[t]he digital output of the broadband tuner (or tuners) is processed by a multiple channel demodulator and decoder 40 to produce one or more MPEG streams comprising multiple video programs derived from the selected transponder channels.” Ex. 1112, 8:65-9:2. In any event, demodulation, which a POSITA would have understood a “demodulator” to perform, *is* extraction of information. Ex. 1115 at 7 (“The reconversion of a modulated signal back into its original form by extracting the data from the modulated carrier”). If the signal being demodulated is a digital datastream, as is the case in Eidson, then the demodulator is extracting information encoded in the digital datastream.

128. Eidson also shows a broadband demodulator 100 in Figure 15 as having A/D converters for received I and Q signals. Ex. 1112, 8:14-16, 11:44-49, Fig. 15. In my opinion, a POSITA would have understood from Eidson that the A/D converters could *either* be part of the broadband tuner or part of the demodulator.

There would be no reason to use A/D converters for *both* the output of the tuner and the input of the demodulator. Thus, the A/D converters of the demodulator would be optional. In other words, a POSITA would have understood Eidson as disclosing two possibilities, in which the broadband tuner could have A/D converters to provide the digital I and Q signals to the demodulator, or in which the demodulator could instead digitize the I and Q signals. Thus, a POSITA would have understood Eidson as disclosing either of these two options for A/D converter location. A POSITA would have also understood that there were two possibilities in Eidson to provide digital I and Q signals to the demodulator for processing – either the broadband tuner digitizes I and Q, or the demodulator digitizes I and Q. Thus, to the extent that it is argued that Eidson does not clearly disclose that the I and Q signals are digital when they are received by the demodulator, a POSITA would have considered it obvious to try either A/D converter location (as part of the broadband tuner or as part of the demodulator), since there are two possible locations for the A/D converters and both locations would result in successfully and predictably providing the demodulator with digital I and Q signals. Thus, the POSITA would be choosing from a finite (two) number of identified, predictable solutions (converting from analog to digital at the output of the broadband tuner, or converting from analog to digital at the input of the demodulator, so as to be compatible with the demodulator) with a reasonable expectation of success. Indeed, a POSITA would have considered the two solutions

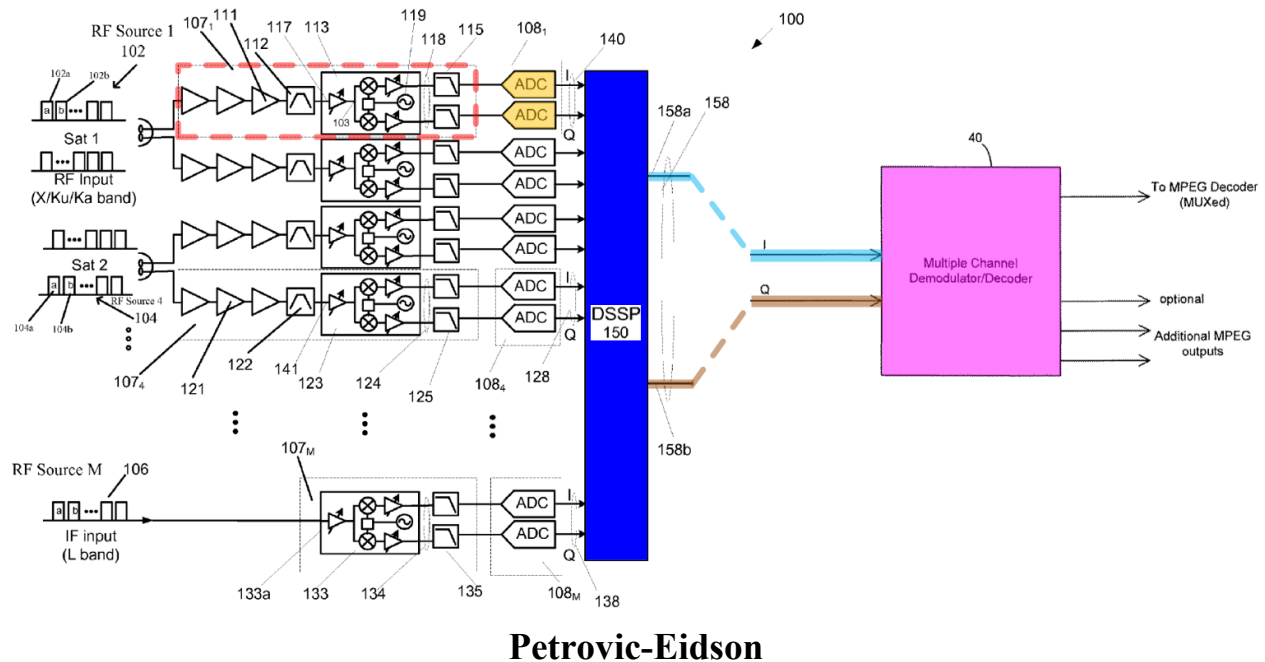
as equivalent and interchangeable, and providing the same result from the point of view of the ultimate demodulation function.

129. In my opinion, the I, Q components received by the Eidson demodulator/decoder 40 from the front end (e.g., the FTM and the tuner 20) are functionally equivalent to the Petrovic I, Q components 158a, 158b, as both sets of I, Q components comprise multiple channels that have been placed into sequential slots of a bandwidth. In particular, the I, Q components received by the Eidson demodulator/decoder 40 are I, Q components of a digital signal for multiple channels that have been selected and placed into contiguous portions of a bandwidth. Ex. 1112, 8:43-9:25, Figs. 8-10. Similarly, the Petrovic I, Q components 158a, 158b are digital components of a signal for multiple channels that have been selected and that have been placed into sequential portions of a bandwidth. Ex. 1108, Title, [0002], [0008], [0028], [0041]-[0044], [0046], [0053]-[0055], [0059]-[0091], [0097], Figs. 3-4, 6, 8; Ex. 1109, Title, [0001], [0004], [0008], [0015], [0025], [0030], [0033]-[0064], [0070], Figs. 1, 3A, 4. Figure 10 of Eidson, for example, shows the spectral content of the I and Q signals in the Eidson broadband tuner and shows how channels have been placed into contiguous portions of bandwidth by a frequency translation module before the broadband tuner. Ex. 1112, 8:30-48, 9:21-22, Figs. 8-10. Similarly, the Petrovic I, Q signals 158a, 158b are digital signals for multiple channels that have been selected and has been placed into sequential portions of a

bandwidth. Ex. 1108, Title, [0002], [0008], [0028], [0041]-[0044], [0046], [0053]-[0055], [0059]-[0091], [0097], Figs. 3-4, 6, 8; Ex. 1109, Title, [0001], [0004], [0008], [0015], [0025], [0030], [0033]-[0064], [0070], Figs. 1, 3A, 4. In particular, Petrovic is directed to a “channel *stacking* system and method,” the purpose of which is to “assembl[e] a desired *sequence of channels* to form a composite signal.” Ex. 1108, Title, [0002]; Ex. 1109, Title, [0001] (*italics added*).

130. In my opinion, a POSITA would have appreciated that the I and Q components output from Petrovic’s DSSP would be readily sent to a demodulator for a STB, such as taught in Eidson. This would have been done in place of Petrovic’s stage 109, or in addition to it. Eidson teaches that its demodulator/decoder 40 operates by receiving I, Q components that are functionally equivalent to the I, Q components 158a, 158b output by the Petrovic DSSP 150. It is further my opinion that a POSITA would have been motivated to combine a Petrovic tuner and the Eidson demodulator/decoder 40 so that the multiple selected channels output by the Petrovic DSSP (as I, Q components 158a, 158b) would be demodulated in the digital domain. Eidson further offers the benefit of digital demodulation with a single demodulator, which would have been more efficient than using multiple simultaneous demodulators for separate channels. Ex. 1112, 4:2-6, 6:36-38. Below is an annotated figure, prepared using excerpts from Petrovic Figure 4 and Eidson

Figure 8, showing the Petrovic-Eidson system in which the Petrovic I, Q components 158a, 158b are the I, Q component inputs to the Eidson demodulator/decoder 40.



131. Combining a Petrovic tuner with an Eidson demodulator/decoder 40 would also allow incorporation of tuning/channel selection and demodulating/decoding functionality into a single device, a configuration known in the art and having the added benefits of digital tuning afforded by Petrovic and multichannel demodulation afforded by Eidson. Ex. 1108, [0007], [0094]; Ex. 1109, [0003], [0069]; Ex. 1112, 3:35-45, 4:2-6, 6:36-38. For instance, Petruzzelli describes a satellite STB that is able to receive multiple satellite signals, tune to channels of the received satellite signals, and demodulate those channels. Ex. 1140, [0019]-[0021], Fig. 2. In particular Petruzzelli discloses that a satellite STB 200 (also

referred to as a television converter 200) “may include one or more tuner devices 206, 246 that may receive a satellite signal 204 ... from satellite television distributor 1,” and that the STB 200 can select a channel from the satellite signal 204. Ex. 1140, [0020], [0023], Fig. 2. Petruzzelli further discloses that the satellite STB 200 performs demodulation on the satellite signal 204, using a demodulator 208. Ex. 1140, [0021], Fig. 2.

132. For example, the Eidson demodulator/decoder 40 would have been added to the Petrovic tuner in a set top box intended to function as a “Media Center STB,” that would feed other set top boxes. Ex. 1112, 2:28-31. In such a set top box, the I, Q components 158a, 158b would have been simultaneously output to the demodulator/decoder 40 (e.g., for demodulation/decoding for output to display or recording devices) and to the Petrovic DAC and Complex to Real Conversion stage 109 for generation of a signal 188 to transmit to other set top boxes or devices. Alternatively, the stage 109 would have been omitted to save cost if “media center STB” functionality was not needed, thereby allowing a further simplified design. Although Petrovic indicates that its channel stacking system “may be implemented as an outdoor unit (ODU) as part of a satellite receiving system,” Petrovic does not limit its channel stacking system or its tuner (e.g., the Petrovic APD stage(s), the Petrovic ADC pair(s), and the Petrovic DSSP) to ODU use. Ex. 1108, [0054]; Ex. 1109, [0030]. A POSITA would have been aware of other uses, as tuners were

ubiquitous at the time, and in any event, Eidson teaches additional uses for the Petrovic tuner, and indeed, for the entire Petrovic channel stacking system.

133. Moreover, in my opinion, combining a Petrovic tuner and the Eidson demodulator/decoder would have been a combination of known prior art elements (Petrovic's APD, ADCs, and DSSP and Eidson's demodulator/decoder) according to known methods (sending I and Q components to the demodulator/decoder, as taught in Eidson) to yield predictable results (the components are demodulated and decoded). As explained above, and as a POSITA would have recognized, the output of a Petrovic tuner is the functional equivalent of the input to the Eidson demodulator/decoder. Thus, a POSITA could have, and would have, easily combined a Petrovic tuner and the Eidson demodulator/decoder, as each would perform the same function in the combination that would be performed individually prior to the combination. For the same reasons, it is my opinion that the results of combining the Petrovic tuner with the Eidson demodulator/decoder would also have been predictable. Neither the function of the Petrovic tuner, nor the function of the Eidson demodulator/decoder, would change appreciably if combined, and thus each element could operate as it did before, leading to an expectation of success.

134. Although my above analysis explains why a POSITA would have added the Eidson demodulator/decoder to the Petrovic tuner, a POSITA would have been just as motivated to add the Petrovic tuner to the Eidson demodulator/decoder.

This is because the I, Q signals output by the Petrovic DSSP are functionally equivalent to the I, Q signals received by the Eidson demodulator/decoder 40, and because the selection and stacking functions performed by the Petrovic tuner and by the Eidson front end are equivalent. Such equivalency would have taught a POSITA that the Petrovic tuner could be readily substituted for the Eidson front end. The advantages of, and motivation for, that combination would be the same as those described above for modification of Petrovic based on Eidson. Moreover, in my opinion and for similar reasons, such a combination would have been merely a combination of known prior art elements according to known methods to yield predictable results with an expectation of success.

135. In the Petrovic-Eidson system, the Petrovic DSSP 150 is the “digital frontend” of limitations [1E] and [1F]. The Petrovic DSSP 150 in Petrovic-Eidson selects the plurality of desired channels from the digitized signal (i.e., selects channels from the signal received by the DSSP) and outputs the selected plurality of channels as a digital datastream (the components 158a, 158b) to a demodulator (the Eidson demodulator/decoder 40) that extracts information encoded in the digital datastream. Thus, it is my opinion that Petrovic-Eidson discloses Element [1F].

9.1.2. Independent Claim 11

136. The limitations of claim 11 appear below and in the Claims Listing Appendix, labeled as limitations [11A]-[11F]. Claim 11 is a device claim directed to

substantially identical subject matter as method 1, in which limitations [11A]-[11F] recast the method steps of limitations[1A]-[1D] as identical structural elements having functionality corresponding to those method steps, and thus are rendered obvious by Petrovic in view of Eidson for the same reasons discussed above with respect to claim 1. See my explanation above at Sections 9.1.1.a through 9.1.1.f. *See also, e.g.*, Ex. 1108, Title (“Channel Stacking System and Method of Operation”) (underscore added), [0008]-[0009]; Ex. 1109, Title, [0004]-[0005]. It is my opinion that Claim 11 recites a television receiver device with the same components and functions thereof that were recited in method claim 1.

a. [11A]: A television receiver device, comprising:”

137. In my opinion, Petrovic-Eidson discloses “[a] television receiver device” as claimed.

138. Preamble [11A] is directed to substantially identical subject matter as preamble [1A] and thus is taught by Petrovic-Eidson for the same reasons I discuss above with respect to preamble [1A]. See my explanation at Section 9.1.1.a. The APD stage 107₁, ADC pair 108₁, and DSSP 150 of Petrovic’s system 100 are the claimed “television receiver device.”

- b. [11B] “an input terminal operable to receive an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels, wherein the plurality of desired channels are non-contiguous;”**

139. In my opinion, Petrovic-Eidson discloses “an input terminal operable to receive an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels, wherein the plurality of desired channels are non-contiguous,” as claimed.

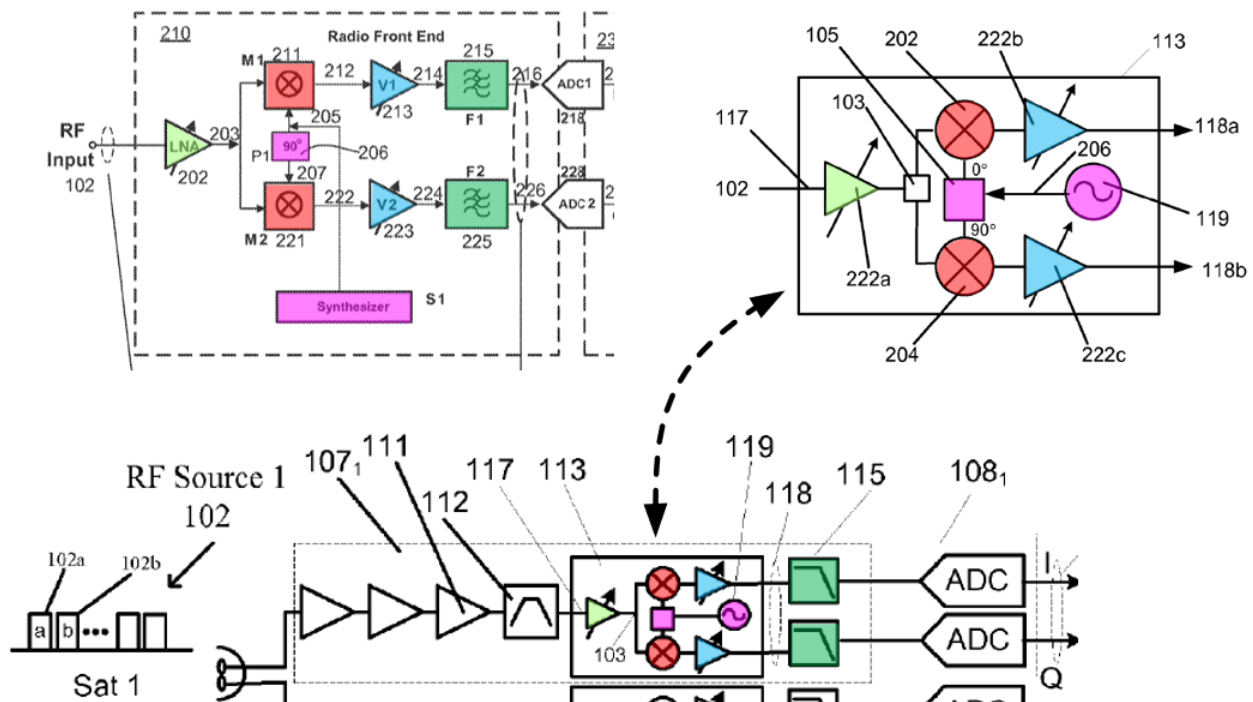
140. Limitation [11B] is directed to substantially identical subject matter as limitation [1B] and thus is taught by Petrovic-Eidson for the same reasons I discuss above with respect to limitation [1B]. See my explanation at Section 9.1.1.b. Petrovic’s input terminal is shown in Petrovic Figure 4, as explained in Section 9.1.1.b.

- c. [11C] “a radio front end, coupled to the input terminal, operable to process the input signal;”**

141. In my opinion, Petrovic-Eidson discloses “a radio front end, coupled to the input terminal, operable to process the input signal,” as claimed.

142. Limitation [11C] is directed to substantially identical subject matter as limitation [1C] and thus is taught by Petrovic-Eidson for the same reasons I discuss above with respect to limitation [1C]. See my explanation at Section 9.1.1.c. Petrovic’s APD stage 107₁ is the radio front end of limitation [11C], as explained in Section 9.1.1.c.

143. To the extent that the “radio front end” of limitation [11C] is construed to be a means-plus-function term, and as seen by the below comparisons of Figures 4 and 5 of Petrovic and Figure 2 of the '275 patent, the Petrovic APD stage 107₁ includes structure that is the same as, or equivalent to, structure of the radio front end 210 of the '275 patent. *See* Section 6. The below composite Figure compares the structure of the radio front end, from '275 patent Figure 2 (left), to the structure of the Petrovic APD stage 107₁ (bottom and right).



Ex. 1102, Fig. 2 (excerpted and annotated) (top left)

Ex. 1108, Fig. 5 (excerpted and annotated) (top right)

Ex. 1108, Fig. 4 (excerpted and annotated) (bottom)

144. The amplifier 222a (light green), mixer pair 202, 204 (red), frequency source 119 (pink), phase shifter 105 (pink), amplifiers 222b, 222c (light blue), and

low pass filters 115 (**green**) of the Petrovic APD stage 107₁ are structure that is the same as, or equivalent to, the amplifier 202 (**light green**), mixers 211, 221 (**red**), synthesizer S1 (**pink**), phase shifter 206 (**pink**), amplifiers 213, 223 (**light blue**), and low pass filters 215, 225 (**green**) of the '275 patent radio front end 210. Any differences between the '275 patent structure (radio front end 210) and the Petrovic APD stage 107₁ are insubstantial. Both perform the same function of processing an input signal by creating amplified, downconverted, and filtered I, Q components of a received RF signal. Ex. 1101, 4:40-5:37, Fig. 2; 1108, [0032]-[0039], Figs. 4-5; Ex. 1109, [0010], [0017], [0031], Figs. 1-2. To the extent that Patent Owner contends that the amplifier 111 and filter 112 of the Petrovic APD stage 107₁ affect the equivalence of the Petrovic APD stage 107₁ and '275 patent radio front end 210, the amplifier 111 and filter 112 are optional. Ex. 1108, [0001]; Ex. 1109, [0017].

d. [11D] “an analog-to-digital converter (ADC), coupled to the radio front end, operable to digitize the processed input signal to generate a digitized signal; and”

145. In my opinion, Petrovic-Eidson discloses “an analog-to-digital converter (ADC), coupled to the radio front end, operable to digitize the processed input signal to generate a digitized signal,” as claimed.

146. Limitation [11D] is directed to substantially identical subject matter as limitation [1D] and thus is taught by Petrovic-Eidson for the same reasons I discuss above with respect to limitation [1D]. See my explanation at Section 9.1.1.d.

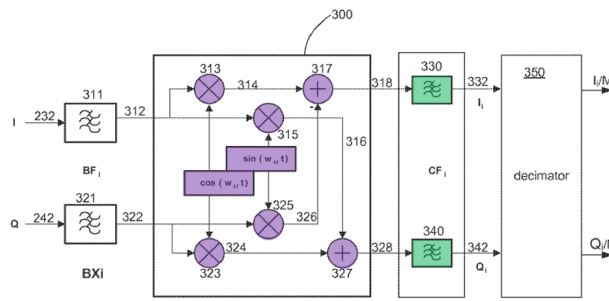
Petrovic's ADC pair 108₁ is the ADC of limitation [11D], as explained in Section 9.1.1.d.

- e. [11E] **“a digital frontend (DFE), coupled to the ADC, operable to select the plurality of desired channels from the digitized signal and”**

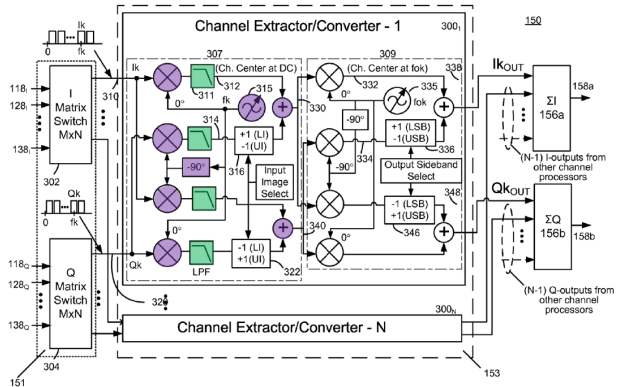
147. In my opinion, Petrovic-Eidson discloses “a digital frontend (DFE), coupled to the ADC, operable to select the plurality of desired channels from the digitized signal,” as claimed.

148. Limitation [11E] is directed to substantially identical subject matter as limitation [1E] and thus is taught by Petrovic-Eidson for the same reasons I discuss above with respect to limitation [1E]. See my explanation at Section 9.1.1.e. Petrovic's DSSP 150 is the DFE of limitations [11E] and [11F], as explained in Sections 9.1.1.e and 9.1.1.f.

149. To the extent that the “digital frontend” of limitations [11E] and [11F] is construed to be a means-plus-function term, and as seen by the below comparisons of Figure 3 of the '275 patent and Figure 6 of Petrovic, the Petrovic DSSP 150 includes structure that is the same as, or equivalent to, structure of the mixer 300 and filters 330 and 340 of the '275 patent. *See* Section 6.



Ex. 1101, Fig. 3 (annotated)

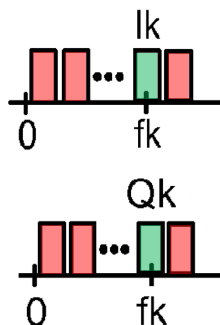


Ex. 1108, Fig. 6 (annotated)

150. Like complex mixer 300 of the '275 patent (**purple**), which is one of N complex mixers 250, the DSSP of Petrovic comprises N stages 307, each of which comprises a complex mixer (**purple**). Ex. 1101, 6:33-7:2; Ex. 1108, [0066]-[0068], Fig. 6; Ex. 1109, [0045]-[0047], Fig. 3A; *see* Section 9.1.1.e; Ex. 1118 at 134, Figs. 2-3; Ex. 1134 at 46-47, Fig. 3.3. Like the filters 330 and 340 of the '275 patent (**green**), which are one of N filter modules 260, each stage 307 of the Petrovic DSSP also comprises low pass filters (LPF) 311 (**green**). Ex. 1101, 7:3-8; Ex. 1108, [0066]-[0069]; Ex. 1109 [0045]-[0048].

151. Referring to Petrovic Figure 6 as annotated above, the DSSP 150 includes multiple sets of low pass filters 311 (four in each stage 307 of each circuit 300) (**green**) that are configured to perform selection of desired television channels. Referring to an excerpted and annotated version of Petrovic Figure 6 below, stage 307 receives the in-phase and quadrature signal components of the downconverted

satellite signal, which contains a desired channel (I_k and Q_k in **green**) and undesired channels (**red**) as shown below. Ex. 1108, [0061]; Ex. 1109, [0040].



Ex. 1108, Fig. 6 (excerpted and annotated)

152. Stage 307 first utilizes a combination of mixers (represented with the symbol “ $\otimes$ ”) to multiply these signals by a LO signal 315 having a frequency f_k , which shifts the desired channel to zero and undesired channels to adjacent frequencies. Ex. 1108, [0066]-[0068]; Ex. 1109, [0045]-[0047]. Low pass filters 311 then select the desired channel by passing I_k and Q_k centered at zero to the output, while removing the undesired channels, which are outside of the filter channel bandwidth. Ex. 1108, [0066]-[0069]; Ex. 1109, [0045]-[0048]. This type of desired channel selection in Petrovic is the same as that described by the '275 patent. Ex. 1101, 7:3-8.

153. In my opinion, any differences between the '275 patent structure (N mixers 300 and N filters 330 and 340) and the Petrovic stages 307 are insubstantial. Both perform the same function of selecting and outputting desired channels, in the same way by downconverting the desired channel to baseband and low pass filtering

to isolate the desired channels, and outputting the result to a demodulator, to achieve the same result of selecting a plurality of desired channels from a digitized signal and outputting those channels to a demodulator. Ex. 1101, 6:8-7:8; Ex. 1108, [0060]-[0070]; Ex. 1109, [0037]-[0054].

- f. [11F] “output the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator is operable to extract information encoded in the digital datastream.”**

154. In my opinion, Petrovic-Eidson discloses “output the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator is operable to extract information encoded in the digital datastream,” as claimed.

155. Limitation [11F] is directed to substantially identical subject matter as limitation [1F] and thus is taught by Petrovic-Eidson for the same reasons I discuss above with respect to limitation [1F]. See my explanation at Section 9.1.1.f. Petrovic’s DSSP 150 is the DFE of limitations [11E] and [11F], as explained in Sections 9.1.1.e, 9.1.1.f, and 9.1.2.e. The Eidson demodulator/decoder 40 is the demodulator of limitation [11F], as explained in Section 9.1.1.f.

9.1.3. Dependent Claims 4 and 14

- [4] “The method of claim 1, wherein the ADC comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.”**

[14] “The television receiver device of claim 11, wherein the ADC comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.”

156. In my opinion, Petrovic-Eidson discloses claims 4 and 14. Claim 4 is a method claim and claim 14 is a device claim directed to substantially identical subject matter as claim 4. As explained in section 9.1.1.d, the claimed ADC is the Petrovic ADC pair 108₁. As shown in the portion of Petrovic Figure 4 included in Section 9.1.1.d, Petrovic’s ADC pair 108₁ comprises first and second ADCs that respectively generate digital in-phase (I) and quadrature signals (Q). Ex. 1108, [0052], Fig. 4; Ex. 1109, [0022], Fig. 1.

9.1.4. Dependent Claims 7-8 and 17-18

[7] “The method of claim 1, wherein the plurality of desired channels comprises at least one television channel.”

[8] “The method of claim 1, wherein the plurality of undesired channels comprises at least one television channel.”

[17] “The television receiver device of claim 11, wherein the plurality of desired channels comprises at least one television channel.”

[18] “The television receiver device of claim 11, wherein the plurality of undesired channels comprises at least one television channel.”

157. In opinion, Petrovic-Eidson discloses claims 7-8 and 17-18. Claims 7-8 are method claims and claims 17-18 are device claims directed to substantially identical subject matter as claims 7-8. As explained in connection with preamble

[1A], a POSITA would have understood the channels of signals 102 in Petrovic to include television channels. Section 9.1.1.a.

9.1.5. Dependent Claims 9 and 19

[9] “The method of claim 1, wherein the broadcast channels comprise satellite broadcast channels.”

[19] “The television receiver device of claim 11, wherein the broadcast channels comprise satellite broadcast channels.”

158. In my opinion, Petrovic-Eidson discloses claims 9 and 19. Claim 9 is a method claim and claim 19 is a device claim directed to substantially identical subject matter as claim 9. As explained in Sections 9.1.1.a and 9.1.1.b, Petrovic’s system 100 receives satellite signals 102 that have multiple channels, Petrovic describes use of system 100 to output to a “rendering device” (thereby indicating output of television programming), and it was well known to broadcast television programming channels to end users via satellite communications.

9.2. Petrovic in View of Eidson and Rabaey Renders Claims 2-3 and 12-13 Obvious

159. In the following, I show how Petrovic in view of Eidson and Rabaey renders claims 2-3 and 12-13 obvious.

9.2.1. Dependent Claims 2-3 and 12-13

[2] “The method of claim 1, wherein the DFE outputs the digital datastream via a serial interface.”

[3] “The method of claim 1, wherein the DFE outputs the digital datastream via a parallel interface.”

[12] “The television receiver device of claim 11, wherein the DFE is operable to output the digital datastream via a serial interface.”

[13] “The television receiver device of claim 11, wherein the DFE is operable to output the digital datastream via a parallel interface.”

160. In my opinion, Petrovic-Eidson-Rabaey discloses claims 2-3 and 12-13. Claims 2 and 3 are similar, and only differ with regard to a type of interface via which the DFE outputs of the digital datastream of limitation [1F]. Ex. 1101, 12:42-45. Claim 2 recites output “via a serial interface,” while claim 3 recites output “via a parallel interface.” *Id.* Claims 12 and 13 are device claims, directed to substantially identical subject matter as claims 2 and 3, that merely recast claims 2 and 3 as required functionality of the DFE. *Id.*, 13:14-19. But as explained below, either option (i.e., output via a serial or parallel interface) would have been an obvious design choice, and thus it is my opinion that claims 2-3 and 12-13 are obvious over Petrovic-Eidson-Rabaey.

161. As I explain in Section 8.5, 9.1.1.e, and 9.1.1.f, Petrovic discloses a DSSP 150 as a DFE that selects desired television channels and outputs the selected channels as a digital datastream. As the '275 patent concedes, the outputting of a digital data steam via serial (claims 2/12) and parallel (claims 3/13) interfaces were

“commonly known methods.” Ex. 1101, 7:16-20. Indeed, as confirmed by dictionaries, basic text books and technical papers on digital integrated circuit design at the time, a POSITA would have understood parallel and serial interfaces as the two common options for outputting data in standard integrated circuits. For example, Pandey explains that the Universal Serial Bus was well known. Ex 1114, 9:44-50. And Rabaey (which I discuss in more detail below) explains that data can be transmitted in a time-multiplexed manner using a serial data transmission architecture or using dedicated transmission resources with a parallel data transmission architecture. Ex. 1116 at 79-80. According to Rabaey, if the data being transmitted were random, then it would make no difference which architecture is used, and if the data has distinct temporal correlation, then it may be more power-efficient to use a parallel architecture. *Id.* On the other hand, a parallel architecture requires more physical electrical transmission conductors than a serial architecture. Compare, for example, the parallel data transmission architecture of Rabaey Figure 6-25(a) having two transmission conductors (one for signal A and another for signal B) as opposed to the serial data transmission architecture of Rabaey Figure 6-25(b) having only a single transmission conductor shared by signals A and B. *Id.*

162. Notably, Petrovic discloses the DSSP 150 and other components of the system 100 may be implemented as “hardware.” Ex. 1108, [0124]-[0125]; Ex. 1109, [0115]. Petrovic also explains that “various actions described herein can be

performed by specific circuits (e.g., discrete circuitry or application specific integrated circuits (ASICs))” and that the DSSP 150 can be an ASIC. Ex. 1108, [0027], [0040]; Ex. 1109, [0009]. A POSITA would have understood Petrovic’s use of the term “hardware” to include “circuits” such as ASICs. Thus, a POSITA would have understood Petrovic as disclosing that various components of the system 100, including the DSSP, may be implemented as hardware such as an ASIC. As I explain in Section 9.1.1.f for limitation [1F], a POSITA would have modified Petrovic so that a Petrovic tuner—which includes a DSSP outputting the digital data stream—would output digital data to the Eidson demodulator/decoder. Eidson indicates that a front end and a multichannel demodulator/decoder could be integrated into a single package, which further indicates digital data would flow from a Petrovic DSSP to an Eidson demodulator/decoder using conventional integrated circuit interfaces. Ex. 1112, 6:33-35.

163. At the most fundamental level, a digital integrated circuit represents data as binary units (referred to as “bits”) in the form of electrical signals on wires (e.g., high and low voltages for binary values “1” and “0” respectively). Ex. 1116 at 23-24, 27-29, 48-51. To output multiple bits (i.e., as a “digital datastream”), the circuit can either transmit the bits over multiple separate wires, one wire for each bit, which was known as a “parallel interface,” or the circuit can transmit the set of bits one at a time as sequential pulses over a single wire, according to a fixed

sequence, which was known as a “serial interface.” See my discussion above, in Section 8.4, about serial versus parallel data communication. *See also*, Ex. 1115 at 5, 8, 10; Ex. 1116 at 79-80 (Figure 6-25, annotated below).

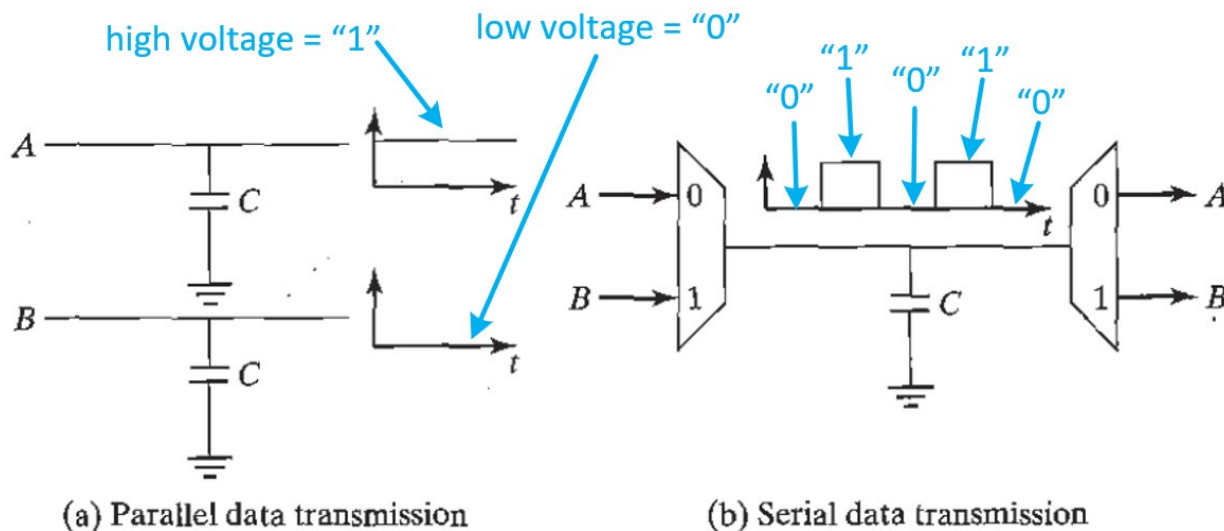


Figure 6-25 Parallel versus time-multiplexed data busses.

Ex. 1116 at 80, Fig. 6-25 (annotated)

164. In my opinion, implementing a data interface between a Petrovic DSSP and an Eidson demodulator/decoder using either option would have been equally obvious as one of two design choices, because both were “commonly known methods” used by POSITAs. Ex. 1114, 30:31-42, 31:15-22; Ex. 1115 at 5, 8, 10 (defining serial and parallel transmission); Ex. 1116 at 79-80; Ex. 1117 at 354-355. *Also see* Section 8.4 above for my discussion of serial data communication and parallel data communication. For the same reasons, implementing serial and parallel interfaces would have been well within the POSITA’s skillset, and thus, a POSITA would have had a high expectation of success leading to a predictable result.

165. Indeed, Rabaey and various background references teach and confirm why a POSITA would have applied parallel and serial interfaces to Petrovic's digital design. For example, Rabaey, a textbook on implementing digital integrated circuits, teaches that both serial and parallel interfaces as illustrated in the Figure 6-25 above were beneficially used in integrated circuits. Ex. 1116 at 79-80. According to Rabaey, time-multiplexing (i.e., a serial interface) "is an often used technique to minimize the implementation area" of a design on a chip, but that this "minimum area solution does not always result in the lowest switching activity," for example, when the data signals have high "temporal correlation." Ex. 1116 at 79-80; *see also Id.* at 72-74. Minimizing circuit area minimizes the cost of the integrated circuit, while minimizing the switching activity minimizes the "dynamic power consumption" of the integrated circuit. Ex. 1116 at 29-33, 43-44, 72-74, 76-80. In fact, the area taken up by a circuit on an integrated circuit can have a major impact on the cost of that integrated circuit. Where a circuit is implemented on a die of an integrated circuit wafer, "die costs are proportional to the fourth power of the area" of the die. Ex. 1116 at 31. Thus, Rabaey teaches both serial and parallel interfaces for transmitting digital data between two points, each of which has advantages over the other, depending upon area and power constraints and the temporal correlation between the signals. Ex. 1116 at 29-33, 43-44, 72-74, 76-80.

166. In my opinion, it would have been obvious to apply either of Rabaey's parallel data or serial interfaces as illustrated in Figure 6-25 to the interconnection between Petrovic's DSSP and Eidson's demodulator/decoder. Petrovic and Eidson teach implementation in an integrated circuit, and the techniques taught in Rabaey would have enabled such implementation. Ex. 1108, [0027], [0040], [0124]; Ex. 1109, [0009], [0115]; Ex. 1116 at 76-80. As such, the modification of Petrovic and Eidson with Rabaey that results in a serial interface (claims 2/12) between Petrovic's DSSP and Eidson's demodulator/decoder would have been nothing more than a combination of prior art elements, namely Petrovic's circuit design and Rabaey's serial interface interconnects, according to known methods (Rabaey's process for implementing circuit designs, including selecting a serial interface to minimize chip area and cost) to yield predictable results (data is sent serially). Likewise, the modification of Petrovic and Eidson with Rabaey that results in a parallel interface (claims 3/13) between Petrovic's DSSP and Eidson's demodulator/decoder would also have been nothing more than a combination of prior art elements (Petrovic's and Eidson's circuit designs and Rabaey's parallel interface interconnects) according to known methods (Rabaey's process for implementing circuit designs, including selecting a parallel interface to minimize switching and power) to yield predictable results (data is sent in parallel).

167. It is my opinion that the resultant combinations of Petrovic, Eidson, and Rabaey were predictable, and that a POSITA would have had a reasonable expectation of success, because Rabaey teaches basic techniques used by POSITAs to design integrated circuits, and because those techniques are specifically directed to overcoming specific issues, such as meeting area and power constraints as I discussed above, that a POSITA would customarily balance in their designs. Ex. 1116 at 29-33, 43-44, 72-74, 76-80.

9.3. Petrovic in view of Eidson and Takahiko Renders Claims 11, 14 and 17-19 Obvious

168. In the following, I provide a limitation-by-limitation analysis showing how Petrovic in view of Eidson and Takahiko also renders claims 11, 14, and 17-19 obvious. To help illustrate how the disclosures of these references map to the claim limitations, I have color coded some of my remarks and some figures in the noted art below.

9.3.1. Independent Claim 11

169. For the following reasons, it is my opinion that claim 11 is also rendered obvious over Petrovic in view of Eidson and Takahiko.

a. Limitations [11A]-[11D]

[11A] “A television receiver device, comprising:”

[11B] “an input terminal operable to receive an input signal comprising broadcast channels, the broadcast channels comprising

a plurality of desired channels and a plurality of undesired channels, wherein the plurality of desired channels are non-contiguous;”

[11C] “a radio front end, coupled to the input terminal, operable to process the input signal;”

[11D] “an analog-to-digital converter (ADC), coupled to the radio front end, operable to digitize the processed input signal to generate a digitized signal; and”

170. Petrovic-Eidson discloses limitations [11A]-[11D] for the reasons explained in Sections 9.1.1.a through 9.1.1.d and 9.1.2 through 9.1.2.d, above.

b. Limitations [11E] and [11F]

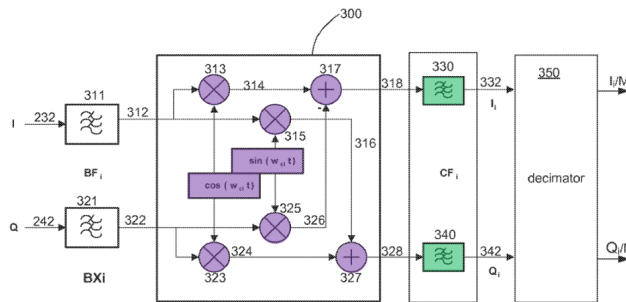
[11E] “a digital frontend (DFE), coupled to the ADC, operable to select the plurality of desired channels from the digitized signal and”

[11F] “output the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator is operable to extract information encoded in the digital datastream.”

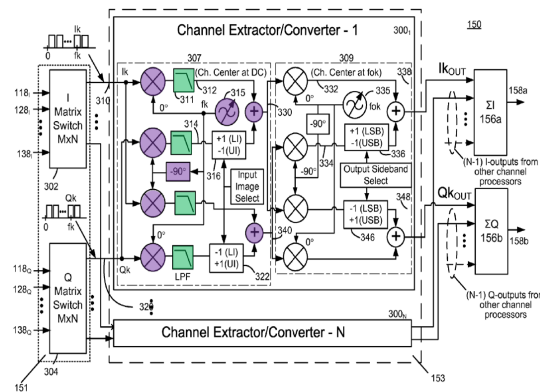
171. Petrovic-Eidson discloses limitations [11E]-[11F] for the reasons explained in Sections 9.1.1.e through 9.1.1.f, 9.1.2, and 9.1.2.e through 9.1.2.f, above. And as I explained in Section 9.1.2.e above, and as illustrated by the side-by-side comparison of Figure 3 of the '275 patent and Figure 6 of Petrovic in Section 9.1.2.e, any differences between the Petrovic first stage 307 and the mixer 300 and filters 330 and 340 of the '275 patent are insubstantial.

172. In my opinion, the location of LPFs 311 within the complex mixer, as shown in Figure 6 of Petrovic (annotated below), is the same or equivalent structure

as the complex mixer 300 and filters 330 and 340 of Figure 3 of the '275 patent (also annotated below). However, to the extent that DFE is treated as a means+function limitation, and to the extent it is argued that the location of LPFs 311 is not the same or equivalent structure as the complex mixer 300 and filters 330 and 340, it is my opinion that placing four low pass filters before adders (the “ $\oplus$ ” symbols in the below Figures) of a complex mixer (as shown in Petrovic Figure 6) or two low pass filters after adders of a complex mixer (as shown in '275 patent Figures 2-3) would have been functionally equivalent and merely a matter of design choice, as both options were well known to a POSITA.

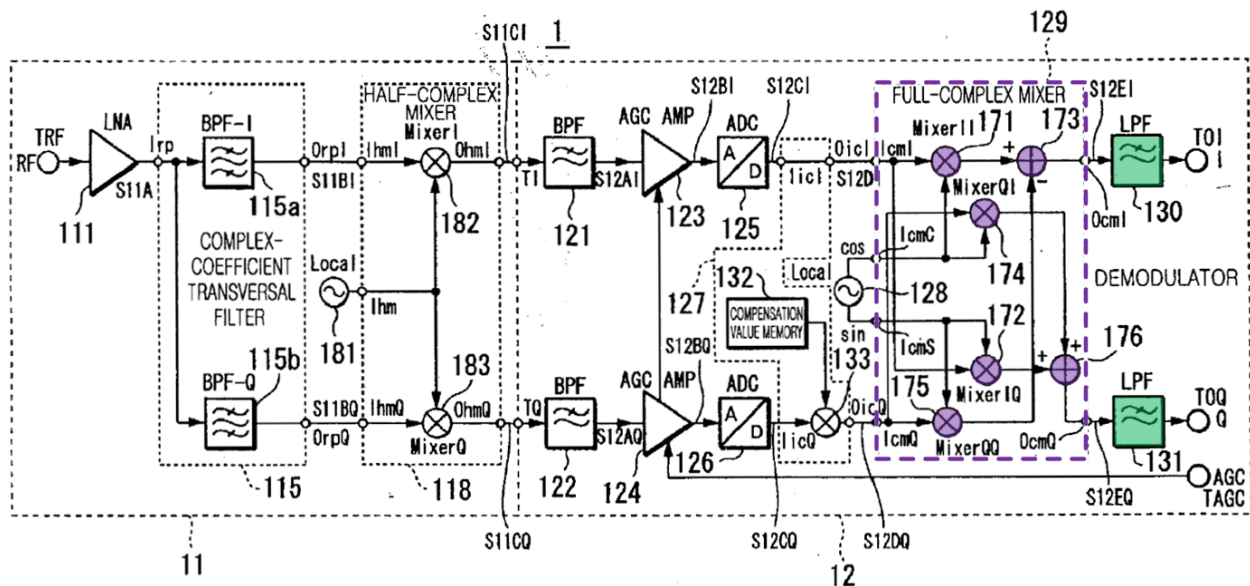


Ex. 1101, Fig. 3 (annotated)



Ex. 1108, Fig. 6 (annotated)

173. For example, Takahiko describes a “downconverter” 1 that is used in a radio receiver, and that is very similar to the receiver of '275 patent Figure 2. Ex. 1161, [0143], Fig. 1.



Ex. 1161, Fig. 1 (annotated)

174. Referring to the annotated figure above, Takahiko's downconverter 1 discloses a "full-complex mixer" 129 (purple, broken-line purple box) and low pass filters (green) 130 and 131 that are the same as what is shown in Figure 3 of the '275 patent. Moreover, in my opinion, Takahiko uses full-complex mixer 129 and filters 130 and 131 in the same way that the '275 patent describes use of complex mixer 300 and filters 330 and 340: downconversion of digital I, Q signals so a desired channel is at baseband and removal of unwanted higher frequencies with low-pass filtering. Ex. 1161, [0153], [0156].

175. In my opinion, a POSITA would have been motivated to modify the complex mixers of the Petrovic stages 307 to use two low pass filters after the adders of the complex mixer, similar to the configuration of the Takahiko full-complex mixer 129 and filters 130 and 131 located after adders 173 and 176, and instead of

four low pass filters within the complex mixer, to make the circuit simpler and less expensive. Such a modification would have merely involved use of known circuit components in known arrangements, because of the similarity between the relevant portions of the Petrovic first sections 307 and the Takahiko full-complex mixer 129 and filters 130 and 131, and because the Takahiko full-complex mixer 129 and filters 130 and 131 would have been functionally equivalent to a Petrovic first section 307. Thus, a POSITA would have had a reasonable expectation of success, and the results of the modification would have been predictable to a POSITA.

176. It is also my opinion that a POSITA would have combined the Petrovic channel stacking system, as modified in view of Takahiko, with the Eidson demodulator/decoder for the reasons explained in Section 9.1.1.f., as the modification would not have affected the input provided to a corresponding second stage 309 of the Petrovic DSSP, nor would it have affected the signals 158a, 158b generated by the DSSP. Accordingly, claims 11, 14, and 17-19 are also obvious over Petrovic-Eidson-Takahiko. To the extent that the DFE of claim 11 is treated as a means+function limitation, the Petrovic stages 307, as modified in view of Takahiko, is the same or similar structure as the mixer 300 and filters 330 and 340 of the '275 patent, and any differences would be insubstantial. Both perform the same function of selecting and outputting desired channels, in the same way by downconverting the desired channel to baseband and low pass filtering with a filter to isolate the

desired channels and outputting the result to a demodulator, to achieve the same result of selecting a plurality of desired channels from a digitized signal and outputting those channels to a demodulator. *See* Section 9.1.2.e.

9.3.2. Dependent Claims 14 and 17-19

[14] “The television receiver device of claim 11, wherein the ADC comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.”

[17] “The television receiver device of claim 11, wherein the plurality of desired channels comprises at least one television channel.”

[18] “The television receiver device of claim 11, wherein the plurality of undesired channels comprises at least one television channel.”

[19] “The television receiver device of claim 11, wherein the broadcast channels comprise satellite broadcast channels.”

177. In my opinion, claims 14 and 17-19 are taught by Petrovic-Eidson-Takahiko for the reasons explained in Sections 9.1.2 through 9.1.5, as the addition of Takahiko does not affect the disclosure by Petrovic-Eidson of those limitations. Accordingly, in addition to being obvious over Petrovic-Eidson as discussed in Sections 9.1.3 through 9.1.5, claims 14 and 17-19 are also obvious over Petrovic-Takahiko-Eidson.

9.4. Petrovic in view of Eidson, Takahiko and Rabaey Renders Claims 12 and 13 Obvious

[12] “The television receiver device of claim 11, wherein the DFE is operable to output the digital datastream via a serial interface.”

[13] “The television receiver device of claim 11, wherein the DFE is operable to output the digital datastream via a parallel interface.”

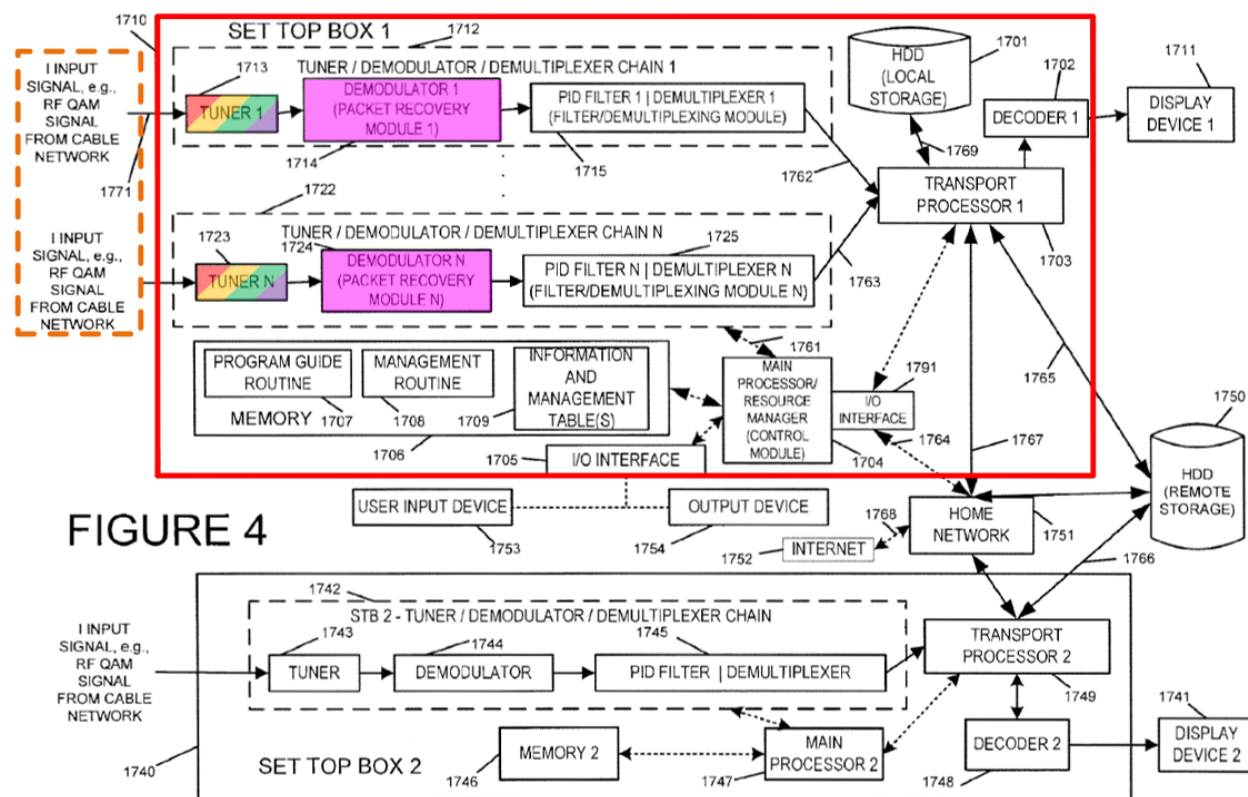
178. In addition to being obvious over Petrovic-Eidson-Rabaey, it is my opinion that claims 12-13 are also obvious over Petrovic-Eidson-Takahiko-Rabaey for the reasons explained in Sections 9.2 and 9.3, as modification in view of Takahiko does not affect modification in view of Rabaey.

9.5. Cholas in view of Petrovic and Maalej Renders Claims 1, 4-5, 7-8, 10-11, 14-15, 17-18 and 20 Obvious

179. In the following, I show how, in my opinion, Cholas in view of Petrovic and Maalej render claims 1, 4-5, 7-8, 10-11, 14-15, 17-18 and 20 obvious. To help illustrate how the disclosures of these references map to the claim limitations, I have color coded some of my remarks and some figures in the noted art below. Before explaining how Cholas-Petrovic-Maalej teaches these claims, I describe how and why a POSITA would, in my opinion, have modified Cholas in view of Petrovic and Maalej.

180. Cholas describes an STB 1710 (**red**) that receives a television signal “from the cable network,” and in particular, an input signal having RF QAM (quadrature amplitude modulation) channels carrying TV programs. Ex. 1158,

Abstract, [0001]-[0002], [0004], [0006], [0010]-[0017], [0022], [0024], [0033], [0044], [0052]-[0057], [0059]-[0071], Figs. 4-6.



Ex. 1158, Fig. 4 (annotated)

181. The STB 1710 receives an input signal (**orange**) having RF QAM (quadrature amplitude modulation) channels carrying TV programs. Ex. 1158, Abstract, [0001], [0002], [0004], [0006], [0011]-[0017], [0033], [0044], [0052]-[0057], Fig. 4. In Cholas, “[a] typical RF signal enters set top box 1 1710 at input 1771 with multiple carriers between, e.g., frequencies 50-1000 MHz.” Ex. 1158, [0045]. This is a bandwidth greater than the 800 MHz bandwidth that the ’275 patent gives as an example of a “wide bandwidth.” Ex. 1101, 2:39.

182. As shown in annotated Figure 4 of Cholas above, the STB 1710 has multiple parallel tuner/demodulator/demultiplexer chains, with chain 1712 being described in detail as “an example of the operation of the tuner/demodulator/demultiplexer chains.” Ex. 1158, [0045], Fig. 4. Each of the tuners (**red/gold/green/purple** striped) of each chain in the STB 1710 “selects a single 6 MHz carrier frequency and passes the signal corresponding to the band” to a demodulator (**pink**). Ex. 1158, [0045].

183. Any of the tuners in multiple chains of the STB 1710 can be available to tune to a particular channel. Ex. 1158, [0062]-[0064], Fig. 6. For example, if a first tuner is available, the first tuner is tuned to a determined channel, but if the first tuner is not available, then a second available tuner is tuned to that determined channel. *Id.* Moreover, it was known to a POSITA (and indeed, it was even common knowledge to a lay person) as of the earliest possible priority date of the '275 patent that typically a single cable TV cable containing all available channels is provided to a premises such as a home (rather than, for example, one cable for some channels and another cable for other channels). Cholas describes its tuners as being deployed in a home premises. Ex. 1158, [0012], [0016].

184. Because a channel is tuned by one of the tuners 1713-1723 in response to a user selection of a program carried on that channel, it is a “desired” channel. Ex. 1158, [0059]-[0063]. There are numerous 6 MHz channels between 50-1000 MHz.

In Cholas, and even if limited to channels between 550 and 862 MHz, the number of 6 MHz contiguous RF channels for the user to select would be relatively large, on the order of about $(862 \text{ MHz} - 550 \text{ MHz}) / 6 \text{ MHz}$, or 52 RF channels, containing at least one television channel. Ex. 1158, [0047], [0052], [0055]-[0057], Fig. 5. *See*, Ex. 1133 at 45, 413, 515-520 (each RF channel is allocated 6 MHz of bandwidth and occupies the RF spectrum in a contiguous manner). Moreover, and as a POSITA would have appreciated, very few (if any) users of a STB would ever have wanted or needed to simultaneously tune more than a handful of channels, much less 52 channels, so there would frequently have been multiple “undesired” channels. A POSITA would have recognized this and taken it into account when designing a STB, as it would have been a relevant consideration when determining how many tuners (such as the Cholas tuners 1713-1723) or tuning circuits (such as the Petrovic first stages 307, described below) to include in an STB. Including more tuners/tuning circuits than would reasonably have been expected to be needed would have increased cost and power consumption of the device and made it needlessly complicated. Therefore, in a conventional cable TV system with numerous 6 MHz channels between 50-1000 MHz, such as Cholas describes, in my opinion a POSITA would have understood from Cholas that there would always be channels that were not tuned by a particular STB, and that were thus “undesired.” Ex. 1158, [0045].

185. Petrovic discloses a channel stacking system 100 that performs tuning functions similar to those described by Cholas. Referring to annotated Figure 4 below of Petrovic, the system 100 receives signal 106 that may be between 950-2150 MHz. Ex. 1108, [0029], [0031], [0050], Fig. 4; Ex. 1109, [0012], [0020], [0028], Fig. 1. Signal 106 is wideband, as it comprises multiple channels. Ex. 1108, [0050], Fig. 4; Ex. 1109, [0028], Fig. 1. Moreover, the bandwidth of the signal 106 is greater than the 800 MHz bandwidth that the '275 patent gives as an example of a “wide bandwidth.” Ex. 1101, 2:39.

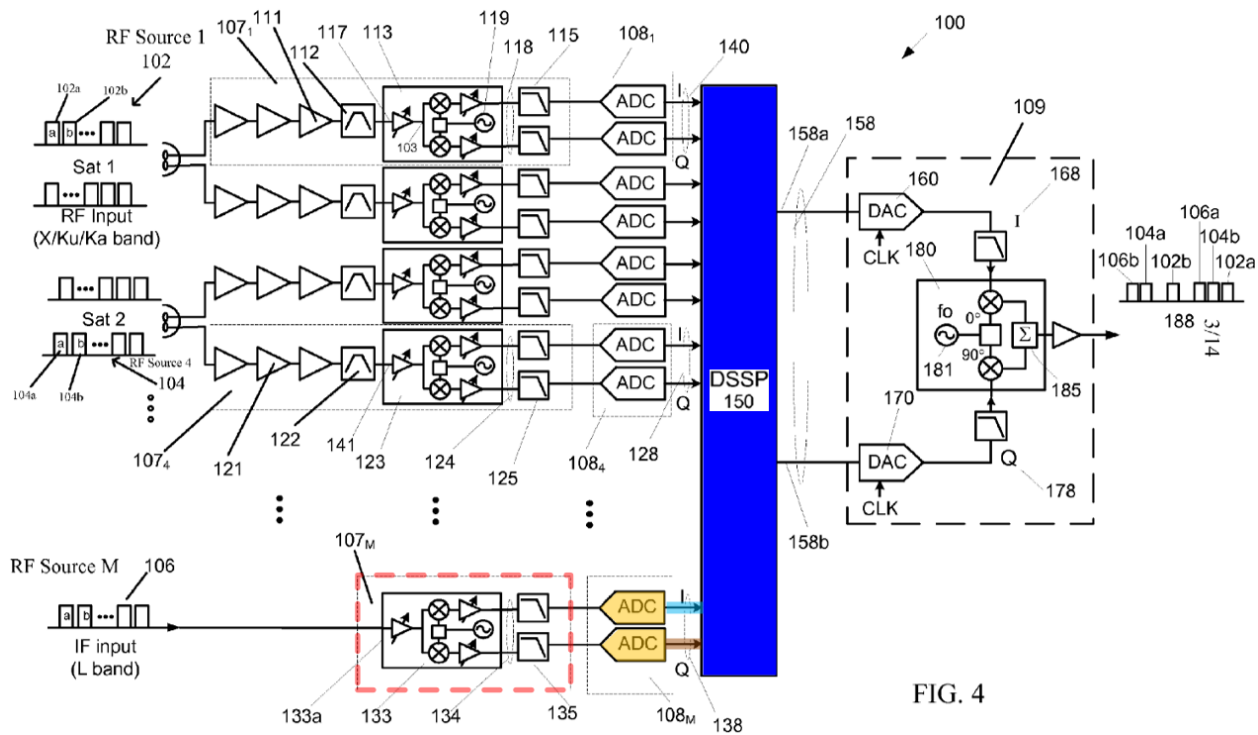


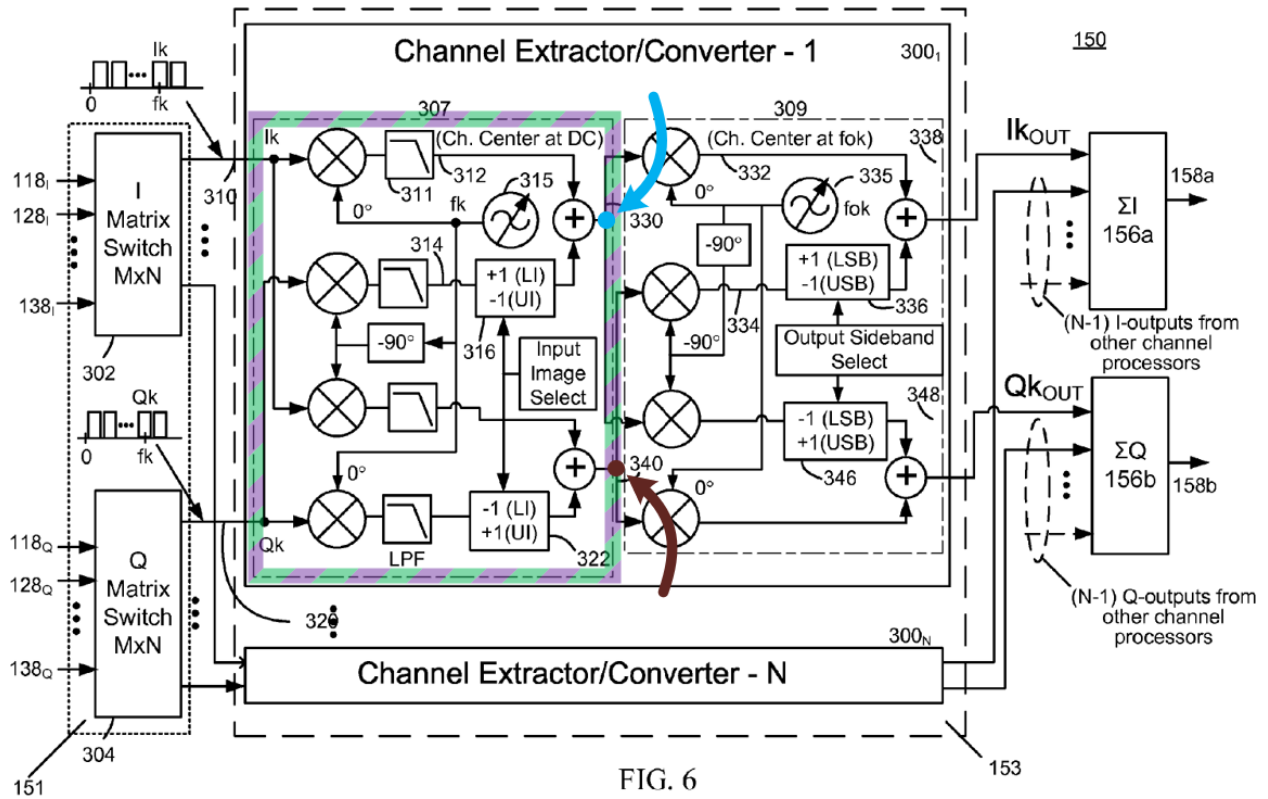
FIG. 4

Ex. 1108, Fig. 4 (annotated)

186. A downconverter in “analog preprocessing and downconversion (APD)” stage 107_M receives RF signal 106 and downconverts RF signal 106 into I, Q intermediate frequency (IF) components 134. Ex. 1108, [0032]-[0035], [0050],

Figs. 4-5; Ex. 1109, [0020], [0028], [0031], [0032], Figs. 1-2. The downconverted I, Q components 134 are filtered and then converted to digital form in analog-to-digital converters (ADCs) 108_M (**gold**). Ex. 1108, [0048], [0050], [0052], Fig. 4; Ex. 1109, [0020], [0022], [0028], Fig. 1. The entire band provided by the APD stage 107_M, which includes all received channels that exist in the signal 106, is digitized by the ADCs 108_M to generate digital I (**light blue**), Q (**brown**) components 138, and the ADCs 108_M are thus “wideband.” Ex. 1108, [0039], Fig. 4; Ex. 1109, [0029], Fig. 1.

187. A digital signal switching and pre-processing (DSSP) stage 150 (**blue**) receives the digitized components 138 and “extract[s] the channels of interest ... (i.e., remove[s] all of the channels that are not of interest).” Ex. 1108, [0040], [0042], Fig. 4; Ex. 1109, [0015], [0025], [0033], Fig. 1. Figure 6 shows additional details of the DSSP 150. Ex. 1108, [0058], Fig. 6; Ex. 1109, [0033], Fig. 3A.



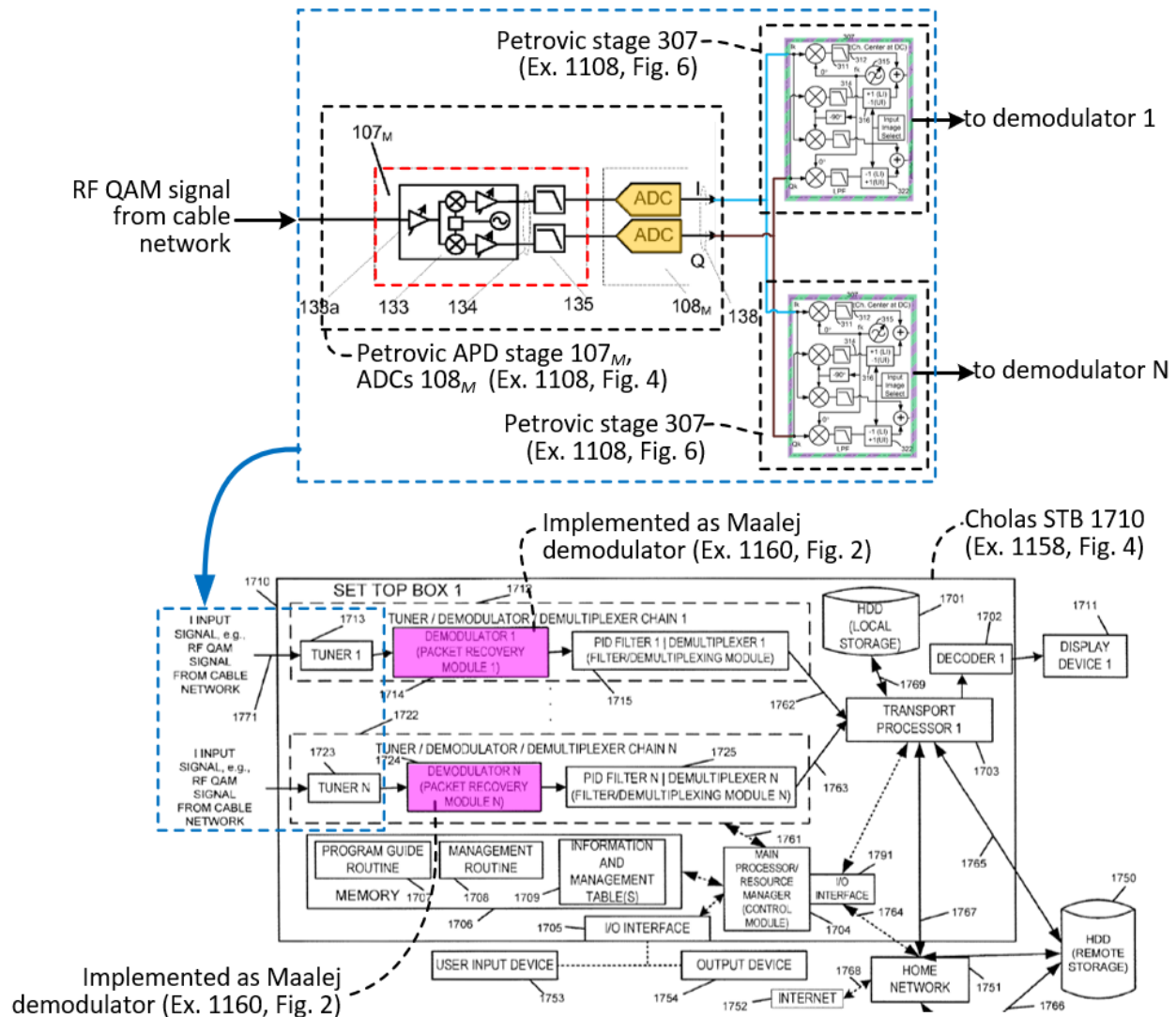
Ex. 1108, Fig. 6 (annotated)

188. Referring to the annotated figure above, the DSSP 150 includes multiple circuits 300, with each of those circuits 300 comprising a stage 307 (**purple/green**), and with each of those stages 307 able to select a different channel. Ex. 1108, [0055], [0059]-[0077], Fig. 6; Ex. 1109, [0033], [0037]-[0054], Fig. 3A. A stage 307 extracts a channel from the digitized I, Q components 138_I, 138_Q corresponding to the RF source 106 by downconverting those components so that a desired channel is at baseband, and filtering the components, in a complex mixer that comprises mixers (“⊗” symbols inside the **purple/green** box) and adders (“⊕” symbols inside the **purple/green** box). Ex. 1108, [0060]-[0077]; Ex. 1109, [0037]-[0054]. The frequency f_k used for the downconversion is selected based on a

frequency corresponding to a desired channel. Ex. 1108, [0066]; Ex. 1109, [0045]. The complex mixer of a stage 307 generates and outputs, from the adders, a digital quadrature pair comprising an I component 330 (**light blue** dot and arrow) and a Q component 340 (**brown** dot and arrow) corresponding to a selected/desired channel. Ex. 1108, [0005], [0007]-[0009], [0028], [0040], [0042], [0045], [0070]-[0077], Figs. 4, 6; Ex. 1109, [0004], [0008]-[0009], [0015], [0025], [0028]-[0029], [0049]-[0054], Figs. 1, 3A.

189. Maalej describes a demodulator that performs demodulation functions similar to those described by Cholas, and in particular, a QAM demodulator 99 that, for example, demodulates 6 MHz CATV channels. Ex. 1160, 1:6-8, 1:27-33, 3:47-52.

demodulator structures taught by Maalej. Below is an annotated Figure, prepared using excerpts from Cholas Figure 4 and Petrovic Figures 4 and 6, showing Cholas-Petrovic-Maalej.



Cholas-Petrovic-Maalej

192. In a system combining Cholas with Petrovic and Maalej, in my opinion a POSITA would have replaced the Cholas tuners 1-N (tuners 1713-1723) with a single Petrovic tuner that would have included the Petrovic APD stage 107_M, ADCs

108_M, and multiple stages 307 of the DSSP 150. Each of the stages 307 would, like one of the replaced Cholas tuners 1-N, output a signal (a digital I, Q pair 330, 340) corresponding to a selected “desired” channel. In the Cholas-Petrovic-Maalej system, the entire received band would be output by the Petrovic APD stage 107_M, including all received channels that exist in the input RF QAM signal (desired and undesired). All of these channels would be digitized by the ADCs 108_M, with the desired channels later being selected by stages 307 of Petrovic’s DSSP, as explained below with respect to limitation [1E]. Ex. 1108, [0039], Fig. 4; Ex. 1109, [0029], Fig. 1; Ex. 1158, [0045], [0052]-[0053], [0055]-[0056], Fig. 5. *See*, Section 9.5.1.e, below (discussing limitation [1E]).

193. In my opinion, a POSITA would have been motivated to implement the Cholas STB with a single Petrovic tuner (e.g., the Petrovic APD stage 107_M, ADCs 108_M, and multiple stages 307 of the DSSP 150) instead of multiple separate tuners 1713-1723. Implementing the Cholas STB with a single tuner would have beneficially simplified the STB and reduced the number of components. This, in turn, would have reduced the cost of manufacturing and power consumption of the STB. Although Cholas does not disclose the tuners 1713-1723 performing downconversion, in my opinion downconversion of a received RF signal prior to further processing was a standard technique used in receivers that was well-known to a POSITA. *See*, Section 8.3.1, above. Moreover, a POSITA would have known

that a single downconverter (as part of the APD stage 107_M) would use less power and be less expensive to implement than separate downconverters for each of multiple tuners.

194. In addition, using a single Petrovic tuner would have improved the Cholas STB with digital tuning. For example, selecting channels in the digital domain avoids the need for bandpass filtering and Hilbert transformers, thereby reducing circuit complexity and power consumption. Ex. 1108, [0007], [0096]; Ex. 1109, [0003], [0069]. And, implementing the STB as described in Cholas with a tuner as described in Petrovic, rather than using multiple separate tuners, would have been a simple substitution of one known element for another to obtain predictable results.

195. For numerous reasons, a POSITA would have been able to substitute a Petrovic tuner for the multiple tuners 1713-1723 of the Cholas STB, and the results would have been predictable. For example, and as I explained above, the output of each Petrovic first stage 307 is an I, Q pair that corresponds to a selected channel. Cholas shows that the output of each tuner is the input to a dedicated QAM demodulator. Ex. 1158, Fig. 4. Generating I, Q components was well-known to a POSITA to be a preliminary step in QAM demodulation. *See*, Section 8.2.3, above. In fact, and as I discuss above in connection with Maalej, it was well-known to a POSITA that QAM demodulators may digitize, and create I, Q components for, a

signal being demodulated. Ex. 1160, 4:5-19, Fig. 2. Therefore, in my opinion a POSITA would have readily recognized that outputs of Petrovic first stages 307 were usable as inputs to existing demodulators. As another example, Petrovic discloses downconverting, digitizing, and tuning channels in a 950-2150 MHz band. Ex. 1108, [0031], Fig. 4; Ex. 1109, [0012], Fig. 1. In my opinion, any bandwidth or frequency differences between that band and the 50-1000 MHz band disclosed by Cholas would not have created any technical challenges to implementing the Cholas STB with a Petrovic tuner. Ex. 1158, [0045].

196. In addition, it is my opinion that modifying a Cholas STB to include a Petrovic tuner instead of multiple separate tuners would have merely involved the use of a known technique to improve a similar device in the same way. For the same reasons explained above, a POSITA would have applied the improvement of the Petrovic tuner (digital tuning, reduced components, reduced power consumption) to the Cholas STB, and the results would have been entirely predictable to the POSITA.

197. Returning to Maalej, in my opinion, the I, Q components output by the Maalej DDS 30 are functionally equivalent to the Petrovic I, Q components 330, 340 in Cholas-Petrovic, as both sets of I, Q components comprise baseband digital I, Q components of a signal that is to be demodulated. Indeed, as mentioned above, Maalej teaches that demodulation of QAM signals (such as in Cholas) is performed after generating digital I, Q components—such as a digital I, Q pair 330, 340 from a

Petrovic stage 307—of a signal to be demodulated. Moreover, and similar to the Cholas demodulators, the Maalej demodulator outputs MPEG2 Transport System (TS) packets. Ex. 1160, 5:12-15; Ex. 1158, [0045]. It is my opinion that a POSITA would have applied Maalej's teachings to Cholas-Petrovic, such that each of the Cholas demodulators would be implemented to include components of the Maalej demodulators (for example, blocks 35, 210, 40, 45, 50, 230, 220, 55, 61, 65, and 70) that receive I, Q components 330, 340 from a Petrovic first section 307 and that output data 93, in the form of MPEG2 TS packets, to a respective Cholas packet identifier (PID) filter. Ex. 1160, 5:12-14.

198. In my opinion, such a modification would have merely been a combination of known prior art elements according to known methods to yield predictable results. The POSITA would have recognized the functional equivalence of a Petrovic first section 307 output and the output from the Maalej DDS 30, as well as the functional equivalence of the Maalej demodulator output and the inputs to the Cholas PID filters/demultiplexers 1715-1725. A POSITA would also have recognized that if I, Q signals of a QAM-modulated signal were to be demodulated so as to output, e.g., MPEG2 TS packets, the components of the Maalej demodulator could beneficially be used as a demodulator in the Cholas-Petrovic STB so that the signal could be demodulated. Thus, the POSITA would have easily combined a Petrovic first section 307 and components of the Maalej demodulator, knowing that

each would perform the same function in the combination that would have been performed individually prior to the combination to beneficially demodulate the I and Q components. For these same reasons, it is also my opinion that the results of combining a Petrovic first section 307 output with Maalej demodulator components would have been highly predictable to a POSITA.

9.5.1. Independent Claims 1, 11

a. Preambles [1A] and [11A]

[1A] “A method for operating a television receiver, comprising:”

[11A] “A television receiver device, comprising:”

199. In my opinion, Cholas-Petrovic-Maalej discloses non-limiting preambles [1A] and [11A], as the Cholas STB, as modified in view of Petrovic and Maalej, receives a television signal from “the cable network.” Ex. 1158, [0004] (“As the number of *television* and other program channels continues to increase, customers are faced with the increasing potential that programs of interest to the customer will be broadcast during the same time slots, on the same or different program channels. Given that set top boxes frequently only include one or two tuners, customers are frequently presented with more programs, movies or other content of interest being broadcast in a given time slot than there are tuners in the customer's STB.”) (*italics added*), [0010] (incorporating by reference U.S. Patent Application No. 11/681,774 (Ex. 1180) and stating that the Cholas methods and

apparatus “can be used alone and/or in combination with one or more of the methods and/or apparatus described in” application 11/681,774), [0011], [0022], [0024], [0044], [0059]-[0071], claim 13 (“wherein said communications device is a cable television set top box”), Figs. 4, 6; Ex. 1180, [0012]-[0014] (“content delivery streams include, for example, multiple television programs”), [0149], [0159], claim 37 (“wherein said receiver is coupled to a cable television input”). Moreover, a POSITA would have understood a cable network such as in Cholas to carry television channels. *Id. See also* Ex. 1181, [0003] (“Cable television (CATV) systems are used to deliver television services to a vast majority of TV-viewing homes in the U.S.”), [0004].

b. Limitations [1B] and [11B]

[1B] “receiving, by an input terminal, an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels, wherein the plurality of desired channels are non-contiguous;”

[11B] “an input terminal operable to receive an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels, wherein the plurality of desired channels are non-contiguous;”

200. In my opinion, Cholas-Petrovic-Maalej discloses limitations [1B] and [11B]. Because the Cholas-Petrovic-Maalej STB receives input from a cable network, a POSITA would have known that, in order to function, it would have included an “input terminal” so that it could connect to that cable network to receive

that input. Ex. 1158, [0044]. Indeed, U.S. Patent Application No. 11/681,774, which Cholas incorporates by reference, claims a STB in which a “receiver is coupled to a cable television input” and describes a STB having a “cable interface module” that couples the STB “to a service provider, e.g., a cable company.” Ex. 1158, [0010]; Ex. 1180, [0074], [0078], claim 37. But in any event, an “input terminal” for connection to a cable network was a well-known feature of STBs. Dua, for example, describes a STB having a transceiver/tuner that “allows a cable/satellite line to be directly connected.” Ex. 1182, [0046], Fig. 1 (showing an open circle, the schematic symbol for a terminal, connected to transceiver/tuner 118). Monk explains that “[t]ypically, a STB connects to a coaxial cable from a network node (such as the wall outlet terminal) to receive cable TV and/or satellite TV signals.” Ex. 1183, [0007]. Banker claims “[a] subscriber terminal apparatus” that comprises “an apparatus input terminal for receiving a television signal comprising a plurality of channels.” Ex. 1184, 12:59-64. These references show that an “input terminal” was a common-well-known feature of STBs that a POSITA would have expected the Cholas STB to have.

201. Moreover, the cable network signal received by the Cholas-Petrovic-Maalej STB input terminal would comprise a plurality of desired channels and a plurality of undesired channels. Cholas tuners 1713-1723 tune channels in response to user selection of a program carried on those channels, thus making the tuned

channels “desired.” Ex. 1158, [0059]-[0063]. This would not change in Cholas-Petrovic-Maalej, which would merely use separate Petrovic stages 307 instead of Cholas tuners 1713-1723 to tune desired channels, but which would, like the replaced Cholas tuners 1713-1723, remain under the direction of Cholas main processor/resource manager 1704. Ex. 1158, [0044]-[0045], [0059]-[0063]. In a conventional cable TV system with numerous 6 MHz channels between 50-1000 MHz, such as Cholas describes, and as explained above in paragraph 184, a POSITA would have understood that there would be “undesired” channels that are not tuned by a particular STB.

202. Cholas-Petrovic-Maalej also teaches that the plurality of desired channels are non-contiguous. Cholas Figure 5 shows that tuner 1 (a first Petrovic stage 307 in Cholas-Petrovic-Maalej) is tuned to QAM channel 1 (in a first frequency band) and that tuner 2 (a second Petrovic stage 307 in Cholas-Petrovic-Maalej) is tuned to QAM channel 7 (in a second frequency band). Ex. 1158, [0029]-[0030], [0042], [0045], [0054]-[0056], Fig. 5.

FIGURE 5

TUNER	QAM CHANNEL/ FREQUENCY	PROGRAM CHANNELS	PID	ROUTING
TUNER 1 1812	CHAN 1 1822	100	10035	LOCAL DECODER
		101	10135	-----
		102	10236	-----
		103	10335	-----
		104	10461	LOCAL HDD
		105	10587	-----
TUNER 2 1814	CHAN 7 1824	700	70068	REMOTE HDD
		701	70151	-----
		702	70282	-----
		703	70384	-----
		704	70487	-----
		705	70588	REMOTE DECODER
TUNER N 1816	---	---	---	---

Ex. 1158, Fig. 5

203. A POSITA, reasonably assuming that QAM channel numbers in Cholas are sequentially assigned to corresponding sequential frequency bands, would understand Cholas to teach that tuned/desired QAM channel 1 is non-contiguous with tuned/desired QAM channel 7, as QAM channels 1-7 are separated by QAM channels 2-6.

204. Moreover, Cholas Figure 5 teaches that there may be at least 3 tuners: “Tuner 1,” “Tuner 2,” and “Tuner N,” and thus at least 3 Petrovic stages 307 to simultaneously tune 3 separate QAM channels. When at least 3 QAM channels are selected, at least 2 of those channels would obviously be “non-contiguous.” Ex.

1158, Fig. 5. The QAM channels occupy separate 6 MHz portions of bandwidth (e.g., 50-1000 MHz) used by a cable network to deliver programs to the Cholas STB. Ex. 1158, [0045]. *See also* Section 8.1. If three of those separate 6 MHz portions of bandwidth are selected/desired, then at least two of those selected/desired 6 MHz portions are not contiguous to one another. *See* Section 9.1.1.b, paragraph 110.

205. Further, as a matter of common experience, and as a POSITA would have understood, users of a STB such as Cholas-Petrovic-Maalej would select channels according to their individual desires to watch content, and without regard to underlying QAM channels used to carry such content. For example, and as explained in Cholas, “Main processor/resource manager 1704 runs program guide routine 1707, which accesses information and management table(s) 1709 to identify the communications channel that includes the desired program, by identifying the program channel associated with the desired program.” Ex. 1158, [0047], [0060]-[0061], Fig. 6 (steps 1902, 1904). In other words, a human user selecting a program would not normally be aware of the QAM channel on which a desired program was carried. Thus, a POSITA would have expected that, inevitably, users would select content channels within non-contiguous QAM channels. Indeed, the ’275 patent recognizes that it was known that, inevitably, users would select (i.e., “desired”) channels that are non-contiguous in a received RF bandwidth. Ex. 1101, 1:44-48, 1:55-58, 2:16-18.

c. Limitations [1C] and [11C]

[1C] “processing, by a radio front end coupled to the input terminal, the input signal to generate a processed input signal;”

[11C] “a radio front end, coupled to the input terminal, operable to process the input signal;”

206. In my opinion, Cholas-Petrovic-Maalej discloses limitations [1C] and [11C]. Cholas-Petrovic-Maalej comprises Petrovic APD stage 107_M, a “radio front end” that is coupled to the input terminal and that generates a processed input signal. Section 9.5; Ex. 1108, [0032]-[0039], [0050], Figs. 4-5; Ex. 1109, [0010], [0017], [0031]-[0032], Figs. 1-2.

207. Similar to the Petrovic APD stage 107₁ discussed in Section 9.1.1.c, the Petrovic APD stage 107_M performs processing that includes amplifying in an amplifier of APD stage 107_M that is similar to Petrovic amplifier 222a (of APD stage 107₁), mixing in mixers of APD stage 107_M that are similar to Petrovic mixers 202 and 204 (of APD stage 107₁) using 90° phase-shifted oscillator signals from a source similar to Petrovic synthesizer/frequency source 119 (of APD stage 107₁) and a phase shifter similar to Petrovic phase shifter 105 (of APD stage 107₁), amplifying by amplifiers of APD stage 107_M that are similar to Petrovic amplifiers 222b and 222c (of APD stage 107₁), and filtering by low pass filters of APD stage 107_M that are similar to Petrovic filters 115 (of APD stage 107₁). Section 9.1.1.c; Ex. 1108, [0032]-[0039], [0050], Figs. 4-5; Ex. 1109, [0010], [0017], [0020], [0031]-[0032],

Figs. 1-2. The processing by the Petrovic APD stage 107_M includes the same type of processing performed by the radio front end 210 of the '275 patent, and generates the same type of processed input signal - downconverted and filtered in-phase and quadrature components of the input signal. Ex. 1101, 4:40-5:25, Fig. 2; Ex. 1108, [0032]-[0039], [0050], Figs. 4-5; Ex. 1109, [0010], [0017], [0020], [0031]-[0032], Figs. 1-2.

208. To the extent that “radio front end” is argued to be a means+function limitation, it is taught by Cholas-Petrovic-Maalej for the reasons explained in Section 9.1.2.c. The structure of the Petrovic APD stage 107_M of Cholas-Petrovic-Maalej is the same as, operates in the same way as, and achieves the same result as the structure of the Petrovic APD stage 107₁ of Petrovic-Eidson. Ex. 1108, [0032]-[0039], [0050], Figs. 4-5; Ex. 1109, [0010], [0017], [0020], [0031]-[0032], Figs. 1-2. Thus, like the Petrovic APD stage 107₁ of Petrovic-Eidson, the Petrovic APD stage 107_M of Cholas-Petrovic-Maalej is the same as, or equivalent to, structure of the radio front end 210 of the '275 patent, and any differences between the '275 patent structure (radio front end 210) and the Petrovic APD stage 107_M are insubstantial. Section 9.1.2.c.

d. Limitations [1D] and [11D]

[1D] “digitizing, by an analog-to-digital converter (ADC) coupled to the radio front end, the processed input signal to generate a digitized signal;”

[11D] “an analog-to-digital converter (ADC), coupled to the radio front end, operable to digitize the processed input signal to generate a digitized signal; and”

209. In my opinion, Cholas-Petrovic-Maalej discloses limitations [1D] and [11D]. ADC pair 108_M is coupled to the radio front end 107_M. Section 9.5; Ex. 1108, [0039], Fig. 4; Ex. 1109, [0005], [0010], [0020], [0022], [0028]-[0029], Fig. 1. The ADC pair 108_M digitizes the processed input signal, received from the radio front end 107_M, to generate a digitized signal. Ex. 1108, [0039], [0051]-[0052], Fig. 4; Ex. 1109, [0005], [0010], [0020], [0022], [0028]-[0029], Fig. 1.

e. Limitations [1E] and [11E]

[1E] “selecting, by a digital frontend (DFE) coupled to the ADC, the plurality of desired channels from the digitized signal; and”

[11E] “a digital frontend (DFE), coupled to the ADC, operable to select the plurality of desired channels from the digitized signal and”

210. Cholas-Petrovic-Maalej discloses limitations [1E] and [11E]. The ADC pair 108_M is coupled to a DFE that comprises a plurality of Petrovic stages 307. Section 9.5; Ex. 1108, [0053], [0055], [0059]-[0077], Figs. 4, 6; Ex. 1109, [0033], [0037]-[0054], Figs. 1, 3A. Each of the Petrovic stages 307 extracts a desired channel from the digitized signal received from the Petrovic ADC pair 108_M. Section 9.5; Ex. 1108, [0060]-[0077]; Ex. 1109, [0037]-[0054].

211. To the extent that “digital frontend” is argued to be a means+function limitation, it is taught by Cholas-Petrovic-Maalej for the reasons explained in

Section 9.1.2.e. As explained in Section 9.1.2.e, any differences between the '275 patent structure (N mixers 300 and N filters 330 and 340) and the Petrovic stages 307 are insubstantial. Both perform the same function of selecting desired channels and outputting to demodulators, in the same way by first downconverting the desired channels to baseband and then low pass filtering with a filter to isolate the channels, to achieve the same result of selecting a plurality of desired channels from a digitized signal and outputting to demodulators.

f. Limitations [1F] and [11F]

[1F] “outputting, by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator extracts information encoded in the digital datastream.”

[11F] “output the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator is operable to extract information encoded in the digital datastream.”

212. Cholas-Petrovic-Maalej discloses limitations [1F] and [11F]. In Cholas-Petrovic-Maalej, the Petrovic stages 307 are the DFE of limitations [1E]/[11E] and [1F]/[11F]. The Petrovic stages 307 select the plurality of desired channels from the digitized signal (i.e., selects channels from the signal received by the stages 307 from the Petrovic ADC pair 108_M) and output the selected plurality of channels as a digital datastream to demodulators (the Cholas demodulators implemented to include components of the Maalej demodulators). Section 9.5. Maalej further teaches “wherein the demodulator extracts information encoded in

the digital datastream.” For example, Maalej teaches that states that “MPEG2 Transport System (TS) packets” are “the output of the demodulator.” Ex. 1160, 5:12-15. In any event, demodulation, which a POSITA would have understood a “demodulator” to perform, *is* extraction of information. Ex. 1115 at 7 (“The reconversion of a modulated signal back into its original form by extracting the data from the modulated carrier”). If the signal being demodulated is a digital datastream, as is the case in Cholas-Petrovic-Maalej, then the demodulator is extracting information encoded in the digital datastream.

9.5.2. Dependent Claims 4 and 14

[4] “The method of claim 1, wherein the ADC comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.”

[14] “The television receiver device of claim 11, wherein the ADC comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.”

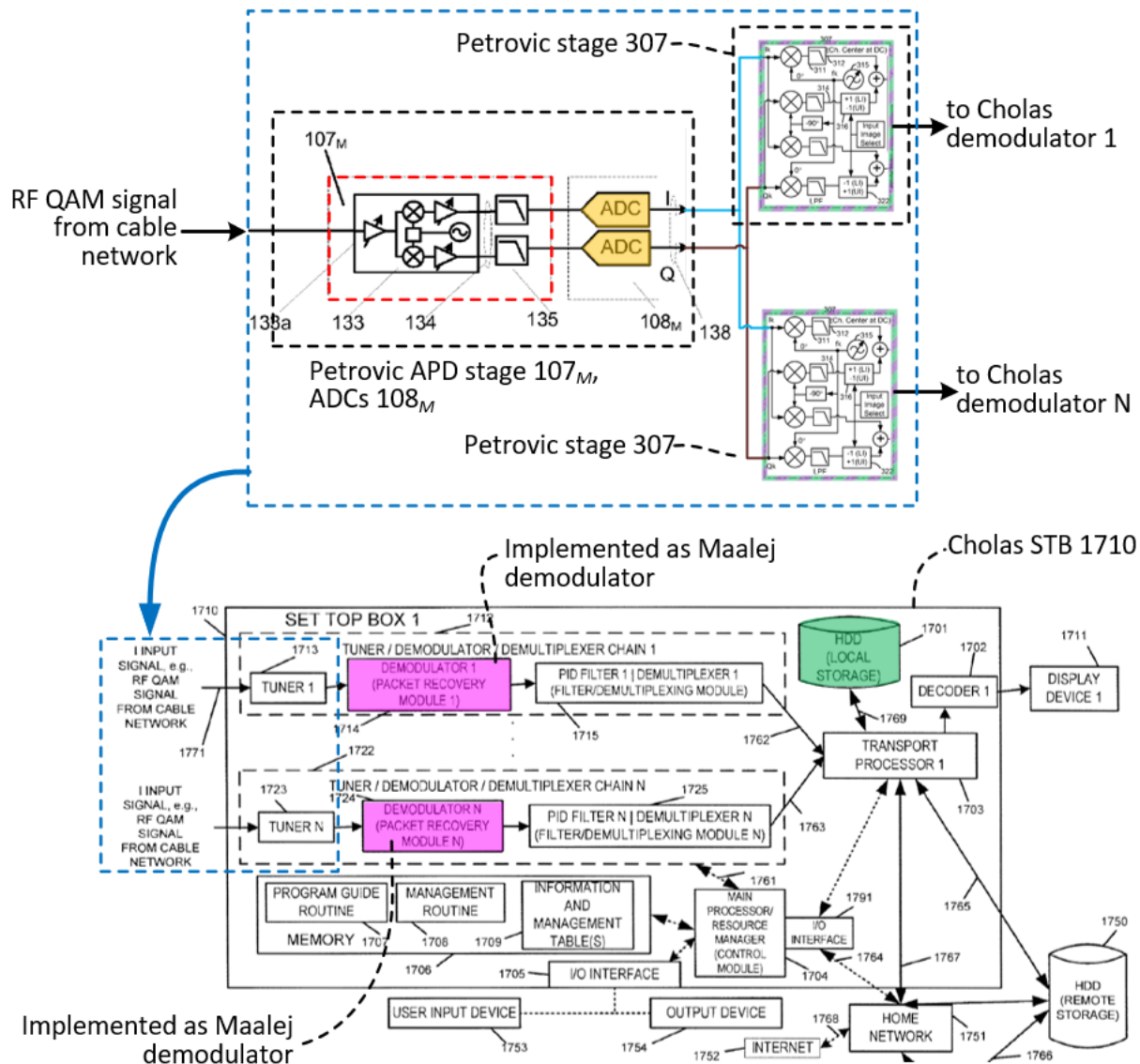
213. In my opinion, Cholas-Petrovic-Maalej discloses claims 4 and 14. Petrovic’s ADC pair 108_M comprises first and second ADCs that respectively generate digital in-phase and quadrature signals. Section 9.5; Ex. 1108, [0052], Fig. 4; Ex. 1109, [0022], Fig. 1.

9.5.3. Dependent Claims 5 and 15

[5] “The method of claim 1, wherein the extracted information is stored for use in a digital video recorder (DVR).”

[15] “The television receiver device of claim 11, wherein the extracted information is stored for use in a digital video recorder (DVR).”

214. In my opinion, Cholas-Petrovic-Maalej discloses claims 5 and 15. Cholas STB 1710 comprises a DVR 1701 (**green**), and this DVR remains in the Cholas-Petrovic-Maalej system. Ex. 1158, [0033] (“a digital storage device, e.g., a DVR, ... corresponding to the STB”), [0045] (streams can be directed to “internal HDD (local storage) 1701, typically a hard drive”), [0054]-[0057], Figs. 4-5.



Cholas-Petrovic-Maalej system

9.5.4. Dependent Claims 7-8 and 17-18

[7] “The method of claim 1, wherein the plurality of desired channels comprises at least one television channel.”

[8] “The method of claim 1, wherein the plurality of undesired channels comprises at least one television channel.”

[17] “The television receiver device of claim 11, wherein the plurality of desired channels comprises at least one television channel.”

[18] “The television receiver device of claim 11, wherein the plurality of undesired channels comprises at least one television channel.”

215. In my opinion, Cholas-Petrovic-Maalej discloses claims 7-8 and 17-18.

As explained in Section 9.5.1.a, the Cholas STB, as modified in view of Petrovic and Maalej, receives a television signal from the cable network, and a POSITA would have understood a cable network such as in Cholas to carry television channels.

9.5.5. Dependent Claims 10 and 20

[10] “The method of claim 1, wherein the broadcast channels comprise cable broadcast channels.”

[20] “The television receiver device of claim 11, wherein the broadcast channels comprise cable broadcast channels.”

216. In my opinion, Cholas-Petrovic-Maalej discloses claims 10 and 20. The Cholas STB, as modified in view of Petrovic and Maalej, receives cable broadcast channels. Section 9.5; Ex. 1158, [0004]-[0006], [0044]-[0057], Figs. 4-5.

9.6. Cholas in view of Petrovic, Maalej and Rabaey Renders Claims 2-3 and 12-13 Obvious

[2] “The method of claim 1, wherein the DFE outputs the digital datastream via a serial interface.”

[3] “The method of claim 1, wherein the DFE outputs the digital datastream via a parallel interface.”

[12] “The television receiver device of claim 11, wherein the DFE is operable to output the digital datastream via a serial interface.”

[13] “The television receiver device of claim 11, wherein the DFE is operable to output the digital datastream via a parallel interface.”

217. In my opinion, Cholas-Petrovic-Maalej-Rabaey discloses claims 2-3 and 12-13. At the most fundamental level, a digital integrated circuit represents data (such as the I, Q components 330, 340 output by a Petrovic stage 307 of Cholas-Petrovic) as binary units referred to as “bits,” in the form of electrical signals on wires (e.g., high and low voltages for binary values “1” and “0” respectively). Ex. 1116 at 23-24, 27-29, 48-51. To output multiple bits (i.e., as a “digital datastream”), the circuit can either transmit the bits over multiple separate wires, one wire for each bit, which was known as a “parallel interface,” or the circuit can transmit the set of bits one at a time as sequential pulses over a single wire, according to a fixed sequence, which was known as a “serial interface.” See my discussion above, in Section 8.4, about serial versus parallel data communication. *See also*, Ex. 1115 at 5, 8, 10; Ex. 1116 at 79-80 (Figure 6-25, annotated below).

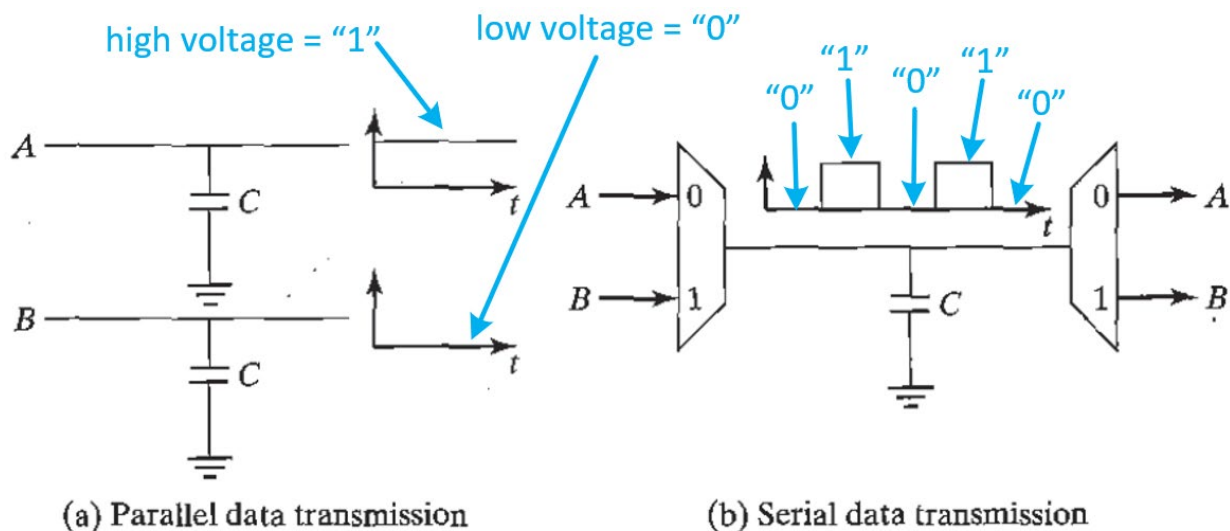


Figure 6-25 Parallel versus time-multiplexed data busses.

Ex. 1116 at 80 (Figure 6-25) (annotated)

218. In my opinion, either interface would have been an obvious design choice in Cholas-Petrovic-Maalej. As explained in Section 9.5, the stages 307 of Petrovic output desired channels as digital I, Q pairs 330, 340 that are functionally equivalent to the digital I, Q components of Maalej, and a POSITA would have applied Maalej's teachings to Cholas-Petrovic, such that each of the Cholas demodulators would be implemented to include components of the Maalej demodulators that receive (i.e., to which are output) I, Q components 330, 340 from a Petrovic first section 307. The '275 patent concedes that outputs of digital data via both serial and parallel types were "commonly known methods." Ex. 1101, 7:16-20. Basic textbooks and technical papers on digital integrated circuit design at the time confirm that a POSITA would have understood these two interfaces were two common options for outputting digital data. Ex. 1114, 30:31-42, 31:15-22; Ex. 1115

at 5, 8, 10 (defining serial and parallel transmission); Ex. 1116 at 79-80; Ex. 1117 at 354-355. Also see Section 8.4 above for my discussion of serial data communication and parallel data communication.

219. For example, Rabaey, a textbook on implementing digital integrated circuits, teaches that both serial and parallel interfaces as illustrated in the Figure 6-25 above beneficially were used in integrated circuits. Ex. 1116 at 79-80. Specifically, Rabaey teaches that time-multiplexing (i.e., a serial interface) “is a technique often used to minimize the implementation area” of a design on a chip, but that this “minimum area solution does not always result in the lowest switching activity,” for example, when the data signals have high “temporal correlation.” Ex. 1116 at 79-80, *see also* 72-74. Minimizing circuit area minimizes the cost of the integrated circuit, while minimizing the switching activity minimizes the “dynamic power dissipation” of the integrated circuit. Ex. 1116 at 29-33, 43-44, 72-74, 76-80. In fact, the area taken up by a circuit on an integrated circuit can have a major impact on the cost of that integrated circuit. Where a circuit is implemented on a die of an integrated circuit wafer, “die costs are proportional to the fourth power of the area” of the die. Ex. 1116 at 31. Thus, Rabaey teaches selecting between serial and parallel interfaces for transmitting digital data between two points, both of which have advantages over each other, depending upon area and power constraints and the temporal correlation between the signals. Ex. 1116 at 31.

220. In my opinion, a POSITA would have applied Rabaey's teachings to Cholas-Petrovic-Maalej in the same manner that they would have been applied to Petrovic-Eidson. It would have been obvious to a POSITA to apply either of Rabaey's parallel or serial interfaces as illustrated in Figure 6-25 to interconnections between Petrovic's stages 307 and demodulators implemented to include components of the Maalej demodulators, as the choice of interface would be a basic engineering choice between limited, predictable alternatives enabled by Rabaey. Ex. 1108, [0027], [0040], [0124]; Ex. 1109, [0009], [0115]; Ex. 1116 at 76-80. Petrovic teaches implementation in an integrated circuit, and the techniques taught in Rabaey would have enabled such implementation. Ex. 1108, [0027], [0040], [0124]; Ex. 1109, [0009], [0115]; Ex. 1116 at 76-80. As such, implementation of either interface in Cholas-Petrovic-Maalej would have been nothing more than a combination of prior art elements (Petrovic's and Maalej's circuit designs and Rabaey's serial or parallel interface interconnects) according to known methods (Rabaey's process for implementing circuit designs, including selecting a serial interface to minimize chip area and cost or a parallel interface to minimize switching and power) to yield predictable results (data being sent serially or in parallel).

221. The resultant combinations of Cholas-Petrovic-Maalej with Rabaey would have been predictable to a POSITA, and a POSITA would have had a reasonable expectation of success, because Rabaey teaches basic techniques used by

POSITAs to design integrated circuits, and how those basic techniques relate to design issues, such as meeting area and power constraints as I discussed above, that are often necessary for a successful design and with which a POSITA was very familiar. Ex. 1116 at 29-33, 43-44, 72-74, 76-80.

9.7. Cholas in view of Petrovic, Maalej and Lee Renders Claims 6 and 16 Obvious

[6] “The method of claim 1, wherein the extracted information is output for a picture-in-picture display.”

[16] “The television receiver device of claim 11, wherein the extracted information is output for a picture-in-picture display.”

222. In my opinion, Cholas-Petrovic-Maalej-Lee discloses claims 6 and 16.

223. Lee discloses that it was known for STBs to tune multiple channels and use the multiple tuned channels to provide picture-in-picture (PIP) functionality. Ex. 1153, [0031]. In my opinion, A POSITA would have configured the Cholas-Petrovic-Maalej STB to provide a PIP display so that the STB could provide beneficial additional functionality for the user. Ex. 1153, [0006].

224. Using the Cholas-Petrovic-Maalej STB to provide PIP functionality would also have been a use of a known technique (providing PIP output using an STB, per Lee) to improve a similar device (a Cholas-Petrovic-Maalej STB) in the same way. A POSITA could have readily modified the Cholas-Petrovic-Maalej STB to provide PIP functionality, as taught by Lee, because PIP output was established

and understood. *See* Section 8.3.2. For the same reasons, the results of that modification would have been predictable and POSITA would have had an expectation of success.

9.8. Cholas in view of Petrovic, Maalej and Takahiko Renders Claims 11, 14-15, 17-18, 20 Obvious

225. In my opinion, a POSITA would have been motivated to modify the complex mixers of the Petrovic stages 307 in view of Takahiko, in the manner described in Section 9.3 and for the reasons explained in Section 9.3. Such modification of Petrovic stages 307 in view of Takahiko would not have affected modification of Cholas in view of Petrovic and Maalej, and thus claims 11, 14-15, 17-18, and 20 are also obvious over Cholas-Petrovic-Maalej-Takahiko for the reasons explained in Sections 9.5 through 9.5.5. To the extent that the DFE of claim 11 is treated as a means+function limitation, the Petrovic stages 307, as modified in view of Takahiko, are still the claimed DFE for the reasons explained in Section 9.3.1.b.

9.9. Cholas in view of Petrovic, Maalej, Takahiko and Rabaey Renders Claims 12-13 Obvious

226. In my opinion, a POSITA would have been motivated to modify the complex mixers of the Petrovic stages 307 in view of Takahiko, in the manner described in Section 9.3 and for the reasons explained in Section 9.3. Such

modification of Petrovic stages 307 in view of Takahiko would not have affected modification of Cholas in view of Petrovic, Maalej, and Rabaey, and thus claims 12-13 are obvious over Cholas-Petrovic-Maalej-Takahiko-Rabaey for the reasons explained in Sections 9.6 and 9.8. To the extent that the DFE of claim 11 is treated as a means+function limitation, the Petrovic stages 307, as modified in view of Takahiko, are still the claimed DFE for the reasons explained in Section 9. 3.1.b.

9.10. Cholas in view of Petrovic, Maalej, Takahiko and Lee Renders Claim 16 Obvious

227. In my opinion, a POSITA would have been motivated to modify the complex mixers of the Petrovic stages 307 in view of Takahiko, in the manner described in Section 9.3 and for the reasons explained in Section 9.3. Such modification of Petrovic stages 307 in view of Takahiko would not have affected modification of Cholas in view of Petrovic, Maalej, and Lee, and thus claim 16 is obvious over Cholas-Petrovic-Maalej-Takahiko-Lee for the reasons explained in Sections 9.7 and 9.8. To the extent that the DFE of claim 11 is treated as a means+function limitation, the Petrovic stages 307, as modified in view of Takahiko, are still the claimed DFE for the reasons explained in Section 9. 3.1.b.

10. CONCLUSION

228. All of the statements made in this declaration of my own knowledge are true. All statements made based on information and belief are believed to be true.

I declare under penalty of perjury that the foregoing is true and correct.

Dated: 11/16/2024 By: David B. Lett
David B. Lett

CLAIM LISTING APPENDIX

U.S. Pat. No. 11,785,275

Designation	Claim Language
Claim 1	
[1A]	A method for operating a television receiver, comprising:
[1B]	receiving by an input terminal, an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels, wherein the plurality of desired channels are non-contiguous;
[1C]	processing, by a radio front end coupled to the input terminal, the input signal to generate a processed input signal;
[1D]	digitizing, by an analog-to-digital converter (ADC) coupled to the radio front end, the processed input signal to generate a digitized signal;
[1E]	selecting, by a digital frontend (DFE) coupled to the ADC, the plurality of desired channels from the digitized signal; and
[1F]	outputting, by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator extracts information encoded in the digital datastream.
Claim 2	
2	The method of claim 1, wherein the DFE outputs the digital datastream via a serial interface.
Claim 3	
3	The method of claim 1, wherein the DFE outputs the digital datastream via a parallel interface.
Claim 4	
4	The method of claim 1, wherein the ADC comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.
Claim 5	
5	The method of claim 1, wherein the extracted information is stored for use in a digital video recorder (DVR).

Designation	Claim Language
Claim 6	
6	The method of claim 1, wherein the extracted information is output for a picture-in-picture display.
Claim 7	
7	The method of claim 1, wherein the plurality of desired channels comprises at least one television channel.
Claim 8	
8	The method of claim 1, wherein the plurality of undesired channels comprises at least one television channel.
Claim 9	
9	The method of claim 1, wherein the broadcast channels comprise satellite broadcast channels.
Claim 10	
10	The method of claim 1, wherein the broadcast channels comprise cable broadcast channels.
Claim 11	
[11A]	A television receiver device, comprising:
[11B]	an input terminal operable to receive an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels, wherein the plurality of desired channels are non-contiguous;
[11C]	a radio front end, coupled to the input terminal, operable to process the input signal;
[11D]	an analog-to-digital converter (ADC), coupled to the radio front end, operable to digitize the processed input signal to generate a digitized signal; and
[11E]	a digital frontend (DFE), coupled to the ADC, operable to select the plurality of desired channels from the digitized signal and
[11F]	output the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator is operable to extract information encoded in the digital datastream.
Claim 12	
12	The television receiver device of claim 11, wherein the DFE is operable to output the digital datastream via a serial interface.

Designation	Claim Language
Claim 13	
13	The television receiver device of claim 11, wherein the DFE is operable to output the digital datastream via a parallel interface.
Claim 14	
14	The television receiver device of claim 11, wherein the ADC comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.
Claim 15	
15	The television receiver device of claim 11, wherein the extracted information is stored for use in a digital video recorder (DVR).
Claim 16	
16	The television receiver device of claim 11, wherein the extracted information is output for a picture-in-picture display.
Claim 17	
17	The television receiver device of claim 11, wherein the plurality of desired channels comprises at least one television channel.
Claim 18	
18	The television receiver device of claim 11, wherein the plurality of undesired channels comprises at least one television channel.
Claim 19	
19	The television receiver device of claim 11, wherein the broadcast channels comprise satellite broadcast channels.
Claim 20	
20	The television receiver device of claim 11, wherein the broadcast channels comprise cable broadcast channels.