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THE UNITED STATES OF AMERICA

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UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

April 17, 2024

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APPLICATION NUMBER: ***17/862,946***
FILING DATE: ***July 12, 2022***
PATENT NUMBER: ***11490152***
ISSUE DATE: ***November 01, 2022***

UNITED STATES PATENT AND TRADEMARK OFFICE
DEPARTMENT OF COMMERCE

Certified by

Kathi

Performing the Functions and Duties of the
Under Secretary of Commerce
for Intellectual Property
and Director of the United States
Patent and Trademark Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Attorney Docket No. 28427US15

In the Application of:	
Madhukar Reddy	**Electronically Filed: July 12, 2022**
Serial No.: Not yet assigned	
Filed: Concurrently	
Title: SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	
Group Art Unit: Not yet assigned	
Confirmation No.: Not yet assigned	
Customer No.: 23466	

PRELIMINARY AMENDMENT

Applicant submits this Preliminary Amendment in connection with the above-identified newly filed continuation application ("Instant Application").

CONTENTS OF THIS CORRESPONDENCE

General Statement on Filing of Amendments begins on page 2.

Amendments to the Specification begin on page 3.

Amendments to the Claims begin on page 4.

Remarks begin on page 8.

Filing Of Amendments

Title 37 USC, §1.125(a) states that "If the number or nature of the amendments or the legibility of the application papers renders it difficult to consider the application, or to arrange the papers for printing or copying, the Office may require the entire specification, including the claims, or any part thereof, be rewritten." The Applicant submits that this does not apply in the present situation because the preliminary amendment submitted was in the proper format, does not include an excessive number of amendments, and is perfectly legible. Accordingly, the Applicant respectfully submits that, in general, a preliminary amendment is a proper vehicle for effecting changes to the claims.

Amendments to the Specification

Please amend the title as follows:

SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL ~~WIDEBAND TUNER ARCHITECTURE~~

Please amend paragraph [0001] as follows:

[0001] This application is a continuation of U.S. patent application 17587,462 filed on January 28, 2022 (allowed), which is a continuation of U.S. patent application 17/217,244 filed on March 30, 2021 (abandoned), which is a continuation of U.S. patent application 16/430,506 (now patent 10,972,781) filed on June 4, 2019, which is a continuation of U.S. patent application 15/792,318 (now patent 10,313,733) filed October 24, 2017, which is a continuation of U.S. patent application 14/948,881 (now patent 9,819,992) filed November 23, 2015, which is a continuation of U.S. patent application 14/617,973 (now patent 9,210,363) filed on February 10, 2015, which is a continuation of U.S. patent application 13/962,871 (now patent 9,100,622) filed on August 08, 2013, which is a continuation of U.S. patent application 12/762,900 filed on April 19, 2010 (now U.S. Patent 8,526,898), which claims the benefit of priority to U.S. provisional application 61/170,526 filed April 17, 2009, now expired. Each of the above referenced documents is hereby incorporated by reference in its entirety.

Amendments to the Claims:

This listing of claims will replace all prior version and listings of claims in the application.

What is claimed is:

1-18 (Cancelled)

19. (New) A method for operating a television receiver, comprising:

receiving, by an input terminal, an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels;

processing, by a radio front end coupled to the input terminal, the input signal to generate a processed input signal;

concurrently digitizing, by an analog-to-digital converter (ADC) coupled to the radio front end, all broadcast channels in the processed input signal to generate a digitized signal;

selecting, by a digital frontend (DFE) coupled to the ADC, the plurality of desired channels from the digitized signal; and

outputting, by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator extracts information encoded in the digital datastream.

20. (New) The method of claim 19, wherein the DFE outputs the digital datastream via a serial interface.

21. (New) The method of claim 19, wherein the DFE outputs the digital datastream via a parallel interface.

22. (New) The method of claim 19, wherein the ADC comprises:
a first ADC configured to generate a digital in-phase signal; and
a second ADC configured to generate a digital quadrature signal.

23. (New) The method of claim 19, wherein the extracted information is stored for use in a digital video recorder (DVR).

24. (New) The method of claim 19, wherein the extracted information is output for a picture-in-picture display.

25. (New) The method of claim 19, wherein the plurality of desired channels comprises at least one television channel.

26. (New) The method of claim 19, wherein the plurality of undesired channels comprises at least one television channel.

27. (New) The method of claim 19, wherein the broadcast channels comprise satellite broadcast channels.

28. (New) The method of claim 19, wherein the broadcast channels comprise cable broadcast channels.

29. (New) A television receiver device, comprising:
an input terminal operable to receive an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels;
a radio front end, coupled to the input terminal, operable to process the input signal;

an analog-to-digital converter (ADC), coupled to the radio front end, operable to concurrently digitize all broadcast channels in the processed input signal to generate a digitized signal; and

a digital frontend (DFE), coupled to the ADC, operable to select the plurality of desired channels from the digitized signal and output the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator is operable to extract information encoded in the digital datastream.

30. (New) The television receiver device of claim 29, wherein the DFE is operable to output the digital datastream via a serial interface.

31. (New) The television receiver device of claim 29, wherein the DFE is operable to output the digital datastream via a parallel interface.

32. (New) The television receiver device of claim 29, wherein the ADC comprises:
a first ADC configured to generate a digital in-phase signal; and
a second ADC configured to generate a digital quadrature signal.

33. (New) The television receiver device of claim 29, wherein the extracted information is stored for use in a digital video recorder (DVR).

34. (New) The television receiver device of claim 29, wherein the extracted information is output for a picture-in-picture display.

35. (New) The television receiver device of claim 29, wherein the plurality of desired channels comprises at least one television channel.

36. (New) The television receiver device of claim 29, wherein the plurality of undesired channels comprises at least one television channel.

37. (New) The television receiver device of claim 29, wherein the broadcast channels comprise satellite broadcast channels.

38. (New) The television receiver device of claim 29, wherein the broadcast channels comprise cable broadcast channels.

REMARKS

The Applicant requests entry of this preliminary amendment prior to prosecution on the merits. No new matter has been added.

With respect to the present application, Applicant hereby rescinds any disclaimer of claim scope made in the parent application or any predecessor or related application. The Examiner is advised that any previous disclaimer of claim scope, if any, and the alleged prior art that it was made to allegedly avoid, may need to be revisited. Nor should a disclaimer of claim scope, if any, in the present application be read back into any predecessor or related application.

The Commissioner is hereby authorized to charge any fees required by this submission including any extra claims fees, to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

Date: July 12, 2022

/Wayne H. Bradley /
Wayne H. Bradley
Reg. No. 39,916

McAndrews, Held & Malloy, Ltd.
500 W. Madison Street - Suite 3400
Chicago, Illinois 60661
(312)-775-8000

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL
First Named Inventor/Applicant Name:	Madhukar Reddy
Filer:	Wayne Bradley/Laura Foley
Attorney Docket Number:	28427US15

Filed as Small Entity

Filing Fees for Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	80	80
UTILITY SEARCH FEE	2111	1	350	350
UTILITY EXAMINATION FEE	2311	1	400	400
REQUEST FOR PRIORITIZED EXAMINATION	2817	1	2100	2100
Pages:				
Claims:				
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
PROCESSING FEE, EXCEPT PROV. APPLS.	2830	1	70	70
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**3000**

Electronic Acknowledgement Receipt	
EFS ID:	46171371
Application Number:	17862946
International Application Number:	
Confirmation Number:	7376
Title of Invention:	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL
First Named Inventor/Applicant Name:	Madhukar Reddy
Customer Number:	23446
Filer:	Wayne Bradley/Laura Foley
Filer Authorized By:	Wayne Bradley
Attorney Docket Number:	28427US15
Receipt Date:	12-JUL-2022
Filing Date:	
Time Stamp:	16:05:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$3000
RAM confirmation Number	E20227BG06224249
Deposit Account	130017
Authorized User	Laura Foley
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Track One Request	28427US15_Track_1_Certification_AIA-424.pdf	113975 e96b13924fbb31e90d75d8d318ea119e88a16ae9	no	2
Warnings:					
Information:					
2	Application Data Sheet	28427US15_ADS.pdf	2197303 6e34281a8fdbc5758e3c4aa47dafb5669a9196f0	no	10
Warnings:					
Information:					
3	Drawings-only black and white line drawings	28427US06_Figures.pdf	4419764 3146aa711b9cb4885113ed88fc4c2537ca051c59	no	10
Warnings:					
Information:					
4	Oath or Declaration filed	28427US06_Declarations_executed.pdf	336661 44750254e8ce14db07258504c15bc9b027a9eb02	no	3
Warnings:					
Information:					
5		28427US08_CON_Specification.pdf	135177 db8ad20ff9549a1be835281e273d2302ebf25b23	yes	27

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	21
Claims	22	26
Abstract	27	27

Warnings:					
Information:					
6	Power of Attorney	Entropic_POA.pdf	178652 e6db8e1b2d4d91029828cff590ccdcff8015ee72	no	2
Warnings:					
Information:					
7	Information Disclosure Statement (IDS) Form (SB08)	28427US15_IDS_sb08a_EFS-WEB.pdf	1237269 8a273b975c757b9017eeaecfb74fb684df5fc428	no	9
Warnings:					
Information:					
8	Foreign Reference	EP2087623A2.pdf	112213 112c7af198fa095a19b1da28e1827b7e61c79aef	no	2
Warnings:					
Information:					
9	Non Patent Literature	NPL_1.pdf	603163 5088d48613579b3d2816d5522ec4dd7a0ecca16f	no	14
Warnings:					
Information:					
10	Non Patent Literature	NPL_2.pdf	443966 4bfc54746c564f3cb9b7cd840dd98df22fb2fe7a	no	8
Warnings:					
Information:					
11	Non Patent Literature	NPL_3.pdf	413840 d2b4d3610b34404f76c07a733fd5e032965754d1	no	7
Warnings:					
Information:					
12		28427US15_FINAL_Prelim_Amendment_.pdf	38242 8279e94bb242c88b1afe67ed0babc702b9c06170	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	2
	Specification	3	3
	Claims	4	7
	Applicant Arguments/Remarks Made in an Amendment	8	8

Warnings:

Information:

13	Fee Worksheet (SB06)	fee-info.pdf	50618 987b66f21a6c425dc3da37e18ba23e91d070b959	no	2

Warnings:

Information:

Total Files Size (in bytes):	10280843

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION UNDER 37 CFR 1.102(e) (Page 1 of 1)

First Named Inventor:	Madhukar Reddy	Nonprovisional Application Number (if known):	
Title of Invention:	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently $0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.

2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.

3. The applicable box is checked below:

I. ☑ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.

---OR---

(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.

ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, **or** the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

i. A request for continued examination has been filed with, or prior to, this form.
ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Wayne H. Bradley/	Date July 12, 2022
Name (Print/Typed) Wayne H. Bradley	Practitioner Registration Number 39,916

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.**

☑ *Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US15
	Application Number	
Title of Invention	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Madhukar		Reddy	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Carlsbad	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	5966 La Place Court
Address 2	Ste. 100
City	Carlsbad
State/Province	CA
Postal Code	92008
Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Curtis		Ling	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Carlsbad	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	5966 La Place Court
Address 2	Ste. 100
City	Carlsbad
State/Province	CA
Postal Code	92008
Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Tim		Gallagher	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

PTO/AIA/14 (01-22)
Approved for use through 05/31/2024. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US15
	Application Number	
Title of Invention	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	

City	Carlsbad	**State/Province**	CA	**Country of Residence**	US

Mailing Address of Inventor:

Address 1	5966 La Place Court		
Address 2	Ste. 100		
City	Carlsbad	**State/Province**	CA
Postal Code	92008	**Country**	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	23446		
Email Address	mhmpto@mcandrews-ip.com	Add Email	Remove Email

Application Information:

Title of the Invention	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL		
Attorney Docket Number	28427US15	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	10	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US15
	Application Number	
Title of Invention	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	23446		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	17587462	2022-01-28
Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
17587462	Continuation of	17217244	2021-03-30
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17217244	Continuation of	16430506	2019-06-04	10972781	2021-04-06
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16430506	Continuation of	15792318	2017-10-24	10313733	2019-06-04
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15792318	Continuation of	14948881	2015-11-23	9819992	2017-11-14

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US15
	Application Number	
Title of Invention	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14948881	Continuation of	14617973	2015-02-10	9210363	2015-12-08
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14617973	Continuation of	13962871	2013-08-08	9100622	2015-08-04
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13962871	Continuation of	12762900	2010-04-19	8526898	2013-09-03
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
12762900	Claims benefit of provisional	61170526	2009-04-17		

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US15
	Application Number	
Title of Invention	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US15
	Application Number	
Title of Invention	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US15
	Application Number	
Title of Invention	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section. Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Entropic Communications, LLC		
Mailing Address Information For Applicant:			
Address 1	1345 Avenues of the Americas		
Address 2	46th Fl.		
City	New York	**State/Province**	NY
Country	US	Postal Code	10105
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US15
	Application Number	
Title of Invention	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Wayne H. Bradley/			Date (YYYY-MM-DD)	2022-07-12
First Name	Wayne H.	Last Name	Bradley	Registration Number	39916

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US15
	Application Number	
Title of Invention	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

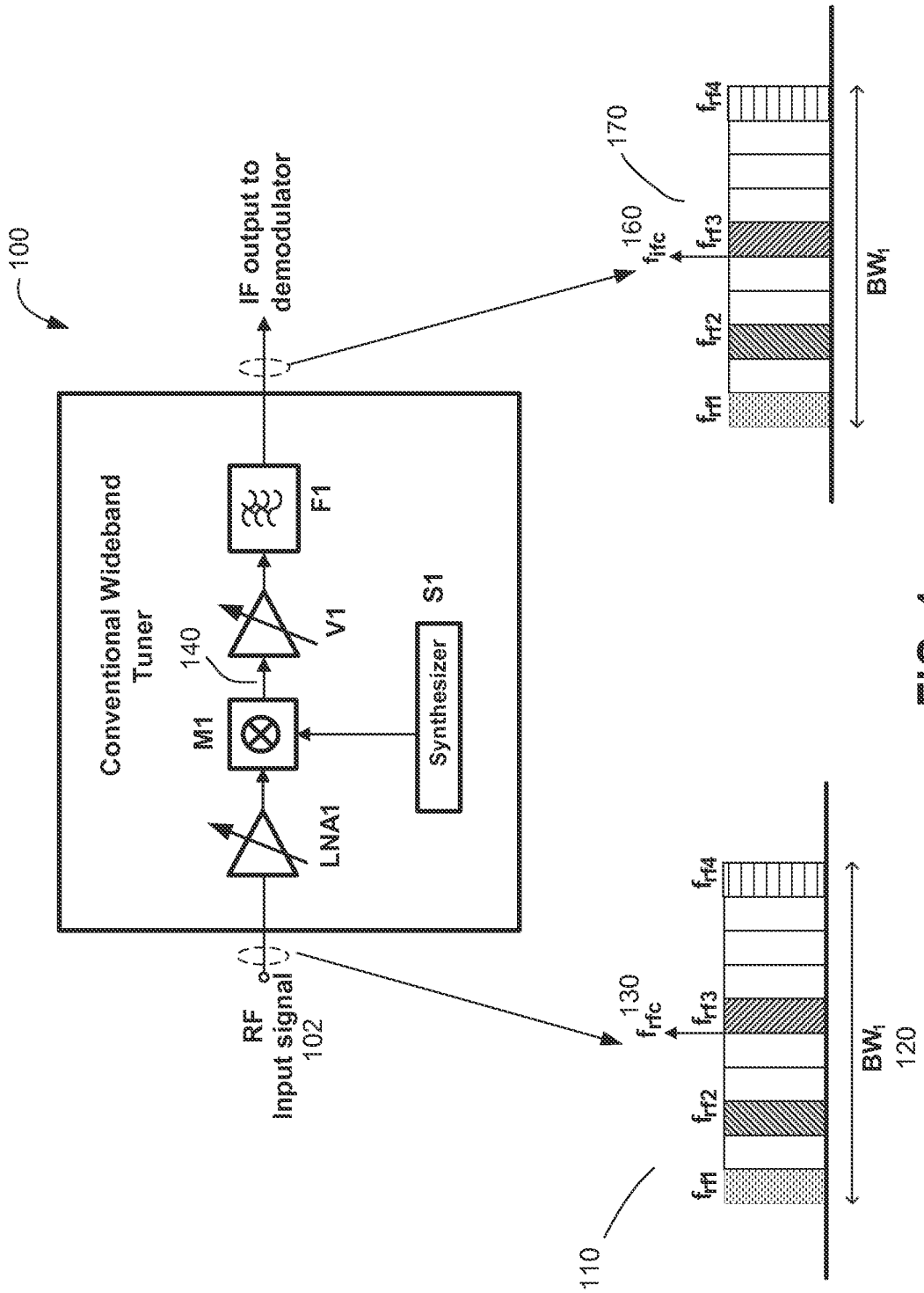

FIG. 1
(Prior Art)

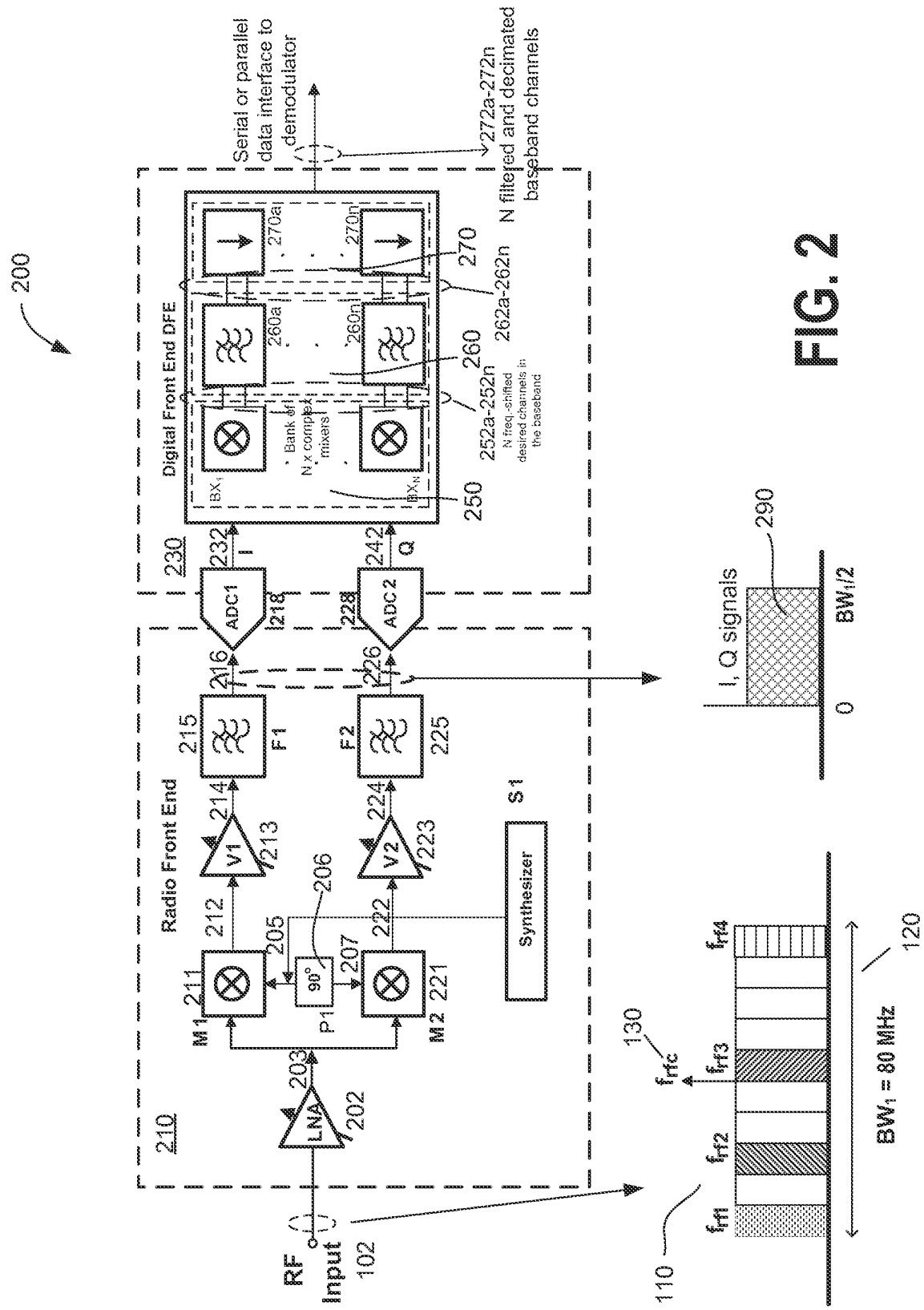
200
210
Radio Front End
230
Digital Front End DFE
RF Input
102
LNA
202
203
M1
211
P1
90°
205
206
207
M2
221
212
V1
213
214
V2
223
224
Synthesizer
S1
215
F1
216
F2
225
226
ADC1
218
ADC2
228
232
I
242
Q
BX1
BXN
Bank of N x complex mixers
250
252a-252n
N freq.-shifted desired channels in the baseband
260
260a
260n
262a-262n
270
270a
270n
Serial or parallel data interface to demodulator
272a-272n
N filtered and decimated baseband channels
I, Q signals
290
0
BW1/2
110
130
frf1
frf2
frfc
frf3
frf4
BW1 = 80 MHz
120

FIG. 2

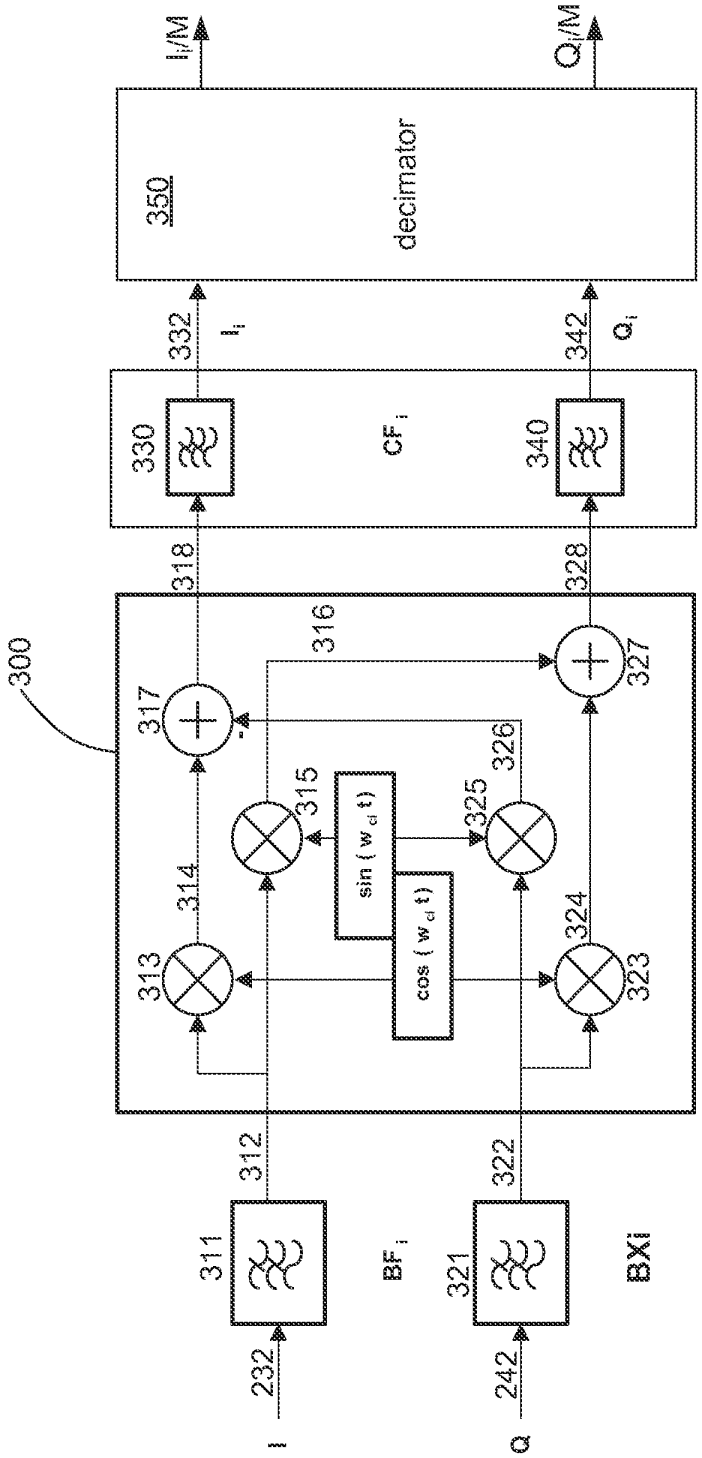
300
I
232
311
312
BF$_i$
Q
242
321
322
BXi
313
314
315
316
317
318
sin (w$_{ci}$ t)
cos (w$_{ci}$ t)
323
324
325
326
327
328
330
332
CF$_i$
340
342
I$_i$
Q$_i$
350
decimator
I$_i$/M
Q$_i$/M

FIG. 3

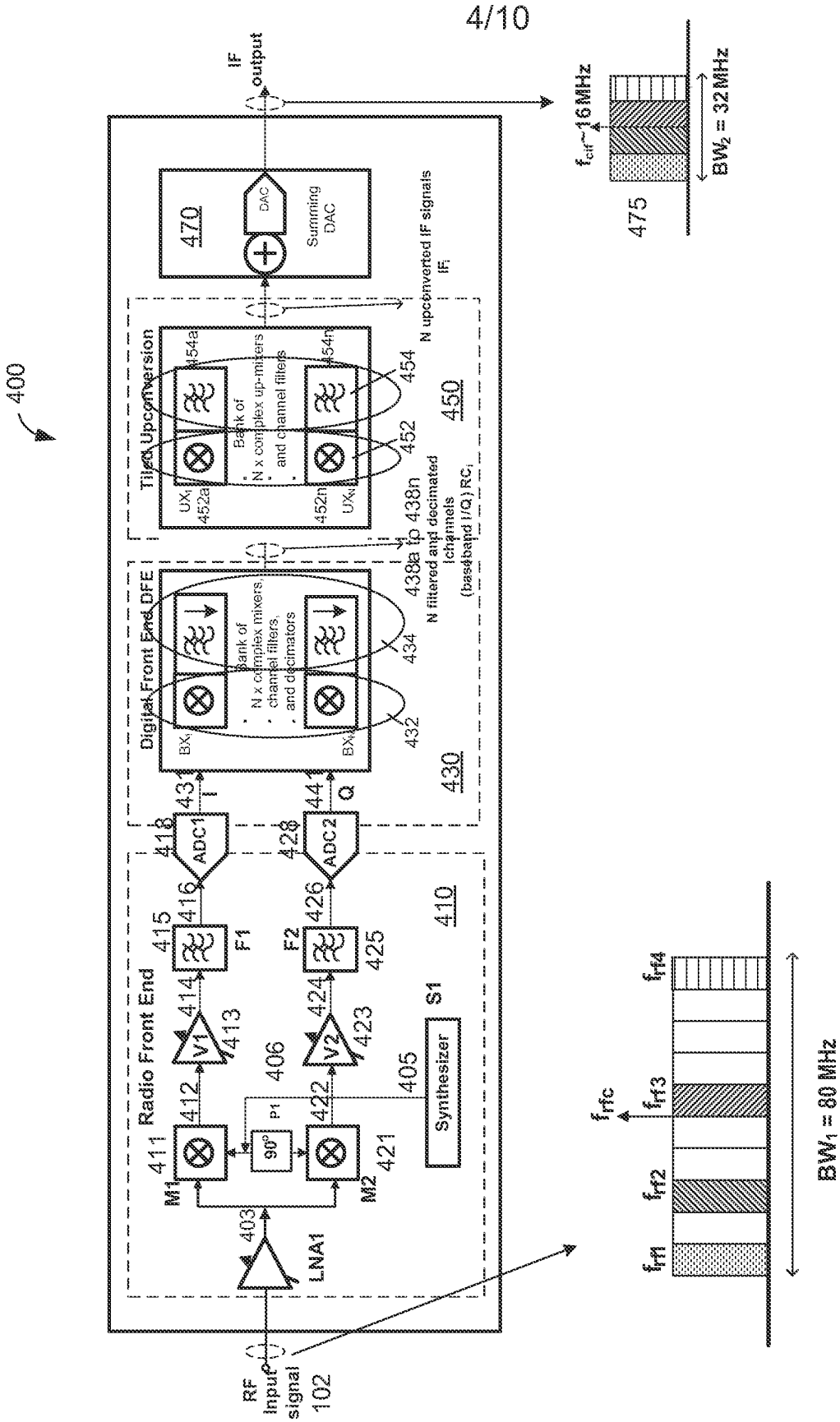
400
RF Input signal 102
LNA1
403
M1
M2
411
421
90°
P1
412
422
406
405
Synthesizer
S1
V1
V2
413
423
414
424
415
425
F1
F2
416
426
418
428
ADC1
ADC2
431
441
I
Q
Radio Front End
410
Digital Front End DFE
430
BX1
BXN
432
434
Bank of N x complex mixers, channel filters, and decimators
438a to 438n
N filtered and decimated channels (baseband I/Q) RCi
Tiled Upconversion
450
UX1
452a
452n
UXN
454a
454n
452
454
Bank of N x complex up-mixers and channel filters
N upconverted IF signals IFi
470
DAC
Summing DAC
IF output
475
fcif~16 MHz
BW2 = 32 MHz
frf1
frf2
frfc
frf3
frf4
BW1 = 80 MHz

FIG. 4

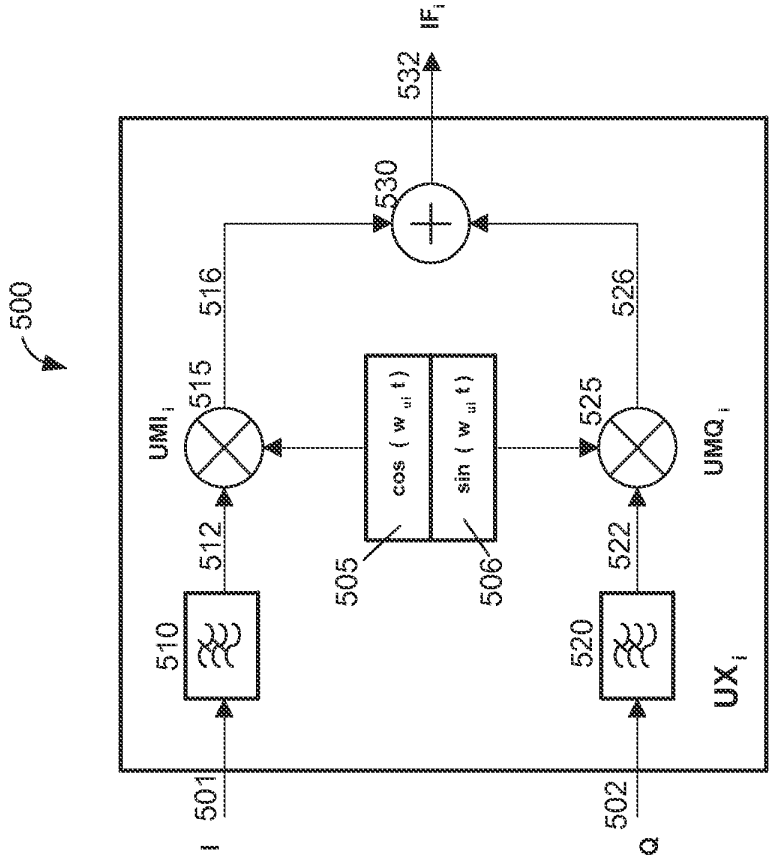
500
I
501
Q
502
510
520
UX$_i$
512
522
UMI$_i$
515
525
UMQ$_i$
516
526
530
532
IF$_i$
505
506
cos (w$_{ui}$ t)
sin (w$_{ui}$ t)

FIG. 5

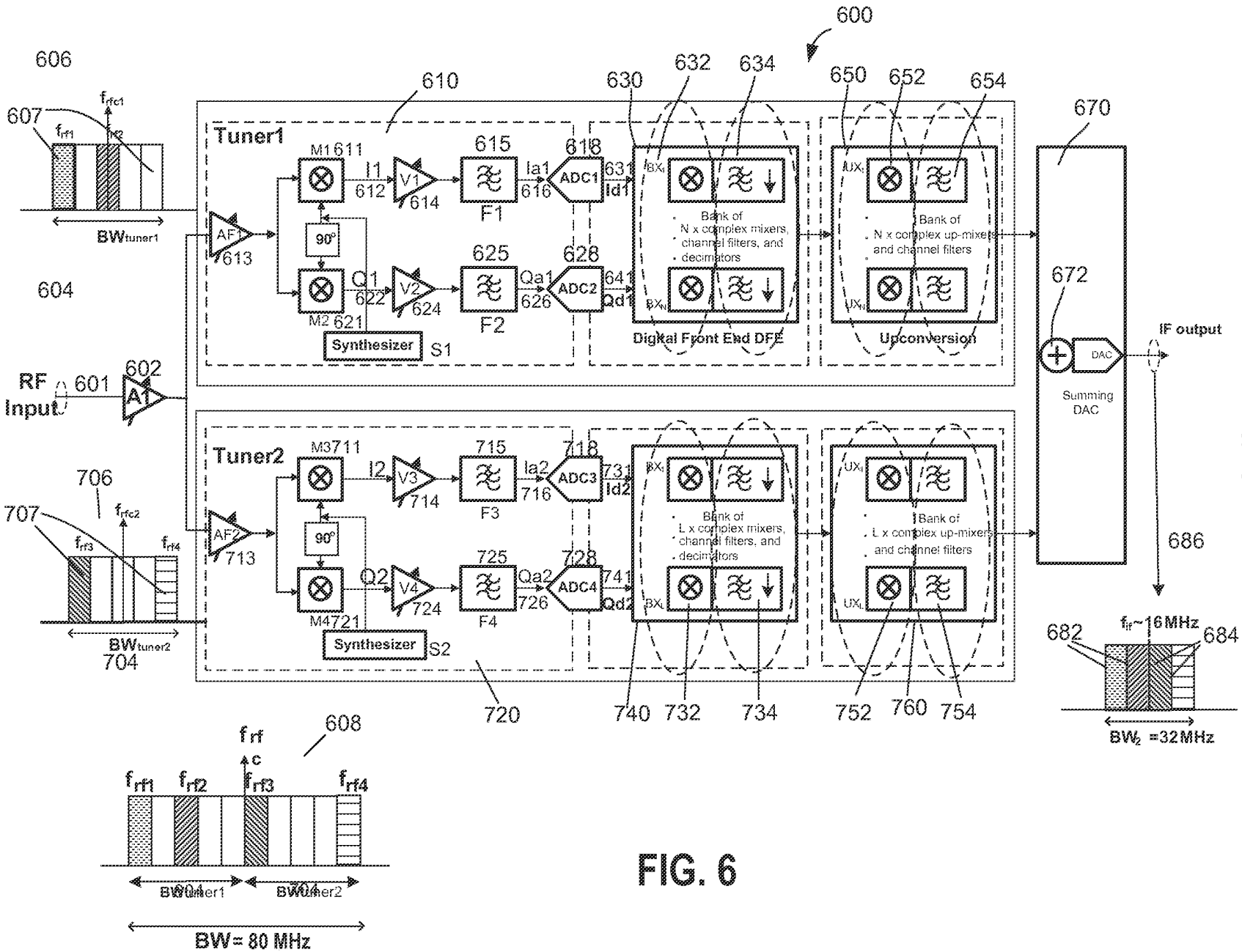
600
606
607
f_{rf1}
f_{rfc1}
f_{rf2}
BW_{tuner1}
604
RF Input
601
602
A1
706
707
f_{rfc2}
f_{rf3}
f_{rf4}
BW_{tuner2}
704
610
Tuner1
M1 611
I1
612
V1
614
615
F1
Ia1
616
618
ADC1
631
Id1
AF1
613
90°
M2 621
Q1
622
V2
624
625
F2
Qa1
626
628
ADC2
641
Qd1
Synthesizer
S1
630
632
634
Bank of
N x complex mixers,
channel filters, and
decimators
Digital Front End DFE
650
652
654
Bank of
N x complex up-mixers
and channel filters
Upconversion
670
672
DAC
Summing DAC
IF output
686
682
f_{if}~16MHz
684
BW_2 =32MHz
Tuner2
M3 711
I2
V3
714
715
F3
Ia2
716
718
ADC3
731
Id2
AF2
713
90°
M4 721
Q2
V4
724
725
F4
Qa2
726
728
ADC4
741
Qd2
Synthesizer
S2
720
740
732
734
Bank of
L x complex mixers,
channel filters, and
decimators
752
760
754
Bank of
L x complex up-mixers
and channel filters
608
f_{rfc}
f_{rf1}
f_{rf2}
f_{rf3}
f_{rf4}
BW_{tuner1}
BW_{tuner2}
BW= 80 MHz

FIG. 6

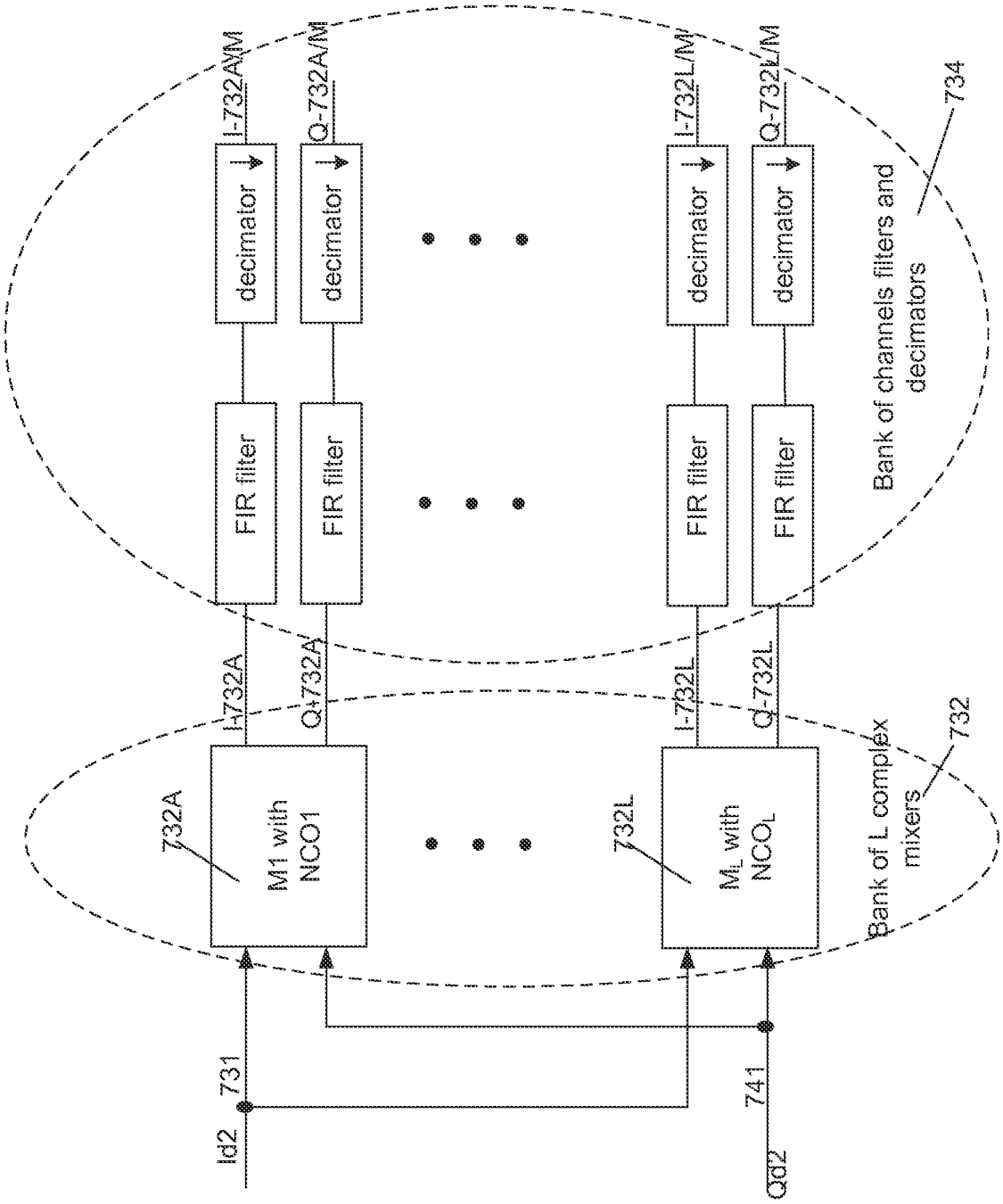
I-732A/M
Q-732A/M
I-732L/M
Q-732L/M
decimator
decimator
decimator
decimator
FIR filter
FIR filter
FIR filter
FIR filter
Bank of channels filters and decimators
734
I-732A
Q-732A
I-732L
Q-732L
732A
M1 with NCO1
732L
M_L with NCO_L
Bank of L complex mixers
732
731
741
Id2
Qd2

FIG. 7

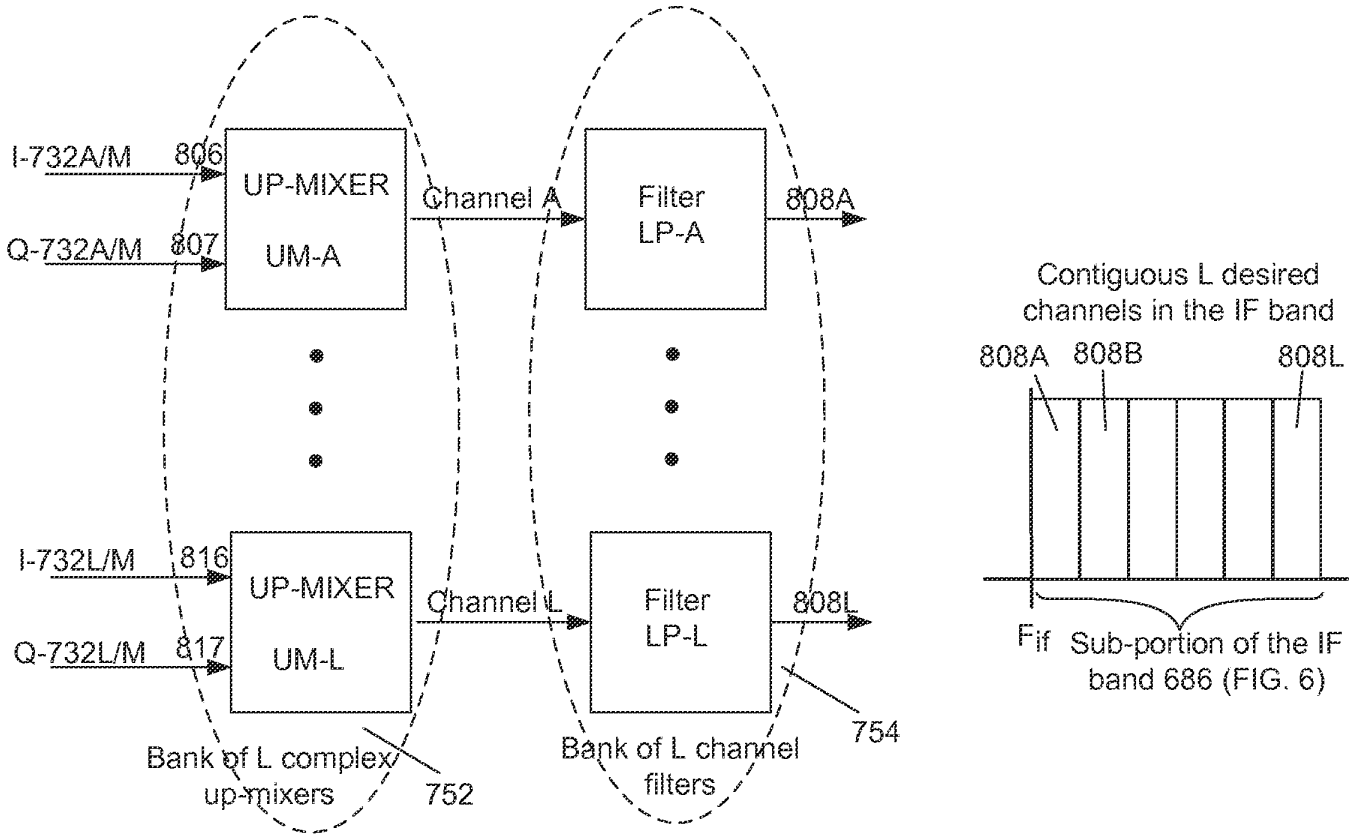
I-732A/M
806
Q-732A/M
807
UP-MIXER
UM-A
Channel A
Filter
LP-A
808A
I-732L/M
816
Q-732L/M
817
UP-MIXER
UM-L
Channel L
Filter
LP-L
808L
Bank of L complex up-mixers
752
Bank of L channel filters
754
Contiguous L desired channels in the IF band
808A
808B
808L
Fif
Sub-portion of the IF band 686 (FIG. 6)

FIG. 8

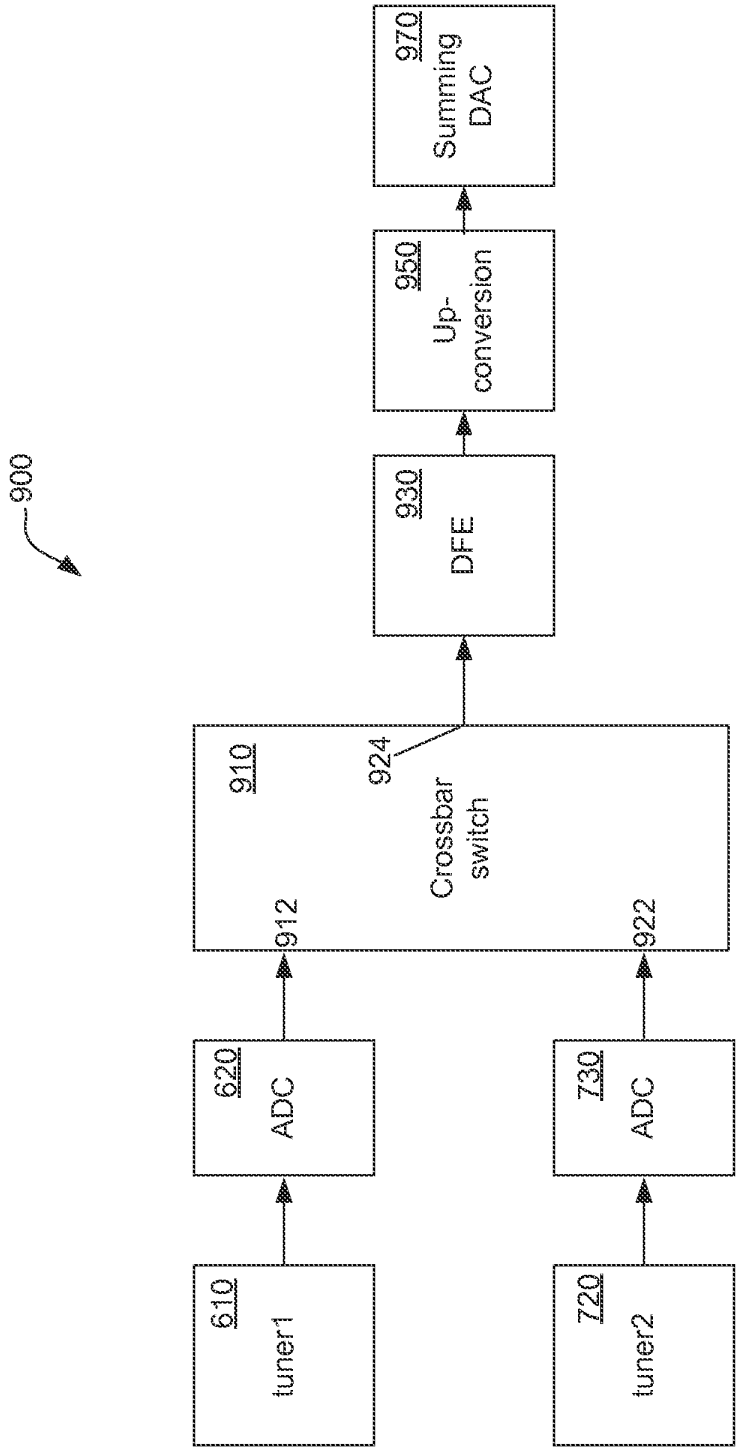
900
610
tuner1
620
ADC
720
tuner2
730
ADC
910
912
922
924
Crossbar
switch
930
DFE
950
Up-
conversion
970
Summing
DAC

FIG. 9

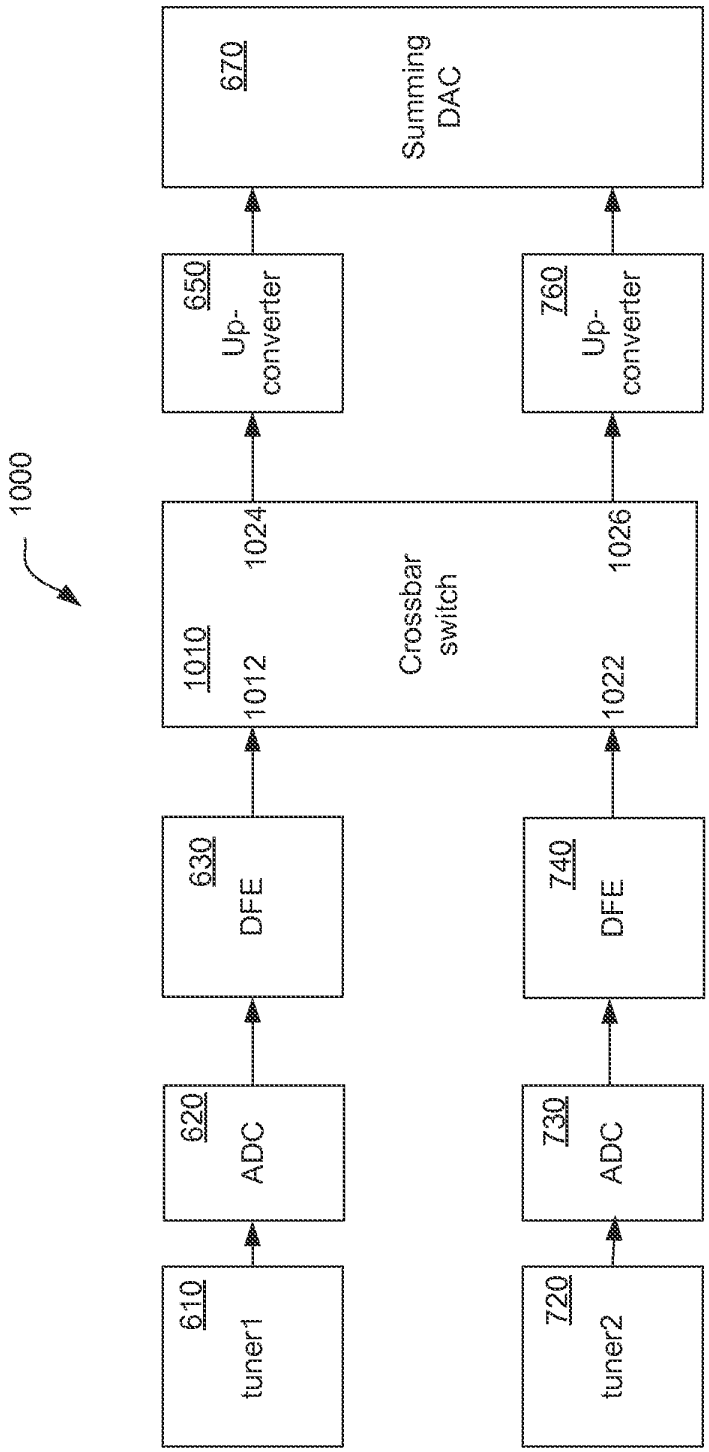
1000
610
tuner1
620
ADC
630
DFE
1010
1012
1024
Crossbar
switch
1022
1026
650
Up-
converter
670
Summing
DAC
720
tuner2
730
ADC
740
DFE
760
Up-
converter

FIG. 10

PTO/AIA/01 (06-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	WIDEBAND TUNER ARCHITECTURE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/962,871 filed on August 8, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Madhukar Reddy Date (Optional) :

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	WIDEBAND TUNER ARCHITECTURE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/962,871 filed on August 8, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

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LEGAL NAME OF INVENTOR

Inventor: Curtis Ling Date (Optional) :

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	WIDEBAND TUNER ARCHITECTURE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/962,871 filed on August 8, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Tim Gallagher Date (Optional) :

Signature:

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WIDEBAND TUNER ARCHITECTURE

PRIORITY CLAIM

[0001] This application is a continuation of U.S. patent application 14/617,973 (now patent 9,210,363) filed on February 10, 2015, which is a continuation of U.S. patent application 13/962,871 (now patent 9,100,622) filed on August 08, 2013, which is a continuation of U.S. patent application 12/762,900 filed on April 19, 2010 (now U.S. Patent 8,526,898), which claims the benefit of priority to U.S. provisional application 61/170,526 filed April 17, 2009, now expired. Each of the above referenced documents is hereby incorporated by reference in its entirety.

BACKGROUND

[0002] This invention relates to wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum. In particular, the invention relates to wideband receiver systems that are capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum and grouping them into a contiguous, or substantially-contiguous, frequency spectrum.

[0003] Receivers used to down-convert and selectively filter TV channels are referred to as tuners, and tuners designed to concurrently receive several TV channels are referred to as wideband tuners. Existing tuners for these applications down-convert a swath of channels to an intermediate frequency, which are then sent to a demodulator. Because the swath of channels is not contiguous, this swath includes the desired channels as well as undesired channels. The demodulator employs a high-speed data converter to capture this swath of desired and undesired channels in the digital domain and subsequently filters out the desired channels.

[0004] In general, television channels broadcasted over the air or over cable networks are distributed across a broad frequency spectrum. That is, the channel frequencies may not be adjacent to each other. In certain applications such as DVR and picture-in-picture, the receiver system may have to concurrently receive several desired channels that may or may not be contiguous. The wideband receiver requirement poses a trade-off to the system to limit either the dynamic range of the wideband tuner or reduce the bandwidth covered by the tuner so that fewer channels may be received and processed by the demodulator.

[0005] FIG. 1 shows a conventional wideband tuner 100. Tuner 100 may be a direct conversion tuner and includes a low noise amplifier LNA1 having an input terminal coupled to a radio frequency (RF) input signal 102 and an output terminal coupled to a mixer M1. The RF signal may include one or more television channels receiving from a cable network via an RF connector or wirelessly via an antenna. The RF input signal may include the VHF and UHF television channels in a terrestrial television broadcasting system or the CATV channels in cable networks. In order to receive all broadcasted channels present in the RF input signal, LNA1 must necessarily have a wide tuning range, high linearity, and low noise. Mixer M1 is coupled to a synthesizer S1 that can generate an oscillator frequency located around the center of the RF signal. Mixer M1 frequency down-converts the received RF input signal to a more convenient intermediate frequency (IF) band. Tuner 100 includes an amplifier V1 having a programmable gain for amplifying the IF signal, which is then band-pass filtered by a filter F1 before outputting to a demodulator.

[0006] In general, the RF signal includes multiple desired channels that are located in non-contiguous portions of a radio frequency spectrum. As shown in FIG. 1, the swath of channels 110 occupies a bandwidth BW1 120 at an RF center frequency f_{rfc} 130. Synthesizer S1 may be tuned to a frequency around the center frequency f_{rfc} 130 for

mixing channels 110 to an intermediate frequency f_{ifc} 160, the frequency down-mixed channels 140 are amplified by amplifier V1 and then filtered by F1 to produce a swath of channels 170 centered around frequency f_{ifc} 160. In an exemplary application shown in FIG. 1, bandwidth BW1 contains 10 channels. In the case where channels are TV channels that are spaced at either 6 MHz or 8 MHz in most parts of the world, bandwidth BW1 120 would span from 60-80 MHz, i.e., the down-converted bandwidth at the intermediate frequency would require a bandwidth equal to at least BW1, or at least 80 MHz when such architecture is used. It is noted that in other applications where the desired RF channels are located in the low band such as channels numbers 2 to 6 (VHF in the terrestrial TV broadcast or CATV) and in the high band such as channels numbers 14 to 83 of the UHF TV broadcast or channel numbers 63-158 of the CATV's ultra band, the bandwidth BW1 can be 800 MHz or higher. This wide bandwidth of 800 MHz would require a very expensive digital processing circuitry such as very high-speed analog to digital conversion and high-speed processor in the demodulator.

[0007] It is desirable to have wideband receiver systems that can increase the dynamic range without requiring expensive data conversion, filtering and channel selection at the demodulator.

BRIEF SUMMARY

[0008] An embodiment of the present invention includes a wideband receiver system that is configured to concurrently receive multiple radio frequency (RF) channels including a number of desired channels that are located in non-contiguous portions of a frequency spectrum and group the desired channels in a contiguous or substantially-contiguous frequency band at an intermediate frequency spectrum, where the term "substantially-contiguous" includes spacing the desired channels close to each other (e.g. as a fraction of the total system bandwidth, or relative to a channel bandwidth) but with a spacing that can be variable to accommodate the needs of overall system. The term "contiguous" heretofore encompasses "substantially-contiguous." The term "spacing" is referred to as the frequency difference between adjacent channels. The system includes a wideband receiver having a complex mixer module for down-shifting the multiple RF channels and transforming them to an in-phase signal and a quadrature signal in the baseband or low intermediate frequency (IF) band. The system further includes a wideband analog-to-digital converter module that digitizes the in-phase and quadrature signals. The digital in-phase and quadrature signals are provided to a digital frontend module that contains a bank of complex mixers that frequency-shift the number of desired channels to a baseband where the desired channels are individually filtered.

[0009] The digital frontend module may also include a decimator module that decimates the desired RF channels by a factor M before demodulating them to a digital data stream.

[0010] In certain embodiments of the present invention, the wideband receiver system additionally includes an up-converter module having multiple complex up-mixers, each of the complex up-mixers is configured to frequency up-shift each one of the desired RF channels to a sub-portion of an IF spectrum, wherein all sub-portions of the desired channels are adjacent to each another and form a contiguous frequency band in the IF

spectrum. The act of frequency shifting the desired channels to the IF spectrum allows the wideband receiver system to directly interface with commercially available demodulators. Allowing the spacing of the desired channels in the contiguous spectrum to be variable allows a system to optimize placement of these desired channels for the purposes of avoiding sensitive portions of the spectrum which may either be vulnerable to spurious signals and interference; or which may generate interference directly or as a harmonic product, to other systems.

[0011] In another embodiment of the present invention, a multi-tuner receiver system having two or more tuners is provided to receive multiple desired RF channels that extend over several non-contiguous sub-portions of a broad frequency spectrum and group them into a contiguous frequency spectrum. The multi-tuner system includes at least a first tuner that processes a first sub-portion of the broad frequency spectrum into a first in-phase signal and a first quadrature signal and a second tuner that processes a second sub-portion of the broad frequency spectrum into a second in-phase signal and a second quadrature signal. The multi-tuner receiver system further includes a first analog-to-digital converter module that digitizes the first in-phase and quadrature signals and a second analog-to-digital converter module that digitizes the second in-phase and quadrature signals. In addition, the multi-tuner system includes a first digital frontend module having a first number of complex mixers corresponding to a first number of the desired RF channels located in the first sub-portion of the broad frequency spectrum and a second digital frontend module having a second number of complex mixers corresponding to a second number of the desired RF channels located in the second sub-portion of the broad frequency spectrum. The first digital frontend module frequency shifts the first number of the desired RF channels to a first plurality of baseband signals and the second digital frontend module frequency shifts the second number of the desired RF channels to a second plurality of baseband signals.

[0012] The multi-tuner system further includes a first up-converter module having a plurality of N complex mixers, wherein N is an integer value equal to the number of desired channel. The first up-converter module frequency up-shifts the first plurality of the baseband signals to a first portion of an intermediate frequency. In addition, the multi-tuner system includes a second up-converter module that frequency up-shifts the second plurality of the baseband signals to a second portion of an intermediate frequency. The first and the second portions of the intermediate frequency are non-overlapping and located adjacent to each other to form a contiguous intermediate frequency (IF) band. The multi-tuner system further includes a digital-to-analog converter that converts the contiguous IF band to an analog waveform signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 is a schematic block diagram of a conventional wideband tuner;

[0014] FIG. 2 is a schematic block diagram of a wideband receiver system according to an embodiment of the present invention;

[0015] FIG. 3 is a simplified circuit diagram of a complex down-mixer according to an embodiment of the present invention;

[0016] FIG. 4 is a simplified schematic block diagram of a wideband receiver system according to another embodiment of the present invention;

[0017] FIG. 5 is a simplified circuit diagram of a complex up-mixer according to an embodiment of the present invention;

[0018] FIG. 6 is a simplified schematic block diagram of a wideband multi-tuner receiver system according to an embodiment of the present invention;

[0019] FIG. 7 is a block diagram illustrating an exemplary digital front end according to an embodiment of the present invention in more detail;

[0020] FIG. 8 is a block diagram illustrating an exemplary tiled up-converter module according to an embodiment of the present invention in more detail;

[0021] FIG. 9 is a simplified block diagram of a wideband multi-tuner receiver system 900 according to an embodiment of the present invention; and

[0022] FIG. 10 is a simplified block diagram of a wideband multi-tuner receiver system 1000 according to another embodiment of the present invention.

DETAILED DESCRIPTION

[0023] FIG. 2 is a schematic block diagram of a wideband receiver system 200 according to an embodiment of the present invention. Wideband receiver system 200 includes a radio front end 210 and a digital front end 230. Radio front end 210 may be a single very wide-band tuner receiver that captures the desired swath of channels located in non-contiguous portions of the spectrum having a frequency bandwidth BW1 120. In this example, the number of available channels in BW1 120 is assumed to be 10 with each channel occupying an 8 MHz bandwidth for a total of 80 MHz. Radio front end 210 is shown as including a low noise amplifier LNA 202 having an input terminal configured to receive an RF input signal 102. In the example shown, RF signal 102 includes four desired RF channels having the respective carrier frequency f_{rf1}, f_{rf2}, f_{rf3}, and f_{rf4} that are located in non-contiguous portions of the wide frequency spectrum BW1. It is understood, however, that spectrum BW1 120 may have any other number of desired frequencies that are not contiguous. LNA 202 has a very low noise figure and very high linearity and a wide tuning range (i.e., very high IIP2 and IIP3 intercept points) to maximize a signal-to-noise-and distortion ratio (SNDR) at the amplifier output. LNA 202 may have a programmable gain to amplify RF signal 102 to adequate voltage levels for mixers M1 211 and M2 221.

[0024] Mixers M1 211 and M2 221 may be conventional mixers formed using, for example, differential Gilbert cells. Each of the mixers 211 and 221 multiplies (mixes) an amplified RF signal 203 with a respective first oscillator frequency signal 205 and a second oscillator frequency signal 207 to generate an in-phase signal 212 and a quadrature signal 222 that have a phase shift of 90° degree between them. Mixers 211 and 221 are identical so that the amplitude of the in-phase signal 212 and quadrature signal 222 are the same. The first and second oscillator frequencies 205 and 207 are identical and have a 90° degree phase shift generated through a 90° degree phase shifter P1 206. Synthesizer S1 may be a single local oscillator operable to generate the oscillator

frequency 205 for converting the receive RF signal 102 to a zero-IF or low-IF band. Synthesizer S1 can be a coarse (large step) phase locked loop. Synthesizer S1 can also be programmable to cover the wideband frequency of the analog and digital terrestrial broadcast and/or the cable television system. The RF signal 102 may have relatively uniform signal strength in a cable network. However, its signal strength may extend in several orders of magnitude in a terrestrial broadcast system, thus, LNA 202 and/or mixers M1 211, M2 221 are required to have a relatively high dynamic range to handle the large variations in the signal strength.

[0025] In-phase signal 212 and quadrature signal 222 are further amplified and filtered by respective amplifiers V1 213, V2 223 and filters F1 215, F2 225 to generate a filtered in-phase signal 216 and a filtered quadrature signal 226. Filters F1 215 and F2 225 may be passive or active low-pass filters to filter out any unwanted frequency components of the signals 214 and 224 before digitizing them for further processing in digital front end 230. It is understood that the in-phase path 216 and the quadrature path 226 must have the same amplitude spectrum and maintain a fixed phase relationship, i.e., amplifiers V1 213, V2 223 and filters F1 215, F2 225 must be substantially identical. Because the two paths 216 and 226 are in quadrature, the spectral components from both positive and negative frequencies can be overlaid so that the bandwidth (cutoff frequency) of filters F1 215 and F2 225 can be one half of the BW1 bandwidth 120.

[0026] Analog-to-digital converters ADC1 218 and ADC2 228 are high-speed (i.e., high sampling rate) converters to maximize the dynamic range. In an exemplary application, radio front end 210 operates as a nominal zero-IF down-mixer so that signals 216 and 226 have a nominal bandwidth 290 equal to one half of the RF signal bandwidth BW1 thanks to the complex down-mixer architecture. In other embodiment, radio front end 210 operates as a low-IF down-mixer so that the nominal bandwidth 290 of signals 216 and 226 is greater than one half of the bandwidth BW1. In practice, the sampling rate

of ADC1 218 and ADC2 228 is chosen to be higher than the Nyquist sampling requirement, i.e., the filtered analog quadrature signals 216 and 226 may be over-sampled in order to reduce or avoid aliasing of undesired signals into the digitized I and Q signals.

[0027] ADC1 218 generates a digital signal I 232 that is a digital representation of the analog filtered signal 216; ADC2 228 generates a digital signal Q 242 that is a digital representation of the analog filtered signal 226. Digital signals I 232 and Q 242 are then applied to a bank of N complex mixers 250, wherein N is an integer value corresponding to the number of desired RF channels located in the non-contiguous portions of the frequency spectrum BW1. It is understood that the number N can be any integer value. In one embodiment, N can be equal to the number of all available channels that exist in the licensed frequency spectrum to provide system flexibility. In other embodiments, N can be equal to the number of all receivable channels within a geographic area. In yet another embodiment, N can be an integer value less than the number of receivable channels with the geographic area to reduce system costs. In the exemplary embodiment shown in FIG. 2, the number of desired channels is 4. That is, each of the 4 complex mixers 250 mixes in-phase and quadrature signals 232 and 242 with an associated frequency to generate a corresponding baseband, which is then individually filtered, decimated and provided to an associated demodulator.

[0028] Each of the N complex mixers 250 receives the digital signals I 232 and Q 242 from ADCs 218 and 228 to extract a different one of the desired channels and frequency-shifts the extracted signals to the baseband frequency. Each of the frequency shifted desired channels 252 is filtered by an associated filter module (identified as 260a to 260n). In an embodiment, each of the filtered signals 260a to 260n may be sent directly to an associated demodulator (identified as 270a to 270n) for extracting the original information transmitted in the associated desired channel. In another embodiment, each

of the filtered signals 262a to 262n is further decimated before providing to a demodulator. A path of digital front end 230 is described in more detail below.

[0029] FIG. 3 is a simplified circuit diagram of one of the signal paths 272a to 272n of digital front end 230 shown in FIG. 2 according to an embodiment of the present invention. In an embodiment, digital signal I 232 may be further filtered by a filter 311 to obtain a filtered signal 312. Similarly, digital signal Q 242 may be further filtered by a filter 321 to obtain a filtered signal 322. Thus, digital signals 312 and 322 only contain low-frequency components with undesired high-frequency components being eliminated by respective filters 311 and 321. It is noted that filtered signals 312 and 322 are interposed between the respective ADCs 218, 228 and the bank of N complex mixers 250.

[0030] Mixer 300, which represents one of the N complex mixers 250, includes four multipliers 313, 315, 323, and 325. Multipliers 313 and 315 multiply the filtered signal 312 with respective $\cos(\omega_{ci}t)$ and $\sin(\omega_{ci}t)$ signals and generate respective products 314 and 316. Similarly, multipliers 323 and 325 multiply the filtered Q signal 322 with respective $\cos(\omega_{ci}t)$ and $\sin(\omega_{ci}t)$ signals and generate respective products 324 and 326. An adder 317 sums the products 314 and 326 to generate a frequency-shifted signal I 318. An adder 327 sums the products 324 and 316 to generate a frequency-shifted signal Q 328. Basically, complex mixer 300 causes a frequency shift of the filtered components 312 and 322 to respective baseband signals 318 and 328 in the digital domain according to the operation:

$$Y(t) = X(t) * e^{-j\omega_c t} \qquad (1)$$

or taken the Fourier transform, we obtain:

$$Y(\omega)=X(\omega-\omega_c) \qquad (2)$$

[0031] Multipliers 313, 315, 323, and 325 are identical digital multipliers. In an embodiment, a numerically controlled oscillator with quadrature output generates the $\cos(\omega_{ci}t)$ and $\sin(\omega_{ci}t)$ signals. Numerically controlled oscillators (NCO) can be implemented using a phase accumulator and a look-up table. NCOs are known to those of skill in the art and will not be described herein. The frequency ω_{ci} is so chosen that each one of the desired channels embedded in the digital signals I 232 and Q 242 will be downshifted to the baseband. In the given example shown in FIG. 2, the bank of N complex mixers will have four complex mixers, each one of the N (i.e., four) complex mixers is coupled to an individual NCO having a distinct frequency ω_{ci} so that when mixing the filtered digital I and Q signals 312 and 322 with that frequency, each one of the complex mixers will generate the signals I (318) and Q (328) of a corresponding one of the desired channels at the baseband.

[0032] In an embodiment, baseband signals 318 and 328 are further individually filtered by respective filters 330 and 340 that are identified as one of the filters 260a-n in FIG. 2. Filters 330 and 340 may be band-pass or low-pass filters having a narrow bandwidth equal to the bandwidth of a desired channel. In certain embodiments, filters 330 and 340 can be analog passive or active low-pass or complex band-pass filters such as polyphase filters. In another embodiment, filters 330 and 340 can be digital low-pass filters, such as finite impulse response (FIR) filters to eliminate high frequency components that may be aliased back to the baseband signals Ii (332) and Qi (342) when decimated by subsequent decimator 350.

[0033] The reduced sampling rate of the N desired baseband channels will be sent as a serial or parallel digital data stream to a demodulator using a serial or parallel data interface according to commonly known methods, as shown in FIG. 2. This approach provides several advantages over conventional tuner architectures. First, it eliminates the need of expensive data conversion, filtering and channel selection on the demodulator

side. Second, it removes undesired channels from the signal path at an early stage, thus relieves the large dynamic range requirement in the demodulator.

[0034] FIG. 4 shows a simplified schematic block diagram of a wideband receiver system 400 according to another embodiment of the present invention. Wideband receiver system 400 includes a radio front end 410, a digital front end 430, a tiled up-conversion module 450, and a summing digital-to-analog converter module DAC 470. Radio front end 410 includes a low noise amplifier LNA1 that receives an RF input signal 102 and provides an amplified RF signal 403 to mixers M1 411 and M2 421. Mixer M1 411 is coupled to an oscillator frequency 405 of a synthesizer S1 whereas mixer M2 421 is coupled with the oscillator frequency 405 via a phase shifter P1 406 that generates a 90° degree phase-shift to the oscillator frequency 405. Mixers M1 411 and M2 421 generate respective in-phase signal 412 and quadrature signal 422 that are further amplified by respective amplifiers V1 413 and V2 423. The amplified in-phase and quadrature signals 414, 424 are then filtered by filters F1 415 and F2 425 to eliminate undesired frequency components that would be aliased back to the in-phase and quadrature signals when digitally sampled by subsequent analog-to-digital converters ADC1 418 and ADC2 428. Digital signals I 422 and Q 442 at the input of digital front end 430 are digital representations of the filtered analog in-phase and quadrature signals 416, 426 before the ADCs. Digital front end 430 include a bank of N complex mixers 432 comprising 432a to 432n identical mixers, where N is an integer value corresponding to the number of the desired channels located in non-contiguous portions of the frequency spectrum. Each of the N complex mixers 432a to 432n frequency down-converts signals I 432 and Q 442 to an associated baseband. Each of the frequency down-converted I and Q signals are coupled to respective low-pass, band-pass, or decimating filters 434. In this regard, the radio front end 410 and the digital front end 430 are similar to respective radio front end 210 and digital front end 230 of FIG. 2 that have been described in detail above.

[0035] In an alternative embodiment of the present invention, the N filtered and decimated channels 438a to 438n (where indices a to n correspond to the associated number of desired channels) are not provided to a demodulator for demodulation. Instead, the N filtered and decimated channels 438a to 438n are further frequency up-converted to an intermediate frequency (IF) spectrum. In order to achieve that, the N filtered and decimated channels are coupled to a tiled up-conversion module 450 that includes a bank of N complex up-mixers, where N is an integer value correspond to the number of desired received channels. The N complex up-mixers include identical digital mixers 452a to 452n that will be described further in detail below with reference to FIG. 5. The N up-shifted channels are then filtered by a subsequent bank of channel filters 454 that, in an embodiment, comprises N individual finite impulse response (FIR) filters. The N filtered channels are then digitally combined and converted to the analog domain by a summing digital-to-analog converter module DAC 470. The N up-shifted channels are adjacent to each other and form a contiguous or substantially-contiguous set of channels 475 in the IF spectrum centered around f_{if} as illustrated in FIG. 4. In an embodiment, the spectra of the mixed products are spaced in such a way so as to avoid overlap with known frequency bands containing potential or actual interferers. In another embodiment, the spectra of the mixed products are spaced in such a way so as to avoid overlap with frequency bands that might introduce interference to other systems. In general, because the bandwidth BW_2 is substantially lower than BW_1, the IF frequency f_{if} can be set proportionally lower, e.g., typically about 16 MHz to accommodate the spectrum of BW2 of up to 32 MHz (corresponding to the total bandwidth of the four desired channels, each having a bandwidth of 8 MHz in this example).

[0036] The up-conversion approach of FIG. 4 provides several advantages over conventional tuner architectures. First, it allows the demodulator to operate the data converter at a lower data rate and with lower resolution (fewer bits) due to the fact that the contiguous channels have a narrower bandwidth. Second, the up-conversion approach

provides full compatibility with existing demodulators that require an analog IF signal. Third, it removes undesired channels from the signal path at an early stage, thus relieves the requirement of a high dynamic range requirement of the demodulator's analog-to-digital converter and the demodulator itself.

[0037] FIG. 5 shows a simplified exemplary circuit diagram of a complex up-mixer 500 according to an embodiment of the present invention. Up-mixer 500 is one of the N complex up-mixers 452a to 452n in tiled up-conversion module 450 shown in FIG. 4. Up-mixer 500 includes filter 510 and 520 configured to eliminate unwanted frequency components present in respective input signals I 501 and Q 502. Filtered signals 512 and 522 are provided to up-mixers UMI 515 and UMQ 525 that multiply the filtered signals 512 and 522 with respective $\cos(\omega_u t)$ and $\sin(\omega_u t)$. The products 516 and 526 are summed in an adder 530 to generate an IF signal 532 according to the following equation:

$$IF(t)=I(t)*\cos(\omega_u t)+Q(t)*\sin(\omega_u t) \qquad (3)$$

[0038] Up-mixers UMI 515 and UMQ 525 are identical digital multipliers that multiply the respective filtered signal 512 and 522 with a cosine function 505 and a sine function 506 that can be generated from a NCO using a digital phase accumulator and a look-up table.

[0039] As described above, TV channels are grouped into multiple frequency bands in North America. For example, channels 2 through 6 are grouped in VHF-low band (aka band I in Europe), channels 7 through 13 in VHF-high band (band III), and channels 14 through 69 in UHF band (bands IV and V). In order to receive such a wide frequency spectrum, the low noise amplifier and mixer must have very low noise, wide tuning range and high linearity as described above in the wideband receiver systems 200 and 400. However, a wideband receiver having a single tuner with high sensitivity may have a high power consumption. For certain applications, it may be advantageous to use multiple tuners that are optimized for a given frequency band, such as a dedicated tuner

for the low VHF band, another dedicated tuner for the high VHF band and the UHF band, and yet other dedicated tuners for receiving the digital video broadcasting (DVB) via satellite (DVB-S), via cable (DVB-C), or terrestrial digital video broadcasting (DVB-T). The multi-tuner approach may also be advantageously applied to cable networks that carry TV programs on an 88 MHz to 860 MHz according to the Data Over Cable Service Interface Specification (DOCSIS) protocol.

[0040] FIG. 6 shows a simplified schematic block diagram of a wideband multi-tuner receiver system 600 according to an embodiment of the present invention. In an embodiment, multi-tuner system 600 includes low noise amplifier A1 602 for receiving an RF input signal 601. Amplifier A1 602 is coupled to at least a tuner1 610 and a tuner2 720. In another embodiment, multi-tuner system 600 may not include amplifier 602 so that RF input signal 601 can be received directly at each tuner 610 and 720.

[0041] Tuner1 610 includes an amplifying filter AF1 613 that filters and amplifies a first portion BWtuner1 604 of a broad frequency spectrum 608 that contains a first plurality of RF channels 606 including desired channels 607 having respective channel frequencies f_{rf1} and f_{rf2}. The first portion of the broad frequency spectrum BWtuner1 604 is then frequency down-converted to a low-IF or zero-IF in-phase signal I1 612 and a quadrature signal Q1 622 through respective mixer M1 611 and M2 621. Signals I1 612 and Q1 622 are further amplified and low-pass filtered before applying to respective analog-to-digital converters ADC1 618 and ADC2 628 that convert analog signals Ia1 616 and Qa1 626 to respective digital in-phase signal Id1 631 and digital quadrature signal Qd1 641. Because tuner1 610 only covers a portion BWtuner1 604 of the entire frequency spectrum 608 having fewer channels, the ADC1 618 and ADC2 628 can be slower-speed analog-to-digital converters with a large number of bits, i.e., large dynamic range.

[0042] Digital signals Id1 631 and Qd1 641 are then provided to a digital front end DFE 630 that includes a first bank of N complex mixers 632 and channel and decimating filters 634. The first bank of N complex filters 632 has N identical complex mixers, where N is an integer value equal to the number of desired channels located in the first portion BWtuner1 604 of the broad frequency spectrum 608. In an embodiment, each one of the first bank of N complex mixers includes four digital mixers that multiply digital stream Id1 631 and Qd1 641 with respective digitized cosine function and sine function to generate the sum and difference frequency components, as shown in FIG. 3. The digitized cosine and sine frequency, i.e., the mixer frequency is so chosen so that when mixing signals Id1 631 and Qd1 641 will move them to a baseband or a low-IF band. In an embodiment, channel and decimating filters have similar structures as filters 330 and 340 and demodulator 350 as shown in FIG. 3. That is, channel and decimating filters include digital low-pass filters 330 and 340 that eliminates unwanted high frequency components of the baseband signals I and Q prior to applying them to a decimator 350 (FIG. 3) that reduces the sample frequency without any loss of information since Id1 631 and Qd1 641 are sampled at a much higher frequency by the respective ADC1 618 and ADC2 628.

[0043] The decimated desired channels are then provided to an up-converter module 650 that includes a bank of N up-mixers. The bank of N up-mixers includes N identical up-mixers whose structure is shown in FIG. 5. In an embodiment, N is an integer value equal to the number of desired channels present in BWtuner1 604. Each one of the up-mixer frequency-shifts the baseband signals I and Q of each one of the desired channels to an appropriate portion of the intermediate frequency band according to Equation (3). In other words, the bank of N up-mixers is “frequency multiplexing” the desired channels onto a first portion 682 of an IF band 686.

[0044] Similarly, tuner2 720 includes an amplifying filter AF2 713 that is configured to receive a second portion BWtuner2 704 of the broad frequency spectrum 608. The second portion 704 contains a second plurality of RF channels 706 including a second number of desired channels. In the exemplary illustration of FIG. 6, the second portion 704 has a frequency bandwidth of BWtuner2 that contains desired channels 707 having respective channel frequencies f_{rf3} and f_{rf4}. Tuner2 720 includes elements such as mixers M3 711, M4 721, amplifiers V3 714, V4 724, filters F3 715, F4 725 and analog-to-digital converters ADC3 731 and ADC4 741 that are substantially the same as the like-named elements of the signal path of tuner1 610. Thus, redundant description is omitted herein.

[0045] Digital in-phase signal Id2 731 and digital quadrature signal Qd2 741 are then provided to digital front end 740. Digital front end 740 includes a bank of L complex filters, where L is an integer value equal to the number of desired channels in the second portion BWtuner2 704 of the broad frequency spectrum 608. Each one of the bank of L complex filters is a digital complex mixer configured to transform the signals Id2 731 and Qd2 741 to baseband signals that are further filtered by individual digital low-pass filters such as FIR filters before decimated by a subsequent decimator. The elements of digital front end 740 are substantially similar to those described in digital front end 630. Thus, redundant description is omitted herein.

[0046] The decimated baseband I and Q channels are further provided to a subsequent up-conversion module 760 that performs a function substantially similar to that of the up-conversion module 650 already described above. The outputs of up-conversion module 650 and 760 can be tiled to generate a contiguous set of IF frequencies 682, 684 centered at f_{if} 686. In an embodiment, the outputs of up-conversion module 650 and 760 are digitally summed and converted to an analog signal by summing DAC 670. In another embodiment, the up-conversion modules 650 and 760 and the

digital summing function 672 can be performed using an inverse discrete Fourier transform or an inverse Fast Fourier transform operation.

[0047] The multi-tuner architecture provides the flexibility that multiple commercially available tuners can be used without the need of designing a wideband tuner. For example, a tuner designed for a terrestrial broadcast digital TV can be used together with a tuner dedicated to receiving a cable signal and/or a tuner for receiving a satellite broadcast signal. The multi-tuner receiver system provides an additional advantage that other tuners can be added quickly to the system to accommodate any future applications. Additionally, the multi-tuner architecture allows the use of slower speed (i.e., lower cost) analog-to-digital converters with a larger number of bits for achieving large dynamic range.

[0048] FIG. 7 shows a block diagram of an exemplary digital front end of the invention in more detail. In an embodiment, in-phase signal Id2 731 and quadrature signal Qd2 741 at the output of respective ADC converters 718 and 728 are provided to each of the L complex mixers 732 comprising mixers 732A to 732L. A more detailed description of each of L complex mixers is shown in FIG. 3. Mixer 732A multiplies Id2 731 and Qd2 741 with a cosine signal and a sine signal that are generated from an NCO1 and produces an I-732A signal and a Q-732A signal that are further individually filtered by an FIR filter before decimating. The bank of L complex mixers corresponds to the block 732 in FIG. 6; and the set of FIR filters and decimator corresponds to the block 734 in FIG. 6. Each decimated pair of I-732i/M in the baseband, where the index "i" is from A to L, is further provided to a subsequent up-mixer for frequency-shifting to an intermediate frequency as shown in FIG. 8.

[0049] FIG. 8 shows an exemplary embodiment of a bank of L complex up-mixers according to the present invention. Each decimated pair of complex signals I-732i/M and Q-732i/M is provided to an associated complex up-mixer, whose frequency is so chosen

that when mixing with the pair of complex signals I-732i/M and Q-732i/M will generate an associated channel at a predetermined sub-portion of the intermediate frequency band 686 (FIG. 6). A more detailed schematic block of one of the L up-mixers is described above together with FIG. 5.

[0050] FIG. 9 is a simplified block diagram of a wideband multi-tuner receiver system 900 according to an embodiment of the present invention. In an embodiment, system 900 includes a crossbar switch 910 having at least an input terminal 912 configured to receive signals from an analog-to-digital converter (ADC) 912 and an input terminal 922 configured to receive signals from an ADC 922. Crossbar switch 910 also includes an output terminal 924 that is coupled to a digital front end 930. In an embodiment, input terminals 912 and 922 of crossbar switch 910 have P inputs, where P is an integer value that is equal to the total number of desired channels received by tuner1 610 and tuner2 720. Output terminal 924 of crossbar switch 910 have Q outputs, where Q is an integer value that is equal to the total number of desired channels received by tuner1 610 and tuner2 720.

[0051] In an embodiment, digital front end 930 may include a bank of R complex mixers that frequency shifts the received channels to a baseband. Digital front end 930 may combine digital front end 630 and 740 shown in FIG. 6. Similarly, a tiled up-conversion module 950 may include up-converter modules 650 and 760 of FIG. 6.

[0052] System 900 further includes a summing DAC that operates similarly as summing DAC 470 and 670 that have been described in detail in relation with respective FIG. 4 and FIG. 6 above. Thus, redundant description is omitted herein.

[0053] FIG. 10 is a simplified block diagram of a wideband multi-tuner receiver system 1000 according to another embodiment of the present invention. System 1000 includes at least tuner1 610 coupled with digital front end 630 through an analog-to-digital converter 620 and tuner2 720 coupled with digital front end 740 through an

analog-to-digital converter 730. System 1000 further includes a crossbar switch 1010 that is interposed between digital front ends 630, 740 and up-conversion modules 650, 760. Crossbar switch 1010 includes an input terminal 1012 having S inputs coupled with DFE 630 and an input terminal 1022 having T inputs coupled with DFE 740. In an embodiment, S is an integer value equal to the number of desired channels processed in DFE 630 and T is an integer value equal to the number of desired channels processed in DFE 740. Crossbar switch 1010 further includes an output terminal 1024 having U outputs coupled with up-converter module 650 and an output terminal 1024 having V outputs coupled with up-converter module 760. In an embodiment, the total number of the outputs U and V is equal to the sum of the inputs S and T. Thus, crossbar switch 1010 allows the routing of any channel from either DFE 630 or DFE 740 to up-converters 650 or 760. It is understood that system 1000 is not as flexible as system 900 because DFE 630 and DFE 740 are already pre-assigned to respective tuner1 (610) and tuner2 (720). However, this pre-assigned arrangement allows a simpler implementation of crossbar switch 1010 that operates at lower speeds.

[0054] While several embodiments in accordance with the present invention have been described, it is to be understood that the above description is intended to be illustrative and not restrictive. Many embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

CLAIMS

What is claimed is:

1. A system comprising:

a first analog-to-digital converter (ADC) configured to digitize a first frequency band comprising a first plurality of channels;

a second ADC configured to digitize a second frequency band comprising a second plurality of channels; and

a digital frontend (DFE) circuit operatively coupled to the first ADC and the second ADC, the DFE being configured to:

frequency shift one or more channels from the first plurality of channels; and

frequency shift one or more channels from the second plurality of channels, wherein the frequency-shifted one or more channels from the first plurality of channels and the frequency-shifted one or more channels from the second plurality of channels are combined into an intermediate frequency (IF) signal.

2. The system of claim 1, wherein the IF signal is a digital signal and the DFE is configured to output the IF signal via a serial interface.

3. The system of claim 1, wherein the IF signal is a digital signal and the DFE is configured to output the IF signal via a parallel interface.

4. The system of claim 1, wherein:

prior to the frequency shift of the one or more channels from the first plurality of channels and the frequency shift of the one or more channels from the second plurality of channels, there is a first, greater amount of separation in frequency between the one or more channels from the first plurality of

channels and the one or more channels from the second plurality of channels; and

after the frequency shift of the one or more channels from the first plurality of channels and the frequency shift of the one or more channels from the second plurality of channels, there is a second, lesser amount of separation in frequency between the frequency-shifted one or more channels from the first plurality of channels and the frequency-shifted one or more channels from the second plurality of channels.

5. The system of claim 1, wherein the DFE comprises a plurality of channel filters configured to perform selection of the one or more channels from the first plurality of channels and the one or more channels from the second plurality of channels.

6. The system of claim 5, wherein each one of the plurality of channel filters is a finite impulse response filter.

7. The system of claim 1, wherein the DFE is configured to:

adjust a sample rate of the frequency-shifted one or more channels from the first plurality of channels; and

adjust a sample rate of the frequency-shifted one or more channels from the second plurality of channels.

8. The system of claim 1, wherein each of the frequency shift of the one or more channels from the first plurality of channels and the frequency shift of the one or more channels from the second plurality of channels comprises a down-shift and an up-shift.

9. The system of claim 1, wherein the first plurality of channels and second plurality of channels are satellite broadcast television channels.

10. A method comprising:

digitizing, by a first analog-to-digital converter (ADC), a first frequency band comprising a first plurality of channels;

digitizing, by a second ADC, a second frequency band comprising a second plurality of channels;

frequency shifting, by a digital frontend (DFE) circuit operatively coupled to the first ADC and the second ADC, one or more channels from the first plurality of channels; and

frequency shifting, by the DFE, one or more channels from the second plurality of channels, wherein the frequency-shifted one or more channels from the first plurality of channels and the frequency-shifted one or more channels from the second plurality of channels are combined into an intermediate frequency (IF) signal.

11. The method of claim 10, comprising outputting, by the DFE, the IF signal via a serial interface.

12. The method of claim 10, comprising outputting, by the DFE, the IF signal via a parallel interface.

13. The method of claim 10, wherein:

prior to the frequency shifting of the one or more channels from the first plurality of channels and the frequency shifting of the one or more channels from the second plurality of channels, there is a first, greater amount of separation in frequency between the one or more channels from the first plurality of

channels and the one or more channels from the second plurality of channels; and

after the frequency shifting of the one or more channels from the first plurality of channels and the frequency shifting of the one or more channels from the second plurality of channels, there is a second, lesser amount of separation in frequency between the frequency-shifted one or more channels from the first plurality of channels and the frequency-shifted one or more channels from the second plurality of channels.

14. The method of claim 10, comprising selecting, by a plurality of channel filters of the DFE, the one or more channels from the first plurality of channels and the one or more channels from the second plurality of channels.

15. The method of claim 14, wherein each one of the plurality of channel filters is a finite impulse response filter.

16. The method of claim 10, comprising:

adjusting, by the DFE, a sample rate of the frequency-shifted one or more channels from the first plurality of channels; and

adjusting, by the DFE, a sample rate of the frequency-shifted one or more channels from the second plurality of channels.

17. The method of claim 10, wherein each of the frequency shifting of the one or more channels from the first plurality of channels and the frequency shifting of the one or more channels from the second plurality of channels comprises down-shifting and up-shifting.

18. The method of claim 10, wherein the first plurality of channels and second plurality of channels are satellite broadcast television channels.

ABSTRACT

A wideband receiver system comprises a wideband analog-to-digital converter (ADC) module and a digital frontend (DFE) module. The wideband ADC is configured to concurrently digitize a band of frequencies comprising a plurality of desired channels and a plurality of undesired channels. The DFE module is coupled to the digital in-phase and quadrature signals. The DFE module is configured to select the plurality of desired channels from the digitized band of frequencies, and generate an intermediate frequency (IF) signal comprising the selected plurality of desired channels and having a bandwidth that is less than a bandwidth of the band of frequencies, where the generation comprises frequency shifting of the selected plurality of desired channels. The IF signal may be a digital signal and the DFE is configured to output the IF signal via a serial or parallel interface.

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First Named Inventor	Madhukar Reddy
Art Unit	
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	1	JEFFREY A. WELDON, et al. "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter With Harmonic-Rejection Mixers, IEEE Journal of Solid-State Circuits, December 2001, pages: 2003-2015, Vol. 36, No. 12, Seattle, Washington.	
	2	Int'l Search Report and Written Opinion Appln No. PCT/2010/031631 mailed June 17, 2010.	
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Applicant(s): R F MAGIC INC [US] ± (R.F. MAGIC INC, ; RF MAGIC, INC)

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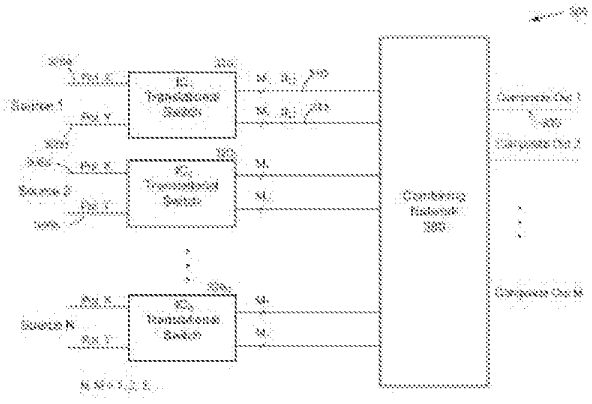
Abstract not available for EP2087623 (A2)
Abstract of corresponding document: US2008112385 (A1)

Circuits, systems, and methods for assembling a composite signal include a frequency translation circuit coupled to receive an input signal and operable to generate a plurality of frequency-translated versions of the input signal at a respective plurality of different frequencies, the plurality of frequency-translated input signals defining a group of frequency translated signals. The plurality of frequency translated signals may each be processed to provide a composite signal.



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A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter With Harmonic-Rejection Mixers

Jeffrey A. Weldon, R. Sekhar Narayanaswami, Jacques C. Rudell, *Member, IEEE*, Li Lin, Masanori Otsuka, Sebastien Dedieu, Luns Tee, *Student Member, IEEE*, King-Chun Tsai, *Student Member, IEEE*, Cheol-Woong Lee, and Paul R. Gray, *Fellow, IEEE*

***Abstract*—A highly integrated 1.75-GHz 0.35-μm CMOS transmitter is described. The I/Q modulator-based transmitter facilitates integration through the use of a unique mixer, termed a harmonic-rejection mixer, and a wide loop bandwidth phase-locked loop (PLL) for the RF synthesizer. The harmonic-rejection mixers are used to eliminate the need for a discrete IF filter and the use of a wide loop bandwidth PLL allowed for the complete integration of the synthesizers using low-Q components while achieving low phase noise. The entire transmit signal path from the digital-to-analog converters to the power amplifier, including two fully integrated frequency synthesizers, is integrated into a single-chip solution. The transmitter was tested with a testing buffer before the power amplifier (PA) and achieved less than 1.3° rms phase error when modulating a DCS-1800 GMSK signal. The prototype consumed 151 mA from a 3-V supply. A class-C PA, capable of driving 25 dBm off-chip, was included and the output was compared to the testing buffer with little change in the transmitter performance.**

***Index Terms*—Class-C power amplifier, CMOS RF, digital-to-analog converter, frequency synthesizer, harmonic-rejection mixer, harmonic-rejection transmitter, image-rejection mixer, low-pass filter, phase-locked loop, power amplifier, quadrature generation, radio architectures, radio transmitter, wireless communications.**

I. Introduction

THE DEMAND for wireless connectivity supporting both voice and data has dramatically increased in recent years. Advancements in wireless technology have largely been driven by the desire for lower cost solutions. One method of achieving this price reduction is through increased levels of integration in both the transmitter and the receiver. In addition to reducing the number of ICs needed, eliminating the need for costly discrete components can also lower the overall cost. Consequently, methods of integration have received considerable attention over the last few years [1], with the goal of complete integration of both the digital and analog circuits onto a single chip. CMOS is amenable to high integration due to the fact that the vast majority of digital integrated circuits as well as many analog integrated circuits [2] are implemented in CMOS technologies. However, maintaining high performance in a wireless system, with an integrated CMOS solution, requires advances at both the architectural and circuit level because many current implementations are not amenable to integration in CMOS.

Recently, significant effort has been directed toward the implementation of integrated CMOS receivers [3], [4]. The focus of this work is to demonstrate techniques that would allow for a highly integrated high-performance CMOS transmitter and eliminate the need for costly discrete components. The challenge was to maintain the high performance needed by cellular communications systems while using low-Q on-chip components inherent to standard CMOS. A prototype was fabricated using a 0.35-μm double-poly five-layer metal CMOS technology. The transmitter operated at 1.75 GHz and was designed for a narrow-band cellular standard, DCS-1800, an up-banded version of GSM. Although the prototype was only tested with one standard, the architecture was chosen to facilitate multistandard operation. The transmitter integrated the entire signal path from the digital-to-analog converters (DACs) to the power amplifier (PA) including two frequency synthesizers. The full integration of the transmitter was facilitated by a number of techniques including the harmonic-rejection mixer (HRM) and a wide-loop-bandwidth phase-locked loop (PLL).

Section II discusses relevant transmitter architectures and their potential for integration in CMOS and multistandard operation. Section III focuses on the harmonic-rejection transmitter in more detail while addressing a few of the key concepts and circuit blocks. Section IV examines the CMOS prototype transmitter used to demonstrate the previously discussed concepts, and Section V presents the measured results from this transmitter. Finally, some conclusions are made in Section VI.

II. Transmitter Architectures

Transmitter implementations to date have used a variety of architectures, each of which exhibits features making them well suited for implementing a specific standard. However, if the goal is multistandard operation, a transmitter architecture with high flexibility is desired. Furthermore, high performance is required if a difficult standard is among the targeted applications. In particular, RF systems with large cell sizes, such as cellular communication systems, generally require higher performance than short-range systems such as Bluetooth. The issue is further complicated by the fact that CMOS integration using low-Q components limits the performance of many circuit techniques. As

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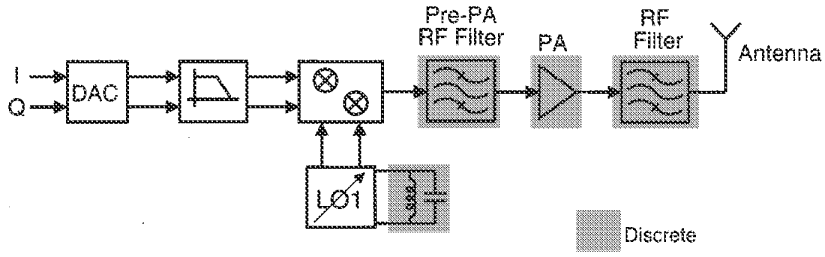


Fig. 1. Direct upconversion transmitter block diagram.

a result, new architectures and circuit techniques must be investigated if the goal is high-performance multistandard operation using CMOS and its inherently low-Q devices.

The vast majority of transmitters fall into two classes: I/Q modulator-based transmitters and voltage-controlled oscillator (VCO)-based transmitters. Although VCO-based transmitters have shown promise with respect to the elimination of discrete components [5], [6], they are fundamentally limited to constant-envelope modulation schemes. In contrast, I/Q modulator-based transmitters can operate with both constant and nonconstant envelope modulation, making them well suited for multistandard operation. To begin the discussion of I/Q modulator-based transmitters, a homodyne or direct upconversion transmitter is evaluated, followed by a discussion of the traditional heterodyne or indirect upconversion transmitter. Finally, a modified heterodyne transmitter is presented called the harmonic-rejection transmitter.

A. Direct-Upconversion Transmitter (Homodyne)

The direct-upconversion transmitter, shown in Fig. 1, is attractive because of the simplicity of the signal path. The in-phase (I) and quadrature (Q) baseband digital signals pass through a DAC and a baseband filter before the signal is upconverted to RF in a single step. The I and Q signals are then combined before passing through a pre-PA RF filter, a PA, and a second RF filter. Channel tuning is typically performed with a single RF channel-select frequency synthesizer. The shaded components in Fig. 1 would likely remain discrete if CMOS integration with low-Q components was attempted for a number of reasons. In particular, integrating a low-phase noise RF channel-select frequency synthesizer using low-Q components would be particularly difficult for narrow-band cellular standards such as GSM. This would lead to the use of a discrete VCO tank circuit to meet the required phase-noise performance with reasonable power consumption. Aside from the tank circuit, a discrete pre-PA RF filter is needed for two reasons. First, the filter reduces potential third-order intermodulation in the PA that could degrade modulation accuracy. This can be seen in Fig. 2 when the third harmonic of the desired signal intermodulates with the desired signal to produce an unwanted third harmonic of the baseband signal. The pre-PA RF filter is also needed to attenuate transmitted noise that in turn reduces the filtering requirement after the PA. This allows the use of a single filter after the PA with potentially lower loss than if a pre-PA filter was not used. Aside from the need for discrete components, the direct upconversion transmitter suffers from some well-known problems. First, the

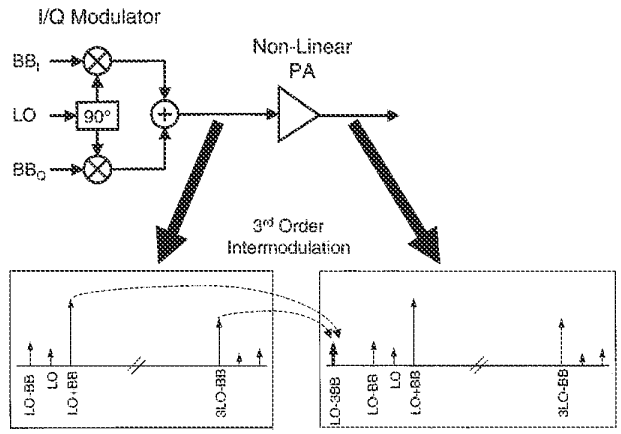


Fig. 2. Third-order intermodulation in PA.

local oscillator (LO) feedthrough is relatively large because of the high frequency used in the I/Q modulator. The second, and potentially more severe, problem is LO pulling which occurs because the transmitted signal is running at the same frequency as the LO. This condition would only get worse with PA integration. One method to reduce LO pulling is offset mixing [7], [8], but this technique does not address any of the other integration issues. To further improve transmitter performance, an indirect upconversion transmitter is often used.

B. Indirect Upconversion Transmitter (Heterodyne)

The indirect upconversion transmitter, shown in Fig. 3, can be viewed as the transmitter version of the superheterodyne receiver. Like the homodyne transmitter, an I/Q modulator is used; however, now the baseband signal is frequency translated to a fixed IF. The signal is then typically filtered to remove unwanted IF harmonics. The IF signal is then upconverted to RF before it passes through a pre-PA RF filter, the PA, and a final RF filter. Like the direct upconversion transmitter, channel tuning is performed with a single RF channel-select frequency synthesizer, and again, the shaded components would likely remain discrete if CMOS integration with low-Q components was attempted. In addition, yet another discrete component, the IF filter, has been added. Furthermore, little has been done to ease the requirements of the RF VCO tank circuit or the pre-PA RF filter. However, this transmitter does have a number of performance advantages. First, LO feedthrough is reduced because of the lower frequency used in the I/Q modulator, and second, LO pulling is reduced because neither oscillator is operating at the transmitted frequency. To further improve performance a modi-

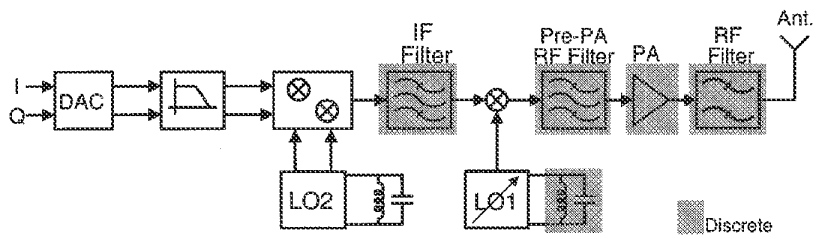


Fig. 3. Indirect upconversion transmitter block diagram.

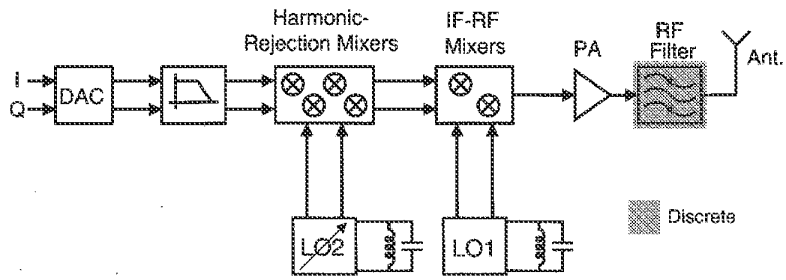


Fig. 4. Harmonic-rejection transmitter block diagram.

fied indirect-upconversion transmitter was used, called the harmonic-rejection transmitter.

C. Harmonic-Rejection Transmitter

The two-step transmitter shown in Fig. 4 is called the harmonic-rejection transmitter (HRT) because of the unique mixers used in the baseband to IF upconversion. This transmitter maintains the performance advantages of the traditional indirect upconversion transmitter in that both LO pulling and LO feedthrough are reduced. In addition, for reasons shown later, the dependency on discrete components has been reduced. For a given performance metric, removal of the IF filter and pre-PA filter may now be possible, as well as complete integration of the RF VCO tank circuit. Integration of the tank circuit is achieved by switching the roles of the synthesizers as compared to a conventional heterodyne transmitter. Channel tuning is now performed with the IF synthesizer while the RF synthesizer is fixed in frequency. By reversing the roles of the two synthesizers, the total phase noise of both synthesizers can be reduced when using low-Q on-chip components for the VCO tank circuitry.

The IF filtering requirement is relaxed by the use of HRMs for the baseband to IF upconversion. As previously mentioned, conventional switching mixers introduce relatively large harmonics at multiples of the IF frequency that require the use of a high-Q filter not amenable to CMOS integration. In contrast, the HRM not only frequency translates the baseband signal to IF but also avoids the need for a discrete filter by attenuating the third and fifth IF harmonics. This attenuation is achieved by effectively multiplying the baseband signal by a 3-bit, amplitude-quantized sinusoid. The details of the HRM will be discussed in more detail in Section III.

In addition to the relaxation of the IF filtering requirement, the requirements on the pre-PA RF filter have also been relaxed. The pre-PA filter is needed to reduce potential third-order intermodulation and to attenuate transmitted noise and spurs. Since the transmitted noise is typically dominated by the phase noise of the synthesizers, switching the roles of the synthesizers potentially allows for low-phase-noise integrated synthesizers which in turn reduce the pre-PA filtering requirement. Also, as previously mentioned, energy located at three times the carrier frequency can intermodulate and degrade the modulation accuracy. In an indirect upconversion transmitter, energy is generated at three times the carrier frequency from the 3LO2 × 3LO1 mixing product. However, due to the rejection of the third IF harmonic, third-order intermodulation is a less significant problem in the HRT. Consequently, the pre-PA RF filter is no longer needed to prevent significant third-order intermodulation. As a result, PA integration is now possible, because the RF filtering can be performed with one RF filter after the PA.

The next section will discuss some of the important details of the HRT, focusing on the HRM and frequency synthesizers.

III. Transmitter Details

A. Harmonic-Rejection Mixer

A key building block in the HRT is the harmonic-rejection mixer (HRM). Switching mixers are commonly used in RF transceivers because of their numerous advantages compared to other mixer topologies [9]. However, these mixers generate harmonics of the local oscillator frequency, which consequently need filtering. The top half of Fig. 5(a) shows a conventional switching mixer in which the baseband signal is effectively multiplied by a square-wave LO2 signal. The resulting upconverted signal now has relatively large copies of the baseband signal located at odd multiples of the LO frequency. Typically, a high-Q filter is needed to attenuate these copies. Alternatively, an HRM could be used to attenuate the third and fifth LO harmonics, reducing the IF filtering requirement. The fundamental concept of the HRM, shown in Fig. 5(b), is to multiply the baseband signal by a 3-bit, amplitude-quantized sinusoid, $f_{\mathrm{LO2h}}(t)$. Because the first harmonic of $f_{\mathrm{LO2h}}(t)$ is located

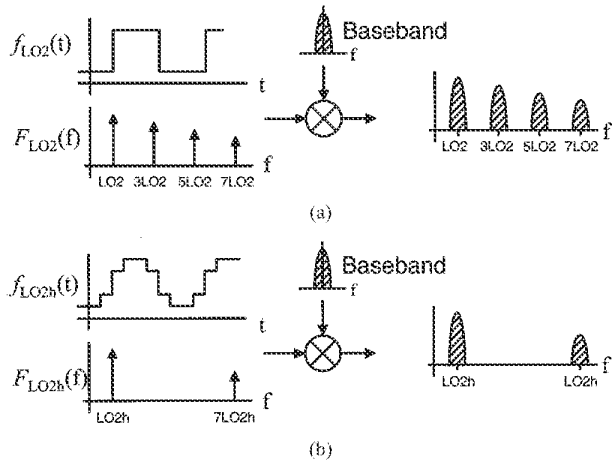


Fig. 5. (a) Conventional switching mixer. (b) Harmonic-rejection fundamentals.

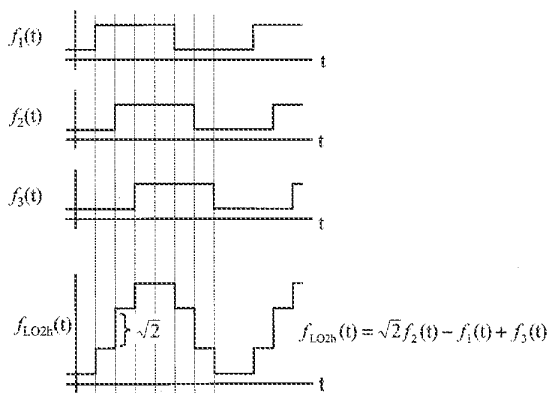


Fig. 6. Harmonic-rejection signal generation.

at seven times the fundamental frequency, the first significant copy of the upconverted baseband signal is also located at seven times the fundamental frequency. Consequently, the IF filtering requirement is greatly relaxed, leading to removal of the IF filter. The next challenge was to generate $f_{\mathrm{LO2h}}(t)$ while maintaining the advantages of using a current-commutating switching mixer. Current-commutating switching mixers allow for a relatively low LO swing, which is critical for integration using low-Q components.

To generate $f_{\mathrm{LO2h}}(t)$, three square waves are summed as shown in Fig. 6. To accurately represent a quantized sinusoid, the magnitude of $f_2(t)$ is scaled by $\sqrt{2}$. To better understand the rejection of the third and fifth harmonics, it is instructive to expand the three square waves using a Fourier series. The Fourier series representation of the three square waves up to the fifth-order component is given by

$$f_1(t) = \frac{\sqrt{2}}{\pi}\left[(\cos(\omega t) - \sin(\omega t)) + \frac{1}{3}(\cos(3\omega t) + \sin(3\omega t)) - \frac{1}{5}(\cos(5\omega t) - \sin(5\omega t))\ldots\right] \quad (1)$$

$$f_2(t) = \frac{2}{\pi}\left[\cos(\omega t) - \frac{1}{3}\cos(3\omega t) + \frac{1}{5}\cos(5\omega t)\ldots\right] \quad (2)$$

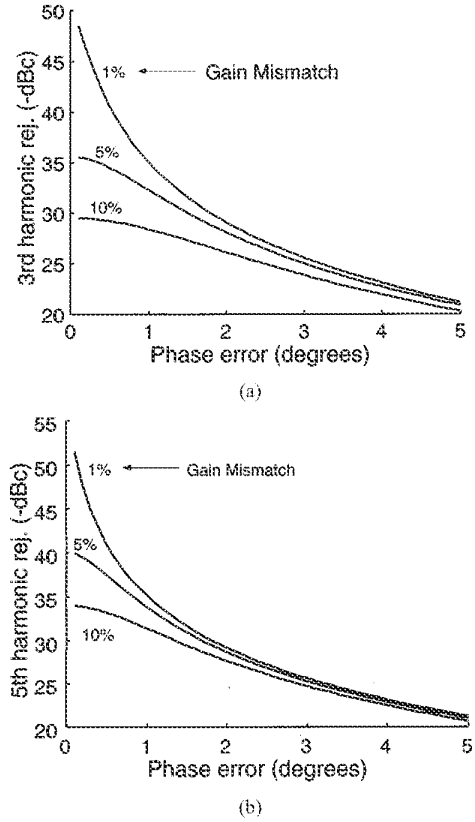


Fig. 7. Harmonic-rejection with mismatch. (a) For third harmonic. (b) For fifth harmonic.

$$f_3(t) = \frac{\sqrt{2}}{\pi}\left[(\cos(\omega t) + \sin(\omega t)) + \frac{1}{3}(\cos(3\omega t) - \sin(3\omega t)) - \frac{1}{5}(\cos(5\omega t) + \sin(5\omega))\ldots\right]. \quad (3)$$

Summing the three ideal square waves with $f_2(t)$ scaled by $\sqrt{2}$ results in the total rejection of the third and fifth harmonics. However, similar to a single-sideband mixer, gain and phase mismatch result in nonideal cancellation of the third and fifth harmonics. The rejection of the third and fifth harmonic are given by

$$\mathrm{HRM}_3 = \left(\frac{1}{9}\right)((1 - \cos(3\theta)(1+\Delta))^2 + ((1+\Delta)\sin(3\theta))) \quad (4)$$

$$\mathrm{HRM}_5 = \left(\frac{1}{25}\right)((1 - \cos(5\theta)(1+\Delta))^2 + ((1+\Delta)\sin(5\theta))) \quad (5)$$

where Δ is the gain mismatch and θ is the phase mismatch. The rejection depends strongly on the phase error in the original signal. Shown in Fig. 7 is the harmonic rejection plotted as a function of phase error for different gain errors. Fig. 7(a) shows the rejection of the third harmonic while Fig. 7(b) shows the rejection of the fifth harmonic. Note that as the phase and gain error increase the rejection of the third harmonic approaches 9.5 dBc while the rejection of the fifth harmonic approaches 14 dBc, which are the levels of an ideal square wave. For one-

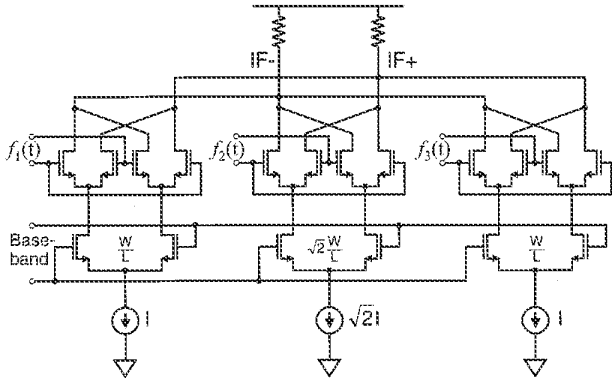


Fig. 8. Harmonic-rejection mixer circuit diagram.

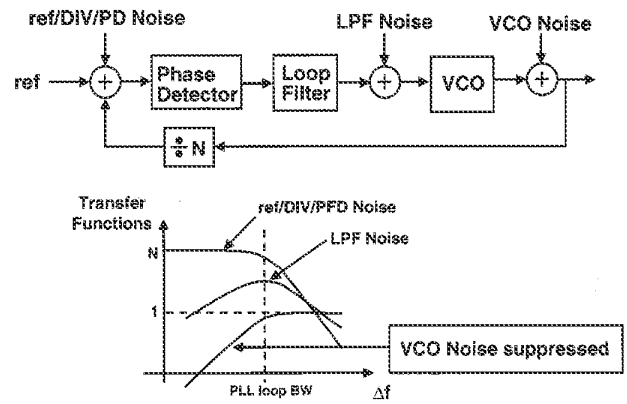


Fig. 9. VCO phase-noise suppression in wide-loop-bandwidth PLL.

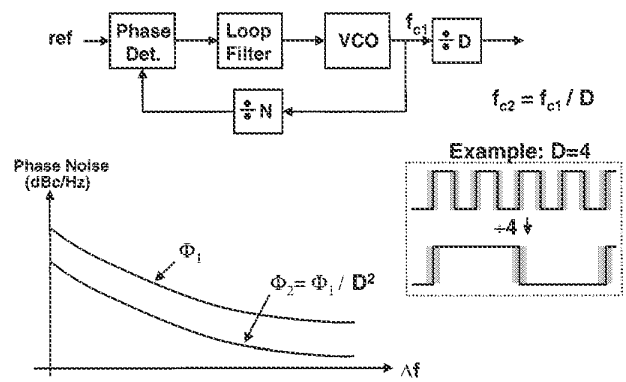


Fig. 10. Phase noise of low-frequency synthesizer.

degree phase error and 1% matching, approximately 35 dB of rejection is achieved for both the third and fifth harmonics.

To implement the HRM, each square wave, $f_1(t)$, $f_2(t)$, and $f_3(t)$, is mixed with the baseband signal and then the three outputs are summed. The advantage of this approach is that a low-noise switching mixer can now be used. However, a potential disadvantage is that scaling the LO voltage, by $\sqrt{2}$ in this case, will not proportionally scale the output voltage swing. The simplified circuit schematic for the HRM is shown in Fig. 8. The HRM consists of three current-commutating submixers. The transconductance stage of each submixer is driven with the identical baseband signal. However, the switches are driven by the three phase-shifted square waves. The current output of the three submixers is summed to generate the final output signal. Consequently, the baseband signal is effectively multiplied by a 3-bit amplitude-quantized sinusoid. To scale $f_2(t)$ by $\sqrt{2}$, the current switched in the middle submixer was increased by $\sqrt{2}$ by scaling the tail current source. Furthermore, to maintain an equivalent linearity performance in the three submixer transconductance stages, the input transistors were also scaled in the middle submixer to give a V_{dsat} that is equal in the three submixers.

B. Frequency Synthesizers

This transmitter architecture offers advantages with respect to full integration of the frequency synthesizer with on-chip low-Q VCOs. As previously mentioned, channel tuning is now performed with the low frequency synthesizer while the RF synthesizer is fixed in frequency. This achieves lower phase noise than the standard configuration because it allows for the use of a wide loop bandwidth for the RF synthesizer.

Performing channel-tuning with the lower frequency IF synthesizer allows the RF synthesizer to have an extended loop bandwidth, which has the effect of suppressing the close-to-carrier phase noise produced by the VCO. This may be better understood by evaluating the phase-noise transfer functions of the various components within a PLL to the output of the synthesizer, as illustrated in Fig. 9. Here, the phase-noise transfer function from the VCO to the PLL output has a high-pass characteristic relative to the carrier. Because the channel tuning is performed using the lower frequency IF synthesizer, the comparison frequency of the RF synthesizer can be significantly raised, by as much as a few orders of magnitude. Typically, for reasons related to the stability of a second-order PLL, the loop bandwidth must be anywhere from a fourth to a tenth of the comparison frequency. Therefore, the higher comparison frequency allows an increased loop bandwidth for the RF synthesizer, significantly extending the close-to-carrier bandwidth where VCO phase-noise suppression will occur. The overall RF synthesizer close-to-carrier phase-noise performance can then be designed such that the phase-noise performance is no longer dominated by a noisy integrated VCO using low-Q components in the tank circuit.

Although the lower frequency synthesizer must now perform channel tuning, lower phase noise, relative to the carrier power, can inherently be achieved due to the lower operating frequency. In this transmitter system, narrow channel tuning must be performed. Consequently, the maximum reference frequency and PLL loop bandwidth are limited, ultimately reducing the band of close-to-carrier VCO phase-noise suppression. The concept of inherently lower phase noise at lower frequencies may be understood with a time-domain interpretation, which is illustrated in Fig. 10. Assume for the moment that the PLL used to synthesize the channel spacing required by a narrow-band system produces an output at RF, instead of IF (again, the loop bandwidth would be small). If the output of this synthesizer is divided down to the IF frequency, there is an inherent lowering in both the rms jitter and phase noise as compared to the carrier.

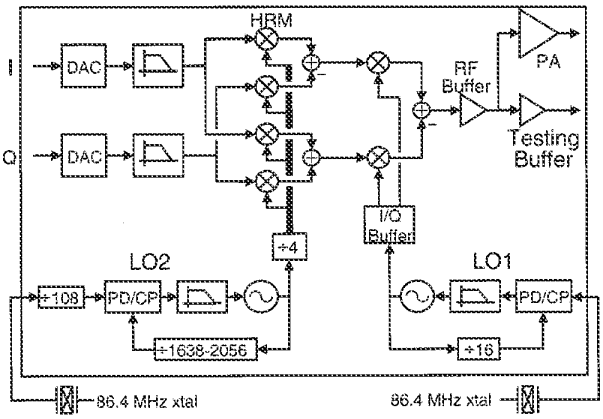


Fig. 11. CMOS prototype HRT block diagram.

This is illustrated in Fig. 10 for $D = 4$, where the time-domain waveform at the output of the synthesizer is shown at the bottom. Before the divider, each edge of the waveform contains jitter, resulting from noise generated inside the PLL. If it is assumed that an idealized noiseless divider is used to lower the frequency by a divider ratio D, then the divider will only capture the timing jitter from one of D edges, yet the period of the fundamental waveform increases by a factor of D. Stated differently, the rms timing jitter on the lower frequency LO, at the divider D output, will have the same timing jitter on each edge, however, the period of the waveform is increased by a factor of D. Thus, the jitter relative to the fundamental period has decreased by a factor D. For close-to-carrier phase noise, the timing error created from edge to edge is correlated at the output of the divider. Because of this correlation in timing error from edge to edge, the effect of a noiseless divider is to reduce the close-to-carrier phase noise by the square of the division ratio, in this case D. In the actual implementation of the IF synthesizer used in the transmitter prototype, the channel-tuning synthesizer produces an output in the range of 1.3104 to 1.4704 GHz, in 800-kHz steps. The IF synthesizer output is then divided down by a factor of 4; thus, the close-to-carrier phase noise produced at the output of the synthesizer is reduced by a factor of 16.

The RF synthesizer used by this prototype transmitter has been previously described in [10] and realizes a 1.3824-GHz oscillator with a loop bandwidth of 8 MHz. The IF synthesizer produces frequencies from 327.6 to 367.6 MHz in 200-kHz steps and has a 40-kHz loop bandwidth.

IV. CMOS Prototype

A CMOS prototype HRT was fabricated in a 0.35-μm double-poly five-layer metal process. A block diagram of the HRT is shown in Fig. 11. The HRT integrated the entire transmit signal path from the DACs to the PA, including two frequency synthesizers. Ten-bit digital I and Q baseband signals are brought on chip and passed through two 10-bit resistor string DACs and then filtered by two Sallen & Key third-order low-pass filters. The signals are then upconverted to a variable IF using four HRMs. Four mixers are used to provide image rejection for the baseband signal and to generate both I and Q IF signals. The IF signals are then upconverted to RF using

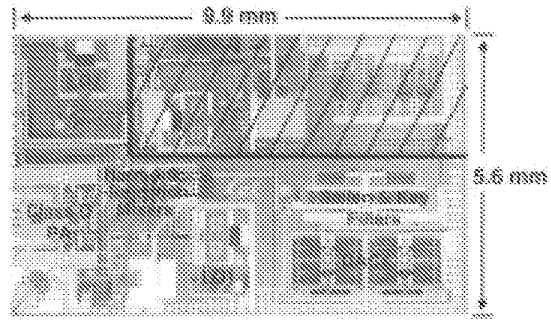


Fig. 12. Die photo.

two inductively loaded current-commutating mixers. The RF signal is then buffered before being driven off-chip with either a testing buffer or an integrated class-C PA. The testing buffer is capable of driving 0 dBm into 50 Ω, while the PA is capable of delivering 25 dBm. A die micrograph is shown in Fig. 12.

With the high level of integration implemented in this work, coupling between circuits and circuit blocks can severely degrade performance. The chip was fabricated in an epitaxial process; the epitaxial layer had a resistivity of 10 Ω·cm, while the substrate had a resistivity of 0.01 Ω·cm. With such a low substrate resistivity, it is quite possible that large signals injected into the substrate from the digital circuits or from the power amplifier (PA) can couple back into the sensitive analog sections. To reduce the effects of substrate coupling, three general techniques were used throughout the chip. First, a fully differential signal path was used from the output of the DACs through the output of both the PA and the testing buffer. Ideally, a differential circuit will see coupling from the substrate, due to other circuit blocks, as common-mode noise, and will reject those signals. Both frequency synthesizers were also implemented in a fully differential fashion, including the VCO control voltages. Differential control voltages were used to maximize the immunity of the frequency synthesizers to coupling through the substrate, from other blocks as well as each other. Second, independent supplies, which were heavily bypassed both on and off chip, were used for each of the circuit blocks. This was done so that the local supply and ground would move together; any voltage fluctuations on either the ground or supply nodes would ideally not impact the signals as they moved through the signal path. Third, multiple substrate contacts were placed around the transistors so that the body would move in unison with the local supply and ground. Therefore, any substrate coupling would also be coupled into the supply and ground local to a given circuit block, and would therefore minimize the effect of that coupling on the differential signal path.

To better understand the circuit implementation, a more detailed description of some of the key circuit blocks will follow. The blocks to be discussed include the DAC, the Sallen & Key filter, the RF quadrature generator, and the PA.

A. DAC

Fig. 13 shows the basic structure of the resistor string DAC used in the transmitter. The digital-to-analog conversion is made

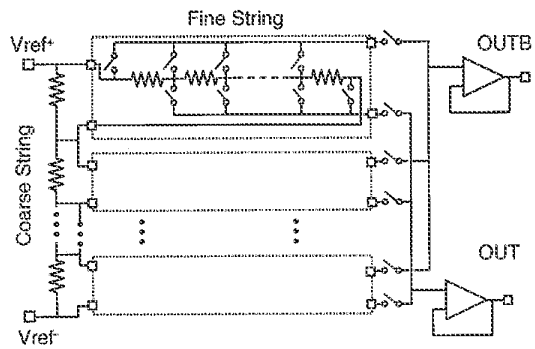


Fig. 13. Dual resistor string DAC schematic.

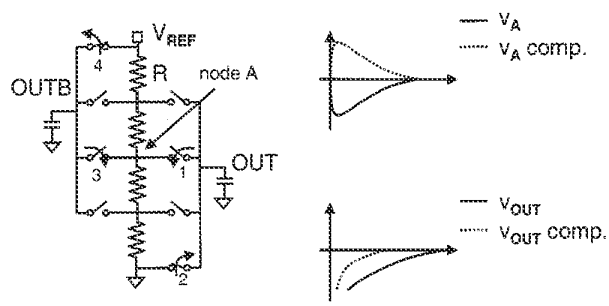


Fig. 14. Glitch reduction circuit technique for DAC.

in two steps using two 5-bit resistor strings that select the appropriate output analog level. In the design of a resistor-string DAC, there is usually a tradeoff between the maximum speed of the DAC and its power consumption. As the total value of the resistance in the resistor string increases, the overall power consumption is reduced, but the time needed for the output voltage to settle is also increased. A critical factor in the settling time is the issue of capacitive coupling between the output and the intermediate nodes in the resistor string. The intermediate nodes in the resistor string should stay at a fixed voltage at all times, but as switches close and open and different intermediate nodes are tied to the output, there is an instantaneous change on the intermediate nodes (for example, node A in Fig. 14) that causes an increase in the settling time of the output. This problem can be reduced through the use of a set of replica switches and a dummy capacitor, as shown in Fig. 14. Switches 3 and 4 switch in opposition to switches 1 and 2, respectively, and thereby induce an equal and opposite effect on the intermediate node voltage A. The uncompensated voltage at node A is summed with the glitch reduction due to the switches 3 and 4, resulting in a reduced fluctuation voltage at node A, as shown in Fig. 14. This allows the voltage at the output to settle more quickly to its desired value; furthermore, in simulation, the power consumption can be reduced as much as 30% for a given settling time. Moreover, the use of complementary switches performs the operation of single-ended to differential conversion. In the actual implementation, the function of the dummy capacitor was performed with the complementary output buffer.

B. Sallen & Key Filter

After the DACs, the I and Q baseband signals are filtered before upconversion. The filtering is performed with a third-order Sallen & Key low-pass filter. The filter uses a buffer in the feedback path to improve the rejection. Shown on the left side of Fig. 15 is a conventional Sallen & Key filter. The feedback capacitor C_1 introduces a zero in the transfer function which decreases the attenuation at higher frequencies. However, the wide-band noise is critical in transmitters, because it may corrupt the highly sensitive receivers nearby. One method of improving the attenuation, at the cost of increased power, is to increase the bandwidth of the forward buffer used in the filter. Alternatively, the effect of the zero may be reduced by adding a buffer in the feedback path as shown in the right side of the Fig. 15. The buffer blocks the zero introduced by the capacitor allowing for a lower bandwidth in the forward buffer. The plot shows the expected attenuation for the two configurations with equal power consumption. At higher frequencies, approximately a 30-dB improvement in the high-frequency attenuation is predicted by simulation with the feedback amplifier, as compared to a conventional Sallen & Key filter consuming equal power.

C. RF Quadrature Generator

The amount of sideband suppression obtained by an image-rejection mixer is highly dependent on the phase accuracy of the I and Q LO signals. For this transmitter system, the quadrature accuracy of the I and Q LO signals further relax the RF filtering requirement of the IF image. Additional and specific requirements of the quadrature generation circuitry used by this transmitter are that both the loading at the output of the synthesizer (or VCO) and the degradation in the VCO tank Q be minimized. Traditional methods of generating quadrature from a single phase include frequency dividers and passive filters realized with resistors and capacitors. The first LO (RF synthesizer) directly generates the frequency required for upconversion by the corresponding mixers, eliminating the possibility of using a frequency divider to generate quadrature LOs. Two common passive filter approaches include using an RC-CR filter or an asymmetric polyphase filter [11]. These passive methods for generating quadrature suffer from a variety of drawbacks, which can include both phase and amplitude frequency dependence, phase error from either component mismatch or process variations, and loss in LO carrier power.

Despite the well-known problems, polyphase filters are still an effective method for generating highly accurate quadrature signals from a single phase. However, there are several mechanisms of loss in this filter that typically require power-consuming buffers at the input and output of the filter. Polyphase filters generate quadrature from a single phase by passing the signal through multiple stages of an RC network when the signal frequency is near the 3-dB frequency of the RC network. Other contributing factors to loss in a polyphase filter include the parasitics associated with bottom plate capacitance used to create the capacitors. If the output is directly coupled to the mixer input, then an ac-coupling capacitor might be needed, which introduces additional parasitics and loss in LO carrier power.

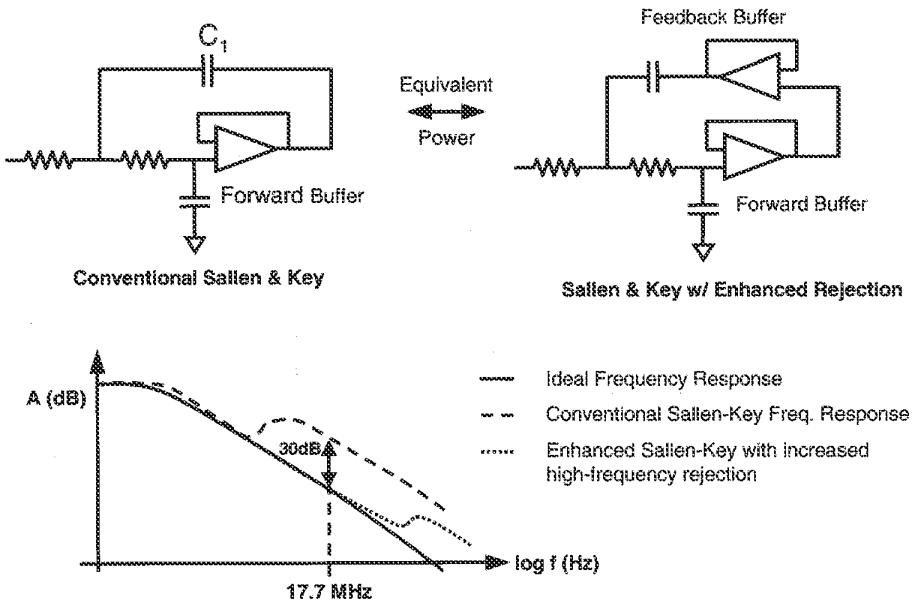
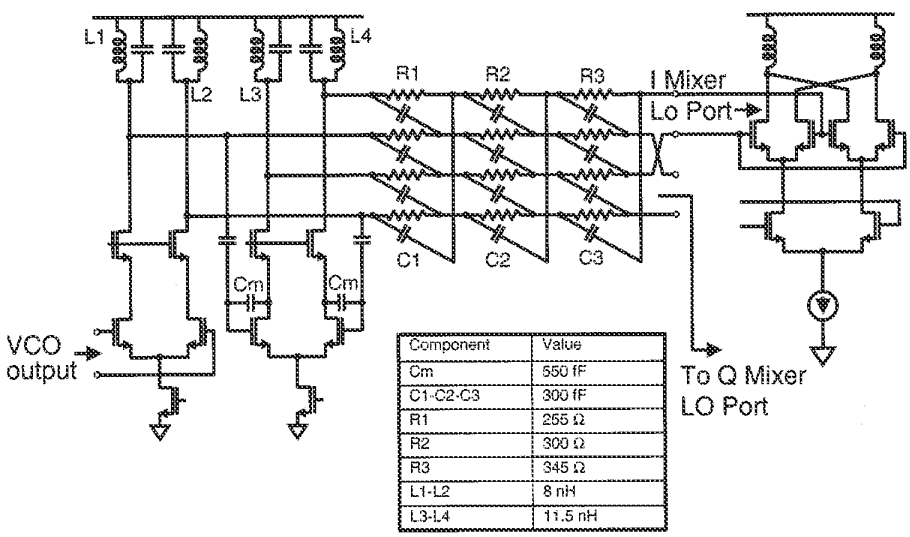


Fig. 15. Improved rejection from Sallen & Key filter.



Component	Value
Cm	550 fF
C1-C2-C3	300 fF
R1	255 Ω
R2	300 Ω
R3	345 Ω
L1-L2	8 nH
L3-L4	11.5 nH

Fig. 16. High-frequency (LO1) VCO buffer quadrature generator circuit schematic.

The circuit shown in Fig. 16 reduces one mechanism of loss in the polyphase filter by using a buffer which drives the input of the filter with signals roughly in quadrature and thus eliminates the inherent 3-dB loss associated with converting a single phase to quadrature phases. Two common source buffers before the polyphase generate signals which are roughly 90° out of phase at the inductively loaded nodes when the operating frequency is near the g_m/C_m of the second buffer [12]. In addition, the input impedance looking into the buffer is capacitive with the exception of the gate resistance r_g, therefore minimizing the reduction in the VCO tank Q and loading. The Q of the LC tank at the buffer output, shown as L1-L4 in Fig. 16, is approximately 1.5 when loaded with the polyphase filter. The mixer LO input was designed to have a common mode at V_{dd} and thus the need for an ac-coupling capacitor has been eliminated as well as its associated loss.

D. Power Amplifier

Previous sections detailed the transmitter architecture, including the benefits of the harmonic rejection architecture with respect to the filtering required before the PA. These benefits allow for the use of an integrated highly nonlinear PA when a constant-envelope modulation scheme is used. Recent efforts that have investigated nonlinear PAs have focused primarily on switch-mode nonlinear PAs, such as class-D and class-E PAs [13], [14]. One drawback to switch-mode PAs, especially with respect to their potential for integration, is the need for a dc–dc converter in order to perform power control, which is

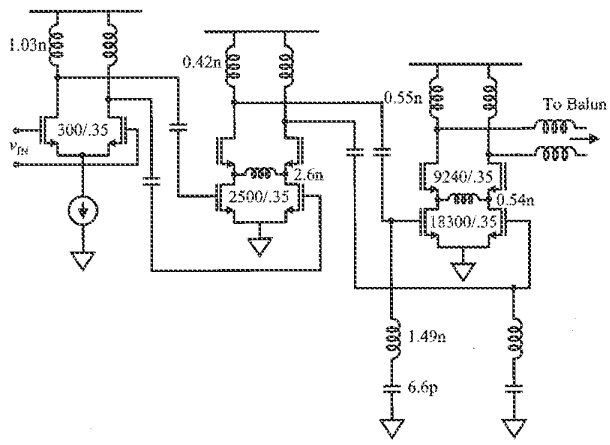


Fig. 17. Class-C power amplifier circuit schematic.

required in most cellular communications systems. In general, the only way to vary the output power level of a switch-mode PA is to vary the power supply; thus the need for the dc–dc converter, which can be difficult to integrate. Therefore, a different solution was explored.

In this work, a class-C architecture was used for the PA. The class-C architecture is an extension of the class-A and class-B architectures. In the class-C architecture, the angle of conduction (the portion of the cycle when the device is on) is less than 180°; the device is biased such that it is off for more than one-half the cycle by setting the dc bias below the threshold voltage of the device. Consequently, the input signal turns the device on for only a fraction of the period. This reduction in the period when the device conducts current serves to reduce the power consumed in the device and thus potentially raises the efficiency of the PA.

In the design of submicron CMOS PAs, a key limitation is the oxide breakdown voltage, which limits the available voltage swing at the drain of the transistor. As a result, the load impedance seen by the device needs to be extremely low in order to deliver the required amount of power without damaging the device. Furthermore, the current level must rise in proportion with the reduced voltage swing. Since CMOS generally has a poor transconductance when compared with silicon bipolar or Gallium Arsenide technologies, the device sizes required can be quite large in order to generate the required output power.

Fig. 17 shows the circuit diagram of the three-stage fully differential class-C PA used in this work. The stages are ac-coupled in order to allow the input device of each stage to be biased independent of the output of the previous stage. Since the PA was to be used in an integrated environment, the previous stages would likely not be able drive a heavy load; therefore, three stages were used in order that the first stage would not load down the output of the mixer. The first stage was biased in a class-A fashion, with a variable tail current source that controls the gain and thus the output power level. The final two stages are biased in a class-C fashion and use a cascode structure with the top devices biased at the supply in order to reduce the stress on the oxide due to voltage excursions at the outputs of those stages. At the input to the final stage, a different tuning technique was used to peak the gain at the desired frequency. Due to the high current drive required and the poor transconductance of CMOS, the output transistor size was extremely large (18 300 μm/0.35 μm); using a single spiral inductor to tune out all the capacitance between the second and third stages required an extremely small value inductor (on the order of 0.1 nH). That inductor was quite difficult to implement without parasitic trace inductance affecting the tuning at that node. Instead, a series LC was used in parallel with the gate capacitance of the final stage in order to provide a peaking of the impedance at that node. Furthermore, inductors were used across the differential cascode node in the second and third stages, in order to reduce the current required to charge and discharge the capacitors at those nodes and boost the efficiency. The inductors used at the output of the first and second stages as well as those at the cascode nodes were implemented as spiral inductors on chip; the other inductors used in this circuit were implemented as bond wires, in order to take advantage of their higher Q. The inputs of the second and third stages were biased at 0.35 V with a bias voltage generated on chip.

V. Results

Although the HRT was designed to facilitate multistandard operation, the performance of the transmitter was tested with the DCS 1800 specifications. This up-banded version of GSM was chosen for a number of reasons. First, it requires very high modulation accuracy from the transmitter. Second, DCS 1800 requires very low unwanted spurious transmission especially in the receive band. Finally, DCS 1800 uses a constant envelope modulation scheme making it well suited for use with a highly nonlinear class-C power amplifier.

A. Measured Results With Testing Buffer

The results in this section were measured using a testing buffer after the mixers, in parallel with the PA, as opposed to the PA itself. The next section will compare some of this data when the measurements were taken at the output of the PA instead of the testing buffer.

A critical test for all transmitters is the single-sideband test in which a single baseband tone is upconverted to RF. Although I/Q modulator-based transmitters are ideal for multistandard operation, gain mismatch and phase error in the modulator generally limit the modulation accuracy. Shown in Fig. 18 is the output of the transmitter when a 50-kHz baseband tone is upconverted to RF. The unwanted image suppression was measured at −56 dBc, implying that the gain and phase were matched very well throughout the transmitter. This was accomplished with careful layout techniques and the measurement transmitter has no external tuning. The carrier suppression was measured at −38 dBc while the third-order distortion was measured at −46 dBc. The third-order distortion was dominated by the baseband inputs of the HRMs.

Another key transmitter performance test is measuring the output when a modulated baseband signal is used as opposed to a single tone. Typically, different RF standards provide a spectral mask under which the transmitted signal must fall. Meeting

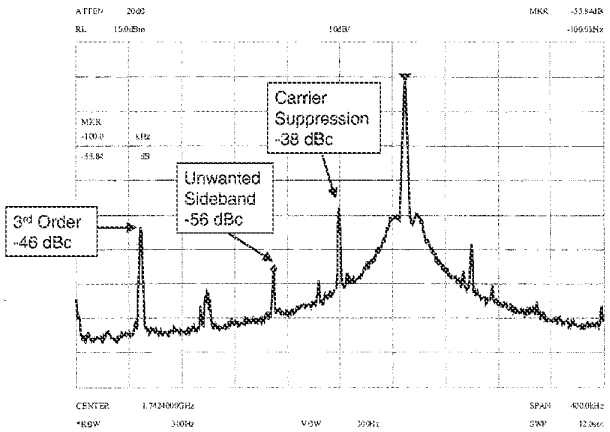


Fig. 18. Transmitter output with single-sideband test.

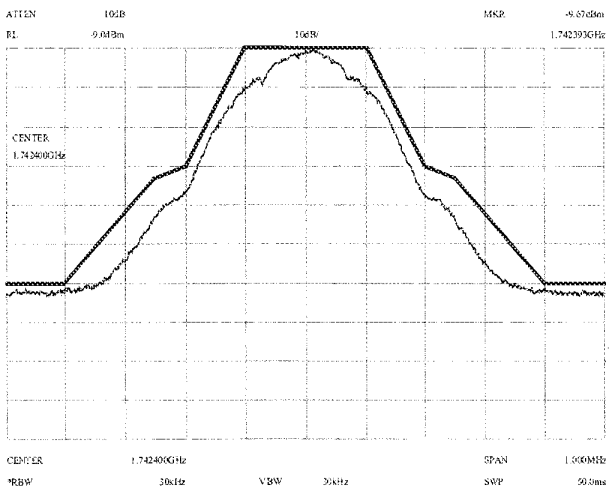


Fig. 19. Transmitter output with modulated baseband signal.

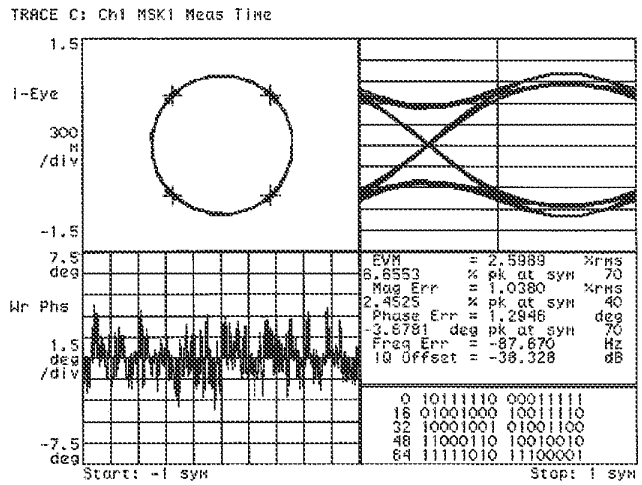


Fig. 20. Modulation accuracy of transmitter.

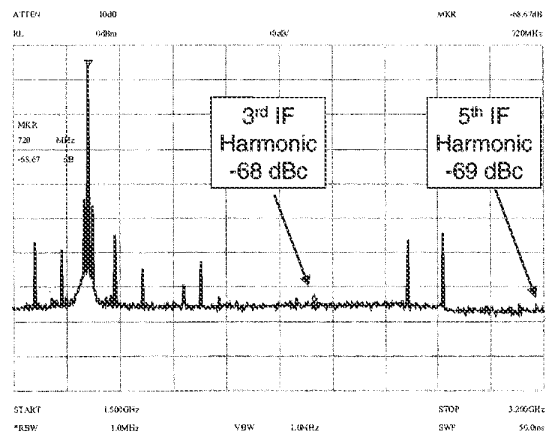


Fig. 21. Wide-band spectrum at transmitter output.

this specification requires low phase noise from the frequency synthesizer and high linearity in the baseband circuits. To test the HRT a DCS 1800 GMSK modulated baseband signal was used. Shown in Fig. 19 is the measured output spectrum along with the DCS-1800 spectral mask requirement. The measured results are limited by the phase noise of the frequency synthesizers.

Although the spectral mask limits the transmitted noise and unwanted spectral emissions, it does not measure the modulation accuracy. This test is typically performed using a modulated baseband signal and comparing the transmitted signal with the ideal signal. The DCS-1800 standard requires that the rms phase error is less than 5° with a peak phase error no larger than 20°. The measured results for the HRT are shown in Fig. 20 and the rms phase error is 1.3° while the peak phase error is 3.7°. This error was probably caused by the nonidealities in the I/Q modulator along with the phase noise of the synthesizers.

In addition to the close-in spectral mask requirements, DCS 1800 limits the unwanted transmissions that could potentially fall in the receive band. Consequently, the limit for the transmitted noise measured at 20-MHz offset from the carrier is −151 dBc/Hz. This transmitter was measured at −126 dBc/Hz. This noise was primarily caused by the phase noise of the frequency synthesizers. To meet the DCS 1800 specification, an RF filter is needed with 25 dB of attenuation at a 20-MHz offset. Such attenuation is achievable with a single RF filter allowing for a highly integrated transmitter requiring only one filter afterwards.

Finally, as a test of the HRM, a wide-band output spectrum was measured. The results are shown in Fig. 21. The suppression of the third IF harmonic was measured to be −68 dBc while the fifth IF harmonic suppression was measured to be −69 dBc. Although the third IF harmonic was further suppressed by the IF–RF image-reject mixer, the fifth IF harmonic was only suppressed by the HRM. The third IF harmonic on the low side of the carrier frequency was only suppressed by the HRM, and it was below the noise floor of the spectrum analyzer.

B. Measured Results With PA

The transmitter was also tested with the class-C PA. Shown in Fig. 22 are the results of a single-sideband test using the same 50-kHz signal. The test setup introduced approximately 2 dB of

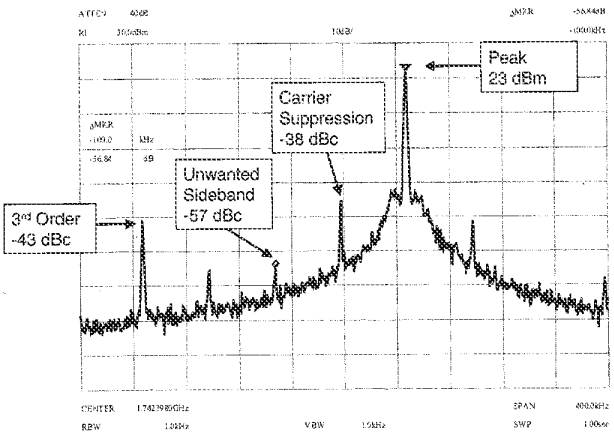


Fig. 22. Single-sideband test with PA output.

TABLE I
SUMMARY OF MEASURED RESULTS

VDD = 3 Volts Temp.= 25°C

	Testing Buffer	PA
Single Sideband Suppression	-56 dBc	-57 dBc
LO2 3rd Harmonic Spur	-68 dBc	-68 dBc
LO2 5th Harmonic Spur	-69 dBc	-69 dBc
IF Image Suppression	-60 dBc	-60 dBc
RF Carrier Suppression	-38 dBc	-38 dBc
RMS Phase Error	1.3°	N/A
Peak Phase Error	3.7°	N/A
20 MHz Carrier Offset Noise	-126 dBc/Hz	-121 dBc/Hz
3rd Order Distortion	-46 dBc	-43 dBc
Output Power	0 dBm	25 dBm
Active Chip Area	20 mm²	24 mm²
Technology	0.35 µm DP-5M CMOS	0.35 µm DP-5M CMOS

loss between the output of the PA and the measurement equipment. The differential to single-ended conversion was accomplished using a microstrip balun similar to the balun described in [14]. Comparing Fig. 22 with Fig. 18 shows very little difference. The integrated PA had little effect on the transmitter output when a single-sideband test was performed. Furthermore, although not shown here, the wide-band spectrum also showed little change compared to the wide-band output measured at the testing buffer. Although the integrated PA had little effect on the modulation performance, the noise at 20-MHz offset was affected by the PA. As previously mentioned, the noise measured with the testing buffer was −126 dBc/Hz while the noise measured with the PA was −121 dBc/Hz. Substrate coupling is the likely cause of the increased noise.

The integrated class-C PA was designed for 1.5-W peak power and was tested as standalone component. The peak measured power of the standalone PA was measured at 1.2 W. This power was not achieved in the integrated version because of the lower than expected gain in the transmitter. This was due to lower than expected Qs for the on-chip spiral inductors which are critical for gain.

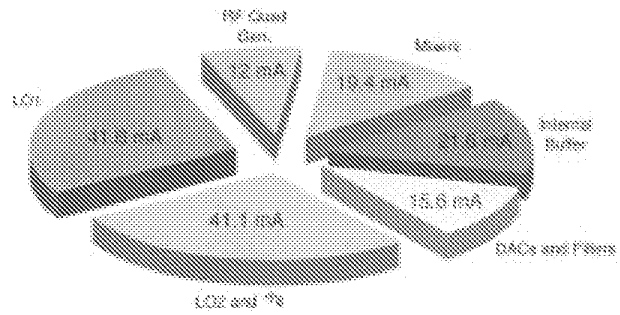


Fig. 23. Transmitter current consumption.

C. Results Summary

A summary of the measured results is shown in Table I. The table shows the results when measured with the testing buffer and the PA. Shown in Fig. 23 is the power consumption of the transmitter excluding the testing buffer and the PA. The lower than expected Qs negatively impacted the power consumption. The current for certain circuit blocks was increased to achieve the desired output power. Because the gain was lower than expected in the transmit path, the power output and the efficiency of the PA were significantly lower than expected.

VI. CONCLUSION

A fully integrated CMOS transmitter has been demonstrated. The entire transmit signal path including the PA and the frequency synthesizers were integrated in a 0.35-μm double-poly five-layer metal CMOS process. The transmitter demonstrated cellular performance requiring only a single RF filter after the PA. The need for pre-PA filtering was removed through the use of a harmonic-rejection transmitter and a wide-loop-bandwidth RF synthesizer. The performance met many of the key requirements of DCS 1800, an up-banded version of GSM. Furthermore, due to careful planning, the effect of on-chip coupling was minimized. This was evident by the fact that the chip incorporated two frequency synthesizers, two DACs, and a 25-dBm PA. Furthermore, the PA had a minimal effect on the performance when the PA output was compared to the output from a post-mixer testing buffer.

ACKNOWLEDGMENT

The authors would like to thank STMicroelectronics for their support and for chip fabrication services. Further, the authors are grateful to Agilent Technologies, Atmel, Conexant Systems, National Semiconductor, Nokia Mobile Phones, Nortel Networks, and Philips Research for their valued contributions.

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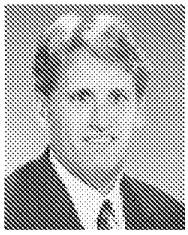
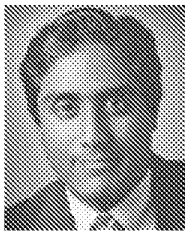


Jeffrey A. Weldon received the B.S. degree from the University of California, Berkeley, in engineering physics in 1992. He is currently working toward the Ph.D. degree at the University of California, Berkeley, in the Electrical Engineering and Computer Science Department, where he is studying analog circuit design for RF applications.

His research focuses on wireless transmitter architectures well suited for high levels of integration in CMOS. In addition, he is investigating CMOS mixers for wireless applications.

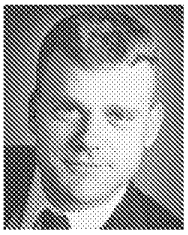
Mr. Weldon was a co-recipient of the 1998 ISSCC Jack Kilby Best Student Paper Award.



R. Sekhar Narayanaswami was born in Lubbock, TX, on November 5, 1971. He received the B.S. and M.S. degrees in electrical engineering and computer sciences in 1993 and 1998, respectively, both from the University of California, Berkeley. He is currently working toward the Ph.D. degree in the area of RF analog circuit design in CMOS technologies.

His research focuses on the implementation and integration of RF power amplifiers for mobile devices in CMOS technologies.

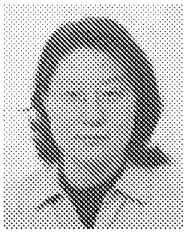
Mr. Narayanaswami is a member of Tau Beta Pi and Eta Kappa Nu.



Jacques C. Rudell (S'96–M'00) received the B.S. degree in electrical engineering from the University of Michigan, Ann Arbor. In his junior year, he was dedicated a James B. Angell Scholar. After graduation, he spent two years as an IC Designer and Project Manager at Delco Electronics, Kokomo, IN. While at Delco, his work focused mainly on bipolar analog circuits for automotive applications. In 1991, he returned to graduate school at the University of California, Berkeley. He received the M.S.E.E. degree in 1993, focusing on high-speed low-power digital adaptive equalization techniques for magnetic disk-drive channels employing class-IV partial response. Also at the University of California, Berkeley, he received the Ph.D. degree in 2000, focusing on wireless receiver architectures and systems suitable for high levels of integration in CMOS as well as multistandard/modal operation.

He worked as a Post-Doctoral Researcher at the University of California, Berkeley, in the spring of 2000. Currently, he is an Independent Consultant in Silicon Valley.

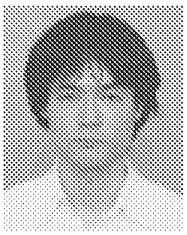
Dr. Rudell is a member of Tau Beta Pi and Eta Kappa Nu. He received the 1998 ISSCC Jack Kilby Best Student Paper Award. In 1999, he received the UC Berkeley EECS Demetri Angelakos Memorial Achievement Award.



Li Lin received the B.S. degree in electrical engineering from Portland State University, Portland, OR, in 1994, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1996 and 2000, respectively.

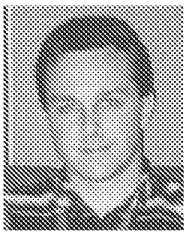
Since 2000, she has been with Broadcom Corporation, San Jose, CA, where she is a Staff Scientist working on RF integrated circuit design for wireless communication.

Dr. Lin is a member of Eta Kappa Nu and Tau Beta Pi.



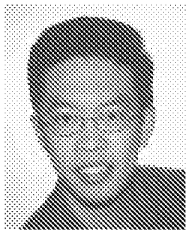
Masanori Otsuka was born in Saitama, Japan, in 1965. He received the B.S. and M.S. degrees in electrical engineering from the Science University of Tokyo, Tokyo, Japan, in 1989 and 1991, respectively.

In 1991, he joined Central Research Laboratory, Hitachi Ltd., Tokyo, and moved to Semiconductor and Integrated Circuits Division in 1995, where he has been engaged in developing CMOS D/A and A/D converters. From 1997 to 1998, he was a Visiting Industrial Fellow in Dr. P. Gray's research group at the University of California, Berkeley. During his stay, he investigated D/A converters for wireless systems.



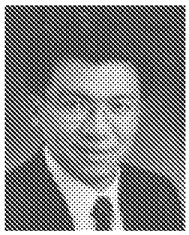
Sebastien Dedieu received the DESS of Microelectronic and the DEA of Electronic degrees from the University of Bordeaux, France, in 1993.

From 1993 until 1998, he was with STMicroelectronics Central R&D, France, as an Analog Design Engineer in the field of phase-locked loops and clock recovery for ATM (SDH/SONET) and GSM/DCS1800 applications. From 1998 to 1999, he was a Visiting Industrial Fellow in Dr. P. Gray's research group at the University of California, Berkeley. During his stay, he implemented a variable gain amplifier and active filters for a fully integrated RF transceiver. Since 1999, he worked at STMicroelectronics, Crolles, France, on phase quadrature locked loop for digital and cable TV receivers. He is currently developing synthesizers for HiperLAN/2 and 802.11applications. His research interests include mixed RF and analog VLSI circuit design in wireless and cable communications.



Luns Tee (S'93) received the B.A.Sc. degree in engineering science from the University of Toronto, Toronto, ON, Canada, in 1995. He is currently working toward the Ph.D. degree in electrical engineering at the University of California, Berkeley.

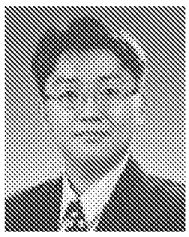
He is currently investigating transmitter linearization techniques for portable wireless applications.



King-Chun Tsai (S'95) received the B.S. degree in electrical engineering from Boston University, Boston, MA, in 1994. He is currently working toward the Ph.D. degree in electrical engineering at the University of California, Berkeley.

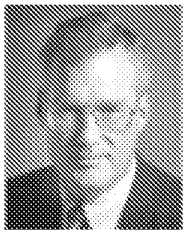
He has been a Teaching Assistant in a number of circuit design classes at the University of California, Berkeley. In the summer of 1998, he was with the Silicon Circuits Research Department at Bell Laboratories, Lucent Technologies, where he conducted research in microwave balun design. He joined Marvell Semiconductor Inc. in 2001, where he continued his work in designing RF ICs for wireless applications.

Mr. Tsai was recognized as an Outstanding Graduate Student Instructor at the University of California, Berkeley, in 1996.



Cheol-Woong Lee received the B.S. degree in electrical engineering from the Seoul National University, Seoul, Korea, in 1997. He is currently working toward the Ph.D. degree in electrical engineering at the University of California, Berkeley, where his interest is in RF and analog integrated circuits.

In 1996 and 1997, he investigated and developed a hardware system for 600-dpi color scanner with Thymedia Company Ltd., Seoul, Korea. In 1999, he designed a board to test the multistandard RF monolithic chip at RF research group in the department of electrical engineering at the University of California, Berkeley.



Paul R. Gray (M'69–SM'76–F'80) was born in Jonesboro, AR, on December 8, 1942. He received the B.S., M.S., and Ph.D. degrees from the University of Arizona, Tucson, in 1963, 1965, and 1969, respectively.

In 1969, he joined the Research and Development Laboratory, Fairchild Semiconductor, Palo Alto, CA, where he was involved in the application of new technologies for analog integrated circuits, including power integrated circuits and data conversion circuits. In 1971, he joined the faculty of the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley. His research interests during this period have included bipolar and MOS circuit design, electrothermal interactions in integrated circuits, device modeling, telecommunications circuits, and analog–digital interfaces in VLSI systems. He is the co-author of a widely used college textbook on analog integrated circuits. During year-long industrial leaves of absence from the University of California, Berkeley, he served as Project Manager for Telecommunications Filters at Intel Corporation, Santa Clara, CA, during 1977–78, and as Director of CMOS Design Engineering at Microlinear Corporation, San Jose, CA, during 1984–1985. At the University of California, Berkeley, he has held several administrative posts, including Director of the Electronics Research Laboratory (1985–1986), Vice-Chairman of the EECS Department for Computer Resources (1988–1990), Chairman of the Department of Electrical Engineering and Computer Sciences (1990–1993), and Dean of the College of Engineering (1996–June 2000). He is currently the Executive Vice Chancellor and Provost and Roy W. Carlson Professor of Engineering.

Dr. Gray has been co-recipient of best paper awards at the IEEE International Solid-State Circuits Conference and the European Solid-State Circuits Conference, and was co-recipient of the IEEE R. W. G. Baker Prize in 1980, the IEEE Morris K. Liebman Award in 1983, and the IEEE Circuits and Systems Society Achievement Award in 1987. In 1994, he received the IEEE Solid-State Circuits Award. He served as editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 1977 through 1979, and as Program Chairman of the 1982 International Solid-State Circuits Conference. He served as President of the IEEE Solid-State Circuits Council from 1988 to 1990. He is a member of the National Academy of Engineering.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: ARDESHIR TABIBI
TOWNSEND AND TOWNSEND AND CREW LLP
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	17 JUN 2010
Applicant's or agent's file reference 22287-28-1PC	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 10/31631	19 April 2010 (19.04.2010)	17 April 2009 (17.04.2009)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - G06F 17/00 (2010.01)
USPC - 700/94

Applicant MAXLINEAR, INC.

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	31 May 2010 (31.05.2010)	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (July 2009)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 10/31631

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
   - [X] the international application in the language in which it was filed.
   - [ ] a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. [ ] This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:
   a. (means)
   - [ ] on paper
   - [ ] in electronic form

   b. (time)
   - [ ] in the international application as filed
   - [ ] together with the international application in electronic form
   - [ ] subsequently to this Authority for the purposes of search

4. [ ] In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 10/31631

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	6, 15, 26	YES
	Claims	1-5, 7-14, 16-25, 27-43	NO
Inventive step (IS)	Claims	None.	YES
	Claims	1-43	NO
Industrial applicability (IA)	Claims	1-43	YES
	Claims	None.	NO

2. Citations and explanations:

Claims 1-5, 7-14, 16-25 and 27-43 lack novelty under PCT Article 33(2) as being anticipated by US 2003/0228855 A1 to Hertz et al. (hereinafter 'Hertz').

As per claim 1, Hertz teaches a wideband multimedia recorder for recording a plurality of radio channels (Abstract, para. [0012]) comprising: a wideband receiver (antenna, 100) configured to concurrently receive the plurality of radio channels (Fig. 2, para. [0013]); an analog-to-digital converter (ADC, 237) configured to digitize the plurality of radio channels (Fig. 2, [0066]); a digital front end module configured to frequency down-convert the digitalized plurality of radio channels to a number of radio channels in a baseband (para.[0045], [0069]); a demodulator module configured to demodulate the number of radio channels to a corresponding number of data streams (para. [0048], [0067]); a digital signal processing circuitry configured to process the demodulated number of data streams (para. [0049]); a storage unit (removable storage, 255) configured to store the processed number of data streams (Fig. 2, para.[0055], [0119]); and a control circuitry having a user interface for receiving control commands (para. [0053], [0108]).

As per claim 2, Hertz further teaches a first mixer and a second mixer, the first mixer is configured to generate an in-phase signal from the digitalized plurality of channels and a second mixer is configured to generate a quadrature signal from the digitized plurality of channels (para. [0087], [0093]).

As per claim 3, Hertz further teaches a pre-select filter that precedes the analog-to-digital converter and is configured to pass through the plurality of channels to the analog-to-digital converter (para. [0062], [0078]).

As per claim 4, Hertz further teaches wherein the radio front end module comprises: a wideband low noise amplifier configured to concurrently receive the plurality of radio channels (para. [0062], [0078]); a frequency synthesizer configured to generate an oscillator frequency (para. [0067]); a mixer module coupled to the low noise amplifier and the frequency synthesizer and configured to generate the in-phase and quadrature signals (para. [0093]); and a low-pass filter configured to eliminate unwanted frequency components in the in-phase and quadrature signals (para. [0062]).

As per claim 5, Hertz further teaches wherein the digital front end comprises a number of mixers, each one of the mixers is coupled to the digital in-phase and quadrature signals and configured to generate an associated radio channel in the baseband (para. [0069], [0093]).

As per claim 7, Hertz further teaches wherein the digital front end module further comprises a decimator module configured to decimate each one of the number of radio channels in the baseband (para. [0070], [0092]).

As per claim 8, Hertz further teaches wherein the demodulator module comprises a number of frequency modulation (FM) demodulators (para. [0067]).

As per claim 9, Hertz further teaches wherein the digital signal processing circuitry comprises a plurality of compression engines that are capable of encoding anyone of the demodulated number of data streams with one of a plurality of compression schemes (para. [0106]).

As per claim 10, Hertz further teaches wherein one of the plurality of compression schemes is one of the W AV, MP3, AC3, WMA, AAC audio formats (WMA, para. [0106]).

As per claim 11, Hertz further teaches wherein the digital processing circuitry comprises at least a decompression engine configured to decompress one of the stored encoded number of data streams (para. [0025]).

As per claim 12, Hertz further teaches wherein the storage unit comprises one of the optical compact disc, magnetic hard-disk, or flash memory (flash memory, para. [0055]).

As per claim 13, Hertz further teaches wherein the control circuitry manages playback and recording operations based on the user's control commands (Abstract, para. [0013], [0108]).

As per claim 14, Hertz further teaches wherein the playback is performed on a third-party device (para. [0013], [0052]).
---See Supplemental Sheet---

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 10/31631

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box V.2 Citations and explanations:

As per claim 16, Hertz further teaches an RBDS decoder for parsing radio broadcast data service information embedded in the demodulated number of data streams (para. [0112], [0113]).

As per claim 17, Hertz further teaches wherein the act of parsing comprises determining an occupancy, a location, an identity, and/or content that is associated with at least one of the demodulated number of data streams (para. [0112], [0113]).

As per claim 18, Hertz further teaches wherein the RBDS decoder comprises a plurality of digital decoding circuits that operate in parallel (para. [0018]).

As per claim 19, Hertz further teaches wherein the parsed radio broadcast data service information is stored in a first section of the storage unit ([para. [0114]).

As per claim 20, Hertz further teaches an output unit configured to transmit wirelessly at least one of the number of data streams in response to a user's control commands (para. [0056], [0095]).

As per claim 21, Hertz teaches a wideband personal radio recorder system (Abstract, para. [0012]) comprising: at least a first tuner and a second tuner (para. [0076]), the first tuner configured to receive a first frequency spectrum (AM band) including a first plurality of radio channels (para. [0076]) and convert the first frequency spectrum to a first in-phase signal and a first quadrature signal (para. [0087], [0093]), the second tuner configured to receive a second frequency spectrum (FM band) including a second plurality of radio channels (para. [0076]) and convert the second frequency spectrum to a second in-phase signal and a second quadrature signal (para. [0087], [0093]); at least a first analog-to-digital converter module and a second analog-to- digital module (para. [0076]), the first analog-to-digital converter module (para. [0076]) configured to digitize the first in- phase and quadrature signals (para. [0087], [0093]) , the second analog-to-digital converter module (para. [0076]) configured to digitize the second in-phase and quadrature signals (para. [0087], [0093]); at least a first digital front end module (para. [0076]) having a first plurality of complex mixers configured to frequency down-convert the first digital in-phase and quadrature signals to a first number of radio channels in a baseband (para.[0045], [0069]), a second digital front end module (para. [0076]) having a second plurality of complex mixers configured to frequency down-convert the second digital in-phase and quadrature signals to a second number of radio channels in the baseband (para.[0045], [0069]); a demodulator module coupled to the first and second digital front end modules (para. [0076]) and configured to demodulate the first and second numbers of radio channels to obtain a plurality of data streams (para. [0048], [0067]); a digital signal processing circuitry coupled to the demodulator module and configured to encode the plurality of data streams (para. [0049]); a storage unit (removable storage, 255) coupled to the digital processing circuitry and configured to store the encoded plurality of data streams (Fig. 2, para.[0055], [0119]); and a control circuitry having a user interface for receiving control commands from a user (para. [0053], [0108]).

As per claim 22, Hertz further teaches wherein the first and second tuners, the first and second analog-to-digital converter modules, and the first and second digital front end modules are configured to operate concurrently)para. [0076]).

As per claim 23, Hertz further teaches wherein the digital signal processing circuitry further comprises an RBDS decoder for parsing radio broadcast data service (RBDS) information embedded in the demodulated number of data streams (para. [0112], [0113]).

As per claim 24, Hertz further teaches wherein the parsed RBDS information is stored in a first section of the storage unit (para. [0114]).

As per claim 25, Hertz further teaches wherein the digital signal processing circuitry further comprises at least a decoding engine configured to decode at least one of the stored plurality of data streams for playback (para. [0025]).

As per claim 27, Hertz teaches a method of recording a plurality of radio channels with a wideband receiver (Abstract, para. [0012]) comprising: receiving a radio signal including the plurality of radio channels (para. [0013]); converting the radio signal to an in-phase signal and a quadrature signal (para. [0093]); digitizing the in-phase and quadrature signals (para. [0066]); frequency-shifting the plurality of radio channels to a baseband by mixing the digital in-phase and quadrature signals concurrently with a plurality of complex mixers (para. [0045], [0069]); demodulating the plurality of radio channels in the baseband to obtain a corresponding plurality of data streams (para. [0048], [0067]); encoding the plurality of data streams (para. [0106]); and storing the encoded plurality of data streams (para. [0055], [0119]).

As per claim 28, Hertz further teaches filtering and decimating the frequency-shifted plurality of channels before demodulating (para. [0097]).

As per claim 29, Hertz further teaches retrieving the stored plurality of data streams (para. [0025]); and decoding at least one of the plurality of data streams for playback (para. [0025]).

As per claim 30, Hertz further teaches wherein the encoding comprises at least one of a plurality of audio compression schemes (para. [0106]).

As per claim 31, Hertz further teaches parsing radio broadcast data service (RBDS) information embedded in the plurality of demodulated data streams (para. [0012]-[0014]); storing the radio data service information (para. [0012]-[0014]); and building a directory based on the stored RBDS information (para. [0014]).

As per claim 32, Hertz further teaches wherein the parsing comprises determining an occupancy, a location, an identity, and/or content that is associated with at least one of the plurality of demodulated data streams (para. [0112], [0113]).

---See Supplemental Sheet---

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 10/31631

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box V.2 Citations and explanations:

As per claim 33, Hertz further teaches transmitting wirelessly, in response to user's control commands, at least one of the plurality of data streams (para. [0056]).

As per claim 34, Hertz teaches a method of recording a plurality of radio channels with a multi-tuner receiver (Abstract, para. [0012]) comprising: providing at least a first tuner and a second tuner (para. [0076]), the first and second tuners configured to operate concurrently (para. [0076]), the first tuner configured to receive a first frequency (AM band) spectrum including a first plurality of radio channels (para. [0076]), the second tuner configured to receive a second frequency spectrum (FM band) including a second plurality of radio channels (para. [0076]), the first tuner (para. [0076]) being configured to convert the first frequency spectrum to a first in-phase signal and a first quadrature signal (para. [0087], [0093]), and the second tuner (para. [0076]) configured to convert the second frequency spectrum to a second in-phase signal and a second quadrature signal (para. [0087], [0093]); converting the first frequency spectrum to a first in-phase and a first quadrature signal (para. [0076], [0087], [0093]); converting the second frequency spectrum to a second in-phase and a second quadrature signal (para. [0076], [0087], [0093]); digitizing the first and second in-phase and quadrature signals (para. [0076]); multiplying the first in-phase and quadrature signals with a first plurality of complex mixers to obtain a first plurality of in-phase and quadrature signals at a baseband (para.[0045], [0069]), wherein each one of the first number of in-phase and quadrature signals represents one of the first plurality of radio channels (para.[0045], [0069]); multiplying the second in-phase and quadrature signals with a second plurality of complex mixers to obtain a second plurality of in-phase and quadrature signals at the baseband, wherein each one of the second number of in-phase and quadrature signals represents one of the second plurality of radio channels (para.[0045], [0069]); demodulating the each one of the first and second pluralities of in-phase and quadrature signals to obtain a plurality of data streams (para. [0048], [0067]); encoding the plurality of data streams (para. [0049]); and storing the encoded plurality of data stream para.[0055], [0119]).

As per claim 35, Hertz further teaches filtering and then decimating the each one of the first and second pluralities of in-phase and quadrature signals before demodulating (para. [0097]).

As per claim 36, Hertz further teaches playing back at least one of the stored plurality of data streams (para. [0025]).

As per claim 37, Hertz further teaches wherein the encoding comprises at least one of the WAV, MP3, AC3, AAC, WMA audio compression formats (WMA, para. [0106]).

As per claim 38, Hertz further teaches wherein the digitizing the first and second inphase and quadrature signals is performed concurrently. (para. [0076]).

As per claim 39, Hertz further teaches wherein the demodulating the each one of the first and second pluralities of in-phase and quadrature signals is performed concurrently (para. [0095]).

As per claim 40, Hertz further teaches wherein the encoding is performed in parallel for each one of the plurality of data streams (para. [0020]).

As per claim 41, Hertz further teaches parsing radio broadcast data service (RBDS) information embedded in the plurality of demodulated data streams (para. [0012]-[0014]); storing the radio data service information (para. [0012]-[0014]); and building a directory based on the stored RBDS information (para. [0114]).

As per claim 42, Hertz further teaches wherein the parsing comprises determining an occupancy, a location, an identity, and/or content that is associated with at least one of the plurality of demodulated data streams (para. [0112], [0113]).

As per claim 43, Hertz further teaches transmitting wire1essly, in response to a user's control commands, at least one 3 of the plurality of data streams (para. [0056]).

Claims 15 and 26 lack an inventive step under PCT Article 33(3) as being obvious over Hertz in view of US 2003/0158614 A1 to Friel et al. (hereinafter 'Friel').

As per claim 15, Hertz does not teach a battery configured to supply power to the recorder for continual operation in the event that an external power supply is turned off. However, Friel does teach a battery configured to supply power to the recorder for continual operation in the event that an external power supply is turned off (para. [0002]). It would have been obvious to one of ordinary skill in the art to modify the recorder, as taught by Hertz, so as to include the use of a battery, as taught by Friel, because the battery ensures that the recorder will maintain tower, thus saving the memory storage and user controls.

As per claim 26, Hertz does not teach a battery configured to supply power to the recorder for continual operation in the event that an external power supply is turned off. However, Friel does teach a battery configured to supply power to the recorder for continual operation in the event that an external power supply is turned off (para. [0002]). It would have been obvious to one of ordinary skill in the art to modify the recorder, as taught by Hertz, so as to include the use of a battery, as taught by Friel, because the battery ensures that the recorder will maintain tower, thus saving the memory storage and user controls.

---See Supplemental Sheet---

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 10/31631

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box V.2 Citations and explanations:

Claim 6 lacks an inventive step under PCT Article 33(3) as being obvious over Hertz in view of US 5705949 A to Alelyunas et al. (hereinafter 'Alelyunas').

As per claim 6, Hertz does not teach wherein each one of the plurality of mixers is a digital complex mixer comprising four digital multipliers and two digital adders. However, Aleyunas does teach wherein each one of the plurality of mixers is a digital complex mixer comprising four digital multipliers and two digital adders (Fig. 1). It would have been obvious to one of ordinary skill in the art to modify the recorder, as taught by Hertz, so as to include a portion of the circuit to include 4 multipliers and 2 adders, as taught by Aleyunas, because they provide for compensation of phase error, thus reducing the potential of errors in the recorder (col. 3, ln 10-24).

Claims 1-43 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 22287-28-1PC	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 10/31631	International filing date *(day/month/year)* 19 April 2010 (19.04.2010)	(Earliest) Priority Date *(day/month/year)* 17 April 2009 (17.04.2009)
Applicant MAXLINEAR, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed.
      ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (see Box No. II).
3. ☐ **Unity of invention is lacking** (see Box No. III).
4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 1
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 10/31631

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 17/00 (2010.01)
USPC - 700/94
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC - 700/94

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 370/203, 206, 215, 297, 307, 310, 464, 546; 700/94; 704/500 (keyword limited; see terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST(PGPB,USPT,EPAB,JPAB); Google Patents; Google. Search Terms Used: record, save, store, radio, channel, broadcast, program, frequency, RBDS, RDS, baseband, base, band, analog, digital, ADC, A/D, digitze, DSP, signal, processing, storage, disc, flash, memory, hard, disk, demodulate, user, owner, operator, human, control, interface, display, co

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---------- Y	US 2003/0228855 A1 (Hertz et al.) 11 December 2003 (11.12.2003) entire document, especially: Fig. 2, Abstract, para. [0012]-[0014], [0018], [0025], [0045], [0048], [0049], [0053], [0055], [0056], [0062]-[0070], [0076],[0078], [0087], [0092], [0093], [0095], [0106]-[0108], [0112]-[0114], [0119]	1-5, 7-14, 16-25, 27-43 ---------- 6, 15, 26
Y	US 2003/0158614 A1 (Friel et al.) 21 August 2003 (21.08.2003) para. [0002]	15, 26
Y	US 5,705,949 A (Alelyunas et al.) 06 January 1998 (06.01.1998) Fig. 1, col. 3, ln 10-24	6
A	US 2007/0179649 A1 (Mitsuno) 02 August 2007 (02.08.2007) entire document	1-43

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 May 2010 (31.05.2010)	17 JUN 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
ARDESHIR TABIBI
TOWNSEND AND TOWNSEND AND CREW LLP
8TH FLOOR
TWO EMBARCADERO CENTER
SAN FRANCISCO, CA 94111

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	18 JUN 2010
Applicant's or agent's file reference 22287-27-1PC	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2010/031627	19 April 2010	17 April 2009

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - H04B 1/06 (2010.01)
USPC - 455/260

Applicant MAXLINEAR, INC.

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	26 May 2010	Blaine Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (April 2007)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2010/031627

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
   - [X] the international application in the language in which it was filed.
   - [ ] a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. [ ] This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:
   a. type of material
      - [ ] a sequence listing
      - [ ] table(s) related to the sequence listing

   b. format of material
      - [ ] on paper
      - [ ] in electronic form

   c. time of filing/furnishing
      - [ ] contained in the international application as filed
      - [ ] filed together with the international application in electronic form
      - [ ] furnished subsequently to this Authority for the purposes of search

4. [ ] In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Form PCT/ISA/237 (Box No. I) (April 2007)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No. PCT/US2010/031627

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	4, 7-9 and 16-25	YES
	Claims	1-3, 5, 6, 10-15, 26 and 27	NO
Inventive step (IS)	Claims	None	YES
	Claims	1-27	NO
Industrial applicability (IA)	Claims	1-27	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1-3, 5, 6, 10-15, 26 and 27 lack novelty under PCT Article 33(2) as being anticipated by Feher.

Regarding claim 1, Feher discloses a wideband receiver system (paragraph [0231]) comprising: a wideband receiver configured to concurrently receive a plurality of desired RF channels (in-phase and quadrature-phase baseband channels, paragraph [0276]); said wideband receiver comprising: a mixer module (multipliers also known as mixers, paragraphs [236] and [0243]) coupled to the plurality of desired RF channels and having a first mixer (mixer 11.13 of Fig. 17b) configured to generate an in-phase signal and a second mixer (mixer 11.16 of Fig. 17b) configured to generate a quadrature signal (an in-phase (I) and quadrature (Q) channels, Fig. 6 and paragraph [0237]); a wideband analog-to-digital converter (ADC) module (paragraph [0247]) having a first wideband ADC (19.15 of Fig. 19) coupled with the in-phase signal and configured to generate a digitalized in-phase signal and a second wideband ADC (19.8 of Fig. 19) coupled with the quadrature signal and configured to generate a digitalized quadrature signal (paragraph [0257]); and a digital frontend (DFE) module (5.17 and 5.5 of Fig. 5) having a plurality of complex mixers (5.8 and 5.20 of Fig. 5) coupled to the digital in-phase and quadrature signals, each one of the plurality of complex mixers frequency-shifting a different one of the plurality of the desired RF channels to a baseband signal (paragraph [0236]).

Regarding claim 2, Feher discloses a local oscillator (5.9 and 5.21 of Fig. 5) having an oscillator frequency centered around the plurality of the desired RF channels (paragraph [0236]).

Regarding claim 3, Feher discloses that the local oscillator comprises a phaselocked loop (paragraph [0247]).

Regarding claim 5, Feher discloses that each one of the plurality of complex mixers comprises a pair of digital multipliers (5.8 and 5.20 of Fig. 5), each pair of the digital multipliers is coupled to a numerically controlled oscillator (5.9 and 5.21 of Fig. 5) (multipliers 5.8 and 5.20 of Fig. 5 are coupled to oscillators 5.9 and 5.21 of Fig. 5, respectively, paragraph [0236]).

Regarding claim 6, Feher discloses that the DFE module (5.17 and 5.5 of Fig. 5) further comprises a plurality of channel filters (5.6 and 5.18 of Fig. 5), each one of the plurality of channel filters is coupled to each one of the plurality of complex mixers (5.8 and 5.20 of Fig. 5) and configured to filter one of the plurality of the desired channels (paragraph [0236]).

Regarding claim 10, Feher discloses an up-converter module (20.4b of Fig. 20) configured to frequency-shift the plurality of desired RF channels in the baseband to an intermediate frequency band (paragraph [0258]).

Regarding claim 11, Feher discloses that the up-converter module (20.4b of Fig. 20) comprises a plurality of N up-mixers (5.8 and 5.20 of Fig. 5) having a plurality of associated oscillator frequencies (5.9 and 5.21 of Fig. 5), wherein N is an integer value equal to the plurality of the desired RF channels (paragraph [0261]); wherein the plurality of associated oscillator frequencies are so chosen so that when mixing with the plurality of desired channels in the baseband, the mixed products occupy a contiguous frequency spectrum, or a substantially-contiguous frequency spectrum with one or more spacings between the desired channels (paragraphs [0246] and [0280]), wherein the one or more spacings are variable (inherent in a spread frequency spectrum), and wherein the one or more spacings are smaller than or comparable to a channel bandwidth, or small measured as a fraction of the bandwidth of the first and second wideband ADCs (paragraphs [0236], [0237] and [0257]).

Regarding claim 12, Feher discloses that the mixed products comprise spectra that are spaced in such a way so as to avoid overlap with known frequency bands containing potential or actual interferers (paragraph [0261]).

Regarding claim 13, Feher discloses that the mixed products comprise spectra that are spaced in such a way so as to avoid overlap with known frequency bands that introduce interference to other systems (paragraph [0261]).

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2010/031627

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

Regarding claim 14, Feher discloses that each one of the plurality of N up-mixers is a digital complex mixer (5.8 and 5.20 of Fig. 5) and each one of the plurality of associated oscillator frequencies (5.9 and 5.21 of Fig. 5) is generated by a numerically controlled oscillator (numerically controlled oscillator, paragraph [0247]).

Regarding claim 15, Feher discloses a digital-to-analog converter (paragraphs [0247] and [0254]) configured to convert the contiguous group of channels in the intermediate frequency spectrum to an analog waveform.

Regarding claim 26, Feher discloses a method of receiving a plurality of radio frequency (RF) channels including a number of desired channels (paragraphs [0221] and [0231]) that are located in non-contiguous portions of a frequency spectrum and grouping the desired channels in a contiguous frequency spectrum (paragraph [0261]), the method comprising: concurrently receiving the plurality of RF channels; producing an in-phase signal and a quadrature signal by mixing the plurality of RF channels (in-phase and quadrature-phase baseband channels, paragraph [0276]) with a first oscillator frequency 5.9 of Fig. 5) and a second local frequency (5.21 of Fig. 5); digitizing the in-phase and quadrature signals (19.10a of Fig. 19); and frequency down-shifting the digital in-phase and quadrature signals to a baseband signal using a number of complex mixers (mixers 11.13 and 11.16 of Fig. 17b, paragraphs [236] and [0243]), wherein the first and second oscillator frequencies are identical and have a phase shift of 90' degree between them, wherein the number of complex mixers correspond to the number of desired channels (Feher, paragraph [0243]).

Regarding claim 27, Feher discloses frequency up-shifting the baseband signal to an intermediate frequency; and converting the frequency up-shifted baseband signal to an analog waveform (paragraphs [0247] and [0254]).

Claims 4 and 16-25 lack an inventive step under PCT Article 33(3) as being obvious over Feher in view of Currivan.

Regarding claims 4 and 24, Feher discloses that the desired RF channels conform to Video over Internet Protocol (VilP) as well as Voice over Internet Protocol (VoIP) (paragraph [0236]). However, Feher fails to disclose that the plurality of desired RF channels conform to a Data Over Cable Service Interface Specification (DOCSIS) protocol. In the same field of endeavor, Currivan discloses that the plurality of desired RF channels conform to a Data Over Cable Service Interface Specification (DOCSIS) protocol (paragraphs [0027] and [0028]). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Currivan to incorporate the above features into the invention of Feher for the benefit of providing an equivalent data throughput of N channels to a user, though the user perceives a single channel (Currivan, paragraph [0027]).

Regarding claim 16, Feher discloses a multi-tuner receiver system (paragraphs [0221] and [0231]) for receiving a plurality of desired radio frequency (RF) channels (in-phase and quadrature-phase baseband channels, paragraph [0276]) that extend over multiple non-contiguous portions of a broad frequency spectrum and grouping them in a contiguous frequency spectrum, the system comprising: a first tuner (multiple receiver, paragraph [0200]) configured to receive a first portion of the broad frequency spectrum, the first tuner includes a first mixer (mixer 11.13 of Fig. 17b) module coupled to a first oscillator (5.9 of Fig. 5) and is configured to generate a first in-phase signal and a first quadrature signal (an in-phase (I) and quadrature (Q) channels, Fig. 6 and paragraph [0237]); a second tuner (multiple receiver, paragraph [0200]) configured to receive a second portion of the broad frequency spectrum, the second tuner includes a second mixer module (mixer 11.16 of Fig. 17b) coupled to a second oscillator (5.21 of Fig. 5) and is configured to generate a second in-phase signal and a second quadrature signal (an in-phase (I) and quadrature (Q) channels, Fig. 6 and paragraph [0237]); a first analog-to-digital converter module (19.10a of Fig. 19) configured to digitize the first in-phase and quadrature signals; a second analog-to-digital converter module (19.2 of Fig. 19) configured to digitize the second in-phase and quadrature signals (paragraphs [0247] and [0254]). Feher fails to disclose first and second digital frontends. In the same field of endeavor, Currivan discloses a first digital frontend (DFE) module (112 sub 1 of Fig. 1) having a first bank of down-mixers coupled to the first digital in-phase and quadrature signals, each of the first bank of down-mixers is configured to frequency shift one of the desired RF channels in the first portion of the broad frequency spectrum (paragraphs [0019], [0031] and [0078]); and a second digital frontend (DFE) module (112 sub 2 of Fig. 1) having a second bank of down-mixers coupled to the second digital in-phase and quadrature signals, each of the second bank of down-mixers is configured to frequency shift one of the desired RF channels in the second portion of the broad frequency spectrum; wherein the first DFE module frequency-shifts the desired RF channels in the first portion of the broad frequency spectrum to a first portion of a baseband signal (paragraphs [0019], [0031] and [0078]); wherein the second DFE module frequency-shifts the desired RF channels in the second portion of the broad frequency spectrum to a second portion of the baseband signal (paragraphs [0018]-[0021]). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Currivan to incorporate the above features into the invention of Feher for the benefit of selecting a first baseband signal corresponding to a first channel and for selecting a second baseband signal corresponding to a second channel, respectively (Currivan, paragraph [0019]).

Regarding claim 17, Currivan discloses a crossbar switch (a carrier adjustment module) interposed between the first and second analog-to-digital converter modules and the first and second DFE modules (paragraph [0019]).

Regarding claim 18, Feher discloses a first up-converter module (20.3b of Fig. 20) having a first bank of up-mixers (mixer 11.13 of Fig. 17b) coupled to the first portion of the baseband signal and configured to frequency shift the first portion of the baseband signal to a first portion of an intermediate frequency spectrum (5.9 of Fig. 5 and an in-phase (I) and quadrature (Q) channels, Fig. 6 and paragraph [0237]); a second up-converter module (20.4b of Fig. 20) having a second bank of up-mixers (mixer 11.16 of Fig. 17b) coupled to the second portion of the baseband signal and configured to frequency shift the second portion of the baseband signal to a second portion of the intermediate frequency spectrum (5.21 of Fig. 5 and an in-phase (I) and quadrature (Q) channels, Fig. 6 and paragraph [0237]); and a digital-to-analog converter (19.10a and 19.2 of Fig. 19) configured to convert the first and second portions of the intermediate frequency spectrum to an analog waveform signal (paragraphs [0247] and [0254]).

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2010/031627

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

Regarding claim 19, Currivan discloses a crossbar switch interposed between the first and second DFE modules and the first and second up-converter modules (a carrier adjustment module).

Regarding claim 20, Feher discloses that the first and second portions are adjacent to each other and non-overlapping (paragraph [0261]).

Regarding claim 21, Feher discloses that each one of the first bank of down-mixers comprises a pair of digital multiplier having an input terminal coupled to a numerically controlled oscillator (multipliers also known as mixers, paragraphs [236] and [0243]).

Regarding claim 22, Feher discloses that the first DFE module (5.17 of Fig. 5) further comprises a plurality of channel filters (5.6 and 5.18 of Fig. 5), each one of the plurality of channel filters is coupled to each one of the first bank of down-mixers (5.8 and 5.20 of Fig. 5) and configured to filter one of the frequency down-shifted RF channels (paragraph [0236]).

Regarding claim 23, Feher discloses that the plurality of desired RF channels conform to one of a digital video broadcasting (DVB) standard (paragraph [0190]).

Regarding claim 25, Feher discloses that the plurality of RF channels conform to a television broadcasting standard (paragraph [0231]).

Claims 7-9 lack an inventive step under PCT Article 33(3) as being obvious over Feher in view of Hoctor.

Regarding claim 7, Feher discloses a plurality of channel filters (5.6 and 5.18 of Fig. 5). Feher fails to disclose that each one of the plurality of channel filters is a finite impulse response filter. In the same field of endeavor, Hoctor discloses that each one of the plurality of channel filters is a finite impulse response filter (paragraph [0061]). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Hoctor to incorporate the above features into the invention of Feher for the benefit of processing signals processed by the decimation filter (Hoctor, paragraph [0061]).

Regarding claim 8, Feher discloses a plurality of channel filters (5.6 and 5.18 of Fig. 5). Feher fails to disclose that the DFE module further comprises a decimator module configured to decimate each one of the plurality of the desired channels in the baseband. In the same field of endeavor, Hoctor discloses that the DFE module (paragraph [0067]) further comprises a decimator module (paragraph [0061]) configured to decimate each one of the plurality of the desired channels in the baseband (paragraph [0059]). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Hoctor to incorporate the above features into the invention of Feher for the benefit of eliminating undesirable signals and reduce the sampling rate to an appropriate frequency for baseband operation (Hoctor, paragraph [0059]).

Regarding claim 9, Feher discloses a plurality of channel filters (5.6 and 5.18 of Fig. 5). Feher fails to disclose that the DFE module further comprises a decimator module configured to decimate each one of the plurality of the desired channels to a demodulator. In the same field of endeavor, Hoctor discloses that the DFE module (paragraph [0067]) further comprises a decimator module (paragraph [0061]) configured to decimate each one of the plurality of the desired channels to a demodulator (paragraph [0064]). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Hoctor to incorporate the above features into the invention of Feher for the benefit of eliminating undesirable signals and reduce the sampling rate to an appropriate frequency for baseband operation (Hoctor, paragraph [0059]).

Claims 1-27 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made or used in industry.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 22287-27-1PC	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US2010/031627	International filing date *(day/month/year)* 19 April 2010	(Earliest) Priority Date *(day/month/year)* 17 April 2009
Applicant MAXLINEAR, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II)

3. ☐ **Unity of invention is lacking** (see Box No. III)

4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant
   ☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 4
      ☒ as suggested by the applicant
      ☐ as selected by this Authority, because the applicant failed to suggest a figure
      ☐ as selected by this Authority, because this figure better characterizes the invention
   b. ☐ none of the figures is to be published with the abstract

Form PCT/ISA/210 (first sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/031627

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H04B 1/06 (2010.01)
USPC - 455/260
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H04B 1/06, 1/00 (2010.01)
USPC - 455/260, 209, 42, 180.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X — Y	US 2007/0032220 A1 (FEHER) 08 February 2007 (08.02.2007) entire document	1-3, 5, 6, 10-15, 26 and 27 ------ 4, 7-9 and 16-25
Y	US 2007/0263754 A1 (CURRIVAN et al) 15 November 2007 (15.11.2007) entire document	4 and 16-25
Y	US 2007/0002961 A1 (HOCTOR et al) 04 January 2007 (04.01.2007) entire document	7-9
A	US 5,590,156 A (CARNEY) 31 December 1996 (31.12.1996) entire document	1-27
A	US 5,768,260 A (KLINE et al) 16 June 1998 (16.06.1998) entire document	1-27

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 May 2010	18 JUN 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2005)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/862,946	07/12/2022	2631	830	28427US15	20	2

CONFIRMATION NO. 7376

FILING RECEIPT

23446
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

Date Mailed: 07/25/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Madhukar Reddy, Carlsbad, CA;
Curtis Ling, Carlsbad, CA;
Tim Gallagher, Carlsbad, CA;

Applicant(s)

Entropic Communications, LLC, New York, NY;

Power of Attorney: The patent practitioners associated with Customer Number 23446

Domestic Priority data as claimed by applicant

This application is a CON of 17/587,462 01/28/2022 PAT 11399206
which is a CON of 17/217,244 03/30/2021 ABN
which is a CON of 16/430,506 06/04/2019 PAT 10972781
which is a CON of 15/792,318 10/24/2017 PAT 10313733
which is a CON of 14/948,881 11/23/2015 PAT 9819992
which is a CON of 14/617,973 02/10/2015 PAT 9210363
which is a CON of 13/962,871 08/08/2013 PAT 9100622
which is a CON of 12/762,900 04/19/2010 PAT 8526898
which claims benefit of 61/170,526 04/17/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 07/21/2022
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/862,946**
Projected Publication Date: 11/03/2022
Non-Publication Request: No
Early Publication Request: No
**** SMALL ENTITY ****
Title

SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL

Preliminary Class

375

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/862,946

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	80		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	350		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	400		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*	x 50 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*	x 240 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	830		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

To: mhmpto@mcandrews-ip.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 23446

Jul 25, 2022 12:45:48 PM

Dear PAIR Customer:

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 23446 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
17862946	APP.FILE.REC	07/25/2022	28427US15

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

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UNITED STATES DEPARTMENT OF COMMERCE
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/862,946	07/12/2022	Madhukar Reddy	28427US15	7376

23446 7590 08/09/2022
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER
CENTRAL, DOCKET

ART UNIT	PAPER NUMBER
2644	

NOTIFICATION DATE	DELIVERY MODE
08/09/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mhmpto@mcandrews-ip.com

PTOL-90A (Rev. 04/07)

Decision Granting Request for Prioritized Examination (Track I)	**Application No.** 17/862,946	**Applicant(s)** Reddy et al.	
	Examiner CHERYL P GIBSON BAYLOR	**Art Unit** OPET	**AIA (FITF) Status** No

1. THE REQUEST FILED 12 July 2022 IS **GRANTED** .

   The above-identified application has met the requirements for prioritized examination
   A. ☑ for an original nonprovisional application (Track I).
   B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination**. The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:

   A. filing a **petition for extension of time** to extend the time period for filing a reply;

   B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims** , or a multiple dependent claim;

   C. filing a **request for continued examination** ;

   D. filing a notice of appeal;

   E. filing a request for suspension of action;

   F. mailing of a notice of allowance;

   G. mailing of a final Office action;

   H. completion of examination as defined in 37 CFR 41.102; or

   I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to CHERYL GIBSON BAYLOR at (571)272-3213. In his/her absence, calls may be directed to Petition Help Desk at (571) 272-3282.

/CHERYL GIBSON BAYLOR/ Paralegal Specialist, OPET	

U.S. Patent and Trademark Office
PTO-2298 (Rev. 02-2012)

To: mhmpto@mcandrews-ip.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 23446

Aug 10, 2022 05:05:53 AM

Dear PAIR Customer:

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 23446 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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Application	Document	Mailroom Date	Attorney Docket No.
17862946	TRACK1.GRANT	08/09/2022	28427US15

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/862,946	07/12/2022	Madhukar Reddy	28427US15	7376

23446 7590 09/07/2022
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER
JACKSON, BLANE J

ART UNIT	PAPER NUMBER
2644	

NOTIFICATION DATE	DELIVERY MODE
09/07/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mhmpto@mcandrews-ip.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 17/862,946	Applicant(s) Reddy et al.	
	Examiner BLANE J JACKSON	Art Unit 2644	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 12 July 2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-18 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-18 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 12 July 2022 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process... may obtain a patent therefor..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the claims that are directed to the same invention so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 1-18 is/are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-18 of prior U.S. Patent No. 10,972,781. This is a statutory double patenting rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):

(b) CONCLUSION The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 3, 11 and 12 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention. The claims of the application, reference claims 1 and 8, 10 and 17, are interpreted as disclosed for the embodiment shown in figure 4 which includes a Summing DAC 470 to generate the analog the IF output with a bandwidth of 32 MHz and 16 MHz center frequency. However, dependent claims 2, 3, 11 and 12 are directed to "the IF signal is a digital signal and the DFE is configured to output the IF signal via a serial (claims 3 and 12; parallel) interface" which is not taught by the Disclosure. As shown in figures 2 and 4, the output of the Digital Front End 230, 430 comprises N filtered and decimated channels *at baseband*, and with respect to figure 2, it is clear this baseband output is coupled with *a serial or parallel data interface* to a demodulator. The embodiment of figure 4 indicates the desired digital base band channels output of the DFE 430 are coupled to a Tiled Upconversion 450, then processed through a Summing DAC 470 to provide the IF output. This IF output is not digital and not configured as a serial or parallel data interface.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BLANE J JACKSON whose telephone number is (571)272-7890. The examiner can normally be reached 7:30-4:30 M-TH; 8-2 FRI.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kathy Wang-Hurst can be reached on 571 270 5371. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BLANE J JACKSON/
Primary Examiner, Art Unit 2644

Notice of References Cited	Application/Control No. 17/862,946	Applicant(s)/Patent Under Reexamination Reddy et al.	
	Examiner BLANE J JACKSON	Art Unit 2644	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-6735421-B1	05-2004	Claxton; Shimen K.	H04B1/0007	455/313
*	B	US-20090075613-A1	03-2009	Safarian; Aminghasem	H04B1/18	455/232.1
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/862,946	Reddy et al.
	Examiner	**Art Unit**
	BLANE J JACKSON	2644

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/30/2022								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/862,946	Reddy et al.
	Examiner	**Art Unit**
	BLANE J JACKSON	2644

CPC - Searched*		
Symbol	**Date**	**Examiner**
H04B 1/001, 1/0007, 1/0014	08/30/2022	BJJ
H04N 5/455, 5/50, 21/4382, 21/4383	08/30/2022	BJJ

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
review of prior continuing patents and IDS; DP to US 10972781 to FAOM	08/30/2022	BJJ

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

Bibliographic Data

Application No: 17/862,946

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /BLANE J JACKSON/ (Examiner's Signature) | Initials

Title: SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
07/12/2022 **RULE**	348	2644	28427US15

APPLICANTS

Entropic Communications, LLC, New York, NY,

INVENTORS

Madhukar Reddy, Carlsbad, CA, UNITED STATES

Curtis Ling, Carlsbad, CA, UNITED STATES

Tim Gallagher, Carlsbad, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 17587462 01/28/2022 PAT 11399206

17587462 is a CON of 17217244 03/30/2021ABN

17217244 is a CON of 16430506 06/04/2019 PAT 10972781

16430506 is a CON of 15792318 10/24/2017 PAT 10313733

15792318 is a CON of 14948881 11/23/2015 PAT 9819992

14948881 is a CON of 14617973 02/10/2015 PAT 9210363

14617973 is a CON of 13962871 08/08/2013 PAT 9100622

13962871 is a CON of 12762900 04/19/2010 PAT 8526898

12762900 has PRO of 61170526 04/17/2009

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

07/21/2022

**** SMALL ENTITY ****

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UNITED STATES

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MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661
UNITED STATES

FILING FEE RECEIVED

$3,000

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	2022-07-12
First Named Inventor	Madhukar Reddy
Art Unit	
Examiner Name	
Attorney Docket Number	28427US14

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6906498		2005-06-14	Breuch et al.	
	2	6992855		2006-01-31	Ehrlich	
	3	7095454		2006-08-22	Waight et al.	
	4	7167694		2007-01-23	Khoini-Poorfard et al.	
	5	7362178		2008-04-22	Montemayor et al.	
	6	7373125		2008-05-13	Godambe et al.	
	7	7421259		2008-09-02	Gomez et al.	
	8	8285240		2012-10-09	Seendripu et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /B.J.J/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2022-07-12
	First Named Inventor	Madhukar Reddy
	Art Unit	
	Examiner Name	
	Attorney Docket Number	28427US14

	9	8374568		2013-02-12	Seendripu et al.	
	10	8374569		2013-02-12	Seendripu et al.	
	11	8374570		2013-02-12	Seendripu et al.	
	12	8526898		2013-09-03	Reddy et al.	
	13	8577319		2013-11-05	Ling et al.	
	14	8666350		2014-03-04	Vauhkonen	
	15	8909187		2014-12-09	Seendripu et al.	
	16	9059672		2015-06-16	Ling et al.	
	17	8300681	B2	2012-10-30	Petrovic et al.	
	18	7145972		2006-12-05	Kumar	
	19	9210362		2015-12-08	Reddy et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2022-07-12
	First Named Inventor	Madhukar Reddy
	Art Unit	
	Examiner Name	
	Attorney Docket Number	28427US14

	20	8526898		2013-09-03	Reddy et al.	
	21	7599673		2009-10-06	Maxim et al.	
	22	5280636		1994-01-18	Kelley et al.	
	23	9100622		2015-08-04	Reddy et al.	
	24	8892225		2014-11-18	Walsh et al.	
	25	6920185		2005-07-19	Hinson	
	26	5590156		1996-12-31	Carney	
	27	5705949		1998-01-06	Alelyunas et al.	
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	29	6253094		2001-06-26	Schmutz	
	30	6262981		2001-07-17	Schmutz	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	2022-07-12
	First Named Inventor	Madhukar Reddy
	Art Unit	
	Examiner Name	
	Attorney Docket Number	28427US14

	31	6282184		2001-08-28	Lehman et al.	
	32	6735421		2004-05-11	Claxton et al.	
	33	6760342		2004-07-06	Skones et al.	
	34	8107916		2012-01-31	Gatta et al.	
	35	8331886		2012-12-11	Wang et al.	
	36	10313733		2019-06-04	Reddy et al.	
	37	9819992		2017-11-14	Reddy et al.	
	38	9210363		2015-12-08	Reddy et al.	
	39	9225373		2015-12-29	Gomez et al.	
	40	9942598		2018-04-10	Reddy et al.	
	41	10972781		2021-04-06	Reddy et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2022-07-12
	First Named Inventor	Madhukar Reddy
	Art Unit	
	Examiner Name	
	Attorney Docket Number	28427US14

	42	11381866		2022-07-05	Reddy et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050040909	A1	2005-02-24	Waight et al.	
	2	20070042742	A1	2007-02-22	Kim et al.	
	3	20070111661	A1	2007-05-17	Bargroff et al.	
	4	20040110522	A1	2004-06-10	Reddy et al.	
	5	20050286562	A1	2005-12-29	Nakao et al.	
	6	20110105068	A1	2011-05-05	Reddy et al.	
	7	20090258629	A1	2009-10-15	Ritchey et al.	
	8	20030158614	A1	2003-08-21	Friel et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /B.J.J/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	2022-07-12
	First Named Inventor	Madhukar Reddy
	Art Unit	
	Examiner Name	
	Attorney Docket Number	28427US14

	9	20030228855	A1	2003-12-11	Herz et al.	
	10	20040058661	A1	2004-03-25	Hsu et al.	
	11	20070002961	A1	2007-01-04	Hoctor et al.	
	12	20070032220	A1	2007-02-08	Feher	
	13	20070179649	A1	2007-08-02	Mitsuno	
	14	20070263754	A1	2007-11-15	Currivan et al.	
	15	20090075613	A1	2009-03-19	Safarian et al.	

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2087623	EP	A2	2009-08-12	RF Magic Inc.		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2022-07-12
	First Named Inventor	Madhukar Reddy
	Art Unit	
	Examiner Name	
	Attorney Docket Number	28427US14

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	JEFFREY A. WELDON, et al. "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter With Harmonic-Rejection Mixers, IEEE Journal of Solid-State Circuits, December 2001, pages: 2003-2015, Vol. 36, No. 12, Seattle, Washington.	
	2	Int'l Search Report and Written Opinion Appln No. PCT/2010/031631 mailed June 17, 2010.	
	3	Int'l Search Report and Written Opinion Appln No. PCT/2010/031627 mailed June 18, 2010.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/BLANE J JACKSON/	Date Considered	08/30/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /B.J.J/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	2022-07-12
	First Named Inventor	Madhukar Reddy
	Art Unit	
	Examiner Name	
	Attorney Docket Number	28427US14

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Wayne H. Bradley/	Date (YYYY-MM-DD)	2022-07-12
Name/Print	Wayne H. Bradley	Registration Number	39916

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	3	"113992206".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/30 09:24 AM
L2	2	"11399206".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/30 09:24 AM
L3	2	"10972781".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/30 09:27 AM
L4	8	"10313733".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2022/08/30 09:37 AM

			CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L5	5	"9819992".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/30 09:40 AM
L6	8	"9210363".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/30 09:42 AM
L7	21	"9100622".pn.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN,	OR	ON	ON	2022/08/30 09:46 AM

			WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L8	3	"8526898".pn.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/30 09:48 AM
L9	98	Reddy-Madhukar.in.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/30 09:50 AM
L10	41	Reddy-Madhukar.in. AND DFE	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/30 09:50 AM
L11	74	Ling-Curtis.in. AND DFE	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	OR	ON	ON	2022/08/30 09:51 AM

			HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L12	19	"20070032220"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/30 11:45 AM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

To: mhmpto@mcandrews-ip.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 23446

Sep 07, 2022 03:26:49 AM

Dear PAIR Customer:

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SUITE 3400
CHICAGO, IL 60661
UNITED STATES

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Application	Document	Mailroom Date	Attorney Docket No.
17862946	CTNF	09/07/2022	28427US15
	892	09/07/2022	28427US15
	1449	09/07/2022	28427US15

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UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Attorney Docket No. 28427US15

Patent Application of: Madhukar Reddy Application No. 17/862,946 Filed: July 12, 2022 Title: SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL Examiner: JACKSON, BLANE J. Group Art Unit: 2644 Confirmation No.: 7376	**EFS ELECTRONIC FILING** **September 12, 2022**

Amendment

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper responds to the Office Action of September 7, 2022 ("OA"). This response is timely filed. The Applicant respectfully requests reconsideration in view of the following remarks.

Amendments to the Claims begin on page 2.

Remarks begin on page 5.

LISTING OF CLAIMS

1-18 (Cancelled)

19. (Previously Presented) A method for operating a television receiver, comprising:
    receiving, by an input terminal, an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels;
    processing, by a radio front end coupled to the input terminal, the input signal to generate a processed input signal;
    concurrently digitizing, by an analog-to-digital converter (ADC) coupled to the radio front end, all broadcast channels in the processed input signal to generate a digitized signal;
    selecting, by a digital frontend (DFE) coupled to the ADC, the plurality of desired channels from the digitized signal; and
    outputting, by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator extracts information encoded in the digital datastream.

20. (Previously Presented) The method of claim 19, wherein the DFE outputs the digital datastream via a serial interface.

21. (Previously Presented) The method of claim 19, wherein the DFE outputs the digital datastream via a parallel interface.

22. (Previously Presented) The method of claim 19, wherein the ADC comprises:
    a first ADC configured to generate a digital in-phase signal; and
    a second ADC configured to generate a digital quadrature signal.

23. (Previously Presented) The method of claim 19, wherein the extracted information is stored for use in a digital video recorder (DVR).

24. (Previously Presented) The method of claim 19, wherein the extracted information is output for a picture-in-picture display.

25. (Previously Presented) The method of claim 19, wherein the plurality of desired channels comprises at least one television channel.

26. (Previously Presented) The method of claim 19, wherein the plurality of undesired channels comprises at least one television channel.

27. (Previously Presented) The method of claim 19, wherein the broadcast channels comprise satellite broadcast channels.

28. (Previously Presented) The method of claim 19, wherein the broadcast channels comprise cable broadcast channels.

29. (Previously Presented) A television receiver device, comprising:

an input terminal operable to receive an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels;

a radio front end, coupled to the input terminal, operable to process the input signal;

an analog-to-digital converter (ADC), coupled to the radio front end, operable to concurrently digitize all broadcast channels in the processed input signal to generate a digitized signal; and

a digital frontend (DFE), coupled to the ADC, operable to select the plurality of desired channels from the digitized signal and output the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator is operable to extract information encoded in the

digital datastream.

30. (Previously Presented) The television receiver device of claim 29, wherein the DFE is operable to output the digital datastream via a serial interface.

31. (Previously Presented) The television receiver device of claim 29, wherein the DFE is operable to output the digital datastream via a parallel interface.

32. (Previously Presented) The television receiver device of claim 29, wherein the ADC comprises:

a first ADC configured to generate a digital in-phase signal; and
a second ADC configured to generate a digital quadrature signal.

33. (Previously Presented) The television receiver device of claim 29, wherein the extracted information is stored for use in a digital video recorder (DVR).

34. (Previously Presented) The television receiver device of claim 29, wherein the extracted information is output for a picture-in-picture display.

35. (Previously Presented) The television receiver device of claim 29, wherein the plurality of desired channels comprises at least one television channel.

36. (Previously Presented) The television receiver device of claim 29, wherein the plurality of undesired channels comprises at least one television channel.

37. (Previously Presented) The television receiver device of claim 29, wherein the broadcast channels comprise satellite broadcast channels.

38. (Previously Presented) The television receiver device of claim 29, wherein the broadcast channels comprise cable broadcast channels.

REMARKS

The present application includes pending claims 19-38. By preliminary amendment dated July 12, 2022, claims 1-18 were cancelled, and claims 19-38 were added.

The Office Action of September 7, 2022 ("OA") has been carefully considered. However, the OA has only examined cancelled claims 1-18. Examination of pending claims 19-38 is respectfully requested.

Final Matters

The Office Action makes various statements, including without limitation statements regarding the claims, 35 U.S.C. § 101, 35 U.S.C. § 112, the cited references, one of ordinary skill in the art, etc., that are now moot in view of the previously presented amendments and/or arguments. Thus, the Applicant will not address all of such statements at the present time. However, the Applicant expressly reserves the right to challenge such statements in the future should the need arise (*e.g.*, if such statements should become relevant by reappearing in a rejection of any current or future claim or be relied upon in any proceeding involving this application or a corresponding patent). The Applicant also respectfully reserves the right to argue additional reasons that support the allowability of all claims, whether or not argued in this Response or previous responses, should that need arise in the future.

Conclusion

The Applicant submits that the pending claims are in condition for allowance and courteously solicits an expeditious Notice of Allowability with respect to all pending claims. If the Examiner has any questions or the Applicant can be of any assistance, the Examiner is invited to contact the undersigned attorney.

The Commissioner is authorized to charge any necessary fees, or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Account No. 13-0017.

Respectfully submitted,

Dated: September 12, 2022

/Wayne H. Bradley/
Wayne H. Bradley
Reg. No. 39,916

McAndrews, Held & Malloy, Ltd.
500 W. Madison Street
34th Floor
Chicago, Il 60661
Phone (312) 775-8000
Fax (312) 775-8100

Electronic Acknowledgement Receipt

EFS ID:	46593199
Application Number:	17862946
International Application Number:	
Confirmation Number:	7376
Title of Invention:	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL
First Named Inventor/Applicant Name:	Madhukar Reddy
Customer Number:	23446
Filer:	Wayne Bradley/Laura Foley
Filer Authorized By:	Wayne Bradley
Attorney Docket Number:	28427US15
Receipt Date:	12-SEP-2022
Filing Date:	12-JUL-2022
Time Stamp:	10:55:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		28427US15_FINAL_response.pdf	34060 db594673689ea7fc4130c66c89834fe62c1746d3	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Request for Reconsideration-After Non-Final Rejection	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	6
Warnings:			
Information:			
	Total Files Size (in bytes):	34060	

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
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SUITE 3400
CHICAGO, IL 60661

Courtesy Reminder for
Application Serial No: 17/862,946

Attorney Docket No: 28427US15
Customer Number: 23446
Date of Electronic Notification: 09/07/2022

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/862,946	Filing Date 07/12/2022	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
	09/12/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $240 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/VINCENT S BUTLER/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

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23446 7590 09/28/2022
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500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER
JACKSON, BLANE J

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 09/28/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/862,946	07/12/2022	Madhukar Reddy	28427US15	7376

TITLE OF INVENTION: SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	12/28/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

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(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/862,946	07/12/2022	Madhukar Reddy	28427US15	7376

TITLE OF INVENTION: SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	12/28/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
JACKSON, BLANE J	2644	348-731000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/862,946	07/12/2022	Madhukar Reddy	28427US15	7376

23446 7590 09/28/2022
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER
JACKSON, BLANE J

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 09/28/2022

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/862,946	Applicant(s) Reddy et al.	
	Examiner BLANE J JACKSON	Art Unit 2644	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the Remarks filed 12 September 2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 19-38 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/BLANE J JACKSON/
Primary Examiner, Art Unit 2644

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

Claims 19-38 are allowed. The following is a statement of reasons for the indication of allowable subject matter: the prior art made of record teach a receiver for a wireless telecommunication system teach all of the adjacent frequency bands in the IF signal passed by a band pass filter in the radio frontend are converted to a digital signal by an ADC and then separated into their respective frequency bands by a channelizer where the separated frequency bands are processed in the normal manner by subsequent DSP devices, see Claxton et al. US 6,735,421. The prior art made of record do not teach selecting, by a digital frontend (DFE) coupled to the ADC, *a plurality of desired channels* from the digitized signal and outputting by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BLANE J JACKSON whose telephone number is (571)272-7890. The examiner can normally be reached 7:30-4:30 M-TH; 8-2 FRI.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is

encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kathy Wang-Hurst can be reached on 571 270 5371. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BLANE J JACKSON/
Primary Examiner, Art Unit 2644

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/862,946	Reddy et al.
	Examiner	**Art Unit**
	BLANE J JACKSON	2644

CPC - Searched*		
Symbol	**Date**	**Examiner**
H04B 1/001, 1/0007, 1/0014, 1/0028, 1/0035, 1/0042, 1/0046	08/30/2022	BJJ
H04N 5/455, 5/50, 21/4382, 21/4383	08/30/2022	BJJ

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
review of prior continuing patents and IDS; DP to US 10972781 to FAOM	08/30/2022	BJJ
review of Remarks and prior art to issue	09/19/2022	BJJ

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
	no interference listed symbol/ group	09/19/2022	BJJ

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/862,946	Reddy et al.
	Examiner	**Art Unit**
	BLANE J JACKSON	2644

CPC

Symbol					Type	Version
H04N	/	21	/	4263	F	2013-01-01
H04B	/	1	/	0014	I	2013-01-01
H04N	/	5	/	50	I	2013-01-01
H04N	/	21	/	4383	I	2013-01-01
H04N	/	21	/	4382	I	2013-01-01
H04N	/	21	/	6193	I	2013-01-01
H04N	/	21	/	6143	I	2013-01-01
H04N	/	5	/	455	I	2013-01-01
H04N	/	21	/	454	I	2013-01-01

CPC Combination Sets

Symbol					Type	Set	Ranking	Version
	/		/					

NONE (Assistant Examiner) (Date)		**Total Claims Allowed:** 20	
/Blane J Jackson/ (Primary Examiner)	19 September 2022 (Date)	O.G. Print Claim(s) 19	O.G. Print Figure 2

U.S. Patent and Trademark Office Part of Paper No.: 20220919

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/862,946	Reddy et al.
	Examiner	**Art Unit**
	BLANE J JACKSON	2644

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H04B	/	1	/	16
H04B	/	1	/	0028

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner) (Date)		**Total Claims Allowed:** 20	
/Blane J Jackson/ (Primary Examiner)	19 September 2022 (Date)	O.G. Print Claim(s) 19	O.G. Print Figure 2

U.S. Patent and Trademark Office Part of Paper No.: 20220919

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/862,946	Reddy et al.
	Examiner	**Art Unit**
	BLANE J JACKSON	2644

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10	1	19	10	28	19	37						
	2		11	2	20	11	29	20	38						
	3		12	3	21	12	30								
	4		13	4	22	13	31								
	5		14	5	23	14	32								
	6		15	6	24	15	33								
	7		16	7	25	16	34								
	8		17	8	26	17	35								
	9		18	9	27	18	36								

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 20	
/Blane J Jackson/ (Primary Examiner) 19 September 2022 (Date)	O.G. Print Claim(s) 19	O.G. Print Figure 2

U.S. Patent and Trademark Office Part of Paper No.: 20220919

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	21	"9100622".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/16 11:31 AM
L2	5	"6735421".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/16 11:46 AM
L3	11	"20090075613"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 01:29 PM
L4	98	Reddy-Madhukar.in.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2022/09/19 01:31 PM

			CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L5	928	Ling-Curtis.in.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 01:33 PM
L6	74	Ling-Curtis.in. AND DFE	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 01:34 PM
L7	22	Gallagher-Tim.in. AND DFE	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA,	OR	ON	ON	2022/09/19 01:34 PM

			VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: 28427US15

Patent Application of:	)	
Madhukar Reddy	)	
	)	
Application No. 17/862,946	)	**Filed electronically on September 28, 2022**
	)	
Filed: July 12, 2022	)	
	)	
Title: SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	)	
	)	
Examiner: JACKSON, BLANE J.	)	
	)	
Group Art Unit: 2644	)	
	)	
Confirmation No.: 7376	)	

POST ALLOWANCE INCOMING LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

On July 12, 2022, Applicants filed via EFS, a Track 1 continuation application, inadvertently paying small entity fees. Applicant is hereby notifying the Patent and Trademark Office that the above patent application was not entitled to small entity status, and all additional large entity fees are being authorized for payment from the deposit account.

The Commissioner is hereby authorized to charge any fees required by this submission including any extra claims fees, to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

Dated: September 28, 2022

/Wayne H. Bradley/
Wayne H. Bradley
Reg. No. 39,916

McAndrews, Held & Malloy, Ltd.
500 W. Madison Street
34th Floor
Chicago, Il 60661
Phone (312) 775-8000
Fax (312) 775-8100

Electronic Acknowledgement Receipt

EFS ID:	46714793
Application Number:	17862946
International Application Number:	
Confirmation Number:	7376
Title of Invention:	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL
First Named Inventor/Applicant Name:	Madhukar Reddy
Customer Number:	23446
Filer:	Wayne Bradley/Laura Foley
Filer Authorized By:	Wayne Bradley
Attorney Docket Number:	28427US15
Receipt Date:	28-SEP-2022
Filing Date:	12-JUL-2022
Time Stamp:	16:56:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	28427US15_Post_Allowance_Transmittal.pdf	20914 93c2af57ff60f539fd30d3b22b541a03daad84d8	no	2

Warnings:

Information:	
Total Files Size (in bytes):	20914

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
17/862,946	07/12/2022	Madhukar Reddy	28427US15	175222

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 09/28/2022 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

☒ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Wayne H. Bradley/
Name:	Wayne H. Bradley
Registration Number:	39916

To: mhmpto@mcandrews-ip.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 23446

Sep 28, 2022 03:22:24 AM

Dear PAIR Customer:

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500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661
UNITED STATES

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Application	Document	Mailroom Date	Attorney Docket No.
17862946	NOA	09/28/2022	28427US15

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Monday - Friday 6:00 a.m. to 12:00 a.m.

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UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: 28427US15

Patent Application of:	)	
Madhukar Reddy	)	
	)	
Application No. 17/862,946	)	**Filed electronically on September 29, 2022**
	)	
Filed: July 12, 2022	)	
	)	
Title: SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL	)	
	)	
Examiner: JACKSON, BLANE J.	)	
	)	
Group Art Unit: 2644	)	
	)	
Confirmation No.: 7376	)	

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop: Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper responds to the Notice of Allowance mailed September 28, 2022 in the above-identified application (the "Application"). Applicants respectfully request entry of the following remarks in the record.

REMARKS

Claims 19-38 are allowed in the Notice of Allowance mailed on September 28, 2022. The Applicant thanks the Examiner for positive consideration of the claim.

However, during the course of prosecution of the Application the Examiner may have provided various reasons for allowing claims 19-38. The Applicants do not agree or disagree at this time with those reasons, but respectfully reserve the right to support or traverse those reasons should the need arise, and argue different reasons for the allowability of the claims.

Respectfully submitted,

Dated: September 29, 2022

/Wayne H. Bradley/
Wayne H. Bradley
Reg. No. 39,916

McAndrews, Held & Malloy, Ltd.
500 W. Madison Street
34th Floor
Chicago, Il 60661
Phone (312) 775-8000
Fax (312) 775-8100

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23446 7590 09/28/2022
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Wayne H. Bradley	(Typed or printed name)
/Wayne H. Bradley/	(Signature)
September 29, 2022	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/862,946	07/12/2022	Madhukar Reddy	28427US15	7376

TITLE OF INVENTION: SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	~~$600~~ ~~XXXX~~ $1200	$0.00	$0.00	~~$600~~ ~~XXXX~~ $1200	12/28/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
JACKSON, BLANE J	2644	348-731000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 McAndrews, Held & Malloy, Ltd.
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Entropic Communications, LLC	New York, NY

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 13-0017

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☒ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Wayne H. Bradley/ Date September 29, 2022

Typed or printed name Wayne H. Bradley Registration No. 39,916

Electronic Patent Application Fee Transmittal

Application Number:	17862946
Filing Date:	12-Jul-2022
Title of Invention:	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL
First Named Inventor/Applicant Name:	Madhukar Reddy
Filer:	Wayne Bradley/Laura Foley
Attorney Docket Number:	28427US15

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1200**

Electronic Acknowledgement Receipt	
EFS ID:	46717530
Application Number:	17862946
International Application Number:	
Confirmation Number:	7376
Title of Invention:	SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL
First Named Inventor/Applicant Name:	Madhukar Reddy
Customer Number:	23446
Filer:	Wayne Bradley/Laura Foley
Filer Authorized By:	Wayne Bradley
Attorney Docket Number:	28427US15
Receipt Date:	29-SEP-2022
Filing Date:	12-JUL-2022
Time Stamp:	06:06:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1200
RAM confirmation Number	E20229S707042968
Deposit Account	130017
Authorized User	Laura Foley
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	28427US15_Comments_on_Reasons_for_Allowance.pdf	21758 56ca9a0453663910ccb5ee2c637be061cc9d9c8c	no	2
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	28427US15_issue_fee_transmittal.pdf	992073 e3b34dfaea9c1d5ae672be0b4e3fb000d2d70511	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	37950 0866e9f7d2fef001791c0c7a80ddca68139e8f14	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1051781		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/862,946	11/01/2022	11490152	28427US15	7376

23446 7590 10/12/2022
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site http://pair.uspto.gov for additional inventors):

Madhukar Reddy, Carlsbad, CA;
Curtis Ling, Carlsbad, CA;
Tim Gallagher, Carlsbad, CA;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Entropic Communications, LLC, New York, NY;

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IR103 (Rev. 10/09)

To: mhmpto@mcandrews-ip.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 23446

Oct 13, 2022 06:06:09 AM

Dear PAIR Customer:

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Application	Document	Mailroom Date	Attorney Docket No.
17862946	ISSUE.NTF	10/12/2022	28427US15

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/862,946	07/12/2022	Madhukar Reddy	28427US15

CONFIRMATION NO. 7376

23446
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

PUBLICATION NOTICE

OC000000137228035

Date Mailed: 11/03/2022

Title:SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL

Publication No.US-2023-0353564-A1
Publication Date:11/03/2022

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/862,946	07/12/2022	Madhukar Reddy	28427US15

CONFIRMATION NO. 7376

23446
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

PUBLICATION NOTICE

OC000000137228035

Date Mailed: 02/14/2023

Title:SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL

Publication No.US-2022-0353564-A1
Publication Date:11/03/2022

NOTICE OF PUBLICATION OF APPLICATION

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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