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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	RFM-30 P
		Application Number	
Title of Invention	Channel Stacking System and Method of Operation		
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				☐ Party of Interest under 35 U.S.C. 118	
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Title of the Invention	Channel Stacking System and Method of Operation		
Attorney Docket Number	RFM-30 P	Small Entity Status Claimed ☐	
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		Application Number	
Title of Invention	Channel Stacking System and Method of Operation		
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Title of Invention	Channel Stacking System and Method of Operation		

Signature	/CliffordBPerry43854/		Date (YYYY-MM-DD)	2008-05-21	
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Channel Stacking System and Method of Operation

BACKGROUND

[0001] The present invention relates to systems and methods for constructing composite signals, and in particular, systems and methods for assembling a desired sequence of channels to form a composite signal.

[0002] Present satellite receiving systems employ multiple downconversion processes. For example, USPN 7,130,576 to Gurantz et al. discloses a two stage downconversion process; a first downconversion in the LNB stage, and a second downconversion stage at IF frequencies. Multi-downconversion systems suffer from the disadvantages of increased circuit complexity and high power consumption.

[0003] Furthermore, the processing of selecting and extracting channels from multiple sources (e.g., satellites) and assembling said channels into a desired sequence is a process which presently employs analog techniques. Such processing is more advantageously employed in the digital domain exclusively, and without the necessity of bandpass filtering or Hilbert Transformers.

SUMMARY OF THE INVENTION

[0004] The present invention provides for a channel stacking system which employs a single downconverter stage and which processes channel selection, extraction and sequencing within the digital domain. A single analog domain downconversion process is employed between reception of the input RF signal and generation of a composite digital signal having the desired sequence. Furthermore, the disclosed system provides for a channel extraction and conversion circuit operable to generate a composite digital signal of a desired channel sequence.

[0005] A channel stacking system in accordance with the invention includes first and second downconverting stages, first and second analog to digital converters, and a signal processor. The first downconverting stage includes a first downconverter circuit having an input for receiving a first RF input signal which includes a multitude of first channels. The first downconverter circuit is operable to frequency downconvert the first RF input signal to a first IF signal which includes the multitude of first channels. The first analog-to-digital converter is operable to convert the first IF signal to a first digital IF signal. The second downconverter stage includes a second downconverter circuit having an input for receiving a second RF input signal which includes a multitude of second channels. The second downconverter circuit is operable to frequency downconvert the second RF input signal to a second IF signal including said multitude of second channels. The second analog-to-digital converter is operable to convert the second IF signal to a second digital IF signal. The signal processor is coupled to receive each of the first and second digital IF signals, and is operable to assemble at least one of the first channels and at least one of the second channels into a digital composite signal.

[0006] These and other features of the invention will be more completely understood when viewed in light of the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] **Fig. 1** illustrates an exemplary embodiment of a channel stacking system in accordance with the present invention.

Fig. 2 illustrates the first and second downconverter circuits shown in the channel stacking system of Fig. 1.

Figs. 3A and 3B illustrate exemplary embodiments of the signal processor 150 shown in the channel stacking system of Fig. 1.

Fig. 4 illustrates the upconverter circuit shown in the channel stacking system of Fig. 1.

Fig. 5 illustrates a second exemplary embodiment of a channel stacking system in accordance with the present invention.

Fig. 6 illustrates a third exemplary embodiment of a channel stacking system in accordance with the present invention.

Fig. 7 illustrates a fourth exemplary embodiment of a channel stacking system in accordance with the present invention.

Fig. 8 illustrates a fifth exemplary embodiment of a channel stacking system in accordance with the present invention.

Fig. 9 illustrates portions of an exemplary downconverter stage in accordance with one embodiment of the present invention.

Fig. 10 illustrates a further exemplary embodiment of a first downconverter stage in accordance with one embodiment of the invention.

Fig. 11 illustrates a further exemplary embodiment of a third downconverter stage in accordance with one embodiment of the invention.

Fig. 12 illustrates an interference cancellation circuit in accordance with the present invention.

Fig. 13 illustrates steps to measure the phase and amplitude level of cross polarization in accordance with the invention.

For clarity, previously-described features retain their reference numbers in subsequent drawings.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0008] **Fig. 1** illustrates an exemplary embodiment of a channel stacking system 100 in accordance with the present invention. The system 100 operates to “stack” or assemble channel resident within an RF signal into a digital composite signal in which the received channels are placed (or sequenced) in desired channel slots for output to a rendering device, such as a set-top box, or other receiver/tuner.

[0009] The channel stacking system 100 includes first and second downconverter stages 110 and 120, and a signal processor 150. The invention is not limited in the number of parallel downconverting stages employed, and the system 100 may include any plurality of parallel downconverting stages, for example, 2, 3, 4, 6, 8, 16, 24, 32, 48, 60, 120, or more. In a particular embodiment of the invention, the signal processor 150 is

implemented as a digital signal processor. In another embodiment, the signal processor 150 is an application specific integrated circuit (ASIC), which may include a Radio-Frequency IC (RFIC). Those skilled in the art will appreciate that other circuits/devices (e.g., programmable gate arrays, etc.) may be used to implement the below-described functions of the signal processor 150, and accordingly, such alternatives may be implemented as well for signal processor 150.

[0010] The first downconverting stage 110 includes a first downconverter 113 having an input 113a for receiving a first RF input signal 102 including a plurality of first channels 102a, 102b, the first downconverter 113 operable to frequency downconvert the first RF input signal 102 to a first IF signal 114 including the plurality of first channels 102a, 102b. Frequency source 10 is operable to provide a reference signal for the downconversion operation. The first downconverting stage 110 further includes a first analog-to-digital converter (ADC) 116 operable to convert the first IF signal 114 to a first digital IF signal 118. The ADC 116 may be of a conventional design to provide the required amount of signal resolution, e.g., be at least 4 bits wide using a clocking frequency at or above the Nyquist rate determined by the downconverted signal supplied thereto. In one embodiment, the RF signal 102 is divided by means of a signal splitter 20 into two signals, which are subsequently downconverted by quadrature-phased reference signals supplied from source 10 into quadrature-phased I and Q signals. In such an embodiment, subsequent I and Q anti-aliasing filters 115 and ADCs 116 are used to process the respective I and Q signals 114.

[0011] In one embodiment of the invention, an “RF signal” is a signal having a center frequency above the frequency range of 3 GHz. RF signals may include signals having a center frequency within the range of 3-40 GHz, more particularly in the range of 5-30 GHz, and even more particularly in the range of 8-26 GHz. In an exemplary embodiment, RF signals include X/Ku/Ka-band signals which may be received from orbital satellites. The X/Ku/Ka bands are exemplified by the frequency ranges of 7 GHz to 12.5 GHz for X-band, 10.7 GHz - 12.75 GHz for Ku-band, and 17.3 GHz – 20.3 GHz for Ka-band.

[0012] Further exemplary, an “IF signal” is a signal having a center frequency below the frequency range of 3 GHz, including baseband (0 Hz center frequency) signals. In particular embodiment, IF signals include signals having a center frequency within the range of 0-2.5 GHz, more particularly, 0-1 GHz, and more particularly 0-500 MHz. As the skilled person will appreciate, the modulation/channel information included within the IF signal will extend beyond the center frequency of the IF signal, and the bandwidth of the IF signal may extend several hundreds of megahertz, a gigahertz, or more. However, the IF center frequency will be below 3 GHz as defined above. In an exemplary embodiment, IF signals include L-band signals (e.g., 950 MHz- 2150 MHz) which are received from a system operable to downconvert satellite signals. In another embodiment, an “IF signal” refers to a signal which has undergone a previous frequency translation within the channel stacking system of the present invention, and an RF signal refers to a signal which has not undergone a previous frequency translation within the channel stacking system of the present invention.

[0013] The second downconverting stage 120 is constructed similarly to the first downconverting stage 110, and includes a second downconverter 123 having an input 123a for receiving a second RF input signal 104 including a plurality of second channels 104a, 104b, the second downconverter 123 operable to frequency downconvert the second RF input signal 104 to a second IF signal 124 including the plurality of second channels 104a, 104b. The second downconverting stage further includes a second analog-to-digital converter 126 operable to convert the second IF signal 124 to a second digital IF signal 128.

[0014] Further particularly, at least one of the first downconverting stage 110, or the second downconverting stage 120 is operable as a single analog domain downconversion stage, whereby the first or second downconverter 113 of 123 included therein is operable as the only analog domain downconverting stage for downconverting the RF input signal 102 or 104 received thereby into an IF signal 118 or 128 produced thereby. In a particular embodiment, each of the first and second downconverting stages 110 and 120 operate as a respective single downconverting stage for the signals processed thereby.

[0015] The digital signal processor 150 is coupled to receive each of the first and second digital IF signals 118 and 128, each of these signals including at least one of their respective first and second channels. The digital signal processor 150 is operable to assemble at least one of the first channels 102a, 102b and at least one of the second channels 104a, 104b into a digital composite signal 158. In a particular embodiment of the invention further described below, the digital signal processor 150 is operable to perform digital filtering, digital frequency translation, and digital signal combining operations in order to extract and order at least one of the first plurality of channels and at least one of the plurality of second channels into the desired channel slot positions.

[0016] The number of first or second channels included in the first or second RF input signals 102 or 104 and/or their respective bandwidths may vary. For example, for the RF input signals 102 and 104, the collective channel bandwidth may be in the range of 100 MHz - 5 GHz, or more particular between 500 MHz – 2 GHz. As an example, the first and second channels may number 28 channels, each at 40 MHz wide, or alternatively may number 40 channels, each channel 29 MHz wide. Further exemplary, 2 GHz wide satellites typically employ 60 transponders per polarization, each channel ranging in bandwidth generally from 6-30 MHz, typically with one channel per transponder. The number of channels may be 4, 6, 8, 16, 24, 28, 32, 40, 48, 60, 120 or more.

[0017] Optional components of the first downconverting stage 110 include an RF amplifier 111 (exemplary a three stage amplifier) operable to provide signal amplification at the input RF frequency of the first input signal 102 (exemplary, X/Ku/Ka band frequencies). Further optionally, an RF filter 112 (exemplary, a bandpass filter) is employed to attenuate out-of-band RF frequency signals which may be present at the input. The first downconverting stage 110 may optionally include an IF filter 115 (exemplary a low pass filter) operable to attenuate signals outside of the downconverted/IF band. Further to the aforementioned embodiment in which the collective channel bandwidth is 2 GHz wide, each of the RF and IF filters similarly provide 2 GHz of passband in order to provide all received channels to the digital signal processor 150. Particular embodiments of the RF and IF filters 112 and 115 include

filters having a fixed or tunable passband width or center (or cutoff) frequency. In an alternative embodiment, the RF and/or IF filters 112, 115 may have a passband which is less than the collective channel bandwidth, i.e., the RF and/or IF filters 112, 115 operates to attenuate/reject at least one of the received channels. Further particularly, the RF and/or IF filters 112, 115 may be tunable and have a passband to pass substantially only one channel. The second downconverting stage 120 is constructed similarly to the first downconverting stage 110, and optionally includes a n RF stage amplifier 121, an RF filter 122, and an IF filter 125, each of which may be of the same construction, type, and operation as the corresponding components of the first downconverting stage 110.

[0018] Several different downconverter architectures may be employed in accordance with the present invention. In one exemplary embodiment shown, each of the first and/or second downconverters 110, 120 are arranged to provide quadrature phase (I and Q) downconverted signals to allow subsequent image rejection, when, for example, the reference frequency (LO) signal places image signals within the band of the downconverted IF signals 114 and 128. In a particular embodiment, the LO frequency may be located midway within the modulation bandwidth of the RF input signal to relax output filtering to a corresponding one-half of the modulation bandwidth, with the subsequent I and Q stage ADCs operating at a clock frequency of at least the clock frequency corresponding to the highest modulating frequency of the input RF signal.

[0019] As an example, first and second downconverter stages 110 and 120 are coupled to receive Ku-band frequency signals operating over the frequency range of 10.7-12.75 GHz. The first downconverter 113 processes the lower band half 10.7-11.725 GHz using a quadrature phase LO signal operating at approximately 11.2125 GHz to provide I and Q zero-IF downconverted baseband signals of approximately 512 MHz bandwidth. Similarly, the second downconverter 123 processes the upper band half 11.725-12.75 GHz using a quadrature phase LO signal operating at 12.2375 GHz to provide I and Q zero-IF downconverted baseband signals of approximately 512 MHz bandwidth. ADCs 116 and 126, each a pair of ADCs, operate at 1.2 GHz clock frequency to convert the quadrature phase IF signals 114, 124 to digital quadrature phase IF signals 118, 128.

[0020] Further exemplary, the system 100 includes a third downconverting stage 130. The third downconverting stage 130 includes a third downconverter 133 having an input 133a for receiving a third RF input signal 106 including a plurality of third channels 106a, 106b, the second downconverter 133 operable to frequency downconvert the third RF input signal 106 to a third IF signal 134 including the plurality of second channels 106a, 106b. The third downconverting stage further includes a third analog-to-digital converter 136 operable to convert the third IF signal 134 to a third digital IF signal 138.

[0021] In a particular embodiment of the invention, the first, second, and third IF signals 114, 124, and 134 operate at substantially the same IF frequency. In one embodiment, the first, second and third IF signals 114, 124, and 134 operate at zero IF frequency, whereby the bandwidth of the IF signal is centered at 0 Hz. As noted above, the bandwidth of the IF signal may extend several hundreds of megahertz for channels located at the outer ends of the IF signal spectrum.

[0022] In another embodiment, the first, second and third IF signals 114, 124, and 134 operate at a “low” IF frequency, i.e., having a center frequency which is offset from 0 Hz, such that the entire signal BW falls above DC, as described further below. Also shown, the first, second or third analog-to-digital converters (ADCs) 116, 126 and 136 may be realized as ADC pairs for processing I and Q channels of one quadrature IF signal pair 114, 124 and 134. These ADCs may be of a conventional design to provide the required amount of signal resolution, e.g., be at least 4 bits wide using a clocking frequency or above the Nyquist rate determined by the downconverted signal supplied thereto. Filters, e.g. lowpass filters, may be implemented prior to the ADCs to attenuate any out-of-band interference and prevent aliasing.

[0023] The second downconverter 123 includes an input 123a for receiving a second input signal 104 having a plurality of second channels 104a, 104b. The second downconverter circuit 123 is operable to frequency downconvert the second input signal 104 to a second IF signal 124 which includes the first channels 102a, 102b. As above with the first downconverter circuit 113, the second downconverter circuit 123 may be

arranged to provide quadrature phase (I and Q) signals, in which case the second IF signal 128 is provided as a quadrature phase signal pair. The number of first channels included in the first signal 104, and/or their respective bandwidths may also vary, a particular embodiment of which, for example with 500 MHz wide satellite would include 16 channels (i.e. transponders), each channel 29 MHz wide. The number of third channels included in the signal 106, and/or their respective bandwidths may also vary, a particular embodiment of which, for example a 1200 MHz wide band would include 28 channels, each at 40 MHz wide, or 40 channels, each channel 29 MHz wide. Further exemplary, the number of channels may be 4, 6, 8, 16, 24, 28, 32, 40, or 48. For wider satellites, for example of 1GHz BW, or 2 GHz BW and more, 60, 120, or more channels may be used.

[0024] The second analog-to-digital converter (ADC) 126 is substantially identical in function and operation with the first ADC 116, the second ADC operable to convert the second IF signal 124 into a second digital IF signal 128. Optional filters may be implemented prior to the ADC 126 to reject any out-of-band interference.

[0025] The system 100 further includes a digital signal processor 150 coupled to receive each of the first and second digital IF signals 118, 128. The digital signal processor 150 is operable to assemble at least one of the first channels 102a, 102b and at least one of the second channels 104a, 104b into a composite signal 158, provided in one embodiment as a pair of quadrature phase signals 158a, 158b. The digital signal processor 150 includes digital filters, channel extraction and sequencing means and signal combining means operable to assemble a composite signal 158 having the desired channels in the desired order. For example, channel extraction in one embodiment is performed by direct digital conversion to zero IF, followed by channel filters. In one exemplary embodiment, assembling channels into composite signal includes direct digital upconversion to the required location in the frequency stacked channel lineup. The channel assembly process occurs in the digital domain, and accordingly, can be modified relatively easily by programming means to generate a different composite signal populated by different

channels and/or in a different sequence. This channel assembly and sequencing process is further described below.

[0026] In a particular embodiment of the invention, the first and second downconverter stages 110, 120 and/or 130 operate as a single analog domain downconversion stage which the channel stacking system 100 employs to assemble the composite signal 158 from received input signals 102 and 104, signals 102 and 104 being satellite signals in one embodiment, e.g., signals in the X/Ku/Ka frequency bands. Specifically, only a single analog domain downconversion is performed between receiving the RF input signals 102 and the sequenced output signal 158.

[0027] In one embodiment, the first and second downconverter stages 110 and 120 are operable to receive satellite frequency signals, e.g., in the X/Ku/Ka bands. In such an embodiment, a satellite antenna dish and pre-downconversion stage amplifiers and filters may be implemented to collect, amplify, and filter each of the first and second input signals 102 and 104 prior to input into each of the first and second downconverter stages 110 and 120.

[0028] In another embodiment, at least one of the input signals is externally-supplied at a carrier frequency or format which differs from that of the first input signal 102. For example, the first input signal 102 may operate with a carrier frequency within the range of the X/Ku/Ka bands, and the second input signal 106 may operate at a carrier frequency within the L band range. Further exemplary, the externally-supplied signals similarly include a plurality of channels 106a, 106b, specific embodiments of the channels including the aforementioned examples for channels located within input signal 102 and 104. The aforementioned second downconverter circuit may be implemented as downconverter circuit 133 having an input 133a operable to receive input signal 106 106. Second downconverter circuit 133 would be operable to downconvert respective input signal 106 to a second downconverted signal 138 having channels 106a, 106b, the second downconverted signal 134 converted into a second digital IF signal 138 by means of second ADC 136. In such an embodiment, the first and second downconverter stages 110

and 130 operate using different reference frequencies in order to downconvert their respective input signals 102 and 106 to signals 118 and 138.

[0029] In one embodiment, the first and second digital IF signals 118, 128, 138 are each zero IF signals. In another embodiment, the first and second digital IF signals 118, 128, 138 operate at a low IF frequency. A “low” IF frequency typically refers to a frequency which is offset from 0 Hz, such that the center frequency and the entire signal BW is contained above DC. Typically the low end of the signal BW is placed near DC (but excludes the DC and it’s immediate close-by frequencies, typically a range of a few hundred kHz or a few MHz, to avoid the adverse effects of the well-known low frequency flicker noise and/or DC leakage terms), in order to minimize the occupied frequency range, thus minimizing the required ADC sampling rate. Further particularly, the system 100 operates as a single downconversion system, whereby only one downconversion occurs in a signal path between reception of the input signals 102, 104, 106 and construction of the composite signal 158. In the illustrated embodiment, the first and second downconverter stages 110, 120, 130 operate as the single downconversion stages for their respective input signals.

[0030] Optionally, the channel stacking system 100 includes post-DSP processing circuits to return the composite signal to the analog domain and/or to re-modulate the signal to a format compliant with a desired signal protocol or standard, for example in a format of a “Multimedia over Coax Alliance” (MoCA) standard, or Ethernet IP TV. In the exemplary embodiment shown in Fig. 1, the system 100 optionally includes first and second digital-to-analog converters (DACs) 160, 170, and an upconverter 180. The first and second DACs 160 and 170 are coupled to receive a respective one of the digital quadrature phase signals 158a, 158b and respective clock signals, each operable to produce a respective one of two quadrature phase analog composite signals 168, 178. The upconverter 180 is coupled to receive both quadrature phase composite analog signals 168, 178, and is operable to produce an upconverted composite signal 188. In a specific embodiment, the DSP 150 outputs quadrature phase signals 158a, 158b at baseband, and the upconverter 180 frequency translates the quadrature phase composite

signals 168, 178 from baseband to the L-band frequency range which can be feed into a receiver, such as a television set top box (STB) or the like. Of course, the upconverter can provide translations to other frequencies as well. Signal demodulation can be performed, followed by remodulation in a different format, such as quadrature amplitude modulation. Furthermore, the DSP and/or upconverter can be used to provide carrier frequency or modulation characteristics consistent with that of a particular signal protocol, such as Internet Protocol or the Multimedia over Coaxial Alliance standard. The channel stacking system 100 may be implemented as an outdoor unit (ODU) as part of a satellite receiving system, such a system provided proximate to the satellite antenna.

[0031] **Fig. 2** illustrates exemplary embodiments of the first and second downconverter circuits 113, 123, 133 shown in the channel stacking system of Fig. 1, with previous features retaining the reference indicia. Referring to the detail of the first downconverter circuit 113 first, the downconverter 113 includes a frequency source 10, a 90-degree phase shifter 14, mixers 16 and 18, signal splitter 20, and amplifiers 22a-c. Frequency source 10, which may be fixed for variable, provides a reference frequency 12 to the 90-degree phase shifter 14 (e.g., a 90-degree hybrid coupler), which supplies 0 and relative 90-degree phase shifted versions of the reference frequency 12 to each of mixers 16 and 18. First input signal 102 is amplified and split to supply each of mixers 16 and 18 therewith. Mixers 16 and 18 accordingly generate quadrature phase downconverted signals 114a and 114b via amplifiers 22b and 22c, respectively. The frequency source 10 may be set to provide a signal 12 of any particular reference frequency. In one embodiment, the frequency source 10 is operable to provide a signal 12 at a frequency for directly downconverting to baseband the input signal 102. In another embodiment, the frequency source 10 is operable to provide a signal 12 at a frequency for downconverting the input signal 102 to low IF.

[0032] The operation and construction of the second downconverter circuit 123 (or 133) is substantially the same as the first downconverter circuit 113. In particular, a frequency source is used to generate a reference frequency which is split into quadrature phase signals supplied to two mixers. Input signal 104 (or 106) is split and supplied to the two

mixers, which produce quadrature phase downconverted signals 124a and 124b (or 134a and 134b). The frequency source may be fixed or variable frequency and operated to provide a reference frequency used to directly downconvert to zero IF or downconvert to near zero IF (low IF) the input signal.

[0033] **Figs. 3A and 3B** illustrate exemplary embodiments of the signal processor 150 shown in the channel stacking system of Fig. 1. In a particular embodiment, the signal processor 150 includes respective I and Q switch matrices 302 and 304 and one or more (n shown) channel extractor/converter circuits 300. As will be described in further detail below, the channel extractor/converter circuits 300, 350 are operable to extract a desired channel and to locate or place it in the desired channel slot of the output signal 158. Exemplary, the number of parallel-connect channel extractor/converter circuits will be equal to the number of available channels (i.e., channel slots) in the output signal 158 (e.g., 4, 6, 8, 16, 24, 28, 32, 40, 48, 60, 120 or more channels), although in other embodiments a larger or smaller number of channel extractor/converter circuits may be employed within the signal processor 150 as well. Further exemplary, the signal processor 150 employs both types of channel extractor/converter circuits 300 and 350, or may employ an architecture which can be configured to either of the circuits 300 and 350, as will be further described below.

[0034] The spectrum at the I and Q outputs of the zero IF downconverter 110 of Fig. 1 is folded around DC, because the LO frequency falls inside the input signal band, typically in the middle of the input BW. Because of this spectral folding, both I and Q signals contain a linear combination of the channels originating from the image frequencies at Ka/Ku Band (images are in respect to the RF LO source 10 at Ku/Ka frequency): LI (Lower Image) and UI (Upper Image). The channel extraction and placement method in the present invention is accomplished in two steps: the first step is to extract the desired image (LI or UI) channels from the incoming signals, and the second step is to upconvert and place these channels to the desired output frequency.

[0035] Two cases may be considered under the foregoing conditions: in a first case, when the RF LO 10 frequency is located in-between two RF channels (i.e. transponders), and a second case, when the RF LO 10 frequency falls inside the BW of a channel/transponder.

[0036] **Fig. 3A** shows an exemplary embodiment of the digital signal processor 150 employing a channel extractor/converter circuit 300 configured for the first case, when the RF LO is in-between two channels (ZIF output is folded at DC, in-between channels). The channel extractor/converter circuit 300 includes two processing stages 307 and 309, each of which is further described below. **Fig. 3B** shows an exemplary embodiment of the –digital signal processor 150 employing a channel extractor/converter 350 in the second case, when the RF LO falls inside of a channel (the channel is then folded around DC at ZIF output). A preferred location of the LO frequency in this case is around the middle of the channel. In this embodiment, the channel extractor/converter circuit 350 includes processing stage 359, which in an exemplary embodiment is identical to processing stage 309 of the channel extractor/converter circuit 300 illustrated in Fig. 3A. Exemplary, the same digital circuit (e.g., channel extractor/converter circuit 300 of Fig. 3A) can be used for both channel extractor/converter circuits 300 and 350, for instance, by bypassing the first stage 307 to configure circuit 300 into that of circuit 350, or reconfiguring the circuit into 300 from the circuit 350 configuration, as may be needed. The reconfiguration in this case means either engaging or bypassing stage 307, using, for example, digital multiplexers or switches when a digital signal processor is the platform.

[0037] Channel extraction from the incoming signal and placement to the desired output frequency/channel slot can be explained with the help of the following analysis.

[0038] Designating the angular frequency of the LO source 10 in Fig. 1 with ω_{RF} , the LI and UI channels of the incoming RF satellite signal (at point 20 in downconverter 110) can be represented with:

$$\cos(\omega_{RF} - \omega_{LI})t + \cos(\omega_{RF} + \omega_{UI})t \dots (1)$$

[0039] Where $\omega_{LI} = \omega_{UI}$, representing the angular frequencies of the image channels relative to the LO frequency ω_{RF} , equally spaced from this LO frequency. The first term in equation (1) represents the lower image (LI) channel, and the second term the upper image (UI) channel, measured in respect to the LO frequency ω_{RF} .

[0040] Regarding the channel extractor/converter embodiment shown in Fig. 3A, the in-phase signal Ik 310 and the quadrature signal Qk 320 are obtained by downconverting the satellite signals in the quadrature downconverters 110, 120, 220, etc. in Fig. 1.

Downconversion is accomplished by multiplying the satellite signals with the in-phase and quadrature LO signals, then low-pass filtering in anti-aliasing filters and digitizing the signals in the ADCs and then selecting/routing the desired signal source by the matrix switches 302 and 304. While the signals Ik 310 and Qk 320 at this point are digital, for the purpose of analysis the signals can be expressed with the following equations (for simplicity, scale factors such as $\frac{1}{2}$, 2, etc. have been omitted in all equations):

[0041] The in-phase signal Ik at 310:

$$[\cos(\omega_{RF} - \omega_{LI})t + \cos(\omega_{RF} + \omega_{UI})t] \cdot \cos(\omega_{RF}t) = \cos(\omega_{LI}t) + \cos(\omega_{UI}t) \dots (2)$$

[0042] Where the sum frequency terms $\sim 2 \cdot \omega_{RF}$ are removed because the signal is low pass filtered.

[0043] Similarly, the quadrature signal Qk at 320:

$$[\cos(\omega_{RF} - \omega_{LI})t + \cos(\omega_{RF} + \omega_{UI})t] \cdot \cos(\omega_{RF}t - 90^\circ) = \cos(\omega_{LI}t - 90^\circ) + \cos(\omega_{UI}t + 90^\circ) \dots (3)$$

[0044] From eqs. (2) and (3) it can be seen that the Ik and Qk terms contain a linear combination of two channels falling on the same frequency ω_{LI} or ω_{UI} ($\omega_{LI} = \omega_{UI}$), originating from image frequencies at Ka/Ku band.

[0045] Next, with a digital LO signal 315 at the frequency f_k (corresponding to angular frequency ω_k , which is selected to be equal to ω_{LI} and ω_{UI} : $\omega_k \approx \omega_{LI} = \omega_{UI}$, i.e. ω_k is in the middle of the channel BW represented by ω_{LI} or ω_{UI}), the I_k and Q_k are downconverted to zero IF as follows:

[0046] The in-phase signal I_k from 310 is converted to zero IF by multiplying the right-hand side of eq. (2) by the in-phase LO = $\cos(\omega_k t)$ and low-pass filtering in 311, which removes the sum terms, the signal at 312 is then:

$$\cos(\omega_{LI} - \omega_k)t + \cos(\omega_{UI} - \omega_k)t \dots (4)$$

[0047] The quadrature signal Q_k from 320 is downconverted by multiplying the right-hand side of eq. (3) by quadrature LO = $\cos(\omega_k t - 90^\circ)$ and low-pass filtering, yielding at 314:

$$\cos(\omega_{LI} - \omega_k)t - \cos(\omega_{UI} - \omega_k)t \dots (5)$$

[0048] The cutoff frequency of the low pass filters (311) are set at about half the channel BW, so that the difference terms containing folded channel BW are passed, while the sum terms at $\sim 2 \cdot \omega_k$ are removed.

[0049] Selecting the + sign (+1) in 316 and summing eqs. (4) and (5) yields the lower image LI at 330:

$$\cos(\omega_{LI} - \omega_k)t \dots (6)$$

[0050] If the minus sign (-1) is selected in 316, the upper image UI is obtained at 330:

$$\cos(\omega_{UI} - \omega_k)t \dots (7)$$

[0051] In a similar way it can be shown that at 340 obtained are signals that are in quadrature with those represented by eqs. (6) or (7): selecting the minus sign (-1) in 322 yields:

$$\cos[(\omega_{LI} - \omega_k)t - 90^\circ] \dots (8)$$

or, selecting the plus sign (+1) in 322 provides:

$$\cos[(\omega_{UI} - \omega_k)t - 90^\circ] \dots (9)$$

[0052] Eq. (6) and (8) represent the quadrature pair of the LI signal, and eq. (7) and (9) are the quadrature pair of the UI signal at zero IF frequency in the digital domain.

[0053] To simplify the further analysis, the above two equations pairs can be consolidated into one equation pair by substituting the difference frequencies $(\omega_{LI} - \omega_k)$ or $(\omega_{UI} - \omega_k)$ with $\Delta\omega_k$:

$$\cos(\Delta\omega_k t) \dots (10)$$

$$\cos(\Delta\omega_k t - 90^\circ) \dots (11)$$

$$\text{where } \Delta\omega_k = \omega_{LI} - \omega_k \text{ or } \Delta\omega_k = \omega_{UI} - \omega_k \dots (12)$$

and since $\omega_k \approx \omega_{LI} = \omega_{UI}$, the $\Delta\omega_k \approx 0$, i.e. the $\Delta\omega_k$ represents zero IF, with signal BW folded around DC.

[0054] Eqs. (10) and (11) represent either the LI or the UI quadrature pair at 330/340, depending upon which input image has been selected. This completes the first step of the present invention method - the channel extraction.

[0055] Next, the second step - the placement of these signals to the output frequency is performed. This is accomplished by upconverting the quadrature pair expressed with eq. (10) and (11) to the output frequency by multiplication with quadrature digital LO 335 (which is variable) at frequency f_{ok} of angular frequency ω_{ok} :

[0056] At the output of the upper mixer, at point 332 the signal is:

$$\cos(\omega_{ok} - \Delta\omega_k)t + \cos(\omega_{ok} + \Delta\omega_k)t \dots (13)$$

[0057] And at point 334:

$$\cos(\omega_{ok} - \Delta\omega_k)t - \cos(\omega_{ok} + \Delta\omega_k)t \dots (14)$$

[0058] Selecting the + sign (+1) in 336 and summing eqs. (13) and (14) yields at 338:

$$\cos(\omega_{ok} - \Delta\omega_k)t \dots (15)$$

[0059] If the minus sign (-1) is selected in 336, at 338 obtained is:

$$\cos(\omega_{ok} + \Delta\omega_k)t \dots (16)$$

[0060] Similarly, it can be shown that at 348 the following is obtained:

With 346 set to -1:

$$\cos[(\omega_{ok} - \Delta\omega_k)t + 90^\circ] \dots (17)$$

and with 346 set to +1:

$$\cos[(\omega_{ok} + \Delta\omega_k)t - 90^\circ] \dots (18)$$

[0061] Equations (15) and (17) represent the I_{kout} , Q_{kout} pair at 338/348 which, after passing through the combiners 156a/156b and DACs 160/170, will yield the LSB sideband at the final output after upconversion in the quadrature upconverter 180 of Fig. 1, and equations (16) and (18) represent the pair that will yield the USB sideband at the final output, as analyzed next.

[0062] Multiplying eq. (15) and (17) with corresponding quadrature components of the LO 181 in Fig. 1 at frequency f_o (angular frequency ω_o) and combining the products in the summing circuit 185 yields:

$$\begin{aligned} \cos(\omega_{ok} - \Delta\omega_k)t \cdot \cos(\omega_o t) - \cos[(\omega_{ok} - \Delta\omega_k)t + 90^\circ] \cdot \cos(\omega_o t - 90^\circ) \\ = \cos(\omega_o - \omega_{ok} + \Delta\omega_k)t \dots \end{aligned} \quad (19)$$

which represents the LSB sideband at the output frequency: $\omega_{out} = \omega_o - \omega_{ok}$.

[0063] Similarly, multiplying the pair of eqs. (16) and (18) with quadrature LO 181 and combining the terms:

$$\begin{aligned} \cos(\omega_{ok} + \Delta\omega_k)t \cdot \cos(\omega_o t) - \cos[(\omega_{ok} + \Delta\omega_k)t - 90^\circ] \cdot \cos(\omega_o t - 90^\circ) \\ = \cos(\omega_o + \omega_{ok} + \Delta\omega_k)t \dots \end{aligned} \quad (20)$$

which is the USB sideband at the output frequency: $\omega_{out} = \omega_o + \omega_{ok}$.

[0064] From eq. (19) or (20), it can be seen that the frequency f_{ok} of the digital oscillator 335 in Fig. 3a represents the distance of the desired output frequency from the LO frequency f_o , above or below the f_o .

[0065] Regarding the channel extractor/converter embodiment circuit of Fig. 3B, this embodiment shows the circuit configuration of the channel extractor/converter 350 when the RF LO falls in the middle of a channel, when the channel after downconversion is folded around DC at ZIF output. In this case the input frequency ω_{in} is equal to the RF LO 10 frequency, i.e. $\omega_{in} \approx \omega_{RF}$ or $(\omega_{in} - \omega_{RF}) \approx 0$. Designating $\omega_{in} - \omega_{RF} = \Delta\omega_o$, the in-phase downconverted, digitized and lowpass-filtered signal at 390 inside the channel extractor/converter 350 can be expressed with:

$$\cos(\Delta\omega_0 t) \dots (21)$$

[0066] Similarly, the quadrature signal at 380 is:

$$\cos(\Delta\omega_0 t - 90^\circ) \dots (22)$$

[0067] The cutoff frequency of the low pass filters (375) are set at about half the channel BW, so that the difference terms containing folded desired channel BW is passed, while all other channels are removed, resulting in only one term remaining in eq. (21) and (22), representing the desired channel.

[0068] Equation pair (21), (22) is identical to eq. pair (10), (11), meaning that the format of the signals at 390/360 in the channel extractor/converter 350 are identical to the signals 330/340 in the channel extractor/converter 300, which in turns means that the subsequent processing of these signals and therefore the circuitry in the channel extractor/converter 350 is identical to that of the channel extractor/converter 300.

[0069] As can be seen, no bandpass channel filters and no Hilbert Transformers are used. Also, separate I and Q summers (156a, 156b, respectively) are used. Because low pass filters are used instead of bandpass filters, filter and circuit complexity are relaxed. The absence of Hilbert transformers provides advantages in that circuit complexity and power consumption are reduced.

[0070] **Fig. 4** illustrates an exemplary upconverter circuit 180 shown in the channel stacking system of Fig. 1. The upconverter 180 includes a frequency source 181 (which may be fixed or variable frequency) operable to provide a reference frequency 182 to a 90-degree phase shifter 183, the phase shifter 183 providing substantially quadrature phase versions of the reference signal to mixers 184a and 184b. The mixers 184a and 184b also receive respective analog quadrature phase composite signals 168 and 178 (after anti-aliasing filtering) to produce upconverted signals that are summed by means of

a signal combiner 185 to produce an upconverted composite signal 188. The upconverted composite signal 188 may be supplied to a receiver, such as a set top box, or another channel stacking system, whereby additional channels are added to those within the composite signal 188. This latter embodiment of the invention is further described below and illustrated in Figs. 6 and 7.

[0071] **Fig. 5** illustrates a second exemplary embodiment of a channel stacking system 500 in accordance with the present invention, with previously-identified features retaining their reference indicia. The system 500 builds upon that of system 100, and further includes a pre-downconversion switch matrix 510, and a frequency translation module 520. The switch matrix 510 includes a plurality of inputs 511_1 - 511_N coupled to receive each of the first and second input signals 102, 104, 106 and a plurality of outputs 512_1 - 512_M . The switch matrix 510 is operable to couple any of the signals received at any switch matrix input to any one or more of the switch matrix outputs, thereby adding increased flexibility of distributing channels and creating diverse composite signals 158, 168, 178 and 188.

[0072] The frequency translation module 520 is employed to frequency translate an externally-supplied signal 106 to the desired input frequency of the switch matrix 510. In a particular embodiment, the externally-supplied signal 106 is an L-band signal, in which the frequency translation module is used to upconvert signal 106 to a frequency in the range of signals 102 and 104, which exemplary operate in the X/Ku/Ka-band frequency ranges. Furthermore, frequency translation module 520 may be omitted if signal 106 is within the desired input frequency range of the switch matrix 510 and of the downconverters. In this embodiment, the Channel Extractor/Converter inside the DSP 150 module is configured per Fig. 3b, configuration 350.

[0073] **Fig. 6** illustrates a third exemplary embodiment of a channel stacking system 600 in accordance with the present invention, with previously-identified features retaining their reference indicia. The system 600 includes a plurality of channel stacking sections which are coupled together in parallel by means of a signal combiner 690.

[0074] A first channel stacking section 100_1 (system 100 in Fig. 1) or ODU_1 provides a first composite signal 188. An M^{th} channel stacking section 100_M or ODU_M provides an M^{th} composite signal 688. The M^{th} channel stacking section 100_M (ODU_M) includes a third downconverter 610 having an input 610a for receiving a third input signal 602 having a plurality of third channels 602a, 602b. The third downconverter 610 is operable to frequency downconvert the third input signal 602 to a third downconverted signal 618, signal 618 including the plurality of third channels 602a, 602b. Construction and operation of the third downconverter 610 is substantially similar to that of the first and second downconverters 110 and 120.

[0075] The M^{th} channel stacking section 100_M further includes a third analog-to-digital converter (ADC) 630 operable to convert the third downconverted signal 618 to a third digital downconverted signal 638. The third ADC 630 is substantially identical in construction and operation to the first ADC 130.

[0076] The M^{th} channel stacking section 100_M further includes a fourth downconverter 620 having an input for receiving a fourth input signal 604 including a plurality of fourth channels 604a, 604b, the fourth downconverter 620 operable to frequency downconvert the fourth input signal 604 to a fourth downconverted signal 628, signal 628 including the plurality of the fourth channels 604a, 604b. A fourth analog-to-digital converter (ADC) 640 is operable to convert the fourth downconverted signal 628 to a fourth digital downconverted signal 648. The fourth downconverter 620 and ADC 640 are substantially identical in construction and operation to the second downconverter 220 and ADC 240.

[0077] The M^{th} channel stacking section 100_M further includes a second (or M^{th}) digital signal processor 650 coupled to receive each of the third and fourth digital downconverted signals 638, 648. Processor 650 is operable to assemble at least one of the third channels 602a, 602b and at least one of the fourth channels 604a, 604b into a

second composite signal 658. Processor 650 is substantially identical in construction and operation to processor 150 of Fig. 1.

[0078] The M^{th} channel stacking section 100_M also includes digital-to-analog converters (DACs) 660, 670, and an upconverter 680, which are substantially identical in construction and operation to DACs 160 and 170 and upconverter 180 of Fig. 1. The M^{th} channel stacking section 100_M provides a second composite signal 688.

[0079] System 600 further includes a signal combiner 690 operable to combine the first and second composite signals 188 and 688 into a combined composite signal 698. In this manner any number of channel stacking sections may be implemented to provide different composite signals having a different mix of channels and/or channel sequences.

[0080] It is further noted that the post-DSP circuitry for each of the channel stacking sections 100_1 - 100_M is optional. In an alternative embodiment, DACs 160, 170, 660, 670, upconverters 180 and 680 are omitted, and signal combiner 690 operates in the digital domain to combine digital composite signals 158 and 658 to produce composite signal 698. DAC(s) and an upconverter circuit may be used to convert the resulting digital composite signal into the analog domain.

[0081] **Fig. 7** illustrates a fourth exemplary embodiment of a channel stacking system 700 in accordance with the present invention, with the previously identified features retaining their reference indicia. System 700 includes a plurality of channel stacking sections which are coupled serially.

[0082] A first channel stacking section 100_1 (system 100 in Fig. 1) or ODU_1 provides a first composite signal 188. A second channel stacking section 100_2 or ODU_2 adds one or more channels from a third signal 702 to the first composite signal 188 to produce a second composite signal 788. The second channel stacking section 100_2 (ODU_2) includes a third downconverter 710 having an input 710a for receiving a third input signal 702 having a plurality of third channels 702a, 702b. The third downconverter 710 is operable

to frequency downconvert the third input signal 702 to a third downconverted signal 718, signal 718 including the plurality of third channels 702a, 702b. Construction and operation of the third downconverter 710 is substantially similar to that of the first and second downconverters 110 and 120.

[0083] The second channel stacking section 100₂ further includes a third analog-to-digital converter (ADC) 730 operable to convert the third downconverted signal 718 to a third digital downconverted signal 738. The third ADC 730 is substantially identical in construction and operation to the first ADC 130. While the embodiment of Fig. 7 illustrates only one signal 702 received in addition to the first composite signal 188, it will be appreciated that additional signal sources (e.g., a source from Sat. 4) may be received as well, and in such an embodiment, the corresponding downconverting and ADC chains would be employed to capture channels included within these additional signals.

[0084] The second channel stacking section 100₂ further includes a second digital signal processor 750 coupled to receive third digital downconverted signal 738 and the first composite signal 188 (in digital form via downconverter and ADCs 720). The second digital signal processor 750 is operable to assemble at least one of the third channels 702a, 702b and at least one of the first or second channels 102a, 102b, 104a, 104b included within the first composite signal 188 into a second composite signal 758. In this manner any number of channel stacking sections may be serially coupled to provide different composite signals having a different mix of channels and/or channel sequences. Furthermore, the first composite signal 188, which provides relatively fewer channels, may be tapped and distributed to a first group of consumers to provide a basic service of channels, while the second composite signal 788, providing a larger number of channels may be distributed to a second group of consumers as a premium service.

[0085] As with the parallel channel stacking system 600 of Fig. 6, the post-DSP circuitry for one or both of the channel stacking sections 100₁ and 100₂ is optional. For example, the DACs 160, 170, and upconverter 180 of the first channel stacking section

100₁ may be omitted, and the downconverter and ADC circuits 720 of the second channel stacking section 100₂ may be omitted, thereby allowing the digital composite signal 158 to be supplied directly to the second DSP 750. The DACs 760 and 770 and upconverter circuit 780 may be used to convert the resulting second digital composite signal into the analog domain for distribution to an analog set top box or other receiver requiring an analog formatted signal. If a third channel stacking section 100₃ (not shown) is to be coupled to receive the second composite signal 788, the DACs 760 and 770 and upconverter 780 may be omitted or removed from the second channel stacking section 100₂ and the second digital composite signal 758 supplied directly to the third processor housed within the third channel stacking section. The sequential coupling of additional channel stacking sections can be continued for any number of channel stacking sections.

[0086] In another embodiment (for instance, as described with Fig. 8), the reference frequency signal is selected such that no image signals are generated within the modulation bandwidth of the input signal, and in such a case, only a single ADC 116 or 126 is required. As an example, first receiver block 110 is operable to receive Ku-band frequency signals operating over the frequency range of 12.2-12.7 GHz, and employs a reference generating a reference signal operating at either band end (i.e., 12.2 GHz or 12.7 GHz) to provide a zero-IF, 500 MHz wide IF signal 114. In this instance, ADC 116 is a single ADC operating at a clock frequency of 1.1 GHz to provide the digital IF signal 118. Signals operating in the Ka-band frequency range may be similarly processed within the first receiver block 110, in which the LO signal operates at bandends of either 17.3 GHz or 17.8 GHz. Furthermore, the second receiver block 120 may also be similarly configured as the first receiver block 110.

[0087] **Fig. 8** illustrates a fifth exemplary embodiment of a channel stacking system 800 in accordance with the present invention, with the previously identified features retaining their reference indicia. System 800 includes a plurality of downconverter stages, each of which may be constructed identically to downconverter stage 810. In particular, downconverter stage 810 operates as a low IF downconverter, whereby the frequency of the reference source within the downconverter circuit 813 is selected to provide a

downconverted signal within a low-IF frequency range. The low-IF frequency range may range from 0.1-500 MHz, and more particularly 5 -505 MHz, or for example 5 -1005 MHz, or 5 - 2055 MHz in the case of wider BW satellites. As the LO frequency is selected such that no image signals are generated within the modulation bandwidth of the downconverted signal 814, and accordingly a single version of the downconverted signal can be processed without the necessity of I and Q signal processing for subsequent image rejection. Construction and operation of the input RF amplifier 811, input RF filter 812, IF filter 815, and ADC 816 may be as described in the previous embodiments above. DSP 850 operates to extract and place channels within desired channel slots to assemble a desired sequence of channels in an output digital signal 859. For this function a digital quadrature downconverter to zero IF, downconverting a selected channel from ADC output 818 line into I, Q ZIF signals and connecting these I, Q signals into 370/360 inputs of the Channel Extractor/Converter 350 of Fig. 3b can be utilized. DAC 860 operates to convert the digital output signal 859 to an analog form, and the output signal 888 is supplied to an analog receiver, such as to a cable set top box (not shown). An optional filter 870 (exemplary, a lowpass filter) is employed to attenuate out-of-band interferers possibly produced by the DAC 860. As illustrated, the downconverter stage 810 operates as a single analog domain downconverter stage between the input RF signal and the output digital signal 859.

[0088] Fig. 9 illustrates portions of an exemplary downconverter stage 810 in accordance with one embodiment of the invention. The downconverter stage 810 includes a downconverter circuit 813, a filter 815 (exemplary, a bandpass filter), and an ADC 816. Optionally, an amplifier (exemplary, a variable gain amplifier) may be implemented prior to the ADC to control the input signal amplitude thereto.

[0089] Downconverter circuit 813 includes a reference 913a (exemplary, a PLL oscillator), a mixer 913b, an input amplifier 913c (exemplary, a variable gain amplifier) and an output amplifier 913d. In the described embodiments in which the input RF signal is a Ku or Ka-band of modulation width or approximately 500 MHz, filter 815 has approximately the same bandwidth, i.e., permits all channels to be passed therethrough.

ADC 816 is clocked at a sufficient rate to allow accurate sampling, consistent with Nyquist sampling criteria, e.g., 1.1 GHz for the 500 MHz modulation bandwidth. The digitized IF signal 818 is supplied to the DSP 859, which extracts selected channels and assembles them into the desired channel sequence as described above.

[0090] **Fig. 10** illustrates a further exemplary embodiment of a first downconverter stage 1010 in accordance with one embodiment of the invention. In a particular embodiment of the invention, the first downconverter stage 1010 is operable to process wideband X-band signals which range between 10.7-11.725 GHz (lower X-band) and 11.725-12.75 GHz (upper X-band), although the stage 1010 could be modified to operate over other frequency ranges as well. The first downconverter stage 1010 is similar in operation to the first downconverter stage 110 illustrated in Fig. 1, but utilizes two downconverter circuits 1013 and 1023 to downconvert both the upper and lower band portions of the wideband X-band input signal while employing relatively narrow band filtering and low sample rate ADCs.

[0091] As shown, the first downconverter stage 1030 includes filters (exemplary, bandpass filters) 1002 and 1004 for supplying low and high portions of the applied input signal. In an alternative embodiment, a diplexer may be used. The lower X-band signal is supplied to first downconverter circuit 1013. The lower L-band signal is amplified and split into two portions, each of which are downconverted by respective mixers, which receive quadrature-phase reference signals originating from a source operating at approximately mid-band of the lower X-band frequency range, or 11.2125 GHz. The downconverted, quadrature-phased lower X-band signals 1014 are supplied to filters 1015, each having a passband of approximately 512 MHz. ADC pair 1016 are used to digitize the quadrature IF signals 1014 at a sufficient Nyquist rate, e.g., 1.2 GHz. The digitized IF signals 1018 are supplied to a DSP (not shown) identical in construction to that shown in Figs. 3A (if the LO is between channels) or 3B (if the LO is mid-channel) for channel extraction and placement.

[0092] The upper X-band signal output from filter 1004 is supplied to a second downconverter circuit 1023. The second downconverter circuit 1023 is configured and operates similarly to the first downconverter circuit 1013, although the reference frequency is tuned to mid-band of the upper X-band, or 12.2375 GHz. The downconverted, quadrature-phased upper X-band signals 1024 are supplied to filters 1025, each having a passband of approximately 512 MHz. ADC pair 1026 is used to digitize the quadrature IF signals 1024 at a sufficient Nyquist rate, e.g. 1.2 GHz. The digitized IF signals 1028 are supplied to a DSP (not shown) identical in construction to that shown in Figs. 3A (if the LO is between channels) or 3B (if the LO is mid-channel) for channel extraction and placement. In this manner, a relatively wideband RF input signal can be processed in the present invention using relatively narrowband filtering and low sampling rate ADCs without signal degradation.

[0093] **Fig. 11** illustrates a further exemplary embodiment of a third downconverter stage 1130 in accordance with one embodiment of the invention. In a particular embodiment, the third downconverter stage 1130 is operable to process L-band signals, specifically, signals ranging from 950-1450 MHz (lower L-band) and 1650-2150 MHz (upper L-band), although the stage 1130 could be modified to operate over other frequency ranges as well. The third downconverter stage 1130 is similar in operation to the third downconverter stage 130 illustrated in Fig. 1, but utilizes two downconverter circuits 1113 and 1123 to downconvert both upper and lower L-band portions while employing relatively narrow band filtering and low sample rate ADCs.

[0094] As shown, the third downconverter stage includes filters 1102 and 1104 for supplying low and high portions of the applied input signal. In an alternative embodiment, a diplexer may be used. The lower L-band signal is supplied to first downconverter circuit 1113. The lower L-band signal is amplified and split into two portions, each of which are downconverted by respective mixers, which receive quadrature-phase reference signals originating from a source operating at approximately mid-band of the lower L-band frequency range, or 1.2 GHz. The downconverted, quadrature-phased lower L-band signals 1114 are supplied to filters 1115, each having a

passband of approximately 250 MHz. ADC pair 1116 is used to digitize the quadrature IF signals 1114 at a sufficient Nyquist rate, e.g., 600 MHz. The digitized IF signals 1118 are supplied to a DSP (not shown) identical in construction to that shown in Figs. 3A (if the LO is between channels) or 3B (if the LO is mid-channel) for channel extraction and placement.

[0095] The upper L-band signal output from filter 1104 is supplied to a second downconverter circuit 1123. The second downconverter circuit 1123 is configured and operates similarly to the first downconverter circuit 1113, although the reference frequency is tuned to mid-band of the upper L-band, or 1.9 GHz. The downconverted, quadrature-phased upper L-band signals 1124 are supplied to filters 1125, each having a passband of approximately 250 MHz. ADC pair 1126 is used to digitize the quadrature IF signals 1124 at a sufficient Nyquist rate, e.g. 600 MHz. The digitized IF signals 1128 are supplied to a DSP (not shown) identical in construction to that shown in Figs. 3A (if the LO is between channels) or 3B (if the LO is mid-channel) for channel extraction and placement. In this manner, a relatively wideband signal can be processed in the present invention using relatively narrowband filtering and low sampling rate ADCs without signal degradation.

[0096] **Fig. 12** illustrates an interference cancellation circuit 1200 in accordance with the present invention. The interference signals typically originate from the opposite polarization of the same satellite, (usually referred to as cross-polarization), and/or from other satellites, referred to as cross-satellite interference or leakage. Interference can come from other sources, for example from terrestrial sources, or from signals inside the receiving unit. The method described herein can be used to cancel the interference of any of these types. In a particular embodiment, the interference cancellation circuit 1200 is implemented within the DSP 150 using digital processing techniques prior to the I and Q matrix switches 302 and 304, or alternatively after these switches, inside the processors 350. If the cancellation is performed before the matrix switches 302/304, the interference is cancelled or reduced in all transponders within a satellite simultaneously, while if the

cancellation is performed after the matrix switches 302/304, it is then done on a per transponder (channel) basis.

[0097] Adjustable phase shifting 1208 and adjustable gain 1206 are applied to signal A (e.g., first digital IF signal 118 or alternatively at points 330/340 or 338/348) and the resulting signal A'' is fed into the B path (e.g., signal path receiving second digital IF signal 128 or alternatively 330/340 or 338/348 in the corresponding processor 300). Likewise, phase shifting and gain are applied to signal B and the resulting signal B'' is fed into the A path. When used as a cancellation circuit, the phase and gain are set to cancel the cross polarization signal present in the received signal by setting the gain to match the amplitude and setting the phase to 180 degrees from the contaminating signal. When used in the measuring mode, the phase and gain are set to test the level of contamination. In one embodiment of the invention, a backend receiver (e.g., a set top box) estimates the C/N ratio and sends this value for processing by the interference cancellation circuitry 1200. Communication between the STB and the circuit 1200 can use well-known techniques for communicating; including FSK control or more advanced and commonly used Digital Satellite Equipment Control (DiSEqC).

[0098] Cancellation circuitry 1204 shows an optional time delay (τ) adjustment 1210. The use of the time delay adjustment depends on system requirements including the required bandwidth of the input signal. The phase shift, the gain and the time delay parameters are adjustable and the cancellation circuit may be implemented such that the parameters are programmable or changed by well known digital circuits.

[0099] **Fig. 13** illustrates steps to measure the phase and amplitude level of cross polarization of the circuit 1200 in accordance with the invention. If cancellation method includes the adjustment of time delay in addition to amplitude and phase adjustment, the method shown in the figure and describe below can be expanded to include the third parameter of time.

[0100] A chosen power level is applied and the phase is stepped through a number of discrete phases. A second power level is applied and the phase is stepped through the range. An averaging loop (using M) is shown so that several measurements can be taken at each phase setting and power level. The order of stepping phase and power can be reversed, where the power is switched between the two levels at each phase setting. Averaging can be taken repeatedly at one setting or on subsequent cycles of the stepping process. The average can be obtained by summing new readings with the accumulated stored value.

[0101] The steps are as follows:

1. Feed signal B into signal A at approximately 10dB attenuation (power 1)
 - a. Measure C/N and record.
 - b. Rotate phase by 1 phase step.
 - c. Repeat steps 1a to 1b until all phase steps are exercised.
 - d. Increase attenuation by p_{diff} dB (resulting in power 2). P_{diff} is the predetermined power level step size.
 - e. Measure C/N and record
 - f. Rotate phase by 1 phase step
 - g. Repeat 1e to 1f until all phase steps are exercised.
2. Determine phase step where the maximum difference of C/N occurred between power 1 and power 2 and record the values of step number, $p1_{max}$ and $p2_{max}$ for that phase step.

[0102] The value of $p1_{max}$ is the power in dBc at the first power level when the phase is adjusted to achieve the maximum constructive interference; $p2_{max}$ is the power in dBc at the second power level.

3. Find phase step where the minimum difference of C/N occurred between power 1 and power 2 and record the values of step number, $p1_{min}$, and $p2_{min}$ for that phase step.

[0103] The value p_{1min} is the power in dBc at the first power level when the phase is adjusted to achieve the maximum destructive interference; the value p_{2min} is the power in dBc at the second power level.

[0104] Inherently in the system, there will be gain/attenuation differences between the different phase steps. This difference will need to be calculated from the p_{1max} , p_{1min} , p_{2max} and p_{2min} values. The resulting error will be called $perrmax$. The value $perrmax$ is defined as the power difference in the phase shifter due to the manufacturability of the phase shifter. In broadband phase shifters, the amplitude is not constant across phases; in this invention, this inaccuracy is compensated by the value $perrmax$ (in dB).

4. Determine the value of $perrmax$.
5. Calculate power of signal B in signal A using the p_{test} function shown in Equation 1.

[0105] Since the relative power of signal B in signal A is not precisely known, it will need to be calculated using β , p_{1max} , p_{1min} , p_{2max} and p_{2min} . The value β is defined as the square root of linear equivalent value of $perrmax$ ($perrmax_{Lin}$). The result of the calculation will be the power of the undesired signal (signal B) relative to desired signal (signal A); this will be called p_{test} . Equation 1 shows the formula to calculate p_{test} (the linear equivalent value of p_{test} is denoted as $p_{testLin}$).

$$\text{Equation 1: } p_{testLin} = -((\beta \cdot \alpha)(A - B) - \alpha^2(C - A) - \alpha(B - A) + D + B) / E$$

Where

β = square root of $perrmax_{Lin}$;

α = the inverse of the square root of the linear equivalent of p_{diff} .

$A = p_{1minLin}$ where $p_{1minLin}$ is the linear equivalent of p_{1min} .

$B = p_{2minLin}$ where $p_{2minLin}$ is the linear equivalent of p_{2min} .

$C = p1_{\max Lin}$ where $p1_{\max Lin}$ is the linear equivalent of $p1_{\max Lin}$.

$D = p2_{\max Lin}$ where $p2_{\max Lin}$ is the linear equivalent of $p2_{\max Lin}$.

$$E = \alpha \cdot (-\beta + (\beta \cdot \alpha^2) + \alpha^2 - 1)$$

[0106] Next, we can calculate the power of the original signal B into signal A (or cross polarization or xpole). Using β , p_{test} , $p1_{\max}$, $p1_{\min}$, $p2_{\max}$, $p2_{\min}$, as well as $pdiff$ numbers from above, the crosspole power can be calculated.

6. Calculate the power of the crosspole power of signal B in signal A using the crosspole function shown in Equation 2:

$$\text{Equation 2: } [(B - D - \alpha^2 \cdot (1 - \beta^2) \cdot p_{testLin}) / (-2 \cdot (\beta + 1) \cdot \alpha)]^2 / p_{testLin}$$

[0107] Finally, if needed, we can estimate the power of the noise of the system under test, using β , p_{test} , p_{xpole} , $p1_{\max}$, $p1_{\min}$, $p2_{\max}$, $p2_{\min}$, as well as $pdiff$.

[0108] This process is repeated for the other signal, where signal A is fed into B and measurements are taken. The phase and gain are calculated to cancel the cross polarization of both signals. Cancellation of the cross polarization signal is needed for both signals because one or more set top boxes may be receiving and processing both polarizations simultaneously.

[0109] In an alternate embodiment, the C/N does not need to be measured at all possible phases. For example, after an initial optimum phase for correction is determined, a narrower range of phase steps centered on the initial optimum phase value can be used to track changes in the optimum phase value. A new search over a suitable range can be initiated after installation, or channel change, or periodically, or at a scheduled time when the system is not being used.

[0110] Previous correction values and ranges of values can be stored to set upper and lower bounds for the range of phases needing to be searched for optimum correction.

Additionally, the sequence for cross pole cancellation can be triggered when a degradation of a predetermined or adaptive amount is detected.

[0111] The cancellation sequence can degrade the live signal. Performing the cancellation procedure during channel changes would minimize the appearance of the cancellation procedure.

[0112] During a maintenance period of the cross pole cancellation, measuring the optimum phase and amplitude is done after the cross pole power is high enough to be detected and measurable as a change in C/N. Upon having this measurement available, the previous canceling cross pole signal can now be used to determine the exact amplitude and phase of the present cross pole degradation. This may be achieved by rotating the phase and monitoring constructive and destructive interference, then changing the power by some known amount and measuring again at the constructive and destructive phases and re-performing the math associated with the determination of the new cross pole phase and relative magnitude. The key here is not to degrade the C/N by any more than is needed while the system is operating. From these measurements, the correct phase can be calculated and applied, then the signal level can be increased while measuring for maximum cancellation of the cross pole signal.

[0113] An approach to determining the correct phase and gain for canceling the interfering signal is to directly measure the C/N for each interferer phase setting, then set the phase to the optimum value and measure the C/N for various interferer gain setting to set the optimum gain. Preferably, the phase is set with a power level from the unwanted interfering path set below the wanted signal level, for example at -10dBc relative to the wanted signal. The phase is swept across all potential phase setting to determine the phase that causes maximum cancellation, for example as measured by C/N in the set-top box. The phase is then fixed at that level and the gain is adjusted up and down to the level that causes maximum cancellation. This direct measurement approach avoids complex calculations to derive phase and gain values.

[0114] This method can be extended for cancellation of multiple interfering signals, for example if several satellites are causing simultaneously interference into a satellite signal path. In this case the method is applied to one interfering signal at a time, treating each interference independently of others.

[0115] As readily appreciated by those skilled in the art, the described processes may be implemented in hardware, software, firmware or a combination of these implementations as appropriate. In addition, some or all of the described processes may be implemented as computer readable instruction code resident on a computer readable medium, the instruction code operable to program a computer or other such programmable device to carry out the intended functions. The computer readable medium on which the instruction code resides may take various forms, for example, a removable disk, volatile or non-volatile memory, etc., or a carrier signal which has been impressed with a modulating signal, the modulating signal corresponding to instructions for carrying out the described operations.

[0116] The terms “a” or “an” are used to refer to one, or more than one feature described thereby. Furthermore, the term “coupled” or “connected” refers to features which are in communication with each other (electrically, mechanically, thermally, as the case may be), either directly, or via one or more intervening structures or substances. The sequence of operations and actions referred to in method flowcharts are exemplary, and the operations and actions may be conducted in a different sequence, as well as two or more of the operations and actions conducted concurrently. Reference indicia (if any) included in the claims serve to refer to one exemplary embodiment of a claimed feature, and the claimed feature is not limited to the particular embodiment referred to by the reference indicia. The scope of the claimed feature shall be that defined by the claim wording as if the reference indicia were absent therefrom. All publications, patents, and other documents referred to herein are incorporated by reference in their entirety. To the extent of any inconsistent usage between any such incorporated document and this document, usage in this document shall control.

[0117] The foregoing exemplary embodiments of the invention have been described in sufficient detail to enable one skilled in the art to practice the invention, and it is to be understood that the embodiments may be combined. The described embodiments were chosen in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined solely by the claims appended hereto.

CLAIMS

What is Claimed is:

1. A channel stacking system, comprising:
 - a first downconverting stage, comprising:
 - a first downconverter circuit having an input for receiving a first RF input signal comprising a plurality of first channels, the first downconverter operable to frequency downconvert the first RF input signal to a first IF signal comprising said plurality of first channels; and
 - a first analog-to-digital converter operable to convert the first IF signal to a first digital IF signal;
 - a second downconverting stage, comprising:
 - a second downconverter circuit having an input for receiving a second RF input signal comprising a plurality of second channels, the second downconverter circuit operable to frequency downconvert the second RF input signal to a second IF signal comprising said plurality of second channels; and
 - a second analog-to-digital converter operable to convert the second IF signal to a second digital IF signal; and
 - a digital signal processor coupled to receive each of the first and second digital IF signals, the digital signal processor operable to assemble at least one of the first channels and at least one of the second channels into a digital composite signal.
2. The channel stacking system of claim 1, wherein the channel system comprises a single downconversion stage comprising said first and second downconverter stages.
3. The channel stacking system of claim 1 or 2, further comprising a third downconverting stage, comprising:
 - a third downconverter circuit having an input for receiving an IF input signal comprising a plurality of third channels, the third downconverter circuit operable to frequency downconvert the IF input signal to a third IF signal comprising said plurality of third channels; and

a third analog-to-digital converter operable to convert the third IF signal to a third digital IF signal.

4. The channel stacking system of one of claims 1-3, wherein the first, second, and third downconverter circuits are zero-IF downconverter circuits, and wherein the first, second and third IF signals comprise a baseband signal substantially centered around 0 Hz.

5. The channel stacking system of one of claims 1-4, further comprising respective first and second reference frequency sources for providing respective first and second reference signals to the respective first and second downconverter stages.

6. The channel stacking system of claim 5, wherein the first and second reference frequency sources are fixed frequency sources or variable frequency sources.

7. The channel stacking system of one of claims 1-6, wherein the first downconverted signal comprises a pair of quadrature phase signals, and wherein the second downconverted signal comprises a pair of quadrature phase signals.

8. The channel stacking system of one of claims 1-6, wherein the composite signal comprises a pair of digital quadrature phase signals output from the digital signal processor.

9. The channel stacking system of claim 8, further comprising:
first and second digital-to-analog converters operable to receive a respective one of the digital quadrature phase signals and to produce a respective one of two quadrature phase analog composite signals; and
an upconverter coupled to received each of the analog quadrature phase composite signals, and operable to produce an upconverted composite signal.

10. The channel stacking system of any one of claims 1-9, wherein each of the first and second input signals comprises signals received in the X-band, Ku-band, or Ka-band frequency range.
11. The channel stacking system of any one of claims 1-9, wherein the first input signal comprises a signal received in the X-band, Ku-band, or Ka-band frequency range, and the second input signal comprises a signal received in the L-band frequency range.
12. The channel stacking system of any one of claims 1-11, further comprising a switch matrix having a plurality of inputs coupled to receive each of the first and second input signals and a plurality of outputs, the switch matrix operable to couple any of the signals received at any switch matrix input to any one or more of the switch matrix outputs.
13. The channel stacking system of any one of claims 1-12, wherein the composite signal comprises a first composite signal, the channel stacking system further comprising:
 - a third downconverter having an input for receiving a third input signal comprising a plurality of third channels, the third downconverter operable to frequency downconvert the third input signal to a third downconverted signal comprising said plurality of third channels;
 - a third analog-to-digital converter operable to convert the third downconverted signal to a third digital downconverted signal;
 - a fourth downconverter having an input for receiving a fourth input signal comprising a plurality of fourth channels, the fourth downconverter operable to frequency downconvert the fourth input signal to a fourth downconverted signal comprising said plurality of fourth channels;
 - a fourth analog-to-digital converter operable to convert the fourth downconverted signal to a fourth digital downconverted signal; and
 - a second digital signal processor coupled to receive each of the third and fourth digital downconverted signals, the second digital signal processor operable to assemble at

least one of the third channels and at least one of the fourth channels into a second composite signal; and

a signal combiner operable to combine the first and second composite signals into a combined composite signal.

14. The channel stacking system of any one of claims 1-12, wherein the composite signal comprises a first composite signal, the channel stacking system further comprising:

a third downconverter having an input for receiving a third input signal comprising a plurality of third channels, the third downconverter operable to frequency downconvert the third input signal to a third downconverted signal comprising said plurality of third channels;

a third analog-to-digital converter operable to convert the third downconverted signal to a third digital downconverted signal; and

a second digital signal processor coupled to receive the third digital downconverted signal and the first composite signal, the second digital signal processor operable to assemble at least one of the third channels and at least one of the first or second channels into a second composite signal.

15. The channel stacking system of claim 14, wherein the first composite signal comprises a digital signal, the channel stacking system further comprising:

digital-to-analog circuitry coupled to receive the first digital composite signal, and to convert the first digital composite signal into a first analog composite signal; and

an analog-to-digital converter operable to convert the first analog signal to a digital signal which is input into the second digital signal processor.

16. A method for assembling channels in a composite signal, the method comprising:

downconverting a first input signal comprising a first plurality of channels to a first IF signal comprising said plurality of first channels;

converting the first IF signal into a first digital IF signal;

downconverting a second input signal comprising a plurality of second channels to a second IF signal comprising said plurality of second channels;

converting the second IF signal into a second digital IF signal; and
assembling, in the digital domain, at least one of the first channels and at least one of the second channels into a digital composite signal.

Channel Stacking System and Method of Operation

Abstract of the Disclosure

A channel stacking system includes first and second downconverting stages, first and second analog to digital converters, and a signal processor. The first downconverting stage includes a first downconverter circuit having an input for receiving a first RF input signal which includes a multitude of first channels. The first downconverter circuit is operable to frequency downconvert the first RF input signal to a first IF signal which includes the multitude of first channels. The first analog-to-digital converter is operable to convert the first IF signal to a first digital IF signal. The second downconverter stage includes a second downconverter circuit having an input for receiving a second RF input signal which includes a multitude of second channels. The second downconverter circuit is operable to frequency downconvert the second RF input signal to a second IF signal including said multitude of second channels. The second analog-to-digital converter is operable to convert the second IF signal to a second digital IF signal. The signal processor is coupled to receive each of the first and second digital IF signals, and is operable to assemble at least one of the first channels and at least one of the second channels into a digital composite signal.

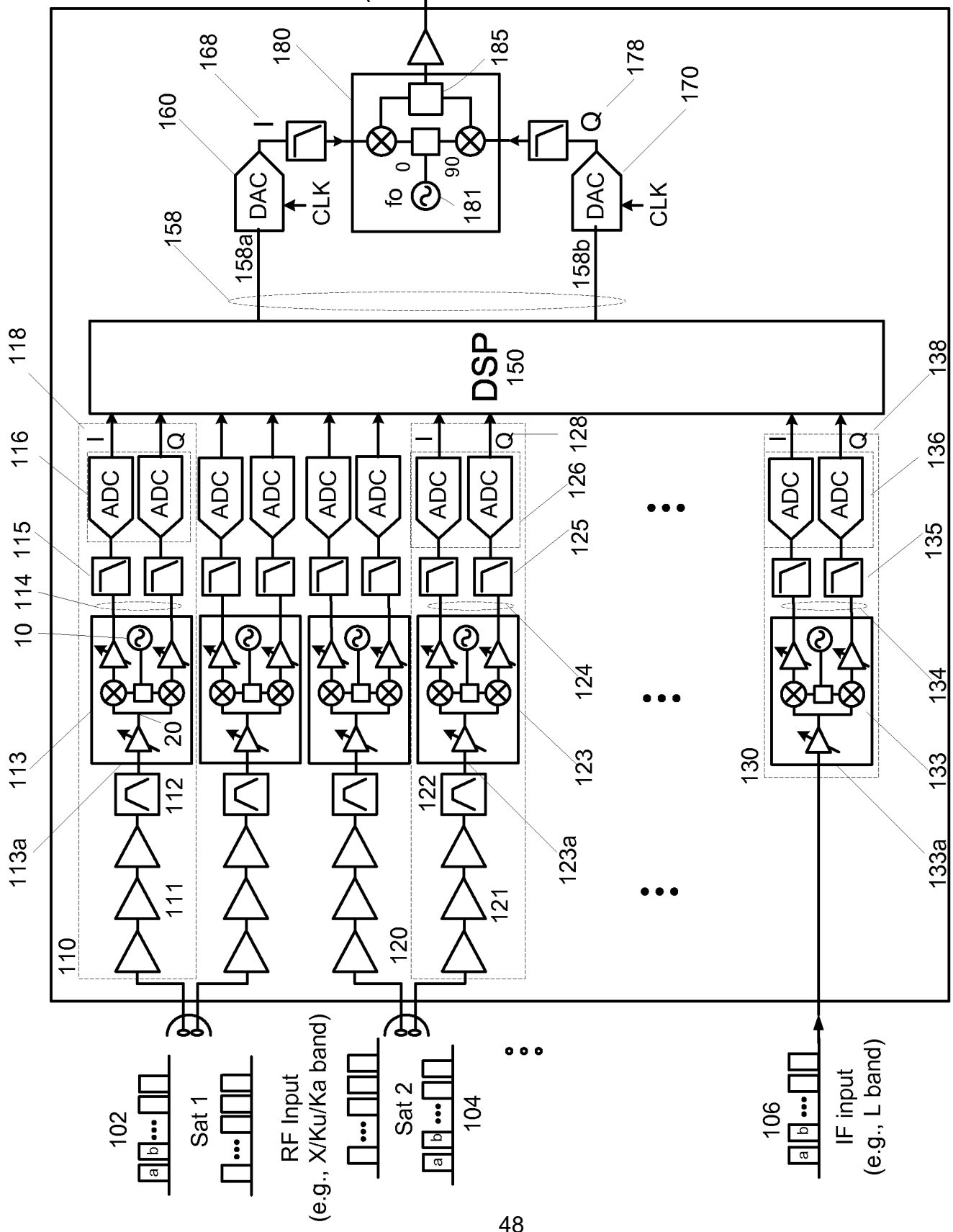


Fig. 1

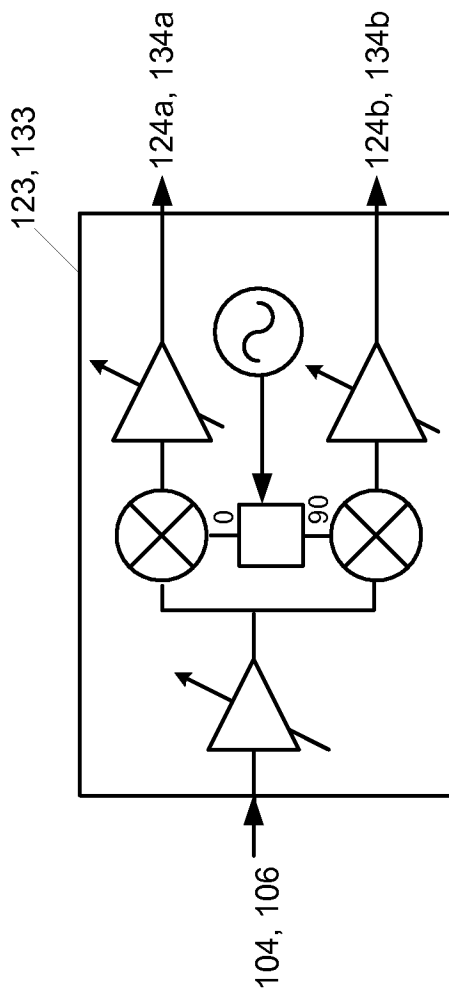
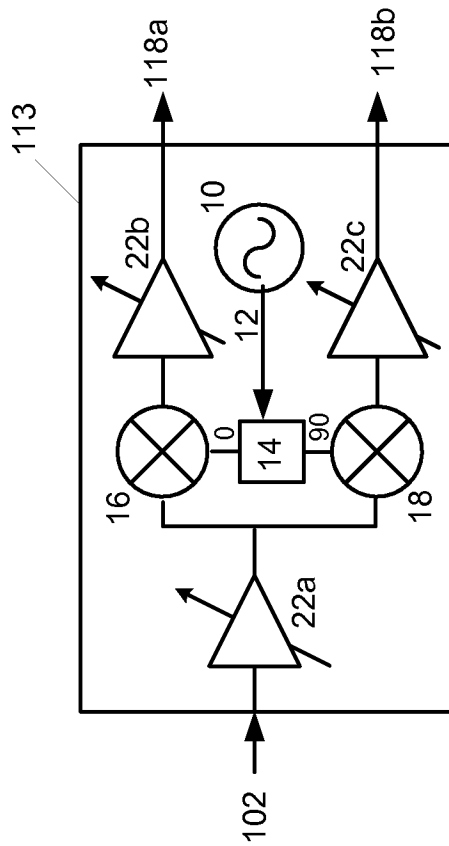


Fig. 2

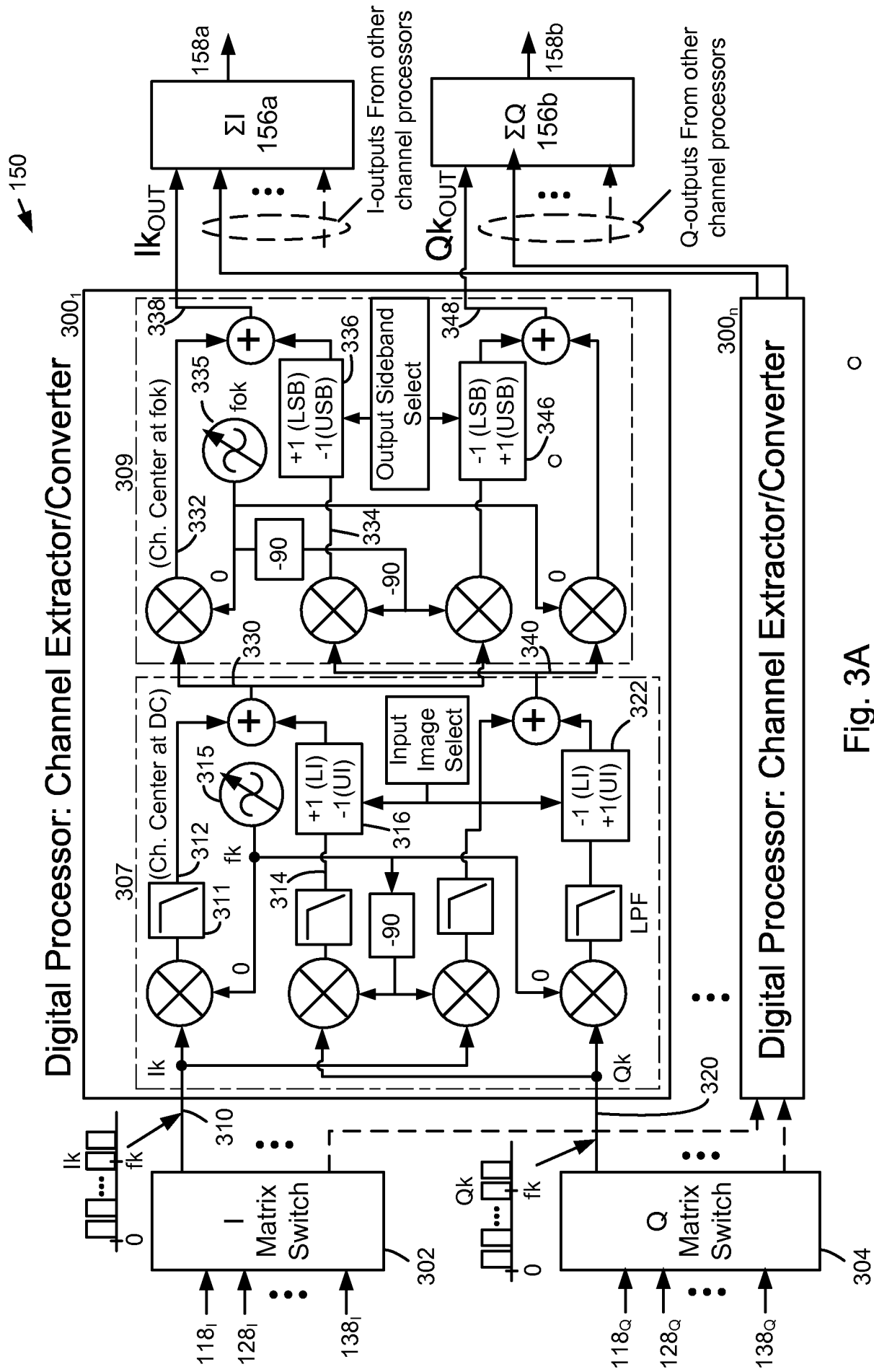


Fig. 3A

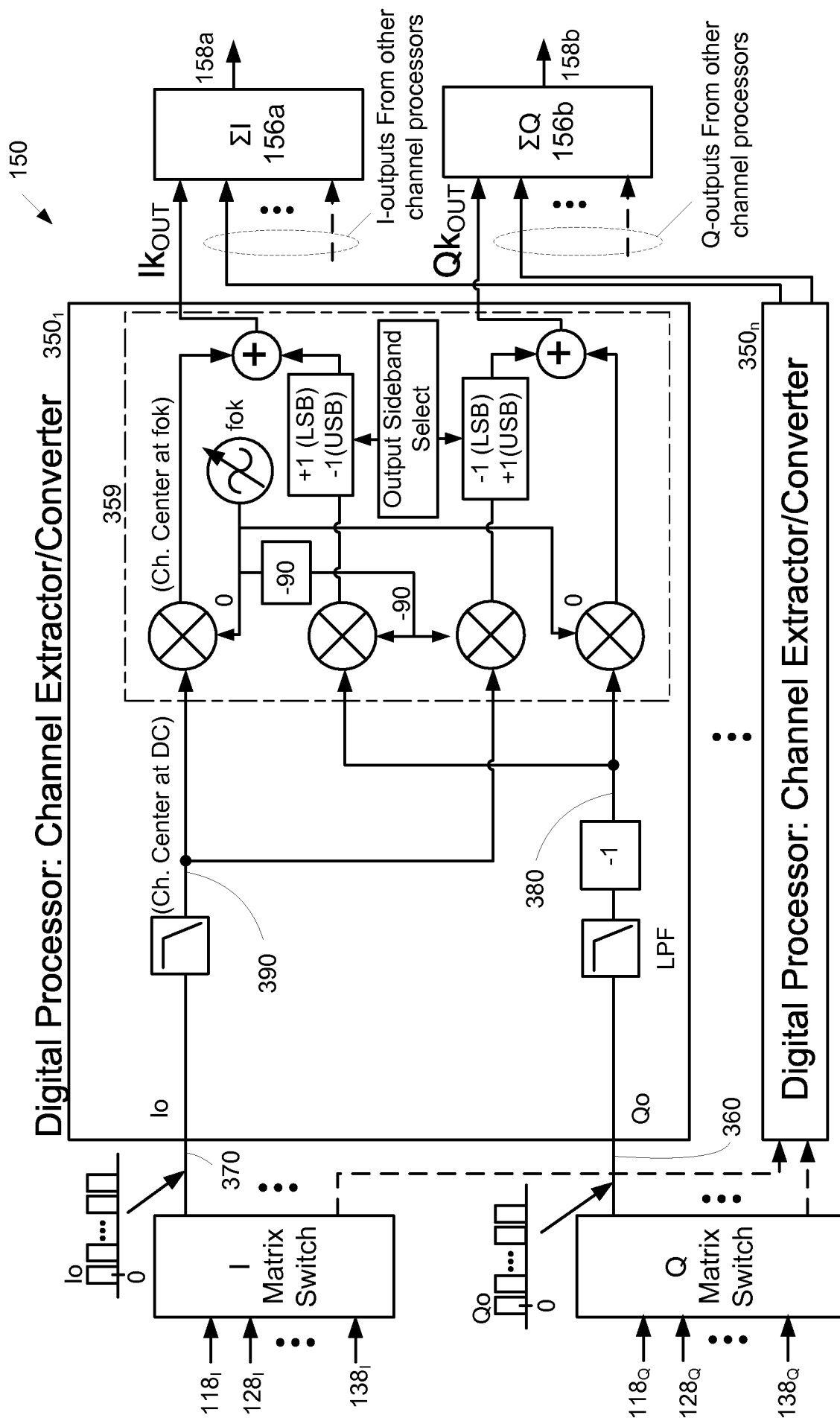


Fig. 3B

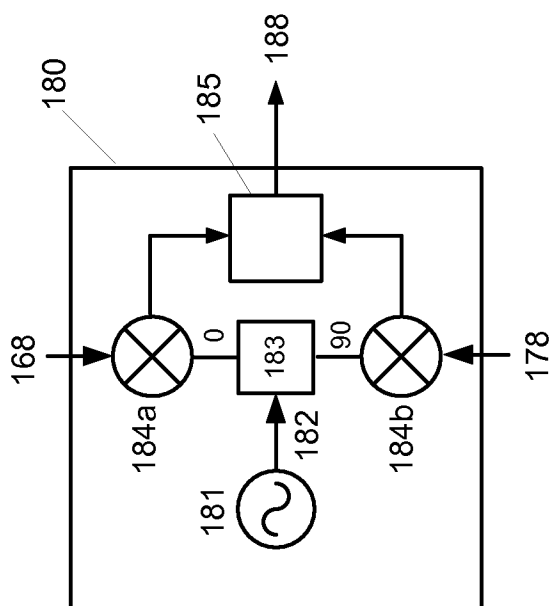


Fig. 4

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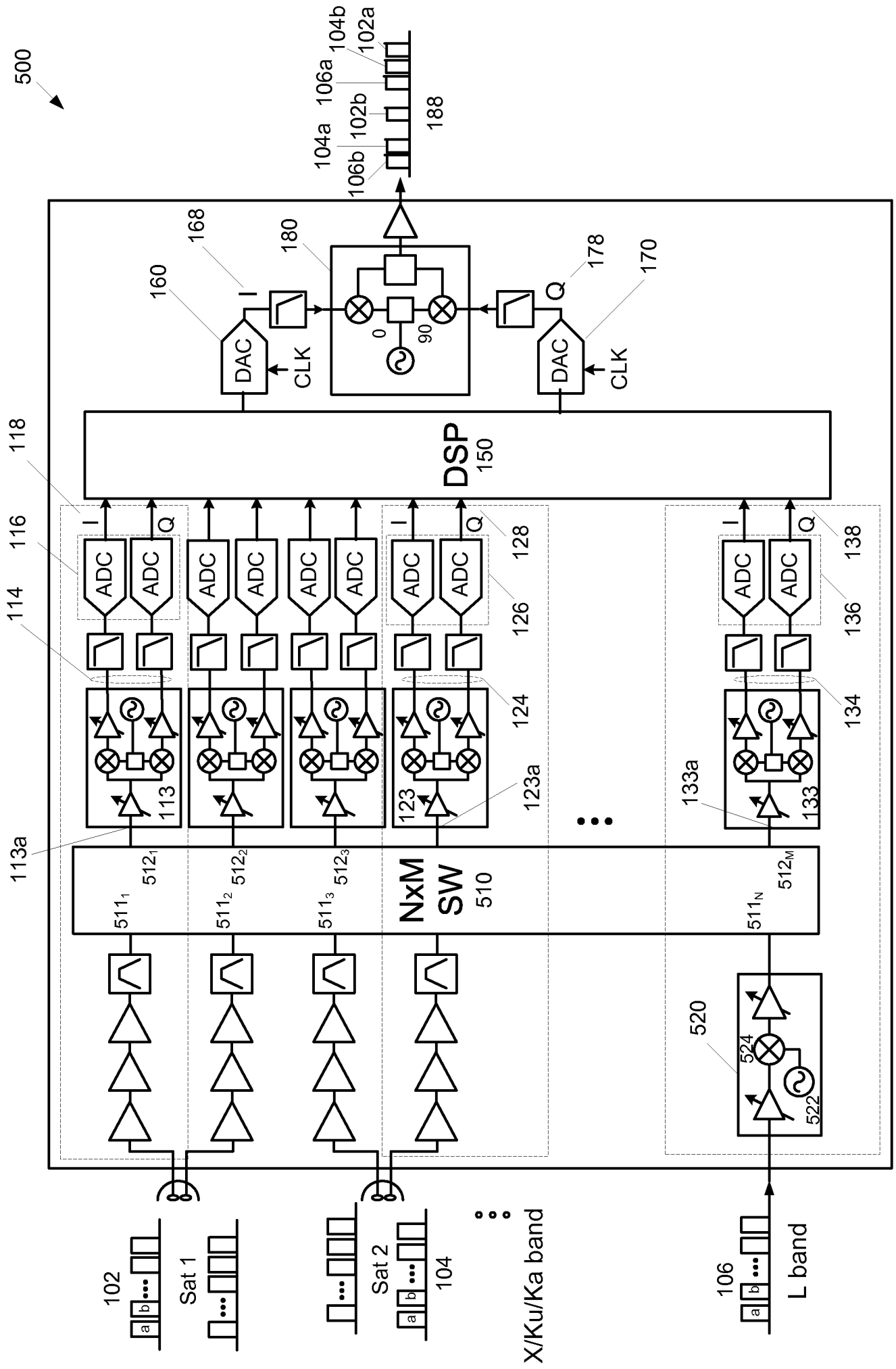
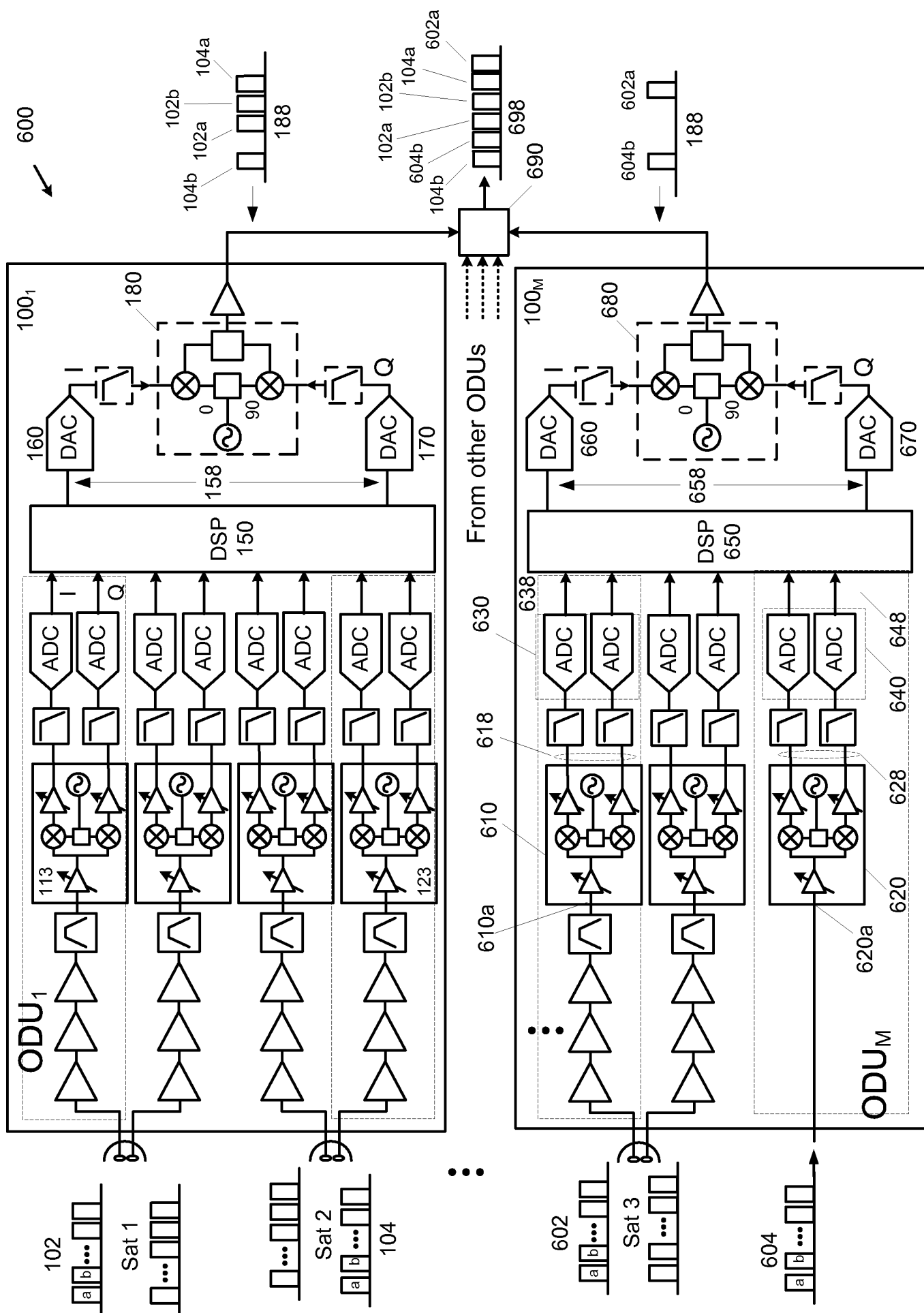
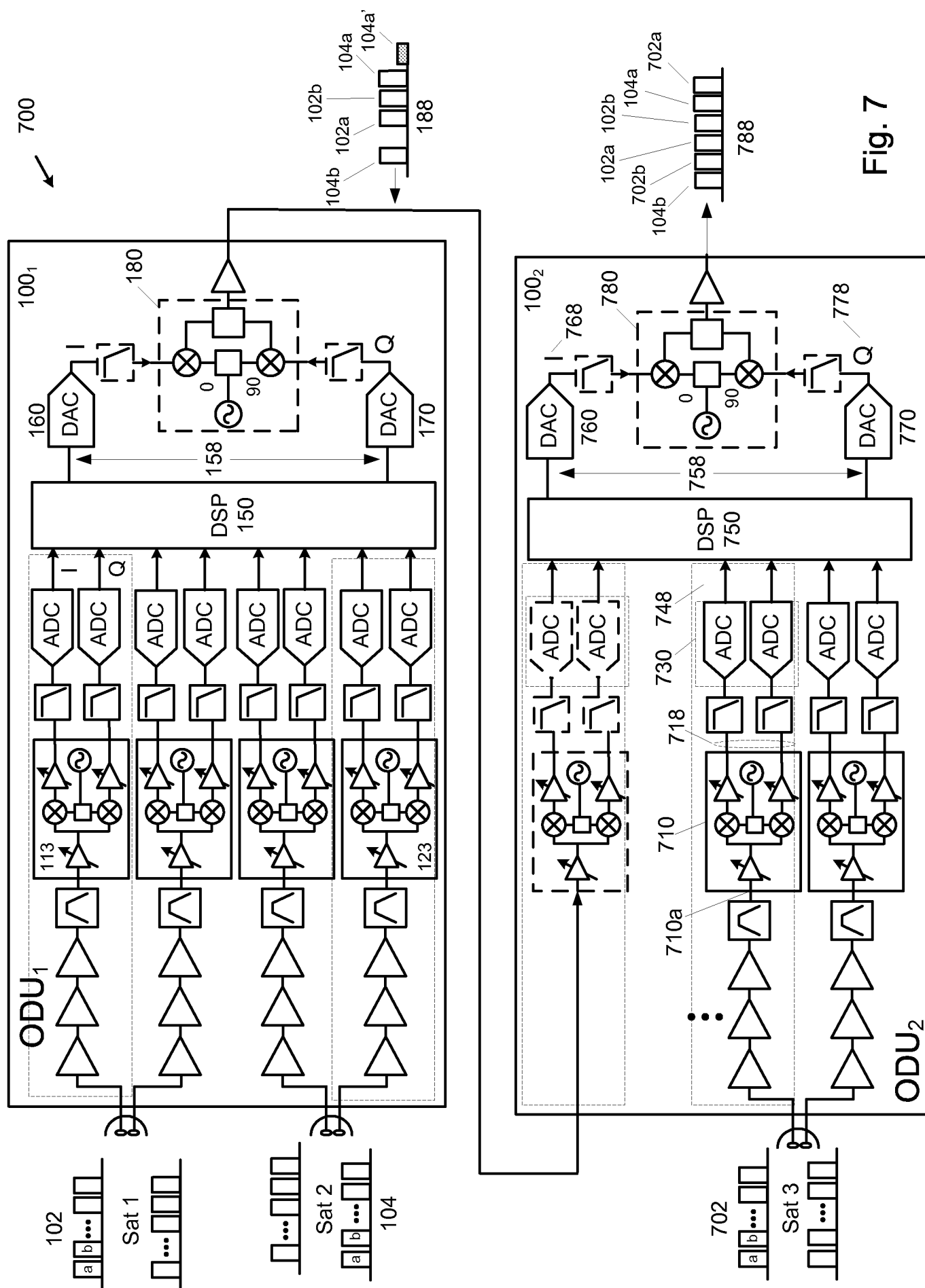


Fig. 5





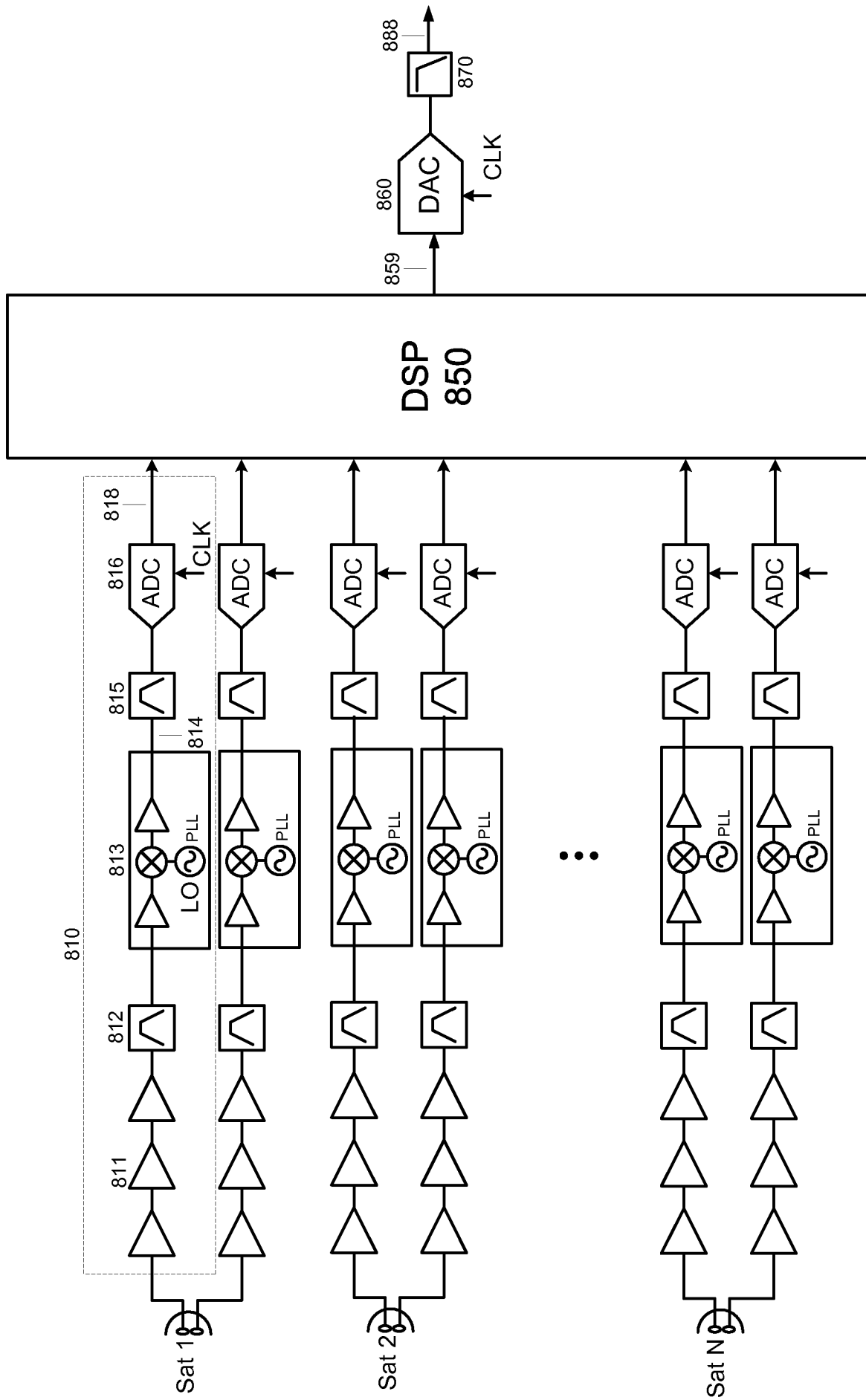


Fig. 8

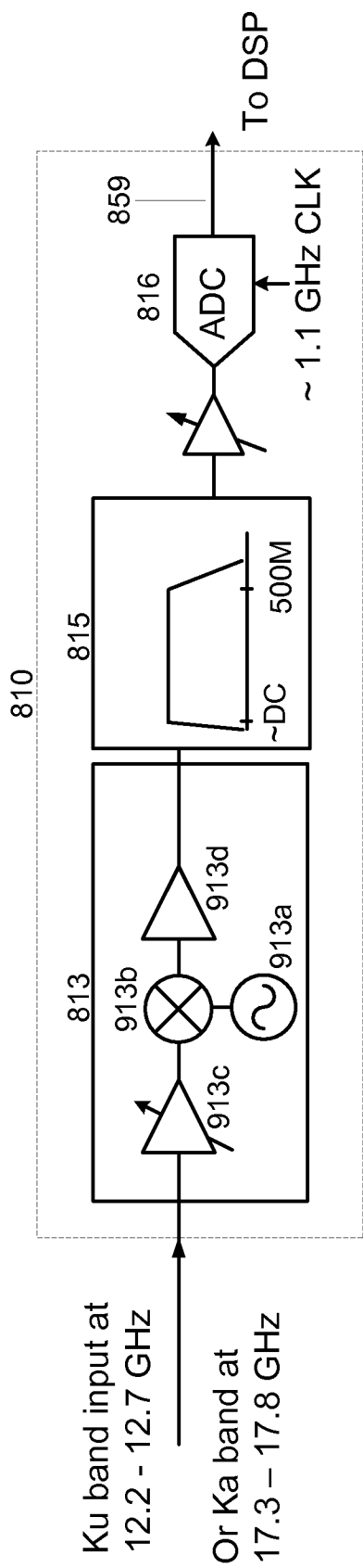


Fig. 9

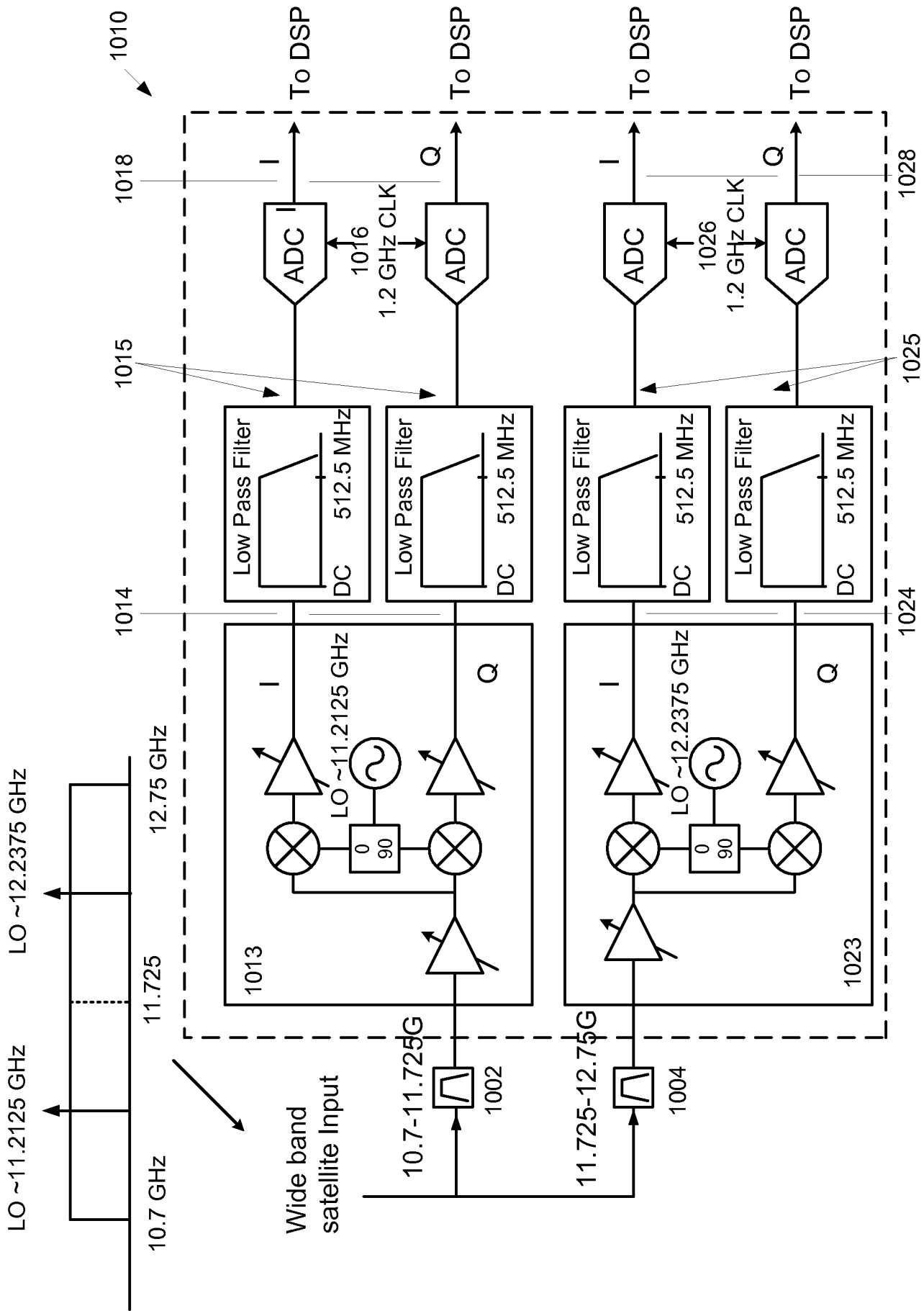


Fig. 10

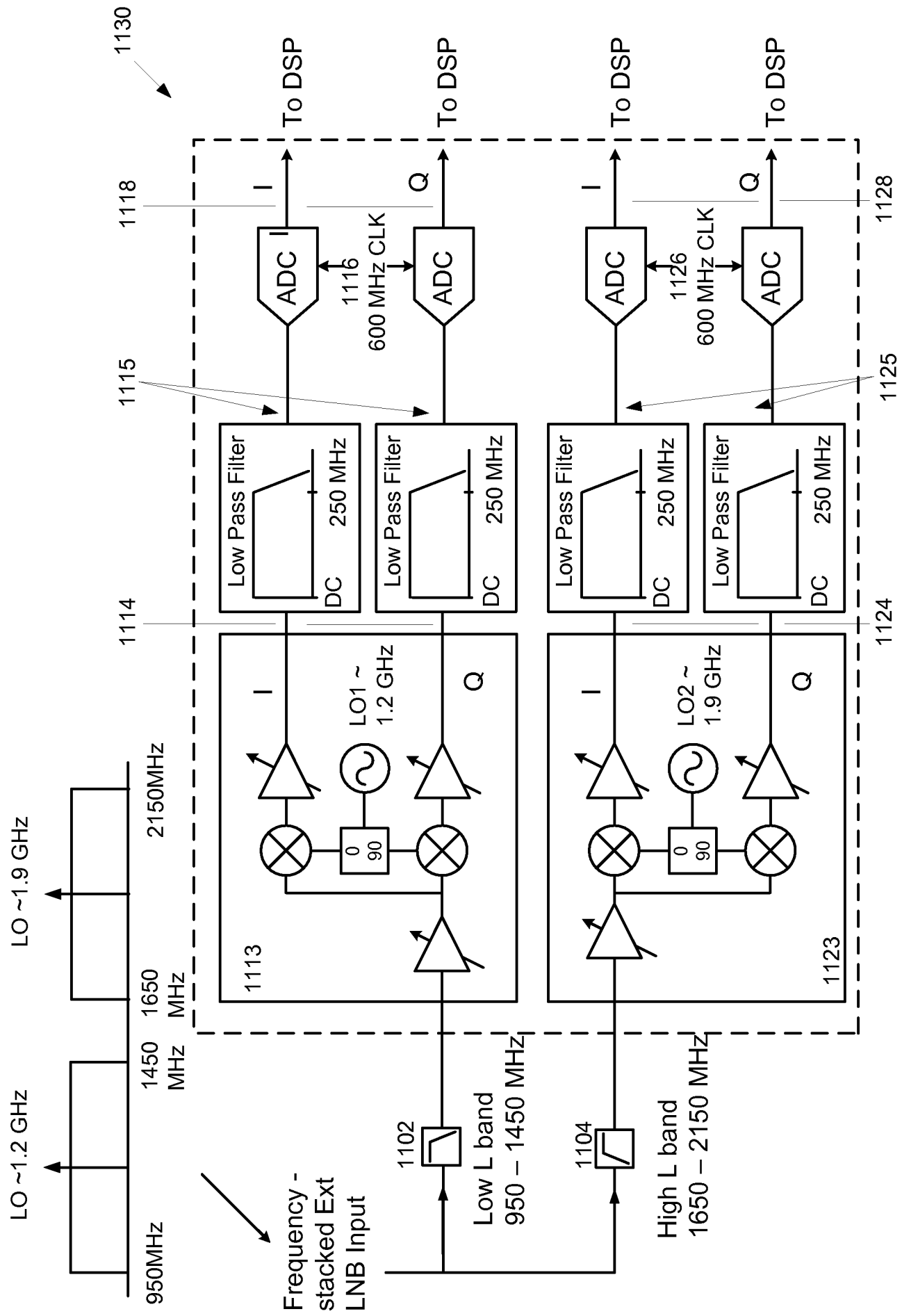


Fig. 11

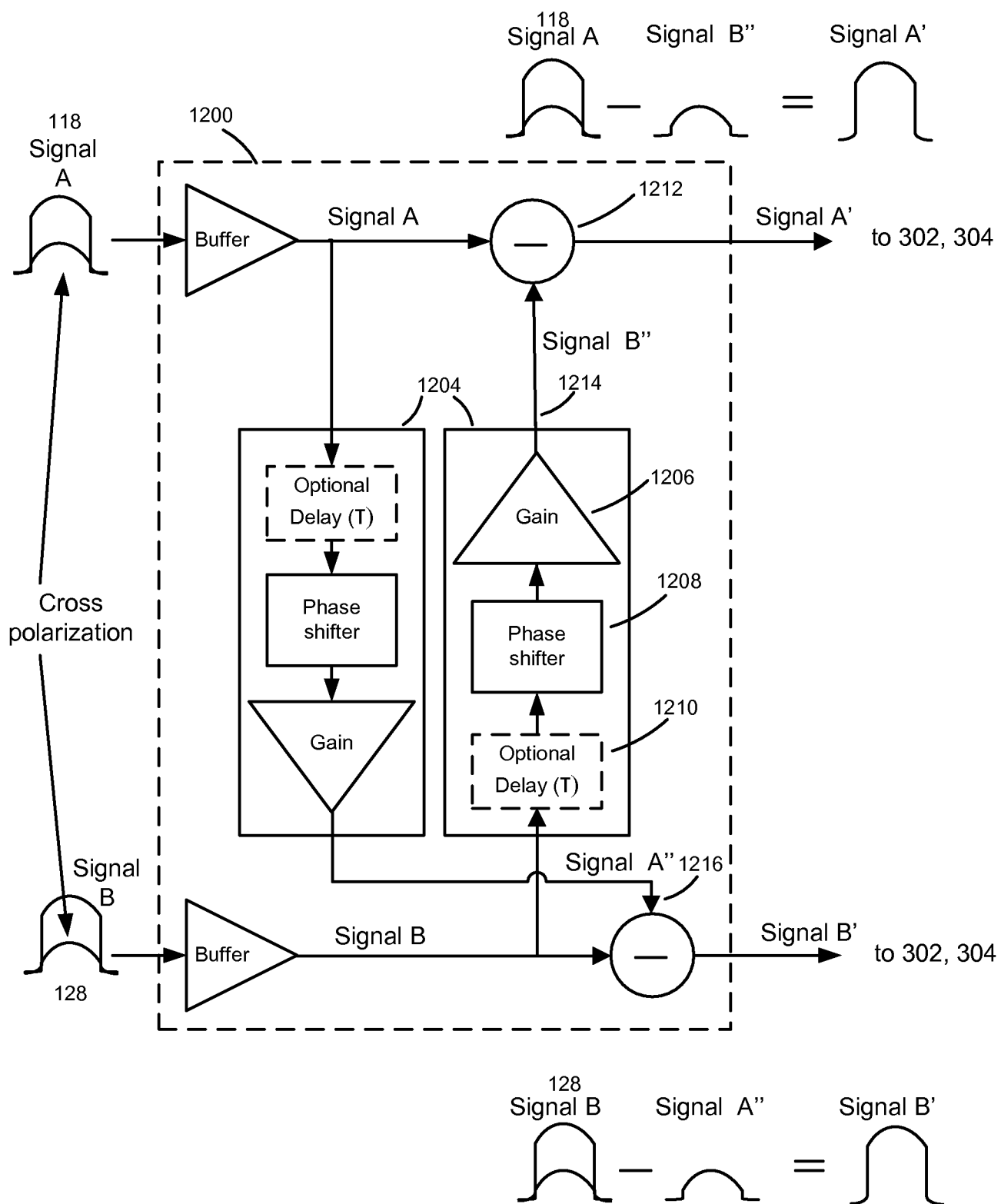


FIG. 12

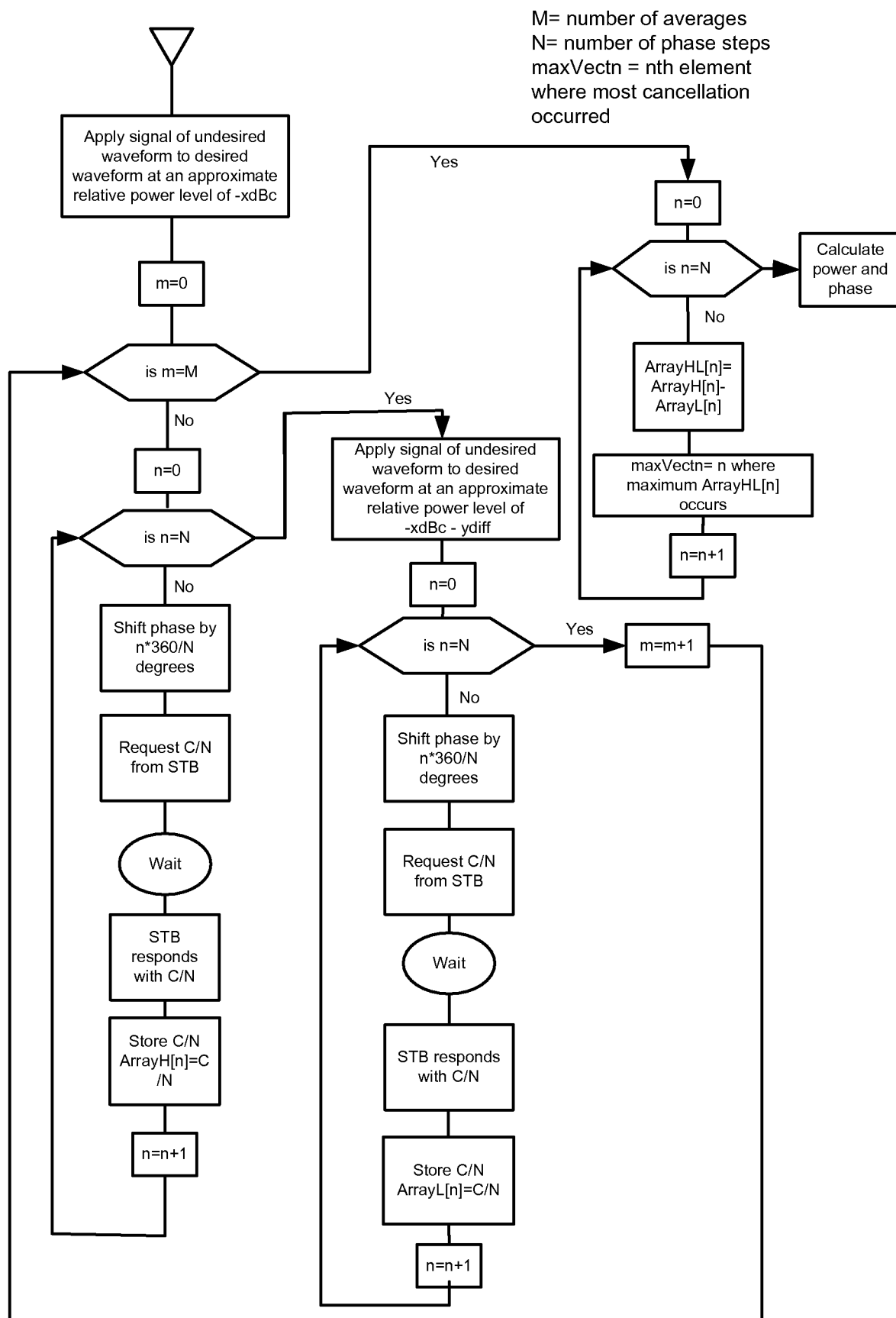


FIG. 13

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Channel Stacking System and Method of Operation		
First Named Inventor/Applicant Name:		Itzhak GURANTZ		
Filer:		Clifford B. Perry		
Attorney Docket Number:		RFM-30 P		
Filed as Large Entity				
Provisional Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Provisional application filing	1005	1	210	210
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				210

Electronic Acknowledgement Receipt

EFS ID:	3335593
Application Number:	61054886
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Confirmation Number:	2599
Title of Invention:	Channel Stacking System and Method of Operation
First Named Inventor/Applicant Name:	Itzhak GURANTZ
Customer Number:	77736
Filer:	Clifford B. Perry
Filer Authorized By:	
Attorney Docket Number:	RFM-30 P
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Filing Date:	
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Application Type:	Provisional

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1		RFM30P-20080521.pdf	511566 d23c547e9a1df6b3a8a7b56497da83f2a23d3be7	yes	60

	Multipart Description/PDF files in .zip description			
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	Specification	5	40	
	Claims	41	45	
	Abstract	46	46	
	Drawings-only black and white line drawings	47	60	

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2	Fee Worksheet (PTO-06)	fee-info.pdf	8111 fb1aa16607e29f01a7b6f5173edb2917be304dfd	no	2
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61/054,886	05/21/2008		210	RFM-30 P		

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Applicant(s)

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/054,886**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

Channel Stacking System and Method of Operation

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