

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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COMCAST CABLE COMMUNICATIONS, LLC,  
Petitioner,

v.

ENTROPIC COMMUNICATIONS, LLC,  
Patent Owner.

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Patent No. 11,785,275  
Filing Date: September 30, 2022  
Issue Date: October 10, 2023  
Title: SYSTEM AND METHOD FOR RECEIVING A TELEVISION SIGNAL

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*Inter Partes* Review No.: IPR2025-00181

**PETITION FOR *INTER PARTES* REVIEW  
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.***

## **TABLE OF CONTENTS**

|                                                                                          |     |
|------------------------------------------------------------------------------------------|-----|
| MANDATORY NOTICES.....                                                                   | vii |
| I. INTRODUCTION .....                                                                    | 1   |
| II. SUMMARY OF ARGUMENT.....                                                             | 1   |
| III. OVERVIEW OF THE '275 PATENT .....                                                   | 2   |
| A. Brief Description .....                                                               | 2   |
| B. Prosecution History .....                                                             | 6   |
| C. Earliest Priority Date for the Claims .....                                           | 7   |
| IV. OVERVIEW OF PRIOR ART .....                                                          | 7   |
| A. Petrovic.....                                                                         | 7   |
| 1. Petrovic Priority Date .....                                                          | 10  |
| 2. Pre-AIA 35 U.S.C. § 103(c) Does Not Apply .....                                       | 11  |
| B. Cholas.....                                                                           | 11  |
| C. Eidson.....                                                                           | 13  |
| D. Rabaey .....                                                                          | 14  |
| E. Lee .....                                                                             | 15  |
| F. Takahiko.....                                                                         | 15  |
| G. Maalej.....                                                                           | 16  |
| V. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R.<br>§ 42.104(b).....                 | 17  |
| A. Claims for Which Review is Requested and Grounds on Which<br>Challenge Is Based ..... | 17  |
| B. 314(a) Discretion Does Not Apply.....                                                 | 18  |
| C. 325(d) Discretion Does Not Apply .....                                                | 19  |
| D. Level of Ordinary Skill .....                                                         | 21  |
| E. Claim Construction .....                                                              | 21  |
| 1. “radio front end” .....                                                               | 21  |
| 2. “digital frontend (DFE)” .....                                                        | 22  |
| VI. SPECIFIC GROUNDS FOR UNPATENTABILITY .....                                           | 22  |

|       |                                                                                   |    |
|-------|-----------------------------------------------------------------------------------|----|
| A.    | Petrovic-Eidson (Claims 1, 4, 7-9, 11, 14, 17-19) .....                           | 22 |
| 1.    | Independent Claim 1 .....                                                         | 23 |
| 2.    | Independent Claim 11 .....                                                        | 40 |
| 3.    | <b>Claims 4, 14</b> .....                                                         | 44 |
| 4.    | <b>Claims 7-8, 17-18</b> .....                                                    | 44 |
| 5.    | <b>Claims 9, 19</b> .....                                                         | 45 |
| B.    | <b>Petrovic-Eidson-Rabaey (Claims 2-3, 12-13)</b> .....                           | 45 |
| C.    | <b>Petrovic-Eidson-Takahiko (Claims 11, 14, 17-19)</b> .....                      | 50 |
| D.    | <b>Petrovic-Eidson-Takahiko-Rabaey (Claims 12-13)</b> .....                       | 53 |
| E.    | <b>Cholas-Petrovic-Maalej (Claims 1, 4-5, 7-8, 10-11, 14-15, 17-18, 20)</b> ..... | 53 |
| 1.    | Independent Claims 1, 11 .....                                                    | 63 |
| 2.    | Claims 4, 14 .....                                                                | 69 |
| 3.    | Claims 5, 15 .....                                                                | 70 |
| 4.    | Claims 7-8, 17-18.....                                                            | 71 |
| 5.    | Claims 10, 20 .....                                                               | 72 |
| F.    | Cholas-Petrovic-Maalej-Rabaey (Claims 2-3, 12-13) .....                           | 72 |
| G.    | Cholas-Petrovic-Maalej-Lee (Claims 6, 16) .....                                   | 73 |
| H.    | Cholas-Petrovic-Maalej-Takahiko (Claims 11, 14-15, 17-18, 20) ....                | 74 |
| I.    | Cholas-Petrovic-Maalej-Takahiko-Rabaey (Claims 12-13) .....                       | 74 |
| J.    | Cholas-Petrovic-Maalej-Takahiko-Lee (Claim 16) .....                              | 74 |
| VII.  | GROUPS FOR STANDING & FEE PAYMENT .....                                           | 75 |
| VIII. | CONCLUSION.....                                                                   | 75 |
|       | CERTIFICATION UNDER 37 CFR § 42.24(d) .....                                       | 76 |
|       | CERTIFICATE OF SERVICE .....                                                      | 77 |
|       | <b>CLAIMS LISTING APPENDIX</b> .....                                              | 78 |

## EXHIBITS

- Ex. 1101: U.S. Patent No. 11,785,275 (“the ’275 patent”)
- Ex. 1102: Expert Declaration of David B. Lett
- Ex. 1103: Curriculum Vitae of David B. Lett
- Ex. 1104: Certified Prosecution History of the ’275 patent
- Ex. 1105: Certified Prosecution History of U.S. Patent No. 11,490,152 (“the parent”)
- Ex. 1106: Reserved
- Ex. 1107: Certified Prosecution History of U.S. Provisional App. No. 61/170,526 (“’526 provisional”)
- Ex. 1108: U.S. Pub. No. 2009/0290659 (“Petrovic”)
- Ex. 1109: Specification and drawings of U.S. Provisional App. No. 61/054,886 (“Petrovic ’886”)
- Ex. 1110: U.S.P.T.O Assignment Record for U.S. Pat. App. No. 12/414,892
- Ex. 1111: Reserved
- Ex. 1112: U.S. Patent No. 7,783,958 (“Eidson”)
- Ex. 1113: Reserved
- Ex. 1114: U.S. Patent No. 7,237,214 (“Pandey”)
- Ex. 1115: Excerpts of “IEEE Std 100-2000, The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition” (IEEE Press. 2000) (“IEEE Std 100”)
- Ex. 1116: Excerpts of Jan M Rabaey, “Digital Integrated Circuits: A Design Perspective” (Pearson, 2nd ed. 2002) (“Rabaey”)
- Ex. 1117: A. P. Chandrakasan, “Ultra low power digital signal processing,” Proceedings of 9th International Conference on VLSI Design, Bangalore, India, 1996, pp. 352-357 (“Chandrakasan”)

- Ex. 1118: S. Mirabbasi and K. Martin, “Classical and Modern Receiver Architectures,” IEEE Communications Magazine, vol. 38, no. 11, pp. 132-139, November 2000 (“Mirabbasi”)
- Ex. 1119: U.S. Patent No. 6,061,406 (“Carson”)
- Ex. 1120: Reserved
- Ex. 1121: “Data-Over-Cable Service Interface Specifications: Radio Frequency Interface Specification CM-SP-RF1v2.0-I11-060602,” DOCSIS, June 2006
- Ex. 1122-1124: Reserved
- Ex. 1125: J. Crols and M. S. J. Steyaert, “Low-IF topologies for high-performance analog front ends of fully integrated receivers,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998 (“Crols”)
- Ex. 1126: Reserved
- Ex. 1127: U.S. Patents and Patent Applications Family Tree for U.S. Pat. No. 11,785,275
- Ex. 1128-1132: Reserved
- Ex. 1133: Excerpts of W. Ciciora, J. Farmer, D. Large, and M. Adams, “Modern Cable Television Technology: Video, Voice, and Data Communications” (2<sup>nd</sup> ed. 2004) (“Ciciora”)
- Ex. 1134: Excerpts of J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design” (1997)
- Ex. 1135: U.S. Patent No. 7,340,230 (“Khoini-Poorfard”)
- Ex. 1136: U.S. Pub. No. 2003/0217362 (“Summers”)
- Ex. 1137: U.S. Pub. No. 2006/0256799 (“Eng”)
- Ex. 1138: U.S. Pub. No. 2006/0083335 (“Seendripu”)
- Ex. 1139: Excerpts of Chris Bowick, “RF Circuit Design” (2<sup>nd</sup> ed. 2008)

Ex. 1140: U.S. Pub. No. 2006/0031894 (“Petruzzelli”)

Ex. 1141: Excerpts of Roland Priemer, “Introductory Signal Processing” (1991)

Ex. 1142: U.S. Patent No. 7,272,375 (“Tuttle”)

Ex. 1143: U.S. Patent No. 7,130,576 (“Gurantz”)

Ex. 1144: U.S. Patent No. 5,278,837 (“Kelley”)

Ex. 1145: Jeffrey Hugh Reed, “Software Radio: A Modern Approach to Radio Engineering” (2002)

Ex. 1146: U.S. Patent No. 7,213,042 (“Cannon”)

Ex. 1147: Reserved

Ex. 1148: Excerpts of William Buchanan, “Computer Busses” (2000)

Ex. 1149: U.S. Patent No. 7,079,528 (“Ziegler”)

Ex. 1150: Excerpts of “Software Defined Radio: Enabling Technologies” (Walter H.W. Tuttlebee ed., 2003)

Exs. 1151-1152: Reserved

Ex. 1153: U.S. Pub. No. 2008/0039036 (“Lee”)

Ex. 1154: U.S. Pub. No. 2003/0220072 (“Coffin”)

Ex. 1155: U.S. Patent No. 6,493,873 (“Williams”)

Ex. 1156: U.S. Pub. No. 2007/0053314 (“Gat”)

Ex. 1157: Reserved

Ex. 1158: U.S. Pub. No. 2010/0020794 (“Cholas”)

Ex. 1159: Reserved

Ex. 1160: U.S. Patent No. 6,160,443 (“Maalej”)

Ex. 1161: U.S. Pub. No. 2006/0256216 (“Takahiko”)

Exs. 1162-1169: Reserved

Ex. 1170: U.S.P.T.O Assignment Record for U.S. Patent No. 8,526,898

Ex. 1171: U.S.P.T.O Assignment Record for U.S. Patent No. 7,783,958 (“Eidson”)

Ex. 1172: Reserved

Ex. 1173: Expert Declaration of Dr. Sylvia Hall-Ellis

Ex. 1174: Reserved

Ex. 1175: U.S. Patent No. 6,791,995 (“Azenkot”)

Ex. 1176: U.S. Patent No. 6,542,203 (“Shadwell”)

Exs. 1177-1179: Reserved

Ex. 1180: Certified Copy of U.S. Pat. App. No. 11/681,774, as-filed March 3, 2007

Ex. 1181: U.S. Pub. No. 2007/0250864 (“Diaz Perez”)

Ex. 1182: U.S. Pub. No. 2007/0180485 (“Dua”)

Ex. 1183: U.S. Pub. No. 2005/0114904 (“Monk”)

Ex. 1184: U.S. Patent No. 5,317,391 (“Banker”)

## MANDATORY NOTICES

### **Real Parties in Interest (37 C.F.R. § 42.8(b)(1))**

The real parties-in-interest for this petition are (i) Comcast Corporation, (ii) Comcast Cable Communications, LLC, and (iii) Comcast Cable Communications Management, LLC. No unnamed entity is funding, controlling, or directing this Petition for *inter partes* review (IPR) of U.S. Patent No. 11,785,275 (“the ’275 patent”), or otherwise has an opportunity to control or direct this Petition or Petitioner’s participation in any resulting IPR.

### **Related Matters (37 C.F.R. § 42.8(b)(2))**

#### Office Proceedings

This is the second of three petitions for *inter partes* review filed by Petitioner against the ’275 patent. Petitioner has previously filed petitions for *inter partes* review of related U.S. Patent Nos. 9,210,362 (“the ’362 patent”) (case nos. IPR2024-00432, IPR2024-00433, and IPR2024-00434), 11,381,866 (“the ’866 patent”) (case nos. IPR2024-00435, IPR2024-00436, and IPR2024-00437), and 11,399,206 (“the ’206 patent”) (case nos. IPR2024-00438, IPR2024-00439, and IPR2024-00440), which include similar claims to claims of the ’275 patent. The Board has already instituted IPR2024-00432 (for the ’362 patent), IPR2024-00435 (for the ’866 patent), and IPR2024-00438 (for the ’206 patent). The petitions for the other IPRs challenging the ’362, ’866, and ’206 patents were discretionarily denied institution without addressing the merits of those petitions.

No other Office proceedings (e.g., *inter partes* review, post-grant review, or covered business method) have been filed against the '275 patent.

According to the Office's records, a request for *ex parte* reexamination (Control No. 90/019,255) was filed September 20, 2023 for claims 1 and 11 of the '362 patent, and an Order granting the request was issued on November 1, 2023. The requestor of the *ex parte* reexamination, Unified Patents, LLC, is not a real party-in-interest for this petition.

#### Litigation matters

Patent Owner has sought leave to assert the '275 patent in *Entropic Communications, LLC v. Comcast Corporation*, No. 2:23-cv-01050 (C.D. Cal. filed Feb. 10, 2023) and *Entropic Communications, LLC v. Cox Communications, Inc.*, No. 2-23-cv-01049 (C.D. Cal. filed Feb. 10, 2023) (collectively, "CA litigation"). These cases have been consolidated and remain pending. The related '362 patent, '866 patent, and '206 patent have been asserted in the CA litigation.

The related '362 patent, '866 patent, and '206 patent were also asserted in *Entropic Communications, LLC v. Charter Communications, Inc.*, No. 2:22-cv-00052-JRG (E.D. Tex. filed Apr. 27, 2022), which case was dismissed on December 10, 2023.

The '275 patent, as well as the related '866 patent and '206 patent, are asserted in *Entropic Communications, LLC v. Vantiva SA*, No. 2:24-cv-00912 (E.D. Tex. filed Nov. 11, 2024).

### Continuity

According to Office records, the '275 patent is a continuation of application No. 17/862,946, filed on Jul. 12, 2022, now Pat. No. 11,490,152, which is a continuation of application No. 17/587,462, filed on Jan. 28, 2022, now Pat. No. 11,399,206, which is a continuation of application No. 17/217,244, filed on Mar. 30, 2021, now abandoned, which is a continuation of application No. 16/430,506, filed on Jun. 4, 2019, now Pat. No. 10,972,781, which is a continuation of application No. 15/792,318, filed on Oct. 24, 2017, now Pat. No. 10,313,733, which is a continuation of application No. 14/948,881, filed on Nov. 23, 2015, now Pat. No. 9,819,992, which is a continuation of application No. 14/617,973, filed on Feb. 10, 2015, now Pat. No. 9,210,363, which is a continuation of application No. 13/962,871, filed on Aug. 8, 2013, now Pat. No. 9,100,622, which is a continuation of application No. 12/762,900, filed on Apr. 19, 2010, now Pat. No. 8,526,898, which claims the benefit of Provisional application No. 61/170,526, filed Apr. 17, 2009.

Also according to Office records, Application No. 18/461,104, filed on Sep. 5, 2023, is a continuation of the '275 patent.

The '275 patent is part of a family that includes numerous patents or applications that purport to claim priority from App. No. 12/762,900. A family tree is included as Ex. 1127.

**Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3))**

Petitioner designates counsel listed below. A power of attorney for counsel is being concurrently filed.

| <b><u>Lead Counsel</u></b>                                                                                                         | <b><u>Back-Up Counsel</u></b>                                                                                                      |
|------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|
| Frederic M. Meeker (Reg. No. 35,282)<br>fmeeker@bannerwitcoff.com                                                                  | H. Wayne Porter (Reg. No. 42,084)<br>wporter@bannerwitcoff.com                                                                     |
| BANNER & WITCOFF, LTD.<br>1100 13th Street, NW<br>Suite 1200<br>Washington, DC 20005<br>Tel: (202) 824-3000<br>Fax: (202) 824-3001 | Craig W. Kronenthal (Reg. No. 58,541)<br>ckronenthal@bannerwitcoff.com                                                             |
|                                                                                                                                    | Paul T. Qualey (Reg. No. 45,027)<br>pqualey@bannerwitcoff.com                                                                      |
|                                                                                                                                    | Joshua L. Davenport (Reg. No. 72,756)<br>jdavenport@bannerwitcoff.com                                                              |
|                                                                                                                                    | BANNER & WITCOFF, LTD.<br>1100 13th Street, NW<br>Suite 1200<br>Washington, DC 20005<br>Tel: (202) 824-3000<br>Fax: (202) 824-3001 |

Please address all correspondence to counsel at the address shown above.

Petitioner consents to electronic service by email at the above email addresses and at [ComcastIPRService@bannerwitcoff.com](mailto:ComcastIPRService@bannerwitcoff.com).

## **I. INTRODUCTION**

Comcast Cable Communications, LLC (“Petitioner”) petitions for *inter partes* review of claims 1-20 of U.S. Patent No. 11,785,275 (“the ’275 patent”) (Ex. 1101).

## **II. SUMMARY OF ARGUMENT**

The ’275 patent generally claims a television receiver and a method of operating it to select and output desired channels. The receiver includes a radio front end for processing a radio frequency (RF) input signal that includes desired and undesired channels, an analog-to-digital converter (ADC) that digitizes the RF input signal, and a digital frontend (DFE) that selects the desired channels and outputs them to at least one demodulator.

The ’275 patent admits that the portion of the television receiver including the radio front end and ADC “is similar to conventional tuners.” Ex. 1107, p. 5; Ex. 1101, 1:6-28. The alleged inventive concept—demodulating multiple digitized channels—simply copies well-known digital circuitry for demodulating each channel. The ’275 patent claims are disclosed or rendered obvious by the prior art, e.g., Petrovic (Ex. 1108) and other references relied on herein.

Accordingly, claims 1-20 of the ’275 patent are unpatentable and should be cancelled.

### III. OVERVIEW OF THE '275 PATENT

#### A. Brief Description

The '275 patent describes a wideband receiver system 200 “capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum.” Ex. 1101, 1:32-35; Ex. 1102, ¶ 36. Figure 2 is a “block diagram of a wideband receiver system 200.” Ex. 1101, 4:40-42; Ex. 1102, ¶ 37.

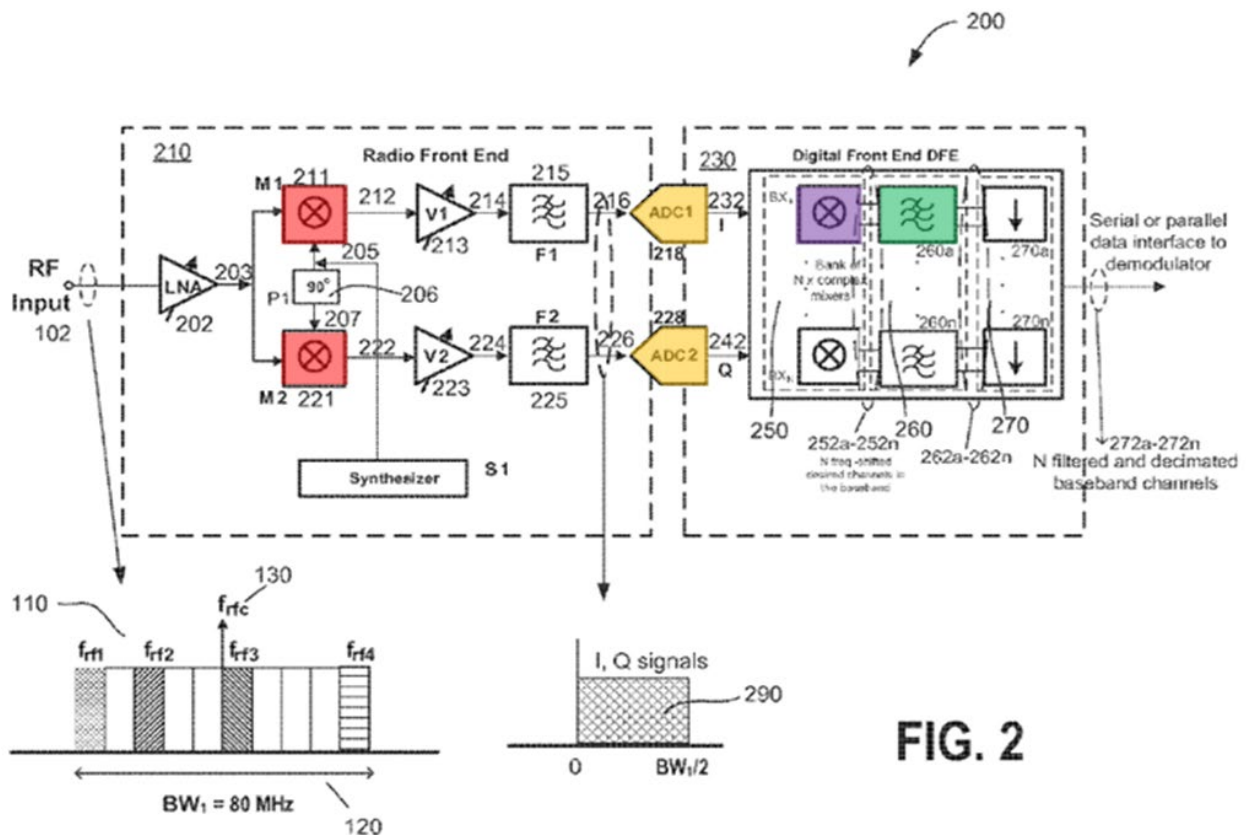


FIG. 2

Ex. 1101, Fig. 2 (annotated)

The wideband receiver system 200 receives both desired and undesired television channels as frequencies dispersed within a frequency bandwidth  $BW_1$ . Ex. 1101, Abstract, 4:43-58; Ex. 1102, ¶ 38. A “radio front end” contains mixers M1 and M2 (red) that “generate an in-phase signal 212 and a quadrature signal 222 that

have a phase shift of 90° degrees between them” and that have been downconverted to “the baseband or low intermediate frequency (IF) band.”<sup>1</sup> Ex. 1101, 4:65-5:4, 2:64-3:1, *see also* 2:10-12. “[U]nwanted frequency components” are filtered from the in-phase and quadrature signals by respective filters 215 and 225. *Id.*, 5:22-29. The filtered signals are then individually digitized by wideband analog-to-digital converters ADC1 and ADC2 (**gold**) to generate a digital in-phase (I) signal 232 and a digital quadrature (Q) signal 242. *Id.*, 3:1-3, 5:53-56. U.S. Provisional App. No. 61/170,526 (“’526 provisional”), which the ’275 patent incorporates by reference, admits that the left side of Figure 2 (up to and including ADC1 and ADC2) “is similar to conventional tuners.” Ex. 1107, p. 5; Ex. 1101, 1:6-28; Ex. 1102, ¶ 38.

The digital I and Q signals 232 and 242 are input to a digital front end 230, containing a bank of N complex mixers 250 (one of which is highlighted in **purple**),

---

<sup>1</sup> A mixer multiplies an input signal (frequency  $f_1$ ) by a reference signal (frequency  $f_2$ ) to produce new signals at the sum and difference frequencies ( $f_1+f_2$  and  $f_1-f_2$ ). Ex. 1102, ¶ 66. The reduced frequency ( $f_1-f_2$ ) version is output as the “down converted” complex signal with real (I) and imaginary (Q) components. *Id.*, ¶¶ 66-67.

where N is “the number of desired RF channels.”<sup>2</sup> Ex. 1101, 5:56-60. “Each of the N complex mixers ... extract a different one of the desired channels” from the I and Q signals 232 and 242 and “frequency-shifts the extracted signals to the baseband frequency.”<sup>3</sup> Ex. 1101, 6:8-11. The output of each mixer 250 leads to an associated filter module 260 (one of which is highlighted in **green**), which filters the frequency-shifted desired channel. Ex. 1101, 6:11-13; Ex. 1102, ¶ 39.

Figure 3 “is a simplified circuit diagram of one of the signal paths 272a to 272n of digital front end 230” and shows the elements in one of the rows of digital front end 230 in Figure 2. Ex. 1101, 6:21-23; Ex. 1102, ¶ 40.

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<sup>2</sup> Complex mixers multiply signals already separated into their complex I and Q components. Ex. 1102, ¶ 66.

<sup>3</sup> Signals have a center frequency  $f$  that is modulated with data. Shifting the signal to baseband reduces  $f$  to zero, enabling filters to easily pass only the modulated data as the output. Ex. 1102, ¶¶ 60-70.

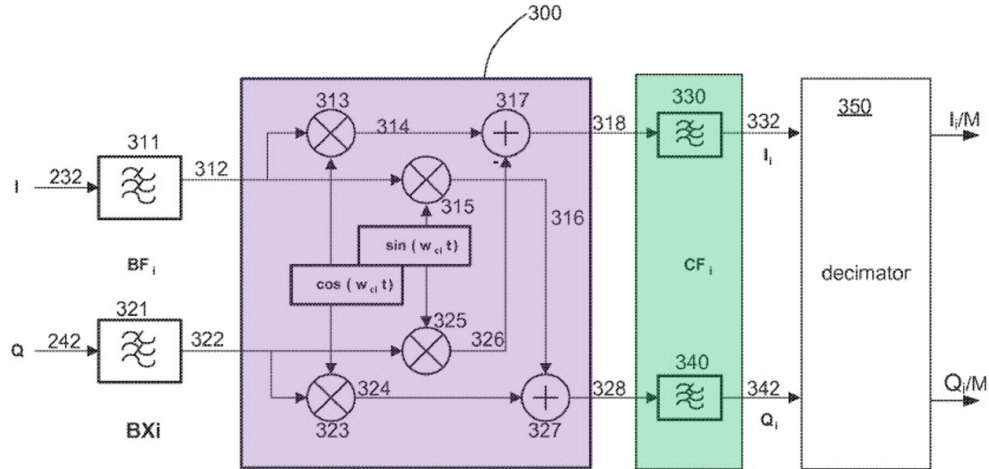


**FIG. 3**

**Ex. 1101, Fig. 3 (annotated)**

Mixer 300 (**purple**) represents one of the complex mixers 250 and has multipliers 313, 315, 323, and 325 and adders 317 and 327. Ex. 1101, 6:33-43. “[C]omplex mixer 300 causes a frequency shift of the filtered components 312 and 322 to respective baseband signals 318 and 328 in the digital domain” by multiplying the I and Q signals by a frequency  $\omega_{ci}$  that is “chosen [so] that each one of the desired channels embedded in the digital signals I 232 and Q 242 will be downshifted to the baseband.” Ex. 1101, 6:43-62. Filters 330 and 340 (**green**), which are one of the filter modules 260a-n in Figure 2, filter baseband signals 318 and 328. Ex. 1101, 7:3-5; Ex. 1102, ¶ 41. This exact structure was a conventional design, simply copied multiple times to downconvert multiple channels, respectively. *See e.g.*, Ex. 1102, ¶¶ 62-69.

Finally, the '275 patent describes that the “N desired baseband channels” may be decimated before being sent to an associated demodulator “using a serial or parallel data interface according to commonly known methods.” Ex. 1101, 6:13-19, 7:16-20, Figs. 2-3; Ex. 1102, ¶ 42.

## **B. Prosecution History**

The application which became the '275 patent was rejected only for nonstatutory double patenting based on its parent (Pat. No. 11,490,152), which had similar claims but did not include the “non-contiguous” limitation. Ex. 1104, pp. 3352-3357; Ex. 1102, ¶¶ 43-46. The examiner stated that such limitation was “an obvious condition.” Ex. 1104, p. 3356. After a terminal disclaimer was filed, the application was allowed. Ex. 1104, pp. 3384-3406.

In the reasons for allowance, the examiner alleged that “[t]he prior art made of record do not teach selecting, by a digital frontend (DFE) coupled to the ADC, a plurality of desired channels from the digitized signal and outputting by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream.” Ex. 1104, p. 3405. This was the same reason for allowance given in the parent, which was also allowed with no substantive prosecution. *Compare* Ex. 1104, p. 3405 *with* Ex. 1105, p. 158; Ex. 1102, ¶ 45. After an RCE and two IDSs to cite litigation documents and references, another notice of allowance was sent and the '275 patent was issued. Ex. 1104, pp. 3415-4831, 4857. None of Petrovic, Cholas,

Rabaey, Maalej, Lee, or Takahiko were considered during prosecution. Ex. 1104, pp. 4824-4831; Ex. 1101, pp. 1-3; Ex. 1102, ¶ 46; *see* Section V.C.

### **C. Earliest Priority Date for the Claims**

The earliest possible effective filing date for the claims of the '275 patent is April 17, 2009. Ex. 1101, cover, page 2; Ex. 1102, ¶ 47. Each reference relied on herein is prior art to that date.

## **IV. OVERVIEW OF PRIOR ART**

### **A. Petrovic**

Petrovic is a publication of U.S. Pat. App. No. 12/414,892, filed March 31, 2009, that claims priority to and incorporates by reference U.S. Provisional App. No. 61/054,886 (“Petrovic ’886”).<sup>4</sup> Ex. 1108, cover, [0001]. Petrovic is pre-AIA 35 U.S.C. § 102(e) prior art, as explained below. Ex. 1102, ¶¶ 78-87.

Petrovic describes a “channel stacking system” that receives wideband RF signals 102-106. Ex. 1108, [0028]-[0029], Fig. 4; Ex. 1109, [0008], [0010]-[0013], [0016], [0023], [0026], Fig. 1; Ex. 1102, ¶¶ 80-81.

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<sup>4</sup> The specification and drawings of Petrovic ’886, cited by paragraph and Figure numbers, are at pages 6-61 of Ex. 1109.

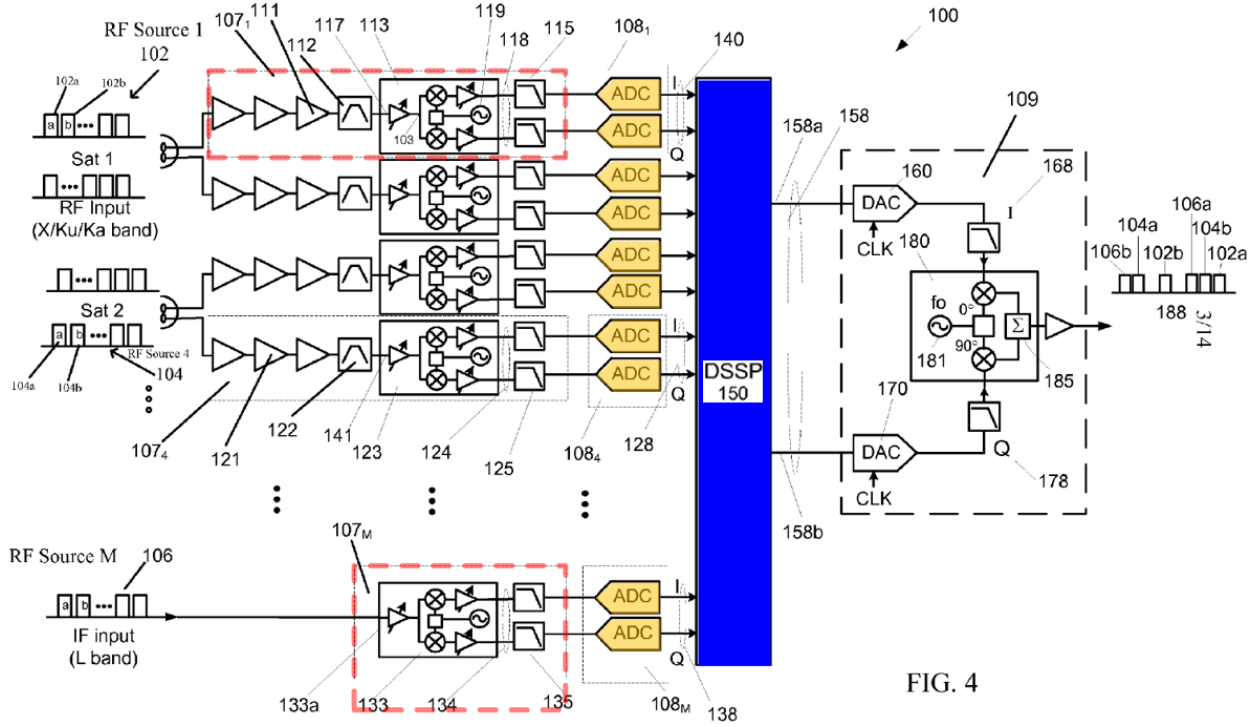


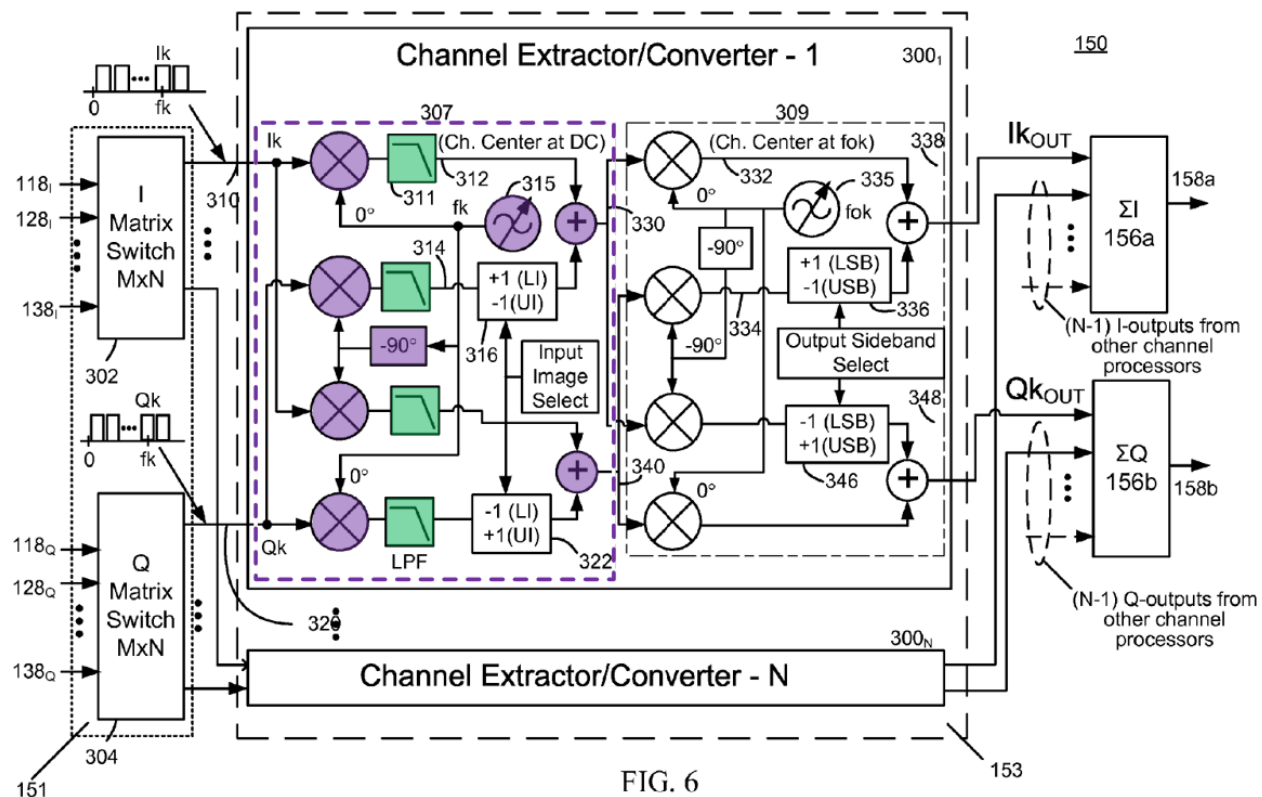
FIG. 4

### Ex. 1108, Fig. 4 (annotated)

The signals 102-106 are coupled to “analog preprocessing and downconversion (APD) stages 107<sub>I-M</sub>” (two marked in **red** broken lines). Ex. 1108, [0032], Fig. 4; Ex. 1109, [0010], [0013], [0020], Fig. 1; Ex. 1102, ¶ 81. Those APD stages downconvert RF signals into in-phase (I) and quadrature (Q) intermediate frequency (IF) signals that are, after filtering, digitized by analog-to-digital converters 108<sub>I-M</sub> (**gold**). Ex. 1108, [0032]-[0039], [0050]-[0052], Figs. 4-6; Ex. 1109, [0010], [0013], [0018]-[0024], [0031]-[0032], Figs. 1-3A; Ex. 1102, ¶ 81.

Digital signal switching and pre-processing stage (DSSP) 150 (**blue**) receives the digitized signals and “extract[s] the channels of interest ... (i.e., remove[s] all the channels that are not of interest).” Ex. 1108, [0042], [0040], Fig. 4; Ex. 1109, [0015], [0025], [0033], Fig. 1; Ex. 1102, ¶ 82. Figure 6 shows details of the DSSP

150, including “channel extractor/converter circuit 300.” Ex. 1108, [0058]; Ex. 1109, [0033], Fig. 3A; Ex. 1102, ¶ 82.



**Ex. 1108, Fig. 6 (annotated)**

Like the '275 patent, a channel is extracted from the digitized I, Q signals corresponding to one of the RF sources 102-106 by downconverting those signals in a complex mixer (**purple** and/or **purple** broken-line box) of a stage 307 so the desired channel is at baseband, and filtering using low pass filters (LPFs) 311 (**green**), to create I, Q components 330, 340 for the extracted channel. Ex. 1108, [0058]-[0077]; Ex. 1109, [0036]-[0054]; Ex. 1102 ¶ 83.

Petrovic is analogous art. Ex. 1102, ¶ 85. Petrovic describes a system and method for receiving wideband RF signals comprising multiple channels, as well as

selecting individual desired channels (in the same way as the '275 patent) by conversion to baseband and filtering. *Id.*; Ex. 1108, Abstract, [0029]-[0030], [0042], [0047], [0050], [0058]-[0077], Figs. 4, 6; Ex. 1109, [0010]-[0011], [0013], [0015]-[0016], [0020], [0023], [0033], [0037]-[0054], Figs. 1, 3A; Ex. 1101, 6:21-7:15, Fig. 3.

### 1. Petrovic Priority Date

Petrovic is pre-AIA 35 U.S.C. § 102(e) prior art based on its March 31, 2009, filing date regardless of whether it is entitled to the priority of Petrovic '886. But Petrovic is entitled to that priority, and thus is prior art as of the May 21, 2008, filing date of Petrovic '886. At least claim 14 of Petrovic is supported by Petrovic '886. Ex. 1102, ¶¶ 86-87.

| Petrovic – Claim 14 (Ex. 1108)                                                                                                                                                                | Petrovic '886 (Ex. 1109)                                           |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|
| 14. A method for assembling channels in a composite signal, the method comprising:                                                                                                            | <i>E.g.</i> , [0001], [0004], [0008], claim 16.                    |
| a) downconverting, in a single frequency translation process, a first input signal comprising a first plurality of channels to a first IF signal comprising said plurality of first channels; | [0005], [0010], [0014], [0029], [0031]-[0032], claim 16, Figs. 1-2 |
| b) converting the first IF signal into a first digital IF signal;                                                                                                                             | [0010], claim 16, Fig. 1                                           |

| <b>Petrovic – Claim 14 (Ex. 1108)</b>                                                                                                                                                             | <b>Petrovic '886 (Ex. 1109)</b>                                           |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|
| c) downconverting, in a single frequency translation process, a second input signal comprising a plurality of second channels to a second IF signal comprising said plurality of second channels; | [0005], [0013]-[0014], [0023], [0029], [0031]-[0032], claim 16, Figs. 1-2 |
| d) converting the second IF signal into a second digital IF signal; and                                                                                                                           | [0005], [0013], [0024], claim 16, Fig.1                                   |
| e) assembling, in the digital domain, at least one of the first channels and at least one of the second channels into a digital composite signal.                                                 | [0015], [0025], [0036]-[0068], [0080], claim 16, Figs. 3A-3B              |

Parallel citations to Petrovic and Petrovic '886 show relied-on disclosure is prior art as of the May 21, 2008, filing date of Petrovic '886.

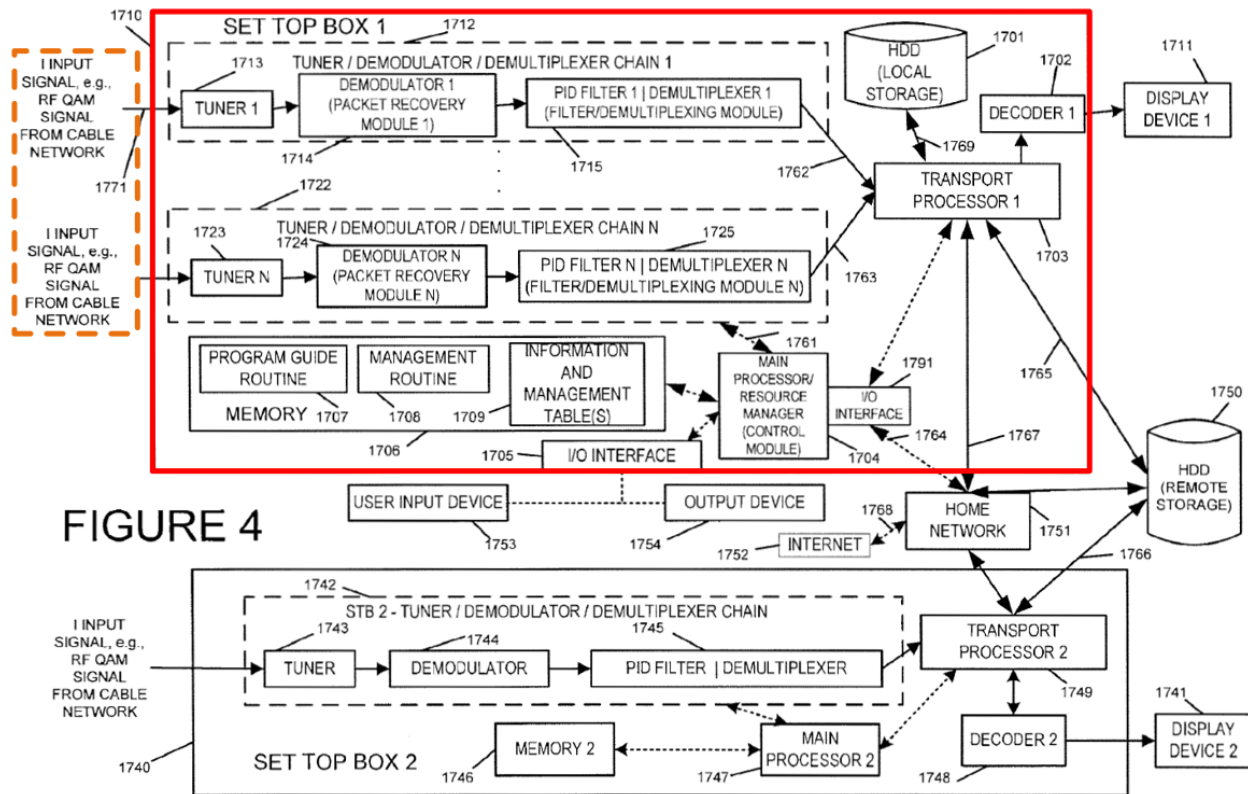
## **2. Pre-AIA 35 U.S.C. § 103(c) Does Not Apply**

Petrovic was assigned to Entropic Communications, Inc. until April 30, 2015. Ex. 1108, cover; Ex. 1110, pp. 3, 24. The claimed invention of the '275 patent was not, at the time made, owned by Entropic Communications, Inc. Ex. 1170, pp. 2-5.

### **B. Cholas**

Cholas, a publication of U.S. Pat. App. No. 11/754,714, filed May 29, 2007, is pre-AIA 35 U.S.C. § 102(e) prior art. Ex. 1158, cover. Cholas describes a set-top box (STB) 1710 (**red**) with tuner/demodulator/demultiplexer chains 1-N that receive

“input signal[s] [orange] ... from the cable network.” *Id.*, [0044], [0010]-[0011], [0024], [0059]-[0071], Figs. 4, 6; Ex. 1102, ¶¶ 88-89.

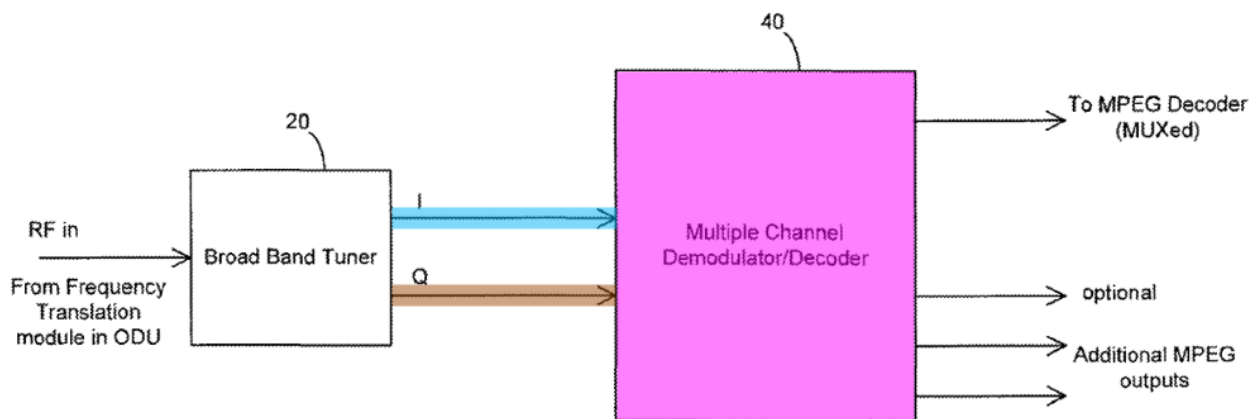


**Ex. 1158, Fig. 4 (annotated)**

Cholas is analogous art. Ex. 1102, ¶ 90. Like the '275 patent, Cholas “relates to wideband receiver systems that are capable of receiving multiple desired television channels.” Ex. 1101, 1:36-37; Ex. 1158, [0001], [0043]-[0045], [0052]-[0057], Figs. 4-5; Ex. 1102, ¶ 90. Cholas also relates to cable network STBs, an expected environment for the wideband receiver system of the '275 patent. Ex. 1101, 1:52-54, 5:12-16, claims 9, 10; Ex. 1158, [0043]-[0045], Fig. 4; Ex. 1102, ¶ 90.

### C. Eidson

Eidson is a U.S. Patent that issued based on an application filed November 1, 2006. Ex. 1112, cover. Eidson is pre-AIA 35 U.S.C. § 102(e) prior art and describes a multiple-channel receiver that demodulates multiple channels using a multiple channel demodulation and error correction decoding engine. Ex. 1112, Abstract, 8:27-30; Ex. 1102, ¶¶ 91-92. Eidson's Figure 8 "shows a broadband tuner and multi-channel demodulator and decoder." Ex. 1112, 7:58-59; Ex. 1102, ¶ 92.



**Ex. 1112, Fig. 8 (annotated)**

A frequency translation module (FTM) located in an outdoor unit selects desired satellite transponder channels and translates those selected channels to a contiguous section of bandwidth that is received by a broad band tuner 20. Ex. 1112, 8:43-57; Ex. 1102, ¶ 93. The digital outputs of the tuner 20 are I (**light blue**) and Q (**brown**) signals that represent multiple selected transponder channels. Ex. 1112, 8:54-57, 9:5-25, Figs. 9-10; Ex. 1102, ¶ 93. As discussed in more detail below, these I and Q signals input to the multiple channel demodulator/decoder 40 (**pink**) are

functionally the same as the summed I signal 158a and the summed Q signal 158b output by the Petrovic DSSP 150. Ex. 1102, ¶ 93. In Eidson, the digital I and Q output of the broadband tuner 20 “is processed by a multiple channel demodulator and decoder 40 to produce one or more MPEG streams comprising multiple video programs derived from the selected transponder channels.” *Id.*; Ex. 1112, 8:65-9:2.

Eidson is analogous art. Ex. 1102, ¶ 94. For example, the '275 patent indicates that signals recovered from received RF signals may be output to a demodulator, but leaves the particulars to “commonly known methods.” *Id.*; Ex. 1101, 7:16-19, Fig. 2. A POSITA would consider Eidson, which relates to demodulation of signals for multiple channels, as a pertinent example of those “commonly known methods.” Ex. 1102, ¶ 94.

Eidson was, at all relevant times, assigned to Entropic Communications, Inc. Ex. 1112, cover; Ex. 1171, pp. 3-11. For reasons similar to those set forth in Section IV.A.2, pre-AIA 35 U.S.C. § 103(c) is inapplicable to Eidson.

#### **D. Rabaey**

Rabaey is a textbook on digital integrated circuit design. Ex. 1116, p. 1. Rabaey was published by October 22, 2003, and publicly available to a POSITA by that date, and is pre-AIA 35 U.S.C. § 102(b) prior art. Ex. 1173, ¶¶ 47-54. Rabaey describes the “commonly known methods” of sending “a serial or parallel digital

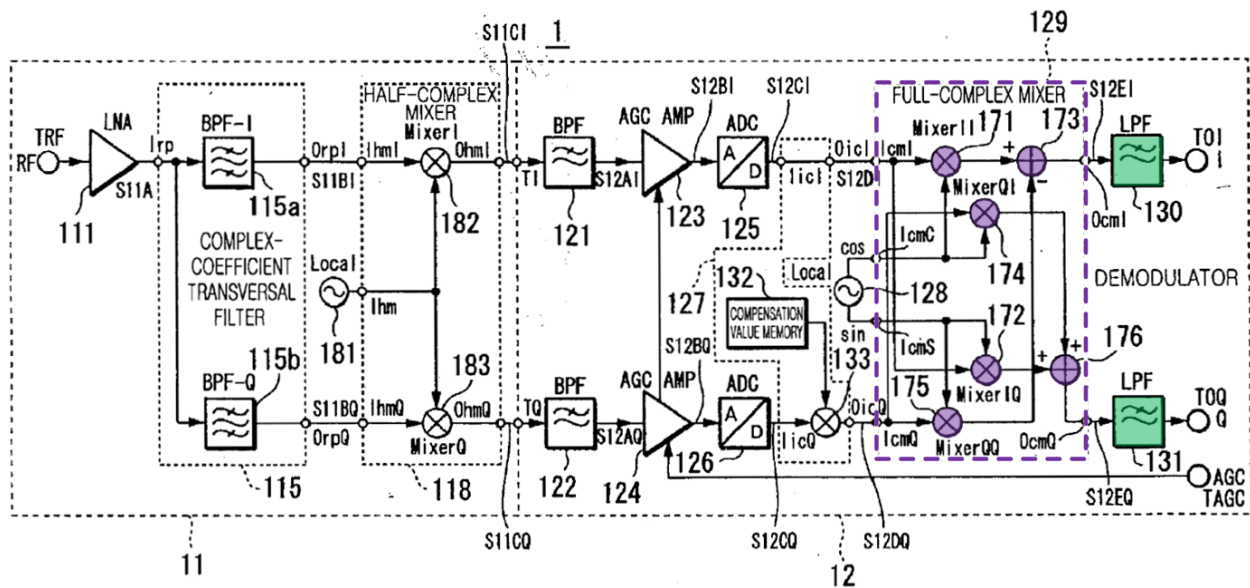
data stream to a demodulator using a serial or parallel data interface” that the ’275 patent references, and is analogous art. Ex. 1101, 7:16-19; Ex. 1102, ¶ 95.

**E. Lee**

Lee, a February 14, 2008, U.S. Patent Application Publication, is pre-AIA 35 U.S.C. § 102(b) prior art. Ex. 1153, cover. Lee describes a STB that receives cable broadcasting signals. Ex. 1153, [0035]; Ex. 1102, ¶ 96. Lee, which is analogous art, describes a STB having claimed features (picture-in-picture display). Ex. 1153, [0007], [0031]; Ex. 1102, ¶ 96.

**F. Takahiko**

Takahiko, a November 16, 2006, U.S. Patent Application Publication, is pre-AIA 35 U.S.C. § 102(b) prior art. Ex. 1161, cover. Takahiko discloses a downconverter of a radio receiver that includes a digital baseband complex mixer (**purple**) and low pass filters (**green**) similar to those of the ’275 patent. Ex. 1161, [0143], [0153], [0156]; Ex. 1102, ¶ 97.



**Ex. 1161, Fig. 1 (annotated)**

Takahiko, which is analogous art, describes circuits also described by the '275 patent and which are used for similar purposes—reception and tuning of RF signals. Ex. 1161, [0143]-[0156], Fig. 1; Ex. 1102, ¶ 98.

### G. Maalej

Maalej, a U.S. Patent that issued December 12, 2000, is pre-AIA 35 U.S.C. § 102(b) prior art. Ex. 1160, cover. Maalej discloses a QAM demodulator for, e.g., demodulating 6 MHz CATV channels. Ex. 1160, 1:6-8, 1:28-33, 3:47-52; Ex. 1102, ¶ 99. Maalej, which is analogous art, relates to a claimed feature (“at least one demodulator”). Ex. 1160, 1:6-8, 1:28-32, 3:47-52; Ex. 1102, ¶ 99.

**V. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R. § 42.104(b)**

**A. Claims for Which Review is Requested and Grounds on Which Challenge Is Based**

Petitioner requests review of claims 1-20 on the following pre-AIA 35 U.S.C.

§ 103 grounds:

| Ground | References                             | Claims Challenged                    |
|--------|----------------------------------------|--------------------------------------|
| A      | Petrovic-Eidson                        | 1, 4, 7-9, 11, 14, 17-19             |
| B      | Petrovic-Eidson-Rabaey                 | 2-3, 12-13                           |
| C      | Petrovic-Eidson-Takahiko               | 11, 14, 17-19                        |
| D      | Petrovic-Eidson-Takahiko-Rabaey        | 12-13                                |
| E      | Cholas-Petrovic-Maalej                 | 1, 4-5, 7-8, 10-11, 14-15, 17-18, 20 |
| F      | Cholas-Petrovic-Maalej-Rabaey          | 2-3, 12-13                           |
| G      | Cholas-Petrovic-Maalej-Lee             | 6, 16                                |
| H      | Cholas-Petrovic-Maalej-Takahiko        | 11, 14-15, 17-18, 20                 |
| I      | Cholas-Petrovic-Maalej-Takahiko-Rabaey | 12-13                                |
| J      | Cholas-Petrovic-Maalej-Takahiko-Lee    | 16                                   |

A supporting declaration of David B. Lett includes a discussion of Mr. Lett's background (Ex. 1102, ¶¶ 1-16), materials he considered and his understanding of legal standards (*id.*, ¶¶ 17-29), skill in the art (*id.*, ¶¶ 30-32), claim construction (*id.*, ¶¶ 33-35), the '275 patent (*id.*, ¶¶ 36-47), and the prior art (*id.*, ¶¶ 48-99), as well as

his opinions and bases therefor (*id.*, ¶¶ 1-228). Mr. Lett at least meets the level of skill of a POSITA. *Id.*, ¶¶ 2-16, 30-32; Ex. 1103.

**B. 314(a) Discretion Does Not Apply**

The Fintiv factors as set forth in the Director's June 21, 2022 Guidance Memorandum do not warrant discretionary denial.

Factor one appears neutral. The PTAB has instituted IPR on seven of the eight patents originally asserted in the District Court in case no. 2:23-cv-01050, and Petitioner is now filing IPR petitions challenging a patent that Patent Owner seeks to add to the case. Petitioner has also requested a stay, as final written decisions on the instituted IPRs in Petitioner's favor would resolve the majority of the litigation.

Factor two favors institution. Petitioner has filed a motion to dismiss the District Court case, Patent Owner has filed motions for leave to file amended complaints, and Petitioner will renew its Motion to Dismiss in order to seek dismissal of the operative complaint. In addition, no schedule beyond claim construction has been entered, and the Court has not set a trial date.

Factor three favors institution. To date, the investment by the District Court has been limited to considering motions to dismiss on the pleadings and hearing arguments on claim construction. The Court has not yet heard claim construction arguments on the '275 patent, and there is presently no schedule in place for claim construction proceedings on the '275 patent.

Factor four strongly favors institution. The petition challenges all claims in the '275 patent while Patent Owner seeks to assert only claims 1, 2, 5, 7, 8, 10-12, 15, 17, 18, and 20 in the District Court.

Factor five does not warrant denial as Petitioner is a defendant in the District Court case.

Factor six favors institution. Petitioner presents compelling unpatentability challenges that merit institution, relying on prior art that was never discussed and arguments that were never presented or were overlooked during prosecution.

**C. 325(d) Discretion Does Not Apply**

Considering the two-part framework discussed in *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH*, No. IPR2019-01469, Paper 6 at 8-9 (PTAB Feb. 13, 2020), the Board should not deny institution. The grounds raised herein are not the same or substantially the same as the art and arguments raised during prosecution, and to the extent that they are, the Examiner erred in a manner material to the patentability of the challenged claims by failing to find and/or fully consider all of the relevant prior art, including Petrovic and Cholas, that teach the limitations of the independent and dependent claims.

No IDS or Office Action cites or mentions Petrovic or U.S. Patent No. 8,345,798 (Petrovic '798), which issued based on Petrovic. Ex. 1104, pp. 4-11, 125-130, 3352-3357, 3418-3420, 4820-22. The patent number of Petrovic '798 appears

twice—without analysis or discussion—buried in 4589 pages of NPL documents that the applicant submitted. Ex. 1104, pp. 2309, 2839. The “Petrovic” mentioned in the claim charts and other analyses included in those NPLs is a different patent with a disclosure different from that of Petrovic ’798. *E.g.*, Ex. 1104, p. 2333. Moreover, Petrovic ’798 is only identified in NPL documents addressing U.S. Patent No. 8,792,008, which is unrelated to the ’275 patent. Ex. 1104, pp. 2293, 2308-2309, 2823, 2838-2839. In sum, there is no basis to assume the examiner considered Petrovic ’798 or Petrovic, much less that the Office meaningfully addressed either reference by evaluating and articulating a meaningful consideration. *See* [Proposed] Patent Trial and Appeal Board Rules of Practice for Briefing Discretionary Denial Issues, and Rules for 325(d) Considerations, Instituting Parallel and Serial Petitions, and Termination Due to Settlement Agreement, 89 Fed. Reg. 28693, 28705 (proposed Apr. 19, 2024).

Eidson was not meaningfully considered. There is a single occurrence of the Eidson patent number in the 4,862 pages of the ’275 patent prosecution history. Ex. 1104, p. 3411. In any event, Eidson is a secondary reference for grounds A-D only. Because the examiner did not consider Petrovic, the examiner did not consider grounds A-D, and in particular, the extent to which Petrovic’s signals 158a and 158b are functionally identical to the inputs of the Eidson demodulator/decoder 40, nor how that functional equivalency would have motivated combination of Petrovic and

Eidson. *See* Section VI.A.1.f. But even assuming, *arguendo*, that the examiner considered Petrovic, the examiner clearly erred not considering that motivation, particularly in light of the other structural and functional similarities between Petrovic and the '275 patent claims described herein.

#### **D. Level of Ordinary Skill**

A person of ordinary skill in the art (a “POSITA”) at the time of the alleged invention would have had a degree in electrical engineering, or a similar discipline, along with three-to-four years of experience with digital signal processing (DSP) and RF tuning systems for satellite and/or cable communications. Ex. 1102, ¶¶ 30-32. Additional education may substitute for professional experience, and significant work experience may substitute for formal education. *Id.*

#### **E. Claim Construction**

All claim terms herein should be given their ordinary and customary meaning to a POSITA as they would be given in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b). No claim constructions should be necessary and there are no means-plus-function terms. The following constructions are only provided in case some terms are considered means-plus-function terms under pre-AIA 35 U.S.C. §112, paragraph 6.

##### **1. “radio front end”**

To the extent “radio front end” of claim 11 is construed to be a means-plus-function term with the function of “process[ing] the input signal” and to the extent

the '275 patent discloses corresponding structure for this limitation, that structure is the radio front end 210 or radio front end 410 illustrated in Figures 2 and 4, respectively. Ex. 1101, 4:43-5:47, 7:31-46, Figs. 2, 4; Ex. 1102, ¶¶ 33-34.

## **2. “digital frontend (DFE)”**

To the extent “digital frontend (DFE)” of claims 11-13 is construed to be a means-plus-function term with the functions of “select[ing] the plurality of desired channels from the digitized signal and output[ting] the selected plurality of desired channels to at least one demodulator as a digital datastream,” (limitations [11E]-[11F]), “output[ting] the digital datastream via a serial interface” (claim 12), and “output[ting] the digital datastream via a parallel interface” (claim 13) and to the extent the '275 patent discloses corresponding structure for this limitation, that structure is the digital front end 230 of Figure 2 (including mixers 250 and filters 260 but not requiring decimators 270). Ex. 1101, 5:56-7:20, Figs. 2-3; Ex. 1102, ¶ 35.

## **VI. SPECIFIC GROUNDS FOR UNPATENTABILITY**

### **A. Petrovic-Eidson (Claims 1, 4, 7-9, 11, 14, 17-19)**

Claims 1, 4, 7-9, 11, 14, and 17-19 are obvious over Petrovic in view of Eidson. Ex. 1102, ¶¶ 100-158, *see also* ¶¶ 48-77.

## 1. Independent Claim 1

### a. [1A] “A method for operating a television receiver, comprising:”

Petrovic discloses non-limiting preamble [1A].<sup>5</sup> Ex. 1102, ¶¶ 102-104. Petrovic describes a method of operating a channel stacking system 100. Ex. 1108, Title, [0008], [0028]-[0096]; Ex. 1109, Title, [0008]-[0069]; Ex. 1102, ¶ 103. That system—including the APD stage 107<sub>1</sub>, ADC 108<sub>1</sub>, and DSSP 150 discussed below—receives satellite signals 102 and is a “receiver.” Ex. 1108, [0028]-[0029]; Ex. 1109, [0010]-[0013]; Ex. 1102, ¶ 103. As explained in Section VI.A.1.b for limitation [1B], those signals comprise multiple channels.

A POSITA would have understood those channels to include television channels. Ex. 1102, ¶ 104. Petrovic discloses outputting signals from system 100 “to a rendering device, such as a set-top box, or other receiver/tuner,” which are devices associated with output of television programming to users. *Id.*; Ex. 1108, [0028], [0054]; Ex. 1109, [0008], [0030]. Because satellite communication was commonly used to transmit television programming to end users, a POSITA would have been motivated to use the Petrovic system 100 in a home satellite reception system for

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<sup>5</sup> The limitations of the claims appear and are labelled in the Claims Listing Appendix.

obtaining and outputting television programming. Ex. 1102, ¶ 104 (citing Ex. 1154, Ex. 1155, Ex. 1156).

Petrovic discloses limitation [1B]. Ex. 1102, ¶¶ 105-111. Petrovic Figure 4 shows an input terminal (**orange**) of system 100. Ex. 1108, [0029], Fig. 4; Ex. 1109, [0010], [0019], Fig. 1; Ex. 1102, ¶ 105.

**Ex. 1108, Fig. 4 (annotated)**

1102, ¶ 106. The '275 patent acknowledges that satellite channels are a type of broadcast channel. *Id.*; Ex. 1101, 12:60-61.

The channels in signal 102 include “a plurality of desired channels” and a “plurality of undesired channels.” Ex. 1108, [0042], [0053], [0055], [0058], Figs. 4, 6; Ex. 1109, [0004]-[0005], [0015], [0025], [0033], [0036], Figs. 1, 3A; Ex. 1102, ¶ 107. As explained in Section VI.A.1.e for limitation [1E], Petrovic discloses extracting, or selecting, less than all of the channels included in a received RF signal. Ex. 1108, [0042], [0053], [0055], [0058], Fig. 4; Ex. 1109, [0004]-[0005], [0015], [0025], [0033], [0036], Fig. 1; Ex. 1102, ¶ 107. Consistent with the '275 patent, a selected Petrovic channel is desired and an unselected Petrovic channel is undesired. Ex. 1101, Abstract, 1:46-51, 3:29-60, 4:43-58, 5:66-6:3, 6:8-20, 6:59-7:2, 7:16-25; Ex. 1102, ¶ 107.

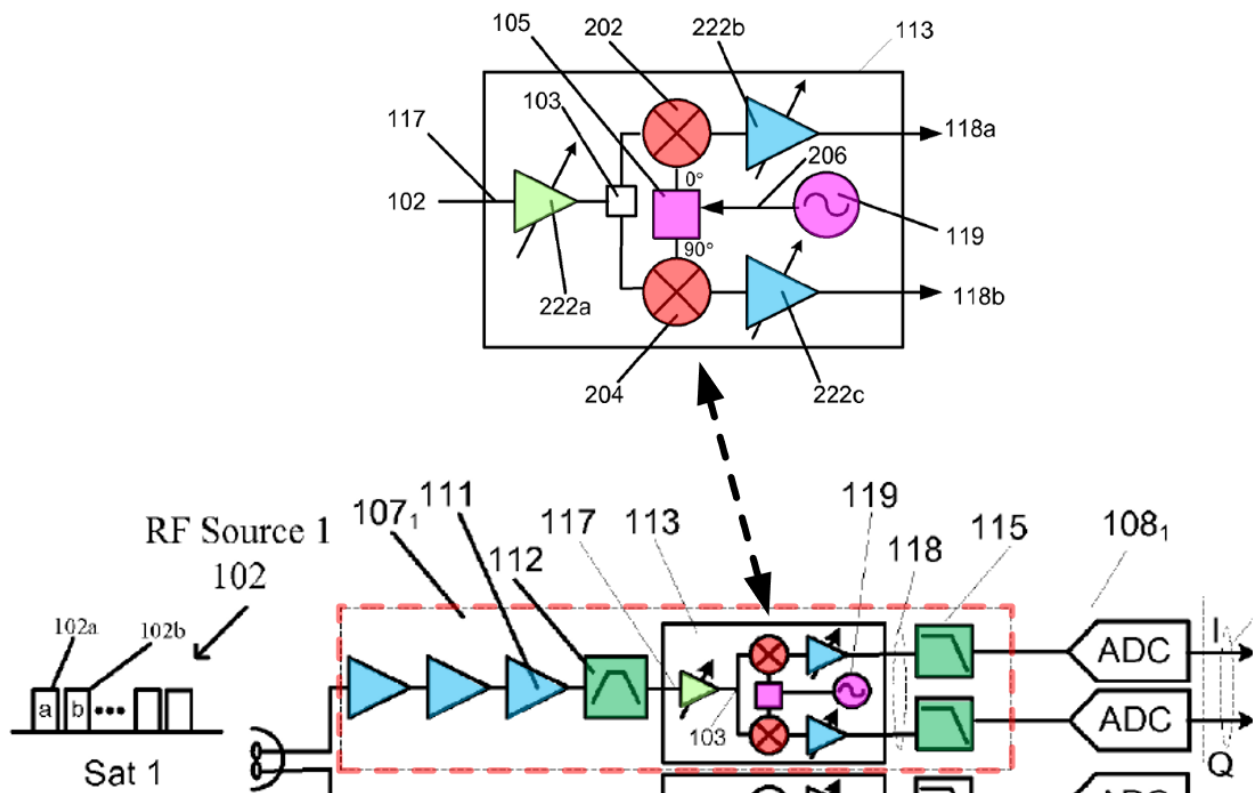
A POSITA would have understood that the Petrovic system would be operated to receive noncontiguous desired channels. Ex. 1102, ¶ 108. The Petrovic system 100 “‘stack[s]’ or assemble[s] channels resident within an RF signal into a composite signal in which the received channels are placed (or sequenced) in desired channel slots for output to a rendering device, such as a set-top box, or other receiver/tuner.” Ex. 1108, [0028]; Ex. 1109, [0008]. The number of available slots in that composite signal may be much less than the total number of channels received by the system 100. Ex. 1108, [0029] (signal 102 may have 120 or more channels), [0055] (output

signal 158 may have as few as four channel slots); Ex. 1109, [0016], [0033]. A POSITA would thus have understood from Petrovic that, in order for the system 100 to stack four channels selected from 120 channels in an input signal, the system 100 would have been configured to select at least two channels that are not contiguous in the received RF signal. Ex. 1102, ¶ 108. As a POSITA would have understood, users of a satellite system such as in Petrovic would select channels according to their individual desires to watch content carried via those channels, and without regard to underlying frequencies used to carry the content channels in the signal 102. Ex. 1112, 1:40-45; Ex. 1102, ¶ 109. Thus, a POSITA would have expected subscriber selection of content from non-contiguous RF channels. Ex. 1102, ¶ 109. The '275 patent recognizes that it was known that, inevitably, users would select (i.e., “desire”) channels that are non-contiguous in a received RF bandwidth. *Id.*; Ex. 1101, 1:44-48, 1:55-58, 2:16-18.

Moreover, a POSITA would have understood that the Petrovic system 100 would be operated so as to select at least 3 channels from a signal 102. Ex. 1108, [0055]; Ex. 1109, [0033]; Ex. 1102, ¶ 110. When at least 3 channels from a signal 102 were selected, at least 2 of those channels (a “plurality”) would be separated by a third of those channels, with those 2 channels thus “non-contiguous” to each other. Ex. 1102, ¶ 110.

- c. [1C] “processing, by a radio front end coupled to the input terminal, the input signal to generate a processed input signal;”

Petrovic discloses limitation [1C]. Ex. 1102, ¶¶ 112-114. The Petrovic system 100 comprises a “radio front end” (red broken line), which Petrovic calls an analog preprocessing and downconversion (APD) stage 107<sub>1</sub>, coupled to the input terminal and that generates a processed input signal. Ex. 1108, [0032]-[0039], Figs. 4-5; Ex. 1109, [0010], [0017], [0031], Figs. 1-2; Ex. 1102, ¶ 112.



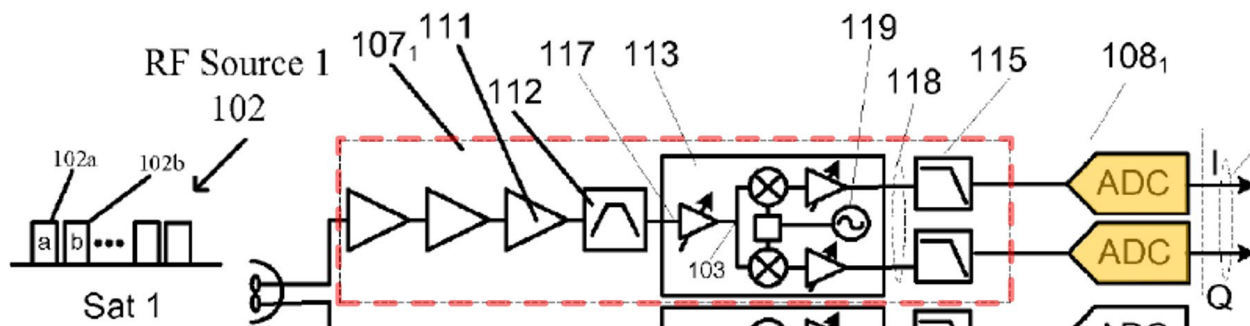
Ex. 1108, Fig. 5 (excerpted and annotated) (top)  
Ex. 1108, Fig. 4 (excerpted and annotated) (bottom)

APD stage 107<sub>1</sub> performs processing that includes amplifying by amplifiers 111 (light blue), filtering by filter 112 (green), amplifying by amplifier 222a (light

green), mixing by mixers 202 and 204 (red) using 90° phase-shifted oscillator signals from a synthesizer/frequency source 119 (pink) and a phase shifter 105 (pink), amplifying by amplifiers 222b and 222c (light blue), and filtering by low pass filters 115 (green). Ex. 1108, [0032]-[0039], Figs. 4-5; Ex. 1109, [0010], [0017], [0031], Figs. 1-2; Ex. 1102, ¶ 113. APD stage 107<sub>1</sub> performs the same type of processing performed by the radio front end 210 of the '275 patent, and generates the same type of processed input signal—downconverted and filtered in-phase and quadrature components of an input signal. Ex. 1101, 4:40-5:25, Fig. 2; Ex. 1108, [0032]-[0039], Figs. 4-5; Ex. 1109, [0010], [0017], [0031], Figs. 1-2; Ex. 1102, ¶¶ 113-114.

**d. [1D] “digitizing, by an analog-to-digital converter (ADC) coupled to the radio front end, the processed input signal to generate a digitized signal;”**

Petrovic discloses limitation [1D]. Ex. 1102, ¶¶ 115-117. An ADC pair 108<sub>1</sub> (gold) is coupled to the APD stage 107<sub>1</sub> (red broken line). Ex. 1108, [0039], Fig. 4; Ex. 1109, [0005], [0010], [0022], Fig. 1; Ex. 1102, ¶ 115.



**Ex. 1108, Fig. 4 (excerpted and annotated)**

The ADC pair 108<sub>1</sub> digitizes the processed input signal, output from the APD stage 107<sub>1</sub>, to generate a digitized signal. Ex. 1108, [0039], [0051]-[0052], Fig. 4; Ex. 1109, [0005], [0010], [0018], [0019], [0022], Fig. 1; Ex. 1102, ¶¶ 116-117.

- e. [1E] “selecting, by a digital frontend (DFE) coupled to the ADC, the plurality of desired channels from the digitized signal; and”

Petrovic discloses limitation [1E]. Ex. 1102, ¶¶ 118-123. The Petrovic DSSP 150 (blue) is a DFE that selects desired channels from the digitized signals received from the ADC pair 108<sub>1</sub>. Ex. 1108, [0042], [0053], [0058]-[0077], Figs. 4, 6; Ex. 1109, [0004] (“[t]he present invention provides for a channel stacking system ... which processes channel selection ... within the digital domain”), [0005], [0015], [0025], [0033], [0037]-[0054], Fig. 1; Ex. 1102, ¶ 118.

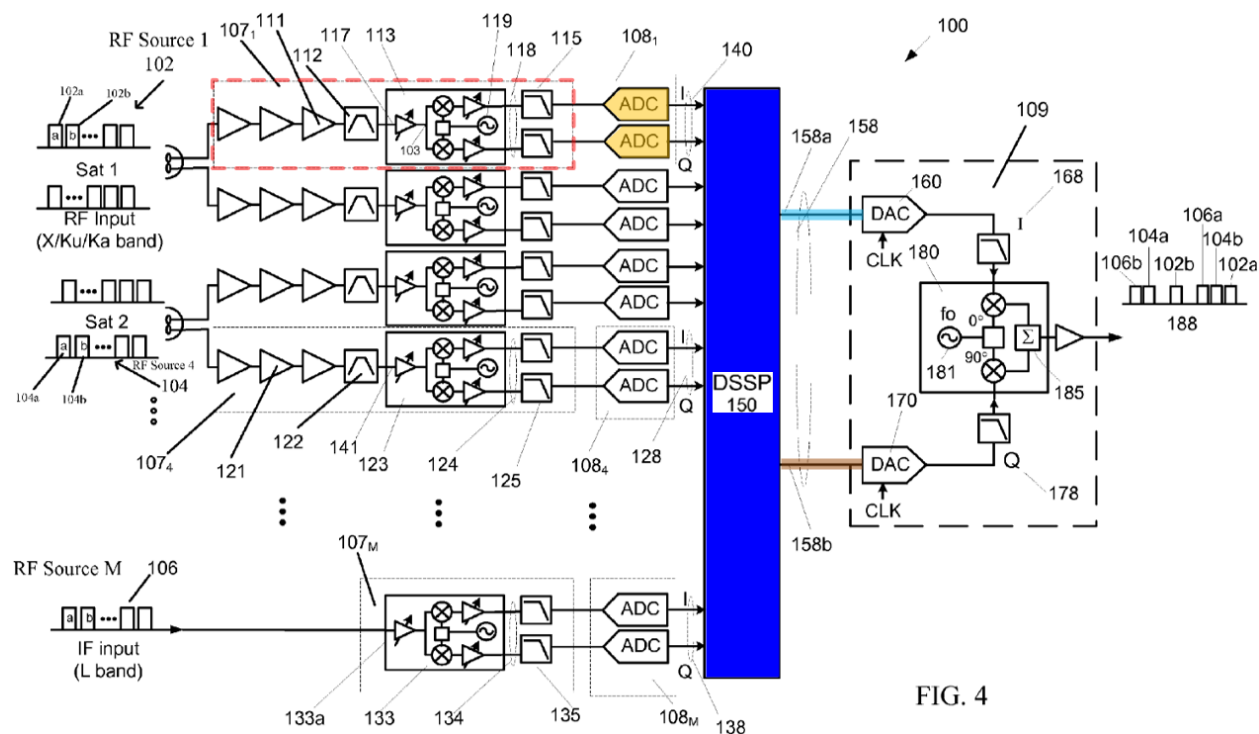
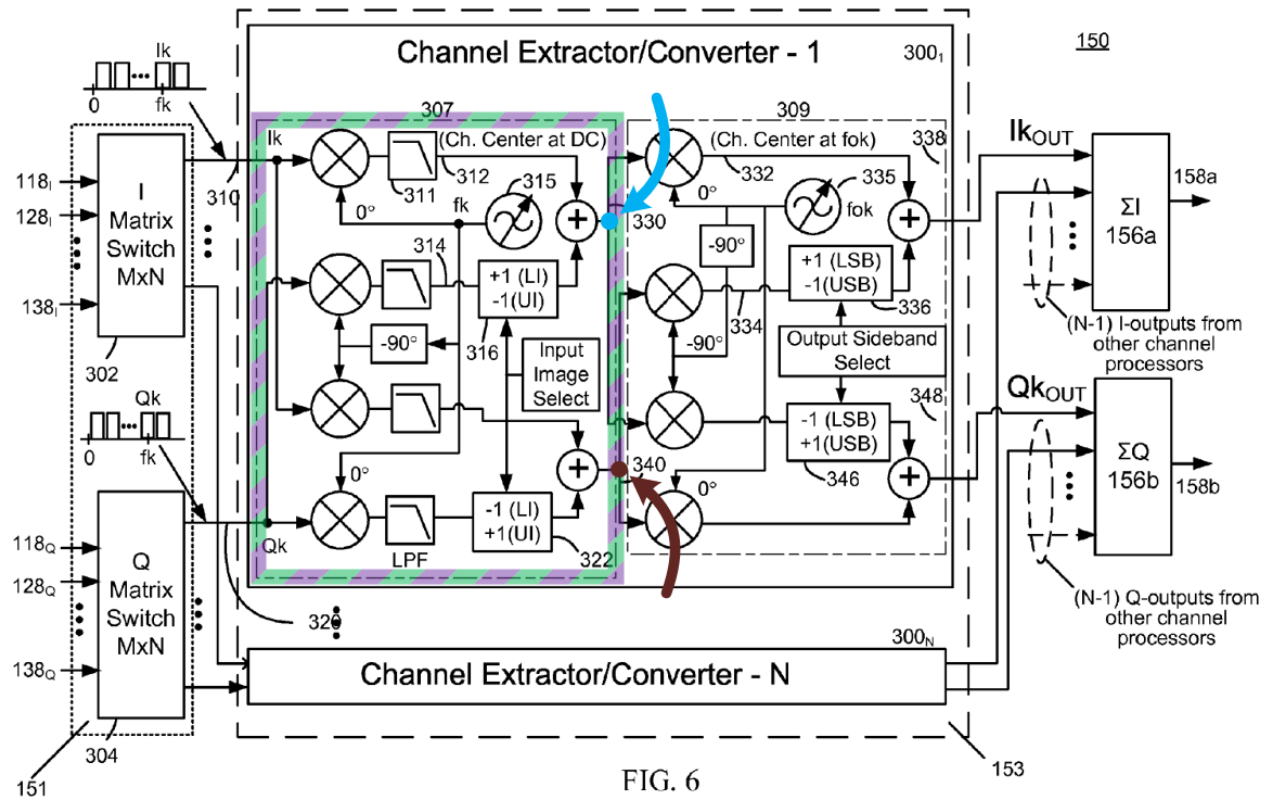


FIG. 4

Ex. 1108, Fig. 4 (annotated)

As explained in Section VI.A.1.d for limitation [1D], and as shown in Figure 4, the ADC pair 108<sub>1</sub> digitizes I,Q components of a signal that include channels (desired and undesired) from a received RF input signal 102. Ex. 1102, ¶ 119. Petrovic Figure 6 shows details of the DSSP 150. *Id.*; Ex. 1108, [0016], [0055]; Ex. 1109, [0007], [0033].



**Ex. 1108, Fig. 6 (annotated)**

The DSSP 150 includes circuits 300 (Channel Extractor/Converter-1 (300<sub>1</sub>) through Channel Extractor/Converter-N (300<sub>N</sub>)), with each circuit 300 comprising a stage 307 (purple/green), and with each of those stages 307 able to select a different channel. Ex. 1108, [0055], [0059]-[0077], Fig. 6; Ex. 1109, [0033], [0037]-[0054], Fig. 3A; Ex. 1102, ¶ 120. The stages 307 “extract [i.e., select] the channels of interest

[i.e., desired channels]” from signals received from the ADC pair 108<sub>1</sub> and “remove all of the channels that are not of interest,” i.e., the claimed “undesired channels.” Ex. 1108, [0042], [0053], [0055], [0058], Figs. 4, 6; Ex. 1109, [0003], [0004] (“[t]he present invention provides for a channel stacking system ... which processes channel selection ... within the digital domain”), [0005], [0015], [0025] (digital signal processor 150 “assemble[s] a composite signal 158 having the desired channels”), [0033] (channel extractor/converter circuits of digital signal processor 150 “extract a desired channel”), [0036], Fig. 1; Ex. 1102, ¶ 120. Stage 307 extracts a desired channel from the digitized I, Q components, corresponding to the RF source 102, received from ADC pair 108<sub>1</sub> and outputs an I component 330 (light blue dot and arrow) and a Q component 340 (brown dot and arrow) corresponding to a selected/desired channel. Ex. 1108, [0051], [0053], [0060]-[0077], Figs. 4, 6; Ex. 1109, [0018]-[0019], [0022], [0025], [0037]-[0054], Figs. 1, 3A; Ex. 1102, ¶ 120.

Petrovic describes the same selection technique described by the '275 patent. *Compare* Ex. 1101, 6:21-7:15 (describing a frequency shift to baseband and filtering of the baseband signal), Fig. 3 *with* Ex. 1108, [0042] (desired channels digitally translated to baseband and “[t]he translated channels are then digitally lowpass filtered ..., leaving only the channel of interest”), [0058]-[0077], Fig. 6, *and* Ex. 1109, [0025] (“channel extraction ... is performed by direct digital conversion to zero IF, followed by channel filters”), [0036]-[0054], Fig. 3A; Ex. 1102, ¶ 121.

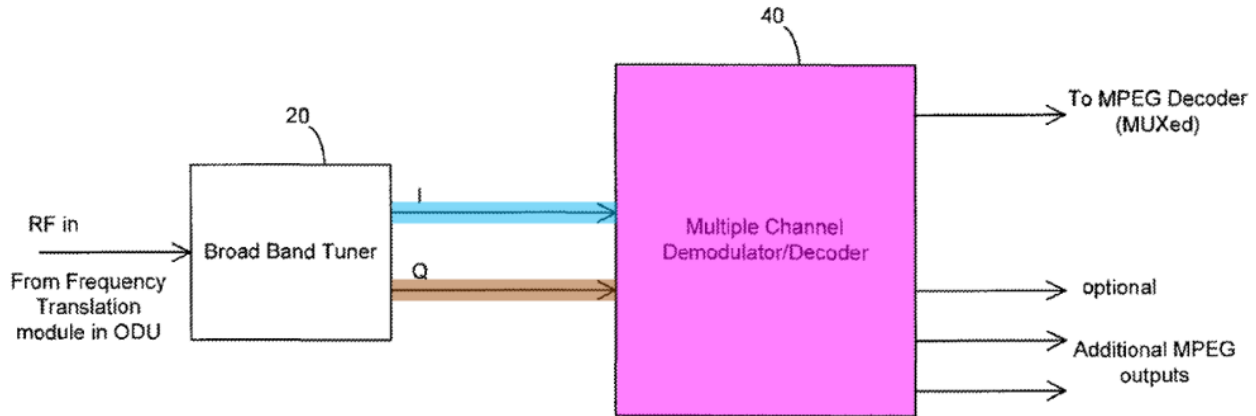
The DSSP 150 upconverts the baseband I, Q components of selected channels output by the stages 307 in corresponding stages 309, sums the upconverted I, Q components to create a combined signal 158 having digital I component 158a (**light blue**) and digital Q component 158b (**brown**), and outputs those summed components. Ex. 1108, [0018]-[0024], [0043], [0053], [0078]-[0096], [0098]-[0122], Figs. 4, 6, 9-15; Ex. 1109, [0005], [0007], [0015], [0025], [0055]-[0069], [0071]-[0095], Figs. 1, 3A, 5-11; Ex. 1102, ¶ 122. The components 158a, 158b are a digital datastream containing selected channels. Ex. 1108, [0009], [0043], [0046] (referring to “digital composite signal 158”), [0054], [0055] (circuits of the DSSP 150 “extract a desired channel and locate or place the channel in the desired channel slot of the output signal 158”), Figs. 4, 6; Ex. 1109, [0005], [0015], [0025], [0030], [0033], Figs. 1, 3A; Ex. 1102, ¶¶ 122-123.

- f. [1F] “outputting, by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator extracts information encoded in the digital datastream.”

Petrovic-Eidson discloses limitation [1F]. Ex. 1102, ¶¶ 124-135. As explained below, a POSITA would have output the Petrovic components 158a and 158b to a demodulator as taught by Eidson. Ex. 1102, ¶ 124.

Eidson’s Figure 8 discloses “a broadband tuner and multi-channel demodulator and decoder [**pink**]” that can be used as a multiple channel receiver of

a set top box. Ex. 1112, 7:58-59, 1:48-50, 2:8-10, 2:25-33, 2:42-51, 5:59-60, 8:27-9:2; Ex. 1102, ¶ 125.



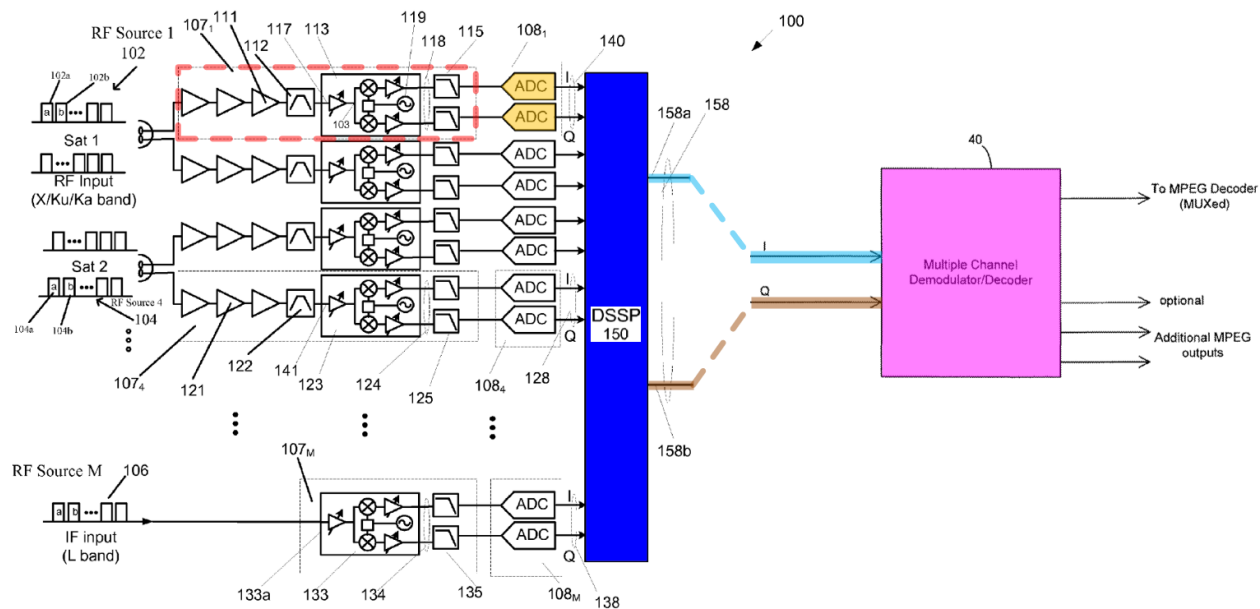
**Ex. 1112, Fig. 8 (annotated)**

The multiple channel demodulator and decoder (“demodulator/decoder”) 40 receives digital I (light blue) and Q (brown) signals from a front end that comprises a broadband tuner 20 and a frequency translation module (FTM) of a satellite outdoor unit (ODU). Ex. 1112, 8:29-9:2, Fig. 8; Ex. 1102, ¶ 126. The FTM selects multiple channels, translates those selected channels to contiguous portions of a bandwidth, and sends an RF signal with those translated channels to the tuner 20. Ex. 1112, 8:30-48, 9:5-25, Figs. 8-10; Ex. 1102, ¶ 126. The tuner 20 (like the RFE and DFE of Petrovic) downconverts the received RF signal, generates I and Q components of that downconverted signal, and digitizes those I and Q components to create digital I, Q components. Ex. 1112, 8:43-48, 9:5-25, Figs. 8-10; Ex. 1102, ¶ 126. Those digital I, Q components are output to the demodulator/decoder 40, which demodulates multiple channels in those components. Ex. 1112, 8:65-9:2,

11:44-12:28, Figs. 8, 15-16; Ex. 1102, ¶ 126. Thus, Eidson teaches a demodulator to which “a selected plurality of television channels” is being output “as a digital datastream.” Ex. 1102, ¶ 126. Eidson further teaches “wherein the demodulator extracts information encoded in the digital datastream.” Ex. 1112, 8:65-9:2; Ex. 1115, p. 7 (demodulation is “reconversion of a modulated signal back into its original form by extracting the data from the modulated carrier”); Ex. 1102, ¶ 127.

The I, Q components received by the Eidson demodulator/decoder 40 from the front end (e.g., the FTM and the tuner 20) are functionally equivalent to the Petrovic I, Q components 158a, 158b, as both sets of I, Q components comprise multiple channels that have been placed into sequential slots of a bandwidth. Ex. 1102, ¶¶ 128-129. The I, Q components received by the Eidson demodulator/decoder 40 are I, Q, components of a digital signal for multiple channels that have been selected and placed into contiguous portions of a bandwidth. Ex. 1112, 8:43-9:25, Figs. 8-10; Ex. 1102, ¶ 129. Similarly, the Petrovic I, Q components 158a, 158b are digital components of a signal for multiple channels that have been selected and has been placed into sequential portions of a bandwidth. Ex. 1108, Title, [0002], [0008], [0028], [0041]-[0044], [0046], [0053]-[0055], [0059]-[0091], [0097], Figs. 3, 4, 6, 8; Ex. 1109, Title, [0001], [0004], [0008], [0015], [0025], [0030], [0033]-[0064], [0070], Figs. 1, 3A, 4; Ex. 1102, ¶ 129.

A POSITA would have appreciated that the I and Q components output from Petrovic's DSSP would be readily sent to a demodulator for a STB, such as taught in Eidson. Ex. 1102, ¶ 130. This would have been done in place of Petrovic's stage 109, or in addition to it. Eidson teaches that its demodulator/decoder 40 operates by receiving I, Q components that are functionally equivalent to the I, Q components 158a, 158b output by the Petrovic DSSP 150. Ex. 1102, ¶ 130. A POSITA would have been motivated to combine a Petrovic tuner and the Eidson demodulator/decoder 40 so that the multiple selected channels output by the Petrovic DSSP (as I, Q components 158a, 158b) would be demodulated in the digital domain. Ex. 1102, ¶ 130. Eidson further offers digital demodulation with a single demodulator, which would have been more efficient than using multiple simultaneous demodulators for separate channels. Ex. 1112, 4:2-6, 6:36-38; Ex. 1102, ¶ 130. The following annotated Figure, prepared with excerpts from Petrovic Figure 4 and Eidson Figure 8, shows the Petrovic-Eidson system in which the Petrovic I, Q components 158a, 158b are the I, Q component inputs to the Eidson demodulator/decoder 40. Ex. 1102, ¶ 130.



### Petrovic-Eidson

Combining a Petrovic tuner with an Eidson demodulator/decoder 40 would also allow incorporation of tuning/channel selection and demodulating/decoding functionality into a single device, a configuration known in the art and having the added benefits of digital tuning (Petrovic) and multichannel demodulation (Eidson). Ex. 1108, [0007], [0094]; Ex. 1109, [0003], [0069]; Ex. 1112, 3:35-45, 4:2-6, 6:36-38; Ex. 1102, ¶ 131 (citing Ex. 1140, which describes a satellite STB able to receive multiple satellite signals, tune channels of received satellite signals, and demodulate those channels). For example, the Eidson demodulator/decoder 40 would have been added to the Petrovic tuner in a set top box intended to function as a “Media Center” STB,” that would feed other set top boxes. Ex. 1112, 2:28-31; Ex. 1102, ¶ 132. In such a set top box, the I, Q components 158a, 158b would have been simultaneously output to the demodulator/decoder 40 (e.g., for demodulation/decoding for output to

display or recording devices) and to the Petrovic DAC and Complex to Real Conversion stage 109 for generation of a signal 188 to transmit to other set top boxes or devices. Ex. 1102, ¶ 132. Alternatively, the stage 109 would have been omitted to save cost if “Media Center’ STB” functionality was not needed, thereby allowing a further simplified design. *Id.*

Although Petrovic indicates that its channel stacking system “may be implemented as an outdoor unit (ODU) as part of a satellite receiving system,” Petrovic does not limit its channel stacking system or its tuner (e.g., the Petrovic APD stage(s), the Petrovic ADC pair(s), and the Petrovic DSSP) to ODU use. Ex. 1108, [0054]; Ex. 1109, [0030]; Ex. 1102, ¶ 132. A POSITA would have been aware of other uses, as tuners were ubiquitous at the time, and in any event, Eidson teaches additional uses for the Petrovic tuner, and indeed, for the entire Petrovic channel stacking system. Ex. 1102, ¶ 132.

Combining a Petrovic tuner and the Eidson demodulator/decoder would have been a combination of known prior art elements (Petrovic’s APD stage 107<sub>1</sub>, ADCs 108<sub>1</sub>, and DSSP and Eidson’s demodulator/decoder) according to known methods (sending I and Q components to the demodulator/decoder, as taught in Eidson) to yield predictable results (the components are demodulated and decoded). Ex. 1102, ¶ 133. As explained above, and as a POSITA would have recognized, the output of a Petrovic tuner is the functional equivalent of the input to the Eidson

demodulator/decoder. *Id.* A POSITA would thus have combined a Petrovic tuner and the Eidson demodulator/decoder, as each would perform the same function in the combination that would be performed individually prior to the combination. *Id.* For the same reasons, the results of combining the Petrovic tuner with the Eidson demodulator/decoder would also have been predictable. *Id.* Neither the function of the Petrovic tuner, nor the function of the Eidson demodulator/decoder, would change appreciably if combined, and thus each element could operate as it did before, leading to an expectation of success. *Id.*

Although the above analysis explains why a POSITA would have added the Eidson demodulator/decoder to the Petrovic tuner, a POSITA would have been just as motivated to add the Petrovic tuner to the Eidson demodulator/decoder. *Id.*, ¶ 134. Petrovic, by virtue of the functional equivalence of the I, Q components output by the Petrovic DSSP to the I, Q components received by the Eidson demodulator/decoder 40, and by virtue of the equivalent selection and stacking functions performed by the Petrovic tuner and by the Eidson front end, teaches that the Petrovic tuner could be readily substituted for the Eidson front end. *Id.* The advantages of and motivation for that combination would be the same as those described above for modification of Petrovic based on Eidson. *Id.* And the combination would similarly have been a combination of known prior art elements

according to known methods to yield predictable results with an expectation of success. *Id.*

In Petrovic-Eidson, the Petrovic DSSP 150 is the “digital front end” of limitations [1E] and [1F]. *Id.*, ¶ 135. The Petrovic DSSP 150 in Petrovic-Eidson selects the plurality of desired channels from the digitized signal (i.e., selects channels from the signal received by the DSSP) and outputs the selected plurality of channels as a digital datastream (the components 158a, 158b) to a demodulator (the Eidson demodulator/decoder 40) that extracts information encoded in the digital datastream. Ex. 1112, 8:65-9:2; Ex. 1102, ¶¶ 127 (citing Ex. 1115), 135.

## 2. Independent Claim 11

**[11A] “A television receiver device, comprising:”**

**[11B] “an input terminal operable to receive an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels, wherein the plurality of desired channels are non-contiguous;”**

**[11C] “a radio front end, coupled to the input terminal, operable to process the input signal;”**

**[11D] “an analog-to-digital converter (ADC), coupled to the radio front end, operable to digitize the processed input signal to generate a digitized signal; and”**

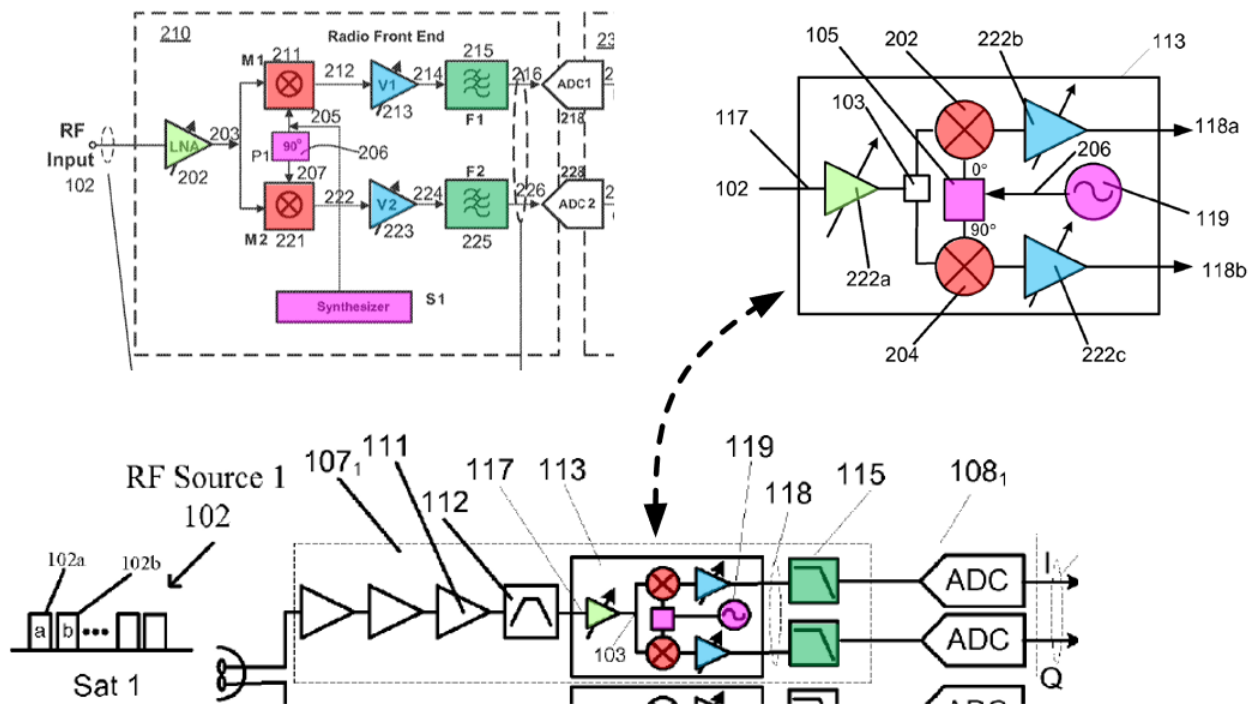
**[11E] “a digital frontend (DFE), coupled to the ADC, operable to select the plurality of desired channels from the digitized signal and”**

**[11F] “output the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator is operable to extract information encoded in the digital datastream.”**

Claim 11 recites a television receiver device with the same components and functions recited in method claim 1. Thus, Petrovic-Eidson renders limitations [11A]-[11F] obvious for the same reasons discussed above for [1A]-[1F], respectively. Section VI.A.1; Ex. 1102, ¶ 136. The APD stage 107<sub>1</sub>, ADC pair 108<sub>1</sub>, and DSSP 150 of Petrovic’s system 100 are the claimed “television receiver device” having the claimed “input terminal.” Section VI.A.1.a-b; Ex. 1102, ¶¶ 137-140. Petrovic’s APD stage 107<sub>1</sub>, ADC pair 108<sub>1</sub>, and DSSP 150 are, respectively, the radio front end of limitation [11C], the ADC of limitation [11D], and the DFE of

limitations [11E] and [11F]. Sections VI.A.1.c-f; Ex. 1102, ¶¶ 139-153. The Eidson demodulator/decoder 40 is the demodulator of limitation [11F]. Section VI.A.1.f; Ex. 1102, ¶¶ 154-155.

“Radio front end” is not a means+function limitation. But even if it were, it is taught by Petrovic-Eidson. Ex. 1102, ¶¶ 143-144. The below Figure compares the structure of the radio front end, from '275 patent Figure 2 (left), to the structure of the Petrovic APD stage 107<sub>1</sub> (bottom and right).



**Ex. 1101, Fig. 2 (excerpted and annotated) (top left)**

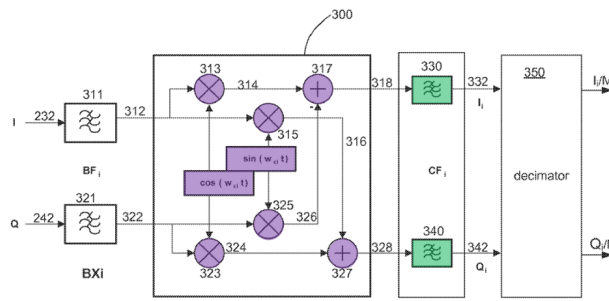
**Ex. 1108, Fig. 5 (excerpted and annotated) (top right)**

**Ex. 1108, Fig. 4 (excerpted and annotated) (bottom)**

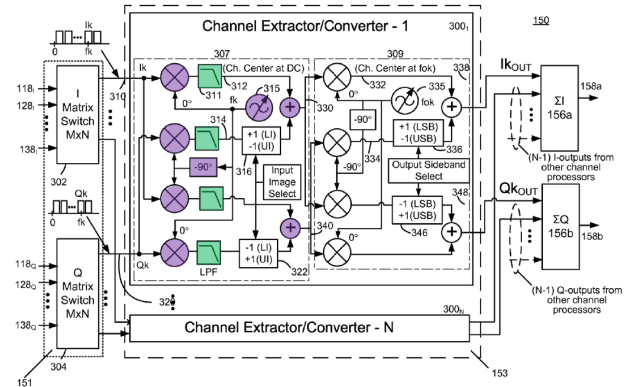
The amplifier 222a (light green), mixer pair 202, 204 (red), frequency source 119 (pink), phase shifter 105 (pink), amplifiers 222b, 222c (light blue), and low pass filters 115 (green) of the Petrovic APD stage 107<sub>1</sub> are structure that is the same

as, or equivalent to, the amplifier 202 (light green), mixers 211, 221 (red), synthesizer S1 (pink), phase shifter 206 (pink), amplifiers 213, 223 (light blue), and low pass filters 215, 225 (green) of the '275 patent radio front end 210. Ex. 1102, ¶ 144. Any differences are insubstantial. Ex. 1102, ¶ 144. Both perform the same function of processing an input signal by creating amplified, downconverted, and filtered I, Q components of a received RF signal. Ex. 1101, 4:40-5:37, Fig. 2; 1108, [0032]-[0039], Figs. 4-5; Ex. 1109, [0010], [0017], [0031], Figs. 1-2; Ex. 1102, ¶ 144. To the extent that Patent Owner contends that the amplifier 111 and filter 112 of the Petrovic APD stage 107<sub>1</sub> affect the equivalence of the Petrovic APD stage 107<sub>1</sub> and '275 patent radio front end 210, the amplifier 111 and filter 112 are optional. Ex. 1108, [0001]; Ex. 1109, [0017]; Ex. 1102, ¶ 144.

“DFE” is not a means+function limitation. But even if it were, it is taught by Petrovic-Eidson. Ex. 1102, ¶¶ 149-153. As seen by the below comparison of Figure 6 of Petrovic and Figure 3 of the '275 patent, the Petrovic DSSP 150 includes structure that is the same as, or equivalent to, structure of the complex mixers 250 and 300 and filters 260, 330, and 340 of the '275 patent. *Id.*, ¶ 149.



**Ex. 1101, Fig. 3 (annotated)**



**Ex. 1108, Fig. 6 (annotated)**

Like complex mixer 300 of the '275 patent (**purple**), which is one of N complex mixers 250, the Petrovic DSSP 150 comprises N stages 307, each of which comprises a complex mixer (**purple**). Ex. 1101, 6:32-7:2; Ex. 1108, [0066]-[0068], Fig. 6; Ex. 1109, [0045]-[0047], Fig. 3A; Ex. 1102, ¶ 150 (citing as background Ex. 1118 and Ex. 1134). Like the filters 330 and 340 of the '275 patent (**green**), which are one of N filter modules 260, each stage 307 of the Petrovic DSSP 150 also comprises low pass filters (LPF) 311 (**green**). Ex. 1101, 7:3-8; Ex. 1108, [0066]-[0069]; Ex. 1109 [0045]-[0048]; Ex. 1102, ¶ 150. Any differences between the '275 patent structure (N mixers 300 and N filters 330 and 340) and the Petrovic N stages 307 are insubstantial. Ex. 1102, ¶¶ 151-153. Both perform the same function of selecting and outputting desired channels, in the same way by downconverting the desired channel to baseband and low pass filtering to isolate the desired channels, and outputting the result to a demodulator, to achieve the same result of selecting a plurality of desired channels from a digitized signal and outputting those channels

to a demodulator. *Id.*; Ex. 1101, 6:8-7:8; Ex. 1108, [0060]-[0070]; Ex. 1109, [0037]-[0054].

### 3. Claims 4, 14

**[4]/[14] “The [method of claim 1]/[television receiver device of claim 11], wherein the ADC comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.”**

Petrovic-Eidson discloses claims 4 and 14. Ex. 1102, ¶ 156. Petrovic’s ADC pair 108<sub>1</sub> comprises first and second ADCs that respectively generate digital in-phase and quadrature signals. *Id.*; Ex. 1108, [0052], Fig. 4; Ex. 1109, [0022], Fig. 1.

### 4. Claims 7-8, 17-18

**[7]/[17] “The [method of claim 1]/[television receiver device of claim 11], wherein the plurality of desired channels comprises at least one television channel.”**

**[8]/[18] “The [method of claim 1]/[television receiver device of claim 11], wherein the plurality of undesired channels comprises at least one television channel.”**

Petrovic-Eidson discloses claims 7-8 and 17-18. Ex. 1102, ¶ 157. As explained in connection with preamble [1A], a POSITA would have understood the channels of signals 102 to include television channels. *Id.*; Section VI.A.1.a.

## 5. Claims 9, 19

**[9]/[19] “The [method of claim 1]/[television receiver device of claim 11], wherein the broadcast channels comprise satellite broadcast channels.”**

Petrovic-Eidson discloses claims [9] and [19]. Ex. 1102, ¶ 158. Petrovic’s system 100 receives satellite signals 102 that have multiple channels. *Id.*; Section VI.A.1.b.

### B. Petrovic-Eidson-Rabaey (Claims 2-3, 12-13)

**[2]/[12] “The [method of claim 1, wherein the DFE outputs]/[television receiver device of claim 11, wherein the DFE is operable to output] the digital datastream via a serial interface.”**

**[3]/[13] “The [method of claim 1, wherein the DFE outputs]/[television receiver device of claim 11, wherein the DFE is operable to output] the digital datastream via a parallel interface.”**

Claims 2/12 and 3/13 differ only with regard to the type of interface via which the digital datastream of limitations [1F]/[11F] is output. Ex. 1101, 12:42-45, 13:14-19. Claims 2/12 recite “a serial interface,” while claims 3/13 recite “a parallel interface.” *Id.* But as explained below, either option would have been an obvious design choice, and claims 2-3 and 12-13 are obvious over Petrovic-Eidson in view of Rabaey. Ex. 1102, ¶¶ 159-167.

As explained in Sections VI.A.1.e-f, the Petrovic DSSP 150 is a DFE that outputs “the selected plurality of desired channels to at least one demodulator as a digital datastream.” Ex. 1102, ¶ 161. As the ’275 patent concedes, the outputting of

a digital data stream via serial and parallel interfaces were “commonly known methods.” *Id.*; Ex. 1101, 7:16-20. Indeed, dictionaries, basic text books, and technical papers at the time confirm that a POSITA would have understood parallel and serial interfaces as the two common options for outputting data in standard integrated circuits. Ex. 1102, ¶¶ 161-164 (citing Ex. 1114, 9:44-50, 30:31-42, 31:15-22; Ex. 1115, pp. 5, 8, 10; Ex. 1116, pp. 79-80; Ex. 1117, pp. 354-355). Notably, Petrovic discloses the DSSP 150 and other components of the system 100 may be implemented as “hardware” such as “application specific integrated circuits.” Ex. 1108, [0027], [0040], [0124]-[0125]; Ex. 1109, [0009], [0115]; Ex. 1102, ¶ 162. As explained in Section VI.A.1.f, a POSITA would have modified Petrovic so that a Petrovic tuner—which includes a DSSP outputting the digital data stream—would output digital data to the Eidson demodulator/decoder. Ex. 1102, ¶ 162. Eidson indicates that a front end and a multichannel demodulator/decoder could be integrated into a single package, which further indicates digital data would flow from a Petrovic DSSP to an Eidson demodulator/decoder using conventional integrated circuit interfaces. *Id.*; Ex. 1112, 6:33-35.

At the most fundamental level, a digital integrated circuit represents data as binary units (“bits”) in the form of electrical signals on wires (e.g., high and low voltages for binary values “1” and “0” respectively). Ex. 1102, ¶ 163; Ex. 1116, pp. 23-24, 27-29, 48-51. Multiple bits can be sent over multiple separate wires, one wire

for each bit (“parallel interface”), or one bit at a time over a single wire (“serial interface”). Ex. 1102, ¶ 163, *see also* ¶¶ 75-76; Ex. 1115, pp. 5, 8, 10; Ex. 1116, pp. 79-80 (Figure 6-25).

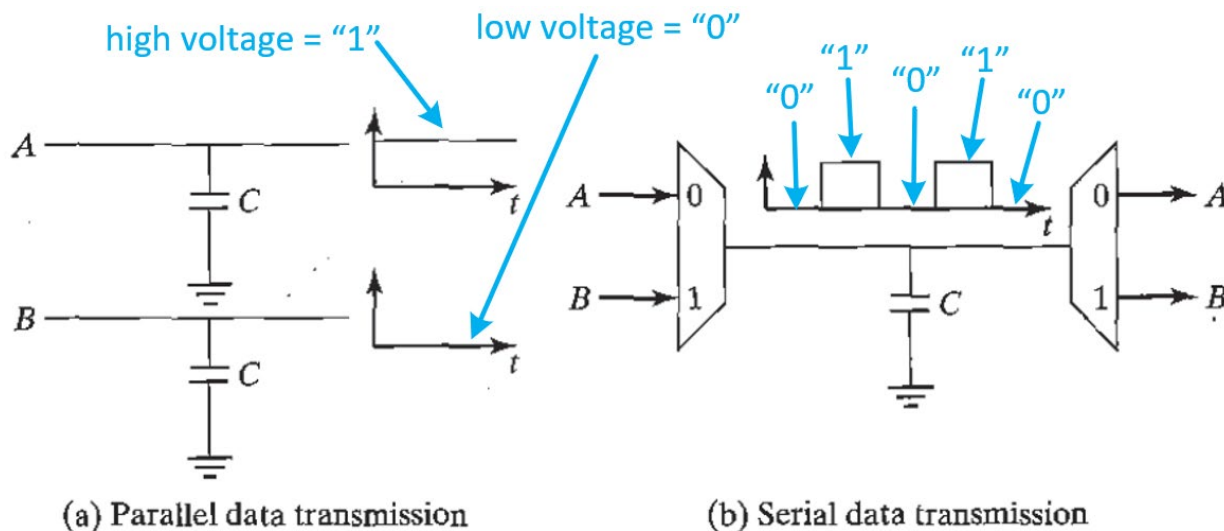


**Figure 6-25** Parallel versus time-multiplexed data busses.

**Ex. 1116, p. 80, Fig. 6-25 (annotated)**

Implementing a data interface between a Petrovic DSSP and an Eidson demodulator/decoder using either option would have been equally obvious as one of two design choices, because both were “commonly known methods” used by POSITAs. Ex. 1102, ¶ 164, *see also* ¶¶ 75-77; Ex. 1114, 30:31-42, 31:15-22; Ex. 1115, pp. 5, 8, 10; Ex. 1116, pp. 79-80; Ex. 1117, pp. 354-355. For the same reasons, implementing serial and parallel interfaces would have been well within the POSITA’s skillset, and thus, a POSITA would have had a high expectation of success leading to a predictable result. Ex. 1102, ¶ 164.

For example, Rabaey, a textbook on implementing digital integrated circuits, teaches that both serial and parallel interfaces as illustrated in the Figure 6-25 above were beneficially used in integrated circuits. Ex. 1116, pp. 79-80; Ex. 1102, ¶ 165. Per Rabaey, time-multiplexing (i.e., a serial interface) “is an often used technique to minimize the implementation area” of a design on a chip, but that this “minimum area solution does not always result in the lowest switching activity,” for example, when the data signals have high “temporal correlation.” Ex. 1116, pp. 79-80, *see also* pp. 72-74; Ex. 1102, ¶ 165. Minimizing circuit area minimizes the cost of the integrated circuit, while minimizing the switching activity minimizes the power consumed by the integrated circuit. Ex. 1116, pp. 29-33, 43-44, 72-74, 76-80; Ex. 1102, ¶ 165. Thus, Rabaey teaches both serial and parallel interfaces for transmitting digital data between two points, each of which has advantages over the other, depending upon area and power constraints and the temporal correlation between the signals. Ex. 1116, pp. 29-33, 43-44, 72-74, 76-80; Ex. 1102, ¶ 165.

It would have been obvious to apply either of Rabaey’s parallel data or serial interfaces as illustrated in Figure 6-25 to the interconnection between Petrovic’s DSSP and Eidson’s demodulator/decoder. Ex. 1102, ¶ 166. Petrovic and Eidson teach implementation in an integrated circuit, and the techniques taught in Rabaey would have enabled such implementation. Ex. 1108, [0027], [0040], [0124]; Ex. 1109, [0009], [0115]; Ex. 1116, pp. 76-80; Ex. 1102, ¶ 166.

As such, the modification of Petrovic and Eidson with Rabaey that results in a serial interface (claims 2/12) between Petrovic's DSSP and Eidson's demodulator/decoder is nothing more than a combination of prior art elements (Petrovic's and Eidson's circuit designs and Rabaey's serial interface interconnects) according to known methods (Rabaey's process for implementing circuit designs, including selecting a serial interface to minimize chip area and cost) to yield predictable results (data is sent serially). Ex. 1102, ¶ 166.

Likewise, the modification of Petrovic and Eidson with Rabaey that results in a parallel interface (claims 3/13) between Petrovic's DSSP and Eidson's demodulator/decoder is also nothing more than a combination of prior art elements (Petrovic's and Eidson's circuit designs and Rabaey's parallel interface interconnects) according to known methods (Rabaey's process for implementing circuit designs, including selecting a parallel interface to minimize switching and power) to yield predictable results (data is sent in parallel). *Id.*

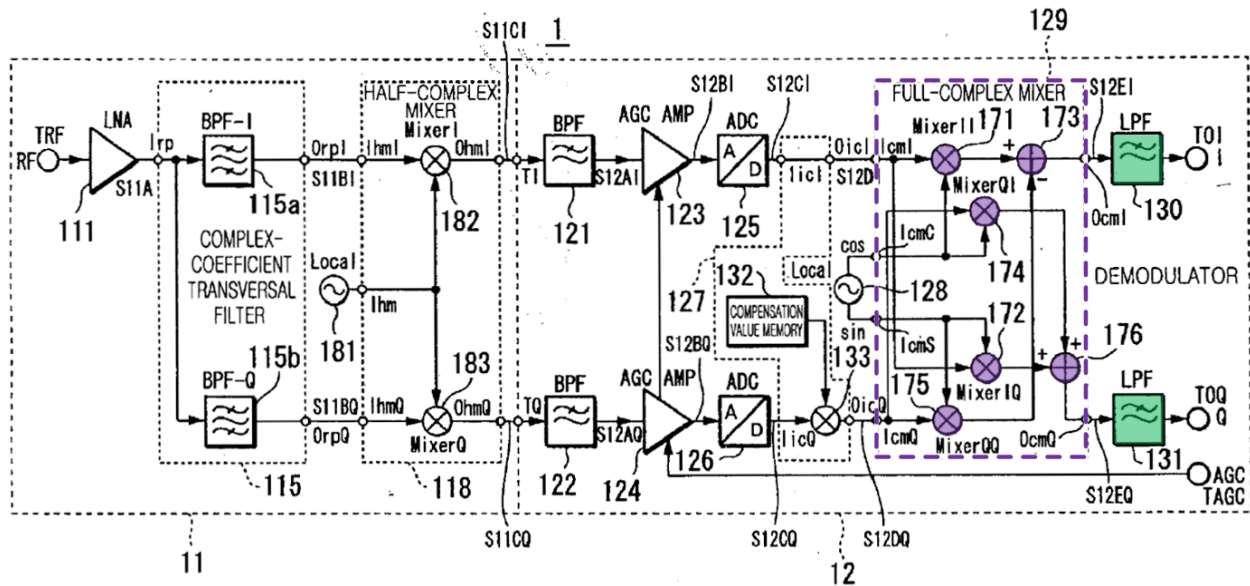
The resultant combinations of Petrovic-Eidson-Rabaey are predictable and a POSITA would have had a reasonable expectation of success, because Rabaey teaches basic techniques used by POSITA to design integrated circuits (admitted by the '275 patent to be commonly known), and because those techniques are specifically directed to overcoming specific issues, such as meeting area and power

constraints, that a POSITA would customarily balance in their designs. Ex. 1116, pp. 29-33, 43-44, 72-74, 76-80; Ex. 1102, ¶ 167.

### **C. Petrovic-Eidson-Takahiko (Claims 11, 14, 17-19)**

To the extent Patent Owner contends that DFE is a means+function limitation, and further contends that the location of LPFs 311 within the complex mixer of Petrovic stage 307, as shown in Figure 6 of Petrovic, is not the same or equivalent structure as the complex mixer 300 and filters 330 and 340 of Figure 3 of the '275 patent (it is), placing four low pass filters before adders (the “ $\oplus$ ” symbols in the side-by-side comparison of Ex. 1101 Figure 3 and Ex. 1108 Figure 6 in Section VI.A.2) of a complex mixer (as shown in Petrovic Figure 6) or two low pass filters after adders of a complex mixer (as shown in '275 patent Figures 2-3) would have been functionally equivalent and a matter of design choice, as both options were well known. Ex. 1102, ¶ 172.

For example, Takahiko describes a “downconverter” 1 that is used in a radio receiver, and that is very similar to the receiver of '275 patent Figure 2. Ex. 1161, [0143], Fig. 1; Ex. 1102 ¶ 173.



**Ex. 1161, Fig. 1 (annotated)**

Takahiko's downconverter 1 discloses a “full-complex mixer” 129 (purple) and low pass filters (green) 130 and 131 that are the same as what is shown in the '275 patent Figure 3. Ex. 1102, ¶ 174. Moreover, Takahiko uses full-complex mixer 129 and filters 130 and 131 in the same way that the '275 patent describes use of complex mixer 300 and filters 330 and 340: downconversion of digital I, Q signals so a desired channel is at baseband and removal of unwanted higher frequencies with low-pass filtering. Ex. 1161, [0153], [0156]; Ex. 1102, ¶ 174.

A POSITA would have been motivated to modify the complex mixers of the Petrovic stages 307 to use two low pass filters after the adders of the complex mixer, similar to the configuration of the Takahiko full-complex mixer 129 and filters 130 and 131 located after adders 173 and 176, and instead of four low pass filters within the complex mixer, to make the circuit simpler and less expensive. Ex. 1102, ¶ 175.

Because such a modification would have involved use of known circuit components in known arrangements, because of the similarity between the relevant portions of the Petrovic first sections 307 and the Takahiko full-complex mixer 129 and filters 130 and 131, and because the Takahiko full-complex mixer 129 and filters 130 and 131 would have been functionally equivalent to a Petrovic first section 307, a POSITA would have had a reasonable expectation of success and the results of the modification would have been predictable. *Id.*

A POSITA would have combined the Petrovic channel stacking system, as modified in view of Takahiko, with the Eidson demodulator/decoder for the reasons explained in Section VI.A.1.f, as the modification would not affect the input provided to a corresponding second stage 309 of the Petrovic DSSP, nor would it affect the components 158a, 158b generated by the DSSP. Ex. 1102, ¶ 176.

Accordingly, claims 11, 14, and 17-19 are also obvious over Petrovic-Eidson-Takahiko. Ex. 1102, ¶¶ 168-177. To the extent that the DFE of claim 11 is treated as a means+function limitation, the Petrovic stages 307, as modified in view of Takahiko, is the same or similar structure as the mixer 300 and filters 330 and 340 of the '275 patent, and any differences would be insubstantial. Ex. 1102, ¶ 176. Both perform the same function of selecting and outputting desired channels, in the same way by downconverting the desired channel to baseband and low pass filtering with a filter to isolate the desired channels and outputting the result to a demodulator, to

achieve the same result of selecting a plurality of desired channels from a digitized signal and outputting those channels to a demodulator. *Id.*; Section VI.A.2.

**D. Petrovic-Eidson-Takahiko-Rabaey (Claims 12-13)**

Claims 12-13 are also obvious over Petrovic-Eidson-Takahiko-Rabaey for the reasons explained in Sections VI.B and VI.C, as modification in view of Takahiko does not affect modification in view of Rabaey. Ex. 1102, ¶ 178.

**E. Cholas-Petrovic-Maalej (Claims 1, 4-5, 7-8, 10-11, 14-15, 17-18, 20)**

Claims 1, 4-5, 7-8, 10-11, 14-15, 17-18, and 20 are obvious over Cholas in view of Petrovic and Maalej. Ex. 1102, ¶¶ 179-216, *see also* ¶¶ 48-77. Before explaining how Cholas-Petrovic-Maalej teaches these claims, modification of Cholas in view of Petrovic and Maalej—and a POSITA’s reasons for that modification—are explained.

Cholas describes an STB 1710 (**red**) that receives a television signal “from the cable network,” and in particular, an input signal having RF QAM (quadrature amplitude modulation) channels carrying TV programs. Ex. 1158, Abstract, [0001]-[0006], [0010]-[0017], [0022]-[0024], [0033], [0044], [0052]-[0071], Figs. 4-6; Ex. 1102, ¶ 180.

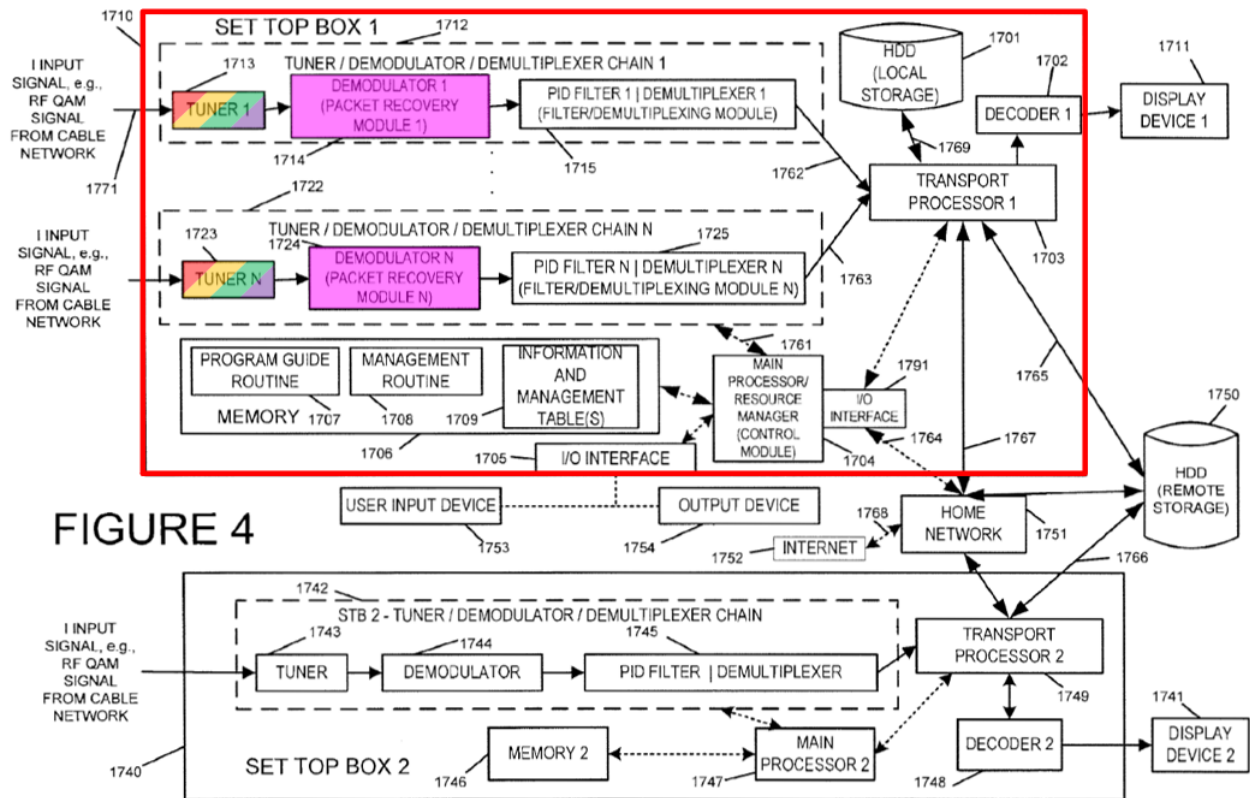


FIGURE 4

Ex. 1158, Fig. 4 (annotated)

“A typical RF signal enters” the STB 1710 “with multiple carriers between, e.g., frequencies 50-1000 MHz.” Ex. 1158, [0045]; Ex. 1102, ¶ 181. That bandwidth is greater than the 800 MHz “wide bandwidth” of the ’275 patent. Ex. 1101, 2:38-39; Ex. 1102, ¶ 181. Each tuner (**red/gold/green/purple** striped) of the STB 1710 “selects a single 6 MHz carrier frequency and passes the signal corresponding to the band” to a demodulator (**pink**). Ex. 1158, [0045]; Ex. 1102, ¶ 182.

Petrovic’s system 100 performs tuning functions similar to those described by Cholas. Ex. 1102, ¶ 185.

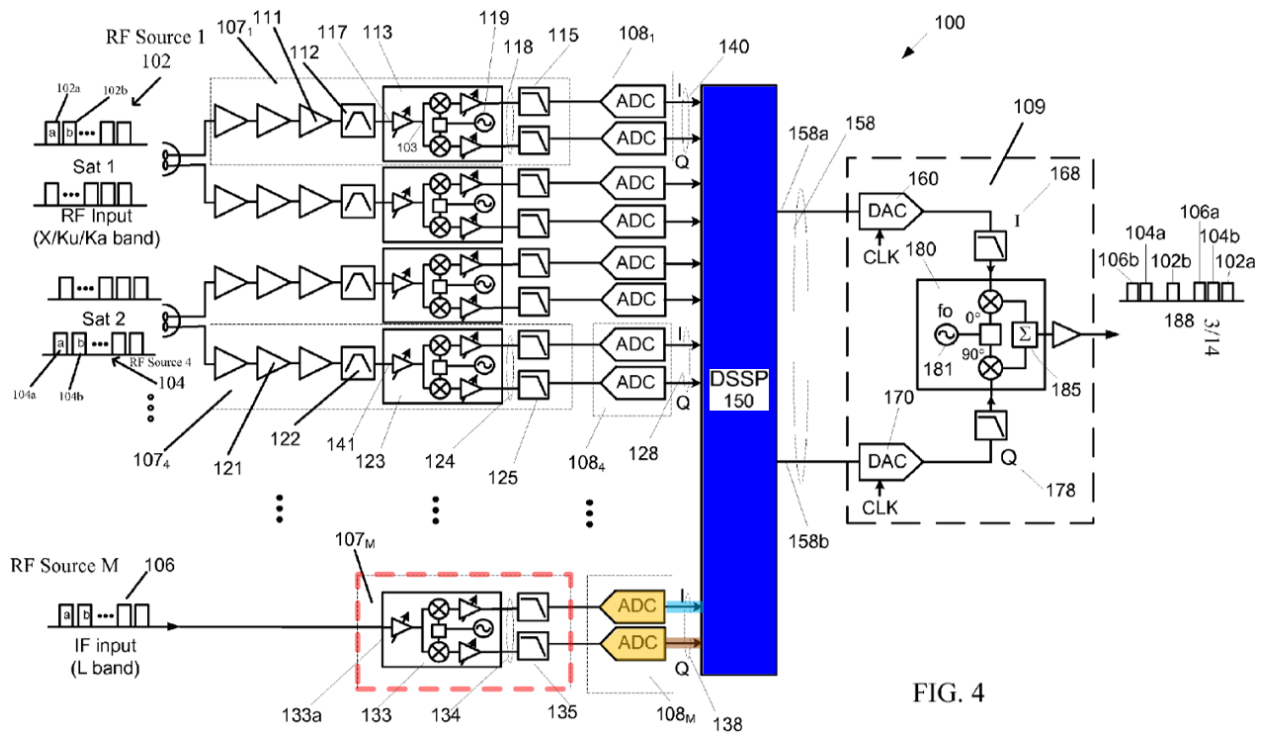
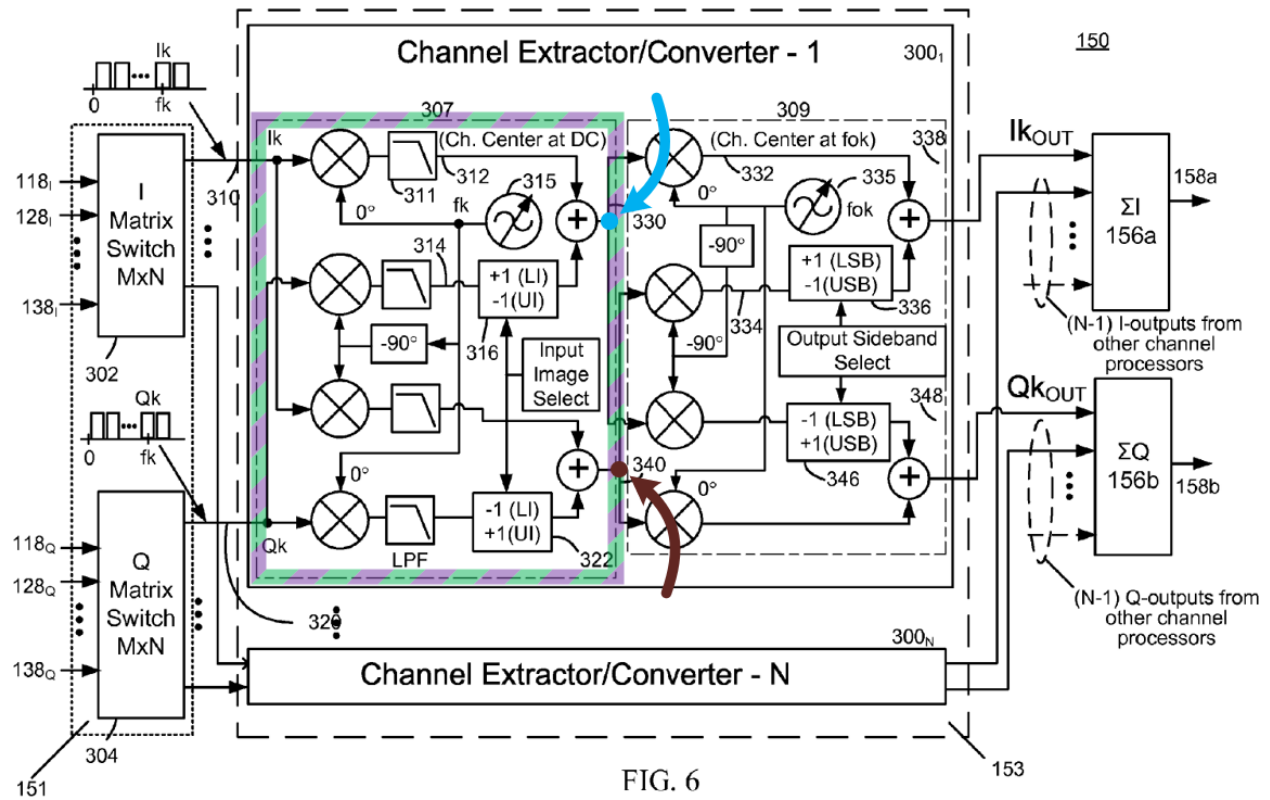


FIG. 4

### Ex. 1108, Fig. 4 (annotated)

APD stage 107<sub>M</sub> (**red** broken-line) of Petrovic's system 100 receives a wideband signal 106 that may be between 950-2150 MHz and that comprises multiple channels. Ex. 1108, [0029], [0031], [0050], Fig. 4; Ex. 1109, [0012], [0020], [0028], Fig. 1; Ex. 1102, ¶¶ 185-186. The bandwidth of the signal 106 is greater than the 800 MHz "wide bandwidth" of the '275 patent. Ex. 1101, 2:38-39; Ex. 1102, ¶ 185. APD stage 107<sub>M</sub> and analog-to-digital converters (ADCs) 108<sub>M</sub> (**gold**) generate digital I (**light blue**), Q (**brown**) components 138 that include all received channels that exist in the signal 106. Ex. 1108, [0032]-[0035], [0039], [0048]-[0052], Figs. 4-5; Ex. 1109, [0020]-[0022], [0028]-[0032], Figs. 1-2; Ex. 1102, ¶ 186.

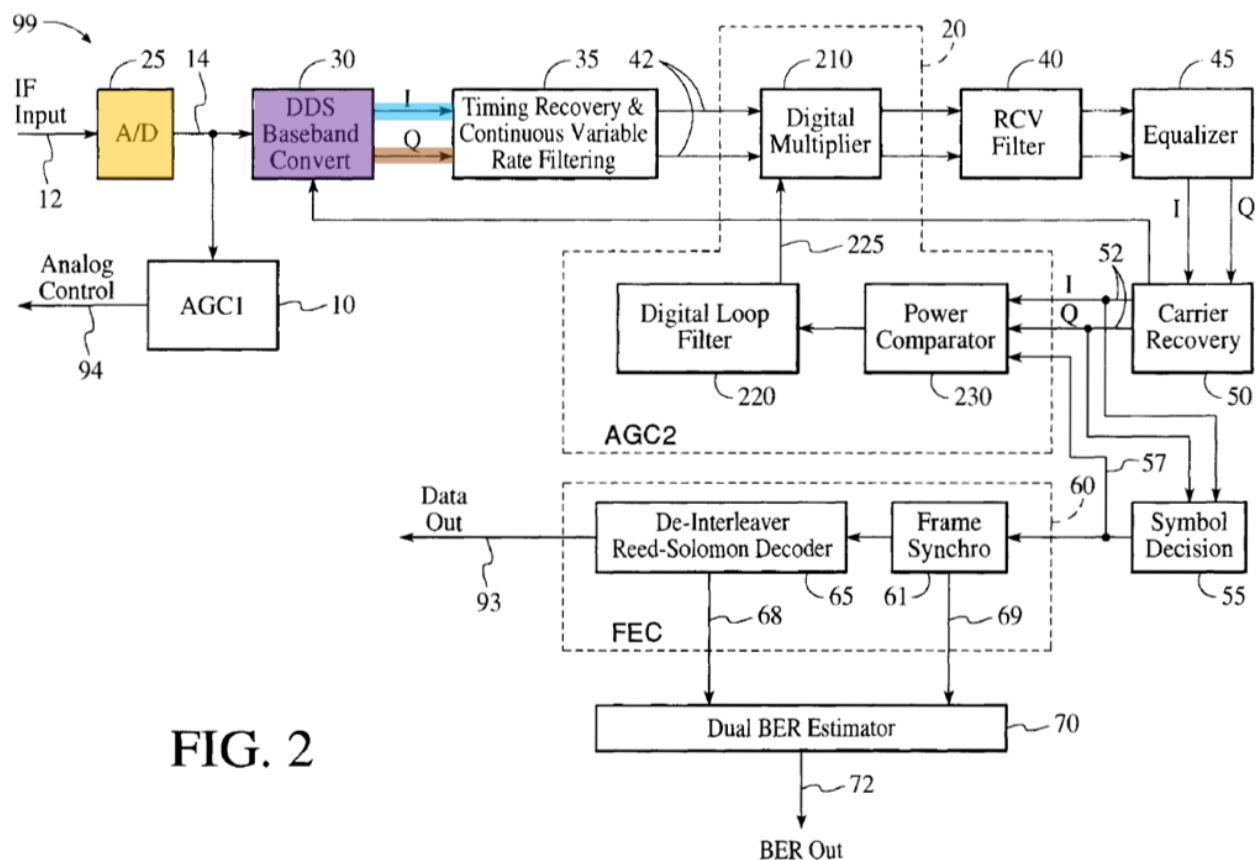
Digital signal switching and pre-processing (DSSP) stage 150 (blue) receives the digitized components 138 and “extract[s] the channels of interest ... (i.e., remove[s] all of the channels that are not of interest).” Ex. 1108, [0040], [0042], Fig. 4; Ex. 1109, [0015], [0025], [0033], Fig. 1; Ex. 1102, ¶ 187. Figure 6 shows details of the DSSP 150. Ex. 1108, [0058]; Ex. 1109, [0033], Fig. 3A; Ex. 1102, ¶ 187.



**Ex. 1108, Fig. 6 (annotated)**

As explained in section VI.A.1.e, stages 307 (purple/green) of the DSSP 150 are able to select different channels. Ex. 1108, [0055], [0059]-[0077], Fig. 6; Ex. 1109, [0033], [0037]-[0054], Fig. 3A; Ex. 1102, ¶ 188. A stage 307 extracts/selects a desired channel from the digitized I, Q components 138<sub>I</sub>, 138<sub>Q</sub> corresponding to the RF source 106 and outputs an I component 330 (light blue dot and arrow) and a

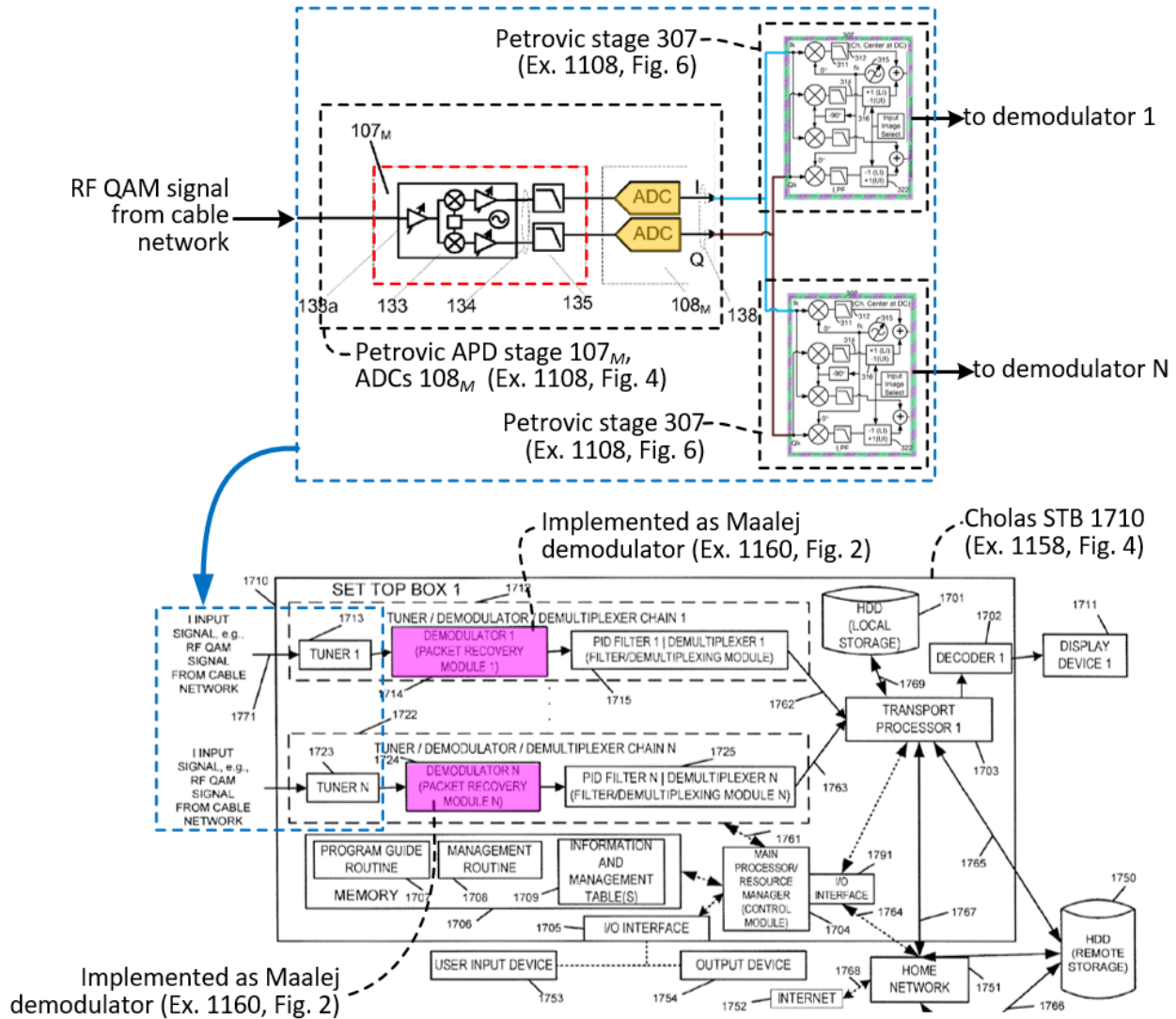
Q component 340 (**brown** dot and arrow) corresponding to a selected/desired channel. Ex. 1108, [0060]-[0077]; Ex. 1109, [0037]-[0054]; Ex. 1102, ¶ 188.



**Ex. 1160, Fig. 2 (annotated)**

Synthesizer (DDS) 30 (**purple**) converts the digitized signal to baseband I (**light blue**), Q (**brown**) components. Ex. 1160, 4:5-21, Fig. 2; Ex. 1102, ¶ 190.

As explained below, a POSITA would have modified Cholas to replace the Cholas tuners 1-N (tuners 1713-1723) with a single Petrovic tuner, and to implement Cholas demodulators 1-N (demodulators 1714-1724) using well-known demodulator structures taught by Maalej. Ex. 1102, ¶ 191. Below is an annotated Figure, prepared using excerpts from Cholas Figure 4 and Petrovic Figures 4 and 6, showing Cholas-Petrovic-Maalej. Ex. 1102, ¶ 191.



## Cholas-Petrovic-Maalej

In Cholas-Petrovic-Maalej, the Cholas tuners 1-N (tuners 1713-1723) would have been replaced with a single Petrovic tuner that would have included the Petrovic APD stage  $107_M$ , ADCs  $108_M$ , and multiple stages 307 of the DSSP 150. Ex. 1102, ¶ 192. Each of the stages 307 would, like one of the replaced Cholas tuners 1-N, output a signal (a digital I, Q pair 330, 340) corresponding to a selected "desired" channel. Ex. 1102, ¶ 192.

A POSITA would have been motivated to implement the Cholas STB with a single Petrovic tuner (e.g., APD stage 107<sub>M</sub>, ADCs 108<sub>M</sub>, and stages 307 of DSSP 150) instead of multiple separate tuners 1713-1723. Ex. 1102, ¶ 193. Implementing the Cholas STB with a single tuner would have beneficially simplified the STB and reduced the number of components. *Id.* And although Cholas does not disclose the tuners 1713-1723 performing downconversion, downconversion of a received RF signal prior to further processing was a standard technique used in receivers. *Id.* A single downconverter (as part of the APD stage 107<sub>M</sub>) would use less power and be less expensive to implement than separate downconverters for each of multiple tuners. *Id.*

Using a single Petrovic tuner would also have improved the Cholas STB with digital tuning. Ex. 1102, ¶ 194. Selecting channels in the digital domain avoids the need for bandpass filtering and Hilbert transformers, thereby reducing circuit complexity and power consumption. *Id.*; Ex. 1108, [0007], [0096]; Ex. 1109, [0003], [0069].

Implementing the Cholas STB with a Petrovic tuner instead of multiple separate tuners would have been a simple substitution of one known element for another to obtain predictable results. Ex. 1102, ¶ 194. For numerous reasons, a POSITA would have been able to substitute a Petrovic tuner for the multiple tuners

1713-1723 of the Cholas STB, and the results would have been predictable. Ex. 1102, ¶ 195.

For example, and as explained above, the output of each Petrovic stage 307 is an I, Q pair that corresponds to a selected channel. Ex. 1102, ¶ 195. Cholas shows that the output of each tuner is the input to a dedicated QAM demodulator. *Id.*; Ex. 1158, Fig. 4. And as taught by Maalej, generating digital I, Q components was a well-known preliminary step in QAM demodulation. Ex. 1160, 4:5-19, Fig. 2; Ex. 1102, ¶ 195. A POSITA would thus have recognized that outputs of Petrovic stages 307 usefully serve as inputs to existing demodulators. Ex. 1102, ¶ 195.

Modifying a Cholas STB to replace multiple separate tuners with a Petrovic tuner would also have been use of a known technique to improve a similar device in the same way. Ex. 1102, ¶ 196. For the reasons explained above, a POSITA would have applied the improvement of the Petrovic tuner (digital tuning, reduced components, reduced power consumption) to the Cholas STB, and the results would have been predictable to a POSITA. *Id.*

Each of the Cholas demodulators 1-N (demodulators 1714-1724) would have been implemented as a demodulator as taught by Maalej. Ex. 1102, ¶¶ 190-191, 197. As mentioned above, Maalej teaches that demodulation of QAM signals (such as in Cholas) is performed after generating digital I, Q components—such as a digital I, Q pair 330, 340 from a Petrovic stage 307—of a signal to be demodulated. Ex. 1102,

¶¶ 190, 197. The I, Q components output by the Maalej DDS 30 are functionally equivalent to the Petrovic I, Q components 330, 340 in Cholas-Petrovic, as both sets of I, Q components comprise baseband digital I, Q components of a signal that is to be demodulated. Ex. 1102, ¶ 197. Moreover, the Maalej demodulator outputs, similar to the Cholas demodulators, MPEG2 Transport System (TS) packets. *Id.*; Ex. 1160, 5:12-15; Ex. 1158, [0045]. Applying Maalej teachings to Cholas-Petrovic, each of the Cholas demodulators would be implemented to include components of the Maalej demodulators (e.g., blocks 35, 210, 40, 45, 50, 230, 220, 55, 61, 65, and 70) that receive I, Q components 330, 340 from a Petrovic stage 307 and that output MPEG2 TS packets to a respective Cholas PID filter. Ex. 1102, ¶ 197.

This would merely have been a combination of known prior art elements according to known methods to yield predictable results. Ex. 1102, ¶ 198. A POSITA would have recognized the functional equivalence of a Petrovic stage 307 output and the output from the Maalej DDS 30, as well as the functional equivalence of the Maalej demodulator output and the inputs to the Cholas PID filters/demultiplexers 1715-1725. *Id.* A POSITA would also have recognized that if I, Q signals of a QAM-modulated signal were to be demodulated so as to output, e.g., MPEG2 TS packets, the components of the Maalej demodulator could beneficially be used as a demodulator in the Cholas-Petrovic STB so that the signal could be demodulated. *Id.* A POSITA would thus have easily combined a Petrovic

stage 307 and components of the Maalej demodulator, as each would perform the same function in the combination that would be performed individually prior to the combination to beneficially demodulate the I and Q components. *Id.* For the same reasons, the results of combining a Petrovic stage 307 with Maalej demodulator components would have been predictable. *Id.*

# **1. Independent Claims 1, 11**

## **a. Preambles [1A], [11A]**

Cholas-Petrovic-Maalej discloses non-limiting preambles [1A] and [11A], as the Cholas STB, as modified in view of Petrovic and Maalej, receives television channels from “the cable network.” Ex. 1158, [0004], [0010]-[0011], [0022], [0024], [0044], [0059]-[0071], claim 13, Figs. 4, 6; Ex. 1180, [0012]-[0014] (“content delivery streams include, for example, multiple television programs”), [0149], [0159], claim 37; Ex. 1102, ¶¶ 183, 199. Moreover, a POSITA would have understood a cable network such as in Cholas to carry television channels. *Id.*; Ex. 1181, [0003]-[0004].

## **b. Limitations [1B], [11B]**

Cholas-Petrovic-Maalej discloses limitations [1B] and [11B]. Ex. 1102, ¶¶ 200-205. Because the Cholas-Petrovic-Maalej STB receives input from a cable network, a POSITA would have known that, in order to function, it would include an “input terminal” so that it could connect to that cable network to receive that input. Ex. 1158, [0044]; Ex. 1102, ¶ 200. An “input terminal” for connection to a

cable network was a well-known feature of STBs, and a POSITA would thus have expected an input terminal to be present. Ex. 1102, ¶ 200 (citing Ex. 1182, Ex. 1183, Ex. 1184). Indeed, Cholas incorporates by reference U.S. Pat. App. No. 11/681,774 ('774 application), which describes a STB having a “cable interface module” that couples the STB “to a service provider, e.g., a cable company.” Ex. 1158, [0010]; Ex. 1180, [0074], [0078], claim 37; Ex. 1102, ¶ 200.

The cable network signal received by the Cholas-Petrovic-Maalej STB input terminal would comprise a plurality of desired channels and a plurality of undesired channels. Ex. 1102, ¶¶ 184, 201. Cholas tuners 1713-1723 tune channels in response to user selection of a program carried on those channels, thus making the tuned channels “desired.” Ex. 1158, [0059]-[0063]; Ex. 1102, ¶¶ 184, 201. This would not change in Cholas-Petrovic-Maalej, which would merely use separate Petrovic stages 307 instead of Cholas tuners 1713-1723 to tune desired channels; Ex. 1102, ¶ 201. In a conventional cable TV system with numerous 6 MHz channels between 50-1000 MHz, such as Cholas describes, there are “undesired” channels that are not tuned by a particular STB. Ex. 1158, [0045]; Ex. 1102, ¶¶ 184, 201.

Cholas-Petrovic-Maalej also teaches that the plurality of desired channels are non-contiguous. Ex. 1102, ¶ 202. Cholas Figure 5 shows that tuner 1 (a first Petrovic stage 307 in Cholas-Petrovic-Maalej) is tuned to QAM channel 1 (in a first frequency band) and that tuner 2 (a second Petrovic stage 307 in Cholas-Petrovic-Maalej) is

tuned to QAM channel 7 (in a second frequency band). Ex. 1158, [0029]-[0030], [0042], [0045], [0054]-[0056], Fig. 5; Ex. 1102, ¶ 202.

| TUNER           | QAM CHANNEL/<br>FREQUENCY | PROGRAM<br>CHANNELS | PID   | ROUTING        |
|-----------------|---------------------------|---------------------|-------|----------------|
| TUNER 1<br>1812 | CHAN 1<br>1822            | 100                 | 10035 | LOCAL DECODER  |
|                 |                           | 101                 | 10135 | -----          |
|                 |                           | 102                 | 10236 | -----          |
|                 |                           | 103                 | 10335 | -----          |
|                 |                           | 104                 | 10461 | LOCAL HDD      |
|                 |                           | 105                 | 10587 | -----          |
| TUNER 2<br>1814 | CHAN 7<br>1824            | 700                 | 70068 | REMOTE HDD     |
|                 |                           | 701                 | 70151 | -----          |
|                 |                           | 702                 | 70282 | -----          |
|                 |                           | 703                 | 70384 | -----          |
|                 |                           | 704                 | 70487 | -----          |
|                 |                           | 705                 | 70588 | REMOTE DECODER |
| TUNER N<br>1816 | -----                     | -----               | ----- | -----          |

**FIGURE 5**

**Ex. 1158, Fig. 5**

A POSITA, reasonably assuming that QAM channel numbers in Cholas are sequentially assigned to corresponding sequential frequency bands, would understand Cholas to teach that tuned/desired QAM channel 1 is non-contiguous with tuned/desired QAM channel 7, as QAM channels 1-7 are separated by QAM channels 2-6. Ex. 1102, ¶ 203.

Moreover, Cholas Figure 5 teaches that there may be at least 3 tuners, and thus at least 3 Petrovic stages 307 to simultaneously tune 3 separate QAM channels.

Ex. 1102, ¶ 204. When at least 3 QAM channels are selected, at least 2 of those channels would be “non-contiguous.” *Id.*

Further, as a matter of common experience, and as a POSITA would have understood, users of a STB such as Cholas-Petrovic-Maalej would select channels according to their individual desires to watch content, and without regard to underlying QAM channels used to carry such content. Ex. 1158, [0047], [0060]-[0061], Fig. 6 (steps 1902, 1904); Ex. 1102, ¶ 205. Thus, a POSITA would have expected a user to operate Cholas-Petrovic-Maalej so as to select content carried by non-contiguous QAM channels. Ex. 1102, ¶ 205. As the '275 admits, it was known that users would select (i.e., “desire”) channels that are non-contiguous in a received RF bandwidth. Ex. 1101, 1:44-48, 1:55-58, 2:16-18; Ex. 1102, ¶ 205.

### **c. Limitations [1C], [11C]**

Cholas-Petrovic-Maalej discloses limitations [1C] and [11C]. Ex. 1102, ¶¶ 206-208. Cholas-Petrovic-Maalej comprises Petrovic’s APD 107<sub>M</sub>, a “radio front end” that is coupled to the input terminal and that generates a processed input signal. Section VI.E; Ex. 1108, [0032]-[0039], [0050], Figs. 4-5; Ex. 1109, [0010], [0017], [0031]-[0032], Figs. 1-2; Ex. 1102, ¶ 206.

Similar to the Petrovic APD stage 107<sub>I</sub> discussed in Section VI.A.1.c, the Petrovic APD stage 107<sub>M</sub> performs processing that includes amplifying in an amplifier of APD stage 107<sub>M</sub> that is similar to Petrovic amplifier 222a (of APD stage

107<sub>1</sub>), mixing in mixers of APD stage 107<sub>M</sub> that are similar to Petrovic mixers 202 and 204 (of APD stage 107<sub>1</sub>) using 90° phase-shifted oscillator signals from a source similar to Petrovic synthesizer/frequency source 119 (of APD stage 107<sub>1</sub>) and a phase shifter similar to Petrovic phase shifter 105 (of APD stage 107<sub>1</sub>), amplifying by amplifiers of APD stage 107<sub>M</sub> that are similar to Petrovic amplifiers 222b and 222c (of APD stage 107<sub>1</sub>), and filtering by low pass filters of APD stage 107<sub>M</sub> that are similar to Petrovic filters 115 (of APD stage 107<sub>1</sub>). Section VI.A.1.c; Ex. 1108, [0032]-[0039], [0050], Figs. 4-5; Ex. 1109, [0010], [0017], [0020], [0031]-[0032], Figs. 1-2; Ex. 1102, ¶ 207. Petrovic APD stage 107<sub>M</sub> performs the same type of processing performed by the radio front end 210 of the '275 patent, and generates the same type of processed input signal—downconverted and filtered in-phase and quadrature components of the input signal. Ex. 1101, 4:40-5:25, Fig. 2; Ex. 1108, [0032]-[0039], [0050], Figs. 4-5; Ex. 1109, [0010], [0017], [0020], [0031]-[0032], Figs. 1-2; Ex. 1102, ¶ 207.

To the extent that “radio front end” is argued to be a means+function limitation, it is taught by Cholas-Petrovic-Maalej for the reasons explained in Section VI.A.2, as the structure of the Petrovic APD stage 107<sub>M</sub> of Cholas-Petrovic-Maalej is the same as, operates in the same way as, and achieves the same result as the structure of the Petrovic APD stage 107<sub>1</sub> of Petrovic-Eidson, and thus is the same as (or equivalent to) the corresponding structure of the radio front end shown in '275

patent Figure 2, with any differences being insubstantial. Section VI.A.2; Ex. 1108, [0032]-[0039], [0050], Figs. 4-5; Ex. 1109, [0010], [0017], [0020], [0031]-[0032], Figs. 1-2; Ex. 1102, ¶ 208.

**d. Limitations [1D], [11D]**

Cholas-Petrovic-Maalej discloses limitations [1D] and [11D]. Ex. 1102, ¶ 209. ADC pair 108<sub>M</sub> is coupled to the radio front end 107<sub>M</sub>. Section VI.E; Ex. 1108, [0039], Fig. 4; Ex. 1109, [0005], [0010], [0020], [0022], [0028]-[0029], Fig. 1; Ex. 1102, ¶ 209. ADC pair 108<sub>M</sub> digitizes the processed input signal, received from the radio front end 107<sub>M</sub>, to generate a digitized signal. Ex. 1108, [0039], [0051]-[0052], Fig. 4; Ex. 1109, [0005], [0010], [0020], [0022], [0028]-[0029], Fig. 1; Ex. 1102, ¶ 209.

**e. Limitations [1E], [11E]**

Cholas-Petrovic-Maalej discloses limitations [1E] and [11E]. Ex. 1102, ¶¶ 210-211. The ADC pair 108<sub>M</sub> is coupled to a DFE that comprises a plurality of Petrovic stages 307. Section VI.E; Ex. 1108, [0053], [0055], [0059]-[0077], Figs. 4, 6; Ex. 1109, [0033], [0037]-[0054], Figs. 1, 3A; Ex. 1102, ¶ 210. Each Petrovic stage 307 extracts a desired channel from the digitized signal received from the ADC pair 108<sub>M</sub>. Section VI.E; Ex. 1108, [0060]-[0077]; Ex. 1109, [0037]-[0054]; Ex. 1102, ¶ 210.

To the extent that “digital front end” is argued to be a means+function limitation, it is taught by Cholas-Petrovic-Maalej (and in particular, the Petrovic stages 307) for the reasons explained in Section VI.A.2. Ex. 1102, ¶ 211.

**f. Limitations [1F], [11F]**

Cholas-Petrovic-Maalej discloses limitations [1F] and [11F]. Ex. 1102, ¶ 212. In Cholas-Petrovic-Maalej, the Petrovic stages 307 are the DFE of limitations [1E]/[11E] and [1F]/[11F]. *Id.* The Petrovic stages 307 select the plurality of desired channels from the digitized signal received by the stages 307 from the Petrovic ADC pair 108<sub>M</sub> and output the selected plurality of channels as a digital datastream to demodulators (the Cholas demodulators implemented to include components of the Maalej demodulators) that extract information encoded in the digital datastream. *Id.*; Ex. 1160, 5:12-15 (“MPEG2 Transport System (TS) packets” are “the output of the demodulator”); Ex. 1115, p. 7 (demodulation is “reconversion of a modulated signal back into its original form by extracting the data from the modulated carrier”); Section VI.E.

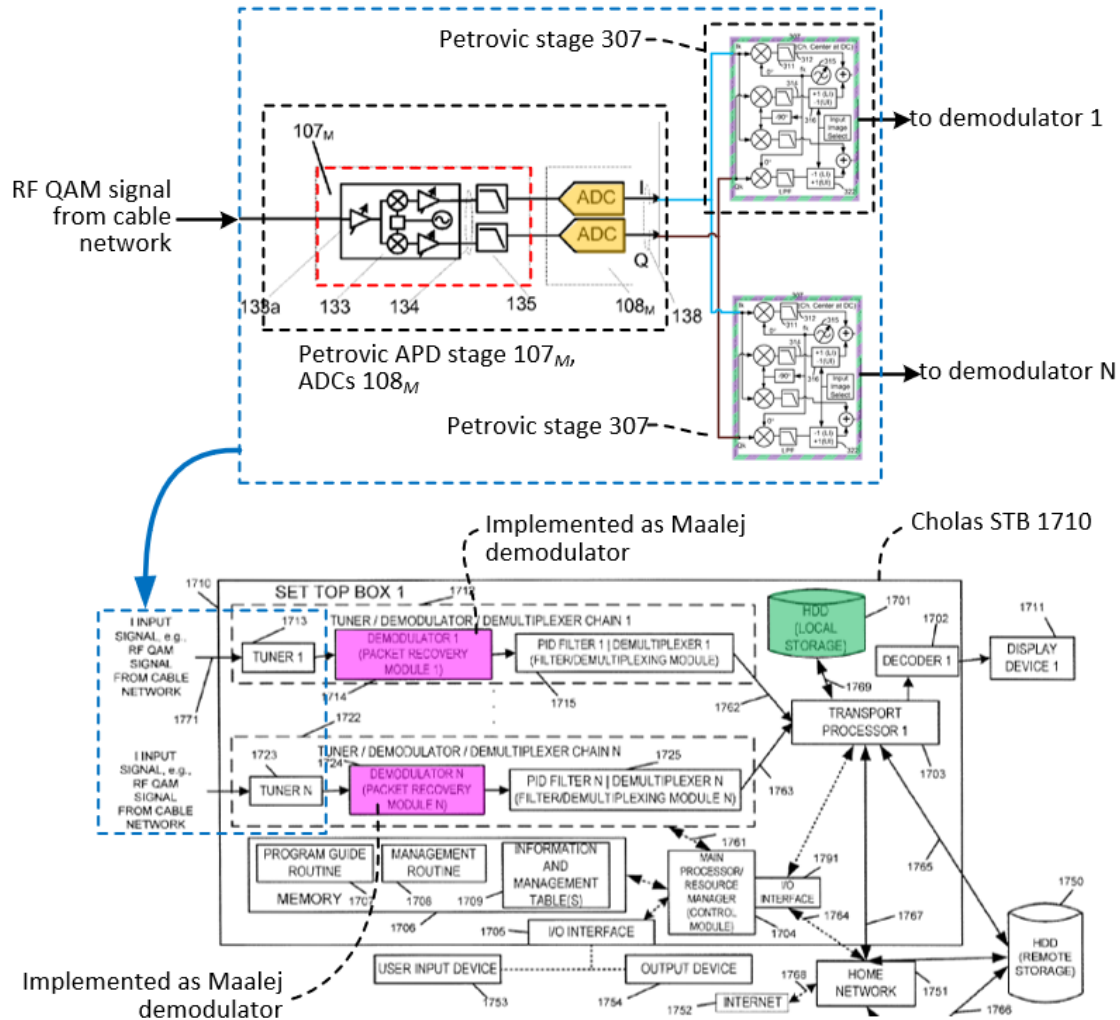
**2. Claims 4, 14**

Cholas-Petrovic-Maalej discloses claims 4 and 14. Ex. 1102, ¶ 213. Petrovic’s ADC pair 108<sub>M</sub> comprises first and second ADCs that respectively generate digital in-phase and quadrature signals—components 138. Section VI.E; Ex. 1108, [0052], Fig. 4; Ex. 1109, [0022], Fig. 1; Ex. 1102, ¶ 213.

### 3. Claims 5, 15

**[5]/[15] “The [method of claim 1]/[television receiver device of claim 11], wherein the extracted information is stored for use in a digital video recorder (DVR).”**

Cholas-Petrovic-Maalej discloses claims 5 and 15. Ex. 1102, ¶ 214. Cholas STB 1710 comprises a DVR 1701 (**green**), and this DVR remains in the Cholas-Petrovic-Maalej system. Ex. 1158, [0033] (“a digital storage device, e.g., a DVR, ... corresponding to the STB”), [0045] (streams can be directed to “internal HDD (local storage) 1701, typically a hard drive”), [0054]-[0057], Figs. 4-5; Ex. 1102, ¶ 214.



## Cholas-Petrovic-Maalej

### 4. Claims 7-8, 17-18

Cholas-Petrovic-Maalej discloses claims 7-8 and 17-18. Ex. 1102, ¶ 215. As explained in connection with preambles [1A] and [11A], Cholas-Petrovic-Maalej receives a television signal from “the cable network,” and a POSITA would have understood a cable network such as in Cholas to carry television channels. Section VI.E.1.a; Ex. 1102, ¶ 215.

## **5. Claims 10, 20**

**[10]/[20] “The [method of claim 1]/[television receiver device of claim 11], wherein the broadcast channels comprise cable broadcast channels.”**

Cholas-Petrovic-Maalej discloses claims 10 and 20. Ex. 1102, ¶ 216. The Cholas STB, as modified in view of Petrovic and Maalej, receives cable broadcast channels. Section VI.E; Ex. 1158, [0004]-[0006], [0044]-[0057], Figs. 4-5; Ex. 1102, ¶ 216.

### **F. Cholas-Petrovic-Maalej-Rabaey (Claims 2-3, 12-13)**

Cholas-Petrovic-Maalej-Rabaey discloses claims 2-3 and 12-13. Ex. 1102, ¶¶ 217-221. Digital data, such as the I, Q components 330, 340 output by a Petrovic stage 307 in Cholas-Petrovic-Maalej, is communicated as binary units (“bits”) in the form of electrical signals on wires. Ex. 1102, ¶ 217; Ex. 1116, pp. 23-24, 27-29, 48-51. Multiple bits can be sent over multiple separate wires, one wire for each bit (“parallel interface”), or one bit at a time over a single wire (“serial interface”). Ex. 1102, ¶ 217; Ex. 1115, pp. 5, 8 (defining “parallel”), 10 (defining “serial”); Ex. 1116, pp. 79-80 (Figure 6-25). As explained in Section VI.E, the Petrovic stages 307 output desired channels as digital I, Q pairs 330, 340, and each of the Cholas demodulators would be implemented to include components of the Maalej demodulators that receive I, Q components 330, 340 from a Petrovic stage 307. Ex. 1108, [0060]-[0077]; Ex. 1109, [0037]-[0054]; Ex. 1160, 4:5-21, Fig. 2; Ex. 1102, ¶ 218. For the same reasons explained in Section VI.B, outputting of a digital datastream from the

Petrovic stages 307 (the DFE of Cholas-Petrovic-Maalej) to demodulators via a serial or parallel interface would have been an obvious design choice as taught by Rabaey, whose teachings would be applied to Cholas-Petrovic-Maalej in the same manner they would be applied to Petrovic-Eidson. Ex. 1102, ¶¶ 218-221.

**G. Cholas-Petrovic-Maalej-Lee (Claims 6, 16)**

**[6]/[16] “The [method of claim 1]/[television receiver device of claim 11], wherein the extracted information is output for a picture-in-picture display.”**

Lee discloses that it was known for STBs to tune multiple channels and use the multiple tuned channels to provide picture-in-picture (PIP) functionality. Ex. 1153, [0031]; Ex. 1102, ¶ 223. A POSITA would have configured the Cholas-Petrovic-Maalej STB to provide a PIP display so that the STB could provide beneficial additional functionality for the user. *Id.*, ¶¶ 222-224; Ex. 1153, [0006].

Using the Cholas-Petrovic-Maalej STB to provide PIP functionality would also have been a use of a known technique (providing PIP output using an STB, per Lee) to improve a similar device (a Cholas-Petrovic-Maalej STB) in the same way. Ex. 1102, ¶ 224. A POSITA could have readily modified the Cholas-Petrovic-Maalej STB to provide PIP functionality, as taught by Lee, because PIP output was established and understood. *Id.*, ¶¶ 71, 224. For the same reasons, the results of that modification would have been predictable and POSITA would have had an expectation of success. *Id.*, ¶ 224.

#### **H. Cholas-Petrovic-Maalej-Takahiko (Claims 11, 14-15, 17-18, 20)**

A POSITA would have been motivated to modify the complex mixers of the Petrovic stages 307 in view of Takahiko, in the manner described in Section VI.C and for the reasons explained in Section VI.C. Ex. 1102, ¶ 225. Such modification of Petrovic stages 307 in view of Takahiko would not have affected modification of Cholas in view of Petrovic and Maalej, and thus claims 11, 14-15, 17-18, and 20 are also obvious over Cholas-Petrovic-Maalej-Takahiko for the reasons explained in Sections VI.E through VI.E.5. *Id.* To the extent that the DFE of claim 11 is treated as a means+function limitation, the Petrovic stages 307, as modified in view of Takahiko, are still the claimed DFE for the reasons explained in Section VI.C. *Id.*

#### **I. Cholas-Petrovic-Maalej-Takahiko-Rabaey (Claims 12-13)**

Claims 12-13 are also obvious over Cholas-Petrovic-Maalej-Takahiko-Rabaey for the reasons explained in Sections VI.F and VI.H, as modification of Petrovic stages 307 in view of Takahiko would not have affected modification of Cholas in view of Petrovic, Maalej, and Rabaey. Ex. 1102, ¶ 226.

#### **J. Cholas-Petrovic-Maalej-Takahiko-Lee (Claim 16)**

Claim 16 is also obvious over Cholas-Petrovic-Maalej-Takahiko-Lee for the reasons explained in Sections VI.G and VI.H, as modification of Petrovic stages 307 in view of Takahiko would not have affected modification of Cholas in view of Petrovic, Maalej, and Lee. Ex. 1102, ¶ 227.

## **VII. GROUNDS FOR STANDING & FEE PAYMENT**

Petitioner hereby certifies that the '275 patent is available for, and Petitioner is not barred or estopped from requesting, *inter partes* review challenging claims 1-20.

Pursuant to 37 C.F.R. § 42.103, the undersigned authorizes the charge of any required fees to Deposit Account No. 19-0733.

## **VIII. CONCLUSION**

*Inter partes* review should be instituted and claims 1-20 canceled.

Dated: December 6, 2024

By: /Frederic M. Meeker/

Frederic M. Meeker  
Reg. No. 35,282  
Banner & Witcoff, Ltd.  
1100 13th Street, NW  
Suite 1200  
Washington, DC 20005  
(202) 824-3000  
fmeeker@bannerwitcoff.com

## **CERTIFICATION UNDER 37 CFR § 42.24(d)**

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for Inter Partes Review totals 13,869, which is less than the 14,000 allowed under 37 CFR § 42.24(a)(1)(i). This total includes 13,762 words as counted by the Word Count feature of Microsoft Word and 107 words used in annotations.

Pursuant to 37 C.F.R. § 42.24(a)(1), this count does not include the table of contents, the table of authorities, mandatory notices under § 42.8, the certificate of service, this certification of word count, the claims listing appendix, or appendix of exhibits.

BANNER & WITCOFF, LTD

Dated: December 6, 2024

By: /Frederic M. Meeker/

Frederic M. Meeker  
Reg. No. 35,282  
Banner & Witcoff, Ltd.  
1100 13th Street, NW  
Suite 1200  
Washington, DC 20005  
(202) 824-3000  
fmeeker@bannerwitcoff.com

## CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105, I hereby certify that I caused a true and correct copy of this Petition for *Inter Partes* Review in connection with U.S. Patent No. 11,785,275 and supporting evidence to be served via FedEx Priority Overnight on December 6, 2024, on the following:

**23446 - MCANDREWS HELD & MALLOY, LTD**  
500 WEST MADISON STREET  
SUITE 3400  
CHICAGO, IL 60661  
UNITED STATES

Dated: December 6, 2024

By: /Frederic M. Meeker/

Frederic M. Meeker  
Reg. No. 35,282

**CLAIMS LISTING APPENDIX**  
U.S. Pat. No. 11,785,275

| Designation | Claim Language                                                                                                                                                                                                                                         |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 1     |                                                                                                                                                                                                                                                        |
| [1A]        | A method for operating a television receiver, comprising:                                                                                                                                                                                              |
| [1B]        | receiving, by an input terminal, an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels, wherein the plurality of desired channels are non-contiguous; |
| [1C]        | processing, by a radio front end coupled to the input terminal, the input signal to generate a processed input signal;                                                                                                                                 |
| [1D]        | digitizing, by an analog-to-digital converter (ADC) coupled to the radio front end, the processed input signal to generate a digitized signal;                                                                                                         |
| [1E]        | selecting, by a digital frontend (DFE) coupled to the ADC, the plurality of desired channels from the digitized signal; and                                                                                                                            |
| [1F]        | outputting, by the DFE, the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator extracts information encoded in the digital datastream.                                                |
| Claim 2     |                                                                                                                                                                                                                                                        |
| 2           | The method of claim 1, wherein the DFE outputs the digital datastream via a serial interface.                                                                                                                                                          |
| Claim 3     |                                                                                                                                                                                                                                                        |
| 3           | The method of claim 1, wherein the DFE outputs the digital datastream via a parallel interface.                                                                                                                                                        |
| Claim 4     |                                                                                                                                                                                                                                                        |
| 4           | The method of claim 1, wherein the ADC comprises:<br>a first ADC configured to generate a digital in-phase signal;<br>and<br>a second ADC configured to generate a digital quadrature signal.                                                          |
| Claim 5     |                                                                                                                                                                                                                                                        |
| 5           | The method of claim 1, wherein the extracted information is stored for use in a digital video recorder (DVR).                                                                                                                                          |

| Designation | Claim Language                                                                                                                                                                                                                                              |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 6     |                                                                                                                                                                                                                                                             |
| 6           | The method of claim 1, wherein the extracted information is output for a picture-in-picture display.                                                                                                                                                        |
| Claim 7     |                                                                                                                                                                                                                                                             |
| 7           | The method of claim 1, wherein the plurality of desired channels comprises at least one television channel.                                                                                                                                                 |
| Claim 8     |                                                                                                                                                                                                                                                             |
| 8           | The method of claim 1, wherein the plurality of undesired channels comprises at least one television channel.                                                                                                                                               |
| Claim 9     |                                                                                                                                                                                                                                                             |
| 9           | The method of claim 1, wherein the broadcast channels comprise satellite broadcast channels.                                                                                                                                                                |
| Claim 10    |                                                                                                                                                                                                                                                             |
| 10          | The method of claim 1, wherein the broadcast channels comprise cable broadcast channels.                                                                                                                                                                    |
| Claim 11    |                                                                                                                                                                                                                                                             |
| [11A]       | A television receiver device, comprising:                                                                                                                                                                                                                   |
| [11B]       | an input terminal operable to receive an input signal comprising broadcast channels, the broadcast channels comprising a plurality of desired channels and a plurality of undesired channels, wherein the plurality of desired channels are non-contiguous; |
| [11C]       | a radio front end, coupled to the input terminal, operable to process the input signal;                                                                                                                                                                     |
| [11D]       | an analog-to-digital converter (ADC), coupled to the radio front end, operable to digitize the processed input signal to generate a digitized signal; and                                                                                                   |
| [11E]       | a digital frontend (DFE), coupled to the ADC, operable to select the plurality of desired channels from the digitized signal and                                                                                                                            |
| [11F]       | output the selected plurality of desired channels to at least one demodulator as a digital datastream, wherein the demodulator is operable to extract information encoded in the digital datastream.                                                        |
| Claim 12    |                                                                                                                                                                                                                                                             |
| 12          | The television receiver device of claim 11, wherein the DFE is operable to output the digital datastream via a serial interface.                                                                                                                            |

| Designation | Claim Language                                                                                                                                                                                                     |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 13    |                                                                                                                                                                                                                    |
| 13          | The television receiver device of claim 11, wherein the DFE is operable to output the digital datastream via a parallel interface.                                                                                 |
| Claim 14    |                                                                                                                                                                                                                    |
| 14          | The television receiver device of claim 11, wherein the ADC comprises:<br>a first ADC configured to generate a digital in-phase signal;<br>and<br>a second ADC configured to generate a digital quadrature signal. |
| Claim 15    |                                                                                                                                                                                                                    |
| 15          | The television receiver device of claim 11, wherein the extracted information is stored for use in a digital video recorder (DVR).                                                                                 |
| Claim 16    |                                                                                                                                                                                                                    |
| 16          | The television receiver device of claim 11, wherein the extracted information is output for a picture-in-picture display.                                                                                          |
| Claim 17    |                                                                                                                                                                                                                    |
| 17          | The television receiver device of claim 11, wherein the plurality of desired channels comprises at least one television channel.                                                                                   |
| Claim 18    |                                                                                                                                                                                                                    |
| 18          | The television receiver device of claim 11, wherein the plurality of undesired channels comprises at least one television channel.                                                                                 |
| Claim 19    |                                                                                                                                                                                                                    |
| 19          | The television receiver device of claim 11, wherein the broadcast channels comprise satellite broadcast channels.                                                                                                  |
| Claim 20    |                                                                                                                                                                                                                    |
| 20          | The television receiver device of claim 11, wherein the broadcast channels comprise cable broadcast channels.                                                                                                      |