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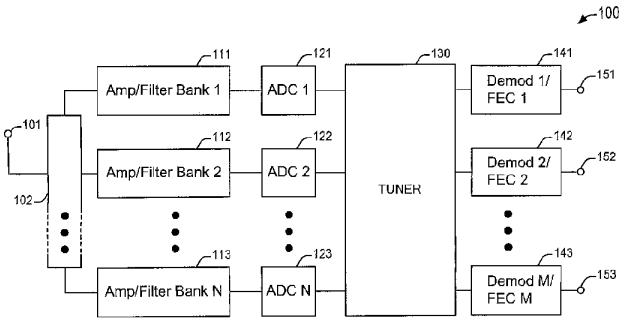
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(54) Title: MULTICHANNEL DIGITAL CABLE TUNER



(57) Abstract: A method and apparatus is presented for simultaneous reception of a plurality of digital RF channels. Specifically, N amplifier-filter circuits (111, 112, 113) are configured to receive and separate a multichannel analog RF input signal into N analog signals, each including a different frequency band. N analog-to-digital converters (121, 122, 123) are provided, each respectively coupled to one of the N amplifier-filter circuits (111, 112, 113) and configured to receive an analog signal and generate a respective digital signal. A digital tuner (130) is coupled to receive and demultiplex the N digital signals generated by the N analog-to-digital converters (121, 122, 123), thereby recovering M digital RF channels. M demodulation circuits (141, 142, 143) are provided for performing demodulation and forward-error-correction of the M digital RF channels (see FIG. 1). This combination of components permits substantially simultaneous reception of multiple digital cable channels within a single digital receiver circuit suitable for use with conventional cable delivery systems and at a reasonable cost.

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MULTICHANNEL DIGITAL CABLE TUNER

Field of the Invention

[0001] The present invention relates to television communications and, in particular, to an apparatus and method for multi-channel television reception.

Background of the Invention

[0002] In order to accommodate the increasing demands of television consumers, cable television (cable TV or CATV) broadcasters have transformed themselves in recent years to provide digital (as opposed to traditional analog) channels among their broadcast content. Cable TV broadcasters have employed digital technology to, for example, increase the number of offered channels, add per-channel programming information, and provide remote-interaction functionality such as pay-per-view (PPV) movies and sporting events.

[0003] As the benefits of digital cable television have become known, consumer demand has continued to rise, along with demand for increased variety of content. This demand for increased variety has reached the end-user level, where several users within a single household may prefer to enjoy different cable television programs simultaneously. Because digital cable television receivers, or set top boxes (STBs), were previously designed to receive only a single channel at a time, multiple simultaneous channel reception presented a problem for multi-user households.

[0004] Traditional solutions to this problem have included the provision of several receivers or STBs, each located in different rooms of the household. In this way, each television reception device, for example a television set, could be coupled to its own STB, and each user could independently receive and control reception of different cable television programs. These traditional solutions suffered from several disadvantages including increased cost of acquiring a plurality of STBs, increased space requirements for the additional STBs, need for additional household coaxial cable wiring, etc.

[0005] In addition to the above-mentioned disadvantages, traditional solutions lack the flexibility required to keep pace with new developments in consumer demand and diversification of that demand. For example, consumers now demand

support for simultaneous reception and display of multiple television channels on a single television screen (e.g., picture-in-picture (PiP)). In addition, the emergence of personal video recorder (PVR) technology increases the demand for multi-channel reception capability. Many PVR's include the ability to tune one or more channels for viewing, while simultaneously tuning one or more additional channels for recording to a recording medium. The information on the recorded channels is then available for later playback or other processing.

[0006] Along with the ability to simultaneously tune multiple channels it would be advantageous for tuning equipment to include a networking functionality that would allow distribution of received content to various locations, such as various rooms within a residence. It would therefore be desirable to have a distribution network coupled to a multichannel tuner device. Furthermore, it would be advantageous if such a distribution network included a networking device that was integral to a tuner system, thus simplifying setup and maintenance of a network for the redistribution of cable channel content.

[0007] Consumers have begun to demand additional flexibility in the location of reception devices, including handheld personal media devices capable of remotely receiving digital television programs as well as digital music programs, without the increased cost of a plurality of STBs.

Summary of the Invention

[0008] Given consumer demand for increased flexibility and convenience, there is a need for a digital television receiver capable of simultaneously receiving a plurality of channels, designed for delivery of a variety of digital content, and suitable for use with conventional cable television delivery systems.

[0009] The present invention is directed to a method and apparatus for simultaneous reception of a plurality of digital television channels. Specifically, the apparatus of the present invention is directed to a multichannel receiver circuit including a plurality of amplifier-filter circuits configured to receive a multichannel analog RF input signal, the plurality of amplifier-filter circuits including at least a first amplifier-filter circuit configured to generate a first analog signal including a first band of frequencies and a second amplifier-filter circuit configured to generate a second analog signal including a second band of frequencies. A plurality of analog-to-digital

converters is provided, each respectively coupled to one of the plurality of amplifier-filter circuits, the plurality of analog-to-digital converters including at least a first analog-to-digital converter configured to receive the first analog signal and generate a first digital signal and a second analog-to-digital converter configured to receive the second analog signal and generate a second digital signal. A digital tuner is provided, coupled to receive at least the first and second digital signals generated by the plurality of analog-to-digital converters, the digital tuner configured to recover a plurality of digital RF channels.

[0010] In an alternate embodiment, in addition to the above a plurality of demodulator circuits is coupled to the digital tuner, the plurality of demodulator circuits including at least a first demodulator circuit configured to receive and demodulate a first channel of the plurality of digital RF channels and a second demodulator circuit being configured to receive and demodulate a second channel of the plurality of digital RF channels. The plurality of demodulator circuits includes circuitry configured for forward error correction.

[0011] The method of the present invention includes receiving at least one multichannel analog RF input signal; separating the multichannel analog RF input signal into at least two analog signals including a first analog signal including a first band of frequencies and a second analog signal including a second band of frequencies; converting the at least two analog signals into at least two respective digital signals, including converting the first analog signal into a first digital signal and converting the second analog signal into a second digital signal; and demultiplexing the at least two digital signals to recover the plurality of digital RF channels.

[0012] In an alternative embodiment, in addition to the above steps the method includes demodulating the plurality of digital RF channels, including at least demodulating a first digital RF channel and demodulating a second digital RF channel; and forward-error-correcting the plurality of digital RF channels, including at least performing a first forward-error-correction of the first digital RF channel and performing a second forward-error-correction of the second digital RF channel.

[0013] This combination of components, when employed in the configuration of the present invention, permits substantially simultaneous reception of a plurality of digital cable television channels within a single digital receiver circuit. These

advantages can be provided in a form suitable for use with conventional cable television delivery systems and at a reasonable cost.

Brief Description of the Drawings

[0014] In the drawings:

[0015] Fig. 1 is a simplified block diagram illustrating an exemplary multichannel receiver circuit in accordance with the present invention;

[0016] Fig. 2 is a simplified block diagram illustrating a portion of the exemplary multichannel receiver circuit shown in Fig. 1;

[0017] Fig. 3 is a simplified block diagram illustrating another portion of the exemplary multichannel receiver circuit shown in Fig. 1;

[0018] Fig. 4 is a flow diagram illustrating an exemplary method of receiving a plurality of digital RF channels in accordance with an alternate embodiment of the present invention.

Detailed Description

[0019] The following discussion of the method and apparatus directed to a multichannel receiver circuit will help illuminate the features and advantages of the present invention, including its ease of formation using conventional techniques of constructing electronic devices and circuits which are well known in the art.

[0020] In the following discussion, the singular term "signal" and plural term "signals" are used interchangeably and are to be understood as including analog or digital information, at a single frequency or a plurality of frequencies, and may or may not include coding, modulation, sideband information, or other features of signals or waveforms well known in the art. Furthermore, when reference is made to a "receiver," "transmitter," "output," or "input," previous process steps may have been utilized to form signals or waveforms compatible with these features.

[0021] In addition, no particular order is required for the method steps described below, with the exception of those logically requiring the results of prior steps, for example converting of the first and second analog signals into first and second digital signals logically requires the prior generation of first and second analog signals. Otherwise, enumerated steps are provided below in an exemplary order which may

be altered. For instance, the several demodulation steps may be rearranged or performed simultaneously.

[0022] An exemplary embodiment of the invention will now be described with reference to FIG. 1. Although the invention will be described using the environment of reception of cable television signals, it should be apparent that the invention may be used in other types of radio-frequency communications systems as well, including reception of digital television channels via satellite and terrestrial television transmission systems. In contrast to the scheme described above, exemplary embodiments of the present invention provide substantially simultaneous recovery of a plurality of digital RF channels within a single multichannel receiver circuit, thereby reducing cost and increasing system flexibility.

[0023] FIG. 1 shows a simplified block diagram representation of a multichannel receiver circuit generally designated 100 in accordance with an aspect of the present invention. The multichannel receiver circuit 100 includes a plurality of amplifier-filter banks or circuits 111, 112, 113, a plurality of analog-to-digital converters 121, 122, 123, a digital tuner 130, and a plurality of demodulator circuits 141, 142, 143. It should be apparent from FIG. 1 that, although three instances of each plurality are shown, the present invention is not so limited and any number of amplifier-filter circuits, analog-to-digital converters, and/or demodulator circuits may be used in accordance with the present invention. In addition, the number (1 . . . M) of demodulator circuits provided is not necessarily related to the number (1 . . . N) of amplifier-filter circuits and/or analog-to-digital converters provided, and accordingly the present invention should not be so limited.

[0024] In operation, according to one embodiment, a multichannel analog RF input signal received at input coupler 101 is split into a plurality of substantially identical signals at splitter 102. Splitter 102 may include one or more amplifiers, filters, or other components (not shown) which reduce or overcome insertion loss or other adverse effects of the split, as should be apparent to one of ordinary skill in the art. The plurality of amplifier-filter circuits 111, 112, 113 then segregates the multichannel analog input signal into a plurality of separate analog signals of differing frequency ranges, or "bands." Each separate analog signal is then converted from analog to digital form in an analog-to-digital converter 121, 122, 123.

[0025] It should be noted that, in one embodiment of the invention, the splitter 102 is omitted. In this embodiment,the respective inputs of the amplifier/filter banks 111, 112, 113 are mutually directly connected to the input coupler 101. The amplifier/filter banks 111, 112, 113 serve as a demultiplexer to demultiplex the incoming signal received at the input coupler 101. In one embodiment, each amplifier/filter bank has particular characteristics that permit the passage of a specific range of frequencies substantially independent of the frequency selection characteristics of the other amplifier/filter banks. For example, one filter might have a pass-band of about 5 to about 300 MHz, while another filter might have a pass band of about 300 to about 600 MHz.

[0026] In one embodiment, the band break edges would be passed through two amplifier sets, e.g., amplifier/filter banks 111, 112. Thus, for example, the channels present just above a distal 300 MHz would pass through both the the 5 to 300 MHz filter and the 300 to 600 MHz filter. This helps to ensure the continuous coverage of all channel despite non-ideal filter characteristics.

[0027] The converted digital signals are coupled to the digital tuner 130, which demultiplexes the converted digital signals to generate a plurality of digital channel signals. Each digital channel signal is then coupled to a separate demodulator 141, 142, 143, which performs demodulation and forward-error-correction (FEC) operations appropriate for the content of that digital channel. Finally, in one embodiment, the resulting digital channel signals are each coupled to a separate output coupler 151, 152, 153 for further processing including for example MPEG transport processing.

[0028] Each of the plurality of amplifier-filter banks or circuits 111, 112, 113 is configured to process frequencies within a specified band. For example, a first amplifier-filter circuit 111 may be configured to process frequencies from about 5 MHz to about 300 MHz, a second amplifier-filter circuit 112 may be configured for frequencies between about 300 MHz and about 600 MHz, and a third amplifier-filter circuit 113 may be configured for frequencies from about 600 MHz to about 900 MHz. In such an example, the present invention may be used to recover a plurality of digital cable television channels from a multichannel analog RF input signal which includes frequencies ranging from about 5 MHz to about 900 MHz.

[0029] Referring now to FIG. 2, each amplifier-filter circuit 111, 112, 113 includes at least an amplifier 201, 203, 205 and a filter 202, 204, 206, respectively. Each of the amplifiers 201, 203, 205 may be a low-noise amplifier (LNA) or other amplifier suitable for use in analog RF front-end applications.

[0030] Each of the filters 202, 204, 206 may be band-pass filters (BPF) or other devices suitable for passing a range or band of frequencies while simultaneously filtering out or attenuating other frequencies outside the range or band. Each of the amplifier-filter circuits 111, 112, 113 may include one or more additional components (not shown) for accomplishing segregation of the analog input signal as described above.

[0031] In addition, each of the filters 202, 204, 206 may include a gain controlled amplifier. In an exemplary embodiment, each of the filters 202, 204, 206 includes a gain control input that allows adjustment of the respective gain of the filter. The system may thus be configured to allow adjustment of the filters to correspond to a range of possible received signal levels from the system while maintaining desirable signal levels at the inputs of the A/D converters. In one embodiment of the invention, a device is provided for comparing an output of the filter to a set-point value and controlling filter gain in a feedback loop.

[0032] Each amplifier-filter circuit 111, 112, 113 should preferably be physically separate and may be configured to amplify a particular range of frequencies without producing substantial intermodulation distortion effects. Alternatively, the amplifier-filter circuits 111, 112, 113 may be co-located in a single package configured to permit processing of signals within each band separately and independently (e.g., substantially free of intermodulation distortion attributable to simultaneous amplification of a wide range of frequencies). The amplifier-filter circuits 111, 112, 113 should preferably be configured to minimize degradation of one or more signal characteristics particularly susceptible to front end effects, such as noise figure, sensitivity, and dynamic range.

[0033] By employing undersampling techniques, various embodiments of the present invention may be economically implemented. As would be understood by one of ordinary skill in the art, the Nyquist criterion is met as long as the bandwidth of a signal is less than half of the sampling frequency. In one embodiment of the invention, each band has a bandwidth of about 300 MHz. Accordingly, each of the

A/D converters 121, 122, 123 can recover a respective target frequency if operated at a sampling frequency of 600 MHz. In addition, since each of the bands has substantially the same bandwidth, a single 600 MHz clock is sufficient to provide a clock frequency for all of the analog-to-digital converters. Consequently, in one embodiment, a single clock device can provide the requisite clock signal for all of the A/D converters. Moreover, the required frequency is not remarkably high, facilitating design and implementation of the clock device.

[0034] Without the use of undersampling the system would require, for example, a first analog-to-digital converter 121 operating with a sampling frequency of about 600 MHz for processing frequencies in a band from about 5 MHz to about 300 MHz , a second analog-to-digital converter 122 operating with a sampling frequency of about 1.2 GHz for processing frequencies in a band between about 300 MHz and about 600 MHz, a third analog-to-digital converter 123 operating with a sampling frequency of about 1.8 GHz, for processing frequencies in a band from about 600 MHz to about 900 MHz, etc.

[0035] In accordance with an aspect of the invention, each analog-to-digital converter 121, 122, 123 may include a frequency selector 211, 212, 213 for setting the sampling frequency and/or input frequency corresponding to the desired band. For example, a first analog-to-digital converter 121 may include a first frequency selector 211 including a clock input coupler on which a clock signal is transmitted, indicating the desired sampling frequency of the first analog-to-digital converter 121. Other forms of communicating a desired sampling frequency of each of the analog-to-digital converters 121, 122, 123 may be utilized in accordance with the present invention, as would be appreciated by one of ordinary skill in the art.

[0036] Each analog-to-digital converter 121, 122, 123 should have resolution and linearity characteristics sufficient for satisfactorily processing digital television signals and associated signals intended for end users in a conventional cable television broadcast system. For example, each analog-to-digital converter 121, 122, 123 may produce from about 1024 to about 65536 discrete values, corresponding to a resolution of 10 (i.e., $2^{10} = 1024$) to 16 (i.e., $2^{16} = 65536$) bits.

[0037] Referring now to FIG. 3, a digital tuner 130 is provided for processing the digital signals converted by the plurality of analog-to-digital converters 121, 122, 123. The digital tuner 130 may include one or more digital multiplexers or demultiplexers

capable of generating a plurality of digital channel signals from the converted digital band signals. The digital tuner 130 may include a multitude of components configured as is well known in the art to recover a plurality of digital channel signals substantially simultaneously using a plurality of separate digital processors or a single digital processor.

[0038] The digital tuner 130 may include a channel selector 315 to permit selection of one or more particular digital channels desired to be recovered. For example, a selected set of digital cable television channels may be communicated to the digital tuner 130 via the channel selector 315 corresponding to a plurality of pay-per-view selections desired by members of a household; the digital tuner 130 may demultiplex only the digital channel signals corresponding to those digital cable television channels. Alternatively, the digital tuner 130 may be configured to demultiplex and recover all of the available digital channel signals.

[0039] It should be appreciated that the digital tuner 130 in accordance with the present invention is not limited to the above-described operations, but the digital tuner 130 may also perform a variety of other processing operations prior to providing digital channel signals suitable for use in each of the demodulation circuits 141, 142, 143. For example, the digital tuner 130 may perform coding, decoding, scrambling, descrambling, rotating, and/or derotating operations prior to passing the digital channel signals to demodulation circuits 141, 142, 143.

[0040] Each of the demodulation circuits 141, 142, 143 may include one or more demodulators 301, 303, 305 and forward-error-correction (FEC) circuitry 302, 304, 306, respectively. Each of the demodulation circuits 141, 142, 143 may include demodulators 301, 303, 305 configured to perform a particular demodulation function or set of functions corresponding to the type of digital content expected to be found within a corresponding digital channel signal. For example, a first demodulator 301 may be configured to perform quadrature amplitude modulation (QAM) demodulation of digital cable television signals; a second demodulator 303 may be configured to perform quadrature phase shift keying (QPSK) demodulation of digital audio signals; and a third demodulator 305 may be configured to perform vestigial sideband (VSB) demodulation of high-definition television (HDTV) signals. Of course, it should be appreciated that more than one of the plurality of demodulation circuits 141, 142, 143

may be configured to perform similar or identical functions or operations on separate digital channel signals substantially simultaneously.

[0041] Forward-error-correction (FEC) circuits 302, 304, 306 may include one or more components configured for coding or decoding, for example a Reed-Solomon decoder. It should be appreciated that each of the demodulation circuits 141, 142, 143 and/or the digital tuner 130 may include circuitry for providing additional functions, for example adaptive filters for removing multi-path propagation effects, co-channel interference, and other types of radio frequency interference (RFI) well known in the art.

[0042] FIG. 4 shows a flow diagram representation of a method of receiving a plurality of digital RF channels generally designated 400 in accordance with an aspect of the present invention. The method 400 includes a separating step 402, a first converting step 403, a second converting step 404, a demultiplexing step 405, a first demodulating step 406, and a second demodulating step 407.

[0043] The method 400 begins at step 401 and proceeds to step 402 in which a multichannel analog RF input signal is separated into a plurality of analog signals including at least first and second analog signals. The first analog signal includes a first band of frequencies and the second analog signal includes a second band of frequencies. It should be appreciated that the input signal may also be separated into at least a third analog signal including a third band of frequencies, and the first, second, and third bands of frequencies may not necessarily be contiguous.

[0044] In step 403, the first analog signal is converted into a first digital signal using a first analog-to-digital converter. In step 404, the second analog signal is converted into a second digital signal using a second analog-to-digital converter independently of the conversion performed in the first analog-to-digital converter. The first and second analog-to-digital converters may convert different frequency bands from analog to digital form, similar to analog-to-digital converters 121, 122, 123 described above with reference to FIGS. 1 and 2, and each should have a sampling frequency of at least twice the bandwidth of the respective frequency band in accordance with the Shannon-Nyquist sampling theorem. The first and second analog-to-digital converters should perform such conversions with resolution and linearity characteristics sufficient for satisfactorily processing digital television signals

and associated signals intended for end users in a conventional cable television broadcast system.

[0045] In step 405, the first digital signal (converted in the first analog-to-digital converter) and the second digital signal (converted in the second analog-to-digital converter) are demultiplexed to generate a plurality of digital RF channel signals including at least first and second digital RF channel signals. Each of the plurality of digital RF channel signals is typically characterized by a different carrier frequency and a bandwidth or range of frequencies assigned to a particular application or type of content to be carried on that channel. It should be apparent that each digital RF channel signal may in turn carry or provide a plurality of data streams, e.g., audio, video, program information, or interactive content.

[0046] In step 406, the first digital RF channel signal is demodulated and forward-error-corrected. In step 407, the second digital RF channel signal is demodulated and forward-error-corrected. Steps 406 and 407 may be accomplished using demodulation circuits 141, 142, 143 described above with reference to FIGS. 1 and 3. However, the present invention is not so limited and steps 406 and 407 may alternatively be accomplished in any of several other ways known in the art, for example demodulation and forward-error correction steps 406 and 407 may be performed within one or more digital processors temporarily or semi-permanently programmed to perform such operations.

[0047] The method then proceeds to step 407, where it ends until another multichannel analog RF input signal is received from which one or more digital RF channels are desired to be recovered.

[0048] As illustrated in the preceding discussion and accompanying figures, the method and apparatus of the present invention represent an improvement in the state of the art for multichannel digital cable receivers and associated methods. The present invention provides a multichannel receiver circuit and method that accomplishes substantially simultaneous reception of a plurality of digital cable television channels at a reasonable cost. These advantages can be embodied in a single digital receiver circuit capable of recovering a wide variety of digital content, and may be configured for use with conventional cable television delivery systems.

[0049] One of skill in the art will appreciate that the invention, as described above, allows a single device to receive a modulated signal at an input and produce

a plurality of video signals, or other information signals, related to the modulated signal. This plurality of video signals may then be received at respective devices such as, for example, a television display device, a PVR device, a videocassette recorder device, or any other appropriate signal receiving device. These devices may be disposed at respective locations which may or may not be remote from one another. Accordingly, for example, a plurality of television receivers, PVR's, or other devices, may be disposed in respective rooms of a house or multi-unit dwelling, in a respective plurality of offices, or in otherwise separated locations while concurrently receiving signals from a common modulated signal input.

[0050] While the invention has been described in detail in connection with the preferred embodiments known at the time, it should be readily understood that the invention is not limited to such disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions, or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. Accordingly, the invention is not to be seen as limited by the foregoing description, but is only limited by the scope of the appended claims.

CLAIMS

1. An apparatus (100), comprising:

first means for processing (111) an input signal comprising signals in a first frequency band and signals in a second frequency band to produce a first analog signal including signals in the first frequency band and substantially excluding the signals in the second frequency band;

second means for processing (112) the input signal comprising signals in a first frequency band and signals in a second frequency band to produce a second analog signal including signals in the second frequency band and substantially excluding the signals in the first frequency band;

a first analog-to-digital converter (121) for processing the first analog signal to produce a first digital signal representing the signals in the first frequency band;

a second analog-to-digital converter (122) for processing the second analog signal to produce a second digital signal representing the signals in the second frequency band; and

a means for processing (130) the first and second digital signals to simultaneously produce a first output signal representing a first digital channel included in the first frequency band and a second output signal representing a second digital channel included in the second frequency band.

2. The apparatus (100) of claim 1 further comprising a third amplifier-filter circuit (113) configured to process signals within a third frequency band and a third analog-to-digital converter (121) configured generate a third digital signal comprising a representation of said processed signals within said third frequency band.

3. The apparatus (100) of claim 2 wherein said first frequency band includes frequencies from about 5 MHz to about 300 MHz, said second band includes frequencies between about 300 MHz and about 600 MHz, and said third band includes frequencies from about 600 MHz to about 900 MHz.

4. The apparatus (100) of claim 3 wherein said first second and third analog-to-digital converters (121, 122, 123) have sampling frequencies of at least 600 MHz.

5. The apparatus (100) of claim 3 wherein said first second and third analog-to-digital converters (121, 122, 123) are configured for an input frequency of up to about 900 MHz.

6. The apparatus (100) of claim 1 wherein the digital processor (130) includes a frequency selector for selecting a desired sampling frequency.

7. The apparatus (100) of claim 1 wherein each of said first, second, and third analog-to-digital converters (121, 122, 123) have a resolution of at least about 10 bits.

8. The apparatus (100) of claim 1 wherein each of said first, second, and third analog-to-digital converters (121, 122, 123) have a resolution from about 10 to about 16 bits.

9. The apparatus (100) of claim 1 wherein said digital processor (130) is configured to recover substantially all signals with said first and second frequency bands.

10. The apparatus (100) of claim 1 wherein said digital processor (130) is configured to recover a selected set of signals with said first and second frequency bands.

11. The apparatus (100) of claim 10 wherein said digital processor (130) is configured to recover said selected set of signals with said first and second frequency bands substantially simultaneously.

12. The apparatus (100) of claim 1 further comprising a first demodulator circuit (141) coupled to said digital processor (130) and a second demodulator circuit (142) coupled to said digital processor (130).

13. The apparatus (100) of claim 12 wherein said first and second demodulator circuits (141, 142) include circuitry configured for forward error correction (302, 304, 306).

14. The apparatus (100) of claim 12 where said digital processor (130) multiplexes said first, second, and third digital signals, downconverts said multiplexed signal and extracts desired information to be coupled to said first and second demodulator circuits (141, 142).

15. The apparatus (100) of claim 12 where said digital processor (130) downconverts and extracts desired information to be coupled to said first and second demodulator circuits (141, 142) from each of said first, second, and third digital signals individually.

16. The apparatus (100) of claim 1 wherein said apparatus (100) processes frequencies between about 5 MHz and about 900 MHz.

17. The apparatus (100) of claim 1 wherein apparatus (100) processes cable television channels.

18. A method (400) processing signals comprising the steps of:

(a) separating an input signal into a first analog signal and a second analog signal;

(b) digitizing said first analog signal to generate a first digital signal;

(c) digitizing said second analog signal to generate a second digital signal;

(d) downconverting said first digital signal and said second signal; and

(e) extracting desired television program information from said downconverted first digital signal and said second digital signal.

19. The method (400) of claim 18, further comprising the steps of:

(a) demodulating (406, 407) said extracted television program information;

(b) forward-error-correcting (406, 407) said extracted television program information;

20. The method (400) of claim 18 further comprising the steps of:

(a) multiplexing said first digital signal and said second digital signal after said digitizing steps and before said downconverting step.

21. The method (400) of claim 18 further where said downconverting step comprises downconverting each of said first and second set of signals individually.

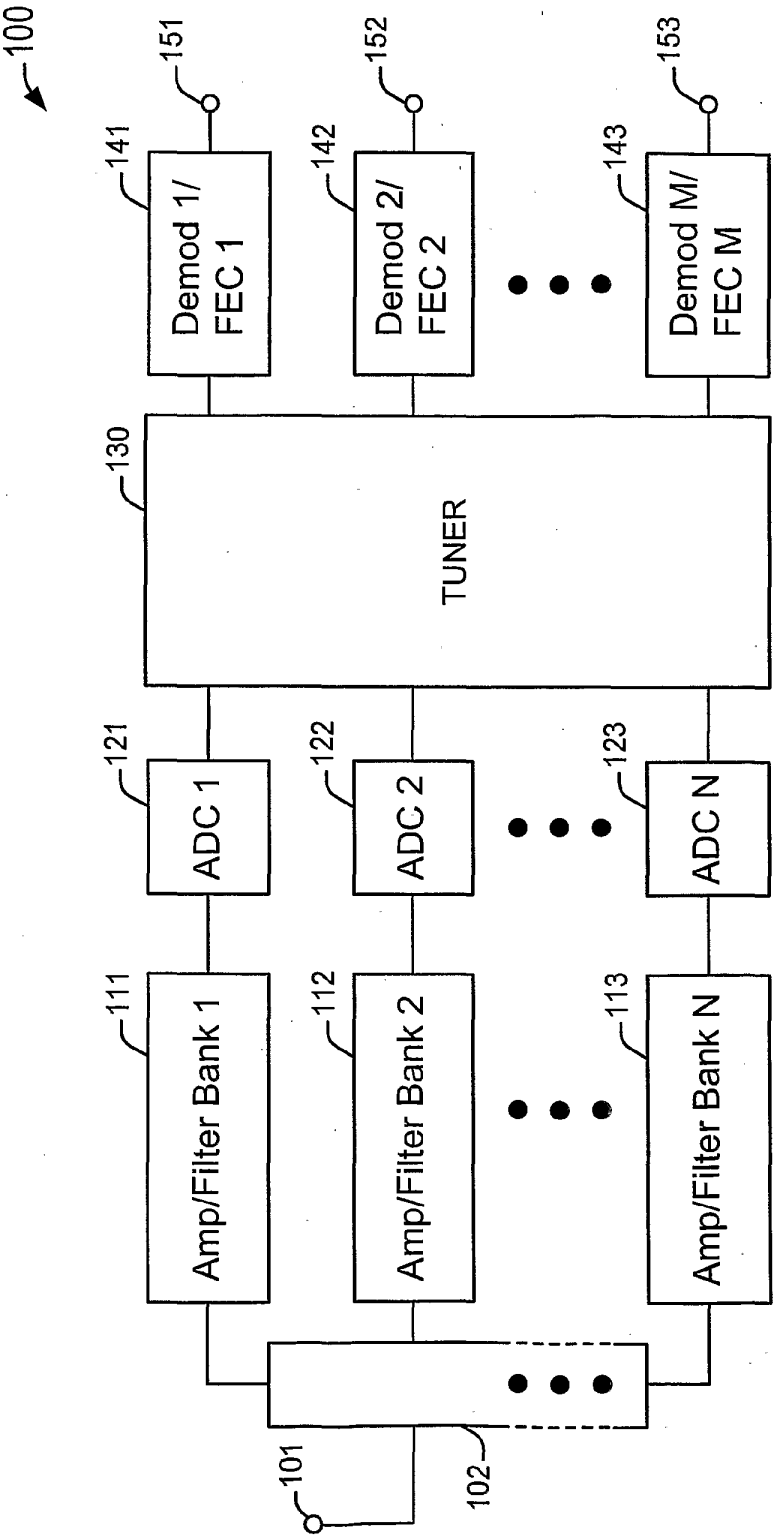

100
151
152
153
141
142
143
Demod 1/ FEC 1
Demod 2/ FEC 2
Demod M/ FEC M
130
TUNER
121
122
123
ADC 1
ADC 2
ADC N
111
112
113
Amp/Filter Bank 1
Amp/Filter Bank 2
Amp/Filter Bank N
101
102

FIG. 1

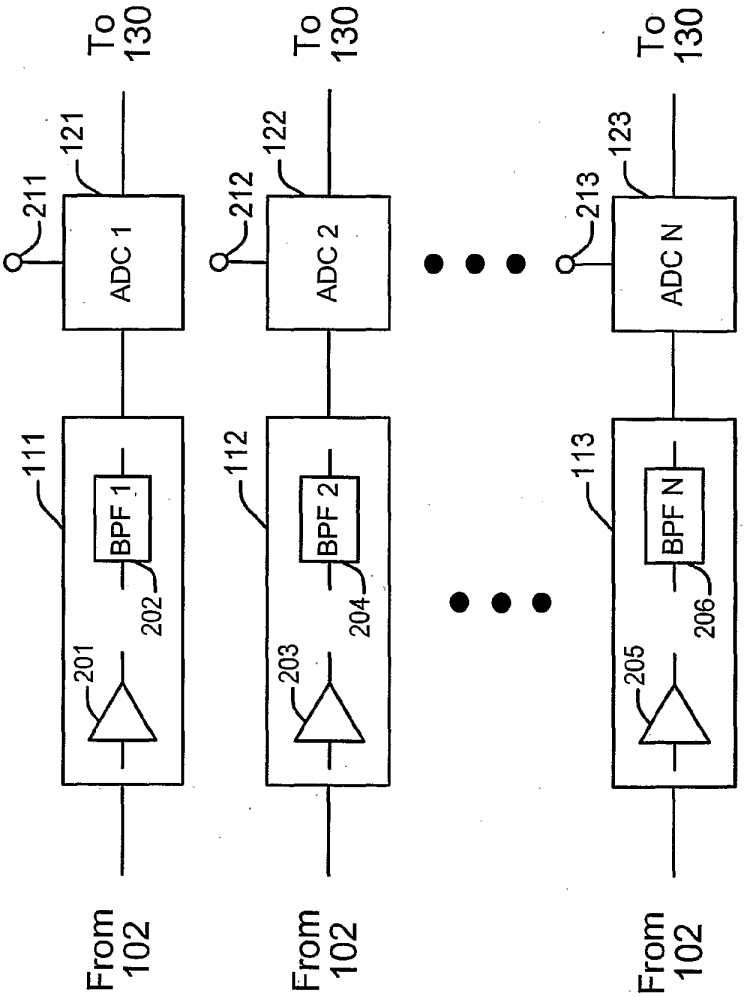

From 102
From 102
From 102
111
112
113
BPF 1
BPF 2
BPF N
201
202
203
204
205
206
211
212
213
ADC 1
ADC 2
ADC N
121
122
123
To 130
To 130
To 130

FIG. 2

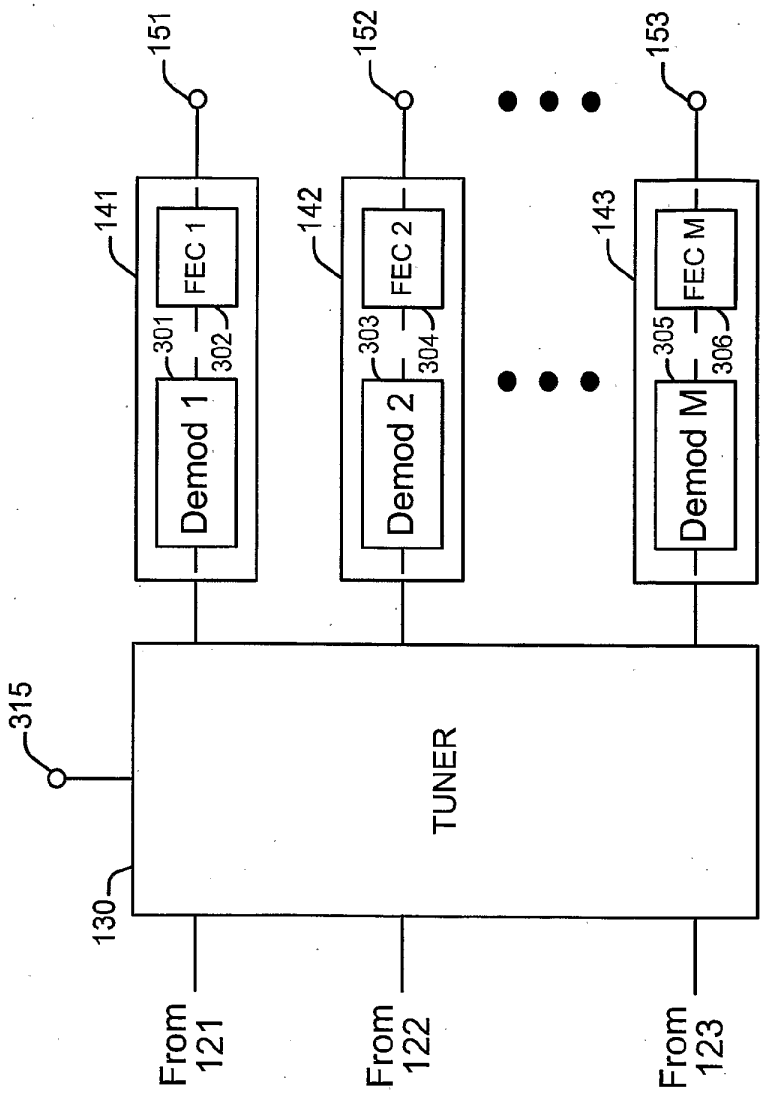

151
152
153
141
142
143
FEC 1
FEC 2
FEC M
301
302
303
304
305
306
Demod 1
Demod 2
Demod M
315
TUNER
130
From 121
From 122
From 123

FIG. 3

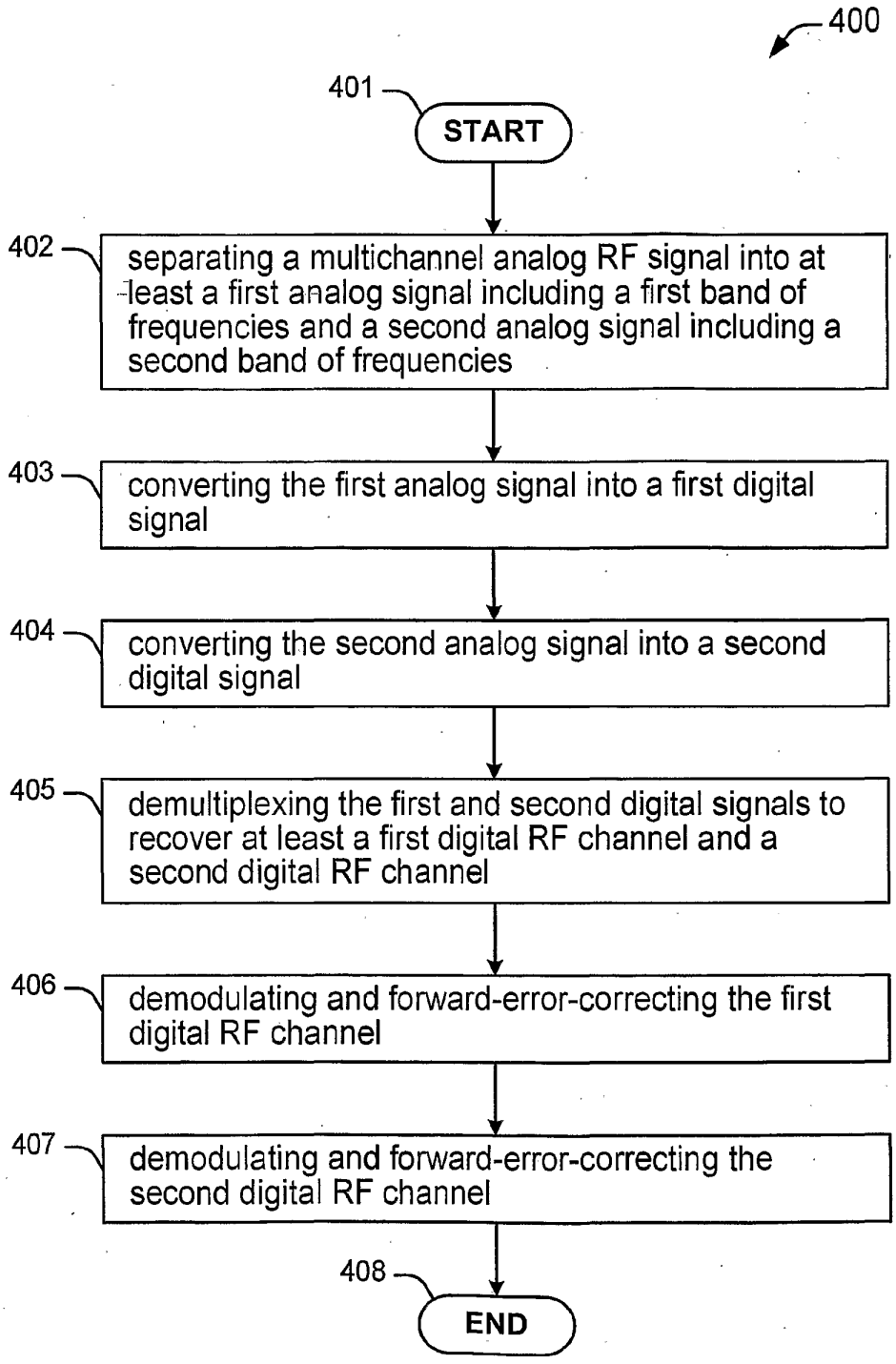

400
401
START
402
separating a multichannel analog RF signal into at least a first analog signal including a first band of frequencies and a second analog signal including a second band of frequencies
403
converting the first analog signal into a first digital signal
404
converting the second analog signal into a second digital signal
405
demultiplexing the first and second digital signals to recover at least a first digital RF channel and a second digital RF channel
406
demodulating and forward-error-correcting the first digital RF channel
407
demodulating and forward-error-correcting the second digital RF channel
408
END

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/023664

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N5/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/204034 A1 (HANRAHAN ROBERT MASON [US]) 14 October 2004 (2004-10-14)	1,2, 9-12,14, 15,17, 18,20,21
Y	the whole document	3-8,13, 16,19
Y	WO 01/20792 A1 (SARNOFF CORP [US]; MALKEMES ROBERT [US]) 22 March 2001 (2001-03-22) page 4, line 19 - page 5, line 27 page 6, line 29 page 8, line 16 - line 22	3-8,16
Y	US 2005/012869 A1 (AKIYAMA TOSHIFUMI [JP]) 20 January 2005 (2005-01-20) figures 4,5	13,19

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
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"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 February 2007	26/02/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Yvonnet, Joel

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/023664

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005/190777 A1 (HESS KENDAL M [US] ET AL) 1 September 2005 (2005-09-01) figures 6,7	1,18
A	US 5 068 918 A (VERHEIJEN PAULUS A M [NL] ET AL) 26 November 1991 (1991-11-26) column 3, line 20 - line 26	1,18

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2006/023664

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		NL 8901460 A	02-01-1991

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
90/019,255	**09/20/2023 02:38:27 PM ET**	**50348.106**

Title of Invention

WIDEBAND TUNER ARCHITECTURE

Application Information

APPLICATION TYPE	Utility / ex parte reexam	PATENT #	9210362
CONFIRMATION #	5785	FILED BY	Krista Myrick
PATENT CENTER #	62831599	AUTHORIZED BY	Raghav Bajaj
CUSTOMER #	23446	FILING DATE	-
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Madhukar Reddy

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
DA / 506990	**E20239JE39175349**	**Krista Myrick**

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1812	REQUEST FOR EX PARTE REEXAM-NON-STREAMLINED	12600.00	1	12600.00
			TOTAL AMOUNT:	**$12,600.00**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C.

371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Exhibit 1012

"RF CMOS Mixer Design and Optimization for Wideband CDMA Application," Li et al., IEEE 2000.

Customer No.: 000027683

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RF CMOS MIXER DESIGN AND OPTIMIZATION FOR WIDEBAND CDMA APPLICATION

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ABSTRACT

This paper presents the design of a Gilbert downconversion mixer for wideband CDMA application. The mixer is designed using a 0.18um 1.5V/3.3V dual-voltage digital CMOS technology. Design methodology is presented to achieve high linearity and low noise figure. A design flow is introduced targeting the automatic design and optimization for mixers.

I. INTRODUCTION

An important driving force in RF ICs development is the pursuing of single-chip integrated RF CMOS transceivers. Compared with GaAs, Bipolar and BiCMOS, CMOS is the most affordable technology. Most of digital systems such as microprocessor and DSP are designed using CMOS technology. Therefore, full integration of RF transceivers in CMOS technology means the possibility of integrating a whole system such as a cellular phone in a single chip. This can greatly reduce system design cost, system volume, as well as power consumption, all of which are highly desirable in today's portable systems.

Downconversion mixer is one of the important building blocks for RF transceivers in wireless communications. Modern wireless communication standards such as GSM, CDMA, DECT, GPS, as well as the under going Bluetooth, demands high performance RF front ends, which are very often constrained by the achievable power gain, noise figure and linearity of the low noise amplifier (LNA) and downconversion mixers. Particularly, many design challenges exist when these RF blocks and a whole transceiver are to be implemented in CMOS process.

This paper presents the design of a Gilbert cell mixer for the wideband CDMA application at the 2.4 – 2.48 GHz ISM band, targeting the full integration of a direct downconversion transceiver. Section II briefly presents the direct downconversion transceiver and the gilbert cell mixer, followed by the discussion of noise performance estimation in section III. Section IV describes the design procedure, which is part of our goal to seek a systematic flow for mixer design and optimization. Finally, we make our conclusions in section V.

This work was supported in part by TI Fellowship

II. CIRCUIT DESCRIPTION

A. Direct downconversion transceiver

Among different transceiver topologies, the direct downconversion (or homodyne) transceiver stucture as shown in Fig. 1 is a good candidate for fully integrated transceivers, since it eliminates the image rejection filter and IF filters which are bulky but necessary in a conventional heterodyne transceiver. A major drawback that limits the wide application of direct downconversion transceivers is DC offset resulting from LO leakage and self-mixing. Specifically, the LO signal of a mixer can leak to the RF port and is returned by the preceding LNA and the antenna. The returned signal then mixes with the LO signal, generating a DC offset voltage that is often large enough to saturate subsequent stages including VGA, ADC, and etc. Extra design effort is required to alleviate the DC offset problem. In our specific case for the wideband CDMA application in the frequency range of 2.4 – 2.48 GHz, signal is spread over a 32 MHz bandwidth through pesudo random sequences. By adopting differential coding scheme, the DC component in the downconverted signal does not contain useful information at all. The bandpass filters in Fig. 1 after the mixer can then serve to remove the DC offset. The lower high-pass conner frequency of the bandpass filters is around 1 to 2 kHz, which further removes flicker noise generated by the LNA and the mixer. Meanwhile, because useful information is spread over a wide frequency band, the relatively very small high-

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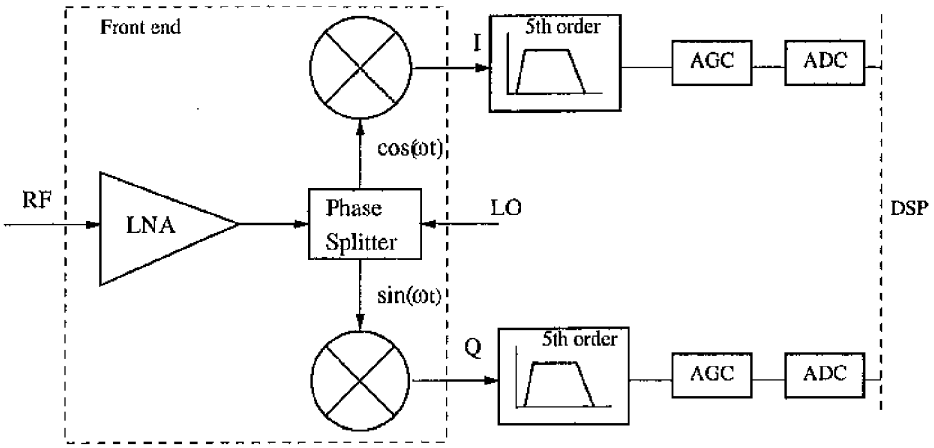


Figure 1: Direct downconversion transceiver

pass conner frequency of the band-pass filter will not seriously degrade system performance.

B. Gilbert mixer

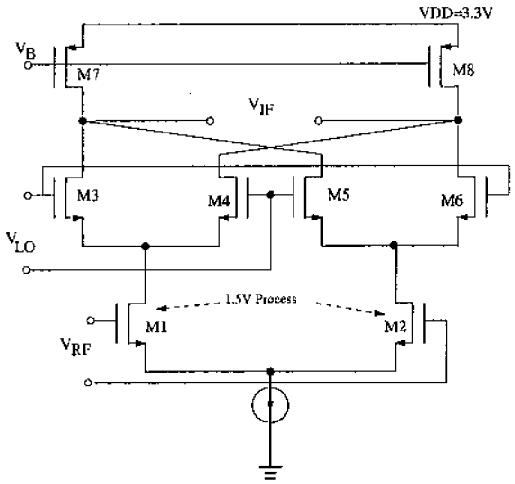


Figure 2: The Gilbert cell

Shown in Fig. 2 is the commonly used Gilbert mixer. Transistors M1-2 form the input transconductors, which convert input RF voltage signal into current signal. Transistors M3-6 are commutating switches, which are turned on and off by the LO signal, accordingly, current signals from the transconductors are delivered to different branches. The net effect of the switching activities is that the RF current signals are multiplyed with the LO signals. Transistors M7-8 serve as active loads. The differential IF output signal is acquisited from these two loads. Fig. 3 demonstrates the downconversion process.

Since the Gilbert mixer is fully differential, any common mode high frequency signals from the LO and RF ports will be substracted at the output. The mixer is expected to have very good RF-to-IF and LO-to-IF isolation performance. In addition, any second order harmonics at the two IF output ports are canceled by the differential output. Note that such quality greatly depends on the switching behavior and transistors working region.

As is well-known, the drain-source current is generally the square of the gate-source voltage for long-channel MOS transistors. The transconductors M1-2 used here hence present nonlinearity when converting input RF voltage signal to current signal. The nonlinearity causes intermodulation. When two signals with close frequencies pass a nonlinear device, the output will contain series of high order harmonics and intermodulation products. Among them, the 2nd and 3rd intermodulation products are of our concern, since they can mix with the LO signal and generate sideproducts which are in the IF frequency band, resulting in signal distortion. Various methods such as source degeneration or translinear loop [2] are used to improve the linearity of the transconductors. We will address this issue later on in this section.

The tail current of the gilbert cell is supplied by a well-known wide-swing current mirror [1] as shown in Fig. 4. The cascaded transistors can provide a nearly constant tail current, while the current of a regular single-stage current mirror will vary over a wide range when its drain source voltage changes. A

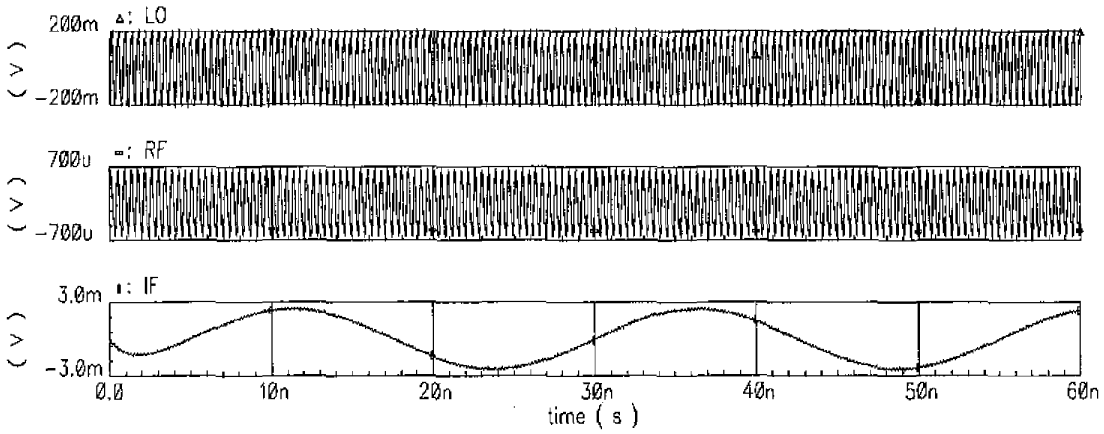


Figure 3: Down mixing with $f_{RF} = 2.4$ G, , $f_{LO} = 2.44$ G

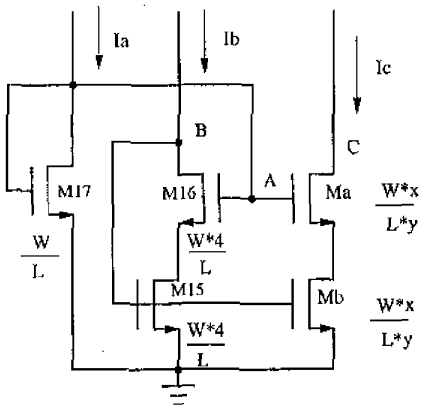


Figure 4: The wide swing current mirror

constant current is desirable because it will simplify the design procedure as will be evidenced in section IV. The wide-swing current mirror is used because its overhead voltage is minimum, namely, the source voltage of the tranconductors M1-2 in Fig. 2 is kept as small as possible. This overhead voltage can be made smaller by using larger transitor aspect ratio (W/L) for the current mirror, since the transistors' effective voltage is reduced with large aspect ratio.

Note that the rail to rail chain now has 5 transistors cascaded, a structure unsuitable for low voltage operation. The CMOS technology used in this design supports dual-voltage, 1.5V and 3.3V respectively, with 0.18 μm minimum length for 1.5V process and 0.34 μm for 3.3V process. We adopt the 3.3V supply voltage. Since the I-V characteristics of CMOS transistors is more linear at short channel length [4], we use the 1.5V process for the two transconductor transistors (M1-2) such that the 0.18 μm minimum channel length can be adopted. The use of minumum channel length for M1-2, does resulting larger flicker noise as clarified in the next section, however, flicker noise is not a serious problem in this application as the bandpass filters after the mixer will suppress it considerably.

III. FIRST-ORDER NOISE ESTIMATION

The design of mixers is a trade-off of many performance specification including conversion gain, noise figure and linearity. Particularly, while conversion gain can be roughly estimated from the conversion gain of the transconductors and the output impedance,

and linearity can be achieved by a few methods as pointed previously, no prior knowledge is available that leads to the satisfactory design of noise figure. In the following discussion we seek to gain some insight about noise performance of mixers.

Noise figure is affected when we scale the sizes of M1-8. The actual noise mechanism of the mixer is hard to describe analytically. We attempt to understand the noise in such a way [3]:

- Baseband noise from M3-8 directly contributes to the output without the need to consider frequency mixing.
- Baseband noise from M1-2 also directly contributes to the output. To understand this, one just needs to notice that M3-M5, and M4-M6 always form a path from M1 or M2 to the IF ports.
- Noise at different band mixes with LO signal and its harmonics and is downconverted to baseband [5].

We further notice that due to the balanced structure of the mixer, noise from the biasing circuitry of M7-8, and from the current mirror that supplies the tail current is canceled out at the differential output.

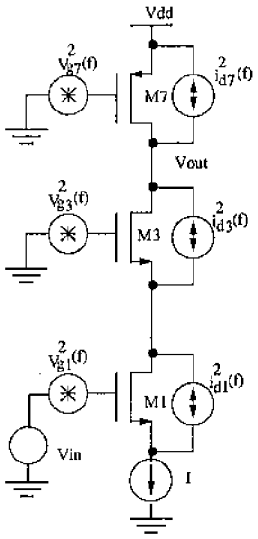


Figure 5: Noise model of the Gilbert cell

To investigate the noise behavior with regard to the transistor geometry, we simplfy the problem and look at only the signal path formed by M1, M3, and M7. The equavalent noise model is illustrated in figure 5. We first assume that all three transistors working in active region (This assumption is true when LO signal are in transtion and can be true when LO amplitude is moderate but still effectively turns on and off the commutating switches.).

Without lengthy derivation, input referred flicker noise is given by

$$\begin{aligned} v_{in,f}^2 &= v_{g1,in}^2 + v_{g3,in}^2 + v_{g7,in}^2 \\ &= v_{g1}^2 + v_{g3}^2 \frac{(\frac{I}{\lambda_n L_1})^2}{g_{m1}^2} + v_{g7}^2 \frac{g_{m7}^2}{g_{m1}^2} \\ &= \frac{K}{W_1 L_1 f} + \frac{K}{W_3 L_3 f} \frac{(\frac{I}{\lambda_n L_1})^2}{2\mu_n C_{ox} \frac{W_1}{L_1} I} \\ &\quad + \frac{K}{W_7 L_7 f} \frac{2\mu_p C_{ox} \frac{W_7}{L_7} I}{2\mu_n C_{ox} \frac{W_1}{L_1} I} \\ &= \frac{K_1}{W_1 L_1 f} + \frac{K_2 I}{W_1 L_1 W_3 L_3 f} + \frac{K_3 L_1}{W_1 L_7^2} \end{aligned} \quad (1)$$

where K_1, K_2, K_3 are process dependent constants.

The input-referred thermal noise is given by

$$\begin{aligned} v_{in,t}^2 &\simeq \frac{i_{d1}^2}{g_{m1}^2} + \frac{i_{d3}^2 r_{ds3}^2}{g_{m1}^2 (r_{ds1} + r_{ds3} + r_{ds7})^2} + \frac{i_{d7}^2 r_{ds7}^2}{g_{m1}^2 r_{ds1}} \\ &\simeq \frac{4kT\frac{2}{3}g_{m1}}{g_{m1}^2} + \frac{4kT\frac{2}{3}g_{m3}}{g_{m1}^2} + \frac{4kT\frac{2}{3}g_{m7}(\frac{\lambda_p L_7}{I})^2}{g_{m1}^2(\frac{\lambda_n L_1}{I})^2} \\ &= K_4 \frac{\sqrt{L_1}}{\sqrt{W_1 I}} + K_5 \frac{L_1\sqrt{W_3}}{W_1\sqrt{L_3 I}} + K_6 \frac{\sqrt{W_7 L_7 L_7}}{W_1 L_1 \sqrt{I}} \end{aligned} \quad (2)$$

where K_4, K_5, K_6 are also process dependent constants.

In situation when M3 possiblly works in triode region (M1 and M7 still in active region). Noise terms contributed by M1 and M7 are still valid in equation (1) and (2). However, by first order approximation, the filcker noise of M3 doesnot have much influence on $V_{in,f}^2$ and can be ignored from equation (1). The input referred thermal noise from M3, is now given by the following equation (in the calculation, thermal noise contributed by M3 is simplely that of a resitor of r_{ds3})

$$\begin{aligned} v_{in,t3}^2 &= \frac{I_n^2 r_{ds3}^2}{g_{m1}^2 r_{ds1}^2} \\ &= \frac{\frac{4kT}{\mu C_{ox}\frac{W_3}{L_3}(V_{gs3}-V_t)}}{2\mu C_{ox}\frac{W_1}{L_1} I (\frac{\lambda_n L_1}{I})^2} \\ &= K5 \frac{L_3 I}{W_3 W_1 L_1 (V_{gs3} - V_t)} \end{aligned} \quad (3)$$

These equations give an intuitive feeling of transistor sizing. They are used in the initial design process. As we nomally expect all the transistors M1, M3, M7 work in saturation region, and we also pointed out that flicker noise are handled by the high-pass filtering, equation 2 therefore is of our primary interest. From equation 2 we expect large W_1/L_1, small W_3/L_3 and small $W_7 \cdot L_7$. However, it should be reminded that this model doesnot take 2nd and higher order parasitic effect into consideration, and it is derived from long channel MOS models.

IV. MIXER DESIGN AND OPTIMIZATION

While it is difficult to automate the design flow for the Gilbert mixer, we attempt to systemize the flow in this section.

A current mirror described previously that provides a relatively constant current over a large voltage range is first constructed. Two design parameters are of our concern, the tail current, which directly determines the conversion gain, and the minimum overhead voltage, below which the tail current will vary noticeably. If any factors in one part of the mixer cause the tail current to vary in big magnitude, parameters predetermined for other parts of the mixer will depart from original design considerably, making the design complicated. The tail current is roughly estimated at initial design stage.

The current (allowing a certain range) and the minmum overhead voltage is then utilized to determine the transistor size and DC bias of the transconductor. The goal in this step is to ensure that the transistor works in saturation region, given a certain variation range for its drain voltage. As discuss in previous sections, noise figure, conversion gain, and linearity are all related to the sizes of the transcondutor transistors. Conversion gain and linearity are major consideration initially, but noise figure should be refined later.

The variation range of the drain voltage of the transconductors is determined by taking in account the variation caused by the LO switching activities. It is now time to determine the LO bias voltage and the size of the commutating switches. According to equation 2, the aspect ratio of the switches should be small, while with the predetermined tail current, the aspect ratio is expected to be larger such that the residue gate-source voltage of the switches is small enough. Small residue gate-source voltage requires small LO amplitude to effectively turn on and off the switches, which reduces LO power consumption and makes the

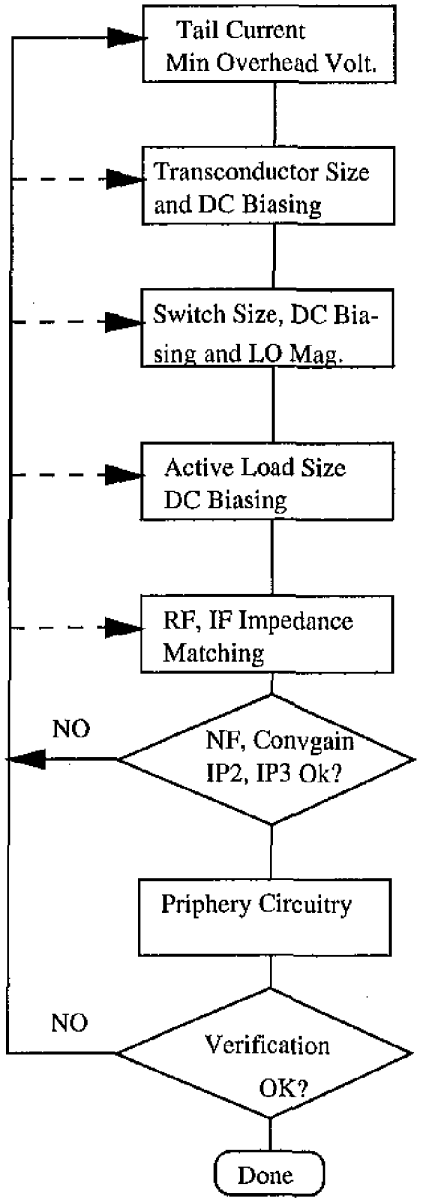


Figure 6: Gilbert cell design flow

switches more ideal. Nonideal switching behavior, that is, the switches are not completely turned on or off, will reduce the conversion gain, and possibly generates more noise. Similar to the transconductors, the switches are designed to work in saturation region, taking the variation of gate source voltage, the variation of the tail current, and the variation of the drain voltage into consideration. Note that the preferred variation range of the drain voltage of the switches is much larger than that of the transconductors, mainly because we want the IF signal to vary over a large voltage range without causing distortion.

Subsequently, the biasing voltage and the transistor sizes of the active loads can be determined. Again, make sure that the active loads operate in saturation region and provide reasonable variation range for the IF signal.

The matching network of the RF port and IF port can now be determined for maximum power transmission. In case noise performance cannot be satisfied, the RF port should be matched for optimal noise figure.

Conversion gain and noise figure, and intermodulation are now obtained. If any of them is not satisfactory, the above procedures are repeated with the adjustment of the tail current and transistor sizes.

These steps form the design flow of the Gilbert cell (Fig. 6). Further peripheral circuitry such as biasing network and common mode feedback is necessary to form a functional mixer, but that will not influence the mixer performance significantly.

As described above, the design procedure of a mixer is particularly time consuming and complicated. While it is hard to automate the whole procedure, each step of the design flow is simply an issue of optimization.

V. CONCLUSIONS

A Gilbert-cell mixer is implemented and will be fabricated in a 0.18 μm dual-voltage (1.5/3.3) CMOS process. A simplified noise analysis model in first order is presented which allows the estimation of noise contribution by each transistors. Dual-voltage process is utilized in the design for better linearity, specifically, short channel length (0.18 μm/1.5V process) is adopted for the transconductors while the mixer operates at 3.3V. A systematic mixer design flow, along with corresponding design considerations, is introduced in an effort to automate the design procedure.

A conversion gain of 12 dB, input referred IP3 of 5 dBm, and noise figure of 11 dB are obtained in simulation.

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Exhibit 1007

Claim Construction Memorandum and Order, *Entropic Communications, LLC v. Charter Communications, LLC*, Case 2:220-cv-00125-JRG, Dkt. 123 (June 26, 2023)

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THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

ENTROPIC COMMUNICATIONS, LLC,	§	
	§	
Plaintiff,	§	
	§	
v.	§	CASE NO. 2:22-CV-00125-JRG
	§	
CHARTER COMMUNICATIONS, INC.,	§	
	§	
Defendant.	§	
	§	
	§	

CLAIM CONSTRUCTION
MEMORANDUM OPINION AND ORDER

Before the Court is the Opening Claim Construction Brief (Dkt. No. 97) filed by Plaintiff Entropic Communications, LLC ("Plaintiff" or "Entropic"). Also before the Court are the Responsive Claim Construction Brief (Dkt. No. 104) filed by Defendant Charter Communications, Inc. ("Defendant" or "Charter") and Plaintiff's reply (Dkt. No. 110). The Court held a hearing on June 13, 2023.

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I. BACKGROUND

Plaintiff alleges infringement of United States Patents No. 8,223,775 ("the '775 Patent"), 8,792,008 ("the '008 Patent"), 9,825,826 ("the '826 Patent"), 8,284,690 ("the '690 Patent"), 9,210,362 ("the '362 Patent"), and 10,135,682 ("the '682 Patent") (collectively, the "patents-in-suit"). (Dkt. 97, Exs. 1–6.)

II. LEGAL PRINCIPLES

It is understood that "[a] claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention." *Burke, Inc. v. Bruno Indep. Living Aids, Inc.*, 183 F.3d 1334, 1340 (Fed. Cir. 1999). Claim construction is an issue of law for the court to decide. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970–71 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996).

"In some cases, however, the district court will need to look beyond the patent's intrinsic evidence and to consult extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period." *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 841 (2015) (citation omitted). "In cases where those subsidiary facts are in dispute, courts will need to make subsidiary factual findings about that extrinsic evidence. These are the 'evidentiary underpinnings' of claim construction that we discussed in *Markman*, and this subsidiary factfinding must be reviewed for clear error on appeal." *Id.* (citing 517 U.S. 370).

To ascertain the meaning of claims, courts look to three primary sources: the claims, the specification, and the prosecution history. *Markman*, 52 F.3d at 979. The specification must contain a written description of the invention that enables one of ordinary skill in the art to make and use the invention. *Id.* A patent's claims must be read in view of the specification, of which

they are a part. *Id.* For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. *Id.* "One purpose for examining the specification is to determine if the patentee has limited the scope of the claims." *Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000).

Nonetheless, it is the function of the claims, not the specification, to set forth the limits of the patentee's invention. Otherwise, there would be no need for claims. *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). The patentee is free to be his own lexicographer, but any special definition given to a word must be clearly set forth in the specification. *Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1388 (Fed. Cir. 1992). Although the specification may indicate that certain embodiments are preferred, particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. *Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994).

This Court's claim construction analysis is substantially guided by the Federal Circuit's decision in *Phillips v. AWH Corporation*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). In *Phillips*, the court set forth several guideposts that courts should follow when construing claims. In particular, the court reiterated that "the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Id.* at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To that end, the words used in a claim are generally given their ordinary and customary meaning. *Id.* The ordinary and customary meaning of a claim term "is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1313. This principle of patent law flows naturally from the recognition that

inventors are usually persons who are skilled in the field of the invention and that patents are addressed to, and intended to be read by, others skilled in the particular art. *Id.*

Despite the importance of claim terms, *Phillips* made clear that "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.* Although the claims themselves may provide guidance as to the meaning of particular terms, those terms are part of "a fully integrated written instrument." *Id.* at 1315 (quoting *Markman*, 52 F.3d at 978). Thus, the *Phillips* court emphasized the specification as being the primary basis for construing the claims. *Id.* at 1314–17. As the Supreme Court stated long ago, "in case of doubt or ambiguity it is proper in all cases to refer back to the descriptive portions of the specification to aid in solving the doubt or in ascertaining the true intent and meaning of the language employed in the claims." *Bates v. Coe*, 98 U.S. 31, 38 (1878). In addressing the role of the specification, the *Phillips* court quoted with approval its earlier observations from *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998):

> Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.

Phillips, 415 F.3d at 1316. Consequently, *Phillips* emphasized the important role the specification plays in the claim construction process.

The prosecution history also continues to play an important role in claim interpretation. Like the specification, the prosecution history helps to demonstrate how the inventor and the United States Patent and Trademark Office ("PTO") understood the patent. *Id.* at 1317. Because the file history, however, "represents an ongoing negotiation between the PTO and the applicant,"

it may lack the clarity of the specification and thus be less useful in claim construction proceedings. *Id.* Nevertheless, the prosecution history is intrinsic evidence that is relevant to the determination of how the inventor understood the invention and whether the inventor limited the invention during prosecution by narrowing the scope of the claims. *Id.*; *see Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1350 (Fed. Cir. 2004) (noting that "a patentee's statements during prosecution, whether relied on by the examiner or not, are relevant to claim interpretation").

Phillips rejected any claim construction approach that sacrificed the intrinsic record in favor of extrinsic evidence, such as dictionary definitions or expert testimony. The *en banc* court condemned the suggestion made by *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002), that a court should discern the ordinary meaning of the claim terms (through dictionaries or otherwise) before resorting to the specification for certain limited purposes. *Phillips*, 415 F.3d at 1319–24. According to *Phillips*, reliance on dictionary definitions at the expense of the specification had the effect of "focus[ing] the inquiry on the abstract meaning of words rather than on the meaning of claim terms within the context of the patent." *Id.* at 1321. *Phillips* emphasized that the patent system is based on the proposition that the claims cover only the invented subject matter. *Id.*

Phillips does not preclude all uses of dictionaries in claim construction proceedings. Instead, the court assigned dictionaries a role subordinate to the intrinsic record. In doing so, the court emphasized that claim construction issues are not resolved by any magic formula. The court did not impose any particular sequence of steps for a court to follow when it considers disputed claim language. *Id.* at 1323–25. Rather, *Phillips* held that a court must attach the appropriate weight to the intrinsic sources offered in support of a proposed claim construction, bearing in mind the general rule that the claims measure the scope of the patent grant.

The Supreme Court of the United States has "read [35 U.S.C.] § 112, ¶ 2 to require that a patent's claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910, 134 S. Ct. 2120, 2129 (2014). "A determination of claim indefiniteness is a legal conclusion that is drawn from the court's performance of its duty as the construer of patent claims." *Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342, 1347 (Fed. Cir. 2005) (citations and internal quotation marks omitted), *abrogated on other grounds by Nautilus*, 572 U.S. 898. "Indefiniteness must be proven by clear and convincing evidence." *Sonix Tech. Co. v. Publ'ns Int'l, Ltd.*, 844 F.3d 1370, 1377 (Fed. Cir. 2017).

III. AGREED TERMS

In their April 4, 2023 P.R. 4-3 Joint Claim Construction and Prehearing Statement, the parties submitted the following agreed-upon constructions (Dkt. No. 84, at 1):

Term	Construction
"the cable modem engine configured to enable upgrades to its software in a manner that is independent of upgrades to the software of the data networking engine" ('775 Patent, Claim 18)	Plain and ordinary meaning
"downstream PDU packets" ('775 Patent, Claim 18)	Plain and ordinary meaning
"parameters" ('690 Patent, Claims 1, 9)	Plain and ordinary meaning
"associated with [the] generation and transmission of [a/the] probe" ('690 Patent, Claim 1)	Plain and ordinary meaning
"wideband analog-to-digital converter (ADC) module"	Plain and ordinary meaning

('362 Patent, Claim 1)	

IV. DISPUTED TERMS IN U.S. PATENT NO. 8,223,775

The '775 Patent, titled "Architecture for a Flexible and High-Performance Gateway Cable Modem," issued on July 17, 2012, and bears a filing date of September 30, 2003. The Abstract of the '775 Patent states:

> A cable modem system and architecture. A cable modem engine performs all cable modem functions, and a data networking engine performs all data and home networking functions. The cable modem engine is completely partitioned from the data networking engine. DOCSIS and VoIP functionality is implemented in the cable modem engine. The VoIP functionality may be in accordance with the Packet-Cable specification. The data networking functionality provided by the data networking engine may be in accordance with the CableHome specification.

1. "a data networking engine implemented in a first circuit that includes at least one processor . . ." and "a cable modem engine implemented in a second circuit that includes at least one processor . . ."

"a data networking engine implemented in a first circuit that includes at least one processor . . ." ('775 Patent, Claim 18)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Indefinite
"a cable modem engine implemented in a second circuit that includes at least one processor . . ." ('775 Patent, Claim 18)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Indefinite

(Dkt. No. 84, at A-1; Dkt. No. 97, at 6; Dkt. No. 104, at 4; Dkt. No. 115, Ex. A, at 1.)

(a) The Parties' Positions

Plaintiff argues that "data networking" and "cable modem" were well-known phrases at the time of the invention and that the generic word "engine," as modified by the phrases "data networking" and "cable modem," would have been readily understood by a person of ordinary skill in this art. (Dkt. No. 97, at 6–7.) Plaintiff also argues that Defendant's indefiniteness arguments should be rejected because "electrical engineers routinely design subcomponents of consumer electronics, even if the components reside on the same chip," and "[a] POSITA would have no trouble determining where one circuit begins and another ends, because integrating functional blocks on 'a chip' does not render them indistinguishable." (*Id.*, at 8.)

Defendant responds that "[t]here is no disclosure of a DNE or CME implemented in any circuit, much less two circuits which are 'separate' from one another." (Dkt. No. 104, at 5.) Defendant argues that Plaintiff cannot simply chose whatever meaning or "level" of the word "circuit" suits its infringement contentions. (*See id.*, at 6–8.)

Plaintiff replies that the term "circuit" is readily understandable and that the specification discloses separation of functions. (Dkt. No. 110, at 1.)

At the June 13, 2023 hearing, Plaintiff argued that although the functionality of the first circuit and the second circuit must be separate, this does not necessarily require physical separation. Defendant responded that it is *not* arguing that the first circuit and the second circuit must be on separate *chips*, but the problem, Defendant argued, is that this claim uses "circuit" in a subjective way and, as a result, there is no way for a person of skill in the art to know if these limitations are satisfied.

(b) Analysis

Claim 18 of the '775 Patent recites (emphasis added):

18. A cable modem system comprising:

a data networking engine implemented in a first circuit that includes at least one processor, the data networking engine programmed with software that when executed by the at least one processor of the first circuit causes the data networking engine to perform home networking functions including interfacing with customer provided equipment;

a cable modem engine implemented in a second circuit that includes at least one processor, the second circuit being *separate* from the first circuit, the cable modem engine programmed with software that when executed by the at least one processor of the second circuit causes the cable modem engine to perform cable modem functions other than the home networking functions performed by the data networking engine, the cable modem functions including interfacing with cable media, and the cable modem engine configured to enable upgrades to its software in a manner that is independent of upgrades to the software of the data networking engine, the cable modem engine including a DOCSIS controller and a DOCSIS MAC processor, the DOCSIS MAC processor configured to process downstream PDU packets and forward the processed packets directly to the data networking engine without the involvement of the DOCSIS controller in order to boost downstream throughput; and

a data bus that connects the data networking engine to the cable modem engine, wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine.

The specification discloses "functional partitioning" and also contrasts the disclosed cable modem system with "current stand-alone cable modem chips":

> Functional Partitioning. Cable modem 100 completely partitions data networking functions . . . from DOCSIS cable modem functionality.
>
> * * *
>
> A chip implementing cable modem system 100 will have only a small incremental hardware cost/functional increase over current stand-alone cable modem chips.

'775 Patent at 4:13–16 & 4:58–60; *see id.* at FIGS. 1 and 2 (illustrating data networking engine ("DNE") 120 and cable modem engine ("CME") 110).

Such disclosure regarding "functionality" is consistent with the technical dictionary cited by Defendant's expert, which defines "circuit" as:

> 1. Any path that can carry electrical current. 2. A combination of electrical components interconnected to perform a particular task. At one level, a computer

> consists of a single circuit; at another, it consists of hundreds of interconnected circuits.

(Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl., App'x C, *Microsoft Computer Dictionary* 99 (5th ed. 2002).)

The specification and this extrinsic evidence are thus consistent with Plaintiff's interpretation that the phrases "first circuit" and "second circuit" are not limited to specific established structures but rather refer to interconnected electrical components that implement the data networking engine functionality and the cable modem engine functionality. *Cf. Linear Tech. Corp. v. Impala Linear Corp.*, 379 F.3d 1311, 1320 (Fed. Cir. 2004) ("when the structure-connoting term 'circuit' is coupled with a description of the circuit's operation, sufficient structural meaning generally will be conveyed to [POSITAs]").

Further, although the claim requires "the second circuit being separate from the first circuit," the "first circuit" and "second circuit" need not be physically separated, such as on separate chips, for example. *Cf. Linear Tech. Corp. v. Int'l Trade Comm'n*, 566 F.3d 1049, 1055 (Fed. Cir. 2009) ("We agree with the Commission's construction of 'second circuit' and 'third circuit,' defining the terms broadly to not require entirely separate and distinct circuits."). This is true even if the disclosed cable modem system 100 is implemented as a "System-on-a-Chip" ("SoC") because even if the SoC is considered to be a single "circuit" (*see* Dkt. No. 97, at 8; *see also* Dkt. No. 104, Ex. 2, May 4, 2023 Kramer dep. at 127:13–22 ("a System on a Chip can be considered an integrated circuit")), this circuit can itself be understood as being composed of multiple circuits. The opinions of Defendant's expert to the contrary are unpersuasive. (*See* Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶¶ 64–68.)

Thus, Defendant does not meet its burden to show any lack of reasonable certainty. *Nautilus*, 572 U.S. at 910. The *Dow* and *Teva* cases cited by Defendant do not compel otherwise

because, for example, the present case does not involve different potential methods of measurement. *See Dow Chemical Co. v. Nova Chemicals Corp. (Canada)*, 803 F.3d 620, 631, 634 (Fed. Cir. 2015) (finding indefiniteness as to "a slope of strain hardening coefficient greater than or equal to 1.3"); *see also Teva Pharmaceuticals USA, Inc. v. Sandoz, Inc.*, 789 F.3d 1335, 1338, 1344–45 (Fed. Cir. 2015) (finding indefiniteness as to "a molecular weight of about 5 to 9 kilodaltons").

The Court therefore hereby expressly rejects Defendant's indefiniteness argument. Defendant presents no alternative proposed constructions, and no further construction is necessary.

The Court accordingly hereby construes **"a data networking engine implemented in a first circuit that includes at least one processor . . ."** and **"a cable modem engine implemented in a second circuit that includes at least one processor . . ."** to have their **plain meaning**.

2. "data bus"

"data bus" ('775 Patent, Claim 18)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Indefinite

(Dkt. No. 84, at A-2; Dkt. No. 97, at 9; Dkt. No. 104, at 8; Dkt. No. 115, Ex. A, at 2.)

(a) The Parties' Positions

Plaintiff argues that the meaning of "data bus" is well known to persons of ordinary skill in the art. (Dkt. No. 97, at 9.)

Defendant responds that, in light of the prosecution history, "the 'data bus' limitation is irreconcilable with the 'completely partitioned' limitation, and claim 18 is therefore indefinite." (Dkt. No. 104, at 8 (citation omitted).)

Plaintiff replies that Defendant's argument is untenable because "[p]rosecution history disclaimers operate to narrow what would otherwise fall within a claim; they do not operate to invalidate claims by eliminating elements textually present." (Dkt. No. 110, at 2.)

At the June 13, 2023 hearing, the parties argued this term together with the above-discussed ". . . in a first circuit . . ." and ". . . in a second circuit . . ." terms.

(b) Analysis

Defendant does not dispute that "data bus" is a well-known term in the relevant art. (*See* Dkt. No. 97, Ex. 10, *The IEEE Standard Dictionary of Electrical and Electronics Terms* 252 (defining "data bus" as "a bus used to communicate data to and from a processing unit or a storage device").)

The parties' dispute pertains not to the term "data bus" in isolation but rather to the accompanying "wherein" clause, which the parties present as a distinct disputed term and which is addressed separately below.

The Court therefore hereby construes **"data bus"** to have its **plain meaning**.

3. "wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine"

"wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine" ('775 Patent, Claim 18)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	The cable modem engine and the data networking engine do not share any connecting circuitry, data paths, or memory devices.

(Dkt. No. 84, at A-4; Dkt. No. 97, at 10; Dkt. No. 104, at 8; Dkt. No. 115, Ex. A, at 2–3.)

(a) The Parties' Positions

Plaintiff argues:

> The disputed claim language explicitly recites that the functions of the DNE [(data networking engine)] and CME [(cable modem engine)] are partitioned. This distinction is key because functions can be partitioned in hardware, software, or both. Functional partitioning is explicitly described in the specification as 'localizing' the cable modem and data networking functions in the separate engines:
>
> * * *
>
> A POSITA would understand that connecting the DNE and CME (e.g., via a data bus) does not eliminate the compartmentalization of their respective functions."

(Dkt. No. 97, at 10 (citations omitted).)

Defendant responds as to this term together with the term "data bus," which is addressed above. (*See* Dkt. No. 104, at 8.) Plaintiff replies likewise. (*See* Dkt. No. 110, at 2–3.)

At the June 13, 2023 hearing, the parties argued this term together with the above-discussed ". . . in a first circuit . . ." and ". . . in a second circuit . . ." terms.

(b) Analysis

Claim 18 of the '775 Patent recites (emphasis added):

> 18. A cable modem system comprising:
>
> a data networking engine implemented in a first circuit that includes at least one processor, the data networking engine programmed with software that when executed by the at least one processor of the first circuit causes the data networking engine to perform home networking functions including interfacing with customer provided equipment;
>
> a cable modem engine implemented in a second circuit that includes at least one processor, the second circuit being separate from the first circuit, the cable modem engine programmed with software that when executed by the at least one processor of the second circuit causes the cable modem engine to perform cable modem functions other than the home networking functions performed by the data networking engine, the cable modem functions including interfacing with cable media, and the cable modem engine configured to enable upgrades to its software in a manner that is independent of upgrades to the software of the data networking engine, the cable modem engine including a DOCSIS controller and a DOCSIS MAC processor, the DOCSIS MAC processor configured to process downstream PDU packets and *forward the processed packets directly to the data networking engine* without the involvement of the DOCSIS controller in order to boost downstream throughput; and

> a *data bus* that connects the data networking engine to the cable modem engine, *wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine*.

The specification discloses "localizing" the *functions*:

> Functional Partitioning. Cable modem 100 completely partitions data networking *functions* (advanced bridging/routing, NAT/firewall, VPN, web server and CableHome applications) from DOCSIS cable modem *functionality*. This is accomplished by localizing data networking *functions* in the data networking engine processor and localizing cable modem *functions* in the cable modem engine processor.

'775 Patent at 4:13–19 (emphasis added). Further, the claim itself recites that the cable modem engine "forward[s] the processed packets directly to the data networking engine," thus implying that such communication is not inconsistent with the cable modem engine and the data networking engine being "completely partitioned" from one another. *See id.* at Figs. 1 & 2 (illustrating data path 118 between CME and DNE); *see also id.* at 3:15–17 ("DS PDU packets are forwarded by [the DOCSIS MAC processor] directly to [DNE] 120 along path 118, bypassing controller 116").

The prosecution history cited by Defendant does not compel otherwise. The patentee distinguished the "Brooks" reference (United States Patent Application Publication No. 2001/0039600) as follows:

> [T]he Office Action make the conclusion statement [*sic*] that "the data networking engine and cable modem engines are represented in Figures 1 and 2 of the [Brooks] reference" . . . . However, Applicant is uncertain how any reasonable interpretation of these Figures can provide correspondence. For example, Figure 2 of [Brooks] discloses only two processors, each of which, therefore, must correspond to the claimed data-networking and cable-modem engines. However, the discussion of Figure 2 makes clear that the cable modem functions are performed by CMAC unit 224 . . . . Therefore, in order for the cable modem engine to contain a processor and perform the CMAC functions as claimed, the cited cable modem engine must include circuitry to connect the processors with the CMAC unit. Because available *connecting circuitry would be shared with the other processor*, Applicant is uncertain how the asserted cable modem engine and home networking engine can be completely partitioned as claimed.

(Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl., App'x G, Apr. 5, 2010 Response to Final Office Action, at 6 (ENTROPIC_CHARTER_0000108) (p. 236 of 290 of Ex. 8) (emphasis added).)

After an advisory action by the examiner, the patentee explained further, distinguishing Brooks as using processors that were not functionally separate:

> The Examiner's apparent designation of the first processor 102 in Brooks '600 as the "data networking engine," and the second processor 104 and the CMAC/CPHY block (114, 118, 224 and 228) as the "cable modem engine," further does not square with the claim 1 feature that "the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine," and the claim 15 feature of "partitioning the data networking engine from the cable modem engine so that the data and home networking functionality is completely decoupled from the DOCSIS and VOOP functionality." This is because the CMAC/CPHY block (114, 118, 224 and 228) communicates with both the processors 102 and 104 by sharing the same data paths and sharing the same direct memory access controller. (See peripheral bus 112 – bridge 110 – system bus 108 in Fig. 1 and APB 214 – OMA Controller/ASB-APB Bridge 212 – ASB 210 in Fig. 2, and paragraphs 0034 and 0035).
>
> Further, accepting the Examiner's assertion that first processor 102 handles data networking *functionality*, and considering the description of paragraphs 0025 and 0026 that processor 102 is programmed to implement the desired MAC *functionality* (which would include typical DOCSIS MAC *functionality*), leads to a conclusion that the Brooks '600 processor 102 does not implement a complete partitioning or a completely decoupled arrangement of the data networking engine from the cable modem engine.
>
> Thus, Brooks '600 does not provide the complete partitioning or completely decoupled arrangement of the data networking engine from the cable modem engine that the Examiner apparently asserts it does.

(*Id.*, June 7, 2010 Response to Final Office Action, at 9 (ENTROPIC_CHARTER_0000134) (p. 254 of 290 of Ex. 8) (emphasis added); *see id.*, at 7–9 (ENTROPIC_CHARTER_0000132–34) (pp. 252–54 of 290 of Ex. 8).)

The patentee thus distinguished Brooks as lacking *functional* separation because what the examiner identified as the cable modem engine in Brooks required interaction with the "CMAC unit," and, the patentee argued, such interaction involved circuitry that was shared with what the

examiner identified as the data networking engine in Brooks. (*See id.*) Thus, no relevant disclaimer is apparent, and in particular the patentee did not disclaim having a data bus that connects the data networking engine to the cable modem engine, as recited in above-reproduced Claim 1 of the '775 Patent. *See Omega Eng'g Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003) ("prosecution disclaimer promotes the public notice function of the intrinsic evidence and protects the public's reliance on *definitive* statements made during prosecution") (emphasis added); *see also id.* at 1325–26 ("for prosecution disclaimer to attach, our precedent requires that the alleged disavowing actions or statements made during prosecution be both *clear and unmistakable*") (emphasis added).

The Court therefore hereby expressly rejects Defendant's proposal that the cable modem engine and the data networking engine cannot share any connecting circuitry, data paths, or memory devices.

The Court accordingly hereby construes **"wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine"** to mean **"wherein the cable modem engine and the data networking engine are not necessarily physically separate but are functionally separate such that the cable modem functions are performed only by the cable modem engine and the home networking functions are performed only by the data networking engine."**

4. "DOCSIS functions"

"DOCSIS functions" ('775 Patent, Claim 19)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	This limitation does not change the scope of claim 18.

(Dkt. No. 84, at A-5; Dkt. No. 97, at 11; Dkt. No. 104, at 8; Dkt. No. 115, Ex. A, at 3.)

(a) The Parties' Positions

Plaintiff argues that Defendant's proposal is contrary to the doctrine of claim differentiation. (Dkt. No. 97, at 12.)

Defendant responds:

> According to claim 19, all DOCSIS functions are localized in the CME. However, as explained . . . above, the specification explains that the sine qua non of a CME is that it 'performs all cable modem functions' including 'the entire DOCSIS cable modem functionality.' Accordingly, claim 19 is redundant and does not further limit the scope of claim 18. Otherwise, the term 'cable modem engine' is indefinite.

(Dkt. No. 104, at 9.)

Plaintiff replies that there is no redundancy because "Claim 18 recites the broader 'cable modem functions,' which does not necessarily have the same scope as 'all *DOCSIS* functions,' referring to the DOCSIS standard." (Dkt. No. 110, at 3.)

At the June 13, 2023 hearing, the parties argued this term together with the above-discussed ". . . in a first circuit . . ." and ". . . in a second circuit . . ." terms.

(b) Analysis

Claim 19 of the '775 Patent depends from Claim 18 and recites:

> 19. A cable modem system as claimed in claim 18, wherein all DOCSIS functions are localized in the cable modem engine.

Plaintiff applies the doctrine of claim differentiation, arguing:

> Claim 18 states that the CME comprises a processor, programmed with software, that when executed causes the CME to perform "cable modem functions other than the home networking functions performed by the [DNE]." Dependent claim 19 increases the burden on the CME—"all DOCSIS functions are localized in the [CME]." Logically, claim 18 does not require that each and every DOCSIS function be executed by the circuitry of the CME, while claim 19 does.

(Dkt. No. 97, at 12.)

As a general matter, "[c]laim differentiation is 'not a hard and fast rule,' but rather a presumption that will be overcome when the specification or prosecution history dictates a contrary construction." *GPNE Corp. v. Apple Inc.*, 830 F.3d 1365, 1371 (Fed. Cir. 2016).

Defendant argues that this limitation set forth in Claim 19 is redundant (and thus does not imply the absence of such a limitation in Claim 18) because Claim 18, read in light of the specification, already requires this limitation. (*See* Dkt. No. 104, at 9.) Defendant argues that "cable modem engine" "is a phrase coined by the inventors" and "[i]f it does not refer to the components of a cable modem that perform all the cable modem functions, then there is no way to know what it is." (*Id.*, at 9.)

Defendant cites disclosure in the Abstract that the CME "performs all cable modem functions" and "implements the entire DOCSIS cable modem functionality." '775 Patent at Abstract & 2:55–56. The Abstract, however, is not limiting, and the portion of the written description cited by Defendant does not purport to limit the entire claimed invention but rather describes a particular embodiment of "cable modem engine 110." *See Phillips*, 415 F.3d at 1323. Further, there is a "presumption that each claim in a patent has a different scope." *Comark Comm'cns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998). The contrary opinion of Defendant's expert is unpersuasive. (*See* Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶ 36 (citing '775 Patent at 2:15–17 ("In one implementation, the VoIP functionality provided by the

cable modem is in accordance with the PacketCable specification and the data networking functionality provided by the data networking engine is in accordance with the CableHome specification."), 2:23–24 ("Data and home networking functionality is provided by a data networking engine, and DOCSIS and VoIP functionality is provided by a cable modem engine.") & 4:19–21).)

The Court therefore hereby expressly rejects Defendant's attempted reliance on Claim 19 to arrive at a narrow interpretation of "cable modem engine" in Claim 18, and no further construction is necessary as to Claim 19. *See U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997) ("Claim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement. It is not an obligatory exercise in redundancy."); *see also O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) ("[D]istrict courts are not (and should not be) required to construe every limitation present in a patent's asserted claims."); *Finjan, Inc. v. Secure Computing Corp.*, 626 F.3d 1197, 1207 (Fed. Cir. 2010) ("Unlike *O2 Micro*, where the court failed to resolve the parties' quarrel, the district court rejected Defendants' construction."); *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1326 (Fed. Cir. 2012); *Summit 6, LLC v. Samsung Elecs. Co., Ltd.*, 802 F.3d 1283, 1291 (Fed. Cir. 2015); *Bayer Healthcare LLC v. Baxalta Inc.*, 989 F.3d 964, 977–79 (Fed. Cir. 2021).

The Court accordingly hereby construes **"DOCSIS functions"** to have its **plain meaning**.

5. "DOCSIS MAC processor" and "DOCSIS controller"

"DOCSIS MAC processor" ('775 Patent, Claim 18)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	The DOCSIS MAC processor as described in the patent specification (*see, e.g.*, '775 Patent at 3:1–20; 4:41–57; *id.* at FIGs. 1 & 2). Otherwise indefinite.
"DOCSIS controller" ('775 Patent, Claim 18)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	The DOCSIS controller as described in the patent specification (*see, e.g.*, '775 Patent at 3:21–48; 4:41–57; *id.* at FIGs. 1 & 2). Otherwise indefinite.

(Dkt. No. 84, at A-6; Dkt. No. 97, at 12; Dkt. No. 115, Ex. A, at 1–2.)

(a) The Parties' Positions

Plaintiff urges that Defendant's proposals would improperly limit these terms to specific exemplary embodiments described in the specification. (Dkt. No. 97, at 12.) Plaintiff also argues that Defendants have already agreed that these are *not* means-plus-function terms governed by 35 U.S.C. § 112, ¶ 6. (*Id.*) Further, Plaintiff submits that "[t]he Federal Circuit and this Court have held that the terms 'processor' and 'controller' denote known classes of structures—generally understood to POSITAs." (*Id.* (citations omitted).)

Defendant responds that "[n]either the phrase 'DOCSIS MAC processor' nor 'DOCSIS controller' has a plain meaning." (Dkt. No. 104, at 9.) Defendant also argues that Plaintiff's proposed construction would either contradict the specification or "make it impossible to distinguish a DOCSIS MAC processor from a DOCSIS controller." (*Id.*, at 9–10.) Defendant

urges that "[t]he only construction of DOCSIS MAC processor and DOCSIS controller that both comports with the specification and provides a basis for distinguishing between the two is a construction whereby each refers to the corresponding device described in the specification." (*Id.*, at 11.)

Plaintiff replies that "the claims themselves describe the functions of the DOCSIS MAC processor and DOCSIS controller," and "Charter has made no argument that the DOCSIS MAC processor and DOCSIS controller should be limited to the specific ARM-based embodiments disclosed in the specification." (Dkt. No. 110, at 3–4.)

At the June 13, 2023 hearing, Defendant submitted that the DOCSIS controller disclosed in the specification performs some MAC functions. Defendant argued that this makes it impossible to distinguish between a "DOCSIS MAC processor" and a "DOCSIS controller," which, in turn, Defendant argued makes it impossible to determine whether an accused instrumentality meets the limitation of "forward[ing] the processed packets directly to the data networking engine without the involvement of the DOCSIS controller."

(b) Analysis

Claim 18 of the '775 Patent recites (emphasis added):

> 18. A cable modem system comprising:
>
> a data networking engine implemented in a first circuit that includes at least one processor, the data networking engine programmed with software that when executed by the at least one processor of the first circuit causes the data networking engine to perform home networking functions including interfacing with customer provided equipment;
>
> a cable modem engine implemented in a second circuit that includes at least one processor, the second circuit being separate from the first circuit, the cable modem engine programmed with software that when executed by the at least one processor of the second circuit causes the cable modem engine to perform cable modem functions other than the home networking functions performed by the data networking engine, the cable modem functions including interfacing with cable media, and the cable modem engine configured to enable upgrades to its software in a manner that is independent of upgrades to the software of the data networking

> engine, the cable modem engine including a *DOCSIS controller* and a *DOCSIS MAC processor*, the *DOCSIS MAC processor* configured to process downstream PDU packets and forward the processed packets directly to the data networking engine without the involvement of the *DOCSIS controller* in order to boost downstream throughput; and
>
> a data bus that connects the data networking engine to the cable modem engine, wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine.

The words "processor" and "controller" refer to known classes of structures in the relevant art, and the parties agree that "DOCSIS" (Data Over Cable Service Interface Specification) and DOCSIS "MAC" (Medium Access Control) have been well-known at all relevant times. (*See, e.g.,* Dkt. No. 97, Ex. 7, Apr. 14, 2023 Kramer Decl. at ¶ 84.)

Defendant proposes to limit these terms to the particular DOCSIS controller and DOCSIS MAC processor disclosed in the specification, but Defendant does not show any definition or disclaimer that would warrant a narrowing of these terms. *See Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1367 (Fed. Cir. 2012) ("The patentee is free to choose a broad term and expect to obtain the full scope of its plain and ordinary meaning unless the patentee explicitly redefines the term or disavows its full scope.").

Moreover, other claims of the patent-in-suit can be considered. *See Phillips*, 415 F.3d at 1314. Claim 1 recites a "DOCSIS MAC processor" and a "DOCSIS controller," and Claim 12 depends from Claim 1 and recites that "the DOCSIS MAC processor is an ARM9TDMI-based RISC processor, and wherein the DOCSIS controller is an ARM940-based RISC processor." Because claim terms should be interpreted consistently throughout all of the claims of a particular patent, *id.*, the doctrine of claim differentiation weighs against limiting the "DOCSIS MAC processor" and a "DOCSIS controller" to ARM9TDMI, ARM940, or any other particular specific implementation.

The disclosure in the specification regarding "functional blocks" is also consistent with interpreting these terms broadly rather than limiting them to particular types of processors. *See* '775 Patent at 2:55–3:38; *see also* Dkt. No. 97, Ex. 7, Apr. 14, 2023 Kramer Decl. at ¶¶ 92–93.

Further, Defendant cites disclosure in which the DOCSIS controller is involved with MAC functions (*see* '775 Patent at 3:27–48), but although the claim requires a "DOCSIS MAC processor configured to . . . forward the processed packets directly to the data networking engine without the involvement of the DOCSIS controller," the absence of involvement of the DOCSIS controller in this particular operation does not preclude the DOCSIS controller from being involved with other MAC functions.

Finally, Defendant cites the opinions of its expert that a person of ordinary skill in the art would be unable to distinguish between a "DOCSIS MAC processor" and a "DOCSIS controller," but these opinions are unpersuasive, particularly given that DOCSIS is a well-established standard and that MAC is also a well-known term in the relevant art. (*See* Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶¶ 76–77.) Any remaining question regarding distinguishing between a "DOCSIS MAC processor" and a "DOCSIS controller" pertains to factual questions of infringement rather than any legal question for claim construction. *See PPG Indus. v. Guardian Indus. Corp.*, 156 F.3d 1351, 1355 (Fed. Cir. 1998) ("after the court has defined the claim with whatever specificity and precision is warranted by the language of the claim and the evidence bearing on the proper construction, the task of determining whether the construed claim reads on the accused product is for the finder of fact"); *see also Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 806 (Fed. Cir. 2007) ("[t]he resolution of some line-drawing problems . . . is properly left to the trier of fact") (citing *PPG*, 156 F.3d at 1355); *Eon Corp. IP Holdings LLC v. Silver Spring*

Networks, Inc., 815 F.3d 1314, 1318–19 (Fed. Cir. 2016) (citing *PPG*, 156 F.3d at 1355; citing *Acumed*, 483 F.3d at 806).

The Court therefore hereby expressly rejects Defendant's proposed constructions, and no further construction is necessary. *See U.S. Surgical*, 103 F.3d at 1568; *see also O2 Micro*, 521 F.3d at 1362; *Finjan*, 626 F.3d at 1207; *ActiveVideo*, 694 F.3d at 1326; *Summit 6*, 802 F.3d at 1291; *Bayer*, 989 F.3d at 977–79.

The Court accordingly hereby construes **"DOCSIS MAC processor"** and **"DOCSIS controller"** to have their **plain meaning**.

V. DISPUTED TERMS IN U.S. PATENT NO. 9,825,826

The '826 Patent is a continuation of the '008 Patent.

Plaintiff submits: "The '826 and the '008 Patents disclose methods and apparatuses that can be implemented in Customer Premises Equipment (CPE) that enable the CPE to: receive a cable or satellite television signal, digitize said signal, determine a characteristic of the digitized signal, and then report the determined characteristic back to the source of the signal (*i.e.*, the network-based service providers) without interrupting normal customer service." (Dkt. No. 97 at 3.)

The '008 Patent, titled "Method and Apparatus for Spectrum Monitoring," issued on July 29, 2014, and bears an earliest priority date of September 8, 2011. The Abstract of the '008 Patent states:

> A system, such as a satellite reception assembly or customer premises gateway, may comprise an analog-to-digital converter operable to digitize a signal spanning an entire television spectrum (e.g., cable television spectrum or satellite television spectrum) comprising a plurality of television channels. The system may comprise a signal monitor operable to analyze a signal to determine a characteristic of the signal. The system may comprise a data processor operable to process a television channel to recover content carried on the television channel. The system may comprise a channelizer operable to select first and second portions of the signal,

and concurrently output the first portion to the signal monitor and the second portion to the data processor.

6. "network management messages"

"network management messages" ('826 Patent, Claim 1)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Messages which report on the status of the network based on an analysis of the measured characteristics.

(Dkt. No. 84, at A-8; Dkt. No. 97, at 15; Dkt. No. 104, at 12; Dkt. No. 115, Ex. A, at 5.)

(a) The Parties' Positions

Plaintiff argues that "[t]he Court should construe this term according to its plain and ordinary meaning because 'network management message' is a plain English phrase that means exactly what it says," and "[t]he '826 Patent's specification confirms the phrase is meant to convey all its ordinary possibilities, in disclosing a list of exemplary types/uses of the messages." (Dkt. No. 97, at 15 (citations omitted).)

Defendant responds that Plaintiff attempts to encompass implementations in which the set-top box returns only a measured characteristic and nothing else to the headend, which Defendant argues is inconsistent with the claim requirement that "said measured characteristic is *different than* said network management messages." (Dkt. No. 104, at 12 (emphasis modified).)

Plaintiff replies that Defendant improperly relies on claim language in the parent '008 Patent in an attempt to limit Claim 1 of the continuation '826 Patent. (Dkt. No. 110, at 4.) Plaintiff also argues that Defendant's argument pertains to a question of fact, not claim construction. (*Id.*)

At the June 13, 2023 hearing, Defendant submitted that although Defendant is *not* arguing that the message cannot include the measured characteristic, the message must include something

that is *not* the measured characteristic. As for Plaintiff's interpretation that a *message* conveying just the measured characteristic is "different" than the measured characteristic *itself*, Defendant argued that this would vitiate the claim requirement that "said measured characteristic is different than said network management messages."

(b) Analysis

Claim 1 of the '826 Patent recites (emphasis added):

> 1. A method comprising:
> performing by one or more circuits of a receiver coupled to a television and data service provider headend via a hybrid fiber coaxial (HFC) network:
> receiving, via said HFC network, a signal that carries a plurality of channels, wherein said channels comprise one or both of television channels and data channels;
> digitizing said received signal to generate a digitized signal;
> selecting a first portion of said digitized signal;
> selecting a second portion of said digitized signal;
> processing said selected second portion of said digitized signal to recover information carried in said plurality of channels;
> analyzing said selected first portion of said digitized signal to measure a characteristic of said received signal; and
> controlling the transmission of *network management messages* back to said headend based on said measured characteristic of said received signal, wherein said measured characteristic is different than said *network management messages*.

On one hand, the specification discloses that messages sent to the headend can include measured characteristics:

> The CMTS 114 may process the messages and, in an example embodiment, adjust transmission parameters (e.g., modulation parameters, transmit power, frequency offsets, etc.) and/or perform other maintenance/management based on the received messages.
>
> * * *
>
> Such message may comprise, for example, network status updates indicating whether one or more communication parameters of one or more received television or DOCSIS channels are outside acceptable bounds, and/or *conveying measured/determined characteristics* back to a source of the received signal (e.g., back to a cable headend).

'826 Patent at 3:11–15 & 3:63–4:2 (emphasis added).

On the other hand, the claim here at issue, Claim 1 of the '826 Patent, recites that "said measured characteristic is *different than* said network management messages." Thus, simply sending the measured characteristic to the headend is insufficient to meet this claim limitation. Also of note, this contrasts with the recital in Claim 1 of the related '008 Patent of "report[ing] said determined characteristic to a source of said received signal."

Nonetheless, Defendant's proposal of an "*analysis* of the measured characteristics" lacks sufficient support in the specification. Defendant cites disclosures regarding "analyz[ing]" and whether one or more channels are "outside acceptable bounds":

> The monitoring module 154 may be operable to *analyze* the band C_{J+1} that it receives from the channelizer 102 to *measure/determine characteristics* such as, for example, signal power level vs. frequency, delay vs. frequency, phase shift vs. frequency, type and/or amount of modulation, code rate, interference levels, signal to noise ratio, a transfer function of the channel of [*sic*] over which the signal was received, an impulse response of the channel over which the signal was received, and/or any other characteristic that may help assess characteristics of the channel over which the signal was received, assess characteristics of the transmitter that sent the signal and/or any otherwise be pertinent to performance of the communication system. . . . Additionally or alternatively, the control signal(s) 160 output by the monitoring module 154 may control the transmission of network management/maintenance messages by the device 150. Such message may comprise, for example, network status updates indicating whether one or more communication parameters of one or more received television or DOCSIS channels are *outside acceptable bounds*, and/or conveying *measured/determined* characteristics back to a source of the received signal (e.g., back to a cable headend)[.]

Id. at 3:45–4:2 (emphasis added).

This disclosure regarding "acceptable bounds" relates to a specific feature of a particular embodiment and does not warrant introducing a "status" or "analysis" limitation into the construction of "network management messages." *See Phillips*, 415 F.3d at 1323. Further, this disclosure that "[t]he monitoring module 154 may be operable to analyze the band C_{J+1} that it

receives from the channelizer 102 to measure/determine characteristics" likewise pertains to a particular embodiment and, moreover, this usage of "analyze" merely reflects what is already recited elsewhere in the claim, namely "analyzing said selected first portion of said digitized signal to measure a characteristic of said received signal." Defendant's proposal of construing "network management messages" in terms of an "analysis" would tend to confuse rather than clarify the scope of the claim.

Nonetheless, although the claim already recites "transmission of network management messages back to said headend *based on* said measured characteristic of said received signal," Defendant's proposal of "based on" will assist the finder of fact in understanding that merely sending the measured characteristic is insufficient. *See 01 Communique Laboratory, Inc. v LogMeIn, Inc.*, 687 F.3d 1292, 1296 (Fed. Cir. 2012) ("01 Communique has not cited, and we have not discovered, any authority for the proposition that construction of a particular claim term may not incorporate claim language circumscribing the meaning of the term.").

Finally, Defendant discusses Plaintiff's infringement contentions (*see* Dkt. No. 104, at 12–13), but any remaining dispute pertains to factual questions regarding infringement rather than any legal question for claim construction. *See PPG*, 156 F.3d at 1355; *see also Acumed*, 483 F.3d at 806 (citing *PPG*, 156 F.3d at 1355); *Eon*, 815 F.3d at 1318–19 (citing *PPG*, 156 F.3d at 1355; citing *Acumed*, 483 F.3d at 806).

The Court therefore hereby construes **"network management messages"** to mean **"messages which report on the network based on the measured characteristics."**

VI. DISPUTED TERMS IN U.S. PATENT NO. 8,792,008

7. "operable to"

"operable to" ('008 Patent, Claim 1)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Configured to

(Dkt. No. 84, at A-8; Dkt. No. 97, at 16; Dkt. No. 104, at 13.)

In their Amended Patent Rule 4-5(d) Joint Claim Construction Chart, the parties agree that "operable to" should be construed to mean "configured to." (Dkt. No. 115, Ex. A, at 3.)

The Court therefore hereby construes **"operable to"** to mean **"configured to."**

8. "digitize a received signal spanning an entire television spectrum comprising a plurality of television channels"

"digitize a received signal spanning an entire television spectrum comprising a plurality of television channels" ('008 Patent, Claim 1)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	The "received signal" contains only television channels.

(Dkt. No. 84, at A-9; Dkt. No. 97, at 16; Dkt. No. 104, at 13; Dkt. No. 115, Ex. A, at 3–4.)

(a) The Parties' Positions

Plaintiff argues that "[t]he plain language of the claim recites '*comprising* a plurality of television channels,' indicating that the 'received signal spanning an entire television spectrum' is *not limited* to only television channels." (Dkt. No. 97, at 16.) Plaintiff also argues that the specification confirms this understanding. (*See id.*, at 17.)

Defendant responds that "'[s]pan' is a plain English word which means the full extent of something from end to end (*e.g.,* 'wing span,' 'life span,' 'span of a bridge')." (Dkt. No. 104, at 14.)

Plaintiff replies that "a television spectrum may contain inside it something in addition to individual television channels," and "[i]t does not cease being a television spectrum if non-video signals are added within the block." (Dkt. No. 110, at 4–5.)

At the June 13, 2023 hearing, Defendant alternatively proposed: "The 'received signal' contains only television channels and data channels which fall between television channels."

(b) Analysis

Claim 1 of the '008 Patent recites (emphasis added):

> 1. A system comprising:
>
> an analog-to-digital converter operable to *digitize a received signal spanning an entire television spectrum comprising a plurality of television channels*, said digitization resulting in a digitized signal;
>
> a signal monitor operable to:
>
> analyze said digitized signal to determine a characteristic of said digitized signal; and
>
> report said determined characteristic to a source of said received signal;
>
> a data processor operable to process a television channel to recover content carried on the television channel; and
>
> a channelizer operable to:
>
> select a first portion of said digitized signal;
>
> select a second portion of said digitized signal; and
>
> concurrently output said first portion of said digitized signal to said signal monitor and said second portion of said digitized signal to said data processor.

As a general matter, "[t]he transitional term 'comprising' . . . is open-ended and does not exclude additional, unrecited elements or method steps." *See Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1371 (Fed. Cir. 2005).

Defendant submits authority that "[t]he usage 'comprising' means that additional components may be present in the device, but does not change the elements that are stated in the claim." *Outside the Box Innovations, LLC v. Travel Caddy, Inc.*, 695 F.3d 1285, 1305 (Fed. Cir. 2012).

But although the claim language refers to "television spectrum" and refers to the television spectrum comprising television channels, this does *not* preclude non-television channels from being present within that spectrum. In other words, Defendant has not shown that this usage of "comprising" is somehow closed-ended. Also, Defendant's reliance at the June 13, 2023 hearing on a general-purpose dictionary definition of "spanning" as referring to the "extent" of something "between any two limits," even if found relevant, is unpersuasive. *Collins English Dictionary* (30th ed.).

This finding is consistent with disclosures in the specification that the received signal may include data from an IP network or may include DOCSIS channels:

> For downstream traffic, the headend 108 may receive television signals via the antenna 102 and the satellite dish 104, and *may receive data via the IP network 106*. The switch 110 may convey the television signals to the video modulator 112 and the data to the CMTS 114. The video modulator 112 may modulate the received television signals onto a carrier. The CMTS 114 may modulate the received data onto carrier. The splitter/combiner 116 may *combine the outputs* of the video modulator 112 and the CMTS 114 resulting in a frequency division multiplexed (FDM) *signal comprising one or more television channels and/or one or more DOCSIS channels*.
>
> * * *
>
> The RF receive front-end 158 may be operable to process a received RF signal S to generate a digital signal D. The signal S may be the result of *a plurality of television and/or DOCSIS channels* being frequency division multiplexed into a *single signal*. The signal S may occupy a frequency band from F_{lo} to F_{hi}.

'008 Patent at 2:44–54 & 3:12–16 (emphasis added); *see id.* at 4:45–47 ("The data processing module 156 may process one or more of bands C_1–C_J to recover data on one or more channels

(e.g., television and/or DOCSIS channels) . . . .") & 5:60–62 ("Accordingly, for cable television/DOCSIS, the ADC 256 may be operable to digitize the entire cable downstream (e.g., from ~55 MHz to ~1002 MHz).").

Further, Defendant points to the express recital in Claim 1 of the '826 Patent that the received signal comprises "one or both of television and data channels," but this recital in a different independent claim in a different (albeit related) patent does not imply or otherwise justify a narrow interpretation of the disputed term in Claim 1 of the '008 Patent. Further, as Plaintiff argued at the June 13, 2023 hearing, whereas Claim 1 of the '826 Patent allows for there being only data channels, Claim 1 of the '008 Patent requires television channels.

Finally, at the June 13, 2023 hearing, Defendant proposed that "[t]he 'received signal' contains only television channels and data channels which fall between television channels." Defendant thus proposes that a data channel cannot overlap (or be subsumed within) a television channel. As discussed above, Defendant does not demonstrate that the disputed term precludes the presence of data channels within the same spectrum as television channels. The Court therefore rejects Defendant's alternative proposal.

The Court thus hereby expressly rejects Defendant's proposed constructions. No further construction is necessary. *See U.S. Surgical*, 103 F.3d at 1568; *see also O2 Micro*, 521 F.3d at 1362; *Finjan*, 626 F.3d at 1207; *ActiveVideo*, 694 F.3d at 1326; *Summit 6*, 802 F.3d at 1291; *Bayer*, 989 F.3d at 977–79.

The Court accordingly hereby construes **"digitize a received signal spanning an entire television spectrum comprising a plurality of television channels"** to have its **plain meaning**.

9. "signal monitor," "data processor," and "channelizer"

"signal monitor" "data processor" "channelizer" ('008 Patent, Claim 1)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Three separate pieces of hardware, configured to perform the functions the claim ascribes to the signal monitor, data processor, and channelizer, respectively.

(Dkt. No. 84, at A-9; Dkt. No. 97, at 17; Dkt. No. 104, at 14; Dkt. No. 115, Ex. A, at 4.)

(a) The Parties' Positions

Plaintiff argues that Defendant's proposal should be rejected because "[n]o phrase [in the claim] even arguably related to separateness is present," and "the specification is clear that these three items do *not* have to be implemented on separate pieces of hardware." (Dkt. No. 97, at 17.)

Defendant responds:

> Entropic contends that there need not be any 'separateness' between the three, and that they can all refer to the same physical device. Entropic provides no support for its contention that this is the 'plain and ordinary meaning' of these terms, or any facts to overcome the presumption that each of these must be a distinct physical component. . . . Nor could Entropic possibly overcome this presumption, as neither the claims nor the specification make any sense unless each of the three is a separate device.

(Dkt. No. 104, at 14–15 (citation omitted).)

Plaintiff replies that Defendant is attempting to argue a question of fact regarding what is separate, as part of claim construction, which Plaintiff submits is improper. (Dkt. No. 110, at 5.) Plaintiff also submits that "[b]y the priority date (2011), it was exceedingly common for a single

SoC [(System on a Chip)] to embody many functional elements, as a POSITA would have been well aware." (*Id.* (footnote omitted).)

At the June 13, 2023 hearing, Defendant argued that these terms refer to three structures that might even be on a single chip but that nonetheless must be physically separate pieces of hardware.

(b) Analysis

Claim 1 of the '008 Patent recites (emphasis added):

> 1. A system comprising:
> an analog-to-digital converter operable to digitize a received signal spanning an entire television spectrum comprising a plurality of television channels, said digitization resulting in a digitized signal;
> a *signal monitor* operable to:
> analyze said digitized signal to determine a characteristic of said digitized signal; and
> report said determined characteristic to a source of said received signal;
> a *data processor* operable to process a television channel to recover content carried on the television channel; and
> a *channelizer* operable to:
> select a first portion of said digitized signal;
> select a second portion of said digitized signal; and
> concurrently output said first portion of said digitized signal to said *signal monitor* and said second portion of said digitized signal to said *data processor*.

As a general matter, "[w]here a claim lists elements separately, 'the clear implication of the claim language' is that those elements are 'distinct component[s]' of the patented invention." *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010); *see Kyocera Senco Indus. Tools Inc. v. Int'l Trade Comm'n*, 22 F.4th 1369, 1382 (Fed. Cir. 2022) (listing components separately in a claim gives rise to "a presumption that those components are distinct").

Defendant does not show, however, that a requirement for "distinct" components, *id.*, necessarily requires separate pieces of hardware. Also, the specification discloses that "[t]he various modules of the subassembly 174," including "the signal monitor 154, data processor 156, and channelizer 152," "may reside in . . . one or more integrated circuits." *See id.* at 4:56–59 & Fig. 1C. Defendant argues that "[w]hat this sentence means is that each individual module can be one or more integrated circuits, not that all of the different modules can be one device" (Dkt. No. 104, at 16), but here, too, the patentee did not express or imply any physical separation.

Finally, at the June 13, 2023 hearing, Defendant emphasized disclosure regarding "[t]he parallel arrangement of the monitoring module 154 and data processing module 156," but this disclosure pertains to a specific embodiment and therefore should not be imported into the claim. *See Phillips*, 415 F.3d at 1323. Also, Defendant does not show that a "parallel arrangement" necessarily implies physically separate structures.

The Court therefore hereby expressly rejects Defendant's proposed construction. No further construction is necessary. *See U.S. Surgical*, 103 F.3d at 1568; *see also O2 Micro*, 521 F.3d at 1362; *Finjan*, 626 F.3d at 1207; *ActiveVideo*, 694 F.3d at 1326; *Summit 6*, 802 F.3d at 1291; *Bayer*, 989 F.3d at 977–79.

The Court accordingly hereby construes **"signal monitor," "data processor,"** and **"channelizer"** to have their **plain meaning**.

VII. DISPUTED TERMS IN U.S. PATENT NO. 8,284,690

The '690 Patent, titled "Receiver Determined Probe," issued on October 9, 2012, and bears an earliest priority date of December 15, 2008. Plaintiff submits that the '690 Patent "relates generally to aiding in the diagnosis of problems with subscriber services." (Dkt. No. 97 at 4.)

The Abstract of the '690 Patent states:

> According to various embodiments of the disclosed method and apparatus, nodes on a network are programmed to generate a probe transmission in response to a request from the node that will be receiving the probe. The receiving node may generate a probe request that specifies a plurality of parameters, such as a modulation profile for the probe; the payload content of the probe; the number of times to transmit the probe; a number of symbols for the payload of the probe; a preamble type for the probe; a cyclic-prefix length for the payload of the probe; a transmit power for the probe; and a transmit power scaling factor for the payload of the probe.

10. "probe" and "physical layer probe"

"probe" ('690 Patent, Claims 1, 7, 8, 9, 11)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	A packet transmitted to a network node which the node compares to a reference packet having a known form in order to determine characteristics of the channel on which the packet was transmitted.
"physical layer probe" ('690 Patent, Claim 9)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	"Physical layer probe" means probe. Otherwise indefinite.

(Dkt. No. 84, at A-10; Dkt. No. 97, at 18; Dkt. No. 104, at 18; Dkt. No. 115, Ex. A, at 7–9 & 11.)

(a) The Parties' Positions

Plaintiff argues that these are different terms and are therefore presumed to have different meanings. (Dkt. No. 97, at 18.) Plaintiff also argues that "Charter's proposed construction imposes on 'probe' a lengthy requirement of a specific function, in clear violation of the rule against importing the specification into the claim." (*Id.* (citation omitted).)

Defendant responds: "Entropic asserts that 'probe' should be construed according to its plain and ordinary meaning, but it does not explain which of the many 'plain meanings' of the word 'probe' applies. Charter's construction, taken from the patent specification, *is* the plain meaning in the context of probes sent between nodes in a network. The DOCSIS specification confirms this." (Dkt. No. 104, at 18.) As for Defendant's proposal of "packet," Defendant submits that "'[p]acket' is in the construction to avoid having the word 'probe' in the construction of 'probe' and because probes *are* packets." (*Id.*)

Plaintiff replies that "Charter grounds its argument to limit 'probe' based on *post-priority, extrinsic* evidence," and "Charter's focus seems to be on the DOCSIS 3.1 cable modems accused of infringement in this case, thereby committing error in construing the claims with reference to the accused devices." (Dkt. No. 110, at 6 (citation omitted).) Also, "with respect to 'physical layer probe,' Charter errs by importing an embodiment into the claims." (*Id.*)

At the June 13, 2023 hearing, Plaintiff alternatively proposed that a "probe" is "a signal used to determine one or more characteristics of a channel." Defendant disagreed with Plaintiff's alternative proposal, but Defendant had no objection to replacing "packet" with "signal" in Defendant's proposed construction.

(b) Analysis

The specification discloses that "probes" are used, for example, to determine characteristics of channels:

> In some instances, probes are sent between nodes of the network in order to allow a receiving node on the network to determine some of the characteristics of the channel between the receiving node and the transmitting node. These probes are typically well defined. Accordingly, the receiving node knows before reception what reference signal was transmitted. By comparing the reference probe with the actual received probe, the receiver can determine some of the characteristics of the channel between the transmitting and receiving node.

> * * *
>
> In various embodiments, these receiver determined probes may be used in a variety of applications. For example, the probes may be used to reach or discover hidden nodes; in networks employing orthogonal frequency division multiple access (OFDMA), the probes may be used for OFDMA subchannel assessment; or in networks accessible by content providers, the probes may be used for off-site network diagnosis.
>
> * * *
>
> In block 204, the requesting node receives the probe generated according to its earlier probe request. The received probe may then be used in further processing in block 205. In one embodiment, the received probe may be used in channel analysis to determine a bitloading table, FEC and other communication parameters for OFDM or OFDMA signals for future transmissions from the probe transmitter. In another embodiment, post reception processing might comprise generating a report from the probe and transmitting this probe report to the requesting node or to a designated entity.

'690 Patent at 1:48–57, 2:20–27 & 6:59–7:11.

Claim 9 of the '690 Patent is limited to a "physical layer probe," and the subsequent recitals of "the probe" in Claim 9 can be readily understood as referring back to the recital of a "physical layer probe" (emphasis added):

> 9. A method comprising:
>
> a) a first node transmitting a probe request to a second node, the probe request specifying a first plurality of probe parameters for *a physical layer probe*, the first plurality of probe parameters comprising a form for *the probe* including a modulation profile for *the probe*;
>
> b) the first node receiving *the probe* from the second node, wherein *the probe* is generated in accordance with the first plurality of parameters and in accordance with a second plurality of parameters determined by the second node.

The other independent claim of the '690 Patent that recites a "probe" is Claim 1, which recites (emphasis added):

> 1. A method comprising:
>
> a) receiving in a first node, a probe request specifying a first plurality of parameters associated with the generation and transmission of *a probe*, wherein the first plurality of parameters at least specify content payload of *the probe* and a second node;

b) determining a second plurality of parameters associated with generation and transmission of *the probe*;

c) generating *the probe* in accordance with the first plurality of parameters and the second plurality of parameters, wherein *the probe* has a form dictated by the first plurality of parameters; and

d) transmitting *the probe* from the first node to the second node.

Defendant argues that a "probe," even in Claim 1, is necessarily a physical layer signal. In some cases, "[d]ifferent terms or phrases in separate claims may be construed to cover the same subject matter where the written description and prosecution history indicate that such a reading of the terms or phrases is proper." *Nystrom v. TREX Co., Inc.*, 424 F.3d 1136, 1143 (Fed. Cir. 2005). Defendant submits that the patent speaks only of generating physical layer ("PHY") packets. (Dkt. No. 104, at 18 (citing '690 Patent at 3:3–5, 3:40–64 & 5:59).) Defendant also submits authority that "[t]he preference for giving meaning to all terms, however, is not an inflexible rule that supersedes all other principles of claim construction." *SimpleAir, Inc. v. Sony Ericsson Mobile Commc'ns AB*, 820 F.3d 419, 429 (Fed. Cir. 2016) (citation omitted).

Defendant also cites the DOCSIS specification, which states "[a] probe is a wideband physical-layer signal . . . ." (Dkt. No. 104, Ex. 4, *Data-Over-Cable Service Interface Specifications, DOCSIS 3.1*, at 20 & 57 (CHARTER_ENTROPIC00101891 & CHARTER_ENTROPIC00101928).) This statement, however, is not set forth as a broadly applicable definition but rather is set forth as part of a discussion of a specific feature. *See id.*

On balance, using a "physical layer" probe is a specific feature of particular disclosed embodiments that should not be imported into the claims. *See Phillips*, 415 F.3d at 1323. To the extent Defendant maintains that a "probe" must be a "physical layer" probe because no other type of probe is disclosed in the specification, Defendant's argument perhaps may pertain to arguments regarding the enablement or written description requirements but does warrant importing such a limitation into the claims.

Further, the recital of "a probe" in Claim 1 and "a physical layer probe" in Claim 9, as set forth above, weighs at least somewhat further against Defendant's proposal of limiting "probe" to being a "physical layer probe." *See id.* at 1314 (noting that "terms are normally used consistently throughout the patent," and "[o]ther claims of the patent in question, both asserted and unasserted, can also be valuable sources of enlightenment as to the meaning of a claim term").

As for Defendant's proposal of referring to a "packet," Defendant submits that the patent relates to packet-based networks, disclosing for example:

> In the illustrated embodiment, the communications protocol specifies a packet based communications system. In this embodiment, physical layer (PHY) packets comprise preambles and payloads.

'690 Patent at 3:40–44. The specification, however, refers more broadly to a probe "signal." *Id.* at 1:48–57. As noted above, at the June 13, 2023 hearing, Defendant was amenable to replacing "packet" with "signal."

Finally, at the June 13, 2023 hearing, Defendant urged that Plaintiff is attempting to interpret "probe" to encompass *new* information, which Defendant argued is contrary to the specification and the plain meaning of "probe" as referring to a signal that is already known (so that it can be compared to a reference signal). Defendant's argument in this regard is persuasive at least so far as "probe" should be limited to a signal that can be compared to a reference signal having a known form, and this is consistent with the Description of the Related Art portion of the specification. *See* '690 Patent at 1:48–57 (reproduced above).

The Court therefore hereby construes these disputed terms as follows:

Term	Construction
"probe" ('362 Patent, Claim 11)	**"a signal transmitted to a network node that the network node can compare to a reference signal having a known form in order to determine characteristics of the channel on which the signal was transmitted"**
"physical layer probe" ('690 Patent, Claim 9)	**Plain meaning** (apart from the Court's construction of "probe," above)

11. "probe request"

"probe request" ('690 Patent, Claims 1, 7, 8, 9, 11, 15, 16)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	A request sent by a first network node to a second network node which defines the form of a probe to be generated and transmitted by the second network node. The probe request specifies at least the content payload of the probe.

(Dkt. No. 84, at A-11; Dkt. No. 97, at 19; Dkt. No. 104, at 19; Dkt. No. 115, Ex. A, at 7–12.)

(a) The Parties' Positions

Plaintiff argues that "[t]he plain language of the claims confirms that 'probe request' means exactly what it sounds like—a request for a probe." (Dkt. No. 97, at 19.) Plaintiff also argues that Defendant's proposed construction is confusing and incorporates features that are recited elsewhere in the claims. (*Id.*, at 20.)

Defendant responds that "'probe request' could not possibly have had a plain and ordinary meaning in the context of the alleged invention" because "[*t*]*he probe request is the invention*." (Dkt. No. 104, at 19.) Defendant submits that "the specification explains exactly

what this allegedly novel 'probe request' is." (*Id.*) Further, Defendant argues that "to whatever extent the inventor's definition of 'probe request' makes that definition redundant with other claim language, the inventor's definition still governs . . . ." (*Id.*, at 20.)

Plaintiff replies that "well-known components can be used or joined in novel ways," and "[h]ere, 'probe request' means simply a request for a probe," which "must meet certain criteria, but those are defined by the other elements of the claim, not by 'probe request' itself." (Dkt. No. 110, at 7.) Plaintiff also argues that "[Defendant's] resort to lexicography fails because the relied-upon passage is a description, not a definition which meets the high and 'exacting' legal hurdle." (*Id.* (citation omitted).)

At the June 13, 2023 hearing, Plaintiff argues that a "probe request" could specify things other than form, such as transmission power.

(b) Analysis

Claim 1 of the '690 Patent recites (emphasis added):

> 1. A method comprising:
>
> a) receiving in a first node, a *probe request* specifying a first plurality of parameters associated with the generation and transmission of a probe, wherein the first plurality of parameters at least specify content payload of the probe and a second node;
>
> b) determining a second plurality of parameters associated with generation and transmission of the probe;
>
> c) generating the probe in accordance with the first plurality of parameters and the second plurality of parameters, wherein the probe has a form dictated by the first plurality of parameters; and
>
> d) transmitting the probe from the first node to the second node.

The Brief Summary section of the specification states:

> The receiving node may generate a probe request that specifies a plurality of parameters to be used in such a "receiver determined" probe to generate a probe having the "form" specified by these parameters. Accordingly, the probe request specifies a plurality of parameters associated with the generation and transmission of a probe, including the content of a payload of the probe. In one embodiment, the parameters further include: the modulation profile for the probe; the payload

> content of the probe; the number of times to transmit the probe; the number of symbols for the payload of the probe; the preamble type for the probe; the cyclic-prefix length for the payload of the probe; the transmit power for the probe; and the transmit power scaling factor for the payload of the probe. Accordingly, the probe that is transmitted in response to the probe request will have a form dictated by the parameters specified in the probe request.

'690 Patent at 2:3–19.

Contrary to Defendant's suggestion that this disclosure amounts to a definition, no lexicography is apparent. That is, Defendant does not identify any expression of a clear intent by the patentee to set forth a definition for the term "probe request." *See Irdeto Access, Inc. v. EchoStar Satellite Corp.*, 383 F.3d 1295, 1301 (Fed. Cir. 2004) ("It is well-established that the patentee can act as his own lexicographer, so long as he *clearly* states any special definitions of the claim terms in the patent specification or file history.") (emphasis added) (citing *Vitronics*, 90 F.3d at 1582).

Nonetheless, "terms coined by the inventor are best understood by reference to the specification." *Intervet Inc. v. Merial Ltd.*, 617 F.3d 1282, 1287 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1315). Plaintiff replies that "'probe request' means simply a request for a probe," but Plaintiff does not demonstrate that the term "probe request" has any established meaning in the art. The above-reproduced disclosure explains that, as used in the '690 Patent, a probe request is sent by one network node to another network node and defines the form of a probe to be generated and transmitted.

As for Defendant's proposal that "[t]he probe request specifies at least the content payload of the probe," however, the above-reproduced disclosure refers to the payload but the above-reproduced claim language already specifically recites "the first plurality of parameters at least specify content payload of the probe and a second node," which weighs against including this specific requirement in the construction of "probe request." *See, e.g., Apple, Inc. v. Ameranth,*

Inc., 842 F.3d 1229, 1237 (Fed. Cir. 2016) ("Construing a claim term to include features of that term already recited in the claims would make those expressly recited features redundant.").

The Court therefore hereby construes **"probe request"** to mean **"a request, sent by one network node to another network node, that specifies the form of a probe to be generated and transmitted."**

12. "generating the probe in accordance with the first plurality of parameters and the second plurality of parameters, wherein the probe has a form dictated by the first plurality of parameters," "wherein the probe is generated in accordance with the first plurality of parameters and in accordance with a second plurality of parameters determined by the second node," and "the first plurality of probe parameters comprising a form for the probe including a modulation profile for the probe"

"generating the probe in accordance with the first plurality of parameters and the second plurality of parameters, wherein the probe has a form dictated by the first plurality of parameters" ('690 Patent, Claim 1) **"wherein the probe is generated in accordance with the first plurality of parameters and in accordance with a second plurality of parameters determined by the second node"** ('690 Patent, Claim 9) **"the first plurality of probe parameters comprising a form for the probe including a modulation profile for the probe"** ('690 Patent, Claim 9)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Indefinite

(Dkt. No. 84, at A-11–A-12; Dkt. No. 97, at 21; Dkt. No. 104, at 20; Dkt. No. 115, Ex. A, at 7–8 & 10–11.)

(a) The Parties' Positions

Plaintiff argues that these terms are not indefinite because "[a] POSITA would understand there are two sets of parameters—one set which relates to the probe's *form*, and another set relating to any characteristic of the probe." (Dkt. No. 97, at 21.)

Defendant argues that "the claims cover the form of the probe being determined only by the parameters in the probe request," and "[t]his renders the claims indefinite" because "[i]f the parameters determined by the probe transmitter are used to generate the probe, those parameters necessarily contribute to defining the form of the probe," and "it is impossible to imagine a parameter used to generate a probe that does not relate to its form." (Dkt. No. 104, at 21.)

Plaintiff replies that "the probe may be based on additional information, namely 'information that previously existed within the transmitting node.'" (Dkt. No. 110, at 8 (citing '690 Patent at 6:42–45).)

At the June 13, 2023 hearing, Defendant urged that any parameter used to generate something is related to its form. Plaintiff responded that the probe transmitter can define some parameters, such as transmission power, based on information existing within the transmitter.

(b) Analysis

Claim 1 of the '690 Patent recites (emphasis added):

> 1. A method comprising:
> a) receiving in a first node, a probe request specifying a first plurality of parameters associated with the generation and transmission of a probe, wherein the first plurality of parameters at least specify content payload of the probe and a second node;
> b) determining a second plurality of parameters associated with generation and transmission of the probe;
> *c) generating the probe in accordance with the first plurality of parameters and the second plurality of parameters, wherein the probe has a form dictated by the first plurality of parameters*; and
> d) transmitting the probe from the first node to the second node.

The "generating . . ." limitation thus involves a "first plurality of parameters" that dictates the form of the probe and a "second plurality of parameters" that is *not* recited as dictating the form of the probe. The manner in which "generating the probe" is "in accordance" with the "second plurality of parameters" thus is not recited.

Defendant does not show that this gives rise to any inconsistency. The same is true as to the ". . . is generated . . ." and "parameters" limitations recited in Claim 9 of the '690 Patent. The indefiniteness opinion of Defendant's expert is unpersuasive. (*See* Dkt. No. 104, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶ 84.) Moreover, the opinion of Plaintiff's expert is persuasive that the "second plurality of parameters" could, for example, affect a payload portion of a probe without affecting the form of the probe. (Dkt. No. 97, Ex. 7, Apr. 14, 2023 Kramer Decl. at ¶ 138.)

Also, Plaintiff persuasively argued at the June 13, 2023 hearing that the transmitter of a probe could define some non-form parameters, such as transmission power, timing, or destination, "based upon information that previously existed within the transmitting node." *See* '690 Patent at 6:33–45.

Finally, Defendant argues that "the specification says nothing about putting parameters into probe payloads." (Dkt. No. 104, at 22.) This argument perhaps may pertain to arguments regarding enablement or written description, but this does not raise any concern regarding indefiniteness.

The Court therefore hereby expressly rejects Defendant's indefiniteness argument, and Defendant presents no alternative proposed constructions.

The Court accordingly hereby construes these terms to have their **plain meaning**.

VIII. DISPUTED TERMS IN U.S. PATENT NO. 9,210,362

The '362 Patent, titled "Wideband Tuner Architecture," issued on December 8, 2015, and bears an earliest priority date of April 19, 2010. Plaintiff submits that the '362 Patent "relates generally to a receiver system configured to receive a number of channels across a broad radio frequency (RF) spectrum." Dkt. No. 97 at 5.

The Abstract of the '362 Patent states:

> A wideband receiver system comprises a mixer module, a wideband analog-to-digital converter (ADC) module, and digital circuitry. The mixer module is configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels. The wideband ADC module is configured to digitize the swatch [*sic*, swath] of frequencies comprising the plurality of desired television channels and the plurality of undesired television channels. The digital circuitry is configured to select the desired plurality of television channels from the digitized plurality of frequencies, and output the selected plurality of television channels to a demodulator as a digital datastream.

13. "downconverting . . . a plurality of frequencies" and Order of Steps in Claim 11

"downconverting . . . a plurality of frequencies" ('362 Patent, Claim 11)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Downconverting a plurality of frequencies of an analog radio frequency (RF) signal.
Order of Steps ('362 Patent, Claim 11)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Claimed steps must be performed in the order recited in the claim.

(Dkt. No. 84, at A-13; Dkt. No. 97, at 22 & 24; Dkt. No. 104, at 24; Dkt. No. 115, Ex. A, at 12–13.)

(a) The Parties' Positions

Plaintiff submits that "[t]here seems to be general agreement that downconverting is well-understood" and that "[t]he process brings 'down' the frequency of a signal, using a 'mixer' or a 'mixing' process." (Dkt. No. 97, at 23.) Plaintiff argues that no order of steps is required because "[t]here is no grammatical or logical reason why digitizing cannot occur before downconverting or *vice versa* since claim 11 states these steps are performed on the same object—the 'plurality of frequencies.'" (Dkt. No. 97, at 25.) Plaintiff also argues that "because the digitizing step does not refer to the output of the 'downconverting' step (but rather its input), the claim itself requires no particular order of those steps." (*Id.*, at 24.) Further, Plaintiff argues that "[v]iewed in light of the differently ordered embodiments disclosed in the specification, Charter's request for an order of the steps limitation is nothing more than a second attempt by Charter to require that the claimed downconverting is done on an analog signal only." (*Id.*, at 25–26.) Finally, Plaintiff argues that there is no basis for limiting the downconverting to only "radio frequency (RF)" signals. (*Id.*)

Defendant responds that "the language of claim 11 itself dictates that the steps be performed in the order written," and "even if the structure of the claim did not mandate the order of the steps (it does), the specification 'directly or implicitly requires' that the claims be performed in order." (Dkt. No. 104, at 24 & 25 (citation omitted).) "Finally," Plaintiff submits, "claim 11 is written to track the order in which the steps are performed in the specification." (*Id.*, at 26.)

Plaintiff replies that "read in light of the specification, the claim envisions digital and/or analog downconversion of desired and undesired channels." (Dkt. No. 110, at 9.)

At the June 13, 2023 hearing, Defendant argued that Plaintiff is attempting to excise the entire invention from the claim because the purported invention is to reduce the need for expensive analog-to-digital converters by downconverting *before* digitizing. *See* '362 Patent at 2:20–27 &

2:45–55. Plaintiff responded that the Defendant's argument is unavailing because the specification also discloses digital downconversion. *See id.* at 5:31–58 & 9:11–34.

(b) Analysis

"As a general rule, '[u]nless the steps of a method [claim] actually recite an order, the steps are not ordinarily construed to require one.'" *Mformation Techs., Inc. v. Research in Motion Ltd.*, 764 F.3d 1392, 1398 (Fed. Cir. 2014) (quoting *Interactive Gift Express, Inc. v. Compuserve, Inc.*, 256 F.3d 1323, 1342 (Fed. Cir. 2001)).

Courts apply a two-part test to determine whether a particular order of steps is required: "First, we look to the claim language to determine if, as a matter of logic or grammar, they must be performed in the order written," and "[i]f not, we next look to the rest of the specification to determine whether *it* directly or implicitly requires such a narrow construction." *Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1369–70 (Fed. Cir. 2003) (citation omitted).

Claim 11 of the '362 Patent recites (emphasis added):

> 11. A method comprising:
> in a wideband receiver system:
> *downconverting*, by a mixer module of said wideband receiver system, *a plurality of frequencies* that comprises a plurality of desired television channels and a plurality of undesired television channels;
> *digitizing*, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, *said plurality of frequencies* comprising said plurality of desired television channels and said plurality of undesired television channels;
> *selecting*, by digital circuitry of said wideband receiver system, said plurality of desired television channels from *said digitized plurality of frequencies*; and
> *outputting*, by said digital circuitry of said wideband receiver system, *said selected plurality of television channels* to a demodulator as a digital datastream.

In some cases, "the sequential nature of the claim steps is apparent from the plain meaning of the claim language." *See Mantech Envtl. Corp. v. Hudson Envtl. Servs., Inc.*, 152 F.3d 1368,

1376 (Fed. Cir. 1998); *see also E-Pass Techs., Inc. v. 3Com Corp.*, 473 F.3d 1213, 1222 (Fed. Cir. 2007) ("[B]ecause the language of most of the steps of its method claim refer to the completed results of the prior step, E–Pass must show that all of those steps were performed in order.").

Here, the "downconverting . . ." step and the "digitizing . . ." step both operate on the same "plurality of frequencies," and there is no reference to "completed results of the prior step." *Id.* Rather, the "downconverting . . ." step and the "digitizing . . ." step both refer to the same "plurality of frequencies" without any indication that one of these steps must necessarily be performed before the other. Further, because the "digitizing . . ." step could potentially be performed before the "downconverting . . ." step, the Court rejects Defendant's proposal to limit "downconverting . . . a plurality of frequencies" to downconverting a plurality of frequencies of an *analog* radio frequency (RF) signal.

The "selecting . . ." step, by contrast, refers to "said digitized plurality of frequencies." The "digitizing . . ." step must therefore be performed before the "selecting . . ." step. *Id.*

The "outputting . . ." step refers to "said selected plurality of television channels." The "selecting . . ." step must therefore be performed before the "outputting . . ." step. *Id.*

Finally, Defendant does not persuasively justify limiting the claim to "radio frequency (RF)" signals. Defendant's reliance on the "complex mixer module" 211/221 illustrated in Figure 2 is unavailing. (*See* Dkt. No. 104, at 25–26 (discussing '362 Patent at Fig. 2).) To the extent the specification discloses downconverting radio frequencies, the use of radio frequencies is a particular feature of disclosed embodiments that should not be imported into the claim. *See Phillips*, 415 F.3d at 1323.

The Court therefore hereby construes these disputed terms as follows:

Term	Construction
"downconverting . . . a plurality of frequencies" ('362 Patent, Claim 11)	**Plain meaning**
Order of Steps in Claim 11 of the '362 Patent	**In Claim 11 of the '362 Patent, the "digitizing . . ." step must be performed before the "selecting . . ." step, and the "selecting . . ." step must be performed before the "outputting . . ." step. No other order of steps is required.**

IX. DISPUTED TERMS IN U.S. PATENT NO. 10,135,682

The '682 Patent, titled "Method and System for Service Group Management in a Cable System," issued on November 20, 2018, and bears an earliest priority date of July 23, 2012. Plaintiff submits that the '682 Patent "relates generally to organizing cable modems (CMs) into service groups based on signal-to-noise ratio (SNR) related metrics." (Dkt. No. 97, at 5.)

The Abstract of the '682 Patent states:

> A cable modem termination system (CMTS) may determine, for a plurality of cable modems served by the CMTS, a corresponding plurality of SNR-related metrics. The CMTS may assigning [*sic*] the modems among a plurality of service groups based on the SNR-related metrics. For any one of the modems, the CMTS may configure physical layer communication parameters to be used by the one of the modems based on a SNR-related metric of a service group to which the one of the modems is assigned. The physical layer communication parameters may include one or more of: transmit power, receive sensitivity, timeslot duration, modulation type, modulation order, forward error correction (FEC) type, and FEC code rate. The CMTS and the modems may communicate using orthogonal frequency division multiplexing (OFDM) over a plurality of subcarriers, and the physical layer communication parameters may be determined on a per-subcarrier basis.

14. "a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics"

"a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics" ('682 Patent, Claim 1)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Indefinite

(Dkt. No. 84, at A-14; Dkt. No. 97, at 26; Dkt. No. 104, at 27; Dkt. No. 115, Ex. A, at 14.)

(a) The Parties' Positions

Plaintiff argues that "[a]ny POSITA familiar with hybrid fiber coaxial ('HFC') networks understands what is meant by an SNR profile and SNR-related metrics," and "the adjectives 'worst-case' and 'composite' have plain meanings to a POSITA." (Dkt. No. 97, at 26 (citations omitted).) Plaintiff also argues that "[t]he specification confirms the claim terms are used in accord with a POSITA's expectations." (*Id.*)

Defendant responds that "[t]here is nothing about this limitation that finds any support in the specification." (Dkt. No. 104, at 27.) Defendant argues: "In view of the specification, 'composite SNR-related metric' *cannot* mean a 'composite *best-case* SNR profile.' It can only refer to the 'worst-case.' And the claim is therefore indefinite, as there is no difference between 'composite SNR-related metric' and 'worst-case SNR profile.'" (*Id.*, at 28.)

Plaintiff replies that "Charter's indefiniteness position is a chain of argument ultimately resting on a false equivalence of 'composite SNR-related metric' and 'worst-case SNR profile,'" but "[t]hey are not the same thing." (Dkt. No. 110, at 9.) Plaintiff also submits that "composite metrics based on SNR-related metrics generally (not merely worst-case) are, in fact, disclosed." (*Id.* (citing '682 Patent at 4:40–52).)

At the June 13, 2023 hearing, Defendant argued that Plaintiff does not provide any purported plain meaning for this "composite" term. Defendant submitted that the specification discloses only a "composite worst-case SNR profile." *See* '682 Patent at 4:9–20. Defendant urged that the disputed term is indefinite because the "composite SNR-related metric" cannot be based on the "worst-case SNR profile" if they are both the same thing. Plaintiff responded that "composite" means that something is for more than one cable modem and that a "profile" is something that involves multiple attributes (such as several frequency ranges). Plaintiff concluded that a person of ordinary skill in the art would understand that the term "composite SNR-related metric" relates to multiple cable modems and could be a profile (such as for several different frequency ranges) or could instead be a single composite metric, such as an average.

(b) Analysis

Claim 1 of the '682 Patent recites (emphasis added):

> 1. A method comprising:
> determining, by a cable modem termination system (CMTS), for each cable modem served by said CMTS, a *corresponding signal-to-noise ratio (SNR) related metric*;
> assigning, by said CMTS, each cable modem among a plurality of service groups based on a respective *corresponding SNR-related metric*;
> generating, by said CMTS for each one of said plurality of service groups, *a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics* corresponding to said one of said plurality of service groups;
> selecting, by said CMTS, one or more physical layer communication parameter to be used for communicating with said one of said plurality of service groups based on said composite SNR-related metric; and
> communicating, by said CMTS, with one or more cable modems corresponding to said one of said plurality of service groups using said selected one or more physical layer communication parameter.

Defendant argues that the specification fails to distinguish between "a composite SNR-related metric" and "a worst-case SNR profile." This argument perhaps may pertain to arguments regarding enablement or written description, but Defendant does not show any lack of reasonable

certainty in the claim language itself. Rather, the claim merely recites a worst-case SNR profile that is based on the SNR-related metrics that correspond to each cable modem, and the composite SNR-related metric, in turn, is based on the worst-case SNR profile. The opinions of Plaintiff's expert are further persuasive in this regard. (*See* Dkt. No. 97, Ex. 7, Apr. 14, 2023 Kramer Decl. at ¶¶ 166 & 168–169; *see, e.g.,* '682 Patent at 4:9–20, 5:7–12 & 5:42–57 & Fig. 2C.) Plaintiff's arguments at the June 13, 2023 hearing (summarized above) are likewise persuasive.

The Court therefore hereby expressly rejects Defendant's indefiniteness argument, and Defendant presents no alternative proposed construction.

The Court accordingly hereby construes **"a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics"** to have its **plain meaning**.

15. "service group[s]"

"service group[s]" ('682 Patent)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	A "service group" is the complete set of downstream and upstream channels within a single CMTS that a single cable modem could potentially receive or transmit on.

(Dkt. No. 84, at A-15; Dkt. No. 97, at 28; Dkt. No. 104, at 28–29; Dkt. No. 115, Ex. A, at 14.)

(a) The Parties' Positions

Plaintiff argues that "[a] 'service group' is a plain English term, and the claim and specification confirm that the groups consist of cable modems (CMs), not *channels*." (Dkt. No. 97, at 28.) "Furthermore," Plaintiff argues, "Charter is attempting to join the upstream and downstream channels without basis in the claim language and contrary to the specification." (*Id.*)

Defendant responds that "[t]he DOCSIS specification itself provides the plain meaning definition of a 'cable modem service group' in the cable television industry (a definition Charter identified in the P.R. 4-3 statement but which Entropic entirely ignores in its brief) . . . ." (Dkt. No. 104, at 29 (citation omitted).)

Plaintiff replies that "[n]othing in the opposition overcomes the central point—the '682 Patent is described in terms of service groups consisting of groups of cable modems (CMs)." (Dkt. No. 110, at 9.) Plaintiff also argues that "whatever DOCSIS might have later said, its use of terms cannot overcome the '682 Patent's usage." (*Id.*, at 10.)

At the June 13, 2023 hearing, the parties submitted this disputed term without oral argument.

(b) Analysis

Claim 1 of the '682 Patent recites (emphasis added):

> 1. A method comprising:
> determining, by a cable modem termination system (CMTS), for each cable modem served by said CMTS, a corresponding signal-to-noise ratio (SNR) related metric;
> assigning, by said CMTS, each cable modem among a plurality of *service groups* based on a respective corresponding SNR-related metric;
> generating, by said CMTS for each one of said plurality of *service groups*, a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics corresponding to said one of said plurality of *service groups*;
> selecting, by said CMTS, one or more physical layer communication parameter to be used for communicating with said one of said plurality of *service groups* based on said composite SNR-related metric; and
> communicating, by said CMTS, with one or more cable modems corresponding to said one of said plurality of *service groups* using said selected one or more physical layer communication parameter.

Defendant relies on the following portion of a DOCSIS specification:

> Cable Modem Service Group

> In the HFC plant topology, the complete set of downstream and upstream channels within a single CMTS that a single Cable Modem could potentially receive or transmit on. In most HFC deployments, a CM-SG corresponds to a single Fiber Node. Usually, a CM-SG serves multiple CMs.

(Dkt. No. 104, Ex. 5, *Data-Over-Cable Service Interface Specifications, DOCSIS 3.0*, at 11 (CHARTER_ENTROPIC00101160).)

Because this definition refers to a set of channels that each cable modem can use (rather than a set of cable modems in a system of cable modems), this definition does not inform how the term "service group" is used in the '682 Patent, which refers to grouping cable modems:

> FIGS. 4A and 4B illustrate the network of FIG 1, with different groupings of CMs [(cable modems)] based on one or both of: measured performance metric(s) and location within the HFC network.
>
> * * *
>
> While FIGS. 3A and 3B depict SNR profiles and location as two separate bases on which to assign CMs to service groups, the two may be used in combination.

See '682 Patent at 2:24–27 & 6:39–41.

The Court therefore hereby expressly rejects Defendant's proposed construction. No further construction is necessary, particularly in light of the above-noted context provided by the specification. *See U.S. Surgical*, 103 F.3d at 1568; *see also O2 Micro*, 521 F.3d at 1362; *Finjan*, 626 F.3d at 1207; *ActiveVideo*, 694 F.3d at 1326; *Summit 6*, 802 F.3d at 1291; *Bayer*, 989 F.3d at 977–79.

The Court accordingly hereby construes **"service group[s]"** to have its **plain meaning**.

16. "[communicating with/corresponding to] said one of said plurality of service groups"

"[communicating with/corresponding to] said one of said plurality of service groups" ('682 Patent, Claim 1)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Indefinite

(Dkt. No. 84, at A-16; Dkt. No. 97, at 30; Dkt. No. 104, at 30; Dkt. No. 115, Ex. A, at 14–15.)

(a) The Parties' Positions

Plaintiff argues that "Claim 1 itself of the '682 Patent is clear on how service groups, composed of cable modems, and the CMTS communicate . . . ." (Dkt. No. 97, at 30.) Plaintiff also submits that "[t]he specification has a multitude of references to the communication with the service group by way of, for example, physical layer parameters since the invention could not work without communication." (*Id.* (citations omitted).) "Further," Plaintiff argues, "the terms 'communicating,' 'corresponding,' and 'plurality' each have plain English meanings that are well-understood, and the combination of the terms do not create any ambiguity." (*Id.*)

Defendant responds: "There is no antecedent basis for 'said one of said plurality of service groups,' and there is no way to know which one service group among the 'plurality of service groups' the 'communicating' and 'corresponding' steps should be performed on. The claim is therefore indefinite." (Dkt. No. 104, at 30.)

Plaintiff replies:

> The '682 Patent criticizes the folly of lumping all CMs together in a "lowest common denominator" approach. '682 Patent, 5:50–57. Instead, the '682 Patent groups CMs based on their performance (SNR). For each group, the invention can choose communication parameters based on group performance. The chosen parameters are used to communicate with that group. *E.g., id.* at 5:42–50. This is precisely what the claim does. The "generating" step requires creating a composite metric for each service group. The "selecting step" uses the composite metric for

a particular service group to choose one or more parameter(s) to use with *that* group. The "communicating" step uses the selected parameter(s) to communicate with *that* group.

(Dkt. No. 110, at 10.)

At the June 13, 2023 hearing, the parties submitted this disputed term without oral argument.

(b) Analysis

Claim 1 of the '682 Patent recites (emphasis added):

1. A method comprising:
determining, by a cable modem termination system (CMTS), for each cable modem served by said CMTS, a corresponding signal-to-noise ratio (SNR) related metric;
assigning, by said CMTS, each cable modem among *a plurality of service groups* based on a respective corresponding SNR-related metric;
generating, by said CMTS for *each one of said plurality of service groups*, a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics corresponding to *said one of said plurality of service groups*;
selecting, by said CMTS, one or more physical layer communication parameter to be used for communicating with *said one of said plurality of service groups* based on said composite SNR-related metric; and
communicating, by said CMTS, with one or more cable modems corresponding to *said one of said plurality of service groups* using said selected one or more physical layer communication parameter.

The recital of "a plurality of service groups" provides antecedent basis for "said plurality of service groups."

The parties dispute whether the recital of "*each one of* said plurality of service groups" provides antecedent basis for "*said one of* said plurality of service groups."

At first blush, the recital of "*said one* of said plurality of service groups" appears to fail to specify *which* one of the *plurality* of service groups. This is the opinion of Defendant's expert. (Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶ 97 ("there is no way to know which one service group among the 'plurality of service groups' is being referred to").)

A fair reading, however, is that "*said one of* said plurality of service groups" refers back to "each *one of* said plurality of service groups." In other words, the steps that refer to "said one of said plurality of service groups" must be performed for each and every one of the plurality of service groups. This is apparent on the face of the claim and is also consistent with Figure 3A of the '682 Patent referring to determining parameters "*per* service group," and the opinion of Plaintiff's expert is further persuasive. (*See* Dkt. No. 97, Ex. 7, Apr. 14, 2023 Kramer Decl. at ¶¶ 176–77.) The contrary opinion of Defendant's expert is unpersuasive. (Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶ 97.)

Indeed, the claim recites only *one* "one of said plurality of service groups," so the reference to "said one" is reasonably clear. Thus, to whatever extent this term is deemed to lack *explicit* antecedent basis, the antecedent basis is *implicit*. *See Energizer Holdings Inc. v. Int'l Trade Comm'n*, 435 F.3d 1366, 1371 (Fed. Cir. 2006) (holding that "an anode gel comprised of zinc as the active anode component" provided implicit antecedent basis for "said zinc anode"); *see also Ex Parte Porter*, 25 U.S.P.Q. 2d (BNA) 1144, 1145 (B.P.A.I. 1992) ("The term 'the controlled fluid' . . . finds reasonable antecedent basis in the previously recited 'controlled stream of fluid . . . .'"); *Fisher-Price, Inc. v. Graco Children's Prods.*, No. 05–1258, 154 F. App'x 903, 909 (Fed. Cir. Nov. 4, 2005) ("[a] claim is not invalid for indefiniteness if its antecedent basis is present by implication") (citations omitted). The burden is on Defendant to show a lack of reasonable certainty, and Defendant has not met that burden. *See Nautilus*, 572 U.S. at 910; *see also Sonix*, 844 F.3d at 1377.

The Court therefore hereby expressly rejects Defendant's indefiniteness argument, and Defendant presents no alternative proposed construction.

The Court accordingly hereby construes **"[communicating with/corresponding to] said one of said plurality of service groups"** to have its **plain meaning**.

X. CONCLUSION

The Court adopts the constructions set forth in this opinion for the disputed terms of the patents-in-suit, and as summarized below.

Disputed Term	The Court's Construction
"a data networking engine implemented in a first circuit that includes at least one processor . . ." ('775 Patent, Claim 18) "a cable modem engine implemented in a second circuit that includes at least one processor . . ." ('775 Patent, Claim 18)	Plain meanings.
"data bus" ('775 Patent, Claim 18)	Plain meaning
"wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine" ('775 Patent, Claim 18)	"wherein the cable modem engine and the data networking engine are not necessarily physically separate but are functionally separate such that the cable modem functions are performed only by the cable modem engine and the home networking functions are performed only by the data networking engine"
"DOCSIS functions" ('775 Patent, Claim 19)	Plain meaning.

"DOCSIS MAC processor" ('775 Patent, Claim 18) "DOCSIS controller" ('775 Patent, Claim 18)	Plain meanings.
"network management messages" ('826 Patent, Claim 1)	"messages which report on the network based on the measured characteristics"
"operable to" ('008 Patent, Claim 1)	"configured to"
"digitize a received signal spanning an entire television spectrum comprising a plurality of television channels" ('008 Patent, Claim 1)	Plain meaning.
"signal monitor" "data processor" "channelizer" ('008 Patent, Claim 1)	Plain meanings.
"probe" ('690 Patent, Claims 1, 7, 8, 9, 11)	"a signal transmitted to a network node that the network node can compare to a reference signal having a known form in order to determine characteristics of the channel on which the signal was transmitted"
"physical layer probe" ('690 Patent, Claim 9)	Plain meaning (apart from the Court's construction of "probe," above).
"probe request" ('690 Patent, Claims 1, 7, 8, 9, 11, 15, 16)	"a request, sent by one network node to another network node, that specifies the form of a probe to be generated and transmitted"

"generating the probe in accordance with the first plurality of parameters and the second plurality of parameters, wherein the probe has a form dictated by the first plurality of parameters" ('690 Patent, Claim 1) "wherein the probe is generated in accordance with the first plurality of parameters and in accordance with a second plurality of parameters determined by the second node" ('690 Patent, Claim 9) "the first plurality of probe parameters comprising a form for the probe including a modulation profile for the probe" ('690 Patent, Claim 9)	Plain meanings.
"downconverting . . . a plurality of frequencies" ('362 Patent, Claim 11)	Plain meaning.
Order of Steps ('362 Patent, Claim 11)	In Claim 11 of the '362 Patent, the "digitizing . . ." step must be performed before the "selecting . . ." step, and the "selecting . . ." step must be performed before the "outputting . . ." step. No other order of steps is required.
"a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics" ('682 Patent, Claim 1)	Plain meaning.
"service group[s]" ('682 Patent)	Plain meaning.

"[communicating with/corresponding to] said one of said plurality of service groups" ('682 Patent, Claim 1)	Plain meaning.

The parties are **ORDERED** that they may not refer, directly or indirectly, to each other's claim construction positions in the presence of the jury. Likewise, the parties are **ORDERED** to refrain from mentioning any portion of this opinion, other than the actual definitions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the definitions adopted by the Court.

So ORDERED and SIGNED this 26th day of June, 2023.

RODNEY GILSTRAP
UNITED STATES DISTRICT JUDGE

Exhibit 1001

U.S. Patent No. 9,210,362

Customer No.: 000027683

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Telephone [214] 651.5000
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US009210362B2

(12) **United States Patent**
Reddy et al.

(10) **Patent No.: US 9,210,362 B2**
(45) **Date of Patent: *Dec. 8, 2015**

(54) **WIDEBAND TUNER ARCHITECTURE**

(71) Applicant: **MaxLinear, Inc.**, Carlsbad, CA (US)

(72) Inventors: **Madhukar Reddy**, Carlsbad, CA (US); **Curtis Ling**, Carlsbad, CA (US); **Tim Gallagher**, Carlsbad, CA (US)

(73) Assignee: **MaxLinear, Inc.**, Carlsbad, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/614,543**

(22) Filed: **Feb. 5, 2015**

(65) **Prior Publication Data**

US 2015/0156535 A1 Jun. 4, 2015

Related U.S. Application Data

(63) Continuation of application No. 13/962,871, filed on Aug. 8, 2013, which is a continuation of application No. 12/762,900, filed on Apr. 19, 2010, now Pat. No. 8,526,898.

(60) Provisional application No. 61/170,526, filed on Apr. 17, 2009.

(51) **Int. Cl.**

H04B 1/16	(2006.01)
H04N 5/50	(2006.01)
H04B 1/00	(2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ***H04N 5/50*** (2013.01); ***H04B 1/0014*** (2013.01); ***H04N 21/4263*** (2013.01); ***H04N 21/4383*** (2013.01); ***H04N 21/454*** (2013.01); ***H04N 21/6193*** (2013.01)

(58) **Field of Classification Search**

USPC 455/131, 140, 207, 214, 313, 315, 323, 455/324, 325, 334

See application file for complete search history.

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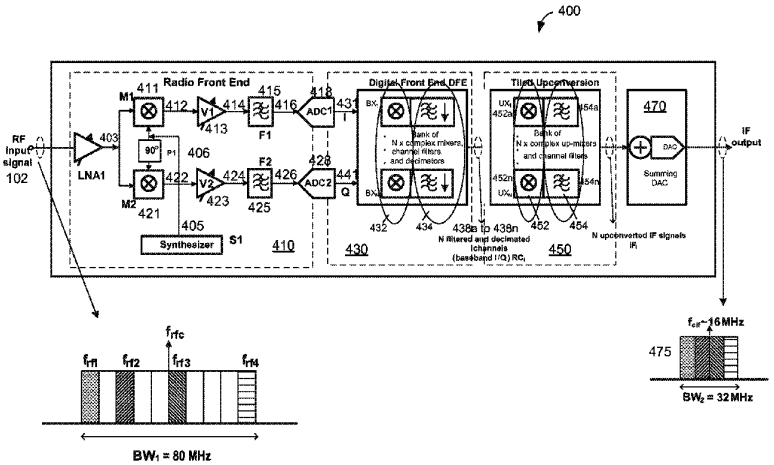
Primary Examiner — Blane J Jackson

(74) *Attorney, Agent, or Firm* — McAndrews, Held & Malloy, Ltd.

(57) **ABSTRACT**

A wideband receiver system comprises a mixer module, a wideband analog-to-digital converter (ADC) module, and digital circuitry. The mixer module is configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels. The wideband ADC module is configured to digitize the swatch of frequencies comprising the plurality of desired television channels and the plurality of undesired television channels. The digital circuitry is configured to select the desired plurality of television channels from the digitized plurality of frequencies, and output the selected plurality of television channels to a demodulator as a digital datastream.

20 Claims, 10 Drawing Sheets



(51) **Int. Cl.**

H04N 21/426	(2011.01)
H04N 21/438	(2011.01)
H04N 21/454	(2011.01)
H04N 21/61	(2011.01)

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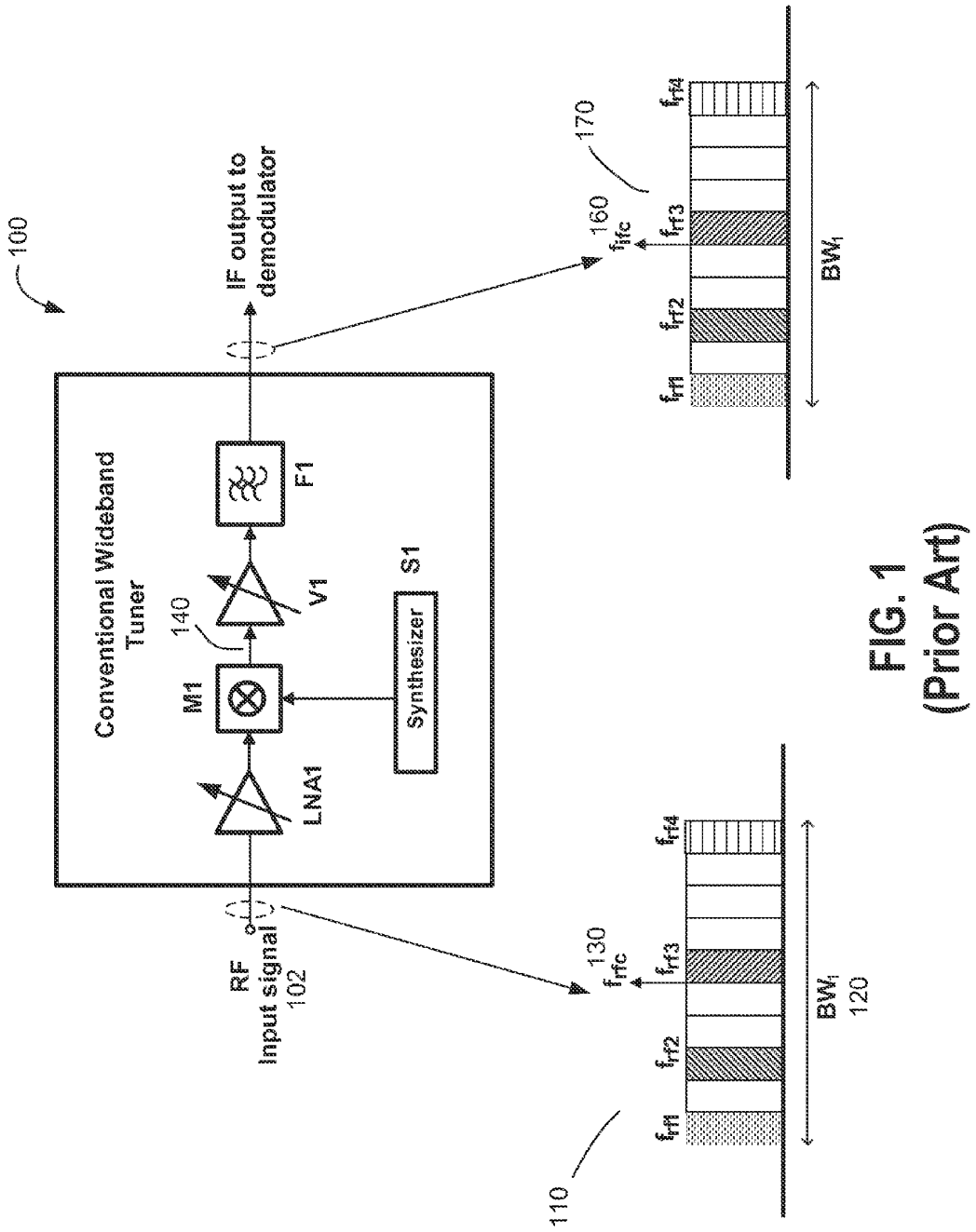


FIG. 1
(Prior Art)

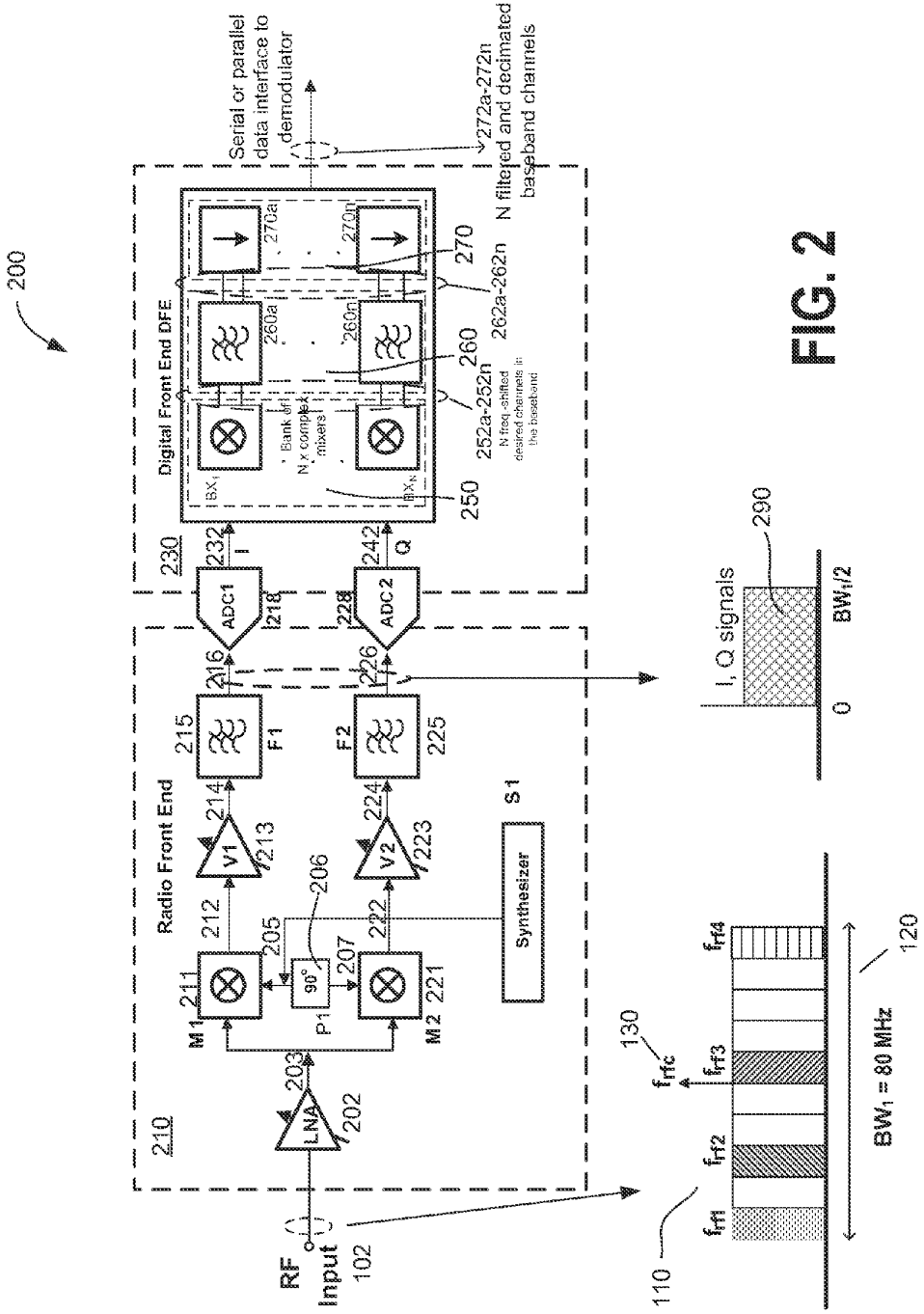

200
Digital Front End DFE
Serial or parallel data interface to demodulator
272a-272n
N filtered and decimated baseband channels
270
262a-262n
260
252a-252n
N freq.-shifted desired channels in the baseband
250
230
ADC1
ADC2
232
242
I
Q
218
228
216
226
F1
F2
215
225
214
224
V1
V2
213
223
Radio Front End
S1
Synthesizer
206
212
222
205
207
M1
M2
211
221
90°
P1
203
LNA
202
210
RF Input
102
I, Q signals
290
BW1/2
0
130
110
120
BW1 = 80 MHz

FIG. 2

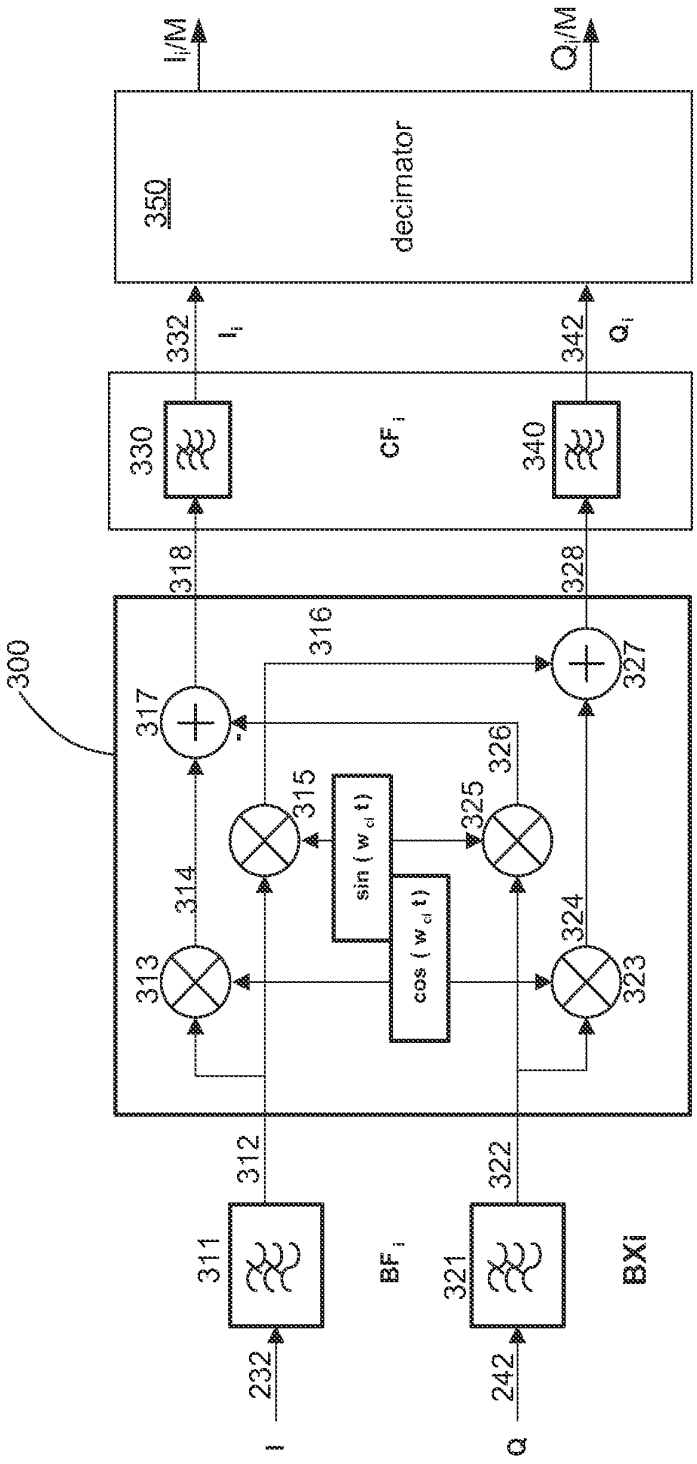

I_i/M
Q_i/M
350
decimator
332
I_i
342
Q_i
330
CF_i
340
318
328
316
300
317
327
326
315
sin (w_ct)
325
314
324
313
cos (w_ct)
323
312
322
311
BF_i
321
BXi
232
242
I
Q

FIG. 3

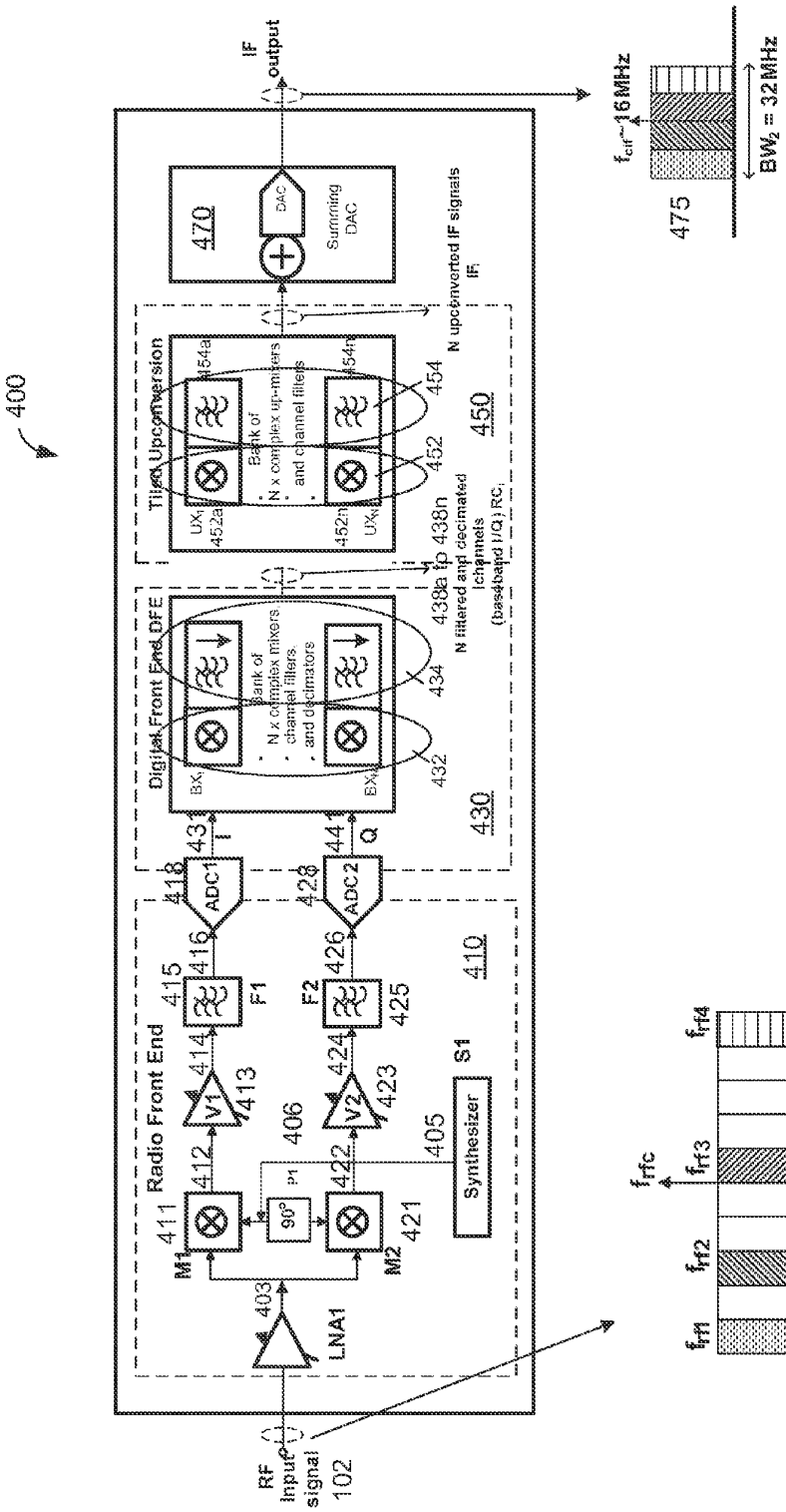

400
RF input signal 102
LNA1
403
M1
M2
411
421
90°
P1
412
422
406
405
Synthesizer
S1
V1
V2
413
423
414
424
415
425
F1
F2
416
426
Radio Front End
410
ADC1
ADC2
418
428
43
44
I
Q
Digital Front End DFE
Bank of
N x complex mixers
channel filters
and decimators
BX1
BXN
432
434
430
N filtered and decimated
I channels
(baseband I/Q) RC1
438a
438n
fp
Tiled Upconversion
Bank of
N x complex up-mixers
and channel filters
UX1
UXN
452a
452n
454a
454n
454
452
450
N upconverted IF signals
IF1
470
DAC
Summing
DAC
IF
output
475
fclr~16MHz
BW2 = 32MHz
frfc
frf1
frf2
frf3
frf4
BW1 = 80 MHz

FIG. 4

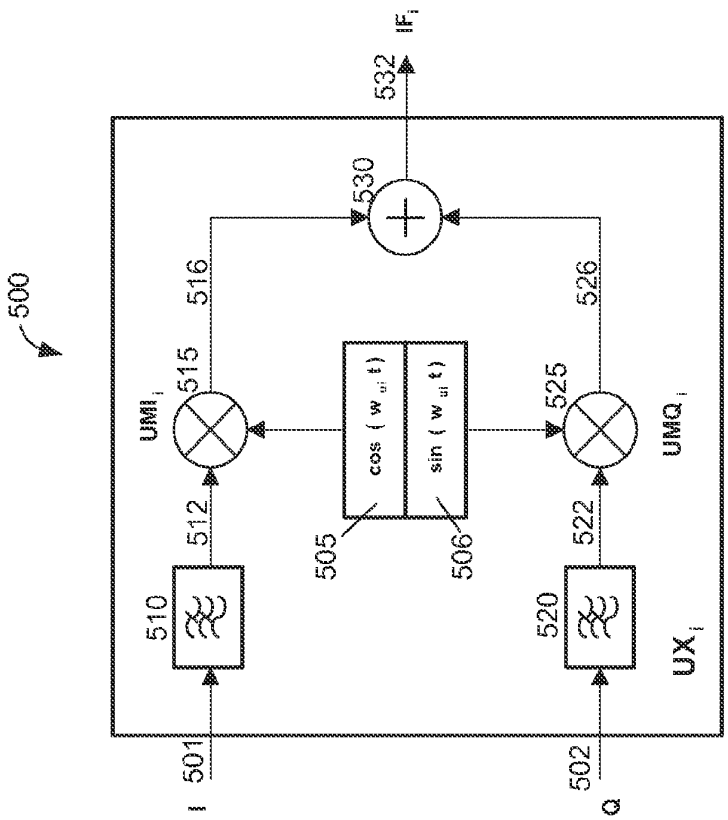

500
532
IF_i
530
516
526
515
525
UMI_i
UMQ_i
cos (w_ui t)
sin (w_ui t)
505
506
512
522
510
520
UX_i
501
502
I
Q

FIG. 5

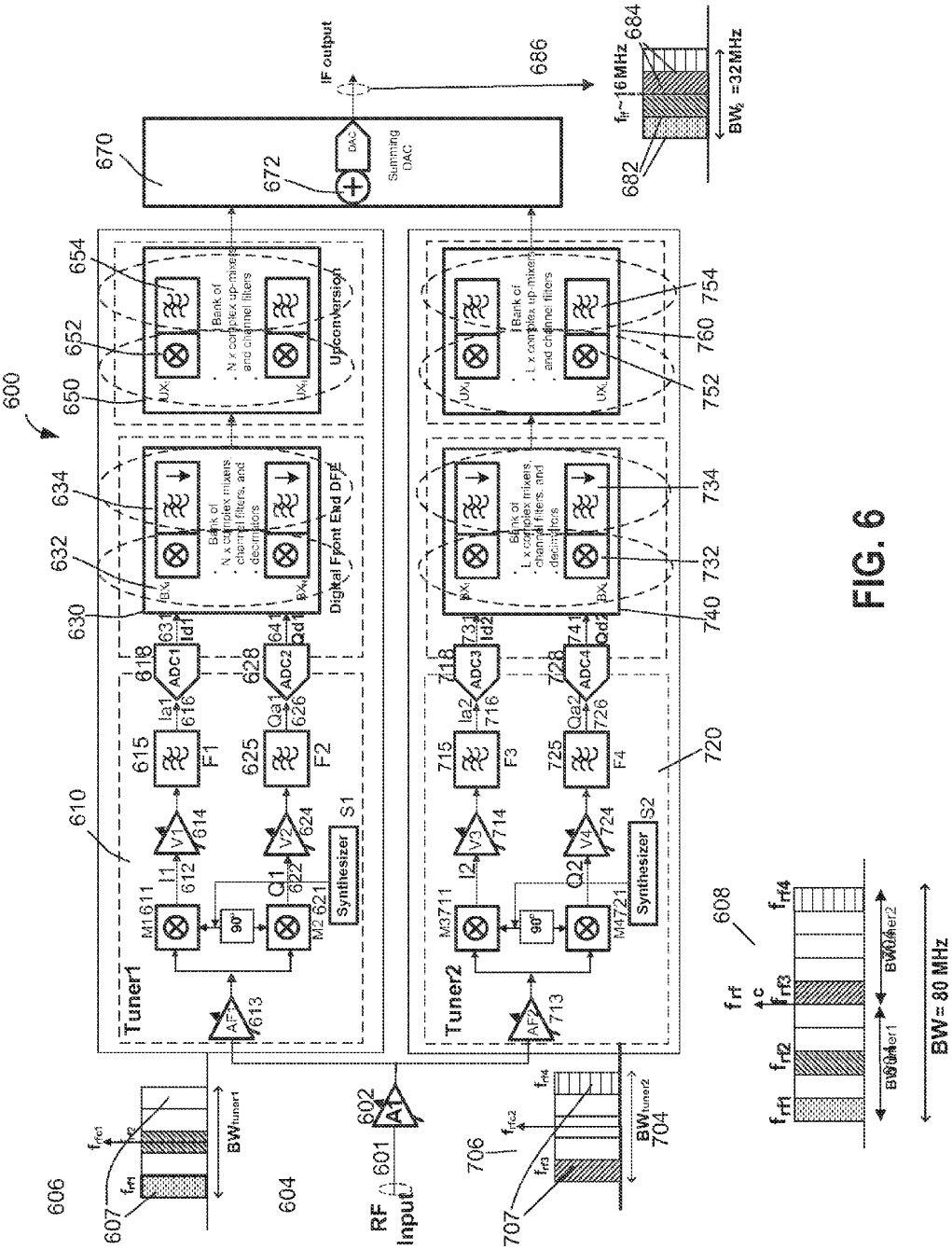

600
610
Tuner1
Tuner2
720
Digital Front End DFE
Bank of N x complex mixers, channel filters, and decimators
Bank of L x complex up-mixers and channel filters
Upconversion
Summing DAC
IF output
RF Input
Synthesizer
S1
S2
ADC1
ADC2
ADC3
ADC4
F1
F2
F3
F4
AF
AT
90°
M1 611
M2 621
M3 711
M4 721
V1 614
V2 624
V3 714
V4 724
672
670
686
682
684
602
601
606
607
604
706
707
704
608
BW = 80 MHz

FIG. 6

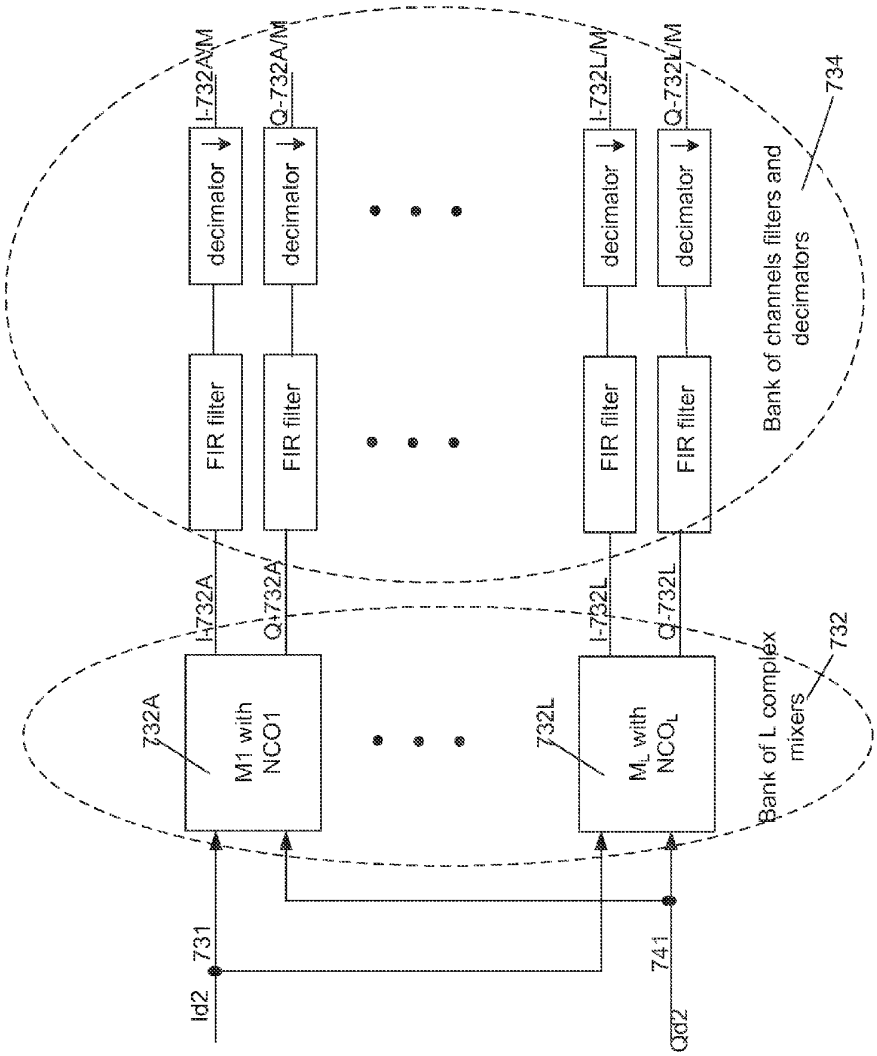

I-732A/M
Q-732A/M
I-732L/M
Q-732L/M
decimator
FIR filter
Bank of channels filters and decimators
734
I-732A
Q-732A
I-732L
Q-732L
732A
M1 with NCO1
732L
ML with NCOL
Bank of L complex mixers
732
731
741
Id2
Qd2

FIG. 7

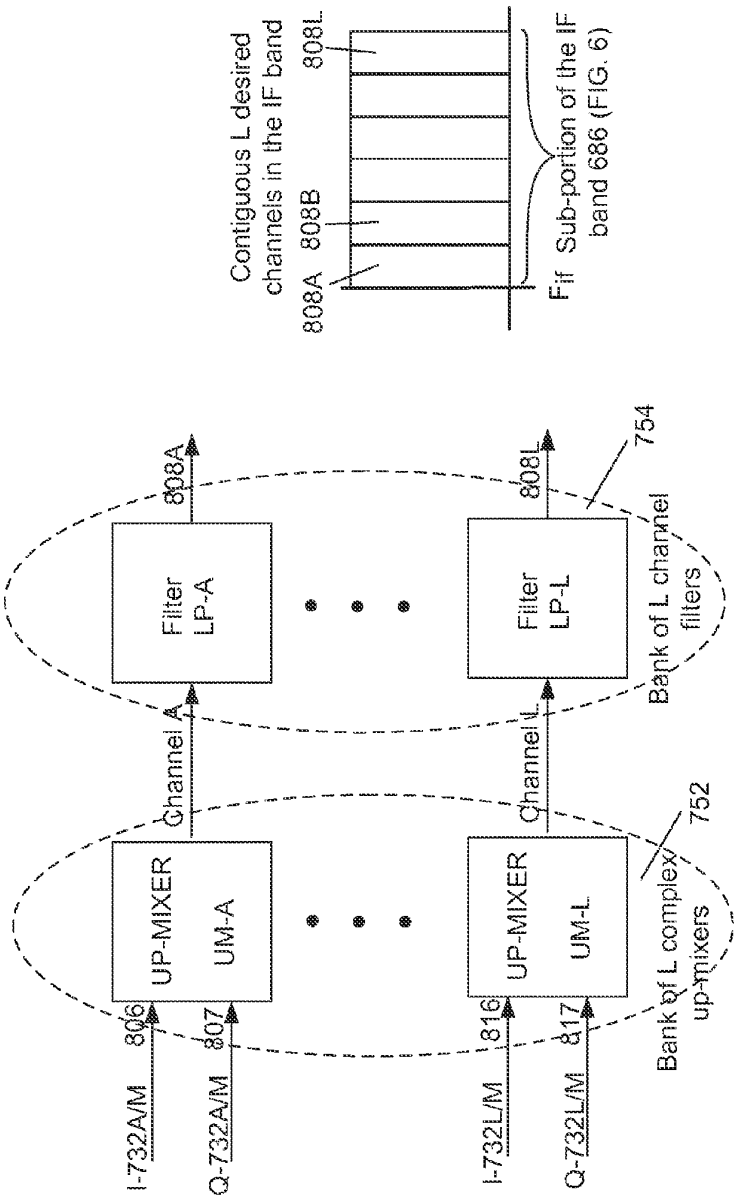

Contiguous L desired channels in the IF band
808A
808B
808L
Fif
Sub-portion of the IF band 686 (FIG. 6)
754
Bank of L channel filters
Filter LP-A
Filter LP-L
808A
808L
Channel A
Channel L
UP-MIXER UM-A
UP-MIXER UM-L
752
Bank of L complex up-mixers
806
807
816
817
I-732A/M
Q-732A/M
I-732L/M
Q-732L/M

FIG. 8

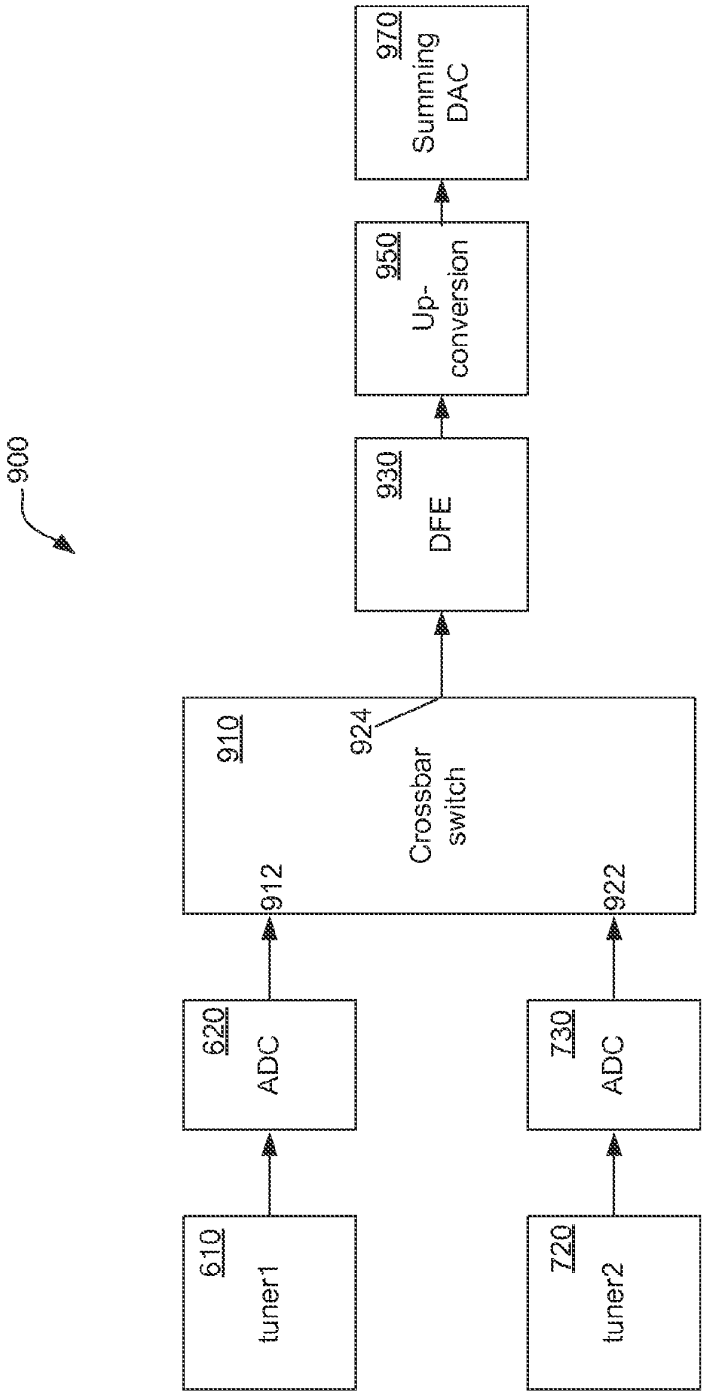

900
610
tuner1
620
ADC
720
tuner2
730
ADC
910
Crossbar switch
912
922
924
930
DFE
950
Up-conversion
970
Summing DAC

FIG. 9

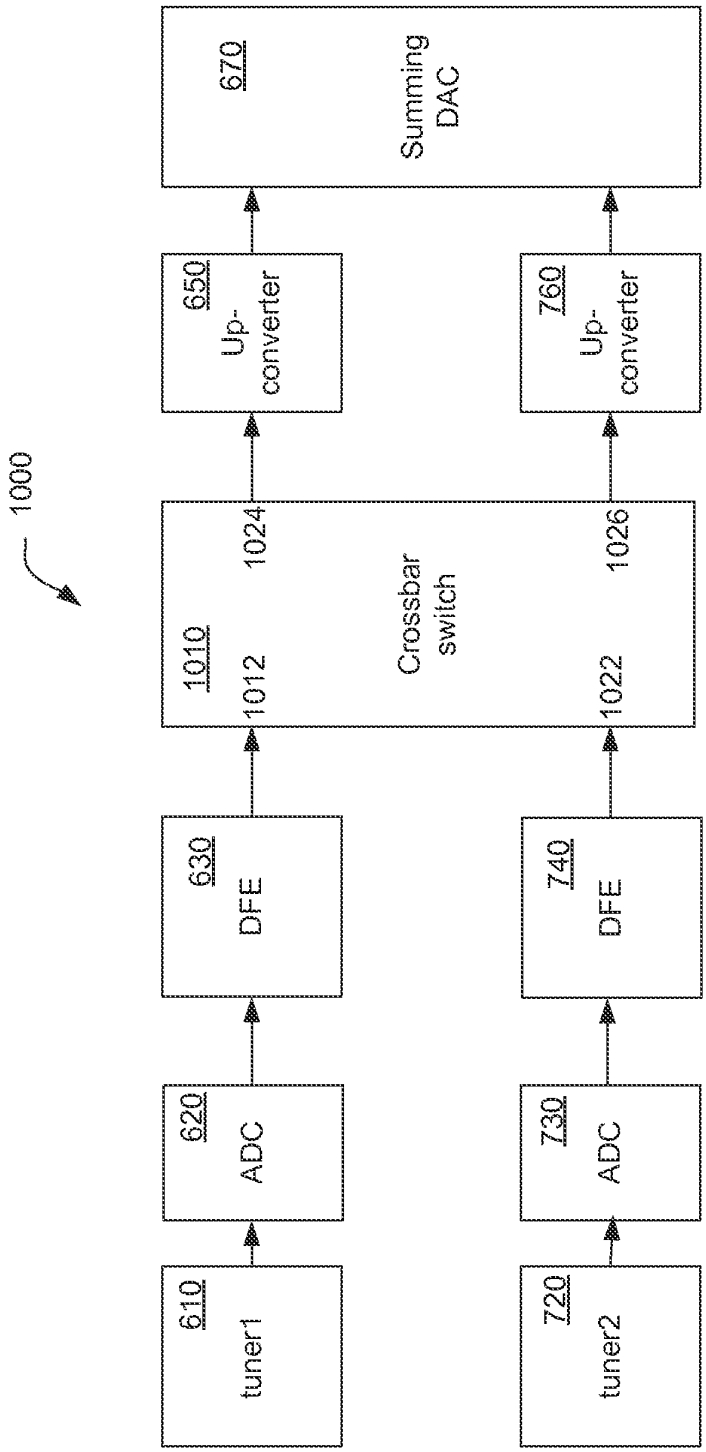

1000
610
tuner1
620
ADC
630
DFE
1010
1012
1022
Crossbar switch
1024
1026
650
Up-converter
670
Summing DAC
720
tuner2
730
ADC
740
DFE
760
Up-converter

FIG. 10

WIDEBAND TUNER ARCHITECTURE

PRIORITY CLAIM

This application is a continuation of U.S. patent application Ser. No. 13/962,871 filed on Aug. 8, 2013, which is a continuation of U.S. patent application Ser. No. 12/762,900 filed on Apr. 19, 2010 (now U.S. Pat. No. 8,526,898), which claims the benefit of priority to U.S. provisional application 61/170,526 filed Apr. 17, 2009. Each of the above referenced documents is hereby incorporated by reference in its entirety.

BACKGROUND

This invention relates to wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum. In particular, the invention relates to wideband receiver systems that are capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum and grouping them into a contiguous, or substantially-contiguous, frequency spectrum.

Receivers used to down-convert and selectively filter TV channels are referred to as tuners, and tuners designed to concurrently receive several TV channels are referred to as wideband tuners. Existing tuners for these applications down-convert a swath of channels to an intermediate frequency, which are then sent to a demodulator. Because the swath of channels is not contiguous, this swath includes the desired channels as well as undesired channels. The demodulator employs a high-speed data converter to capture this swath of desired and undesired channels in the digital domain and subsequently filters out the desired channels.

In general, television channels broadcasted over the air or over cable networks are distributed across a broad frequency spectrum. That is, the channel frequencies may not be adjacent to each other. In certain applications such as DVR and picture-in-picture, the receiver system may have to concurrently receive several desired channels that may or may not be contiguous. The wideband receiver requirement poses a trade-off to the system to limit either the dynamic range of the wideband tuner or reduce the bandwidth covered by the tuner so that fewer channels may be received and processed by the demodulator.

FIG. **1** shows a conventional wideband tuner **100**. Tuner **100** may be a direct conversion tuner and includes a low noise amplifier LNA1 having an input terminal coupled to a radio frequency (RF) input signal **102** and an output terminal coupled to a mixer M1. The RF signal may include one or more television channels receiving from a cable network via an RF connector or wirelessly via an antenna. The RF input signal may include the VHF and UHF television channels in a terrestrial television broadcasting system or the CATV channels in cable networks. In order to receive all broadcasted channels present in the RF input signal, LNA1 must necessarily have a wide tuning range, high linearity, and low noise. Mixer M1 is coupled to a synthesizer S1 that can generate an oscillator frequency located around the center of the RF signal. Mixer M1 frequency down-converts the received RF input signal to a more convenient intermediate frequency (IF) band. Tuner **100** includes an amplifier V1 having a programmable gain for amplifying the IF signal, which is then band-pass filtered by a filter F1 before outputting to a demodulator.

In general, the RF signal includes multiple desired channels that are located in non-contiguous portions of a radio frequency spectrum. As shown in FIG. **1**, the swath of channels **110** occupies a bandwidth BW1 **120** at an RF center frequency f_{rfc} **130**. Synthesizer S1 may be tuned to a frequency around the center frequency f_{rfc} **130** for mixing channels **110** to an intermediate frequency f_{ifc} **160**, the frequency down-mixed channels **140** are amplified by amplifier V1 and then filtered by F1 to produce a swath of channels **170** centered around frequency f_{ifc} **160**. In an exemplary application shown in FIG. **1**, bandwidth BW1 contains 10 channels. In the case where channels are TV channels that are spaced at either 6 MHz or 8 MHz in most parts of the world, bandwidth BW1 **120** would span from 60-80 MHz, i.e., the down-converted bandwidth at the intermediate frequency would require a bandwidth equal to at least BW1, or at least 80 MHz when such architecture is used. It is noted that in other applications where the desired RF channels are located in the low band such as channels numbers 2 to 6 (VHF in the terrestrial TV broadcast or CATV) and in the high band such as channels numbers 14 to 83 of the UHF TV broadcast or channel numbers 63-158 of the CATV's ultra band, the bandwidth BW1 can be 800 MHz or higher. This wide bandwidth of 800 MHz would require a very expensive digital processing circuitry such as very high-speed analog to digital conversion and high-speed processor in the demodulator.

It is desirable to have wideband receiver systems that can increase the dynamic range without requiring expensive data conversion, filtering and channel selection at the demodulator.

BRIEF SUMMARY

An embodiment of the present invention includes a wideband receiver system that is configured to concurrently receive multiple radio frequency (RF) channels including a number of desired channels that are located in non-contiguous portions of a frequency spectrum and group the desired channels in a contiguous or substantially-contiguous frequency band at an intermediate frequency spectrum, where the term "substantially-contiguous" includes spacing the desired channels close to each other (e.g. as a fraction of the total system bandwidth, or relative to a channel bandwidth) but with a spacing that can be variable to accommodate the needs of overall system. The term "contiguous" heretofore encompasses "substantially-contiguous." The term "spacing" is referred to as the frequency difference between adjacent channels. The system includes a wideband receiver having a complex mixer module for down-shifting the multiple RF channels and transforming them to an in-phase signal and a quadrature signal in the baseband or low intermediate frequency (IF) band. The system further includes a wideband analog-to-digital converter module that digitizes the in-phase and quadrature signals. The digital in-phase and quadrature signals are provided to a digital frontend module that contains a bank of complex mixers that frequency-shift the number of desired channels to a baseband where the desired channels are individually filtered.

The digital frontend module may also include a decimator module that decimates the desired RF channels by a factor M before demodulating them to a digital data stream.

In certain embodiments of the present invention, the wideband receiver system additionally includes an up-converter module having multiple complex up-mixers, each of the complex up-mixers is configured to frequency up-shift each one of the desired RF channels to a sub-portion of an IF spectrum, wherein all sub-portions of the desired channels are adjacent to each another and form a contiguous frequency band in the IF spectrum. The act of frequency shifting the desired channels to the IF spectrum allows the wideband receiver system

to directly interface with commercially available demodulators. Allowing the spacing of the desired channels in the contiguous spectrum to be variable allows a system to optimize placement of these desired channels for the purposes of avoiding sensitive portions of the spectrum which may either be vulnerable to spurious signals and interference; or which may generate interference directly or as a harmonic product, to other systems.

In another embodiment of the present invention, a multi-tuner receiver system having two or more tuners is provided to receive multiple desired RF channels that extend over several non-contiguous sub-portions of a broad frequency spectrum and group them into a contiguous frequency spectrum. The multi-tuner system includes at least a first tuner that processes a first sub-portion of the broad frequency spectrum into a first in-phase signal and a first quadrature signal and a second tuner that processes a second sub-portion of the broad frequency spectrum into a second in-phase signal and a second quadrature signal. The multi-tuner receiver system further includes a first analog-to-digital converter module that digitizes the first in-phase and quadrature signals and a second analog-to-digital converter module that digitizes the second in-phase and quadrature signals. In addition, the multi-tuner system includes a first digital frontend module having a first number of complex mixers corresponding to a first number of the desired RF channels located in the first sub-portion of the broad frequency spectrum and a second digital frontend module having a second number of complex mixers corresponding to a second number of the desired RF channels located in the second sub-portion of the broad frequency spectrum. The first digital frontend module frequency shifts the first number of the desired RF channels to a first plurality of baseband signals and the second digital frontend module frequency shifts the second number of the desired RF channels to a second plurality of baseband signals.

The multi-tuner system further includes a first up-converter module having a plurality of N complex mixers, wherein N is an integer value equal to the number of desired channel. The first up-converter module frequency up-shifts the first plurality of the baseband signals to a first portion of an intermediate frequency. In addition, the multi-tuner system includes a second up-converter module that frequency up-shifts the second plurality of the baseband signals to a second portion of an intermediate frequency. The first and the second portions of the intermediate frequency are non-overlapping and located adjacent to each other to form a contiguous intermediate frequency (IF) band. The multi-tuner system further includes a digital-to-analog converter that converts the contiguous IF band to an analog waveform signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic block diagram of a conventional wideband tuner;

FIG. **2** is a schematic block diagram of a wideband receiver system according to an embodiment of the present invention;

FIG. **3** is a simplified circuit diagram of a complex down-mixer according to an embodiment of the present invention;

FIG. **4** is a simplified schematic block diagram of a wideband receiver system according to another embodiment of the present invention;

FIG. **5** is a simplified circuit diagram of a complex up-mixer according to an embodiment of the present invention;

FIG. **6** is a simplified schematic block diagram of a wideband multi-tuner receiver system according to an embodiment of the present invention;

FIG. **7** is a block diagram illustrating an exemplary digital front end according to an embodiment of the present invention in more detail;

FIG. **8** is a block diagram illustrating an exemplary tiled up-converter module according to an embodiment of the present invention in more detail;

FIG. **9** is a simplified block diagram of a wideband multi-tuner receiver system **900** according to an embodiment of the present invention; and

FIG. **10** is a simplified block diagram of a wideband multi-tuner receiver system **1000** according to another embodiment of the present invention.

DETAILED DESCRIPTION

FIG. **2** is a schematic block diagram of a wideband receiver system **200** according to an embodiment of the present invention. Wideband receiver system **200** includes a radio front end **210** and a digital front end **230**. Radio front end **210** may be a single very wide-band tuner receiver that captures the desired swath of channels located in non-contiguous portions of the spectrum having a frequency bandwidth BW1 **120**. In this example, the number of available channels in BW1 **120** is assumed to be 10 with each channel occupying an 8 MHz bandwidth for a total of 80 MHz. Radio front end **210** is shown as including a low noise amplifier LNA **202** having an input terminal configured to receive an RF input signal **102**. In the example shown, RF signal **102** includes four desired RF channels having the respective carrier frequency f_{rf1}, f_{rf2}, f_{rf3}, and f_{rf4} that are located in non-contiguous portions of the wide frequency spectrum BW1. It is understood, however, that spectrum BW1 **120** may have any other number of desired frequencies that are not contiguous. LNA **202** has a very low noise figure and very high linearity and a wide tuning range (i.e., very high IIP2 and IIP3 intercept points) to maximize a signal-to-noise-and distortion ratio (SNDR) at the amplifier output. LNA **202** may have a programmable gain to amplify RF signal **102** to adequate voltage levels for mixers M1 **211** and M2 **221**.

Mixers M1 **211** and M2 **221** may be conventional mixers formed using, for example, differential Gilbert cells. Each of the mixers **211** and **221** multiplies (mixes) an amplified RF signal **203** with a respective first oscillator frequency signal **205** and a second oscillator frequency signal **207** to generate an in-phase signal **212** and a quadrature signal **222** that have a phase shift of 90° degree between them. Mixers **211** and **221** are identical so that the amplitude of the in-phase signal **212** and quadrature signal **222** are the same. The first and second oscillator frequencies **205** and **207** are identical and have a 90° degree phase shift generated through a 90° degree phase shifter P1 **206**. Synthesizer S1 may be a single local oscillator operable to generate the oscillator frequency **205** for converting the receive RF signal **102** to a zero-IF or low-IF band. Synthesizer S1 can be a coarse (large step) phase locked loop. Synthesizer S1 can also be programmable to cover the wide-band frequency of the analog and digital terrestrial broadcast and/or the cable television system. The RF signal **102** may have relatively uniform signal strength in a cable network. However, its signal strength may extend in several orders of magnitude in a terrestrial broadcast system, thus, LNA **202** and/or mixers M1 **211**, M2 **221** are required to have a relatively high dynamic range to handle the large variations in the signal strength.

In-phase signal **212** and quadrature signal **222** are further amplified and filtered by respective amplifiers V1 **213**, V2 **223** and filters F1 **215**, F2 **225** to generate a filtered in-phase signal **216** and a filtered quadrature signal **226**. Filters F1 **215**

and F2 **225** may be passive or active low-pass filters to filter out any unwanted frequency components of the signals **214** and **224** before digitizing them for further processing in digital front end **230**. It is understood that the in-phase path **216** and the quadrature path **226** must have the same amplitude spectrum and maintain a fixed phase relationship, i.e., amplifiers V1 **213**, V2 **223** and filters F1 **215**, F2 **225** must be substantially identical. Because the two paths **216** and **226** are in quadrature, the spectral components from both positive and negative frequencies can be overlaid so that the bandwidth (cutoff frequency) of filters F1 **215** and F2 **225** can be one half of the BW1 bandwidth **120**.

Analog-to-digital converters ADC1 **218** and ADC2 **228** are high-speed (i.e., high sampling rate) converters to maximize the dynamic range. In an exemplary application, radio front end **210** operates as a nominal zero-IF down-mixer so that signals **216** and **226** have a nominal bandwidth **290** equal to one half of the RF signal bandwidth BW1 thanks to the complex down-mixer architecture. In other embodiment, radio front end **210** operates as a low-IF down-mixer so that the nominal bandwidth **290** of signals **216** and **226** is greater than one half of the bandwidth BW1. In practice, the sampling rate of ADC1 **218** and ADC2 **228** is chosen to be higher than the Nyquist sampling requirement, i.e., the filtered analog quadrature signals **216** and **226** may be over-sampled in order to reduce or avoid aliasing of undesired signals into the digitized I and Q signals.

ADC1 **218** generates a digital signal I **232** that is a digital representation of the analog filtered signal **216**; ADC2 **228** generates a digital signal Q **242** that is a digital representation of the analog filtered signal **226**. Digital signals I **232** and Q **242** are then applied to a bank of N complex mixers **250**, wherein N is an integer value corresponding to the number of desired RF channels located in the non-contiguous portions of the frequency spectrum BW1. It is understood that the number N can be any integer value. In one embodiment, N can be equal to the number of all available channels that exist in the licensed frequency spectrum to provide system flexibility. In other embodiments, N can be equal to the number of all receivable channels within a geographic area. In yet another embodiment, N can be an integer value less than the number of receivable channels with the geographic area to reduce system costs. In the exemplary embodiment shown in FIG. **2**, the number of desired channels is 4. That is, each of the 4 complex mixers **250** mixes in-phase and quadrature signals **232** and **242** with an associated frequency to generate a corresponding baseband, which is then individually filtered, decimated and provided to an associated demodulator.

Each of the N complex mixers **250** receives the digital signals I **232** and Q **242** from ADCs **218** and **228** to extract a different one of the desired channels and frequency-shifts the extracted signals to the baseband frequency. Each of the frequency shifted desired channels **252** is filtered by an associated filter module (identified as **260***a* to **260***n*). In an embodiment, each of the filtered signals **260***a* to **260***n* may be sent directly to an associated demodulator (identified as **270***a* to **270***n*) for extracting the original information transmitted in the associated desired channel. In another embodiment, each of the filtered signals **262***a* to **262***n* is further decimated before providing to a demodulator. A path of digital front end **230** is described in more detail below.

FIG. **3** is a simplified circuit diagram of one of the signal paths **272***a* to **272***n* of digital front end **230** shown in FIG. **2** according to an embodiment of the present invention. In an embodiment, digital signal I **232** may be further filtered by a filter **311** to obtain a filtered signal **312**. Similarly, digital signal Q **242** may be further filtered by a filter **321** to obtain a filtered signal **322**. Thus, digital signals **312** and **322** only contain low-frequency components with undesired high-frequency components being eliminated by respective filters **311** and **321**. It is noted that filtered signals **312** and **322** are interposed between the respective ADCs **218**, **228** and the bank of N complex mixers **250**.

Mixer **300**, which represents one of the N complex mixers **250**, includes four multipliers **313**, **315**, **323**, and **325**. Multipliers **313** and **315** multiply the filtered signal **312** with respective $\cos(\omega_{ci}t)$ and $\sin(\omega_{ci}t)$ signals and generate respective products **314** and **316**. Similarly, multipliers **323** and **325** multiply the filtered Q signal **322** with respective $\cos(\omega_{ci}t)$ and $\sin(\omega_{ci}t)$ signals and generate respective products **324** and **326**. An adder **317** sums the products **314** and **326** to generate a frequency-shifted signal I **318**. An adder **327** sums the products **324** and **316** to generate a frequency-shifted signal Q **328**. Basically, complex mixer **300** causes a frequency shift of the filtered components **312** and **322** to respective baseband signals **318** and **328** in the digital domain according to the operation:

$$Y(t)=X(t)*e^{-j\omega_{ci}t} \quad (1)$$

or taken the Fourier transform, we obtain:

$$Y(\omega)=X(\omega-\omega_c) \quad (2)$$

Multipliers **313**, **315**, **323**, and **325** are identical digital multipliers. In an embodiment, a numerically controlled oscillator with quadrature output generates the $\cos(\omega_{ci}t)$ and $\sin(\omega_{ci}t)$ signals. Numerically controlled oscillators (NCO) can be implemented using a phase accumulator and a look-up table. NCOs are known to those of skill in the art and will not be described herein. The frequency ω_{ci} is so chosen that each one of the desired channels embedded in the digital signals I **232** and Q **242** will be downshifted to the baseband. In the given example shown in FIG. **2**, the bank of N complex mixers will have four complex mixers, each one of the N (i.e., four) complex mixers is coupled to an individual NCO having a distinct frequency ω_{ci} so that when mixing the filtered digital I and Q signals **312** and **322** with that frequency, each one of the complex mixers will generate the signals I (**318**) and Q (**328**) of a corresponding one of the desired channels at the baseband.

In an embodiment, baseband signals **318** and **328** are further individually filtered by respective filters **330** and **340** that are identified as one of the filters **260***a-n* in FIG. **2**. Filters **330** and **340** may be band-pass or low-pass filters having a narrow bandwidth equal to the bandwidth of a desired channel. In certain embodiments, filters **330** and **340** can be analog passive or active low-pass or complex band-pass filters such as polyphase filters. In another embodiment, filters **330** and **340** can be digital low-pass filters, such as finite impulse response (FIR) filters to eliminate high frequency components that may be aliased back to the baseband signals Ii (**332**) and Qi (**342**) when decimated by subsequent decimator **350**.

The reduced sampling rate of the N desired baseband channels will be sent as a serial or parallel digital data stream to a demodulator using a serial or parallel data interface according to commonly known methods, as shown in FIG. **2**. This approach provides several advantages over conventional tuner architectures. First, it eliminates the need of expensive data conversion, filtering and channel selection on the demodulator side. Second, it removes undesired channels from the signal path at an early stage, thus relieves the large dynamic range requirement in the demodulator.

FIG. **4** shows a simplified schematic block diagram of a wideband receiver system **400** according to another embodiment of the present invention. Wideband receiver system **400**

includes a radio front end **410**, a digital front end **430**, a tiled up-conversion module **450**, and a summing digital-to-analog converter module DAC **470**. Radio front end **410** includes a low noise amplifier LNA1 that receives an RF input signal **102** and provides an amplified RF signal **403** to mixers M1 **411** and M2 **421**. Mixer M1 **411** is coupled to an oscillator frequency **405** of a synthesizer S1 whereas mixer M2 **421** is coupled with the oscillator frequency **405** via a phase shifter P1 **406** that generates a 90° degree phase-shift to the oscillator frequency **405**. Mixers M1 **411** and M2 **421** generate respective in-phase signal **412** and quadrature signal **422** that are further amplified by respective amplifiers V1 **413** and V2 **423**. The amplified in-phase and quadrature signals **414**, **424** are then filtered by filters F1 **415** and F2 **425** to eliminate undesired frequency components that would be aliased back to the in-phase and quadrature signals when digitally sampled by subsequent analog-to-digital converters ADC1 **418** and ADC2 **428**. Digital signals I **422** and Q **442** at the input of digital front end **430** are digital representations of the filtered analog in-phase and quadrature signals **416**, **426** before the ADCs. Digital front end **430** include a bank of N complex mixers **432** comprising **432***a* to **432***n* identical mixers, where N is an integer value corresponding to the number of the desired channels located in non-contiguous portions of the frequency spectrum. Each of the N complex mixers **432***a* to **432***n* frequency down-converts signals I **432** and Q **442** to an associated baseband. Each of the frequency down-converted I and Q signals are coupled to respective low-pass, band-pass, or decimating filters **434**. In this regard, the radio front end **410** and the digital front end **430** are similar to respective radio front end **210** and digital front end **230** of FIG. **2** that have been described in detail above.

In an alternative embodiment of the present invention, the N filtered and decimated channels **438***a* to **438***n* (where indices a to n correspond to the associated number of desired channels) are not provided to a demodulator for demodulation. Instead, the N filtered and decimated channels **438***a* to **438***n* are further frequency up-converted to an intermediate frequency (IF) spectrum. In order to achieve that, the N filtered and decimated channels are coupled to a tiled up-conversion module **450** that includes a bank of N complex up-mixers, where N is an integer value correspond to the number of desired received channels. The N complex up-mixers include identical digital mixers **452***a* to **452***n* that will be described further in detail below with reference to FIG. **5**. The N up-shifted channels are then filtered by a subsequent bank of channel filters **454** that, in an embodiment, comprises N individual finite impulse response (FIR) filters. The N filtered channels are then digitally combined and converted to the analog domain by a summing digital-to-analog converter module DAC **470**. The N up-shifted channels are adjacent to each other and form a contiguous or substantially-contiguous set of channels **475** in the IF spectrum centered around f_{if} as illustrated in FIG. **4**. In an embodiment, the spectra of the mixed products are spaced in such a way so as to avoid overlap with known frequency bands containing potential or actual interferers. In another embodiment, the spectra of the mixed products are spaced in such a way so as to avoid overlap with frequency bands that might introduce interference to other systems. In general, because the bandwidth BW_2 is substantially lower than BW_1, the IF frequency f_{if} can be set proportionally lower, e.g., typically about 16 MHz to accommodate the spectrum of BW2 of up to 32 MHz (corresponding to the total bandwidth of the four desired channels, each having a bandwidth of 8 MHz in this example).

The up-conversion approach of FIG. **4** provides several advantages over conventional tuner architectures. First, it allows the demodulator to operate the data converter at a lower data rate and with lower resolution (fewer bits) due to the fact that the contiguous channels have a narrower bandwidth. Second, the up-conversion approach provides full compatibility with existing demodulators that require an analog IF signal. Third, it removes undesired channels from the signal path at an early stage, thus relieves the requirement of a high dynamic range requirement of the demodulator's analog-to-digital converter and the demodulator itself.

FIG. **5** shows a simplified exemplary circuit diagram of a complex up-mixer **500** according to an embodiment of the present invention. Up-mixer **500** is one of the N complex up-mixers **452***a* to **452***n* in tiled up-conversion module **450** shown in FIG. **4**. Up-mixer **500** includes filter **510** and **520** configured to eliminate unwanted frequency components present in respective input signals I **501** and Q **502**. Filtered signals **512** and **522** are provided to up-mixers UMI **515** and UMQ **525** that multiply the filtered signals **512** and **522** with respective $\cos(\omega_u t)$ and $\sin(\omega_u t)$. The products **516** and **526** are summed in an adder **530** to generate an IF signal **532** according to the following equation:

$$IF(t)=I(t)*\cos(\omega_u t)+Q(t)*\sin(\omega_u t) \quad (3)$$

Up-mixers UMI **515** and UMQ **525** are identical digital multipliers that multiply the respective filtered signal **512** and **522** with a cosine function **505** and a sine function **506** that can be generated from a NCO using a digital phase accumulator and a look-up table.

As described above, TV channels are grouped into multiple frequency bands in North America. For example, channels 2 through 6 are grouped in VHF-low band (aka band I in Europe), channels 7 through 13 in VHF-high band (band III), and channels 14 through 69 in UHF band (bands IV and V). In order to receive such a wide frequency spectrum, the low noise amplifier and mixer must have very low noise, wide tuning range and high linearity as described above in the wideband receiver systems **200** and **400**. However, a wideband receiver having a single tuner with high sensitivity may have a high power consumption. For certain applications, it may be advantageous to use multiple tuners that are optimized for a given frequency band, such as a dedicated tuner for the low VHF band, another dedicated tuner for the high VHF band and the UHF band, and yet other dedicated tuners for receiving the digital video broadcasting (DVB) via satellite (DVB-S), via cable (DVB-C), or terrestrial digital video broadcasting (DVB-T). The multi-tuner approach may also be advantageously applied to cable networks that carry TV programs on an 88 MHz to 860 MHz according to the Data Over Cable Service Interface Specification (DOCSIS) protocol.

FIG. **6** shows a simplified schematic block diagram of a wideband multi-tuner receiver system **600** according to an embodiment of the present invention. In an embodiment, multi-tuner system **600** includes low noise amplifier A1 **602** for receiving an RF input signal **601**. Amplifier A1 **602** is coupled to at least a tuner1 **610** and a tuner2 **720**. In another embodiment, multi-tuner system **600** may not include amplifier **602** so that RF input signal **601** can be received directly at each tuner **610** and **720**.

Tuner1 **610** includes an amplifying filter AF1 **613** that filters and amplifies a first portion BWtuner1 **604** of a broad frequency spectrum **608** that contains a first plurality of RF channels **606** including desired channels **607** having respective channel frequencies f_{rf1} and f_{rf2}. The first portion of the broad frequency spectrum BWtuner1 **604** is then frequency down-converted to a low-IF or zero-IF in-phase signal I1 **612** and a quadrature signal Q1 **622** through respective mixer M1

611 and M2 621. Signals I1 612 and Q1 622 are further amplified and low-pass filtered before applying to respective analog-to-digital converters ADC1 618 and ADC2 628 that convert analog signals Ia1 616 and Qa1 626 to respective digital in-phase signal Id1 631 and digital quadrature signal Qd1 641. Because tuner1 610 only covers a portion BWtuner1 604 of the entire frequency spectrum 608 having fewer channels, the ADC1 618 and ADC2 628 can be slower-speed analog-to-digital converters with a large number of bits, i.e., large dynamic range.

Digital signals Id1 631 and Qd1 641 are then provided to a digital front end DFE 630 that includes a first bank of N complex mixers 632 and channel and decimating filters 634. The first bank of N complex filters 632 has N identical complex mixers, where N is an integer value equal to the number of desired channels located in the first portion BWtuner1 604 of the broad frequency spectrum 608. In an embodiment, each one of the first bank of N complex mixers includes four digital mixers that multiply digital stream Id1 631 and Qd1 641 with respective digitized cosine function and sine function to generate the sum and difference frequency components, as shown in FIG. 3. The digitized cosine and sine frequency, i.e., the mixer frequency is so chosen so that when mixing signals Id1 631 and Qd1 641 will move them to a baseband or a low-IF band. In an embodiment, channel and decimating filters have similar structures as filters 330 and 340 and demodulator 350 as shown in FIG. 3. That is, channel and decimating filters include digital low-pass filters 330 and 340 that eliminates unwanted high frequency components of the baseband signals I and Q prior to applying them to a decimator 350 (FIG. 3) that reduces the sample frequency without any loss of information since Id1 631 and Qd1 641 are sampled at a much higher frequency by the respective ADC1 618 and ADC2 628.

The decimated desired channels are then provided to an up-converter module 650 that includes a bank of N up-mixers. The bank of N up-mixers includes N identical up-mixers whose structure is shown in FIG. 5. In an embodiment, N is an integer value equal to the number of desired channels present in BWtuner1 604. Each one of the up-mixer frequency-shifts the baseband signals I and Q of each one of the desired channels to an appropriate portion of the intermediate frequency band according to Equation (3). In other words, the bank of N up-mixers is "frequency multiplexing" the desired channels onto a first portion 682 of an IF band 686.

Similarly, tuner2 720 includes an amplifying filter AF2 713 that is configured to receive a second portion BWtuner2 704 of the broad frequency spectrum 608. The second portion 704 contains a second plurality of RF channels 706 including a second number of desired channels. In the exemplary illustration of FIG. 6, the second portion 704 has a frequency bandwidth of BWtuner2 that contains desired channels 707 having respective channel frequencies f_{rf3} and f_{rf4}. Tuner2 720 includes elements such as mixers M3 711, M4 721, amplifiers V3 714, V4 724, filters F3 715, F4 725 and analog-to-digital converters ADC3 731 and ADC4 741 that are substantially the same as the like-named elements of the signal path of tuner1 610. Thus, redundant description is omitted herein.

Digital in-phase signal Id2 731 and digital quadrature signal Qd2 741 are then provided to digital front end 740. Digital front end 740 includes a bank of L complex filters, where L is an integer value equal to the number of desired channels in the second portion BWtuner2 704 of the broad frequency spectrum 608. Each one of the bank of L complex filters is a digital complex mixer configured to transform the signals Id2 731 and Qd2 741 to baseband signals that are further filtered by individual digital low-pass filters such as FIR filters before decimated by a subsequent decimator. The elements of digital front end 740 are substantially similar to those described in digital front end 630. Thus, redundant description is omitted herein.

The decimated baseband I and Q channels are further provided to a subsequent up-conversion module 760 that performs a function substantially similar to that of the up-conversion module 650 already described above. The outputs of up-conversion module 650 and 760 can be tiled to generate a contiguous set of IF frequencies 682, 684 centered at f_{if} 686. In an embodiment, the outputs of up-conversion module 650 and 760 are digitally summed and converted to an analog signal by summing DAC 670. In another embodiment, the up-conversion modules 650 and 760 and the digital summing function 672 can be performed using an inverse discrete Fourier transform or an inverse Fast Fourier transform operation.

The multi-tuner architecture provides the flexibility that multiple commercially available tuners can be used without the need of designing a wideband tuner. For example, a tuner designed for a terrestrial broadcast digital TV can be used together with a tuner dedicated to receiving a cable signal and/or a tuner for receiving a satellite broadcast signal. The multi-tuner receiver system provides an additional advantage that other tuners can be added quickly to the system to accommodate any future applications. Additionally, the multi-tuner architecture allows the use of slower speed (i.e., lower cost) analog-to-digital converters with a larger number of bits for achieving large dynamic range.

FIG. 7 shows a block diagram of an exemplary digital front end of the invention in more detail. In an embodiment, in-phase signal Id2 731 and quadrature signal Qd2 741 at the output of respective ADC converters 718 and 728 are provided to each of the L complex mixers 732 comprising mixers 732A to 732L. A more detailed description of each of L complex mixers is shown in FIG. 3. Mixer 732A multiplies Id2 731 and Qd2 741 with a cosine signal and a sine signal that are generated from an NCO1 and produces an I-732A signal and a Q-732A signal that are further individually filtered by an FIR filter before decimating. The bank of L complex mixers corresponds to the block 732 in FIG. 6; and the set of FIR filters and decimator corresponds to the block 734 in FIG. 6. Each decimated pair of I-732*i*/M in the baseband, where the index "i" is from A to L, is further provided to a subsequent up-mixer for frequency-shifting to an intermediate frequency as shown in FIG. 8.

FIG. 8 shows an exemplary embodiment of a bank of L complex up-mixers according to the present invention. Each decimated pair of complex signals I-732*i*/M and Q-732*i*/M is provided to an associated complex up-mixer, whose frequency is so chosen that when mixing with the pair of complex signals I-732*i*/M and Q-732*i*/M will generate an associated channel at a predetermined sub-portion of the intermediate frequency band 686 (FIG. 6). A more detailed schematic block of one of the L up-mixers is described above together with FIG. 5.

FIG. 9 is a simplified block diagram of a wideband multi-tuner receiver system 900 according to an embodiment of the present invention. In an embodiment, system 900 includes a crossbar switch 910 having at least an input terminal 912 configured to receive signals from an analog-to-digital converter (ADC) 912 and an input terminal 922 configured to receive signals from an ADC 922. Crossbar switch 910 also includes an output terminal 924 that is coupled to a digital front end 930. In an embodiment, input terminals 912 and 922 of crossbar switch 910 have P inputs, where P is an integer value that is equal to the total number of desired channels received by tuner1 610 and tuner2 720. Output terminal 924

of crossbar switch **910** have Q outputs, where Q is an integer value that is equal to the total number of desired channels received by tuned **610** and tuner2 **720**.

In an embodiment, digital front end **930** may include a bank of R complex mixers that frequency shifts the received channels to a baseband. Digital front end **930** may combine digital front end **630** and **740** shown in FIG. **6**. Similarly, a tiled up-conversion module **950** may include up-converter modules **650** and **760** of FIG. **6**.

System **900** further includes a summing DAC that operates similarly as summing DAC **470** and **670** that have been described in detail in relation with respective FIG. **4** and FIG. **6** above. Thus, redundant description is omitted herein.

FIG. **10** is a simplified block diagram of a wideband multi-tuner receiver system **1000** according to another embodiment of the present invention. System **1000** includes at least tuner1 **610** coupled with digital front end **630** through an analog-to-digital converter **620** and tuner2 **720** coupled with digital front end **740** through an analog-to-digital converter **730**. System **1000** further includes a crossbar switch **1010** that is interposed between digital front ends **630**, **740** and up-conversion modules **650**, **760**. Crossbar switch **1010** includes an input terminal **1012** having S inputs coupled with DFE **630** and an input terminal **1022** having T inputs coupled with DFE **740**. In an embodiment, S is an integer value equal to the number of desired channels processed in DFE **630** and T is an integer value equal to the number of desired channels processed in DFE **740**. Crossbar switch **1010** further includes an output terminal **1024** having U outputs coupled with up-converter module **650** and an output terminal **1024** having V outputs coupled with up-converter module **760**. In an embodiment, the total number of the outputs U and V is equal to the sum of the inputs S and T. Thus, crossbar switch **1010** allows the routing of any channel from either DFE **630** or DFE **740** to up-converters **650** or **760**. It is understood that system **1000** is not as flexible as system **900** because DFE **630** and DFE **740** are already pre-assigned to respective tuner1 (**610**) and tuner2 (**720**). However, this pre-assigned arrangement allows a simpler implementation of crossbar switch **1010** that operates at lower speeds.

While several embodiments in accordance with the present invention have been described, it is to be understood that the above description is intended to be illustrative and not restrictive. Many embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

What is claimed is:

1. A wideband receiver system comprising:

a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

digital circuitry configured to:

select said plurality of desired television channels from said digitized plurality of frequencies; and

output said selected plurality of television channels to a demodulator as a digital datastream.

2. The wideband receiver system of claim **1**, wherein said output of said digital datastream is via a serial interface.

3. The wideband receiver system of claim **1**, wherein said output of said digital datastream is via a parallel interface.

4. The wideband receiver system of claim **1**, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.

5. The wideband receiver system of claim **1**, wherein said wideband analog-to-digital converter comprises:

a first ADC configured to generate a digital in-phase signal; and

a second ADC configured to generate a digital quadrature signal.

6. The wideband receiver system of claim **5**, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.

7. The wideband receiver system of claim **6**, wherein:

prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and

after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.

8. The wideband receiver system of claim **1**, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.

9. The wideband receiver system of claim **8**, wherein each one of said plurality of channel filters is a finite impulse response filter.

10. The wideband receiver system of claim **1**, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels.

11. A method comprising:

in a wideband receiver system:

downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and

outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.

12. The method of claim **11**, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface.

13. The method of claim **11**, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface.

14. The method of claim **11**, comprising:

generating, by a first mixer of said mixer module, an in-phase signal; and

generating, by a second mixer of said mixer module, a quadrature signal.

15. The method of claim **11**, comprising:

generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and

generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.

16. The method of claim **15**, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry.

17. The method of claim **16**, wherein:

prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and

after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum.

18. The method of claim **11**, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.

19. The method of claim **18**, wherein each one of said plurality of channel filters is a finite impulse response filter.

20. The method of claim **11**, comprising decimating, by said digital circuitry, one or more of said selected plurality of desired television channels prior to said outputting of said selected plurality of television channels.

* * * * *

Exhibit 1006

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Frequency Translation Method for Low Frequency Variable Gain Amplification and Filtering

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Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Masters of Engineering in Electrical Engineering and Computer Science

at the

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Frequency Translation Method for Low Frequency Variable Gain Amplification and Filtering

by

Mabel Y. Feng

Submitted to the Department of Electrical Engineering and Computer Science
on May 11, 2007, in partial fulfillment of the
requirements for the degree of
Masters of Engineering in Electrical Engineering and Computer Science

Abstract

This thesis discusses an innovative solution to an industry challenge. A frequency translation method is designed to shift low frequency signals to intermediate frequencies in order to utilize higher-frequency components. This solution, appropriate for applications involving 1-10MHz signals, can provide continuously variable gain and filtering at little cost in dynamic performance. The working system converts the low frequency signals up to the 70MHz band to achieve up to 28dB attenuation and 60-86MHz variable filtering. A Single Side Band system has a Signal-to-Noise Ratio (SNR) of 71dB with a 73dB SNR Analog-to-Digital Converter (ADC), 44 dB Output Third-Order Intercept Point (OIP3), and a Noise Figure (NF) of 14dB. Ultrasound and other applications in the 1-10MHz range benefit greatly from this upconversion scheme.

VI-A Company Thesis Supervisor: Richard Reay
Title: Design Engineer

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Title: Professor

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Chapter 1

Introduction

1.1 Problem Statement

Ultrasound, sonar, and medical imaging rely on a method of receiving dispatched signals and properly processing them for image conversion. High-end ultrasound applications require a high dynamic range system for minimal interference and distortion. This would give the higher resolution imaging necessary in high-end image processing. One challenge in ultrasound has been how to implement a truly continuously adjustable gain control in a system with low distortion at the operational frequencies. Designing such a system can be a challenging feat and is not an easily solvable problem for engineers. Hence, if a solution that is simple to both implement and understand can be developed for this industry challenge, then there are many uses for the application. The following section expands the ultrasound background so that the reader may fully understand the scope of the problem at hand.

1.2 Background

1.2.1 Ultrasound

Much of medical imaging is made possible by ultrasound. The images are obtained by emitting an energy beam throughout the body or mass and reconstructing the

reflected energies into an image with analog to digital processing. This is similar to how radar and sonar sweep across an area and study the echoes back at the source. A transducer probe receives the reflected signal energies at different times across the surface structure, allowing the image to be reconstructed based on a signal attenuation versus time relation. Higher frequencies provide higher resolution images but attenuate faster as the signal travels through the body. The image energies are transmitted at frequencies optimized for signal strength and resolution, so ultrasound frequencies typically range from 2-7 MHz [35].

As an energy beam travels through a mass medium such as the human body, the signal strength decreases due to interfering media and noise. The reflected signal is more attenuated if it has traveled a longer distance in the body and through electronic cables. The beam signals can be subsequently amplified before digital conversion. Hence ultrasound systems require at least gain and attenuation control as well as a means of reducing noise degradation.

Current ultrasound applications incorporate time gain compensation (TGC) amplifiers to maintain a strong (and consistent) energy level as the signals are picked up by the transducer. A standard time-independent amplifier provides the same dB gain to every reflected signal, no matter how far away the signal. Hence, the reflected echoes are still of different magnitudes [Figure 1-1(a)]. With a TGC, the gain increases over time to maintain a constant level of signal attenuation in reflected pulses [Figure 1-1(b)].

What has been described so far is the analog domain of ultrasound. There is, however, the digital processing side that converts the analog echoes to digital signals for digital image processing. At the analog-to-digital converter (ADC) interface, high performance systems require low distortion and noise at the input to the ADC before digital processing. It is important to ensure also that the ADC quantization noise is not a significant factor to the overall noise; it sets the bit resolution. Also, interfering signals about the main desired signal (fundamental) can be prominent distortion sources in ultrasound. If the system has poor intermodulation distortion, the ADC will take the additional spurs as signals in the system and the reconstructed

signal will be heavily distorted. Using high dynamic range and high resolution ADCs like Linear Technology's LTC2249 allows designers to meet the high standards of ultrasound imaging.The system block diagram is shown below in Figure 1-2.

In the analog domain dynamic performance can be limited by ADCs and TGC amplifiers. It was established that the ADCs can meet the specifications for high performance so we take a look at the types of TGC or varying gain amplifiers to devise a high-end solution.

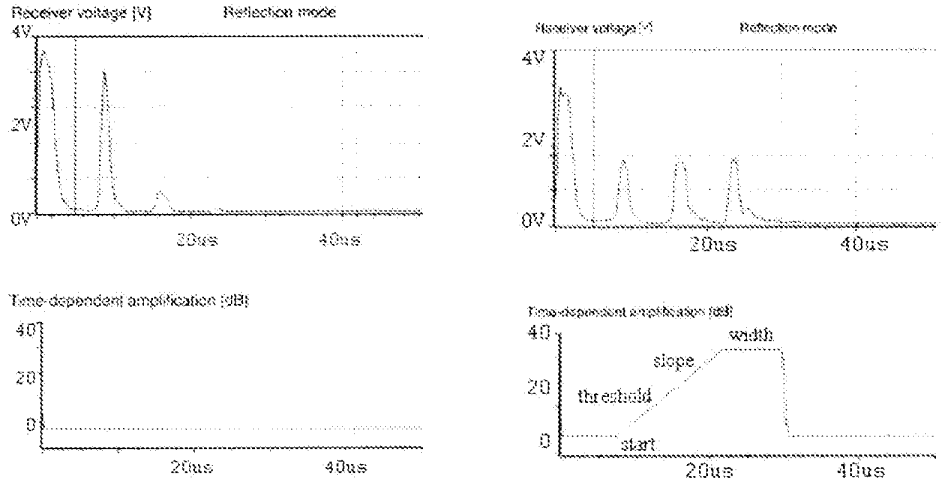


Figure 1-1: Ultrasound Time Gain Compensation. (a) Constant Gain Amplification. (b) TIme Varying Gain Amplification. [36]

1.2.2 The Frequency Spectrum

The challenge at hand is to find variable gain devices that are usable at specific parts on the frequency spectrum. Consider the entire frequency spectrum, from DC up to GHz (radio frequency RF or ultra high frequency). On the low frequency end (DC to 1 MHz), there are several options available for designers. There are discrete programmable step gain amplifiers but for ultrasound, continually adjustable gain amplifiers are more suitable. Instead of adjusting gain in the analog domain, it is also possible to first digitize the low frequency signal with an oversampling ADC and then digitally adjust the gain. Once we progress into the MHz range, we are offered the choice of using Analog Devices' patented XAmp continuous VGAs [23].

However, most adjustable gain amplifiers do not provide the same performance at low frequencies as in higher bandwidths (less than 100MHz).

At intermediate frequencies (IF) and above, continuous variable gain can be realized using PIN (p-intrinsicSi-n structure) diodes. This is a common component found in radio receiver and transmitter paths. PIN diodes are limited on the lower frequency side by two things : physical size and carrier lifetime. A more thorough background on PIN diodes is given in Section 2.4.

In addition to continuous variable gain capabilities, it is important to filter out interfering signals for the best signal processing. High frequency and RF use surface acoustic wave (SAW) filters for their steep filter response, but they are also limited on the low frequency end by size. As in the PIN diodes, a more thorough background on SAW filters is given in Section 2.3. Lower frequency applications would just implement high order filters to achieve as ideal of a filter response as possible. A quality filter in the signal path improves the dynamic performance of the system by preventing out of band noise from getting to the ADC.

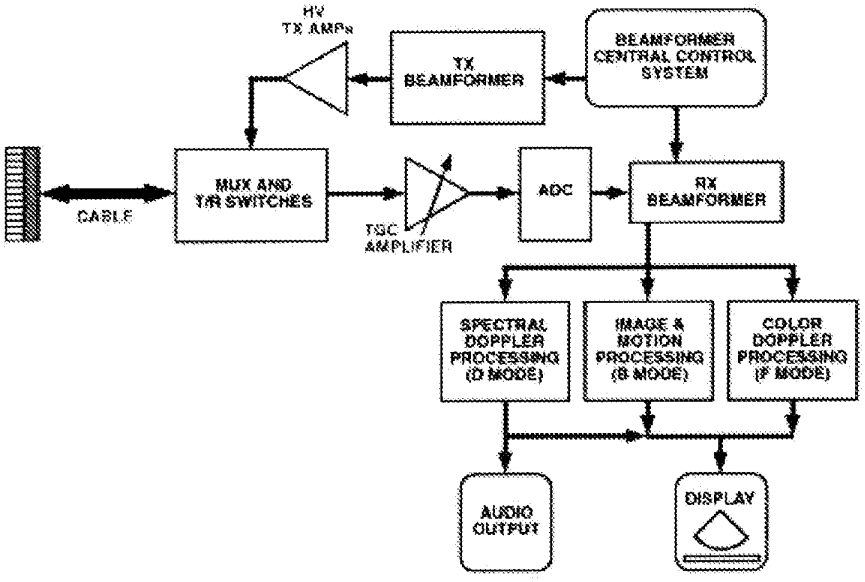


Figure 1-2: Ultrasound System Block Diagram. From [35]

1.3 Proposed Method

The background in the prior section discusses some of the challenges and limitations in low frequency applications. By using frequency translation, one can essentially move the problem to higher frequencies to take advantage of high frequency components. This method can provide continuously variable gain and filtering for ultrasound. The challenge then is to be able to design a system that offers good dynamic performance, on par or better than what low frequency processing can achieve. The thesis explains this method of frequency translation and develops a solution that meets the standards in the ultrasound industry.

1.4 Organization

The thesis is organized as follows: Chapter 2 describes the various components that will be used in the system and also defines the performance figures used. Chapters 3 and 4 discuss design solutions and modifications made to the system. Chapter 5 leads a discussion of the results and how they compare to theoretical expectations of the entire system. Chapter 6 gives a conclusive summary of the merits and drawbacks of this application and suggests future work.

Chapter 2

Building Blocks and Measuring Stick

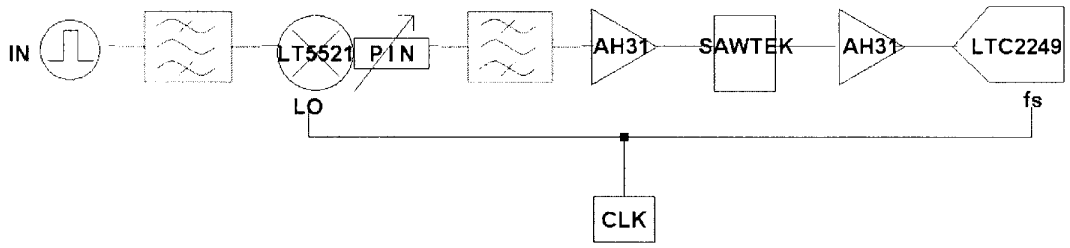


Figure 2-1: Frequency Translation Method General Block Diagram.

The general block diagram of the system is shown in Figure 2-1. This chapter provides background information for the building blocks of the system.

2.1 Frequency Translation

Frequency translation is the process of shifting a signal from one frequency to another, without loss of information in the signal. This is useful in any application that does not care at what frequency the information is transmitted (i.e. the carrier frequency contains no information). In modern communications, frequency translation is used in receivers to downconvert RF to a lower frequency and used in transmitters to upconvert baseband signals to RF.

Modulation is a standard example of frequency translation at work. Essentially, there is information summarized by the function $f(t) = A\cos(\omega_i t)$, and we want to transmit it at a frequency $f_c(t)$. The modulated signal $f_m(t)$ is now of the form $f_m(t) = \cos([\omega_i - \omega_c]t) + \cos([\omega_i + \omega_c]t)$, and is the frequency translated version of the original $f(t)$ signal. The information is preserved because modulation scales the amplitude of the signal but does not distort it. In downconversion, $f_c < f_i$ and in upconversion, $f_c > f_i$.

2.2 Undersampling

In sampling schemes, the choice of sampling frequency determines the quality of the sampled output signal. It makes sense that more samples taken over a period would ensure a better reconstruction of the signal. And, if the signal is not sampled at a fast enough rate, then the conversion will not produce an output that resembles anything like the input. The criterion for proper sampling is the Nyquist theorem (Equation 2.1). The input signal frequency f and the ADC sampling frequency f_s need to satisfy the Nyquist theorem to ensure that no information is lost in sampling:

$$\omega_s \geq 2\omega, \ where\ \omega = 2\pi f\ and\ \omega_s = 2\pi f_s. \tag{2.1}$$

One of the ways to sample signals for analog-to-digital conversion is undersampling. For undersampling, we are concerned more about the input bandwidth rather than the input frequency. Here, the Nyquist theorem is concerned with the comparison between the sampling frequency and the input bandwidth.

It is important to note here the distinction between input signal bandwidth and input signal frequency. In an upconversion scheme, the input of interest has a bandwidth of the low frequency about the local oscillator frequency (i.e. 10MHz about LO=70MHz). The input signal frequency goes up to 80MHz but its bandwidth is 10MHz. Because the input does not have information from DC up to 80MHz, it is appropriate to consider only the 10MHz input bandwidth in Nyquist. Input bandwidths less than the Nyquist frequency ($\frac{f_s}{2}$) are fully recovered. Input bandwidths

greater than the Nyquist frequency will fold back into the baseband (DC to $\frac{f_s}{2}$) region. Therefore, if the input signal bandwidth is limited to one Nyquist zone at any location on the frequency spectrum, foldback of the signal will not cause the signal to fold on top of itself.

If the Nyquist criterion is not met, the ADC can produce an aliased component within the signal bandwidth. This aliased component is an undesired signal that needs to be pushed outside of the signal bandwidth. Figure 2-2 shows the frequency effects of aliasing.

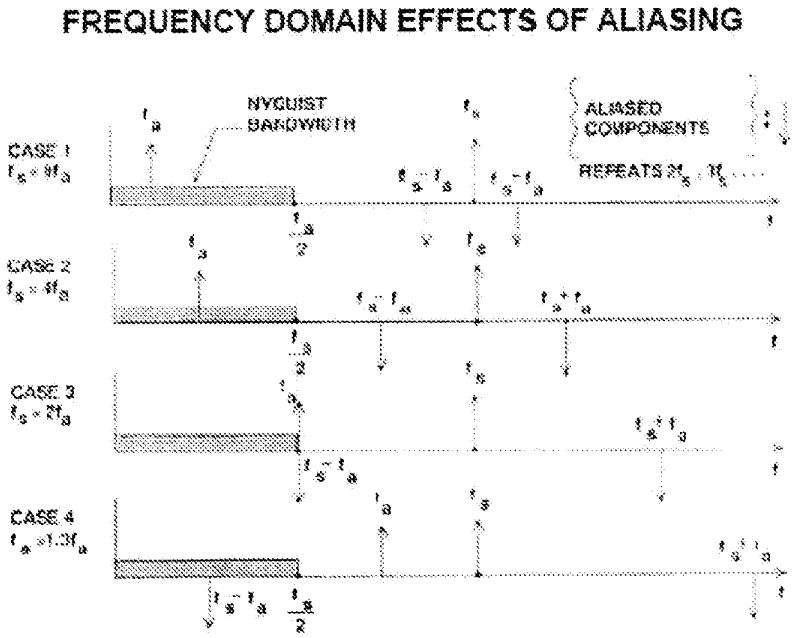


Figure 2-2: Sampling Analog Input Signal f_a at Sampling Rate f_s. For different f_s, the effects of aliasing can be seen in Case 3 when the Nyquist criterion is not met, because the aliased component $(f_s - f_a)$ is at the Nyquist frequency $\frac{f_s}{2}$. From [37].

Undersampled systems allow direct sampling at the IF frequencies as opposed to downconverting the IF signal down to baseband before sampling. Existence of high performance and high sampling rate ADCs (130MSPS or more) allow pre-receiver design to be simplified in cost and design.

Although undersampled systems eliminate the need to sample at the base rate, they tend to exhibit bad noise figures. Due to harmonic folding, every input frequency

harmonic is folded back into the Nyquist zone, which degrades noise performance. Typically, noise performance increases when bandwidth decreases. Another factor that degrades noise is flicker ($1/f$) noise that is introduced with direct-IF sampling receivers. Instead, efforts to improve linearity have to be made, to mitigate the degraded noise performance.

2.3 SAW Filters

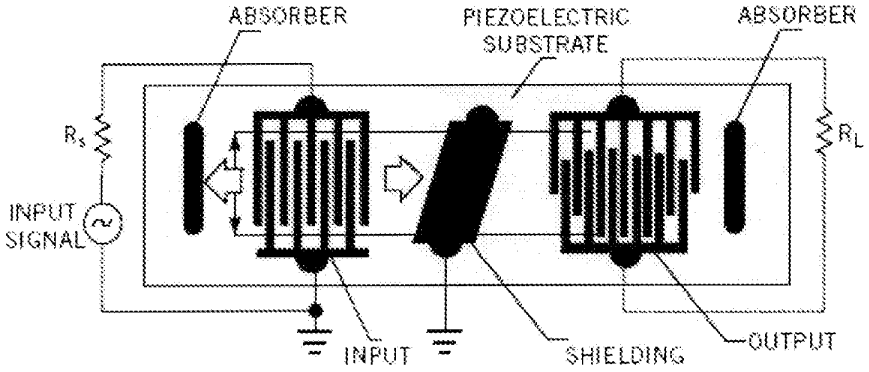


Figure 2-3: Physical Construction of a Typical Surface-Acoustic-Wave (SAW) Filter. [16]

In a surface acoustic wave filter, a mechanical wave travels along the surface of a material with elasticity, and has a decaying amplitude correlated with the depth of the surface [Figure 2-3]. SAW filters use piezoelectric crystals to convert electrical signals to mechanical waves, seen as vibrations. The wave is then delayed as it propagates across the crystal before being converted back to an electric wave. Only waves vibrating at certain (passband) frequencies are converted back into electric waves. SAW filters are ubiquitous in the communications market because they provide significant advantages in not just performance but also cost and size over other types of filters.

SAW filters provide much sharper frequency roll-off than other filters [Figure 2-4]. For example, to achieve the same order response, a passive LC (inductive-capacitive) filter needs to be very high order (possibly 7th-9th order). With their steep stopband

attenuation, the SAW filters are excellent at removing nearby interference, easing the dynamic range parameters of the ADC. This is especially important here because ultrasound signals are often subject to a lot of noise and interference, as discussed before.

In wave propogation, there is an intrinsic delay. If the signal is too low in frequency, the period of the signal becomes greater than this propogation delay, making SAW filters inappropriate for low frequency applications. For higher frequencies, there is a smaller delay so the size of the filters can be physically smaller. Hence SAW filters are better suited for higher frequency applications.

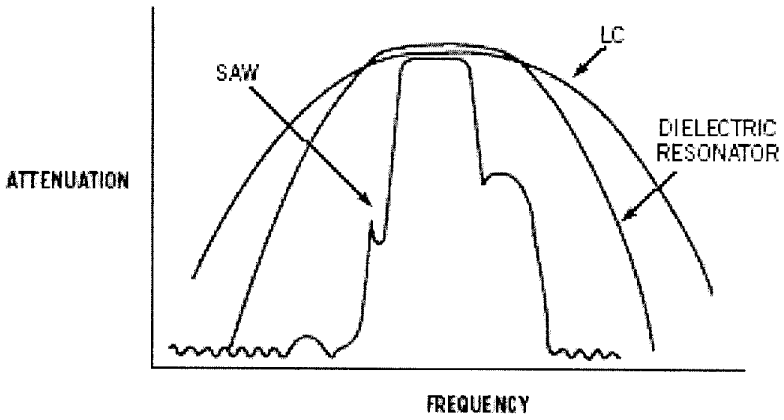


Figure 2-4: Comparison of Different Types of Filters.
SAW filters, seen here provide the sharpest rolloff. [16]

Although SAW filters provide impressive stopband response, they do have a higher insertion loss than passive LC filters. A following low-distortion amplifier can compensate for the gain loss.

The SAW filters used are from SAWTEK : f_c at 70MHz with both 5MHz and 20MHz bandwidths. The insertion loss was 7.25dB and 14.5dB respectively and the group delay variation was 80ns and 65ns respectively [7], [8].

2.4 PIN Diodes

P-Intrinsic-N diodes are often used in high frequency attenuator circuits. These devices are relatively simple devices yet they are excellent for providing continuously adjustable gain with little distortion, cost, and almost ideal linear resistive behavior. Many RF engineers are satisfied with the harmonic distortion and intermodulation distortion performances of available PIN diodes [33]. In addition, the wide range of gain can be achieved at very little DC excitation, which is suitable for low-power applications [28]. To understand the operation of the PIN diode, it is best to start with the well-known 'standard' PN diode and develop the model of the PIN diode from there.

A standard diode has an abrupt PN junction, with the well known I-V characteristic curve and equation $I = I_s(e^{\frac{qV}{kT}} - 1)$, where I_s is the saturation current, q is the charge of an electron, k is Boltzmann's constant, and T is the temperature, in Kelvin. It has a small signal dynamic resistance $r_d = \frac{kT}{qI}$ in forward bias ($V > 0$). We focus only on the forward bias of the diode here.

In the PIN diode, the lightly doped intrinsic region (of width W) inbetween the heavily doped P and N regions affects charge storage and resistive behavior of the device. The resistance of the PIN diode is controlled by a DC current bias I_d. When the PIN diode is forward biased, minority charge carriers are injected into the intrinsic layer (from both P and N doping regions). Therefore, there is charge in the intrinsic layer, which is the basis for the operation of the PIN diode. At frequencies greater than the inverse of the carrier lifetime τ, the intrinsic region charge $Q = I_d\tau$ dominates the resistance of the PIN diode. The carrier lifetime can be thought of as the average time that an injected (minority) carrier survives in the lightly doped intrinsic-region (until recombination in the intrinsic-region or the carrier has traveled a mean distance W to the other heavily doped region).

A simple model of the PIN diode is shown in Figure 2-5(a). The PIN diode has two junctions (P-I and I-N), each modeled as an ideal standard diode. The intrinsic region behaves as variable resistor R_{rf}, controlled by the current bias. The small

signal model of the PIN diode is in Figure 2-5(b). r_d is the small signal resistance found earlier from the I-V curve, and C_d is the capacitance of the junction.

The resistance R_{rf} can be derived using device geometry (W/L_D) and Einstein's relation $(qD = \mu kT)$ and its expression is given by:

$$R_{rf} = (W/L_D)^2 V_{th}/(2I_d) = \frac{W^2}{2\mu I_d \tau_{eff}}, \tag{2.2}$$

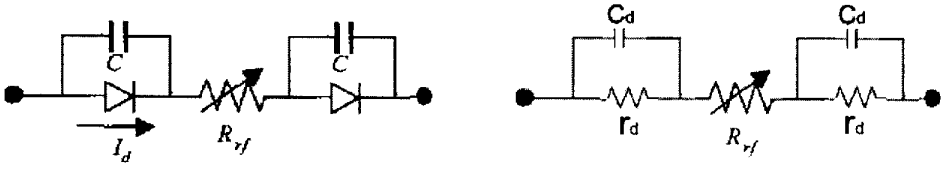
where $V_{th} = kT/q$, μ = mobility, I_d = DC forward current, τ_{eff} = effective carrier lifetime, W = width of intrinsic region, and $L_D = (D\tau_{eff})^{1/2}$, the diffusion length and the ratio $(W/L_D) < 1$. The D in Einstein's relation refers to the ambipolar diffusion constant, $D = 2D_nD_p/(D_n + D_p)$. τ_{eff} is discussed later in this section. With the device geometry less than unity, this approximation is useful for thin-PIN diodes. [32]

With this nonzero R_{rf}, the entire voltage drop across the PIN diode is

$$V_{PIN} = 2V_d + V_{rf} = 2V_d + I_d R_{rf}, \tag{2.3}$$

where V_d is the diode drop across the ideal PN diode and V_{rf} is the voltage drop across the variable resistance. The same I_d runs through the entire PIN diode, so one could add a load line for R_{rf} on-top the I-V curve for the PIN diode. The PIN diode I-V characteristic can be found then by fitting the points to the curve I_d v. V_{PIN}. The plot, in accordance with the model in Figure 2-5(a) is depicted in Figure 2-6.

The total small signal impedance across the entire PIN diode is $Z = 2r_d + R_{rf}$.



(a) Model (b) Small Signal Circuit

Figure 2-5: (a) Circuit Model of PIN Diode in two parts - two ideal PN diodes with capacitance C across them for reverse-bias operation, and the variable resistance R_{rf}. (b) Small Signal Equivalent Circuit of PIN Diode - r_d and C_d are small signal parameters of a standard diode. [33]

From the equivalent circuit in Figure 2-5(b), we see that Z is actually frequency dependent. At low (down to DC) frequencies, the PIN diode behaves as a standard PN diode. In thin PIN diodes (where the device geometry is less than unity) R_{rf} is less than r_d, so for large currents, $Z \approx 2r_d$. At high frequencies, C_d shorts out r_d and $Z \approx R_{rf}$. The two approximations for Z at low and high frequencies hold for all non-zero values of forward bias current.

The current level affects the linearity of the variable resistor. Ideally, R_{rf} is K/I_d, where K is a constant value that is a function of the parameters in Equation 2.2. In

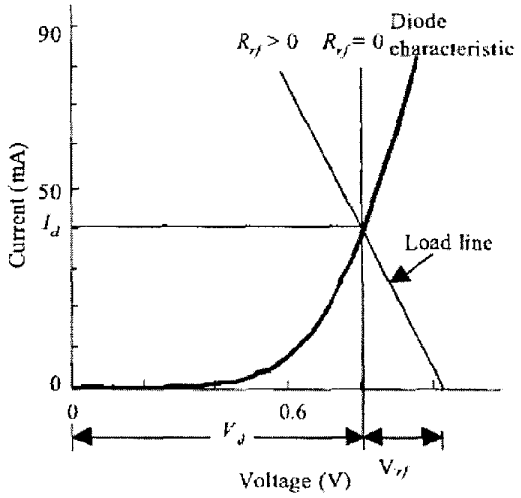


Figure 2-6: I-V Characteristic of PIN Diode, with standard PN I-V curve and load line for non-zero R_{rf} for high frequency operation of the diode. [30]

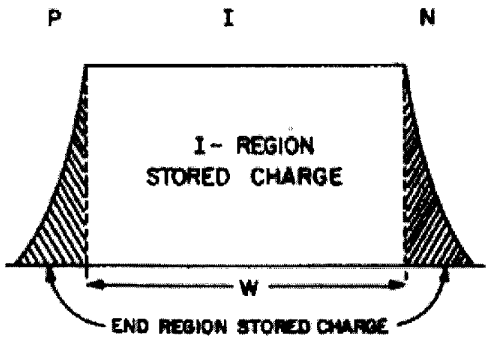


Figure 2-7: Plot of charge stored in a forward biased PIN diode, including end-region and intrinsic-region stored charge. [31]

the high-frequency case where Z is dominated by R_{rf}, increasing the DC bias current does not increase Z linearly. At low levels of bias, $\tau_{eff} \approx \tau$, which is a parameter that can be extracted experimentally and is not a function of bias current itself. Then K is a constant value and $R_{rf}I_d$ product is also constant. At higher levels of bias, there is a greater injection of carriers into the intrinsic region, and a buildup at the end regions occurs, as seen in Figure 2-7. There is a nonlinear increase in recombination rates in the end regions, which lowers the amount of charge stored in the intrinsic region. The effective charge in the intrinsic region is not $Q = I_d\tau$ anymore, but a new $Q_{eff} = I_d\tau_{eff}$ where τ_{eff} lumps the effects in the end regions with the intrinsic-region behavior for an empirical effective carrier lifetime [31].

Oftentimes, the parasitic elements are modeled in the PIN diode equivalent circuit to account for packaging. For example, a parasitic inductance L from packaging may be added in series with R_{rf}, making it a series RL circuit in forward bias. For simplicity, we design the PIN diode into the system without considering the L, because the 70MHz frequency of interest is not near the RF range that PIN diodes are often used.

The PIN diode used was the BAP50-05 from Philips Semiconductors. This double diode package (common cathode) provides a forward resistance up to 600Ω from 10μA to 10mA bias current [14]. Since 70MHz is not quite RF, we redefined R_{rf} to be R_{PIN}. Fitting the datasheet points to the I_d v. V_{PIN} curve, R_{PIN} can be modeled to have an exponential relationship with I_d,

$$R_{PIN} = AI_d^{-K}, \tag{2.4}$$

where A and K are determined by curve fitting the datasheet values of the BAP50-05 PIN diode [14]. A was found to be 14.538 and $K = 0.6862$ in Figure 2-8.

With I_d measurements and extrapolated A and K values from the PIN diode model, the diode resistance was plotted across a range of forward bias current, shown in Figure 2-9.

2.5 Varactor Diodes

Varactor diodes provide a variable capacitance as a reverse bias voltage is applied to the diode junction. If a diode is reverse biased, then there is a region void of carriers, nominally called the depletion region. The reverse-biased diode then is a P-region (plate), depletion region (dielectric), and a N-region (plate), which models a capacitor. The variable capacitance value arises from the change in depletion region in response to the applied voltage. Oftentimes, varactors are used for tuning over a range of frequencies. At higher frequencies, there is a wider tuning range possible for varactors. The varactors used are the Philips BB207 double diode package [15].

2.6 Mixers

Much of the pre-ADC design of this application resemble a standard receiver system where a signal is shifted in frequency then goes through a signal processing chain of various amplifiers and filters before being sampled by the ADC. In the design for the new application, mixers, amplifiers and filters will also be used. Thus design

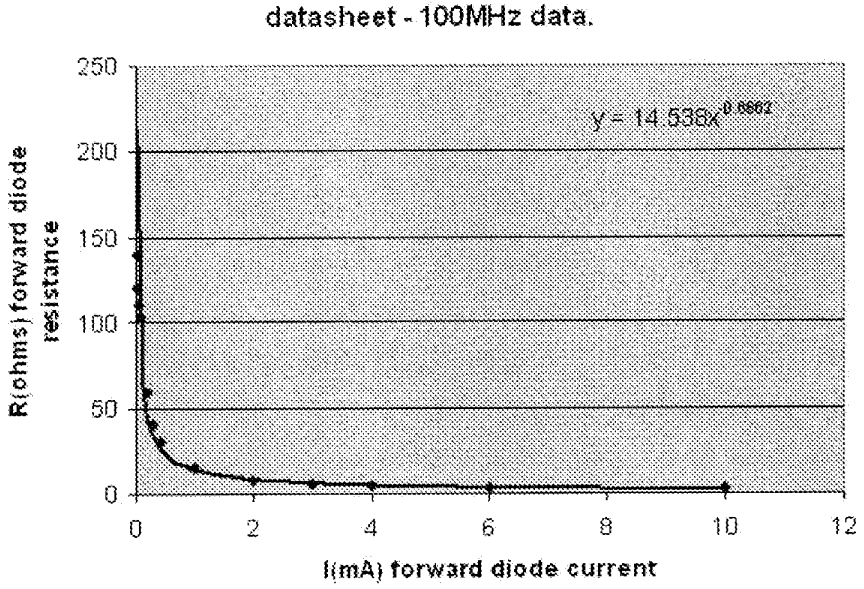


Figure 2-8: Fitted Curve to BAP50-05 Datasheet Values for 100 MHz Data.

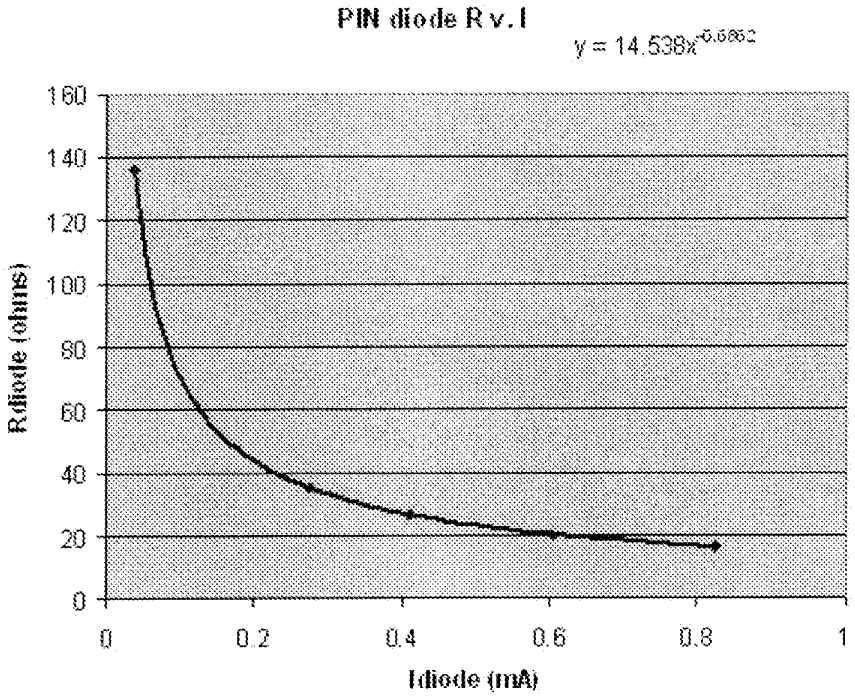


Figure 2-9: Diode Resistance Derived from Datasheet Equation, at $f_c = 70$MHz.

considerations for each of these analog components are important. Here, we look at the mixer design in more detail. In the proposed work, mixers will be used in the low frequency (MHz) domain instead of the RF domain. Their primary function is to perform upconversion like in transmitter systems rather than downcoversion mixers in standard receivers.

The mixer takes an input, often a low noise amplified signal, and translates it to a different frequency. Frequency translation is possible through the linear addition or subtraction of frequencies. The design of the mixer will be extremely important in this thesis because it is here where many considerations of modulation, noise, image rejection, and others must be accounted for in order to translate low-frequency signals to the IF band for further processing.

The mixer takes two signals and multiplies them in the time domain. Mathematically, if the two signals are $A\cos(\omega_1 t)$ and $B\cos(\omega_2 t)$, the product of the two signals is:

$$\frac{AB}{2}[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t]. \tag{2.5}$$

The output of the mixer results in two output signals operating at the sum and difference of the two input frequencies. The mixer stage in the receiver is shown diagrammatically in Figure 2-10.

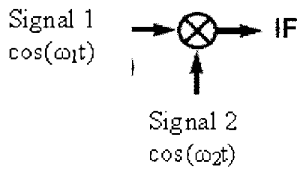


Figure 2-10: Mixer Diagram.

Signal 1 and Signal 2 multiply to produce a frequency shifted output signal in the IF Band. From Equation 2.5, A=B=1.

There are several nonidealities in mixers that need to be considered in design. Noise, linearity, dynamic range and isolation are discussed briefly.

Noise figure characterizes how effective the device is at rejecting noise while maintaining the signal. It is defined as the ratio of input signal-to-noise ratio (SNR) to output IF SNR. It varies across different types of mixers because it is highly dependent on whether or not both output frequencies are desired. If both bands (frequencies) are desirable because they contain useful information, there is twice the signal power. Noise figure improves in this case, which is termed the double-sideband (DSB) case. In the single-sideband (SSB) case where only one of the bands is considered, the noise figure is degraded by 3 dB ($3dB = 10\log(0.5)$). In the case that the mixer has the worst noise figure in the system additional pre-mixer stages may be necessary to improve the noise figure of the system. If SSB is preferred, it is possible that an image rejection filter will be implemented before the mixer to greatly attenuate the image signal before mixing.

Here, linearity and dynamic range are also important in mixer design. Linearity characterizes how the mixer output amplitude (power) varies as the input amplitude (power) changes, at a given frequency. Besides noise figure, gain, and power consid-

erations, the mixer must maintain linear operation with both strong and weak input signals. Distortion, in particular when a weak signal is in presence of a strong interfering signal, must be minimized. This is cruical in the application of ultrasound. Dynamic performance of the system may be dominated by the dynamic performance of the mixer as it is not only the first element in the signal chain but also a challenging element to design.

There are many topologies for mixers, such as square law mixers, multiplier based mixers and double-balanced mixers, to name a few [17]. Since dynamic performance is important, the active double-balanced mixer was selected. Active devices, although they require power, can provide conversion gain instead of loss. A double balanced mixer provides better isolation between the local oscillator and the output port of the mixer. Image reject and I/Q mixers were considered for SSB to properly obtain one sideband. However, these mixers are much more complicated. For this application if good filtering through SAWs can attenuate both the clock and image feedthrough signals, then the more complicated mixers are not necessary.

The mixer used in the thesis is Linear Technology's own LT5521 active double-balanced mixer. It has low distortion, 40dBm clock feedthrough, and an impressive 24.dBm output IP3 at output frequency 1.95GHz. The noise figure is acceptable at 12.5dB. Although designed for high frequencies, it is usable at the intermediate frequencies if it is designed with the proper network. The topology of the LT5521 follows a Gilbert cell mixer, with differential inputs feeding into degenerated common emitters of the differential pairs in the Gilbert topology [17]. The high frequency local oscillator switches between the differential pairs. The open collector differential output has 300Ω resistance across it. Additional information can be found in [2].

2.7 Amplifiers

The test experiment used two low noise AH31 amplifiers, with +16 to +20dB gain over 44MHz to 95MHz. The application circuit is shown in Figure 2-11. The ouput IP3 point is 42dBm at 75MHz and the noise figure is 2.4dB. Both amplifiers were

needed to ensure that the mixer would not be overdriven by a large input power. It is recommended that +20dB gain amplifiers with very low distortion are used in the system. It is also desirable to have a more limiting bandwidth amplifier. A bandwidth less than the Nyquist zone prevents foldback of any noise or distortion from the amplifier.

2.8 Analog-to-Digital Converters (ADCs)

The LTC2249 14-bit 80MSPS analog to digital converter was used for this particular experiment. This six stage pipelined ADC is low power, high resolution, and has 73dB SNR. Refer to [1] for more information.

2.9 Clock Sources

The clock rate of 70MHz is a typical intermediate frequency (IF) and many components such as SAW filters and IF amplifiers are designed with a center frequency of 70MHz, or a multiple of it. Two clocks are required: one for the ADC sampling source and another for the upconversion local oscillator (LO). The design lab owned a 70MHz crystal oscillator. For a clock frequency other than 70MHz, a narrowband tunable helical filter with a standard signal generator can be used as a clock source.

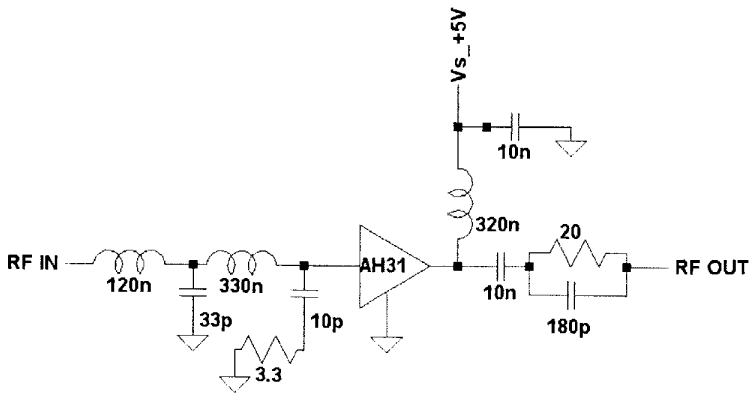


Figure 2-11: AH31 Amplifier Application Circuit.

Chapter 3

Design Modifications

3.1 Setup

In the application setup, there were many design considerations in the system. Some design changes were made after initial setup of the application, done in the Design Lab. Some design modifications were made directly on the demonstration boards while some required construction of a new part. Tools used were laboratory measuring and analyzing tools and programs for design and simulation.

3.2 Simulation

The program used for simulation was Linear Technology's SwitcherCAD SPICE simulator, available online at zero cost. Models of various components and filter designs were constructed in this program, and laboratory results were compared to simulation output.

3.3 Design

The signal chain, shown again in Figure 3-1, starts with a low frequency signal which is translated to a higher frequency using the LT5521 before going through a series of amplifiers, filters, and varying element networks. The end of the signal chain goes

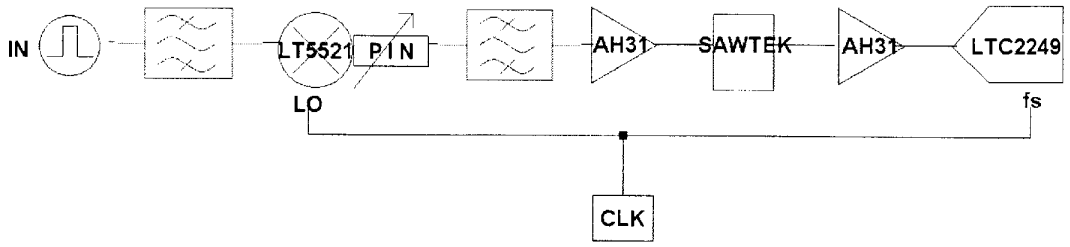


Figure 3-1: Frequency Translation Method General Block Diagram.

into the ADC input and is sampled by a clock source for data conversion.

Design components in the thesis were broken down into four categories: passive filters, mixer, variable gain devices, variable filter devices. Each component design is detailed in its own section, with references back to the complete system design.

3.3.1 Filter Design

The signal is filtered throughout the pre-ADC path in order to present a high quality, undistorted signal at the ADC input. Several types of filters are needed and were investigated for appropriate applications. The filters designed and used in this frequency translation method include: 1MHz – 40MHz cascaded lowpass–highpass elliptic section filter, 70MHz Butterworth wideband bandpass filter, 60 – 86MHz variable bandpass filter.

A 1MHz–40MHz bandpass filter was designed to filter the low frequency signal before upconversion. This filter was comprised of cascaded lowpass and highpass elliptic sections, each 5 poles. The filter design tables were taken from Williams' *Filter Design Handbook* and modified for a 1MHz high pass and 40MHz low pass with stopband attenuation $A_{min} = 40dB$ at a stopband frequency at 70MHz [38]. The high pass filter has a stopband frequency at 800kHz.

The 70MHz bandpass filter is designed with more relaxed requirements, because other components in the signal chain will subsequently filter the passband signal content. The bandpass filter diagram in Figure 3-2 shows the design specifications. In the passband, it is desirable to have as little loss from input to output. The

designed filter has -0.7dB insertion loss. It is also desirable for this bandpass filter to block reflected waves in the passband. The S11 or S22 parameters indicate return loss, so minimal levels of return loss in the passband is desired. A -24dB return loss in the passband is sufficient for the application. The filter performance matches expectations from simulation.

Elliptic sections, although more complicated to design than Butterworth or Chebyshev filters, provide a steeper stopband response and hence greater attenuation in regions outside the passband. These filters are useful for providing a steep attenuation at each of the stopbands. To prevent any interference from input signal harmonics at or around the local oscillator of the mixer, it is advantageous to design an elliptic section filter with a stopband at the particular local oscillator frequency. In the test system, LO=70MHz, so this 1MHz-40MHz filter has a stopband at 70MHz with 55dB attenuation. The schematic is shown in Figure 3-3(a).

The system requires approximately 20dB gain while using lossy SAW filters so two AH31 amplifiers are needed after the mixer and before the ADC to achieve a full scale ADC input. Instead of having the mixer output go straight to one of the amplifiers, it is better to bandpass filter the signal before one of the amplifiers. This ensures second (and higher order) harmonics are not passed through the amplifier, which will cause

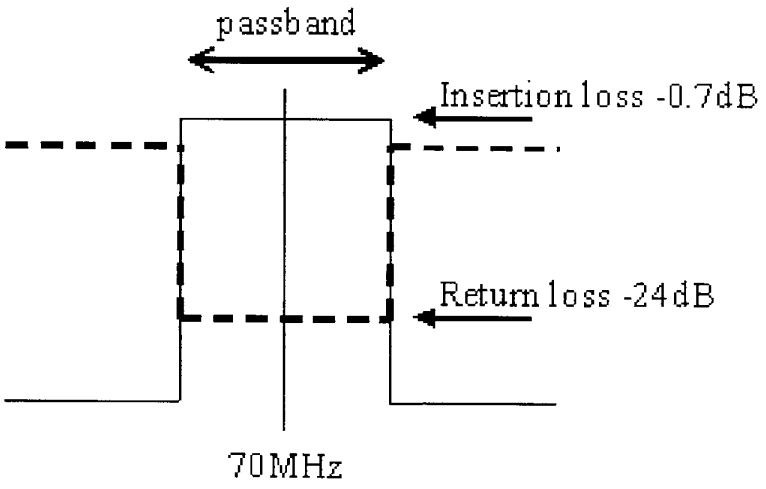
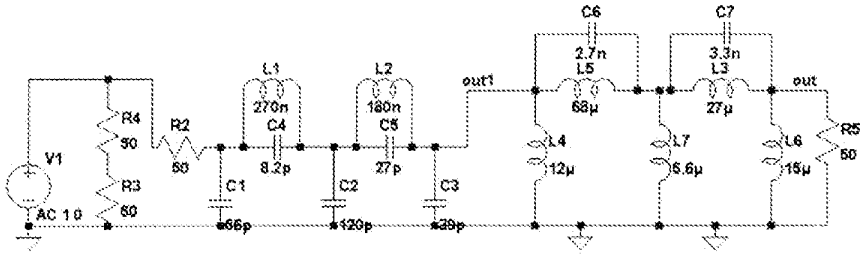
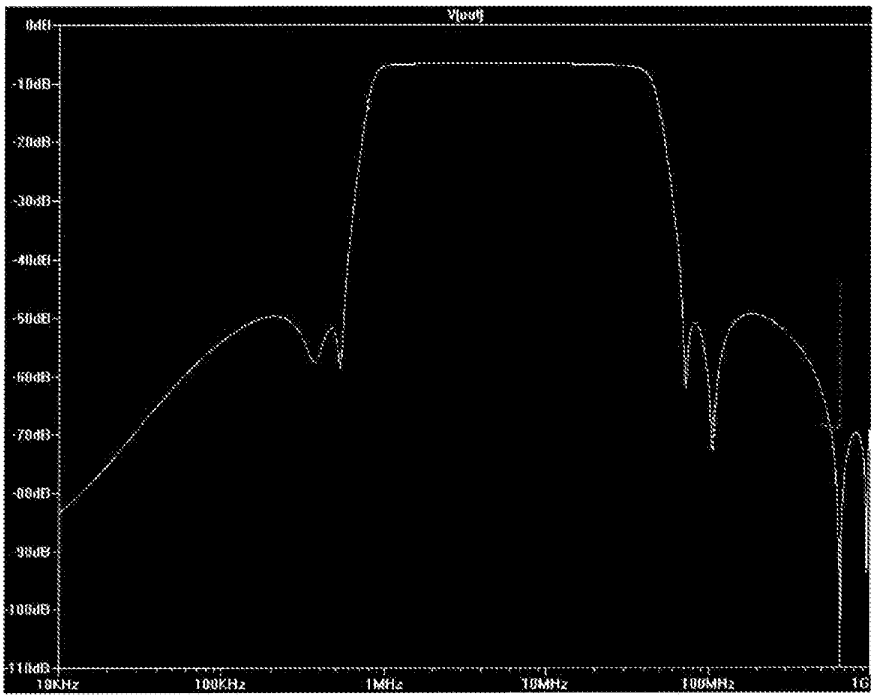


Figure 3-2: Diagram of 70MHz wideband bandpass filter.



(a) Schematic

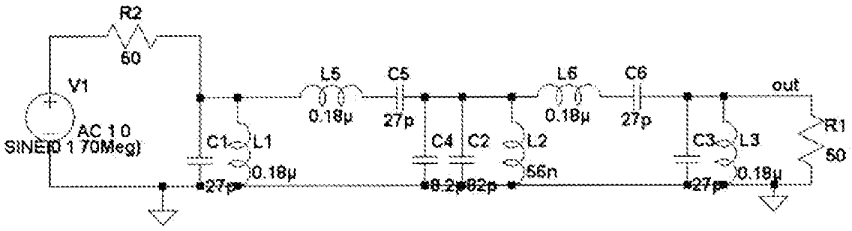


(b) Simulation

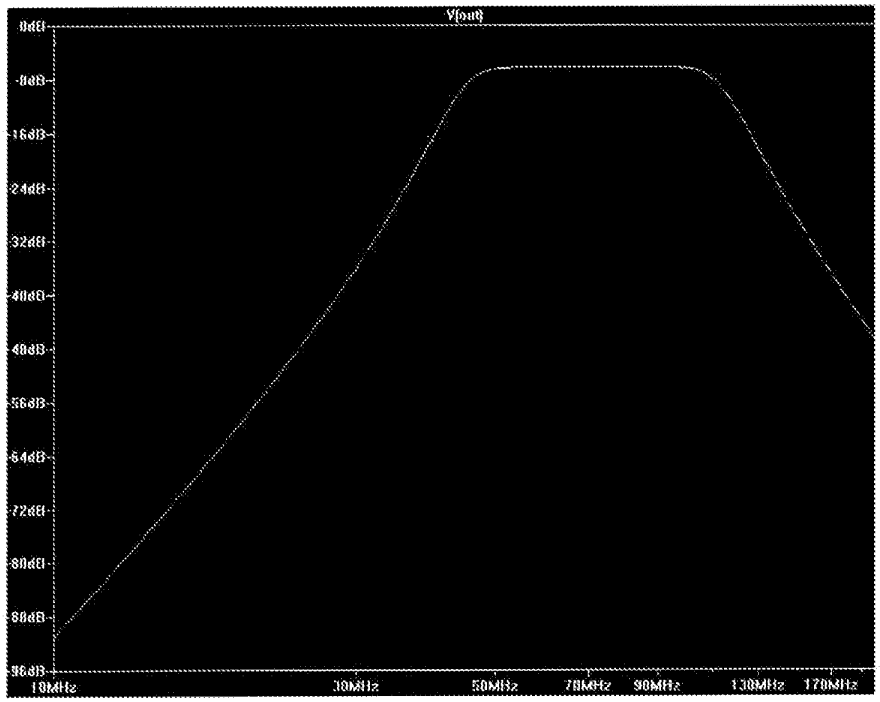
Figure 3-3: Passive Low Frequency Bandpass Filter.

distortion. The filter designed need not have a steep stopband attenuation factor, so elliptic sections are not required. A standard butterworth bandpass filter will suffice.

For a mixing LO frequency of 70MHz, a 40M – 100MHz 5-pole bandpass filter was designed, with -1.3dB insertion loss. The filter attenuates the 140MHz second harmonic by 24dB. The simulation results in Figure 3-4(b) match the design expectations and lab implementation.



(a) Schematic



(b) Simulation

Figure 3-4: Passive Bandpass Filter, $f_c = 70$ MHz

The variable filter, useful in some applications, was designed to provide approximately 20 – 30MHz variation. The discussion of this design is reserved for Section

3.3.4.

3.3.2 Mixer Network Design

The LT5521 was designed for an IF input and an upconversion to RF (GHz) and thus the DC642A demonstration board was configured for such an application. Because this frequency translation is operating at a much lower frequency range, modifications to the demo board circuit must be made to maximize the performance of the mixer.

The existing stock DC642A is shown in Figure 3-5 for $f_{IF} = 250MHz, V_{cc} = 5V$.

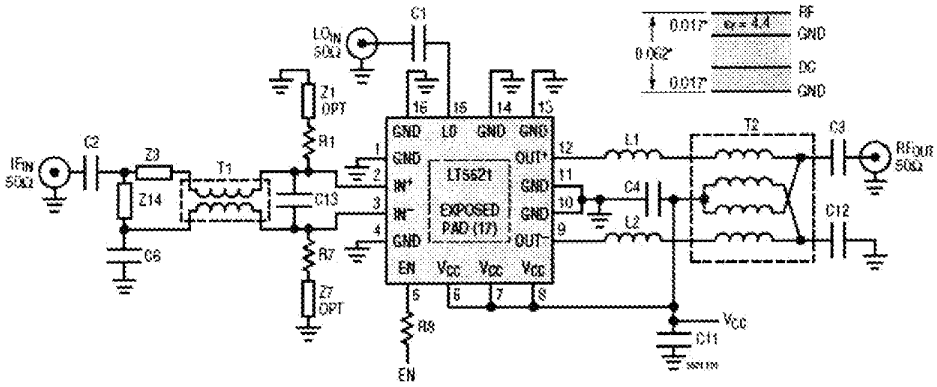


Figure 1. Demonstration Board Schematic

Table 1. Demonstration Board Bill of Materials[1, 2]

REF	f_{IF} = 250MHz, f_{RF} = 1.95GHz f_{LO} = 1.7GHz, V_{CC} = 5V	f_{IF} = 44MHz, f_{RF} = 1.045GHz f_{LO} = 1.001GHz, V_{CC} = 5V	f_{IF} = 250MHz, f_{RF} = 1.95GHz f_{LO} = 1.7GHz, V_{CC} = 3.3V
R1, R7	110Ω, 1%	110Ω, 1%	22.6Ω, 1%
Z14	18pF	120nH	18pF
Z3	0Ω	150pF	0Ω
L1, L2	2.7nH	10nH	2.7nH
T1	M/A-COM MABACT0010[3]	M/A-COM MABACT0010[3]	M/A-COM MABACT0010[3]
T2	M/A-COM ETC1-6-4-2-3	M/A-COM ETC1-6-4-2-3	M/A-COM ETC1-6-4-2-3
C1, C13	6.8pF	27pF	6.8pF
C3	82pF	3.9pF	82pF
C12	82pF	1nF	82pF
C2, C4, C6	1nF	1nF	1nF
C11	1µF	1µF	1µF
Z1, Z7	0Ω	0Ω	180nH
THIS COMPONENT CAN BE REPLACED BY PCB TRACE ON FINAL APPLICATION			
R8	10k	10k	10k

Note 1: Tabulated values are used for characterization measurements.
Note 2: Components shown on the schematic are included for consistency with the demo board. If no value is shown for the component, the site is unpopulated.
Note 3: T1 also M/A-COM ETC1-1-13 and Sprague Goodman GLSW4M202. These alternative transformers have been measured and have similar performance.

Figure 3-5: LT5521 Stock Demonstration Board (DC642A).

To adjust for a 1M – 10MHz input IF frequency, the coupling capacitors C2, C6,

C3 and C12 were changed to 100nF capacitance. L1 and L2 were replaced with wires for minimal resistance. T1 and T2 must be selected for the appropriate impedance matching and frequency. It was suggested[1] T2 be a 4:1 MABAES0054 transmission line transformer, with 5-1000MHz frequency range, -1dB insertion loss [10].

In initial testing of this circuit, it was discovered that there was a considerable DC offset at the output. Since the upconverted signal is sampled at a rate equal to the clock (LO), any clock feedthrough would be interpreted as DC offset. With the stock DC642A, there was offset on the order of 100-150mV from clock feedthrough. This offset is significant and reduces the dynamic range of the signal (there will be considerable clipping on one side of the signal, distorting the final output).

If LO feedthrough is significant, then DSB is not a practical method with this application because the LO frequency will pass through to the ADC. But design modifications can be made to attenuate carrier feedthrough. The bottleneck was found to be in the mixer design. Because the mixer was designed for much higher frequencies, certain transformers provide better isolation and impedance matching than others. But those transformers cannot be used at IF 70MHz when they are optimal in the GHz range. An unbalanced network at the mixer output can kill any quality output-LO isolation the mixer itself may have. So, even if the mixer datasheet isolation figure given at higher frequencies is about the same at the lower IF frequency, the output network design is important to ensure that there is a balanced differential output. Otherwise, local oscillator feedthrough can become significant.

Measuring the LO-output port isolation on Agilent's 8561EC Spectrum Analyzer, the stock board has -48dBm isolation (no signal at the IN port) with LO=70MHz, 0dBm. However, with an input signal at 3.58MHz -19dBm, the mixer output had the desired signals of -19.33dBm at the sum and difference frequencies (73.58MHz and 66.42MHz) and the undesired LO feedthrough of -52dBm. It is attenuated by only 32dBm from the desired output signal. With a post-mixer gain of about 20dB, the LO feedthrough seen would then be -12dB, which is very undesirable in the upconversion scheme.

[1]Suggestion made by Doug Stuetzle, Designer, Linear Technology. July 2006.

The output circuit was redesigned as such: Instead of just one T2 transformer (the 4:1 MABAES0054), a second transformer follows it, shown in Figure 3-6. This output circuit provides a much more balanced network in the desirable IF output frequencies. T1 is a 1:1 ETC1-1-13 M/A-COM balun transformer, 1.1-3000MHz frequency range, -1dB insertion loss. T1's purpose is to properly convert differential to single ended output. The values of the coupling capacitors were increased from 82pF to 100nF. Also, L1 and L2 are used to configure the output to a particular frequency, but they were replaced with wire again (mixer output directly connects to T2).

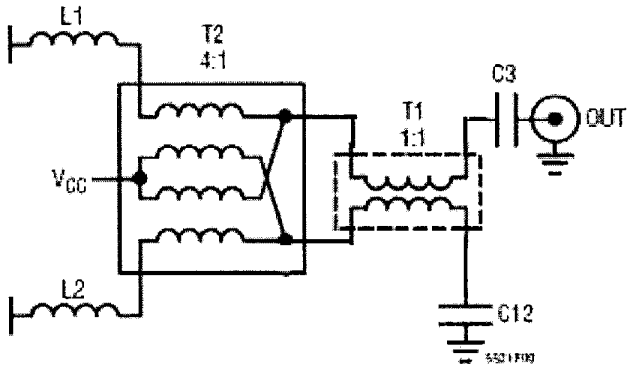


Figure 3-6: Redesigned LT5521 Output Network.

With this design modification, the entire system has a DC offset of -25dB. This is equivalent to 50mV or 400 of 8192 units. This was measured in two ways. The DC level can be measured with the same sample and mixing clock frequency. It can also be measured using PScope with different clocks, offset enough so that they do not a)interfere with each other nor b) lie at the same frequency as the upconverted input signal. The carrier feedthrough was measured to be -25dB in two cases : f_s = 70MHz (ADC clock), LO = 72MHz (mixer); and f_s = 70MHz, LO = 70.5MHz.

However, the spectrum still does not look incredibly clean. There is an elevated noise level about the desired frequency in Figure 3-7. Looking at the input network of the LT5521, it is not matched to at 50Ω output at 70MHz frequency. In fact, it is only 20Ω at 70MHz. This means an impedance transformation must occur through the input network. Thus, a 1:1 balun transformer like the ETC1-1-13 will not be

sufficient. Additionally, baluns at low frequencies (in the 1-10MHz range) do not function as intended, so a flux-coupled transformer is more appropriate. The ETC1-1T is the 1:1 flux-coupled transformer but it is 1:1. A 3:1 flux-coupled WBC3-1TL transformer from Coilcraft works from 0.3-900MHz and a -0.6dB insertion loss. This is the more appropriate choice for the input transformer, to convert the 50Ω line to the 20Ω differential input of the LT5521 mixer.

A quick check was to look at the return loss of the input network before and after impedance matching to a 50Ω transmission line. With the ETC1-1-13 1:1 balun in the input network, the S11 parameter was -3dB. With the WBC3-1TL 3:1 flux-coupled transformer, the S11 parameter was -12dB, a significant improvement over the original setup.

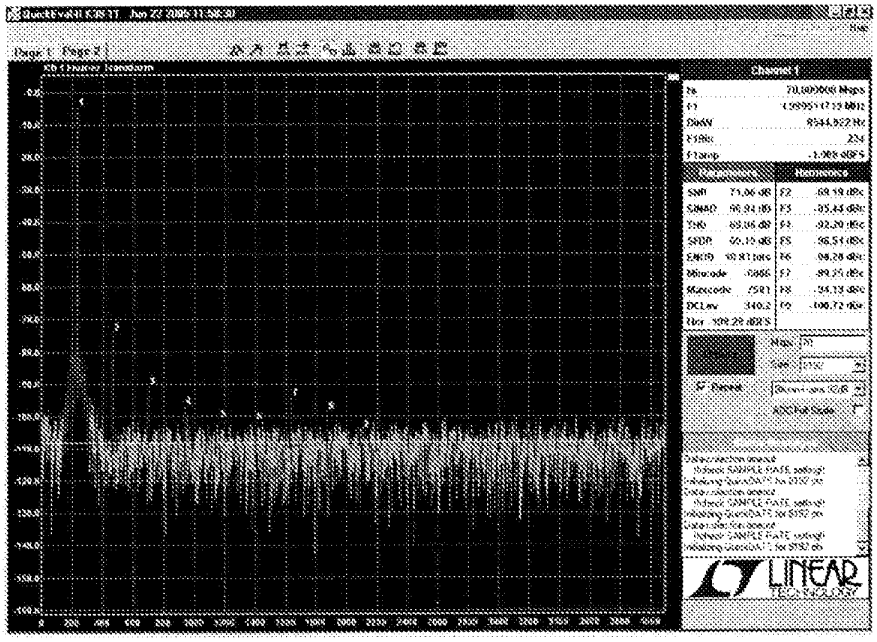
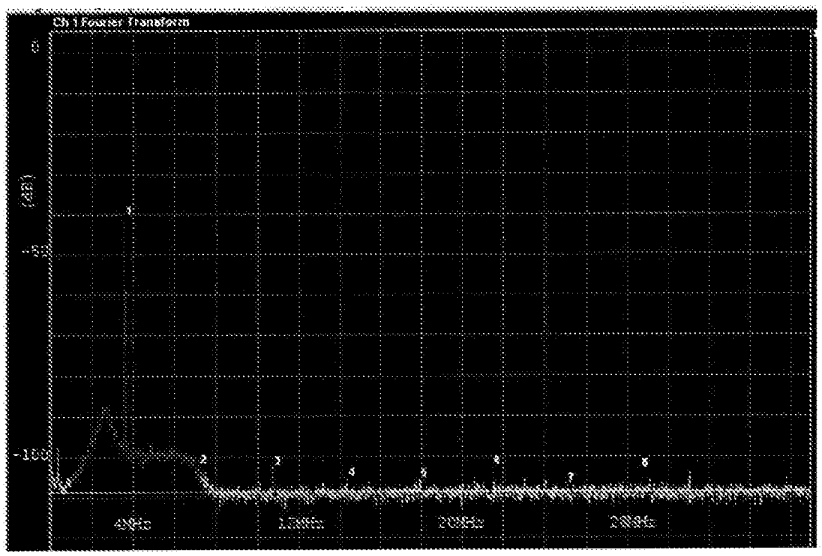


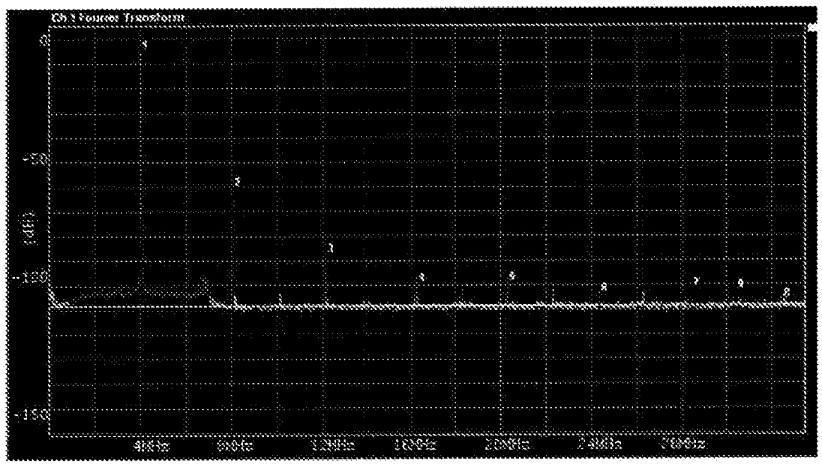
Figure 3-7: Mixer Output – Mismatched Input Impedance.

A comparison can be made between the upconversion scheme with a working modified board and the stock demonstration board, shown in Figure 3-8. The original board is not configured for the specified frequency range and cannot obtain full scale with the same input power level and signal chain as the working board. There is no significant DC level offset because it is attenuated by more than 30dB (expected

fundamental amplitude is full scale at -1dB). The working board can achieve full scale output and a much lower noise floor. The slightly raised noise level about the fundamental frequency is the ADC input bandwidth, limited by the 5MHz SAW filter.



(a) Stock Board



(b) Modified Board

Figure 3-8: Output Improvement with Modified LT5521 Board

3.3.3 Variable Gain Design

The PIN diodes' varying resistance changes the gain of the system. Placing the diodes at the output network of one of the components in the signal chain changes

the output impedance and the overall gain of the system. The mixer output has an internal impedance of 300Ω, so by placing the PIN diode at the output of the mixer, it is possible to achieve an output impedance of $0-300\Omega$. The LT5521 has a differential output, hence the choice of the double diode package (with a common cathode) is very useful here. By placing the two diodes across the differential output, then biasing the cathode of the diodes we can achieve variable mixer output impedance. The PIN diodes are placed right on the legs of the IC package to minimize parasitics on the board like in Figure 3-9.

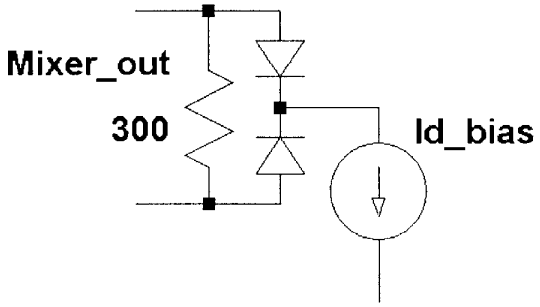


Figure 3-9: PIN Diode Package in System Design.

The anodes of the diodes are biased to the supplies through the center-tapped transmission line T2 transformer. Id_{bias} is determined by a control voltage and resistor $R_b = 180\Omega$. The bias network makes it easy to measure the current through the PIN diodes, using the 180Ω resistor. The voltage drop across the diode is about 0.8V in forward bias, and the voltage drop across R_b can be measured to find Id_{bias}. Each diode receives half the bias current Id_{bias}. The differential impedance of the diode is $2R_{PIN}$, R_{PIN} found in Equation 2.4, and the effective output impedance of the entire mixer network is $\frac{2R_{PIN} \| Z_o}{4}$, where Z_o is the mixer output impedance, and the 4:1 transformer is used. With this variation in mixer output impedance, a range of 27dB attenuation was achieved with a 0-5V bias (see Figure 3-10). The relationship between the overall system attenuation and the effective output impedance is plotted over a 400mV bias range in Figure 3-11.

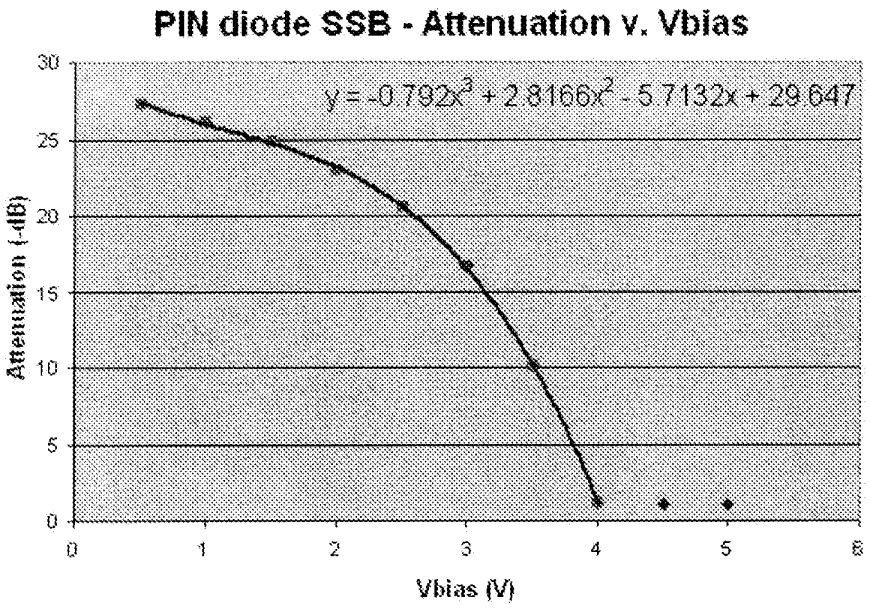


Figure 3-10: System Attenuation v. Bias Voltage on the PIN Diodes.

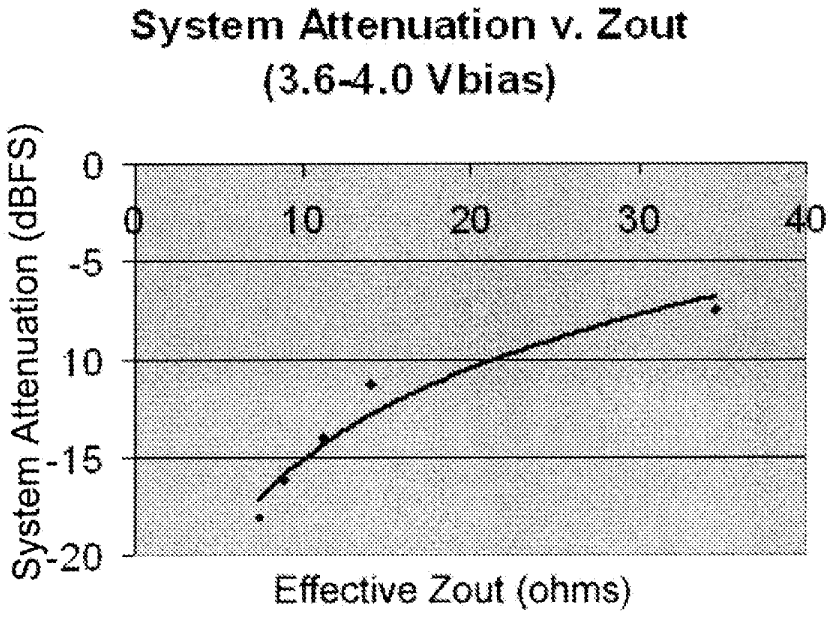


Figure 3-11: Attenuation v. Effective Output Impedance of the System

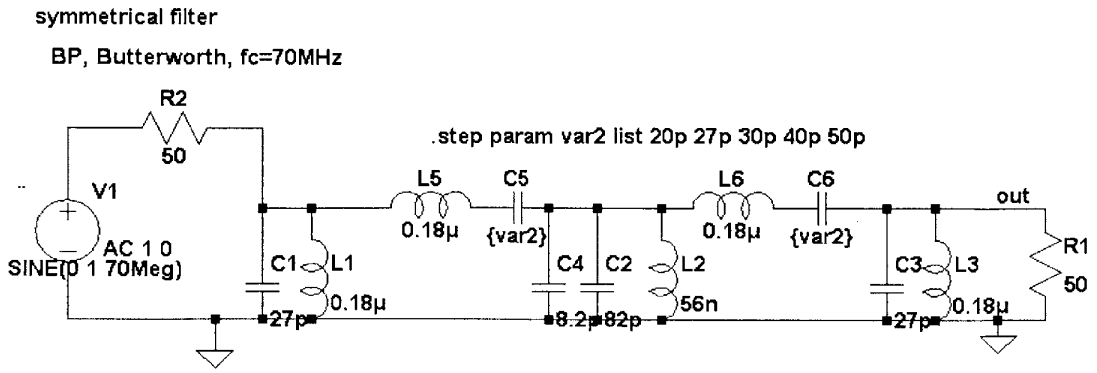
3.3.4 Variable Filter Design

The varactor diodes were fairly simple to design into the system. Each diode acts as a variable capacitor, so placing them in parallel with a capacitor in a filter design will suffice. The diodes can be biased at cathodes with a large resistor and control voltage (much like the PIN diode setup). The challenging part was determining what type of design to actually use. As discussed before, Butterworth and Chebyshev filter designs are easier to design than elliptic section filters. However, a simple test showed that adding varactor diodes into a Butterworth filter was much harder to do than anticipated.

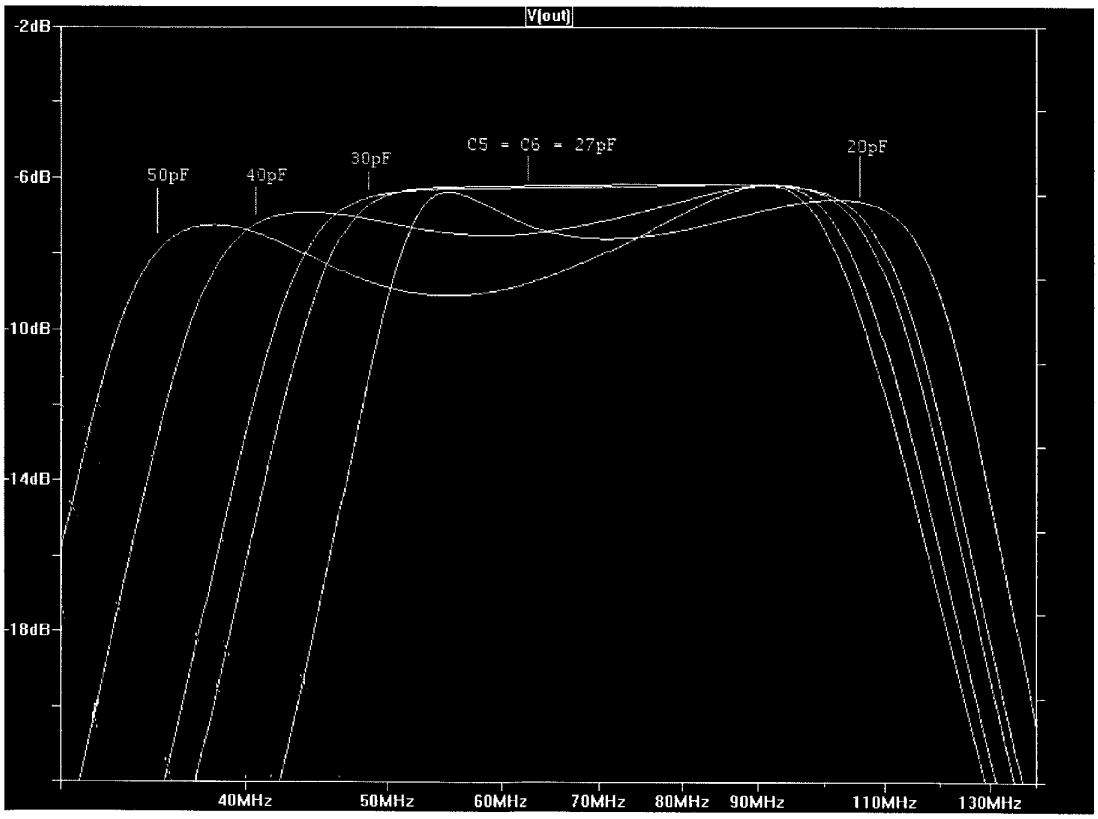
Figure 3-12(a) shows how C5 and C6 values were varied to producing the effects of a varactor diode circuit. To produce the original 70MHz bandpass five-pole butterworth filter, $C5 = C6 = 27pF$. Here, they are varied from 20pF to 50pF. The simulation results in Figure 3-12(b) show an inconsistent filter response across the capacitor range, quite unsatisfactory for a true variable filter. The ideal response is to have the same filter response shifted over a certain frequency range to provide the same performance in the system.

Elliptic sections were considered because their topologies allow for each section to have their own tuning varactor diodes. Construction of these filters with varactor diodes are easy, because the diodes can be just placed on top of each elliptic section. Although this is not a wideband filter, highpass 7-pole and lowpass 5-pole elliptic filters were designed independently, so that the effect of variable filter could be observed independently at each 3dB point. Figure 3-13 shows the two elliptic filters individually with varactor diodes. For the low pass filter $f_{3dB} = 80$MHz and for the high pass filter, $f_{3dB} = 70$MHz. These results show the highpass filter with varactor diodes across one of the elliptic sections. The behavior deviates from the expected response around the 3dB frequency.

Combining the two elliptic section filters as in Figure 3-14(a), and placing varactor diodes on each elliptic section to maintain the same response, produced the bandpass response in Figure 3-14(b). The varactor diodes are modeled in SPICE with the line



(a) Schematic



(b) Simulation

Figure 3-12: Variable Filter Design using Passive LC Bandpass Filter. In (b) the 5 plots correspond to simulations for different capacitor values (C5 and C6 as shown in (a)).

statement :

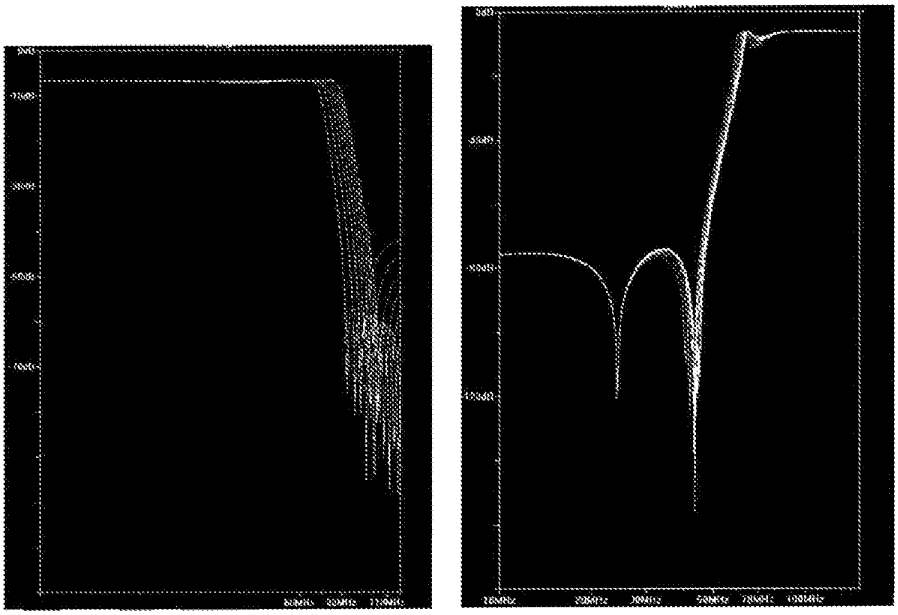
$$.model\ BB207VarCap\ D(R_s = 0.3\ \ C_{jo} = 122.5p\ \ M = 0.81153\ \ V_j = 1.4881$$
$$\text{mfg} = \text{Philips}\quad \text{type} = \text{Varactor})$$

The V2 voltage source is stepped from 1 to 10V, with 3-10V being the suitable operating range in the actual system setup. Each section has additional capacitance from the BB207 package and they are all stepped by the V2 voltage source.

The resultant elliptic section bandpass filter in Figure 3-14(b) shows consistent filter response across 60 to 85MHz. There is less than 0.2dB ripple in the passband across the filter range.

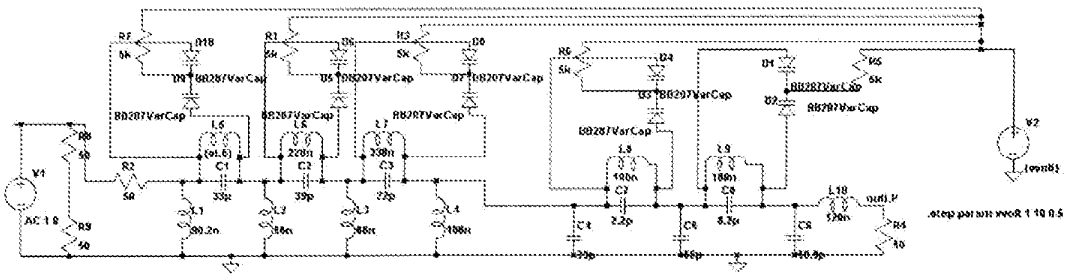
Figure 3-14(c) is the actual filter response of the design constructed on a copper clad board, with 50Ω transmission line. The measurement was made by the Network Analyzer. There is a greater change in passband insertion loss, but the filter response is similar to expected results.

The system achieved 60 to 86MHz variable filtering across a 10V bias range of the varactor diodes. From the network analyzer, the constructed elliptic bandpass filter

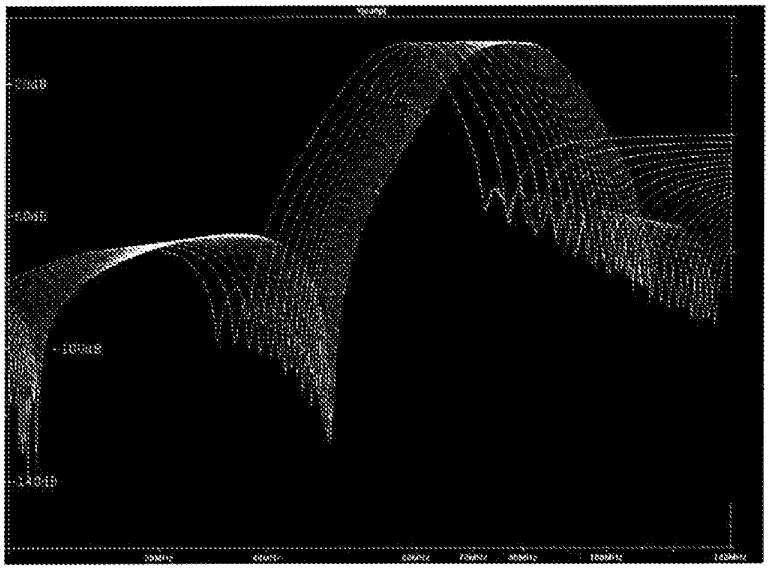


(a) Elliptic Low Pass Filter (b) Elliptic High Pass Filter

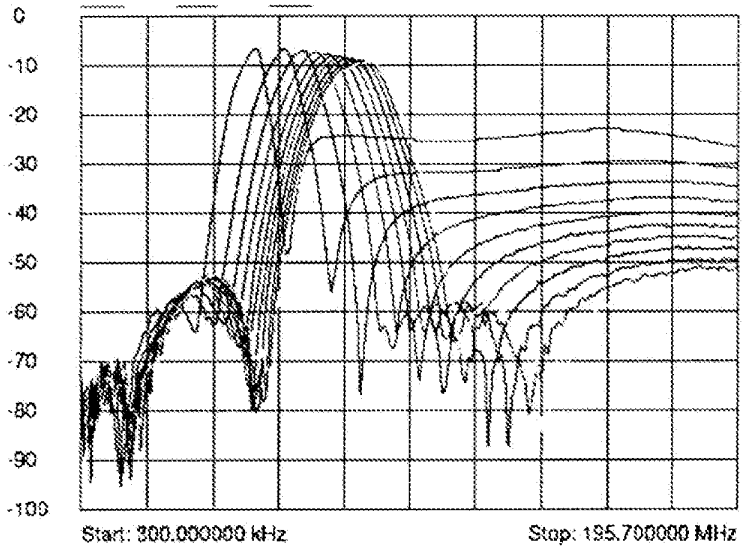
Figure 3-13: Simulation of Elliptic Filters with Varactor Diodes



(a) Schematic



(b) Simulation



(c) Network Plot

Figure 3-14: Elliptic Bandpass Variable Filter

has characteristics shown in Table 3.3.4.

Voltage Bias (V)	Center Freq (MHz)	S22 (-dB)
0	51.87	26
1	60.66	16
2	65.88	13
3	70	11.3
4	73.6	10.4
5	76.31	9.5
6	78.64	9
7	80.535	8.5
8	82.236	8
9	84.4	7.8
10	86.2	7.5

Table 3.1: Variable Filter Characteristics

The entire upconversion scheme with the varactor diodes biased at 2.8V, a 70MHz clock, and 2MHz input has 69dBFS SNR. As expected, adding variable filtering did not compromise the dynamic performance of the system.

3.3.5 Design Conclusion

Each component design was unique and challenging in its own respects, with novel techniques used to ensure practical implementation. Besides designing actual circuit networks, construction of the filters and setup of the system (it is after all heavily application based) are very important. I was able to design filters that work close to expected results from simulation, and achieve an improvement in results from mixer design. It became clear that filter and mixer design are two limiting components of such a frequency translation scheme. However, other application issues arise, as the next section highlights in the presentation and interpretation of results.

Chapter 4

Applications Setup

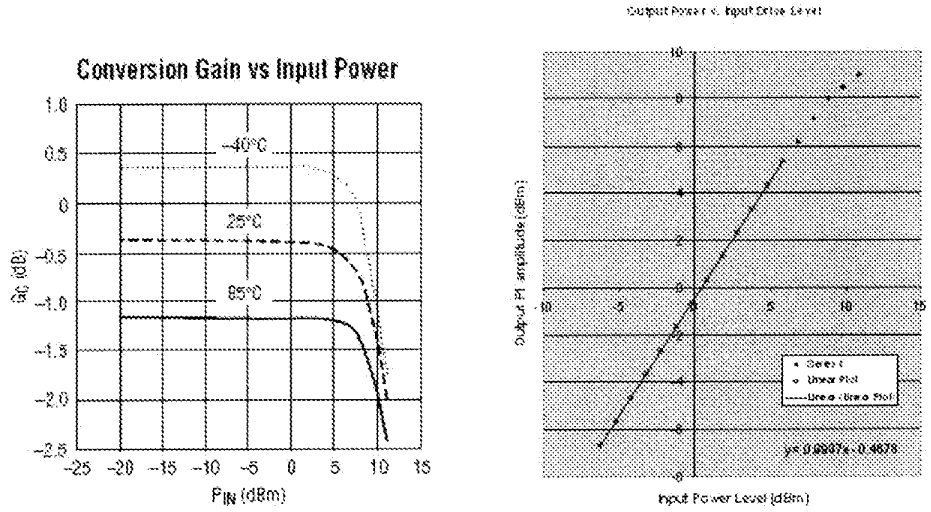
The setup for the application system was carried out in the Design Laboratory of Linear Technology in Milpitas, California under the supervision of one of the senior application engineers. Standard lab equipment was used and all components were either samples from the company or designed myself. The proprietary program PScope developed at Linear Technology was used to process the digitized signal with an 8192-point FFT and Blackman-Harris windowing function. Equipment used included signal generators from Hewlett Packard (model 8644B, 100kHz - 3.2MHz frequency range), a network analyzer from Hewlett Packard (model 8753C, 300kHz-6GHz frequency range), and a spectrum analyzer from Agilent (model 8561EC, 30Hz-6.5GHz frequency range).

This section describes some applications setup issues encountered in designing the frequency translation system. Most are standard high frequency issues not usually seen by ultrasound customers but are everyday issues for radio designers. Signal overdrive, reflected waves, impedance matching, single side-band, and double side-band are discussed here.

4.1 Signal Input Limitations

The signal level into the mixer cannot be too high. If overdriven, the mixer outputs a distorted signal compared to the lower frequency input, rather than a pure frequency-

shifted signal. For linearity, it is best to keep the input range less than 5dBm for the LT5521 [2]. A simple experiment verified datasheet specifications. Figure 4-1(a) shows that the gain falls drastically at $P_{in} > 5dBm$. The mixer input was driven from -24dBm to above 10.8dBm but the region of interest (-5 to +10 dBm) is plotted here in Figure 4-1(b). Up to 5dBm, the output fundamental amplitude and input power level have a linear relation, slope of 1 and gain approximately -0.5dBm (the intercept). Above 5dBm, the mixer reaches saturation because the points fall from the linear extrapolation, indicating that the mixer is now overdriven.



(a) Datasheet Figure, IN=250MHz and LO=1.7GHz. [2]

(b) LT5521, IN=4MHz and LO=70MHz

Figure 4-1: LT5521 Output v. Input Power

Thus, there is a minimum amount of gain required to bring the mixer output to full scale for the ADC. With a minimum 5dBm mixer input, -0.4 mixer conversion gain[1], and required +10dBm analog ADC input produces -1dBFS fullscale output, the minimum gain post-mixer is 4.67dB. The PScope plot in Figure 4-2 shows the distorted output due to an overdriven mixer. Using just one AH31 amplifier, one SAW filter (narrowband 5MHz bandwidth) and proper attenuator pads, the post-mixer gain was about 4-5dB, which is barely enough. There is significant distortion from the harmonics.

[1]Measured with Agilent 8561EC Spectrum Analyzer, with the modified LT5521 network design.

4.2 Clock Jitter

Clock jitter is a slight variation in the period of the signal, due to noise in the oscillatory system. Statistically, the period can be modeled as having a Gaussian distribution[25]. The jitter induces error in the output voltage proportional to jitter magnitude and input slew rate[26]. At higher frequencies and therefore higher slew rates, the effect of jitter is more pronounced. Since this application shifts a signal to higher frequency, clock jitter issues may arise.

With two clocks - one for the frequency translation and one for the ADC sampling, the jitter from the clocks can create an elevated noise floor or induce close in-phase noise about the fundamental signal. These effects degrade the dynamic range and the SNR of the system.

Since the upconversion will shift the signal to the IF range, which is in the range of sampling frequencies for the LTC2249, it proved advantageous to sample and shift

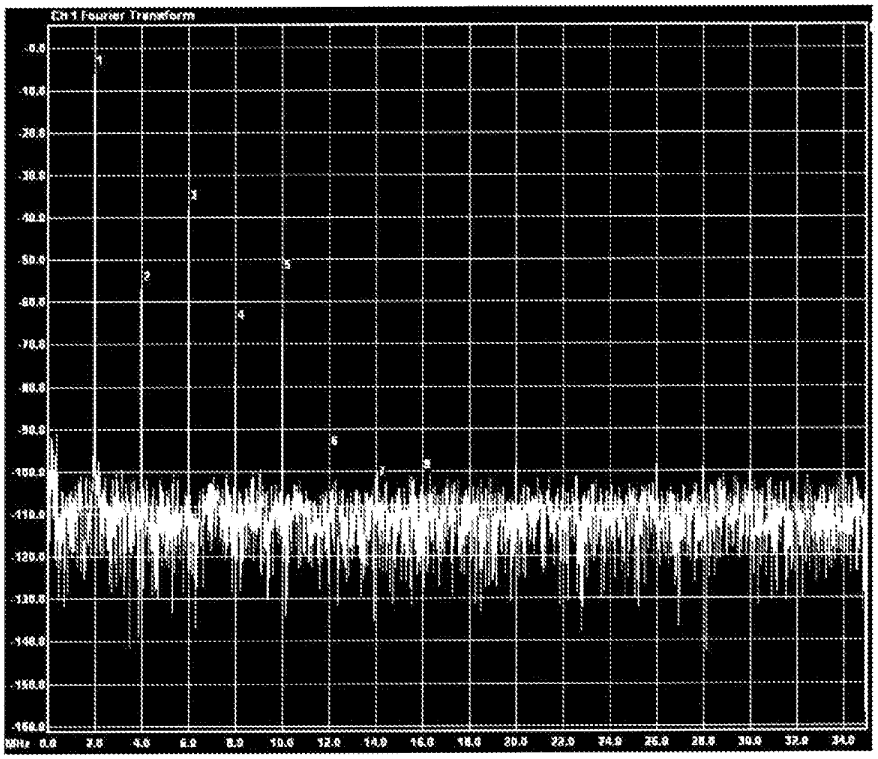


Figure 4-2: Input Overdrive System.

with the same clock source. Any oscillator fluctuation (in time or frequency) will at least be from the same source. The only difference between the two clock signals is the relative phase difference seen at the ADC, since one clock signal is at the front of the signal chain, and one clock signal samples the ADC. Jitter and random phase fluctuations should be cancelled out using the same clock source. Using the same frequency for LO and f_s in the upconversion scheme will make carrier feedthrough look as a DC offset, eliminating it from the AC spectrum.

Figure 4-3 illustrates the effects of two 70MHz clock sources used for f_s and LO, with a 2MHz input into the system. The noise floor is elevated considerably due to oscillator phase noise.

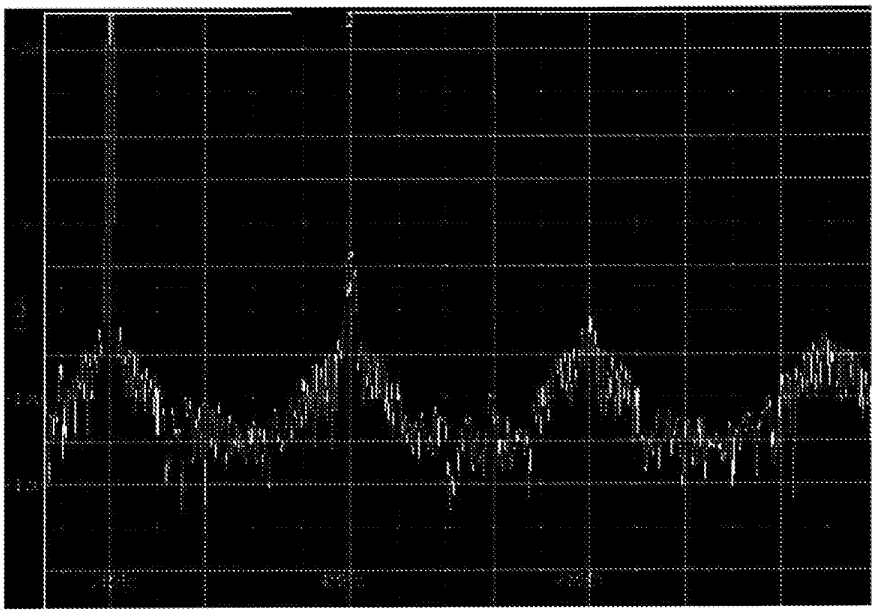


Figure 4-3: Separate Clock Sources for ADC and Mixer.

The work presented here assumes the same clock source unless otherwise indicated.

4.3 Reflected Waves

In higher frequency applications, reflections can affect the system output quality. The measurements used to determine the quality of the system in minimizing reflections are the S parameters, namely the S11 and S22 return loss parameters. Thus, it is

important to look at these parameters of each device in the signal chain. The AH31 amplifiers report S11 = S22 = -25dB and the LC bandpass filter has S11 = S22 = -16dB, which indicate there is sufficient attenuation of reflected waves. However, the SAWTEK filters do not have good S11 and S22 parameters. The data in the Figures 4-4, 4-5, and Tables 4.1 and 4.2 are from published online data from the vendor[2]. In the 5MHz bandwidth SAW, the S22 parameter in the passband is only 7-10dB attenuation. In the 20MHz bandwidth SAW, the S11 and S22 parameters are poor at about 3-5dB attenuation.

In a cascade system as in the presented application, reflected waves can compound on one another, adding undesirable signal level to the output and distorting the digitized signal. These reflections will degrade the SINAD and SFDR figures. In the case that the reflected wave is at the same frequency and phase as the incoming wave, a standing wave forms.

It was advantageous in the setup to place attenuator pads in between stages where reflections can degrade the output. Thus the mixer output, SAW input, and SAW output were all buffered by attenuator pads of 1dB to 5dB.

Freq (MHz)	S11 (dB)	S21 (dB)	S22 (dB)
65	-1.398	-58.811	-1.017
66	-2.784	-27.081	-1.299
67	-6.806	-11.631	-3.674
68	-10.530	-7.585	-7.310
69	-15.131	-7.002	-7.533
70	-16.826	-7.053	-8.945
71	-15.049	-7.036	-9.584
72	-8.065	-7.508	-8.192
73	-5.467	-13.597	-4.261

Table 4.1: SAWTEK 854660 S Parameters

[2]http://www.triquint.com/prodserv/types/filters/if/std_70mhz_family.cfm

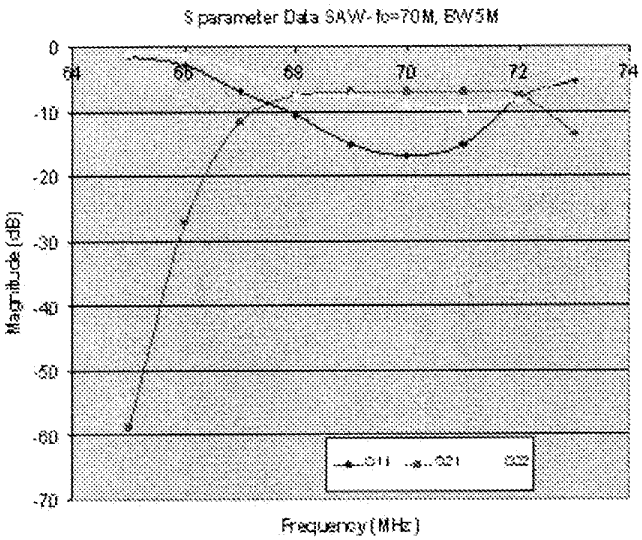


Figure 4-4: S parameter Data from SAW Filter Part 854660.

Freq (MHz)	S11 (dB)	S21 (dB)	S22 (dB)
60	-3.327	-15.791	-3.102
61	-3.728	-14.334	-3.363
62	-3.669	-14.176	-3.317
63	-3.614	-14.161	-3.323
64	-3.834	-14.237	-3.424
65	-4.095	-14.069	-3.625
66	-4.138	-14.040	-3.669
67	-3.945	-14.008	-3.581
68	-4.156	-13.991	-3.664
69	-4.302	-13.998	-3.834
70	-4.418	-14.061	-3.959
71	-4.112	-14.094	-3.757
72	-4.088	-14.051	-3.630
73	-4.428	-14.123	-3.863
74	-4.556	-14.052	-4.057
75	-4.268	-13.984	-3.796
76	-4.155	-14.040	-3.658
77	-4.256	-14.126	-3.710
78	-4.732	-13.837	-4.247
79	-4.570	-13.954	-4.181
80	-3.531	-16.773	-3.181

Table 4.2: SAWTEK 854670 S Parameters

4.4 Single Sideband v. Double Sideband

Mixers translate frequencies to signals at the sum and difference of the two input frequencies (IN and LO). One of these frequencies is the desired sideband, the other is the image sideband. In some cases the sidebands contain different information, but in most cases the desired and image sidebands represent identical information [17]. Thus only one band is necessary, and the signal is filtered as a single sideband (SSB). If both sidebands are needed, double sideband (DSB) filtering is necessary in the signal chain.

SSB and DSB offer different advantages. SSB filters are much more narrowband (they need only be half the bandwidth of a DSB filter) and can be more complex to design. SSB filters can be designed to filter out the mixer carrier frequency, making the system insensitive to LO feedthrough. As discovered in Chapter 4, the local oscillator feedthrough can be a limiting factor in system performance. Feedthrough contributes to a DC offset if the same clock source is used for sampling and upconversion. In DSB, the carrier frequency appears at the output so LO feedthrough becomes a factor. Mixer design, mainly port isolation and balanced network, is cru-

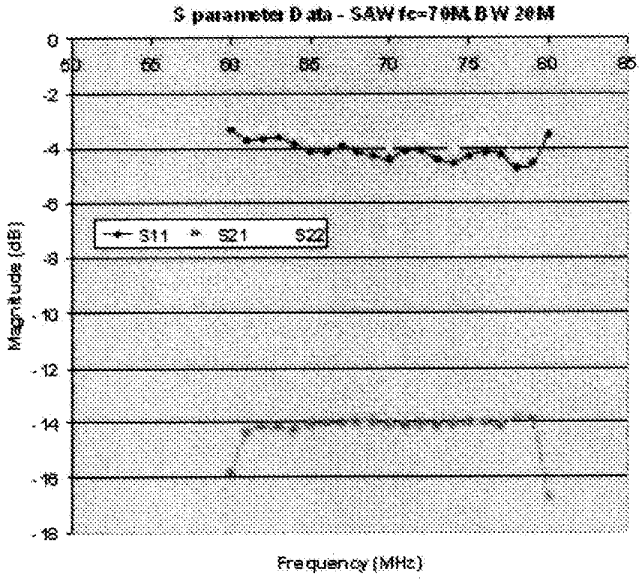


Figure 4-5: S parameter Data from SAW Filter Part 854670.

cial in DSB. Given the same input level in the system, the DSB setup should have a higher SNR and a better noise figure (NF). In DSB, there is twice as much signal, and a $\sqrt{2}$ increase in noise. Noise is measured in RMS and hence does not double like the signal level. A 2x increase is a 6dB gain and a $\sqrt{2}$ increase is a 3dB gain. Thus, the SNR increases by 3dB. With a higher SNR, the noise floor is lower and therefore the noise figure should improve with DSB. These metrics for dynamic performance will be presented in the following section and values for SSB and DSB will both be shown.

4.4.1 Phase Delay Offset

Another difference in SSB and DSB is how they are affected by a timing delay. In DSB, there are two sidebands to consider in the frequency spectrum, which means the time version of this is a signal (i.e. $\cos([\omega_i+\omega_c]t)$) that is modulated by the second (i.e. $\cos([\omega_i-\omega_c]t)$) frequency. Because of the modulation, phase delay becomes significant in sampling time. The system has two clocks traveling different signal path lengths the sampling clock directly to the ADC and the upconversion clock that has to travel the entire signal chain from mixer through amplifiers and filters all the way to the ADC input. Therefore it is important, when looking at double sideband, to ensure that the timing is such that the ADC clock is sampling at the peaks of the modulated analog input signal. Otherwise, it is possible to be sampling near the zero-crossing of the signal. The ADC would falsely output as a very low level signal even if the system is working properly, except for the timing of the clocks.

A SSB scenario has just one sideband, which is the transform of a sinusoid. When the signal is sampled, phase offset is trivial because the signal is not being modulated by another frequency[3].

Thus in the application setup, the length of the signal chain was adjusted so that proper DSB sampling could take place. This involved exchanging BNC cables of different lengths in the middle of the chain. Either the ADC sampling clock could

[3]This of course assumes that interfering signals are heavily attenuated in the signal, otherwise they are a source for modulation.

be delayed, or the signal chain can be lengthened so that the clock would sample at the next peak maxima. In a more realistic applications setting, this can be more of a nuisance than anything, so SSB may be heavily preferred over DSB. With SSB timing delay becomes a nonissue.

4.5 System Gain

Without variable components, the net system gain ranges from 15 to 23 dB. The measured gains of each component in the signal chain is listed in Table 4.3.

Part	Gain or Insertion Loss (dB)	Bandwidth
Input filters (TTE)	-3.4	Narrowband bandpass, input-frequency dependent
Butterworth Bandpass filter	-1.3	Fc=70MHz, BW=30MHz
SAW (1)	-7.25	Fc=70MHz, BW=5MHz
SAW (2)	-14.5	Fc=70MHz, BW=20MHz
AH31 (1)	+18.5	BW 44-90MHz
AH31 (2)	+19.1	BW 44-90MHz

Table 4.3: Gain and Bandwidth Values for Each Component

Throughout the system, the attenuator pads used to reduce reflections and standing waves, described in Section 4.3, sum to 6dB. Using the narrowband SAW(1) the system gain is 23dB. With the wideband SAW(2) the system gain is 15.8dB[4].

With the wideband 20MHz SAW filter care must be taken, as described in Section 4.1, not to just overdrive the system to achieve full scale. A step attenuator can be used to compensate for the 7dB difference in the insertion loss of the two SAW filters. From Section 4.4, the narrowband SAW(1) can be used for SSB filtering and the wider SAW(2) can be used for DSB filtering. To ensure consistency in testing, the same input level is configured for both tests. That level is set with the signal chain for DSB to achieve full scale output. Since the narrowband SAW(2) has a lower insertion loss,

[4]The gain of the system is defined from the filtered input, so the insertion loss of the filter is accounted for in the input level, not in the system gain. The filter is a test setup requirement, but in a real system, it is assumed that the input is well-filtered and a relatively clean signal.

a step attenuator can be used to lower the gain in the SSB chain to achieve full scale output while maintaining the same input power.

One thing to take note here is that adding PIN diodes in the system only decreases the system gain. They cannot increase the gain of the system because of the way they are implemented into the system design. PIN diodes are acting virtually as shunting resistors with increasing current bias. The maximum gain achievable for this upconversion scheme is with either no PIN diodes or reverse-biased PIN diodes.

Chapter 5

Dynamic Performance Results

The heart of this application is looking at the dynamic performance of the entire system. If the system can achieve high dynamic range without requiring the absolute top of the line components, this indicates the robustness of the application. The current application setup allows customers to determine the gain blocks of the system based on the components available at hand, the upconverting frequency, the sampling rate, and allows design room for sharp filtering for improved dynamic range. The dynamic figures of interest are Signal-to-Noise Ratio (SNR), Signal-to-Noise-and-Distortion Ratio (SINAD), Spurious-Free-Dynamic-Range (SFDR) of the entire signal chain (and ADC) as well as harmonic distortion, noise figure (NF), and output third-order intercept point (IP3).

5.1 SNR, SINAD, SFDR

The SNR of the system was generally found to be about 69-71dBFS. Different bandwidth SAW filters provided slightly varying figures, clearly the narrowband 5MHz SAW produced a higher SNR. Also, the SSB and DSB setup provided different SNR values, as anticipated in the discussion in Section 5.3. It was expected that the DSB SNR would be 3dB higher, it was found to be 1-2dB higher in most setups. Given the realistic setup on the lab bench, this is as expected. The dominant harmonics tend to be the second and third harmonics, but SINAD is typically about 62dBc and SFDR

63dBc. The system SNR comes close to the ADC LTC2249 SNR of 73dBFS, the upper limit of the expected system SNR. This suggests the method to be a low noise application, as observed with a 108dB noise floor with an 8192-point FFT. However, the SINAD and SFDR figures indicate that there is distortion in the system setup. The narrowband 5MHz SAW filter keeps higher order harmonics out, so the source of distortion lies in the components in the signal chain. Most likely the distortion arises from the mixer or amplifiers rather than the filters.

Tests were performed to look at the effects of the mixer distortion and amplifier distortion separately. In Figure 5-1 Test 1 has an IF input at 70MHz, processed through the signal chain and sampled by a 74MHz clock. Test 1 has a SNR of 69.2dBc and SINAD 67.2dBc at full scale output. Test 2 has a low frequency 4MHz input, mixed up to 74MHz, processed through the same signal chain and sampled by the same 74MHz clock. Test 2 has a SNR of 67.6dBc, and SINAD 64.8dBc.



Figure 5-1: System Distortion With and Without Mixer.
Test 1: IF input, without mixer. Test 2: LF input, with mixer.

Looking at this test, it was interesting to note that the mixer did not actually degrade the SNR or SINAD by more than a few dB. The mixer definitely contributes some noise and distortion into the signal chain, but does not seem to be the dominant factor. Therefore, the attention was shifted to the AH31 amplifiers.

If the AH31 amplifiers have poor distortion, the second AH31 which is right at the ADC input, will have the most pronounced effect at the output. The previous amplifier in the chain is followed by a narrowband SAW filter, which bandwidth limits the amplifier output.

In Figure 5-1 Test 1 has a filter in between the amplifier and ADC input network. If the order of the two parts were swapped, would the distortion change?

In Figure 5-2, a comparison was made between the order of a LC bandpass filter and AH31 amplifier in the input signal chain to the ADC. Test 1 with a cascade

of AH31-bandpass filter provides SNR = 70dBc and SINAD = 67dBc. Test 2 gives SNR=70dBc and SINAD=55dBc! Therefore, there is a large level of distortion of the AH31 when placed right before the ADC. The AH31 was designed for a bandwidth of 45MHz to 90MHz. This is greater than the Nyquist bandwidth of 35MHz, suggesting that the distortion folds back into the Nyquist zone.

The AH31 amplifiers were selected as off-the-shelf sufficient amplifiers. They are cheap and have fairly low distortion. From the two tests, it is simple to see that placing a filter after the AH31 and before the ADC will improve the SINAD and SFDR values. As long as the AH31 distortion does not affect the more realistic intermodulation test, these amplifiers are still useful components for this application.

5.1.1 SSB v. DSB

Let us compare now the difference between the figures for DSB and SSB. Comparing the two schemes is challenging, because it is hard to determine what the most equal test between the two is. The main difference in the DSB and SSB is the ease of filtering achievable. So most applications of DSB have a wider range filter than SSB. However that changes the signal gain of the post-mixer chain because the two options available are the 5MHz SAW (for SSB) and 20MHz SAW (for DSB). The other factor to consider when looking at SNR and SINAD values is the input power level. With DSB allowing both sidebands for twice the input level than in SSB, it is easy to overdrive the input in DSB. Setting the system up as described in Section 4.4 allows for a fair comparison of SSB and DSB filtering, with equal input levels an an attenuator to adjust post-mixer gain.

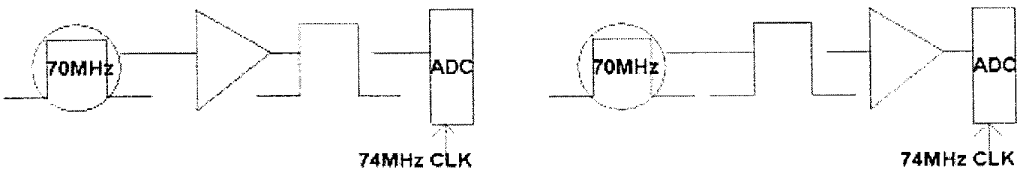


Figure 5-2: ADC Input Distortion. Having the amplifier output post-filtered improves the dynamic results.

The expected difference between SSB and DSB SNR is 3dB, as discussed previously. In the setups discussed, it was very hard to achieve a comparison where the DSB SNR is actually close to 3dB higher. The results of a DSB v. SSB test are depicted in Table 5.1:

Parameter	SSB	DSB
f_s	74MHz	70MHz
Input f	4MHz	4MHz
SAW, f_c=70MHz	5MHz BW	20MHz BW
SNR (with F1=-1dBFS)	66.7dBc	69.7dBc

Table 5.1: Double Side Band and Single Side Band Results.

5.1.2 PIN Diode Dynamic Performance

Now the attention focuses on the dynamic performance of the upconversion scheme with the PIN diodes. After all, the purpose of upconversion is to provide variable gain and filtering. It is important to measure the dynamic performance of the system with the PIN diodes in place.

With the same input level, the output amplitude dropped from full scale -1dBFS to -24dBFS at a 1V bias voltage on the PIN diodes (refer to Table 5.2). This verifies the amplitude has about 25dB gain range. The S11 parameter of the mixer with PIN diodes shows the effect of the varying output impedance matched to the 50Ω transmission line. The measurements were made with the network analyzer with 50Ω matching. In essence, the PIN diodes lower the 50Ω impedance, so that the attenuation observed at the output is due to impedance mismatch.

It is desirable to see that the SNR, SINAD, and SFDR values do not change considerably with the addition of the variable PIN diodes. In the shunt resistor configuration of the PIN diodes, it is possible that some distortion may arise. However, a comparison of SNR and SINAD values in a system with and without PIN diodes showed no change in SNR and less than 1dB change in SINAD, indicating that the distortion from PIN diodes is almost negligible.

In Ultrasound, it is possible that the gain must be adjusted depending on the input level to achieve full scale. Full scale output is desirable. To mimic the application, the PIN diodes were biased at 0.5V intervals across the gain range, and the input level was adjusted accordingly to achieve full scale at the ADC. The SFDR and SINAD values stayed consistent at 73dBFS. The SNR dropped 4dB when the PIN diode became forward biased.

5.2 Noise Figure (NF)

To validate this application of frequency translation, it is important to verify that the noise figure is acceptable. Because a mixer (which usually has a relatively poor noise figure) is in the system chain, the noise figure is not expected to be as good as a single chip VGA. Two methods of noise figure calculations were done, first with Friss' equation and second with the SNR and Gain calculation.

We are looking at noise figure, seen at the input of the system. A cascade system has an overall noise figure determined by the equation :

$$NF = F1 + \sum_{i \neq 1} \frac{F_i - 1}{\prod_{j<i} G_j}, \ where \tag{5.1}$$

F1 = First stage noise figure,

$F_i = i^{th}$ stage noise figure, and $G_j = j^{th}$ stage noise figure.

V_{bias}V	Attenuation (dB)	Return Loss S11 (dB)
5.0	-1	-18.2
4.5	-1	-13.4
4.0	-1	-2.77
3.5	-1.2	-1.83
3.0	-11	-1.41
2.5	-18	-1.30
2.0	-21.3	-1.17
1.5	-23.2	negl.
1.0	-24.47	negl.

Table 5.2: PIN Diode Attenuation and Return Loss.

As seen in Equation 5.1 the first component in the system contributes the most to the noise figure when we assume the system provides overall gain not attenuation. Here, the first component, the mixer, with the worst noise figure is expected to degrade the noise figure the most.

The table shows the noise figures and gains of each component in the system, as specified by their datasheets.

Stage	Gain (dB)	Noise (dB)
Mixer LT5521	-0.5	12.5
Bandpass Filter	-1.3	1.3
Amplifier AH31	+18.5	2.4
Amplifier AH31	+19.1	2.4
SAW filter, 5MHz	-7.5	Negligible
SAW filter, 20MHz	-14.5	Negligible

Table 5.3: Individual Stage Gain and Noise Figures.

Single sideband setup gives NF=13.02 dBFS. Double sideband setup gives NF=13.34dBFS. The difference arises from using different SAW filters for SSB And DSB.

From PScope, the noise figure can be extracted from the gain and SNR values. The relationship is shown in Figure 5-3.

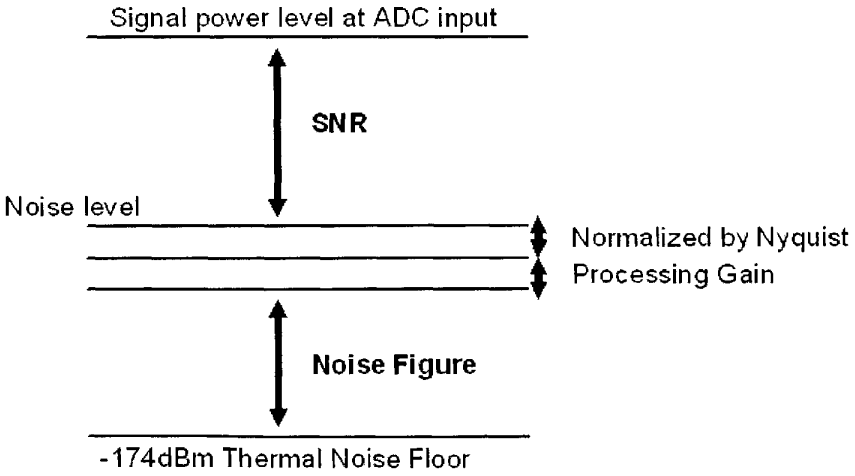


Figure 5-3: Noise Figure.

The equation is as such for a system with filter bandwidth $B < \frac{f_s}{2}$ (Nyquist):

$$NF_{out}(dB) = S_{out} - SNR - NTH - 10\log\frac{f_s}{2} - 10\log\frac{\frac{f_s}{2}}{BW} \quad (5.2)$$

$$NF_{in}(dB) = NF_{out} - Gain. \quad (5.3)$$

S_{out} = signal power level.

NTH = Thermal noise floor.

Processing Gain is $10\log\frac{\frac{f_s}{2}}{BW}$.

Nyquist Normalization is $10\log\frac{f_s}{2}$.

Essentially, the noise floor of the system is calculated, given the SNR and the output signal level. The normalization to Nyquist limits the spectrum to the Nyquist zone, or $\frac{f_s}{2}$. The processing gain scales the noise figure to the bandwidth of interest by further limiting the system to the input bandwidth, when it is less than Nyquist. In a system where the signal is bandlimited to be within Nyquist but has no additional filtering, the processing gain term is not needed. Then the difference between the noise level and the ideal -174dBm noise floor derived from ktB is the calculated noise figure of the system.

For single sideband 4MHz input upconverted to and sampled at 74MHz, the SNR was calculated to be 70dBFS, with a gain of 15. The ADC input was measured at 9.4dBm (ideally 10dBm, but slight loss to input transformer network). The noise figure at the output was 29dB, at the input (NF_{out} - Gain) was 14dB. This is comparable to the 13dB found by the cascaded gain system. The system used the 5MHz bandwidth SAW to allow for single sideband filtering, and thus the processing gain was $10\log\frac{\frac{74M}{2}}{5M}$.

5.2.1 Sources of Noise

From the equation, it is easy to see that the first component, the mixer, should be the dominant factor in the noise figure calculations. To verify whether or not this is true in the system, the mixer was replaced by a signal-generator IF frequency signal (at

the upconverted frequency). To minimize noise from the generator, a step attenuator was used, followed by a narrowband filter to block harmonics. The SNR increased by 5dB, therefore the noise figure improved by 5dB. In the Friss equation with the mixer taken out of the signal chain, the noise figure drops to 6.4dB in a single sideband system (including a -6dB loss from the step attenuator). It is important to note that the mixer plays a significant role in degrading the noise figure of the overall system. Although the amplifiers contribute noise to the system, they are very far down the signal chain. Looking at the equation, the noise figure of each component is divided by the preceding gain. Hence the overall input-referred noise figure is dominated by the mixer.

5.3 Intermodulation Test (IMD)

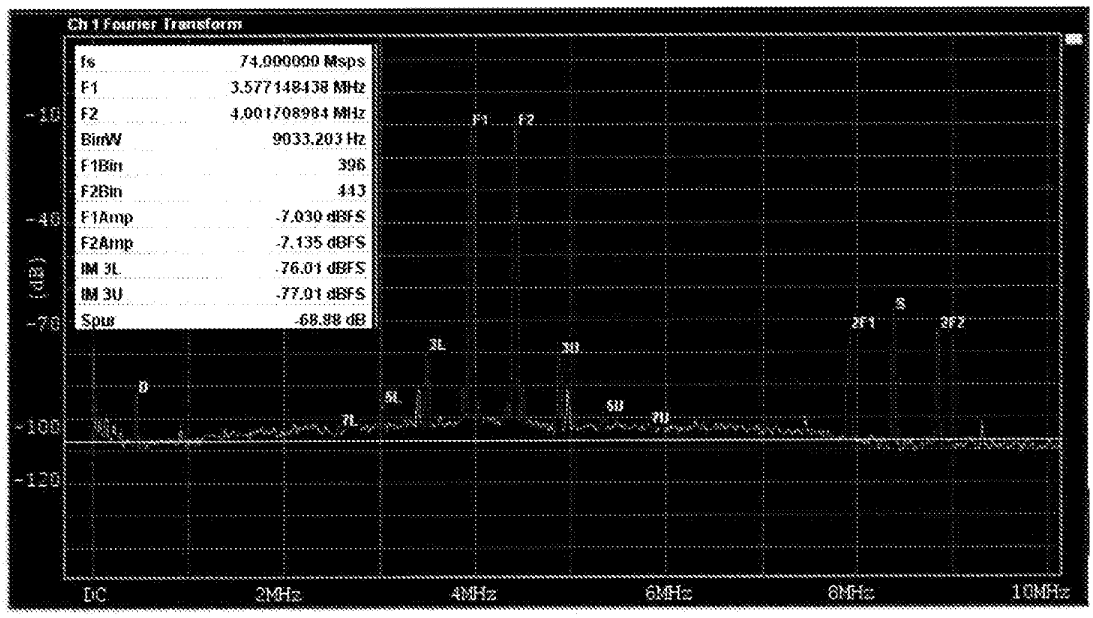


Figure 5-4: Intermodulation Test
Input signals $f_{in1} = 3.58MHz$ *and* $f_{in2} = 4MHz$, Sampling frequency 74MHz.

One of the more realistic methods of characterizing the system is to perform an intermodulation distortion test (IMD). By combining two close-in-frequency signals at the input of the system, this test shows how good the system is at rejecting interfering

signals. This measurement is extremely important in the case of ultrasound, because interfering signals arise close in frequency to the signal and require a high dynamic performing system to process the signal accurately. With a 3.58MHz and 4MHz signal in the ultrasound range, mixed up by a 74MHz clock and sampled with the same clock, 77dB was achieved for attenuation of the third order intermod signal, results in Figure 5-4. The third order IMD is a convenient measurement because it requires just two test signals, and can be set up so that the third order products are within the passband.

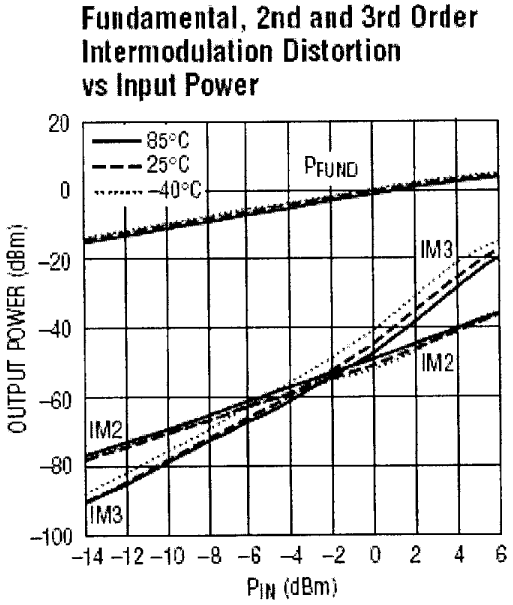


Figure 5-5: LT5521 Mixer Linearity. From Datasheet.

For linearity of the system, it is important to look at how the output fundamental and third order products change in response to input power levels. The LT5521 mixer has high linearity, given by Figure 5-5. The third order IMD gives the hypothetical OIP3 (output third order intercept point) of the system. This value gives the output power at which the third intermod signal equals the fundamental signal level. For every dB change in the fundamental, the third IMD changes by 3dB. It is hypothetical because the system would be saturated before the OIP3 point can be reached. Sweeping the input power of the system (both input signal levels were

stepped synchronously), the output F1 and IM3 amplitudes were plotted in Figure 5-6. Here, the linear portions of the plots were fitted to a line and the intersection of the two extrapolated lines gives the OIP3 point. In this test, OIP3 was found to be 44.2dBFS.

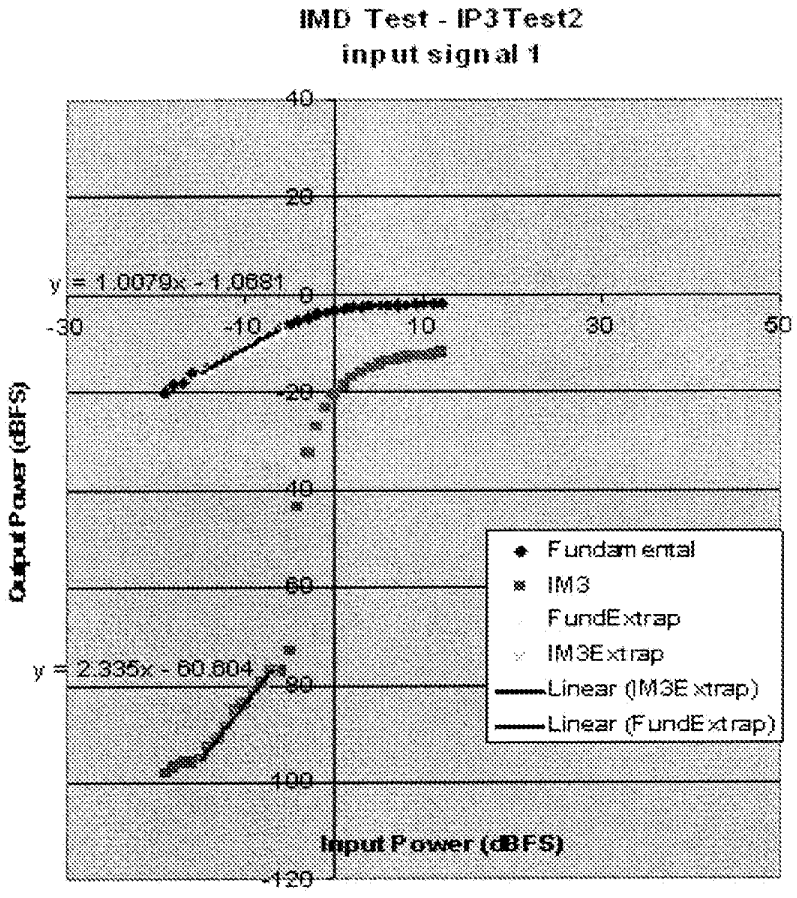


Figure 5-6: IP3 Extrapolation from Intermodulation Test.

Where is the IMD coming from?

The IMD test is performed routinely on mixers, so the LT5521 datasheet specs for +24dBFS IP3 point. This is of course, under a specific set of test parameters, but this value was used as the basic benchmark value. With a gain of 20dB post-mixer, the IP3 level is 44dBFS, which matches the extrapolated OIP3 value.

If the IP3 point and the intermodulation distortion is truly limited by the mixer, then a measurement of the IP3 of the system without the mixer would indicate such.

As in the single tone distortion test, the mixer was taken out of the equation. Two helically-filtered signals (from the signal generator) at 71MHz and 72MHz were inputs to the pre-ADC IF signal chain. The IMD test was carried out with these input signals. The results of this test showed slight improvement in IM3 values (77-80dBFS) and an IP3 improvement to 48dB. This seems to indciate that the mixer degrades the IP3 by 3dB.

However, it is highly possible that the IP3 improvement was masked by the IP3 value of the AH31 amplifier at the end of the signal chain (before the ADC). The typical datasheet OIP3 value for the AH31 is +42dBm, measured with two tones at 10dBm output power separated by 1MHz [9]. The measurements taken are already slightly higher than the typical value for the AH31. Because of the +20dB gain following the mixer, it is possible that the IP3 value of 48dB without the mixer does not really show how much the mixer actually degrades the IP3 value. In this application, it seems that the amplifier is partially responsible for limiting the IP3 value of the system. Fortunately, the system has good intermodulation distortion and attenuation of intermod products. The mixer and the amplifier both contribute to IP3 and intermod products, but the overall application is sufficient for ultrasound requirements.

Chapter 6

Conclusion

6.1 Summary

After a careful analysis of the frequency translation system designed for continuously variable gain and filtering, the performance was found to be desirable and definitely a possibility for the future of high-end ultrasound applications. With a continuous gain range up to 25dB and a 25MHz range of filtering capabilities, the upconversion scheme is palatable for ultrasound. This application is fairly straightforward to put together, and results of over 70dBFS SNR, more than 75dBFS IM3, and 44dB IP3 were achieved.

6.2 Future Work

The integration of the upconversion scheme into a working ultrasound application is challenging as is. However extensions of this thesis work can incorporate more design considerations into the application system. The following highlights possible future work.

There is no limitation in terms of sample rate and clock speed. It is possible to upconvert to a frequency higher than 70MHz, and continue sampling with the same clock source. The upper limit lies in the ADCs, with Linear's parts sampling at or more than 250MSPS.

One of the performance-limiting parts was the LT5521 mixer. Although a great part at high frequencies, it has drawbacks at 70MHz. Naturally, upconversion to higher frequencies can improve the mixer noise and distortion performance. If 70MHz is the desired translation frequency, it is possible to redesign the Gilbert-cell based mixer to improve its dynamic performance.

PIN diodes provide more than 25dB attenuation range across a bias voltage of 5V. However, the gain drops in a third-order polynomial form. It is possible to program the system to provide linear-in-dB gain control using PIN diodes to improve the user interface with the system.

There is also the option of making a module for this product. The idea of making a module out of this entire application system was discussed extensively throughout my thesis work. There are advantages and disadvantages to doing it. In the setup I have configured for my thesis work, there is sensitivity to noise and oscillation. Laying it out on a board or module will eliminate much of the ancilliary issues. However, it is important to consider the time and cost of such a project. The intended market, primarily the high-end ultrasound consumers, may not include the rapidly expanding medical ultrasound industry. In this case, it may not be economically viable to invest resources for fabricating the module. Additional market research should be done to better understand the demand for such integrated boards and/or modules for the upconversion scheme.

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Exhibit 1005

U.S. Patent No. 8,224,274 to Ramon Gomez et al.

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(12) **United States Patent**
Gomez et al.

(10) **Patent No.: US 8,224,274 B2**
(45) **Date of Patent: Jul. 17, 2012**

(54) **SCALABLE ARCHITECTURE FOR SATELLITE CHANNEL SWITCH**

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(73) Assignee: **Broadcom Corporation**, Irvine, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 627 days.

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(22) Filed: **Dec. 17, 2008**

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Related U.S. Application Data

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(51) **Int. Cl.**
H03M 1/12 (2006.01)

(52) **U.S. Cl.** **455/179.1**; 341/155

(58) **Field of Classification Search** 455/179.1, 455/130, 188.1, 139; 341/144, 155
See application file for complete search history.

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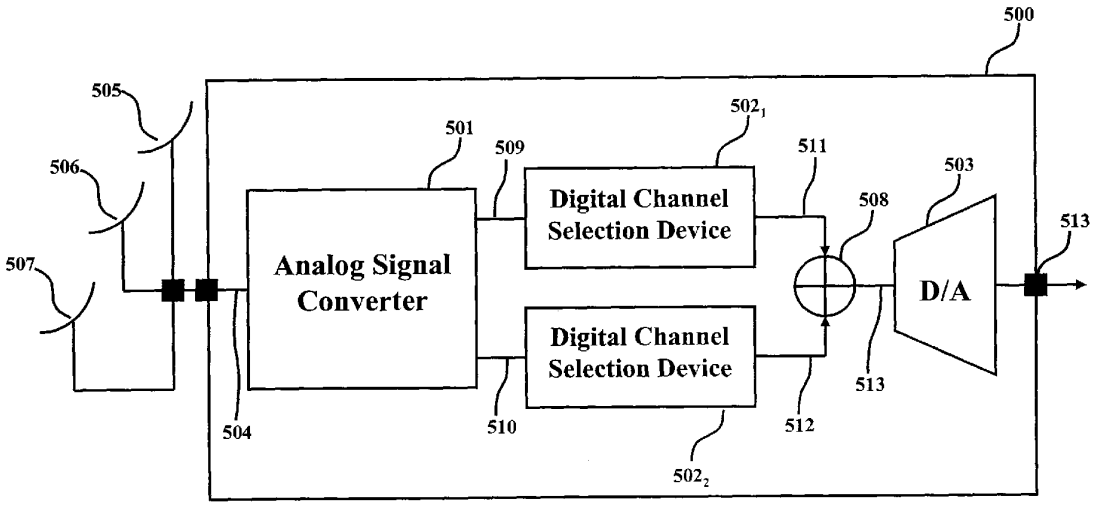
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Primary Examiner — Peguy Jean Pierre
(74) *Attorney, Agent, or Firm* — Sterne, Kessler, Goldstein & Fox P.L.L.C.

(57) **ABSTRACT**

A frequency translation module for a broadband multi-channel communication system may include an analog signal converter, a digital channel selection device, and a digital-to-analog (D/A) converter. The analog signal converter is configured to receive a plurality of analog signals, to select analog signals residing in a predefined frequency band, and to convert each of the selected analog signals into a digital signal. The digital channel selection device is configured to process digital signals corresponding to the selected analog signals and to generate a composite output of digital signals representative of the selected analog signals. The D/A converter is configured to translate the composite output to an analog signal output decodable by a receiver. Further, the frequency translation module may include a mixer configured to upconvert the analog signal output to a frequency decodable by the receiver.

22 Claims, 17 Drawing Sheets



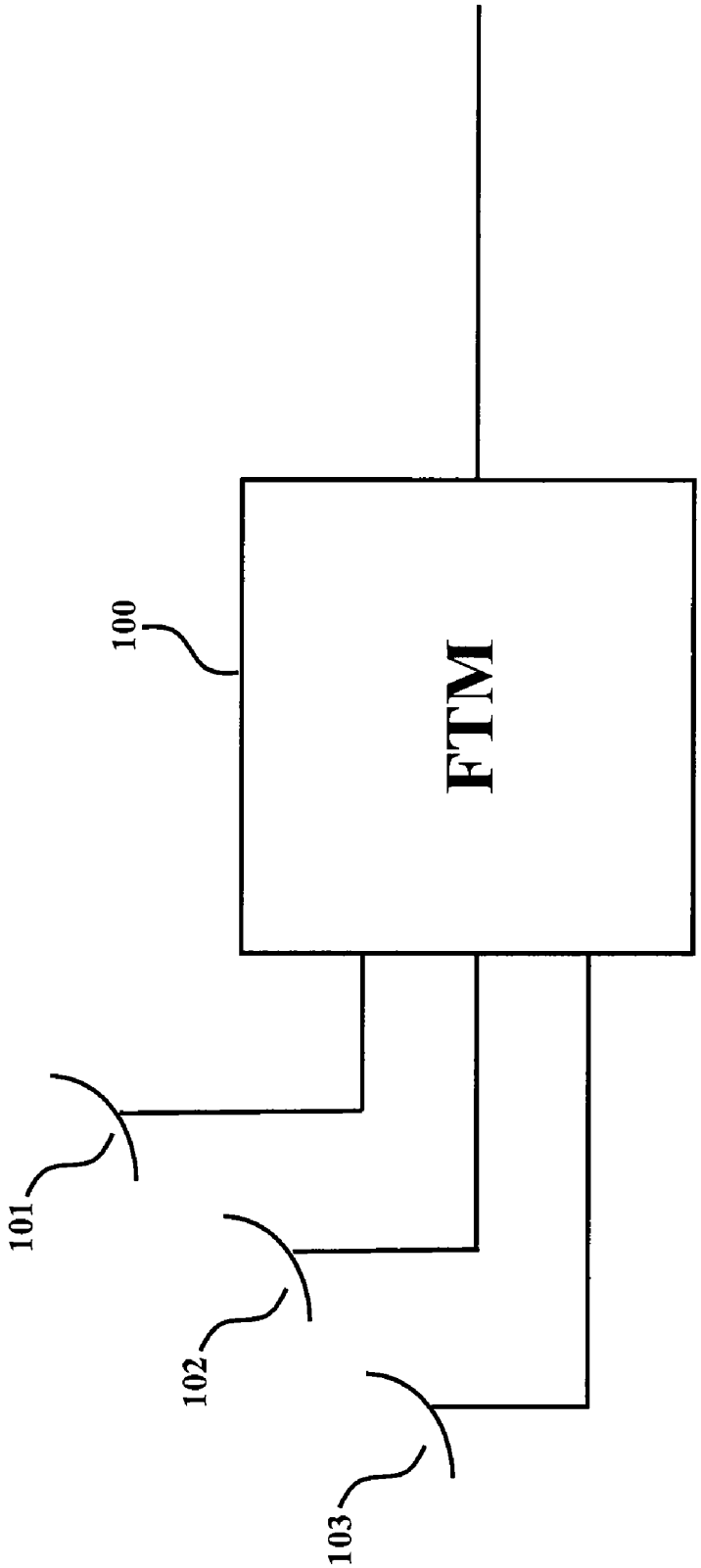


Figure 1

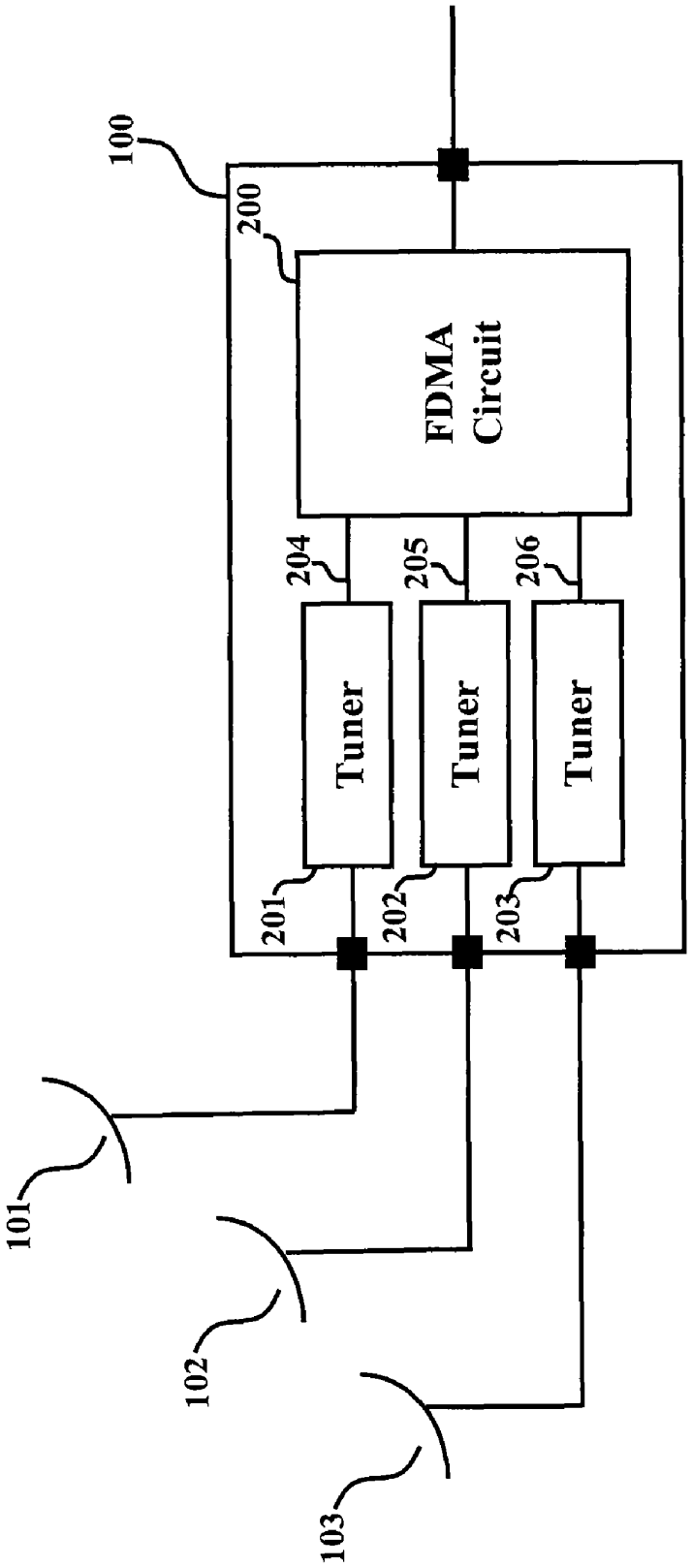

100
200
FDMA Circuit
204
205
206
Tuner
Tuner
Tuner
201
202
203
101
102
103

Figure 2

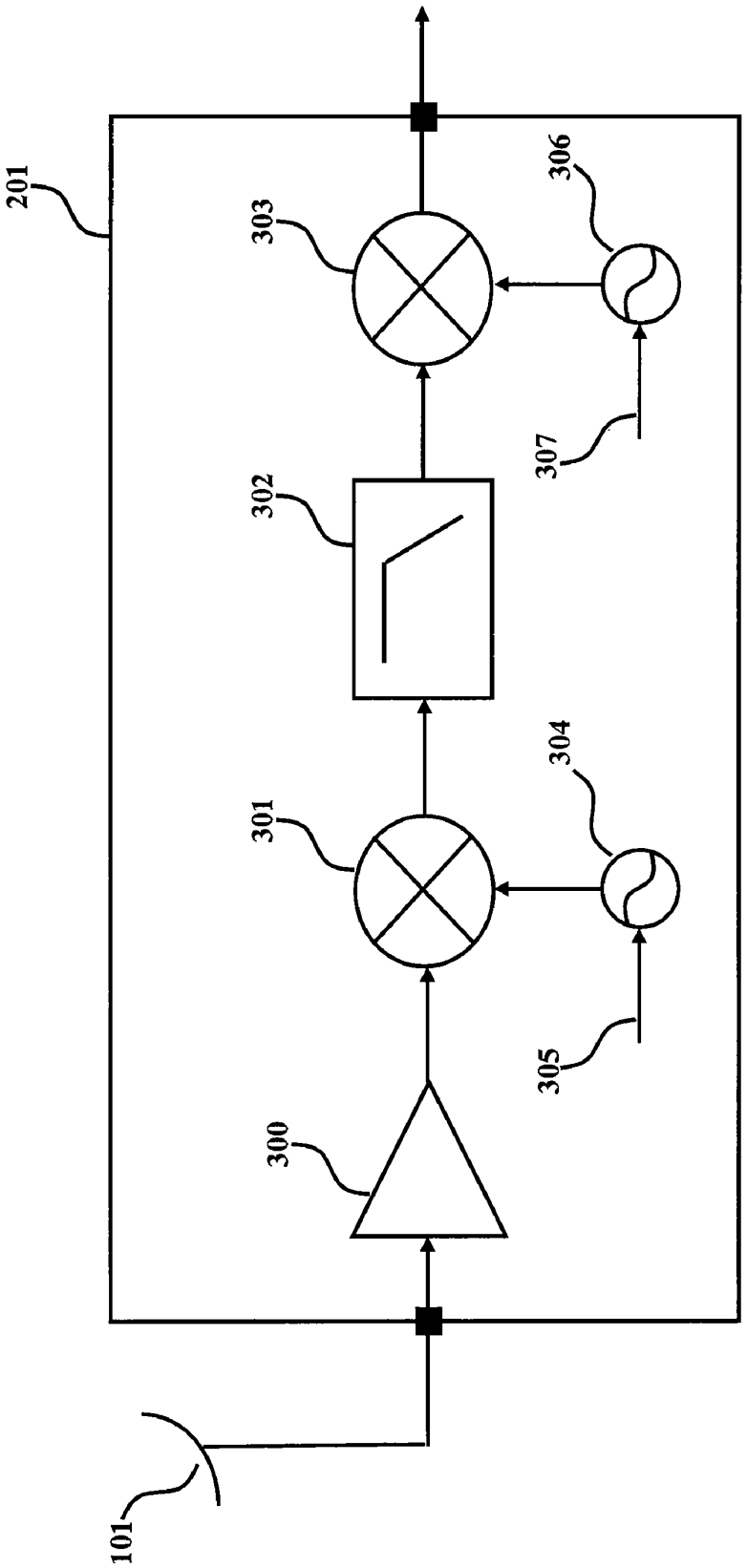


Figure 3

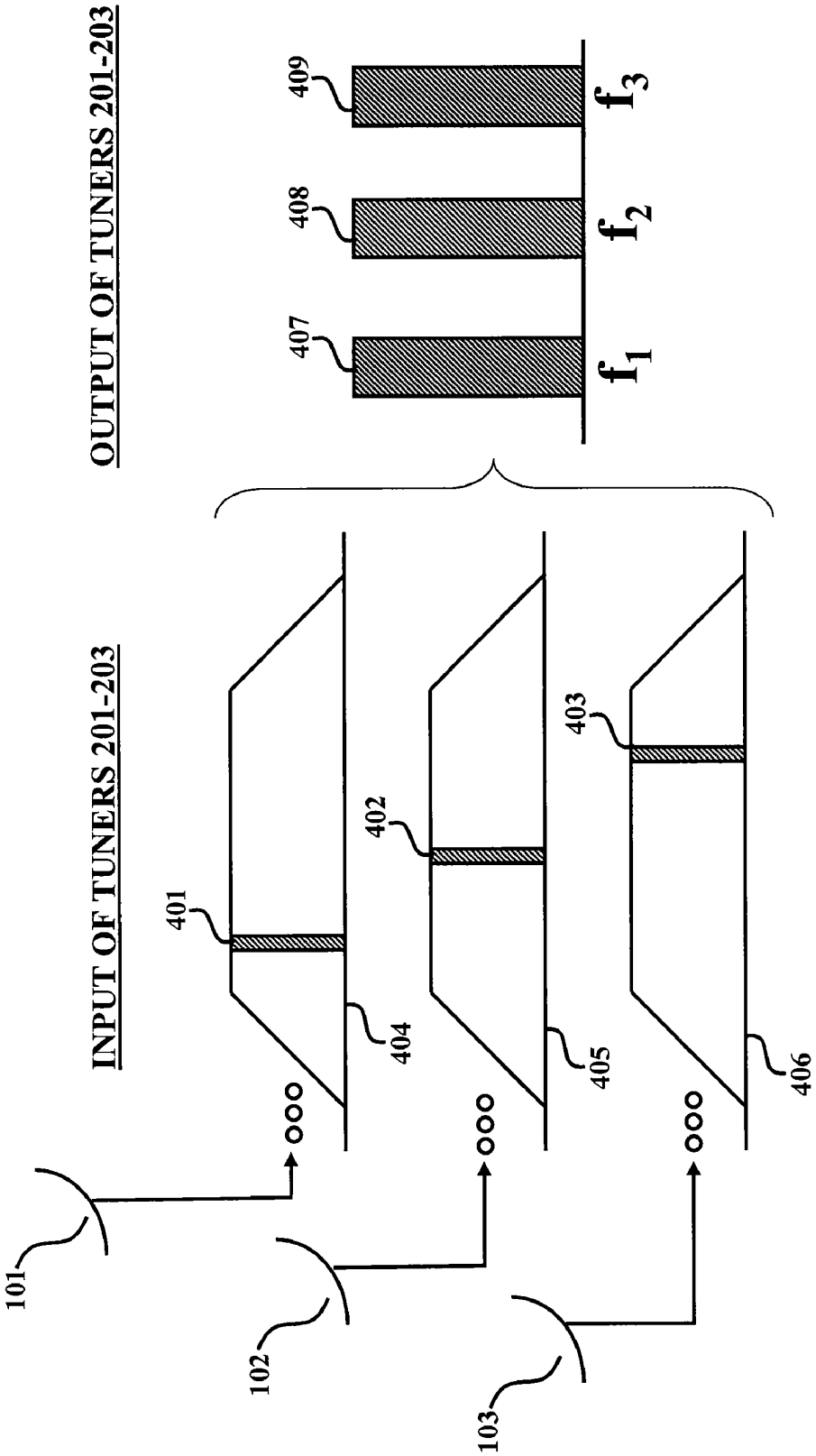

OUTPUT OF TUNERS 201-203
INPUT OF TUNERS 201-203
409
408
407
f_3
f_2
f_1
401
402
403
404
405
406
101
102
103

Figure 4

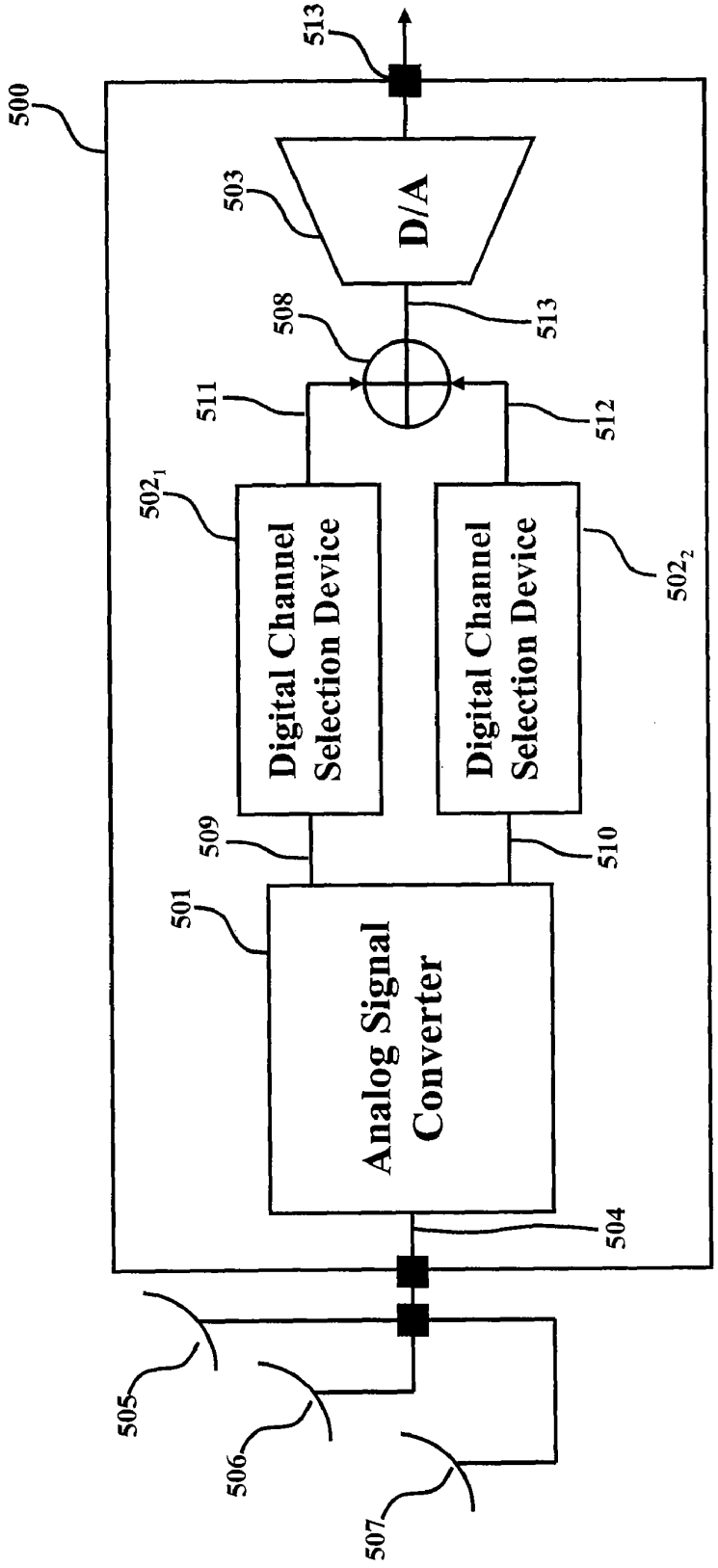

500
513
503
D/A
508
513
511
512
502_1
Digital Channel Selection Device
Digital Channel Selection Device
502_2
509
510
501
Analog Signal Converter
504
505
506
507

Figure 5

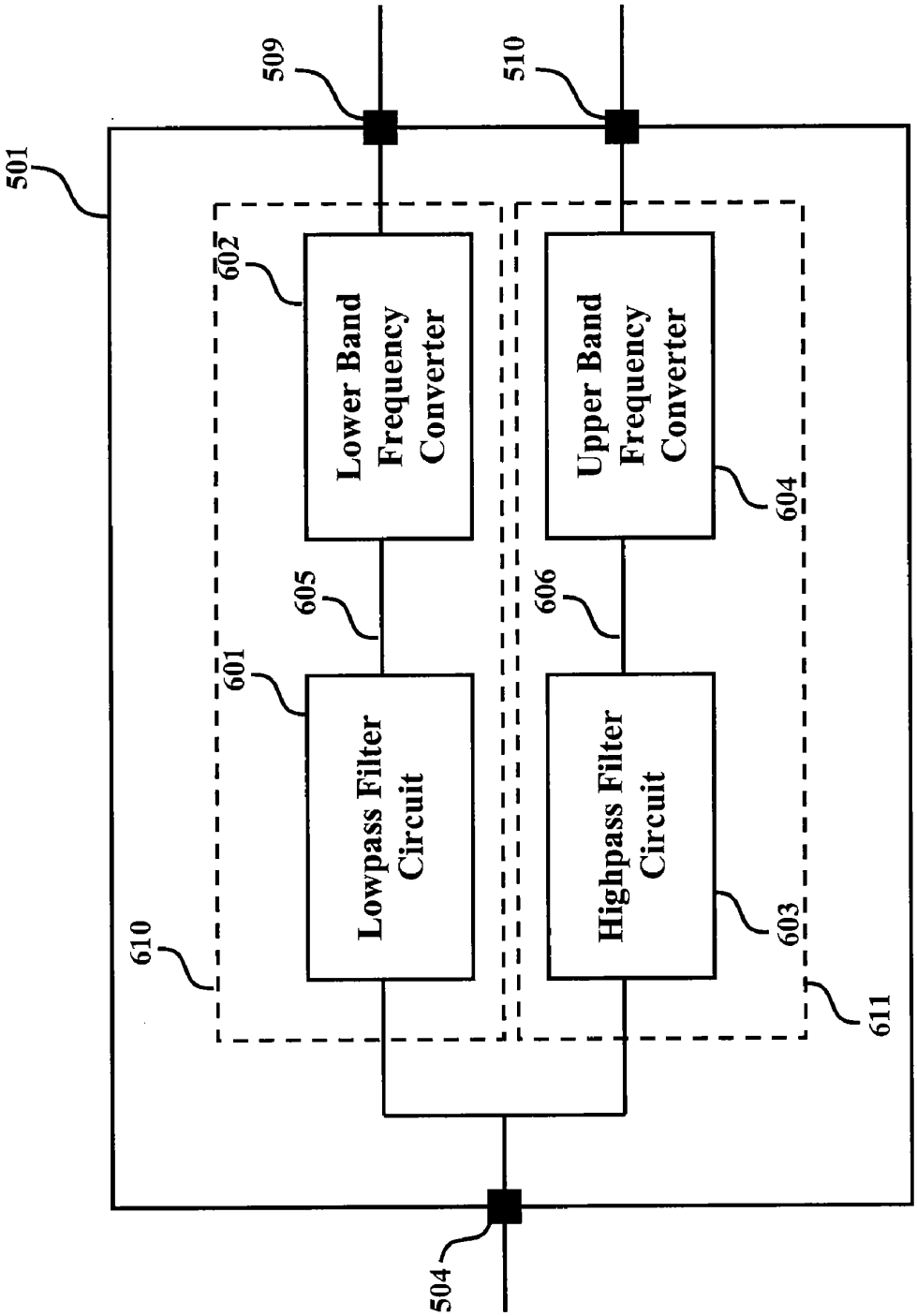

509
510
501
602
Lower Band Frequency Converter
Upper Band Frequency Converter
604
605
606
601
Lowpass Filter Circuit
Highpass Filter Circuit
603
610
611
504

Figure 6

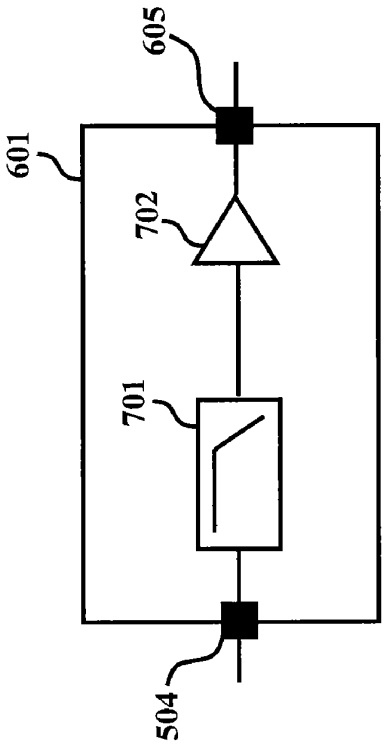


Figure 7

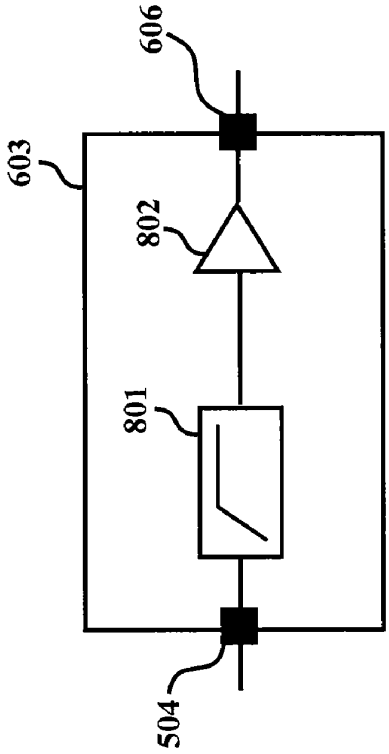


Figure 8

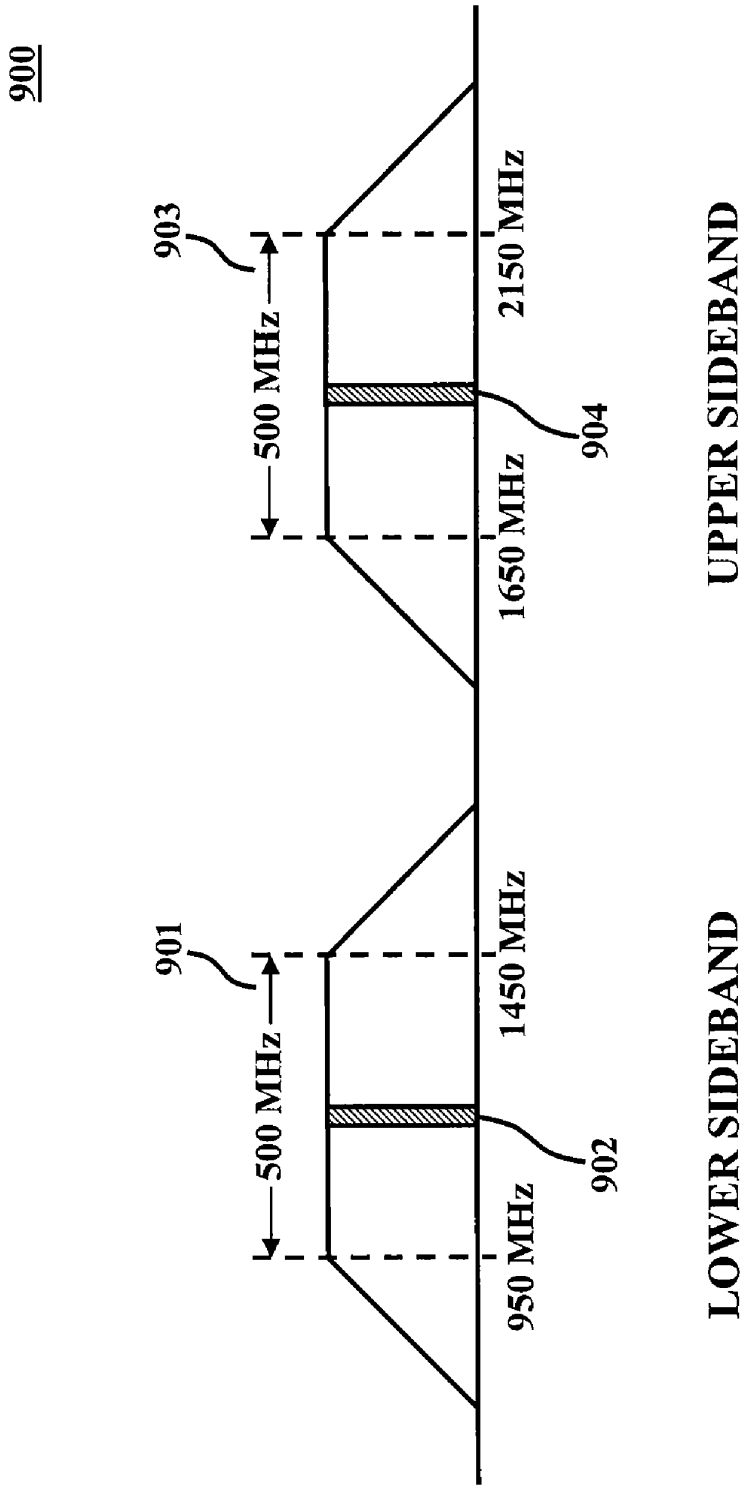

900
903
500 MHz
2150 MHz
904
1650 MHz
UPPER SIDEBAND
901
500 MHz
1450 MHz
902
950 MHz
LOWER SIDEBAND

Figure 9

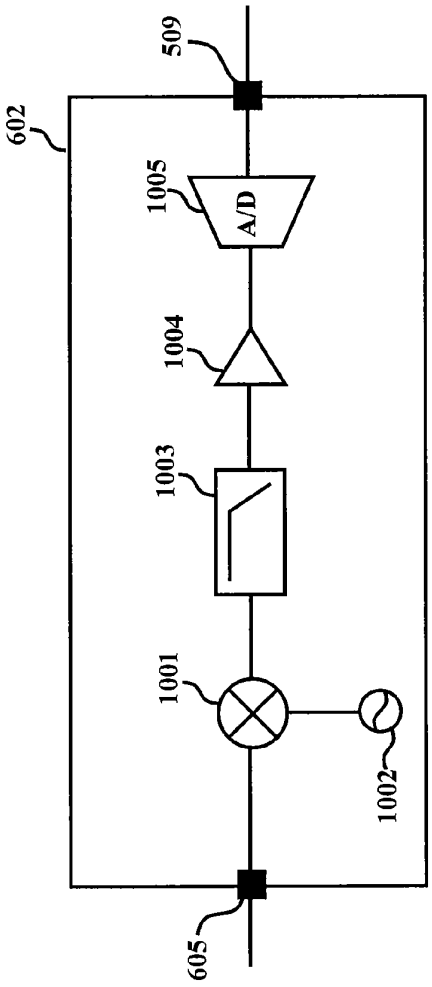


Figure 10

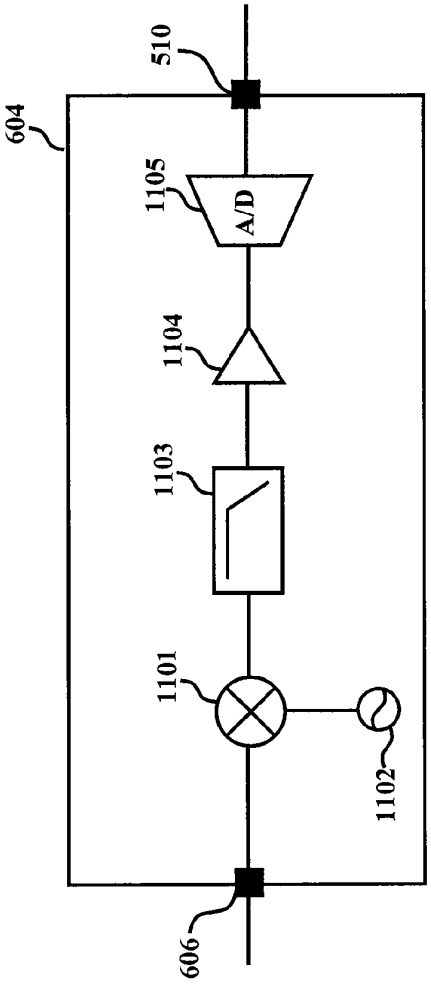


Figure 11

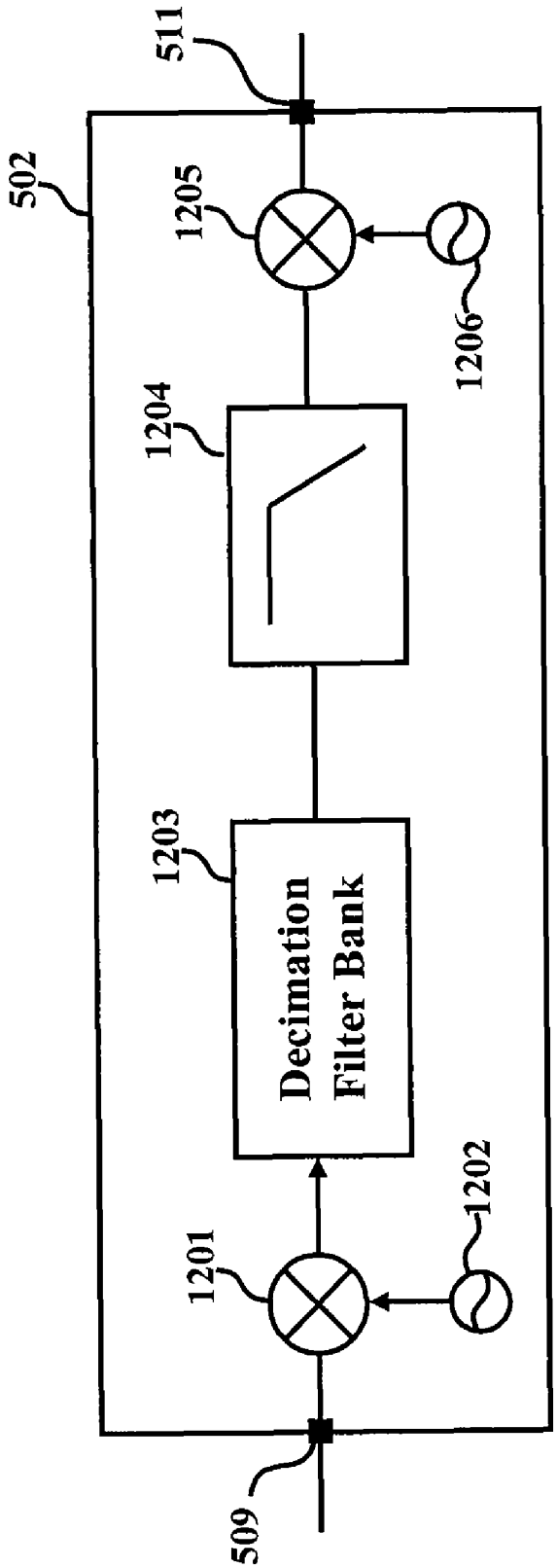

511
502
1205
1206
1204
1203
Decimation
Filter Bank
1202
1201
509

Figure 12

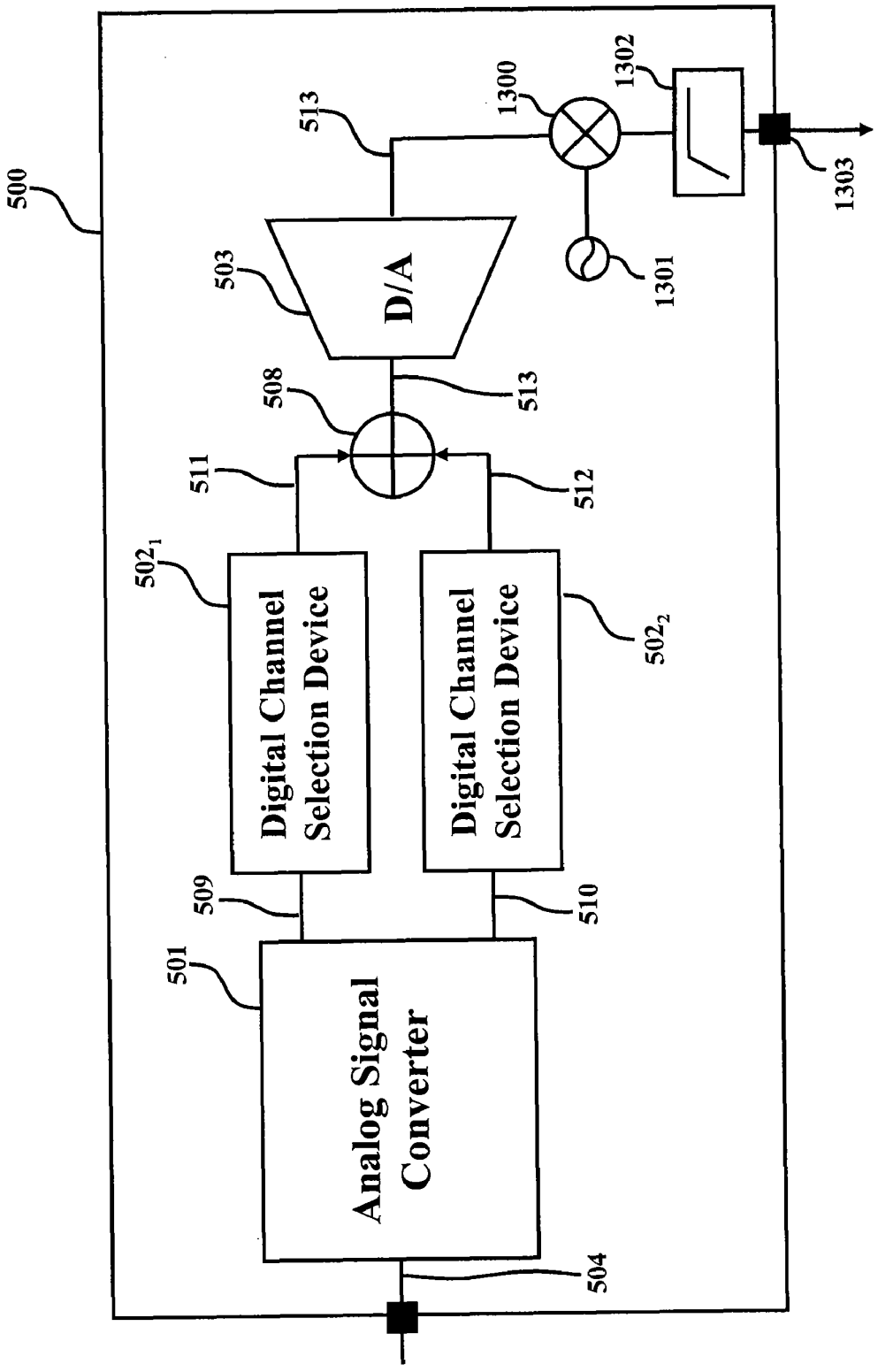

500
513
1300
1302
1303
1301
503
D/A
508
513
511
512
502_1
Digital Channel Selection Device
502_2
Digital Channel Selection Device
509
510
501
Analog Signal Converter
504

Figure 13

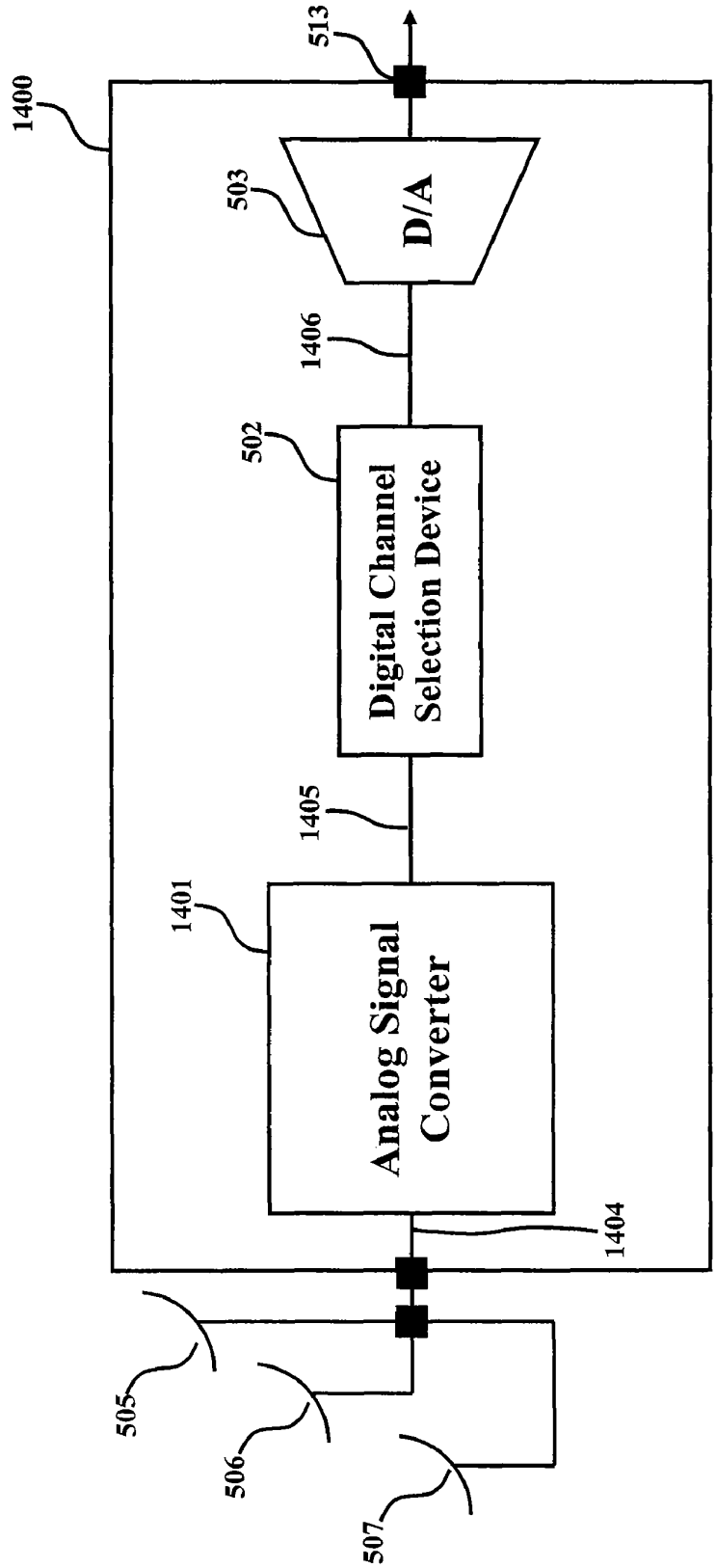

1400
513
503
D/A
1406
502
Digital Channel Selection Device
1405
1401
Analog Signal Converter
1404
505
506
507

Figure 14

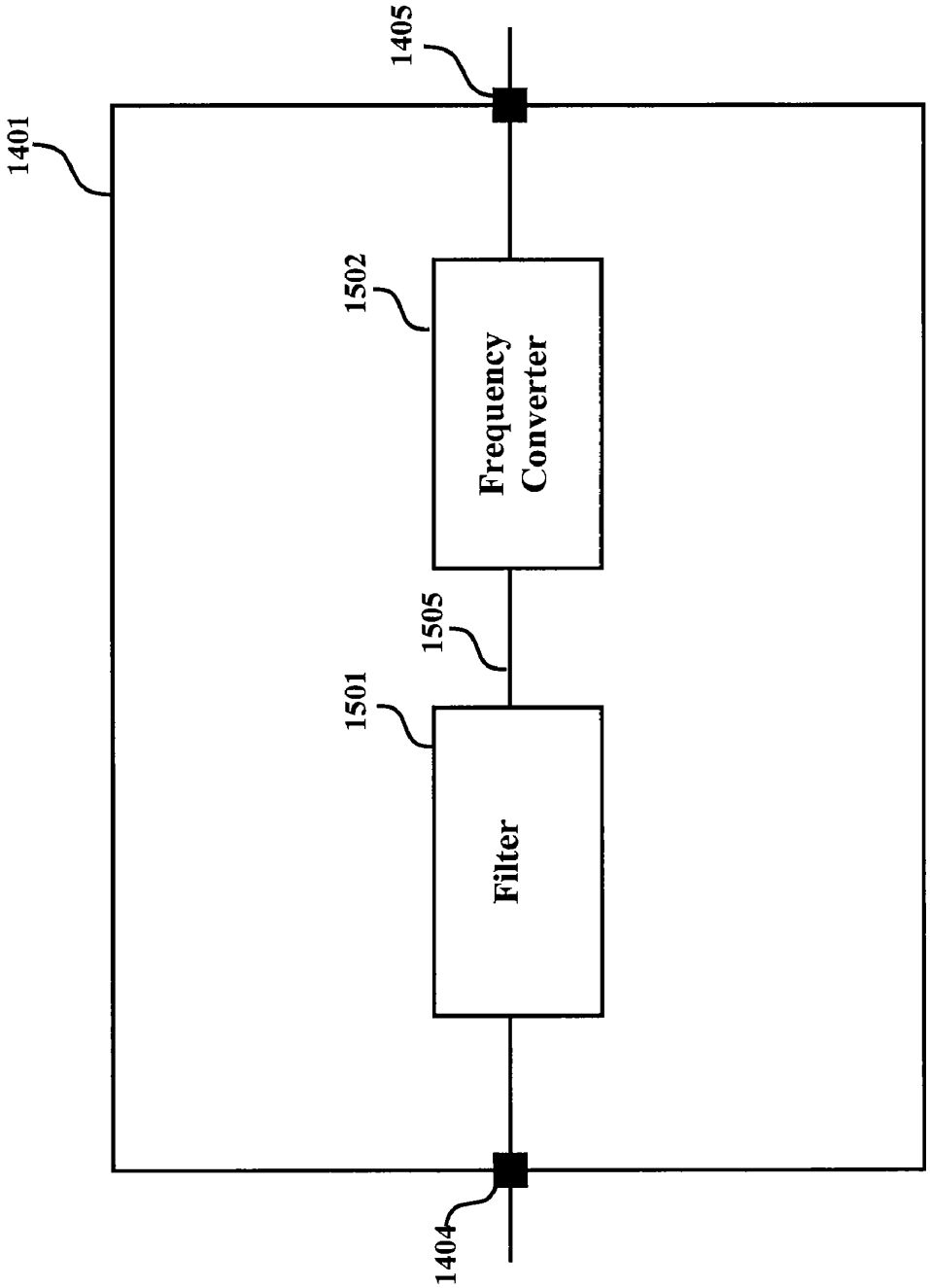


Figure 15

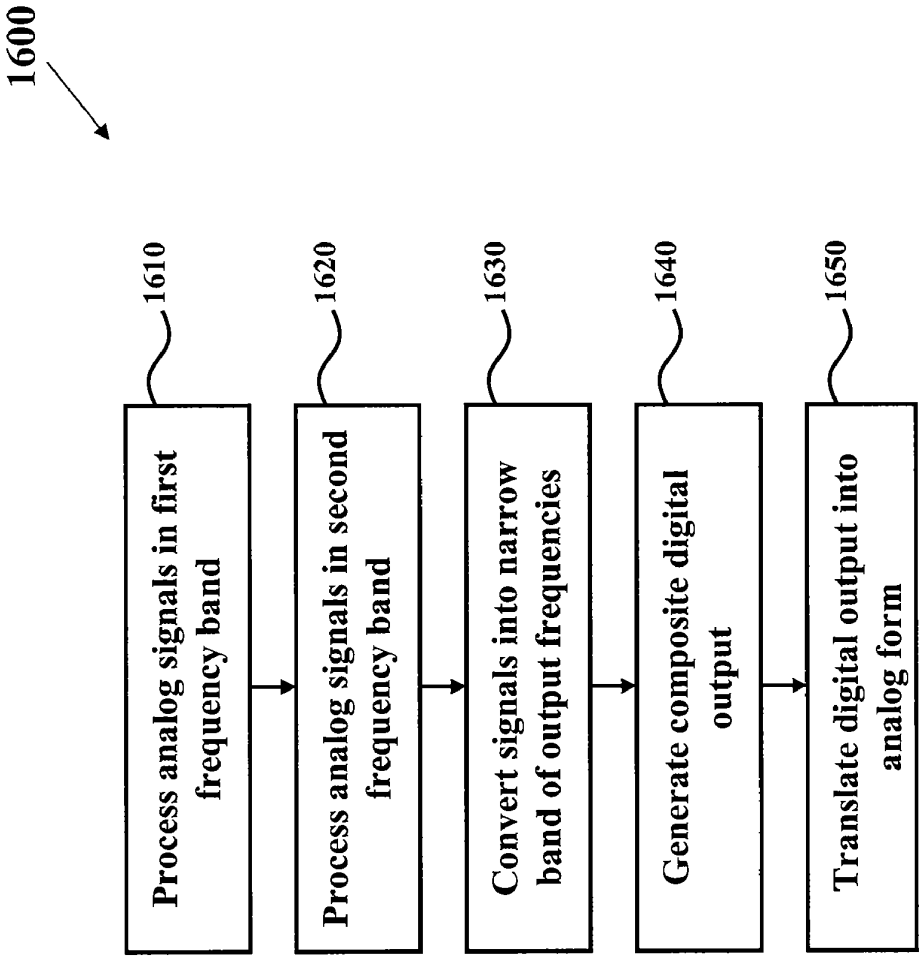

1600
1610
Process analog signals in first frequency band
1620
Process analog signals in second frequency band
1630
Convert signals into narrow band of output frequencies
1640
Generate composite digital output
1650
Translate digital output into analog form

Figure 16

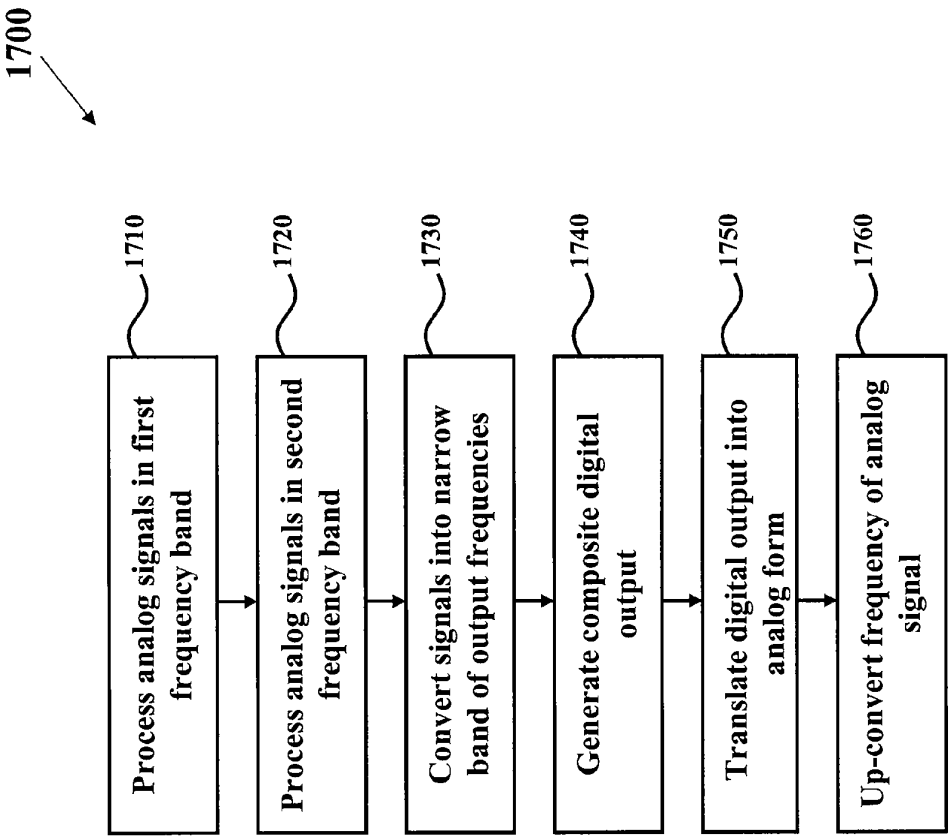

1700
1710
Process analog signals in first frequency band
1720
Process analog signals in second frequency band
1730
Convert signals into narrow band of output frequencies
1740
Generate composite digital output
1750
Translate digital output into analog form
1760
Up-convert frequency of analog signal

Figure 17

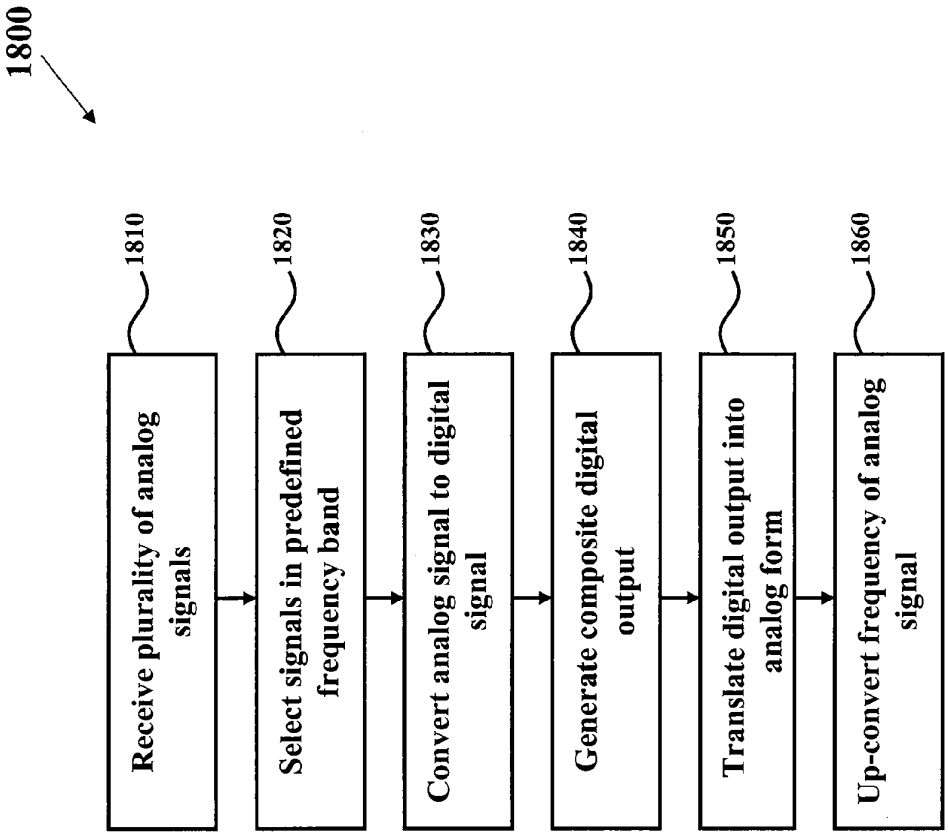

1800
1810
Receive plurality of analog signals
1820
Select signals in predefined frequency band
1830
Convert analog signal to digital signal
1840
Generate composite digital output
1850
Translate digital output into analog form
1860
Up-convert frequency of analog signal

Figure 18

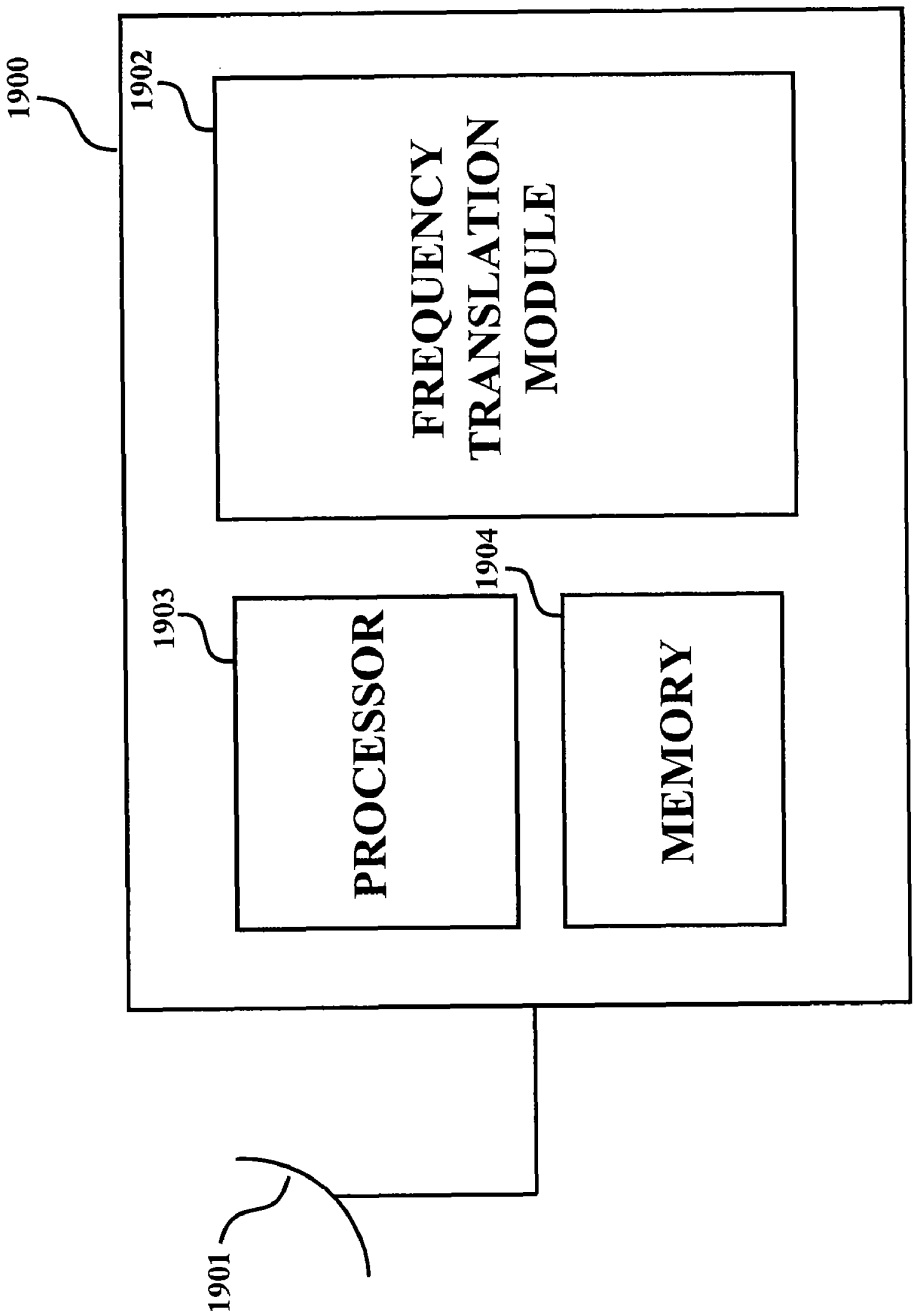

1900
1902
FREQUENCY TRANSLATION MODULE
1903
PROCESSOR
1904
MEMORY
1901

Figure 19

SCALABLE ARCHITECTURE FOR SATELLITE CHANNEL SWITCH

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application No. 61/006,186 (BP 6605; SKGF Ref. No. 2875.1940000), filed Dec. 28, 2007, titled "Scalable Architecture for Satellite Channel Switch," which is incorporated herein by reference in its entirety.

BACKGROUND

1. Field

The present invention generally relates to the field of channel switches in a multi-channel communication system. More specifically, the present invention relates to processing one or more input channels to a frequency translation module through a scalable switch architecture.

2. Background

A growing portion of television programming is broadcast directly to home receivers via satellite. Satellite television provides a wide array of programming and is broadcasted from various orbital positions in space. Satellite antennas receive signals from these specific orbital locations. Integrated receiver decoders (IRD) decode the signals received by the antenna signals and pass them to a television for viewing. Oftentimes, households subscribe to additional satellite programs, such as high-definition and specialized programming, where multiple antennas may be required to receive broadcasts from satellites in different orbital locations. The broadcast signal from each satellite may contain a number of distinct bands based on, for example, frequency and polarization. Alternatively, a single antenna (e.g., satellite dish) may be used to receive broadcast signals from the different satellites.

A frequency translation module (FTM) enables a user to selectively switch the signals received from each satellite antenna and deliver these signals to an IRD located within a household. Conventional FTMs contain one or more tuners, where each tuner is coupled to one satellite antenna. The tuner selects and down-converts a desired channel from the satellite signal to an intermediate frequency (IF) signal or a baseband signal, which is suitable for processing and display on a television or computer monitor.

Conventional approaches to the design of tuners employ analog components, such as fixed-frequency filters, mixers, and local oscillators. Consequently, FTMs require extensive hardware, including at least one oscillator and one mixer for each tuner, making the module costly and too large for some applications. Furthermore, as the channel capacity of a FTM grows, the module consumes more power due to the increase in analog components.

What is needed is a method or apparatus for implementing a scalable switch architecture for a FTM that minimizes circuit area and power consumption.

SUMMARY

In order to reduce circuit area and power consumption as the capacity of FTMs grow, digital frequency converters and filters, which are compact in modern integrated circuit technology and consume less power than their analog counterparts, may be used to implement a scalable FTM architecture. In an embodiment of the present invention, a frequency translation module for a broadband multi-channel communication system may include the following: an analog signal converter configured to receive a plurality of analog signals, to select analog signals residing in a predefined frequency band, and to convert each of the selected analog signals into a digital signal; a digital channel selection device configured to process digital signals corresponding to the selected analog signals and to generate a composite output of digital signals representative of the selected analog signals; and, a digital-to-analog (D/A) converter configured to translate the composite output to an analog signal output decodable by a receiver. The frequency translation module may also include a mixer configured to upconvert the analog signal output to a frequency decodable by the receiver.

In another embodiment, a method of switching channels on a broadband multi-channel communication system with a scalable switch architecture may include the following steps: (1) receiving a plurality of analog signals; (2) selecting analog signals whose frequency resides in a predefined frequency band of the communication system; (3) converting each of the selected analog signals into a digital signal; (4) processing the digital signal, corresponding to each of the selected analog signals, into a composite output of digital signals; and, (5) translating the composite output to an analog signal output decodable by a receiver. The method may further include upconverting the analog signal output to a frequency decodable by the receiver.

In another embodiment, a system for switching channels on a broadband multi-channel communication system with a scalable switch architecture may include an antenna, a FTM, a processor, and a memory. The FTM may receive signals through the antenna. Further, the processor may control the operation of the FTM. The memory is in communication with the processor and may store processing instructions. These processing instructions may include directing the processor to perform the following functions: receive a plurality of analog signals; select analog signals whose frequency resides in a predefined frequency band of the communication system; convert each of the selected analog signals into a digital signal; process the digital signal, corresponding to each of the select analog signals, into a composite output of digital signals; and, translate the composite output to an analog signal output decodable by a receiver. The processing instruction may also include directing the processor to upconvert the analog signal output to a frequency decodable by the receiver.

Further embodiments, features, and advantages of the present invention, as well as the structure and operation of the various embodiments are described in detail below with reference to accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which:

FIG. **1** illustrates a conventional frequency translation module.

FIG. **2** illustrates a configuration of components in a conventional frequency translation module.

FIG. **3** illustrates a tuner circuit used in a conventional frequency translation module.

FIG. **4** illustrates a processing of signals through a tuner and frequency division multiple access circuit in a conventional frequency translation module.

FIG. **5** illustrates one embodiment of a frequency translation module for a broadband multi-channel communication system.

FIG. **6** illustrates one embodiment of an analog signal converter.

FIG. **7** illustrates one embodiment of a lowpass filter circuit.

FIG. **8** illustrates one embodiment of a highpass filter circuit.

FIG. **9** illustrates a two sideband communication system with a lower sideband and an upper sideband frequency spectrum.

FIG. **10** illustrates one embodiment of a lower band frequency converter.

FIG. **11** illustrates one embodiment of an upper band frequency converter.

FIG. **12** illustrates one embodiment of a digital channel selection device.

FIG. **13** illustrates another embodiment of a frequency translation module for a broadband multi-channel communication system.

FIG. **14** illustrates another embodiment of a frequency translation module for a broadband multi-channel communication system.

FIG. **15** illustrates another embodiment of an analog signal converter.

FIG. **16** illustrates one embodiment of a method of switching channels on a broadband multi-channel communication system with a scalable switch architecture.

FIG. **17** illustrates another embodiment of a method of switching channels on a broadband multi-channel communication system with a scalable switch architecture.

FIG. **18** illustrates yet another embodiment of a method of switching channels on a broadband multi-channel communication system with a scalable switch architecture.

FIG. **19** illustrates one embodiment of a system for switching channels on a broadband multi-channel communication system with a scalable switch architecture.

DETAILED DESCRIPTION

FIG. **1** illustrates frequency translation module (FTM) **100** with three signal inputs. In one embodiment, each signal input may be coupled to a satellite antenna **101-103**, each receiving a signal from a different orbital location and satellite broadcast. For example, antenna **101** may receive a signal from a satellite source in one orbital location that broadcasts one set of high-definition channels, antenna **102** may receive a signal from a satellite source in another orbital location that broadcasts another set of high-definition channels, and antenna **103** may receive a signal from a satellite source in another orbital location that broadcasts other specialized programming. Alternatively, FTM **100** may receive its inputs from a single antenna with multiple outputs, where each output corresponds to, for example, a different satellite transmission frequency, polarization, or location. Further, each signal input of FTM **100** may also be derived from a cable television (CATV) system or an off-air antenna. However, these mentioned communication broadcast sources are not meant to limit the invention.

FIG. **2** illustrates a configuration of components in FTM **100**. FTM **100** translates each signal input into a channel of interest through a tuner **201-203** and a frequency division multiple access (FDMA) circuit **200**. Each tuner **201-203** is coupled to an antenna **101-103**. Further, an output of each tuner **201-203** is coupled to FDMA circuit **200**. For satellite broadcasts, tuners **201-203** each down-convert a radio frequency (RF) input to a baseband signal. In one embodiment, the RF input signal may be an analog television signal having a plurality of television channels that occupy a particular frequency spectrum. FDMA circuit **200** translates each output from tuners **201-203** into a particular frequency band that can be decoded by an integrated receiver decoder (IRD).

As illustrated in FIG. **3**, tuner **201** includes an amplifier **300**, mixers **301** and **303**, a lowpass filter **302**, and phase lock loops (PLLs) **304** and **306**. Tuner **201** performs a dual frequency conversion to select and down-convert a desired or selected channel from a RF input signal **101**. In doing so, amplifier **300** receives and amplifies RF input signal **101**, which contains a plurality of television channels. Mixer **301** receives RF input signal **101** from amplifier **300** and also receives a local oscillator (LO) signal from PLL **304**. For direct conversion, the frequency of PLL **304** is tuned to the frequency of the desired channel in RF input signal **101** so that it is down-converted to baseband, for further processing. For example, if the desired channel in RF input signal **101** is at 100 MHz, then PLL **304** is tuned to 100 MHz, so that mixer **301** down-converts the desired channel in RF signal **101** to DC.

In television and cable tuners, PLL **304** can be controlled by a control signal **305** so to tune the frequency of the LO signal produced by PLL **304**, and thereby control the channel selection that is down-converted to baseband by mixer **301**. Control signals for tuner control are well known to those skilled in the relevant art.

Lowpass filter **302** filters the output of mixer **301** to remove unwanted spurious energy that is above baseband. In another embodiment of tuner **201**, image rejection techniques may be implemented to reduce undesired signals at the output of mixer **301**. For example, a Hartley circuit architecture or Weaver circuit architecture may be incorporated in the design of tuner **201** to further suppress image signals. Image rejection techniques are known to those skilled in the relevant art.

Mixer **303** receives the output of lowpass filter **302** and also receives a LO signal from PLL **306**. Mixer **303** up-converts the output of lowpass filter **302** to generate a RF signal containing the channel of interest. Typically, the frequency of PLL **306** is tuned to a frequency within a frequency bandwidth that may be decoded by the IRD. The specific frequencies mentioned in the description of tuner **201**, and throughout this application, are given for example purposes only and are not meant to be limiting. Those skilled in the relevant art will recognize other frequency applications for tuner **201** based on the discussion given herein. These other frequency applications are within the scope and spirit of the present invention.

In returning to FIG. **2**, antennas **101-103** may receive signals in different frequency spectrums (e.g., antenna **101** may receive high-definition signals in one frequency spectrum, tuner **102** may receive specialized programming in another frequency spectrum, and so forth). Exemplary frequency spectrums **404-406** are illustrated in FIG. **4**, where each frequency spectrum **404-406** contains a channel of interest (e.g., channels **401**, **402**, and **403**). Tuners **201-203** process channels **401-403** to generate outputs **407-409** within the same frequency spectrum using the frequency conversion process described above with respect to FIG. **3**.

FDMA circuit **200** receives each output **407-409** and further processes each signal into a composite signal within a given frequency bandwidth that can be decoded by the IRD. The IRD decodes these signals and separates them into viewer channels, which are then passed to a television or computer monitor for viewing by a user. FDMA circuits and IRDs are known to those skilled in the relevant art.

The FTM architecture described above may be adequate for applications with a small number of FTM input sources, but the architecture does not scale well when there are many

input channel sources. That is, as FTMs grow in capacity, the number of analog components also grows as a result of the number of tuners required for each signal input. For example, for a six-channel FTM, six tuners are required to process each input channel signal; likewise, for a nine-channel FTM, nine tuners are required to process each input channel signal; and, so forth. Many external discrete components may be necessary for signal filtering, which results in an increase in circuit area.

In addition to circuit area, power consumption also increases as a result of growth in FTM capacity. In certain communication system designs, such as mobile or portable applications, circuit area constraints and power consumption requirements may limit the number of channels in a FTM. For example, the analog components in tuner **201** may consume over **1** watt of power. As FTM **100** grows in channel capacity, the number of tuners increases and, consequently, power consumption increases as well. By using digital frequency converters and filters, which are compact in modern integrated circuit technology and consume less power than their analog counterparts, a scalable FTM architecture may be implemented.

FIG. **5** illustrates a FTM **500** according to one embodiment of the present invention. For explanation purposes, FTM **500** operates in a satellite system that broadcasts signals within two frequency bands (e.g., a lower sideband of 950-1450 MHz and an upper sideband of 1650-2150 MHz). Based on the description herein, a person skilled in the relevant art will recognize that FTM **500** can be designed for a communication system that broadcasts signals in one or more frequency bands.

FTM **500** employs an analog signal converter **501** to convert input signals from analog domain to digital domain. Subsequently, digital channel selection devices $\mathbf{502}_1$ and $\mathbf{502}_2$ process the digital information through a series of frequency converters and filters to produce a digital stream of data. The digital stream of data contains one or more channels of interest in both a lower and upper frequency band of the satellite system. Finally, a digital summer **508** and a digital-to-analog (D/A) converter **503** transform the digital data to an analog format, such that an IRD can decode the resulting signals and separate them into viewer channels. The channels are then passed to a television or computer monitor for viewing by the user.

Unlike the conventional FTM architecture described above with respect to FTM **100**, FTM **500** is a scalable architecture in which analog signal converter **501** can be used for two or more input channel sources (e.g., antennas **505-507**) without growth in size or complexity. For instance, as noted above with respect to FTM **100**, a six-channel FTM would require six tuners and, accordingly, a nine-channel FTM would require nine tuners. Both the number of analog components and power consumption grow proportionately with the number of channels in the conventional design of FTM **100**.

On the other hand, the number of analog components and power consumption do not grow proportionately with an increase in the number of input channel sources in FTM **500**. The number of analog components in analog signal converter **501** remains the same regardless of the number of input channel sources received by FTM **500**. The number of digital components may grow as a result of the increase in input channel sources. However, the power consumption from the increase in digital components in FTM **500** will typically be far less than the power consumption from an increase in analog components in the conventional design of FTM **100**

In referring to FIG. **5**, a signal input **504** to FTM **500** may be coupled to one or more broadcast sources. In one embodiment, signal input **504** may be coupled to three satellite antennas **505-507**, each receiving a signal from a different orbital location. In another embodiment, signal input **504** may be coupled to a single antenna with multiple outputs, where each output corresponds to, for example, a different transmission frequency, polarization, or location. Further, signal input **504** of FTM **500** may also be coupled to other broadcast sources, such as a CATV system or off-air antennas. However, these communication broadcast sources are not meant to limit the invention.

Analog signal converter **501** translates RF signals from antennas **505-507** into digital format. FIG. **6** illustrates one embodiment of analog signal converter **501**, which includes two signal converters **610** and **611**. In one embodiment, signal converter **610** includes a lowpass filter circuit **601** and a lower band frequency converter **602**. In another embodiment, lowpass filter circuit **601** can be replaced with a bandpass filter configured to filter out frequencies residing in a lower frequency band (e.g., lower sideband 950-1450 MHz). In one embodiment, signal converter **611** includes a highpass filter circuit **603** and an upper band frequency converter **604**. In another embodiment, highpass filter circuit **603** can be replaced with a bandpass filter configured to filter out frequencies residing in an upper frequency band (e.g., upper sideband 1650-2150 MHz). FIG. **7** illustrates one embodiment of lowpass filter circuit **601**, which includes a lowpass filter **701** and an amplifier **702**. Further, FIG. **8** illustrates one embodiment of highpass filter circuit **603**, which includes a highpass filter **801** and an amplifier **802**.

As mentioned above, a communication system with two frequency bands will be discussed to facilitate in the explanation of FTM **500**. For example, FIG. **9** illustrates a communication system **900** that broadcasts RF signals in two frequency bands—a lower sideband **901** and an upper sideband **903**—that each has a bandwidth of 500 MHz. In this communication system, lowpass and highpass filter circuits **601** and **603** filter one or more FTM input signals into either lower sideband **901** or upper sideband **903** frequency spectrum. For instance, if antennas **505** and **506** receive RF signals between 950 MHz and 1.45 GHz and antenna **507** receives a RF signal between 1.65 GHz and 2.15 GHz, then lowpass filter circuit **601** selectively passes the RF signals from antennas **505** and **506** and suppresses the higher RF signal from antenna **507**. Conversely, highpass filter circuit **603** selectively passes the RF signal from antenna **507** and suppresses the lower RF signals from antennas **505** and **506**. Amplifier **702** in lowpass filter circuit **601** receives and amplifies the signal from lowpass filter **701**. Likewise, amplifier **802** in highpass filter circuit **603** receives and amplifies the signal from highpass filter **801**.

The specific frequency bands mentioned in the description of the communication system above, and throughout this application, are given for example purposes only and are not meant to be limiting. Those skilled in the relevant art will recognize that other frequency bands and communication system applications based on the discussion given herein. The other communication systems are within the scope and spirit of the present invention.

Lower band frequency converter **602** receives the amplified signal from lowpass filter circuit **601**. As illustrated in FIG. **10**, lower band frequency converter **602** includes a mixer **1001**, a PLL **1002**, a lowpass filter **1003**, an amplifier **1004**, and an analog-to-digital (A/D) converter **1005**. Mixer **1001** receives the RF input signal from low pass filter circuit **601** and also receives a LO signal from PLL **1002**. In reference to the communication system illustrated in FIG. **9**, the frequency of PLL **1002** may be tuned to a frequency **902** sub-

stantially in the center of lower sideband **901**. For example, if lower sideband **901** has a frequency range between 950 MHz and 1.45 GHz, then PLL **1002** may be tuned to 1.2 GHz.

In tuning PLL **1002** to a frequency **902** substantially in the center of lower sideband **901**, one or more RF signals residing in lower sideband **601** may be down-converted to an alternate frequency. For example, in reference to FIG. **5**, FTM **500** may be coupled to three satellite antennas **505-507** broadcasting television channels in a frequency range residing in lower sideband **901**. After the RF signals received from each satellite antenna **505-507** are filtered by lowpass filter circuit **601**, mixer **1001** down-converts these signals to another frequency.

Lowpass filter **1003** filters the output of mixer **1001** to remove unwanted spurious energy that is above baseband. Similar to the description with respect to FIG. **3**, in another embodiment of lower band frequency converter **602**, image rejection techniques may be implemented to reduce undesired signals at the output of mixer **1001**. For example, a Hartley circuit architecture or Weaver circuit architecture may be implemented to further suppress image rejection. Image rejection techniques are known to those skilled in the relevant art

In FIG. **10**, amplifier **1004** receives the output of lowpass filter **1003** and amplifies the RF signal. A/D converter **1005** samples the RF signal to translate the analog signal into a digital format. The digital data is then processed by digital channel selection device **502** to filter unwanted noise and to increase the resolution of the digital signal. An example of A/D converter **1005** is a sigma-delta A/D converter and flash A/D converter. Alternatively, other types of A/D converters may be used.

FIG. **11** illustrates an embodiment of upper band frequency converter **604**, which includes a mixer **1101**, a PLL **1102**, a lowpass filter **1103**, an amplifier **1104**, and an A/D converter **1105**. Mixer **1101** receives the RF input signal from highpass filter circuit **603** and also receives a LO signal from PLL **1102**. In reference to the communication system illustrated in FIG. **9**, the frequency of PLL **1102** may be tuned to a frequency **904** substantially in the center of upper sideband **903**. For example, if upper sideband **903** has a frequency range between 1.65 GHz and 2.15 GHz, then PLL **1102** may be tuned to 1.9 GHz.

In tuning PLL **1102** to a frequency **904** substantially in the center of upper sideband **903**, RF signals residing in upper sideband **903** may be down-converted to an alternate frequency. For example, in reference to FIG. **5**, FTM **500** may be coupled to three satellite antennas **505-507** broadcasting television channels in a frequency range residing in upper sideband **903**. After RF signals from each satellite antenna **505-507** are filtered by highpass filter circuit **603**, mixer **1101** down-converts the signals to another frequency. Lowpass filter **1103**, amplifier **1104**, and A/D converter **1105** function in a similar manner to that described in FIG. **10**.

An output of lower band frequency converter **602** is coupled to a digital channel selection device $\mathbf{502}_1$. Likewise, an output of upper band frequency converter **604** is coupled to a digital channel selection device $\mathbf{502}_2$. Digital channel selection devices $\mathbf{502}_1$ and $\mathbf{502}_2$ reduce the sampling rate from the digital outputs of A/D converters **1005** and **1105**, filter unwanted noise signals, and increase the resolution of the digital output. As illustrated in FIG. **12**, digital channel selection device **502** includes mixers **1201** and **1205**, PLLs **1202** and **1206**, a decimation filter bank **1203**, and a lowpass filter **1204**.

Mixer **1201** receives digital data from A/D converters **1005** and **1105** at a particular sampling rate. The frequency of PLL **1202** is tuned to a frequency that reduces the data rate to a more useful value for processing by decimation filter bank **1203**. An example of PLL **1202** is a direct digital frequency synthesis (DDFS) device. A DDFS device may be a phase accumulator that generates a digitized waveform. DDFS devices are known to those skilled in the relevant art. Alternatively, other types of PLLs may be used.

Decimation filter bank **1203** receives the output of mixer **1201**. Decimation filter bank **1203** is designed to down-sample, or decimate, the output of mixer **1201** and to filter the digital signal such that a proper frequency response and signal-to-noise ratio are achieved. For example, in referring to the communication system illustrated in FIG. **9**, antenna **505** may receive a RF signal with a frequency of 1.3 GHz, which resides in lower sideband **901**. Lowpass filter circuit **601** selectively passes the 1.3 GHz signal to lower band frequency converter **602**. As described with respect to FIG. **10**, PLL **1002** may be tuned to a frequency **902** substantially in the center of lower sideband **901**. In FIG. **9**, this center frequency is approximately 1.1 GHz. The output of mixer **1001** contains the sum and difference of its two frequency inputs (i.e., input frequencies, 1.3 and 1.1 GHz), to produce an output signal with frequencies of 0.2 GHz and 2.4 GHz. Lowpass filter **1003** filters-out the frequency summation output of mixer **1001** (i.e., 1.3 GHz+1.1 GHz=2.4 GHz), leaving a signal with a frequency of the difference of the two input frequencies (i.e., 1.3 GHz−1.1 GHz=0.2 GHz) at the output of lowpass filter **1003**. The intermediate frequency output of lowpass filter **1003** is then processed into a digital signal through amplifier **1004** and A/D converter **1005**. The frequency of the digital signal at the output of A/D converter **1005** is then converted to another intermediate frequency. Highpass filter circuit **603** and upper band frequency converter **604** process RF signals that reside in upper sideband **903** in a similar manner to that described above.

Decimation filter bank **1203** receives the output of mixer **1201** and processes the digital data into a narrow band of output frequencies. This narrow band of frequencies contains the channels of interest. Decimation filters are known to those skilled in the relevant art.

Lowpass filter **1204** filters the output of decimation filter bank **1203** to remove unwanted spurious energy that is above baseband. Further, mixer **1205** receives the output of lowpass filter **1204** and also receives a LO signal from PLL **1206**. Mixer **1205** up-converts the frequency of the digital signal output of lowpass filter **1204** to an alternate frequency. The up-converted frequency may be in a frequency bandwidth that may be decoded by the IRD. PLL **1206** functions in a similar manner to that described with respect to PLL **1202**. A person skilled in the relevant art will appreciate that for a given set of frequencies within lower sideband **901**, lower band frequency converter **602** may output a narrow band of frequencies containing a channel of interest from this band of frequencies; likewise, upper band frequency converter **604** may also output a narrow band of frequencies containing a channel of interest from frequencies in upper sideband **903**.

In returning to FIG. **5**, digital summer **508** sums the outputs of digital channel selection devices $\mathbf{502}_1$ and $\mathbf{502}_2$. Digital summer **508** produces a composite digital representation of a reduced bandwidth signal containing channels of interest from among a full spectrum of RF signals received by antennas **505-507**. D/A converter **503** receives the output from digital summer **508** and translates the digital output into an analog signal that may be decoded by an IRD. The IRD decodes the RF signals and separates them into viewer channels, which are then passed to a television or computer moni-

tor for viewing by a user. Digital summer devices and D/A converters are known to those skilled in the relevant art.

In view of the discussion above with respect to FIGS. **5-12**, as the number of input channel sources received by FTM **500** increase, the architecture of FTM **500** not only occupies a smaller circuit footprint than conventional FTM **100**, but also consumes less power than FTM **100**. Specifically, as the number of input channel sources grows, analog converter **501** in FTM **500** does not increase in size or complexity, whereas FTM **100** would require an additional tuner for each additional input channel source. Even though the number of digital circuits may grow in FTM **500** as a result of an increase in input channel sources, integrated digital circuits typically consume far less circuit area than analog components in tuner designs. Further, since FTM **100** would require an additional tuner for each additional input channel source, each additional tuner in FTM **100** would typically consume far more power than digital circuits used in the signal processing in FTM **500**.

FIG. **13** illustrates another embodiment of FTM **500**, where a mixer **1300**, a PLL **1301**, and a lowpass filter **1302** are coupled to an output **513** of D/A converter **503**. Mixer **1300** may be used to up-convert the output of D/A converter **508** to a RF signal containing the channel of interest. The frequency of PLL **1301** may be tuned to a frequency within a frequency bandwidth that may be decoded by an IRD. Highpass filter **1302** filters the output of mixer **1300** to remove unwanted spurious energy that is above baseband. The IRD decodes the signals at an output **1303** of highpass filter **1302** and separates them into viewer channels, which are then passed to a television or computer monitor for viewing by a user. IRDs are known to those skilled in the relevant art.

FIG. **14** illustrates a FTM **1400** according to an embodiment of the present invention. FTM **1400** includes an analog signal converter **1401**, digital channel selection device **502**, and D/A converter **503**. Digital channel selection device **502** and D/A converter **503** function in the same manner as described above with respect to FIG. **5**.

FIG. **15** illustrates an embodiment of analog signal converter **1401**. Analog signal converter **1401** includes a filter **1501** and a frequency converter **1502**. Analog signal converter **1401** functions in a similar manner as signal converters **610** and **611** described above with respect to FIG. **6**. However, unlike the processing of signals residing in the lower and upper frequency bands by signal converters **610** and **611**, respectively, analog signal converter **1401** processes signals residing in both the lower and upper frequency bands (e.g., a frequency spectrum compatible with a broadband communication system in which FTM **1400** is implemented). A person skilled in the relevant art will recognize, based on the description herein, that analog signal converter **1401** can process signals in communication systems with broadcasts in one or more frequency bands.

Filter **1501** selectively passes RF signals from antennas **505-507** to frequency converter **1502**. In one embodiment, filter **1501** may be a bandpass filter configured to filter out signals residing in a predefined frequency band such as, for example, 950-2150 MHz. In an embodiment, the predefined frequency band can be an entire frequency spectrum compatible with a broadband communication system in which FTM **1400** is implemented or a sub-set of the frequency spectrum. Similar to amplifiers **702** and **802** in FIGS. **7** and **8**, respectively, an output signal of the bandpass filter may be amplified before being passed to frequency converter **1502** according to an embodiment of the present invention. In another embodiment, filter **1501** can be a lowpass or a highpass filter.

Frequency converter **1502** functions in a similar manner as lower band frequency converter **602** and upper band frequency converter **604** in FIGS. **10** and **11**, respectively. In particular, frequency converter **1502** receives a filtered signal from filter **1501**, processes the filtered signal through a mixer, filters the signal from an output of the mixer to remove unwanted spurious energy above baseband, amplifies the resulting filtered signal, and samples the amplified signal to translate the analog signal into a digital format. The mixer in frequency converter **1502** receives a LO signal from a PLL, where in one embodiment, the frequency of the PLL may be tuned to a frequency substantially in the center of a predefined frequency band. For instance, if FTM **1400** operates in a satellite system that broadcasts signals between 950-2150 MHz, then the PLL may be tuned to 1.55 GHz.

Further, in an embodiment of FTM **1400**, a mixer, a PLL, and a lowpass filter can be coupled to an output of D/A converter **503**. The configuration and operation of the mixer, PLL, and lowpass filter are similar to that of mixer **1300**, PLL **1301**, and lowpass filter **1302** of FIG. **13**.

FIG. **16** illustrates one embodiment of a method **1600** to switch channels on a broadband multi-channel communication system with a scalable switch architecture. Method **1600** may occur using, for example, FTM **500**. In step **1610**, an analog signal whose frequency resides in a first frequency band of the communication system is processed. In step **1620**, an analog signal whose frequency resides in a second frequency band of the communication system is processed. The first frequency band may correlate to a lower sideband frequency spectrum and the second frequency band may correlate to an upper sideband frequency spectrum in a two frequency sideband communication system. An example of a communication system with two frequency sidebands is illustrated in FIG. **9**.

In returning to FIG. **16**, step **1630** converts the processed analog signals, from the first and second frequency bands, into a narrow band of digital output frequencies. For example, digital channel selection device **502** may be used to perform step **1630**. In turning to step **1640**, a composite digital output from the narrow band of digital output frequencies is generated. Digital summer **508** in FIG. **5** may be used to perform this step. In step **1650**, the digital signals resulting from step **1640** are translated into analog form such that a receiver may decode the signals. D/A converter **503** in FIG. **5** may be used to perform step **1650**.

FIG. **17** illustrates another embodiment of a method **1700** to switch channels on a broadband multi-channel communication system with a scalable switch architecture. Steps **1710-1740** perform in a similar manner to steps **1610-1640** in FIG. **16**. Step **1750** translates the digital signals resulting from step **1740** into analog form. In step **1760**, the resulting analog signals from step **1750** are up-converted to a frequency within a frequency bandwidth that may be decoded by a receiver. Mixer **1300**, PLL **1301**, and highpass filter **1302** in FIG. **13** may be used to up-convert the frequency of the analog signal such that a receiver may decode the analog signal.

FIG. **18** illustrates yet another embodiment of a method **1800** to switch channels of a broadband multi-channel communication system with a scalable switch architecture. In step **1810**, a plurality of analog signals is received by a frequency translation module. FTM **1400** can be used, for example, to receive the plurality of analog signals, where the plurality of analog signals can be received from different satellite orbital locations, polarizations, and satellite transmission frequencies. In an embodiment, the plurality of analog signals reside in a frequency spectrum compatible with the broadband multi-channel communication system (e.g., 950-2150 MHz).

In step **1820**, analog signals whose frequencies reside in a predefined frequency band of the communication system are selected. In an embodiment, the analog signals can be selected using a bandpass filter. In another embodiment, the analog signal can be selected using a lowpass filter. The analog signal can also be selected using a highpass filter according to yet another embodiment of the present invention.

In step **1830**, each of the selected analog signals from step **820** are converted into a digital signal. A/D converter **1005** or A/D converter **1105** of FIGS. **10** and **11**, respectively, can be used, for example, to convert the selected analog signals into a digital format.

In step **1840**, a composite digital output is generated from the converted digital signals in step **830**. For example, digital channel selection device **502** may be used to perform step **1840**.

Step **1850** translates the composite digital output into an analog signal output decodable by a receiver. Further, step **1860** upconverts the analog signal output to a frequency decodable by the receiver.

FIG. **19** illustrates one embodiment of a system **1900** for switching channels on a broadband multi-channel communication system with a scalable switch architecture. System **1900** includes an antenna **1901**, a FTM **1902**, a processor **1903**, and a memory **1904**. The representative signal processing functions described herein can be implemented in hardware, software, or some combination thereof. For instance, the signal processing functions can be implemented using computer processors, computer logic, application specific circuits (ASICs), digital signal processors, etc., as will be understood by those skilled in the arts based on the discussion given herein. Accordingly, any processor that performs the signal processing functions described herein is within the scope and spirit of the present invention.

Further, the signal processing functions described herein could be embodied by computer program instructions that are executed by a computer processor or any one of the hardware devices listed above. The computer program instructions cause the processor to perform the signal processing functions described herein. The computer program instructions (e.g., software) can be stored in a computer usable medium, computer program medium, or any storage medium that can be accessed by a computer or processor. Such media include a memory device such as a RAM or ROM, or other type of computer storage medium such as a computer disk or CD ROM, or the equivalent. Accordingly, any computer storage medium having computer program code that cause a processor to perform the signal processing functions described herein are within the scope and spirit of the present invention.

In reference to FIG. **19**, FTM **1902** is coupled to antenna **1901** and receives signals through antenna **1901**. Processor **1903** is coupled to FTM **1902** and controls the operation of FTM **1902**. Memory **1904** is in communication with processor **1903** and stores processing instructions. In one embodiment of the present invention, these processing instructions direct processor **1903** to perform the procedures of method **1800**. Specifically, the processing instructions direct processor **1903** to perform the following: (1) receive a plurality of analog signals; (2) filter out analog signals whose frequency resides in a predefined frequency band of the communication system; (3) convert each of the filtered analog signals into a digital signal; (4) process the digital signal, corresponding to each of the filtered analog signals, into a composite output of digital signals; and, (5) translate the composite output to an analog signal output decodable by a receiver. The processing instructions can also direct processor **1903** to upconvert the analog signal output to a frequency decodable by the receiver.

In one embodiment, the processing direction for directing processor **1903** to convert each of the filtered analog signals may include filtering the analog signal with a filter (e.g., a lowpass filter, highpass filter, and a bandpass filter), mixing the filtered analog signal with a local oscillator (LO) signal with a predefined LO frequency, and digitizing the mixed analog signal with an analog-to-digital (A/D) converter. Further, in one embodiment, the processing direction for directing processor **1903** to mix the filtered analog signal may include mixing the filtered analog signal with a LO signal with a frequency substantially in the center of the predefined frequency band.

In another embodiment of the present invention, the processing instructions stored in memory **1904** direct processor **1903** to perform the procedures of method **1600**. In yet another embodiment of the present invention, the processing instructions stored in memory **1904** direct processor **1904** to perform the procedures of method **1700**.

In one embodiment, the processing direction for directing the processor to process the analog signal residing in the first frequency band may include tuning a mixer's local oscillator input to a frequency substantially in the center of the first frequency band. Similarly, in one embodiment, the processing direction for directing the processor to process the analog signal residing in the second frequency band may include tuning a mixer's local oscillator input to a frequency substantially in the center of the second frequency band. Further, in one embodiment, the processing direction for directing the processor to convert the analog signals may include processing digital signals through a series of digital up-conversion, digital down-conversion, and filtering of the digital signals.

The foregoing description of the specific embodiments will so fully reveal the general nature of the invention that others can, by applying knowledge within the skill of the relevant art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present invention. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance. Accordingly, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What is claimed is:

1. A frequency translation module for a broadband multi-channel communication system, comprising:

an analog signal converter configured to receive a plurality of analog signals, to select analog signals associated with a predefined frequency band to produce selected analog signals, and to convert each of the selected analog signals into respective digital signals;

a digital channel selection device configured to process the respective digital signals corresponding to the selected analog signals to generate a composite output of digital signals representative of the selected analog signals, wherein the digital channel selection device includes a plurality of mixers, a plurality of phase lock loop circuits, a decimation filter bank, and a filter; and

a digital-to-analog (D/A) converter configured to translate the composite output to an analog signal output decodable by a receiver.

2. The frequency translation module of claim **1**, further comprising an antenna configured to receive the plurality of analog signals, wherein the antenna includes a plurality of outputs, each output corresponding to at least one of a different satellite transmission frequency, polarization, and satellite orbital location.

3. The frequency translation module of claim **1**, further comprising a plurality of antennas, wherein each antenna is configured to receive a satellite signal from a different orbital location.

4. The frequency translation module of claim **1**, further comprising a mixer configured to upconvert the analog signal output to a frequency decodable by the receiver.

5. The frequency translation module of claim **1**, wherein the plurality of analog signals are associated with a frequency spectrum compatible with the broadband multi-channel communication system.

6. The frequency translation module of claim **1**, wherein the analog signal converter comprises a filter, a mixer, and an analog-to-digital (A/D) converter configured to process at least one of the selected analog signals whose frequency is associated with the predefined frequency band.

7. The frequency translation module of claim **6**, wherein the filter comprises a bandpass filter.

8. The frequency translation module of claim **6**, wherein a frequency of a local oscillator (LO) input of the mixer correlates to a frequency substantially in the center of the predefined frequency band.

9. The frequency translation module of claim **1**, wherein the decimation filter bank is configured to down-sample a digital output of a mixer to generate a second digital signal and to filter the second digital signal to achieve a predefined frequency response and signal-to-noise ratio.

10. A method of switching channels on a broadband multi-channel communication system with a scalable switch architecture, comprising:

receiving a plurality of analog signals;

selecting, from the plurality of analog signals, analog signals having frequencies associated with a predefined frequency band of the communication system as selected analog signals;

converting each of the selected analog signals into respective digital signals;

combining the respective digital signals, corresponding to each of the selected analog signals, to generate a composite output of digital signals, wherein combining the respective digital signals includes,

down-sampling a digital signal from the respective digital signals to generate a down-sampled digital signal, and

filtering the down-sampled digital signal to achieve a predefined frequency response and signal-to-noise ratio; and

converting the composite output to an analog signal output decodable by a receiver.

11. The method of claim **10**, further comprising:

upconverting the analog signal output to a frequency decodable by the receiver.

12. The method of claim **10**, wherein receiving the plurality of analog signals comprises receiving a plurality of satellite broadcasts from at least one of a plurality of orbital locations, a plurality of polarizations, and a plurality of satellite transmission frequencies.

13. The method of claim **10**, wherein selecting signals comprises selecting signals that are associated with a frequency spectrum compatible with the broadband multi-channel communication system.

14. The method of claim **10**, wherein converting each of the filtered analog signals comprises:

filtering the analog signal into a filtered analog signal with at least one of a lowpass filter, highpass filter, and a bandpass filter;

mixing the filtered analog signal with a local oscillator (LO) signal having a predefined LO frequency to generate a mixed analog signal;

digitizing the mixed analog signal using an analog-to-digital (A/D) converter.

15. The method of claim **14**, wherein mixing the filtered analog signal comprises mixing the filtered analog signal with a LO signal having a frequency substantially in the center of the predefined frequency band.

16. The method of claim **10**, wherein processing the digital signal comprises generating a narrow band of output frequencies that contain channels of interest through a series of digital up-conversion, digital down-conversion, and filtering of the digital signal.

17. A system for switching channels on a broadband multi-channel communication system with a scalable switch architecture, comprising:

an antenna;

a frequency translation module coupled to the antenna, wherein the frequency translation module is configured to receive signals through the antenna;

a processor coupled to the frequency translation module, wherein the processor is configured to control the operation of the frequency translation module; and

a memory in communication with the processor, the memory configured to store a plurality of processing instructions for directing the processor to:

receive a plurality of analog signals;

select, from the plurality of analog signals, analog signals having frequencies associated with a predefined frequency band of the communication system, resulting in selected analog signals;

convert each of the selected analog signals into respective digital signals;

combine the respective digital signals, corresponding to each of the selected analog signals, to generate a composite output of digital signals, wherein to combine the respective digital signals the processor is further instructed to

down-sample a digital signal from the respective digital signals to generate and down-sampled digital signal, and

filter the down-sampled digital signal to achieve a predefined frequency response and signal-to-noise ratio; and

translate the composite output to an analog signal output decodable by a receiver.

18. The system of claim **17**, wherein the memory is configured to store a plurality of processing instructions for directing the processor to upconvert the analog signal output to a frequency decodable by the receiver.

19. The system of claim **17**, wherein the instructions for directing the processor to convert each of the filtered analog signals comprise instructions for directing the processor to

filter the analog signal to generate a filtered analog signal using at least one of a lowpass filter, highpass filter, and a bandpass filter;

mix the filtered analog signal with a local oscillator (LO) signal having a predefined LO frequency to generate a mixed analog signal; and

digitize the mixed analog signal with an analog-to-digital (A/D) converter.

20. The system of claim **19**, wherein the instructions for directing the processor to mix the filtered analog signal comprise instructions for directing the processor to mix the filtered analog signal with a LO signal having a frequency substantially in the center of the predefined frequency band.

21. The system of claim **17**, wherein the instructions for directing the processor to process the respective digital signals comprise instructions for directing the processor to generate a narrow band of output frequencies that contain channels of interest through a series of operations including digital up-conversion, digital down-conversion, and filtering on the respective digital signals.

22. A frequency translation module for a broadband multichannel communication system, comprising:

an analog signal converter configured to select analog signals associated with a predefined frequency band to produce selected analog signals, and to convert each of the selected analog signals into respective digital signals;

a digital channel selection device configured to process the respective digital signals corresponding to the selected analog signals to generate a composite output of digital signals representative of the selected analog signals, wherein the digital channel selection device comprises a decimation filter bank configured to

down-sample a digital signal from the respective digital signals to generate a down-sampled digital signal, and

filter the down-sampled digital signal to achieve a predefined frequency response and signal-to-noise ratio; and

a digital-to-analog (D/A) converter configured to translate the composite output to an analog signal.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	: 8,224,274 B2
APPLICATION NO.	: 12/337046
DATED	: July 17, 2012
INVENTOR(S)	: Ramon Gomez

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At column 14, line 51, please replace "generate and down-sampled" with --generate a down-sampled--.

Signed and Sealed this
Twenty-fifth Day of September, 2012

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of: Madhukar Reddy *et al.*	§	REQUEST FOR *Ex Parte* REEXAMINATION
	§	
U.S. Patent No. 9,210,362	§	
	§	Attorney Docket No.: 50348.106
Filed: February 5, 2015	§	
	§	Customer No.: 27683
Issued: December 8, 2015	§	
	§	
Title: WIDEBAND TUNER ARCHITECTURE	§	Real Party in Interest: Unified Patents, LLC
	§	

REQUESTER'S POWER OF ATTORNEY PURSUANT TO 37 CFR 1.510(f)

Pursuant to 37 CFR 1.510(f) Requester, **Unified Patents, LLC**, hereby appoints the Practitioner(s) associated with **Customer Number 27683**, as its attorney(s) to prosecute and to transact all business in the United States Patent and Trademark Office in connection with the above-identified request for *Ex Parte* Reexamination. Please recognize the correspondence address (including any electronic mail address) associated with **Customer Number 27683** for the above-identified *Ex Parte* Reexamination proceeding number to be the address associated with the appointed counsel(s).

The undersigned is authorized to sign this Power of Attorney on behalf of the Requester.

Executed on 9/18/2023.

Unified Patents, LLC

By: Jonathan Stroud

Printed Name: Jonathan Stroud

Title: General Consel

Exhibit 1002

File History of U.S. Patent No. 9,210,362

Customer No.: 000027683

Haynes and Boone, LLP
IP Section
2323 Victory Avenue, Suite 700
Dallas, Texas 75219
Telephone [214] 651.5000
Fax [214] 200.0853

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22-cv-125	4/27/2022	Eastern District of Texas

PLAINTIFF	DEFENDANT
ENTROPIC COMMUNICATIONS, LLC	CHARTER COMMUNICATIONS, INC., ET AL

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	8,223,775	7/17/2012	Entropic Communications, LLC
2	8,284,690	10/9/2012	Entropic Communications, LLC
3	8,792,008	7/29/2014	Entropic Communications, LLC
4	9,210,362	12/8/2015	Entropic Communications, LLC
5	9,825,826	11/21/2017	Entropic Communications, LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 **Director of the U.S. Patent and Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22-cv-125	4/27/2022	Eastern District of Texas

PLAINTIFF	DEFENDANT
ENTROPIC COMMUNICATIONS, LLC	CHARTER COMMUNICATIONS, INC., ET AL

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	10,135,682	11/20/2018	Entropic Communications, LLC
2			
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/614,543	02/05/2015	Madhukar Reddy	28427US04

CONFIRMATION NO. 5785

23446
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

POA ACCEPTANCE LETTER

OC000000125764692

Date Mailed: 05/24/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/18/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sibrahim/

PTO/AIA/80 (07-17)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no person is required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

[X] Practitioners associated with Customer Number: 23,446

OR

[ ] Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

[X] The address associated with Customer Number: 23,446

OR

[ ]

Firm or individual name		
Address		
City	State	Zip
Country		
Telephone	Email	

Assignee name and address: ENTROPIC COMMUNICATIONS, LLC
1345 AVENUE OF THE AMERICAS, 46TH FLOOR
NEW YORK, NY 10105

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee.

Signature /Andrea L. Gothing/	Date 2021-05-04
Name Andrea L. Gothing	Telephone 415-830-0613
Title Licensing Officer and Authorized Signatory, Entropic Communications, LLC	

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 18 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	42754953
Application Number:	14614543
International Application Number:	
Confirmation Number:	5785
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
First Named Inventor/Applicant Name:	Madhukar Reddy
Customer Number:	23446
Filer:	Ronald H. Spuhler/Deborah Wilson
Filer Authorized By:	Ronald H. Spuhler
Attorney Docket Number:	28427US04
Receipt Date:	18-MAY-2021
Filing Date:	05-FEB-2015
Time Stamp:	16:21:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73	28427US04_373c_Statement_AIA-96.pdf	120583 b06b63dd21b75ce08cdcdf221fb3c1091eef2781	no	3

Warnings:

Information:					
2	Power of Attorney	Entropic-POA_General_Assignee_EntropicCommunications_ALG.pdf	487892 51444e06ae84b241bfc127dc47c5d6c646944dd7	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	608475	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: ENTROPIC COMMUNICATIONS, LLC

Application No./Patent No.: 14/614,543 Filed/Issue Date: 2015-02-05

Titled: WIDEBAND TUNER ARCHITECTURE

ENTROPIC COMMUNICATIONS, LLC, a limited liability company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Curtis Ling, Madhukar Reddy, Tim Gallagher To: MAXLINEAR, INC.

   The document was recorded in the United States Patent and Trademark Office at
   Reel 031851, Frame 0086, or for which a copy thereof is attached.

2. From: MAXLINEAR, INC. To: ENTROPIC COMMUNICATIONS, LLC

   The document was recorded in the United States Patent and Trademark Office at
   Reel 055898, Frame 0230, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Ronald H. Spuhler/	2021-05-18
Signature	Date
Ronald H. Spuhler	52245
Printed or Typed Name	Title or Registration Number

[Page 2 of 2]

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
14/614,543	02/05/2015	MaxLinear, Inc.	28427US04	85006

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 04/03/2019 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Christopher C. Winslade/
Name:	/Christopher C. Winslade/
Registration Number:	36308

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/614,543	12/08/2015	9210362	28427US04	5785

23446 7590 11/18/2015

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Madhukar Reddy, Carlsbad, CA;
MaxLinear, Inc., Carlsbad, CA;
Curtis Ling, Carlsbad, CA;
Tim Gallagher, Carlsbad, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/614,543	02/05/2015	Madhukar Reddy	28427US04	5785

23446 7590 11/06/2015

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER
JACKSON, BLANE J

ART UNIT	PAPER NUMBER
2649	

NOTIFICATION DATE	DELIVERY MODE
11/06/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mhmpto@mcandrews-ip.com

Response to Rule 312 Communication	Application No.	Applicant(s)
	14/614,543	REDDY ET AL.
	Examiner	Art Unit
	BLANE J. JACKSON	2649

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on *26 October 2015* under 37 CFR 1.312 has been considered, and has been:

a) ☒ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/BLANE J JACKSON/
Primary Examiner, Art Unit 2649

OK TO ENTER: /B.J./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Attorney Docket No. 28427US04)

In the Application of:	
	Madhukar Reddy
Serial No.:	14/614,543
Filed:	Feb 5, 2015
Title:	WIDEBAND TUNER ARCHITECTURE
Confirmation No.:	5785
Customer No.:	23446

AMENDMENT UNDER 37 C.F.R. § 1.312

This paper is submitted concurrently with the issue fee and responds to the Notice of Allowance mailed Oct 5, 2015 in the above-identified application. Applicant respectfully requests entry of the following remarks in the record and entry of the following claim amendments pursuant to 37 C.F.R. § 1.312.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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P.O. Box 1450
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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23446 7590 10/05/2015
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission via EFS
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Chad M. Gilles	(Depositor's name)
/Chad M. Gilles/	(Signature)
October 26, 2015	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/614,543	02/05/2015	Madhukar Reddy	28427US04	5785

TITLE OF INVENTION: WIDEBAND TUNER ARCHITECTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	01/05/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
JACKSON, BLANE J	2649	455-207000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 McAndrews, Held & Malloy, Ltd.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: MaxLinear, Inc.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Carlsbad, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 13-0017 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Chad M. Gilles/ Date October 26, 2015
Typed or printed name Chad M. Gilles Registration No. 60,590

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Attorney Docket No. 28427US04)

In the Application of:	
	Madhukar Reddy
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AMENDMENT UNDER 37 C.F.R. § 1.312

This paper is submitted concurrently with the issue fee and responds to the Notice of Allowance mailed Oct 5, 2015 in the above-identified application. Applicant respectfully requests entry of the following remarks in the record and entry of the following claim amendments pursuant to 37 C.F.R. § 1.312.

LISTING OF CLAIMS

1. (Original) A wideband receiver system comprising:

a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

digital circuitry configured to:

select said plurality of desired television channels from said digitized plurality of frequencies; and

output said selected plurality of television channels to a demodulator as a digital datastream.

2. (Original) The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface.

3. (Original) The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface.

4. (Original) The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.

5. (Currently Amended) The wideband receiver system of claim 1, wherein said [[a]] wideband analog-to-digital converter comprises:

a first ADC configured to generate a digital in-phase signal; and

a second ADC configured to generate a digital quadrature signal.

6. (Currently Amended) The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.

7. (Currently Amended) The wideband receiver system f claim 6, wherein:

prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and

after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.

8. (Original) The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.

9. (Original) The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter.

10. (Currently Amended) The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels.

11. (Original) A method comprising:

in a wideband receiver system:

downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and

outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.

12. (Original) The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface.

13. (Original) The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface.

14. (Original) The method of claim 11, comprising:

generating, by a first mixer of said mixer module, an in-phase signal; and

generating, by a second mixer of said mixer module, a quadrature signal.

15. (Original) The method of claim 11, comprising:

generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and

generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.

16. (Currently Amended) The method of claim 15, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry.

17. (Currently Amended) The method of claim 16, wherein:

prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and

after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum.

18. (Original) The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.

19. (Original) The method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter.

20. (Currently Amended) The method of claim 11, comprising decimating, by said digital circuitry, one or more of said selected plurality of desired television channels prior to said outputting of said selected plurality of television channels.

REMARKS

In the Notice of Allowance, claims 1–20 were allowed. The Applicant thanks the Examiner for positive consideration of the claims. By this correspondence, claims 5–7, 10, 16–17, and 20 amended. The Applicant does not believe the above claim amendments should have any impact on the allowability of the claim since the amendments merely clarify the antecedent basis for certain claim terms.

Regarding the Examiner's reasons for allowance, the Applicant does not agree or disagree with the specific reasons for allowance set forth by the Examiner in the Notice of Allowance, and respectfully asserts that the allowability of the claims is based upon the features of the claims and the totality of the record. Applicant reserves the right to traverse the Examiner's stated reasons and/or to argue other reasons to support allowance of the claims, should the need arise in the future.

Respectfully submitted,

Dated: Oct 26, 2015

By: /Chad M. Gilles/
Chad M. Gilles
Reg. No. 60,590

McAndrews, Held & Malloy, Ltd.
500 West Madison Street - Ste. 3400
Chicago, Illinois 60661
(312) 775-8000

Electronic Patent Application Fee Transmittal

Application Number:	14614543
Filing Date:	05-Feb-2015
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
First Named Inventor/Applicant Name:	Madhukar Reddy
Filer:	Chad M. Gilles/Laura Foley
Attorney Docket Number:	28427US04

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt	
EFS ID:	23883899
Application Number:	14614543
International Application Number:	
Confirmation Number:	5785
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
First Named Inventor/Applicant Name:	Madhukar Reddy
Customer Number:	23446
Filer:	Chad M. Gilles/Laura Foley
Filer Authorized By:	Chad M. Gilles
Attorney Docket Number:	28427US04
Receipt Date:	26-OCT-2015
Filing Date:	05-FEB-2015
Time Stamp:	09:14:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
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Payment was successfully received in RAM	$960
RAM confirmation Number	7721
Deposit Account	130017
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	28427US04_issue_fee_transmittal.pdf	1064924 ae7ffcd07015577c7c1970a81843a8c92bbe4ee6	no	1
Warnings:					
Information:					
2		28427US04_312_amendment_.pdf	39944 45b3b82582d702ca749852f609ba1701b5af7a99	yes	6

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment after Notice of Allowance (Rule 312)	1	1
Claims	2	5
Applicant Arguments/Remarks Made in an Amendment	6	6

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30577 4ade398e6af89b19e63491f3604c21aeddcfefa7	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1135445		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

23446 7590 10/05/2015

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER
JACKSON, BLANE J

ART UNIT	PAPER NUMBER
2649	

DATE MAILED: 10/05/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/614,543	02/05/2015	Madhukar Reddy	28427US04	5785

TITLE OF INVENTION: WIDEBAND TUNER ARCHITECTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	01/05/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

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HOW TO REPLY TO THIS NOTICE:

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If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

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23446 7590 10/05/2015
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500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

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Certificate of Mailing or Transmission
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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/614,543	02/05/2015	Madhukar Reddy	28427US04	5785

TITLE OF INVENTION: WIDEBAND TUNER ARCHITECTURE

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nonprovisional	SMALL	$480	$0	$0	$480	01/05/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
JACKSON, BLANE J	2649	455-207000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
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NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/614,543	02/05/2015	Madhukar Reddy	28427US04	5785

23446 7590 10/05/2015

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500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
JACKSON, BLANE J	

ART UNIT	PAPER NUMBER
2649	

DATE MAILED: 10/05/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/614,543	Applicant(s) REDDY ET AL.	
	Examiner BLANE J. JACKSON	Art Unit 2649	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the RCE filed 11 September 2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 11 September 2015 has been entered.

Information Disclosure Statement

The Information Disclosure Statement filed 11 September 2015 is made of record.

Allowable Subject Matter

Claims 1-20 are allowed. The following is a statement of reasons for the indication of allowable subject matter: the Information Disclosure Statement filed with the RCE on 11 September 2015 did not present prior art that comprises the inventive claimed subject matter.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BLANE J. JACKSON whose telephone number is (571)272-7890. The examiner can normally be reached on Monday through Friday, 8:30 AM-5:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BLANE J JACKSON/
Primary Examiner, Art Unit 2649

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"6992855".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 11:35
L2	3	"7095454".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 11:36
L3	3	"7167694".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 11:37
L4	2	"7362178".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 11:40
L5	2	"7373125".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 11:41
L6	2	"7421259".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 11:44
L7	3	"8285240".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 11:45
L8	2	"8374568".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 12:01
L9	2	"8374569".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 12:02
L10	2	"8374570".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 12:02
L11	4	"8526898".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 12:03
L12	2	"8577319".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 12:03
L13	3	"8666350".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 12:04
L14	7	"8909187".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 12:05
L15	3	"9059672".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 12:05
L16	4	"20070042742"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 12:06
L17	42	Reddy-Madhukar.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 12:07
S1	7	"6906498".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/16 09:24

9/16/2015 12:08:42 PM

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14614543	REDDY ET AL.
	Examiner	**Art Unit**
	BLANE J JACKSON	2649

CPC						
Symbol					**Type**	**Version**
H04N		5	/	50	F	2013-01-01
H04B		1	/	0014	I	2013-01-01
H04N		21	/	4263	I	2013-01-01
H04N		21	/	4383	I	2013-01-01
H04N		21	/	454	I	2013-01-01
H04N		21	/	6193	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/BLANE J JACKSON/ Primary Examiner.Art Unit 2649	09/16/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

U.S. Patent and Trademark Office — Part of Paper No. 20150916

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14614543	REDDY ET AL.
	Examiner	**Art Unit**
	BLANE J JACKSON	2649

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
455	207	H	0	4	B	1 / 16 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
455	214				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/BLANE J JACKSON/ Primary Examiner.Art Unit 2649	09/16/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14614543	REDDY ET AL.
	Examiner	**Art Unit**
	BLANE J JACKSON	2649

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
3	3	19	19												
4	4	20	20												
5	5														
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11	11														
12	12														
13	13														
14	14														
15	15														
16	16														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/BLANE J JACKSON/ Primary Examiner.Art Unit 2649	09/16/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

U.S. Patent and Trademark Office

Part of Paper No. 20150916

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14614543	REDDY ET AL.
	Examiner	Art Unit
	BLANE J JACKSON	2649

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
H04B 1/16	05/08/15	BJJ

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
455	131, 140, 207, 214, 313, 315, 323, 324, 325, 334	05/08/15	BJJ

SEARCH NOTES		
Search Notes	Date	Examiner
Review of IDS; review of prior art and similar application 14/617,973 to FAOM	05/08/15	BJJ
update search; review of TD to issue	07/30/15	BJJ
The IDS filed with the RCE was reviewed to issue	09/16/15	BJJ

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	no interference listed class/ subclass or symbol/ group	09/16/15	BJJ

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	14614543
	Filing Date	2015-02-05
	First Named Inventor	Madhukar Reddy
	Art Unit	2649
	Examiner Name	JACKSON, Blane J.
	Attorney Docket Number	28427US04

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/B.J./	1	6906498		2005-06-14	Breuch et al.	
/B.J./	2	6992855		2006-01-31	Ehrlich	
/B.J./	3	7095454		2006-08-22	Waight et al.	
/B.J./	4	7167694		2007-01-23	Khoini-Poorfard et al.	
/B.J./	5	7362178		2008-04-22	Montemayor et al.	
/B.J./	6	7373125		2008-05-13	Godambe et al.	
/B.J./	7	7421259		2008-09-02	Gomez et al.	
/B.J./	8	8285240		2012-10-09	Seendripu et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14614543 14614543 - GAU: 2649
	Filing Date	2015-02-05
	First Named Inventor	Madhukar Reddy
	Art Unit	2649
	Examiner Name	JACKSON, Blane J.
	Attorney Docket Number	28427US04

/B.J./	9	8374568		2013-02-12	Seendripu et al.	
/B.J./	10	8374569		2013-02-12	Seendripu et al.	
/B.J./	11	8374570		2013-02-12	Seendripu et al.	
/B.J./	12	8526898		2013-09-03	Reddy et al.	
/B.J./	13	8577319		2013-11-05	Ling et al.	
/B.J./	14	8666350		2014-03-04	Vauhkonen	
/B.J./	15	8909187		2014-12-09	Seendripu et al.	
/B.J./	16	9059672		2015-06-16	Ling et al.	

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/B.J./	1	20050040909	A1	2005-02-24	Waight et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14614543 14614543 - GAU: 2649
	Filing Date	2015-02-05
	First Named Inventor	Madhukar Reddy
	Art Unit	2649
	Examiner Name	JACKSON, Blane J.
	Attorney Docket Number	28427US04

/B.J./	2	20070042742	A1	2007-02-22	Kim et al.		

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	1							☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/B.J./	1	JEFFREY A. WELDON, et al. "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter With Harmonic-Rejection Mixers, IEEE Journal of Solid-State Circuits, December 2001, pages: 2003-2015, Vol. 36, No. 12, Seattle, Washington.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Blane Jackson/	Date Considered	09/16/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14614543 14614543 - GAU: 2649
	Filing Date	2015-02-05
	First Named Inventor	Madhukar Reddy
	Art Unit	2649
	Examiner Name	JACKSON, Blane J.
	Attorney Docket Number	28427US04

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Chad M. Gilles/	Date (YYYY-MM-DD)	2015-09-11
Name/Print	Chad M. Gilles	Registration Number	60590

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

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Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	14614543	Filing Date	2015-02-05	Docket Number (if applicable)	28427US04	Art Unit	2649
First Named Inventor	Madhukar Reddy			Examiner Name	JACKSON, Blane J.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 130017

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Chad M. Gilles/	Date (YYYY-MM-DD)	2015-09-11
Name	Chad M. Gilles	Registration Number	60590

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	14614543
	Filing Date	2015-02-05
	First Named Inventor	Madhukar Reddy
	Art Unit	2649
	Examiner Name	JACKSON, Blane J.
	Attorney Docket Number	28427US04

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6906498		2005-06-14	Breuch et al.	
	2	6992855		2006-01-31	Ehrlich	
	3	7095454		2006-08-22	Waight et al.	
	4	7167694		2007-01-23	Khoini-Poorfard et al.	
	5	7362178		2008-04-22	Montemayor et al.	
	6	7373125		2008-05-13	Godambe et al.	
	7	7421259		2008-09-02	Gomez et al.	
	8	8285240		2012-10-09	Seendripu et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Attorney Docket Number	28427US04

	9	8374568		2013-02-12	Seendripu et al.	
	10	8374569		2013-02-12	Seendripu et al.	
	11	8374570		2013-02-12	Seendripu et al.	
	12	8526898		2013-09-03	Reddy et al.	
	13	8577319		2013-11-05	Ling et al.	
	14	8666350		2014-03-04	Vauhkonen	
	15	8909187		2014-12-09	Seendripu et al.	
	16	9059672		2015-06-16	Ling et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050040909	A1	2005-02-24	Waight et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14614543
	Filing Date	2015-02-05
	First Named Inventor	Madhukar Reddy
	Art Unit	2649
	Examiner Name	JACKSON, Blane J.
	Attorney Docket Number	28427US04

	2	20070042742	A1	2007-02-22	Kim et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	JEFFREY A. WELDON, et al. "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter With Harmonic-Rejection Mixers, IEEE Journal of Solid-State Circuits, December 2001, pages: 2003-2015, Vol. 36, No. 12, Seattle, Washington.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14614543
	Filing Date	2015-02-05
	First Named Inventor	Madhukar Reddy
	Art Unit	2649
	Examiner Name	JACKSON, Blane J.
	Attorney Docket Number	28427US04

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Chad M. Gilles/	Date (YYYY-MM-DD)	2015-09-11
Name/Print	Chad M. Gilles	Registration Number	60590

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	14614543
Filing Date:	05-Feb-2015
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
First Named Inventor/Applicant Name:	Madhukar Reddy
Filer:	Chad M. Gilles/Julia Villarreal
Attorney Docket Number:	28427US04

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for Continued Examination	2801	1	600	600
		Total in USD ($)		**600**

Electronic Acknowledgement Receipt	
EFS ID:	23473533
Application Number:	14614543
International Application Number:	
Confirmation Number:	5785
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
First Named Inventor/Applicant Name:	Madhukar Reddy
Customer Number:	23446
Filer:	Chad M. Gilles/Julia Villarreal
Filer Authorized By:	Chad M. Gilles
Attorney Docket Number:	28427US04
Receipt Date:	11-SEP-2015
Filing Date:	05-FEB-2015
Time Stamp:	18:38:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$600
RAM confirmation Number	5709
Deposit Account	130017
Authorized User	GILLES, CHAD
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	28427US04_Request_for_Continued_Examination_sb30.pdf	697607 bde283d5d6b32b9da5d830d33f6aceade3351584	no	3
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	28427US04_IDS__sb08a_EFS-WEB.pdf	613115 06650c3fde3f01c5ad52cfc3493817e7c6a3d92a	no	5
Warnings:					
Information:					
3	Non Patent Literature	NPL1_Weldon_Article.pdf	1970159 93b8c9066e2cd9443818c07aaf7824194c53cc58	no	14
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30544 6b43f86ab2f28e16a4f3d9f093260c55218fd43c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3311425		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

23446 7590 08/07/2015

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER
JACKSON, BLANE J

ART UNIT	PAPER NUMBER
2649	

DATE MAILED: 08/07/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/614,543	02/05/2015	Madhukar Reddy	28427US04	5785

TITLE OF INVENTION: WIDEBAND TUNER ARCHITECTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	11/09/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23446 7590 08/07/2015
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/614,543	02/05/2015	Madhukar Reddy	28427US04	5785

TITLE OF INVENTION: WIDEBAND TUNER ARCHITECTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	11/09/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
JACKSON, BLANE J	2649	348-731000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/614,543	02/05/2015	Madhukar Reddy	28427US04	5785

23446 7590 08/07/2015

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
JACKSON, BLANE J	

ART UNIT	PAPER NUMBER
2649	

DATE MAILED: 08/07/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/614,543	Applicant(s) REDDY ET AL.	
	Examiner BLANE J. JACKSON	Art Unit 2649	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the TD filed 15 May 2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Terminal Disclaimer

The terminal disclaimer filed on 15 May 2015 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US 8,526,898 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowable Subject Matter

Claims 1-20 are allowed. The following is a statement of reasons for the indication of allowable subject matter: the prior art made of record teach a wideband receiver system but do not also teach digital circuitry configured to select a plurality of desired television channels from the digitized plurality of frequencies and output said plurality of television channels to a demodulator as a digital datastream.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BLANE J. JACKSON whose telephone number is (571)272-7890. The examiner can normally be reached on Monday through Friday, 8:30 AM-5:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BLANE J JACKSON/
Primary Examiner, Art Unit 2649

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	"8526898".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/30 10:23
L2	41	Reddy-Madhukar.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/30 11:18

7/30/2015 11:20:12 AM

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14614543	REDDY ET AL.
	Examiner	**Art Unit**
	BLANE J JACKSON	2649

CPC						
Symbol					**Type**	**Version**
H04N		21	/	4263	F	2013-01-01
H04B		1	/	0014	I	2013-01-01
H04N		5	/	50	I	2013-01-01
H04N		21	/	4383	I	2013-01-01
H04N		21	/	454	I	2013-01-01
H04N		21	/	6193	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/BLANE J JACKSON/ Primary Examiner.Art Unit 2649	07/30/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

U.S. Patent and Trademark Office — Part of Paper No. 20150730

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14614543	REDDY ET AL.
	Examiner	**Art Unit**
	BLANE J JACKSON	2649

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
455	207	H	0	4	B	1 / 16 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
455	214				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/BLANE J JACKSON/ Primary Examiner.Art Unit 2649	07/30/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14614543	REDDY ET AL.
	Examiner	**Art Unit**
	BLANE J JACKSON	2649

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
3	3	19	19												
4	4	20	20												
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9	9														
10	10														
11	11														
12	12														
13	13														
14	14														
15	15														
16	16														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/BLANE J JACKSON/ Primary Examiner.Art Unit 2649	07/30/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

U.S. Patent and Trademark Office

Part of Paper No. 20150730

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14614543	REDDY ET AL.
	Examiner	Art Unit
	BLANE J JACKSON	2649

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
H04B 1/16	05/08/15	BJJ

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
455	131, 140, 207, 214, 313, 315, 323, 324, 325, 334	05/08/15	BJJ

SEARCH NOTES		
Search Notes	Date	Examiner
Review of IDS; review of prior art and similar application 14/617,973 to FAOM	05/08/15	BJJ
update search; review of TD to issue	07/30/15	BJJ

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	no interference listed class/ subclass or symbol/ group	07/30/15	BJJ

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/614,543	02/05/2015	Madhukar Reddy	28427US04

CONFIRMATION NO. 5785

23446
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

PUBLICATION NOTICE

OC000000075549784

Title:WIDEBAND TUNER ARCHITECTURE

Publication No.US-2015-0156535-A1
Publication Date:06/04/2015

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Attorney Docket No. 28427US04)

In the Application of:	
	Madhukar Reddy et al.
Serial No.:	14/614,543
Filed:	February 5, 2015
Title:	WIDEBAND TUNER ARCHITECTURE
Examiner:	JACKSON, Blane J.
Art Unit:	2649
Confirmation No.:	5785
Customer No.:	23446

RESPONSE UNDER 37 C.F.R. § 1.111

This paper responds to the non-final office action mailed May 14, 2015 ("Office Action") in the above-identified application ("Instant Application"). The only rejections outstanding are obviousness type double patenting rejections, which are obviated by the e-terminal disclaimer submitted herewith.

A Notice of Allowance is courteously solicited.

Respectfully submitted,

Date: May 15, 2015

/Chad M. Gilles/
Chad M. Gilles
Registration No. 60,590
Representative for Applicant

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
(312) 775-8000

Electronic Acknowledgement Receipt

EFS ID:	22358195
Application Number:	14614543
International Application Number:	
Confirmation Number:	5785
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
First Named Inventor/Applicant Name:	Madhukar Reddy
Customer Number:	23446
Filer:	Chad M. Gilles/Laura Foley
Filer Authorized By:	Chad M. Gilles
Attorney Docket Number:	28427US04
Receipt Date:	15-MAY-2015
Filing Date:	05-FEB-2015
Time Stamp:	12:49:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	28427US04_OA_14MAY2015_Response_with_eterminal_discl.pdf	14297 9cf5a11c2b5cc6e9fbc3a864f6af2505b4e2ba0a	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	14297

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	14614543
Filing Date	05-Feb-2015
First Named Inventor	Madhukar Reddy
Attorney Docket Number	28427US04
Title of Invention	WIDEBAND TUNER ARCHITECTURE

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
MaxLinear, Inc.	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

8526898

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.	
Applicant claims the following fee status: ◉ Small Entity ○ Micro Entity ○ Regular Undiscounted I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.	
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application Registration Number 60590 ○ A sole inventor ○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ○ A joint inventor; all of whom are signing this request	
Signature	/Chad M. Gilles/
Name	Chad M. Gilles

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	14614543
Filing Date:	05-Feb-2015
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
First Named Inventor/Applicant Name:	Madhukar Reddy
Filer:	Chad M. Gilles/Laura Foley
Attorney Docket Number:	28427US04

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Statutory or Terminal Disclaimer	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 14614543

Filing Date: 05-Feb-2015

Applicant/Patent under Reexamination: Reddy et al.

Electronic Terminal Disclaimer filed on May 15, 2015

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt	
EFS ID:	22358248
Application Number:	14614543
International Application Number:	
Confirmation Number:	5785
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
First Named Inventor/Applicant Name:	Madhukar Reddy
Customer Number:	23446
Filer:	Chad M. Gilles/Laura Foley
Filer Authorized By:	Chad M. Gilles
Attorney Docket Number:	28427US04
Receipt Date:	15-MAY-2015
Filing Date:	05-FEB-2015
Time Stamp:	12:54:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$160
RAM confirmation Number	9069
Deposit Account	130017
Authorized User	GILLES, CHAD
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Electronic Terminal Disclaimer-Filed	eTerminal-Disclaimer.pdf	33450 a5bab44ea054ea04a04a5edbb4fb6047012 1287b	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30276 1c2b7f4c2e62ae5e1dbaae9f5c94a098caf7 7eb7	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	63726		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/614,543	02/05/2015	Madhukar Reddy	28427US04	5785

23446 7590 05/14/2015
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
JACKSON, BLANE J	

ART UNIT	PAPER NUMBER
2649	

NOTIFICATION DATE	DELIVERY MODE
05/14/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mhmpto@mcandrews-ip.com

Office Action Summary	Application No. 14/614,543	Applicant(s) REDDY ET AL.	
	Examiner BLANE J. JACKSON	Art Unit 2649	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *02 May 2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Information Disclosure Statement

The Information Disclosure Statement filed 10 February 2015 is made of record.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory

double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-27 of U.S. Patent No. 8,526,898. Although the claims at issue are not identical, they are not patentably distinct from each other because the instant application comprises claims which are broad in scope and with the same or fewer claim elements than the claims of the parent patent.

Conclusion

With respect to the preceding rejection, the claims as filed comprise potentially allowable subject matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BLANE J. JACKSON whose telephone number is

(571)272-7890. The examiner can normally be reached on Monday through Friday, 8:30 AM-5:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BLANE J JACKSON/
Primary Examiner, Art Unit 2649

Notice of References Cited	Application/Control No. 14/614,543	Applicant(s)/Patent Under Reexamination REDDY ET AL.	
	Examiner BLANE J. JACKSON	Art Unit 2649	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,526,898	09-2013	Reddy et al.	455/207
*	B	US-7,599,673	10-2009	Maxim et al.	455/179.1
*	C	US-5,280,636	01-1994	Kelley et al.	455/131
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	14614543
	Filing Date	2015-02-05
	First Named Inventor	Madhukar Reddy
	Art Unit	
	Examiner Name	
	Attorney Docket Number	28427US04

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/B.J./	1	8300681	B2	2012-10-30	Petrovic et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/B.J./	1	20070111661	A1	2007-05-17	Bargroff et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
/B.J./	1	2087623	EP	A2	2009-08-12	RF Magic Inc.		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

Receipt date: 02/10/2015	Application Number	14614543	14614543 - GAU: 2649
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2015-02-05	
	First Named Inventor	Madhukar Reddy	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	28427US04	

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/Blane Jackson/	Date Considered	05/08/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

Receipt date: 02/10/2015	Application Number	14614543	14614543 - GAU: 2649
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2015-02-05	
	First Named Inventor	Madhukar Reddy	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	28427US04	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Chad M. Gilles/	Date (YYYY-MM-DD)	2015-02-10
Name/Print	Chad M. Gilles	Registration Number	60590

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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BIB DATA SHEET

CONFIRMATION NO. 5785

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/614,543	02/05/2015	348	2649	28427US04

APPLICANTS

MaxLinear, Inc., Carlsbad, CA, Assignee (with 37 CFR 1.172 Interest);

INVENTORS

Madhukar Reddy, Carlsbad, CA;
Curtis Ling, Carlsbad, CA;
Tim Gallagher, Carlsbad, CA;

**** CONTINUING DATA ***************************

This application is a CON of 13/962,871 08/08/2013
which is a CON of 12/762,900 04/19/2010 PAT 8526898
which claims benefit of 61/170,526 04/17/2009

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
02/19/2015

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /BLANE J JACKSON/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	10	20	2

ADDRESS

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661
UNITED STATES

TITLE

WIDEBAND TUNER ARCHITECTURE

FILING FEE RECEIVED		
730	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14614543	REDDY ET AL.
	Examiner	Art Unit
	BLANE J JACKSON	2649

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
H04B 1/16	05/08/15	BJJ

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
455	131, 140, 207, 214, 313, 315, 323, 324, 325, 334	05/08/15	BJJ

SEARCH NOTES		
Search Notes	Date	Examiner
Review of IDS; review of prior art and similar application 14/617,973 to FAOM	05/08/15	BJJ

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14614543	REDDY ET AL.
	Examiner	**Art Unit**
	BLANE J JACKSON	2649

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/08/2015								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
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	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	15	"8300681".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/08 17:41
L2	4	"20070111661"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/08 17:42
L3	34	"2087623"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/08 17:42
L4	7	Reddy-Madhukar.in. and wideband adj3 receiver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/08 17:44

5/8/2015 5:45:04 PM

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500 WEST MADISON STREET
SUITE 3400
CHICAGO IL 60661

MAILED
MAR 05 2015
OFFICE OF PETITIONS

Doc Code: TRACK1.GRANT

Decision Granting Request for Prioritized Examination (Track I or After RCE)	Application No.: 14/614,543

1. THE REQUEST FILED February 05, 2015 IS **GRANTED.**

The above-identified application has met the requirements for prioritized examination

A. ☒ for an original nonprovisional application (Track I).
B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination.** The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:

A. filing a **petition for extension of time** to extend the time period for filing a reply;
B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims**, or a multiple dependent claim;
C. filing a **request for continued examination**;
D. filing a notice of appeal;
E. filing a request for suspension of action;
F. mailing of a notice of allowance;
G. mailing of a final Office action;
H. completion of examination as defined in 37 CFR 41.102; or
I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to **Michelle R. Eason** at (571) 272-4231.

In his/her absence, calls may be directed to Brian W. Brown at (571) 272-5338.

/Michelle R. Eason/
(*Signature*)

Paralegal Specialist, Office of Petitions
(Title)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Attorney Docket No. 28427US04

In the Application of:	
Madhukar Reddy, et al.	
Serial No.:	14/614,543
Filed:	February 5, 2015
Title:	WIDEBAND TUNER ARCHITECTURE
Group Art Unit:	2631
Confirmation No.:	5785
Customer No.:	23446

PRELIMINARY AMENDMENT

Applicant submits this Preliminary Amendment in connection with the above-identified continuation application ("Instant Application").

I. CONTENTS OF THIS CORRESPONDENCE

Amendments to the specification begin on page 2.

Amendments to the Specification:

A. Please replace paragraph [0001] with the following amended paragraph:

[0001] This application is a continuation of U.S. patent application 13/962,871 filed on August 08, 2013, which is a continuation of U.S. patent application 12/762,900 filed on April ~~14~~ 19, 2010 (now U.S. Patent 8,526,898), which claims the benefit of priority to U.S. provisional application 61/170,526 filed April 17, 2009, now expired. Each of the above referenced documents is hereby incorporated by reference in its entirety.

The Commissioner is hereby authorized to charge any fees required by this submission including any extra claims fees, to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

Date: February 26, 2015

/Chad M. Gilles /
Chad M. Gilles
Reg. No. 60,590

McAndrews, Held & Malloy, Ltd.
500 W. Madison Street - Suite 3400
Chicago, Illinois 60661
(312)-775-8000

Electronic Acknowledgement Receipt

EFS ID:	21606260
Application Number:	14614543
International Application Number:	
Confirmation Number:	5785
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
First Named Inventor/Applicant Name:	Madhukar Reddy
Customer Number:	23446
Filer:	Chad M. Gilles/Laura Foley
Filer Authorized By:	Chad M. Gilles
Attorney Docket Number:	28427US04
Receipt Date:	26-FEB-2015
Filing Date:	05-FEB-2015
Time Stamp:	12:07:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		28427US04_Prelim_Amendment.pdf	21005 2c047aef2d2022c9ba4f22e22ff9479042bf50cc	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Specification	2	2
Warnings:			
Information:			
	Total Files Size (in bytes):	21005	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/614,543	02/05/2015	2631	730	28427US04	20	2

CONFIRMATION NO. 5785

23446
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

FILING RECEIPT

OC000000073501362

Date Mailed: 02/25/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Madhukar Reddy, Carlsbad, CA;
Curtis Ling, Carlsbad, CA;
Tim Gallagher, Carlsbad, CA;

Applicant(s)

MaxLinear, Inc., Carlsbad, CA

Power of Attorney: The patent practitioners associated with Customer Number 23446

Domestic Priority data as claimed by applicant

This application is a CON of 13/962,871 08/08/2013
which is a CON of 12/762,900 04/19/2010 PAT 8526898
which claims benefit of 61/170,526 04/17/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 02/19/2015
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/614,543**
Projected Publication Date: 06/04/2015

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

WIDEBAND TUNER ARCHITECTURE

Preliminary Class

375

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/614,543

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*	x 40 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	730		TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	14614543
	Filing Date	2015-02-05
	First Named Inventor	Madhukar Reddy
	Art Unit	
	Examiner Name	
	Attorney Docket Number	28427US04

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8300681	B2	2012-10-30	Petrovic et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						Add

U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20070111661	A1	2007-05-17	Bargroff et al.	
If you wish to add additional U.S. Published Application citation information please click the Add button.						Add

FOREIGN PATENT DOCUMENTS								Remove
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2087623	EP	A2	2009-08-12	RF Magic Inc.		☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								Add

NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14614543
	Filing Date	2015-02-05
	First Named Inventor	Madhukar Reddy
	Art Unit	
	Examiner Name	
	Attorney Docket Number	28427US04

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14614543
	Filing Date	2015-02-05
	First Named Inventor	Madhukar Reddy
	Art Unit	
	Examiner Name	
	Attorney Docket Number	28427US04

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Chad M. Gilles/	Date (YYYY-MM-DD)	2015-02-10
Name/Print	Chad M. Gilles	Registration Number	60590

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Espacenet

Bibliographic data: EP2087623 (A2) — 2009-08-12

SATELLITE SIGNAL FREQUENCY TRANSLATION AND STACKING

Inventor(s): PETROVIC BRANISLAV [US]; HANCOCK DALE [US]; GOLDBLATT JEREMY [US]; BARGROFF KEITH [US] ± (PETROVIC, BRANISLAV, ; HANCOCK, DALE, ; GOLDBLATT, JEREMY, ; BARGROFF, KEITH)

Applicant(s): R F MAGIC INC [US] ± (R.F. MAGIC INC, ; RF MAGIC, INC)

Classification: **- international:** ***H03J1/00; H04B1/28; H04H40/90***
- cooperative: **H04B1/28**; **H04H40/90**

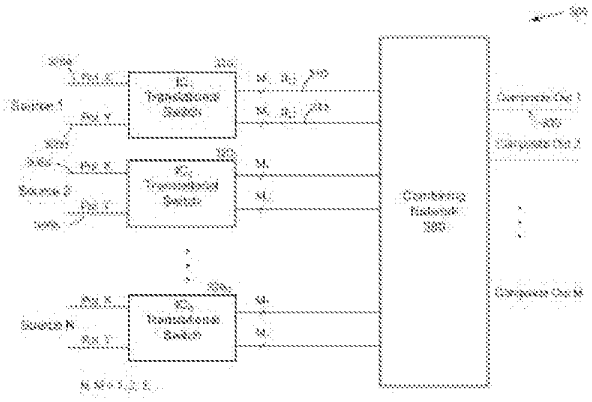
Application number: EP20070870121 20071231

Priority number(s): WO2007US89192 20071231 ; US20060864352P 20061103 ; US20070885814P 20070119 ; US20070886933P 20070128

Also published as: EP2087623 (B1) US2008112385 (A1) US2012099623 (A1) US8892026 (B2) WO2008064371 (A2) more

Abstract not available for EP2087623 (A2)
Abstract of corresponding document: US2008112385 (A1)

Circuits, systems, and methods for assembling a composite signal include a frequency translation circuit coupled to receive an input signal and operable to generate a plurality of frequency-translated versions of the input signal at a respective plurality of different frequencies, the plurality of frequency-translated input signals defining a group of frequency translated signals. The plurality of frequency translated signals may each be processed to provide a composite signal.



(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Veröffentlichungsnummer:
(11) Publication number: **EP 2 087 623 A0**
(11) Numéro de publication:

Internationale Anmeldung veröffentlicht durch die Weltorganisation für geistiges Eigentum unter der Nummer:

WO 2008/064371 (Art. 153(3) EPÜ).

International application published by the World Intellectual Property Organization under number:

WO 2008/064371 (Art. 153(3) EPC).

Demande internationale publiée par l'Organisation Mondiale de la Propriété Intellectuelle sous le numéro:

WO 2008/064371 (art. 153(3) CBE).

Electronic Acknowledgement Receipt

EFS ID:	21447138
Application Number:	14614543
International Application Number:	
Confirmation Number:	5785
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
First Named Inventor/Applicant Name:	Madhukar Reddy
Customer Number:	23446
Filer:	Chad M. Gilles/Laura Foley
Filer Authorized By:	Chad M. Gilles
Attorney Docket Number:	28427US04
Receipt Date:	10-FEB-2015
Filing Date:	
Time Stamp:	09:58:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	28427US04_IDS__sb08a_EFS-WEB.pdf	612298 bd13fe91bf17a2e635f435e0e2221e015aeb7033	no	4

Warnings:	
Information:	

2	Foreign Reference	EP2087623A2.pdf	112213 112c7af198fa095a19b1da28e1827b7e61c79aef	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	724511

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New Applications Under 35 U.S.C. 111
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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: TRACK1.REQ
Document Description: TrackOne Request

PTO/AIA/424 (04-14)

CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION UNDER 37 CFR 1.102(e) (Page 1 of 1)

First Named Inventor:	Madhukar Reddy	Nonprovisional Application Number (if known):	
Title of Invention:	WIDEBAND TUNER ARCHITECTURE		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently $0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.

2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.

3. The applicable box is checked below:

I. ☑ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.

---OR---

(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.

ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, **or** the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

i. A request for continued examination has been filed with, or prior to, this form.
ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Chad M. Gilles/	Date February 5, 2015
Name (Print/Typed) Chad M. Gilles	Practitioner Registration Number 60,590

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.**

☑ *Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US04
	Application Number	
Title of Invention	WIDEBAND TUNER ARCHITECTURE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Madhukar		Reddy	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Carlsbad	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	2051 Palomar Airport Rd.		
Address 2	Ste. 100		
City	Carlsbad	State/Province	CA
Postal Code	92011	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Curtis		Ling	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Carlsbad	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	2051 Palomar Airport Rd.		
Address 2	Ste. 100		
City	Carlsbad	State/Province	CA
Postal Code	92011	Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Tim		Gallagher	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US04
	Application Number	
Title of Invention	WIDEBAND TUNER ARCHITECTURE	

City	Carlsbad	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	2051 Palomar Airport Rd.		
Address 2	Ste. 100		
City	Carlsbad	**State/Province**	CA
Postal Code	92011	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	23446		
Email Address	mhmpto@mcandrews-ip.com	Add Email	Remove Email

Application Information:

Title of the Invention	WIDEBAND TUNER ARCHITECTURE		
Attorney Docket Number	28427US04	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	10	**Suggested Figure for Publication (if any)**	

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country i

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US04
	Application Number	
Title of Invention	WIDEBAND TUNER ARCHITECTURE	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	23446		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	13962871	2013-08-08

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13962871	Continuation of	12762900	2010-04-19	8526898	2013-09-03

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12762900	Claims benefit of provisional	61170526	2009-04-17

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US04
	Application Number	
Title of Invention	WIDEBAND TUNER ARCHITECTURE	

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US04
	Application Number	
Title of Invention	WIDEBAND TUNER ARCHITECTURE	

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(●) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. [X]

Organization Name	MaxLinear, Inc.

Mailing Address Information For Applicant:

Address 1	2051 Palomar Airport Rd.		
Address 2	Ste. 100		
City	Carlsbad	**State/Province**	CA
Country [i]	US	Postal Code	92011
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

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If the Assignee or Non-Applicant Assignee is an Organization check here. [ ]

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	28427US04
	Application Number	
Title of Invention	WIDEBAND TUNER ARCHITECTURE	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Chad M. Gilles/			Date (YYYY-MM-DD)	2015-02-05
First Name	Chad	Last Name	Gilles	Registration Number	60590

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

WIDEBAND TUNER ARCHITECTURE

PRIORITY CLAIM

[0001] This application is a continuation of U.S. patent application 13/962,871 filed on August 08, 2013, which is a continuation of U.S. patent application 12/762,900 filed on April 14, 2010 (now U.S. Patent 8,526,898), which claims the benefit of priority to U.S. provisional application 61/170,526 filed April 17, 2009, now expired. Each of the above referenced documents is hereby incorporated by reference in its entirety.

BACKGROUND

[0002] This invention relates to wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum. In particular, the invention relates to wideband receiver systems that are capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum and grouping them into a contiguous, or substantially-contiguous, frequency spectrum.

[0003] Receivers used to down-convert and selectively filter TV channels are referred to as tuners, and tuners designed to concurrently receive several TV channels are referred to as wideband tuners. Existing tuners for these applications down-convert a swath of channels to an intermediate frequency, which are then sent to a demodulator. Because the swath of channels is not contiguous, this swath includes the desired channels as well as undesired channels. The demodulator employs a high-speed data converter to capture this swath of desired and undesired channels in the digital domain and subsequently filters out the desired channels.

[0004] In general, television channels broadcasted over the air or over cable networks are distributed across a broad frequency spectrum. That is, the channel frequencies may not be adjacent to each other. In certain applications such as DVR and

picture-in-picture, the receiver system may have to concurrently receive several desired channels that may or may not be contiguous. The wideband receiver requirement poses a trade-off to the system to limit either the dynamic range of the wideband tuner or reduce the bandwidth covered by the tuner so that fewer channels may be received and processed by the demodulator.

[0005] FIG. 1 shows a conventional wideband tuner 100. Tuner 100 may be a direct conversion tuner and includes a low noise amplifier LNA1 having an input terminal coupled to a radio frequency (RF) input signal 102 and an output terminal coupled to a mixer M1. The RF signal may include one or more television channels receiving from a cable network via an RF connector or wirelessly via an antenna. The RF input signal may include the VHF and UHF television channels in a terrestrial television broadcasting system or the CATV channels in cable networks. In order to receive all broadcasted channels present in the RF input signal, LNA1 must necessarily have a wide tuning range, high linearity, and low noise. Mixer M1 is coupled to a synthesizer S1 that can generate an oscillator frequency located around the center of the RF signal. Mixer M1 frequency down-converts the received RF input signal to a more convenient intermediate frequency (IF) band. Tuner 100 includes an amplifier V1 having a programmable gain for amplifying the IF signal, which is then band-pass filtered by a filter F1 before outputting to a demodulator.

[0006] In general, the RF signal includes multiple desired channels that are located in non-contiguous portions of a radio frequency spectrum. As shown in FIG. 1, the swath of channels 110 occupies a bandwidth BW1 120 at an RF center frequency f_{rfc} 130. Synthesizer S1 may be tuned to a frequency around the center frequency f_{rfc} 130 for mixing channels 110 to an intermediate frequency f_{ifc} 160, the frequency down-mixed channels 140 are amplified by amplifier V1 and then filtered by F1 to produce a swath of channels 170 centered around frequency f_{ifc} 160. In an exemplary application shown in

FIG. 1, bandwidth BW1 contains 10 channels. In the case where channels are TV channels that are spaced at either 6 MHz or 8 MHz in most parts of the world, bandwidth BW1 120 would span from 60-80 MHz, i.e., the down-converted bandwidth at the intermediate frequency would require a bandwidth equal to at least BW1, or at least 80 MHz when such architecture is used. It is noted that in other applications where the desired RF channels are located in the low band such as channels numbers 2 to 6 (VHF in the terrestrial TV broadcast or CATV) and in the high band such as channels numbers 14 to 83 of the UHF TV broadcast or channel numbers 63-158 of the CATV's ultra band, the bandwidth BW1 can be 800 MHz or higher. This wide bandwidth of 800 MHz would require a very expensive digital processing circuitry such as very high-speed analog to digital conversion and high-speed processor in the demodulator.

[0007] It is desirable to have wideband receiver systems that can increase the dynamic range without requiring expensive data conversion, filtering and channel selection at the demodulator.

BRIEF SUMMARY

[0008] An embodiment of the present invention includes a wideband receiver system that is configured to concurrently receive multiple radio frequency (RF) channels including a number of desired channels that are located in non-contiguous portions of a frequency spectrum and group the desired channels in a contiguous or substantially-contiguous frequency band at an intermediate frequency spectrum, where the term "substantially-contiguous" includes spacing the desired channels close to each other (e.g. as a fraction of the total system bandwidth, or relative to a channel bandwidth) but with a spacing that can be variable to accommodate the needs of overall system. The term "contiguous" heretofore encompasses "substantially-contiguous." The term "spacing" is referred to as the frequency difference between adjacent channels. The system includes a wideband receiver having a complex mixer module for down-shifting the multiple RF channels and transforming them to an in-phase signal and a quadrature signal in the baseband or low intermediate frequency (IF) band. The system further includes a wideband analog-to-digital converter module that digitizes the in-phase and quadrature signals. The digital in-phase and quadrature signals are provided to a digital frontend module that contains a bank of complex mixers that frequency-shift the number of desired channels to a baseband where the desired channels are individually filtered.

[0009] The digital frontend module may also include a decimator module that decimates the desired RF channels by a factor M before demodulating them to a digital data stream.

[0010] In certain embodiments of the present invention, the wideband receiver system additionally includes an up-converter module having multiple complex up-mixers, each of the complex up-mixers is configured to frequency up-shift each one of the desired RF channels to a sub-portion of an IF spectrum, wherein all sub-portions of the desired channels are adjacent to each another and form a contiguous frequency band in the IF

spectrum. The act of frequency shifting the desired channels to the IF spectrum allows the wideband receiver system to directly interface with commercially available demodulators. Allowing the spacing of the desired channels in the contiguous spectrum to be variable allows a system to optimize placement of these desired channels for the purposes of avoiding sensitive portions of the spectrum which may either be vulnerable to spurious signals and interference; or which may generate interference directly or as a harmonic product, to other systems.

[0011] In another embodiment of the present invention, a multi-tuner receiver system having two or more tuners is provided to receive multiple desired RF channels that extend over several non-contiguous sub-portions of a broad frequency spectrum and group them into a contiguous frequency spectrum. The multi-tuner system includes at least a first tuner that processes a first sub-portion of the broad frequency spectrum into a first in-phase signal and a first quadrature signal and a second tuner that processes a second sub-portion of the broad frequency spectrum into a second in-phase signal and a second quadrature signal. The multi-tuner receiver system further includes a first analog-to-digital converter module that digitizes the first in-phase and quadrature signals and a second analog-to-digital converter module that digitizes the second in-phase and quadrature signals. In addition, the multi-tuner system includes a first digital frontend module having a first number of complex mixers corresponding to a first number of the desired RF channels located in the first sub-portion of the broad frequency spectrum and a second digital frontend module having a second number of complex mixers corresponding to a second number of the desired RF channels located in the second sub-portion of the broad frequency spectrum. The first digital frontend module frequency shifts the first number of the desired RF channels to a first plurality of baseband signals and the second digital frontend module frequency shifts the second number of the desired RF channels to a second plurality of baseband signals.

[0012] The multi-tuner system further includes a first up-converter module having a plurality of N complex mixers, wherein N is an integer value equal to the number of desired channel. The first up-converter module frequency up-shifts the first plurality of the baseband signals to a first portion of an intermediate frequency. In addition, the multi-tuner system includes a second up-converter module that frequency up-shifts the second plurality of the baseband signals to a second portion of an intermediate frequency. The first and the second portions of the intermediate frequency are non-overlapping and located adjacent to each other to form a contiguous intermediate frequency (IF) band. The multi-tuner system further includes a digital-to-analog converter that converts the contiguous IF band to an analog waveform signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 is a schematic block diagram of a conventional wideband tuner;

[0014] FIG. 2 is a schematic block diagram of a wideband receiver system according to an embodiment of the present invention;

[0015] FIG. 3 is a simplified circuit diagram of a complex down-mixer according to an embodiment of the present invention;

[0016] FIG. 4 is a simplified schematic block diagram of a wideband receiver system according to another embodiment of the present invention;

[0017] FIG. 5 is a simplified circuit diagram of a complex up-mixer according to an embodiment of the present invention;

[0018] FIG. 6 is a simplified schematic block diagram of a wideband multi-tuner receiver system according to an embodiment of the present invention;

[0019] FIG. 7 is a block diagram illustrating an exemplary digital front end according to an embodiment of the present invention in more detail;

[0020] FIG. 8 is a block diagram illustrating an exemplary tiled up-converter module according to an embodiment of the present invention in more detail;

[0021] FIG. 9 is a simplified block diagram of a wideband multi-tuner receiver system 900 according to an embodiment of the present invention; and

[0022] FIG. 10 is a simplified block diagram of a wideband multi-tuner receiver system 1000 according to another embodiment of the present invention.

DETAILED DESCRIPTION

[0023] FIG. 2 is a schematic block diagram of a wideband receiver system 200 according to an embodiment of the present invention. Wideband receiver system 200 includes a radio front end 210 and a digital front end 230. Radio front end 210 may be a single very wide-band tuner receiver that captures the desired swath of channels located in non-contiguous portions of the spectrum having a frequency bandwidth BW1 120. In this example, the number of available channels in BW1 120 is assumed to be 10 with each channel occupying an 8 MHz bandwidth for a total of 80 MHz. Radio front end 210 is shown as including a low noise amplifier LNA 202 having an input terminal configured to receive an RF input signal 102. In the example shown, RF signal 102 includes four desired RF channels having the respective carrier frequency f_{rf1}, f_{rf2}, f_{rf3}, and f_{rf4} that are located in non-contiguous portions of the wide frequency spectrum BW1. It is understood, however, that spectrum BW1 120 may have any other number of desired frequencies that are not contiguous. LNA 202 has a very low noise figure and very high linearity and a wide tuning range (i.e., very high IIP2 and IIP3 intercept points) to maximize a signal-to-noise-and distortion ratio (SNDR) at the amplifier output. LNA 202 may have a programmable gain to amplify RF signal 102 to adequate voltage levels for mixers M1 211 and M2 221.

[0024] Mixers M1 211 and M2 221 may be conventional mixers formed using, for example, differential Gilbert cells. Each of the mixers 211 and 221 multiplies (mixes) an amplified RF signal 203 with a respective first oscillator frequency signal 205 and a second oscillator frequency signal 207 to generate an in-phase signal 212 and a quadrature signal 222 that have a phase shift of 90° degree between them. Mixers 211 and 221 are identical so that the amplitude of the in-phase signal 212 and quadrature signal 222 are the same. The first and second oscillator frequencies 205 and 207 are identical and have a 90° degree phase shift generated through a 90° degree phase shifter P1 206. Synthesizer S1 may be a single local oscillator operable to generate the oscillator

frequency 205 for converting the receive RF signal 102 to a zero-IF or low-IF band. Synthesizer S1 can be a coarse (large step) phase locked loop. Synthesizer S1 can also be programmable to cover the wideband frequency of the analog and digital terrestrial broadcast and/or the cable television system. The RF signal 102 may have relatively uniform signal strength in a cable network. However, its signal strength may extend in several orders of magnitude in a terrestrial broadcast system, thus, LNA 202 and/or mixers M1 211, M2 221 are required to have a relatively high dynamic range to handle the large variations in the signal strength.

[0025] In-phase signal 212 and quadrature signal 222 are further amplified and filtered by respective amplifiers V1 213, V2 223 and filters F1 215, F2 225 to generate a filtered in-phase signal 216 and a filtered quadrature signal 226. Filters F1 215 and F2 225 may be passive or active low-pass filters to filter out any unwanted frequency components of the signals 214 and 224 before digitizing them for further processing in digital front end 230. It is understood that the in-phase path 216 and the quadrature path 226 must have the same amplitude spectrum and maintain a fixed phase relationship, i.e., amplifiers V1 213, V2 223 and filters F1 215, F2 225 must be substantially identical. Because the two paths 216 and 226 are in quadrature, the spectral components from both positive and negative frequencies can be overlaid so that the bandwidth (cutoff frequency) of filters F1 215 and F2 225 can be one half of the BW1 bandwidth 120.

[0026] Analog-to-digital converters ADC1 218 and ADC2 228 are high-speed (i.e., high sampling rate) converters to maximize the dynamic range. In an exemplary application, radio front end 210 operates as a nominal zero-IF down-mixer so that signals 216 and 226 have a nominal bandwidth 290 equal to one half of the RF signal bandwidth BW1 thanks to the complex down-mixer architecture. In other embodiment, radio front end 210 operates as a low-IF down-mixer so that the nominal bandwidth 290 of signals 216 and 226 is greater than one half of the bandwidth BW1. In practice, the sampling rate

of ADC1 218 and ADC2 228 is chosen to be higher than the Nyquist sampling requirement, i.e., the filtered analog quadrature signals 216 and 226 may be over-sampled in order to reduce or avoid aliasing of undesired signals into the digitized I and Q signals.

[0027] ADC1 218 generates a digital signal I 232 that is a digital representation of the analog filtered signal 216; ADC2 228 generates a digital signal Q 242 that is a digital representation of the analog filtered signal 226. Digital signals I 232 and Q 242 are then applied to a bank of N complex mixers 250, wherein N is an integer value corresponding to the number of desired RF channels located in the non-contiguous portions of the frequency spectrum BW1. It is understood that the number N can be any integer value. In one embodiment, N can be equal to the number of all available channels that exist in the licensed frequency spectrum to provide system flexibility. In other embodiments, N can be equal to the number of all receivable channels within a geographic area. In yet another embodiment, N can be an integer value less than the number of receivable channels with the geographic area to reduce system costs. In the exemplary embodiment shown in FIG. 2, the number of desired channels is 4. That is, each of the 4 complex mixers 250 mixes in-phase and quadrature signals 232 and 242 with an associated frequency to generate a corresponding baseband, which is then individually filtered, decimated and provided to an associated demodulator.

[0028] Each of the N complex mixers 250 receives the digital signals I 232 and Q 242 from ADCs 218 and 228 to extract a different one of the desired channels and frequency-shifts the extracted signals to the baseband frequency. Each of the frequency shifted desired channels 252 is filtered by an associated filter module (identified as 260a to 260n). In an embodiment, each of the filtered signals 260a to 260n may be sent directly to an associated demodulator (identified as 270a to 270n) for extracting the original information transmitted in the associated desired channel. In another embodiment, each

of the filtered signals 262a to 262n is further decimated before providing to a demodulator. A path of digital front end 230 is described in more detail below.

[0029] FIG. 3 is a simplified circuit diagram of one of the signal paths 272a to 272n of digital front end 230 shown in FIG. 2 according to an embodiment of the present invention. In an embodiment, digital signal I 232 may be further filtered by a filter 311 to obtain a filtered signal 312. Similarly, digital signal Q 242 may be further filtered by a filter 321 to obtain a filtered signal 322. Thus, digital signals 312 and 322 only contain low-frequency components with undesired high-frequency components being eliminated by respective filters 311 and 321. It is noted that filtered signals 312 and 322 are interposed between the respective ADCs 218, 228 and the bank of N complex mixers 250.

[0030] Mixer 300, which represents one of the N complex mixers 250, includes four multipliers 313, 315, 323, and 325. Multipliers 313 and 315 multiply the filtered signal 312 with respective $\cos(\omega_{ci}t)$ and $\sin(\omega_{ci}t)$ signals and generate respective products 314 and 316. Similarly, multipliers 323 and 325 multiply the filtered Q signal 322 with respective $\cos(\omega_{ci}t)$ and $\sin(\omega_{ci}t)$ signals and generate respective products 324 and 326. An adder 317 sums the products 314 and 326 to generate a frequency-shifted signal I 318. An adder 327 sums the products 324 and 316 to generate a frequency-shifted signal Q 328. Basically, complex mixer 300 causes a frequency shift of the filtered components 312 and 322 to respective baseband signals 318 and 328 in the digital domain according to the operation:

$$Y(t) = X(t) * e^{-j\omega_c t} \quad (1)$$

or taken the Fourier transform, we obtain:

$$Y(\omega)=X(\omega-\omega_c) \quad (2)$$

[0031] Multipliers 313, 315, 323, and 325 are identical digital multipliers. In an embodiment, a numerically controlled oscillator with quadrature output generates the $\cos(\omega_{ci}t)$ and $\sin(\omega_{ci}t)$ signals. Numerically controlled oscillators (NCO) can be implemented using a phase accumulator and a look-up table. NCOs are known to those of skill in the art and will not be described herein. The frequency ω_{ci} is so chosen that each one of the desired channels embedded in the digital signals I 232 and Q 242 will be downshifted to the baseband. In the given example shown in FIG. 2, the bank of N complex mixers will have four complex mixers, each one of the N (i.e., four) complex mixers is coupled to an individual NCO having a distinct frequency ω_{ci} so that when mixing the filtered digital I and Q signals 312 and 322 with that frequency, each one of the complex mixers will generate the signals I (318) and Q (328) of a corresponding one of the desired channels at the baseband.

[0032] In an embodiment, baseband signals 318 and 328 are further individually filtered by respective filters 330 and 340 that are identified as one of the filters 260a-n in FIG. 2. Filters 330 and 340 may be band-pass or low-pass filters having a narrow bandwidth equal to the bandwidth of a desired channel. In certain embodiments, filters 330 and 340 can be analog passive or active low-pass or complex band-pass filters such as polyphase filters. In another embodiment, filters 330 and 340 can be digital low-pass filters, such as finite impulse response (FIR) filters to eliminate high frequency components that may be aliased back to the baseband signals Ii (332) and Qi (342) when decimated by subsequent decimator 350.

[0033] The reduced sampling rate of the N desired baseband channels will be sent as a serial or parallel digital data stream to a demodulator using a serial or parallel data interface according to commonly known methods, as shown in FIG. 2. This approach provides several advantages over conventional tuner architectures. First, it eliminates the need of expensive data conversion, filtering and channel selection on the demodulator

side. Second, it removes undesired channels from the signal path at an early stage, thus relieves the large dynamic range requirement in the demodulator.

[0034] FIG. 4 shows a simplified schematic block diagram of a wideband receiver system 400 according to another embodiment of the present invention. Wideband receiver system 400 includes a radio front end 410, a digital front end 430, a tiled up-conversion module 450, and a summing digital-to-analog converter module DAC 470. Radio front end 410 includes a low noise amplifier LNA1 that receives an RF input signal 102 and provides an amplified RF signal 403 to mixers M1 411 and M2 421. Mixer M1 411 is coupled to an oscillator frequency 405 of a synthesizer S1 whereas mixer M2 421 is coupled with the oscillator frequency 405 via a phase shifter P1 406 that generates a 90° degree phase-shift to the oscillator frequency 405. Mixers M1 411 and M2 421 generate respective in-phase signal 412 and quadrature signal 422 that are further amplified by respective amplifiers V1 413 and V2 423. The amplified in-phase and quadrature signals 414, 424 are then filtered by filters F1 415 and F2 425 to eliminate undesired frequency components that would be aliased back to the in-phase and quadrature signals when digitally sampled by subsequent analog-to-digital converters ADC1 418 and ADC2 428. Digital signals I 422 and Q 442 at the input of digital front end 430 are digital representations of the filtered analog in-phase and quadrature signals 416, 426 before the ADCs. Digital front end 430 include a bank of N complex mixers 432 comprising 432a to 432n identical mixers, where N is an integer value corresponding to the number of the desired channels located in non-contiguous portions of the frequency spectrum. Each of the N complex mixers 432a to 432n frequency down-converts signals I 432 and Q 442 to an associated baseband. Each of the frequency down-converted I and Q signals are coupled to respective low-pass, band-pass, or decimating filters 434. In this regard, the radio front end 410 and the digital front end 430 are similar to respective radio front end 210 and digital front end 230 of FIG. 2 that have been described in detail above.

[0035] In an alternative embodiment of the present invention, the N filtered and decimated channels 438a to 438n (where indices a to n correspond to the associated number of desired channels) are not provided to a demodulator for demodulation. Instead, the N filtered and decimated channels 438a to 438n are further frequency up-converted to an intermediate frequency (IF) spectrum. In order to achieve that, the N filtered and decimated channels are coupled to a tiled up-conversion module 450 that includes a bank of N complex up-mixers, where N is an integer value correspond to the number of desired received channels. The N complex up-mixers include identical digital mixers 452a to 452n that will be described further in detail below with reference to FIG. 5. The N up-shifted channels are then filtered by a subsequent bank of channel filters 454 that, in an embodiment, comprises N individual finite impulse response (FIR) filters. The N filtered channels are then digitally combined and converted to the analog domain by a summing digital-to-analog converter module DAC 470. The N up-shifted channels are adjacent to each other and form a contiguous or substantially-contiguous set of channels 475 in the IF spectrum centered around f_{if} as illustrated in FIG. 4. In an embodiment, the spectra of the mixed products are spaced in such a way so as to avoid overlap with known frequency bands containing potential or actual interferers. In another embodiment, the spectra of the mixed products are spaced in such a way so as to avoid overlap with frequency bands that might introduce interference to other systems. In general, because the bandwidth BW_2 is substantially lower than BW_1, the IF frequency f_{if} can be set proportionally lower, e.g., typically about 16 MHz to accommodate the spectrum of BW2 of up to 32 MHz (corresponding to the total bandwidth of the four desired channels, each having a bandwidth of 8 MHz in this example).

[0036] The up-conversion approach of FIG. 4 provides several advantages over conventional tuner architectures. First, it allows the demodulator to operate the data converter at a lower data rate and with lower resolution (fewer bits) due to the fact that the contiguous channels have a narrower bandwidth. Second, the up-conversion approach

provides full compatibility with existing demodulators that require an analog IF signal. Third, it removes undesired channels from the signal path at an early stage, thus relieves the requirement of a high dynamic range requirement of the demodulator's analog-to-digital converter and the demodulator itself.

[0037] FIG. 5 shows a simplified exemplary circuit diagram of a complex up-mixer 500 according to an embodiment of the present invention. Up-mixer 500 is one of the N complex up-mixers 452a to 452n in tiled up-conversion module 450 shown in FIG. 4. Up-mixer 500 includes filter 510 and 520 configured to eliminate unwanted frequency components present in respective input signals I 501 and Q 502. Filtered signals 512 and 522 are provided to up-mixers UMI 515 and UMQ 525 that multiply the filtered signals 512 and 522 with respective $\cos(\omega_u t)$ and $\sin(\omega_u t)$. The products 516 and 526 are summed in an adder 530 to generate an IF signal 532 according to the following equation:

$$IF(t)=I(t)*\cos(\omega_u t)+Q(t)*\sin(\omega_u t) \qquad (3)$$

[0038] Up-mixers UMI 515 and UMQ 525 are identical digital multipliers that multiply the respective filtered signal 512 and 522 with a cosine function 505 and a sine function 506 that can be generated from a NCO using a digital phase accumulator and a look-up table.

[0039] As described above, TV channels are grouped into multiple frequency bands in North America. For example, channels 2 through 6 are grouped in VHF-low band (aka band I in Europe), channels 7 through 13 in VHF-high band (band III), and channels 14 through 69 in UHF band (bands IV and V). In order to receive such a wide frequency spectrum, the low noise amplifier and mixer must have very low noise, wide tuning range and high linearity as described above in the wideband receiver systems 200 and 400. However, a wideband receiver having a single tuner with high sensitivity may have a high power consumption. For certain applications, it may be advantageous to use multiple tuners that are optimized for a given frequency band, such as a dedicated tuner

for the low VHF band, another dedicated tuner for the high VHF band and the UHF band, and yet other dedicated tuners for receiving the digital video broadcasting (DVB) via satellite (DVB-S), via cable (DVB-C), or terrestrial digital video broadcasting (DVB-T). The multi-tuner approach may also be advantageously applied to cable networks that carry TV programs on an 88 MHz to 860 MHz according to the Data Over Cable Service Interface Specification (DOCSIS) protocol.

[0040] FIG. 6 shows a simplified schematic block diagram of a wideband multi-tuner receiver system 600 according to an embodiment of the present invention. In an embodiment, multi-tuner system 600 includes low noise amplifier A1 602 for receiving an RF input signal 601. Amplifier A1 602 is coupled to at least a tuner1 610 and a tuner2 720. In another embodiment, multi-tuner system 600 may not include amplifier 602 so that RF input signal 601 can be received directly at each tuner 610 and 720.

[0041] Tuner1 610 includes an amplifying filter AF1 613 that filters and amplifies a first portion BWtuner1 604 of a broad frequency spectrum 608 that contains a first plurality of RF channels 606 including desired channels 607 having respective channel frequencies f_{rf1} and f_{rf2}. The first portion of the broad frequency spectrum BWtuner1 604 is then frequency down-converted to a low-IF or zero-IF in-phase signal I1 612 and a quadrature signal Q1 622 through respective mixer M1 611 and M2 621. Signals I1 612 and Q1 622 are further amplified and low-pass filtered before applying to respective analog-to-digital converters ADC1 618 and ADC2 628 that convert analog signals Ia1 616 and Qa1 626 to respective digital in-phase signal Id1 631 and digital quadrature signal Qd1 641. Because tuner1 610 only covers a portion BWtuner1 604 of the entire frequency spectrum 608 having fewer channels, the ADC1 618 and ADC2 628 can be slower-speed analog-to-digital converters with a large number of bits, i.e., large dynamic range.

[0042] Digital signals Id1 631 and Qd1 641 are then provided to a digital front end DFE 630 that includes a first bank of N complex mixers 632 and channel and decimating filters 634. The first bank of N complex filters 632 has N identical complex mixers, where N is an integer value equal to the number of desired channels located in the first portion BWtuner1 604 of the broad frequency spectrum 608. In an embodiment, each one of the first bank of N complex mixers includes four digital mixers that multiply digital stream Id1 631 and Qd1 641 with respective digitized cosine function and sine function to generate the sum and difference frequency components, as shown in FIG. 3. The digitized cosine and sine frequency, i.e., the mixer frequency is so chosen so that when mixing signals Id1 631 and Qd1 641 will move them to a baseband or a low-IF band. In an embodiment, channel and decimating filters have similar structures as filters 330 and 340 and demodulator 350 as shown in FIG. 3. That is, channel and decimating filters include digital low-pass filters 330 and 340 that eliminates unwanted high frequency components of the baseband signals I and Q prior to applying them to a decimator 350 (FIG. 3) that reduces the sample frequency without any loss of information since Id1 631 and Qd1 641 are sampled at a much higher frequency by the respective ADC1 618 and ADC2 628.

[0043] The decimated desired channels are then provided to an up-converter module 650 that includes a bank of N up-mixers. The bank of N up-mixers includes N identical up-mixers whose structure is shown in FIG. 5. In an embodiment, N is an integer value equal to the number of desired channels present in BWtuner1 604. Each one of the up-mixer frequency-shifts the baseband signals I and Q of each one of the desired channels to an appropriate portion of the intermediate frequency band according to Equation (3). In other words, the bank of N up-mixers is “frequency multiplexing” the desired channels onto a first portion 682 of an IF band 686.

[0044] Similarly, tuner2 720 includes an amplifying filter AF2 713 that is configured to receive a second portion BWtuner2 704 of the broad frequency spectrum 608. The second portion 704 contains a second plurality of RF channels 706 including a second number of desired channels. In the exemplary illustration of FIG. 6, the second portion 704 has a frequency bandwidth of BWtuner2 that contains desired channels 707 having respective channel frequencies f_{rf3} and f_{rf4}. Tuner2 720 includes elements such as mixers M3 711, M4 721, amplifiers V3 714, V4 724, filters F3 715, F4 725 and analog-to-digital converters ADC3 731 and ADC4 741 that are substantially the same as the like-named elements of the signal path of tuner1 610. Thus, redundant description is omitted herein.

[0045] Digital in-phase signal Id2 731 and digital quadrature signal Qd2 741 are then provided to digital front end 740. Digital front end 740 includes a bank of L complex filters, where L is an integer value equal to the number of desired channels in the second portion BWtuner2 704 of the broad frequency spectrum 608. Each one of the bank of L complex filters is a digital complex mixer configured to transform the signals Id2 731 and Qd2 741 to baseband signals that are further filtered by individual digital low-pass filters such as FIR filters before decimated by a subsequent decimator. The elements of digital front end 740 are substantially similar to those described in digital front end 630. Thus, redundant description is omitted herein.

[0046] The decimated baseband I and Q channels are further provided to a subsequent up-conversion module 760 that performs a function substantially similar to that of the up-conversion module 650 already described above. The outputs of up-conversion module 650 and 760 can be tiled to generate a contiguous set of IF frequencies 682, 684 centered at f_{if} 686. In an embodiment, the outputs of up-conversion module 650 and 760 are digitally summed and converted to an analog signal by summing DAC 670. In another embodiment, the up-conversion modules 650 and 760 and the

digital summing function 672 can be performed using an inverse discrete Fourier transform or an inverse Fast Fourier transform operation.

[0047] The multi-tuner architecture provides the flexibility that multiple commercially available tuners can be used without the need of designing a wideband tuner. For example, a tuner designed for a terrestrial broadcast digital TV can be used together with a tuner dedicated to receiving a cable signal and/or a tuner for receiving a satellite broadcast signal. The multi-tuner receiver system provides an additional advantage that other tuners can be added quickly to the system to accommodate any future applications. Additionally, the multi-tuner architecture allows the use of slower speed (i.e., lower cost) analog-to-digital converters with a larger number of bits for achieving large dynamic range.

[0048] FIG. 7 shows a block diagram of an exemplary digital front end of the invention in more detail. In an embodiment, in-phase signal Id2 731 and quadrature signal Qd2 741 at the output of respective ADC converters 718 and 728 are provided to each of the L complex mixers 732 comprising mixers 732A to 732L. A more detailed description of each of L complex mixers is shown in FIG. 3. Mixer 732A multiplies Id2 731 and Qd2 741 with a cosine signal and a sine signal that are generated from an NCO1 and produces an I-732A signal and a Q-732A signal that are further individually filtered by an FIR filter before decimating. The bank of L complex mixers corresponds to the block 732 in FIG. 6; and the set of FIR filters and decimator corresponds to the block 734 in FIG. 6. Each decimated pair of I-732i/M in the baseband, where the index "i" is from A to L, is further provided to a subsequent up-mixer for frequency-shifting to an intermediate frequency as shown in FIG. 8.

[0049] FIG. 8 shows an exemplary embodiment of a bank of L complex up-mixers according to the present invention. Each decimated pair of complex signals I-732i/M and Q-732i/M is provided to an associated complex up-mixer, whose frequency is so chosen

that when mixing with the pair of complex signals I-732i/M and Q-732i/M will generate an associated channel at a predetermined sub-portion of the intermediate frequency band 686 (FIG. 6). A more detailed schematic block of one of the L up-mixers is described above together with FIG. 5.

[0050] FIG. 9 is a simplified block diagram of a wideband multi-tuner receiver system 900 according to an embodiment of the present invention. In an embodiment, system 900 includes a crossbar switch 910 having at least an input terminal 912 configured to receive signals from an analog-to-digital converter (ADC) 912 and an input terminal 922 configured to receive signals from an ADC 922. Crossbar switch 910 also includes an output terminal 924 that is coupled to a digital front end 930. In an embodiment, input terminals 912 and 922 of crossbar switch 910 have P inputs, where P is an integer value that is equal to the total number of desired channels received by tuner1 610 and tuner2 720. Output terminal 924 of crossbar switch 910 have Q outputs, where Q is an integer value that is equal to the total number of desired channels received by tuner1 610 and tuner2 720.

[0051] In an embodiment, digital front end 930 may include a bank of R complex mixers that frequency shifts the received channels to a baseband. Digital front end 930 may combine digital front end 630 and 740 shown in FIG. 6. Similarly, a tiled up-conversion module 950 may include up-converter modules 650 and 760 of FIG. 6.

[0052] System 900 further includes a summing DAC that operates similarly as summing DAC 470 and 670 that have been described in detail in relation with respective FIG. 4 and FIG. 6 above. Thus, redundant description is omitted herein.

[0053] FIG. 10 is a simplified block diagram of a wideband multi-tuner receiver system 1000 according to another embodiment of the present invention. System 1000 includes at least tuner1 610 coupled with digital front end 630 through an analog-to-digital converter 620 and tuner2 720 coupled with digital front end 740 through an

analog-to-digital converter 730. System 1000 further includes a crossbar switch 1010 that is interposed between digital front ends 630, 740 and up-conversion modules 650, 760. Crossbar switch 1010 includes an input terminal 1012 having S inputs coupled with DFE 630 and an input terminal 1022 having T inputs coupled with DFE 740. In an embodiment, S is an integer value equal to the number of desired channels processed in DFE 630 and T is an integer value equal to the number of desired channels processed in DFE 740. Crossbar switch 1010 further includes an output terminal 1024 having U outputs coupled with up-converter module 650 and an output terminal 1024 having V outputs coupled with up-converter module 760. In an embodiment, the total number of the outputs U and V is equal to the sum of the inputs S and T. Thus, crossbar switch 1010 allows the routing of any channel from either DFE 630 or DFE 740 to up-converters 650 or 760. It is understood that system 1000 is not as flexible as system 900 because DFE 630 and DFE 740 are already pre-assigned to respective tuner1 (610) and tuner2 (720). However, this pre-assigned arrangement allows a simpler implementation of crossbar switch 1010 that operates at lower speeds.

[0054] While several embodiments in accordance with the present invention have been described, it is to be understood that the above description is intended to be illustrative and not restrictive. Many embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

CLAIMS

What is claimed is:

1. A wideband receiver system comprising:

a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

digital circuitry configured to:

select said plurality of desired television channels from said digitized plurality of frequencies; and

output said selected plurality of television channels to a demodulator as a digital datastream.

2. The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface.

3. The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface.

4. The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.

5. The wideband receiver system of claim 1, wherein said a wideband analog-to-digital converter comprises:

a first ADC configured to generate a digital in-phase signal; and

a second ADC configured to generate a digital quadrature signal.

6. The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of television channels.

7. The wideband receiver system f claim 6, wherein:

prior to said frequency shift, said selected plurality of television channels occupy non-contiguous portions of a frequency spectrum; and

after said frequency shift, said selected plurality of television channels occupy a contiguous frequency spectrum.

8. The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.

9. The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter.

10. The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of television channels.

11. A method comprising:

in a wideband receiver system:

downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and

outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.

12. The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface.

13. The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface.

14. The method of claim 11, comprising:

generating, by a first mixer of said mixer module, an in-phase signal; and

generating, by a second mixer of said mixer module, a quadrature signal.

15. The method of claim 11, comprising:

generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and

generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.

16. The method of claim 15, comprising frequency shifting said selected plurality of television channels via a plurality of complex mixers of said digital circuitry.

17. The method of claim 16, wherein:

prior to said frequency shifting, said selected plurality of television channels occupy non-contiguous portions of a frequency spectrum; and

after said frequency shifting, said selected plurality of television channels occupy a contiguous frequency spectrum.

18. The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.

19. The method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter.

20. The method of claim 11, comprising decimating, by said digital circuitry, one or more of said selected plurality of television channels prior to said outputting of said selected plurality of television channels.

ABSTRACT

A wideband receiver system comprises a mixer module, a wideband analog-to-digital converter (ADC) module, and digital circuitry. The mixer module is configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels. The wideband ADC module is configured to digitize the swatch of frequencies comprising the plurality of desired television channels and the plurality of undesired television channels. The digital circuitry is configured to select the desired plurality of television channels from the digitized plurality of frequencies, and output the selected plurality of television channels to a demodulator as a digital datastream.

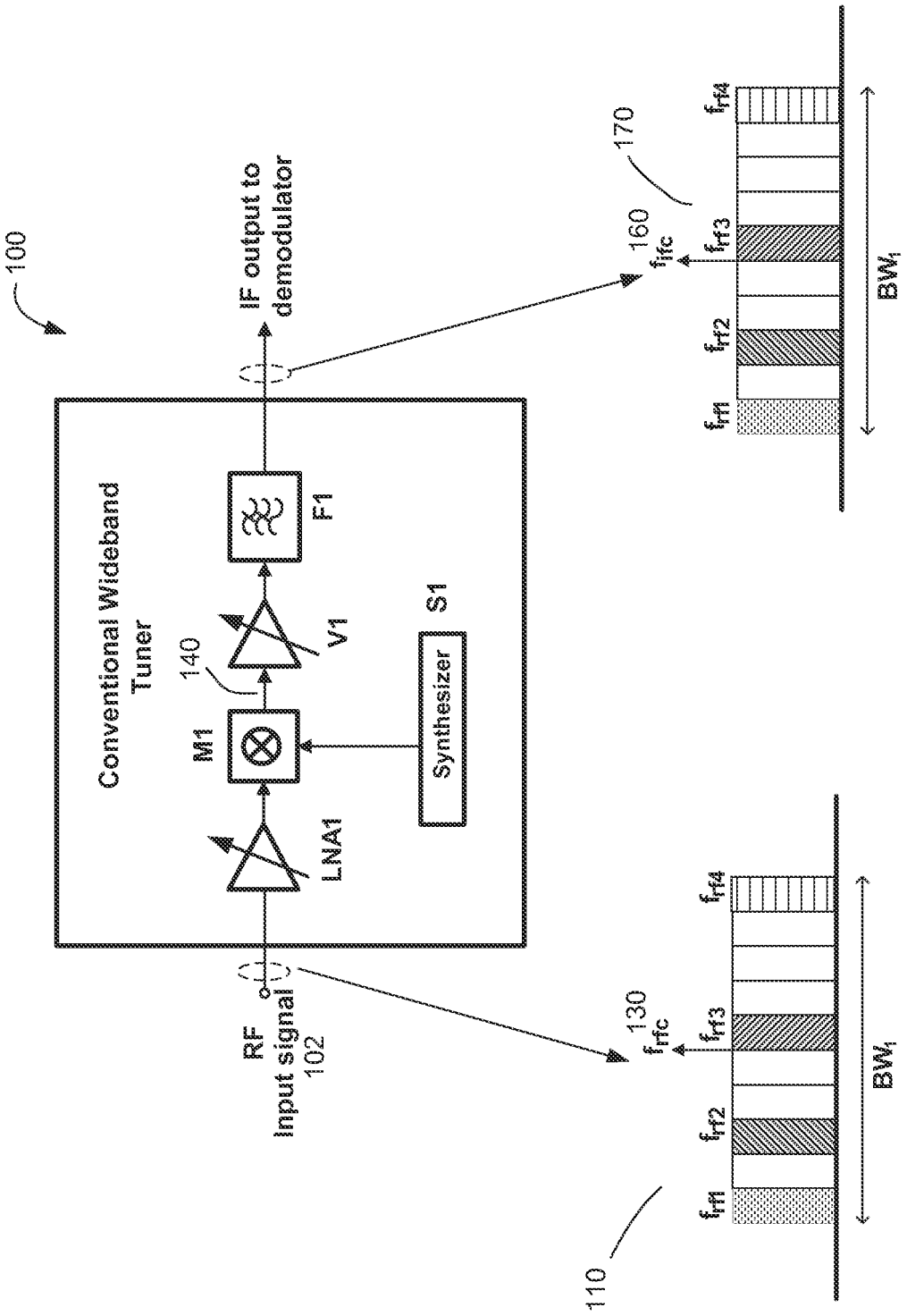


FIG. 1
(Prior Art)

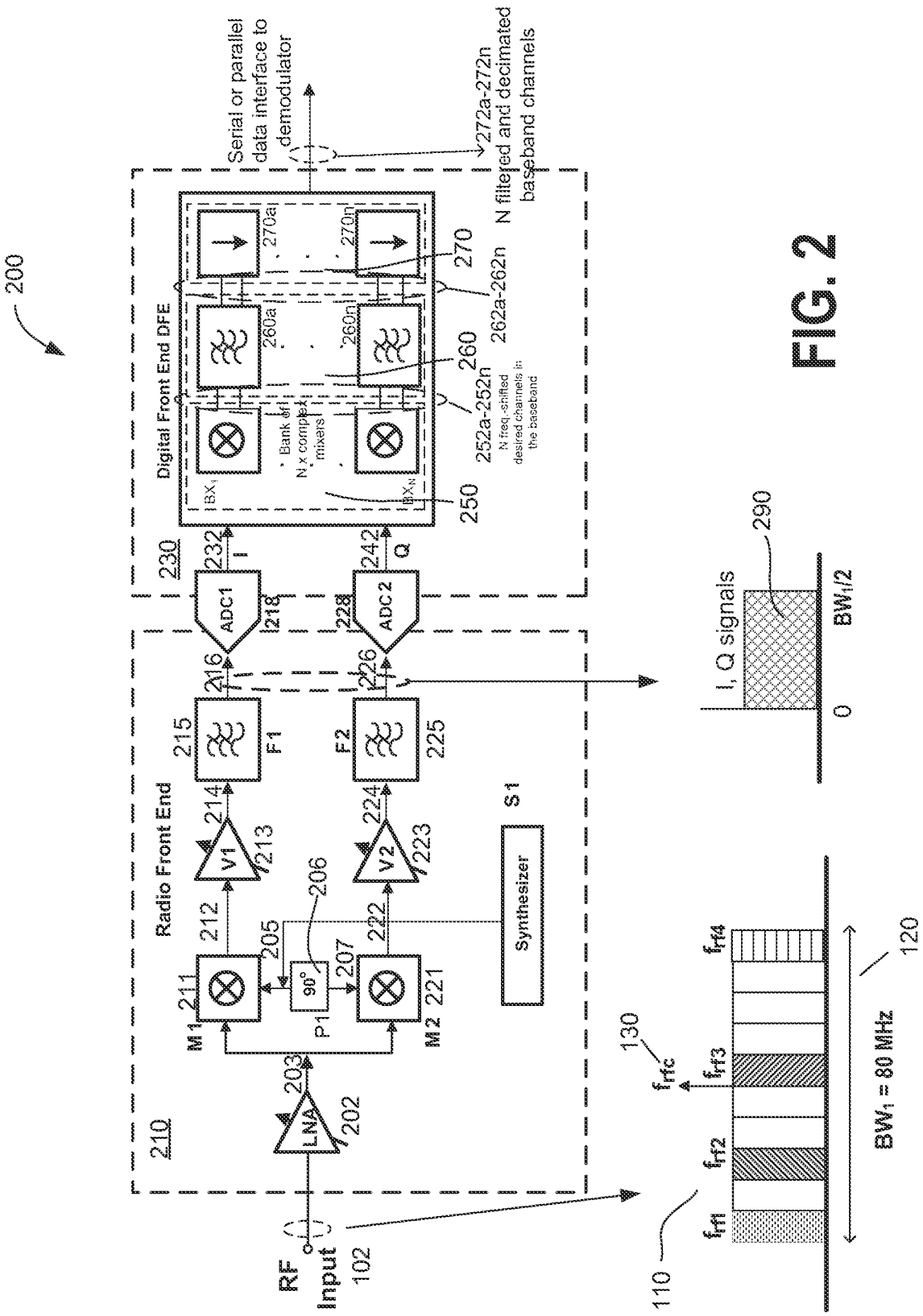

200
RF Input
102
210
LNA
202
203
M1
211
M2
221
P1
90°
205
206
207
212
222
Synthesizer
S1
V1
213
214
V2
223
224
Radio Front End
215
F1
225
F2
216
226
ADC1
218
ADC2
228
230
232
242
I
Q
Digital Front End DFE
250
260
270
260a
260n
270a
270n
Bank of 1 N x complex mixers
252a-252n
N freq.-shifted desired channels in the baseband
262a-262n
N filtered and decimated baseband channels
272a-272n
Serial or parallel data interface to demodulator
I, Q signals
290
0
BW1/2
110
130
120
BW1 = 80 MHz

FIG. 2

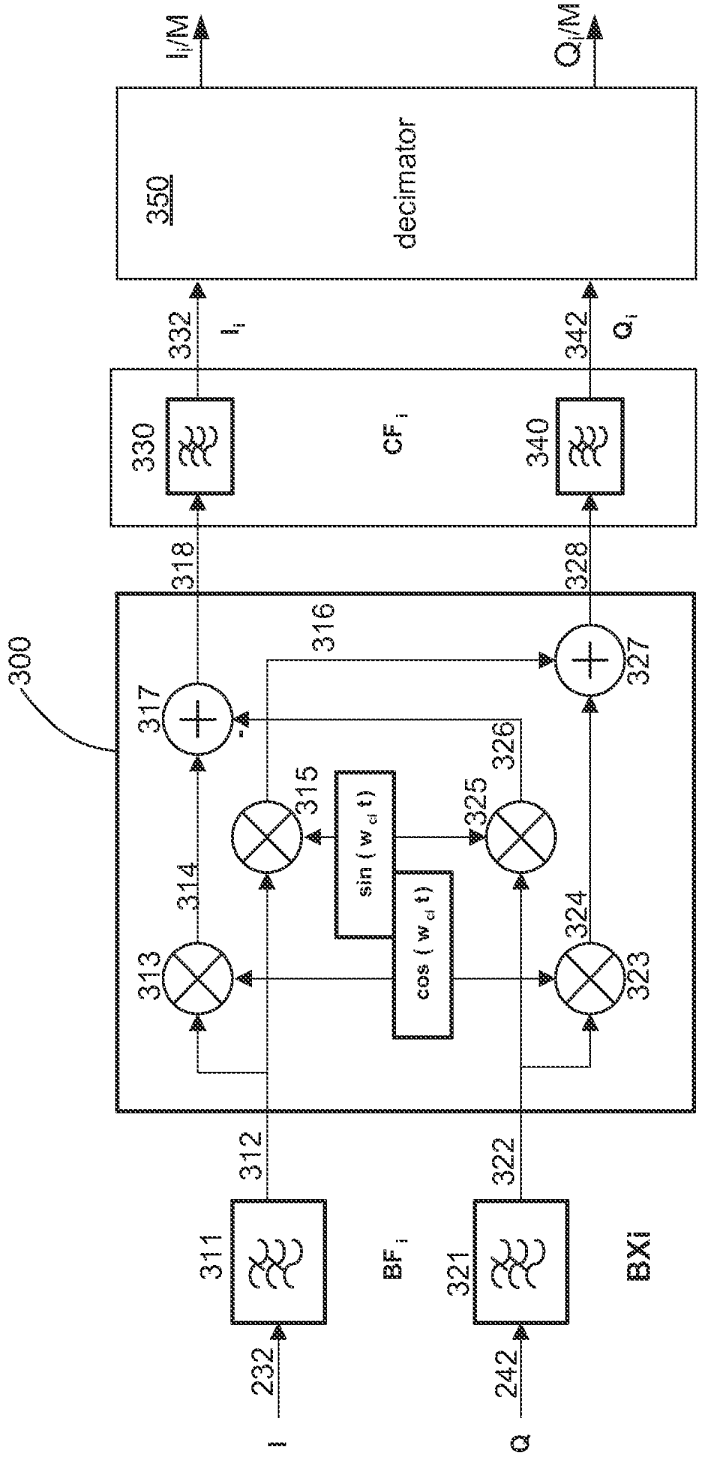

I
Q
232
242
311
321
312
322
BF$_i$
BXi
313
323
314
324
315
325
326
316
317
327
318
328
sin (w$_{ci}$ t)
cos (w$_{ci}$ t)
300
330
340
332
342
CF$_i$
I$_i$
Q$_i$
350
decimator
I$_i$/M
Q$_i$/M

FIG. 3

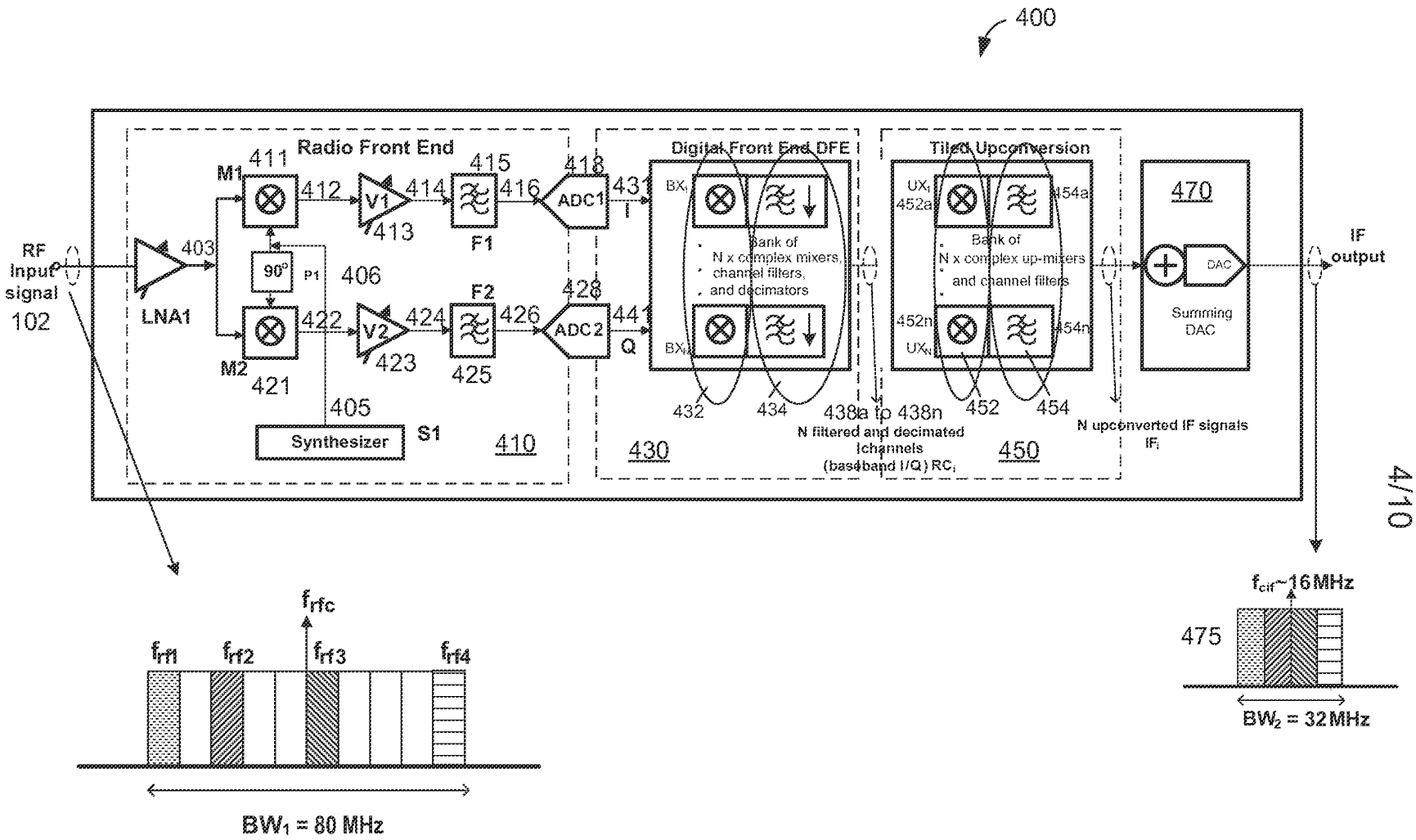

400
Radio Front End
Digital Front End DFE
Tiled Upconversion
RF input signal
102
LNA1
403
M1
M2
411
412
413
414
415
416
418
421
422
423
424
425
426
428
90°
P1
406
405
Synthesizer
S1
410
F1
F2
ADC1
ADC2
431
441
I
Q
BX1
BXN
Bank of
N x complex mixers,
channel filters,
and decimators
UX1
452a
454a
452n
UXN
454n
Bank of
N x complex up-mixers
and channel filters
470
DAC
Summing
DAC
IF output
432
434
438a to 438n
N filtered and decimated
channels
(baseband I/Q) RC1
430
450
452
454
N upconverted IF signals
IF1
4/10
frfc
frf1
frf2
frf3
frf4
BW1 = 80 MHz
fcif~16MHz
475
BW2 = 32MHz

FIG. 4

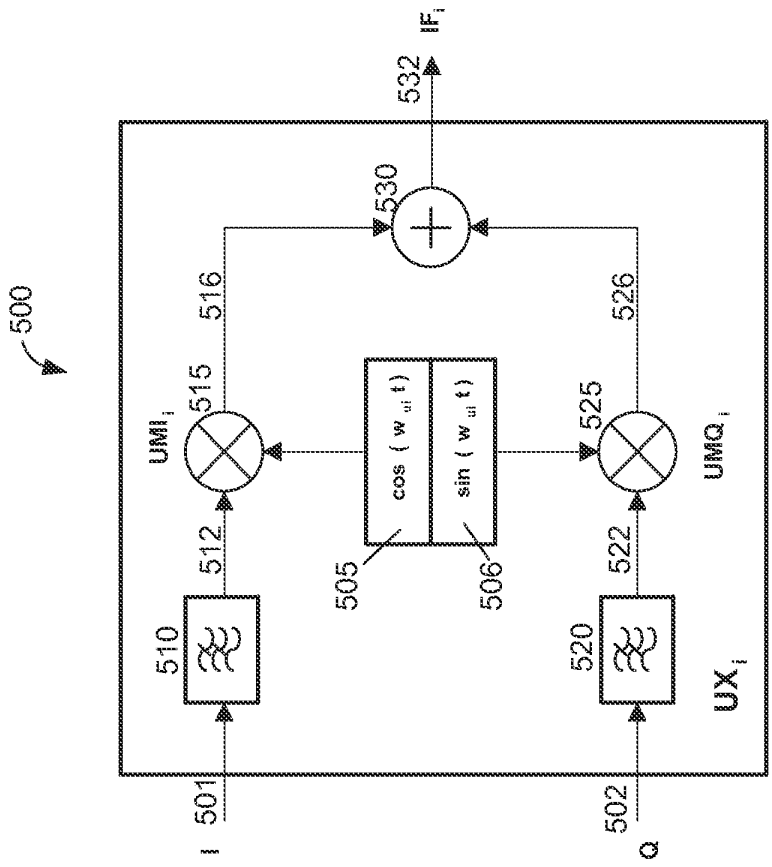

500
532
IF_i
530
516
526
515
525
UMI_i
UMQ_i
cos (w_ui t)
sin (w_ui t)
505
506
512
522
510
520
UX_i
501
502
I
Q

FIG. 5

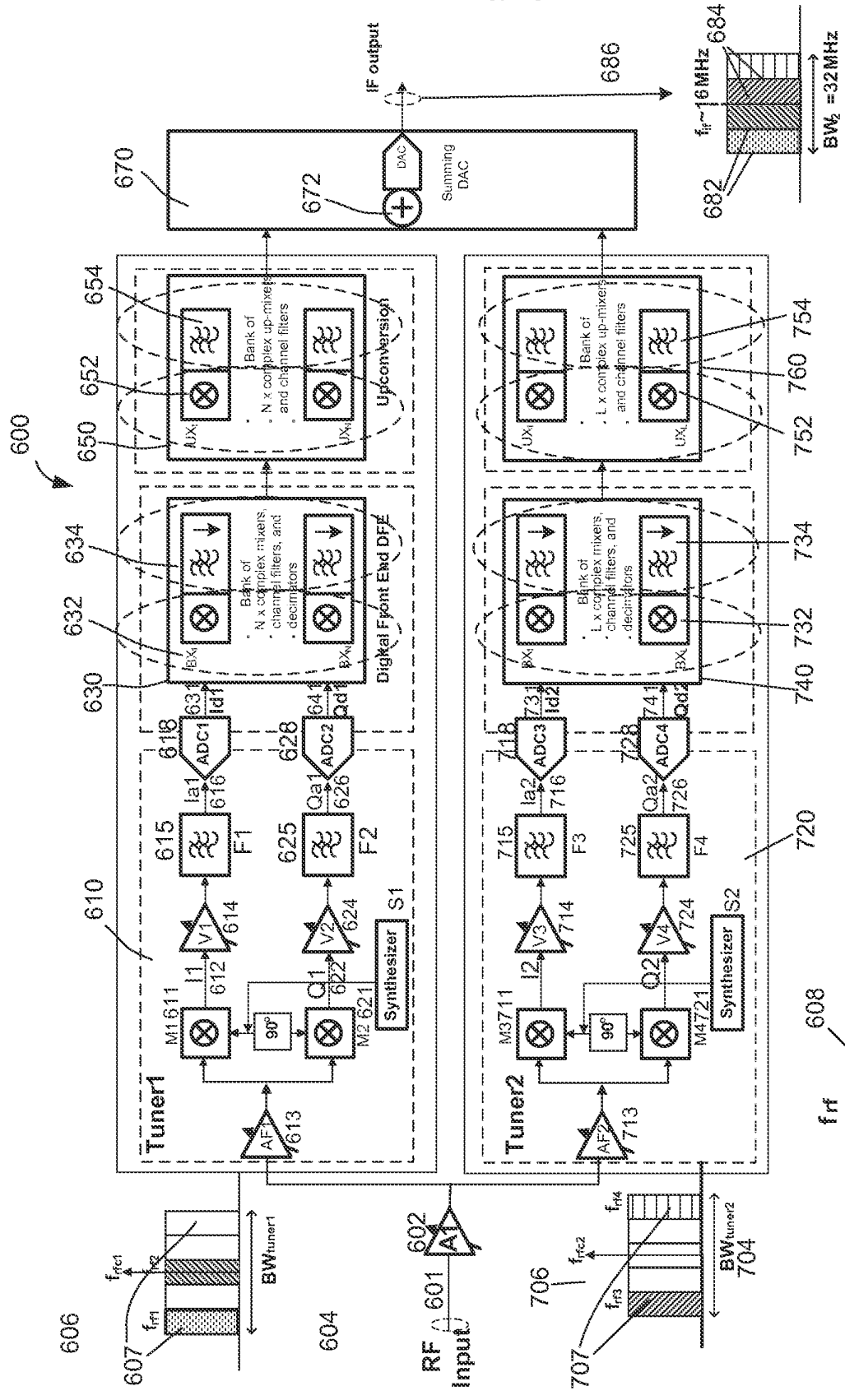

600
606
604
610
Tuner1
607
f_{rf1}
f_{rf2}
BW_{Tuner1}
602
A1
601
RF input
AF1
613
M1 611
M2 621
90°
I1 612
Q1 622
V1 614
V2 624
615
F1
625
F2
Synthesizer
S1
616
626
618
628
ADC1
ADC2
Ia1
Qa1
Id1
Qd1
63
64
630
632
634
Bank of
N x complex mixers,
channel filters, and
decimators
Digital Front End DFE
650
652
654
Upconversion
Bank of
N x complex up-mixers
and channel filters
670
672
Summing DAC
DAC
IF output
686
682
684
f_{if}~16 MHz
BW_2 =32 MHz
706
707
f_{rf3}
f_{rf4}
BW_{Tuner2}
704
720
Tuner2
AF2
713
M3 711
M4 721
I2
Q2
V3
V4
714
724
715
F3
725
F4
Synthesizer
S2
716
726
718
728
ADC3
ADC4
Ia2
Qa2
Id2
Qd2
73
74
740
732
734
Bank of
L x complex mixers,
channel filters, and
decimators
750
752
754
Bank of
L x complex up-mixers
and channel filters
760
608
f rf
c
f_{rf1}
f_{rf2}
f_{rf3}
f_{rf4}
BW_{Tuner1}
BW_{Tuner2}
BW= 80 MHz

FIG. 6

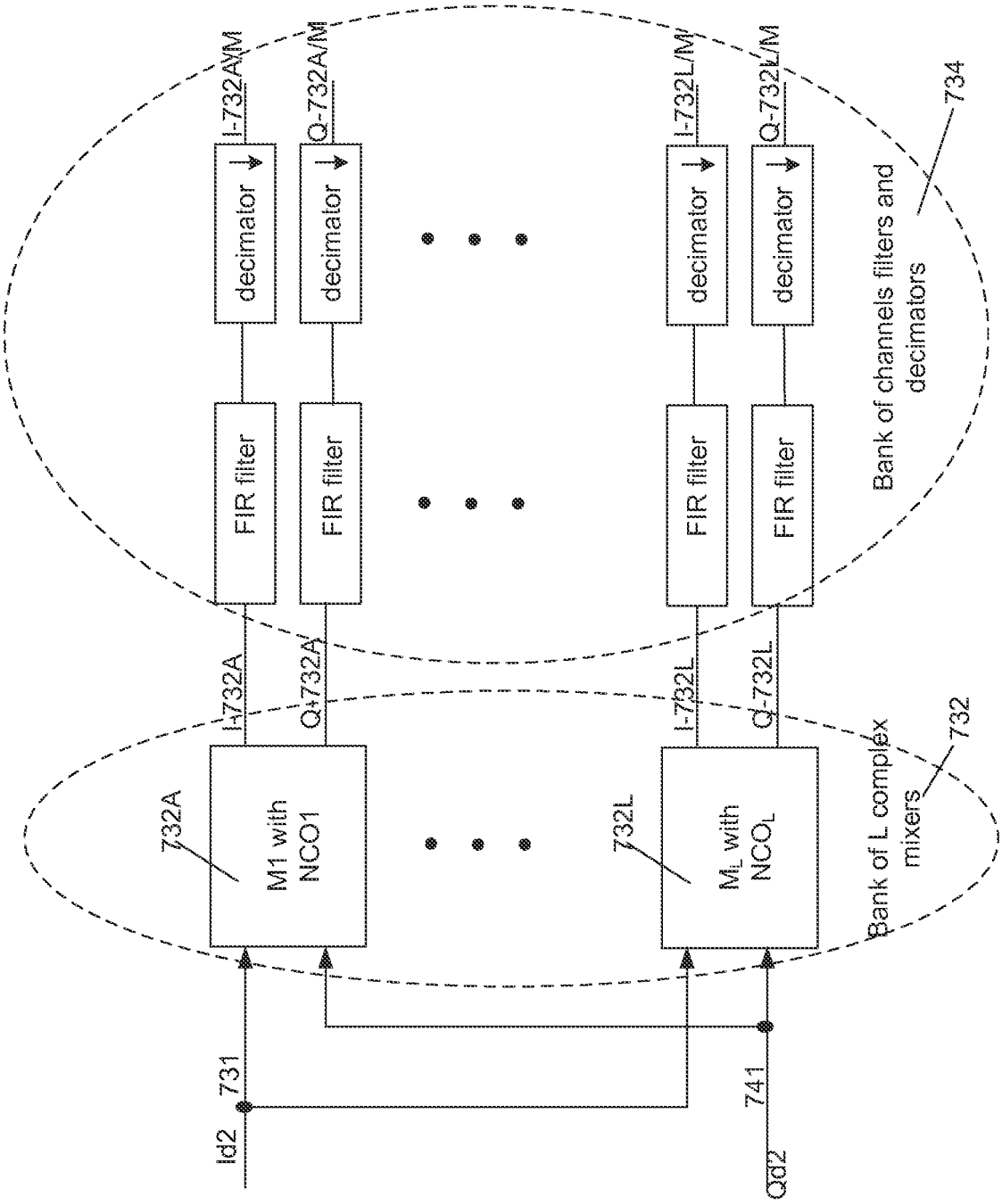

Id2
731
Qd2
741
732A
M1 with NCO1
732L
M_L with NCO_L
Bank of L complex mixers
732
I-732A
Q-732A
I-732L
Q-732L
FIR filter
decimator
I-732A/M
Q-732A/M
I-732L/M
Q-732L/M
Bank of channels filters and decimators
734

FIG. 7

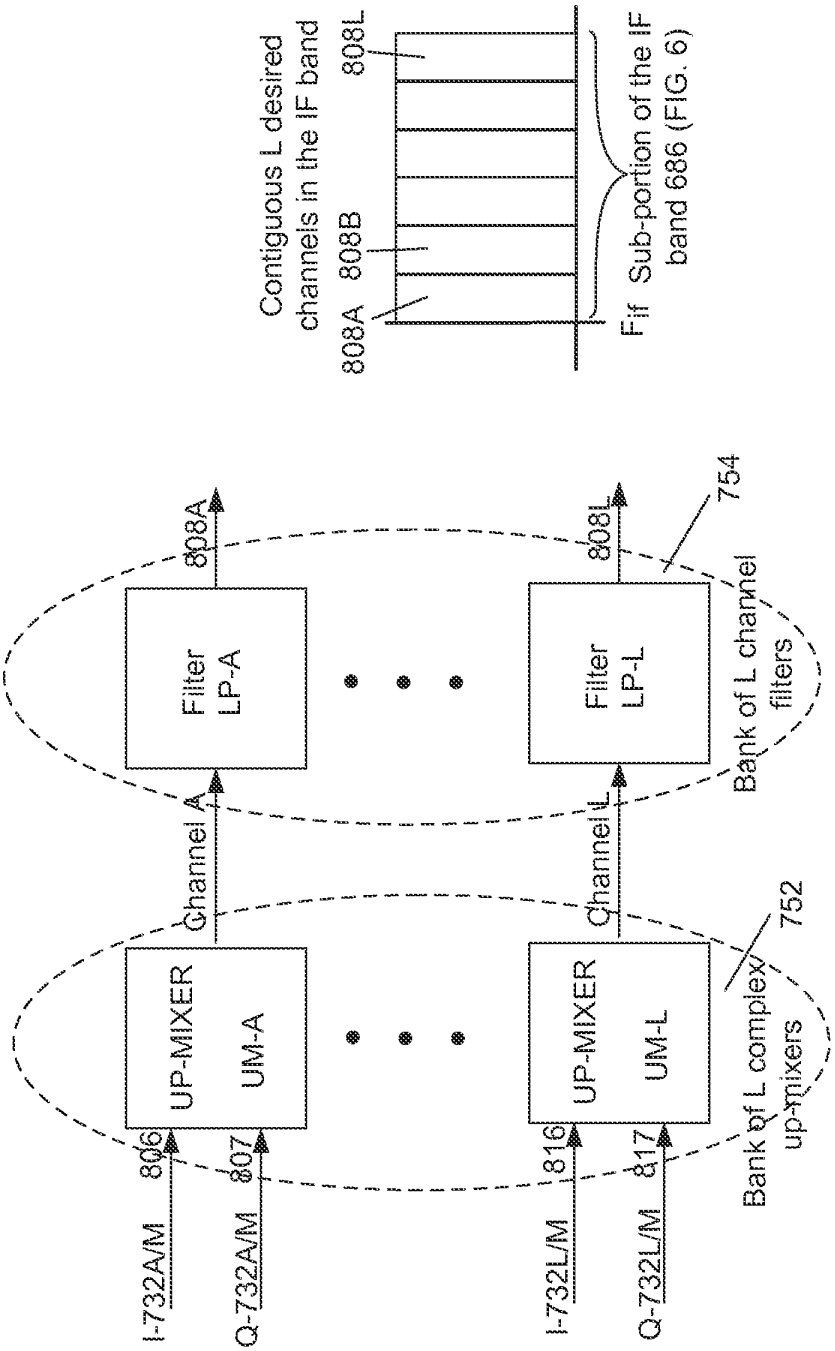

Contiguous L desired channels in the IF band
808L
808B
808A
Fif
Sub-portion of the IF band 686 (FIG. 6)
754
808A
808L
Filter LP-A
Filter LP-L
Bank of L channel filters
Channel A
Channel L
752
UP-MIXER UM-A
UP-MIXER UM-L
Bank of L complex up-mixers
806
807
816
817
I-732A/M
Q-732A/M
I-732L/M
Q-732L/M

FIG. 8

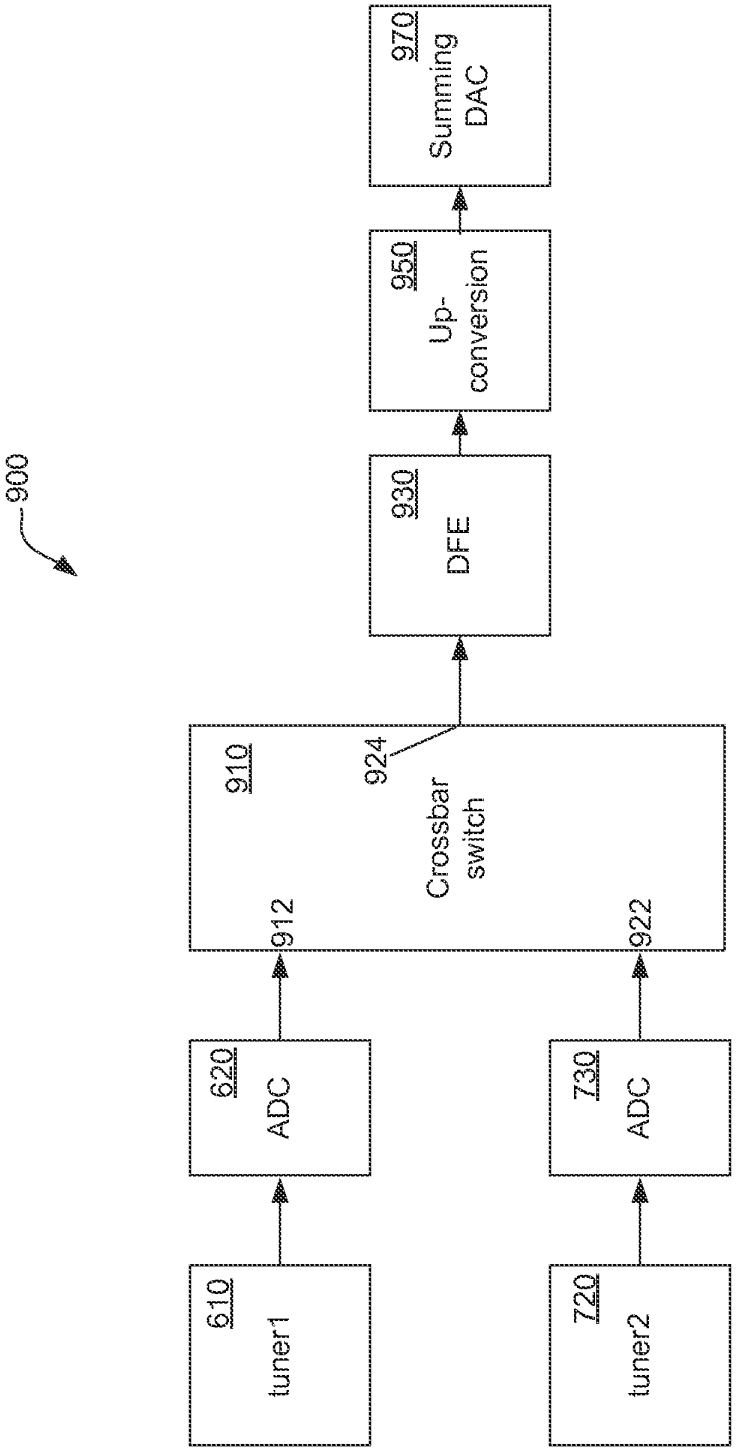

900
610
tuner1
620
ADC
912
910
Crossbar
switch
924
930
DFE
950
Up-
conversion
970
Summing
DAC
720
tuner2
730
ADC
922

FIG. 9

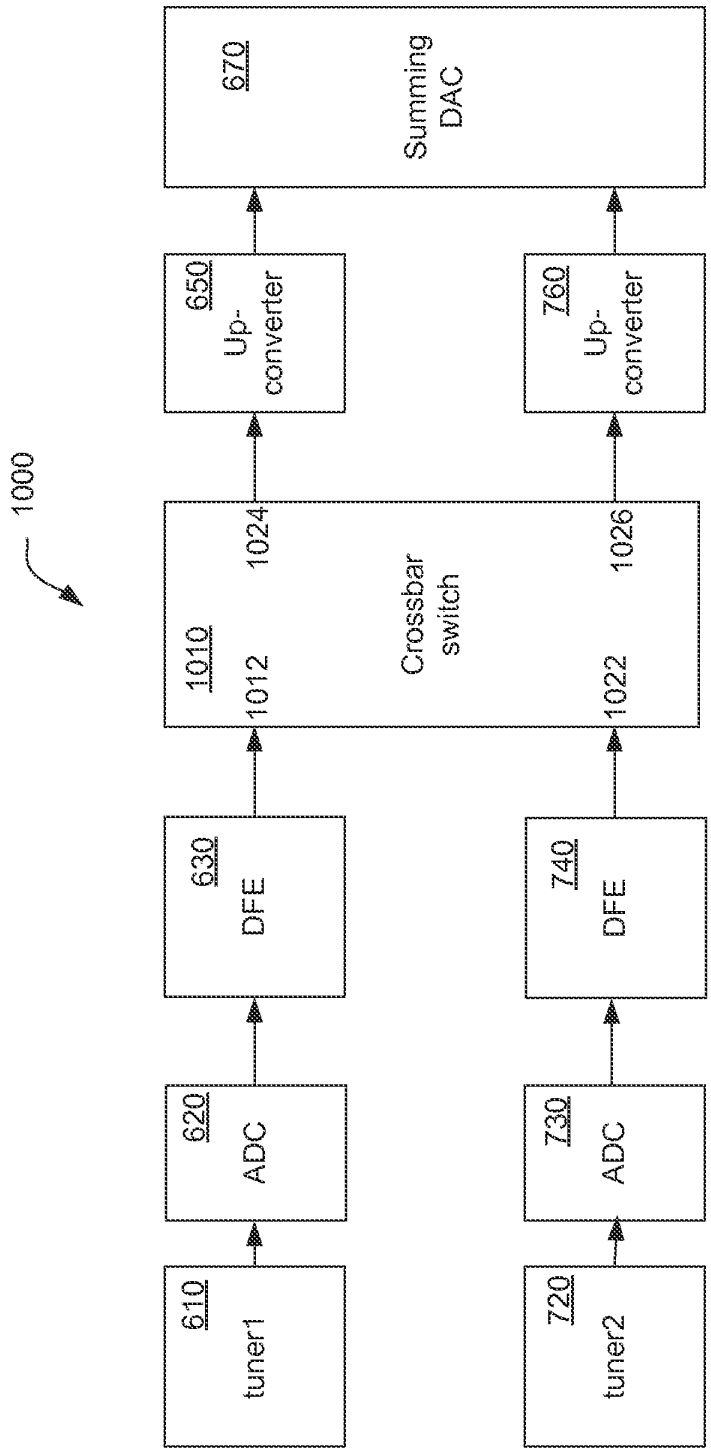

1000
610
tuner1
620
ADC
630
DFE
1010
1012
1022
Crossbar switch
1024
1026
650
Up-converter
670
Summing DAC
720
tuner2
730
ADC
740
DFE
760
Up-converter

FIG. 10

Attorney Docket No. 89194-002720US-883946

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	WIDEBAND TUNER ARCHITECTURE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/962,871 filed on August 8, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

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LEGAL NAME OF INVENTOR

Inventor: Madhukar Reddy Date (Optional) :

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Curtis Ling Date (Optional) :

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Tim Gallagher Date (Optional): _____

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☑ Practitioners associated with Customer Number: 23,446

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications a ssigned only to the undersigned according to the USPTO assignment records or assignments docu ments attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 23,446

OR

☐	Firm or Individual Name		
	Address		
	City		
	Country		
	Telephone		Email

Assignee Name and Address: MaxLinear, Inc.
2051 Palomar Airport Road, Suite 100
Carlsbad, CA 92011

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	12Dec2017
Name	Curtis Ling, Ph.D.	Telephone	(760) 692-0711
Title	Chief Technology Officer		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
First Named Inventor/Applicant Name:	Madhukar Reddy
Filer:	Chad M. Gilles/Laura Foley
Attorney Docket Number:	28427US04

Filed as Small Entity

Filing Fees for Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	70	70
Utility Search Fee	2111	1	300	300
Utility Examination Fee	2311	1	360	360
Request for Prioritized Examination	2817	1	2000	2000
Pages:				
Claims:				
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Publ. Fee- Early, Voluntary, or Normal	1504	1	0	0
PROCESSING FEE, EXCEPT PROV. APPLS.	2830	1	70	70
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2800**

Electronic Acknowledgement Receipt	
EFS ID:	21407506
Application Number:	14614543
International Application Number:	
Confirmation Number:	5785
Title of Invention:	WIDEBAND TUNER ARCHITECTURE
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Customer Number:	23446
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Exhibit 1013

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Classical and Modern Receiver Architectures

Shahriar Mirabbasi and Ken Martin, University of Toronto

ABSTRACT

This article is a review of several classical and modern wireless receiver architectures used in wideband wireless communication systems. The emphasis is on configurations suitable for integration on a single silicon chip. A full understanding of the design trade-offs discussed in this article is necessary for the proper introduction of a new modulation scheme presented in the companion article, "Hierarchical QAM: A Spectrally Efficient DC-Free Modulation Scheme" [1].

INTRODUCTION

The recent surge in applications of radio frequency (RF) transceivers has been accompanied by aggressive design goals such as low cost, low power dissipation, small form factor [2], and high-speed data transfer. These goals are driven by both the need for better portability and affordability, and the ever-increasing demand for higher-speed data communications. Such objectives, together with the usual bandwidth limitations, not only call for highly integrable transceiver architectures, but also for bandwidth-efficient modulation schemes.

To address the demand for better portability and affordability, recent research has been focused toward the development of monolithic transceiver architectures, especially using low-cost complementary metal-oxide semiconductor (CMOS) technology. This approach provides the possibility of integrating analog and digital circuitry on the same chip. In addition, the use of new systems and circuit design techniques facilitates the highest levels of receiver and transmitter integration [3]. Various suitable architectures have been proposed for implementation in deep-submicron CMOS technologies [2–5].

In this article, we review several classical and recently proposed receiver architectures, and discuss their advantages and disadvantages. In a companion article [1], a new spectrally efficient dc-free modulation scheme, suitable for highly integrable receiver architectures, is introduced.

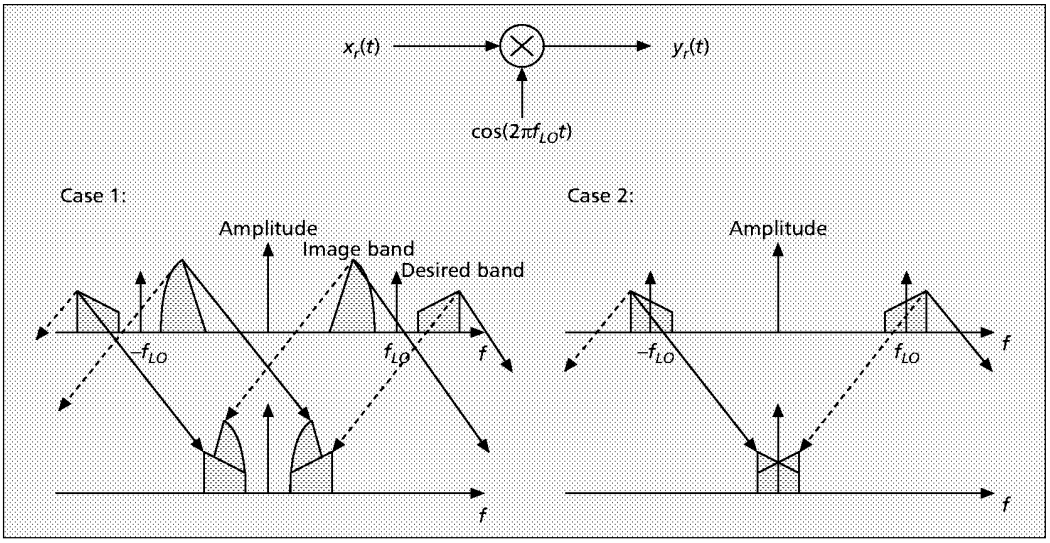


Figure 1. *Mixing a real signal with a real sinusoid for two cases, where* f_{LO} *is not equal (case 1) and equal (case 2) to the center freqeuncy of the desired signal. The spectra of the inputs of the mixer and the corresponding spectrum of the output of the mixer are shown.*

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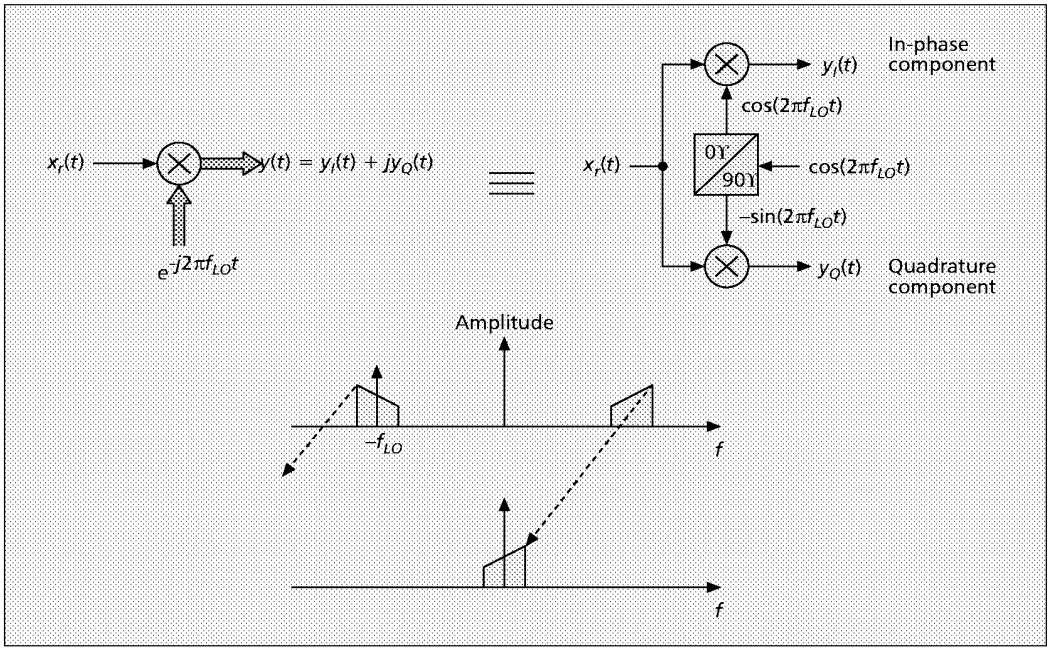


Figure 2. *Mixing a real signal with a complex exponential. The spectra of the real and complex inputs of the mixer, and the spectrum of the complex output of the mixer are shown. Here, complex signals are represented by double lines.*

To address the demand for better portability and affordability, recent research has been focused toward the development of monolithic transceiver architectures, especially using low-cost complementary metal-oxide semiconductor technology.

BACKGROUND: REAL AND COMPLEX MIXING

In preparation for the main discussion on receiver architectures, it is useful to review the *image band problem* related to frequency downconversion, an essential operation in any RF receiver. This will be done using complex representation of signals and complex mixing, techniques also useful for the discussions in the companion article [1].

Typically, frequency downconversion of a passband signal is performed by multiplying (mixing) the signal with a sinusoid such as $\cos(2\pi f_{LO}t)$. This is illustrated in Fig. 1 for the two cases in which the frequency of the sinusoid is different from and equal to the center frequency of the signal. Note that for a real signal, the negative and positive Fourier components are complex conjugates of each other. A multiplication in the time domain is equivalent to a convolution in the frequency domain. Since the Fourier transform of a sinusoid contains two equal-amplitude impulses symmetrically placed around zero on the frequency axis, the spectrum of the mixer output signal is the superposition of the positive and negative shifted versions of the spectrum of the input signal. As shown in Fig. 1, two frequency bands symmetric around the multiplying frequency are downconverted to the same output band. The undesired input signal band, which will be superimposed on the desired signal band after mixing, is called the *image band*. It is necessary to suppress any signal in the image band prior to the mixing operation. This is the task of the image-reject (IR) filter which usually precedes the mixer. In the special case where the multiplying frequency is equal to the center frequency of the incoming signal, the image band is the same as the signal band, and the image cannot be eliminated using filtering. Notice that the mixing operation with a real sinusoid generates additional signals above the multiplying frequency. In a typical receiver these high-frequency components (not shown explicitly in Fig. 1) are usually filtered out with a low-pass filter.

The previously discussed image problem arises due to the fact that the frequency spectrum of a real sinusoid contains impulses at both positive and negative frequencies. One way to avoid this problem is to mix the signal with a complex exponential, say $e^{-j2\pi f_{LO}t}$, which has only a single frequency component, in this case at a negative frequency ($-f_{LO}$). Although all physical signals are real, complex signals are a convenient mathematical representation for a pair of real signals [5, 6]. A complex signal, $x(t) = x_r(t) + jx_i(t)$, consists of a real part and an imaginary part, $x_r(t)$ and $x_i(t)$, respectively, where $x_r(t)$ and $x_i(t)$ are real signals and

$$j = \sqrt{-1}.$$

Complex signals are processed according to the rules of complex arithmetic. In general, they can have negative and positive frequency components totally different from each other. As an example, the complex exponential $e^{-j2\pi f_{LO}t} = \cos(2\pi f_{LO}t) - j\sin(2\pi f_{LO}t)$, has only a single negative-frequency component. Therefore, mixing a real signal with this negative-frequency complex exponential gives a complex signal whose spectrum is a shifted version of the real signal spectrum. *Theoretically*, this eliminates the image problem associated with frequency shifting when mixing with a real sinusoid.

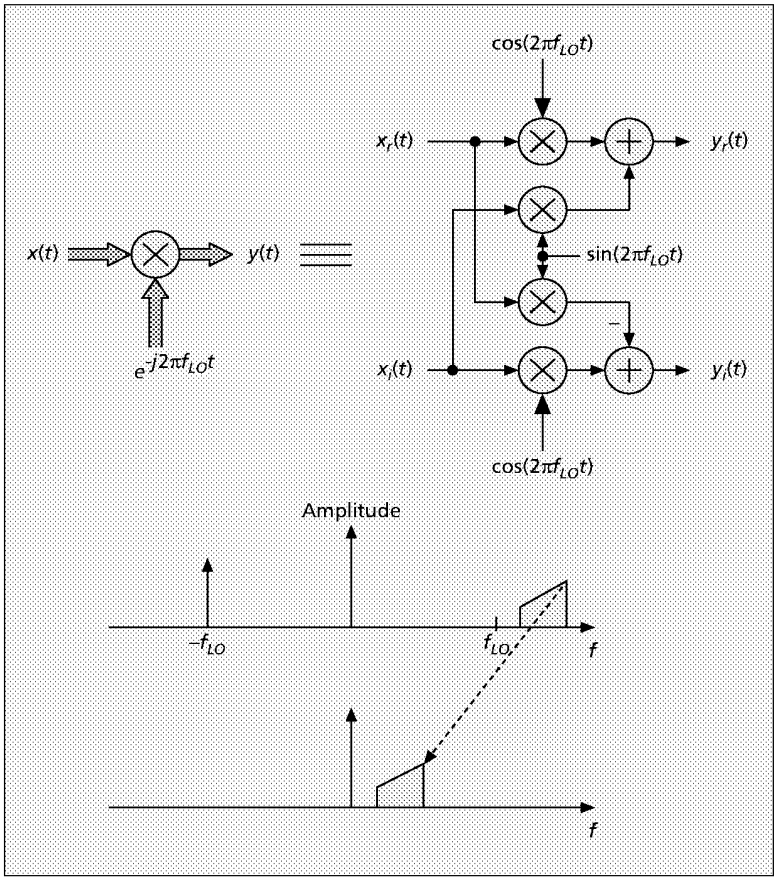


Figure 3. *Mixing a complex signal with a complex exponential. The spectra of the complex inputs of the mixer, and the spectrum of the complex output of the mixer are shown.*

The realization of a multiplier for mixing a real signal with a complex exponential requires two real multipliers, as illustrated in Fig. 2. The real and imaginary parts of the mixer output are called the *in-phase* (I) and *quadrature* (Q) components of the downconverted signal (since cosine and sine are in quadrature). In Fig. 2 the frequency of the complex exponential is chosen to be the same as the center frequency of the passband signal, for comparison with case 2 in Fig. 1. In this case there is no image problem associated with the complex mixer. As discussed in the following section, this fundamental property is used in homodyne receivers.

Now, consider the general case of mixing two complex signals $x(t) = x_r(t) + jx_i(t)$ and $z(t) = z_r(t) + jz_i(t)$: $x(t) \cdot z(t) = (x_r(t) \cdot z_r(t) - x_i(t) \cdot z_i(t)) + j(x_r(t) \cdot z_i(t) + x_i(t) \cdot z_r(t))$. A practical realization of this complex mixer using four real mixers is shown in Fig. 3. Complex mixing is used in IR mixers. These mixers are employed in some recently proposed receiver architectures, discussed later.

In some cases, only the real or imaginary part of a complex mixer output is of interest. One example is the quadrature amplitude modulation (QAM) system modulator [6]. Extracting the real (or imaginary) part of a complex mixer output can be implemented efficiently as shown in Fig. 4. Here, the complex mixer is implemented with two real mixers and one adder.

As a final point, it should be mentioned that in analyzing receivers for undesired image components, it is often necessary to isolate the positive and negative frequency components of the received signal. Figure 5 shows a block diagram of the system for converting an arbitrary complex signal into one that contains only the positive frequency components of the original signal. In this figure, the block with transfer function $-j \cdot \text{sgn}(\omega)$ is the well known Hilbert transformer which shifts its input signal phase by –90° for positive frequencies and +90° for negative frequencies.

Receiver Architectures

Most of the wireless transceivers used so far are based on a conventional heterodyne architecture. These transceivers have good performance, but suffer from high production costs and require a relatively large form factor due to expensive and nonintegrable RF and intermediate frequency (IF) filters. In this section we briefly review the conventional heterodyne receiver topology along with some other recently developed receiver architectures, and discuss their advantages and disadvantages. For each particular receiver architecture, there exists a corresponding transmitter architecture with essentially the same fundamental building blocks. The exception to this regards the transmitter power amplifier, which, although important, is beyond the scope of this article. Therefore, in our review we focus on receiver structures. Further discussions of transmitter architectures can be found in [5, 7].

Conventional Heterodyne Receivers

Most of today's commercially available RF transceivers utilize some variant of conventional heterodyne architecture. In a heterodyne receiver, as shown in Fig. 6, the RF front-end (preselection) filter serves to remove out-of-band signal energy as well as partially reject image band signals. After this prefiltering, the received signal is amplified by a low-noise amplifier (LNA). The IR filter following the LNA further attenuates the undesired signals at the image band frequencies. The desired signal at the output of the IR filter is then downconverted from the carrier frequency to a fixed IF by multiplication (mixing) with the output of a local oscillator (LO). Commonly, in heterodyne receivers, high-performance, low-phase-noise voltage-controlled oscillators (VCOs) employed as LOs are realized with discrete components such as high-quality-factor (Q) inductors and varactor diodes [3].

At the output of the mixer an IF filter, typically followed by a programmable-gain IF amplifier, selects the desired channel and reduces the distortion and dynamic range requirements of the subsequent receiver blocks [3]. The signal can be shifted to baseband and demodulated as shown in Fig. 6, or alternatively further downconverted to lower IFs, and then shifted to baseband and demodulated.

Since, at the carrier frequency, the desired band and image band are separated by twice the IF, it is desirable to choose a high IF to reduce

the requirements on the IR filter. In fact, if the IF is chosen high enough that the preselection RF filter can sufficiently attenuate the image band, it might be possible to directly connect the output of the LNA to the mixer without including an IR filter [7]. On the other hand, since channel selection in a heterodyne system is done at the IF, a low IF allows employment of higher-quality channel-select filters. Therefore, the choice of IF depends on the trade-off between image rejection and channel selection. Other factors influencing the choice of IF are availability and the physical size of commercial filters for different frequencies [2].

Conventionally, all the filters used in the heterodyne system are high-Q discrete component filters, such as surface acoustic wave (SAW) or ceramic filters. Compared to other more integrable receiver architectures, the heterodyne receiver has superior performance with respect to *selectivity*, a measure of a receiver's ability to separate the desired band around the carrier frequency from signals received at other frequencies, and *sensitivity*, the minimal signal at the receiver input for which there is sufficient signal-to-noise ratio (SNR) at the receiver output. This is achieved with the use of high-Q discrete components [3].

Employing high-Q elements does come with some drawbacks. A major limitation is that the off-chip IR filters have low input impedance. This requires a high drive capability for the preceding LNA, inevitably leading to more severe trade-offs between gain, noise figure, stability, and power dissipation in the amplifier [7]. Furthermore, these high-Q filters are difficult and somewhat impractical when realized at high frequencies in an integrated solution, primarily because integrated inductors have at best only moderate Q-factors. In addition, the narrowband discrete-component IF channel-select filter of the heterodyne receiver tailors the particular implementation to a specific standard [3].

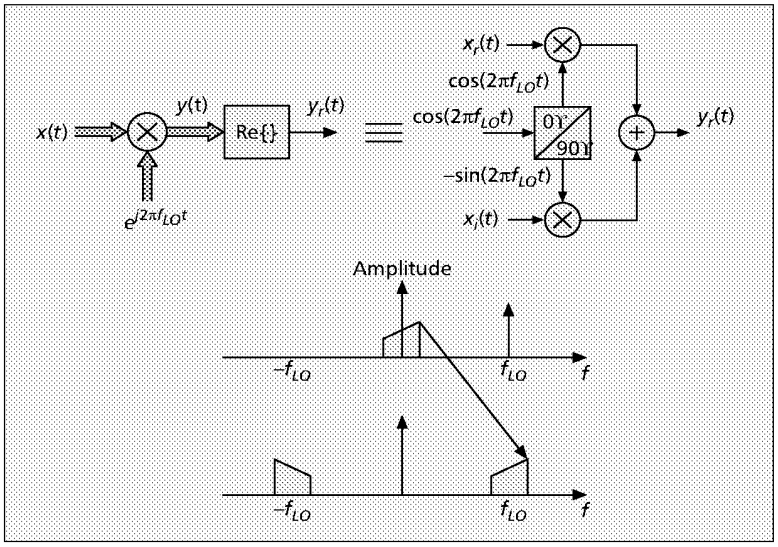


Figure 4. *An efficient implementation for a complex mixer when only a real part of the mixer output is of interest. The spectra of the complex inputs of the mixer, and the spectrum of the real part of the mixer output are shown. Note that since the final output is real signal, its spectrum is complex-conjugate symmetric.*

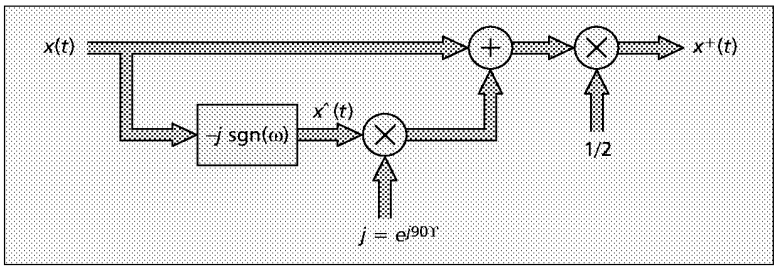


Figure 5. *A system that extracts positive frequency components of the input signal. By changing* $e^{j90°}$ *to* $e^{-j90°}$ *(i.e.,* j *to* –j*) in the multiplier, the system would extract the negative frequency components of the input.*

Direct-Conversion Architecture

Direct conversion, also known as *homodyne* or *zero-IF conversion*, is a natural approach to downconverting an RF signal directly to baseband. Alternately, one can think of choosing IF to be zero. This architecture, shown in Fig. 7, employs low-pass filtering in the baseband to suppress nearby interferers and select the desired channel. The quadrature downconversion (I and Q channels) is necessary in typical amplitude and phase or frequency modulated signals because in general the two side-bands of the RF spectrum are different. Mixing with a real sinusoid would result in irreversible corruption of the transmitted information [2]. Note that quadrature downconversion is equivalent to complex mixing, discussed previously (Fig. 2).

The homodyne architecture has several fundamental advantages over the heterodyne counterpart. The intermediary IF stages are removed,

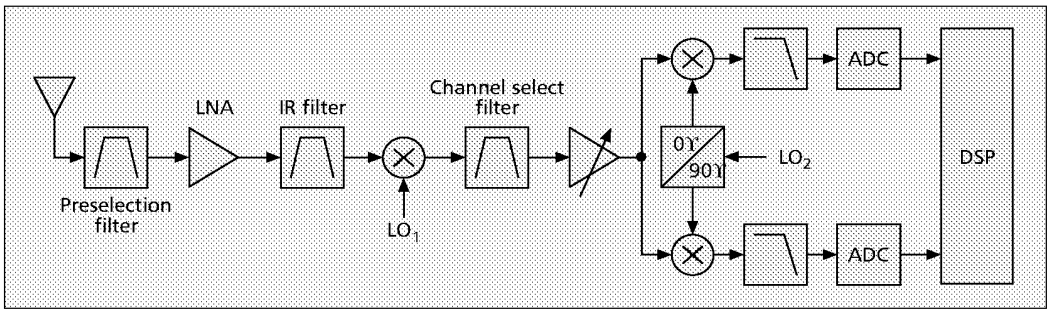


Figure 6. *A generic heterodyne receiver.*

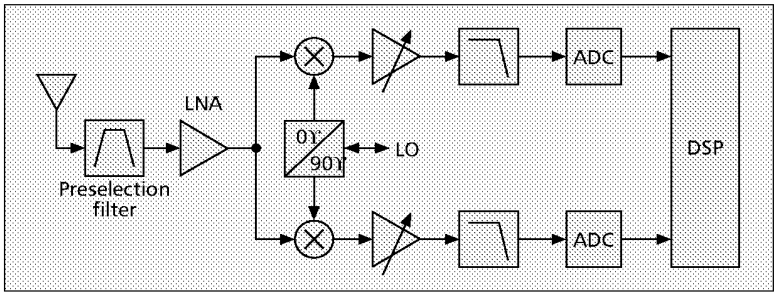


Figure 7. *A generic homodyne receiver.*

and the need for the IR filter is eliminated. Furthermore, the absence of the bulky off-chip IR filters removes the LNA requirement to drive a low impedance load. The functions of channel selection and subsequent amplification at a nonzero IF are replaced with low-pass filtering and baseband amplification, amenable to monolithic integration.

Despite this suitability for higher levels of integration, a homodyne receiver exacerbates a number of issues that either do not exist or are not as serious in a heterodyne receiver. Next, we will briefly review some of these issues.

DC-Offsets — Perhaps the most serious problem is that of dc-offset in the baseband section of the homodyne receiver [4]. These extraneous offset voltages can corrupt the desired signal and/or saturate the following stages. They arise due to the self-mixing phenomenon of the local oscillator or the in-band interferer, aside from the usual element mismatch in the signal path circuitry.

To better understand the origin of these offsets, consider the received signal path shown in Fig. 8. First, the isolation between the LO port and the inputs of the mixer and the LNA is not perfect, and a finite amount of feedthrough exists from the LO port to the other mixer input and to the input of the LNA. Known as *LO leakage*, this effect arises from capacitive and substrate coupling and, if the LO signal is provided externally, through bond-wire coupling. The leakage signal appearing at the inputs of the LNA and the mixer is now mixed with the original LO signal, thus producing a dc component at the output of the mixer. This LO self-mixing can be quite severe, and a time-varying dc-offset occurs when the LO signal leaks out through the antenna, and is radiated and reflected from nearby objects back to the receiver. A similar effect occurs if a large in-band interferer (in the passband of the RF preselection filter) leaks from the LNA output to the mixer LO port and gets multiplied by itself [7]. It should be noted that these dc-offsets exist in heterodyne receivers as well, but are mostly eliminated naturally by the IF band-pass filters.

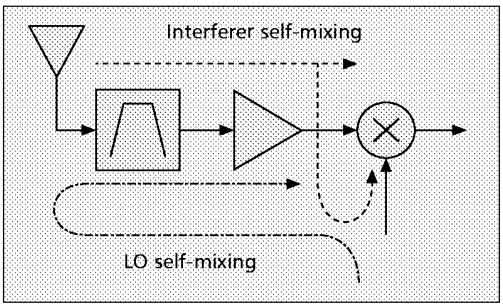


Figure 8. *Self-mixing of the LO and/or of an interferer in homodyne receiver front-end.*

Thus, direct-conversion receivers require appropriate methods to remove undesired dc offsets. A simple approach is to use ac-coupling in the downconverted signal path. However, since the spectra of all the spectrally efficient modulation schemes currently used exhibit significant energy at dc, such signals are corrupted by ac-coupling filters [4]. A better method is the use of baseband analog and/or digital signal processing (DSP) techniques for offset estimation and cancellation [3][7]. However, these techniques add complexity and do not solve the problems associated with $1/f$ noise at low frequencies in CMOS implementations, a significant issue.

A natural system solution to the dc offset problem in direct-conversion receivers is to minimize the baseband signal energy near dc by choosing a "dc-free" modulation scheme and use ac-coupling for offset elimination. This approach has been successfully used in pager systems with frequency shift keying (FSK) modulation, despite the spectral inefficiency of FSK [4]. In the companion article [1] we introduce a new spectrally efficient dc-free modulation scheme.

LO Leakage — In addition to introducing dc offsets, leakage of the LO signal to the antenna and radiation from there creates in-band interference for other receivers using the same standard [7]. This problem becomes less severe as more sections of RF receivers are fabricated on the same chip. With differential LOs, the net coupling to the antenna can approach acceptably low levels [2].

I/Q Mismatch — As mentioned earlier, for most currently used modulation schemes, a homodyne receiver must incorporate quadrature downconversion. This requires shifting either the RF signal or the LO output by 90°. Since phase-shifting the RF signal generally entails severe noise-power-gain trade-offs [2] and is especially difficult for the wideband signals used in high-data-rate systems, it is often desirable to shift the LO output (Fig. 7). In either case, the errors in the nominally 90° phase shift and mismatches between the amplitudes of the I and Q signal paths corrupt the downconverted signal constellation, thereby increasing the bit error rate. Note that all sections of the circuit in the I and Q paths contribute to gain and phase mismatches.

To gain more insight into the effect of I /Q mismatch, and show the versatility and convenience of using complex formulation, consider the practical case where the quadrature LO generates the complex signal $x_{LO}(t) = \cos(\omega_{LO}t) - j(1 + \varepsilon)\sin(\omega_{LO}t + \theta)$. Here, ε and θ represent LO gain and phase errors. One can rewrite the quadrature LO output as

$$x_{LO}(t) = \frac{1}{2}\left[1-(1+\varepsilon)e^{j\theta}\right]e^{j\omega_{LO}t} + \frac{1}{2}\left[1+(1+\varepsilon)e^{-j\theta}\right]e^{-j\omega_{LO}t}.$$

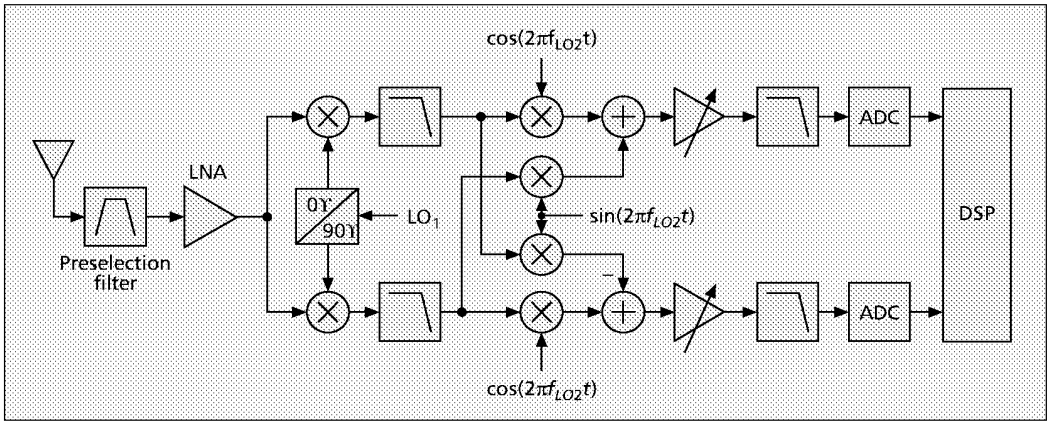


Figure 9. *A double-conversion wideband IF receiver.*

Aside from the problems mentioned here, direct-conversion receivers are sensitive to even-order distortions. Also, since the downconverted spectrum is located around zero frequency, the flicker noise of the devices has a profound effect on the SNR, a severe problem in CMOS implementations.

Ideally, the complex LO output should contain only the negative frequency. However, from the above expression it is apparent that, due to gain and phase errors, there is a positive frequency component with a magnitude of $|1 - (1 + \varepsilon)e^{j\theta}|/2$. This component causes interfering images and, if not compensated for, can deteriorate receiver performance. One can consider the effects of gain and phase mismatches separately. The magnitude of the undesired positive frequency component for gain mismatch is $|\varepsilon|/2$, and for phase mismatch $|\sin(\theta/2)|$, which can be approximated by $|\theta|/2$ when the phase mismatch is small.

Aside from the problems mentioned above, direct-conversion receivers are sensitive to even-order distortions. Also, since the downconverted spectrum is located around zero frequency, the flicker ($1/f$) noise of the devices has a profound effect on the SNR, a severe problem in CMOS implementations [2]. Furthermore, integrating the high-frequency low-phase-noise channel-select frequency synthesizer is difficult to achieve with low-Q VCOs available on integrated circuits [3].

Despite all these problems, direct-conversion transceivers for digital mobile phones using silicon bipolar technology have been in full production at Alcatel since 1991 [8]. The same company recently introduced a direct-conversion transceiver in a silicon germanium BiCMOS process [9] for the Global System for Mobile Communications (GSM) group of standards. In these transceivers, in order to handle the problems associated with static and dynamic dc offsets, DSP algorithms are used. These algorithms rely on the constant-envelope property of the modulation scheme used in GSM. To the best of the authors' knowledge, direct-conversion transceivers have not been used commercially in systems with nonconstant envelope modulation schemes, which are required in high-data-rate communication systems.

Wideband IF with Double-Conversion Receiver Architecture

This alternative architecture [3, 10], well suited to full integration, is shown in Fig. 9. In this receiver, after preselection filtering and amplification, all potential RF channels are complex-mixed and downconverted to IF. As discussed previously related to Fig. 2, there is no image problem. A second complex mixing is done from IF to baseband, using a tunable channel-select frequency-synthesizer. In this complex mixer, by properly adding the outputs of the real multipliers in pairs, the image frequencies are canceled while the desired channels add constructively. If the IF is chosen high enough, additional image rejection may be obtained from the RF front-end preselection filter [3].

Comparing the two integrated solutions discussed so far, in both architectures channel selection is performed at baseband, allowing the possibility of a programmable integrated channel-select filter for multistandard receiver applications. However, the wideband IF architecture has some advantages over the homodyne counterpart, which will now be discussed. Due to the fact that channel tuning is performed not using the first (RF) synthesizer but the lower-frequency (IF) LO, the RF LO can be implemented as a fixed-frequency crystal-controlled oscillator. Several techniques may be utilized to realize a low-phase-noise fixed LO with low-Q on-chip components [3]. Also, since tuning is performed with the IF LO operating at a lower frequency, the phase-noise performance of this oscillator can be significantly better than that of the tunable RF oscillator employed in a homodyne receiver. Furthermore, since in the wideband IF system there is no LO operating at the same frequency as the incoming RF carrier, the potential problems associated with LO leakage and time-varying dc offsets are minimized. Although in the wideband IF system the second LO is at the same frequency as the desired IF channel, the dc offset which results at the baseband from self-mixing is relatively constant and may be cancelled using adaptive signal processing methods [3].

The particular IR mixer used in this architecture, which is similar to the Weaver technique [11], has several advantages. First, lossy passive phase-shifting filters are not required in the signal path to generate the correct phase shift between the image and desired bands. Second, assuming again that the upconverted terms are removed, the image-rejection is very

As in wideband IF systems, if one employs two quadrature downconversion paths in a heterodyne receiver, then all of the required information for the separation of the wanted signal from unwanted signals, such as images, is available in the two IF signals.

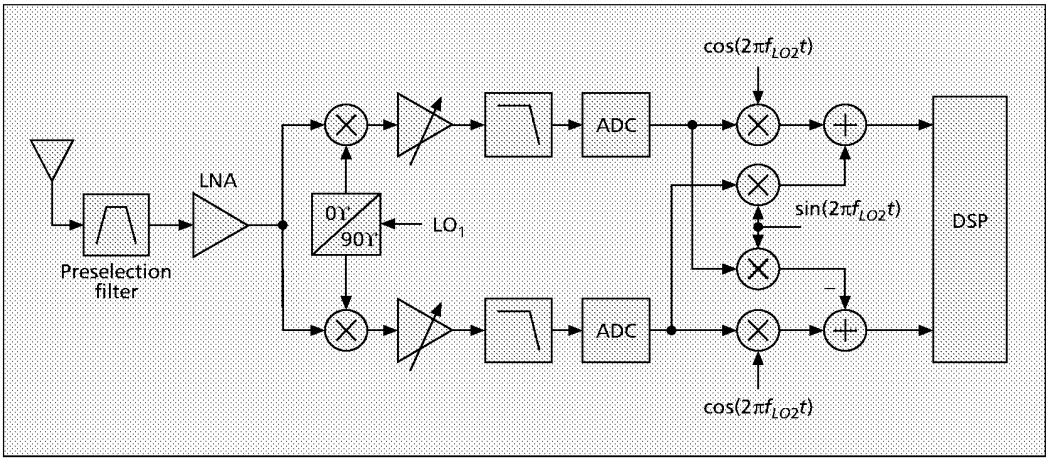


Figure 10. *A low-IF receiver.*

wideband. Also, it can be shown that the edge of the image attenuation band is set by the frequency of the first LO, which leads to the third advantage. If it is assumed that a multistandard-capable receiver is built where the frequency of the first LO can perform a course adjustment to accommodate the carrier frequency of a different standard, the image rejection will follow the first LO, and it can be thought of as a self-aligning IR mixer [3]. Note that the structure of this IR mixer (consisting of four multipliers and two adders) is the same as that of the complex mixer of Fig. 3. A detailed analysis of this IR mixer based on complex signal theory is given in [5].

The limitations of wideband IF receivers are as follows. Since the first LO is fixed in frequency, all channels must pass through the IF stage (the desired channel is selected using a second LO). This has two problematic implications: first, as a result of moving the channel selection to a lower frequency, the IF synthesizer requires a VCO with the capability of tuning across a broader frequency range as a percentage of the nominal operating frequency; second, by removing the channel-select filter at IF, strong adjacent channel interferers are now a concern for the second mixer stage as well as the baseband blocks. This implies a higher dynamic range requirement for these latter receiver stages. Also, as with conventional IR mixers, any I/Q phase and gain mismatch would degrade the performance of the receiver [3].

Low-IF Receiver Architecture

The idea behind low-IF topologies is similar to that of double-conversion wideband IF, and the goal is to combine the advantages of both heterodyne and homodyne receivers [12]. As in wideband IF systems, if one employs two quadrature downconversion paths in a heterodyne receiver, all of the required information for the separation of the wanted signal from unwanted signals, such as images, is available in the two IF signals.

Among the different low-IF topologies mentioned in [5, 10, 12], a preferred version is shown in Fig. 10. This architecture is fairly similar to that of the wideband IF architecture, although there are several subtle differences between the two. First is the choice of IF. While the IF in the wideband IF architecture is typically high, in the low-IF system the IF is chosen as low as one or two times the channel bandwidth. Note that this alleviates the dc offset problem in these two architectures compared to their homodyne counterparts, simply because after the first downconversion the wanted signal is not located around dc. Second, in the low-IF topology it is more feasible to sample the low-IF signal after the first mixer stage with a high resolution analog-to-digital convertor (ADC). Sampling at this point requires an ADC with higher resolution than that required after the IR mixer in wideband IF receivers, because in the former case the wanted signal and unwanted image are sampled. After the first mixer stage, the unwanted image can be much larger than the desired signal.

Although the low-IF architecture requires higher-performance ADCs than does the wideband IF architecture, the signal path to the ADC can be ac-coupled in the low-IF architecture, which in turn eliminates the need for complicated dc offset cancellation circuitry. *Another advantage of this low-IF topology is that part of the complex IR mixer is implemented in the digital domain with no gain and phase I/Q mismatches.* The I/Q imbalances introduced in the preceding analog sections can be corrected using adaptive techniques [13]. Therefore, this strategy shifts the hard specifications from the analog part to the ADCs. Since the performance of integrated ADCs is improving rapidly, this architecture will likely be preferred [12].

Finally, it should be noted that digitizing the received signal at the IF stage can also be employed in conventional heterodyne receiver systems. This approach is sometimes called *digital IF* [7]. In this architecture, the high ADC performance requirements are more challenging to accomplish within a reasonable power dissipation. Despite the advantage of avoiding the I and Q mismatches for typical first IFs in heterodyne receivers, this technique requires a prohibitively fast high-linearity high-dynamic-range ADC, currently limiting its utilization to only base stations [7].

CONCLUSION

In this tutorial, traditional and recent wireless receiver architectures suitable for a single-chip transceiver are reviewed. To simplify analysis of these architectures and gain more insight into their structures, complex signal representation is used. The advantages and disadvantages of each architecture are discussed with emphasis on practical considerations.

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BIOGRAPHIES

SHAHRIAR MIRABBASI [S] (shahriar@eecg.toronto.edu) received a B.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1990, and an M.A.Sc. degree in electrical engineering from the University of Toronto, Ontario, Canada, in 1997. During the summer of 1997 he worked at Gennum Corporation, Burlington, Ontario, Canada, on the design of cable equalizers for serial digital video andHDTV applications. He is currently working toward a Ph.D. degree in electrical engineering at the University of Toronto. His current research interests include highly integrable wireless transceiver architectures and bandwidth-efficient modulation schemes suitable for high data-rate communication systems.

KEN MARTIN [S'75-M'80-SM'89-F'91] received B.A.Sc., M.A.Sc., and Ph.D. degrees from the University of Toronto, Canada, in 1975, 1977, and 1980. From 1977 to 1978 he was a member of the scientific research staff at Bell Northern Research, Ottawa, Canada, where he did some of the early research in integrated switched-capacitor networks. Between 1980 and 1992 he was consecutively an assistant, associate, and full professor at the University of California at Los Angeles. In 1992 he accepted the endowed Stanley Ho Professorship in Microelectronics at the University of Toronto. He has co-authored a textbook entitled *Analog Integrated Circuit Design* (Wiley, 1997) in addition to three other books co-authored in cooperation with former Ph.D. students. His newest book, *Digital Integrated Circuit Design* (Oxford, 2000), was released in Oct. 1999. He has published over 100 papers and five patents. He was appointed Circuits and Systems IEEE Press Representative (1985–1986). He was selected by the Circuits and Systems Society for the Outstanding Young Engineer Award that was presented at the IEEE Centennial Keys to the Future Program in 1984. He was elected by the Circuits and Systems Society members to their administrative committee (ADCOM 1985-1987) and as a member of the Circuits and Systems BOG (1995-1997). He has served as Associate Editor of *Transactions on Circuits and Systems* from 1985 to 1987.

It should be noted that digitizing the received signal at the IF stage can also be employed in conventional heterodyne receiver systems. This approach is sometimes called "digital IF" architecture.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of Madhukar Reddy et al.	§	REQUEST FOR *EX PARTE*
	§	REEXAMINATION
U.S. Patent No. 9,210,362	§	
	§	Attorney Docket No.: 50348.106
Filed: February 5, 2015	§	
	§	
Priority: April 17, 2009	§	
	§	Customer No.: 27683
Issued: December 8, 2015	§	
	§	Proceeding No.: *to be assigned*
Title: WIDEBAND TUNER ARCHITECTURE	§	
	§	
	§	
	§	
	§	
	§	

REQUEST FOR EX PARTE REEXAMINATION

Mail Stop *Ex Parte* Reexam
Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the provisions of 35 U.S.C. §§ 301-307, Unified Patents, LLC ("Requester") hereby requests an *ex parte* reexamination of claims 1 and 11 of United States Patent No. 9,210,362 ("the '362 Patent," EX1001), which issued on December 8, 2015, to Madhukar Reddy et al., resulting from U.S. Patent Application No. 14/614,543 filed on February 5, 2015, claiming priority to U.S. Provisional Patent Application No. 61/170,526 filed on April 17, 2009. The '362 Patent is presently assigned to Entropic Communications, LLC ("Entropic"). The assignment to Entropic is recorded in the U.S. Patent and Trademark Office ("USPTO") at reel/frame 055899/0291.

Requester submits that this Request presents prior art references and analysis that are non-cumulative of the prior art that was before the Examiner during the original prosecution of the '362 Patent and that claims 1 and 11 of the '362 Patent are invalid over these references. Requester

therefore requests that an order for reexamination and an Office Action rejecting claims 1 and 11 be issued.

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I. STATEMENT POINTING OUT SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY

Prior to describing the substantial new questions of patentability presented in this Request, provided below is an overview of the '362 Patent, a discussion of claim construction, and a listing of the prior art being discussed in the present Request.

A. Overview of the '362 Patent and its History

(i) Scope of the '362 Patent

The '362 Patent is titled "Wideband Tuner Architecture" and it is directed to a "wideband receiver system" which "comprises a mixer module, a wideband analog-to-digital converter (ADC) module, and digital circuitry." '362 Patent (EX1001), Abstract. The '362 Patent Abstract parallels claim 11 closely, and states:

> "The mixer module is configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels. The wideband ADC module is configured to digitize the swatch of frequencies comprising the plurality of desired television channels and the plurality of undesired television channels. The digital circuitry is configured to select the desired plurality of television channels from the digitized plurality of frequencies, and output the selected plurality of television channels to a demodulator as a digital datastream."

'362 Patent (EX1001), Abstract.

Copies of the '362 Patent and its file history are provided as Exhibits 1001 and 1002, respectively. To provide a background of the '362 Patent, independent claim 11, for which reexamination is requested, is reproduced below.

> 11. A method comprising:
> in a wideband receiver system:
> downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;
> digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said

> plurality of desired television channels and said plurality of undesired television channels;
>
> selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and
>
> outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.

However, similar architectures and methods were known prior to the '362 Patent. For example, prior to the '362 Patent's priority date, McNeely disclosed a "method and apparatus … for simultaneous reception of a plurality of digital RF channels." McNeely (EX1003), Abstract. Pugel similarly disclosed a "desire to have a solution providing receiving and re-synthesizing of channels for distribution in a more optimal manner" and thus described a method and system for receiving signals "containing a plurality of channels" and "selecting channels from the plurality of channels" for transmission and output. Pugel (EX1004), 3:15–31. Claims 1 and 11 are rendered obvious by the teachings of Pugel, McNeely, and Gomez, as shown by the analysis presented in this request.

(i) Prosecution History of the '362 Patent

The '362 Patent issued from U.S. Application No. 14/614,543, filed on February 5, 2015 (the "'543 Application"). The '543 Application claims priority to multiple previous applications, the earliest of which, U.S. Provisional Patent Application No. 61/170,526, was filed April 17, 2009.

The claims filed with the '543 Application were not amended during prosecution. The claims were only rejected once, under the ground of double patenting over the parent patent. EX1002, pp. 80–84. The examiner did not reject the claims as anticipated by or obvious over any prior art. In the Notice of Allowance, the examiner provided "a statement of reasons for the indication of allowable subject matter: the prior art made of record teach a wideband receiver system but do not also teach digital circuitry configured to select a plurality of desired television channels from the digitized plurality of frequencies and output said plurality of television channels to a demodulator as a digital datastream." *Id.* at 62.

However, this Request presents and applies new prior art with analysis that discloses or renders obvious every feature of claims 1 and 11. Specifically, McNeely, Pugel, and Gomez were not considered by the examiner and render obvious each limitation of claims 1 and 11. Thus, the prior art presented in this Request, along with the analysis presented by Mr. Lipoff (attached as Exhibit 1008), presents substantial new questions of patentability.

Requester therefore asks that an Order for Reexamination be issued and that the reexamination proceeding continue to reject and cancel claims 1 and 11 of the '362 Patent.

B. Level of Ordinary Skill in the Art

A person of ordinary skill in the art at and before the priority date of the '362 Patent ("POSITA") would have had a bachelor's degree in electrical engineering, or a related subject, and two to three years of work experience in the field of radio frequency systems (e.g., cable television systems). A lack of experience can be remedied with additional education (e.g., a Master's degree), and likewise, a lack of education can be remedied with additional work experience (e.g., 5–6 years). Lipoff (EX1008), ¶¶ 45–47.

C. Claim Construction

"During patent examination, the pending claims must be 'given their broadest reasonable interpretation consistent with the specification.'" MPEP § 2111. The '362 Patent has not yet expired; thus, the broadest reasonable interpretation standard applies. MPEP § 2258. The present Request presents the following claim analysis in a manner that is consistent with the broadest reasonable interpretation consistent with the specification. Requester provides analysis below for consistency with a district court interpretation of the challenged claims.

(i) Order of Steps in Claim 11

In parallel district court litigation, the court construed claim 11 as follows: "[i]n Claim 11 of the '362 Patent, the 'digitizing …' step must be performed before the 'selecting …' step, and the 'selecting …' step must be performed before the 'outputting …' step. No other order of steps is required." EX1007, p. 52. In the court's analysis, the court noted that "the 'downconverting …' step and the 'digitizing …' step both refer to the same 'plurality of frequencies' without any indication that one of these steps must necessarily be performed before the other." *Id.* at p. 51.

D. Listing of Prior Art Patents and Printed Publications

Reexamination of claims 1 and 11 of the '362 Patent[1] is requested in view of the following references:

Exhibit 1003 ("McNeely") WO 2006/119490 to David Lowell McNeely, filed May 4, 2006, published November 9, 2006, which is prior art at least under pre-AIA 35 U.S.C. § 102(b).

Exhibit 1004 ("Pugel") WO 2007/145637 to Michael Anthony Pugel, filed June 16, 2006, published December 21, 2007, which is prior art at least under pre-AIA 35 U.S.C. § 102(b).

Exhibit 1005 ("Gomez") U.S. Patent No. 8,224,274 to Ramon Gomez et al., filed December 17, 2008, and issued July 17, 2012, which is prior art at least under pre-AIA 35 U.S.C. § 102(e).

McNeely, Pugel, and Gomez[2] were not cited or applied during the original prosecution of the '362 Patent. As demonstrated below, McNeely, Pugel, and Gomez present substantial new questions of patentability.

(i) Overview of McNeely

McNeely describes an "apparatus and method for performing frequency translation." McNeely (EX1003), Abstract. McNeely's apparatus includes a "receiver … for receiving and digitizing a plurality of first signals" and "recovering a set of selected channels from the plurality of first signals." *Id.* McNeely also describes "combining the set of selected channels to form a second signal and transmitting the second signal." *Id.* at 3:27–31.

McNeely is analogous art to the '362 Patent. Lipoff (EX1008), ¶¶ 61–62. The field of endeavor of the '362 Patent is "wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum." '362 Patent (EX1001), 1:15–18. McNeely discloses a receiver and

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[1] The '362 Patent issued from an application filed prior to the enactment of the America Invents Act ("AIA"). Thus, the pre-AIA statutory framework applies.

[2] U.S. Patent 7,421,259 to Gomez appears on the face of the '362 Patent, but is unrelated to the reference applied in this Request.

techniques applicable to signals occupying "1 GHz of bandwidth," (McNeely (EX1003), 7:9–11)[3] and is thus within the field of endeavor of the '362 Patent. McNeely is also reasonably pertinent to at least one problem addressed by the '362 Patent. The '362 Patent states it is "desirable to have wideband receiver systems that can increase the dynamic range without requiring expensive data conversion, filtering and channel selection at the demodulator." That is, the '362 Patent seeks to perform conversion, filtering, and channel selection from signals before those signals reach a demodulator. McNeely similarly discloses techniques of conversion, filtering and channel selection, and combined with the teachings of Pugel below, performs these functions on signals before those signals reach a demodulator. Lipoff (EX1008), ¶ 62. Accordingly, McNeely is analogous art to the '362 Patent for this reason as well.

(ii) Overview of Pugel

Pugel relates to "multi-channel television reception." Pugel (EX1004), ¶ 1. Pugel notes a "need for a digital television receiver capable of simultaneously receiving a plurality of channels." *Id.* at ¶ 8. Pugel describes a "method and apparatus … for simultaneous reception of a plurality of digital RF channels." Pugel (EX1004), Abstract. Pugel's method includes "receiving at least one multichannel RF input signal" and separating the RF input signal. *Id.* at ¶ 11. Subsequently, the analog signals are converted into "digital signals" and then demultiplexed "to recover the plurality of digital RF channels." *Id.* Pugel's method also includes "demodulating the plurality of digital RF channels." *Id.* at ¶ 12.

Pugel is analogous art to the '362 Patent. Lipoff (EX1008), ¶¶ 64–65. The field of endeavor of the '362 Patent is "wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum." '362 Patent (EX1001), 1:15–18. Pugel discloses techniques applicable to

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[3] The '362 Patent explains that a tuner, or receiver, designed to "concurrently receive several TV channels" is referred to as wideband (1:24–27), and it provides an example of a wideband receiver system having a "single very wide-band tuner" that receives signals having "80 MHz" of bandwidth (4:16–25). Because McNeely's receiver techniques are applicable to signals occupying 1 GHz of bandwidth (which is greater than the '362 Patent's example bandwidth), it too describes a wideband receiver. Lipoff (EX1008), ¶ 61 n.1.

"analog signals of differing frequency ranges" and is thus within the field of endeavor of the '362 Patent.[4] Pugel is also reasonably pertinent to at least one problem addressed by the '362 Patent. The '362 Patent states it is "desirable to have wideband receiver systems that can increase the dynamic range without requiring expensive data conversion, filtering and channel selection at the demodulator." As detailed above, the '362 Patent seeks to perform conversion, filtering, and channel selection on received signals before those signals reach a demodulator. Pugel discloses techniques of conversion, filtering and channel selection before signals reach a demodulator. Lipoff (EX1008), ¶ 65. Accordingly, Pugel is analogous art to the '362 Patent for this reason as well.

(iii) Overview of Gomez

Gomez describes a "frequency translation module for a broadband multi-channel communication system." As pertinent to the analysis in this Request, Gomez's frequency translation module (FTM) 100 includes a "tuner 201" which includes an "amplifier 300" and "mixers 301 and 303." Gomez (EX1005), 4:4–6. The mixer 301 may perform down conversion on a signal. *See id.* at 4:4–19.

Gomez is analogous art to the '362 Patent. Lipoff (EX1008), ¶¶ 67–68. The field of endeavor of the '362 Patent is "wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum." '362 Patent (EX1001), 1:15–18. Gomez similarly describes applicability to "a broadband multi-channel communication system" and is thus within the field of endeavor of the '362 Patent. For example, just as the '362 Patent discusses that wideband receivers receive multiple channels, Gomez also discloses its receivers may "receive a signal" including a "set of high-definition channels." Gomez (EX1005), 3:40–50. Gomez is also reasonably pertinent to at least one problem addressed by the '362 Patent. One problem addressed by the '362 Patent is the

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[4] As detailed above, the '362 Patent provides an example of a wideband receiver system having a "single very wide-band tuner" that receives signals having "80 MHz" of bandwidth (4:16–25). Pugel's receiver techniques, in one example, apply to signals having 300 MHz of bandwidth, (which is greater than the '362 Patent's example bandwidth), and thus it too describes a wideband receiver. Lipoff (EX1008), ¶ 64 n.2.

need for "expensive digital processing circuitry" and Gomez likewise addresses the issue of frequency translation modules being too "costly … for some applications." Gomez (EX1005), 1:49–52. Accordingly, Gomez is analogous art to the '362 Patent for this reason as well.

E. McNeely, Pugel, and Gomez Each Present Substantial New Questions of Patentability

As shown below, Requester submits that the prior art references McNeely, Pugel, and Gomez raise a "substantial question of patentability" because "the teaching of the (prior art) patents and printed publications is such that a reasonable examiner would consider the teaching to be important in deciding whether or not the claim is patentable." *See* MPEP § 2242 (emphasis in original). Further, the "same question of patentability as to the claim has not been decided by the Office in an earlier concluded examination or review of the patent" at least because none of the references were before the Office during the original prosecution of the '362 Patent. *See id.*; *id.* § 2216. Thus, as presented herein, each of McNeely, Pugel, and Gomez present a substantial new question of patentability.

The present Request proposes the following rejection based on McNeely, Pugel, and Gomez:

Proposed Rejection A1: Claims 1 and 11 are rendered obvious by McNeely and Pugel under 35 U.S.C. § 103(a).

Proposed Rejection B1: Claims 1 and 11 are rendered obvious by Pugel and Gomez under 35 U.S.C. § 103(a).

(i) McNeely Presents Substantial New Questions of Patentability

As demonstrated in the proposed rejection A1 below, McNeely, when combined with the teachings of Pugel, renders obvious claims 1 and 11 of the '362 Patent. Specifically, McNeely discloses or at least renders obvious substantially all elements of claims 1 and 11. McNeely therefore presents a substantial new question of patentability, and a reasonable examiner would consider the reference important in determining whether claims 1 and 11 are patentable, because McNeely was not cited by the examiner. A detailed explanation of the pertinence and manner of applying McNeely to the claim for which reexamination is requested is set for in Section II, below.

(ii) Pugel Presents Substantial New Questions of Patentability

As demonstrated in the proposed rejections A1 and B1 below, Pugel, when combined with the teachings of McNeely or Gomez, renders obvious claims 1 and 11 of the '362 Patent. Specifically, in the combination with McNeely, Pugel is relied upon to teach outputting television channels to a demodulator. In the combination with Gomez, Pugel is relied upon to disclose or at least render obvious substantially all elements of claims 1 and 11. Pugel therefore presents substantial new questions of patentability, and a reasonable examiner would consider the reference important in determining whether claims 1 and 11 are patentable, because Pugel was not cited by the examiner. A detailed explanation of the pertinence and manner of applying Pugel to the claim for which reexamination is requested is set forth in Section II below.

(iii) Gomez Presents Substantial New Questions of Patentability

As demonstrated in the proposed rejection B1 below, Gomez, when combined with the teachings of Pugel, renders obvious claims 1 and 11 of the '362 Patent. Specifically, Gomez discloses or teaches downconversion by a "mixer module" as recited in claims 1 and 11. Gomez therefore presents substantial new questions of patentability, and a reasonable examiner would consider the reference important in determining whether claims 1 and 11 are patentable, because Gomez was not cited by the examiner. A detailed explanation of the pertinence and manner of applying Gomez to the claim for which reexamination is requested is set forth in Section II below.

II. DETAILED EXPLANATION OF THE PERTINENCE AND MANNER OF APPLYING THE PRIOR ART REFERENCES TO EVERY CLAIM FOR WHICH REEXAMINATION IS REQUESTED

A. Proposed Rejections of the Claim

The present request presents proposed rejections based on the references McNeely, Pugel, and Gomez.

Proposed rejections A1 and B1 are based on obviousness under 35 U.S.C. § 103(a). Requester notes that, even if there are minor differences between cited disclosures of the prior art and the claimed concepts, the claims are still obvious, as a POSITA would not have appreciated "some new synergy" or unexpected results from the limitations given the disclosures of the prior art and the general knowledge of a POSITA. *KSR Intern. Co. v. Teleflex Inc.*, 550 US 398, 417

(2007). When compared with the prior art described below and in light of the knowledge of a POSITA, any "differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains." 35 U.S.C. § 103.

The proposed rejections are listed below and above and are described in further detail in the claim chart that follows below.

(i) Proposed Rejection A1: Claims 1 and 11 are rendered obvious by McNeely in view of Pugel under 35 U.S.C. § 103(a).

U.S. Patent No. 9,210,362	McNeely/Pugel
Claim 11[5]	
[11.0] A method comprising: in a wideband receiver system:	McNeely discloses or at least renders obvious a *method … in a wideband receiver system* (e.g., McNeely's apparatus including a receiver). First, McNeely discloses a *method*: "The disclosed embodiments relate to an apparatus and **method** for performing frequency translation." McNeely (EX1003), Abstract. Second, McNeely's method is performed *in a wideband receiver system*. The '362 Patent states: "Receivers used to down-convert and selectively filter TV channels are referred to as tuners, and **tuners designed to concurrently receive several TV channels are referred to as wideband tuners**." '362 Patent (EX1001), 1:24-27. Thus, a POSITA would have recognized a *wideband receiver system* as one which concurrently receives several TV channels. McNeely discloses such a system, as it states: "The present invention relates to an **apparatus** and method for performing frequency translation. The **apparatus includes a receiver** for receiving and digitizing a plurality of first signals, each signal containing channels and for simultaneously

[5] Emphasis added throughout unless otherwise specified.

U.S. Patent No. 9,210,362	McNeely/Pugel
	recovering a set of selected channels from the plurality of first signals." McNeely (EX1003), 3:20–24. "The single L-band signal, as an analog input, is processed through an RF processing block 210. The RF processing block 210 may contain circuitry for filtering undesired energy outside the signal frequency range, may correct for any frequency response errors introduced, and may amplify the signal to a level necessary for input to the analog to digital (A/D) converter 220." McNeely (EX1003), 9:7–12. "As previously described, each L-band signal may occupy 1 GHz of bandwidth, and a typical customer premises cable installation may only support less than 2 GHz of total signal bandwidth. The FTM 110 extracts certain ranges of frequencies containing selected physical channels as portions of the three L-band signals provided." McNeely (EX1003), 7:9–15. Because McNeely describes a receiver system that extracts certain ranges of frequencies containing multiple physical channels, it discloses, or at least renders obvious, performing its methods *in a wideband receiver system* as recited. Lipoff (EX1008), ¶¶ 70–75.

U.S. Patent No. 9,210,362	McNeely/Pugel
[11.1] downconverting, by a mixer module[6] of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;	McNeely discloses, or at least renders obvious *downconverting* (e.g., processing the L-band signal by positioning it in the correct frequency range), *by a mixer module* (e.g., mixing circuits of block 210) *of said wideband receiver system* (e.g., McNeely's apparaus including a receiver), *a plurality of frequencies* (e.g., the L-band signal) *that comprises a plurality of desired television channels* (e.g., set of selected channels) *and a plurality of undesired television channels* (e.g., the set of channels not selected). First, McNeely discloses *a mixer module of said wideband receiver system*: "The input RF processing block 210 may also contain any **mixing circuits** necessary to position the L-band signal in the correct frequency range for operation of the A/D converter 220." McNeely (EX1003), 9:12–15; Lipoff (EX1008), ¶ 77.

[6] The claimed "mixer module" does not invoke 35 U.S.C. § 112 ¶ 6 because a POSITA would have understood the term "to have a sufficiently definite meaning as the name for the structure that performs the function." MPEP 2181.A; Lipoff (EX1008), ¶¶ 40–42.

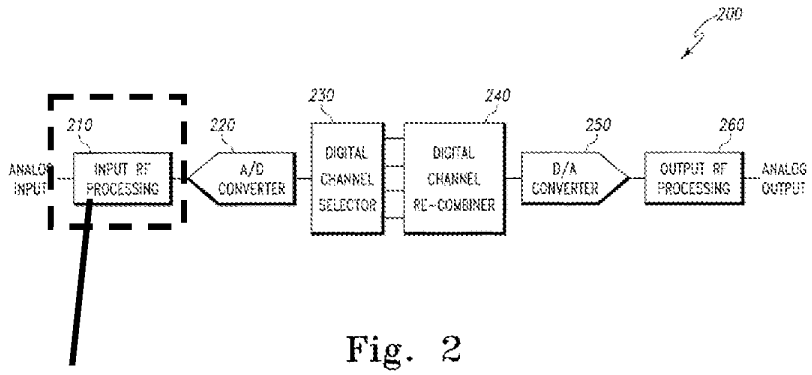


Fig. 2

McNeely (EX1003), Fig. 2 (annotated).

Second, McNeely teaches *downconverting ... a plurality of frequencies*.

As detailed in the above disclosure, the mixing circuits "position the L-band signal" (the analog input in Fig. 2) "in the correct frequency range." McNeely (EX1003), 9:12–15. In McNeely, "each L-band signal may occupy 1 GHz of bandwidth" (*id.*, 7:9–11) and thus, each signal comprises a *plurality of frequencies* as recited. Additionally, McNeely teaches that the "L-band signal" includes multiple "physical channels" (*id.*, 14:26–28) and thus, each L-band signal comprises a *plurality of frequencies* as recited.

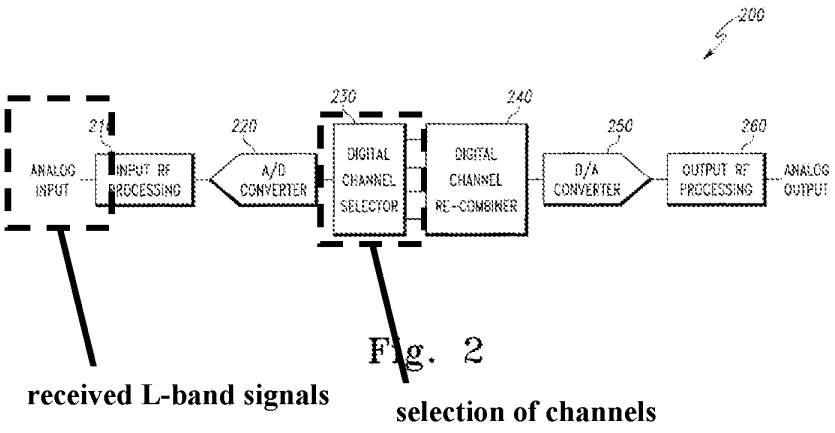
This disclosure corresponds to, and teaches to a POSITA, *downconverting*, because a POSITA would have recognized that it was well-known for receivers to use frequency translation techniques (like the technique of positioning the L-band signal disclosed in McNeely) to downconvert RF signals to a lower frequency. Lipoff (EX1008), ¶¶ 78–80 (citing, e.g., Tseng (EX1011), p. 1 ("directly downconvert the desired RF signal"); Li (EX1012), p. 1 ("Downconversion mixer is one of the important building blocks for RF transceviers"); Mirabbasi (EX1013), p. 133 ("frequency downconversion" is "an essential operation in any RF receiver.");

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	Feng (EX1006), p. 19 (in "modern communications, frequency translation is used in receivers to **downconvert RF to a lower frequency**."); '362 Patent (EX1001), 1:27–29 (admitting as prior art that "[e]xisting tuners for these applications **downconvert a swath of channels to an intermediate frequency**, which are then sent to a demodulator.")). For example, the Tseng paper states that downconverting a desired RF signal "can significantly relax the demand for fast ADCs." Tseng (EX1011), p. 1; *see also* Mirabbasi (EX1013), p. 136 (Figure 7 depicting downconversion before digitizing by an ADC). Consistent with the background knowledge of a POSITA, because McNeely also performs frequency positioning before digitizing by an analog-to-digital converter (ADC) as described below in limitation [11.2], a POSITA would have recognized McNeely to teach *downconverting* as recited. Additionally, McNeely teaches that the L-band signal input to the RF processing block 210 is in the 1–2 GHz frequency range (*see* McNeely (EX1003), 7:26–28). McNeely further teaches that the A/D converter acts upon processed L-band signals "between the frequencies of 975 and 1425 MHz." *Id.* at 9:16–19. Thus, McNeely repositions the signals to a lower frequency range and performs *downconverting* as recited. Lipoff (EX1008), ¶ 81. McNeely's disclosure is described in the context of a receiver, as detailed in the analysis of limitation [11.0] and thus, McNeely's description of "position[ing] the L-band signal in the correct frequency range" is a teaching of *downconverting ... a plurality of frequencies* as recited. Lipoff (EX1008), ¶ 80.[7]

[7] McNeely's later disclosure of digital channel selector 230 proceeding to "down-convert each of the individual physical channels that have been selected" does not impact this teaching of McNeely, as a POSITA would have recognized that this later reference to downconversion relates to later downconversion of **digital** signals, and thus does not impact McNeely's teaching of

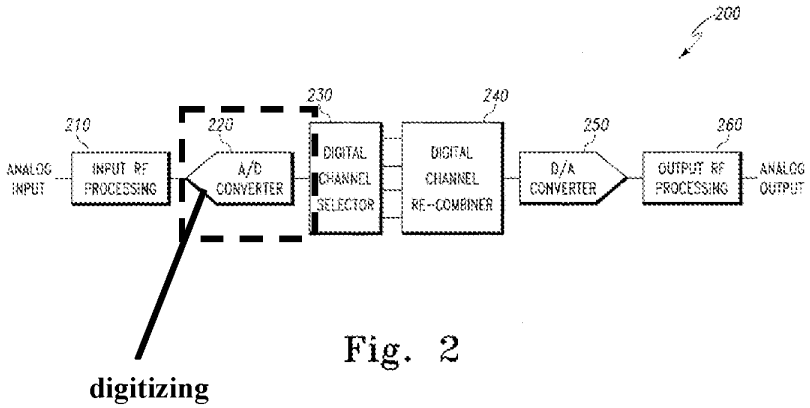
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	Third, McNeely teaches that the *plurality of frequencies … comprises a plurality of desired television channels and a plurality of undesired television channels*: "The apparatus includes a receiver for receiving and digitizing a plurality of first signals, each signal containing channels and for simultaneously **recovering a set of selected channels** from the plurality of first signals. The apparatus also includes a transmitter for combining the set of selected channels to produce a second signal." McNeely (EX1003), Abstract. McNeely also discloses: "A method (600) for providing frequency translation comprising: receiving (602) a first signal having a plurality of different frequency channels; selecting (606) a set of frequency channels from said plurality of different frequency channels;…" McNeely (EX1003), 22:7–11 (claim 13). Consistent with claim 13 and McNeely's disclosure, therefore, analog L-band signals ("a first signal having a plurality of different frequency channels") are received, processed, converted to digital, and then channel selection occurs in the digital channel selector 230

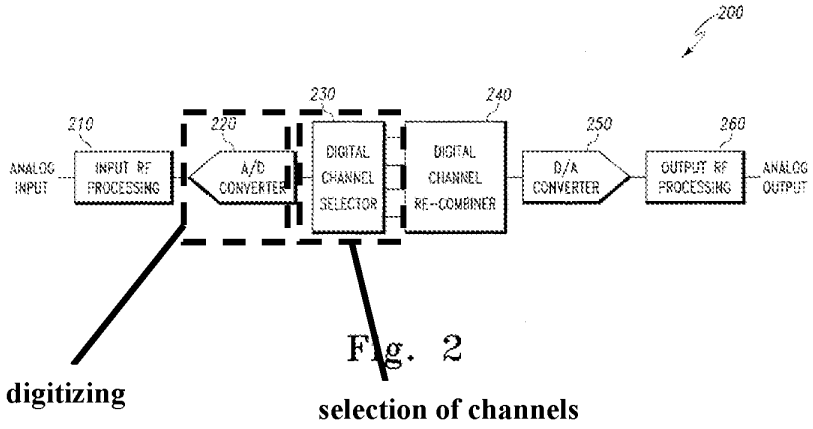
downconversion in its description of positioning L-band **analog** signals in the correct frequency range cited here. Lipoff (EX1008), ¶ 81.

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	("selecting (606) a set of frequency channels from said plurality of different frequency channels"). Thus, the received L-band signals (the received *plurality of frequencies*) includes the selected channels and the unselected channels (the *plurality of desired television channels and [] plurality of undesired television channels*). Additionally, in McNeely, the "selected channels" are recovered by the digital channel selector 230 in Figure 2, which occurs after the downconversion of the received signals (the analog input) by mixing circuits in the input RF processing block 210; thus, the received signals (the *plurality of frequencies*) includes the selected channels and the unselected channels (the *plurality of desired television channels and [] plurality of undesired television channels*).  **McNeely (EX1003), Fig. 2 (annotated)** The "set of selected channels" corresponds to the recited *plurality of desired television channels*. Lipoff (EX1008), ¶¶ 82–86. Further, because McNeely's receiver recovers a set of selected channels from the first signals, the channels not recovered from the first signals would correspondingly be the *plurality of undesired television channels* as recited. Lipoff (EX1008), ¶ 86.

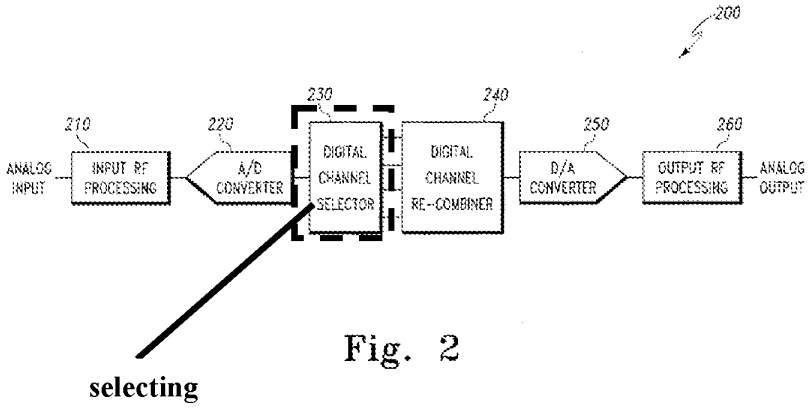
U.S. Patent No. 9,210,362	McNeely/Pugel
	Thus, McNeely discloses, or at least renders obvious, this limitation. Lipoff (EX1008), ¶¶ 76–87.
[11.2] digitizing, by a wideband analog-to-digital converter (ADC) module[8] of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;	McNeely discloses, or at least renders obvious *digitizing* (e.g., digitizing the processed L-band signal into a series of samples), *by a wideband analog-to-digital converter (ADC) module* (e.g., A/D converter 220) *of said wideband receiver system* (e.g., McNeely's receiver system), *said plurality of frequencies* (e.g., the downconverted L-band signals) *comprising said plurality of desired television channels* (e.g., set of selected channels) *and said plurality of undesired television channels* (e.g., the set of unselected channels). First, McNeely discloses *digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system*: "The **A/D converter 220 digitizes the processed L-band signal into a series of samples**, each sample containing a group of bits. In an exemplary embodiment, the processed satellite signal is located between the frequencies of 975 and 1425 MHz. The A/D converter 220 samples the processed L-band signal at a rate of 933 megasamples per second (MSPS) generating a digital signal containing a series of samples, each sample represented by 8 bits. The A/D converter 220 may also generate a translated frequency image of the L-band signal essentially translating the signal from an initial frequency range in the analog domain to a different frequency range based on sampling principles."

[8] The claimed "wideband analog-to-digital converter (ADC) module" does not invoke 35 U.S.C. § 112 ¶ 6 because a POSITA would have understood the term "to have a sufficiently definite meaning as the name for the structure that performs the function." MPEP 2181.A; Lipoff (EX1008), ¶¶ 43–44.

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	McNeely (EX1003), 9:16–26. Because McNeely's A/D converter operates on a processed L-band signal between the frequencies of 975 and 1425 MHz (i.e., 450 MHz of bandwidth), the A/D converter is a *wideband analog-to-digital converter (ADC) module* as recited, at least because the 450 MHz bandwidth in McNeely is greater than the example wideband receiver system with an analog-to-digital converter in the '362 Patent which operates on a total of 80 MHz of bandwidth. Lipoff (EX1008), ¶¶ 89–90.  Fig. 2 **McNeely (EX1003), Fig. 2 (annotated)** "Turning now to FIG. 2 a block diagram 200 of an embodiment of the present invention is shown. The diagram shows an implementation of the FTM 110 that includes digital signal processing in order to increase the performance and available bandwidth for selected channels." McNeely (EX1003), 9:1–5. Second, because the A/D converter 220 in McNeely converts the signals from the input RF processing block 210, for the same reasons

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	as set forth in limitation [11.1], McNeely discloses, or at least renders obvious, that the digitizing is performed on the *plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels* as recited. Lipoff (EX1008), ¶¶ 91–92.  Fig. 2 **McNeely (EX1003), Fig. 2 (annotated)** Specifically, as detailed in the analysis of limitation [11.1], *supra*, in McNeely, the "selected channels" are recovered by the digital channel selector 230 in Figure 2, which occurs after the downconversion of the received signals by mixing circuits in the input RF processing block 210 and digitizing by A/D converter 220 thus, the digitized signals (the *plurality of frequencies*) includes the selected channels and the unselected channels (the *plurality of desired television channels and [] plurality of undesired television channels*). Thus, McNeely discloses, or at least renders obvious, this limitation. Lipoff (EX1008), ¶¶ 88–93.
[11.3] selecting, by digital circuitry of said wideband	McNeely discloses, or at least renders obvious *selecting* (e.g., selecting), *by digital circuitry* (e.g., digital channel selector 230) *of*

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receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and	*said wideband receiver system* (e.g., McNeely's receiver system), *said plurality of desired television channels* (e.g., set of selected channels) *from said digitized plurality of frequencies* (e.g., the output of A/D converter 220): "The **A/D converter 220 digitizes the processed L-band signal into a series of samples**, each sample containing a group of bits. McNeely (EX1003), 9:16–26. As detailed above in the analysis of limitation [11.2], the L-band signal comprises the *plurality of desired television channels*. Lipoff (EX1008), ¶¶ 94–95. After digitizing the L-band signal into the samples, McNeely discloses: "The **digital channel selector 230** receives the sampled [L-band] signal and **proceeds to select** and down-convert **each of the individual physical channels that have been selected**. After processing, each of the selected individual channels are located within the same frequency range at or near to baseband, but are contained as individual signals on separate signal lines. The number of bits representing each selected individual channel may be different from the original sampled signal based on the processing method employed. The use of digital signal processing and processing of the signal in parallel permits narrower filtering constraints and more efficient channel selection within the FTM 110." McNeely (EX1003), 10:1–11.

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	 Fig. 2 **McNeely (EX1003), Fig. 2 (annotated)** "7. The apparatus (500) of claim 1, wherein said receiver (530a-c) further comprises a selector (360) operatively connected to said distributor (350) for selecting said plurality of selected channels." McNeely (EX1003), claim 7. "13. A method (600) for providing frequency translation comprising:… selecting (606).a set of frequency channels from said plurality of different frequency channels;" McNeely (EX1003), claim 13. "22. An apparatus (500) for frequency translation comprising.…

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	means for selecting (530a-c) a set of channels from said set of signals;" McNeely (EX1003), claim 22. Because McNeely discloses selecting each of the individual physical channels that have been selected by the digital channel selector, which is *digital circuitry*, it discloses, or at least renders obvious, *selecting, by digital circuitry of said wideband receiver system* (e.g., digital channel selector 230), *said plurality of television channels from said digitized plurality of frequencies* (the individual physical channels that have been selected). Lipoff (EX1008), ¶¶ 94–97.
[11.4] outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.	McNeely and Pugel render obvious *outputting, by said digital circuitry* (e.g., digital channel selector 230 and digital channel re-combiner 240) *of said wideband receiver system* (e.g., McNeely's receiver system), *said selected plurality of television channels* (e.g., McNeely's selected channels) *to a demodulator* (e.g., Pugel's demodulator) *as a digital datastream* (e.g., selected digital signal). First, McNeely discloses *outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels ... as a digital datastream*: "Each of the individual selected channels is provided to the digital channel re-combiner 240. The **digital channel re-combiner 240** frequency translates the individual selected channels each to a different and separate frequency range and combines these signals together to form **a single selected digital signal**." McNeely (EX1003), 10:12–16. The output of "digital channel re-combiner 240" (i.e., the "single selected digital signal") is *a digital datastream* because, as shown in Figure 2, the output is transmitted (in McNeely) to the D/A converter

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	(digital-to-analog converter), and thus, a POSITA would have recognized the output as being a *digital datastream* as recited. Lipoff (EX1008), ¶¶ 99–100. In McNeely, the "selected digital signal" is supplied to the digital to analog (D/A) converter 250. However, it was known at the time of the '362 Patent that such digital signals could, and would be provided *to a demodulator* as recited. Lipoff (EX1008), ¶ 101. Specifically, Pugel teaches "demodulating the plurality of digital RF channels" in a system which "permits substantially simultaneous reception of a plurality of digital cable television channels within a single digital receiver circuit." Pugel (EX1004), ¶¶ 11–12. Pugel also discloses: "The converted digital signals are coupled to the digital tuner 130, which demultiplexes the converted digital signals to generate a plurality of digital channel signals. **Each digital channel signal is then coupled to a separate demodulator 141, 142, 143**, which performs demodulation and forward-error-correction (FEC) operations appropriate for the content of that digital channel." Pugel (EX1004), ¶ 27. "[A] plurality of demodulator circuits is coupled to the digital tuner, the plurality of demodulator circuits including at least a first demodulator circuit configured to receive and demodulate a first channel of the plurality of digital RF channels and a second demodulator circuit being configured to receive and demodulate a second channel of the plurality of digital RF channels."

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	Pugel (EX1004), ¶ 10. Thus, Pugel teaches *outputting ... to a demodulator* as recited. The combined teachings of McNeely and Pugel therefore render obvious this limitation. Lipoff (EX1008), ¶¶ 103–104. A POSITA would have been motivated to combine the teachings of McNeely and Pugel. Lipoff (EX1008), ¶¶ 105–109. First, McNeely acknowledges that demodulators were known: "Likewise, other than the inventive concept, transmission concepts such as satellite transponders, down-link signals, eight-level vestigial sideband (8-VSB), Quadrature Amplitude Modulation (QAM), and receiver components such as a radio-frequency (RF) front-end, or receiver section, such as a low noise block, tuners, and **demodulators** is assumed." McNeely (EX1003), 5:16–21. "At each installation location in the premises 120, the selected signal is provided to a standalone terminal 130 or to a combination settop box 140a-c and display device 150a-c. The terminal 130 and settop box 140a-c operate in a similar manner. Each of them receive the selected signal, tune to the desired physical channel within the selected signal, **demodulate the physical channel to produce a transport stream**, and extract the desired bit stream(s) from the transport stream." McNeely (EX1003), 8:1–7. The '362 Patent confirms demodulators were known, as it discloses in the Background:

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	"Existing tuners for these applications down convert a swath of channels to an intermediate frequency, **which are then sent to a demodulator.** Because the swath of channels is not contiguous, this swath includes the desired channels as well as undesired channels. The demodulator employs a high-speed data converter to capture this swath of desired and undesired channels in the digital domain and subsequently filters out the desired channels." '362 Patent (EX1001), 5:27-34. Given this knowledge in the art, a POSITA would have been motivated to combine the teachings of McNeely with Pugel as doing so would have been no more than the combination of known prior art elements. McNeely and Pugel disclose each and every limitation of the claims, albeit not within one reference. A POSITA could have, and would have been motivated to combine the teachings of McNeely with those of Pugel to provide for display of the selected TV channels on a display device (e.g., display device 150a-c in McNeely). In combination, each element performs the same function as previously: McNeely's apparatus downconverts, digitizes, and selects channels, and Pugel provides a demodulator that demodulates the channels for display. Additionally, the results of the combination would have been predictable, as McNeely acknowledges that demodulation was known in the context of its methods. Thus, a POSITA would have combined the teachings of McNeely and Pugel to render obvious this limitation. Lipoff (EX1008), ¶ 108. Additionally, a POSITA would have been motivated to combine the teachings of McNeely with Pugel as doing so would have been nothing more than the substitution of one known element for another to obtain predictable results. Specifically, combining the references would have involved no more than substituting McNeely's D/A

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	converter and output RF processing with Pugel's demodulator teachings. As detailed above, demodulators were well-known at the time of the '362 Patent, as Pugel discloses and as the '362 Patent itself admits. A POSITA would have found it straightforward to replace McNeely's components with Pugel's demodulator, and the results of such a substitution would have been predictable, as Pugel's demodulator would perform the same function in the combination as it did previously alone. Thus, a POSITA would have combined the teachings of McNeely and Pugel to render obvious this limitation. Lipoff (EX1008), ¶ 109.

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Claim 1	
[1.0] A wideband receiver system comprising:	*See* analysis of limitation [11.0], *supra*.
[1.1] a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;	*See* analysis of limitation [11.1], *supra*.
[1.2] a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;	*See* analysis of limitation [11.2], *supra*.
[1.3] digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and	*See* analysis of limitation [11.3], *supra*.
[1.4] [digital circuitry configured to:]… output said selected plurality of television channels to a	*See* analysis of limitation [11.4], *supra*.

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demodulator as a digital datastream.	

(ii) Proposed Rejection B1: Claims 1 and 11 are obvious over Pugel in view of Gomez under 35 U.S.C. § 103(a).

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Claim 11	
[11.0] A method comprising: in a wideband receiver system:	Pugel discloses or at least renders obvious a *method … in a wideband receiver system* (e.g., Pugel's apparatus that receives input signals). First, Pugel discloses a *method*: "A **method** (400) processing signals comprising the steps of:" Pugel (EX1004), claim 18. Second, Pugel discloses a method *in a wideband receiver system*. The '362 Patent states: "Receivers used to down-convert and selectively filter TV channels are referred to as tuners, and **tuners designed to concurrently receive several TV channels are referred to as wideband tuners**." '362 Patent (EX1001), 1:24-27. Thus, a POSITA would have recognized a *wideband receiver system* as one which concurrently receives several TV channels. Pugel discloses: "An apparatus (100), comprising: first means for processing (111) an input signal comprising **signals in a first frequency band and signals in a second frequency band** to produce a first

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	analog signal including signals in the first frequency band and substantially excluding the signals in the second frequency band; second means for processing (112) the input signal comprising signals in a first frequency band and signals in a second frequency band to produce a second analog signal including signals in the second frequency band and substantially excluding the signals in the first frequency band;" Pugel (EX1004), claim 1. "The apparatus (100) of claim 1 **wherein said apparatus (100) processes frequencies between about 5 MHz and about 900 MHz**." Pugel (EX1004), claim 16. "A method and apparatus is presented for simultaneous reception of a plurality of digital RF channels. Specifically, N amplifier-filter circuits (111, 112, 113) are configured to receive and separate a multichannel analog RF input signal into N analog signals, each including a different frequency band." Pugel (EX1004), Abstract. "In operation, according to one embodiment, a multichannel analog RF input signal received at input coupler 101 is split into a plurality of substantially identical signals at splitter 102. Splitter 102 may include one or more amplifiers, filters, or other components (not shown) which reduce or overcome insertion loss or other adverse effects of the split, as should be apparent to one of ordinary skill in the art.

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	The plurality of amplifier-filter circuits 111, 112, 113 then segregates the multichannel analog input signal into a plurality of separate analog signals of differing frequency ranges, or 'bands.' Each separate analog signal is then converted from analog to digital form in an analog-to-digital converter 121, 122, 123." Pugel (EX1004), ¶ 24. "Each of the plurality of amplifier-filter banks or circuits 111, 112, 113 is configured to process frequencies within a specified band. For example, a first amplifier-filter circuit 111 may be configured to process frequencies from about 5 MHz to about 300 MHz, a second amplifier-filter circuit 112 may be configured for frequencies between about 300 MHz and about 600 MHz, and a third amplifier-filter circuit 113 may be configured for frequencies from about 600 MHz to about 900 MHz. In such an example, the present invention may be used to recover a plurality of digital cable television channels from a multichannel analog RF input signal which includes frequencies ranging from about 5 MHz to about 900 MHz." Pugel (EX1004), ¶ 28. "This combination of components permits substantially simultaneous reception of multiple digital cable channels within a **single digital receiver circuit** suitable for use with conventional cable delivery systems and at a reasonable cost." Pugel (EX1004), Abstract. Thus, because Pugel discloses an apparatus which processes frequencies in the range between 5 MHz and 900 MHz, it discloses,

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	or at least renders obvious, performing its methods *in a wideband receiver system* as recited. Lipoff (EX1008), ¶¶ 116–122.
[11.1] downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;	Pugel and Gomez render obvious *downconverting* (e.g., Pugel's downconverting of digital signals), *by a mixer module* (e.g.., Gomez's teaching of mixers that downconvert) *of said wideband receiver system* (Pugel's apparatus), *a plurality of frequencies* (Pugel's plurality of separate analog signals of differing frequency ranges) *that comprises a plurality of desired television channels* (Pugel's digital channels desired to be recovered) *and a plurality of undesired television channels* (the channels in Pugel not desired to be recovered). First, Pugel discloses *downconverting ... a plurality of frequencies*. Pugel explains first that analog signals are received and converted to digital: "In operation, according to one embodiment, a multichannel analog RF input signal received at input coupler 101 is split into a plurality of substantially identical signals at splitter 102. Splitter 102 may include one or more amplifiers, filters, or other components (not shown) which reduce or overcome insertion loss or other adverse effects of the split, as should be apparent to one of ordinary skill in the art. The plurality of amplifier-filter circuits 111, 112, 113 then segregates the multichannel analog input signal into a **plurality of separate analog signals of differing frequency ranges**, or 'bands.' **Each separate analog signal is then converted from analog to digital form in an analog-to-digital converter 121, 122, 123**." Pugel (EX1004), ¶ 24.

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	After the analog frequencies are converted to digital, Pugel teaches *downconverting* the *plurality of frequencies*: "A method (400) processing signals comprising the steps of: (a) separating an input signal into a first analog signal and a second analog signal; (b) digitizing said first analog signal to generate a first digital signal; (c) digitizing said second analog signal to generate a second digital signal; (d) **downconverting** said first digital signal and said second signal; and (e) extracting desired television program information from said downconverted first digital signal and said second digital signal." Pugel (EX1004), claim 18. Pugel further states that "the digital tuner 130 may also perform a variety of other processing operations prior to providing digital channel signals suitable for use in each of the demodulation circuits 141, 142, 143" and that the digital tuner "may include a multitude of components configured as is well known in the art to recover a plurality of digital channel signals substantially simultaneously." Pugel (EX1004), ¶ 37. A POSITA would have recognized that such components used to recover a plurality of digital channel signals would include components to perform *downconverting*, as it was well-known prior to the '362 Patent to perform *downconverting* on signals. For example, as acknowledged by the '362 Patent and numerous contemporaneous references, *downconverting* was well-

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	known by POSITAs at the time of the '362 Patent. Lipoff (EX1008), ¶¶ 124–128 (citing, e.g., Tseng, Li, Mirabbasi, Feng). As detailed above in the Claim Construction section, the *downconverting* step may be performed prior to the *digitizing* step, as these two steps need not be performed in any specific order. EX1007, pp. 51–52. Pugel does not explicitly disclose that the downconverting is performed *by a mixer module of said wideband receiver system*. However, this was a known implementation detail at the time of the '362 Patent. For example, in the same field, Gomez describes: "Tuner 201 performs a dual frequency conversion to select and down-convert a desired or selected channel from a RF input signal 101. In doing so, amplifer 300 receives and amplifes RF input signal 101, which contains a plurality of television channels. Mixer 301 receives RF input signal 101 from amplifier 300 and also receives a local oscillator (LO) signal from PLL 304. For direct conversion, the frequency of PLL 304 is tuned to the frequency of the desired channel in RF input signal 101 so that it is down-converted to baseband, for further processing. For example, if the desired channel in RF input signal 101 is at 100 MHZ, then PLL 304 is tuned to 100 MHZ, so that **mixer 301 down-converts the desired channel in RF signal** 101 to DC." Gomez (EX1005), 4:6–19. Thus, Gomez teaches downconverting *by a mixer module*. Lipoff (EX1008), ¶¶ 129–130. A POSITA would have been motivated to combine the teachings of Gomez with Pugel, because doing so would have been nothing more

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	than the use of a known technique to improve a similar device in the same way. Pugel teaches that downconverting is performed, but it does not describe the circuitry for doing so. The '362 Patent Background acknowledges that "[e]xisting tuners … down-convert a swath of channels to an intermediate frequency." '362 Patent (EX1001), 1:27–29. The '362 Patent also acknowledges as prior art a "mixer" which "frequency down-converts the received RF input signal to a more convenient intermediate frequency (IF) band." *Id.* at 1:58–62. Thus, it was known to perform *downconverting* using a *mixer module*. Gomez explicitly teaches the circuitry (i.e., a mixer) to perform the known technique of downconversion. A POSITA would have been motivated to apply this teaching in Gomez of downconversion by a mixer module to the teachings of Pugel to provide the hardware necessary to perform Pugel's downconversion. The results would have been predictable to a POSITA, as the results would have simply represented Gomez's mixer module performing downconversion in the context of Pugel's system that also performs downconversion. Accordingly, a POSITA would have been motivated to combine the teachings for at least this reason. Lipoff (EX1008), ¶¶ 131–133. Likewise, combining the teachings of Gomez and Pugel would have been nothing more than combining prior art elements according to known methods to yield predictable results. Together, Pugel and Gomez include each element claimed, with the only difference being the lack of actual combination in a single prior art reference. A POSITA would have been motivated to, and would have been capable of, combining Gomez's teachings of downconversion by a mixer module with Pugel's teachings of downconversion, and in combination, each element performs the same function as it does separately. A POSITA would have further recognized the predictability of the combination, as the combination simply adds to

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	Pugel appropriate circuitry for performing the functions disclosed in Pugel. Accordingly, a POSITA would have been motivated to combine the teachings for this additional reason as well. Lipoff (EX1008), ¶ 134. Pugel explains that the *plurality of frequencies … comprises a plurality of desired television channels and a plurality of undesired television channels*: "The digital tuner 130 may include a channel selector 315 to permit selection of one or more particular **digital channels desired to be recovered**. For example, a selected set of digital cable television channels may be communicated to the digital tuner 130 via the channel selector 315 corresponding to a plurality of pay-per-view selections desired by members of a household; the digital tuner 130 may demultiplex only the digital channel signals corresponding to those digital cable television channels." Pugel (EX1004), ¶ 38. "It should be apparent that each digital RF channel signal may in turn carry or provide a plurality of data streams, e.g., audio, video, program information, or interactive content." Pugel (EX1004) ¶ 45. "FIG. 4 shows a flow diagram representation of a method of **receiving a plurality of digital RF channels** generally designated 400 in accordance with an aspect of the present invention….The method 400 begins at step 401 and proceeds to step 402 in which a multichannel analog RF input signal is separated into

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	a plurality of analog signals including at least first and second analog signals. In step 403, the first analog signal is converted into a first digital signal using a first analog-to-digital converter. In step 404, the second analog signal is converted into a second digital signal using a second analog-to-digital converter independently of the conversion performed in the first analog-to-digital converter. The first and second analog-to-digital converters may convert different frequency bands from analog to digital form, similar to analog-to-digital converters 121, 122, 123 described above with reference to FIGS. 1 and 2…. In step 405, the first digital signal (converted in the first analog-to-digital converter) and the second digital signal (converted in the second analog-to-digital converter) are demultiplexed to generate a plurality of digital RF channel signals including at least first and second digital RF channel signals." Pugel (EX1004), ¶¶ 43–45. Thus, in Pugel, the multichannel analog RF input signal includes all channels (desired and undesired), which signal is then digitized and downconverted (as detailed in Pugel's claim 18) in the process of recovering the digital channels desired to be recovered. Thus, the multichannel analog RF input signal, subsequently digitized, *comprises a plurality of desired television channels and a plurality of undesired television channels* as recited. In particular, because Pugel teaches selection of "digital channels **desired** to be recovered," a POSITA would have recognized that the signal also includes digital channels **not desired** to be recovered. Accordingly, the plurality of frequencies that is subsequently digitized and downconverted *comprises a plurality of desired*

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	television channels and a plurality of undesired television channels as recited. Thus, the combined teachings of Pugel and Gomez render obvious this limitation. Lipoff (EX1008), ¶¶ 123–138.
[11.2] digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;	Pugel discloses, or at least renders obvious, *digitizing* (e.g., converting), *by a wideband analog-to-digital converter (ADC) module* (e.g., analog-to-digital converters) *of said wideband receiver system* (e.g., Pugel's apparatus), *said plurality of frequencies* (e.g., Pugel's plurality of separate analog signals of differing frequency ranges) *comprising said plurality of desired television channels* (e.g., Pugel's digital channels desired to be recovered) *and said plurality of undesired television channels* (e.g., the channels in Pugel not desired to be recovered). First, Pugel discloses *a wideband analog-to-digital converter (ADC) module of said wideband receiver* system: "A plurality of **analog-to-digital converters** is provided, each respectively coupled to one of the plurality of amplifier-filter circuits, the plurality of analog-to-digital converters including at least a first analog-to-digital converter configured to receive the first analog signal and generate a first digital signal and a second analog-to-digital converter configured to receive the second analog signal and generate a second digital signal." Pugel (EX1004), ¶ 9. "In operation, according to one embodiment, a multichannel analog RF input signal received at input coupler 101 is split into a plurality of substantially identical signals at splitter 102. Splitter 102 may include one or more amplifiers, filters, or other

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	components (not shown) which reduce or overcome insertion loss or other adverse effects of the split, as should be apparent to one of ordinary skill in the art. The plurality of amplifier-filter circuits 111, 112, 113 then segregates the multichannel analog input signal into a **plurality of separate analog signals of differing frequency ranges**, or 'bands.' **Each separate analog signal is then converted from analog to digital form in an analog-to-digital converter 121, 122, 123**." Pugel (EX1004), ¶ 24. "In one embodiment, each amplifier/filter bank has particular characteristics that permit the passage of a specific range of frequencies substantially independent of the frequency selection characteristics of the other amplifier/filter banks. For example, one filter might have a pass-band of about 5 to about 300 MHz, while another filter might have a pass band of about 300 to about 600 MHz." Pugel (EX1004), ¶ 25. "**a first analog-to-digital converter (121)** for processing the first analog signal to produce a first digital signal representing the signals in the first frequency band; **a second analog-to-digital converter (122)** for processing the second analog signal to produce a second digital signal representing the signals in the second frequency band;" Pugel (EX1004), claim 1.

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	Because Pugel's analog-to-digital converters operate on frequencies ranging, in one example, from 300 to 600 MHz, Pugel's analog-to-digital converters teach *digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system* as recited. Second, Pugel discloses *digitizing ... said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels*: "A method (400) processing signals comprising the steps of: (a) separating an input signal into a first analog signal and a second analog signal; (b) **digitizing** said first analog signal to generate a first digital signal; (c) **digitizing** said second analog signal to generate a second digital signal; (d) downconverting said first digital signal and said second signal; and (e) extracting desired television program information from said downconverted first digital signal and said second digital signal." Pugel (EX1004), claim 18. As detailed in the analysis of limitation [11.1], *supra*, the *plurality of frequencies* comprises *said plurality of desired television channels and said plurality of undesired television channels* as recited. Specifically, because the digitizing occurs before the step of extracting desired television programs (the *selecting* step detailed below), all channels comprised in the input signal, including *desired*

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	television channels and *undesired television channels* are digitized as recited. Thus, Pugel discloses, or at least renders obvious, this limitation. Lipoff (EX1008), ¶¶ 139–144.
[11.3] selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and	Pugel discloses, or at least renders obvious *selecting* (e.g., extracts or selects), *by digital circuitry* (e.g., digital channel selector of the digital tuner) *of said wideband receiver system* (e.g., Pugel's apparatus), *said plurality of desired television channels* (e.g., Pugel's digital channels desired to be recovered) *from said digitized plurality of frequencies* (e.g., from the digitized analog signals). Specifically, Pugel discloses extracting desired television programs (e.g., particular digital channels desired to be recovered) from the downconverted, digitized frequencies (e.g., the "downconvert[ed] … first digital signal and … second digital signal."). Pugel discloses: "The digital tuner 130 may include a **channel selector 315 to permit selection of one or more particular digital channels desired to be recovered**. For example, a selected set of digital cable television channels may be communicated to the digital tuner 130 via the channel selector 315 corresponding to a plurality of pay-per-view selections desired by members of a household; the digital tuner 130 may **demultiplex only the digital channel signals corresponding to those digital cable television channels**. Alternatively, the digital tuner 130 may be configured to demultiplex and recover all of the available digital channel signals." Pugel (EX1004), ¶ 38.

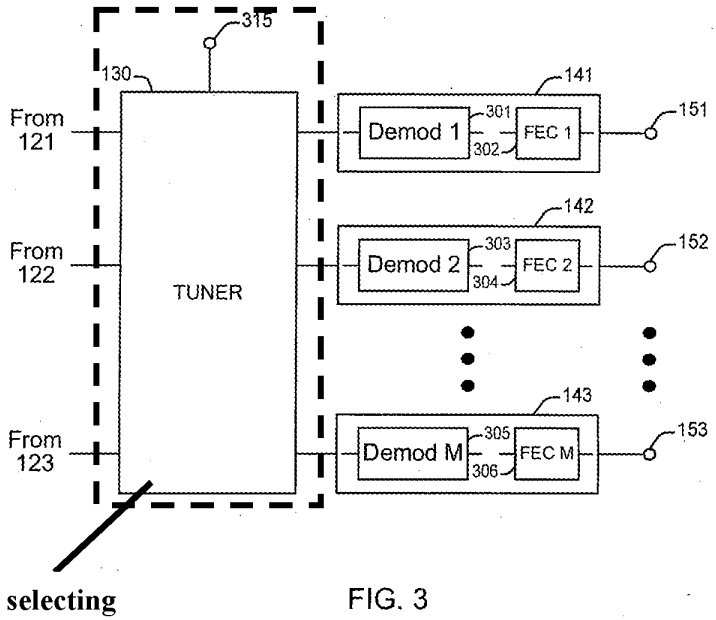


FIG. 3

Pugel (EX1004), Fig. 3 (annotated)

Pugel also refers to channel selection as "extracting," as it refers to this functionality in the claims as the tuner 130 (which includes channel selector 315) extracting desired information to be provided to demodulators (e.g., as shown in Fig. 3 above):

> "The apparatus (100) of claim 12 where said digital processor (130) multiplexes said first, second, and third digital signals, downconverts said multiplexed signal and extracts desired information to be coupled to said first and second demodulator circuits (141, 142)."

Pugel (EX1004), claim 14.

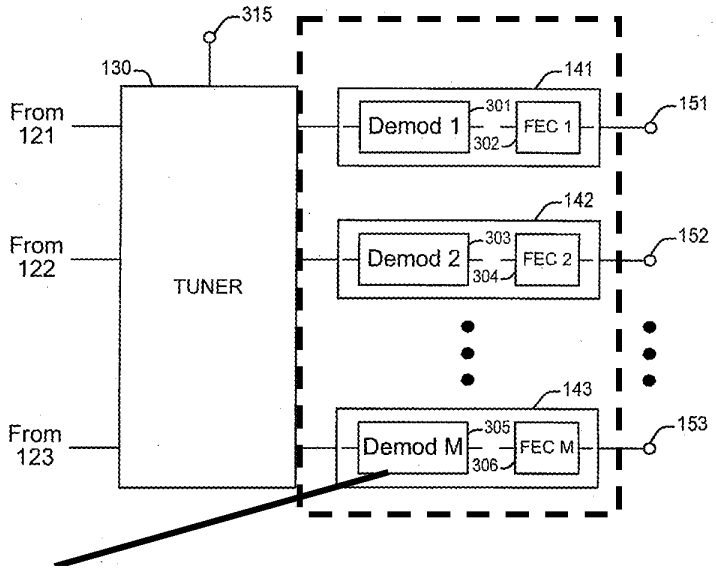
> "A method (400) processing signals comprising the steps of:
>
> (a) separating an input signal into a first analog signal and a second analog signal;

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	(b) digitizing said first analog signal to generate a first digital signal; (c) digitizing said second analog signal to generate a second digital signal; (d) downconverting said first digital signal and said second signal; and (e) **extracting desired television program information** from said downconverted first digital signal and said second digital signal." Pugel (EX1004), claim 18. "FIG. 4 shows a flow diagram representation of a method of **receiving a plurality of digital RF channels** generally designated 400 in accordance with an aspect of the present invention….The method 400 begins at step 401 and proceeds to step 402 in which a multichannel analog RF input signal is separated into a plurality of analog signals including at least first and second analog signals. In step 403, the first analog signal is converted into a first digital signal using a first analog-to-digital converter. In step 404, the second analog signal is converted into a second digital signal using a second analog-to-digital converter independently of the conversion performed in the first analog-to-digital converter. The first and second analog-to-digital converters may convert different frequency bands from analog to digital form, similar to analog-to-digital converters 121, 122, 123 described above with reference to FIGS. 1 and 2….

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	In step 405, the first digital signal (converted in the first analog-to-digital converter) and the second digital signal (converted in the second analog-to-digital converter) are demultiplexed to generate a plurality of digital RF channel signals including at least first and second digital RF channel signals." Pugel (EX1004), ¶¶ 42–45. "It should be apparent that **each digital RF channel** signal may in turn carry or provide a plurality of data streams, e.g., audio, video, **program information**, or interactive content." Pugel (EX1004), ¶ 45. "A method and apparatus is presented for simultaneous **reception of a plurality of digital RF channels**….This combination of components permits substantially **simultaneous reception of multiple digital cable channels** within a single digital receiver circuit suitable for use with conventional cable delivery systems and at a reasonable cost." Pugel (EX1004), Abstract. Because Pugel discloses extracting the desired television program information from the digital RF channels, and that the channel selector permits selection of digital RF channels desired to be recovered, Pugel discloses, or at least renders obvious, *selecting, by digital circuitry of said wideband receiver system* (e.g., channel selector 315), *said plurality of television channels from said digitized plurality of frequencies* (the digital channels desired to be recovered). Lipoff (EX1008), ¶¶ 145–148.

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[11.4] outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.	Pugel discloses, or at least renders obvious *outputting* (e.g., coupling selected digital channels to a demodulator), *by said digital circuitry* (e.g., digital tuner) *of said wideband receiver system* (e.g., Pugel's apparatus), *said selected plurality of television channels* (e.g., Pugel's digital channels desired to be recovered) *to a demodulator* (e.g., demodulation circuits, including demodulators) *as a digital datastream* (e.g., digital channel signals). Pugel discloses: "In operation, according to one embodiment, a multichannel analog RF input signal received at input coupler 101 is split into a plurality of substantially identical signals at splitter 102. Splitter 102 may include one or more amplifiers, filters, or other components (not shown) which reduce or overcome insertion loss or other adverse effects of the split, as should be apparent to one of ordinary skill in the art. The plurality of amplifier-filter circuits 111, 112, 113 then segregates the multichannel analog input signal into a plurality of separate analog signals of differing frequency ranges, or 'bands.' **Each separate analog signal is then converted from analog to digital form in an analog-to-digital converter 121, 122, 123**." Pugel (EX1004), ¶ 24. "The converted digital signals are coupled to the digital tuner 130, which demultiplexes the converted digital signals to generate a plurality of digital channel signals. **Each digital channel signal is then coupled to a separate demodulator 141, 142, 143**, which performs demodulation and forward-error-correction (FEC) operations appropriate for the content of that digital channel."

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	Pugel (EX1004), ¶ 27. "In an alternate embodiment, in addition to the above **a plurality of demodulator circuits is coupled to the digital tuner**, the plurality of demodulator circuits including at least a first demodulator circuit configured to receive and **demodulate a first channel of the plurality of digital RF channels and a second demodulator circuit being configured to receive and demodulate a second channel of the plurality of digital RF channels**. The plurality of demodulator circuits includes circuitry configured for forward error correction." Pugel (EX1004), ¶ 10; *see also* ¶¶ 38 ("a selected set of digital cable television channels may be communicated to the digital tuner 130 via the channel selector 315…the digital tuner 130 may demultiplex only the digital channel signals corresponding to those digital cable television channels."), 39 ("the digital tuner 130 may also perform a variety of other processing operations prior to providing digital channel signals suitable for use in each of the demodulation circuits 141, 142, 143").

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	 FIG. 3 **Pugel (EX1004), Fig. 3 (annotated)** "Each of the **demodulation circuits** 141, 142, 143 may include one or more demodulators 301, 303, 305 and forward-error-correction (FEC) circuitry 302, 304, 306, respectively." Pugel (EX1004), ¶ 40. Thus, Pugel teaches *outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream* as recited. Lipoff (EX1008), ¶¶ 149–151.

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Claim 1	
[1.0] A wideband receiver system comprising:	*See* analysis of limitation [11.0], *supra*.
[1.1] a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;	*See* analysis of limitation [11.1], *supra*.
[1.2] a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;	*See* analysis of limitation [11.2], *supra*.
[1.3] digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and	*See* analysis of limitation [11.3], *supra*.
[1.4] [digital circuitry configured to:]… output said selected plurality of television channels to a	*See* analysis of limitation [11.4], *supra*.

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demodulator as a digital datastream.	

III. DISCLOSURE OF CONCURRENT LITIGATION AND REEXAMINATION PROCEEDINGS

Requester is aware of the following litigations in which the '362 Patent is involved:

Entropic Communications, LLC v. Charter Communications, Inc., Case No. 2:22-cv-00125 (E.D. Tex.).

Entropic Communications, LLC v. Cox Communications, Inc. et al., Case No. 2:23-cv-01049 (C.D. Cal.).

Entropic Communications, LLC v. Comcast Corporation et al., Case No. 2:23-cv-01050 (C.D. Cal.).

IV. CERTIFICATION REGARDING NO ESTOPPEL

In accordance with 37 C.F.R. § 1.510(b)(6), the Requester hereby certifies that the estoppel provisions of 35 U.S.C. § 315(e)(1) or 35 U.S.C. § 325(e)(1) do not prohibit the Requester from filing this Request.

V. THIS REQUEST SHOULD NOT BE DENIED UNDER 35 U.S.C. § 325(D)

As discussed in Section I.D above, this Request raises substantial new questions of patentability with respect to the Challenged Claims. This Reexamination Request should ***not*** be rejected under 35 U.S.C. § 325(d), because none of the proposed rejections presented in this Request present prior art and arguments that includes "the same or substantially the same prior art or arguments" previously presented to the Office. *See* 35 U.S.C. § 325(d) ("In determining whether to institute or order a proceeding under this chapter, chapter 30, or chapter 31, the Director may take into account whether, and reject the petition or request because, the same or substantially the

same prior art or arguments previously were presented to the Office."). Thus, there is no basis to exercise discretion under 35 U.S.C. § 325(d).

VI. LIST OF EXHIBITS

Exhibit 1001	U.S. Patent No. 9,210,362
Exhibit 1002	File History of U.S. Patent No. 9,210,362
Exhibit 1003	WO 2006/119490 to David Lowell McNeely
Exhibit 1004	WO 2007/145637 to Michael Anthony Pugel
Exhibit 1005	U.S. Patent No. 8,224,274 to Ramon Gomez et al.
Exhibit 1006	"Frequency Translation Method for Low Frequency Variable Gain Amplification and Filtering," Mabel Y. Feng, June 2007
Exhibit 1007	Claim Construction Memorandum and Order, *Entropic Communications, LLC v. Charter Communications, LLC*, Case 2:220-cv-00125-JRG, Dkt. 123 (June 26, 2023)
Exhibit 1008	Declaration of Stuart Lipoff
Exhibit 1009	[reserved]
Exhibit 1010	[reserved]
Exhibit 1011	"Direct Downconversion of Multiband RF Signals Using Bandpass Sampling," Tseng et al., IEEE Transactions on Wireless Communications, 2006
Exhibit 1012	"RF CMOS Mixer Design and Optimization for Wideband CDMA Application," Li et al., IEEE 2000.
Exhibit 1013	"Classical and Modern Receiver Architectures," Mirabbasi et al., Topics in Circuits for Communications, IEEE 2000.

VII. CONCLUSION

For the reasons set forth above, it is clear that substantial new questions of patentability are raised in connection with claims 1 and 11 by this request for *ex parte* reexamination since claims 1 and 11 are rendered obvious in view of the above-listed prior art references. Therefore, Requester asks that this request for reexamination be granted and that claims 1 and 11 be canceled.

As identified in the attached Certificate of Service and in accordance with 37 C.F.R. §§ 1.33(c) and 1.510(b)(5), a copy of the present request, in its entirety, is being served to the address of the attorney or agent of record.

Please direct all correspondence in this matter to the undersigned.

Respectfully submitted,

/Raghav Bajaj/
Raghav Bajaj
Registration No. 66,630
Attorney for Requester

Dated: September 20, 2023
HAYNES AND BOONE, LLP
Customer No. 27683
Telephone: 512/867-8520
Facsimile: 214/200-0853
Attorney Docket No.: 50348.106

CERTIFICATE OF SERVICE

I hereby certify that this correspondence, all attachments, and any corresponding filing fee are being transmitted via the Electronic Filing System (Patent Center) with the United States Patent and Trademark Office on September 20, 2023.

/Raghav Bajaj/
Raghav Bajaj

VIII. CERTIFICATE OF SERVICE

The undersigned certifies that copies of the following,

(1) Request for Ex Parte Reexamination Transmittal Form;

(2) PTO 1449 Modified Form;

(3) Request for Ex Parte Reexamination; and

(4) Exhibits 1001 through 1008 and 1011 through 1013.

in their entirety were served on:

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET, SUITE 3400
CHICAGO, IL 60661

the attorney of record for the assignee of U.S. Patent No. 9,210,362, in accordance with 37 C.F.R. § 1.510(b)(5), on the 20th day of September 2023.

/Raghav Bajaj/
Raghav Bajaj
Registration No. 66,630

PTO/SB/57 (01-18)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(Also referred to as FORM PTO-1465)

REQUEST FOR *EX PARTE* REEXAMINATION TRANSMITTAL FORM

Address to:
Mail Stop *Ex Parte* Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney Docket No.: 50348.106

Date: September 20, 2023

1. ■ This is a request for *ex parte* reexamination pursuant to 37 CFR 1.510 of patent number 9,210,362 issued December 8, 2015. The request is made by:
   ☐ patent owner. ■ third party requester.

2. ■ The name and address of the person requesting reexamination is:
   Raghav Bajaj, HAYNES AND BOONE, LLP
   2323 Victory Avenue, Suite 700
   Dallas, Texas 75219

3. Requester ☐ asserts small entity status (37 CFR 1.27) or ☐ certifies micro entity status (37 CFR 1.29). Only a patent owner requester can certify micro entity status. Form PTO/SB/15A or B must be attached to certify micro entity status.

4. This request is accompanied by payment of the reexamination fee as set forth in:
   ■ 37 CFR 1.20(c)(2); **or**
   ☐ 37 CFR 1.20(c)(1). **In checking this box for payment of the fee set forth in 37 CFR 1.20(c)(1), requester asserts that this request has forty (40) or fewer pages and complies with all other requirements of 37 CFR 1.20(c)(1).**

   Payment of the reexamination fee is made by the method set forth below.
   a. ☐ A check in the amount of $_____ is enclosed to cover the reexamination fee;
   b. ■ The Director is hereby authorized to charge the reexamination fee to Deposit Account No. 50-6990;
   c. ☐ Payment by credit card. Form PTO-2038 is attached; **or**
   d. ■ Payment made via EFS-Web.

   ■ In addition, the Director is hereby authorized to charge any fee deficiencies to Deposit Account No. 50-6990.

5. ■ Any refund should be made by ☐ check or ■ credit to Deposit Account No. 50-6990. 37 CFR 1.26(c). If payment is made by credit card, refund must be to credit card account.

6. ■ A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.510(b)(4).

7. ☐ CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
   ☐ Landscape Table on CD

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0064. Public burden for this form is estimated to average 18 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **If filing this completed form by mail, send to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

8. ☐ Nucleotide and/or Amino Acid Sequence Submission
If applicable, items a. – c. are required.
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM (2 copies) or CD-R (2 copies) **or**
      ii. ☐ paper
   c. ☐ Statements verifying identity of above copies.

9. ■ A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.

10. ■ Reexamination of claim(s) 1 and 11 is requested.

11. ■ A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.

12. ■ An English language translation of all necessary and pertinent non-English language patents and/or printed publications is attached.

13. ■ The attached detailed request includes at least the following items:
   a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.510(b)(1).
   b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR1.510(b)(2).

14. ☐ A proposed amendment is included (only where the patent owner is the requester). 37 CFR 1.510(e).

15. ■ It is certified that the statutory estoppel provisions of 35 U.S.C. 315(e)(1) or 35 U.S.C. 325(e)(1) do not prohibit requester from filing this *ex parte* reexamination request. 37 CFR 1.510(b)(6).

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      The name and address of the party served are:

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      CHICAGO, IL 60661

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18. ☒ The patent is currently the subject of the following concurrent proceeding(s):

a. ☐ Copending reissue Application No. _____

b. ☐ Copending reexamination Control No. _____

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Entropic Communications, LLC v. Charter Communications, Inc., Case No. 2:22-cv-00125 (E.D. Tex.).; Entropic Communications, LLC v. Cox Communications, Inc. et al., Case No. 2:23-cv-01049 (C.D. Cal.).

Entropic Communications, LLC v. Comcast Corporation et al., Case No. 2:23-cv-01050 (C.D. Cal.).

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In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	In Ex Parte Reexamination of 9,210,362
				Filing Date	Herewith
				First Inventor Name	Madhukar Reddy et al.
				Art Unit	TBD
				Examiner Name	TBD
SHEET	1	OF	1	Attorney Docket Number	50348.106

U. S. PATENTS				
Examiner's Initials	**Cite No.**	**Document Number**	**Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of Cited Document**
	Exhibit 1005	8,224,274	07-17-2012	Ramon Gomez et al.

U. S. PATENT APPLICATION PUBLICATIONS				
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FOREIGN PATENT DOCUMENTS					
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	Exhibit 1003	WO 2006/119490	11-09-2006	David Lowell McNeely	
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Customer No. 27683

Exhibit 1011

"Direct Downconversion of Multiband RF Signals Using Bandpass Sampling," Tseng et al., IEEE Transactions on Wireless Communications, 2006

Customer No.: 000027683

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Direct Downconversion of Multiband RF Signals Using Bandpass Sampling

Ching-Hsiang Tseng and Sun-Chung Chou

Abstract—**Bandpass sampling can be used by radio receivers to directly digitize the radio frequency (RF) signals. Although the bandpass sampling theory for single-band RF signals is well established, its counterpart for multiband RF signals is relatively immature. In this paper, we propose a novel and efficient method to find the ranges of valid bandpass sampling frequency for direct downconverting multiband RF signals. Simple formulas for the ranges of valid bandpass sampling frequency in terms of the frequency locations of the multiple RF bands are derived. The result can be used to design a multiband receiver for software defined radios.**

Index Terms—**Software defined radio, bandpass sampling, sampling methods, analog-digital conversion, signal sampling.**

I. Introduction

MOBILE communication standards emerged in an increasing speed in recent years. The software defined radio (SDR) [1], which was originally conceived for military applications [2], has the agility of changing its functionality through replacement of the application program and hence provides a relatively economical way to accommodate the rapid emerging mobile communication standards. The main philosophy in designing a SDR receiver front end is to push the analog-to-digital converter (ADC) as close to the antenna as possible. The ultimate goal, would be direct digitizing the radio frequency (RF) signal at the receiver antenna output [3]. To achieve this goal, one can manage to use a wideband high-speed ADC to convert the RF signal to digital. However, the required sampling rate for the ADC could often be too high to be attained if the Nyquist sampling theorem is to be satisfied [4]. Alternatively, being aware of the bandpass nature of the radio signal, one can use the bandpass sampling [5] instead to directly downconvert the desired RF signal from the RF to an intermediate frequency (IF). This can significantly relax the demand for fast ADCs and digital signal processors (DSPs) in a SDR design.

In military and commercial SDRs, there is a need for a single radio to communicate simultaneously with many radios using different RF bands and different modulation schemes [2], [6], [7], [8]. To attain this goal, methods for direct downconversion of multiband RF signals using a single ADC may be appreciated. One possible SDR receiver front end design fulfilling this purpose is shown in Fig. 1(a) [9], where the input signal to the ADC would be a multiband RF signal whose spectrum is like that shown in Fig. 1(b). A method to determine the bandpass sampling frequency for the ADC in Fig. 1(a) has been proposed in [9]. This method, however, is computationally intensive. Its computational complexity can be alleviated to certain extent by using the method presented in [10].

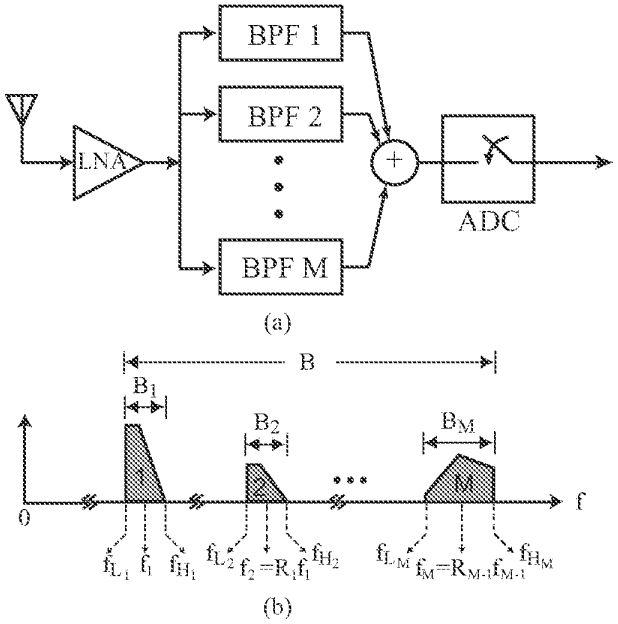


Fig. 1. (a) The SDR receiver front end. (b) The spectrum of the multiband RF signal at the input of the ADC.

In this paper, a novel method is proposed to obtain the valid bandpass sampling frequency ranges for direct downconversion of multiband RF signals. In the proposed method, we first observe that a valid sampling frequency must not cause aliasing in the sampled signal. To be immune from aliasing, the spectral replicas (which are produced by sampling) of the signals at different bands must be positioned in frequency in a particular order without overlapping in the sampled signal spectrum. By analyzing the constraints on the sampling frequency for all the possible orders of spectral replicas, we derive an efficient procedure for finding the valid sampling frequency ranges. Compared to the conventional approach, the proposed method is superior in the sense of both computational complexity and ease of implementation. Computer simulation on direct downconversion of multiband

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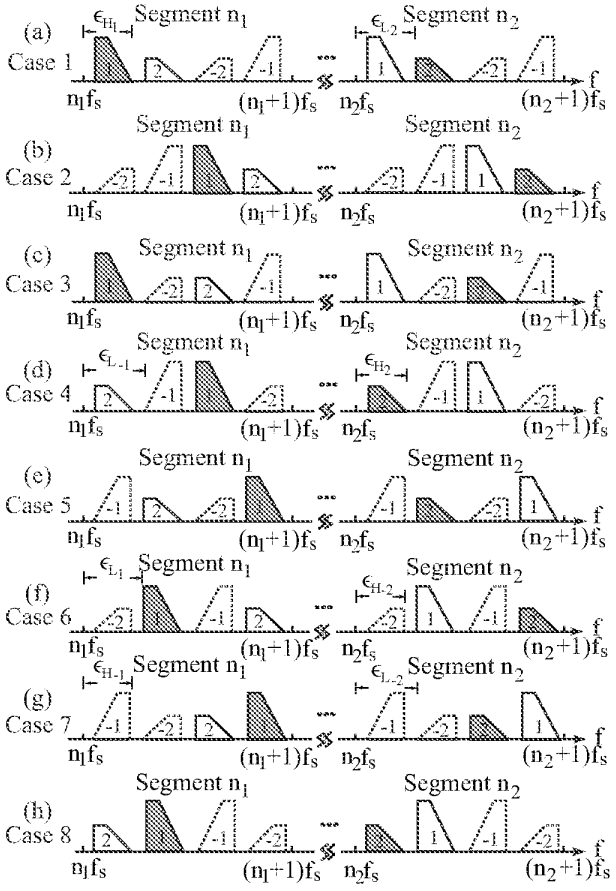


Fig. 2. The dual-band signal shown in Fig. 1(b) (assuming $M = 2$) after bandpass sampling. The 8 possible replica orders are shown in (a) to (h). The parameters ϵ_{L_i} and ϵ_{H_i} $(i = \pm 1, \pm 2)$ are defined in (a), (d), (f), and (g).

GSM signals is conducted to demonstrate the usage of the proposed method.

II. Bandpass Sampling Dual-band RF Signals

Consider the problem of sampling a dual-band RF signal whose spectrum is like that shown in Fig. 1(b) with $M = 2$. To be immune from aliasing, the sampling frequency f_s needs to be chosen without causing spectral overlapping in the sampled signal spectrum. This leads to the 8 possible replica orders shown in Fig. 2, where we use shaded trapezoids to denote the spectrum of the original signal, and solid and dashed trapezoids to denote the replicas for positive-frequency and negative-frequency spectra, respectively.

For a given replica order, the sampling frequency must satisfy two types of constraints: one is referred to as the neighbor constraint and the other is referred to as the boundary constraint in this paper. Note that, as shown in Figs. 2(a) and 2(b), the replicas '1' and '2' are neighbors in the first half of a segment in Case 1 and in the second half of a segment in Case 2. Since the positions of replica 'i' and '$-i$' are symmetric with respective to the midpoint of a segment, one can also see from Figs. 2(a) and 2(b) that the replicas '-2' and '-1' are neighbors in the second half of a segment in Case 1 and in the first half of a segment in Case 2. If those cases having the same neighboring replicas in either the first or the second half of a segment are considered as in one group, we may categorize the 8 cases in Fig. 2 into 4 groups, as shown in Table I, where the neighboring relation between two replicas j and k is denoted by $\langle j, k\rangle$. The two cases in each group have the same neighboring replicas and thus share the same neighbor constraint. However, they have different boundary constraints because the neighboring replicas show up in different halves of a segment.

TABLE I
The Neighbor Constraints for the 8 Cases in Fig. 2.

Group	Neighbors	Case	Shorthand	Constraint
1	$\langle$ 1, 2$\rangle$ $\langle$-2,-1$\rangle$	1 2	$\epsilon_{H_1} \le \epsilon_{L_2}$	$f_s \le \frac{f_{L_2} - f_{H_1}}{n_2 - n_1}$
2	$\langle$ 1,-2$\rangle$ $\langle$ 2,-1$\rangle$	3 4	$\epsilon_{H_1} \le \epsilon_{L_{-2}}$	$f_s \ge \frac{f_{H_1} + f_{H_2}}{n_1 + n_2 + 1}$
3	$\langle$-1, 2$\rangle$ $\langle$-2, 1$\rangle$	5 6	$\epsilon_{H_{-1}} \le \epsilon_{L_2}$	$f_s \le \frac{f_{L_1} + f_{L_2}}{n_1 + n_2 + 1}$
4	$\langle$-1,-2$\rangle$ $\langle$ 2, 1$\rangle$	7 8	$\epsilon_{H_{-1}} \le \epsilon_{L_{-2}}$	$f_s \ge \frac{f_{H_2} - f_{L_1}}{n_2 - n_1}$

For simplicity, we define ϵ_{L_i} and ϵ_{H_i} $(i = \pm 1, \pm 2)$ as the relative lowest and highest frequencies of replica 'i' in a segment, as shown in Figs. 2(a), 2(d), 2(f), and 2(g). By comparing Figs. 2(a), 2(d), 2(f), and 2(g) to Fig. 1(b), one can easily see that

$$\epsilon_{H_i} = f_{H_i} - n_i f_s, \quad i = 1, 2, \tag{1}$$
$$\epsilon_{H_{-i}} = (n_i + 1) f_s - f_{L_i}, \quad i = 1, 2, \tag{2}$$
$$\epsilon_{L_i} = f_{L_i} - n_i f_s, \quad i = 1, 2, \tag{3}$$
$$\epsilon_{L_{-i}} = (n_i + 1) f_s - f_{H_i}, \quad i = 1, 2. \tag{4}$$

In deriving (2) and (4), we have used the following relations

$$\epsilon_{H_{-i}} = f_s - \epsilon_{L_i}, \quad i = 1, 2, \tag{5}$$
$$\epsilon_{L_{-i}} = f_s - \epsilon_{H_i}, \quad i = 1, 2, \tag{6}$$

which are due to the fact that the relative positions of the replicas 'i' and '$-i$' in each segment are symmetric with respect to the midpoint of the segment.

Let's consider the neighbor constraint first. From Table I we see that the neighboring relation in Group *1* is $\langle 1, 2\rangle$ (or equivalently, $\langle -2, -1\rangle$). This relation may be written in a shorthand representation as $\epsilon_{H_1} \le \epsilon_{L_2}$ (see Fig. 2(a)), which can lead to $f_s \le \frac{f_{L_2} - f_{H_1}}{n_2 - n_1}$ with the aid of (1) and (3). Similarly, one can easily find the shorthand representations of the neighbor relations and their corresponding constraints on f_s for the other three groups. The result is summarized in Table I. The boundary constraints for each case can be obtained by observing Fig. 2. Taking Case 1 as an example, the neighboring replicas $\langle 1, 2\rangle$ must be completely inside the first half of a segment. We therefore see from Fig. 2(a) that the shorthand representations of the boundary constraints for spectra '1' and '2' are $\epsilon_{L_1} \ge 0$ and $\epsilon_{H_2} \le f_s/2$, respectively, which can result in $f_s \le \frac{f_{L_1}}{n_1}$ and $f_s \ge \frac{f_{H_2}}{n_2 + 1/2}$ by using (1) and (3). Following the same procedure, it is straightforward to derive the boundary constraints for all other cases. The result

TABLE II
THE BOUNDARY CONSTRAINTS FOR THE 8 CASES IN FIG. 2.

Spectrum	Group	Case	Shorthand	Constraint
'1'	1	1 3	$\epsilon_{L_1} \geq 0$	$f_s \leq \frac{f_{L_1}}{n_1}$
	2	2 4	$\epsilon_{H_{-1}} \leq \frac{f_s}{2}$	$f_s \leq \frac{f_{L_1}}{n_1+1/2}$
	3	5 7	$\epsilon_{L_{-1}} \geq 0$	$f_s \geq \frac{f_{H_1}}{n_1+1}$
	4	6 8	$\epsilon_{H_1} \leq \frac{f_s}{2}$	$f_s \geq \frac{f_{H_1}}{n_1+1/2}$
'2'	1	4 8	$\epsilon_{L_2} \geq 0$	$f_s \leq \frac{f_{L_2}}{n_2}$
	2	3 7	$\epsilon_{H_{-2}} \leq \frac{f_s}{2}$	$f_s \leq \frac{f_{L_2}}{n_2+1/2}$
	3	2 6	$\epsilon_{L_{-2}} \geq 0$	$f_s \geq \frac{f_{H_2}}{n_2+1}$
	4	1 5	$\epsilon_{H_2} \leq \frac{f_s}{2}$	$f_s \geq \frac{f_{H_2}}{n_2+1/2}$

is listed in Table II. Note that the boundary constraints for spectra '1' and '2' are listed separately in Table II. For each spectrum i ($i = 1, 2$), its boundary constraints for the 8 cases can be categorized into 4 groups. Each group includes 2 cases which share the same boundary constraint.

A valid sampling frequency must satisfy both the neighbor and boundary constraints. By combining Tables I and II, one obtains Table III (here $j = 1$, $k = 2$, and $M = 2$), where the ranges of valid sampling frequency for the 8 cases in Fig. 2 are shown.

III. BANDPASS SAMPLING M-BAND RF SIGNALS

In this section, the analysis described in Section II is extended to RF signals with an arbitrary number of bands. Consider an M-band RF signal shown in Fig. 1(b). When the M-band RF signal is sampled at f_s Hz, the spectrum of the sampled signal can be obtained by replicating the spectrum of the original signal at multiples of f_s. Due to spectral replication, there will be a replica of spectrum 'i' ($i = 1, 2, \ldots, M$) and a replica of spectrum '$-i$' in each segment of the spectrum of the sampled signal. For each pair of replicas 'i' and '$-i$', there are two choices of ordering them in a segment: placing replica 'i' in the first half and replica '$-i$' in the second half, or the other way around. Since there are M such pairs of replicas need to be allocated in a segment, the total number of choices is equal to 2^M. To be immune from aliasing, the M replicas allocated to the first half of a segment can not overlap. Hence there are $M!$ ways of ordering the allocated replicas. Therefore, the total number of possible replica orders in one segment is equal to $2^M \times M!$.

For each possible replica order in the first half of a segment, say, $\langle i_1, i_2, \ldots, i_M \rangle$ ($i_m \in \{\pm 1, \pm 2, \ldots, \pm M\}$ for $m = 1, 2, \ldots, M$), there are $M - 1$ neighbor constraints on the neighboring relations $\langle i_1, i_2 \rangle$, $\langle i_2, i_3 \rangle$, ..., $\langle i_{M-1}, i_M \rangle$ and 2 boundary constraints on replicas 'i_1' and 'i_M'. The neighbor constraint on any neighboring relation, say, $\langle j, k \rangle$, can be written in shorthand as $\epsilon_{H_j} \leq \epsilon_{L_k}$. The boundary constraint on a replica, say, 'j', in the first half of a segment is either $\epsilon_{L_j} \geq 0$ (if replica 'j' is ordered the first) or $\epsilon_{H_j} \leq \frac{f_s}{2}$ (if replica 'j' is ordered the last). The corresponding constraints on f_s for the shorthand representations can then be easily obtained with the aid of (1)-(4). By combining all the neighbor constraints on the neighboring relations $\langle i_1, i_2 \rangle$, $\langle i_2, i_3 \rangle$, ..., $\langle i_{M-1}, i_M \rangle$ and the boundary constraints on 'i_1' and 'i_M', one can obtain the range of valid sampling frequency for the replica order $\langle i_1, i_2, \ldots, i_M \rangle$.

IV. SEARCHING FOR THE RANGES OF VALID SAMPLING FREQUENCY

The derivation in Sections II and III shows how one can obtain the range of f_s for a particular replica order provided that n_i ($i = 1, 2, \ldots, M$) are given. Since n_i is the index of the segment where spectrum 'i' is located, we have

$$n_1 = \left\lfloor \frac{f_{L_1}}{f_s} \right\rfloor \leq \left\lfloor \frac{f_{L_1}}{2(B_1 + B_2 + \cdots + B_M)} \right\rfloor \tag{7}$$

where $\lfloor x \rfloor$ denotes the largest integer less than or equal to x, and B_1, B_2, ..., and B_M are defined in Fig. 1(b). In deriving (7), we have used the fact that the bandwidth of a segment should at least accommodate the $2M$ nonoverlapping replicas '1', '-1', '2', '-2', ..., 'M', and '$-M$' (i.e., $f_s \geq 2(B_1 + B_2 + \ldots + B_M)$). In addition, the center frequency of spectrum 'i' (say, f_i) is bounded by

$$n_i f_s < f_i < (n_i + 1) f_s. \tag{8}$$

Multiplying (8) by $\frac{R_i}{f_s}$ and using the relation $f_{i+1} = R_i f_i$ (see Fig. 1(b)), one obtains

$$R_i n_i < \frac{f_{i+1}}{f_s} < R_i (n_i + 1), \quad i = 1, 2, \ldots, M - 1 \tag{9}$$

Taking $\lfloor\ \rfloor$ on (9) and using the fact that $n_{i+1} = \left\lfloor \frac{f_{i+1}}{f_s} \right\rfloor$, we have

$$\lfloor R_i n_i \rfloor \leq n_{i+1} \leq \lfloor R_i n_i + R_i \rfloor, \quad i = 1, 2, \ldots, M - 1. \tag{10}$$

We see that the possible values of n_{i+1} can be determined given n_i.

Based on the above analysis, we may summarize the procedure for obtaining the ranges of valid sampling frequency for M-band RF signals as follows. First we choose an appropriate n_1 using (7), then we choose appropriate n_2, n_3, ..., and n_M using (10). Given the $(n_1, n_2, \ldots, n_M)$, we find the neighbor and boundary constraints for each of the $2^M \times M!$ possible replica orders. The combination of all the constraints yields the range of valid sampling frequency. The above procedure (called the standard procedure hereafter) is conceptually straightforward. However, for typical applications, one may find that examining all the possible replica orders eventually ends up with only few valid replica orders which yield nonempty sampling frequency ranges.

An alternative procedure to find the valid replica orders and their corresponding sampling frequency ranges for an M-band RF signal is to modify the standard procedure as follows. For a given $(n_1, n_2, \ldots, n_M)$, we first determine the valid replica orders for every pair of bands in the M bands. Namely, for any pair of bands, say, the j-th and k-th bands, one can use the procedure described in Section II for dual-band RF signals to determine the valid sampling frequency

TABLE III
THE RANGES OF VALID SAMPLING FREQUENCY FOR THE DUAL-BAND SIGNAL CONSISTING OF THE j-TH AND k-TH BANDS OF AN M-BAND RF SIGNAL.

Case	Range of Valid f_s
1	$\frac{f_{H_k}}{n_k+\frac{1}{2}} \le f_s \le \min\{\frac{f_{L_j}}{n_j}, \frac{f_{L_k}-f_{H_j}}{n_k-n_j}\}$
2	$\frac{f_{H_k}}{n_k+1} \le f_s \le \min\{\frac{f_{L_j}}{n_j+\frac{1}{2}}, \frac{f_{L_k}-f_{H_j}}{n_k-n_j}\}$
3	$\frac{f_{H_j}+f_{H_k}}{n_j+n_k+1} \le f_s \le \min\{\frac{f_{L_j}}{n_j}, \frac{f_{L_k}}{n_k+\frac{1}{2}}\}$
4	$\frac{f_{H_j}+f_{H_k}}{n_j+n_k+1} \le f_s \le \min\{\frac{f_{L_j}}{n_j+\frac{1}{2}}, \frac{f_{L_k}}{n_k}\}$
5	$\max\{\frac{f_{H_j}}{n_j+1}, \frac{f_{H_k}}{n_k+\frac{1}{2}}\} \le f_s \le \frac{f_{L_j}+f_{L_k}}{n_j+n_k+1}$
6	$\max\{\frac{f_{H_j}}{n_j+\frac{1}{2}}, \frac{f_{H_k}}{n_k+1}\} \le f_s \le \frac{f_{L_j}+f_{L_k}}{n_j+n_k+1}$
7	$\max\{\frac{f_{H_j}}{n_j+1}, \frac{f_{H_k}-f_{L_j}}{n_k-n_j}\} \le f_s \le \frac{f_{L_k}}{n_k+\frac{1}{2}}$
8	$\max\{\frac{f_{H_j}}{n_j+\frac{1}{2}}, \frac{f_{H_k}-f_{L_j}}{n_k-n_j}\} \le f_s \le \frac{f_{L_k}}{n_k}$

ranges for all the possible replica orders. The result would be that shown in Table III. Such a table is constructed for each pair of bands in the M bands, hence we have C_2^M tables like Table III. It is easy to see that an M-band replica order, say, $\langle i_1, i_2, \ldots, i_M\rangle$, is a valid replica order (which yields a nonempty sampling frequency range) only if $\langle i_1, i_2\rangle$, $\langle i_2, i_3\rangle$,..., and $\langle i_{M-1}, i_M\rangle$ are valid dual-band replica orders. That is, a valid M-band replica order must be a concatenation of valid replica orders in those C_2^M tables like Table III. Therefore, one can consider only those M-band replica orders which can be concatenated with the valid dual-band replica orders in the C_2^M tables instead of all the possible M-band replica orders. Suppose the number of the M-band replica orders which can be concatenated with the valid dual-band replica orders is small, it is shown in the Appendix that this alternative procedure can be more computationally efficient.

V. COMPUTER SIMULATION - DIRECT DOWNCONVERSION OF GSM SIGNALS

To demonstrate the usage of the proposed method, we conducted two simulations on direct downconverting GSM signals [11]. In the first simulation, the SDR receiver front end in Fig. 1(a) with $M = 2$ was used to directly downconvert the entire service bands of GSM 900 (935-960 MHz) and GSM 1800 (1805-1880 MHz) systems. Therefore, the input signal to the ADC is a dual-band RF signal like that shown in Fig. 1(b) with $M = 2$, where $f_1 = 947.5$, $f_2 = 1842.5$, $B_1 = 25$, and $B_2 = 75$ MHz.

Given the problem, we utilized the proposed method to find the ranges of valid sampling frequency. The result is shown in Table IV. In obtaining Table IV, we found that there were 12 possible (n_1, n_2)'s to be considered. Since Table III demands 35 operations (see Appendix), we see that $12 \times 35 = 420$ operations were used to obtain Table IV. If the method in [9] were used instead, testing the validity of all the frequencies from 100 to 935 MHz would be required. Even if the tests were conducted in steps of 1 MHz, we would still need 835 tests (each needs 12 operations). The number of tests could be reduced to 442 by using the method in [10]. However, the number of involved operations ($442 \times 12 = 5304$) would still be way larger than that for the proposed method.

TABLE IV
THE RANGES OF VALID SAMPLING FREQUENCY FOR THE DUAL-BAND GSM SIGNAL.

n_1	n_2	Case	Range of Valid f_s (MHz)
3	7	7	$240.000000 \le f_s \le 240.666667$
2	5	7	$320.000000 \le f_s \le 328.181818$
2	5	5	$341.818182 \le f_s \le 342.500000$
2	5	4	$355.000000 \le f_s \le 361.000000$
2	4	6	$384.000000 \le f_s \le 391.428571$
2	4	1	$417.777778 \le f_s \le 422.500000$
1	3	7	$480.000000 \le f_s \le 515.714286$
1	3	5	$537.142857 \le f_s \le 548.000000$
1	3	4	$568.000000 \le f_s \le 601.666667$
1	2	6	$640.000000 \le f_s \le 685.000000$
1	2	3	$710.000000 \le f_s \le 722.000000$
1	2	1	$752.000000 \le f_s \le 845.000000$

In the second simulation, the SDR receiver front end in Fig. 1(a) with $M = 3$ was used to receive signals from the GSM 900, GSM 1800, and GSM 1900 (1930-1990 MHz) systems. Therefore, the input signal to the ADC is a three-band RF signal. Given the received signal, we utilized the procedure described in Section IV to search for ranges of valid sampling frequency. Only 5 ranges of valid sampling frequency were found for all possible (n_1, n_2, n_3). By taking a closer look, we found that all the 5 ranges have $n_1 = 1$. With such a small value of n_1, the valid sampling frequencies in the 5 ranges are all higher than about 600 MHz. One way to lower the sampling rate is by using BPFs with bandwidths narrower than the GSM service bands in Fig. 1(a) to prefilter the received signal. By varying the center frequencies of the BPFs, any channel in the GSM service bands can be preselected as wanted.

As an example, in this simulation we assumed that three BPFs centering at $f_1 = 936$, $f_2 = 1806$, and $f_3 = 1931$ MHz and having a bandwidth of 2 MHz were used in Fig. 1(a). Hence the resulting signal to the ADC has three bands, where bands 1, 2, and 3 are at 935-937, 1805-1807, and 1930-1932 MHz, respectively. Using these parameters and following the procedure described in Section IV, a total of 611 ranges of valid sampling frequency were obtained for all possible (n_1, n_2, n_3). By examining the 611 valid ranges we found that, although the number of possible replica orders is 48, the maximum number of replica orders which can be concatenated with the dual-band valid replica orders is $L = 14$ for a given (n_1, n_2, n_3). Using the formulas in the Appendix we see that, in this case, the alternative procedure should be more computationally efficient than the standard procedure. To verify this, both the standard and the alternative procedures were used. The result shows that the alternative procedure indeed requires about 13% less CPU time than the standard procedure.

VI. CONCLUSION

In this paper, we have presented an efficient method to determine the ranges of valid bandpass sampling frequency for multiband RF signals. The result can be used to efficiently choose an appropriate bandpass sampling frequency for the ADC in a multiband SDR receiver front end. Note that the

selection of the sampling frequency could be more flexible if nonuniform sampling is allowed, but this would complicate the design of the direct downconverter. It could be beneficial if the sampling process is synchronized with the carrier of the transmitted RF signal. For example, one might be able to use the digital quadrature sampling technique [12] to simplify the data acquisition process.

There are some practical issues to be considered before using the proposed method. Firstly, in performing bandpass sampling, the analog input bandwidth of the ADC needs to meet the spectral range of the RF signals [3]. This is challenging because the attainable maximum analog input frequency of the ADC is limited by its aperture jitter [4]. Secondly, the relatively large sampling rate used by the proposed scheme suggests that high power dissipation is required [13]. This situation can only be improved through the advances of low power consumption ADC technologies (such as the CMOS technology). Thirdly, since the second-order or third-order product distortions caused by nonlinearities in the system could be downconverted to appear in the desired bands, special care should be taken in choosing the sampling frequency in case that nonlinearities exist. Lastly, the prefiltering RF filters need to have steep rolloffs to provide sufficient attenuation of adjacent channel signals, otherwise aliasing may occur in the sampled signal. The currently available RF filters (surface acoustic wave (SAW) or ceramic) have limited stopband attenuation and are designed for a fixed center frequency and a fixed bandwidth. They are not suitable for the proposed flexible filtering scheme. This might be able to be solved by using a micro-electro-mechanical structure (MEMS) filter in the future [14].

APPENDIX

It is easy to see that Tables I, II, and III require 7, 12, and 35 operations (adds, divides, or compares) for a given (n_1, n_2). For an M bands RF signal, we need to consider C_2^M neighbor constraint tables like Table I and C_2^M boundary constraint tables like Table II for a given $(n_1, n_2, \ldots, n_M)$. These tables require $7C_2^M + 12C_2^M = 19C_2^M$ operations. In addition, to see whether a particular replica order is valid, we need M compares. Since there are $2^M \times M!$ possible replica orders, we need a total of $M \times 2^M \times M!$ compares for each $(n_1, n_2, \ldots, n_M)$. The total number of operations required for the standard procedure is thus $M \times 2^M \times M! + 19C_2^M$ for each $(n_1, n_2, \ldots, n_M)$. If the alternative procedure is used, we need to consider C_2^M dual-band valid sampling frequency tables like Table III, which requires $35C_2^M$ operations. If the number of replica orders which can be obtained by concatenating the valid dual-band replica orders in the C_2^M tables is L for a given $(n_1, n_2, \ldots, n_M)$, we will need additional $L \times (2M - 3)$ compares to see whether the L replica orders are valid. The total number of operations required for the alternative procedure is thus $35C_2^M + L \times (2M - 3)$ for each $(n_1, n_2, \ldots, n_M)$. For typical applications, the number L is significantly smaller than the total number of replica orders $2^M \times M!$. Therefore, the alternative procedure is more computationally efficient when M is large. For example, if $M = 3$ and $L = 14$, the numbers of operations required by the standard and the alternative procedures are 201 and 147, respectively. The difference between the two numbers will in general increase with M.

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Exhibit 1003

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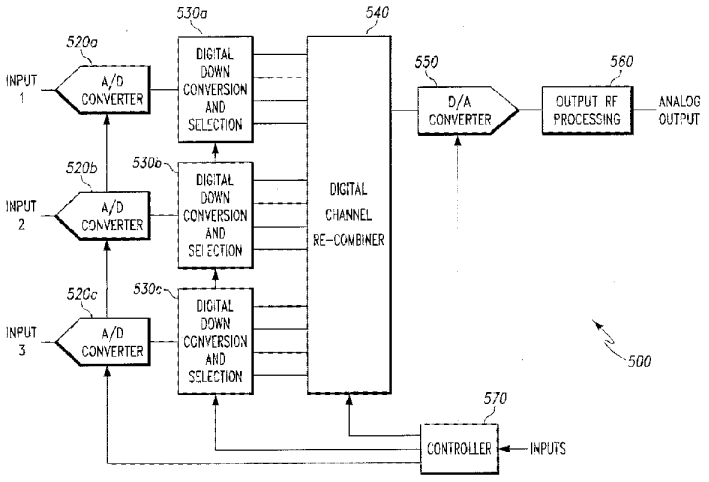
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(54) Title: APPARATUS AND METHOD FOR FREQUENCY TRANSLATION



(57) Abstract: The disclosed embodiments relate to an apparatus and method for performing frequency translation. The apparatus includes a receiver (520a-c, 530a-c) for receiving and digitizing a plurality of first signals, each signal containing channels and for simultaneously recovering a set of selected channels from the plurality of first signals. The apparatus also includes a transmitter (540, 550, 560) for combining the set of selected channels to produce a second signal. The method of the present invention includes receiving a first signal (602) containing a plurality of different channels, selecting a set of selected channels (606) from the plurality of different channels, combining the set of selected channels (608) to form a second signal and transmitting the second signal (612).

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Apparatus and Method for Frequency Translation

This application claims the benefit under 35 U.S.C.§ 119 of a provisional application 60/677563 filed in the United States on May 4, 2005.

FIELD OF THE INVENTION

The present invention generally relates to communications systems. More specifically, the present invention relates to the receiving and retransmission of content within a communications system.

BACKGROUND OF THE INVENTION

This section is intended to introduce the reader to various aspects of art, which may be related to various aspects of the present invention that are described and/or claimed below. This discussion is believed to be helpful in providing the reader with background information to facilitate a better understanding of the various aspects of the present invention. Accordingly, it should be understood that these statements are to be read in this light, and not as admissions of prior art.

In today's data communication systems such as used in satellite TV, data of different types often reside in what are known as virtual channels. The data from these virtual channels is separately disassembled into data packets, aggregated within and across different data types into bit streams and conveyed by packet delivery systems. Data consumer appliances, such as satellite receivers, select from physical channels available to them, convert the signals on these channels to digital form (packets) and collect the data packets required to re-assemble the desired virtual channels of information (e.g., audio, video, program guide, transactional data, etc.). At different points along the data path between a content provider and a content consumer data

management opportunities occur. A piece of data may come from one of many sources, be routed through one of many satellites, pass through several of many transponders aboard the satellite, be received by a consumer antenna, and be distributed to places of consumption.

Consumer receivers are often capable of receiving only one of the physical channels from the satellite at a time for display. However, new receivers may contain advanced features the consumer can use. For instance, a receiving device may contain more than one tuner for use in either two picture simultaneous display systems or content recording. Additionally, consumer households often include multiple receivers, each receiver requiring the tuning of one or more channels for use.

The ever-expanding amount of content for delivery has made it very difficult to deliver that content to all places at all times. Systems receiving data from up to four separate satellites to deliver programming to the home can no longer deliver all of the content on one coaxial cable connection. Various approaches have been adapted including the use of multiple cables or complex switching arrangements. Many of these approaches are in some manner suboptimal for a home installation due to high cost or high complexity.

Another solution may be to employ a system of preselecting, combining, and redistributing the incoming content based on the physical channels requested by the user(s) using analog signal processing. As a result, only the channels required for delivery to the receivers in a household are selected from the initial available content. The desired channels may then be provided on a single cable that is relatively easy to distribute around the household. The solution relies on coarse analog signal tuning and re-mixing to move channels or frequency regions of signals from an original spectral location in frequency at the input to another spectral location in frequency on a common signal at the output. Further, channels or signal regions at the same frequency but on different satellites may be combined by moving one or both of the

original channels or regions. These relocated signals containing the desired channels are then provided on the single cable, eliminating the need for any additional switching and multiple cable connections.

The analog solution involving preselection, combination, and redistribution remains limited in the number of channels that can be provided due to the inherent shortcomings of performing the processing in the analog domain. Narrow band filters used to select individual physical channels while rejecting others are impractical at frequencies above the range of one gigahertz (GHz). Available filters having a practical bandwidth require additional channel separation in order to prevent undesired interferences in the output signal. Additionally as the desire to deliver more requested channels to the home increases, the subsequent increase in analog circuit complexity results in an expensive and inefficient design with potential problems due to analog crosstalk. Therefore there is a desire to have a solution providing receiving and re-synthesizing of channels for distribution in a more optimal manner.

SUMMARY OF THE INVENTION

The present invention relates to an apparatus and method for performing frequency translation. The apparatus includes a receiver for receiving and digitizing a plurality of first signals, each signal containing channels and for simultaneously recovering a set of selected channels from the plurality of first signals. The apparatus also includes a transmitter for combining the set of selected channels to produce a second signal.

The method of the present invention includes receiving a first signal containing a plurality of different channels, selecting a set of selected channels from the plurality of different channels, combining the set of selected channels to form a second signal and transmitting the second signal.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a block diagram of an exemplary system using the present invention.

FIG. 2 is a block diagram of an embodiment of the present invention

FIG. 3 is a block diagram of another embodiment of the present invention.

FIG. 4 is a block diagram of yet another embodiment of the present invention.

FIG. 5 is a block diagram of a further embodiment of the present invention.

FIG. 6 is a flow chart illustrating a method of the present invention.

The characteristics and advantages of the present invention may become more apparent from the following description, given by way of example.

DETAILED DESCRIPTION

One or more specific embodiments of the present invention will be described below. In an effort to provide a concise description of these embodiments, not all features of an actual implementation are described in the specification. It should be appreciated that in the development of

any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming, but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

It is noted that familiarity with television broadcasting and receivers is assumed and is not described in detail herein. For example, other than the inventive concept, familiarity with current and proposed recommendations for TV standards such as National Television Systems Committee (NTSC), Phase Alternation Lines (PAL), Sequential Couleur Avec Memoire (SECAM), Advanced Television Systems Committee (ATSC), and Direct Broadcast Satellite (DBS) is assumed. Likewise, other than the inventive concept, transmission concepts such as satellite transponders, down-link signals, eight-level vestigial sideband (8-VSB), Quadrature Amplitude Modulation (QAM), and receiver components such as a radio-frequency (RF) front-end, or receiver section, such as a low noise block, tuners, and demodulators is assumed. Similarly, formatting and encoding methods (such as Moving Picture Expert Group (MPEG)-2 Systems Standard (ISO/IEC 13818-1)) for generating transport bit streams are well-known and not described herein. In addition, the inventive concept may be implemented using conventional programming techniques which, as such, will not be described herein.

The following describes a circuit used for processing satellite signals. Other systems utilized to receive other types of signals where the signal input may be supplied by some other means may include very similar structures. Those of ordinary skill in the art will appreciate that the embodiment of the circuits described herein is merely one potential

embodiment. As such, in alternate embodiments, the components of the circuit may be rearranged or omitted, or additional components may be added. For example, with minor modifications, the circuits described may be configured to for use in non-satellite video and audio services such as those delivered from a cable network. Further, the invention described could be used in conjunction with a home networking system. The device may receive inputs from a satellite or cable network, process them, and provide them as an output to the home network system. The output may in the form of a wired or wireless transmission.

Turning now to the drawings and referring initially to FIG. 1, an overall block diagram 100 of a system using the present invention is shown. FIG. 1 represents a typical satellite system installation at a customer home. A similar installation may also exist at an apartment complex or hotel where the system may be augmented with additional equipment often incorporated in multi-dwelling unit applications. Satellite transponders located on satellites 102a-c transmit satellite signals to satellite dishes 104a-c. Each satellite dish contains a reflector, a feed horn and a low noise block converter (LNB).

Each of the satellite signals may represent one or more individual physical channels. Each of the physical channels may in turn represent one or more preferably digital data streams of information combined together, encoded, and modulated using various analog and/or digital modulation techniques. The physical channels are often grouped to cover a limited frequency range such as 500 to 1000 MHz of bandwidth. The satellite signals are often located in the microwave frequency range, for instance 11-13 Gigahertz (GHz). The LNBs in the satellite dishes 104a-c will amplify and convert the satellite signal in the 11-13 GHz range to an L-band signal in the 1-2 GHz frequency range. Although three satellite dishes are shown, the orbital locations of the satellites 102a-c may permit using one satellite dish containing one reflector and three feed horns and LNBs. Also, systems may utilize more or fewer

than the three satellites signals illustrated here. The systems may additionally use techniques such as polarization diversity to increase the number of satellite signals delivered from each satellite.

Each of the three L-band signals from the satellite dishes 104a-c are provided through separate coaxial cables to a frequency translation module (FTM) 110. The three L-band signals in their entirety cannot be supplied through a single coaxial cable for delivery into the customer home, because the L-band signals occupy too much frequency bandwidth. As previously described, each L-band signal may occupy 1 GHz of bandwidth, and a typical customer premises cable installation may only support less than 2 GHz of total signal bandwidth. The FTM 110 extracts certain ranges of frequencies containing selected physical channels as portions of the three L-band signals provided. The FTM 110 also frequency translates the extracted ranges as needed and re-combines them to form a new single selected L-band signal. The process used by the FTM 110 may be described as a preselection of certain physical channels. However, the process used by the FTM 110 is different from a direct tuning of those certain physical channels since other energy besides the selected channel may be present, and the channels are then recombined to form a new signal for further distribution. Note that the FTM 110 may reside physically outside the customer home as shown, or may reside very near to the entry point into the customer home.

Once the FTM 110 has preselected the physical channels for use, the selected signal is provided over a single coaxial cable to the customer's premises 120. The selected signal may pass through a set of signal splitters 122a-c, as needed, to supply each of the locations for the premises installation. The splitters 122a-c may contain passive circuits such as transformers and resistors or may also contain amplifiers in order to increase the signal level at the installation location.

At each installation location in the premises 120, the selected signal is provided to a standalone terminal 130 or to a combination settop box 140a-c and display device 150a-c. The terminal 130 and settop box 140a-c operate in a similar manner. Each of them receive the selected signal, tune to the desired physical channel within the selected signal, demodulate the physical channel to produce a transport stream, and extract the desired bit stream(s) from the transport stream. The terminal 130 may be used for local storage of various bit streams or for distribution of these bitstreams over a different network such as a wireless network or an Ethernet connection. The settop box 140a-c converts the desired bitstream(s) into video and audio signals for display on the display device 150a-c.

The terminal 130 and settop boxes 140a-c may provide one or more control signals back onto the cable to the FTM 110. The control signal is generated based on inputs provided, for instance by a customer. The control signal sent to FTM 110 contains information necessary to perform the preselection of frequency ranges and physical channels from each of the L-band signals. The communication protocol to the FTM 110 may be done in a manner suitable for delivery as is known in the art, such as frequency shift keying FSK protocol. The control signal may alternately be supplied through a wireless link. Electrical power may also be passed through the coaxial cable to the FTM 110 and further on to the satellite dishes 104a-c.

As described earlier, a conventional FTM contains analog signal processing used for the filtering, mixing, and recombining of the L-band signals. Analog signal processing contains limitations when operating at high frequencies in the 1GHz range, and the complexity of the analog signal processor increases significantly with an increase of the number of selected physical channels. The utilization of digital signal processing within the FTM structure permits greater flexibility and removes some of the limitations of analog signal processing.

Turning now to FIG. 2 a block diagram 200 of an embodiment of the present invention is shown. The diagram shows an implementation of the FTM 110 that includes digital signal processing in order to increase the performance and available bandwidth for selected channels. In order to facilitate a further understanding of the invention, an FTM 110 will be described here using only a single L-band signal as an input. The single L-band signal, as an analog input, is processed through an RF processing block 210. The RF processing block 210 may contain circuitry for filtering undesired energy outside the signal frequency range, may correct for any frequency response errors introduced, and may amplify the signal to a level necessary for input to the analog to digital (A/D) converter 220. The input RF processing block 210 may also contain any mixing circuits necessary to position the L-band signal in the correct frequency range for operation of the A/D converter 220.

The A/D converter 220 digitizes the processed L-band signal into a series of samples, each sample containing a group of bits. In an exemplary embodiment, the processed satellite signal is located between the frequencies of 975 and 1425 MHz. The A/D converter 220 samples the processed L-band signal at a rate of 933 megasamples per second (MSPS) generating a digital signal containing a series of samples, each sample represented by 8 bits. The A/D converter 220 may also generate a translated frequency image of the L-band signal essentially translating the signal from an initial frequency range in the analog domain to a different frequency range based on sampling principles. A clock signal, not shown, is supplied to the A/D converter for performing the sampling. The clock signal may be generated by a crystal or as part of a voltage controlled oscillator. The clock signal may also directly, or through additional multipliers and dividers, supply signals to other blocks within the FTM 110.

The digital channel selector 230 receives the sampled signal and proceeds to select and down-convert each of the individual physical channels that have been selected. After processing, each of the selected individual channels are located within the same frequency range at or near to baseband, but are contained as individual signals on separate signal lines. The number of bits representing each selected individual channel may be different from the original sampled signal based on the processing method employed. The use of digital signal processing and processing of the signal in parallel permits narrower filtering constraints and more efficient channel selection within the FTM 110.

Each of the individual selected channels is provided to the digital channel re-combiner 240. The digital channel re-combiner 240 frequency translates the individual selected channels each to a different and separate frequency range and combines these signals together to form a single selected digital signal. The selected digital signal is supplied to a digital to analog (D/A) converter 250. The D/A converter 250 converts the selected digital signal to a selected analog signal. In a preferred embodiment, the selected digital signal provided to the D/A converter 250 is a series of 10 bit samples at a rate of 950 MSPS. The D/A converter 250 outputs a selected analog signal within a frequency range of DC to 475 MHz.

The selected analog signal is passed to the RF processing block 260. The RF processing block 260 provides any analog signal processing necessary to properly send the selected analog signal on the coaxial cable to the customer home. The RF processing block 260 may contain circuitry for filtering undesired signal energy outside the signal frequency range, such as the images produced by the sampling process in D/A converter 250. The RF processing block 260 may also correct for any other frequency response errors introduced, and may amplify the signal as necessary to provide the signal onto a coaxial cable. The RF

processing block 260 may also contain a mixing circuit necessary to position the selected analog signal in the correct L-band frequency range, for instance 975 - 1425 MHz.

Some additional circuitry may also be included such as circuitry for controlling the blocks, receiving and processing user inputs, and additional signal processing, although this circuitry is not shown here.

Turning now to FIG. 3, an illustrative block diagram of a circuit 300 of an embodiment of a portion of the present invention is shown. Circuit 300 represents circuitry contained with the digital channel converter block 230. A sampled signal, converted from an L-band signal by A/D converter 220, is provided to the sample demultiplexer 310. Sample demultiplexer 310 resamples at a demultiplexer sampling rate, F_F, (or post-decimation sampling rate) to provide a number of decimated sample streams in parallel.

Each of the decimated sample streams represents a sampled and time shifted version of the original signal with each of the folded spectra, from the decimation, aliased into the same decimated frequency space. The number of decimated sample streams, N, may be integrally related to the number of virtual channels in the original signal. In a preferred embodiment, the number of physical channels is sixteen. Further, the sample demulitplexer 310 sampling rate is preferably two times the data rate of one of the physical channels, or $F_F = 2F_S$ where F_s is the data rate of the physical channel. Each of the decimated sample streams passes through a sampling interface block 320. The sampling interface block 320 provides any sampling domain adjustments necessary in moving the signal from the A/D converter 220 and sample demulitplexer 310 to the filter bank 330a-N, connected to the sampling interface block 320. The filter bank 330a-N may provide a number of process steps including filtering the physical channels that are distributed within the decimated sample streams prior to the physical channels being separated. The filtering provides rejection of any energy not within a

physical channel while generating a reconstructive set of base signals for selecting out the physical channels in further downstream processing. The filter bank 330a-N may also provide a time realignment of each of the decimated sample streams. In a preferred embodiment, the filter bank 330a-N consists of a bank of bifurcated filters that collectively generate a filtered signal vector. Since all the bifurcated filters have a similar structure, only one bifurcated filter is described in detail herein.

A bifurcated filter may typically consist of two parallel branches of coefficient multiply and delay operations with the operations in each of the branches separately summed together. Each branch is designated as either an even output signal or an odd output signal. The number of multiply and delay operations in each branch may vary based on design criteria. For instance, sixteen weighted multiply and a number of coefficient multipliers may be used in each bifurcated filter. The delay element is controlled by a decimated sample clock signal, not shown, at a frequency F_f. The summing node separately adds together the values from each of the odd weighted multipliers and even weighted multipliers to form the odd and even output signal. The orientation of the filter branches and operations within the branches allows special properties to exist. These properties include amplitude inversion of the signal or time reversing the signal within the branch. As noted, other filter structures may be used, as known by those skilled in the art, in conjunction with the various techniques of simultaneous channel reception techniques.

The output signal, a filter signal vector containing 2N signal streams, from the filter bank 330a-N connects to a bank of summing nodes 340a-N. Referring to the preferred embodiment, the even and odd outputs from each of the different bifurcated filters may be combined in a cross-coupling pattern. The even output of filter 0 is summed with the odd output of filter N-1, even output of filter 1 with the odd output of filter N-2, and so on as shown. The summing nodes 340a-N generate a set of filtered sample streams.

The filtered sample streams at the output of summing nodes 340a-N connect to a distributor block 350. The main purpose of the distributor block 350 is to process the filtered sample streams generated by the filter block 330a-N and summing nodes 340a-N to reconstruct the set of physical channels, originally provided in the L-band signal, from the decimated and filtered sample streams. The processing may include recombining the streams in a manner using mathematical operations. In a preferred embodiment the distributor block 350 uses a type IV Discrete Cosine Transform (DCT) for processing the filtered sample streams. The bifurcated filter structure described previously further permits a small DCT structure in implementation by making use of the inversion and time reversal properties of the filter. The bifurcated filter structure may also permit use of a DCT employing a sparse matrix decomposition structure.

The combination of the filter bank 330a-N, summing node 340a-N, and distributor 350 results in generating a set of output streams, each representing the separated data content from a physical channel. The set of individual physical channels from the distributor 350 are generated from the set of decimated sample streams where each stream contains content from each of the physical channels in a sample aliased condition. It should be noted that other methods may be employed for accomplishing recovery of separate physical channels simultaneously from a single signal.

The output of distributor block 350 represents N individual physical channels positioned at or near to baseband frequency. Each physical channel, in digital signal form, may be located on a separate signal line at the output of distributor block 350. Each of the separate signal lines connect to a channel selector block 360. The channel selector block 360 may select a set of physical channels from the original N input channels provided. Any number of channels up to the full number N may be selected. For instance, four channels may be selected. The number of channels permitted for selection in channel selector block 360 is a

design choice, and the full number of permitted channels for selection does not have to be selected at any one time. Additionally, any further physical channel separation may be performed, such as removing any aliasing components present due to the complex form of the signal as a result of the previously described processing.

The channel selector block 360 receives inputs from a controller 370 regarding which, if any, of the originally received physical channels is currently requested by the customer. The controller 370 may connect to the sample demultiplexer 310, interface 320, filter bank 330a-N, and distributor 350 in addition to connecting to channel selector 360. The controller 370 may also provide an interface for user inputs or a communications input in order to receive and convey the user requested channel information from multiple locations. As described previously, the user inputs may be supplied through the signal cable or through some other communications means. Also, as described previously, a home or customer premises may supply more than one customer input. In addition, controller 370 may provide additional functions for operation of the demultiplexer 310, interface 320, filter bank 330a-N, and assembler 350, such as clock functions, as necessary. The controller 370 may also be embodied as a portion of a larger controller function responsible for controlling and managing, for instance, the entire FTM device.

Turning now to FIG. 4, a block diagram 400 of a further embodiment of the present invention is shown. FIG. 4 illustrates an implementation of the digital channel re-combiner 240. The M outputs, representing a set of selected physical channels, of channel selector 360 are provided to the assembler 410. As described previously, the M outputs of the channel selector 360 may be equal to or less than the N physical channels present in the original L-band signal. In a preferred embodiment, the assembler 410 may receive up to N inputs. If the number of signals provided from channel selector 360 is less than N, the remaining inputs of channel assembler 410 are placed in a condition of

"null" or no input. Additionally, the assembler 410 may also provide the ability to re-order the M input signals. For instance, if the M signals provided to the assembler 410 are physical channels in positions 1, 2, 3, and 4 from selection of the original N channels, the assembler 410 may re-position the M signals by addressing them as inputs 1, 5, 9, and N-1. In this manner, further processing, including internal or external filtering may be simplified. Also, the re-positioning permits re-spacing of the M signals.

The assembler 410 provides processing for converting the selected channels into a set of signals forming a base set of parallel data streams that can then be filtered prior to remultiplexing and converting to an analog signal. The channel re-combiner 410 provides N outputs as a set of converted sample streams to inverse filter bank 420a-N. The inverse filter bank 420a-N provides filtering and/or time delay operations necessary to permit signal remultiplexing. The output of the inverse filter bank 420a-N provides a set of inverse filtered sample streams.

The inverse filtered sample streams at the output of the inverse filter bank 420a-N are provided to the sample multiplexer 430. The sample multiplexer 430 re-combines the samples, in a time multiplexing fashion, into a single sample stream. The sampling rate of the new single sample stream is preferably $2NF_s$ (F_s is the data rate of one channel). Clock signals representing both the input parallel sample stream rate and the new sampling rate at the output of the sample multiplexer 430 are also provided.

In a preferred embodiment, the assembler 410 is realized as an inverse type IV DCT, and the filter bank 420a-N is realized as an effective inverse bifurcated filter bank with respect to filter bank 330a-N as previously described. In this and other possible approaches, advantages exist due to the sparse matrix factorization stages containing a defined sparse inverse as well as the complementary form of the filtering stages. For example, the Type IV DCT is its own inverse i.e.,

(DCT IV)^2=I (identity matrix), and the bifurcated filters work with the transform elements to shape the bands of independent physical channels. Also, the inverse filter bank 420a-N, shown as a bifurcated filter structure has a signal splitting at its input for providing a cross coupling of signals to the even and odd branches of the individual filters. After each branch in the individual filters has completed processing, the even and odd branches of each individual filter are summed together to form the individual output signal.

Alternatively, since the type IV DCT function in both the distributor 350 and assembler 410 may be the same, only one block for both operations may be used. For example, a single block may, in conjunction with a signal multiplexer (not shown), provide either an output signal representing the set of individual physical channels or the base set of parallel data streams in alternating operations.

A controller 470 may connect to the assembler 410, filter bank 420a-N, and sample multiplexer 430. The controller 470 may control the final selection process and ordering of selected physical channels in assembler 410. The controller 470 may follow a pre-programmed allocation and ordering algorithm, or may process user inputs to determine the allocation and ordering. The controller 470 may also provide an interface for user inputs or a communications input in order to receive and convey the user requested channel information from multiple locations. As described earlier, a home or customer premises may supply more than one customer input. In addition, controller 470 may provide additional functions for operation of the assembler 410, filter bank 420a-N, and multiplexer 430 such as clock functions, as necessary. The controller 470 may also be embodied as a portion of a larger controller function responsible for controlling and managing, for instance, the entire FTM device.

Additionally, if the M signals at the input to the assembler 410 are less than the N original channels, the channel re-combiner may also

change the overall sampling rate. The assembler 410 may be reconfigured to process the M signals in an M point transform, producing M parallel data streams. The filter bank may subsequently contain only M branches and the sample multiplexer process only M inputs. The clocks, supplied to the D/A converter as well as other blocks with diagram 400 may also be a scaled version of the clock used for digital channel selector 230. For instance, if M is one half the number N, then the clock signal for the digital channel re-combiner 240 may be one half the frequency of the clock signal for the digital channel selector 230. Note that the clock signal supplied to the other blocks working on parallel data streams may remain unaffected.

Further, the choice of value of M may be chosen to permit a maximum of allowable channels at any time. However, in actual operation, a number less than M channels may actually be in use.

Turning now to FIG. 5, a block diagram of another embodiment of the present invention is shown. FIG. 5 illustrates a three L-band signal input FTM utilizing the inventive concept described herein. Each L-band input signal is processed through RF input processing, not shown. Each L-band signal is further processed in A/D converter 520a-c, and digital channel selectors 530a-c as described previously. Also, D/A converter 550 and output RF processing block 560 operate as described previously.

Each digital channel selector 530a-c is capable of producing M outputs representing M physical channels where M is less than or equal to the N original physical channels from an L-band signal. Each L-band signal may provide a different number of physical channels.

The digital channel re-combiner 540 may process up to N channels in its assembler block as described above. The assembler in the digital channel re-combiner 540 also includes switching and selection circuits to manage which of the M inputs from each of the digital channel selectors 530a-c are processed in the digital channel re-combiner 540.

The management and switching function is controlled by the controller 570.

The controller 570 provides functions to ensure that a selected combination of the M outputs from the selectors 530a-c does not exceed the N inputs for selected channels possible for processing in digital channel re-combiner 540. The controller 570 receives inputs from the one or more users and processes the inputs to determine the correct combination of inputs. In a preferred embodiment, each of the digital channel selectors 530a-c may provide up to six signals to the digital channel re-combiner. The digital channel re-combiner 540 may accept only sixteen signals. The controller 570 may determine, for instance based on inputs from users, that only five inputs will be used from digital channel selectors 530a and 530b, and all six will be used from digital channel selector 530c. Additional user inputs may then require a change to this apportionment. The controller 570 may also provide control or other necessary signals such as clock signals to A/D converters 520a-c, digital channel selectors 530a-c and D/A converter 550.

The digital channel re-combiner 540 may also contain signal processing such as digital signal level adjustment applied to each of the selected channels. Level adjustment may allow all selected channels to be delivered at approximately the same signal level improving the operation of home equipment such as settop boxes.

Block diagram 500 forms a multi-input, single output channel selection, translation, and distribution device. The device produces an output of up to N channels in a single signal for delivery over a single coaxial cable, from an input containing up to three times N possible input channels presented in three separate signals. The use of three inputs is illustrative, and a greater or fewer number of inputs containing a greater or fewer number of possible input channels may be used.

Turning now to FIG. 6, a flow chart 600 showing an embodiment of the method of the present invention is shown. At step 602, one or more

incoming satellite signals are received by a device, such as the FTM device described previously in block diagram 500. Next, at 604, the incoming satellite signals are converted to digital signals. The conversion is preferably performed by A/D converters 530a-c, and may further include a processing means for separating the individual physical channels after the conversion such as described in digital channel selectors 530a-c.

Next, at step 606, the desired physical channels are selected to form a group of selected physical digital channels in parallel. The selected physical channels are selected in the digital channel selectors 530a-c based on requests by the customer's home equipment processes and managed by, for instance, controller 570. The controller 570 may be responsible for receiving and managing multiple requests and providing the proper information to the digital channel selectors 530a-c as well as the digital channel re-combiner 540.

The group of selected digital channels, at step 608, are re-combined in a frequency diverse manner to form a signal occupying a range of frequencies and containing the selected digital channels at separate frequencies. The recombination may include a means for processing the group of selected digital channels such as described for digital channel re-combiner 540. At step 610, the recombined frequency diverse signals are converted back into an analog signal containing the selected channels at separate frequencies. The conversion may be done using a D/A converter 550 and may also include any additional processing as described for output RF processing block 560. Finally, at step 612, the analog signal is sent or transmitted to additional devices, for instance devices found in customer premises connected by a single coaxial cable.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. The

foregoing merely illustrates the principles of the invention and it will thus be appreciated that those skilled in the art will be able to devise numerous alternative arrangements which, although not explicitly described herein, embody the principles of the invention and are within its spirit and scope. For example, although illustrated in the context of separate functional elements, these functional elements may be embodied on one or more integrated circuits (ICs). Similarly, although shown as separate elements, any or all of the elements of may be implemented in hardware, software, or a combination of both. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the scope of the present invention as defined by the appended claims.

What is claimed is:

1. An apparatus (500) comprising:

a receiver (520a-c, 530a-c) for receiving and digitizing a plurality of first signals, each signal containing one or more different channels and for simultaneously recovering a plurality of selected channels from said plurality of first signals; and

a transmitter (540, 550, 560) for combining said plurality of selected channels and producing a second signal.

2. The apparatus (500) set forth in claim 1, wherein said receiver (520a-c, 530a-c) further comprises:

a sampler (310, 320, 330a-N) for sampling said plurality of first signals to provide a plurality of decimated sample streams; and

a distributor (350) operatively connected to said sampler (310, 320, 330a-N) for processing said plurality of decimated sample streams to provide output signals representative of said one or more different physical channels.

3. The apparatus (500) of claim 2, wherein said distributor (350) includes a transform element.

4. The apparatus (500) of claim 3, wherein said transform element performs matrix-based processing on said plurality of decimated sample steams using a sparse matrix factorization of a type IV discrete cosine transform.

5. The apparatus (500) of claim 2, wherein said sampler (310, 320, 330a-N) further comprises:

a demultiplexer (310) for demultiplexing the signal into said plurality of decimated sample streams; and

a plurality of filters (330a-N) operatively connected to said demultiplexer (310) for processing said plurality of decimated sample streams.

6. The apparatus (500) of claim 5, wherein said plurality of filters (330a-N) includes a plurality of bifurcated filters.

7. The apparatus (500) of claim 1, wherein said receiver (530a-c) further comprises a selector (360) operatively connected to said distributor (350) for selecting said plurality of selected channels.

8. The apparatus (500) of claim 1, wherein said transmitter (540, 550, 560) further comprises:

an assembler (410) that assembles said plurality of selected channels to provide a set of parallel data streams representing the combination of said plurality of channels; and

a converter (420a-N, 430) for converting said parallel data streams into said second signal.

9. The apparatus (500) of claim 8, wherein said assembler (410) includes a transform element.

10. The apparatus (500) of claim 9, wherein said transform element performs matrix-based processing on said plurality of selected channels using a sparse matrix factorization of type IV discrete cosine transform.

11. The apparatus (500) of claim 8, wherein said converter further comprises:

a plurality of filters (420a-N) for processing said plurality of parallel data streams; and

a multiplexer connected to said plurality of filters for multiplexing said plurality of parallel data streams into a single sample stream.

12. The apparatus (500) of claim 11, wherein said plurality of filters (420a-N) includes a plurality of bifurcated filters.

13. A method (600) for providing frequency translation comprising:

receiving (602) a first signal having a plurality of different frequency channels;

selecting (606) a set of frequency channels from said plurality of different frequency channels;

combining (608) said set of frequency channels to form a second signal; and

transmitting (612) said second signal.

14. The method (600) of claim 13, wherein the step of selecting further comprises:

processing (604) said first signal to provide a plurality of decimated sample streams; and

performing (606) a transform on said number of decimated sample streams to provide transform output signals.

15. The method (600) of claim 14, wherein the step of processing (604) includes:

demultiplexing the signal into the number of decimated sample streams; and

filtering said number of decimated sample streams with a plurality of filters for matching said transform.

16. The method (600) of claim 15, wherein said plurality of filters include a plurality of bifurcated filters and said transform is a type IV discrete cosine transform.

17. The method (600) of claim 13, wherein the step of selecting further comprises re-ordering said set of frequency channels.

18. The method (600) of claim 13, wherein said step of combining (608) further comprises:

performing transform-based processing on said set of different frequency channels to provide a plurality of parallel data streams; and

processing said plurality of parallel data streams to provide said second signal.

19. An integrated circuit (500) for use in a receiving system, which receives signals representing a plurality of channels, the integrated circuit comprising:

a demultiplexing element (310) for demultiplexing a received sampled signal to produce a plurality of first data streams;

a transform element (350, 410) for transforming said plurality of first data streams into a plurality of transform output signals, and for transforming at least two of said plurality of transform output signals into a plurality of second data streams; and

a multiplexing element (430) for mulitplexing said plurality of second data streams and outputting a sampled signal.

20. The integrated circuit (500) of claim 19, wherein said transform element (350, 410) uses a type IV discrete cosine transform.

21. The integrated circuit (500) of claim 20, further comprising:

a first filter element (330a-N) operative to filter said plurality of first data streams prior to providing said plurality of first data streams to said transform element; and

a second filter element (420a-N) operative to filter said plurality of second data streams prior to providing said plurality of second data streams to said multiplexing element.

22. An apparatus (500) for frequency translation comprising:

means for receiving (520a-c) a first signal having a plurality of different frequency channels;

means for translating (530a-c) said first signal into a set of signals representing said plurality of different frequency channels;

means for selecting (530a-c) a set of channels from said set of signals;

means for combining (540) said set of channels to form a second signal; and

means for transmitting (550, 560) said second signal.

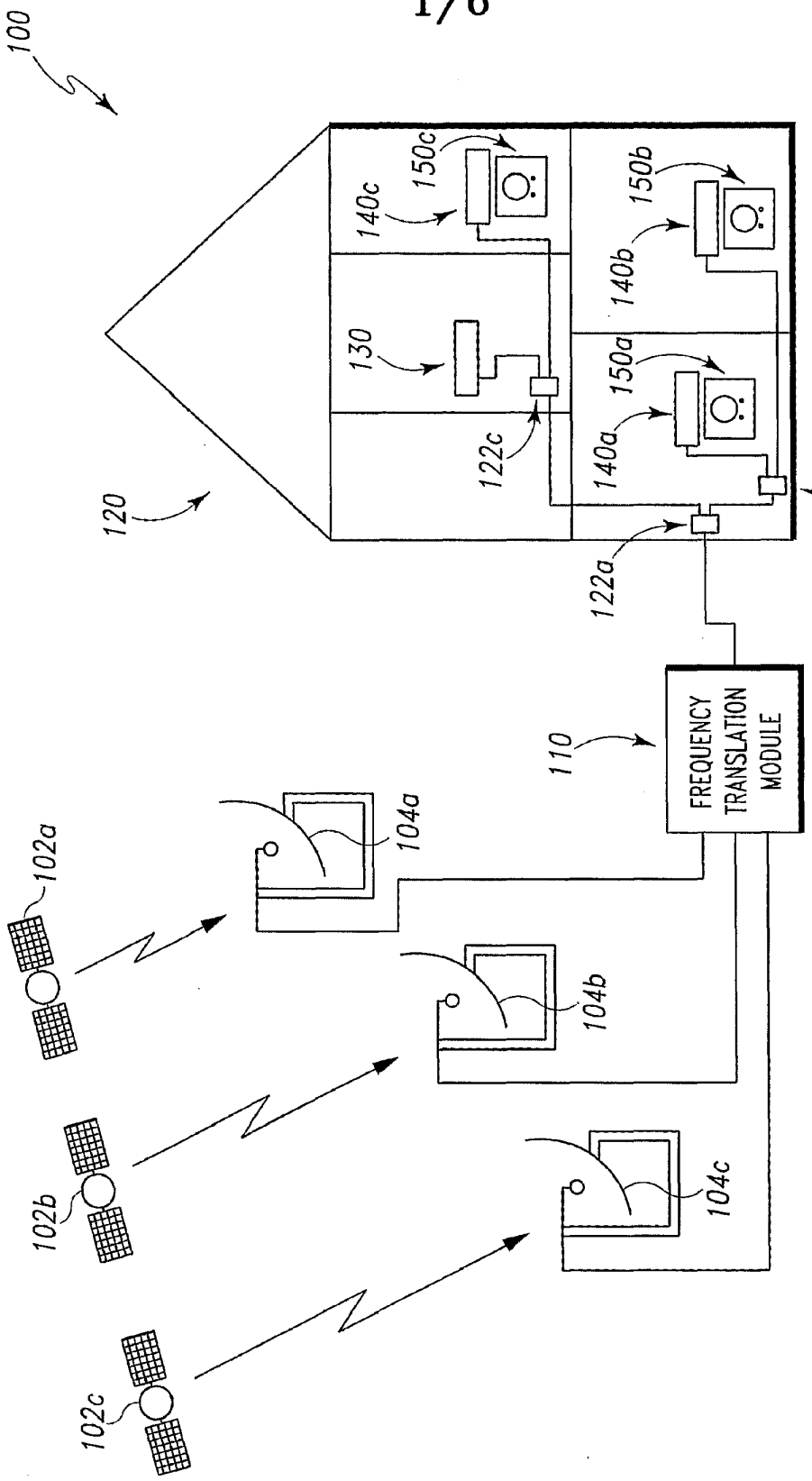

100
120
130
140a
140b
140c
150a
150b
150c
122a
122b
122c
110
FREQUENCY TRANSLATION MODULE
102a
102b
102c
104a
104b
104c

Fig. 1

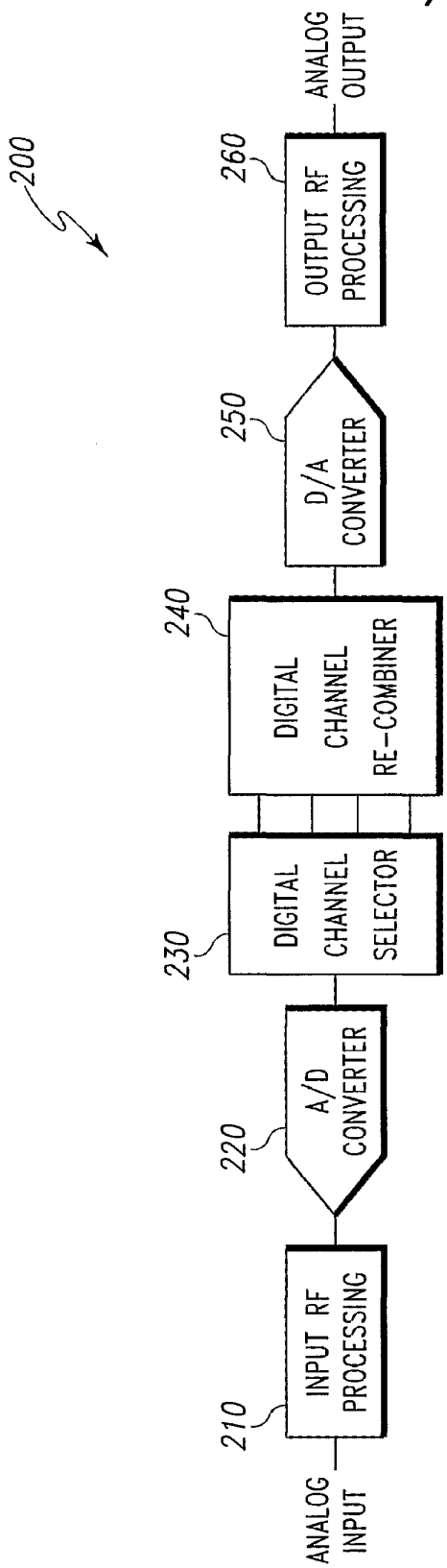

200
ANALOG INPUT
210
INPUT RF PROCESSING
220
A/D CONVERTER
230
DIGITAL CHANNEL SELECTOR
240
DIGITAL CHANNEL RE-COMBINER
250
D/A CONVERTER
260
OUTPUT RF PROCESSING
ANALOG OUTPUT

Fig. 2

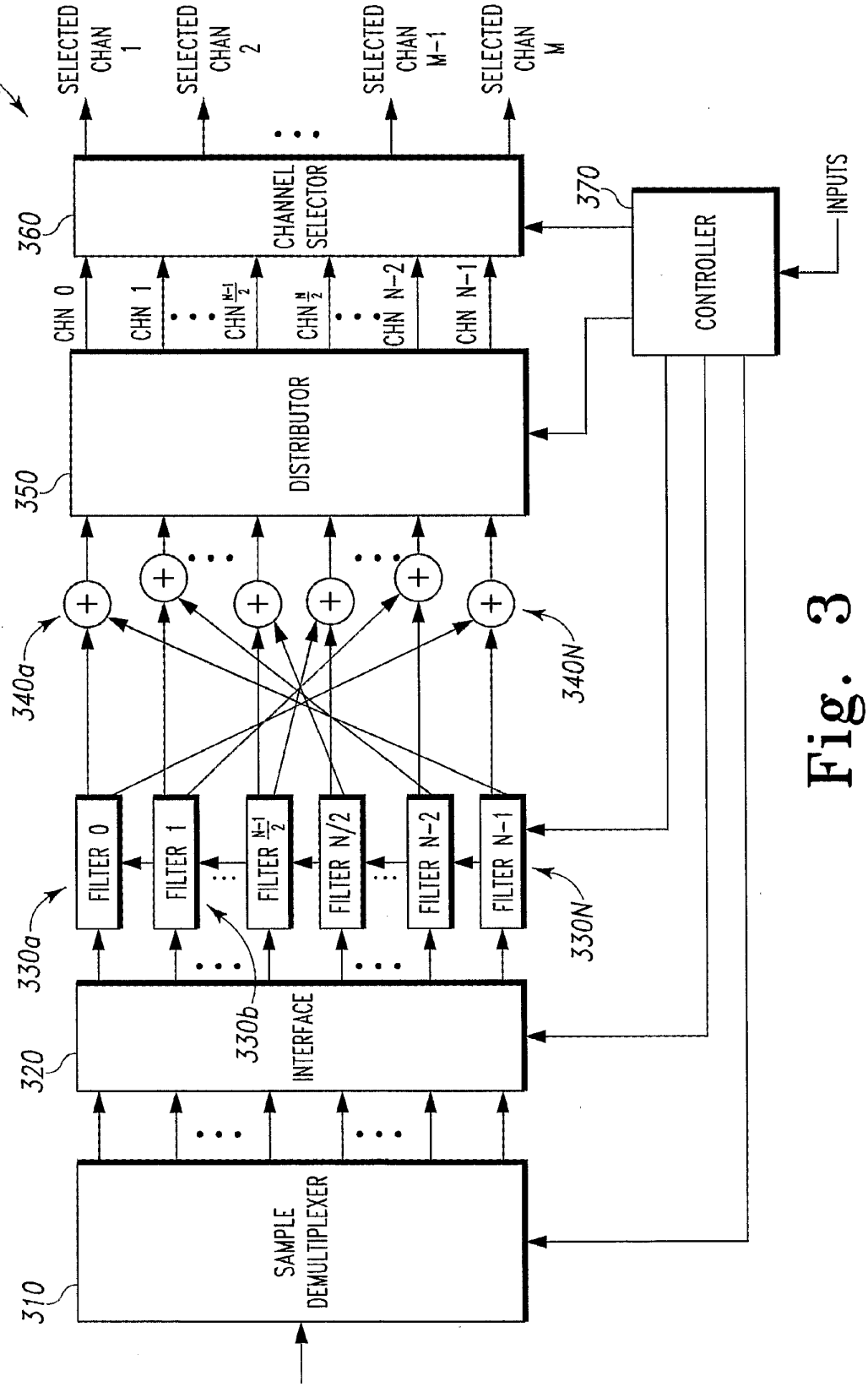

300
SELECTED CHAN 1
SELECTED CHAN 2
SELECTED CHAN M-1
SELECTED CHAN M
360
CHANNEL SELECTOR
370
CONTROLLER
INPUTS
CHN 0
CHN 1
CHN (N-1)/2
CHN N/2
CHN N-2
CHN N-1
350
DISTRIBUTOR
340a
340N
FILTER 0
FILTER 1
FILTER (N-1)/2
FILTER N/2
FILTER N-2
FILTER N-1
330a
330b
330N
320
INTERFACE
310
SAMPLE DEMULTIPLEXER

Fig. 3

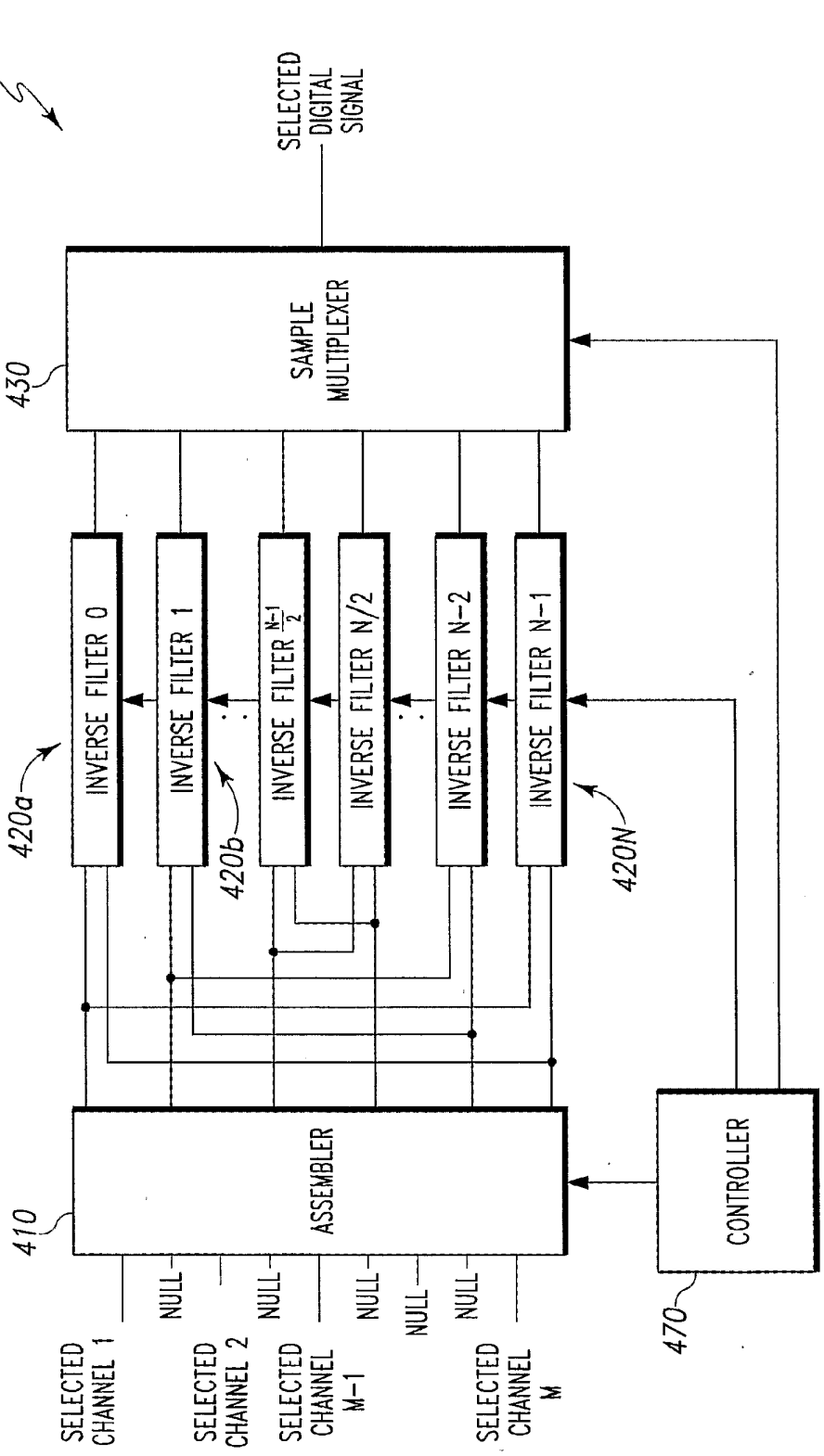

400
SELECTED DIGITAL SIGNAL
SAMPLE MULTIPLEXER
430
INVERSE FILTER 0
INVERSE FILTER 1
INVERSE FILTER $\frac{N-1}{2}$
INVERSE FILTER N/2
INVERSE FILTER N-2
INVERSE FILTER N-1
420a
420b
420N
ASSEMBLER
410
CONTROLLER
470
SELECTED CHANNEL 1
NULL
SELECTED CHANNEL 2
NULL
SELECTED CHANNEL M-1
NULL
NULL
SELECTED CHANNEL M

Fig. 4

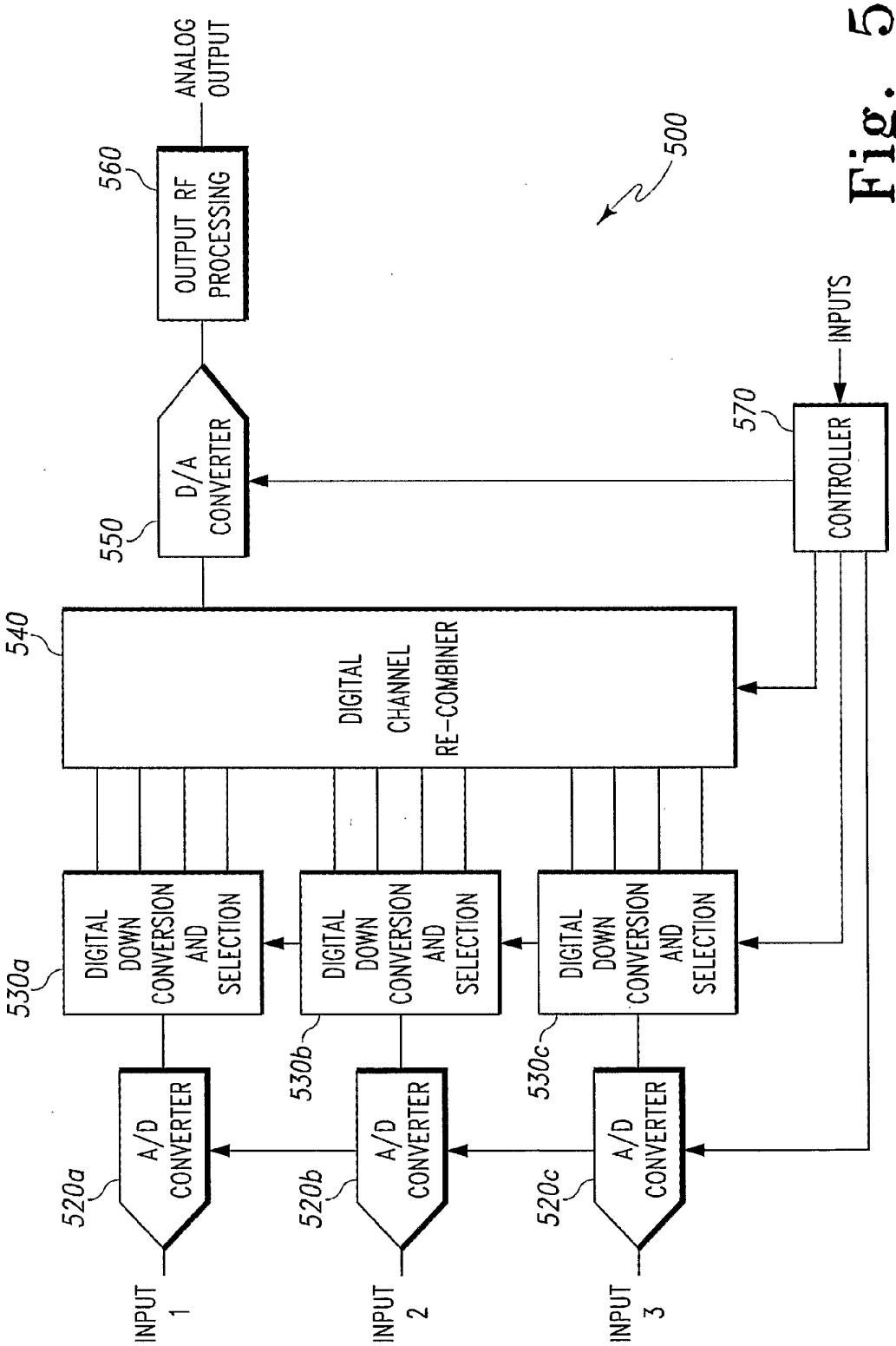

500
560
OUTPUT RF PROCESSING
ANALOG OUTPUT
550
D/A CONVERTER
570
CONTROLLER
INPUTS
540
DIGITAL CHANNEL RE-COMBINER
530a
DIGITAL DOWN CONVERSION AND SELECTION
530b
DIGITAL DOWN CONVERSION AND SELECTION
530c
DIGITAL DOWN CONVERSION AND SELECTION
520a
A/D CONVERTER
520b
A/D CONVERTER
520c
A/D CONVERTER
INPUT 1
INPUT 2
INPUT 3

Fig. 5

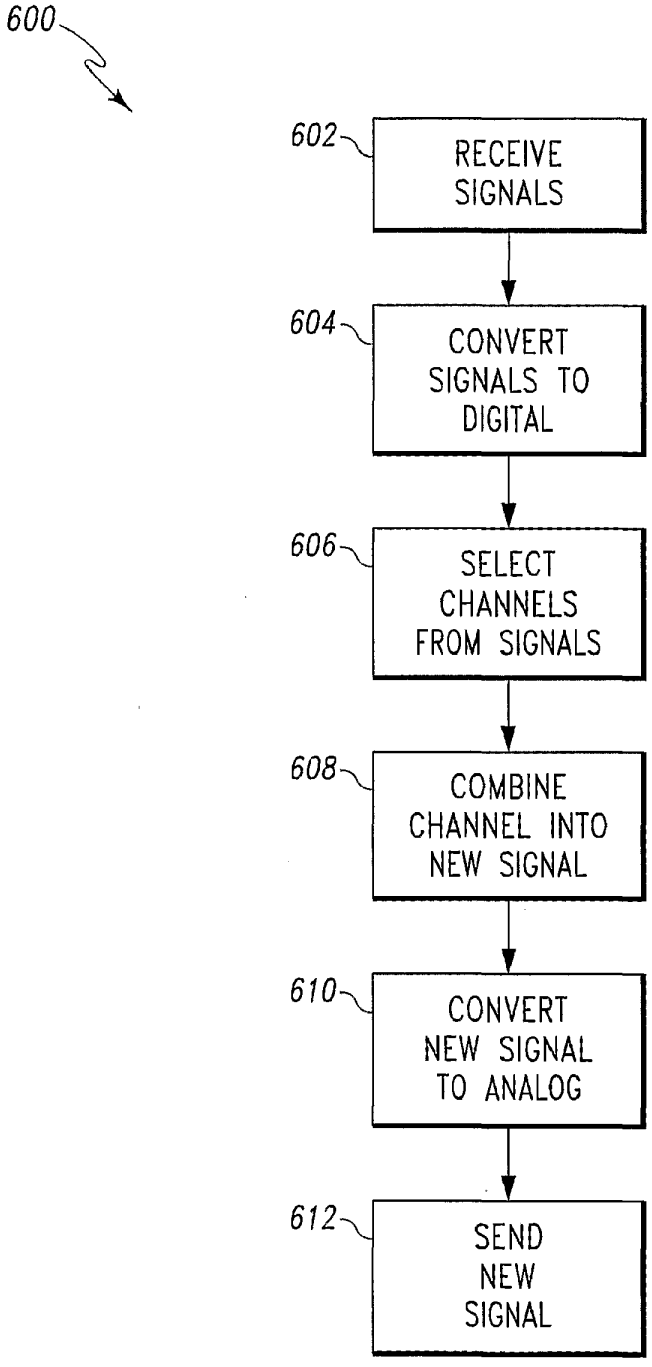

600
602
RECEIVE SIGNALS
604
CONVERT SIGNALS TO DIGITAL
606
SELECT CHANNELS FROM SIGNALS
608
COMBINE CHANNEL INTO NEW SIGNAL
610
CONVERT NEW SIGNAL TO ANALOG
612
SEND NEW SIGNAL

Fig. 6

Exhibit 1008

Declaration of Stuart Lipoff

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNIFIED PATENTS, LLC
Requester

v.

ENTROPIC COMMUNICATIONS, LLC
Patent Owner

Reexamination No. *to be assigned*
U.S. Patent 9,210,362

DECLARATION OF STUART LIPOFF

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I. INTRODUCTION

1. My name is Stuart Lipoff, and I am over 21 years and otherwise competent to make this Declaration. I make this Declaration based on facts and matters within my own knowledge and on information provided to me by others, and, if called as a witness, I could and would competently testify to the matters set forth herein.

2. I have been retained as a technical expert witness in this matter by Counsel for the Requester, Unified Patents, LLC ("Requester") to provide my independent opinions on certain issues requested by Counsel for Requester relating to the accompanying Ex Parte Reexamination of U.S. Patent No. 9,210,362 ("the '362 Patent"), challenging Claims 1 and 11 (the "Challenged Claims"). My compensation in this matter is not based on the substance of my opinions or on the outcome of this matter. I have been informed that Entropic Communications, LLC ("Patent Owner") is the purported owner of the '362 Patent. I note that I have no financial interest in Requester or Patent Owner, and I have no other interest in the outcome of this matter.

3. I have reviewed, had input into, and endorse the discussions in the Requester's Request for Ex Parte Reexamination of the '362 Patent (the "Request"), including the statements in the Request regarding the '362 Patent and its prosecution history, the scope of the claim, the prior art's disclosure of the claim, and the

statements throughout the Request regarding a POSITA's knowledge and understanding.

II. QUALIFICATIONS

4. In formulating my opinions, I have relied on my knowledge, training, and experience in the relevant field, which I have summarized below.

5. I am currently president of IP Action Partners Inc., a consulting practice that serves the telecommunications, information technology, media, electronics, and e-business industries.

6. I earned a Bachelor of Science degree in Electrical Engineering in 1968 and a second Bachelor of Science degree in Engineering Physics in 1969, both from Lehigh University. I earned a Master of Science degree in Electrical Engineering from Northeastern University in 1974, and then a Master of Business Administration degree from Suffolk University in 1983.

7. I hold a Federal Communications Commission ("FCC") General Radiotelephone License. I also hold a Certificate in Data Processing from the Institute for the Certification of Computing Professionals ("ICCP"), which is supported by the Association for Computing Machinery ("ACM").

8. I am also a registered professional engineer (PE) in the Commonwealth of Massachusetts and in the State of Nevada.

9. I am a fellow of the Institute of Electrical and Electronics Engineers

("IEEE") Consumer Electronics, Communications, Computer, Circuits, and Vehicular Technology Groups. I have been a member of the IEEE Consumer Electronics Society National Board of Governors (formerly known as the Administrative Committee) since 1981, and I was Boston Chapter Chairman of the IEEE Vehicular Technology Society from 1974 to 1976. I served as the 1996-1997 President of the IEEE Consumer Electronics Society, and from 1999 to 2018 I served as Chairman of the Society's Technical Activities and Standards Committee and as Vice President of Publications for the Society. Since 2018 I have served as Vice President of Standards and Industry Activities for the Society. I have also served as an Ibuka Award committee member for the IEEE's Award in the field of consumer electronics.

10. I have prepared and presented numerous papers at the IEEE and at other professional meetings. For example, in fall 2000, I served as general program chair for IEEE's Vehicular Technology Conference on advanced wireless communication technology. I have organized sessions at The International Conference on Consumer Electronics, and I was the 1984 program chairman. I conducted an eight-week IEEE-sponsored short course on Fiber Optics System Design. I received IEEE's Centennial Medal in 1984, and I received IEEE's Millennium Medal in 2000.

11. As Vice President and Standards Group Chairman for the Association of Computer Users ("ACU") from 1980 to 1983, I served as the ACU representative

to the ANSI X3 Standards Group. From 1976 to 1978, I served as Chairman of the task group on user rule compliance for the FCC's Citizens Advisory Committee on Citizen's Band Radio.

12. Over the last 25 years, I have been a member of the Society of Cable Television Engineers, the Association for Computing Machinery, and The Society of Motion Picture and Television Engineers. From 2001 to 2004, I served as a member of the USA advisory board to the National Science Museum of Israel. In 1998, I presented a short course on international product development strategies as a faculty member for Technion Institute of Management in Israel. From 2001 to 2003, I served as a member of the board or directors of The Massachusetts Future Problem Solving Program.

13. I am a named inventor on seven United States patents and have several publications on data communications in publications, including Electronics Design, Microwaves, EDN, the Proceedings of the Frequency Control Symposium, Optical Spectra, and IEEE publications.

14. During my professional career dating from 1969 to the present, I have been heavily engaged in the study, analysis, evaluation, design, and implementation of products and technology associated with consumer electronics and electronic appliances.

15. For 25 years, I worked for Arthur D. Little, Inc. ("ADL"), where I

became Vice President and Director of Communications, Information Technology, and Electronics ("CIE"). Prior to my time at ADL, I served as a Section Manager for Bell & Howell Communications Company for four years, and prior to that, as a Project Engineer for Motorola's Communications Division for three years.

16. At ADL, I was responsible for the firm's global CIE practice in laboratory- based contract engineering, product development, and technology-based consulting. At both Bell & Howell and Motorola, I had project design responsibility for wireless communication and paging products.

17. While employed at ADL, I served as the leader of a project that developed a series of specifications for residential cable modems known as Data over Cable Service Interface Specification, or "DOCSIS." The scope of work for this project included developing a roadmap and strategic framework for evolving the business from internet services to broadband services combining voice, data, and secure electronic content delivery. This project was performed by ADL under contract to the Multimedia Cable Network System ("MCNS") consortium and the specifications resulting from that project have since been adopted by the United Nations as a global telecommunications specification.

18. Following my time at ADL, I managed a project (through IP Action Partners) for Next Generation Network Architecture, LLC ("NGNA") that produced a five-year planning horizon for services and technology in the cable industry. The

services and vision were then mapped to overall architectures impacting network elements in the back office, head-end, outside plant, and customer premises, and documented in next generation network recommendations. The project involved coordination with senior technical staff of several multiple service operators ("MSOs") as well as interactions with over one hundred suppliers and vendors of systems, software, and products in the cable industry.

19. Additional details about my employment history, fields of expertise, and publications are included in my curriculum vitae (attached as Appendix A).

A. Materials Considered

20. As part of my work in forming my opinions in connection with this proceeding, I have reviewed the following materials, which I believe those in the field would reasonably rely upon in forming opinions regarding the subject matter of this proceeding:

Exhibit 1003	("McNeely") WO 2006/119490 to David Lowell McNeely
Exhibit 1004	("Pugel") WO 2007/145637 to Michael Anthony Pugel
Exhibit 1005	("Gomez") U.S. Patent No. 8,224,274 to Ramon Gomez et al.

For ease of citation, when I cite to any of the non-patent/application references, I refer to the exhibit page number added at the bottom or cover page.

III. LEGAL FRAMEWORK

21. I am a technical expert and do not offer any legal opinions. However, I have been informed about certain legal principles regarding patentability and related matters under United States patent law, which I have applied in performing my analysis and arriving at my technical opinions in this matter.

A. Anticipation

22. I am informed that a person cannot obtain a patent on an invention if it is anticipated by an earlier prior art reference. It is my understanding that, to anticipate a claim under 35 U.S.C. § 102, a reference must disclose each and every element of the claim, arranged as in the claim.

B. Obviousness

i. General Framework

23. I am informed that a person cannot obtain a patent on an invention if the differences between the invention and the prior art are such that the subject matter as a whole would have been to a person having ordinary skill in the art obvious at the time of the invention. I am informed that a conclusion of obviousness may be founded upon more than a single item of prior art. I am also informed that obviousness is determined by evaluating the following factors: (1) the scope and content of the prior art, (2) the differences between the prior art and the claim at issue, (3) the level of ordinary skill in the pertinent art, and (4) secondary

considerations of non-obviousness. In addition, the obviousness inquiry should not be done in hindsight. Instead, the obviousness inquiry should be done through the eyes of a person having ordinary skill in the art at the time of the alleged invention.

24. In considering whether certain prior art renders a particular patent claim obvious, I am informed that one must consider the scope and content of the prior art, examples of which include disclosures in patents, trade publications, journal articles, conference papers, industry standards, product literature and documentation, texts describing competitive technologies, requests for comment published by standard setting organizations, and materials from industry conferences.

25. I am informed that for a patent claim to be found obvious, the proper perspective to consider is that of a person having ordinary skill in the art (often referred to as a "PHOSITA," "POSITA," or "POSA") at the time of the alleged invention. I am informed that the factors to consider in determining the level of ordinary skill in the art include (1) the educational level and experience of people working in the field at the time the invention was made, (2) the types of problems faced in the art and the solutions found to those problems, and (3) the sophistication of the technology in the field.

ii. Analogous Art

26. I am informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be "analogous art" to the claimed

invention. I am informed that a reference is analogous art to the claimed invention if: (1) the reference is from the same field of endeavor as the claimed invention (even if it addresses a different problem); or (2) the reference is reasonably pertinent to the problem faced by the inventor (even if it is not in the same field of endeavor as the claimed invention). In order for a reference to be "reasonably pertinent" to the problem, it must logically have commended itself to an inventor's attention in considering his problem. In determining whether a reference is reasonably pertinent, one should consider the problem faced by the inventor, as reflected either explicitly or implicitly, in the specification. I believe that all of the references I considered in forming my opinions in this reexamination are well within the range of references a person having ordinary skill in the art would have consulted by the time of the invention to address the type of problems described in the Challenged Claims.

iii. Combining Known Elements in the Art, Common Sense

27. I am informed that, in order to establish that a claimed invention was obvious based on a combination of prior art elements, a clear articulation of the reason(s) why a claimed invention would have been obvious must be provided. Specifically, I am informed that, under the U.S. Supreme Court's KSR decision, a combination of multiple items of prior art renders a patent claim obvious when there was an apparent reason for a person having ordinary skill at the time of the invention to combine or modify the prior art. I am informed that such reason may include, but

is not limited to, one or more of the following rationales: (A) combining prior art methods according to known methods to yield predictable results; (B) substituting one known element for another to obtain predictable results; (C) using a known technique to improve a similar device in the same way; (D) applying a known technique to a known device ready for improvement to yield predictable results; (E) trying a finite number of identified, predictable potential solutions, with a reasonable expectation of success; (F) identifying that known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; or (G) identifying an explicit teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine the prior art references to arrive at the claimed invention.

28. I am informed that the test for obviousness is *not* whether the features of a secondary reference may be *bodily incorporated* into the structure of the primary reference, but rather whether one of skill would have been motivated to combine the teachings of the prior art references to achieve the claimed invention. Nevertheless, I am informed that an invention that is a combination of prior art must do more than yield predictable results to be non-obvious and that, even where one or more motivations to combine exist, claims are not necessarily obvious unless a person

having ordinary skill in the art would have had a reasonable expectation of success in implementing or applying the proposed combination at the time of the invention.

29. I also am informed that in conducting an obviousness analysis, a precise teaching directed to the specific subject matter of the challenged claim need not be sought out because it is appropriate to take account of the inferences and creative steps that a person having ordinary skill in the art at the time of the invention would employ. In other words, the prior art need not be directed towards solving the same specific problem as the problem addressed by the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem. The prior art considered can be directed to any need or problem known in the field of endeavor at the time of invention and can provide a reason for combining the elements of the prior art in the manner claimed. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and a person having ordinary skill in the art will often have been able to fit the teachings of multiple prior art references like pieces of a puzzle. I am informed that, under the *KSR* standard, common sense is important and should be considered.

30. I also am informed that the fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is

likely the result of ordinary skill and common sense rather than innovation. I am further informed that in many fields it may be that there is little discussion of obvious techniques or combinations, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive the design of an innovation. When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person having ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation, but of ordinary skill and common sense.

iv. Teaching Away

31. I am informed that it is improper to combine references where the references teach away from their combination. I am informed that a reference may be said to teach away when a person of skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the patent applicant. In general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the patentee. I am informed that a reference teaches away, for example, if (1) the combination would produce a seemingly inoperative device, or (2) the references leave the impression that the product would not have the property sought by the

patentee. However, I am informed that a reference does not teach away if it merely expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into the invention claimed. Further, a person of skill will often appreciate that different courses of action often have simultaneous advantages and disadvantages, and I am informed the existence of such does not necessarily obviate a motivation to combine.

v. Secondary Considerations

32. I am informed that even if a *prima facie* case of obviousness is established, the final determination of obviousness must also consider "secondary considerations" if presented. I am informed that in most instances, the patentee raises these secondary considerations of non-obviousness. In that context, the patentee argues an invention would not have been obvious in view of these considerations, which include: (a) commercial success of a product due to the merits of the claimed invention; (b) a long-felt, but unsatisfied need for the invention; (c) failure of others to find the solution provided by the claimed invention; (d) deliberate copying of the invention by others; (e) unexpected results achieved by the invention; (f) praise of the invention by others skilled in the art; (g) lack of independent simultaneous invention within a comparatively short space of time; (h) teaching away from the invention in the prior art.

33. I am further informed that secondary-considerations evidence is only

relevant if the offering party establishes a connection, or nexus, between the evidence and the claimed invention. The nexus cannot be based on prior art features. For example, if commercial success of products allegedly embodying the claims is presented as a secondary indicium of non-obviousness, the patent owner must show that such success is due to features of the claimed invention, and not features unrelated to the claimed invention or that already existed in the prior art. The establishment of a nexus is a question of fact. While I understand that the Patent Owner here has not offered any secondary considerations at this time, I will supplement my opinions in the event that Patent Owner raises secondary considerations during the course of this proceeding.

C. Claim Construction

34. I am informed that in performing an obviousness analysis, it is necessary to understand the scope of the claims. I am also informed the first step in an unpatentability analysis, therefore, involves construing the claims. Second, the construed claim language is then compared to the disclosures of the prior art.

35. I am informed that claims in a reexamination are given their broadest reasonable interpretation consistent with the patent specification. I am informed that, for the purposes of claim construction, expert testimony may be helpful to provide background on the technology at issue, to explain how an invention works, to ensure an understanding of the technical aspects of the patent is consistent with that of a

POSITA, or to establish that a particular term in the patent had a particular meaning in the pertinent field at the time of the invention. However, I am also informed that it is not the role of technical experts to supplant the examiner or the USPTO in applying principles of claim interpretation.

36. For purposes of this proceeding, Counsel has instructed me to understand the claim terms of the Challenged Claim in a way that is generally consistent with the terms' broadest reasonable interpretation consistent with the specification of the '362 Patent. My analysis below is consistent with these principles. I provide analysis for certain terms below, and have interpreted the remainder of the claim terms in accordance with their broadest reasonable interpretation consistent with the specification.

i. Order of Steps in Claim 1

37. Claim 1 recites a step of "downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies" and a step of "digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies."

38. I have been informed that a district court has construed these steps such that the two steps need not be performed in order. *See* EX1007. That is, the step of "downconverting … a plurality of frequencies" step does not need to be performed before the step of "digitizing … said plurality of frequencies."

39. I have applied this construction in my analysis below.

ii. **"mixer module"**

40. Claim 11 recites "downconverting, by a **mixer module** of said wideband receiver system, a plurality of frequencies..." Claim 1 recites a "**mixer module** configured to downconvert a plurality of frequencies…"

41. I understand that certain claim terms can be drafted in "means-plus-function" format, when the claim uses the term "means" (or another nonce word) for performing a function without reciting specific structure for performing the function. I understand that, in these circumstances, the claim is to be interpreted such that the structure for performing the function includes corresponding structure recited in the specification. However, I also understand that, even if a claim term uses the word "means" or a nonce word for performing a function, the term may not be considered a means-plus-function term if the claim term, to a POSITA, has sufficiently definite meaning as the name for structure that performs the function.

42. In the context of the claims' "mixer module" it is my opinion that a POSITA would have recognized the term to have a sufficiently definite meaning as the name for structure that performs the function in the claims of downconverting a plurality of frequencies. For example, the specification of the '362 Patent describes a "mixer" that performs this function, which a POSITA would understand as an example of the meaning of the "mixer module" recited in the claims.

iii. "wideband analog-to-digital converter (ADC) module"

43. Claim 11 recites "digitizing, by a **wideband analog-to-digital converter (ADC) module** of said wideband receiver system, said plurality of frequencies…" Claim 1 recites "a **wideband analog-to-digital converter (ADC) module** configured to digitize said plurality of frequencies…"

44. In the context of the claims' "wideband analog-to-digital converter (ADC) module" it is my opinion that a POSITA would have recognized the term to have a sufficiently definite meaning as the name for structure that performs the function in the claims of digitizing a plurality of frequencies. For example, the specification of the '362 Patent describes "[a]nalog-to-digital converters ADC1 218 and ADC2 228" that perform this function, which a POSITA would understand as an example of the meaning of the "wideband analog-to-digital converter (ADC) module" recited in the claims.

IV. OPINION

A. Level of Skill of a Person Having Ordinary Skill in the Art

45. I was asked to provide my opinion as to the level of skill of a person having ordinary skill in the field of the '362 Patent at the time of the claimed invention (referred to herein as a "POSITA"). I have been instructed to assume that the time of the claimed invention of the '362 Patent is April 17, 2009. In determining the characteristics of a POSITA, I was told to consider several factors, including the

type of problems encountered in the art, the solutions to those problems, the rapidity with which innovations are made in the field, the sophistication of the technology, and the education level of active workers in the field. I also placed myself back in the time frame of the claimed invention and considered the colleagues with whom I had worked at that time.

46. In my opinion, a POSITA would be a person having, as of April 17, 2009: (1) an undergraduate degree in electrical engineering, or a closely related field, or similar advanced post-undergraduate education; and (2) two to three years of work experience in the field of radio frequency systems (e.g., cable television systems), with more education substituting for less experience and vice versa. Such a person of ordinary skill in the art would have been capable of understanding the '362 Patent and the prior art references discussed herein.

47. Based on my education, training, and professional experience in the field of the claimed invention, I am familiar with the level and abilities of a POSITA. Additionally, I met at least these minimum qualifications at least as of April 17, 2009. Further, although my qualifications may exceed those of the hypothetical person defined above, my analysis and opinions regarding the '362 Patent have been rendered from the perspective of a POSITA during the relevant time frame.

B. Background of the Technology

i. Background of the '362 Patent

48. The '362 Patent is titled Wideband Tuner Architecture" and it is directed to a "wideband receiver system" which "comprises a mixer module, a wideband analog-to-digital converter (ADC) module, and digital circuitry." '362 Patent (EX1001), Abstract.

49. The '362 Patent Abstract provides a summary of the claims discussed below:

> A wideband receiver system comprises a mixer module, a wideband analog-to-digital converter (ADC) module, and digital circuitry. The mixer module is configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels. The wideband ADC module is configured to digitize the swatch of frequencies comprising the plurality of desired television channels and the plurality of undesired television channels. The digital circuitry is configured to select the desired plurality of television channels from the digitized plurality of frequencies, and output the selected plurality of television channels to a demodulator as a digital datastream.

'362 Patent (EX1001), Abstract.

50. In more detail, the '362 Patent purports to relate to "wideband receiver systems that are capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum and grouping them into a contiguous, or substantially-contiguous, frequency spectrum."

'362 Patent (EX1001), 1:15-23. I note, however, that the claims challenged below do not discuss contiguous or non-contiguous portions of a frequency spectrum.

51. The '362 Patent details as background information that:

> "Receivers used to down-convert and selectively filter TV channels are referred to as tuners, and tuners designed to concurrently receive several TV channels are referred to as wideband tuners. Existing tuners for these applications down-convert a swath of channels to an intermediate frequency, which are then sent to a demodulator. Because the swath of channels is not contiguous, this swath includes the desired channels as well as undesired channels. The demodulator employs a high-speed data converter to capture this swath of desired and undesired channels in the digital domain and subsequently filters out the desired channels."

'362 Patent (EX1001), 1:24-34.

52. The '362 Patent notes that "channel frequencies may not be adjacent to each other" and as a result "the receiver system may have to concurrently receive several desired channels that may or may not be contiguous." '362 Patent (EX1001), 1:35-41. Thus, the "wideband receiver requirement poses a trade-off to the system to limit either the dynamic range of the wideband tuner or reduce the bandwidth covered by the tuner so that fewer channels may be received and processed by the demodulator." '362 Patent (EX1001), 1:41-45. The '362 Patent then goes through an example of a "conventional wideband tuner" which it alleges requires "very

expensive digital processing circuitry" and thus, the '362 Patent states it is "desirable to have wideband receiver systems that can increase the dynamic range without requiring expensive data conversion, filtering and channel selection at the demodulator." '362 Patent (EX1001), 1:46-2:27.

53. Figure 2 of the '362 Patent provides a "wideband receiver system 200 according to an embodiment of the present invention."

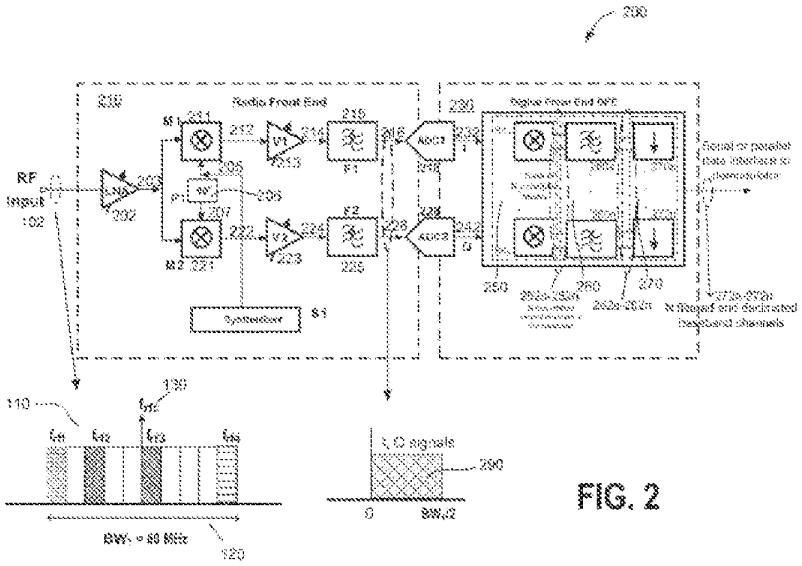


FIG. 2

54. In describing Figure 2, and with reference to the components and steps recited in the claims analyzed below, the '362 Patent explains the components of its system. For example, with respect to the claimed "wideband receiver system," the '362 Patent explains: "Wideband receiver system 200 includes a radio front end 210 and a digital front end 230. Radio front end 210 may be a single very wide-band tuner receiver that captures the desired swath of channels located in non-contiguous

portions of the spectrum having a frequency bandwidth BW1 120. In this example, the number of available channels in BW1 120 is assumed to be 10 with each channel occupying an 8 MHz bandwidth for a total of 80 MHz." '362 Patent (EX1001), 4:16-39.

55. The challenged claims also recite a "mixer module" and "downconverting, by a mixer module," which is explained in part by the '362 Patent as follows: "Mixers M1 211 and M2 221 may be conventional mixers formed using, for example, differential Gilbert cells. Each of the mixers 211 and 221 multiplies (mixes) an amplified RF signal 203 with a respective first oscillator frequency signal 205 and a second oscillator frequency signal 207 to generate an in-phase signal 212 and a quadrature signal 222 that have a phase shift of 90° degree between them." '362 Patent (EX1001), 4:40-5:12.

56. The challenged claims also recite "digitizing" which is described in part as follows: "Analog-to-digital converters ADC1 218 and ADC2 228 are high-speed (i.e., high sampling rate) converters to maximize the dynamic range. In an exemplary application, radio front end 210 operates as a nominal zero-IF down-mixer so that signals 216 and 226 have a nominal bandwidth 290 equal to one half of the RF signal bandwidth BW1 thanks to the complex down-mixer architecture. In other embodiment, radio front end 210 operates as a low-IF down-mixer so that the nominal bandwidth 290 of signals 216 and 226 is greater than one half of the

bandwidth BW1." '362 Patent (EX1001), 5:13-27.

57. Finally, the challenged claims recite "selecting" channels and "outputting" channels, which is described in part as follows: "ADC1 218 generates a digital signal I 232 that is a digital representation of the analog filtered signal 216; ADC2 228 generates a digital signal Q 242 that is a digital representation of the analog filtered signal 226." '362 Patent (EX1001), 5:28-48. Additionally: "Each of the N complex mixers 250 receives the digital signals I 232 and Q 242 from ADCs 218 and 228 to extract a different one of the desired channels and frequency-shifts the extracted signals to the baseband frequency." '362 Patent (EX1001), 5:49-61.

58. However, similar architectures and methods were known prior to the '362 Patent. For example, the Background section of the '362 Patent acknowledges that components such as mixers, analog-to-digital converters, and demodulators, were known prior to the '362 Patent. '362 Patent (EX1001), 1:24-2:23. Prior art references confirmed that these concepts were known. For example, prior to the '362 Patent's priority date, McNeely disclosed a "method and apparatus … for simultaneous reception of a plurality of digital RF channels." McNeely (EX1004), Abstract. Pugel similarly disclosed a "desire to have a solution providing receiving and re-synthesizing of channels for distribution in a more optimal manner" and thus described a method and system for receiving signals "containing a plurality of channels" and "selecting channels from the plurality of channels" for transmission

and output. Pugel (EX1003), 3:15–31.

59. Thus, the challenged claims recite nothing more than concepts and elements that were well-known prior to the '362 Patent.

C. Prior Art References

i. Overview of McNeely

60. McNeely describes an "apparatus and method for performing frequency translation." McNeely (EX1003), Abstract. McNeely's apparatus includes a "receiver … for receiving and digitizing a plurality of first signals" and "recovering a set of selected channels from the plurality of first signals." *Id.* McNeely also describes "combining the set of selected channels to form a second signal and transmitting the second signal." *Id.* at 3:27–31.

61. In my opinion, McNeely is analogous art to the '362 Patent. The field of endeavor of the '362 Patent is "wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum." '362 Patent (EX1001), 1:15–18. McNeely discloses a receiver and techniques applicable to signals occupying "1 GHz of bandwidth" (McNeely (EX1003), 7:9–11)[1] and is thus within the field of

[1] The '362 Patent explains that a tuner, or receiver, designed to "concurrently receive several TV channels" is referred to as wideband (1:24–27), and it provides an example of a wideband receiver system having a "single very wide-band tuner" that receives signals having "80 MHz" of bandwidth (4:16–25). Because McNeely's

endeavor of the '362 Patent.

62. McNeely is also reasonably pertinent to at least one problem addressed by the '362 Patent. The '362 Patent states it is "desirable to have wideband receiver systems that can increase the dynamic range without requiring expensive data conversion, filtering and channel selection at the demodulator." That is, the '362 Patent seeks to perform conversion, filtering, and channel selection from signals before those signals reach a demodulator. McNeely similarly discloses techniques of conversion, filtering and channel selection, and combined with the teachings of Pugel below, performs these functions on signals before those signals reach a demodulator.

ii. Overview of Pugel

63. Pugel relates to "multi-channel television reception." Pugel (EX1004), ¶ 1. Pugel notes a "need for a digital television receiver capable of simultaneously receiving a plurality of channels." *Id.* at ¶ 8. Pugel describes a "method and apparatus … for simultaneous reception of a plurality of digital RF channels." Pugel (EX1004), Abstract. Pugel's method includes "receiving at least one multichannel RF input signal" and separating the RF input signal. Pugel (EX1004), ¶ 11.

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receiver techniques are applicable to signals occupying 1 GHz of bandwidth (which is greater than the '362 Patent's example bandwidth), it too describes a wideband receiver.

Subsequently, the analog signals are converted into "digital signals" and then demultiplexed "to recover the plurality of digital RF channels." *Id.* Pugel's method also includes "demodulating the plurality of digital RF channels." *Id.* at ¶ 12.

64. In my opinion, Pugel is analogous art to the '362 Patent. The field of endeavor of the '362 Patent is "wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum." '362 Patent (EX1001), 1:15–18. Pugel discloses techniques applicable to "analog signals of differing frequency ranges" and is thus within the field of endeavor of the '362 Patent.[2]

65. Pugel is also reasonably pertinent to at least one problem addressed by the '362 Patent. The '362 Patent states it is "desirable to have wideband receiver systems that can increase the dynamic range without requiring expensive data conversion, filtering and channel selection at the demodulator." As detailed above, the '362 Patent seeks to perform conversion, filtering, and channel selection on received signals before those signals reach a demodulator. Pugel discloses techniques of conversion, filtering and channel selection before signals reach a

[2] As detailed above, the '362 Patent provides an example of a wideband receiver system having a "single very wide-band tuner" that receives signals having "80 MHz" of bandwidth (4:16–25). Pugel's receiver techniques, in one example, apply to signals having 300 MHz of bandwidth, (which is greater than the '362 Patent's example bandwidth), and thus it too describes a wideband receiver.

demodulator. Accordingly, Pugel is analogous art to the '362 Patent for this reason as well.

iii. Overview of Gomez

66. Gomez describes a "frequency translation module for a broadband multi-channel communication system." As pertinent to the analysis in this Request, Gomez's frequency translation module (FTM) 100 includes a "tuner 201" which includes an "amplifier 300" and "mixers 301 and 303." Gomez (EX1005), 4:4–6. The mixer 301 may perform down conversion on a signal. *See id.* at 4:4–19.

67. In my opinion, Gomez is analogous art to the '362 Patent. The field of endeavor of the '362 Patent is "wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum." '362 Patent (EX1001), 1:15–18. Gomez similarly describes applicability to "a broadband multi-channel communication system" and is thus within the field of endeavor of the '362 Patent. For example, just as the '362 Patent discusses that wideband receivers receive multiple channels, Gomez also discloses its receivers may "receive a signal" including a "set of high-definition channels." Gomez (EX1005), 3:40–50.

68. Gomez is also reasonably pertinent to at least one problem addressed by the '362 Patent. One problem addressed by the '362 Patent is the need for "expensive digital processing circuitry" and Gomez likewise addresses the issue of

frequency translation modules being too "costly … for some applications." Gomez (EX1005), 1:49–52. Accordingly, Gomez is analogous art to the '362 Patent for this reason as well.

D. Disclosure and Teachings of Prior Art References

i. Obviousness of Claims 1 and 11 by McNeely and Pugel

69. In my opinion, each and every limitation of claims 1 and 11 is rendered obvious by the combined teachings of McNeely and Pugel. The analysis below begins with independent claim 11 and then turns to independent claim 1.

Claim 11

[11.0] A method comprising: in a wideband receiver system

70. McNeely discloses or at least renders obvious a *method … in a wideband receiver system*.

71. McNeely discloses a *method*:

> "The disclosed embodiments relate to an apparatus and method for performing frequency translation."

McNeely (EX1003), Abstract.

72. The '362 Patent states: "Receivers used to down-convert and selectively filter TV channels are referred to as tuners, and **tuners designed to concurrently receive several TV channels are referred to as wideband tuners**." '362 Patent (EX1001), 1:24-27. Thus, a POSITA would have recognized a

wideband receiver system as one which concurrently receives several TV channels.

73. McNeely discloses such a system, as it states:

> "The present invention relates to an apparatus and method for performing frequency translation. The apparatus includes a receiver for receiving and digitizing a plurality of first signals, each signal containing channels and for simultaneously recovering a set of selected channels from the plurality of first signals."

McNeely (EX1003), 3:20–24.

> "The single L-band signal, as an analog input, is processed through an RF processing block 210. The RF processing block 210 may contain circuitry for filtering undesired energy outside the signal frequency range, may correct for any frequency response errors introduced, and may amplify the signal to a level necessary for input to the analog to digital (A/D) converter 220."

McNeely (EX1003), 9:7–12.

74. McNeely also states:

> "As previously described, each L-band signal may occupy 1 GHz of bandwidth, and a typical customer premises cable installation may only support less than 2 GHz of total signal bandwidth. The FTM 110 extracts certain ranges of frequencies containing selected physical channels as portions of the three L-band signals provided."

McNeely (EX1003), 7:9–15.

75. Because McNeely describes a receiver system that extracts certain

ranges of frequencies containing multiple physical channels, it discloses, or at least renders obvious, performing its methods *in a wideband receiver system* as recited.

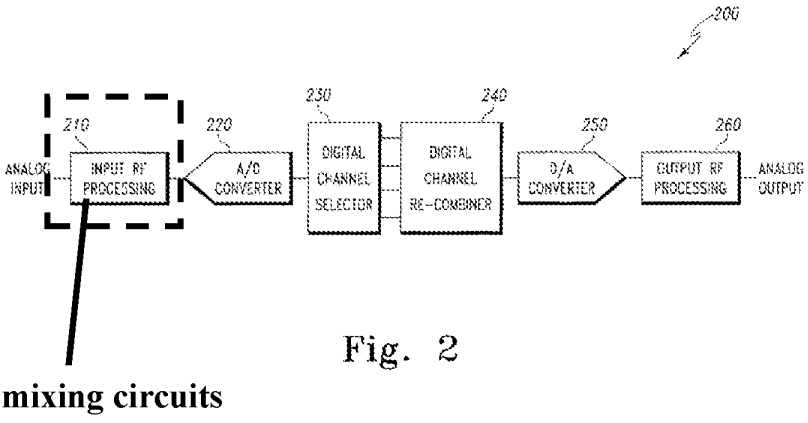
[11.1] downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

76. McNeely discloses, or at least renders obvious, this limitation.

77. First, McNeely discloses *a mixer module of said wideband receiver system*:

> "The input RF processing block 210 may also contain any **mixing circuits** necessary to position the L-band signal in the correct frequency range for operation of the A/D converter 220."

McNeely (EX1003), 9:12–15.



McNeely (EX1003), Fig. 2 (annotated)

78. Second, McNeely teaches *downconverting … a plurality of frequencies.* As detailed in the above disclosure, the mixing circuits "position the L-band signal"

(the analog input in Fig. 2) "in the correct frequency range." McNeely (EX1003), 9:12–15. In McNeely, "each L-band signal may occupy 1 GHz of bandwidth" (*id.*, 7:9–11) and thus, each signal comprises a *plurality of frequencies* as recited. Additionally, McNeely teaches that the "L-band signal" includes multiple "physical channels" (*id.*, 14:26–28) and thus, each L-band signal comprises *a plurality of frequencies* as recited.

79. McNeely's disclosure corresponds to, and teaches to a POSITA, *downconverting*, because a POSITA would have recognized that receivers use frequency translation techniques (like the technique disclosed in McNeely) to downconvert RF signals to a lower frequency. For example, the Tseng paper, which describes techniques in radio receivers, confirms that "one can use the bandpass sampling [5] instead to **directly downconvert the desired RF signal** from the RF to an intermediate frequency (IF)" which can "relax the demand for fast ADCs." Tseng (EX1011), p. 1. The Li paper states: "Downconversion mixer is one of the **important building blocks for RF transceivers** in wireless communications." Li (EX1012), p. 1. Li also depicts a "Direct downconversion transceiver." *Id.* at 2. Mirabbasi likewise states that "frequency downconversion" is "an essential operation in **any RF receiver**." Mirabbasi (EX1013), p. 133. The '362 Patent similarly acknowledges as background information: "Existing tuners for these applications **downconvert a swath of channels to an intermediate frequency**,

which are then sent to a demodulator." '362 Patent (EX1001), 1:27–29. Likewise, the Feng thesis, which discusses frequency translation, notes: "In modern communications, frequency translation is used in receivers to downconvert RF to a lower frequency…." Feng (EX1006), p. 19. The Tseng paper also states that downconverting a desired RF signal "can significantly relax the demand for fast ADCs." Tseng (EX1011), p. 1; see also Mirabbasi (EX1013), p. 136 (Figure 7 depicting downconversion before digitizing by an ADC). Consistent with the background knowledge of a POSITA, because McNeely also performs frequency positioning before digitizing by an analog-to-digital converter (ADC) as described below in limitation [11.2], a POSITA would have recognized McNeely to teach *downconverting* as recited.

80. Also, McNeely's disclosure is described in the context of a receiver, as detailed in the analysis of limitation [11.0] and thus, McNeely's description of "position[ing] the L-band signal in the correct frequency range" is a teaching of *downconverting … a plurality of frequencies* as recited.

81. Additionally, although McNeely later states that the digital channel selector 230 proceeds to "down-convert each of the individual physical channels that have been selected," a POSITA would have still understood that McNeely's discussion of "position[ing] the L-band signal in the correct frequency range for operation of the A/D converter" teaches *downconverting* as recited. This is because

the mixing circuits in McNeely downconvert **analog** RF signals so that they can be digitized by the A/D converter; for example, McNeely describes that the L-band signal input to the RF processing block 210 is in the 1-2 GHz frequency range (McNeely (EX1003), 7:26–28) but the A/D converter digitizes processed L-band signals in the 975-1425 MHz range (McNeely (EX1003), 9:16–19), indicating a repositioning to a lower frequency range, i.e., *downconverting*. Thus, the fact that later, **digitized** signals are also downconverted in McNeely, does not change that this disclosure of McNeely of repositioning by mixing circuits teaches *downconverting* as recited.

82. Third, McNeely teaches that the *plurality of frequencies … comprises a plurality of desired television channels and a plurality of undesired television channels*:

> "The apparatus includes a receiver for receiving and digitizing a plurality of first signals, each signal containing channels and for simultaneously **recovering a set of selected channels** from the plurality of first signals. The apparatus also includes a transmitter for combining the set of selected channels to produce a second signal."

McNeely (EX1003), Abstract.

83. McNeely also discloses:

> "A method (600) for providing frequency translation comprising: receiving (602) a first signal having a plurality of different frequency

channels;

selecting (606) a set of frequency channels from said plurality of different frequency channels;…"

McNeely (EX1003), 22:7–11 (claim 13).

84. Consistent with claim 13 and McNeely's disclosure, analog L-band signals ("a first signal having a plurality of different frequency channels") are received, processed, converted to digital, and then channel selection occurs in the digital channel selector 230 ("selecting (606) a set of frequency channels from said plurality of different frequency channels"). Thus, the received L-band signals (the received plurality of frequencies) includes the selected channels and the unselected channels (*the plurality of desired television channels and [] plurality of undesired television channels*).

85. Additionally, in McNeely, the "selected channels" are recovered by the digital channel selector 230 in Figure 2, which occurs after the downconversion of the received signals (the analog input) by mixing circuits in the input RF processing block 210; thus, the received signals (the *plurality of frequencies*) includes the selected channels and the unselected channels (the *plurality of desired television channels and [] plurality of undesired television channels*).

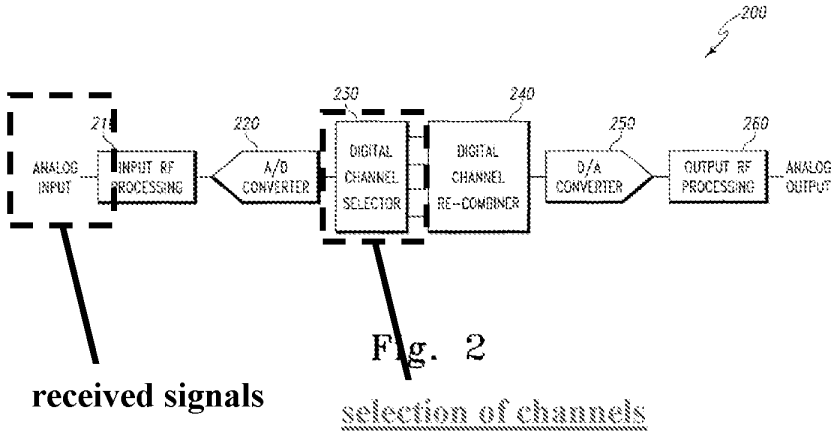


Fig. 2

McNeely (EX1003), Fig. 2 (annotated)

86. The "set of selected channels" corresponds to the recited *plurality of desired television channels*. Further, because McNeely's receiver recovers a set of selected channels from the first signals, the channels not recovered from the first signals would correspondingly be the *plurality of undesired television channels* as recited.

87. Thus, McNeely discloses, or at least renders obvious, this limitation.

[11.2] digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

88. McNeely discloses, or at least renders obvious, this limitation.

89. First, McNeely discloses *digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver* system:

"The A/D converter 220 **digitizes the processed L-band signal into a series of samples**, each sample containing a group of bits. In an exemplary embodiment, the processed satellite signal is located between the frequencies of 975 and 1425 MHz. The A/D converter 220 samples the processed L-band signal at a rate of 933 megasamples per second (MSPS) generating a digital signal containing a series of samples, each sample represented by 8 bits. The A/D converter 220 may also generate a translated frequency image of the L-band signal essentially translating the signal from an initial frequency range in the analog domain to a different frequency range based on sampling principles."

McNeely (EX1003), 9:16–26.

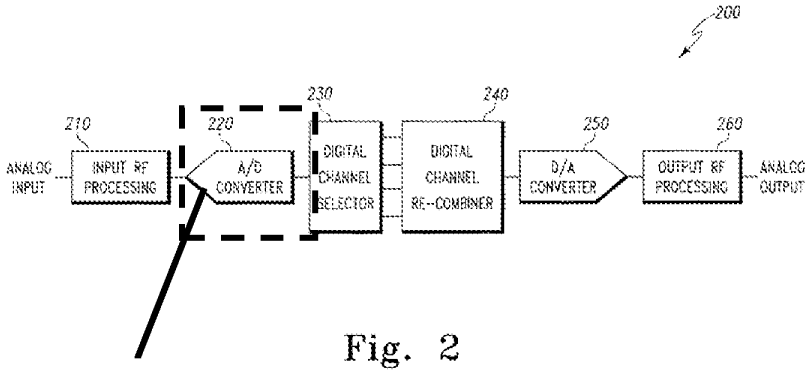


Fig. 2

McNeely (EX1003), Fig. 2

"Turning now to FIG. 2 a block diagram 200 of an embodiment of the present invention is shown. The diagram shows an implementation of the FTM 110 that includes digital signal processing in order to increase the performance and available bandwidth for selected channels."

McNeely (EX1003), 9:1–5.

90. Because McNeely's A/D converter operates on a processed L-band signal between the frequencies of 975 and 1425 MHz (i.e., 450 MHz of bandwidth), the A/D converter is a *wideband analog-to-digital converter (ADC) module* as recited, at least because the 450 MHz bandwidth in McNeely is greater than the example wideband receiver system with an analog-to-digital converter in the '362 which operates on a total of 80 MHz of bandwidth.

91. Second, because the A/D converter 220 in McNeely converts the signals from the input RF processing block 210, for the same reasons as set forth in limitation [11.1], McNeely discloses, or at least renders obvious, that the digitizing is performed on the *plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels* as recited.

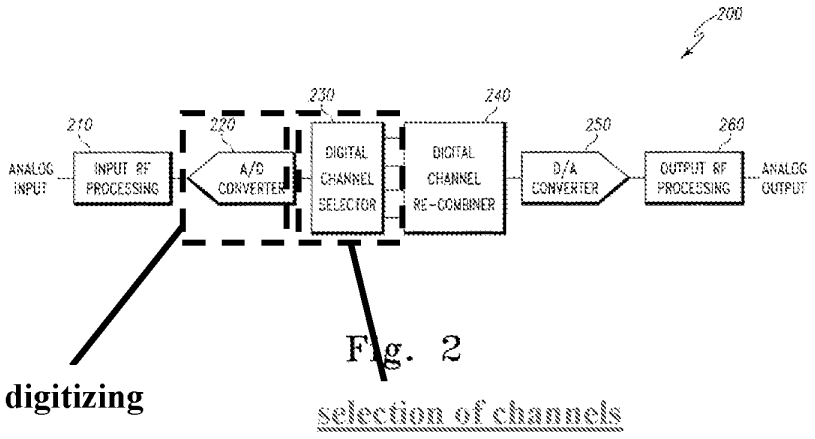


Fig. 2

McNeely (EX1003), Fig. 2 (annotated)

92. Specifically, as detailed in the analysis of limitation [11.1], *supra*, in McNeely, the "selected channels" are recovered by the digital channel selector 230 in Figure 2, which occurs after the downconversion of the received signals by mixing circuits in the input RF processing block 210 and digitizing by A/D converter 220 thus, the digitized signals (the *plurality of frequencies*) includes the selected channels and the unselected channels (the *plurality of desired television channels and [] plurality of undesired television channels*).

93. Thus, McNeely discloses, or at least renders obvious, this limitation.

[11.3] selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and

94. McNeely discloses, or at least renders obvious, this limitation:

> "The A/D converter 220 **digitizes the processed L-band signal into a series of samples**, each sample containing a group of bits.

McNeely (EX1003), 9:16–26.

95. As detailed above in the analysis of limitation [11.2], the L-band signal comprises the *plurality of desired television channels*. After digitizing the L-band signal into the samples, McNeely discloses:

> "The **digital channel selector 230** receives the sampled [L-band] signal and **proceeds to select** and down-convert **each of the individual physical channels that have been selected**. After processing, each of the selected individual channels are located within the same frequency range at or near to baseband, but are contained as individual signals on

separate signal lines. The number of bits representing each selected individual channel may be different from the original sampled signal based on the processing method employed. The use of digital signal processing and processing of the signal in parallel permits narrower filtering constraints and more efficient channel selection within the FTM 110."

McNeely (EX1003), 10:1–11.

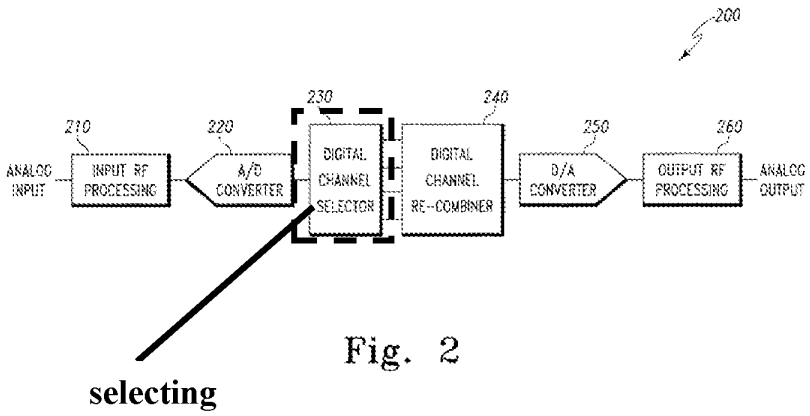


Fig. 2

McNeely (EX1003), Fig. 2 (annotated)

96. McNeely also discloses:

"7. The apparatus (500) of claim 1, wherein said receiver (530a-c) further comprises a selector (360) operatively connected to said distributor (350) for selecting said plurality of selected channels."

McNeely (EX1003), claim 7.

"13. A method (600) for providing frequency translation comprising:… selecting (606).a set of frequency channels from said plurality of

different frequency channels;"

McNeely (EX1003), claim 13.

"22. An apparatus (500) for frequency translation comprising….

means for selecting (530a-c) a set of channels from said set of signals;"

McNeely (EX1003), claim 22.

97. Because McNeely discloses selecting each of the individual physical channels that have been selected by the digital channel selector, which is *digital circuitry*, it discloses, or at least renders obvious, *selecting, by digital circuitry of said wideband receiver system* (e.g., digital channel selector 230), *said plurality of television channels from said digitized plurality of frequencies* (the individual physical channels that have been selected).

[11.4] outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.

98. McNeely and Pugel render obvious this limitation.

99. First, McNeely discloses *outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels … as a digital datastream*:

> "Each of the individual selected channels is provided to the digital channel re-combiner 240. The digital channel re-combiner 240 frequency translates the individual selected channels each to a different and separate frequency range and combines these signals together to form **a single selected digital signal**."

McNeely (EX1003), 10:12–16.

100. The output of "digital channel re-combiner 240" (i.e., the "single selected digital signal") is *a digital datastream* because, as shown in Figure 2, the output is transmitted (in McNeely) to the D/A converter (digital-to-analog converter), and thus, a POSITA would have recognized the output as being a *digital datastream* as recited.

101. In McNeely, the "selected digital signal" is supplied to the digital to analog (D/A) converter 250. However, it was known at the time of the '362 Patent that such digital signals could, and would be provided *to a demodulator* as recited.

102. Specifically, Pugel teaches "demodulating the plurality of digital RF channels" in a system which "permits substantially simultaneous reception of a plurality of digital cable television channels within a single digital receiver circuit." Pugel (EX1004), ¶¶ 11–12.

103. Pugel also discloses:

> "The converted digital signals are coupled to the digital tuner 130, which demultiplexes the converted digital signals to generate a plurality of digital channel signals. **Each digital channel signal is then coupled to a separate demodulator 141, 142, 143**, which performs demodulation and forward-error-correction (FEC) operations appropriate for the content of that digital channel."

Pugel (EX1004), ¶ 27.

104. Thus, Pugel teaches *outputting … to a demodulator* as recited. The combined teachings of McNeely and Pugel therefore render obvious this limitation.

105. A POSITA would have been motivated to combine the teachings of McNeely and Pugel.

106. First, McNeely acknowledges that demodulators were known:

> "Likewise, other than the inventive concept, transmission concepts such as satellite transponders, down-link signals, eight-level vestigial sideband (8-VSB), Quadrature Amplitude Modulation (QAM), and receiver components such as a radio-frequency (RF) front-end, or receiver section, such as a low noise block, tuners, and **demodulators** is assumed."

McNeely (EX1003), 5:16–21.

> "At each installation location in the premises 120, the selected signal is provided to a standalone terminal 130 or to a combination settop box 140a-c and display device 150a-c. The terminal 130 and settop box 140a-c operate in a similar manner. Each of them receive the selected signal, tune to the desired physical channel within the selected signal, **demodulate the physical channel to produce a transport stream**, and extract the desired bit stream(s) from the transport stream."

McNeely (EX1003), 8:1–7.

107. The '362 Patent confirms demodulators were known, as it discloses in the Background:

> "Existing tuners for these applications down convert a swath of

> channels to an intermediate frequency, which are then sent to a demodulator. Because the swath of channels is not contiguous, this swath includes the desired channels as well as undesired channels. The demodulator employs a high-speed data converter to capture this swath of desired and undesired channels in the digital domain and subsequently filters out the desired channels."

'362 Patent (EX1001), 5:27-34.

108. Given this knowledge in the art, a POSITA would have been motivated to combine the teachings of McNeely with Pugel as doing so would have been no more than the combination of known prior art elements. McNeely and Pugel disclose each and every limitation of the claims, albeit not within one reference. A POSITA could have, and would have been motivated to combine the teachings of McNeely with those of Pugel to provide for display of the selected TV channels on a display device (e.g., display device 150a-c in McNeely). In combination, each element performs the same function as previously: McNeely's apparatus downconverts, digitizes, and selects channels, and Pugel provides a demodulator that demodulates the channels for display. Additionally, the results of the combination would have been predictable, as McNeely acknowledges that demodulation was known in the context of its methods. Thus, a POSITA would have combined the teachings of McNeely and Pugel to render obvious this limitation.

109. Additionally, a POSITA would have been motivated to combine the

teachings of McNeely with Pugel as doing so would have been nothing more than the substitution of one known element for another to obtain predictable results. Specifically, combining the references would have involved no more than substituting McNeely's D/A converter and output RF processing with Pugel's demodulator teachings. As detailed above, demodulators were well-known at the time of the '362 Patent, as Pugel discloses and as the '362 Patent itself admits. A POSITA would have found it straightforward to replace McNeely's components with Pugel's demodulator, and the results of such a substitution would have been predictable, as Pugel's demodulator would perform the same function in the combination as it did previously alone. Thus, a POSITA would have combined the teachings of McNeely and Pugel to render obvious this limitation.

Claim 1

[1.0] A wideband receiver system comprising:

110. *See* analysis of limitation [11.0], *supra*.

[1.1] a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

111. *See* analysis of limitation [11.1], *supra*.

[1.2] a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels:

112. *See* analysis of limitation [11.2], *supra*.

[1.3] digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and

113. *See* analysis of limitation [11.3], *supra*.

[1.4] digital circuitry configured to:]… output said selected plurality of television channels to a demodulator as a digital datastream.

114. *See* analysis of limitation [1.4], *supra*.

ii. Obviousness of Claims 1 and 11 by Pugel and Gomez

115. In my opinion, each and every limitation of claims 1 and 11 is rendered obvious by the combined teachings of Pugel and Gomez. The analysis below begins with independent claim 11 and then continues to independent claim 1.

Claim 11

[11.0] A method comprising: in a wideband receiver system

116. Pugel discloses or at least renders obvious a *method … in a wideband receiver system*.

117. First, Pugel discloses a *method*:

"A **method** (400) processing signals comprising the steps of:"

Pugel (EX1004), claim 18.

118. Second, Pugel discloses a method *in a wideband receiver system*.

119. The '362 Patent states: "Receivers used to down-convert and selectively filter TV channels are referred to as tuners, and **tuners designed to concurrently receive several TV channels are referred to as wideband tuners**."

'362 Patent (EX1001), 1:24-27. Thus, a POSITA would have recognized a *wideband receiver system* as one which concurrently receives several TV channels.

120. Pugel discloses such a system, as it states:

> "An apparatus (100), comprising:
> first means for processing (111) an input signal comprising **signals in a first frequency band and signals in a second frequency band** to produce a first analog signal including signals in the first frequency band and substantially excluding the signals in the second frequency band;
> second means for processing (112) the input signal comprising signals in a first frequency band and signals in a second frequency band to produce a second analog signal including signals in the second frequency band and substantially excluding the signals in the first frequency band;"

Pugel (EX1004), claim 1.

121. Pugel also states:

> "The apparatus (100) of claim 1 **wherein said apparatus (100) processes frequencies between about 5 MHz and about 900 MHz**."

Pugel (EX1004), claim 16.

> "A method and apparatus is presented for simultaneous reception of a plurality of digital RF channels. Specifically, N amplifier-filter circuits (111, 112, 113) are configured to receive and separate a multichannel analog RF input signal into N analog signals, each including a different frequency band."

Pugel (EX1004), Abstract.

> "In operation, according to one embodiment, a multichannel analog RF input signal received at input coupler 101 is split into a plurality of substantially identical signals at splitter 102. Splitter 102 may include one or more amplifiers, filters, or other components (not shown) which reduce or overcome insertion loss or other adverse effects of the split, as should be apparent to one of ordinary skill in the art. The plurality of amplifier-filter circuits 111, 112, 113 then segregates the multichannel analog input signal into a plurality of separate analog signals of differing frequency ranges, or 'bands.' Each separate analog signal is then converted from analog to digital form in an analog-to-digital converter 121, 122, 123."

Pugel (EX1004), ¶ 24.

> "Each of the plurality of amplifier-filter banks or circuits 111, 112, 113 is configured to process frequencies within a specified band. For example, a first amplifier-filter circuit 111 may be configured to process frequencies from about 5 MHz to about 300 MHz, a second amplifier-filter circuit 112 may be configured for frequencies between about 300 MHz and about 600 MHz, and a third amplifier-filter circuit 113 may be configured for frequencies from about 600 MHz to about 900 MHz. In such an example, the present invention may be used to recover a plurality of digital cable television channels from a multichannel analog RF input signal which includes frequencies ranging from about 5 MHz to about 900 MHz."

Pugel (EX1004), ¶ 28.

122. Thus, because Pugel discloses an apparatus which processes frequencies in the range between 5 MHz and 900 MHz, it discloses, or at least renders obvious, performing its methods *in a wideband receiver system* as recited.

[11.1] downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

123. Pugel and Gomez render obvious this limitation.

124. First, Pugel discloses *downconverting ... a plurality of frequencies*. Pugel explains first that analog signals are converted to digital:

> "In operation, according to one embodiment, a multichannel analog RF input signal received at input coupler 101 is split into a plurality of substantially identical signals at splitter 102. Splitter 102 may include one or more amplifiers, filters, or other components (not shown) which reduce or overcome insertion loss or other adverse effects of the split, as should be apparent to one of ordinary skill in the art. The plurality of amplifier-filter circuits 111, 112, 113 then segregates the multichannel analog input signal into a **plurality of separate analog signals of differing frequency ranges**, or 'bands.' **Each separate analog signal is then converted from analog to digital form in an analog-to-digital converter 121, 122, 123**."

Pugel (EX1004), ¶ 24.

125. After the analog frequencies are converted to digital, Pugel teaches *downconverting* the *plurality of frequencies*:

"A method (400) processing signals comprising the steps of:

(a) separating an input signal into a first analog signal and a second analog signal;

(b) digitizing said first analog signal to generate a first digital signal;

(c) digitizing said second analog signal to generate a second digital signal;

(d) **downconverting** said first digital signal and said second signal; and

(e) extracting desired television program information from said downconverted first digital signal and said second digital signal."

Pugel (EX1004), claim 18.

126. As detailed above in the Claim Construction section, the *downconverting* step may be performed prior to the *digitizing* step, as these two steps need not be performed in any specific order. EX1007, pp. 51–52.

127. Pugel further states that "the digital tuner 130 may also perform a variety of other processing operations prior to providing digital channel signals suitable for use in each of the demodulation circuits 141, 142, 143" and that the digital tuner "may include a multitude of components configured as is well known in the art to recover a plurality of digital channel signals substantially simultaneously." Pugel (EX1004), ¶ 37.

128. A POSITA would have recognized that such components used to recover a plurality of digital channel signals would include components to perform *downconverting*, as it was well-known prior to the '362 Patent to perform *downconverting* on signals. For example, as acknowledged by the '362 Patent and

numerous contemporaneous references, such as Tseng, Li, Mirabbasi, and Feng, *downconverting* was well-known by POSITAs at the time of the '362 Patent.

129. However, Pugel does not explicitly disclose that the downconverting is performed *by a mixer module of said wideband receiver system*. This was a known implementation detail at the time of the '362 Patent. For example, in the same field, Gomez describes:

> "Tuner 201 performs a dual frequency conversion to select and down-convert a desired or selected channel from a RF input signal 101. In doing so, amplifer 300 receives and amplifes RF input signal 101, which contains a plurality of television channels. Mixer 301 receives RF input signal 101 from amplifier 300 and also receives a local oscillator (LO) signal from PLL 304. For direct conversion, the frequency of PLL 304 is tuned to the frequency of the desired channel in RF input signal 101 so that it is down-converted to baseband, for further processing. For example, if the desired channel in RF input signal 101 is at 100 MHZ, then PLL 304 is tuned to 100 MHZ, so that **mixer 301 down-converts the desired channel in RF signal** 101 to DC."

Gomez (EX1005), 4:6–19.

130. Thus, Gomez teaches downconverting *by a mixer module*.

131. A POSITA would have been motivated to combine the teachings of Gomez with Pugel, because doing so would have been nothing more than the use of a known technique to improve a similar device in the same way.

132. Pugel teaches that downconverting is performed, but it does not describe the circuitry for doing so. The '362 Patent Background acknowledges that "[e]xisting tuners … down-convert a swath of channels to an intermediate frequency." '362 Patent (EX1001), 1:27–29. The '362 Patent also acknowledges as prior art a "mixer" which "frequency down-converts the received RF input signal to a more convenient intermediate frequency (IF) band." *Id.* at 1:58–62. Thus, it was known to perform *downconverting* using a *mixer module*.

133. Gomez explicitly teaches the circuitry (i.e., a mixer) to perform the known technique of downconversion. A POSITA would have been motivated to apply this teaching in Gomez of downconversion by a mixer module to the teachings of Pugel to provide the hardware necessary to perform Pugel's downconversion.[3] The results would have been predictable to a POSITA, as the results would have simply represented Gomez's mixer module performing downconversion in the context of Pugel's system that also performs downconversion. Accordingly, a POSITA would have been motivated to combine the teachings for at least this reason.

[3] To the extent the *downconverting* limitation is not disclosed, or rendered obvious by Pugel alone, Gomez (and numerous other cited references) disclose a mixer module that downconverts an RF signal to a lower intermediate frequency that is more compatible with the Pugel A/D converters. It would have been obvious to a POSITA to combine the specific RF downconverting mixer module of Gomez with the Pugel system (in one example) by placing the Gomez downconverter in front of the Pugel 101 RF input and 102 splitter.

134. Likewise, combining the teachings of Gomez and Pugel would have been nothing more than combining prior art elements according to known methods to yield predictable results. Together, Pugel and Gomez include each element claimed, with the only difference being the lack of actual combination in a single prior art reference. A POSITA would have been motivated to, and would have been capable of, combining Gomez's teachings of downconversion by a mixer module with Pugel's teachings of downconversion, and in combination, each element performs the same function as it does separately. A POSITA would have further recognized the predictability of the combination, as the combination simply adds to Pugel appropriate circuitry for performing the functions disclosed in Pugel. Accordingly, a POSITA would have been motivated to combine the teachings for this additional reason as well.

135. Pugel explains that the *plurality of frequencies … comprises a plurality of desired television channels and a plurality of undesired television channels*:

> "The digital tuner 130 may include a channel selector 315 to permit selection of one or more particular **digital channels desired to be recovered**. For example, a selected set of digital cable television channels may be communicated to the digital tuner 130 via the channel selector 315 corresponding to a plurality of pay-per-view selections desired by members of a household; the digital tuner 130 may demultiplex only the digital channel signals corresponding to those

digital cable television channels."

Pugel (EX1004), ¶ 38.

"It should be apparent that each digital RF channel signal may in turn carry or provide a plurality of data streams, e.g., audio, video, program information, or interactive content."

Pugel (EX1004) ¶ 45.

"FIG. 4 shows a flow diagram representation of a method of **receiving a plurality of digital RF channels** generally designated 400 in accordance with an aspect of the present invention….The method 400 begins at step 401 and proceeds to step 402 in which a multichannel analog RF input signal is separated into a plurality of analog signals including at least first and second analog signals.

In step 403, the first analog signal is converted into a first digital signal using a first analog-to-digital converter. In step 404, the second analog signal is converted into a second digital signal using a second analog-to-digital converter independently of the conversion performed in the first analog-to-digital converter. The first and second analog-to-digital converters may convert different frequency bands from analog to digital form, similar to analog-to-digital converters 121, 122, 123 described above with reference to FIGS. 1 and 2….

In step 405, the first digital signal (converted in the first analog-to-digital converter) and the second digital signal (converted in the second analog-to-digital converter) are demultiplexed to generate a plurality of digital RF channel signals including at least first and second digital RF channel signals."

Pugel (EX1004), ¶¶ 43–45.

136. Thus, in Pugel, the multichannel analog RF input signal includes all channels (desired and undesired), which signal is then digitized and downconverted (as detailed in Pugel's claim 18) in the process of recovering the digital channels desired to be recovered. Thus, the multichannel analog RF input signal, subsequently digitized, *comprises a plurality of desired television channels and a plurality of undesired television channels* as recited.

137. In particular, because Pugel teaches selection of "digital channels **desired** to be recovered," a POSITA would have recognized that the signal also includes digital channels **not desired** to be recovered. Accordingly, the plurality of frequencies that is subsequently digitized and downconverted *comprises a plurality of desired television channels and a plurality of undesired television channels* as recited.

138. Thus, the combined teachings of Pugel and Gomez render obvious this limitation.

[11.2] digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

139. Pugel discloses, or at least renders obvious, this limitation.

140. First, Pugel discloses *a wideband analog-to-digital converter (ADC) module of said wideband receiver* system:

"A plurality of **analog-to-digital converters** is provided, each respectively coupled to one of the plurality of amplifier-filter circuits, the plurality of analog-to-digital converters including at least a first analog-to-digital converter configured to receive the first analog signal and generate a first digital signal and a second analog-to-digital converter configured to receive the second analog signal and generate a second digital signal."

Pugel (EX1004), ¶ 9.

"In operation, according to one embodiment, a multichannel analog RF input signal received at input coupler 101 is split into a plurality of substantially identical signals at splitter 102. Splitter 102 may include one or more amplifiers, filters, or other components (not shown) which reduce or overcome insertion loss or other adverse effects of the split, as should be apparent to one of ordinary skill in the art. The plurality of amplifier-filter circuits 111, 112, 113 then segregates the multichannel analog input signal into a **plurality of separate analog signals of differing frequency ranges**, or 'bands.' **Each separate analog signal is then converted from analog to digital form in an analog-to-digital converter 121, 122, 123**."

Pugel (EX1004), ¶ 24.

"The plurality of amplifier-filter circuits 111, 112, 113 then segregates the multichannel analog input signal into a plurality of separate analog signals of differing frequency ranges, or 'bands.'"

Pugel (EX1004), ¶ 24.

"In one embodiment, each amplifier/filter bank has particular characteristics that permit the passage of a specific range of frequencies

> substantially independent of the frequency selection characteristics of the other amplifier/filter banks. For example, one filter might have a pass-band of about 5 to about 300 MHz, while another filter might have a pass band of about 300 to about 600 MHz."

Pugel (EX1004), ¶ 25.

> "a first analog-to-digital converter (121) for processing the first analog signal to produce a first digital signal representing the signals in the first frequency band;
> a second analog-to-digital converter (122) for processing the second analog signal to produce a second digital signal representing the signals in the second frequency band;"

Pugel (EX1004), claim 1.

141. Because Pugel's analog-to-digital converters operate on frequencies ranging, in one example, from 300 to 600 MHz, Pugel's analog-to-digital converters teach *digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system* as recited.

142. Second, Pugel discloses *digitizing ... said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels*:

> "A method (400) processing signals comprising the steps of:
> (a) separating an input signal into a first analog signal and a second analog signal;
> (b) **digitizing** said first analog signal to generate a first digital signal;

(c) **digitizing** said second analog signal to generate a second digital signal;

(d) downconverting said first digital signal and said second signal; and

(e) extracting desired television program information from said downconverted first digital signal and said second digital signal."

Pugel (EX1004), claim 18.

143. As detailed in the analysis of limitation [11.1], *supra*, the *plurality of frequencies* comprises *said plurality of desired television channels and said plurality of undesired television channels* as recited. Specifically, because the digitizing occurs before the step of extracting desired television programs (the *selecting* step detailed below), all channels comprised in the input signal, including *desired television channels* and *undesired television channels* are digitized as recited.

144. Thus, Pugel discloses, or at least renders obvious, this limitation.

[11.3] selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and

145. Pugel discloses, or at least renders obvious, this limitation, as it discloses extracting desired television programs from the downconverted frequencies.

146. Pugel discloses:

"The digital tuner 130 may include a **channel selector 315 to permit selection of one or more particular digital channels desired to be recovered**. For example, a selected set of digital cable television

channels may be communicated to the digital tuner 130 via the channel selector 315 corresponding to a plurality of pay-per-view selections desired by members of a household; the digital tuner 130 may demultiplex only the digital channel signals corresponding to those digital cable television channels. Alternatively, the digital tuner 130 may be configured to demultiplex and recover all of the available digital channel signals."

Pugel (EX1004), ¶ 38.

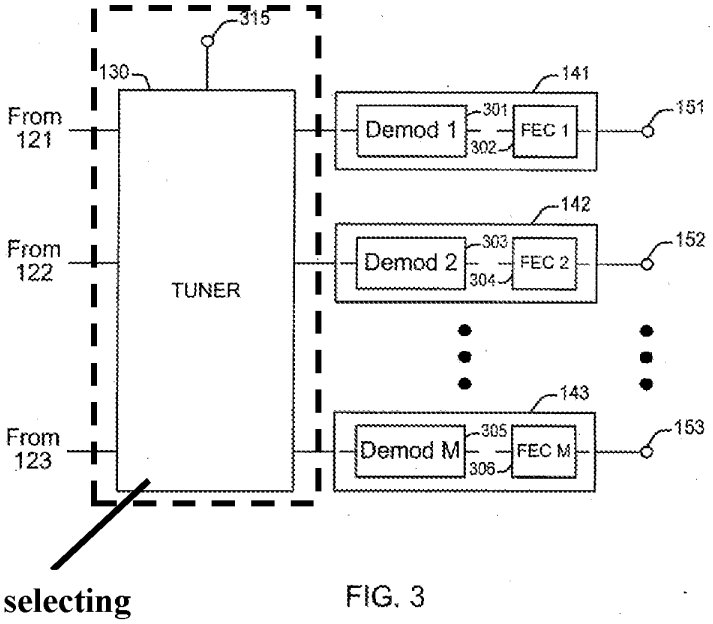


FIG. 3

Pugel (EX1004), Fig. 3 (annotated)

147. Pugel also refers to channel selection as "extracting," as it refers to this functionality in the claims as the tuner 130 (which includes channel selector 315) extracting desired information to be provided to demodulators (e.g., as shown in Fig.

3 above):

> "The apparatus (100) of claim 12 where said digital processor (130) multiplexes said first, second, and third digital signals, downconverts said multiplexed signal and **extracts desired information** to be coupled to said first and second demodulator circuits (141, 142)."

Pugel (EX1004), claim 14.

> "A method (400) processing signals comprising the steps of:
> (a) separating an input signal into a first analog signal and a second analog signal;
> (b) digitizing said first analog signal to generate a first digital signal;
> (c) digitizing said second analog signal to generate a second digital signal;
> (d) downconverting said first digital signal and said second signal; and
> **(e) extracting desired television program information** from said downconverted first digital signal and said second digital signal."

Pugel (EX1004), claim 18.

> "FIG. 4 shows a flow diagram representation of a method of **receiving a plurality of digital RF channels** generally designated 400 in accordance with an aspect of the present invention….The method 400 begins at step 401 and proceeds to step 402 in which a multichannel analog RF input signal is separated into a plurality of analog signals including at least first and second analog signals.
> In step 403, the first analog signal is converted into a first digital signal using a first analog-to-digital converter. In step 404, the second analog signal is converted into a second digital signal using a second analog-

> to-digital converter independently of the conversion performed in the first analog-to-digital converter. The first and second analog-to-digital converters may convert different frequency bands from analog to digital form, similar to analog-to-digital converters 121, 122, 123 described above with reference to FIGS. 1 and 2….
>
> In step 405, the first digital signal (converted in the first analog-to-digital converter) and the second digital signal (converted in the second analog-to-digital converter) are demultiplexed to generate a plurality of digital RF channel signals including at least first and second digital RF channel signals."

Pugel (EX1004), ¶¶ 43–45.

> "It should be apparent that **each digital RF channel** signal may in turn carry or provide a plurality of data streams, e.g., audio, video, **program information**, or interactive content."

Pugel (EX1004), ¶ 45.

> "A method and apparatus is presented for simultaneous **reception of a plurality of digital RF channels**….This combination of components permits substantially **simultaneous reception of multiple digital cable channels** within a single digital receiver circuit suitable for use with conventional cable delivery systems and at a reasonable cost."

Pugel (EX1004), Abstract

148. Because Pugel discloses extracting the desired television program information from the digital RF channels, and that the channel selector permits selection of digital RF channels desired to be recovered, Pugel discloses, or at least

renders obvious, *selecting, by digital circuitry of said wideband receiver system* (e.g., channel selector 315), *said plurality of television channels from said digitized plurality of frequencies* (the digital channels desired to be recovered).

[11.4] outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.

149. Pugel discloses, or at least renders obvious, this limitation.

150. Pugel discloses:

> "In operation, according to one embodiment, a multichannel analog RF input signal received at input coupler 101 is split into a plurality of substantially identical signals at splitter 102. Splitter 102 may include one or more amplifiers, filters, or other components (not shown) which reduce or overcome insertion loss or other adverse effects of the split, as should be apparent to one of ordinary skill in the art. The plurality of amplifier-filter circuits 111, 112, 113 then segregates the multichannel analog input signal into a plurality of separate analog signals of differing frequency ranges, or 'bands.' Each separate analog signal is then converted from analog to digital form in an analog-to-digital converter 121, 122, 123."

Pugel (EX1004), ¶ 24

> "The converted digital signals are coupled to the digital tuner 130, which demultiplexes the converted digital signals to generate a plurality of digital channel signals. **Each digital channel signal is then coupled to a separate demodulator 141, 142, 143**, which performs demodulation and forward-error-correction (FEC) operations

appropriate for the content of that digital channel."

Pugel (EX1004), ¶ 27.

> "In an alternate embodiment, in addition to the above a plurality of demodulator circuits is coupled to the digital tuner, the plurality of demodulator circuits including at least **a first demodulator circuit configured to receive and demodulate a first channel** of the plurality of digital RF channels and **a second demodulator circuit being configured to receive and demodulate a second channel** of the plurality of digital RF channels. The plurality of demodulator circuits includes circuitry configured for forward error correction."

Pugel (EX1004), ¶ 10; *see also* ¶¶ 38 ("a selected set of digital cable television channels may be communicated to the digital tuner 130 via the channel selector 315…the digital tuner 130 may demultiplex only the digital channel signals corresponding to those digital cable television channels."), 39 ("the digital tuner 130 may also perform a variety of other processing operations prior to providing digital channel signals suitable for use in each of the demodulation circuits 141 , 142, 143").

> "Each of the demodulation circuits 141, 142, 143 may include one or more demodulators 301, 303, 305 and forward-error-correction (FEC) circuitry 302, 304, 306, respectively."

Pugel (EX1004), ¶ 40.

151. Thus, Pugel teaches *outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream* as recited.

Claim 1

[1.0] A wideband receiver system comprising:

152. *See* analysis of limitation [11.0], *supra*.

[1.1] a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

153. *See* analysis of limitation [11.1], *supra*.

[1.2] a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels:

154. *See* analysis of limitation [11.2], *supra*.

[1.3] digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and

155. *See* analysis of limitation [11.3], *supra*.

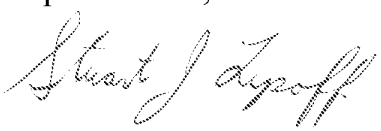
[1.4] digital circuitry configured to:]… output said selected plurality of television channels to a demodulator as a digital datastream.

156. *See* analysis of limitation [11.4], *supra*.

V. CONCLUSION

157. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: September 18, 2023

By: 

Stuart Lipoff

Appendix A

Stuart J. Lipoff

Mr. Lipoff is president of IP Action Partners Inc, a consulting practice in TIME (telecommunications, information technology, media, electronics, and ebusiness) industries and technologies. He draws upon his 30+ years of experience in a wide variety of technologies and industries to assist clients with knowledge based consulting services involving complex business decisions and problem resolution.

Mr. Lipoff was employed 25 years by Arthur D Little, Inc (ADL) as VP and Director of Communications, Information Technology, and Electronics (CIE); 4 years by Bell & Howell Communications Company as a Section Manager, and 3 years by Motorola's Communications Division as a Project Engineer. At ADL he was responsible for the firm's global CIE practice in laboratory based contract engineering, product development, and technology based consulting. At both Bell & Howell and Motorola, he had project design responsibility for wireless communications and paging products.

Stuart Lipoff has Bachelor's Degrees in Electrical Engineering and in Engineering Physics, both from Lehigh University. He also has received a Masters Degree in Electrical Engineering from Northeastern University, and a MBA degree from Suffolk University.

Mr. Lipoff is a fellow of the IEEE Consumer Electronics, Communications, Computer, Circuits, and Vehicular Technology groups. He is a member of the IEEE Consumer Electronics Society National Administration Committee, and was the Boston Chapter Chairman of the IEEE Vehicular Technology Society. He served as 1996-7 President of the IEEE Consumer Electronics Society and as Chairman of the Consumer Electronics Society Technical Activities and Standards Committee; served as VP of Publications for The IEEE Consumer Electronics Society; and currently serves as VP of Industry Activities and Standards. He has also chaired the search committee for Sony supported Mazura Ibuka Award in consumer electronics and is a current committee member. As Vice President and Standards Group Chairman of the Association of Computer Users, he served as the ACU representative to The ANSI X3 Standards group. For the Federal Communications Commission's Citizens advisory committee on CB radio (PURAC), he served as Chairman of the task group on user rule compliance. He has been elected to membership in the Society of Cable Television Engineers (SCTE), The Association of Computing Machinery (ACM) , and The Society of Motion Picture and Television Engineers (SMPTE).

Stuart Lipoff holds a FCC General Radiotelephone License and a Certificate in Data Processing (CDP) from the ACM supported Institute for the Certification of Computing Professionals (ICCP). He is a registered professional engineer (by examination) in The Commonwealth of Massachusetts.

Mr. Lipoff holds seven USA patents and has published articles in Electronics Design, Microwaves, EDN, The Proceedings of the Frequency Control Symposium, Optical Spectra, and numerous IEEE publications. He has presented papers at many IEEE and other meetings. In the fall of 2000, he served as general program chair for The IEEE Vehicular Technology Conference

on advanced wireless communications technology. He has organized sessions at The International Conference on Consumer Electronics and was the 1984 program chairman. He conducted an eight week IEEE sponsored short course on Fiber Optics Systems Design. In 1984, he was awarded IEEE's Centennial Medal and in 2000 IEEE's Millennium Metal.

He has served as a member of the USA advisory board to the National Science Museum of Israel and has presented a short course on international product development strategies as a faculty member of Technion Institute of Management in Israel. He also as a member of the board of directors of The Massachusetts Future Problem Solving Program.

Mr Lipoff is internationally recognized as an authority and opinion leader in new economy related businesses and technology. Citations supporting his recognition can be found on his web site at http://www.ipaction.com .

Some examples of projects he has performed in the cable TV and telecommunications sector include:

- For Next Generation Network Architecture llc (NGNA llc) consortium of Comcast, Cox, and Time-Warner; he managed the project that produced a five year planning horizon vision for the services and technology the cable industry will seek to deploy. The services and vision were then mapped to overall architectures impacting network elements in the back office, head-end, outside plant, and customer premises and documented in next generation network recommendations. The project involved coordination with over fifty senior technical staff in the three cable MSO sponsors as well as interactions with over 100 suppliers of systems, software, and products to the cable industry. The recommendations and findings were wide ranging including, for example: software defined downloadable conditional access (CA) systems, migration of the outside plant from low to mid split, bridging from network CA to in-home network digital rights management systems (DRM), and migration from 1way to 2way digital TV.

- For Chameleon Network Inc (CNI), a consumer electronic wallet startup, he served as CTO developing overall systems architecture, prototype development, and developing an intellectual property patent portfolio for which he a named inventor. The CNI system employed multilayer security and feature management controls that facilitated trusted interactions between end consumers, bank financial service providers, and merchants.

- For Comcast, he explored opportunities to acquire spectrum to launch an advanced high speed public network wireless system that is optimized to deliver multimedia content such as video and music entertainment in addition to competitive voice services. This project involved looking beyond today's evolutionary air interface road maps to new 4th and 5th generation air interface technologies.

- Leadership of the project for CableLabs that studied the technology and economics of wireless personal communications technology. This project is highlighted in the history of CableLabs in their website as one of the significant accomplishments of The Labs. The

project included the selection of CDMA technologies and the development of strategies to compete with incumbent cellular carriers. This effort led to the formation of a consortium between Sprint and the cable MSOs that has evolved into the present Sprint PCS business.

- Security audit, design review, and recommendations for product improvement of a new digital rights management (DRM) hardware/software module developed by DataPlay for deployment in mass market advanced optical media and for electronic music distribution via the internet including meeting with each of the major record labels to satisfy their concerns regarding security robustness and ability to support flexible business models for content and rights management.

- For a project jointly funded by the RIAA and IFPI, on behalf of the music industry, he performed a project to identify technology solutions and business models to protect the music content on CD-Audio media. The project involved coordination with a committee of each of the major content owners and record labels.

- On behalf of a leading law firm representing TV-Com International, he supported the client as a damages expert in patent litigation related to digital conditional access and encryption technology employed to protect video entertainment delivered over cable television networks. This project required the develop of sophisticated financial models which demonstrated the value of the patents by computing the impact the technology had on the overall enterprise value of the defendant.

- On behalf of a leading law firm representing IPPV Enterprises, he supported the client as damages expert in patent ligtigation related to secure key exchange and key management as employed by the defendant- Echostar. As above, this project required the development of sophisticated financial models which demonstrated the value of the patents by computing the impact the technology had on the overall enterprise value of the defendant

- Leadership of the project which developed the series of DOCSIS specifications for high speed residential cable modems. The scope of work included developing a roadmap and strategic framework for evolving the business from simple high speed internet services to multimedia broadband services combining voice, data, and secure electronic content delivery. This project was performed under contract to the MCNS consortium of cable TV operators representing 85% of the subscriber base in North America and has since been adopted by the United Nations as a global telecommunications standard.

- Under contract to The National Cable Telecommunications Association (NCTA), he represented the point of view of the cable industry in an FCC workshop on universal broadband availability. This project involved a presentation on the technical capabilities of the cable industry DOCSIS cablemodem infrastructure, a comparison of cablemodem services with DSL, fiber to home, and wireless broadband. Issues related to net neutrality were included in the discussion. Following the FCC workshop, I was further commissioned

by NCTA to prepare a white paper comparing DOCSIS cablemodem services with fiber to the home services such as FiOS.

- For The National Association of Broadcasters (NAB) he managed a project to engage NAB members in the development of new applications and services for over-the-air radio and television broadcasting. The project included developing a list and priority recommendations for research projects for consideration of funding by NAB which would explore the most promising candidate research projects.

- For the cable operator consortium SpectrumCo I am supporting exploration of alternative means to provide competitive public network wireless services to existing cable and new customers. The project involves exploring 3rd and 4th generation wireless air-interface technologies and developing models that integrate capital expenditures forecasts with operating profits to develop financial performance perspectives of alternatives. A unique aspect of this project includes developing technology forecasts and estimates of subscriber equipment capable of supporting video and multimedia content delivery to handsets.

- For COMCAST Cablevision of Philadelphia, I assisted in the development of a family of advanced two-way, residential digital services, including: development of system/service concepts and specification/selection of a range of equipment to provide this service. Detailed operating and balance sheet financial models of were developed to measure financial attractiveness of alternatives and use as a tool to select specific strategies.

- For a division of Westinghouse in cooperation with Kansai Electric (Japan), I developed detailed business plans for the launch of cable TV and associated broadband services. The project involved demand studies to assess adoption and desires of consumers followed by recommendations on marketing, operating, and technology strategies.

- For the Westinghouse Teleprompter Cable Company, I studied the market for a fiberoptic based institutional data network in Pittsburgh and developed the business and financial models to examine the financial attractiveness of offering these services.

- For Times Mirror Cable TV, I developed business plans for the upgrade of selected systems to 2way capability and exploration of alternative telephony and other advanced services to be provided. I worked with the client to develop risk/reward perspectives for specific service options and develop a roadmap in order of most attractive priorities.

- Analysis and recommendations in a study funded by CableLabs which led to today's hybrid-fiber coax architecture widely deployed worldwide for delivering broadband multimedia services to the home. The project involved developing forecasts of technology trends in parallel with projecting the business applications. Detailed proforma financial models were developed to make the cost/benefit of deploying this technology visible to the cable industry, and strategies were developed and recommended to the industry.

- On behalf of a leading law firm representing TV-Com International, he supported the client as a damages expert in patent litigation related to digital conditional access and encryption technology employed to protect video entertainment delivered over cable television networks. This project required the develop of sophisticated financial models which demonstrated the value of the patents by computing the impact the technology had on the overall enterprise value of the defendant.

- On behalf of a leading law firm representing IPPV Enterprises, he supported the client as damages expert in patent litigation related to secure key exchange and key management as employed by the defendant- Echostar. As above, this project required the develop of sophisticated financial models which demonstrated the value of the patents by computing the impact the technology had on the overall enterprise value of the defendant

- Leadership of a project jointly funded by The National Association of Broadcasters and Maximum Service TV Association to analyze options to accelerate the adoption of digital TV technology by consumers. His recommendations were provided to the FCC and were the basis for the August 2002 report and order the FCC issued to mandate a roll-out schedule for digital TV receivers.

- For Bell South I contributed to a major operations improvement project involving developing forecasts of the future competitive environment, customer needs, a strategy to compete, and new business models. These forecasts were then applied to develop business redesign recommendations and a list of new services offerings.

- For Magnavox Cable TV (a division of N.A. Philips) I performed comparative cost and technical analysis of fiber optics versus conventional coax systems. This analysis was followed by the development of strategies and sales support materials to pitch the new HFC systems to cable TV operators.

- I performed additional work for The Cable Television Laboratories in which I studied the application of remote and distributed antennas supporting microcellular PCS on hybrid fiber-coax cable TV systems. A key issue explored was the requirement for the fiber optic portion of the plant to carry the PCS carriers in analog form and deal with the wide dynamic range demands for inbound signals.

- For a consortium of the major cable TV operators consisting of Comcast, Time Warner, Cox, and Rogers; I developed models for prediction of reliability of alternative HFC architectures and their suitability to provide local exchange voice services competitive with ILECs. The project required understanding the reliability specifications employed in conventional local exchange carrier telephone plant and the contributions between hardware, power, and workmanship failures. Each of three alternative fiber optic architectures for cable delivered voice telephony were studied and modeled to develop reliability predictions and recommendations were made as to which aspects of the three alternatives were the best choice for cable delivered voice telephony.

- For GTE Systems I prepared a presentation on developing commercial opportunities for wide-bandwidth ATM switching. The scope of applications included: metro area network LAN interconnect, broadcast studio digital video routing and switching, and distributed switching for digital wireless personal communications networks. The goal of the project was to explore cable TV and other commercial applications for their military systems broadband switching technology.

- For Bellcore (now Telcordia division of SAIC), I evaluated the R&D portfolio of their Applied Research Group. The main components of this portfolio were DWDM technologies for long haul interLATA communications as well as optical multiplexing components for passive optical network applications in cable TV and advanced broadband residential services. I provided R&D planning assistance on the allocation of funding and priorities to the R&D efforts and identified opportunities for securing intellectual property rights to critical R&D efforts.

- For the ViaSat Division of Modern Times Group (Sweden) he developed business plans for the launch of a new service that bundled discounted long distance telephone services with direct to home satellite TV services and other interactive services including gambling via the set-top box.

- For Magnavox Cable TV, he supported the development of a set-top-box cable converter with a microcomputer based user interface and conditional access system. The product was sold in both the USA and Canada.

- For Southern New England Telephone (SNET), he supported the launch of a video dial tone service. He contribution to the project included engineering and cost analysis of system alternatives as well as assisting with the preparing of RFPs for set-top-boxes and other network elements.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
90/019,255	**09/20/2023 02:38:27 PM ET**	**50348.106**

Title of Invention

WIDEBAND TUNER ARCHITECTURE

Application Information

APPLICATION TYPE	Utility / ex parte reexam	PATENT #	9210362
CONFIRMATION #	5785	FILED BY	Krista Myrick
PATENT CENTER #	62831599	FILING DATE	-
CUSTOMER #	23446	FIRST NAMED INVENTOR	Madhukar Reddy
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Raghav Bajaj

Documents

TOTAL DOCUMENTS: 16

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
50348.106 Entropic 362 Request.pdf		56	-	515 KB
50348.106 Entropic 362 Request-RXOSUB.R.pdf	(1-55)	55	Receipt of Original Ex Parte Request by Third Party	502 KB
50348.106 Entropic 362 Request-RXC/SR.pdf	(56-56)	1	Reexam Certificate of Service	150 KB
50348-106 Reexamination Transmittal.pdf		4	Receipt of Original Ex Parte Request by Third Party	285 KB
50348.106- PTO 1449 modified form - Ex Parte Reexam Request.pdf		1	Reexam - Info Disclosure Statement Filed by 3rd Party	151 KB

50348.106 Unified Entropic 362 - Power of Attorney.pdf	1	Power of Attorney	114 KB
EX1001 US9210362.pdf	20	Copy of patent for which reexamination is requested	1365 KB
EX1002 23446_14614543.pdf	165	Reexam - Affidavit/Declaration/Exhibit Filed by 3rd Party	6383 KB
EX1003 WO2006119490A2.pdf	33	Reexam - Affidavit/Declaration/Exhibit Filed by 3rd Party	4312 KB
EX1004 WO2007145637 Pugel.pdf	24	Reexam - Affidavit/Declaration/Exhibit Filed by 3rd Party	2484 KB
EX1005 US-8224274-B2 [Gomez].pdf	28	Reexam - Affidavit/Declaration/Exhibit Filed by 3rd Party	1296 KB
EX1006 Feng 4406233.pdf	79	Reexam - Affidavit/Declaration/Exhibit Filed by 3rd Party	9605 KB
EX1007 2_22-cv-00125-JRG_123_PRIMARY DOCUMENT.pdf	65	Reexam - Affidavit/Declaration/Exhibit Filed by 3rd Party	482 KB
EX1008 Lipoff Declaration.pdf	75	Reexam - Affidavit/Declaration/Exhibit Filed by 3rd Party	806 KB
EX1011 ching-hsiangtseng2006.pdf	6	Reexam - Affidavit/Declaration/Exhibit Filed by 3rd Party	207 KB
EX1012 rf-cmos-mixer-design-and-optimization-for-	7	Reexam - Affidavit/Declaration/Exhibit	529 KB

wideband-cdma-applicat.pdf		Filed by 3rd Party	
EX1013 Mirabbasi.pdf	9	Reexam - Affidavit/Declaration/Exhibit Filed by 3rd Party	220 KB

Digest

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50348.106 Unified Entropic 362 - Power of Attorney.pdf	7705EBDB1C36DB08D43EE4805F4F1430BC8417D8A560FA2FCE985C1207110D4C008DC146A8E3D623ED97C5674113A39643687863083935CA5D33FF2DB38D16AF
EX1001 US9210362.pdf	010AC93152806AB9C9213085BDB0CEB8655B5E15B290F72FC2A7F67A74927F7E069731531211B1C255E9283E309EA30BEC57572F0483218F85C4623F698A7254

EX1002 23446_14614543.pdf	CF24C49CF49FF366B46DECBB797A36CAC74E006992800A324 A5634858ED427D70C37200A21A214E123F30CB91580964B1A8 36BC45587E7E56F4689713F960522
EX1003 WO2006119490A2.pdf	925C2C1DC320EB8201CC9A77F884DF2ECD829D89637FCB1E 84D0ABDD6CC404F20D7BCBA1C15FE02CD86D7C3A49136B0 FE9AA8DB26195A77FFBC2344850195B60
EX1004 WO2007145637 Pugel.pdf	A1E35C00C47722646719F13671FADE145F8FFA5B2353732634 5C114629BF78F2D325E522E19668B15F2C9BFDF2D7D37E51C 2C29109A896DF944931AB196AE876
EX1005 US-8224274-B2 [Gomez].pdf	B8DF28EF48B580CD745791F449E4CD6D7ECE3CEA6CDF7A48 BCD32B437392EEC88876DA19D98EDC071229B97963163A3E7 4B6BF37E49445F51F9C21B371F64248
EX1006 Feng 4406233.pdf	B39B4D13AC5E894267C2918193CFC04ECEE110D5EC9DEE23 4FECF83F7AD077E6973933C6A2542EFE190F48A05F63C54A0 C5E9F9CE2A9160EEF3ECFFBF2201970
EX1007 2_22-cv-00125-JRG_123_PRIMARY DOCUMENT.pdf	64D11D7777525826DC215FCF0C8BD7A5A7A5EDC2C1074E7D 8B6532BAA48A2FCC44C406A4B418C85D92D796ACB4F42417E 17A0CD3352B3967B47DF8C16126AA7F
EX1008 Lipoff Declaration.pdf	21DCCB1D2E436E2B9DC4DF938DC3BB8A8071BEC94544BCE C0CEEF8FBDC262D1D54F6227B92C00EE256D5E90273140CD BDDE026936621575493621 5AB6668A0BF
EX1011 ching-hsiangtseng2006.pdf	468242435B2FBB68AE1E9DACD6A21270C0FFC5EAFE40754A9 346B514DA08DCA80686B60F31C758778F39BC15AC50C1AC4A 7A6289BF6742A8658CAAAA546FE801
EX1012 rf-cmos-mixer-design-and-optimization-for-wideband-cdma-applicat.pdf	6E58E74DC2361E50C0B92AB88B548931D1B78F5A9D9D10B88 13CF26F5EAFCC3994FE9F72E95C7C1AE774CB1C735194EE68 48A17191ECDB555976ECBD120E5A1D
EX1013 Mirabbasi.pdf	7F5D55879E0B773D7E2499EFE92B733BD6E0525A29824252AD D048B0EB0B4E5C6EFEACD529C442776DF3147B8DAF85A812 D8FD7C9D5715833D7AA7AFD2E28459

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Patent Assignment Abstract of Title

Total Assignments: 5

Application #: 14614543 **Filing Dt:** 02/05/2015 **Patent #:** 9210362 **Issue Dt:** 12/08/2015
PCT #: NONE **Intl Reg #:** **Publication #:** US20150156535 **Pub Dt:** 06/04/2015
Inventors: Madhukar Reddy, Curtis Ling, Tim Gallagher
Title: WIDEBAND TUNER ARCHITECTURE

Assignment: 1

Reel/Frame:	Received:	Recorded:	Mailed:	Pages:
042453 / 0001	05/12/2017	05/12/2017	05/23/2017	104

Conveyance: SECURITY AGREEMENT

Assignors: MAXLINEAR, INC. **Exec Dt:** 05/12/2017
ENTROPIC COMMUNICATIONS, LLC (F/K/A ENTROPIC COMMUNICATIONS, INC.) **Exec Dt:** 05/12/2017
EXAR CORPORATION **Exec Dt:** 05/12/2017

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Assignment: 2

Reel/Frame:	Received:	Recorded:	Mailed:	Pages:
053115 / 0842	07/01/2020	07/01/2020	07/06/2020	101

Conveyance: SUCCESSION OF AGENCY (REEL 042453 / FRAME 0001)

Assignor: JPMORGAN CHASE BANK, N.A. **Exec Dt:** 07/01/2020

Assignee: MUFG UNION BANK, N.A.
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Correspondent: CT CORPORATION
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SUITE 125
COLUMBUS, OH 43219

Assignment: 3

Reel/Frame:	Received:	Recorded:	Mailed:	Pages:
055779 / 0001	03/31/2021	03/31/2021	04/01/2021	58

Conveyance: RELEASE BY SECURED PARTY (SEE DOCUMENT FOR DETAILS).

Assignor: MUFG UNION BANK, N.A. **Exec Dt:** 03/31/2021

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REEXAM CONTROL NUMBER	FILING OR 371 (c) DATE	PATENT NUMBER
90/019,255	09/20/2023	

CONFIRMATION NO. 5785
REEXAMINATION REQUEST NOTICE

Haynes and Boone, LLP
IP Section
2801 N. Harwood St.
Suite 2300
Dallas, TEXAS 75201

NOTICE OF REEXAMINATION REQUEST FILING DATE

(Third Party Requester)

Requester is hereby notified that the filing date of the request for reexamination is 09/20/2023, the date that the filing requirements of 37 CFR § 1.510 were received.

A decision on the request for reexamination will be mailed within three months from the filing date of the request for reexamination. (See 37 CFR 1.515(a)).

A copy of the Notice is being sent to the person identified by the requester as the patent owner. Further patent owner correspondence will be the latest attorney or agent of record in the patent file. (See 37 CFR 1.33). Any paper filed should include a reference to the present request for reexamination (by Reexamination Control Number).

cc: Patent Owner
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MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

/rbell/

Legal Instruments Examiner
Central Reexamination Unit 571-272-7705; FAX No. 571-273-9900

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REEXAM CONTROL NUMBER	FILING OR 371 (c) DATE	PATENT NUMBER
90/019,255	09/20/2023	

CONFIRMATION NO. 5785

REEXAM ASSIGNMENT NOTICE

23446
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SUITE 3400
CHICAGO, IL 60661

"OC00000006251 4604"

Date Mailed: 09/28/2023

NOTICE OF ASSIGNMENT OF REEXAMINATION REQUEST

The above-identified request for reexamination has been assigned to Art Unit 3992. All future correspondence to the proceeding should be identified by the control number listed above and directed to the assigned Art Unit.

A copy of this Notice is being sent to the latest attorney or agent of record in the patent file or to all owners of record. (See 37 CFR 1.33(c)). If the addressee is not, or does not represent, the current owner, he or she is required to forward all communications regarding this proceeding to the current owner(s). An attorney or agent receiving this communication who does not represent the current owner(s) may wish to seek to withdraw pursuant to 37 CFR 1.36 in order to avoid receiving future communications. If the address of the current owner(s) is unknown, this communication should be returned within the request to withdraw pursuant to Section 1.36.

NOTICE OF USPTO EX PARTE REEXAMINATION PATENT OWNER STATEMENT WAIVER PROGRAM

The USPTO has implemented a pilot program where, after a reexamination proceeding has been granted a filing date and before the examiner begins his or her review, the patent owner may orally waive the right to file a patent owner's statement. See *"Pilot Program for Waiver of Patent Owner's Statement in Ex Parte Reexamination Proceedings,"* 75 FR 47269 (August 5, 2010). One goal of the pilot program is to reduce the pendency of reexamination proceedings and improve the efficiency of the reexamination process.

Ordinarily when ex parte reexamination is ordered, the USPTO must wait until after the receipt of the patent owner's statement and the third party requester's reply, or after the expiration of the time period for filing the statement and reply (a period that can be as long as 5 to 6 months), before mailing a first determination of patentability. The USPTO's first determination of patentability is usually a first Office action on the merits or a Notice of Intent to Issue Reexamination Certificate (NIRC).

Under the pilot program, the patent owner's oral waiver allows the USPTO to act on the first determination of patentability immediately after determining that reexamination will be ordered, and in a suitable case issue the reexamination order and the first determination of patentability (which could be a NIRC if the claims under reexamination are confirmed) at the same time.

Benefits to the Patent Owner for participating in this pilot program include reduction in pendency.

To participate in this pilot program, Patent Owners may contact the USPTO's Central Reexamination Unit (CRU) at 571-272-7705. The USPTO will make the oral waiver of record in the reexamination file in an interview summary and a copy will be mailed to the patent owner and any third party requester.

cc: Third Party Requester(if any)
Haynes and Boone, LLP
IP Section
2801 N. Harwood St.
Suite 2300
Dallas, TEXAS 75201

/rbell/

Legal Instruments Examiner
Central Reexamination Unit 571-272-7705; FAX No. 571-273-9900

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Under Secretary of Commerce for Intellectual Property and
Director of the United States Patent and Trademark Office

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Kathi Vidal

Kathi Vidal
Under Secretary of Commerce for Intellectual Property and
Director of the United States Patent and Trademark Office

Derrick Brent
Deputy Under Secretary of Commerce for Intellectual Property and
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BIB DATA SHEET

CONFIRMATION NO. 5785

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
90/019,255	09/20/2023 RULE	455	3992	50348.106

APPLICANTS

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INVENTORS

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IP Section Haynes and Boone, LLP, Residence Not Provided;
CURTIS LING, CARLSBAD, CA;
TIM GALLAGHER, CARLSBAD, CA;

**** CONTINUING DATA ***************************

This application is a REX of 14/614,543 02/05/2015 PAT 9210362
which is a CON of 13/962,871 08/08/2013 PAT 9100622
which is a CON of 12/762,900 04/19/2010 PAT 8526898
which claims benefit of 61/170,526 04/17/2009

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

Foreign Priority claimed ❑ Yes ❑ No 35 USC 119(a-d) conditions met ❑ Yes ❑ No Verified and Acknowledged Examiner's Signature	❑ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
				20	2

ADDRESS

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500 WEST MADISON STREET
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UNITED STATES

TITLE

WIDEBAND TUNER ARCHITECTURE

FILING FEE RECEIVED		
0.00	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

BIB (Rev. 05/07).

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CONFIRMATION NO. 5785

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
90/019,255	09/20/2023 RULE	455	3992	50348.106

APPLICANTS

ENTROPIC COMMUNICATIONS LLC(OWNER), Residence Not Provided;
RAGHAV BAJAJ, DALLAS, TX;

INVENTORS

9210362, Residence Not Provided;
IP Section Haynes and Boone, LLP, Residence Not Provided;
CURTIS LING, CARLSBAD, CA;
TIM GALLAGHER, CARLSBAD, CA;

**** CONTINUING DATA ***************************

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which is a CON of 13/962,871 08/08/2013 PAT 9100622
which is a CON of 12/762,900 04/19/2010 PAT 8526898
which claims benefit of 61/170,526 04/17/2009

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**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

Foreign Priority claimed ☐ Yes ☐ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and Acknowledged _____ Examiner's Signature	☐ Met after Allowance _____ Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
				20	2

ADDRESS

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500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661
UNITED STATES

TITLE

WIDEBAND TUNER ARCHITECTURE

FILING FEE RECEIVED		
0.00	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Litigation Search Report CRU 3999

Reexamination Control No. 90/019,255

To:	LIE	**From:**	MANUEL SALDANA
Location:	REM04C71	**Location:**	REM04C71
Art Unit:	3992	**Phone:**	571-272-7740
Date:	31 October 2023	**E-mail:**	MANUEL.SALDANA@USPTO.GOV

Search Notes

(CLOSED) 2:23cv1050, Entropic Communications, Llc V. Comcast Corporation Et Al

(OPEN) 2:23cv1049, Entropic Communications, Llc V. Cox Communications, Inc. Et Al

(OPEN) 2:22cv125, Entropic Communications, Llc V. Charter Communications, Inc. Et Al

1. Performed a KeyCite Search in Westlaw, which retrieves all history on the patent including any litigation.
2. Performed a search on the patent in Lexis CourtLink for any open dockets or closed cases.
3. Performed a search in Lexis in the Federal Courts and Administrative Materials databases for any cases found.
4. Performed a search in Lexis in the IP Journal and Periodicals database for any articles on the patent.
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Paper No. 20231031



User Name: Manuel Saldana
Date and Time: Tuesday, October 31, 2023 11:31:00AM EDT
Job Number: 209366376

Document (1)

1. *2:23cv1049, Entropic Communications, Llc V. Cox Communications, Inc. Et Al*
   Client/Matter: -None-
   Search Terms: number(2:23CV1049)
   Search Type: Natural Language
   Narrowed by:

Content Type	Narrowed by
Dockets	Case Status: Open,Unknown,Closed

2:23cv1049, Entropic Communications, Llc V. Cox Communications, Inc. Et Al

US District Court Docket

United States District Court, California Central

(Western Division - Los Angeles)

This case was retrieved on 10/26/2023

Header

Case Number: 2:23cv1049
Date Filed: 02/10/2023
Assigned To: Judge John W. Holcomb
Referred To: Magistrate Judge Karen E. Scott
Nature of Suit: Patent (830)
Cause: Patent Infringement
Lead Docket: None
Other Docket: 2:22cv07775
Jurisdiction: Federal Question

Class Code: Open
Statute: 35:271
Jury Demand: Plaintiff
Demand Amount: $0
NOS Description: Patent

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Coxcom, LLC **Defendant**	Mitchell G. Stockwell LEAD ATTORNEY;PRO HAC VICE;ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 1100 Peachtree Street, Suite 2800 Altanta, GA 30309-4530 USA 404-815-6214 Fax: 404-541-3403 Email:Mstockwell@kilpatricktownsend.Com Andrew N. Saul PRO HAC VICE;ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 1100 Peachtree Street Ne, Suite 2800 Atlanta, GA 30309 USA 404-815-6500 Fax: 404-815-5555 Email:Asaul@kilpatricktownsend.Com April Elizabeth Isaacson ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 2 Embarcadero Center, Suite 1900 San Francisco, CA 94111 USA 415-273-8306 Fax: 415-354-3519 Email:Aisaacson@kilpatricktownsend.Com Christopher S. Leah PRO HAC VICE;ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 1100 Peachtree Street Ne, Suite 2800 Atlanta, GA 30309 USA 404-815-6081 Fax: 404-541-4664 Email:Cleah@kilpatricktownsend.Com Courtney S. Dabbiere PRO HAC VICE;ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 1100 Peachtree Street Ne, Suite 2800 Atlanta, GA 30309 USA
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Cox Communications California, LLC **Defendant**	Mitchell G. Stockwell LEAD ATTORNEY;PRO HAC VICE;ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 1100 Peachtree Street, Suite 2800 Altanta, GA 30309-4530 USA 404-815-6214 Fax: 404-541-3403 Email:Mstockwell@kilpatricktownsend.Com Andrew N. Saul PRO HAC VICE;ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 1100 Peachtree Street Ne, Suite 2800 Atlanta, GA 30309 USA 404-815-6500 Fax: 404-815-5555 Email:Asaul@kilpatricktownsend.Com April Elizabeth Isaacson ATTORNEY TO BE NOTICED
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David M Keyzer **Special Master**	David Keyzer LEAD ATTORNEY;ATTORNEY TO BE NOTICED Law Office of David Keyzer PC 5170 Golden Foothill Parkway El Dorado Hills, CA 95762 USA 916-243-5259 Fax: 916-404-0436 Email:David@keyzerlaw.Com
Cox Communications California, LLC **Counter Claimant**	Mitchell G. Stockwell LEAD ATTORNEY;ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 1100 Peachtree Street, Suite 2800 Atlanta, GA 30309-4530 USA 404-815-6214 Fax: 404-541-3403 Email:Mstockwell@kilpatricktownsend.Com Andrew N. Saul PRO HAC VICE;ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 1100 Peachtree Street Ne, Suite 2800 Atlanta, GA 30309 USA 404-815-6500 Fax: 404-815-5555 Email:Asaul@kilpatricktownsend.Com April Elizabeth Isaacson ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 2 Embarcadero Center, Suite 1900 San Francisco, CA 94111 USA 415-273-8306 Fax: 415-354-3519 Email:Aisaacson@kilpatricktownsend.Com Christopher S. Leah ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 1100 Peachtree Street Ne, Suite 2800 Atlanta, GA 30309 USA 404-815-6081 Fax: 404-541-4664 Email:Cleah@kilpatricktownsend.Com Courtney S. Dabbiere ATTORNEY TO BE NOTICED Kilpatrick Townsend and Stockton LLP 1100 Peachtree Street Ne, Suite 2800 Atlanta, GA 30309 USA 404-815-6027 Fax: 404-541-4757 Email:Cdabbiere@kilpatricktownsend.Com Michael J. Turton ATTORNEY TO BE NOTICED

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Proceedings

#	Date	Proceeding Text	Source
1	02/10/2023	COMPLAINT Receipt No: ACACDC-34782888 - Fee: $402, filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3, # 4 Exhibit 4, # 5 Exhibit 5, # 6 Exhibit 6, # 7 Exhibit 7, # 8 Exhibit 8, # 9 Exhibit 9, # 10 Exhibit 10, # 11 Exhibit 11, # 12 Exhibit 12, # 13 Exhibit 13, # 14 Exhibit 14, # 15 Exhibit 15, # 16 Exhibit 16, # 17 Exhibit 17) (Attorney Christina N. Goodrich added to party Entropic Communications, LLC(pty:pla))(Goodrich, Christina) (Entered: 02/10/2023)	
2	02/10/2023	CIVIL COVER SHEET filed by Plaintiff Entropic Communications, LLC. (Goodrich, Christina) (Entered: 02/10/2023)	
3	02/10/2023	Request for Clerk to Issue Summons on Complaint (Attorney Civil Case Opening),, 1 filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Summons to CoxCom, LLC, # 2 Proposed Summons to Cox Communications California,	

#	Date	Proceeding Text	Source
		LLC)(Goodrich, Christina) (Entered: 02/10/2023)	
4	02/10/2023	Certification and NOTICE of Interested Parties filed by Plaintiff Entropic Communications, LLC, (Goodrich, Christina) (Entered: 02/10/2023)	
5	02/10/2023	NOTICE of Related Case(s) filed by Plaintiff Entropic Communications, LLC. Related Case(s): 2:23-cv-01047; 2:22-cv-07775-JWH-JEM; 2:22-cv-07959-JWH-JEM (Goodrich, Christina) (Entered: 02/10/2023)	
6	02/10/2023	REPORT ON THE FILING OF AN ACTION Regarding a Patent or a Trademark (Initial Notification) filed by Entropic Communications, LLC. (Goodrich, Christina) (Entered: 02/10/2023)	
7	02/13/2023	NOTICE OF ASSIGNMENT to District Judge Otis D. Wright, II and Magistrate Judge Jean P. Rosenbluth. (lh) (Entered: 02/13/2023)	
8	02/13/2023	NOTICE TO PARTIES OF COURT-DIRECTED ADR PROGRAM filed. (lh) (Entered: 02/13/2023)	
9	02/13/2023	Notice to Counsel Re Consent to Proceed Before a United States Magistrate Judge. (lh) (Entered: 02/13/2023)	
10	02/13/2023	21 DAY Summons Issued re Complaint (Attorney Civil Case Opening), 1 as to Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Summons as to Defendant CoxCom, LLC, # 2 Summons as to Defendant Cox Communications California, LLC) (lh) (Entered: 02/13/2023)	
11	02/14/2023	MINUTE ORDER (IN CHAMBERS) by Judge Otis D. Wright, II. This action has been assigned to the calendar of Judge Otis D. Wright II. Counsel are STRONGLY encouraged to review the Central District's website for additional information. See minute order for details. (lom) (Entered: 02/14/2023)	
12	02/15/2023	ORDER RE TRANSFER PURSUANT TO GENERAL ORDER 21-01-Related Case- filed. Related Case No: 2:22-cv-07775 JWH(JEMx). Case transferred from Magistrate Judge Jean P. Rosenbluth and Judge Otis D. Wright, II to Judge John W. Holcomb and Magistrate Judge Karen E. Scott for all further proceedings. The case number will now reflect the initials of the transferee Judge 2:23-cv-01049 JWH(KESx). Signed by Judge John W. Holcomb (rn) (Entered: 02/15/2023)	
13	02/21/2023	MINUTE ORDER TO SHOW CAUSE REGARDING CONSOLIDATION (IN CHAMBERS) by Judge John W. Holcomb. The Court ORDERS the parties to show cause why these two cases-Nos. 2:23-CV-01049-JWH-KES AND 2:23-CV-01050-JWH-KES should not be consolidated for pretrial purposes in view of the overlap in subject matter. The parties are DIRECTED to file no later than 3/10/23, a joint response detailing their collective or respective positions regarding pretrial consolidation. A hearing on the Order to Show Case is SET for March 31, 2023 at 9:00 a.m.. IT IS SO ORDERED. (yl) (Entered: 02/22/2023)	
14	02/23/2023	STANDING ORDER by Judge John W. Holcomb. (cla) (Entered: 02/23/2023)	
15	02/23/2023	PROOF OF SERVICE Executed by Plaintiff Entropic Communications, LLC, upon Defendant Cox Communications, Inc. served on 2/15/2023, answer due 3/8/2023. Service of the Summons and Complaint were executed upon Lynanne Gares, Managing Agent, Corporation Service Company in compliance with Federal Rules of Civil Procedure by service on a domestic corporation, unincorporated association, or public entity.Original Summons NOT returned. (Goodrich, Christina) (Entered: 02/23/2023)	

#	Date	Proceeding Text	Source
16	02/23/2023	PROOF OF SERVICE Executed by Plaintiff Entropic Communications, LLC, upon Defendant CoxCom, LLC served on 2/16/2023, answer due 3/9/2023. Service of the Summons and Complaint were executed upon Trudy Desbiens, CSC Authorized Agent in compliance with Federal Rules of Civil Procedure by service on a domestic corporation, unincorporated association, or public entity.Original Summons NOT returned. (Goodrich, Christina) (Entered: 02/23/2023)	
17	02/23/2023	PROOF OF SERVICE Executed by Plaintiff Entropic Communications, LLC, upon Defendant Cox Communications California, LLC served on 2/16/2023, answer due 3/9/2023. Service of the Summons and Complaint were executed upon Trudy Desbiens, CSC Authorized Agent in compliance with Federal Rules of Civil Procedure by service on a domestic corporation, unincorporated association, or public entity.Original Summons NOT returned. (Goodrich, Christina) (Entered: 02/23/2023)	
18	03/06/2023	APPLICATION of Non-Resident Attorney Jason A. Engel to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-34906348) filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Order) (Goodrich, Christina) (Entered: 03/06/2023)	
19	03/06/2023	APPLICATION of Non-Resident Attorney Darlene F. Ghavimi to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-34906355) filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Order) (Goodrich, Christina) (Entered: 03/06/2023)	
20	03/06/2023	APPLICATION of Non-Resident Attorney James A. Shimota to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-34906366) filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Order) (Goodrich, Christina) (Entered: 03/06/2023)	
21	03/07/2023	NOTICE of Appearance filed by attorney April Elizabeth Isaacson on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC (Attorney April Elizabeth Isaacson added to party Cox Communications California, LLC(pty:dft), Attorney April Elizabeth Isaacson added to party Cox Communications, Inc.(pty:dft), Attorney April Elizabeth Isaacson added to party CoxCom, LLC(pty:dft))(Isaacson, April) (Entered: 03/07/2023)	
22	03/07/2023	NOTICE of Appearance filed by attorney Rishi Gupta on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC (Attorney Rishi Gupta added to party Cox Communications California, LLC(pty:dft), Attorney Rishi Gupta added to party Cox Communications, Inc.(pty:dft), Attorney Rishi Gupta added to party CoxCom, LLC(pty:dft))(Gupta, Rishi) (Entered: 03/07/2023)	
23	03/07/2023	NOTICE of Deficiency in Electronically Filed Pro Hac Vice Application RE: APPLICATION of Non-Resident Attorney Darlene F. Ghavimi to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-34906355) 19 . The following error(s) was/were found: Local Rule 83-2.1.3.3(d) Certificate of Good Standing not attached for every state court listed to which the applicant has been admitted. Other error(s) with document(s): Missing GSC from NJ. (lt) (Entered: 03/07/2023)	

#	Date	Proceeding Text	Source
24	03/08/2023	Joint STIPULATION Extending Time to Answer the complaint as to Cox Communications, Inc. answer now due 4/7/2023, re Complaint (Attorney Civil Case Opening),, 1 filed by Plaintiff Entropic Communications, LLC.(Goodrich, Christina) (Entered: 03/08/2023)	
25	03/08/2023	NOTICE of Appearance filed by attorney Kenneth Bridges on behalf of Plaintiff Entropic Communications, LLC (Attorney Kenneth Bridges added to party Entropic Communications, LLC(pty:pla))(Bridges, Kenneth) (Entered: 03/08/2023)	
26	03/08/2023	Joint STIPULATION Extending Time to Answer the complaint as to CoxCom, LLC answer now due 4/8/2023, re Complaint (Attorney Civil Case Opening),, 1 filed by Plaintiff Entropic Communications, LLC.(Goodrich, Christina) (Entered: 03/08/2023)	
27	03/08/2023	Joint STIPULATION Extending Time to Answer the complaint as to Cox Communications California, LLC answer now due 4/8/2023, re Complaint (Attorney Civil Case Opening),, 1 filed by Plaintiff Entropic Communications, LLC.(Goodrich, Christina) (Entered: 03/08/2023)	
28	03/08/2023	Text Only ORDER GRANTING APPLICATION of Non-Resident Attorney Jason A. Engel to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC 18 , APPLICATION of Non-Resident Attorney Darlene F. Ghavimi to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC 19 , APPLICATION of Non-Resident Attorney James A. Shimota to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC 20 by Judge John W. Holcomb. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 03/08/2023)	
29	03/10/2023	RESPONSE filed by Plaintiff Entropic Communications, LLCto Minutes of In Chambers Order/Directive - no proceeding held,,, Set/Reset Hearing,, 13 - JOINT RESPONSE TO OSC RE CONSOLIDATION (Goodrich, Christina) (Entered: 03/10/2023)	
30	03/16/2023	APPLICATION of Non-Resident Attorney Mitchell G. Stockwell to Appear Pro Hac Vice on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-34967403) filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Certificate of Good Standing - GA State Bar, # 2 Proposed Order Proposed Order) (Attorney Mitchell G Stockwell added to party Cox Communications California, LLC(pty:dft), Attorney Mitchell G Stockwell added to party Cox Communications, Inc.(pty:dft), Attorney Mitchell G Stockwell added to party CoxCom, LLC(pty:dft)) (Stockwell, Mitchell) (Entered: 03/16/2023)	
31	03/16/2023	NOTICE of Deficiency in Electronically Filed Pro Hac Vice Application RE: APPLICATION of Non-Resident Attorney Mitchell G. Stockwell to Appear Pro Hac Vice on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-34967403) 30 . The following error(s) was/were found: Local Rule 5-4.3.4 Application not hand-signed. Please note that electronic, image or stamp signatures are not allowed for either applicant or local counsel. See Instructions for Applicants (1). (lt) (Entered: 03/16/2023)	
32	03/20/2023	Text Only ORDER GRANTING APPLICATION of Non-Resident Attorney Mitchell G. Stockwell to Appear Pro Hac Vice on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC 30 by Judge John W.	

#	Date	Proceeding Text	Source
		Holcomb. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 03/20/2023)	
33	03/21/2023	Joint STIPULATION to Continue Hearing on Order to Show Cause re Consolidation from March 31, 2023 to April 21, 2023 Re: Minutes of In Chambers Order/Directive - no proceeding held,,, Set/Reset Hearing,, 13 filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Order on Joint Stipulation to Request Continuance)(Goodrich, Christina) (Entered: 03/21/2023)	
34	03/23/2023	APPLICATION of Non-Resident Attorney Michael J. Turton to Appear Pro Hac Vice on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-35006990) filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Certificate of Good Standing - GA State Bar, # 2 Certificate of Good Standing - TX State Bar, # 3 Proposed Order Proposed Order) (Attorney Michael J. Turton added to party Cox Communications California, LLC(pty:dft), Attorney Michael J. Turton added to party Cox Communications, Inc.(pty:dft), Attorney Michael J. Turton added to party CoxCom, LLC(pty:dft)) (Turton, Michael) (Entered: 03/23/2023)	
35	03/23/2023	ORDER GRANTING JOINT STIPULATION TO REQUEST CONTINUANCE OF HEARING ON ORDER TO SHOW CAUSE REGARDING CONSOLIDATION by Judge John W. Holcomb, re Stipulation to Continue 33 . it is hereby ORDERED that the March 31, 2023, hearing on the Order to Show Cause Regarding Consolidation is CONTINUED from March 31, 2023, to April 21, 2023, at 9:00 a.m. IT IS SO ORDERED. (et) (Entered: 03/23/2023)	
36	03/28/2023	APPLICATION of Non-Resident Attorney Vaibhav P. Kadaba to Appear Pro Hac Vice on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-35031686) filed by Vaibhav P. Kadaba Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Certificate of Good Standing - GA State Bar, # 2 Proposed Order Proposed Order) (Attorney Vaibhav P Kadaba added to party Cox Communications California, LLC(pty:dft), Attorney Vaibhav P Kadaba added to party Cox Communications, Inc.(pty:dft), Attorney Vaibhav P Kadaba added to party CoxCom, LLC(pty:dft)) (Kadaba, Vaibhav) (Entered: 03/28/2023)	
37	03/28/2023	APPLICATION of Non-Resident Attorney Christopher S. Leah to Appear Pro Hac Vice on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-35035078) filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Certificate of Good Standing - GA State Bar, # 2 Proposed Order Proposed Order) (Gupta, Rishi) (Entered: 03/28/2023)	
38	03/29/2023	Text Only ORDER GRANTING APPLICATION of Non-Resident Attorney Michael J. Turton to Appear Pro Hac Vice on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC 34 , APPLICATION of Non-Resident Attorney Vaibhav P. Kadaba to Appear Pro Hac Vice on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC 36 , APPLICATION of Non-Resident Attorney Christopher S. Leah to Appear Pro Hac Vice on behalf of Defendants Cox Communications California, LLC, Cox	

#	Date	Proceeding Text	Source
		Communications, Inc., CoxCom, LLC 37 by Judge John W. Holcomb. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 03/29/2023)	
39	03/31/2023	Joint STIPULATION for Extension of Time to File Answer to May 8, 2023 re Complaint (Attorney Civil Case Opening),, 1 filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Proposed Order)(Isaacson, April) (Entered: 03/31/2023)	
40	03/31/2023	NOTICE of Appearance filed by attorney Sarah Y Kamran on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC (Attorney Sarah Y Kamran added to party Cox Communications California, LLC(pty:dft), Attorney Sarah Y Kamran added to party Cox Communications, Inc.(pty:dft), Attorney Sarah Y Kamran added to party CoxCom, LLC(pty:dft))(Kamran, Sarah) (Entered: 03/31/2023)	
42	04/03/2023	MINUTE ORDER TO SHOW CAUSE REGARDING APPOINTMENT OF SPECIAL MASTER REGARDING DISCOVERY DISPUTES (IN CHAMBERS) by Judge John W. Holcomb. These cases will likely generate a substantial number of discovery disputes. For that reason, the Court is considering appointing a Special Master to assist the Court in managing and deciding discovery matters, and, therefore, it issues this order to show cause (OSC). For the foregoing reasons, the Court hereby ORDERS as follows: 1. No later than April 14, 2023, the parties are DIRECTED to respond to this OSC by each filing a statement either consenting to the appointment of a Special Master for discovery purposes or showing cause why a Special Master should not be appointed. 2. A hearing on this OSC is SET for April 21, 2023, at 9:00 a.m. See minute order for details. (lom) (Entered: 04/04/2023)	
41	04/04/2023	ORDER GRANTING TO REQUEST AN ADDITIONAL 30-DAY EXTENSION OF TIME FOR DEFENDANTS TO ANSWER OR OTHERWISE RESPOND TO PLAINTIFF'S COMPLAINT 39 by Judge John W. Holcomb. It is hereby ORDERED that the deadline for Defendants to answer or otherwise respond to Plaintiff's Complaint is EXTENDED up to and including May 8, 2023. (lom) (Entered: 04/04/2023)	
43	04/07/2023	APPLICATION of Non-Resident Attorney Courtney S. Dabbiere to Appear Pro Hac Vice on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-35100112) filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Certificate of Good Standing - GA State Bar, # 2 Proposed Order) (Gupta, Rishi) (Entered: 04/07/2023)	
44	04/11/2023	Text Only ORDER GRANTING APPLICATION of Non-Resident Attorney Courtney S. Dabbiere to Appear Pro Hac Vice on behalf of Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC 43 by Judge John W. Holcomb. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 04/11/2023)	
45	04/14/2023	STATEMENT JOINTLY SUBMITTED BY THE PARTIES IN RESPONSE TO ORDER TO SHOW CAUSE RE APPOINTMENT OF A SPECIAL MASTER filed by Plaintiff Entropic Communications, LLC re: Minutes of In Chambers Order/Directive - no proceeding held,,,, Set/Reset Deadlines/Hearings,,, 42 . (Goodrich, Christina) (Entered: 04/14/2023)	
46	04/17/2023	Notice OF INTERESTED PARTIES (LOCAL RULE 7.1-1)	

#	Date	Proceeding Text	Source
		(AMENDED) filed by Plaintiff Entropic Communications, LLC. (Goodrich, Christina) (Entered: 04/17/2023)	
47	04/18/2023	Notice of Appearance or Withdrawal of Counsel: for attorney Peter E Soskin counsel for Plaintiff Entropic Communications, LLC. Adding Peter Soskin as counsel of record for Entropic Communications, LLC for the reason indicated in the G-123 Notice. Filed by Plaintiff Entropic Communications, LLC. (Attorney Peter E Soskin added to party Entropic Communications, LLC(pty:pla))(Soskin, Peter) (Entered: 04/18/2023)	
48	04/21/2023	MINUTE ORDER OF HEARING RE: ORDER TO SHOW CAUSE RE CONSOLIDATION held before Judge John W. Holcomb. Counsel state their appearances. The Court confers with counsel regarding the posture of the case. For the reasons stated on the record, the parties are DIRECTED to meet and confer regarding a proposed order pertaining to consolidation and the appointment of Special Master. IT IS SO ORDERED. Court Reporter: Debbie Hino-Span. (yl) (Entered: 04/24/2023)	
49	05/08/2023	ANSWER to Complaint (Attorney Civil Case Opening),, 1 with JURY DEMAND - Answer and Defenses to Complaint filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC.(Isaacson, April) (Entered: 05/08/2023)	
50	05/08/2023	CORPORATE DISCLOSURE STATEMENT - DEFENDANTS FED. R. CIV. P. 7.1 DISCLOSURE STATEMENT AND L.R. 7.1-1 NOTICE OF INTERESTED PARTIES filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC identifying Cox Enterprises, Inc. as Corporate Parent. (Isaacson, April) (Entered: 05/08/2023)	
51	05/14/2023	TRANSCRIPT for proceedings held on 4/21/2023 at 8:59 a.m. ****Transcript may be viewed at the court public terminal or purchased through Court Reporter DEBBIE HINO-SPAAN at: WEBSITE www.debbiehinospaan.com; E-mail, dhinospaan@yahoo.com before the deadline for Release of Transcript restriction. After that date, it may be obtained from the Court Reporter or through PACER. Additional formats of the transcript (ASCII, Condensed, and Word Indexing/Concordance) are also available to be purchased at any time through the Court Reporter. Notice of Intent to Redact due within 7 days of this date.** Redaction Request due 6/5/2023. Redacted Transcript Deadline set for 6/14/2023. Release of Transcript Restriction set for 8/14/2023. (dhs) (Entered: 05/14/2023)	
52	05/14/2023	NOTICE OF FILING TRANSCRIPT filed for proceedings 4/21/2023 at 8:59 a.m. re Transcript 51 THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (dhs) TEXT ONLY ENTRY (Entered: 05/14/2023)	
53	05/17/2023	ORDER SETTING SCHEDULING CONFERENCE by Judge John W. Holcomb. Scheduling Conference set for 6/30/2023 at 9:00 AM before Judge John W. Holcomb. (cla) (Entered: 05/17/2023)	
54	05/17/2023	SCHEDULING NOTICE AND ORDER by Judge John W. Holcomb: On its own motion, the Court SETS a Status Conference on June 9, 2023, at 11:00 a.m. The parties are DIRECTED to file a Joint Status Report no later than Friday, May 26, 2023, that includes an update regarding the appointment of a Special Master and case consolidation. The parties are DIRECTEDto appear in person in Courtroom 9D, on the 9th Floor of the Ronald Reagan Federal Building and United States Courthouse at 411 W. Fourth Street Santa Ana, CA 92701. IT IS SO ORDERED.THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered:	

#	Date	Proceeding Text	Source
		05/17/2023)	
55	05/26/2023	STATUS REPORT re Consolidation and Appointment of Special Master Prepared Jointly by All Parties filed by Plaintiff Entropic Communications, LLC. (Goodrich, Christina) (Entered: 05/26/2023)	
56	05/26/2023	APPLICATION of Non-Resident Attorney George C. Summerfield to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-35393516) filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Order) (Goodrich, Christina) (Entered: 05/26/2023)	
57	05/30/2023	SCHEDULING NOTICE AND ORDER by Judge John W. Holcomb: On its own motion, the Court CONTINUES the Status Conference from June 9, 2023, at 11:00 a.m., to June 9, 2023, at 9:00 a.m. ***TIME CHANGE ONLY*** The parties are DIRECTED to appear in person in Courtroom 9D, on the 9th Floor of the Ronald Reagan Federal Building and United States Courthouse at 411 W. Fourth Street Santa Ana, CA 92701. IT IS SO ORDERED.THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (ev) TEXT ONLY ENTRY (Entered: 05/30/2023)	
58	05/31/2023	Text Only ORDER GRANTING APPLICATION of Non-Resident Attorney George C. Summerfield to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC 56 by Judge John W. Holcomb. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (ev) TEXT ONLY ENTRY (Entered: 05/31/2023)	
59	06/06/2023	Joint STIPULATION to Continue Scheduling Conference from June 30, 2023 to July 21, 2023 Re: Initial Order Setting R26 Scheduling Conference - form only 53 filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Proposed Order)(Isaacson, April) (Entered: 06/06/2023)	
60	06/08/2023	Joint STIPULATION for Order to Appoint Special Master filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Affidavit of David M. Keyzer Pursuant to Fed. R. Civ. P. 53(b)(3)(A), # 2 Proposed Order)(Goodrich, Christina) (Entered: 06/08/2023)	
61	06/09/2023	MINUTE ORDER OF STATUS CONFERENCE held before Judge John W. Holcomb. For the reasons stated on the record, the Court hereby ORDERS as follows: The parties Joint Stipulation for Continuance of the Scheduling Conference [ECF No. 59] is APPROVED. The Scheduling Conference is CONTINUED to July 21, 2023, at 11:00 a.m. IT IS SO ORDERED. Court Reporter: Debbie Hino-Span. (yl) (Entered: 06/13/2023)	
62	07/05/2023	ORDER APPOINTING DAVID KEYZER, ESQ. AS SPECIAL MASTER FOR DISCOVERY PURPOSES by Judge John W. Holcomb, re Stipulation 60 : Pursuant to Fed. R. Civ. P. 53(b)(3)(A), and good cause shown, it is hereby ORDERED as follows: 1. Appointment: The Court determines that the appointment of David Keyzer, Esq. (the "Special Master") is appropriate under Rule 53(a)(1)(C) of the Federal Rules of Civil Procedure to address pretrial matters that cannot be effectively and timely addressed by an available district judge or magistrate judge in this district. (see document for further details) (bm) (Entered: 07/05/2023)	
63	07/07/2023	JOINT REPORT Rule 26(f) Discovery Plan ; estimated length of trial 6 to 8 days, filed by Plaintiff Entropic Communications, LLC.. (Goodrich, Christina) (Entered: 07/07/2023)	

#	Date	Proceeding Text	Source
64	07/10/2023	SCHEDULING NOTICE AND ORDER by Judge John W. Holcomb: On its own motion, the Court CONTINUES the Scheduling Conference from Friday, July 21, 2023, to Wednesday, August 9, 2023, at 10:00 a.m. The parties are DIRECTED to appear in person in Courtroom 9D, on the 9th Floor of the Ronald Reagan Federal Building and United States Courthouse at 411 W. Fourth Street Santa Ana, CA 92701. IT IS SO ORDERED.THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 07/10/2023)	
65	07/17/2023	TRANSCRIPT for proceedings held on 6/9/2023 at 9:05 a.m. ****Transcript may be viewed at the court public terminal or purchased through Court Reporter DEBBIE HINO-SPAAN at: WEBSITE www.debbiehinospaan.com; E-mail, dhinospaan@yahoo.com before the deadline for Release of Transcript restriction. After that date, it may be obtained from the Court Reporter or through PACER. Additional formats of the transcript (ASCII, Condensed, and Word Indexing/Concordance) are also available to be purchased at any time through the Court Reporter. Notice of Intent to Redact due within 7 days of this date.** Redaction Request due 8/7/2023. Redacted Transcript Deadline set for 8/17/2023. Release of Transcript Restriction set for 10/16/2023. (dhs) (Entered: 07/17/2023)	
66	07/17/2023	NOTICE OF FILING TRANSCRIPT filed for proceedings 6/9/2023 at 9:05 a.m. re Transcript 65 THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (dhs) TEXT ONLY ENTRY (Entered: 07/17/2023)	
67	07/24/2023	Notice of Special Master Order No. SM-1 filed by Special Master David M Keyzer. pursuant to July 5, 2023 appointment Order, setting special master preliminary conference for July 26, 2023, at 12:00 P.M., by videoconference (Attachments: # 1 Special Master Order No. SM-1)(Keyzer, David) (Entered: 07/24/2023)	
68	07/26/2023	Notice of Special Master Minutes filed by Special Master David M Keyzer. minutes of preliminary conference conducted by the special master on July 26, 2023, pursuant to the Court's July 5, 2023 Order appointing special master (Attachments: # 1 Special Master Minutes)(Keyzer, David) (Entered: 07/26/2023)	
69	08/01/2023	Notice of Appearance or Withdrawal of Counsel: for attorney Cassidy Young counsel for Plaintiff Entropic Communications, LLC. Adding Cassidy Young as counsel of record for Plaintiff Entropic Communications, LLC for the reason indicated in the G-123 Notice. Filed by Plaintiff Entropic Communications, LLC. (Attorney Cassidy Young added to party Entropic Communications, LLC(pty:pla))(Young, Cassidy) (Entered: 08/01/2023)	
70	08/04/2023	Notice of Special Master Order No. SM-2 filed by Special Master David M Keyzer. regarding Discovery Dispute Resolution Procedures (Attachments: # 1 Special Master Order No. SM-2 re Discovery Dispute Resolution Procedures)(Keyzer, David) (Entered: 08/04/2023)	
71	08/09/2023	HEARING RE: SCHEDULING CONFERENCE held before Judge John W. Holcomb. Counsel are DIRECTED to meet and confer forthwith regarding the Claim Construction Schedule. The parties are DIRECTED to file no later than August 18, 2023, a Stipulation and Proposed Order setting a Claim Construction Schedule. IT IS SO ORDERED. Court Reporter: Miriam Baird. (yl) (Entered: 08/14/2023)	
72	08/18/2023	TRANSCRIPT for proceedings held on 8/9/23. Court Reporter/Electronic Court Recorder: miriam baird, phone number	

#	Date	Proceeding Text	Source
		mvb11893@aol.com. Transcript may be viewed at the court public terminal or purchased through the Court Reporter/Electronic Court Recorder before the deadline for Release of Transcript Restriction. After that date it may be obtained through PACER. Notice of Intent to Redact due within 7 days of this date. Redaction Request due 9/8/2023. Redacted Transcript Deadline set for 9/18/2023. Release of Transcript Restriction set for 11/16/2023. (Baird, Miriam) (Entered: 08/18/2023)	
73	08/18/2023	NOTICE OF FILING TRANSCRIPT filed for proceedings 8/9/23 re Transcript 72 THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (Baird, Miriam) TEXT ONLY ENTRY (Entered: 08/18/2023)	
74	08/18/2023	STIPULATION for Order Setting Claim Construction Schedule filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Young, Cassidy) (Entered: 08/18/2023)	
75	08/21/2023	ORDER GRANTING STIPULATION SETTING CLAIM CONSTRUCTION SCHEDULE by Judge John W. Holcomb. The dates for the claim construction are as follows: The Claim Construction hearing is on Tuesday, July 16, 2024, at 10:00 a.m.. The Reply Claim is due Friday, June 21, 2024. The Completion of Claim Discovery is due Friday, May 3, 2024 (SEE DOCUMENT FOR FURTHER DETAILS). IT IS SO ORDERED. (yl) (Entered: 08/22/2023)	
76	08/25/2023	APPLICATION to file document - Amended Answer, Defenses and Counterclaims under seal filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Proposed Order Granting Mot. to Seal, # 2 Redacted Document - Memo ISO Mot to Amend Answer, # 3 Redacted Document - Amended Answer, # 4 Redacted Document - Exh. A to Amended Answer)(Isaacson, April) (Entered: 08/25/2023)	
77	08/25/2023	SEALED DECLARATION IN SUPPORT OF APPLICATION to file document - Amended Answer, Defenses and Counterclaims under seal 76 filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Unredacted Document - Memo ISO Mot to Amend Answer, # 2 Unredacted Document - Amended Answer, # 3 Unredacted Document - Ex. A to Amended Answer)(Isaacson, April) (Entered: 08/25/2023)	
78	08/25/2023	CERTIFICATE OF SERVICE filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC, re Sealed Declaration in SupportDeclaration, 77 served on August 25, 2023. (Isaacson, April) (Entered: 08/25/2023)	
79	08/25/2023	NOTICE OF MOTION AND MOTION to AMEND ANSWER AND JOINDER filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. Motion set for hearing on 9/22/2023 at 08:45 AM before Judge John W. Holcomb. (Attachments: # 1 Memorandum of Points and Authorities - REDACTED, # 2 Proposed Order, # 3 - Amended Answer - REDACTED, # 4 Exhibit A to Amended Answer - REDACTED, # 5 Exhibit B to Amended Answer, # 6 Exhibit C to Amended Answer, # 7 Exhibit D to Amended Answer, # 8 - Redline Compare Original Answer to Amended Answer - REDACTED) (Isaacson, April) (Entered: 08/25/2023)	
80	08/28/2023	SCHEDULING NOTICE AND ORDER by Judge John W. Holcomb: On its own motion, the Court RESETS the hearing on Defendant's Motion to Amend Answer to Complaint [ECF No. 79] to September 22, 2023, at 9:00 a.m. ***TIME CHANGE ONLY***	

#	Date	Proceeding Text	Source
		The parties are DIRECTED to appear in person in Courtroom 9D, on the 9th Floor of the Ronald Reagan Federal Building and United States Courthouse at 411 W. Fourth Street Santa Ana, CA 92701. IT IS SO ORDERED. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 08/28/2023)	
81	08/30/2023	ORDER GRANTING COX COMMUNICATIONS, INC., COXCOM, LLC, AND COX COMMUNICATIONS CALIFORNIA, LLC'S APPLICATION FOR LEAVE TO FILE UNDER SEAL by Judge John W. Holcomb. The Court, having considered all papers filed in support of the application finds that there is a good cause for granting the application in its entirety. Accordingly, it is hereby ORDERED that Plaintiff's Application is GRANTED. IT IS SO ORDERED.(yl) (Entered: 08/31/2023)	
82	08/31/2023	SEALED DOCUMENT - Memo of Points and Authorities for Cox's Motion for Leave to Amend Answer re NOTICE OF MOTION AND MOTION to AMEND ANSWER AND JOINDER 79 , Order on Motion for Leave to File Document Under Seal, 81 filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Unredacted Document - Amended Answer, # 2 Unredacted Document - Exhibit A to Amended Answer)(Isaacson, April) (Entered: 08/31/2023)	
83	09/01/2023	NOTICE OF NON-OPPOSITION to NOTICE OF MOTION AND MOTION to AMEND ANSWER AND JOINDER 79 filed by Plaintiff Entropic Communications, LLC. (Young, Cassidy) (Entered: 09/01/2023)	
84	09/14/2023	Joint STIPULATION to Waive Oral Argument for Hearing on Defendants' Motion for Leave to Amend Answer filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Proposed Order)(Isaacson, April) (Entered: 09/14/2023)	
85	09/15/2023	(IN CHAMBERS) ORDER by Judge John W. Holcomb: The Court finds that the Defendant's Motion for Leave to Amend Answer to Complaint [ECF No. 79] is appropriate for resolution without a hearing. See Fed. R. Civ. P. 78; L.R. 7-15. Accordingly, the Court VACATES the hearing set on September 22, 2023. The motion stands submitted on the papers timely filed. IT IS SO ORDERED. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 09/15/2023)	
86	10/05/2023	ORDER GRANTING MOTION OF DEFENDANTS COX COMMUNICATIONS, INC.; COXCOM, LLC; AND COX COMMUNICATIONS CALIFORNIA, LLC FOR LEAVE TO AMEND ANSWER AND JOINDER [ECF NO. 79] by Judge John W. Holcomb. The Court GRANTS Cox's Motion for Leave to Amend. The Court need not decide whether Rule 15 or Rule 16 applies because Cox has met both standards. Under Rule 16, Cox has shown good cause by acting with diligence and filing this motion based on information obtained somewhat recently during discovery. The Court also GRANTS Cox's Motion for Joinder. Cox has at least met the permissive Rule 20 standard. MaxLinear may be joined at least because Cox asserts breach of contract and unjust enrichment claims against MaxLinear and because there are common question of fact surrounding the DOCSIS License Agreement, which potentially affects Entropics allegations of patent infringement. Entropic presents no evidence or argument countering Cox's joinder request. For the foregoing reasons, the Court GRANTS Cox's Motion. Cox is DIRECTED to file its amended answer and counterclaims no later than October 20, 2023. IT IS SO ORDERED. (See document for further details) (yl)	

#	Date	Proceeding Text	Source
		(Entered: 10/06/2023)	
87	10/06/2023	SEALED DOCUMENT - Amended Answer, Defenses and Counterclaims re Complaint (Attorney Civil Case Opening),, 1 , Order on Motion for Leave,,,, 86 filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Exhibit A to the Complaint - SEALED, # 2 Exhibit B to the Complaint, # 3 Exhibit C to the Complaint, # 4 Exhibit D to the Complaint)(Isaacson, April) (Entered: 10/06/2023)	
88	10/06/2023	CERTIFICATE OF SERVICE filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC, re Sealed Document, 87 - Amended Answer, Defenses and Counterclaims served on October 6, 2023. (Isaacson, April) (Entered: 10/06/2023)	
89	10/12/2023	SEALED DOCUMENT Counterclaims on ENTROPIC COMMUNICATIONS LLC; MAXLINEAR, INC.; MAXLINEAR COMMUNICATIONS LLC re Order on Motion for Leave,,,, 86 filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Exhibit A - SEALED, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D)(Isaacson, April) (Entered: 10/12/2023)	
90	10/12/2023	Request for Clerk to Issue Summons on Sealed Document, 89 filed by Counter-Claimants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Isaacson, April) (Entered: 10/12/2023)	
91	10/12/2023	CERTIFICATE OF SERVICE filed by Counter-Claimants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC, re Sealed Document, 89 served on 10/12/23. (Isaacson, April) (Entered: 10/12/2023)	
92	10/13/2023	STIPULATION to Continue Deadline to Respond to Counterclaims from October 27, 2023 to November 27, 2023 filed by Counter-Defendant Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Young, Cassidy) (Entered: 10/13/2023)	
93	10/16/2023	STIPULATION to Consolidate Cases as to 2:23-cv-01049 and 2:23-cv-01050 filed by Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Proposed Order)(Isaacson, April) (Entered: 10/16/2023)	
94	10/16/2023	ANSWER to Complaint (Attorney Civil Case Opening),, 1 with JURY DEMAND - Amended Answer, Defenses and Counterclaims, COUNTERCLAIM against Entropic Communications, LLC, MaxLinear Communications LLC filed by Defendants Cox Communications California, LLC, CoxCom, LLC, Cox Communications, Inc.. (Attachments: # 1 Exhibit A to the Complaint - Redacted, # 2 Exhibit B to the Complaint, # 3 Exhibit C to the Complaint, # 4 Exhibit D to the Complaint)(Isaacson, April) (Entered: 10/16/2023)	
95	10/16/2023	ORDER GRANTING JOINT STIPULATION TO CONSOLIDATE CASES 93 by Judge John W. Holcomb. The Parties' Joint Stipulation to Consolidate Cases is GRANTED. The following cases are CONSOLIDATED into a single action for pretrial purposes through the date of the Markman hearing: Case No. 2:23-cv-01049-JWH-KES and Case No. 2:23-cv-01050-JWH-KES. The Clerk is DIRECTED to close the following case administratively: Case No. 2:23-cv-01050-JWH-KES. IT IS SO ORDERED. (yl) (Entered: 10/17/2023)	
96	10/18/2023	21 DAY Summons Issued as to Counter defendants MaxLinear Communications LLC, and MaxLinear, Inc.. (yl) (Entered: 10/18/2023)	

#	Date	Proceeding Text	Source
97	10/19/2023	APPLICATION of Non-Resident Attorney Andrew N. Saul to Appear Pro Hac Vice on behalf of Counter Claimants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC, Defendants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-36255900) filed by Defendants and Counter-Claimants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC. (Attachments: # 1 Proposed Order) (Gupta, Rishi) (Entered: 10/19/2023)	
98	10/24/2023	Text Only ORDER GRANTING APPLICATION of Non-Resident Attorney Andrew N. Saul to Appear Pro Hac Vice on behalf of Counter Claimants Cox Communications California, LLC, Cox Communications, Inc., CoxCom, LLC, Defendants Cox Communications California, LLC, Cox Communications, Inc 97 by Judge John W. Holcomb. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 10/24/2023)	
99	10/24/2023	STIPULATION for Protective Order filed by Plaintiff Entropic Communications, LLC.(Goodrich, Christina) (Entered: 10/24/2023)	
100	10/24/2023	STIPULATION for Protective Order filed by Plaintiff Entropic Communications, LLC.(Goodrich, Christina) (Entered: 10/24/2023)	
101	10/24/2023	(IN CHAMBERS) ORDER by Judge John W. Holcomb: The Court has reviewed the parties' Stipulation [ECF No. 92], and it is hereby APPROVED. Entropic's deadline to respond to Cox's Counterclaims [ECF No.87] is CONTINUED from October 27, 2023, to November 27, 2023. IT IS SO ORDERED. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 10/24/2023)	
102	10/30/2023	Notice of Special Master Order No. SM-4 filed by Special Master David M Keyzer. setting special master discovery hearing for November 3, 2023, at 12:30 P.M., by videoconference (Attachments: # 1 Special Master Order No. SM-4)(Keyzer, David) (Entered: 10/30/2023)	Events since last full update
103	10/30/2023	Joint STIPULATION Extending Time to Answer the complaint as to MaxLinear Communications LLC answer now due 12/8/2023, re Answer to Complaint (Attorney Civil Case Opening),, Counterclaim, 94 filed by Defendants MaxLinear Communications LLC; MaxLinear, Inc.. (Attachments: # 1 Proposed Order)(Attorney Rose S Lee added to party MaxLinear Communications LLC(pty:cd), Attorney Rose S Lee added to party MaxLinear, Inc.(pty:cd))(Lee, Rose) (Entered: 10/30/2023)	Events since last full update

Patents

Number	Title	Issued	Class	Subclass
8,223,775	Architecture for a flexible and high-performance gateway cable modem	07/17/2012	370	401
8,284,690	Receiver determined probe	10/09/2012	370	252
8,792,008	Method and apparatus for spectrum monitoring	07/29/2014	348	192
9,210,362	Wideband tuner architecture	12/08/2015	1	1
9,825,826	Method and apparatus for spectrum monitoring	11/21/2017	1	1
10,135,682	Method and system for service group management in a cable network	11/20/2018	1	1
11,381,866	Cable television device	07/05/2022	1	1
11,399,206	Method for receiving a television signal	07/26/2022	1	1

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User Name: Manuel Saldana
Date and Time: Tuesday, October 31, 2023 11:35:00AM EDT
Job Number: 209366960

Document (1)

1. *2:22cv125 Entropic Communications, Llc V. Charter Communications, Inc. Et Al*
   Client/Matter: -None-
   Search Terms: number(2:22CV125)
   Search Type: Natural Language
   Narrowed by:

Content Type	Narrowed by
Dockets	Case Status: Open,Unknown,Closed

2:22cv125, Entropic Communications, Llc V. Charter Communications, Inc. Et Al

US District Court Docket

United States District Court, Texas Eastern

(Marshall)

This case was retrieved on 10/31/2023

Header

Case Number: 2:22cv125

Date Filed: 04/27/2022
Assigned To: District Judge Rodney Gilstrap
Nature of Suit: Patent (830)
Cause: Patent Infringement
Lead Docket: None
Other Docket: 2:22cv00050, 2:22cv00051, 2:22cv00052
Jurisdiction: Federal Question

Class Code: Open
Statute: 35:271
Jury Demand: Plaintiff
Demand Amount: $0
NOS Description: Patent

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Proceedings

#	Date	Proceeding Text	Source
1	04/27/2022	COMPLAINT against Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC (Filing fee $ 402 receipt number 0540-8892861.), filed by Entropic Communications, LLC. (Attachments: # 1 Civil Cover Sheet, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L)(Hill, Jack) (Entered: 04/27/2022)	
2	04/27/2022	Notice of Filing of Patent/Trademark Form (AO 120). AO 120 mailed to the Director of the U.S. Patent and Trademark Office. (Hill, Jack) (Entered: 04/27/2022)	
3	04/27/2022	CORPORATE DISCLOSURE STATEMENT filed by Entropic Communications, LLC identifying Corporate Parent Entropic Holdings, LLC for Entropic Communications, LLC. (Hill, Jack) (Entered: 04/27/2022)	
4	04/27/2022	DEMAND for Trial by Jury by Entropic Communications, LLC. (Hill, Jack) (Entered: 04/27/2022)	
	04/27/2022	Case assigned to District Judge Rodney Gilstrap. (ch,) (Entered: 04/27/2022)	
	04/27/2022	In accordance with the provisions of 28 USC Section 636(c), you are hereby notified that a U.S. Magistrate Judge of this district court is available to conduct any or all proceedings in this case including a jury or non-jury trial and to order the entry of a final judgment. The form Consent to Proceed Before Magistrate Judge is available on our website. All signed consent forms, excluding pro se parties, should be filed electronically using the event Notice Regarding Consent to Proceed Before Magistrate Judge. (ch,) (Entered: 04/27/2022)	
5	04/27/2022	SUMMONS Issued as to Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC. (Attachments: # 1 Summons(es), # 2 Summons(es))(ch,) (Entered: 04/27/2022)	
6	05/09/2022	SUMMONS Returned Executed by Entropic Communications, LLC. Charter Communications, Inc. served on 5/3/2022, answer due 5/24/2022. (Hill, Jack) (Entered: 05/09/2022)	
7	05/09/2022	SUMMONS Returned Executed by Entropic Communications, LLC. Spectrum Advanced Services, LLC served on 5/3/2022,	

#	Date	Proceeding Text	Source
		answer due 5/24/2022. (Hill, Jack) (Entered: 05/09/2022)	
8	05/09/2022	SUMMONS Returned Executed by Entropic Communications, LLC. Spectrum Management Holding Company, LLC served on 5/3/2022, answer due 5/24/2022. (Hill, Jack) (Entered: 05/09/2022)	
9	05/18/2022	NOTICE of Attorney Appearance by Andrea Leigh Fair on behalf of Entropic Communications, LLC (Fair, Andrea) (Entered: 05/18/2022)	
10	05/23/2022	Defendant's Unopposed First Application for Extension of Time to Answer Complaint re Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC.(Dacus, Deron) (Entered: 05/23/2022)	
	05/23/2022	Defendant's Unopposed First Application for Extension of Time to Answer Complaint is granted pursuant to Local Rule CV-12 for Spectrum Management Holding Company, LLC to 6/23/2022; Spectrum Advanced Services, LLC to 6/23/2022; Charter Communications, Inc. to 6/23/2022. 30 Days Granted for Deadline Extension.(nkl,) (Entered: 05/23/2022)	
11	05/23/2022	Defendant's Unopposed Second Application for Extension of Time to Answer Complaint re Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC.(Dacus, Deron) (Entered: 05/23/2022)	
	05/23/2022	Defendant's Unopposed Second Application for Extension of Time to Answer Complaint is granted pursuant to Local Rule CV-12 for Spectrum Management Holding Company, LLC to 7/8/2022; Spectrum Advanced Services, LLC to 7/8/2022; Charter Communications, Inc. to 7/8/2022. 15 Days Granted for Deadline Extension.(nkl,) (Entered: 05/23/2022)	
12	05/24/2022	AMENDED COMPLAINT against Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC, filed by Entropic Communications, LLC. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I, # 10 Exhibit J, # 11 Exhibit K, # 12 Exhibit L, # 13 Exhibit M, # 14 Exhibit N)(Hill, Jack Wesley) (Entered: 05/24/2022)	
13	06/14/2022	ORDER - Scheduling Conference set for 7/19/2022 10:00 AM before District Judge Rodney Gilstrap. Signed by District Judge Rodney Gilstrap on 6/14/2022. (ch,) (Entered: 06/15/2022)	
14	07/06/2022	NOTICE of Discovery Disclosure by Entropic Communications, LLC (P.R. 3-1 and P.R. 3-2 Disclosures) (Hill, Jack Wesley) (Entered: 07/06/2022)	
15	07/08/2022	NOTICE of Attorney Appearance - Pro Hac Vice by Palak Mayani Parikh on behalf of Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC. Filing fee $ 100, Receipt #ATXEDC-9010087. (nkl,) (Entered: 07/08/2022)	
16	07/08/2022	NOTICE of Attorney Appearance - Pro Hac Vice by Albert John Boardman on behalf of All Defendants. Filing fee $ 100, receipt number ATXEDC-9010246. (Boardman, Albert) (Entered: 07/08/2022)	
17	07/08/2022	NOTICE of Attorney Appearance - Pro Hac Vice by David S Benyacar on behalf of All Defendants. Filing fee $ 100, receipt number ATXEDC-9010286. (Benyacar, David) (Entered: 07/08/2022)	
18	07/08/2022	MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) by Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC. (Attachments: # 1 Declaration - Armstrong, # 2 Declaration -	

#	Date	Proceeding Text	Source
		Burdett, # 3 Declaration - Nelson, # 4 Declaration - Smith, # 5 Text of Proposed Order)(Dacus, Deron) (Entered: 07/08/2022)	
19	07/08/2022	CORPORATE DISCLOSURE STATEMENT filed by Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC (Dacus, Deron) (Entered: 07/08/2022)	
20	07/08/2022	NOTICE of Attorney Appearance - Pro Hac Vice by Daniel Reisner on behalf of All Defendants. Filing fee $ 100, receipt number ATXEDC-9010457. (Reisner, Daniel) (Entered: 07/08/2022)	
21	07/13/2022	NOTICE of Attorney Appearance - Pro Hac Vice by James A Shimota on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9017573. (Shimota, James) (Entered: 07/13/2022)	
22	07/13/2022	NOTICE of Attorney Appearance - Pro Hac Vice by Jason A Engel on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9017576. (Engel, Jason) (Entered: 07/13/2022)	
23	07/13/2022	NOTICE of Attorney Appearance by George C Summerfield on behalf of Entropic Communications, LLC (Summerfield, George) (Entered: 07/13/2022)	
	07/19/2022	Minute Entry for proceedings held before District Judge Rodney Gilstrap: Scheduling Conference held on 7/19/2022. Counsel for the parties appeared. Court asked whether they consented to trial before the U.S. Magistrate Judge. Court then gave counsel Claim Construction and Jury Selection/Trial dates. (Court Reporter Shawn McRoberts, RMR, CRR) (aeb) (Entered: 07/19/2022)	
24	07/22/2022	Joint MOTION for Extension of Time to File Response/Reply as to 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) and for Limited Expedited Venue Discovery by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 07/22/2022)	
25	07/25/2022	ORDER granting 24 Joint MOTION for Extension of Time to File Response/Reply as to 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) and for Limited Expedited Venue Discovery ORDERED that the parties may conduct venue discovery subject to the agreements set forth in the Motion. (Dkt. No. 24 at 23.) It is ORDERED that the venue discoveryshall be completed by September 30, 2022 and the deadline for Entropics response to Charters Motionto Dismiss for Improper Venue (Dkt. No. 18) is extended until October 14, 2022. Signed by District Judge Rodney Gilstrap on 7/25/2022. (ch,) (Entered: 07/25/2022)	
26	08/02/2022	Unopposed MOTION for Extension of Time to File by Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC. (Attachments: # 1 Text of Proposed Order)(Dacus, Deron) (Entered: 08/02/2022)	
27	08/03/2022	ORDER granting 26 Unopposed MOTION for Extension of Time to File Docket Control Order. Signed by District Judge Rodney Gilstrap on 8/3/2022. (ch,) (Entered: 08/03/2022)	
28	08/05/2022	NOTICE of Attorney Appearance - Pro Hac Vice by Nicholas F. Lenning on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9055865. (Lenning, Nicholas) (Entered: 08/05/2022)	
29	08/05/2022	Agreed MOTION for Entry of Docket Control Order by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 08/05/2022)	
30	08/05/2022	Agreed MOTION for Entry of Discovery Order by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 08/05/2022)	

#	Date	Proceeding Text	Source
31	08/09/2022	Unopposed MOTION for Extension of Time to File by Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC. (Attachments: # 1 Text of Proposed Order)(Dacus, Deron) (Entered: 08/09/2022)	
32	08/09/2022	Agreed MOTION for Entry of Protective Order by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 08/09/2022)	
33	08/10/2022	ORDER granting 31 Motion for Extension of Time to File Disclosures. Signed by District Judge Rodney Gilstrap on 8/10/2022. (ch,) (Entered: 08/10/2022)	
34	08/10/2022	DISCOVERY ORDER granting 30 Agreed MOTION for Entry of Discovery Order. Signed by District Judge Rodney Gilstrap on 8/10/2022. (ch,) (Entered: 08/10/2022)	
35	08/10/2022	DOCKET CONTROL ORDER granting 29 Agreed MOTION for Entry of Docket Control Order. Pretrial Conference set for 10/30/2023 09:00 AM before District Judge Rodney Gilstrap., Amended Pleadings due by 3/28/2023., Jury Selection set for 12/4/2023 09:00AM before District Judge Rodney Gilstrap., Markman Hearing set for 6/13/2023 09:00 AM before District Judge Rodney Gilstrap., Motions due by 10/10/2023., Proposed Pretrial Order due by 10/23/2023.). Signed by District Judge Rodney Gilstrap on 8/10/2022. (ch,) (Entered: 08/10/2022)	
36	08/10/2022	STIPULATED PROTECTIVE ORDER. Signed by District Judge Rodney Gilstrap on 8/10/2022. (ch,) (Entered: 08/10/2022)	
37	08/15/2022	NOTICE by Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC Notice of Compliance (Dacus, Deron) (Entered: 08/15/2022)	
38	08/18/2022	NOTICE of Discovery Disclosure by Entropic Communications, LLC (Initial Disclosures) (Hill, Jack Wesley) (Entered: 08/18/2022)	
39	08/30/2022	Agreed MOTION Agreed Motion for Entry of First Amended Docket Control Order re 35 Order,,, Terminate Motions,,, Scheduling Order,. by Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC. (Attachments: # 1 Text of Proposed Order)(Dacus, Deron) (Entered: 08/30/2022)	
40	08/31/2022	FIRST AMENDED DOCKET CONTROL ORDER granting 39 Agreed MOTION Agreed Motion for Entry of First Amended Docket Control Order re 35 Order. Signed by District Judge Rodney Gilstrap on 8/31/2022. (ch,) (Entered: 09/01/2022)	
41	09/08/2022	NOTICE by Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC Notice of Compliance (Dacus, Deron) (Entered: 09/08/2022)	
42	09/23/2022	Unopposed MOTION for Extension of Time to File Response/Reply as to 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 09/23/2022)	
43	09/26/2022	ORDER granting 42 Unopposed MOTION for Extension of Time to File Response/Reply as to 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) , 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) Responses due by 11/11/2022. Signed by District Judge Rodney Gilstrap on 9/26/2022. (ch,) (Entered: 09/27/2022)	
44	09/27/2022	NOTICE of Attorney Appearance by Matthew Alexander Blair on behalf of Entropic Communications, LLC (Blair, Matthew) (Entered: 09/27/2022)	
45	09/28/2022	NOTICE of Attorney Appearance by Darlene Fae Ghavimi on behalf of All Plaintiffs (Ghavimi, Darlene) (Entered: 09/28/2022)	

#	Date	Proceeding Text	Source
46	10/25/2022	Unopposed MOTION for Extension of Time to File Response/Reply as to 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 10/25/2022)	
47	10/31/2022	ORDER granting 46 Unopposed MOTION for Extension of Time to File Response/Reply as to 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) . Signed by District Judge Rodney Gilstrap on 10/31/2022. (ch,) (Entered: 10/31/2022)	
48	12/02/2022	Unopposed MOTION for Extension of Time to File Response/Reply as to 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 12/02/2022)	
49	12/08/2022	ORDER granting 48 Unopposed MOTION for Extension of Time to File Response/Reply as to 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) , 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) Responses due by 1/6/2023. Signed by District Judge Rodney Gilstrap on 12/8/2022. (ch,) (Entered: 12/08/2022)	
50	01/04/2023	NOTICE of Attorney Appearance by Elizabeth Anne Long on behalf of All Defendants (Long, Elizabeth) (Entered: 01/04/2023)	
51	01/04/2023	Unopposed MOTION for Extension of Time to File Response/Reply as to 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 01/04/2023)	
52	01/05/2023	ORDER granting 51 Unopposed MOTION for Extension of Time to File Response/Reply as to 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3). Extended to 1/10/2023. Signed by District Judge Rodney Gilstrap on 1/5/2023. (ch,) (Entered: 01/05/2023)	
53	01/10/2023	AMENDED COMPLAINT (Second) against Charter Communications, Inc., filed by Entropic Communications, LLC. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I, # 10 Exhibit J, # 11 Exhibit K, # 12 Exhibit L, # 13 Exhibit M, # 14 Exhibit N)(Hill, Jack Wesley) (Entered: 01/10/2023)	
54	01/10/2023	SEALED RESPONSE to Motion re 18 MOTION to Dismiss For Improper Venue Pursuant to FRCP 12(b)(3) filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of M. Blair, # 2 Exhibit A to Blair Declaration, # 3 Exhibit B to Blair Declaration, # 4 Exhibit C to Blair Declaration, # 5 Exhibit D to Blair Declaration, # 6 Exhibit E to Blair Declaration, # 7 Exhibit F to Blair Declaration, # 8 Exhibit G to Blair Declaration, # 9 Exhibit H to Blair Declaration, # 10 Exhibit I to Blair Declaration, # 11 Exhibit J to Blair Declaration, # 12 Exhibit K to Blair Declaration, # 13 Exhibit L to Blair Declaration, # 14 Exhibit M to Blair Declaration, # 15 Exhibit N to Blair Declaration, # 16 Exhibit O to Blair Declaration, # 17 Exhibit P to Blair Declaration, # 18 Exhibit Q to Blair Declaration, # 19 Exhibit R to Blair Declaration, # 20 Exhibit S to Blair Declaration, # 21 Exhibit T to Blair Declaration, # 22 Exhibit U to Blair Declaration, # 23 Exhibit V to Blair Declaration, # 24 Exhibit W to Blair Declaration, # 25 Exhibit X to Blair Declaration, # 26 Exhibit Y to Blair Declaration, # 27 Text of Proposed Order proposed order)(Hill, Jack Wesley) (Entered: 01/10/2023)	
55	01/17/2023	REPLY to Response to Motion re 18 MOTION to Dismiss For	

#	Date	Proceeding Text	Source
		Improper Venue Pursuant to FRCP 12(b)(3) filed by Charter Communications, Inc., Spectrum Advanced Services, LLC, Spectrum Management Holding Company, LLC. (Long, Elizabeth) (Entered: 01/17/2023)	
56	01/18/2023	REDACTION to 54 Sealed Response to Motion,.., by Entropic Communications, LLC. (Attachments: # 1 Declaration of M. Blair, # 2 Exhibit A through E to Blair Declaration (Sealed in Entirety), # 3 Exhibit F to Blair Declaration, # 4 Exhibit G through H to Blair Declaration (Sealed in Entirety), # 5 Exhibit I to Blair Declaration, # 6 Exhibit J to Blair Declaration, # 7 Exhibit K to Blair Declaration, # 8 Exhibit L to Blair Declaration, # 9 Exhibit M to Blair Declaration, # 10 Exhibit N to Blair Declaration, # 11 Exhibit O to Blair Declaration, # 12 Exhibit P to Blair Declaration, # 13 Exhibit Q to Blair Declaration, # 14 Exhibit R to Blair Declaration, # 15 Exhibit S to Blair Declaration, # 16 Exhibit T to Blair Declaration, # 17 Exhibit U to Blair Declaration, # 18 Exhibit V to Blair Declaration, # 19 Exhibit W to Blair Declaration, # 20 Exhibit X to Blair Declaration, # 21 Exhibit Y to Blair Declaration (Sealed in Entirety), # 22 Text of Proposed Order proposed order)(Hill, Jack Wesley) (Entered: 01/18/2023)	
57	01/19/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Melissa A. Brown on behalf of All Defendants. Filing fee $ 100, receipt number ATXEDC-9315923. (Brown, Melissa) (Entered: 01/19/2023)	
58	01/23/2023	Unopposed MOTION for Extension of Time to File Answer re 53 Amended Complaint, by Charter Communications, Inc.. (Attachments: # 1 Text of Proposed Order)(Dacus, Deron) (Entered: 01/23/2023)	
59	01/25/2023	ORDER granting 58 Unopposed MOTION for Extension of Time to File Answer re 53 Amended Complaint. Charter Communications, Inc. answer due 1/30/2023.. Signed by District Judge Rodney Gilstrap on 1/25/2023. (ch,) (Entered: 01/25/2023)	
60	01/27/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Kenneth H. Bridges on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9330960. (Bridges, Kenneth) (Entered: 01/27/2023)	
61	01/30/2023	SEALED MOTION to Dismiss by Charter Communications, Inc.. (Attachments: # 1 Text of Proposed Order, # 2 Declaration, # 3 Exhibit 1, # 4 Exhibit 2, # 5 Exhibit 3, # 6 Exhibit 4, # 7 Exhibit 5, # 8 Exhibit 6, # 9 Exhibit 7, # 10 Exhibit 8, # 11 Exhibit 9, # 12 Exhibit 10, # 13 Exhibit 11, # 14 Exhibit 12)(Dacus, Deron) (Entered: 01/30/2023)	
62	02/06/2023	REDACTION to 61 SEALED MOTION to Dismiss by Charter Communications, Inc.. (Attachments: # 1 Text of Proposed Order, # 2 Declaration, # 3 Exhibit 1, # 4 Exhibit 2, # 5 Exhibit 3, # 6 Exhibit 4, # 7 Exhibit 5, # 8 Exhibit 6, # 9 Exhibit 7-12)(Dacus, Deron) (Entered: 02/06/2023)	
63	02/06/2023	STIPULATION of Dismissal by Charter Communications, Inc.. (Dacus, Deron) (Entered: 02/06/2023)	
64	02/06/2023	Unopposed MOTION Motion to Amend Case Caption re 63 Stipulation of Dismissal by Charter Communications, Inc.. (Attachments: # 1 Text of Proposed Order)(Dacus, Deron) (Entered: 02/06/2023)	
65	02/07/2023	ORDER re 63 Stipulation of Dismissal without prejudice as too Spectrum Advanced Services, LLC and Spectrum Management Holding Company, LLC. Signed by District Judge Rodney Gilstrap on 2/7/2023. (ch,) (Entered: 02/07/2023)	
66	02/08/2023	Unopposed MOTION for Extension of Time to File Response/Reply as to 61 SEALED MOTION to Dismiss by	

#	Date	Proceeding Text	Source
		Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Fair, Andrea) (Entered: 02/08/2023)	
67	02/10/2023	ORDER granting 66 Unopposed MOTION for Extension of Time to File Response/Reply as to 61 SEALED MOTION to Dismiss . 61 SEALED MOTION to Dismiss Responses due by 2/20/2023. Signed by District Judge Rodney Gilstrap on 02/10/2023. (klc,) (Entered: 02/10/2023)	
68	02/21/2023	SEALED RESPONSE to Motion re 61 SEALED MOTION to Dismiss filed by Entropic Communications, LLC. (Attachments: # 1 Affidavit Declaration of M. Blair, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L, # 14 Exhibit M, # 15 Exhibit N, # 16 Exhibit O, # 17 Exhibit P, # 18 Exhibit Q, # 19 Exhibit R, # 20 Exhibit S, # 21 Exhibit T, # 22 Exhibit U, # 23 Exhibit V, # 24 Exhibit W, # 25 Exhibit X, # 26 Exhibit Y, # 27 Exhibit Z, # 28 Exhibit AA, # 29 Exhibit AB, # 30 Exhibit AC, # 31 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 02/21/2023)	
69	02/27/2023	Unopposed MOTION for Extension of Time to File by Charter Communications, Inc.. (Attachments: # 1 Text of Proposed Order)(Dacus, Deron) (Entered: 02/27/2023)	
70	02/28/2023	REDACTION to 68 Sealed Response to Motion,, by Entropic Communications, LLC. (Attachments: # 1 Affidavit Declaration of M. Blair, # 2 Exhibit A-E, # 3 Exhibit F, # 4 Exhibit G-H, # 5 Exhibit I, # 6 Exhibit J, # 7 Exhibit K, # 8 Exhibit L, # 9 Exhibit M, # 10 Exhibit N, # 11 Exhibit O, # 12 Exhibit P, # 13 Exhibit Q, # 14 Exhibit R, # 15 Exhibit S, # 16 Exhibit T, # 17 Exhibit U, # 18 Exhibit V, # 19 Exhibit W, # 20 Exhibit X, # 21 Exhibit Y-AB, # 22 Exhibit AC, # 23 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 02/28/2023)	
71	02/28/2023	ORDER granting 69 Motion for Extension of Time to File Reply. Signed by District Judge Rodney Gilstrap on 2/28/2023. (ch,) (Entered: 02/28/2023)	
72	02/28/2023	Agreed MOTION to Amend/Correct 40 Order on Motion for Miscellaneous Relief by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Fair, Andrea) (Entered: 02/28/2023)	
73	03/02/2023	SECOND AMENDED DOCKET CONTROL ORDER granting 72 Agreed MOTION to Amend/Correct 40 Order on Motion for Miscellaneous Relief. Signed by District Judge Rodney Gilstrap on 3/2/2023. (ch,) (Entered: 03/02/2023)	
74	03/06/2023	Sealed Document. SUPPLEMENT re 68 SEALED RESPONSE to Motion re 61 SEALED MOTION to Dismiss filed by Entropic Communications, LLC. (Hill, Jack Wesley) (Entered: 03/06/2023)	
75	03/09/2023	SEALED REPLY to Response to Motion re 61 SEALED MOTION to Dismiss filed by Charter Communications, Inc.. (Attachments: # 1 Declaration, # 2 Exhibit 13, # 3 Exhibit 14)(Dacus, Deron) (Entered: 03/09/2023)	
76	03/13/2023	REDACTION to 74 Sealed Document by Entropic Communications, LLC. (Hill, Jack Wesley) (Entered: 03/13/2023)	
77	03/13/2023	Unopposed MOTION for Extension of Time to File Response/Reply as to 61 SEALED MOTION to Dismiss (to File Sur-Reply) by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 03/13/2023)	
78	03/15/2023	ORDER granting 77 Unopposed MOTION for Extension of Time to File Response/Reply as to 61 SEALED MOTION to Dismiss (to File Sur-Reply), 61 SEALED MOTION to Dismiss Responses due by 3/23/2023. Signed by District Judge Rodney Gilstrap on 3/15/2023. (ch,) (Entered: 03/16/2023)	

#	Date	Proceeding Text	Source
79	03/16/2023	REDACTION to 75 Sealed Reply to Response to Motion re 61 Motion to Dismiss filed by Charter Communications, Inc.. (Attachments: # 1 Declaration, # 2 Exhibit 13, # 3 Exhibit 14)(Brown, Melissa) (Entered: 03/16/2023)	
80	03/23/2023	SEALED SUR-REPLY to Reply to Response to Motion re 61 SEALED MOTION to Dismiss filed by Entropic Communications, LLC. (Hill, Jack Wesley) (Entered: 03/23/2023)	
81	03/29/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Katherine L. Allor on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9426592. (Allor, Katherine) (Entered: 03/29/2023)	
82	03/29/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Peter E. Soskin on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9426688. (Soskin, Peter) (Entered: 03/29/2023)	
83	04/03/2023	REDACTION to 80 Sealed Sur-Reply to Reply to Response to Motion by Entropic Communications, LLC. (Hill, Jack Wesley) (Entered: 04/03/2023)	
84	04/04/2023	Sealed Document. Joint Claim Construction and Pre-Hearing Statement (P.R. 4-3) (Shimota, James) (Entered: 04/04/2023)	
85	04/05/2023	NOTICE by Charter Communications, Inc. of Service of Expert Witness Disclosures Pursuant to PR 4-3(b) (Dacus, Deron) (Entered: 04/05/2023)	
86	04/12/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Samuel Patrick Richey on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9448177. (Richey, Samuel) (Entered: 04/12/2023)	
87	04/14/2023	***WITHDRAWN PER ORDER #94*** SEALED MOTION to Disqualify Cathleen Quigley by Entropic Communications, LLC. (Attachments: # 1 Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Text of Proposed Order)(Shimota, James) Modified on 5/9/2023 (ch,). (Entered: 04/14/2023)	
88	04/19/2023	Agreed MOTION to Amend/Correct Docket Control Order by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Fair, Andrea) (Entered: 04/19/2023)	
89	04/20/2023	AMENDED DOCKET CONTROL ORDER granting 88 Agreed MOTION to Amend/Correct Docket Control Order. Signed by District Judge Rodney Gilstrap on 4/20/2023. (ch,) (Entered: 04/21/2023)	
90	04/27/2023	Unopposed MOTION for Extension of Time to File Response/Reply as to 87 SEALED MOTION to Disqualify Cathleen Quigley by Charter Communications, Inc.. (Attachments: # 1 Text of Proposed Order)(Brown, Melissa) (Entered: 04/27/2023)	
92	05/05/2023	Unopposed MOTION to Withdraw 87 SEALED MOTION to Disqualify Cathleen Quigley by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Hill, Jack Wesley) (Entered: 05/05/2023)	
93	05/05/2023	ORDER granting 90 Unopposed MOTION for Extension of Time to File Response/Reply as to 87 SEALED MOTION to Disqualify Cathleen Quigley , 87 SEALED MOTION to Disqualify Cathleen Quigley Responses due by 5/5/2023. Signed by District Judge Rodney Gilstrap on 5/5/2023. (ch,) (Entered: 05/08/2023)	
94	05/08/2023	ORDER granting 92 Motion to Withdraw 87 SEALED MOTION to Disqualify >. Signed by District Judge Rodney Gilstrap on 5/8/2023. (ch,) (Entered: 05/09/2023)	
95	05/09/2023	NOTICE by Entropic Communications, LLC of Compliance	

#	Date	Proceeding Text	Source
		Regarding Technical Tutorial (Fair, Andrea) (Entered: 05/09/2023)	
96	05/09/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Amy L DeWitt on behalf of Charter Communications, Inc.. Filing fee $ 100, receipt number ATXEDC-9490163. (DeWitt, Amy) (Entered: 05/09/2023)	
97	05/09/2023	PLAINTIFF'S OPENING CLAIM CONSTRUCTION BRIEF filed by Entropic Communications, LLC. (Attachments: # 1 Exhibit 1 - U.S. Patent No. 8,223,775, # 2 Exhibit 2 - U.S. Patent No. 8,792,008, # 3 Exhibit 3 - U.S. Patent No. 9,825,826, # 4 Exhibit 4 - U.S. Patent No. 8,284,690, # 5 Exhibit 5 - U.S. Patent No. 9,210,362, # 6 Exhibit 6 - U.S. Patent No. 10,135,682, # 7 Exhibit 7 - Rebuttal Declaration of Richard A. Kramer, # 8 Exhibit 8 - Declaration of Dr. Kevin Almeroth, # 9 Exhibit 9 - Almeroth Condensed Deposition Transcript, # 10 Exhibit 10 - IEEE Dictionary, # 11 Exhibit 11 - Email from A. Boardman)(Fair, Andrea) (Entered: 05/09/2023)	
98	05/10/2023	NOTICE by Charter Communications, Inc. - Joint Notice of Redaction of Docket 91 - (Attachments: # 1 Exhibit 1 - Redacted Order, dated May 3, 2023 to the docket in 22-cv-125 (ED Tex))(Brown, Melissa) (Entered: 05/10/2023)	
99	05/11/2023	Opposed MOTION TO CONSOLIDATE THIS ACTION WITH NO. 2:23-CV-00052-JRG AND TO AMEND THE CASE SCHEDULE by Charter Communications, Inc.. (Attachments: # 1 Ex 1 - Proposed Consolidated Order, # 2 Ex 2 - Claim Charts, # 3 Text of Proposed Order)(Reisner, Daniel) (Entered: 05/11/2023)	
100	05/11/2023	ORDER - Court hereby appoints David Keyzer as the Courts technical advisor. Signed by District Judge Rodney Gilstrap on 5/11/2023. (ch,) (Entered: 05/12/2023)	
101	05/17/2023	Sealed Document. Defendant's Answer to Second Amended Complaint (Dacus, Deron) (Entered: 05/17/2023)	
102	05/17/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Courtney Neufeld on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9505527. (Neufeld, Courtney) (Entered: 05/17/2023)	
103	05/18/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Connor James Meggs on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9506343. (Meggs, Connor) (Entered: 05/18/2023)	
104	05/23/2023	REPLY to 97 Claim Construction Brief,. filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Albert Boardman in Support of Charter's Responsive Claim Construction Brief, # 2 Exhibit 1, # 3 Exhibit 2, # 4 Exhibit 3, # 5 Exhibit 4, # 6 Exhibit 5)(Long, Elizabeth) (Entered: 05/23/2023)	
105	05/24/2023	REDACTION to 101 Sealed Document Answer by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 05/24/2023)	
106	05/25/2023	FILED IN ERROR PER ATTORNEY Unopposed MOTION for Extension of Time to File Response/Reply as to 99 Opposed MOTION TO CONSOLIDATE THIS ACTION WITH NO. 2:23-CV-00052-JRG AND TO AMEND THE CASE SCHEDULE by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Hill, Jack Wesley) Modified on 5/25/2023 (nkl,). (Entered: 05/25/2023)	
	05/25/2023	***FILED IN ERROR PER ATTORNEY. Document # 106, Unopposed MOTION for Extension of Time to File Response/Reply. PLEASE IGNORE.*** (nkl,) (Entered: 05/25/2023)	
107	05/25/2023	NOTICE by Charter Communications, Inc. of its Designation of Daniel L. Reisner as Lead Counsel (Long, Elizabeth) (Entered: 05/25/2023)	

#	Date	Proceeding Text	Source
108	05/26/2023	Unopposed MOTION for Leave to Supplement Infringement Contentions by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Fair, Andrea) (Entered: 05/26/2023)	
109	05/26/2023	Unopposed MOTION for Extension of Time to File Response/Reply as to 99 Opposed MOTION TO CONSOLIDATE THIS ACTION WITH NO. 2:23-CV-00052-JRG AND TO AMEND THE CASE SCHEDULE by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Hill, Jack Wesley) (Entered: 05/26/2023)	
110	05/30/2023	PLAINTIFF'S REPLY CLAIM CONSTRUCTION BRIEF filed by Entropic Communications, LLC. (Attachments: # 1 Exhibit 12 - U.S. Patent Publication No. 2021/0337543, # 2 Exhibit 13 - Newtons Telecom Dictionary Excerpt, # 3 Exhibit 14 - Microsoft Computer Dictionary Excerpt, # 4 Exhibit 15 - Entropic's Technology Tutorial Slides)(Shimota, James) (Entered: 05/30/2023)	
111	05/31/2023	ORDER Before the Court is Plaintiff's Unopposed Motion for Leave to Supplement Infringement Contentions filed by Entropic Communications LLC. (Dkt. No. 109 .) In the Motion, Entropic requests leave to supplement its infringement contentions. (Id. at 1.) Entropic served its supplemental infringement contentions on March 10, 2023. (Id.) The Motion is unopposed. (Id. at 1, 3) Having considered the Motion, and noting its unopposed nature, the Court finds that it should be and hereby is GRANTED. Accordingly, the Court ORDERS that Entropic is granted leave to supplement its infringement contentions as requested. Signed by District Judge Rodney Gilstrap on 5/30/2023. (psm) (Entered: 05/31/2023)	
112	05/31/2023	ORDER Before the Court is the Unopposed Motion for Extension of Time to Respond to Charter's Motion to Consolidate filed by Plaintiff Entropic Communications, LLC. (Dkt. No. 109 .) In the Motion, Entropic requests an extension of time to file a response in opposition to Defendant Charter Communications, Inc.'s Motion to Consolidate and Amend the Case Schedule (Dkt. No. 99). (Id. at 1.) The requested extension would move the deadline for Entropic to file its opposition up to and including May 31, 2023. (Id.) The Motion is unopposed. (Id. at 1, 3.) Having considered the Motion, and noting its unopposed nature, the Court finds that it should be and hereby is GRANTED. Accordingly, the Court ORDERS that the deadline for Entropic to file a response to the Motion to Consolidate is extended up to and including May 31, 2023. Signed by District Judge Rodney Gilstrap on 5/30/2023. (psm) (Entered: 05/31/2023)	
113	05/31/2023	RESPONSE in Opposition re 99 Opposed MOTION TO CONSOLIDATE THIS ACTION WITH NO. 2:23-CV-00052-JRG AND TO AMEND THE CASE SCHEDULE filed by Entropic Communications, LLC. (Attachments: # 1 Proposed Order Proposed Order)(Hill, Jack Wesley) (Entered: 05/31/2023)	
114	06/02/2023	P.R. 4-5(d) Joint Claim Construction Chart by Charter Communications, Inc.. (Attachments: # 1 Exhibit A(Long, Elizabeth) (Entered: 06/02/2023)	
115	06/06/2023	Amended P.R. 4-5(d) Joint Claim Construction Chart by Charter Communications, Inc.. (Attachments: # 1 Exhibit A)(Long, Elizabeth) (Entered: 06/06/2023)	
116	06/08/2023	REPLY to Response to Motion re 99 Opposed MOTION TO CONSOLIDATE THIS ACTION WITH NO. 2:23-CV-00052-JRG AND TO AMEND THE CASE SCHEDULE filed by Charter Communications, Inc.. (Attachments: # 1 Declaration of Daniel Reisner)(Brown, Melissa) (Entered: 06/08/2023)	

#	Date	Proceeding Text	Source
117	06/12/2023	NOTICE by Entropic Communications, LLC re 97 Claim Construction Brief,, Corrected Exhibit 7 (ECF No. 97-7) (Attachments: # 1 Exhibit Corrected Exhibit 7)(Hill, Jack Wesley) (Entered: 06/12/2023)	
118	06/13/2023	Minute Entry for proceedings held before District Judge Rodney Gilstrap: Markman Hearing held on 6/13/2023. (from 09:02 AM to 12:49 PM) (Court Reporter Shelly Holmes) (Attachments: # 1 Attorney Attendance Sheet) (aeb) (Entered: 06/13/2023)	
119	06/15/2023	SUR-REPLY to Reply to Response to Motion re 99 Opposed MOTION TO CONSOLIDATE THIS ACTION WITH NO. 2:23-CV-00052-JRG AND TO AMEND THE CASE SCHEDULE filed by Entropic Communications, LLC. (Attachments: # 1 Exhibit A - Declaration of James Shimota)(Shimota, James) (Entered: 06/15/2023)	
120	06/21/2023	USCA FEDERAL CIRCUIT - ORDER filed directing Entropic Communications, LLC to respond to the petition no later than seven days from the date of filing of this order. Any reply in support of the petition is due no later than three days thereafter (23-136) (ch,) (Entered: 06/21/2023)	
121	06/22/2023	NOTICE of Attorney Appearance by Paul Isaac Margulies on behalf of Charter Communications, Inc. (Margulies, Paul) (Entered: 06/22/2023)	
122	06/23/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Marc A Cohn on behalf of Charter Communications, Inc.. Filing fee $ 100, receipt number ATXEDC-9566636. (Cohn, Marc) (Entered: 06/23/2023)	
123	06/26/2023	CLAIM CONSTRUCTION MEMORANDUM OPINION AND ORDER. Signed by District Judge Rodney Gilstrap on 6/26/2023. (ch,) (Entered: 06/26/2023)	
124	06/27/2023	NOTICE of Attorney Appearance by Jacob Michael Bass on behalf of Charter Communications, Inc. (Bass, Jacob) (Entered: 06/27/2023)	
125	06/27/2023	NOTICE OF FILING OF OFFICIAL TRANSCRIPT of Proceedings held on 3/13/23 (Claim Construction Hearing) before Judge Rodney Gilstrap. Court Reporter/Transcriber: Shelly Holmes, CSR, TCRR,Telephone number: (903) 794-1018 (Shelly_Holmes@txed.uscourts.gov). NOTICE RE REDACTION OF TRANSCRIPTS: The parties have seven (7) days to file with the Court a Notice of Intent to Request Redaction of this transcript. If no such Notice is filed, the transcript will be made remotely electronically available to the public without redaction after 90 calendar days. The policy is located on our website at www.txed.uscourts.gov Transcript may be viewed at the court public terminal or purchased through the Court Reporter/Transcriber before the deadline for Release of Transcript Restriction. After that date it may be obtained through PACER.. Motion to Redact due 7/18/2023. Release of Transcript Restriction set for 9/25/2023. (Holmes, Shelly) (Entered: 06/27/2023)	
126	07/05/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Ketajh Brown on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9583870. (Brown, Ketajh) (Entered: 07/05/2023)	
127	07/06/2023	NOTICE of Attorney Appearance - Pro Hac Vice by David Eric Shapland on behalf of Charter Communications, Inc.. Filing fee $ 100, receipt number ATXEDC-9585909. (Shapland, David) (Entered: 07/06/2023)	
128	07/10/2023	PAPER TRANSCRIPT REQUEST by Charter Communications, Inc. for proceedings held on 6-13-23- Claim Construction Hearing before Judge Gilstrap. (Dacus, Deron) (Main Document 128	

#	Date	Proceeding Text	Source
		replaced with flattened image on 7/10/2023) (ch,). (forwarded to Shelly Holmes) Modified on 7/10/2023 (ch,). (Entered: 07/10/2023)	
129	07/10/2023	ORDER - Court has received Mr. Keyzers invoice for services through June 27, 2023, court hereby ORDERS payment to be promptly made as follows. Signed by District Judge Rodney Gilstrap on 7/10/2023. (ch,) (Entered: 07/10/2023)	
130	07/11/2023	***WITHDRAWN PER #140**Unopposed SEALED MOTION to Compel Responses to Interrogatories 8, 16, 23, and 29 by Charter Communications, Inc.. (Attachments: # 1 Proposed Order)(Long, Elizabeth) Modified on 7/28/2023 (ch,). (Entered: 07/11/2023)	
131	07/12/2023	Joint MOTION for Leave to Supplement Contentions by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Hill, Jack Wesley) (Entered: 07/12/2023)	
132	07/13/2023	ORDER granting 131 Joint MOTION for Leave to Supplement Contentions. Signed by District Judge Rodney Gilstrap on 7/13/2023. (ch,) (Entered: 07/14/2023)	
133	07/14/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Christina N Goodrich on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9600975. (Goodrich, Christina) (Entered: 07/14/2023)	
134	07/18/2023	REDACTION to 130 Unopposed SEALED MOTION to Compel Responses to Interrogatories 8, 16, 23, and 29 by Charter Communications, Inc.. (Attachments: # 1 Proposed Order)(Brown, Melissa) (Entered: 07/18/2023)	
135	07/21/2023	SEALED MOTION for Leave to Supplement Infringement Contentions by Entropic Communications, LLC. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Proposed Order)(Shimota, James) (Entered: 07/21/2023)	
136	07/21/2023	Joint MOTION for Extension of Time to Complete Discovery (Joint Motion to Complete Limited Fact Discovery Out of Time) by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Shimota, James) (Entered: 07/21/2023)	
137	07/24/2023	NOTICE of Attorney Appearance by Charles Everingham, IV on behalf of Entropic Communications, LLC (Everingham, Charles) (Entered: 07/24/2023)	
138	07/25/2023	ORDER granting 136 Joint MOTION for Extension of Time to Complete Discovery (Joint Motion to Complete Limited Fact Discovery Out of Time). Signed by District Judge Rodney Gilstrap on 7/25/2023. (ch,) (Entered: 07/25/2023)	
139	07/27/2023	Unopposed MOTION to Withdraw 130 Unopposed SEALED MOTION to Compel Responses to Interrogatories 8, 16, 23, and 29 by Charter Communications, Inc.. (Attachments: # 1 Proposed Order)(Long, Elizabeth) (Entered: 07/27/2023)	
140	07/28/2023	ORDER granting 139 Motion to Withdraw 130 Unopposed SEALED MOTION to Compel Responses to Interrogatories 8, 16, 23, and 29 . Signed by District Judge Rodney Gilstrap on 7/28/2023. (ch,) (Entered: 07/28/2023)	
141	07/28/2023	SEALED MOTION to Strike the Expert Report of David O. Taylor by Entropic Communications, LLC. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Proposed Order)(Shimota, James) (Entered: 07/28/2023)	
142	07/31/2023	REDACTION to 87 SEALED MOTION to Disqualify Cathleen Quigley by Entropic Communications, LLC. (Attachments: # 1 Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Proposed Order)(Shimota, James) (Entered: 07/31/2023)	
143	08/07/2023	SEALED RESPONSE to Motion re 135 SEALED MOTION for	

#	Date	Proceeding Text	Source
		Leave to Supplement Infringement Contentions filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration Declaration of Paul Margulies, # 2 Exhibit 1, # 3 Exhibit 2, # 4 Exhibit 3, # 5 Exhibit 4, # 6 Exhibit 5, # 7 Exhibit 6)(Margulies, Paul) (Entered: 08/07/2023)	
144	08/11/2023	SEALED RESPONSE to Motion re 141 SEALED MOTION to Strike the Expert Report of David O. Taylor filed by Charter Communications, Inc. (Long, Elizabeth) (Entered: 08/11/2023)	
145	08/14/2023	Joint MOTION for Leave to File Supplement Expert Reports by Charter Communications, Inc.. (Attachments: # 1 Proposed Order)(Long, Elizabeth) (Entered: 08/14/2023)	
146	08/14/2023	REDACTION to 143 Sealed Response to Motion, by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Paul Margulies, # 2 Exhibit 1-6)(Brown, Melissa) (Entered: 08/14/2023)	
147	08/14/2023	SEALED REPLY to Response to Motion re 135 SEALED MOTION for Leave to Supplement Infringement Contentions filed by Entropic Communications, LLC. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D)(Shimota, James) (Entered: 08/14/2023)	
148	08/15/2023	ORDER granting 145 Joint MOTION for Leave to File Supplement Expert Reports. Signed by District Judge Rodney Gilstrap on 8/15/2023. (ch,) (Entered: 08/16/2023)	
149	08/17/2023	REDACTION to 135 SEALED MOTION for Leave to Supplement Infringement Contentions by Entropic Communications, LLC. (Shimota, James) (Entered: 08/17/2023)	
150	08/18/2023	REDACTION to 144 Sealed Response to Motion DEFENDANT CHARTER COMMUNICATIONS, INC.'S OPPOSITION TO PLAINTIFFS MOTION TO STRIKE THE EXPERT REPORT OF DAVID O. TAYLOR by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 08/18/2023)	
151	08/18/2023	SEALED REPLY to Response to Motion re 141 SEALED MOTION to Strike the Expert Report of David O. Taylor filed by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of Jim Shimota, # 2 Exhibit A)(Shimota, James) (Entered: 08/18/2023)	
152	08/22/2023	SEALED SUR-REPLY to Reply to Response to Motion re 135 SEALED MOTION for Leave to Supplement Infringement Contentions filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Paul Margulies, # 2 Exhibit 7, # 3 Exhibit 8, # 4 Exhibit 9)(Margulies, Paul) (Entered: 08/22/2023)	
153	08/23/2023	Agreed MOTION to Amend/Correct Docket Control Order by Entropic Communications, LLC. (Attachments: # 1 Text of Proposed Order)(Shimota, James) (Entered: 08/23/2023)	
154	08/25/2023	ORDER granting 153 Motion to Amend/Correct. Signed by District Judge Rodney Gilstrap on 8/24/23. (bga) (Entered: 08/25/2023)	
155	08/28/2023	SEALED RESPONSE by Charter Communications, Inc. to 151 Sealed Reply to Response to Motion filed by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 08/28/2023)	
156	08/29/2023	REDACTION to 152 Sealed Sur-Reply to Reply to Response to Motion, by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Paul Margulies, # 2 Exhibit 7, # 3 Exhibit 8, # 4 Exhibit 9)(Brown, Melissa) (Entered: 08/29/2023)	
157	08/29/2023	MEMORANDUM OPINION AND ORDER - denying 99 . Signed by District Judge Rodney Gilstrap on 8/29/2023. (ch,) (Entered: 08/30/2023)	
158	08/29/2023	MEMORANDUM OPINION AND ORDER - denying 135 Motion for Leave to Supplement Infringement Contentions. Signed by District	

#	Date	Proceeding Text	Source
		Judge Rodney Gilstrap on 8/29/2023. (ch,) (Entered: 08/30/2023)	
159	08/31/2023	Unopposed SEALED MOTION Motion for Leave to Take Third-Party Deposition of Vantiva USA LLC by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota In Support Of Motion for Leave, # 2 Exhibit A to Shimota Declaration, # 3 Exhibit B to Shimota Declaration, # 4 Exhibit C to Shimota Declaration, # 5 Exhibit D to Shimota Declaration, # 6 Exhibit E to Shimota Declaration, # 7 Proposed Order)(Shimota, James) (Entered: 08/31/2023)	
160	09/01/2023	ORDER granting 159 Sealed Motion. Signed by District Judge Rodney Gilstrap on 09/01/2023. (klc,) (Entered: 09/01/2023)	
161	09/05/2023	ORDER USCA FEDERAL CIRCUIT - filed denying 2 Petition for Writ of Mandamus filed by Charter Communications, Inc (23-136) (ch,) (Entered: 09/05/2023)	
162	09/05/2023	REDACTION to 155 Response to Non-Motion Defendant Charter Communications, Inc.'s Sur-Reply in Further Opposition to Plaintiff's Motion to Strike the Expert Report of David O. Taylor by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 09/05/2023)	
163	09/07/2023	NOTICE of Designation of Mediator, Gary McGowan, filed by Entropic Communications, LLC. (Hill, Jack Wesley) (Entered: 09/07/2023)	
164	09/07/2023	AGREED MOTION to Amend/Correct Docket Control Order by Charter Communications, Inc.. (Attachments: # 1 Proposed Order)(Long, Elizabeth) (Entered: 09/07/2023)	
165	09/10/2023	FIFTH AMENDED DOCKET CONTROL ORDER granting 164 AGREED MOTION to Amend/Correct Docket Control Order. Signed by District Judge Rodney Gilstrap on 9/10/2023. (ch,) (Entered: 09/11/2023)	
166	09/11/2023	SEALED MOTION CHARTER'S MOTION TO STRIKE DR. SOURI'S IMPROPER OPINIONS by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration Declaration of E. Long ISO Charter's Motion to Strike Dr. Souri's Improper Opinions, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Proposed Order)(Long, Elizabeth) (Entered: 09/11/2023)	
167	09/11/2023	SEALED MOTION CHARTER'S MOTION TO STRIKE DR. KRAMER'S IMPROPER OPINIONS by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration Declaration of Elizabeth Long In Support of Charter's Motion to Strike Dr. Kramer's Improper Opinions, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Proposed Order)(Long, Elizabeth) (Entered: 09/11/2023)	
168	09/11/2023	MOTION to Strike Opinions of Steven Goldberg by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of Jim Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Proposed Order)(Shimota, James) (Entered: 09/11/2023)	
169	09/11/2023	SEALED MOTION CHARTER'S MOTION TO EXCLUDE THE EXPERT OPINIONS OF STEPHEN DELL by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration Declaration of Elizabeth Long In Support of Charter's Motion to Exclude The Expert Opinions of Stephen Dell, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Proposed Order)(Long, Elizabeth) (Entered: 09/11/2023)	
170	09/11/2023	MOTION for Summary Judgment Of No Invalidity Under 32 U.S.C. 102 & 103 by Entropic Communications, LLC. (Attachments: # 1	

#	Date	Proceeding Text	Source
		Affidavit/Declaration of Jim Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Proposed Order)(Shimota, James) (Entered: 09/11/2023)	
171	09/11/2023	SEALED MOTION CHARTER'S MOTION TO STRIKE ENTROPIC'S IMPROPER SECONDARY CONSIDERATIONS POSITIONS by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration Declaration of Elizabeth Long In Support of Charter's Motion to Strike Entropic's Improper Secondary Considerations Positions, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Proposed Order)(Long, Elizabeth) (Entered: 09/11/2023)	
172	09/11/2023	SEALED MOTION (CHARTER'S MOTION FOR PARTIAL SUMMARY JUDGMENT OF NO PRE-SUIT DAMAGES) by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Elizabeth Long In Support of Charter's Motion for Partial Summary Judgment of No Pre-Suit Damage, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L, # 14 Exhibit M, # 15 Exhibit N, # 16 Exhibit O, # 17 Exhibit P, # 18 Proposed Order)(Long, Elizabeth) (Entered: 09/11/2023)	
173	09/11/2023	SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT) by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Elizabeth Long In Support of Charter's Motion for Partial Summary Judgment of No Pre-Suit Damage, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Proposed Order)(Long, Elizabeth) (Entered: 09/11/2023)	
174	09/11/2023	SEALED MOTION to Strike Opinions of Christopher Bakewell by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L, # 14 Exhibit M, # 15 Exhibit N, # 16 Exhibit O, # 17 Exhibit P, # 18 Exhibit Q, # 19 Exhibit R, # 20 Exhibit S, # 21 Exhibit T, # 22 Exhibit U, # 23 Exhibit V, # 24 Exhibit W, # 25 Exhibit X, # 26 Exhibit Y, # 27 Exhibit Z, # 28 Exhibit AA, # 29 Exhibit AB, # 30 Exhibit AC, # 31 Affidavit/Declaration of Darlene Ghavimi, # 32 Exhibit A - to Ghavimi Declaration)(Shimota, James) (Additional attachment(s) added on 9/12/2023: # 33 Proposed Order) (nkl,). (Entered: 09/11/2023)	
175	09/11/2023	SEALED MOTION to Strike Opinions of Dr. Kevin Almeroth by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Proposed Order)(Shimota, James) (Entered: 09/11/2023)	
176	09/11/2023	SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF THE ASSERTED CLAIMS OF THE '682 AND '690 PATENTS) by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration OF ELIZABETH LONG IN SUPPORT OF CHARTER'S MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF THE ASSERTED CLAIMS OF THE '682 AND '690 PATENTS, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L, # 14 Exhibit M, # 15	

#	Date	Proceeding Text	Source
		Exhibit N, # 16 Exhibit O, # 17 Exhibit P, # 18 Exhibit Q, # 19 Exhibit R, # 20 Exhibit S, # 21 Exhibit T, # 22 Exhibit U, # 23 Exhibit V, # 24 Proposed Order)(Long, Elizabeth) (Entered: 09/11/2023)	
177	09/11/2023	SEALED MOTION for Summary Judgment of No License Defense Based on DOCSIS by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Proposed Order)(Shimota, James) (Entered: 09/11/2023)	
178	09/12/2023	Filed in Error. Attorney to Refile MOTION for Summary Judgment for Summary Judgment of No License Defense Based on DOCSIS by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Proposed Order)(Shimota, James) Modified on 9/12/2023 (klc,). (Entered: 09/12/2023)	
179	09/12/2023	SEALED MOTION of Partial Summary Judgment That Devices With MaxLinear Chips are Not Non-Infringing Alternatives Affecting the Reasonable Royalty Rate by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Proposed Order)(Shimota, James) (Entered: 09/12/2023)	
180	09/12/2023	SEALED MOTION for Summary Judgment of No Unclean Hands Defense by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Proposed Order)(Shimota, James) (Entered: 09/12/2023)	
181	09/12/2023	MOTION for Summary Judgment of Validity Under 35 U.S.C. 101 (CORRECTION OF ECF DOCUMENT TITLE) by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Proposed Order)(Shimota, James) (Entered: 09/12/2023)	
182	09/18/2023	AGREED MOTION to Amend/Correct 165 Order on Motion to Amend/Correct Docket Control Order by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Shimota, James) (Entered: 09/18/2023)	
183	09/18/2023	REDACTION to 166 SEALED MOTION CHARTER'S MOTION TO STRIKE DR. SOURI'S IMPROPER OPINIONS by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Proposed Order)(Long, Elizabeth) (Entered: 09/18/2023)	
184	09/18/2023	REDACTION to 167 SEALED MOTION CHARTER'S MOTION TO STRIKE DR. KRAMER'S IMPROPER OPINIONS by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Proposed Order)(Long, Elizabeth) (Entered: 09/18/2023)	
185	09/18/2023	REDACTION to 169 SEALED MOTION CHARTER'S MOTION TO EXCLUDE THE EXPERT OPINIONS OF STEPHEN DELL by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Exhibit, # 9 Exhibit, # 10 Exhibit, # 11 Exhibit, # 12 Exhibit, # 13 Proposed Order)(Long, Elizabeth) (Entered: 09/18/2023)	
186	09/18/2023	REDACTION to 171 SEALED MOTION CHARTER'S MOTION TO STRIKE ENTROPIC'S IMPROPER SECONDARY CONSIDERATIONS POSITIONS by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Exhibit, # 9 Exhibit, # 10 Proposed Order)(Long, Elizabeth) (Entered:	

#	Date	Proceeding Text	Source
		09/18/2023)	
187	09/18/2023	REDACTION to 172 SEALED MOTION (CHARTER'S MOTION FOR PARTIAL SUMMARY JUDGMENT OF NO PRE-SUIT DAMAGES) by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Exhibit, # 9 Exhibit, # 10 Exhibit, # 11 Exhibit, # 12 Exhibit, # 13 Exhibit, # 14 Exhibit, # 15 Exhibit, # 16 Exhibit, # 17 Exhibit, # 18 Proposed Order)(Long, Elizabeth) (Entered: 09/18/2023)	
188	09/18/2023	REDACTION to 173 SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT) by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Exhibit, # 9 Exhibit, # 10 Exhibit, # 11 Exhibit, # 12 Exhibit, # 13 Proposed Order)(Long, Elizabeth) (Entered: 09/18/2023)	
189	09/18/2023	REDACTION to 176 SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF THE ASSERTED CLAIMS OF THE '682 AND '690 PATENTS) by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Exhibit, # 9 Exhibit, # 10 Errata, # 11 Exhibit, # 12 Exhibit, # 13 Exhibit, # 14 Exhibit, # 15 Exhibit, # 16 Exhibit, # 17 Exhibit, # 18 Exhibit, # 19 Exhibit, # 20 Exhibit, # 21 Exhibit, # 22 Exhibit, # 23 Exhibit, # 24 Proposed Order)(Long, Elizabeth) (Entered: 09/18/2023)	
190	09/20/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Michael T Pieja on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9713369. (Pieja, Michael) (Entered: 09/20/2023)	
191	09/20/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Alan E Littmann on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9713422. (Littmann, Alan) (Entered: 09/20/2023)	
192	09/20/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Doug Winnard on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9713441. (Winnard, Doug) (Additional attachment(s) added on 9/20/2023: # 1 Sealed Attachment) (nkl,). (Entered: 09/20/2023)	
193	09/20/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Shaun Zhang on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9713465. (Zhang, Shaun) (Entered: 09/20/2023)	
194	09/20/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Jennifer M. Hartjes on behalf of Entropic Communications, LLC. Filing fee $ 100, receipt number ATXEDC-9713473. (Hartjes, Jennifer) (Entered: 09/20/2023)	
195	09/21/2023	ORDER granting 182 AGREED MOTION to Amend/Correct 165 Order on Motion to Amend/Correct Docket Control Order. Signed by District Judge Rodney Gilstrap on 9/21/2023. (ch,) (Entered: 09/21/2023)	
196	09/25/2023	SEALED RESPONSE to Motion re 167 SEALED MOTION CHARTER'S MOTION TO STRIKE DR. KRAMER'S IMPROPER OPINIONS filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Proposed Order)(Shimota, James) (Entered: 09/25/2023)	
197	09/25/2023	RESPONSE in Opposition re 172 SEALED MOTION (CHARTER'S MOTION FOR PARTIAL SUMMARY JUDGMENT	

#	Date	Proceeding Text	Source
		OF NO PRE-SUIT DAMAGES) filed by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Shimota, James) (Entered: 09/25/2023)	
198	09/25/2023	SEALED ADDITIONAL ATTACHMENTS to Main Document: 197 Response in Opposition to Motion. (Declaration of James Shimota in Support of Plaintiff's Opposition) (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G)(Shimota, James) (Entered: 09/25/2023)	
199	09/25/2023	***FILED IN ERROR***Additional Attachments to Main Document: 197 Response in Opposition to Motion.. (Attachments: # 1 Exhibit H (Public))(Shimota, James) Modified on 9/25/2023 (ch,). (Entered: 09/25/2023)	
	09/25/2023	***FILED IN ERROR. FILED UNDER THE WRONG EVENT Document # 199, Additional attachments. PLEASE IGNORE.*** (ch,) (Entered: 09/25/2023)	
200	09/25/2023	REDACTION to 198 Sealed Additional Attachments to Main Document, by Entropic Communications, LLC. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H)(Shimota, James) (Entered: 09/25/2023)	
201	09/25/2023	SEALED RESPONSE to Motion re 171 SEALED MOTION CHARTER'S MOTION TO STRIKE ENTROPIC'S IMPROPER SECONDARY CONSIDERATIONS POSITIONS filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of Nicholas Lenning, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L, # 14 Exhibit M, # 15 Exhibit N, # 16 Proposed Order)(Shimota, James) (Entered: 09/25/2023)	
202	09/25/2023	SEALED RESPONSE to Motion re 180 SEALED MOTION for Summary Judgment of No Unclean Hands Defense filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration Declaration of Elizabeth Long, # 2 Exhibit D, # 3 Exhibit E, # 4 Exhibit F, # 5 Exhibit G, # 6 Exhibit H, # 7 Exhibit I, # 8 Exhibit J, # 9 Exhibit K, # 10 Exhibit L, # 11 Exhibit M, # 12 Exhibit N, # 13 Exhibit O, # 14 Exhibit P, # 15 Exhibit Q, # 16 Exhibit R, # 17 Proposed Order)(Reisner, Daniel) (Entered: 09/25/2023)	
203	09/25/2023	SEALED RESPONSE to Motion re 169 SEALED MOTION CHARTER'S MOTION TO EXCLUDE THE EXPERT OPINIONS OF STEPHEN DELL filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L, # 14 Exhibit M, # 15 Exhibit N, # 16 Proposed Order)(Shimota, James) (Entered: 09/25/2023)	
204	09/25/2023	***FILED IN ERROR***SEALED RESPONSE to Motion re 181 MOTION for Summary Judgment of Validity Under 35 U.S.C. 101 (CORRECTION OF ECF DOCUMENT TITLE) filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Elizabeth Long, # 2 Exhibit E, # 3 Proposed Order)(Reisner, Daniel) Modified on 9/26/2023 (ch,). (Entered: 09/25/2023)	
205	09/25/2023	SEALED RESPONSE to Motion re 166 SEALED MOTION CHARTER'S MOTION TO STRIKE DR. SOURI'S IMPROPER OPINIONS filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L, # 14 Exhibit M, # 15 Exhibit N, # 16 Exhibit O, # 17	

#	Date	Proceeding Text	Source
		Proposed Order)(Shimota, James) (Entered: 09/25/2023)	
206	09/25/2023	SEALED RESPONSE to Motion re 170 MOTION for Summary Judgment Of No Invalidity Under 32 U.S.C. 102 & 103 filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Elizabeth Long, # 2 Exhibit E, # 3 Proposed Order)(Reisner, Daniel) (Entered: 09/25/2023)	
207	09/25/2023	RESPONSE in Opposition re 173 SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT) filed by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Shimota, James) (Entered: 09/25/2023)	
208	09/25/2023	SEALED ADDITIONAL ATTACHMENTS to Main Document: 207 Response in Opposition to Motion, (Declaration of James Shimota in Support of Plaintiff's Opposition). (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D)(Shimota, James) (Entered: 09/25/2023)	
209	09/25/2023	RESPONSE to Motion re 181 MOTION for Summary Judgment of Validity Under 35 U.S.C. 101 (CORRECTION OF ECF DOCUMENT TITLE), 178 MOTION for Summary Judgment for Summary Judgment of No License Defense Based on DOCSIS filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Elizabeth Long, # 2 Exhibit C, # 3 Exhibit D, # 4 Exhibit E, # 5 Exhibit F, # 6 Exhibit G, # 7 Exhibit H, # 8 Exhibit I, # 9 Exhibit J, # 10 Proposed Order)(Reisner, Daniel) (Entered: 09/25/2023)	
210	09/25/2023	SEALED RESPONSE to Motion re 176 SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF THE ASSERTED CLAIMS OF THE '682 AND '690 PATENTS) filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of James Shimota, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Proposed Order)(Shimota, James) (Entered: 09/25/2023)	
211	09/25/2023	SEALED RESPONSE to Motion re 179 SEALED MOTION of Partial Summary Judgment That Devices With MaxLinear Chips are Not Non-Infringing Alternatives Affecting the Reasonable Royalty Rate filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Elizabeth Long, # 2 Exhibit G, # 3 Exhibit H, # 4 Exhibit I, # 5 Exhibit J, # 6 Errata K, # 7 Exhibit L, # 8 Exhibit M, # 9 Exhibit N, # 10 Proposed Order)(Reisner, Daniel) (Entered: 09/25/2023)	
212	09/25/2023	SEALED RESPONSE to Motion re 174 SEALED MOTION to Strike Opinions of Christopher Bakewell filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Elizabeth Long, # 2 Exhibit AD, # 3 Exhibit AE, # 4 Exhibit AF, # 5 Exhibit AG, # 6 Exhibit AH, # 7 Exhibit AI, # 8 Exhibit AJ, # 9 Exhibit AK, # 10 Exhibit AL, # 11 Exhibit AM, # 12 Exhibit AN, # 13 Exhibit AO, # 14 Exhibit AP, # 15 Exhibit AQ, # 16 Exhibit AR, # 17 Exhibit AS, # 18 Exhibit AT, # 19 Exhibit AU, # 20 Exhibit AV, # 21 Proposed Order)(Reisner, Daniel) (Entered: 09/25/2023)	
213	09/25/2023	SEALED RESPONSE to Motion re 175 SEALED MOTION to Strike Opinions of Dr. Kevin Almeroth filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Elizabeth Long, # 2 Exhibit K, # 3 Exhibit L, # 4 Exhibit M, # 5 Exhibit N, # 6 Exhibit O, # 7 Exhibit P, # 8 Exhibit Q, # 9 Exhibit R, # 10 Exhibit S, # 11 Exhibit T, # 12 Proposed Order)(Reisner, Daniel) (Entered: 09/25/2023)	
214	09/25/2023	SEALED RESPONSE to Motion re 168 MOTION to Strike Opinions of Steven Goldberg filed by Charter Communications,	

#	Date	Proceeding Text	Source
		Inc.. (Attachments: # 1 Affidavit/Declaration of Elizabeth Long, # 2 Exhibit G, # 3 Exhibit H, # 4 Exhibit I, # 5 Exhibit J, # 6 Exhibit K, # 7 Exhibit L, # 8 Proposed Order)(Reisner, Daniel) (Entered: 09/25/2023)	
215	09/25/2023	SEALED RESPONSE to Motion re 177 SEALED MOTION for Summary Judgment of No License Defense Based on DOCSIS filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration of Elizabeth Long, # 2 Exhibit E, # 3 Exhibit F, # 4 Exhibit G, # 5 Exhibit H, # 6 Exhibit I, # 7 Exhibit J, # 8 Exhibit K, # 9 Exhibit L, # 10 Exhibit M, # 11 Exhibit N, # 12 Exhibit O, # 13 Exhibit P, # 14 Exhibit Q, # 15 Exhibit R, # 16 Exhibit S, # 17 Exhibit T, # 18 Exhibit U, # 19 Exhibit V, # 20 Exhibit W, # 21 Exhibit X, # 22 Proposed Order)(Reisner, Daniel) (Entered: 09/25/2023)	
	09/26/2023	***FILED IN ERROR. PER ATTORNEY Document # 204, Sealed Response. PLEASE IGNORE.*** (ch,) (Entered: 09/26/2023)	
216	09/26/2023	OPPOSED MOTION to Amend/Correct Docket Control Order by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Proposed Order)(Long, Elizabeth) (Entered: 09/26/2023)	
217	10/02/2023	SEALED REPLY to Response to Motion re 167 SEALED MOTION CHARTER'S MOTION TO STRIKE DR. KRAMER'S IMPROPER OPINIONS filed by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/02/2023)	
218	10/02/2023	SEALED REPLY to Response to Motion re 172 SEALED MOTION (CHARTER'S MOTION FOR PARTIAL SUMMARY JUDGMENT OF NO PRE-SUIT DAMAGES) filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration OF ELIZABETH LONG IN SUPPORT OF CHARTER'S REPLY BRIEF IN SUPPORT OF ITS MOTION FOR PARTIAL SUMMARY JUDGMENT OF NO PRE-SUIT DAMAGES, # 2 Exhibit - Q PRESUIT DAMAGES SJ)(Long, Elizabeth) (Entered: 10/02/2023)	
219	10/02/2023	REDACTION to 202 Sealed Response to Motion,, re 180 SEALED MOTION for Summary Judgment of No Unclean Hands Defense by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Exhibit, # 9 Exhibit, # 10 Exhibit, # 11 Exhibit, # 12 Exhibit, # 13 Exhibit, # 14 Exhibit, # 15 Exhibit, # 16 Exhibit, # 17 Proposed Order)(Long, Elizabeth) (Entered: 10/02/2023)	
220	10/02/2023	REDACTION to 206 Sealed Response to Motion, re 170 MOTION for Summary Judgment Of No Invalidity Under 35 U.S.C. 102 & 10 by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Proposed Order)(Long, Elizabeth) (Entered: 10/02/2023)	
221	10/02/2023	REDACTION to 211 Sealed Response to Motion, re 179 SEALED MOTION of Partial Summary Judgment That Devices With MaxLinear Chips are Not Non-Infringing Alternatives Affecting the Reasonable Royalty Rate f by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Exhibit, # 9 Exhibit, # 10 Proposed Order)(Long, Elizabeth) (Entered: 10/02/2023)	
222	10/02/2023	REDACTION to 212 Sealed Response to Motion,, re 174 SEALED MOTION to Strike Opinions of Christopher Bakewell by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Exhibit, # 9 Exhibit, # 10 Exhibit, # 11 Exhibit, # 12 Exhibit, # 13 Exhibit, # 14 Exhibit, # 15 Exhibit, # 16 Exhibit, # 17 Exhibit, # 18 Exhibit, # 19 Exhibit, # 20 Exhibit, # 21 Proposed Order)(Long,	

#	Date	Proceeding Text	Source
		Elizabeth) (Entered: 10/02/2023)	
223	10/02/2023	REDACTION to 214 Sealed Response to Motion, re 168 MOTION to Strike Opinions of Steven Goldberg by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Proposed Order)(Long, Elizabeth) (Entered: 10/02/2023)	
224	10/02/2023	REDACTION to 215 Sealed Response to Motion,, re 177 SEALED MOTION for Summary Judgment of No License Defense Based on DOCSIS by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Exhibit, # 9 Exhibit, # 10 Exhibit, # 11 Exhibit, # 12 Exhibit, # 13 Exhibit, # 14 Exhibit, # 15 Exhibit, # 16 Exhibit, # 17 Exhibit, # 18 Exhibit, # 19 Exhibit, # 20 Exhibit, # 21 Exhibit, # 22 Proposed Order)(Long, Elizabeth) (Entered: 10/02/2023)	
225	10/02/2023	REDACTION to 213 Sealed Response to Motion, re 175 SEALED MOTION to Strike Opinions of Dr. Kevin Almeroth by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Exhibit, # 9 Exhibit, # 10 Exhibit, # 11 Exhibit, # 12 Proposed Order)(Long, Elizabeth) (Entered: 10/02/2023)	
226	10/03/2023	***FILED IN ERROR***RESPONSE in Support re 173 SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT) filed by Charter Communications, Inc.. (Long, Elizabeth) Modified on 10/3/2023 (ch,). (Entered: 10/03/2023)	
	10/03/2023	***FILED IN ERROR. FILED UNDER THE WRONG EVENT Document # 226, Response. PLEASE IGNORE.*** (ch,) (Entered: 10/03/2023)	
227	10/03/2023	***FILED IN ERROR***RESPONSE to Motion re 173 SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT) CHARTER'S REPLY IN FURTHER SUPPORT OF ITS MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT filed by Charter Communications, Inc.. (Long, Elizabeth) Modified on 10/3/2023 (ch,). (Entered: 10/03/2023)	
	10/03/2023	***FILED IN ERROR. PLEASE FILE YOUR REPLY UNDER CORRECT EVENT Document # 227, Response to Motion. PLEASE IGNORE.*** (ch,) (Entered: 10/03/2023)	
228	10/03/2023	REPLY to Response to Motion re 173 SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT) CHARTER'S REPLY IN FURTHER SUPPORT OF ITS MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT filed by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/03/2023)	
229	10/03/2023	***DEFICIENT DOCUMENT***SEALED ADDITIONAL ATTACHMENTS to Main Document: 228 Reply to Response to Motion,. DECLARATION OF ELIZABETH LONG IN SUPPORT OF CHARTER'S REPLY IN SUPPORT OF ITS MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT (Attachments: # 1 Exhibit L, # 2 Exhibit M)(Long, Elizabeth) Modified on 10/3/2023 (ch,). (Entered: 10/03/2023)	
230	10/03/2023	SEALED REPLY to Response to Motion re 176 SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF THE ASSERTED CLAIMS OF THE '682 AND '690 PATENTS) filed by Charter Communications, Inc..	

#	Date	Proceeding Text	Source
		(Long, Elizabeth) (Entered: 10/03/2023)	
	10/03/2023	NOTICE of Deficiency regarding the 229 submitted Needs Certificate of Authorization to file under seal and Certificate of Service. Correction should be made by one business day (ch.) (Entered: 10/03/2023)	
231	10/03/2023	Additional Attachments to Main Document: 230 Sealed Reply to Response to Motion,.. (Attachments: # 1 Exhibit W, # 2 Exhibit X)(Long, Elizabeth) (Entered: 10/03/2023)	
232	10/03/2023	SEALED ADDITIONAL ATTACHMENTS to Main Document: 228 Reply to Response to Motion,. DECLARATION OF ELIZABETH LONG IN SUPPORT OF CHARTER'S REPLY IN SUPPORT OF ITS MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT (Attachments: # 1 Exhibit L, # 2 Exhibit M)(Long, Elizabeth) (Entered: 10/03/2023)	
233	10/03/2023	SEALED REPLY to Response to Motion re 166 SEALED MOTION CHARTER'S MOTION TO STRIKE DR. SOURI'S IMPROPER OPINIONS filed by Charter Communications, Inc..CHARTER'S REPLY BRIEF IN SUPPORT OF ITS MOTION TO STRIKEDR. SOURI'S IMPROPER OPINIONS (Long, Elizabeth) (Entered: 10/03/2023)	
234	10/03/2023	SEALED REPLY to Response to Motion re 171 SEALED MOTION CHARTER'S MOTION TO STRIKE ENTROPIC'S IMPROPER SECONDARY CONSIDERATIONS POSITIONS filed by Charter Communications, Inc.. (Attachments: # 1 DECLARATION OF ELIZABETH LONG IN SUPPORT OF CHARTER'S MOTION TO STRIKE ENTROPICS IMPROPER SECONDARY CONSIDERATIONS POSITIONS(Long, Elizabeth) (Entered: 10/03/2023)	
235	10/03/2023	REPLY to Response to Motion re 168 MOTION to Strike Opinions of Steven Goldberg filed by Entropic Communications, LLC. (Shimota, James) (Entered: 10/03/2023)	
236	10/03/2023	REPLY to Response to Motion re 170 MOTION for Summary Judgment Of No Invalidity Under 32 U.S.C. 102 & 103 filed by Entropic Communications, LLC. (Shimota, James) (Entered: 10/03/2023)	
237	10/03/2023	SEALED REPLY to Response to Motion re 177 SEALED MOTION for Summary Judgment of No License Defense Based on DOCSIS filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of James Shimota, # 2 Exhibit E)(Shimota, James) (Entered: 10/03/2023)	
238	10/03/2023	SEALED REPLY to Response to Motion re 180 SEALED MOTION for Summary Judgment of No Unclean Hands Defense filed by Entropic Communications, LLC. (Shimota, James) (Entered: 10/03/2023)	
239	10/03/2023	SEALED REPLY to Response to Motion re 169 SEALED MOTION CHARTER'S MOTION TO EXCLUDE THE EXPERT OPINIONS OF STEPHEN DELL filed by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration OF ELIZABETH LONG IN SUPPORT OF CHARTER'S REPLY IN SUPPORT OF ITS MOTION TO EXCLUDE THE OPINIONS OF STEPHEN DELL, # 2 Exhibit L, # 3 Exhibit M)(Long, Elizabeth) (Entered: 10/03/2023)	
240	10/03/2023	SEALED REPLY to Response to Motion re 174 SEALED MOTION to Strike Opinions of Christopher Bakewell filed by Entropic Communications, LLC. (Shimota, James) (Entered: 10/03/2023)	
241	10/03/2023	SEALED REPLY to Response to Motion re 175 SEALED MOTION to Strike Opinions of Dr. Kevin Almeroth filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of James Shimota, # 2 Exhibit K)(Shimota, James) (Entered: 10/03/2023)	

#	Date	Proceeding Text	Source
242	10/03/2023	SEALED REPLY to Response to Motion re 179 SEALED MOTION of Partial Summary Judgment That Devices With MaxLinear Chips are Not Non-Infringing Alternatives Affecting the Reasonable Royalty Rate filed by Entropic Communications, LLC. (Shimota, James) (Entered: 10/03/2023)	
243	10/03/2023	REPLY to Response to Motion re 181 MOTION for Summary Judgment of Validity Under 35 U.S.C. 101 (CORRECTION OF ECF DOCUMENT TITLE) filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of James Shimota, # 2 Exhibit C)(Shimota, James) (Entered: 10/03/2023)	
244	10/03/2023	OPPOSED SEALED MOTION for Leave to File Out of Time Plaintiff's Motion to Compel Testimony and Documents Improperly Withheld as Privileged by Entropic Communications, LLC. (Attachments: # 1 Declaration of Nicholas Lenning, # 2 Lenning Declaration, Ex. A, # 3 Lenning Declaration, Ex. B, # 4 Lenning Declaration, Ex. C, # 5 Lenning Declaration, Ex. D, # 6 Lenning Declaration, Ex. E, # 7 Lenning Declaration, Ex. F, # 8 Lenning Declaration, Ex. G, # 9 Lenning Declaration, Ex. H, # 10 Lenning Declaration, Ex. I, # 11 Lenning Declaration, Ex. J, # 12 Lenning Declaration, Ex. K, # 13 Declaration of Peter Soskin, # 14 Soskin Declaration, Ex. A, # 15 Soskin Declaration, Ex. B, # 16 Soskin Declaration, Ex. C, # 17 Proposed Order)(Shimota, James) (Entered: 10/03/2023)	
245	10/03/2023	OPPOSED SEALED MOTION to Compel Testimony and Documents Improperly Withheld as Privileged by Entropic Communications, LLC. (Attachments: # 1 Declaration of Nicholas Lenning, # 2 Lenning Declaration, Ex. A, # 3 Lenning Declaration, Ex. B, # 4 Lenning Declaration, Ex. C, # 5 Lenning Declaration, Ex. D, # 6 Lenning Declaration, Ex. E, # 7 Lenning Declaration, Ex. F, # 8 Lenning Declaration, Ex. G, # 9 Lenning Declaration, Ex. H, # 10 Lenning Declaration, Ex. I, # 11 Lenning Declaration, Ex. J, # 12 Lenning Declaration, Ex. K, # 13 Lenning Declaration, Ex. L, # 14 Lenning Declaration, Ex. M, # 15 Lenning Declaration, Ex. N, # 16 Lenning Declaration, Ex. O, # 17 Declaration of Peter Soskin, # 18 Soskin Declaration, Ex. A, # 19 Soskin Declaration, Ex. B, # 20 Soskin Declaration, Ex. C, # 21 Proposed Order)(Shimota, James) (Entered: 10/03/2023)	
246	10/10/2023	SUR-REPLY to Reply to Response to Motion re 172 SEALED MOTION (CHARTER'S MOTION FOR PARTIAL SUMMARY JUDGMENT OF NO PRE-SUIT DAMAGES) filed by Entropic Communications, LLC. (Shimota, James) (Entered: 10/10/2023)	
247	10/10/2023	REDACTION to 217 Sealed Reply to Response to Motion to Strike Dr. Kramer's Improper Opinions by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/10/2023)	
248	10/10/2023	REDACTION to 218 Sealed Reply to Response to Motion, FOR PARTIAL SUMMARY JUDGMENT OF NO PRE-SUIT DAMAGES by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit)(Long, Elizabeth) (Entered: 10/10/2023)	
249	10/10/2023	REDACTION to 230 Sealed Reply to Response to Motion, FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF THE ASSERTED CLAIMS OF THE '682 AND '690 PATENTS by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/10/2023)	
250	10/10/2023	REDACTION to 233 Sealed Reply to Response to Motion, TO STRIKE DR. SOURI'S IMPROPER OPINIONS by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/10/2023)	
251	10/10/2023	REDACTION to 234 Sealed Reply to Response to Motion, TO STRIKE ENTROPIC'S IMPROPER SECONDARY	

#	Date	Proceeding Text	Source
		CONSIDERATIONS POSITIONS by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration)(Long, Elizabeth) (Entered: 10/10/2023)	
252	10/10/2023	REDACTION to 239 Sealed Reply to Response to Motion, TO EXCLUDE THE EXPERT OPINIONS OF STEPHEN DELL by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit)(Long, Elizabeth) (Entered: 10/10/2023)	
253	10/10/2023	REDACTION to 232 Sealed Additional Attachments to Main Document, 228 Reply to Response to Motion,. DECLARATION OF ELIZABETH LONG IN SUPPORT OF CHARTER'S REPLY IN SUPPORT OF ITS MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT by Charter Communications, Inc.. (Attachments: # 1 Exhibit, # 2 Exhibit)(Long, Elizabeth) (Entered: 10/10/2023)	
254	10/10/2023	SUR-REPLY to Reply to Response to Motion re 167 SEALED MOTION CHARTER'S MOTION TO STRIKE DR. KRAMER'S IMPROPER OPINIONS filed by Entropic Communications, LLC. (Shimota, James) (Entered: 10/10/2023)	
255	10/10/2023	SEALED ADDITIONAL ATTACHMENTS to Main Document: 254 Sur-Reply to Reply to Response to Motion (Declaration of James Shimota in Support of Entropic's Sur-Reply) (Attachments: # 1 Exhibit H)(Shimota, James) (Entered: 10/10/2023)	
256	10/10/2023	SUR-REPLY to Reply to Response to Motion re 173 SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF THE ASSERTED CLAIMS OF THE '362 PATENT) filed by Entropic Communications, LLC. (Shimota, James) (Entered: 10/10/2023)	
257	10/10/2023	OPPOSED SEALED MOTION in Limine by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L, # 14 Exhibit M, # 15 Exhibit N, # 16 Exhibit O, # 17 Proposed Order)(Brown, Melissa) (Entered: 10/10/2023)	
258	10/10/2023	OPPOSED SEALED MOTION IN LIMINE by Entropic Communications, LLC. (Attachments: # 1 SEALED Declaration of Michael T. Pieja, # 2 Exhibit A - SEALED Boglioli 8-11-23 Dep Tr (excerpts), # 3 Exhibit B - SEALED Entropic Witness List, # 4 Exhibit C - SEALED Charter Witness List, # 5 Exhibit D - SEALED Bakewell Reb. Rpt. (excerpts), # 6 Exhibit E - SEALED Dell Rpt. (excerpts), # 7 Exhibit F - SEALED Kirchoff 8-16-23 Dep Tr (excerpts), # 8 Exhibit G - SEALED Cangiane 07-17-23 Dep Tr (excerpts), # 9 Exhibit H - SEALED Almeroth Reb. Rpt. (excerpts), # 10 Proposed Order)(Pieja, Michael) (Entered: 10/10/2023)	
259	10/11/2023	RESPONSE in Opposition re 216 OPPOSED MOTION to Amend/Correct Docket Control Order filed by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Shimota, James) (Entered: 10/11/2023)	
260	10/11/2023	SEALED SUR-REPLY to Reply to Response to Motion re 166 SEALED MOTION CHARTER'S MOTION TO STRIKE DR. SOURI'S IMPROPER OPINIONS filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of James Shimota, # 2 Exhibit P)(Shimota, James) (Entered: 10/11/2023)	
261	10/11/2023	REDACTION to 141 SEALED MOTION to Strike the Expert Report of David O. Taylor by Entropic Communications, LLC. (Shimota, James) (Entered: 10/11/2023)	
262	10/11/2023	SUR-REPLY to Reply to Response to Motion re 168 MOTION to Strike Opinions of Steven Goldberg filed by Charter	

#	Date	Proceeding Text	Source
		Communications, Inc.. (Long, Elizabeth) (Entered: 10/11/2023)	
263	10/11/2023	REDACTION to 151 Sealed Reply to Response to Motion by Entropic Communications, LLC. (Shimota, James) (Entered: 10/11/2023)	
264	10/11/2023	SUR-REPLY to Reply to Response to Motion re 170 MOTION for Summary Judgment Of No Invalidity Under 32 U.S.C. 102 & 103 filed by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/11/2023)	
265	10/11/2023	REDACTION to 174 SEALED MOTION to Strike Opinions of Christopher Bakewell by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota, # 2 Affidavit/Declaration of Darlene Ghavimi)(Shimota, James) (Entered: 10/11/2023)	
266	10/11/2023	SUR-REPLY to Reply to Response to Motion re 181 MOTION for Summary Judgment of Validity Under 35 U.S.C. 101 (CORRECTION OF ECF DOCUMENT TITLE) filed by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/11/2023)	
267	10/11/2023	SEALED SUR-REPLY to Reply to Response to Motion re 177 SEALED MOTION for Summary Judgment of No License Defense Based on DOCSIS filed by Charter Communications, Inc. (Long, Elizabeth) (Entered: 10/11/2023)	
268	10/11/2023	SEALED SUR-REPLY to Reply to Response to Motion re 179 SEALED MOTION of Partial Summary Judgment That Devices With MaxLinear Chips are Not Non-Infringing Alternatives Affecting the Reasonable Royalty Rate filed by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/11/2023)	
269	10/11/2023	REDACTION to 175 SEALED MOTION to Strike Opinions of Dr. Kevin Almeroth by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota)(Shimota, James) (Entered: 10/11/2023)	
270	10/11/2023	SEALED SUR-REPLY to Reply to Response to Motion re 180 SEALED MOTION for Summary Judgment of No Unclean Hands Defense filed by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/11/2023)	
271	10/11/2023	SEALED SUR-REPLY to Reply to Response to Motion re 174 SEALED MOTION to Strike Opinions of Christopher Bakewell filed by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/11/2023)	
272	10/11/2023	REDACTION to 177 SEALED MOTION for Summary Judgment of No License Defense Based on DOCSIS by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota)(Shimota, James) (Entered: 10/11/2023)	
273	10/11/2023	SEALED SUR-REPLY to Reply to Response to Motion re 175 SEALED MOTION to Strike Opinions of Dr. Kevin Almeroth filed by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/11/2023)	
274	10/11/2023	REDACTION to 179 SEALED MOTION of Partial Summary Judgment That Devices With MaxLinear Chips are Not Non-Infringing Alternatives Affecting the Reasonable Royalty Rate by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota)(Shimota, James) (Entered: 10/11/2023)	
275	10/11/2023	REDACTION to 180 SEALED MOTION for Summary Judgment of No Unclean Hands Defense by Entropic Communications, LLC. (Attachments: # 1 Affidavit/Declaration of James Shimota)(Shimota, James) (Entered: 10/11/2023)	
276	10/11/2023	REDACTION to 237 Sealed Reply to Response to Motion, by Entropic Communications, LLC. (Shimota, James) (Entered:	

#	Date	Proceeding Text	Source
		10/11/2023)	
277	10/11/2023	REDACTION to 238 Sealed Reply to Response to Motion by Entropic Communications, LLC. (Shimota, James) (Entered: 10/11/2023)	
278	10/11/2023	REDACTION to 240 Sealed Reply to Response to Motion by Entropic Communications, LLC. (Shimota, James) (Entered: 10/11/2023)	
279	10/11/2023	REDACTION to 241 Sealed Reply to Response to Motion by Entropic Communications, LLC. (Shimota, James) (Entered: 10/11/2023)	
280	10/11/2023	REDACTION to 242 Sealed Reply to Response to Motion, by Entropic Communications, LLC. (Shimota, James) (Entered: 10/11/2023)	
281	10/11/2023	SEALED SUR-REPLY to Reply to Response to Motion re 169 SEALED MOTION CHARTER'S MOTION TO EXCLUDE THE EXPERT OPINIONS OF STEPHEN DELL filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of Nicholas Lenning, # 2 Lenning Declaration, Ex. A)(Shimota, James) (Entered: 10/11/2023)	
282	10/11/2023	SEALED SUR-REPLY to Reply to Response to Motion re 171 SEALED MOTION CHARTER'S MOTION TO STRIKE ENTROPIC'S IMPROPER SECONDARY CONSIDERATIONS POSITIONS filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of Nicholas Lenning, # 2 Lenning Declaration, Ex. A)(Shimota, James) (Entered: 10/11/2023)	
283	10/11/2023	SEALED SUR-REPLY to Reply to Response to Motion re 176 SEALED MOTION (CHARTER'S MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF THE ASSERTED CLAIMS OF THE '682 AND '690 PATENTS) filed by Entropic Communications, LLC. (Attachments: # 1 Declaration of James Shimota, # 2 Exhibit A)(Shimota, James) (Entered: 10/11/2023)	
284	10/12/2023	NOTICE by Entropic Communications, LLC of Request for Daily Trial Transcripts and Real-Time Reporting (Fair, Andrea) (Entered: 10/12/2023)	
285	10/13/2023	NOTICE by Charter Communications, Inc. NOTICE OF REQUEST FOR DAILY TRANSCRIPTS AND REAL TIME REPORTING (Long, Elizabeth) (Entered: 10/13/2023)	
286	10/13/2023	NOTICE of Attorney Appearance by Johnny Ward, Jr on behalf of Entropic Communications, LLC (Ward, Johnny) (Entered: 10/13/2023)	
287	10/13/2023	OPPOSED MOTION for Leave to File Out of Time Plaintiff's Supplemental Motion to Strike Opinions of Christopher Bakewell by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Shimota, James) (Entered: 10/13/2023)	
288	10/13/2023	***DEFICIENT DOCUMENT***SEALED ADDITIONAL ATTACHMENTS to Main Document: 287 OPPOSED MOTION for Leave to File Out of Time Plaintiff's Supplemental Motion to Strike Opinions of Christopher Bakewell. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D)(Shimota, James) Modified on 10/16/2023 (ch,). (Entered: 10/13/2023)	
289	10/13/2023	MOTION to Strike Supplemental Motion to Strike Opinions of Christopher Bakewell by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Shimota, James) (Entered: 10/13/2023)	
290	10/13/2023	***DEFICIENT DOCUMENT***SEALED ADDITIONAL ATTACHMENTS to Main Document: 289 MOTION to Strike Supplemental Motion to Strike Opinions of Christopher Bakewell. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Shimota, James)	

#	Date	Proceeding Text	Source
		Modified on 10/16/2023 (ch,). (Entered: 10/13/2023)	
	10/16/2023	NOTICE of Deficiency regarding the 288 submitted Needs Certificate of Authorization to file under seal and Certificate of Service. Correction should be made by one business day (ch,) (Entered: 10/16/2023)	
	10/16/2023	NOTICE of Deficiency regarding the 290 submitted Needs Certificate of Authorization to file under seal and Certificate of Service. Correction should be made by one business day (ch,) (Entered: 10/16/2023)	
291	10/16/2023	SEALED ADDITIONAL ATTACHMENTS to Main Document: 287 OPPOSED MOTION for Leave to File Out of Time Plaintiff's Supplemental Motion to Strike Opinions of Christopher Bakewell. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D)(Shimota, James) (Entered: 10/16/2023)	
292	10/16/2023	SEALED ADDITIONAL ATTACHMENTS to Main Document: 289 MOTION to Strike Supplemental Motion to Strike Opinions of Christopher Bakewell. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Shimota, James) (Entered: 10/16/2023)	
293	10/16/2023	REDACTION to 196 Sealed Response to Motion, by Entropic Communications, LLC. (Shimota, James) (Entered: 10/16/2023)	
294	10/16/2023	REDACTION to 201 Sealed Response to Motion., by Entropic Communications, LLC. (Shimota, James) (Entered: 10/16/2023)	
295	10/16/2023	REDACTION to 203 Sealed Response to Motion,, by Entropic Communications, LLC. (Shimota, James) (Entered: 10/16/2023)	
296	10/16/2023	REDACTION to 205 Sealed Response to Motion., by Entropic Communications, LLC. (Shimota, James) (Entered: 10/16/2023)	
297	10/16/2023	REDACTION to 210 Sealed Response to Motion, by Entropic Communications, LLC. (Shimota, James) (Entered: 10/16/2023)	
298	10/16/2023	REDACTION to 260 Sealed Sur-Reply to Reply to Response to Motion, by Entropic Communications, LLC. (Shimota, James) (Entered: 10/16/2023)	
299	10/16/2023	REDACTION to 281 Sealed Sur-Reply to Reply to Response to Motion, by Entropic Communications, LLC. (Shimota, James) (Entered: 10/16/2023)	
300	10/16/2023	REDACTION to 282 Sealed Sur-Reply to Reply to Response to Motion, by Entropic Communications, LLC. (Shimota, James) (Entered: 10/16/2023)	
301	10/16/2023	REDACTION to 283 Sealed Sur-Reply to Reply to Response to Motion, by Entropic Communications, LLC. (Shimota, James) (Entered: 10/16/2023)	
302	10/16/2023	OPPOSED MOTION for Leave to Serve Mr. Dell's Third Supplemental Expert Report Out of Time by Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Shimota, James) (Entered: 10/16/2023)	
303	10/16/2023	SEALED ADDITIONAL ATTACHMENTS to Main Document:. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Shimota, James) (Entered: 10/16/2023)	
304	10/17/2023	REDACTION to 258 OPPOSED SEALED MOTION IN LIMINE by Entropic Communications, LLC. (Attachments: # 1 Declaration of Michael T. Pieja, # 2 Additional Attachment(s) Exhibits A-H Filed Under Seal)(Pieja, Michael) (Entered: 10/17/2023)	
305	10/17/2023	REPLY to Response to Motion re 216 OPPOSED MOTION to Amend/Correct Docket Control Order filed by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/17/2023)	
	10/17/2023	Pretrial Conference originally set for 10/30/2023 has been RESET for 11/6/2023 at 09:00 AM in Ctrm 106 (Marshall) before District Judge Rodney Gilstrap. (aeb) (Entered: 10/17/2023)	

#	Date	Proceeding Text	Source
306	10/17/2023	NOTICE of Attorney Appearance by William Owen Young, Jr on behalf of Charter Communications, Inc. (Young, William) (Entered: 10/17/2023)	
307	10/17/2023	REDACTION to 257 OPPOSED SEALED MOTION in Limine by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit A (under seal), # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D - O (under seal), # 6 Proposed Order)(Brown, Melissa) (Entered: 10/17/2023)	
308	10/18/2023	AGREED MOTION to Amend/Correct 195 Order on Motion to Amend/Correct by Entropic Communications, LLC. (Shimota, James) (Entered: 10/18/2023)	
309	10/18/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Thomas J. Carr on behalf of Charter Communications, Inc.. Filing fee $ 100, receipt number ATXEDC-9764999. (Carr, Thomas) (Entered: 10/18/2023)	
310	10/18/2023	NOTICE of Attorney Appearance - Pro Hac Vice by Natalie Steiert on behalf of Charter Communications, Inc.. Filing fee $ 100, receipt number ATXEDC-9765076. (Steiert, Natalie) (Entered: 10/18/2023)	
311	10/18/2023	SEALED RESPONSE to Motion re 244 OPPOSED SEALED MOTION for Leave to File Out of Time Plaintiff's Motion to Compel Testimony and Documents Improperly Withheld as Privileged filed by Charter Communications, Inc. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Proposed Order)(Long, Elizabeth) (Entered: 10/18/2023)	
312	10/18/2023	SEALED RESPONSE to Motion re 245 OPPOSED SEALED MOTION to Compel Testimony and Documents Improperly Withheld as Privileged filed by Charter Communications, Inc. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Proposed Order)(Long, Elizabeth) (Entered: 10/18/2023)	
313	10/18/2023	UNOPPOSED MOTION to Withdraw as Attorney Paul I. Margulies by Charter Communications, Inc.. (Attachments: # 1 Proposed Order)(Long, Elizabeth) (Entered: 10/18/2023)	
314	10/18/2023	REDACTION to 267 Sealed Sur-Reply to Reply to Response to Motion FOR SUMMARY JUDGMENT OF NO LICENSE DEFENSE BASED ON DOCSIS by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/18/2023)	
315	10/18/2023	REDACTION to 268 Sealed Sur-Reply to Reply to Response to Motion, PARTIAL SUMMARY JUDGMENT THAT DEVICES WITH MAXLINEAR CHIPS ARE NOT NON-INFRINGING ALTERNATIVES AFFECTING THE REASONABLE ROYALTY RATE by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/18/2023)	
316	10/18/2023	REDACTION to 270 Sealed Sur-Reply to Reply to Response to Motion FOR SUMMARY JUDGMENT OF NO UNCLEAN HANDS DEFENSE by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/18/2023)	
317	10/18/2023	REDACTION to 271 Sealed Sur-Reply to Reply to Response to Motion TO STRIKE OPINIONS OF CHRISTOPHER BAKEWELL by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/18/2023)	
318	10/18/2023	REDACTION to 273 Sealed Sur-Reply to Reply to Response to Motion TO STRIKE OPINIONS OF DR. KEVIN ALMEROTH by Charter Communications, Inc.. (Long, Elizabeth) (Entered: 10/18/2023)	
319	10/19/2023	SEVENTH AMENDED DOCKET CONTROL ORDER granting 308 Motion to Amend/Correct. Signed by District Judge Rodney	

#	Date	Proceeding Text	Source
		Gilstrap on 10/19/2023. (ch,) (Entered: 10/20/2023)	
320	10/19/2023	ORDER granting 313 Motion to Withdraw as Attorney. Attorney Paul Isaac Margulies terminated. Signed by District Judge Rodney Gilstrap on 10/19/2023. (ch,) (Entered: 10/20/2023)	
321	10/20/2023	NOTICE by Entropic Communications, LLC re 244 OPPOSED SEALED MOTION for Leave to File Out of Time Plaintiff's Motion to Compel Testimony and Documents Improperly Withheld as Privileged Fully Briefed - Notice to Forgo Reply (Shimota, James) (Entered: 10/20/2023)	
322	10/20/2023	NOTICE by Entropic Communications, LLC re 245 OPPOSED SEALED MOTION to Compel Testimony and Documents Improperly Withheld as Privileged Fully Briefed - Notice to Forgo Reply (Shimota, James) (Entered: 10/20/2023)	
323	10/23/2023	SEALED RESPONSE to Motion re 258 OPPOSED SEALED MOTION IN LIMINE filed by Charter Communications, Inc. (Attachments: # 1 Affidavit/Declaration Long Decl ISO Charter Response to Entropic's MILs, # 2 Exhibit Ex. I, # 3 Exhibit Ex. J, # 4 Exhibit Ex. K, # 5 Exhibit Ex. L, # 6 Exhibit Ex. M, # 7 Exhibit Ex. N, # 8 Exhibit Ex. O, # 9 Proposed Order Proposed Order)(Long, Elizabeth) (Entered: 10/23/2023)	
324	10/23/2023	SEALED RESPONSE to Motion re 257 OPPOSED SEALED MOTION in Limine filed by Entropic Communications, LLC. (Attachments: # 1 SEALED Declaration of Michael T. Pieja, # 2 Exhibit P - SEALED Goldberg Rpt (excerpts), # 3 Exhibit Q - SEALED Interrog Resp (excerpts), # 4 Proposed Order)(Pieja, Michael) (Entered: 10/23/2023)	
325	10/25/2023	REDACTION to 311 Sealed Response to Motion, FOR LEAVE TO FILE OUT OF TIME PLAINTIFFS MOTION TO COMPEL by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Exhibit, # 7 Exhibit, # 8 Proposed Order)(Long, Elizabeth) (Entered: 10/25/2023)	
326	10/25/2023	REDACTION to 312 Sealed Response to Motion, to Compel Testimony and Documents Improperly Withheld as Privilege by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, # 6 Proposed Order)(Long, Elizabeth) (Entered: 10/25/2023)	
327	10/30/2023	REDACTION to 323 Sealed Response to Motion, MOTION IN LIMINE by Charter Communications, Inc.. (Attachments: # 1 Affidavit/Declaration Long Decl ISO Charter Response to Entropic's MILs, # 2 Exhibit Ex. I, # 3 Exhibit Ex. J, # 4 Exhibit Ex. K, # 5 Exhibit Ex. L, # 6 Exhibit Ex. M, # 7 Exhibit Ex. N, # 8 Exhibit Ex. O, # 9 Proposed Order Proposed Order)(Long, Elizabeth) (Entered: 10/30/2023)	
328	10/30/2023	RESPONSE in Opposition re 287 OPPOSED MOTION for Leave to File Out of Time Plaintiff's Supplemental Motion to Strike Opinions of Christopher Bakewell filed by Charter Communications, Inc.. (Attachments: # 1 Proposed Order)(Long, Elizabeth) (Entered: 10/30/2023)	
329	10/30/2023	SEALED RESPONSE to Motion re 289 MOTION to Strike Supplemental Motion to Strike Opinions of Christopher Bakewell filed by Charter Communications, Inc. (Attachments: # 1 Affidavit/Declaration Long Decl ISO Charter Opp'n to Motion to Strike Bakewell, # 2 Exhibit Ex. A, # 3 Exhibit Ex. B, # 4 Exhibit Ex. C, # 5 Exhibit Ex. D, # 6 Exhibit Ex. E, # 7 Exhibit Ex. F, # 8 Proposed Order Proposed Order)(Long, Elizabeth) (Entered: 10/30/2023)	
330	10/30/2023	RESPONSE in Opposition re 302 OPPOSED MOTION for Leave	

#	Date	Proceeding Text	Source
		to Serve Mr. Dell's Third Supplemental Expert Report Out of Time filed by Charter Communications, Inc.. (Attachments: # 1 Proposed Order Proposed Order)(Long, Elizabeth) (Entered: 10/30/2023)	
331	10/30/2023	SEALED ADDITIONAL ATTACHMENTS to Main Document: 330 Response in Opposition to Motion, (Attachments: # 1 Exhibit Ex. C, # 2 Exhibit Ex. D, # 3 Exhibit Ex. E)(Long, Elizabeth) (Entered: 10/30/2023)	
332	10/30/2023	REDACTION to 324 Sealed Response to Motion, by Entropic Communications, LLC. (Attachments: # 1 Declaration of Michael T. Pieja, # 2 Exhibit P - Goldberg Rpt (excerpts), # 3 Exhibit Q - Filed Under Seal, # 4 Proposed Order)(Pieja, Michael) (Entered: 10/30/2023)	
333	10/31/2023	Sealed Document. Joint Proposed Pretrial Order (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I)(Shimota, James) (Entered: 10/31/2023)	Events since last full update

Patents

Number	Title	Issued	Class	Subclass
8,223,775	Architecture for a flexible and high-performance gateway cable modem	07/17/2012	370	401
8,284,690	Receiver determined probe	10/09/2012	370	252
8,792,008	Method and apparatus for spectrum monitoring	07/29/2014	348	192
9,210,362	Wideband tuner architecture	12/08/2015	1	1
9,825,826	Method and apparatus for spectrum monitoring	11/21/2017	1	1
10,135,682	Method and system for service group management in a cable network	11/20/2018	1	1

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End of Document



User Name: Manuel Saldana
Date and Time: Tuesday, October 31, 2023 11:24:00AM EDT
Job Number: 209365443

Documents (2)

1. *Entropic Communs., LLC v. Charter Communs., Inc., 2023 U.S. Dist. LEXIS 152825*

Client/Matter: -None-
Search Terms: 9,210,362
Search Type: Natural Language
Narrowed by:

Content Type	Narrowed by
Cases	-None-

2. *Entropic Commc'ns, LLC v. Charter Commc'ns, Inc., 2023 U.S. Dist. LEXIS 109786*

Client/Matter: -None-
Search Terms: 9,210,362
Search Type: Natural Language
Narrowed by:

Content Type	Narrowed by
Cases	-None-

Neutral
As of: October 31, 2023 3:24 PM Z

Entropic Communs., LLC v. Charter Communs, Inc.

United States District Court for the Eastern District of Texas, Marshall Division

August 29, 2023, Decided; August 29, 2023, Filed

CIVIL ACTION NO. 2:22-CV-00125-JRG

Reporter
2023 U.S. Dist. LEXIS 152925 *; 2023 WL 5613185

ENTROPIC COMMUNICATIONS, LLC, Plaintiff, v. CHARTER COMMUNICATIONS, INC., Defendant.

Prior History: Entropic Commc'ns, LLC v. Charter Commc'ns, Inc., 2023 U.S. Dist. LEXIS 109706 (E.D. Tex., June 26, 2023)

Core Terms

consolidation, argues, cases

Counsel: **[*1]** For Entropic Communications, LLC, Plaintiff: Darlene Fae Ghavimi, LEAD ATTORNEY, K&L Gates, LLP, Austin, TX; James A Shimota, LEAD ATTORNEY, Jason A Engel, Katherine L. Allor, K&L Gates LLP - Chicago, Chicago, IL; Andrea Leigh Fair, Jack Wesley Hill, Ward, Smith & Hill, PLLC, Longview, TX; Connor James Meggs, K&L Gates LLP, Los Angeles, CA; Courtney Neufeld, Nicholas F. Lenning, K&L Gates LLP, Seattle, WA; George C Summerfield, K & L Gates LLP - Chicago, Chicago, IL; Kenneth H. Bridges, Bridges IP Consulting, Nashville, TN; Matthew Alexander Blair, K&L Gates, Austin, TX; Peter E. Soskin, K&L Gates LLP - San Francisco, San Francisco, CA; Samuel Patrick Richey, K&L Gates LLP, Chicago, IL.

For Charter Communications, Inc., Defendant: Daniel Reisner, Palak Mayani Parikh, LEAD ATTORNEYS, Albert John Boardman, Elizabeth Anne Long, Melissa A. Brown, Arnold & Porter Kaye Scholer LLP, New York, NY; Paul Isaac Margulies, LEAD ATTORNEY, Amy L DeWitt, Arnold & Porter Kaye Scholer, LLP - Wash DC, Washington, DC; David S Benyacar, Kaye Scholer - New York, New York, NY; Deron R Dacus, The Dacus Firm, PC, Tyler, TX; Marc A Cohn, PRO HAC VICE, Arnold & Porter Kaye Scholer LLP, Washington, DC.

Judges: RODNEY GILSTRAP, **[*2]** UNITED STATES DISTRICT JUDGE.

Opinion by: RODNEY GILSTRAP

Opinion

MEMORANDUM OPINION AND ORDER

I. INTRODUCTION

Before the Court is Defendant Charter Communications, Inc.'s ("Charter") Opposed Motion to Consolidate this Action with No. 2:23-cv-00052-JRG and to Amend the Case Schedule (the "Motion"). (Dkt. No. 99.) In the Motion, Charter requests that the above-captioned case (the "First Action") be consolidated with the *Entropic Communications, LLC v. Charter Communications, Inc.*, Case No. 2:23-cv-052-JRG (the "Second Action") pursuant to Federal Rule of Civil Procedure 42(a). (Dkt. No. 99 at 1.) Plaintiff Entropic Communications, LLC ("Entropic") opposes the Motion. (Dkt. No. 113.) For the following reasons, the Court finds that the Motion should be **DENIED**.

II. BACKGROUND

Entropic filed the First Action on April 27, 2022. (Dkt. No. 1.) It asserts that Charter infringes six U.S. Patents, including U.S. Patent No. ***9,210,362*** (the "'362 Patent"). (Dkt. No. 15 at ¶ 1.) The First Action is set to for trial on December 4, 2023 (Dkt. No. 154.)

Entropic filed the Second Action on February 10, 2023. 2:23-cv-052-JRG, Dkt. No. 1. In this action, Entropic asserts that Charter infringes U.S. Patent Nos. 11,381,866 (the "'866 Patent") and 11,399,206 (the "'206 Patent"). 2:23-cv-052-JRG, Dkt. No. 11 at 2. These patents are from the same family as **[*3]** the '362 Patent from the First Action. (Dkt. No. 99 at 1.) Accordingly, the '362, '866, and '206 Patents share a specification and inventors, and have similar claims.

(*Id.*) The Second Action, which is currently consolidated with 2:23-cv-051-JRG, is set for trial on October 7, 2024. 2:23-cv-051-JRG, Dkt. No. 52.

III. LEGAL STANDARD

Under Rule 42(a), where actions involve a common question of law or fact, "the court *may* . . . consolidate the actions." ContentGuard Holdings, Inc. v. Google, Inc., Nos. 2:14-cv-00061-JRG, Nos. 2:13-cv-01112, 2014 U.S. Dist. LEXIS 51676, 2014 WL 1477670, at *4 (E.D. Tex. Apr. 15, 2014) (quoting Fed. R. Civ. P. 41(a)) (emphasis in original)). This rule "is permissive and vests a purely discretionary power in the district court." *Id.* (quoting Whiteman v. Pirie, 220 F.2d 914, 918 (5th Cir. 1955)).

IV. ANALYSIS

Charter argues that the Court should consolidate the First and Second Actions because the law and facts substantially overlap. (Dkt. No. 99 at 7.) The '362, '866, and '206 Patents share the same specification and inventors, and have similar claims. (*Id.* at 7-8.) Moreover, the Accused Products and Accused Services have the same definition in each Action. (*Id.* at 8.) Charter further argues that trying the First and Second cases separately will lead to jury confusion because the jury in the Second Action will be required to account for the events that occurred in the First Action. (*Id.* at 9-10.) Moreover, Charter argues, consolidation would avoid substantial **[*4]** inefficiencies, namely litigating claim splitting and issue preclusion in the Second Action. (*Id.* at 10-14.) Last, Charter argues that if the Court adopts Charter's proposed schedule, there is no prejudice to Entropic. (*Id.* at 14-15.) Under Charter's proposed schedule, the consolidated case would proceed to trial in April 2024. (Dkt. No. 99-1 at 1.) Charter argues that there would be no prejudice to Entropic because the shorter time-to-trial for the Second Action would offset the longer time-to-trial in the First Action. (Dkt. No. 99 at 14-15.) Charter further argues that there is no prejudice to Entropic because Entropic is a non-practicing entity seeking only money damages. (*Id.* at 14.)

In response, Entropic argues that it is not possible to assess whether consolidation would promote efficiency given that the Second Action is in its earliest stages. (Dkt. No. 113 at 4-7.) Further, Entropic argues that consolidation would force Entropic to present too many complex, technical issues to a jury, making the presentation of evidence even more difficult for the jury to grapple with. (*Id.* at 8-9.) Last, Entropic argues that any delay in trial in the First Action would be prejudicial. (*Id.* ***[*5]*** at 9-10.)

In reply Charter argues that Entropic's argument that consolidation would mean there is "too much material" in one case rings hollow because (1) Entropic previously indicated that "it would be amenable to consolidation" and (2) Entropic filed a case in California that included all eight patents from both the First and Second Actions here. (Dkt. No. 116 at 1 (citing Dkt. No. 113 at 2).) Moreover, Charter notes that Entropic does not dispute the risks of jury confusion. (*Id.* at 2.) Further, the fact that the cases are at different stages is the fault of Entropic, Charter argues. (*Id.* at 3-4.) Finally, Charter argues that there is minimal prejudice to Entropic because the delay in time-to-trial is for a specified length, and, in any event, any prejudice to Entropic is far outweighed by the prejudice of forcing Charter to litigate two very similar cases instead of just one. (*Id.* at 4-5.)

In sur-reply Entropic argues that it only ever stated that it would "consider" consolidation on the existing trial schedule. (Dkt. No. 118 at 1.) Moreover, the other cases that Entropic filed which include all eight patents from the First and Second Actions here, were not filed in front of this **[*6]** Court, but in front of a Court that does not have a tradition of one-week trials. (*Id.* at 1-2.)

The Court, in its discretion, finds that the First and Second Actions should not be consolidated. The cases are simply too far apart for it to be practical to consolidate them at this point. The First Action is nearing the end of expert discovery, while fact discovery is just opening in the Second Action. Further, Entropic should not have to delay in bringing its case to trial before a jury. *See* Koninklijke KPN N.V. v. Telefonaktiebolaget LM Ericsson, No. 2:21-CV-00113-JRG, 2022 U.S. Dist. LEXIS 222809, 2022 WL 17484264, at *2 (E.D. Tex. July 7, 2022) ("this Court has repeatedly found that a delay in recovering monetary damages is far from non-prejudicial") (quotations omitted).

The Court is sympathetic to Charter's concern that it should not have to litigate the same case twice, but this concern is overstated. It is the Court's expectation that discovery between these actions will overlap, such that discovery does not have to be wholly duplicative between the First and Second Actions. The Court also expects that the similarities between the patents-in-suit will simplify claim construction. Moreover, the Court will

instruct the jury and cabin party arguments to limit jury confusion, which is an inherent risk when any single case from a group of **[*7]** complex cases goes to trial. Charter may litigate claim-splitting and issue preclusion if it wishes. Entropic knew the risks of bringing two cases that cover similar subject matter and it is not unfair to Charter to ask it to defend itself.

It is not lost upon the Court that this ruling may require some additional costs that the parties (and the Court) must bear. However, these additional costs are, in the Court's view, insufficient to overcome the burdens of consolidating two cases that are at very different stages of development and readiness.

V. CONCLUSION

For the foregoing reasons, the Court finds that the Motion (Dkt. No. 99) should be and hereby is **DENIED**.

So ORDERED and SIGNED this 29th day of August, 2023.

/s/ Rodney Gilstrap

RODNEY GILSTRAP

UNITED STATES DISTRICT JUDGE

End of Document

Neutral
As of: October 31, 2023 3:24 PM Z

Entropic Commc'ns, LLC v. Charter Commc'ns, Inc.

United States District Court for the Eastern District of Texas, Marshall Division

June 26, 2023, Decided; June 26, 2023, Filed

CASE NO. 2:22-CV-00125-JRG

Reporter
2023 U.S. Dist. LEXIS 109786 *; 2023 WL 4181266

ENTROPIC COMMUNICATIONS, LLC, Plaintiff, v. CHARTER COMMUNICATIONS, INC., Defendant.

Subsequent History: Motion denied by, Without prejudice Entropic Commc'ns, LLC v. Charter Commc'ns, Inc., 2023 U.S. Dist. LEXIS 152927 (E.D. Tex., Aug. 29, 2023)

Motion denied by Entropic Communs., LLC v. Charter Communs, Inc., 2023 U.S. Dist. LEXIS 152925 (E.D. Tex., Aug. 29, 2023)

Related proceeding at Entropic Commc'ns, LLC v. Charter Commc'ns, Inc., 2023 U.S. Dist. LEXIS 152924 (E.D. Tex., Aug. 29, 2023)

Petition denied by In re Charter Commc'ns, Inc., 2023 U.S. App. LEXIS 23486 (Fed. Cir., Sept. 5, 2023)

Core Terms

probe, cable, modem, networking, plurality, engine, signal, parameters, specification, channels, processor, functions, television, digitized, node, proposed construction, comprising, recites, metric, argues, terms, module, ordinary meaning, plain meaning, patent, frequencies, indefiniteness, composite, messages, profile

Counsel: **[*1]** For Entropic Communications, LLC, Plaintiff: Darlene Fae Ghavimi, LEAD ATTORNEY, K&L Gates, LLP, Austin, TX; James A Shimota, LEAD ATTORNEY, Jason A Engel, Katherine L. Allor, K&L Gates LLP - Chicago, Chicago, IL; Andrea Leigh Fair, Jack Wesley Hill, Ward, Smith & Hill, PLLC, Longview, TX; Connor James Meggs, K&L Gates LLP, Los Angeles, CA; Courtney Neufeld, Nicholas F. Lenning, K&L Gates LLP, Seattle, WA; George C Summerfield, K & L Gates LLP - Chicago, Chicago, IL; Kenneth H. Bridges, Bridges IP Consulting, Nashville, TN; Matthew Alexander Blair, K&L Gates, Austin, TX; Peter E. Soskin, K&L Gates LLP - San Francisco, San Francisco, CA; Samuel Patrick Richey, K&L Gates LLP, Chicago, IL.

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Judges: RODNEY GILSTRAP, **[*2]** UNITED STATES DISTRICT JUDGE.

Opinion by: RODNEY GILSTRAP

Opinion

CLAIM CONSTRUCTION MEMORANDUM OPINION AND ORDER

Before the Court is the Opening Claim Construction Brief (Dkt. No. 97) filed by Plaintiff Entropic Communications, LLC ("Plaintiff" or "Entropic"). Also before the Court are the Responsive Claim Construction Brief (Dkt. No. 104) filed by Defendant Charter Communications, Inc. ("Defendant" or "Charter") and Plaintiff's reply (Dkt. No. 110). The Court held a hearing on June 13, 2023.

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I. BACKGROUND

Plaintiff alleges infringement of United States Patents No. 8,223,775 ("the '775 Patent"), 8,792,008 ("the '008 Patent"), 9,825,826 ("the '826 Patent"), 8,284,690 ("the '690 Patent"), **[*4]** ***9,210,362*** ("the '362 Patent"), and 10,135,682 ("the '682 Patent") (collectively, the "patents-in-suit"). (Dkt. 97, Exs. 1-6.)

II. LEGAL PRINCIPLES

It is understood that "[a] claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention." *Burke, Inc. v. Bruno Indep. Living Aids, Inc.*, 183 F.3d 1334, 1340 (Fed. Cir. 1999). Claim construction is an issue of law for the court to decide. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970-71 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370, 116 S. Ct. 1384, 134 L. Ed. 2d 577 (1996).

"In some cases, however, the district court will need to look beyond the patent's intrinsic evidence and to consult extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period." *Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 135 S. Ct. 831, 841, 190 L. Ed. 2d 719 (2015) (citation omitted). "In cases where those subsidiary facts are in dispute, courts will need to make subsidiary factual findings about that extrinsic evidence. These are the 'evidentiary underpinnings' of claim construction that we discussed in *Markman*, and this subsidiary factfinding must be reviewed for clear error on appeal." *Id.* (citing *517 U.S. 370*).

To ascertain the meaning of claims, courts look to three primary sources: the claims, the specification, and the prosecution history. *Markman*, 52 F.3d at 979. The **[*5]** specification must contain a written description of the invention that enables one of ordinary skill in the art to make and use the invention. *Id.* A patent's claims must be read in view of the specification, of which they are a part. *Id.* For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. *Id.* "One purpose for examining the specification is to determine if the patentee has limited the scope of the claims." *Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000).

Nonetheless, it is the function of the claims, not the specification, to set forth the limits of the patentee's invention. Otherwise, there would be no need for claims. *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). The patentee is free to be his own lexicographer, but any special definition given to a word must be clearly set forth in the specification. *Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1388 (Fed. Cir. 1992). Although the specification may indicate that certain embodiments are preferred, particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. *Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994).

This Court's claim construction analysis is substantially guided by the Federal Circuit's decision in *Phillips v. AWH Corporation*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). In *Phillips*, the court set forth several **[*6]** guideposts that courts should follow when construing claims. In particular, the court reiterated that "the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Id. at 1312* (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To that end, the words used in a claim are generally given their ordinary and customary meaning. *Id.* The ordinary and customary meaning of a claim term "is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id. at 1313*. This principle of patent law flows naturally from the recognition that inventors are usually persons who are skilled in the field of the invention and that patents are addressed to, and intended to be read by, others skilled in the particular art. *Id.*

Despite the importance of claim terms, *Phillips* made clear that "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.* Although the claims themselves may provide guidance as to the meaning of particular terms, those terms **[*7]** are part of "a fully integrated written instrument." *Id. at 1315* (quoting *Markman*, 52 F.3d at 978). Thus, the *Phillips* court emphasized the specification as being the primary basis for construing the claims. *Id. at 1314-17*. As the Supreme Court stated long ago, "in case of doubt or ambiguity it is proper in all cases to refer back to the descriptive portions of the specification to aid in solving the doubt or in ascertaining the true intent and meaning of the

language employed in the claims." Bates v. Coe, 98 U.S. 31, 38, 25 L. Ed. 68, 1879 Dec. Comm'r Pat. 365 (1878). In addressing the role of the specification, the Phillips court quoted with approval its earlier observations from Renishaw PLC v. Marposs Societa' per Azioni, 158 F.3d 1243, 1250 (Fed. Cir. 1998):

> Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.

Phillips, 415 F.3d at 1316. Consequently, Phillips emphasized the important role the specification plays in the claim construction process.

The prosecution history also continues to play an important role in claim interpretation. Like the specification, the prosecution history helps to demonstrate how the inventor **[*8]** and the United States Patent and Trademark Office ("PTO") understood the patent. Id. at 1317. Because the file history, however, "represents an ongoing negotiation between the PTO and the applicant," it may lack the clarity of the specification and thus be less useful in claim construction proceedings. *Id.* Nevertheless, the prosecution history is intrinsic evidence that is relevant to the determination of how the inventor understood the invention and whether the inventor limited the invention during prosecution by narrowing the scope of the claims. *Id.*; *see* Microsoft Corp. v. Multi-Tech Sys., Inc., 357 F.3d 1340, 1350 (Fed. Cir. 2004) (noting that "a patentee's statements during prosecution, whether relied on by the examiner or not, are relevant to claim interpretation").

Phillips rejected any claim construction approach that sacrificed the intrinsic record in favor of extrinsic evidence, such as dictionary definitions or expert testimony. The *en banc* court condemned the suggestion made by Texas Digital Systems, Inc. v. Telegenix, Inc., 308 F.3d 1193 (Fed. Cir. 2002), that a court should discern the ordinary meaning of the claim terms (through dictionaries or otherwise) before resorting to the specification for certain limited purposes. Phillips, 415 F.3d at 1319-24. According to Phillips, reliance on dictionary definitions at the expense of the specification had the effect of "focus[ing] the **[*9]** inquiry on the abstract meaning of words rather than on the meaning of claim terms within the context of the patent." Id. at 1321. Phillips emphasized that the patent system is based on the proposition that the claims cover only the invented subject matter. *Id.*

Phillips does not preclude all uses of dictionaries in claim construction proceedings. Instead, the court assigned dictionaries a role subordinate to the intrinsic record. In doing so, the court emphasized that claim construction issues are not resolved by any magic formula. The court did not impose any particular sequence of steps for a court to follow when it considers disputed claim language. Id. at 1323-25. Rather, Phillips held that a court must attach the appropriate weight to the intrinsic sources offered in support of a proposed claim construction, bearing in mind the general rule that the claims measure the scope of the patent grant.

The Supreme Court of the United States has "read 35 U.S.C.I.S. 112, ¶ 2 to require that a patent's claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty." Nautilus, Inc. v. Biosig Instruments, Inc., 572 U.S. 898, 910, 134 S. Ct. 2120, 2129, 189 L. Ed. 2d 37 (2014). "A determination of claim indefiniteness is a legal conclusion that is drawn from the court's **[*10]** performance of its duty as the construer of patent claims." Datamize, LLC v. Plumtree Software, Inc., 417 F.3d 1342, 1347 (Fed. Cir. 2005) (citations and internal quotation marks omitted), *abrogated on other grounds by* Nautilus, 572 U.S. 898. "Indefiniteness must be proven by clear and convincing evidence." Sonix Tech. Co. v. Publ'ns Int'l, Ltd., 844 F.3d 1370, 1377 (Fed. Cir. 2017).

III. AGREED TERMS

In their April 4, 2023 P.R. 4-3 Joint Claim Construction and Prehearing Statement, the parties submitted the following agreed-upon constructions (Dkt. No. 84, at 1):

Go to table2

IV. DISPUTED TERMS IN U.S. PATENT NO. 8,223,775

The '775 Patent, titled "Architecture for a Flexible and High-Performance Gateway Cable Modem," issued on July 17, 2012, and bears a filing date of September 30, 2003. The Abstract of the '775 Patent states:

> A cable modem system and architecture. A cable modem engine performs all cable modem

functions, **[*11]** and a data networking engine performs all data and home networking functions. The cable modem engine is completely partitioned from the data networking engine. DOCSIS and VoIP functionality is implemented in the cable modem engine. The VoIP functionality may be in accordance with the Packet-Cable specification. The data networking functionality provided by the data networking engine may be in accordance with the CableHome specification.

1. "a data networking engine implemented in a first circuit that includes at least one processor . . ." and "a cable modem engine implemented in a second circuit that includes at least one processor . . ."

Go to table3

(Dkt. No. 84, at A-1; Dkt. No. 97, at 6; Dkt. No. 104, at 4; Dkt. No. 115, Ex. **[*12]** A, at 1.)

(a) The Parties' Positions

Plaintiff argues that "data networking" and "cable modem" were well-known phrases at the time of the invention and that the generic word "engine," as modified by the phrases "data networking" and "cable modem," would have been readily understood by a person of ordinary skill in this art. (Dkt. No. 97, at 6-7.) Plaintiff also argues that Defendant's indefiniteness arguments should be rejected because "electrical engineers routinely design subcomponents of consumer electronics, even if the components reside on the same chip," and "[a] POSITA would have no trouble determining where one circuit begins and another ends, because integrating functional blocks on 'a chip' does not render them indistinguishable." (*Id.*, at 8.)

Defendant responds that "[t]here is no disclosure of a DNE or CME implemented in any circuit, much less two circuits which are 'separate' from one another." (Dkt. No. 104, at 5.) Defendant argues that Plaintiff cannot simply chose whatever meaning or "level" of the word "circuit" suits its infringement contentions. (*See id.*, at 6-8.)

Plaintiff replies that the term "circuit" is readily understandable and that the specification discloses **[*13]** separation of functions. (Dkt. No. 110, at 1.)

At the June 13, 2023 hearing, Plaintiff argued that although the functionality of the first circuit and the second circuit must be separate, this does not necessarily require physical separation. Defendant responded that it is *not* arguing that the first circuit and the second circuit must be on separate *chips*, but the problem, Defendant argued, is that this claim uses "circuit" in a subjective way and, as a result, there is no way for a person of skill in the art to know if these limitations are satisfied.

(b) Analysis

Claim 18 of the '775 Patent recites (emphasis added):

> 18. A cable modem system comprising:
>
> *a data networking engine implemented in a first circuit that includes at least one processor*, the data networking engine programmed with software that when executed by the at least one processor of the first circuit causes the data networking engine to perform home networking functions including interfacing with customer provided equipment;
>
> *a cable modem engine implemented in a second circuit that includes at least one processor*, the second circuit being *separate* from the first circuit, the cable modem engine programmed with software that when executed **[*14]** by the at least one processor of the second circuit causes the cable modem engine to perform cable modem functions other than the home networking functions performed by the data networking engine, the cable modem functions including interfacing with cable media, and the cable modem engine configured to enable upgrades to its software in a manner that is independent of upgrades to the software of the data networking engine, the cable modem engine including a DOCSIS controller and a DOCSIS MAC processor, the DOCSIS MAC processor configured to process downstream PDU packets and forward the processed packets directly to the data networking engine without the involvement of the DOCSIS controller in order to boost downstream throughput; and
>
> a data bus that connects the data networking engine to the cable modem engine, wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine.

The specification discloses "functional partitioning" and also contrasts the disclosed cable modem system with "current stand-alone cable modem chips":

> Functional Partitioning. Cable modem 100 completely partitions **[*15]** data networking functions . . . from DOCSIS cable modem functionality.
>
> * * *
>
> A chip implementing cable modem system 100 will have only a small incremental hardware cost/functional increase over current stand-alone cable modem chips.

'775 Patent at 4:13-16 & 4:58-60; *see id.* at FIGS. 1 and 2 (illustrating data networking engine ("DNE") 120 and cable modem engine ("CME") 110).

Such disclosure regarding "functionality" is consistent with the technical dictionary cited by Defendant's expert, which defines "circuit" as:

> 1. Any path that can carry electrical current. 2. A combination of electrical components interconnected to perform a particular task. At one level, a computer consists of a single circuit; at another, it consists of hundreds of interconnected circuits.

(Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl., App'x C, *Microsoft Computer Dictionary* 99 (5th ed. 2002).)

The specification and this extrinsic evidence are thus consistent with Plaintiff's interpretation that the phrases "first circuit" and "second circuit" are not limited to specific established structures but rather refer to interconnected electrical components that implement the data networking engine functionality and the cable modem **[*16]** engine functionality. *Cf. Linear Tech. Corp. v. Impala Linear Corp., 379 F.3d 1311, 1320 (Fed. Cir. 2004)* ("when the structure-connoting term 'circuit' is coupled with a description of the circuit's operation, sufficient structural meaning generally will be conveyed to [POSITAs]").

Further, although the claim requires "the second circuit being separate from the first circuit," the "first circuit" and "second circuit" need not be physically separated, such as on separate chips, for example. *Cf. Linear Tech. Corp. v. Int'l Trade Comm'n, 566 F.3d 1049, 1055 (Fed. Cir. 2009)* ("We agree with the Commission's construction of 'second circuit' and 'third circuit,' defining the terms broadly to not require entirely separate and distinct circuits."). This is true even if the disclosed cable modem system 100 is implemented as a "System-on-a-Chip" ("SoC") because even if the SoC is considered to be a single "circuit" (*see* Dkt. No. 97, at 8; *see also* Dkt. No. 104, Ex. 2, May 4, 2023 Kramer dep. at 127:13-22 ("a System on a Chip can be considered an integrated circuit")), this circuit can itself be understood as being composed of multiple circuits. The opinions of Defendant's expert to the contrary are unpersuasive. (*See* Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶¶ 64-68.)

Thus, Defendant does not meet its burden to show any lack of reasonable **[*17]** certainty. *Nautilus, 572 U.S. at 910*. The *Dow* and *Teva* cases cited by Defendant do not compel otherwise because, for example, the present case does not involve different potential methods of measurement. *See Dow Chemical Co. v. Nova Chemicals Corp. (Canada), 803 F.3d 620, 631, 634 (Fed. Cir. 2015)* (finding indefiniteness as to "a slope of strain hardening coefficient greater than or equal to 1.3"); ***see also*** *Teva Pharmaceuticals USA, Inc. v. Sandoz, Inc., 789 F.3d 1335, 1338, 1344-45 (Fed. Cir. 2015)* (finding indefiniteness as to "a molecular weight of about 5 to 9 kilodaltons").

The Court therefore hereby expressly rejects Defendant's indefiniteness argument. Defendant presents no alternative proposed constructions, and no further construction is necessary.

The Court accordingly hereby construes **"a data networking engine implemented in a first circuit that includes at least one processor . . ."** and **"a cable modem engine implemented in a second circuit that includes at least one processor . . ."** to have their **plain meaning. 2. "data bus"**

Go to table4

(Dkt. No. 84, at A-2; Dkt. No. 97, at 9; Dkt. No. 104, at 8; Dkt. No. 115, Ex. A, at 2.)

(a) The Parties' Positions

Plaintiff argues that the meaning of "data bus" is well known to persons of ordinary skill in the **[*18]** art. (Dkt. No. 97, at 9.)

Defendant responds that, in light of the prosecution history, "the 'data bus' limitation is irreconcilable with the 'completely partitioned' limitation, and claim 18 is therefore indefinite." (Dkt. No. 104, at 8 (citation omitted).)

Plaintiff replies that Defendant's argument is untenable because "[p]rosecution history disclaimers operate to narrow what would otherwise fall within a claim; they do not operate to invalidate claims by eliminating elements

textually present." (Dkt. No. 110, at 2.)

At the June 13, 2023 hearing, the parties argued this term together with the above-discussed ". . . in a first circuit . . ." and ". . . in a second circuit . . ." terms.

(b) Analysis

Defendant does not dispute that "data bus" is a well-known term in the relevant art. (*See* Dkt. No. 97, Ex. 10, *The IEEE Standard Dictionary of Electrical and Electronics Terms* 252 (defining "data bus" as "a bus used to communicate data to and from a processing unit or a storage device").)

The parties' dispute pertains not to the term "data bus" in isolation but rather to the accompanying "wherein" clause, which the parties present as a distinct disputed term and which is addressed separately **[*19]** below.

The Court therefore hereby construes **"data bus"** to have its **plain meaning**.

3. "wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine"

Go to table5

(Dkt. No. 84, at A-4; Dkt. No. 97, at 10; Dkt. No. 104, at 8; Dkt. No. 115, Ex. A, at 2-3.)

(a) The Parties' Positions

Plaintiff argues:

> The disputed claim language explicitly recites that the functions of the DNE [(data networking engine)] and CME [(cable modem engine)] are partitioned. This distinction is key because functions can be partitioned in hardware, software, or both. Functional partitioning is explicitly described in the specification as 'localizing' the cable modem and data networking functions in the separate **[*20]** engines:
>
> * * *
>
> A POSITA would understand that connecting the DNE and CME (e.g., via a data bus) does not eliminate the compartmentalization of their respective functions."

(Dkt. No. 97, at 10 (citations omitted).)

Defendant responds as to this term together with the term "data bus," which is addressed above. (*See* Dkt. No. 104, at 8.) Plaintiff replies likewise. (*See* Dkt. No. 110, at 2-3.)

At the June 13, 2023 hearing, the parties argued this term together with the above-discussed ". . . in a first circuit . . ." and ". . . in a second circuit . . ." terms.

(b) Analysis

Claim 18 of the '775 Patent recites (emphasis added):

> 18. A cable modem system comprising:
>
> a data networking engine implemented in a first circuit that includes at least one processor, the data networking engine programmed with software that when executed by the at least one processor of the first circuit causes the data networking engine to perform home networking functions including interfacing with customer provided equipment;
>
> a cable modem engine implemented in a second circuit that includes at least one processor, the second circuit being separate from the first circuit, the cable modem engine programmed with software that when executed **[*21]** by the at least one processor of the second circuit causes the cable modem engine to perform cable modem functions other than the home networking functions performed by the data networking engine, the cable modem functions including interfacing with cable media, and the cable modem engine configured to enable upgrades to its software in a manner that is independent of upgrades to the software of the data networking engine, the cable modem engine including a DOCSIS controller and a DOCSIS MAC processor, the DOCSIS MAC processor configured to process downstream PDU packets and *forward the processed packets directly to the data networking engine* without the involvement of the DOCSIS controller in order to boost downstream throughput; and
>
> a *data bus* that connects the data networking engine to the cable modem engine, *wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine.*

The specification discloses "localizing" the *functions*:

> Functional Partitioning. Cable modem 100 completely partitions data networking *functions* (advanced bridging/routing, NAT/firewall, VPN, web server and **[*22]** CableHome applications) from DOCSIS cable modem *functionality*. This is accomplished by localizing data networking *functions* in the data networking engine processor and localizing cable modem *functions* in the cable modem engine processor.

'775 Patent at 4:13-19 (emphasis added). Further, the claim itself recites that the cable modem engine "forward[s] the processed packets directly to the data networking engine," thus implying that such communication is not inconsistent with the cable modem engine and the data networking engine being "completely partitioned" from one another. *See id.* at Figs. 1 & 2 (illustrating data path 118 between CME and DNE); *see also id.* at 3:15-17 ("DS PDU packets are forwarded by [the DOCSIS MAC processor] directly to [DNE] 120 along path 118, bypassing controller 116").

The prosecution history cited by Defendant does not compel otherwise. The patentee distinguished the "Brooks" reference (United States Patent Application Publication No. 2001/0039600) as follows:

> [T]he Office Action make the conclusion statement [s*ic*] that "the data networking engine and cable modem engines are represented in Figures 1 and 2 of the [Brooks] reference" . . . . However, Applicant is uncertain **[*23]** how any reasonable interpretation of these Figures can provide correspondence. For example, Figure 2 of [Brooks] discloses only two processors, each of which, therefore, must correspond to the claimed data-networking and cable-modem engines. However, the discussion of Figure 2 makes clear that the cable modem functions are performed by CMAC unit 224 . . . . Therefore, in order for the cable modem engine to contain a processor and perform the CMAC functions as claimed, the cited cable modem engine must include circuitry to connect the processors with the CMAC unit. Because available *connecting circuitry would be shared with the other processor*, Applicant is uncertain how the asserted cable modem engine and home networking engine can be completely partitioned as claimed.

(Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl., App'x G, Apr. 5, 2010 Response to Final Office Action, at 6 (ENTROPIC_CHARTER_0000108) (p. 236 of 290 of Ex. 8) (emphasis added).)

After an advisory action by the examiner, the patentee explained further, distinguishing Brooks as using processors that were not functionally separate:

> The Examiner's apparent designation of the first processor 102 in Brooks '600 as the "data **[*24]** networking engine," and the second processor 104 and the CMAC/CPHY block (114, 118, 224 and 228) as the "cable modem engine," further does not square with the claim 1 feature that "the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine," and the claim 15 feature of "partitioning the data networking engine from the cable modem engine so that the data and home networking functionality is completely decoupled from the DOCSIS and VOOP functionality." This is because the CMAC/CPHY block (114, 118, 224 and 228) communicates with both the processors 102 and 104 by sharing the same data paths and sharing the same direct memory access controller. (See peripheral bus 112 — bridge 110 — system bus 108 in Fig. 1 and APB 214 — OMA Controller/ASB-APB Bridge 212 — ASB 210 in Fig. 2, and paragraphs 0034 and 0035).
>
> Further, accepting the Examiner's assertion that first processor 102 handles data networking *functionality*, and considering the description of paragraphs 0025 and 0026 that processor 102 is programmed to implement the desired MAC *functionality* (which would include typical DOCSIS MAC **[*25]** *functionality*), leads to a conclusion that the Brooks '600 processor 102 does not implement a complete partitioning or a completely decoupled arrangement of the data networking engine from the cable modem engine.
>
> Thus, Brooks '600 does not provide the complete partitioning or completely decoupled arrangement of the data networking engine from the cable modem engine that the Examiner apparently asserts it does.

(*Id.*, June 7, 2010 Response to Final Office Action, at 9 (ENTROPIC_CHARTER_0000134) (p. 254 of 290 of Ex. 8) (emphasis added); *see id.*, at 7-9 (ENTROPIC_CHARTER_0000132-34) (pp. 252-54 of 290 of Ex. 8).)

The patentee thus distinguished Brooks as lacking *functional* separation because what the examiner identified as the cable modem engine in Brooks required

interaction with the "CMAC unit," and, the patentee argued, such interaction involved circuitry that was shared with what the examiner identified as the data networking engine in Brooks. (*See id.*) Thus, no relevant disclaimer is apparent, and in particular the patentee did not disclaim having a data bus that connects the data networking engine to the cable modem engine, as recited in above-reproduced Claim 1 of the '775 Patent. *See Omega Eng'g Inc. v. Raytek Corp., 334 F.3d 1314, 1324 (Fed. Cir. 2003)* ("prosecution **[*26]** disclaimer promotes the public notice function of the intrinsic evidence and protects the public's reliance on *definitive* statements made during prosecution") (emphasis added); *see also id. at 1325-26* ("for prosecution disclaimer to attach, our precedent requires that the alleged disavowing actions or statements made during prosecution be both *clear and unmistakable*") (emphasis added).

The Court therefore hereby expressly rejects Defendant's proposal that the cable modem engine and the data networking engine cannot share any connecting circuitry, data paths, or memory devices.

The Court accordingly hereby construes **"wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine"** to mean **"wherein the cable modem engine and the data networking engine are not necessarily physically separate but are functionally separate such that the cable modem functions are performed only by the cable modem engine and the home networking functions are performed only by the data networking engine."**

4. "DOCSIS functions"

Go to table6

(Dkt. No. 84, at A-5; Dkt. No. 97, at 11; Dkt. No. 104, at 8; Dkt. No. 115, Ex. A, at 3.)

(a) The Parties' Positions

Plaintiff argues that Defendant's proposal is contrary to the doctrine of claim differentiation. (Dkt. No. 97, at 12.)

Defendant responds:

> According to claim 19, all DOCSIS functions are localized in the CME. However, as explained . . . above, the specification explains that the sine qua non of a CME is that it 'performs all cable modem functions' including 'the entire DOCSIS cable modem functionality.' Accordingly, claim 19 is redundant and does not further limit the scope of claim 18. Otherwise, the term 'cable modem engine' is indefinite.

(Dkt. No. 104, at 9.)

Plaintiff replies that there is no redundancy because "Claim 18 recites the broader 'cable modem functions,' which does not necessarily have the same scope as 'all *DOCSIS* functions,' referring to the DOCSIS standard." (Dkt. No. 110, at 3.)

At the June 13, 2023 hearing, the parties argued this term together with the above-discussed ". . . in a first circuit . . ." and ". . . in a second circuit . . ." terms.

(b) Analysis **[*28]**

Claim 19 of the '775 Patent depends from Claim 18 and recites:

> 19. A cable modem system as claimed in claim 18, wherein all DOCSIS functions are localized in the cable modem engine.

Plaintiff applies the doctrine of claim differentiation, arguing:

> Claim 18 states that the CME comprises a processor, programmed with software, that when executed causes the CME to perform "cable modem functions other than the home networking functions performed by the [DNE]." Dependent claim 19 increases the burden on the CME—"all DOCSIS functions are localized in the [CME]." Logically, claim 18 does not require that each and every DOCSIS function be executed by the circuitry of the CME, while claim 19 does.

(Dkt. No. 97, at 12.)

As a general matter, "[c]laim differentiation is 'not a hard and fast rule,' but rather a presumption that will be overcome when the specification or prosecution history dictates a contrary construction." *GPNE Corp. v. Apple Inc., 830 F.3d 1365, 1371 (Fed. Cir. 2016).*

Defendant argues that this limitation set forth in Claim 19 is redundant (and thus does not imply the absence of such a limitation in Claim 18) because Claim 18, read in light of the specification, already requires this limitation. (*See* Dkt. No. 104, at 9.) Defendant argues that "cable modem **[*29]** engine" "is a phrase coined by the inventors" and "[i]f it does not refer to the components of a cable modem that perform all the cable modem

functions, then there is no way to know what it is." (*Id.*, at 9.)

Defendant cites disclosure in the Abstract that the CME "performs all cable modem functions" and "implements the entire DOCSIS cable modem functionality." '775 Patent at Abstract & 2:55-56. The Abstract, however, is not limiting, and the portion of the written description cited by Defendant does not purport to limit the entire claimed invention but rather describes a particular embodiment of "cable modem engine 110." *See* *Phillips*, 415 F.3d at 1323. Further, there is a "presumption that each claim in a patent has a different scope." *Comark Communs., Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998). The contrary opinion of Defendant's expert is unpersuasive. (*See* Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶ 36 (citing '775 Patent at 2:15-17 ("In one implementation, the VoIP functionality provided by the cable modem is in accordance with the PacketCable specification and the data networking functionality provided by the data networking engine is in accordance with the CableHome specification."), 2:23-24 ("Data and home networking functionality is provided by a data networking engine, **[*30]** and DOCSIS and VoIP functionality is provided by a cable modem engine.") & 4:19-21).)

The Court therefore hereby expressly rejects Defendant's attempted reliance on Claim 19 to arrive at a narrow interpretation of "cable modem engine" in Claim 18, and no further construction is necessary as to Claim 19. *See* *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997) ("Claim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement. It is not an obligatory exercise in redundancy."); *see also* *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) ("[D]istrict courts are not (and should not be) required to construe every limitation present in a patent's asserted claims."); *Finjan, Inc. v. Secure Computing Corp.*, 626 F.3d 1197, 1207 (Fed. Cir. 2010) ("Unlike *O2 Micro*, where the court failed to resolve the parties' quarrel, the district court rejected Defendants' construction."); *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1326 (Fed. Cir. 2012); *Summit 6, LLC v. Samsung Elecs. Co., Ltd.*, 802 F.3d 1283, 1291 (Fed. Cir. 2015); *Bayer Healthcare LLC v. Baxalta Inc.*, 989 F.3d 964, 977-79 (Fed. Cir. 2021).

The Court accordingly hereby construes **"DOCSIS functions"** to have its **plain meaning**.

5. "DOCSIS MAC processor" and "DOCSIS controller"

Go to table7

(Dkt. No. 84, at A-6; Dkt. No. 97, at 12; Dkt. No. 115, Ex. A, at 1-2.)

(a) The Parties' Positions

Plaintiff urges that Defendant's proposals would improperly limit these terms to specific exemplary embodiments described in the specification. (Dkt. No. 97, at 12.) Plaintiff also argues that Defendants have already agreed that these are *not* means-plus-function terms governed by *35 U.S.C. § 112*, ¶ 6. (*Id.*) Further, Plaintiff submits that "[t]he Federal Circuit and this Court have held that the terms 'processor' and 'controller' denote known classes of structures—generally understood to POSITAs." (*Id.* (citations omitted).)

Defendant responds that "[n]either the phrase 'DOCSIS MAC processor' nor 'DOCSIS controller' has a plain meaning." (Dkt. No. 104, at 9.) Defendant also argues that Plaintiff's proposed construction would either contradict the specification **[*32]** or "make it impossible to distinguish a DOCSIS MAC processor from a DOCSIS controller." (*Id.*, at 9-10.) Defendant urges that "[t]he only construction of DOCSIS MAC processor and DOCSIS controller that both comports with the specification and provides a basis for distinguishing between the two is a construction whereby each refers to the corresponding device described in the specification." (*Id.*, at 11.)

Plaintiff replies that "the claims themselves describe the functions of the DOCSIS MAC processor and DOCSIS controller," and "Charter has made no argument that the DOCSIS MAC processor and DOCSIS controller should be limited to the specific ARM-based embodiments disclosed in the specification." (Dkt. No. 110, at 3-4.)

At the June 13, 2023 hearing, Defendant submitted that the DOCSIS controller disclosed in the specification performs some MAC functions. Defendant argued that this makes it impossible to distinguish between a "DOCSIS MAC processor" and a "DOCSIS controller," which, in turn, Defendant argued makes it impossible to determine whether an accused instrumentality meets the limitation of "forward[ing] the processed packets

directly to the data networking engine without the involvement **[*33]** of the DOCSIS controller."

(b) Analysis

Claim 18 of the '775 Patent recites (emphasis added):

> 18. A cable modem system comprising:
>
> a data networking engine implemented in a first circuit that includes at least one processor, the data networking engine programmed with software that when executed by the at least one processor of the first circuit causes the data networking engine to perform home networking functions including interfacing with customer provided equipment;
>
> a cable modem engine implemented in a second circuit that includes at least one processor, the second circuit being separate from the first circuit, the cable modem engine programmed with software that when executed by the at least one processor of the second circuit causes the cable modem engine to perform cable modem functions other than the home networking functions performed by the data networking engine, the cable modem functions including interfacing with cable media, and the cable modem engine configured to enable upgrades to its software in a manner that is independent of upgrades to the software of the data networking engine, the cable modem engine including a *DOCSIS controller* and a *DOCSIS MAC processor*, the *DOCSIS MAC processor* ***[*34]*** configured to process downstream PDU packets and forward the processed packets directly to the data networking engine without the involvement of the *DOCSIS controller* in order to boost downstream throughput; and
>
> a data bus that connects the data networking engine to the cable modem engine, wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine.

The words "processor" and "controller" refer to known classes of structures in the relevant art, and the parties agree that "DOCSIS" (Data Over Cable Service Interface Specification) and DOCSIS "MAC" (Medium Access Control) have been well-known at all relevant times. (*See, e.g.*, Dkt. No. 97, Ex. 7, Apr. 14, 2023 Kramer Decl. at ¶ 84.)

Defendant proposes to limit these terms to the particular DOCSIS controller and DOCSIS MAC processor disclosed in the specification, but Defendant does not show any definition or disclaimer that would warrant a narrowing of these terms. *See* *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1367 (Fed. Cir. 2012) ("The patentee is free to choose a broad term and expect to obtain the full scope of its plain and ordinary meaning unless the patentee explicitly redefines the **[*35]** term or disavows its full scope.").

Moreover, other claims of the patent-in-suit can be considered. *See* *Phillips*, 415 F.3d at 1314. Claim 1 recites a "DOCSIS MAC processor" and a "DOCSIS controller," and Claim 12 depends from Claim 1 and recites that "the DOCSIS MAC processor is an ARM9TDMI-based RISC processor, and wherein the DOCSIS controller is an ARM940-based RISC processor." Because claim terms should be interpreted consistently throughout all of the claims of a particular patent, *id.*, the doctrine of claim differentiation weighs against limiting the "DOCSIS MAC processor" and a "DOCSIS controller" to ARM9TDMI, ARM940, or any other particular specific implementation.

The disclosure in the specification regarding "functional blocks" is also consistent with interpreting these terms broadly rather than limiting them to particular types of processors. *See* '775 Patent at 2:55-3:38; *see also* Dkt. No. 97, Ex. 7, Apr. 14, 2023 Kramer Decl. at ¶¶ 92-93.

Further, Defendant cites disclosure in which the DOCSIS controller is involved with MAC functions (*see* '775 Patent at 3:27-48), but although the claim requires a "DOCSIS MAC processor configured to . . . forward the processed packets directly to the data networking engine without the involvement **[*36]** of the DOCSIS controller," the absence of involvement of the DOCSIS controller in this particular operation does not preclude the DOCSIS controller from being involved with other MAC functions.

Finally, Defendant cites the opinions of its expert that a person of ordinary skill in the art would be unable to distinguish between a "DOCSIS MAC processor" and a "DOCSIS controller," but these opinions are unpersuasive, particularly given that DOCSIS is a well-established standard and that MAC is also a well-known term in the relevant art. (*See* Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶¶ 76-77.) Any remaining question regarding distinguishing between a "DOCSIS MAC processor" and a "DOCSIS controller" pertains to factual questions of infringement rather than any legal question for claim construction. *See* *PPC Indus. v. Guardian Indus. Corp.*, 156 F.3d 1351, 1355 (Fed. Cir.

1998) ("after the court has defined the claim with whatever specificity and precision is warranted by the language of the claim and the evidence bearing on the proper construction, the task of determining whether the construed claim reads on the accused product is for the finder of fact"); *see also* Acumed LLC v. Stryker Corp., 483 F.3d 800, 806 (Fed. Cir. 2007) ("[t]he resolution of some line-drawing problems . . . is properly left to the trier of **[*37]** fact") (citing PPG, 156 F.3d at 1355); Eon Corp. IP Holdings LLC v. Silver Spring Networks, Inc., 815 F.3d 1314, 1318-19 (Fed. Cir. 2016) (citing PPG, 156 F.3d at 1355; citing Acumed, 483 F.3d at 806).

The Court therefore hereby expressly rejects Defendant's proposed constructions, and no further construction is necessary. *See* U.S. Surgical, 103 F.3d at 1568; *see also* O2 Micro, 521 F.3d at 1362; Finisar, 524 F.3d at 1207; ActiveVideo, 694 F.3d at 1326; Summit 6, 802 F.3d at 1291; Bayer, 989 F.3d at 977-79.

The Court accordingly hereby construes **"DOCSIS MAC processor"** and **"DOCSIS controller"** to have their **plain meaning**.

V. DISPUTED TERMS IN U.S. PATENT NO. 9,825,826

The '826 Patent is a continuation of the '008 Patent.

Plaintiff submits: "The '826 and the '008 Patents disclose methods and apparatuses that can be implemented in Customer Premises Equipment (CPE) that enable the CPE to: receive a cable or satellite television signal, digitize said signal, determine a characteristic of the digitized signal, and then report the determined characteristic back to the source of the signal (*i.e.*, the network-based service providers) without interrupting normal customer service." (Dkt. No. 97 at 3.)

The '008 Patent, titled "Method and Apparatus for Spectrum Monitoring," issued on July 29, 2014, and bears an earliest priority date of September 8, 2011. The Abstract of the '008 Patent states:

> A system, such as a satellite reception assembly or customer premises gateway, may comprise an analog-to-digital converter operable to digitize a signal spanning an entire television spectrum (e.g., cable television **[*38]** spectrum or satellite television spectrum) comprising a plurality of television channels. The system may comprise a signal monitor operable to analyze a signal to determine a characteristic of the signal. The system may comprise a data processor operable to process a television channel to recover content carried on the television channel. The system may comprise a channelizer operable to select first and second portions of the signal, and concurrently output the first portion to the signal monitor and the second portion to the data processor.

6. "network management messages"

Go to table8

(Dkt. No. 84, at A-8; Dkt. No. 97, at 15; Dkt. No. 104, at 12; Dkt. No. 115, Ex. A, at 5.)

(a) The Parties' Positions

Plaintiff argues that "[t]he Court should construe this term according to its plain and ordinary meaning because 'network management message' is a plain English phrase that means exactly what it says," and "[t]he '826 Patent's specification confirms the **[*39]** phrase is meant to convey all its ordinary possibilities, in disclosing a list of exemplary types/uses of the messages." (Dkt. No. 97, at 15 (citations omitted).)

Defendant responds that Plaintiff attempts to encompass implementations in which the set-top box returns only a measured characteristic and nothing else to the headend, which Defendant argues is inconsistent with the claim requirement that "said measured characteristic is *different than* said network management messages." (Dkt. No. 104, at 12 (emphasis modified).)

Plaintiff replies that Defendant improperly relies on claim language in the parent '008 Patent in an attempt to limit Claim 1 of the continuation '826 Patent. (Dkt. No. 110, at 4.) Plaintiff also argues that Defendant's argument pertains to a question of fact, not claim construction. (*Id.*)

At the June 13, 2023 hearing, Defendant submitted that although Defendant is *not* arguing that the message cannot include the measured characteristic, the message must include something that is *not* the measured characteristic. As for Plaintiff's interpretation that a *message* conveying just the measured characteristic is "different" than the measured characteristic *itself*, Defendant argued that this would **[*40]** vitiate the claim requirement that "said measured characteristic is different than said network management messages."

(b) Analysis

Claim 1 of the '826 Patent recites (emphasis added):

> 1. A method comprising:
>
> performing by one or more circuits of a receiver coupled to a television and data service provider headend via a hybrid fiber coaxial (HFC) network:
>
> receiving, via said HFC network, a signal that carries a plurality of channels, wherein said channels comprise one or both of television channels and data channels;
>
> digitizing said received signal to generate a digitized signal;
>
> selecting a first portion of said digitized signal;
>
> selecting a second portion of said digitized signal;
>
> processing said selected second portion of said digitized signal to recover information carried in said plurality of channels;
>
> analyzing said selected first portion of said digitized signal to measure a characteristic of said received signal; and
>
> controlling the transmission of *network management messages* back to said headend based on said measured characteristic of said received signal, wherein said measured characteristic is different than said *network management messages*.

On one hand, the specification discloses that messages **[*41]** sent to the headend can include measured characteristics:

> The CMTS 114 may process the messages and, in an example embodiment, adjust transmission parameters (e.g., modulation parameters, transmit power, frequency offsets, etc.) and/or perform other maintenance/management based on the received messages.
>
> * * *
>
> Such message may comprise, for example, network status updates indicating whether one or more communication parameters of one or more received television or DOCSIS channels are outside acceptable bounds, and/or *conveying measured/determined characteristics* back to a source of the received signal (e.g., back to a cable headend).

'826 Patent at 3:11-15 & 3:63-4:2 (emphasis added).

On the other hand, the claim here at issue, Claim 1 of the '826 Patent, recites that "said measured characteristic is *different than* said network management messages." Thus, simply sending the measured characteristic to the headend is insufficient to meet this claim limitation. Also of note, this contrasts with the recital in Claim 1 of the related '008 Patent of "report[ing] said determined characteristic to a source of said received signal."

Nonetheless, Defendant's proposal of an "*analysis* of the measured characteristics" lacks sufficient **[*42]** support in the specification. Defendant cites disclosures regarding "analyz[ing]" and whether one or more channels are "outside acceptable bounds":

> The monitoring module 154 may be operable to *analyze* the band CJ+1 that it receives from the channelizer 102 to *measure/determine characteristics* such as, for example, signal power level vs. frequency, delay vs. frequency, phase shift vs. frequency, type and/or amount of modulation, code rate, interference levels, signal to noise ratio, a transfer function of the channel of [*sic*] over which the signal was received, an impulse response of the channel over which the signal was received, and/or any other characteristic that may help assess characteristics of the channel over which the signal was received, assess characteristics of the transmitter that sent the signal and/or any otherwise be pertinent to performance of the communication system. . . . Additionally or alternatively, the control signal(s) 160 output by the monitoring module 154 may control the transmission of network management/maintenance messages by the device 150. Such message may comprise, for example, network status updates indicating whether one or more communication parameters **[*43]** of one or more received television or DOCSIS channels are *outside acceptable bounds*, and/or conveying *measured/determined* characteristics back to a source of the received signal (e.g., back to a cable headend)[.]

Id. at 3:45-4:2 (emphasis added).

This disclosure regarding "acceptable bounds" relates to a specific feature of a particular embodiment and does not warrant introducing a "status" or "analysis" limitation into the construction of "network management messages." *See* Phillips, 415 F.3d at 1323. Further, this disclosure that "[t]he monitoring module 154 may be operable to analyze the band CJ+1 that it receives from the channelizer 102 to measure/determine characteristics" likewise pertains to a particular

embodiment and, moreover, this usage of "analyze" merely reflects what is already recited elsewhere in the claim, namely "analyzing said selected first portion of said digitized signal to measure a characteristic of said received signal." Defendant's proposal of construing "network management messages" in terms of an "analysis" would tend to confuse rather than clarify the scope of the claim.

Nonetheless, although the claim already recites "transmission of network management messages back to said headend **[*44]** *based on* said measured characteristic of said received signal," Defendant's proposal of "based on" will assist the finder of fact in understanding that merely sending the measured characteristic is insufficient. *See* *01 Communique Laboratory, Inc. v LogMeIn, Inc.*, 687 F.3d 1292, 1296 (Fed. Cir. 2012) ("01 Communique has not cited, and we have not discovered, any authority for the proposition that construction of a particular claim term may not incorporate claim language circumscribing the meaning of the term.").

Finally, Defendant discusses Plaintiff's infringement contentions (*see* Dkt. No. 104, at 12-13), but any remaining dispute pertains to factual questions regarding infringement rather than any legal question for claim construction. *See* *PPG*, 156 F.3d at 1355; *see also* *Acumed*, 483 F.3d at 806 (citing *PPG*, 156 F.3d at 1355); *Eon*, 815 F.2d at 1318-19 (citing *PPG*, 156 F.3d at 1355; citing *Acumed*, 483 F.3d at 806).

The Court therefore hereby construes **"network management messages"** to mean **"messages which report on the network based on the measured characteristics."**

VI. DISPUTED TERMS IN U.S. PATENT NO. 8,792,008

7. "operable to"

Go to table9

(Dkt. No. 84, at A-8; Dkt. No. 97, at 16; Dkt. No. 104, at 13.)

In their Amended Patent Rule 4-5(d) Joint Claim Construction Chart, the parties agree that "operable **[*45]** to" should be construed to mean "configured to." (Dkt. No. 115, Ex. A, at 3.)

The Court therefore hereby construes **"operable to"** to mean **"configured to."**

8. "digitize a received signal spanning an entire television spectrum comprising a plurality of television channels"

Go to table10

(Dkt. No. 84, at A-9; Dkt. No. 97, at 16; Dkt. No. 104, at 13; Dkt. No. 115, Ex. A, at 3-4.)

(a) The Parties' Positions

Plaintiff argues that "[t]he plain language of the claim recites '*comprising* a plurality of television channels,' indicating that the 'received signal spanning an entire television spectrum' is *not limited* to only television channels." (Dkt. No. 97, at 16.) Plaintiff also argues that the specification confirms this understanding. (*See id.*, at 17.)

Defendant responds that "'[s]pan' is a plain English word which means the full extent of something from end to end (*e.g.*, 'wing span,' 'life span,' 'span of a bridge')." **[*46]** (Dkt. No. 104, at 14.)

Plaintiff replies that "a television spectrum may contain inside it something in addition to individual television channels," and "[i]t does not cease being a television spectrum if non-video signals are added within the block." (Dkt. No. 110, at 4-5.)

At the June 13, 2023 hearing, Defendant alternatively proposed: "The 'received signal' contains only television channels and data channels which fall between television channels."

(b) Analysis

Claim 1 of the '008 Patent recites (emphasis added):

> 1. A system comprising:
>
> an analog-to-digital converter operable to *digitize a received signal spanning an entire television spectrum comprising a plurality of television channels*, said digitization resulting in a digitized signal;
>
> a signal monitor operable to:
>
> analyze said digitized signal to determine a characteristic of said digitized signal; and

> report said determined characteristic to a source of said received signal;
>
> a data processor operable to process a television channel to recover content carried on the television channel; and
>
> a channelizer operable to:
>
> select a first portion of said digitized signal;
>
> select a second portion of said digitized signal; and
>
> concurrently output said first **[*47]** portion of said digitized signal to said signal monitor and said second portion of said digitized signal to said data processor.

As a general matter, "[t]he transitional term 'comprising' . . . is open-ended and does not exclude additional, unrecited elements or method steps." *See* Gillette Co. v. Energizer Holdings, Inc., 405 F.3d 1367, 1371 (Fed. Cir. 2005).

Defendant submits authority that "[t]he usage 'comprising' means that additional components may be present in the device, but does not change the elements that are stated in the claim." Outside the Box Innovations, LLC v. Travel Caddy, Inc., 695 F.3d 1285, 1305 (Fed. Cir. 2012).

But although the claim language refers to "television spectrum" and refers to the television spectrum comprising television channels, this does *not* preclude non-television channels from being present within that spectrum. In other words, Defendant has not shown that this usage of "comprising" is somehow closed-ended. Also, Defendant's reliance at the June 13, 2023 hearing on a general-purpose dictionary definition of "spanning" as referring to the "extent" of something "between any two limits," even if found relevant, is unpersuasive. *Collins English Dictionary* (30th ed.).

This finding is consistent with disclosures in the specification that the received signal may include data from an IP network or may include DOCSIS channels: **[*48]**

> For downstream traffic, the headend 108 may receive television signals via the antenna 102 and the satellite dish 104, and *may receive data via the IP network 106*. The switch 110 may convey the television signals to the video modulator 112 and the data to the CMTS 114. The video modulator 112 may modulate the received television signals onto a carrier. The CMTS 114 may modulate the received data onto carrier. The splitter/combiner 116 may *combine the outputs* of the video modulator 112 and the CMTS 114 resulting in a frequency division multiplexed (FDM) *signal comprising one or more television channels and/or one or more DOCSIS channels*.
>
> * * *
>
> The RF receive front-end 158 may be operable to process a received RF signal S to generate a digital signal D. The signal S may be the result of *a plurality of television and/or DOCSIS channels* being frequency division multiplexed into a *single signal*. The signal S may occupy a frequency band from F_{lo} to F_{hi}.

'008 Patent at 2:44-54 & 3:12-16 (emphasis added); *see id.* at 4:45-47 ("The data processing module 156 may process one or more of bands C_1—C_J to recover data on one or more channels (e.g., television and/or DOCSIS channels) . . . .") & 5:60-62 ("Accordingly, **[*49]** for cable television/DOCSIS, the ADC 256 may be operable to digitize the entire cable downstream (e.g., from ~55 MHz to ~1002 MHz).").

Further, Defendant points to the express recital in Claim 1 of the '826 Patent that the received signal comprises "one or both of television and data channels," but this recital in a different independent claim in a different (albeit related) patent does not imply or otherwise justify a narrow interpretation of the disputed term in Claim 1 of the '008 Patent. Further, as Plaintiff argued at the June 13, 2023 hearing, whereas Claim 1 of the '826 Patent allows for there being only data channels, Claim 1 of the '008 Patent requires television channels.

Finally, at the June 13, 2023 hearing, Defendant proposed that "[t]he 'received signal' contains only television channels and data channels which fall between television channels." Defendant thus proposes that a data channel cannot overlap (or be subsumed within) a television channel. As discussed above, Defendant does not demonstrate that the disputed term precludes the presence of data channels within the same spectrum as television channels. The Court therefore rejects Defendant's alternative proposal.

The Court thus hereby expressly rejects Defendant's **[*50]** proposed constructions. No further construction is necessary. *See* U.S. Surgical, 103 F.3d at 1568; *see also* O2 Micro, 521 F.3d at 1362; Finjan, 626 F.3d at 1207; ActiveVideo, 694 F.3d at 1326; Summit 6, 802 F.3d at 1291; Bayer, 989 F.3d at 977-79.

The Court accordingly hereby construes **"digitize a**

received signal spanning an entire television spectrum comprising a plurality of television channels" to have its **plain meaning**.

9. "signal monitor," "data processor," and "channelizer"

Go to table 1.1

(Dkt. No. 84, at A-9; Dkt. No. 97, at 17; Dkt. No. 104, at 14; Dkt. No. 115, Ex. A, at 4.)

(a) The Parties' Positions

Plaintiff argues that Defendant's proposal should be rejected because "[n]o phrase [in the claim] even arguably related to separateness is present," and "the specification is clear that these three items do *not* have to be implemented on separate pieces of hardware." (Dkt. No. 97, at 17.)

Defendant responds:

> Entropic contends that there need not be any 'separateness' between the three, and that they can all refer to the same physical **[*51]** device. Entropic provides no support for its contention that this is the 'plain and ordinary meaning' of these terms, or any facts to overcome the presumption that each of these must be a distinct physical component. . . . Nor could Entropic possibly overcome this presumption, as neither the claims nor the specification make any sense unless each of the three is a separate device.

(Dkt. No. 104, at 14-15 (citation omitted).)

Plaintiff replies that Defendant is attempting to argue a question of fact regarding what is separate, as part of claim construction, which Plaintiff submits is improper. (Dkt. No. 110, at 5.) Plaintiff also submits that "[b]y the priority date (2011), it was exceedingly common for a single SoC [(System on a Chip)] to embody many functional elements, as a POSITA would have been well aware." (*Id.* (footnote omitted).)

At the June 13, 2023 hearing, Defendant argued that these terms refer to three structures that might even be on a single chip but that nonetheless must be physically separate pieces of hardware.

(b) Analysis

Claim 1 of the '008 Patent recites (emphasis added):

> 1. A system comprising:
>
> an analog-to-digital converter operable to digitize a received signal spanning an entire **[*52]** television spectrum comprising a plurality of television channels, said digitization resulting in a digitized signal;
>
> a *signal monitor* operable to:
>
> analyze said digitized signal to determine a characteristic of said digitized signal; and report said determined characteristic to a source of said received signal;
>
> a *data processor* operable to process a television channel to recover content carried on the television channel; and
>
> a *channelizer* operable to:
>
> select a first portion of said digitized signal;
>
> select a second portion of said digitized signal; and
>
> concurrently output said first portion of said digitized signal to said *signal monitor* and said second portion of said digitized signal to said *data processor*.

As a general matter, "[w]here a claim lists elements separately, 'the clear implication of the claim language' is that those elements are 'distinct component[s]' of the patented invention." *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP, 616 F.3d 1249, 1254 (Fed. Cir. 2010)*; *see Kyocera Senco Indus. Tools Inc. v. Int'l Trade Comm'n, 22 F.4th 1369, 1382 (Fed. Cir. 2022)* (listing components separately in a claim gives rise to "a presumption that those components are distinct").

Defendant does not show, however, that a requirement for "distinct" components, *id.*, necessarily requires separate pieces of hardware. Also, the specification discloses that "[t]he various **[*53]** modules of the subassembly 174," including "the signal monitor 154, data processor 156, and channelizer 152," "may reside in . . . one or more integrated circuits." *See id.* at 4:56-59 & Fig. 1C. Defendant argues that "[w]hat this sentence means is that each individual module can be one or more integrated circuits, not that all of the different modules can be one device" (Dkt. No. 104, at 16), but here, too, the patentee did not express or imply any physical separation.

Finally, at the June 13, 2023 hearing, Defendant

emphasized disclosure regarding "[t]he parallel arrangement of the monitoring module 154 and data processing module 156," but this disclosure pertains to a specific embodiment and therefore should not be imported into the claim. *See* Phillips, 415 F.3d at 1323. Also, Defendant does not show that a "parallel arrangement" necessarily implies physically separate structures.

The Court therefore hereby expressly rejects Defendant's proposed construction. No further construction is necessary. *See* U.S. Surgical, 103 F.3d at 1568; *see also* O2 Micro, 521 F.3d at 1362; Finjan, 626 F.3d at 1207; ActiveVideo, 694 F.3d at 1326; Summit 6, 802 F.3d at 1291; Bayer, 989 F.3d at 977-79.

The Court accordingly hereby construes **"signal monitor," "data processor,"** and **"channelizer"** to have their **plain meaning**.

VII. DISPUTED TERMS IN U.S. PATENT NO. 8,284,690

The '690 Patent, titled "Receiver Determined Probe," issued **[*54]** on October 9, 2012, and bears an earliest priority date of December 15, 2008. Plaintiff submits that the '690 Patent "relates generally to aiding in the diagnosis of problems with subscriber services." (Dkt. No. 97 at 4.)

The Abstract of the '690 Patent states:

> According to various embodiments of the disclosed method and apparatus, nodes on a network are programmed to generate a probe transmission in response to a request from the node that will be receiving the probe. The receiving node may generate a probe request that specifies a plurality of parameters, such as a modulation profile for the probe; the payload content of the probe; the number of times to transmit the probe; a number of symbols for the payload of the probe; a preamble type for the probe; a cyclic-prefix length for the payload of the probe; a transmit power for the probe; and a transmit power scaling factor for the payload of the probe.

10. "probe" and "physical layer probe"

Go to table12

(Dkt. No. 84, at A-10; Dkt. No. 97, at 18; Dkt. No. 104, at 18; Dkt. No. 115, Ex. A, at 7-9 & 11.)

(a) The Parties' Positions

Plaintiff argues that these are different terms and are therefore presumed to have different meanings. (Dkt. No. 97, at 18.) Plaintiff also argues that "Charter's proposed construction imposes on 'probe' a lengthy requirement of a specific function, in clear violation of the rule against importing the specification into the claim." (*Id.* (citation omitted).)

Defendant responds: "Entropic asserts that 'probe' should be construed according to its plain and ordinary meaning, but it does not explain which of the many 'plain meanings' of the word 'probe' applies. Charter's construction, taken from the patent specification, *is* the plain meaning in the context of probes sent between nodes in a network. The DOCSIS specification confirms this." (Dkt. No. 104, at 18.) As for Defendant's proposal of "packet," **[*56]** Defendant submits that "'[p]acket' is in the construction to avoid having the word 'probe' in the construction of 'probe' and because probes *are* packets." (*Id.*)

Plaintiff replies that "Charter grounds its argument to limit 'probe' based on *post-priority, extrinsic* evidence," and "Charter's focus seems to be on the DOCSIS 3.1 cable modems accused of infringement in this case, thereby committing error in construing the claims with reference to the accused devices." (Dkt. No. 110, at 6 (citation omitted).) Also, "with respect to 'physical layer probe,' Charter errs by importing an embodiment into the claims." (*Id.*)

At the June 13, 2023 hearing, Plaintiff alternatively proposed that a "probe" is "a signal used to determine one or more characteristics of a channel." Defendant disagreed with Plaintiff's alternative proposal, but Defendant had no objection to replacing "packet" with "signal" in Defendant's proposed construction.

(b) Analysis

The specification discloses that "probes" are used, for example, to determine characteristics of channels:

> In some instances, probes are sent between nodes of the network in order to allow a receiving node on the network to determine some of the characteristics **[*57]** of the channel between the receiving node and the transmitting node. These

> probes are typically well defined. Accordingly, the receiving node knows before reception what reference signal was transmitted. By comparing the reference probe with the actual received probe, the receiver can determine some of the characteristics of the channel between the transmitting and receiving node.
> * * *
> In various embodiments, these receiver determined probes may be used in a variety of applications. For example, the probes may be used to reach or discover hidden nodes; in networks employing orthogonal frequency division multiple access (OFDMA), the probes may be used for OFDMA subchannel assessment; or in networks accessible by content providers, the probes may be used for off-site network diagnosis.
> * * *
> In block 204, the requesting node receives the probe generated according to its earlier probe request. The received probe may then be used in further processing in block 205. In one embodiment, the received probe may be used in channel analysis to determine a bitloading table, FEC and other communication parameters for OFDM or OFDMA signals for future transmissions from the probe transmitter. In another **[*58]** embodiment, post reception processing might comprise generating a report from the probe and transmitting this probe report to the requesting node or to a designated entity.

'690 Patent at 1:48-57, 2:20-27 & 6:59-7:11.

Claim 9 of the '690 Patent is limited to a "physical layer probe," and the subsequent recitals of "the probe" in Claim 9 can be readily understood as referring back to the recital of a "physical layer probe" (emphasis added):

> 9. A method comprising:
>
> a) a first node transmitting a probe request to a second node, the probe request specifying a first plurality of probe parameters for *a physical layer probe*, the first plurality of probe parameters comprising a form for *the probe* including a modulation profile for *the probe*;
>
> b) the first node receiving *the probe* from the second node, wherein *the probe* is generated in accordance with the first plurality of parameters and in accordance with a second plurality of parameters determined by the second node.

The other independent claim of the '690 Patent that recites a "probe" is Claim 1, which recites (emphasis added):

> 1. A method comprising:
>
> a) receiving in a first node, a probe request specifying a first plurality of parameters associated with the generation and transmission **[*59]** of *a probe*, wherein the first plurality of parameters at least specify content payload of *the probe* and a second node;
>
> b) determining a second plurality of parameters associated with generation and transmission of *the probe*;
>
> c) generating *the probe* in accordance with the first plurality of parameters and the second plurality of parameters, wherein *the probe* has a form dictated by the first plurality of parameters; and
>
> d) transmitting *the probe* from the first node to the second node.

Defendant argues that a "probe," even in Claim 1, is necessarily a physical layer signal. In some cases, "[d]ifferent terms or phrases in separate claims may be construed to cover the same subject matter where the written description and prosecution history indicate that such a reading of the terms or phrases is proper." *Nystrom v. TREX Co., Inc., 424 F.3d 1136, 1143 (Fed. Cir. 2005)*. Defendant submits that the patent speaks only of generating physical layer ("PHY") packets. (Dkt. No. 104, at 18 (citing '690 Patent at 3:3-5, 3:40-64 & 5:59).) Defendant also submits authority that "[t]he preference for giving meaning to all terms, however, is not an inflexible rule that supersedes all other principles of claim construction." *SimpleAir, Inc. v. Sony Ericsson Mobile Commc'ns AB, 820 F.3d 419, 429 (Fed. Cir. 2016)* (citation omitted).

Defendant also cites the DOCSIS specification, **[*60]** which states "[a] probe is a wideband physical-layer signal . . . ." (Dkt. No. 104, Ex. 4, *Data-Over-Cable Service Interface Specifications, DOCSIS 3.1*, at 20 & 57 (CHARTER_ENTROPIC00101891 & CHARTER_ENTROPIC00101928).) This statement, however, is not set forth as a broadly applicable definition but rather is set forth as part of a discussion of a specific feature. *See id.*

On balance, using a "physical layer" probe is a specific feature of particular disclosed embodiments that should not be imported into the claims. *See Phillips, 415 F.3d at 1323*. To the extent Defendant maintains that a

"probe" must be a "physical layer" probe because no other type of probe is disclosed in the specification, Defendant's argument perhaps may pertain to arguments regarding the enablement or written description requirements but does warrant importing such a limitation into the claims.

Further, the recital of "a probe" in Claim 1 and "a physical layer probe" in Claim 9, as set forth above, weighs at least somewhat further against Defendant's proposal of limiting "probe" to being a "physical layer probe." *See id. at 1314* (noting that "terms are normally used consistently throughout the patent," and "[o]ther claims of the patent in question, **[*61]** both asserted and unasserted, can also be valuable sources of enlightenment as to the meaning of a claim term").

As for Defendant's proposal of referring to a "packet," Defendant submits that the patent relates to packet-based networks, disclosing for example:

> In the illustrated embodiment, the communications protocol specifies a packet based communications system. In this embodiment, physical layer (PHY) packets comprise preambles and payloads.

'690 Patent at 3:40-44. The specification, however, refers more broadly to a probe "signal." *Id.* at 1:48-57. As noted above, at the June 13, 2023 hearing, Defendant was amenable to replacing "packet" with "signal."

Finally, at the June 13, 2023 hearing, Defendant urged that Plaintiff is attempting to interpret "probe" to encompass *new* information, which Defendant argued is contrary to the specification and the plain meaning of "probe" as referring to a signal that is already known (so that it can be compared to a reference signal). Defendant's argument in this regard is persuasive at least so far as "probe" should be limited to a signal that can be compared to a reference signal having a known form, and this is consistent with the Description of the Related **[*62]** Art portion of the specification. *See* '690 Patent at 1:48-57 (reproduced above).

The Court therefore hereby construes these disputed terms as follows:

Go to table13

11. "probe request"

Go to table14

(Dkt. No. 84, at A-11; Dkt. No. 97, at 19; Dkt. No. 104, at 19; Dkt. No. 115, Ex. A, at 7-12.)

(a) The Parties' Positions

Plaintiff argues that "[t]he plain language of the claims confirms that 'probe request' means exactly what it sounds like—a request for a probe." (Dkt. No. 97, at 19.) Plaintiff also argues that Defendant's **[*63]** proposed construction is confusing and incorporates features that are recited elsewhere in the claims. (*Id.*, at 20.)

Defendant responds that "'probe request' could not possibly have had a plain and ordinary meaning in the context of the alleged invention" because "*[t]he probe request is the invention.*" (Dkt. No. 104, at 19.) Defendant submits that "the specification explains exactly what this allegedly novel 'probe request' is." (*Id.*) Further, Defendant argues that "to whatever extent the inventor's definition of 'probe request' makes that definition redundant with other claim language, the inventor's definition still governs . . . ." (*Id.*, at 20.)

Plaintiff replies that "well-known components can be used or joined in novel ways," and "[h]ere, 'probe request' means simply a request for a probe," which "must meet certain criteria, but those are defined by the other elements of the claim, not by 'probe request' itself." (Dkt. No. 110, at 7.) Plaintiff also argues that "[Defendant's] resort to lexicography fails because the relied-upon passage is a description, not a definition which meets the high and 'exacting' legal hurdle." (*Id.* (citation omitted).)

At the June 13, 2023 hearing, Plaintiff **[*64]** argues that a "probe request" could specify things other than form, such as transmission power.

(b) Analysis

Claim 1 of the '690 Patent recites (emphasis added):

> 1. A method comprising:
>
> a) receiving in a first node, a *probe request* specifying a first plurality of parameters associated with the generation and transmission of a probe, wherein the first plurality of parameters at least specify content payload of the probe and a second node;
>
> b) determining a second plurality of parameters associated with generation and transmission of the probe;

> c) generating the probe in accordance with the first plurality of parameters and the second plurality of parameters, wherein the probe has a form dictated by the first plurality of parameters; and
> d) transmitting the probe from the first node to the second node.

The Brief Summary section of the specification states:

> The receiving node may generate a probe request that specifies a plurality of parameters to be used in such a "receiver determined" probe to generate a probe having the "form" specified by these parameters. Accordingly, the probe request specifies a plurality of parameters associated with the generation and transmission of a probe, including the content **[*65]** of a payload of the probe. In one embodiment, the parameters further include: the modulation profile for the probe; the payload content of the probe; the number of times to transmit the probe; the number of symbols for the payload of the probe; the preamble type for the probe; the cyclic-prefix length for the payload of the probe; the transmit power for the probe; and the transmit power scaling factor for the payload of the probe. Accordingly, the probe that is transmitted in response to the probe request will have a form dictated by the parameters specified in the probe request.

'690 Patent at 2:3-19.

Contrary to Defendant's suggestion that this disclosure amounts to a definition, no lexicography is apparent. That is, Defendant does not identify any expression of a clear intent by the patentee to set forth a definition for the term "probe request." *See* *Infeto Access, Inc. v. EchoStar Satellite Corp.*, 383 F.3d 1295, 1301 (Fed. Cir. 2004) ("It is well-established that the patentee can act as his own lexicographer, so long as he *clearly* states any special definitions of the claim terms in the patent specification or file history.") (emphasis added) (citing *Vitronics*, 90 F.3d at 1582).

Nonetheless, "terms coined by the inventor are best understood by reference to the specification." *Interval Inc. v. Merial Ltd.*, 617 F.3d 1282, 1287 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1315). Plaintiff replies **[*66]** that "'probe request' means simply a request for a probe," but Plaintiff does not demonstrate that the term "probe request" has any established meaning in the art. The above-reproduced disclosure explains that, as used in the '690 Patent, a probe request is sent by one network node to another network node and defines the form of a probe to be generated and transmitted.

As for Defendant's proposal that "[t]he probe request specifies at least the content payload of the probe," however, the above-reproduced disclosure refers to the payload but the above-reproduced claim language already specifically recites "the first plurality of parameters at least specify content payload of the probe and a second node," which weighs against including this specific requirement in the construction of "probe request." *See, e.g.*, *Apple, Inc. v. Ameranth, Inc.*, 842 F.3d 1229, 1237 (Fed. Cir. 2016) ("Construing a claim term to include features of that term already recited in the claims would make those expressly recited features redundant.").

The Court therefore hereby construes **"probe request"** to mean **"a request, sent by one network node to another network node, that specifies the form of a probe to be generated and transmitted."**

12. "generating the probe in accordance with the first [*67] plurality of parameters and the second plurality of parameters, wherein the probe has a form dictated by the first plurality of parameters," "wherein the probe is generated in accordance with the first plurality of parameters and in accordance with a second plurality of parameters determined by the second node," and "the first plurality of probe parameters comprising a form for the probe including a modulation profile for the probe"

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(Dkt. No. 84, at A-11—A-12; Dkt. No. 97, at 21; Dkt. No. 104, at 20; Dkt. No. 115, Ex. A, at 7-8 & 10-11.)

(a) The Parties' Positions **[*68]**

Plaintiff argues that these terms are not indefinite because "[a] POSITA would understand there are two sets of parameters—one set which relates to the probe's *form*, and another set relating to any characteristic of the probe." (Dkt. No. 97, at 21.)

Defendant argues that "the claims cover the form of the probe being determined only by the parameters in the probe request," and "[t]his renders the claims indefinite" because "[i]f the parameters determined by the probe transmitter are used to generate the probe, those parameters necessarily contribute to defining the form of the probe," and "it is impossible to imagine a parameter used to generate a probe that does not relate to its

form." (Dkt. No. 104, at 21.)

Plaintiff replies that "the probe may be based on additional information, namely 'information that previously existed within the transmitting node.'" (Dkt. No. 110, at 8 (citing '690 Patent at 6:42-45).)

At the June 13, 2023 hearing, Defendant urged that any parameter used to generate something is related to its form. Plaintiff responded that the probe transmitter can define some parameters, such as transmission power, based on information existing within the transmitter.

(b) Analysis

Claim 1 **[*69]** of the '690 Patent recites (emphasis added):

> 1. A method comprising:
> a) receiving in a first node, a probe request specifying a first plurality of parameters associated with the generation and transmission of a probe, wherein the first plurality of parameters at least specify content payload of the probe and a second node;
> b) determining a second plurality of parameters associated with generation and transmission of the probe;
>
> *c) generating the probe in accordance with the first plurality of parameters and the second plurality of parameters, wherein the probe has a form dictated by the first plurality of parameters*; and
> d) transmitting the probe from the first node to the second node.

The "generating . . ." limitation thus involves a "first plurality of parameters" that dictates the form of the probe and a "second plurality of parameters" that is *not* recited as dictating the form of the probe. The manner in which "generating the probe" is "in accordance" with the "second plurality of parameters" thus is not recited.

Defendant does not show that this gives rise to any inconsistency. The same is true as to the ". . . is generated . . ." and "parameters" limitations recited in Claim 9 of the '690 Patent. The indefiniteness **[*70]** opinion of Defendant's expert is unpersuasive. (*See* Dkt. No. 104, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶ 84.) Moreover, the opinion of Plaintiff's expert is persuasive that the "second plurality of parameters" could, for example, affect a payload portion of a probe without affecting the form of the probe. (Dkt. No. 97, Ex. 7, Apr. 14, 2023 Kramer Decl. at ¶ 138.)

Also, Plaintiff persuasively argued at the June 13, 2023 hearing that the transmitter of a probe could define some non-form parameters, such as transmission power, timing, or destination, "based upon information that previously existed within the transmitting node." *See* '690 Patent at 6:33-45.

Finally, Defendant argues that "the specification says nothing about putting parameters into probe payloads." (Dkt. No. 104, at 22.) This argument perhaps may pertain to arguments regarding enablement or written description, but this does not raise any concern regarding indefiniteness.

The Court therefore hereby expressly rejects Defendant's indefiniteness argument, and Defendant presents no alternative proposed constructions.

The Court accordingly hereby construes these terms to have their **plain meaning**.

VIII. DISPUTED TERMS IN U.S. PATENT NO. 9,210,362

The '362 Patent, titled "Wideband **[*71]** Tuner Architecture," issued on December 8, 2015, and bears an earliest priority date of April 19, 2010. Plaintiff submits that the '362 Patent "relates generally to a receiver system configured to receive a number of channels across a broad radio frequency (RF) spectrum." Dkt. No. 97 at 5.

The Abstract of the '362 Patent states:

> A wideband receiver system comprises a mixer module, a wideband analog-to-digital converter (ADC) module, and digital circuitry. The mixer module is configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels. The wideband ADC module is configured to digitize the swatch [*sic*, swath] of frequencies comprising the plurality of desired television channels and the plurality of undesired television channels. The digital circuitry is configured to select the desired plurality of television channels from the digitized plurality of frequencies, and output the selected plurality of television channels to a demodulator as a digital datastream.

13. "downconverting . . . a plurality of frequencies"

and Order of Steps in Claim 11

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(Dkt. No. 84, at A-13; Dkt. No. 97, at 22 & 24; Dkt. No. 104, at 24; Dkt. No. 115, Ex. A, at 12-13.)

(a) The Parties' Positions

Plaintiff submits that "[t]here seems to be general agreement that downconverting is well-understood" and that "[t]he process brings 'down' the frequency of a signal, using a 'mixer' or a 'mixing' process." (Dkt. No. 97, at 23.) Plaintiff argues that no order of steps is required because "[t]here is no grammatical or logical reason why digitizing cannot occur before downconverting or *vice versa* since claim 11 states these steps are performed on the same object—the 'plurality of frequencies.'" (Dkt. No. 97, at 25.) Plaintiff also argues that "because the digitizing step does not refer to the output of the 'downconverting' step (but rather its input), the claim itself **[*73]** requires no particular order of those steps." (*Id.*, at 24.) Further, Plaintiff argues that "[v]iewed in light of the differently ordered embodiments disclosed in the specification, Charter's request for an order of the steps limitation is nothing more than a second attempt by Charter to require that the claimed downconverting is done on an analog signal only." (*Id.*, at 25-26.) Finally, Plaintiff argues that there is no basis for limiting the downconverting to only "radio frequency (RF)" signals. (*Id.*)

Defendant responds that "the language of claim 11 itself dictates that the steps be performed in the order written," and "even if the structure of the claim did not mandate the order of the steps (it does), the specification 'directly or implicitly requires' that the claims be performed in order." (Dkt. No. 104, at 24 & 25 (citation omitted).) "Finally," Plaintiff submits, "claim 11 is written to track the order in which the steps are performed in the specification." (*Id.*, at 26.)

Plaintiff replies that "read in light of the specification, the claim envisions digital and/or analog downconversion of desired and undesired channels." (Dkt. No. 110, at 9.)

At the June 13, 2023 hearing, Defendant **[*74]** argued that Plaintiff is attempting to excise the entire invention from the claim because the purported invention is to reduce the need for expensive analog-to-digital converters by downconverting *before* digitizing. *See* '362 Patent at 2:20-27 & 2:45-55. Plaintiff responded that the Defendant's argument is unavailing because the specification also discloses digital downconversion. *See id.* at 5:31-58 & 9:11-34.

(b) Analysis

"As a general rule, '[u]nless the steps of a method [claim] actually recite an order, the steps are not ordinarily construed to require one.'" *Mformation Techs., Inc. v. Research in Motion Ltd., 764 F.3d 1392, 1398 (Fed. Cir. 2014)* (quoting *Interactive Gift Express, Inc. v. CompuServe Inc., 256 F.3d 1323, 1342 (Fed. Cir. 2001)*).

Courts apply a two-part test to determine whether a particular order of steps is required: "First, we look to the claim language to determine if, as a matter of logic or grammar, they must be performed in the order written," and "[i]f not, we next look to the rest of the specification to determine whether *it* directly or implicitly requires such a narrow construction." *Altiris, Inc. v. Symantec Corp., 318 F.3d 1363, 1369-70 (Fed. Cir. 2003)* (citation omitted).

Claim 11 of the '362 Patent recites (emphasis added):

> 11. A method comprising:
>
> in a wideband receiver system:
>
> *downconverting*, by a mixer module of said wideband receiver system, *a plurality of frequencies* that comprises a plurality of desired television channels **[*75]** and a plurality of undesired television channels;
>
> *digitizing*, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, *said plurality of frequencies* comprising said plurality of desired television channels and said plurality of undesired television channels;
>
> *selecting*, by digital circuitry of said wideband receiver system, said plurality of desired television channels from *said digitized plurality of frequencies*; and
>
> *outputting*, by said digital circuitry of said wideband receiver system, *said selected plurality of television channels* to a demodulator as a digital datastream.

In some cases, "the sequential nature of the claim steps

is apparent from the plain meaning of the claim language." *See* Mantech Envtl. Corp. v. Hudson Envtl. Servs., Inc., 152 F.3d 1368, 1376 (Fed. Cir. 1998); *see also* E-Pass Techs., Inc. v. 3Com Corp., 473 F.3d 1213, 1222 (Fed. Cir. 2007) ("[B]ecause the language of most of the steps of its method claim refer to the completed results of the prior step, E—Pass must show that all of those steps were performed in order.").

Here, the "downconverting . . ." step and the "digitizing . . ." step both operate on the same "plurality of frequencies," and there is no reference to "completed results of the prior step." *Id.* Rather, the "downconverting . . ." step and the "digitizing . . ." step both refer **[*76]** to the same "plurality of frequencies" without any indication that one of these steps must necessarily be performed before the other. Further, because the "digitizing . . ." step could potentially be performed before the "downconverting . . ." step, the Court rejects Defendant's proposal to limit "downconverting . . . a plurality of frequencies" to downconverting a plurality of frequencies of an *analog* radio frequency (RF) signal.

The "selecting . . ." step, by contrast, refers to "said digitized plurality of frequencies." The "digitizing . . ." step must therefore be performed before the "selecting . . ." step. *Id.*

The "outputting . . ." step refers to "said selected plurality of television channels." The "selecting . . ." step must therefore be performed before the "outputting . . ." step. *Id.*

Finally, Defendant does not persuasively justify limiting the claim to "radio frequency (RF)" signals. Defendant's reliance on the "complex mixer module" 211/221 illustrated in Figure 2 is unavailing. (*See* Dkt. No. 104, at 25-26 (discussing '362 Patent at Fig. 2).) To the extent the specification discloses downconverting radio frequencies, the use of radio frequencies is a particular feature of disclosed **[*77]** embodiments that should not be imported into the claim. *See* Phillips, 415 F.3d at 1323.

The Court therefore hereby construes these disputed terms as follows:

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IX. DISPUTED TERMS IN U.S. PATENT NO. 10,135,682

The '682 Patent, titled "Method and System for Service Group Management in a Cable System," issued on November 20, 2018, and bears an earliest priority date of July 23, 2012. Plaintiff submits that the '682 Patent "relates generally to organizing cable modems (CMs) into service groups based on signal-to-noise ratio (SNR) related metrics." (Dkt. No. 97, at 5.)

The Abstract of the '682 Patent states:

> A cable modem termination system (CMTS) may determine, for a plurality of cable modems served by the CMTS, a corresponding plurality of SNR-related metrics. The CMTS may assigning [*sic*] the modems among a plurality of service groups based on the SNR-related metrics. For any one of the modems, the CMTS may configure physical layer communication **[*78]** parameters to be used by the one of the modems based on a SNR-related metric of a service group to which the one of the modems is assigned. The physical layer communication parameters may include one or more of: transmit power, receive sensitivity, timeslot duration, modulation type, modulation order, forward error correction (FEC) type, and FEC code rate. The CMTS and the modems may communicate using orthogonal frequency division multiplexing (OFDM) over a plurality of subcarriers, and the physical layer communication parameters may be determined on a per-subcarrier basis.

14. "a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics"

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(Dkt. No. 84, at A-14; Dkt. No. 97, at 26; Dkt. No. 104, at 27; Dkt. No. 115, Ex. A, at 14.)

(a) The Parties' Positions

Plaintiff argues that "[a]ny POSITA familiar with hybrid fiber coaxial ('HFC') networks understands what is meant by an SNR profile and SNR-related **[*79]** metrics," and "the adjectives 'worst-case' and 'composite' have plain meanings to a POSITA." (Dkt. No. 97, at 26 (citations omitted).) Plaintiff also argues that "[t]he specification confirms the claim terms are used in accord with a POSITA's expectations." (*Id.*)

Defendant responds that "[t]here is nothing about this

limitation that finds any support in the specification." (Dkt. No. 104, at 27.) Defendant argues: "In view of the specification, 'composite SNR-related metric' *cannot* mean a 'composite *best-case* SNR profile.' It can only refer to the 'worst-case.' And the claim is therefore indefinite, as there is no difference between 'composite SNR-related metric' and 'worst-case SNR profile.'" (*Id.*, at 28.)

Plaintiff replies that "Charter's indefiniteness position is a chain of argument ultimately resting on a false equivalence of 'composite SNR-related metric' and 'worst-case SNR profile,'" but "[t]hey are not the same thing." (Dkt. No. 110, at 9.) Plaintiff also submits that "composite metrics based on SNR-related metrics generally (not merely worst-case) are, in fact, disclosed." (*Id.* (citing '682 Patent at 4:40-52).)

At the June 13, 2023 hearing, Defendant argued that Plaintiff does not provide **[*80]** any purported plain meaning for this "composite" term. Defendant submitted that the specification discloses only a "composite worst-case SNR profile." *See* '682 Patent at 4:9-20. Defendant urged that the disputed term is indefinite because the "composite SNR-related metric" cannot be based on the "worst-case SNR profile" if they are both the same thing. Plaintiff responded that "composite" means that something is for more than one cable modem and that a "profile" is something that involves multiple attributes (such as several frequency ranges). Plaintiff concluded that a person of ordinary skill in the art would understand that the term "composite SNR-related metric" relates to multiple cable modems and could be a profile (such as for several different frequency ranges) or could instead be a single composite metric, such as an average.

(b) Analysis

Claim 1 of the '682 Patent recites (emphasis added):

> 1. A method comprising:
>
> determining, by a cable modem termination system (CMTS), for each cable modem served by said CMTS, a *corresponding signal-to-noise ratio (SNR) related metric*;
>
> assigning, by said CMTS, each cable modem among a plurality of service groups based on a respective *corresponding SNR-related metric* ***[*81]*** ;
>
> generating, by said CMTS for each one of said plurality of service groups, *a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics* corresponding to said one of said plurality of service groups;
>
> selecting, by said CMTS, one or more physical layer communication parameter to be used for communicating with said one of said plurality of service groups based on said composite SNR-related metric; and
>
> communicating, by said CMTS, with one or more cable modems corresponding to said one of said plurality of service groups using said selected one or more physical layer communication parameter.

Defendant argues that the specification fails to distinguish between "a composite SNRrelated metric" and "a worst-case SNR profile." This argument perhaps may pertain to arguments regarding enablement or written description, but Defendant does not show any lack of reasonable certainty in the claim language itself. Rather, the claim merely recites a worst-case SNR profile that is based on the SNR-related metrics that correspond to each cable modem, and the composite SNR-related metric, in turn, is based on the worst-case SNR profile. The opinions of Plaintiff's **[*82]** expert are further persuasive in this regard. (*See* Dkt. No. 97, Ex. 7, Apr. 14, 2023 Kramer Decl. at ¶¶ 166 & 168-169; *see, e.g.*, '682 Patent at 4:9-20, 5:7-12 & 5:42-57 & Fig. 2C.) Plaintiff's arguments at the June 13, 2023 hearing (summarized above) are likewise persuasive.

The Court therefore hereby expressly rejects Defendant's indefiniteness argument, and Defendant presents no alternative proposed construction.

The Court accordingly hereby construes **"a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics"** to have its **plain meaning**.

15. "service group[s]"

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(Dkt. No. 84, at A-15; Dkt. No. 97, at 28; Dkt. No. 104, at 28-29; Dkt. No. 115, Ex. A, at 14.)

(a) The Parties' Positions

Plaintiff argues that "[a] 'service group' is a plain English term, and the claim and specification confirm that the groups consist of cable modems (CMs), not *channels*."

(Dkt. **[*83]** No. 97, at 28.) "Furthermore," Plaintiff argues, "Charter is attempting to join the upstream and downstream channels without basis in the claim language and contrary to the specification." (*Id.*)

Defendant responds that "[t]he DOCSIS specification itself provides the plain meaning definition of a 'cable modem service group' in the cable television industry (a definition Charter identified in the P.R. 4-3 statement but which Entropic entirely ignores in its brief) . . . ." (Dkt. No. 104, at 29 (citation omitted).)

Plaintiff replies that "[n]othing in the opposition overcomes the central point—the '682 Patent is described in terms of service groups consisting of groups of cable modems (CMs)." (Dkt. No. 110, at 9.) Plaintiff also argues that "whatever DOCSIS might have later said, its use of terms cannot overcome the '682 Patent's usage." (*Id.*, at 10.)

At the June 13, 2023 hearing, the parties submitted this disputed term without oral argument.

(b) Analysis

Claim 1 of the '682 Patent recites (emphasis added):

> 1. A method comprising:
> determining, by a cable modem termination system (CMTS), for each cable modem served by said CMTS, a corresponding signal-to-noise ratio (SNR) related metric;
>
> assigning, by said CMTS, each cable modem among **[*84]** a plurality of *service groups* based on a respective corresponding SNR-related metric;
>
> generating, by said CMTS for each one of said plurality of *service groups*, a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics corresponding to said one of said plurality of *service groups*;
>
> selecting, by said CMTS, one or more physical layer communication parameter to be used for communicating with said one of said plurality of *service groups* based on said composite SNR-related metric; and
>
> communicating, by said CMTS, with one or more cable modems corresponding to said one of said plurality of *service groups* using said selected one or more physical layer communication parameter.

Defendant relies on the following portion of a DOCSIS specification:

> Cable Modem Service Group
> In the HFC plant topology, the complete set of downstream and upstream channels within a single CMTS that a single Cable Modem could potentially receive or transmit on. In most HFC deployments, a CM-SG corresponds to a single Fiber Node. Usually, a CM-SG serves multiple CMs.

(Dkt. No. 104, Ex. 5, *Data-Over-Cable Service Interface Specifications, DOCSIS 3.0*, at 11 (CHARTER_ENTROPIC00101160).) **[*85]**

Because this definition refers to a set of channels that each cable modem can use (rather than a set of cable modems in a system of cable modems), this definition does not inform how the term "service group" is used in the '682 Patent, which refers to grouping cable modems:

> FIGS. 4A and 4B illustrate the network of FIG 1, with different groupings of CMs [(cable modems)] based on one or both of: measured performance metric(s) and location within the HFC network.
> * * *
> While FIGS. 3A and 3B depict SNR profiles and location as two separate bases on which to assign CMs to service groups, the two may be used in combination.

See '682 Patent at 2:24-27 & 6:39-41.

The Court therefore hereby expressly rejects Defendant's proposed construction. No further construction is necessary, particularly in light of the above-noted context provided by the specification. *See U.S. Surgical*, 103 F.3d at 1568; *see also* *O2 Micro*, 521 F.3d at 1362; *Finjan*, 626 F.3d at 1207; *ActiveVideo*, 694 F.3d at 1326; *Summit 6*, 802 F.3d at 1291; *Bayer*, 989 F.3d at 977-79.

The Court accordingly hereby construes **"service group[s]"** to have its **plain meaning**.

16. "[communicating with/corresponding to] said one of said plurality of service groups"

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(Dkt. No. 84, at A-16; Dkt. No. 97, at 30; Dkt. No. 104, at 30; Dkt. No. 115, Ex. A, at 14-15.)

(a) The Parties' Positions

Plaintiff argues that "Claim 1 itself of the '682 Patent is clear on how service groups, composed of cable modems, and the CMTS communicate . . . ." (Dkt. No. 97, at 30.) Plaintiff also submits that "[t]he specification has a multitude of references to the communication with the service group by way of, for example, physical layer parameters since the invention could not work without communication." (*Id.* (citations omitted).) "Further," Plaintiff argues, "the terms 'communicating,' 'corresponding,' and 'plurality' each have plain English meanings that are well-understood, and the combination of the terms do not create any ambiguity." (*Id.*)

Defendant responds: "There is no antecedent basis for 'said one of said plurality of service groups,' and there is no way to know which one service group among the 'plurality of service groups' the 'communicating' and 'corresponding' steps should be performed on. The claim is therefore indefinite." (Dkt. No. 104, at 30.)

Plaintiff replies:

> The '682 Patent criticizes the folly of lumping all CMs together **[*87]** in a "lowest common denominator" approach. '682 Patent, 5:50-57. Instead, the '682 Patent groups CMs based on their performance (SNR). For each group, the invention can choose communication parameters based on group performance. The chosen parameters are used to communicate with that group. *E.g., id.* at 5:42-50. This is precisely what the claim does. The "generating" step requires creating a composite metric for each service group. The "selecting step" uses the composite metric for a particular service group to choose one or more parameter(s) to use with *that* group. The "communicating" step uses the selected parameter(s) to communicate with *that* group.

(Dkt. No. 110, at 10.)

At the June 13, 2023 hearing, the parties submitted this disputed term without oral argument.

(b) Analysis

Claim 1 of the '682 Patent recites (emphasis added):

> 1. A method comprising:
> determining, by a cable modem termination system (CMTS), for each cable modem served by said CMTS, a corresponding signal-to-noise ratio (SNR) related metric;
>
> assigning, by said CMTS, each cable modem among *a plurality of service groups* based on a respective corresponding SNR-related metric;
>
> generating, by said CMTS for *each one of said plurality of service groups*, a composite **[*88]** SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics corresponding to *said one of said plurality of service groups*;
>
> selecting, by said CMTS, one or more physical layer communication parameter to be used for communicating with *said one of said plurality of service groups* based on said composite SNR-related metric; and
>
> communicating, by said CMTS, with one or more cable modems corresponding to *said one of said plurality of service groups* using said selected one or more physical layer communication parameter.

The recital of "a plurality of service groups" provides antecedent basis for "said plurality of service groups."

The parties dispute whether the recital of "*each one of* said plurality of service groups" provides antecedent basis for "*said one of* said plurality of service groups."

At first blush, the recital of "*said one* of said plurality of service groups" appears to fail to specify *which* one of the *plurality* of service groups. This is the opinion of Defendant's expert. (Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶ 97 ("there is no way to know which one service group among the 'plurality of service groups' is being referred to").)

A **[*89]** fair reading, however, is that "*said one of* said plurality of service groups" refers back to "each *one of* said plurality of service groups." In other words, the steps that refer to "said one of said plurality of service groups" must be performed for each and every one of the plurality of service groups. This is apparent on the face of the claim and is also consistent with Figure 3A of the '682 Patent referring to determining parameters "*per* service group," and the opinion of Plaintiff's expert is further persuasive. (*See* Dkt. No. 97, Ex. 7, Apr. 14, 2023 Kramer Decl. at ¶¶ 176-77.) The contrary opinion of Defendant's expert is unpersuasive. (Dkt. No. 97, Ex. 8, Apr. 4, 2023 Almeroth Decl. at ¶ 97.)

Indeed, the claim recites only *one* "one of said plurality of service groups," so the reference to "said one" is reasonably clear. Thus, to whatever extent this term is deemed to lack *explicit* antecedent basis, the

antecedent basis is *implicit*. *See* Energizer Holdings Inc. v. Int'l Trade Comm'n, 435 F.3d 1366, 1371 (Fed. Cir. 2006) (holding that "an anode gel comprised of zinc as the active anode component" provided implicit antecedent basis for "said zinc anode"); *see also Ex Parte Porter*, 25 U.S.P.Q.2d (BNA) 1144, 1145 (B.P.A.I. 1992) ("The term 'the controlled fluid' . . . finds reasonable antecedent basis in the previously recited 'controlled **[*90]** stream of fluid . . . ."'); Fisher-Price, Inc. v. Graco Children's Prods., No. 05-1258, 154 F. App'x 903, 909 (Fed. Cir. Nov. 4, 2005) ("[a] claim is not invalid for indefiniteness if its antecedent basis is present by implication") (citations omitted). The burden is on Defendant to show a lack of reasonable certainty, and Defendant has not met that burden. *See* Nautilus, 572 U.S. at 910; *see also* Sonix, 844 F.3d at 1377.

The Court therefore hereby expressly rejects Defendant's indefiniteness argument, and Defendant presents no alternative proposed construction.

The Court accordingly hereby construes **"[communicating with/corresponding to] said one of said plurality of service groups"** to have its **plain meaning**.

X. CONCLUSION

The Court adopts the constructions set forth in this opinion for the disputed terms of the patents-in-suit, and as summarized below.

Go to table 21

The parties are **[*93]** **ORDERED** that they may not refer, directly or indirectly, to each other's claim construction positions in the presence of the jury. Likewise, the parties are **ORDERED** to refrain from mentioning any portion of this opinion, other than the actual definitions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the definitions adopted by the Court.

So ORDERED and SIGNED this 26th day of June, 2023.

/s/ Rodney Gilstrap

RODNEY GILSTRAP

UNITED STATES DISTRICT JUDGE

Table1 (*Return to related document text*)

I. BACKGROUND

II. LEGAL PRINCIPLES

III. AGREED TERMS

IV. DISPUTED TERMS IN U.S. PATENT NO. 8,223,775

1. "a data networking engine implemented in a first circuit that includes at least one processor . . ." and "a cable modem engine implemented in a second circuit that includes at least one processor . . ."

2. "data bus"

3. "wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine"

4. "DOCSIS functions"

5. "DOCSIS MAC processor" and "DOCSIS controller"

V. DISPUTED TERMS IN U.S. PATENT NO. 9,825,826

6. "network management messages"

VI. DISPUTED TERMS IN U.S. PATENT NO. 8,792,008

7. "operable to"

8. "digitize a received signal spanning an entire television spectrum comprising a plurality **[*3]** of television channels"

9. "signal monitor," "data processor," and "channelizer"

VII. DISPUTED TERMS IN U.S. PATENT NO. 8,284,690

10. "probe" and "physical layer probe"

11. "probe request"

12. "generating the probe in accordance with the first plurality of parameters and the second plurality of parameters, wherein the probe has a form dictated by the first plurality of parameters," "wherein the probe is generated in accordance with the first plurality of parameters and in accordance with a second plurality of parameters determined by the second node," and "the first plurality of probe parameters comprising a form for the probe including a modulation profile for the probe"

VIII. DISPUTED TERMS IN U.S. PATENT NO. *9,210,362*

13. "downconverting . . . a plurality of frequencies" and Order of Steps in Claim 11

IX. DISPUTED TERMS IN U.S. PATENT NO. 10,135,682

14. "a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics"

15. "service group[s]"

16. "[communicating with/corresponding to] said one of said plurality of service groups" ... 58

X. CONCLUSION

Table1 (*Return to related document text*)

Table2 (*Return to related document text*)

Term	Construction
modem engine configured to enable o its software in a manner that is nt of upgrades to the software of the orking engine" nt, Claim 18)	Plain and ordinary meaning
am PDU packets" nt, Claim 18)	Plain and ordinary meaning
rs" nt, Claims 1, 9)	Plain and ordinary meaning
d with [the] generation and on of [a/the] probe" nt, Claim 1)	Plain and ordinary meaning
analog-to-digital converter (ADC) nt, Claim 1)	Plain and ordinary meaning

Table2 (*Return to related document text*)

Table3 (*Return to related document text*)

"a data networking engine implemented in a first circuit that includes at least one processor . . ."
('775 Patent, Claim 18)

Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Indefinite

"a cable modem engine implemented in a second circuit that includes at least one processor . . ."
('775 Patent, Claim 18)

Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Indefinite

Table3 (*Return to related document text*)

Table4 (*Return to related document text*)

"data bus"
('775 Patent, Claim 18)

iff's Proposed Construction	Defendant's Proposed Construction
and ordinary meaning. nstruction necessary.	Indefinite

Table4 (*Return to related document text*)

Table5 (*Return to related document text*)

"wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home networking functions performed by the data networking engine"
('775 Patent, Claim 18)

Plaintiff's Proposed Construction	**Defendant's Proposed Constructi**
Plain and ordinary meaning. No construction necessary.	The cable modem engine and the d networking engine do not share any connecting circuitry, data paths, or memory dev

Table5 (*Return to related document text*)

Table6 (*Return to related document text*)

"DOCSIS functions"
('775 Patent, Claim 19)

ıposed Construction	Defendant's Proposed Construction [*27]
ıary meaning. ın necessary.	This limitation does not change the scope of claim 18.

Table6 (*Return to related document text*)

Table7 (*Return to related document text*)

"DOCSIS MAC processor"
('775 Patent, Claim 18)

sed Construction	Defendant's Proposed Construction
y meaning. ıecessary.	The DOCSIS MAC processor as described in the patent specification (see, **[*31]** e.g., '775 Patent at 3:1-20; 4:41-57; id. at FIGs. 1 & 2). Otherwise indefinite.

"DOCSIS controller"
('775 Patent, Claim 18)

sed Construction	Defendant's Proposed Construction
y meaning. ıecessary.	The DOCSIS controller as described in the patent specification (see, e.g., '775 Patent at 3:21-48; 4:41-57; id. at FIGs. 1 & 2). Otherwise indefinite.

Table7 (*Return to related document text*)

Table8 (*Return to related document text*)

"network management messages"
('826 Patent, Claim 1)

ıposed Construction	Defendant's Proposed Construction
ıary meaning. ın necessary.	Messages which report on the status of the network based on an analysis of the measured characteristics.

Table8 (*Return to related document text*)

Table9 (*Return to related document text*)

"operable to"
('008 Patent, Claim 1)

Plaintiff's Proposed Construction	Defendant's Proposed Construction
Plain and ordinary meaning. No construction necessary.	Configured to

Table9 (*Return to related document text*)

Table10 (*Return to related document text*)

"digitize a received signal spanning an entire television spectrum comprising a plurality of television channels"
('008 Patent, Claim 1)

Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	The "received signal" contains only television channels.

Table10 (*Return to related document text*)

Table11 (*Return to related document text*)

"signal monitor"
"data processor"
"channelizer"
('008 Patent, Claim 1)

osed Construction	Defendant's Proposed Construction
ary meaning. necessary.	Three separate pieces of hardware, configured to perform the functions the claim ascribes to the signal monitor, data processor, and channelizer, respectively.

Table11 (*Return to related document text*)

Table12 (*Return to related document text*)

"probe"
('690 Patent, Claims 1, 7, 8, 9, 11)

sed Construction	Defendant's Proposed Construction
meaning. ecessary.	A packet transmitted to a network node which the node compares to a reference packet having a known form in order to determine **[*55]** characteristics of the channel on which the packet was transmitted.

"physical layer probe"
('690 Patent, Claim 9)

sed Construction	Defendant's Proposed Construction
meaning. ecessary.	"Physical layer probe" means probe. Otherwise indefinite.

Table12 (*Return to related document text*)

Table13 (*Return to related document text*)

Term	Construction
Claim 11)	**"a signal transmitted to a network node that the network node can compare to a reference signal having a known form in order to determine characteristics of the channel on which the signal was transmitted"**
er probe" Claim 9)	**Plain meaning** (apart from the Court's construction of probe," above)

Table13 (*Return to related document text*)

Table14 (*Return to related document text*)

"probe request"
('690 Patent, Claims 1, 7, 8, 9, 11, 15, 16)

Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	A request sent by a first network node to a second network node which defines the form of a probe to be generated and transmitted by the second network node. The probe request specifies at least the content payload of the probe.

Table14 (*Return to related document text*)

Table15 (*Return to related document text*)

"generating the probe in accordance with the first plurality of parameters and the second plurality of parameters, wherein the probe has a form dictated by the first plurality of parameters" ('690 Patent, Claim 1) **"wherein the probe is generated in accordance with the first plurality of parameters and in accordance with a second plurality of parameters determined by the second node"** ('690 Patent, Claim 9) **"the first plurality of probe parameters comprising a form for the probe including a modulation profile for the probe"** ('690 Patent, Claim 9)	
Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Indefinite

Table15 (*Return to related document text*)

Table16 (*Return to related document text*)

"downconverting . . . a plurality of frequencies"
('362 Patent, Claim 11)

Plaintiff's [*72] Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Downconverting a plurality of frequencies of an analog radio frequency (RF) signal.

Order of Steps
('362 Patent, Claim 11)

Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Claimed steps must be performed in the order recited in the claim.

Table16 (*Return to related document text*)

Table17 (*Return to related document text*)

Term	Construction
"downconverting . . . a plurality of frequencies" ('362 Patent, Claim 11)	Plain meaning
Order of Steps in Claim 11 of the '362 Patent	In Claim 11 of the '362 Patent, the "digitizing . . ." step must be performed before the "selecting . . ." step, and the "selecting . . ." step must be performed before the "outputting . . ." step. No other order of steps is required.

Table17 (*Return to related document text*)

Table18 (*Return to related document text*)

"a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics"
('682 Patent, Claim 1)

Plaintiff's Proposed Construction	**Defendant's Proposed Construction**
Plain and ordinary meaning. No construction necessary.	Indefinite

Table18 (*Return to related document text*)

Table19 (*Return to related document text*)

"service group[s]"
('682 Patent)

oposed Construction	**Defendant's Proposed Construction**
inary meaning. on necessary.	A "service group" is the complete set of downstream and upstream channels within a single CMTS that a single cable modem could potentially receive or transmit on.

Table19 (*Return to related document text*)

Table20 (*Return to related document text*)

'communicating with/corresponding to] said one of said plurality of service groups"
('682 Patent, Claim 1)

ed Construction	**Defendant's Proposed Construction**
dinary meaning. cessary.	Indefinite

Table20 (*Return to related document text*)

Table21 (*Return to related document text*)

Disputed Term	The Court's Construction
"a data networking engine implemented in a first circuit that includes at least one processor . . ." ('775 Patent, Claim 18)	Plain meanings.
"a cable modem engine implemented in a second circuit that includes at least one processor . . ." ('775 Patent, Claim 18)	
"data bus" ('775 Patent, Claim 18)	Plain meaning
"wherein the cable modem functions performed by the cable modem engine are completely partitioned from the home **[*91]** networking functions performed by the data networking engine" ('775 Patent, Claim 18)	"wherein the cable modem engine and the data networking engine are not necessarily physically separate but are functionally separate such that the cable modem functions are performed only by the cable modem engine and the home networking functions are performed only by the data networking engine"
"DOCSIS functions" ('775 Patent, Claim 19)	Plain meaning.
"DOCSIS MAC processor" ('775 Patent, Claim 18)	Plain meanings.
"DOCSIS controller" ('775 Patent, Claim 18)	

Disputed Term	The Court's Construction
"network management messages" ('826 Patent, Claim 1)	"messages which report on the network based on the measured characteristics"
"operable to" ('008 Patent, Claim 1)	"configured to"
"digitize a received signal spanning an entire television spectrum comprising a plurality of television channels" ('008 Patent, Claim 1)	Plain meaning.
"signal monitor" "data processor" "channelizer" ('008 Patent, Claim 1)	Plain meanings.
"probe" ('690 Patent, Claims 1, 7, 8, 9, 11)	"a signal transmitted to a network node that the network node can compare to a reference signal having a known form in order to determine characteristics of the channel on which the signal was transmitted"
"physical layer probe" ('690 Patent, Claim 9)	Plain meaning (apart from the Court's construction of "probe," above).
"probe request" ('690 Patent, Claims 1, 7, 8, 9, 11, 15, 16)	"a request, sent by one network node to another network **[*92]** node, that specifies the form of a probe to be generated and transmitted"
"generating the probe in accordance with the first plurality of parameters and the second plurality of parameters, wherein the probe has a form dictated by the first plurality of parameters"	Plain meanings.

Disputed Term	The Court's Construction
('690 Patent, Claim 1)	
"wherein the probe is generated in accordance with the first plurality of parameters and in accordance with a second plurality of parameters determined by the second node" ('690 Patent, Claim 9)	
"the first plurality of probe parameters comprising a form for the probe including a modulation profile for the probe" ('690 Patent, Claim 9)	
"downconverting . . . a plurality of frequencies" ('362 Patent, Claim 11)	Plain meaning.
Order of Steps ('362 Patent, Claim 11)	In Claim 11 of the '362 Patent, the "digitizing . . ." step must be performed before the "selecting . . ." step, and the "selecting . . ." step must be performed before the "outputting . . ." step. No other order of steps is required.
"a composite SNR-related metric based at least in part on a worst-case SNR profile of said SNR-related metrics" ('682 Patent, Claim 1)	Plain meaning.
"service group[s]" ('682 Patent)	Plain meaning.
"[communicating with/corresponding to] said one of said plurality of service groups"	Plain meaning.

Manuel Saldana

Disputed Term	The Court's Construction
('682 Patent, Claim 1)	

Table21 (*Return to related document text*)

End of Document

User Name: Manuel Saldana
Date and Time: Tuesday, October 31, 2023 11:23:00AM EDT
Job Number: 209365341

Documents (2)

1. *Maxlinear Inc Awarded Patent for Wideband Tuner Architecture*
   Client/Matter: -None-
   Search Terms: 9,210,362
   Search Type: Natural Language
   Narrowed by:

Content Type	Narrowed by
News	-None-

2. *Maxlinear Inc Awarded Patent for Wideband Tuner Architecture*
   Client/Matter: -None-
   Search Terms: 9,210,362
   Search Type: Natural Language
   Narrowed by:

Content Type	Narrowed by
News	-None-

Maxlinear Inc Awarded Patent for Wideband Tuner Architecture

Global IP News. Information Technology Patent News

December 8, 2015 Tuesday

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Length: 298 words

Body

Publication Name: Information Technology Patent News Patent Application Number: 14/614,543 Patent Publication Number: ***9,210,362*** International Patent Classification Codes: H04N 5/50 (20130101), H04B 1/0014 (20130101), H04N 21/4263 (20130101), H04N 21/4383 (20130101), H04N 21/454 (20130101), H04N 21/6193 (20130101) Patent Status: Granted

Alexandria, Dec. 8 -- Maxlinear Inc has been awarded a patent for wideband tuner architecture. This invention was developed by Reddy Madhukar, Ling Curtis and Gallagher Tim. The patent application number is 14/614,543. The International Patent Classification codes are H04B 1/16 (20060101), H04N 21/438 (20110101), H04N 21/426 (20110101), H04B 1/00 (20060101), H04N 5/50 (20060101), H04N 21/454 (20110101) and H04N 21/61 (20110101). Cooperative Patent Classification codes are H04N 5/50 (20130101), H04B 1/0014 (20130101), H04N 21/4263 (20130101), H04N 21/4383 (20130101), H04N 21/454 (20130101) and H04N 21/6193 (20130101).

The abstract released by U.S. Patent and Trademark Office states, "A wideband receiver system comprises a mixer module, a wideband analog-to-digital converter (ADC) module, and digital circuitry. The mixer module is configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels. The wideband ADC module is configured to digitize the swatch of frequencies comprising the plurality of desired television channels and the plurality of undesired television channels. The digital circuitry is configured to select the desired plurality of television channels from the digitized plurality of frequencies, and output the selected plurality of television channels to a demodulator as a digital datastream."

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Maxlinear Inc Awarded Patent for Wideband Tuner Architecture

Global IP News. Information Technology Patent News

December 8, 2015 Tuesday

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Length: 300 words

Dateline: New Delhi

Body

FULL TEXT

Publication Name: Information Technology Patent News**Patent Application Number:** 14/614,543**Patent Publication Number:** ***9,210,362*****International Patent Classification Codes:** H04N 5/50 (20130101), H04B 1/0014 (20130101), H04N 21/4263 (20130101), H04N 21/4383 (20130101), H04N 21/454 (20130101), H04N 21/6193 (20130101)**Patent Status:** Granted

Alexandria, Dec. 8 -- Maxlinear Inc has been awarded a patent for wideband tuner architecture. This invention was developed by Reddy Madhukar, Ling Curtis and Gallagher Tim. The patent application number is 14/614,543. The International Patent Classification codes are H04B 1/16 (20060101), H04N 21/438 (20110101), H04N 21/426 (20110101), H04B 1/00 (20060101), H04N 5/50 (20060101), H04N 21/454 (20110101) and H04N 21/61 (20110101). Cooperative Patent Classification codes are H04N 5/50 (20130101), H04B 1/0014 (20130101), H04N 21/4263 (20130101), H04N 21/4383 (20130101), H04N 21/454 (20130101) and H04N 21/6193 (20130101).

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End of Document

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Job Number: 209365926

Document (1)

1. *2:23cv1050 Entropic Communications, Llc V. Comcast Corporation Et Al*
   Client/Matter: -None-
   Search Terms: number(2:23CV1050)
   Search Type: Natural Language
   Narrowed by:

Content Type	Narrowed by
Dockets	Case Status: Open,Unknown,Closed

2:23cv1050, Entropic Communications, Llc V. Comcast Corporation Et Al

US District Court Docket

United States District Court, California Central

(Western Division - Los Angeles)

This case was retrieved on 10/25/2023

Header

Case Number: ***2:23cv1050***

Date Filed: 02/10/2023
Assigned To: Judge John W. Holcomb
Referred To: Magistrate Judge Karen E. Scott
Nature of Suit: Patent (830)
Cause: Patent Infringement
Lead Docket: 2:23cv01049
Other Docket: 2:22cv07775
Jurisdiction: Federal Question

Class Code: Closed
Closed: 10/16/2023
Statute: 35:271
Jury Demand: Plaintiff
Demand Amount: $0
NOS Description: Patent

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Proceedings

#	Date	Proceeding Text	Source
1	02/10/2023	COMPLAINT Receipt No: ACACDC-34782917 - Fee: $402, filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3, # 4 Exhibit 4, # 5 Exhibit 5, # 6 Exhibit 6, # 7 Exhibit 7, # 8 Exhibit 8, # 9 Exhibit 9, # 10 Exhibit 10, # 11 Exhibit 11, # 12 Exhibit 12, # 13 Exhibit 13, # 14 Exhibit 14, # 15 Exhibit 15, # 16 Exhibit 16, # 17 Exhibit 17) (Attorney Christina N. Goodrich added to party Entropic Communications, LLC(pty:pla))(Goodrich, Christina) (Entered: 02/10/2023)	
2	02/10/2023	CIVIL COVER SHEET filed by Plaintiff Entropic Communications, LLC. (Goodrich, Christina) (Entered: 02/10/2023)	

#	Date	Proceeding Text	Source
3	02/10/2023	Request for Clerk to Issue Summons on Complaint (Attorney Civil Case Opening),, 1 filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Summons to Comcast Cable Communications, LLC, # 2 Proposed Summons to Comcast Cable Communications Management, LLC)(Goodrich, Christina) (Entered: 02/10/2023)	
4	02/10/2023	Certification and NOTICE of Interested Parties filed by Plaintiff Entropic Communications, LLC. (Goodrich, Christina) (Entered: 02/10/2023)	
5	02/10/2023	NOTICE of Related Case(s) filed by Plaintiff Entropic Communications, LLC. Related Case(s): 2:23-cv-01048; 2:23-cv-01049; 2:22-cv-07775-JWH-JEM; 2:22-cv-07959-JWH-JEM (Goodrich, Christina) (Entered: 02/10/2023)	
6	02/10/2023	REPORT ON THE FILING OF AN ACTION Regarding a Patent or a Trademark (Initial Notification) filed by Entropic Communications, LLC. (Goodrich, Christina) (Entered: 02/10/2023)	
7	02/13/2023	NOTICE OF ASSIGNMENT to District Judge Andre Birotte Jr and Magistrate Judge Autumn D. Spaeth. (lh) (Entered: 02/13/2023)	
8	02/13/2023	NOTICE TO PARTIES OF COURT-DIRECTED ADR PROGRAM filed. (lh) (Entered: 02/13/2023)	
9	02/13/2023	Notice to Counsel Re Consent to Proceed Before a United States Magistrate Judge. (lh) (Entered: 02/13/2023)	
10	02/13/2023	21 DAY Summons Issued re Complaint (Attorney Civil Case Opening), 1 as to Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Summons as to Defendant Comcast Cable Communications, LLC, # 2 Summons as to Comcast Cable Communications Management, LLC) (lh) (Entered: 02/13/2023)	
11	02/14/2023	STANDING ORDER upon filing of the complaint by Judge Andre Birotte Jr. (cb) (Entered: 02/14/2023)	
12	02/15/2023	ORDER RE TRANSFER PURSUANT TO GENERAL ORDER 21-01-Related Case- filed. Related Case No: 2:22-cv-07775 JWH(JEMx). Case transferred from Judge Andre Birotte Jr and Magistrate Judge Autumn D. Spaeth to Judge John W. Holcomb and Magistrate Judge Karen E. Scott for all further proceedings. The case number will now reflect the initials of the transferee Judge 2:23-cv-01050 JWH(KESx). Signed by Judge John W. Holcomb (rn) (Entered: 02/15/2023)	
13	02/21/2023	MINUTE ORDER TO SHOW CAUSE REGARDING CONSOLIDATION (IN CHAMBERS) by Judge John W. Holcomb. The Court ORDERS the parties to show cause why these two cases-Nos. 2:23-cv-01049-JWH-KES and 2:23-cv-01050-JWH-KES should not be consolidated for pretrial purposes in view of the overlap in subject matter. The parties are DIRECTED to file no later than March 10, 2023, a joint response detailing their collective or respective positions regarding pretrial consolidation. A hearing on this Order to Show Cause is SET for March 31, 2023, at 9:00 a.m. in Courtroom 9D of the Ronald Reagan Federal Building and U.S. Courthouse, 411 W. 4th Street, Santa Ana, California. IT IS SO ORDERED. (yl) (Entered: 02/22/2023)	
14	02/23/2023	STANDING ORDER by Judge John W. Holcomb. (cla) (Entered: 02/23/2023)	
15	02/23/2023	PROOF OF SERVICE Executed by Plaintiff Entropic Communications, LLC, upon Defendant Comcast Corporation served on 2/16/2023, answer due 3/9/2023. Service of the Summons and Complaint were executed upon Diana Ruiz, Authorized Agent, CT Corporation System in compliance with	

#	Date	Proceeding Text	Source
		Federal Rules of Civil Procedure by service on a domestic corporation, unincorporated association, or public entity.Original Summons NOT returned. (Goodrich, Christina) (Entered: 02/23/2023)	
16	02/23/2023	PROOF OF SERVICE Executed by Plaintiff Entropic Communications, LLC, upon Defendant Comcast Cable Communications, LLC served on 2/16/2023, answer due 3/9/2023. Service of the Summons and Complaint were executed upon Diana Ruiz, Authorized Agent, CT Corporation System in compliance with Federal Rules of Civil Procedure by service on a domestic corporation, unincorporated association, or public entity.Original Summons NOT returned. (Goodrich, Christina) (Entered: 02/23/2023)	
17	02/23/2023	PROOF OF SERVICE Executed by Plaintiff Entropic Communications, LLC, upon Defendant Comcast Cable Communications Management, LLC served on 2/16/2023, answer due 3/9/2023. Service of the Summons and Complaint were executed upon Diana Ruiz, Authorized Agent, CT Corporation System in compliance with Federal Rules of Civil Procedure by service on a domestic corporation, unincorporated association, or public entity.Original Summons NOT returned. (Goodrich, Christina) (Entered: 02/23/2023)	
18	03/08/2023	Notice of Appearance or Withdrawal of Counsel: for attorney Krishnan Padmanabhan counsel for Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. Adding Krishnan Padmanabhan as counsel of record for Comcast Corporation; Comcast Cable Communications, LLC; and Comcast Cable Communications Management, LLC for the reason indicated in the G-123 Notice. Filed by Defendants Comcast Corporation; Comcast Cable Communications, LLC; and Comcast Cable Communications Management, LLC. (Attorney Krishnan Padmanabhan added to party Comcast Cable Communications Management, LLC(pty:dft), Attorney Krishnan Padmanabhan added to party Comcast Cable Communications, LLC(pty:dft), Attorney Krishnan Padmanabhan added to party Comcast Corporation(pty:dft))(Padmanabhan, Krishnan) (Entered: 03/08/2023)	
19	03/08/2023	Joint STIPULATION Extending Time to Answer the complaint as to All Defendants, re Complaint (Attorney Civil Case Opening)., 1 filed by Plaintiff Entropic Communications, LLC.(Goodrich, Christina) (Entered: 03/08/2023)	
20	03/10/2023	RESPONSE filed by Plaintiff Entropic Communications, LLCto Minutes of In Chambers Order/Directive - no proceeding held,,, Set/Reset Hearing,, 13 - JOINT RESPONSE TO OSC RE CONSOLIDATION (Goodrich, Christina) (Entered: 03/10/2023)	
21	03/21/2023	Joint STIPULATION to Continue Hearing on Order to Show Cause re Consolidation from March 31, 2023 to April 21, 2023 Re: Minutes of In Chambers Order/Directive - no proceeding held,,, Set/Reset Hearing,, 13 filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Order on Joint Stipulation to Request Continuance)(Goodrich, Christina) (Entered: 03/21/2023)	
22	03/23/2023	ORDER GRANTING JOINT STIPULATION TO REQUEST CONTINUANCE OF HEARING ON ORDER TO SHOW CAUSE REGARDING CONSOLIDATION by Judge John W. Holcomb, re Stipulation to Continue 21 , it is hereby ORDERED that the March 31, 2023, hearing on the Order to Show Cause Regarding Consolidation is CONTINUED from March 31, 2023, to April 21, 2023, at 9:00 a.m. IT IS SO ORDERED. (et) (Entered: 03/23/2023)	

#	Date	Proceeding Text	Source
23	03/30/2023	Joint STIPULATION for Extension of Time to File Answer to May 8, 2023 re Complaint (Attorney Civil Case Opening),, 1 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Proposed Order)(Padmanabhan, Krishnan) (Entered: 03/30/2023)	
24	03/30/2023	ORDER GRANTING JOINT STIPULATION TO REQUEST AN ADDITIONAL 30-DAY EXTENSION OF TIME FOR DEFENDANT TO ANSWER OR OTHERWISE RESPOND TO PLAINTIFF'S COMPLAINT by Judge John W. Holcomb. Having considered the Parties Joint Stipulation, and for good cause shown, it is hereby ORDERED that the deadline for Defendants to answer or otherwise respond to Plaintiff's Complaint is EXTENDED up to and including May 8, 2023. IT IS SO ORDERED (See document for further details) (yl) (Entered: 03/31/2023)	
25	04/03/2023	MINUTE ORDER TO SHOW CAUSE REGARDING APPOINTMENT OF SPECIAL MASTER REGARDING DISCOVERY DISPUTES (IN CHAMBERS) by Judge John W. Holcomb. These cases will likely generate a substantial number of discovery disputes. For that reason, the Court is considering appointing a Special Master to assist the Court in managing and deciding discovery matters, and, therefore, it issues this order to show cause (OSC). For the foregoing reasons, the Court hereby ORDERS as follows: 1. No later than April 14, 2023, the parties are DIRECTED to respond to this OSC by each filing a statement either consenting to the appointment of a Special Master for discovery purposes or showing cause why a Special Master should not be appointed. 2. A hearing on this OSC is SET for April 21, 2023, at 9:00 a.m. See minute order for details. (lom) (Entered: 04/04/2023)	
26	04/14/2023	STATEMENT JOINTLY SUBMITTED BY THE PARTIES IN RESPONSE TO ORDER TO SHOW CAUSE RE APPOINTMENT OF A SPECIAL MASTER filed by Plaintiff Entropic Communications, LLC re: Minutes of In Chambers Order/Directive - no proceeding held,,,, Set/Reset Deadlines/Hearings,,, 25 . (Goodrich, Christina) (Entered: 04/14/2023)	
27	04/17/2023	APPLICATION of Non-Resident Attorney James A. Shimota to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-35149476) filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Order) (Goodrich, Christina) (Entered: 04/17/2023)	
28	04/17/2023	Notice OF INTERESTED PARTIES (LOCAL RULE 7.1-1) (AMENDED) filed by Plaintiff Entropic Communications, LLC. (Goodrich, Christina) (Entered: 04/17/2023)	
29	04/18/2023	Notice of Appearance or Withdrawal of Counsel: for attorney Peter E Soskin counsel for Plaintiff Entropic Communications, LLC. Adding Peter Soskin as counsel of record for Entropic Communications, LLC for the reason indicated in the G-123 Notice. Filed by Plaintiff Entropic Communications, LLC. (Attorney Peter E Soskin added to party Entropic Communications, LLC(pty:pla))(Soskin, Peter) (Entered: 04/18/2023)	
30	04/20/2023	APPLICATION of Non-Resident Attorney Saranya Raghavan to Appear Pro Hac Vice on behalf of Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-35173283) filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation.	

#	Date	Proceeding Text	Source
		(Attachments: # 1 Proposed Order) (Attorney Diana Hughes Leiden added to party Comcast Cable Communications Management, LLC(pty:dft), Attorney Diana Hughes Leiden added to party Comcast Cable Communications, LLC(pty:dft), Attorney Diana Hughes Leiden added to party Comcast Corporation(pty:dft)) (Leiden, Diana) (Entered: 04/20/2023)	
31	04/21/2023	MINUTE ORDER OF HEARING RE: ORDER TO SHOW CAUSE held before Judge John W. Holcomb. For the reasons stated on the record, the parties are DIRECTED to meet and confer regarding a proposed order pertaining to consolidation and the appointment of Special Master. IT IS SO ORDERED. Court Reporter: Debbie Hino-Span. (yl) (Entered: 04/24/2023)	
32	04/24/2023	Text Only ORDER GRANTING APPLICATIONS of Non-Resident Attorney James A. Shimota, to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC 27 , and Non-Resident Attorney Saranya Raghavan, to Appear Pro Hac Vice on behalf of Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, and Comcast Corporation 30 by Judge John W. Holcomb. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (ev) TEXT ONLY ENTRY (Entered: 04/24/2023)	
33	05/05/2023	Joint STIPULATION for Extension of Time to File Answer to May 15, 2023 re Complaint (Attorney Civil Case Opening),, 1 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Proposed Order)(Padmanabhan, Krishnan) (Entered: 05/05/2023)	
34	05/08/2023	ORDER GRANTING STIPULATION TO EXTEND TIME TO RESPOND TO COMPLAINT by Judge John W. Holcomb. Having considered the Parties' Joint Stipulation, and for good cause shown, it is hereby ORDERED that the deadline for Defendants to respond to Plaintiffs Complaint is EXTENDED up to and including May 15, 2023. IT IS SO ORDERED. (yl) (Entered: 05/08/2023)	
35	05/14/2023	TRANSCRIPT for proceedings held on 4/21/2023 at 8:59 a.m. ****Transcript may be viewed at the court public terminal or purchased through Court Reporter DEBBIE HINO-SPAAN at: WEBSITE www.debbiehinospaan.com; E-mail, dhinospaan@yahoo.com before the deadline for Release of Transcript restriction. After that date, it may be obtained from the Court Reporter or through PACER. Additional formats of the transcript (ASCII, Condensed, and Word Indexing/Concordance) are also available to be purchased at any time through the Court Reporter. Notice of Intent to Redact due within 7 days of this date.** Redaction Request due 6/5/2023. Redacted Transcript Deadline set for 6/14/2023. Release of Transcript Restriction set for 8/14/2023. (dhs) (Entered: 05/14/2023)	
36	05/14/2023	NOTICE OF FILING TRANSCRIPT filed for proceedings 4/21/2023 at re Transcript 35 THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (dhs) TEXT ONLY ENTRY (Entered: 05/14/2023)	
37	05/15/2023	APPLICATION of Non-Resident Attorney Brian E. Ferguson to Appear Pro Hac Vice on behalf of Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-35315149) filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Proposed Order) (Leiden, Diana) (Entered: 05/15/2023)	

#	Date	Proceeding Text	Source
38	05/15/2023	APPLICATION to file document (Memorandum of Points & Authorities ISO Motion to Dismiss; and Exhibits A, B, C & D to Padmanabhan Declaration in Support Thereof) under seal filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Proposed Order, # 2 Redacted Document - Memorandum of Points & Authorities ISO Motion to Dismiss, # 3 Redacted Document - Exhibit A to Padmanabhan Decl., # 4 Redacted Document - Exhibit B to Padmanabhan Decl., # 5 Redacted Document - Exhibit C to Padmanabhan Decl., # 6 Redacted Document - Exhibit D to Padmanabhan Decl.)(Padmanabhan, Krishnan) (Entered: 05/15/2023)	
39	05/15/2023	SEALED DECLARATION IN SUPPORT OF APPLICATION to file document (Memorandum of Points & Authorities ISO Motion to Dismiss; and Exhibits A, B, C & D to Padmanabhan Declaration in Support Thereof) under seal 38 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Unredacted Document - Memorandum of Points & Authorities ISO Motion to Dismiss, # 2 Unredacted Document - Exhibit A to Padmanabhan Decl., # 3 Unredacted Document - Exhibit B to Padmanabhan Decl., # 4 Unredacted Document - Exhibit C to Padmanabhan Decl., # 5 Unredacted Document - Exhibit D to Padmanabhan Decl.)(Padmanabhan, Krishnan) (Entered: 05/15/2023)	
40	05/15/2023	NOTICE OF MOTION AND MOTION to Dismiss Complaint Under F.R.C.P. 12(b)(6) filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. Motion set for hearing on 6/30/2023 at 09:00 AM before Judge John W. Holcomb. (Attachments: # 1 Declaration of Krishnan Padmanabhan, # 2 Exhibit A (Redacted), # 3 Exhibit B (Redacted), # 4 Exhibit C (Redacted), # 5 Exhibit D (Redacted), # 6 Exhibit E, # 7 Proposed Order) (Padmanabhan, Krishnan) (Entered: 05/15/2023)	
41	05/15/2023	Corporate Disclosure Statement and Notice of Interested Parties filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Padmanabhan, Krishnan) (Entered: 05/15/2023)	
42	05/15/2023	PROOF OF SERVICE filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation, re Sealed Declaration in SupportDeclaration,, 39 served on 5/15/2023. (Padmanabhan, Krishnan) (Entered: 05/15/2023)	
43	05/16/2023	NOTICE of Deficiency in Electronically Filed Pro Hac Vice Application RE: APPLICATION of Non-Resident Attorney Brian E. Ferguson to Appear Pro Hac Vice on behalf of Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation (Pro Hac Vice Fee - $500 Fee Paid, Receipt 37 . The following error(s) was/were found: Local Rule 5-4.3.4 Application not hand-signed. Other error(s) with document(s): Please note t-hat electronic, image or stamp signatures are not allowed for either applicant or local counsel. See Instructions for Applicants (1). (lt) (Entered: 05/16/2023)	
44	05/17/2023	ORDER SETTING SCHEDULING CONFERENCE by Judge John W. Holcomb. Scheduling Conference set for 6/30/2023 at 9:00 AM before Judge John W. Holcomb. (cla) (Entered: 05/17/2023)	

#	Date	Proceeding Text	Source
45	05/17/2023	SCHEDULING NOTICE AND ORDER by Judge John W. Holcomb: On its own motion, the Court SETS a Status Conference on June 9, 2023, at 11:00 a.m. The parties are DIRECTED to file a Joint Status Report no later than Friday, May 26, 2023, that includes an update regarding the appointment of a Special Master and case consolidation. The parties are DIRECTEDto appear in person in Courtroom 9D, on the 9th Floor of the Ronald Reagan Federal Building and United States Courthouse at 411 W. Fourth Street Santa Ana, CA 92701. IT IS SO ORDERED.THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 05/17/2023)	
46	05/17/2023	APPLICATION of Non-Resident Attorney Nicholas F. Lenning to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-35334406) filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Order) (Goodrich, Christina) (Entered: 05/17/2023)	
47	05/17/2023	ORDER by Judge John W. Holcomb: Granting 38 Defendants' APPLICATION For Leave to File Under Seal In Connection With Defendants' Motion to Dismiss Under Fed. R.Civ.P.12(B)(6). SEE DOCUMENT FOR FURTHER INFORMATION. (twdb) (Entered: 05/18/2023)	
48	05/18/2023	SEALED NOTICE OF MOTION AND MOTION TO DISMISS UNDER F.R.C.P. 12(b)(6) re Order on Motion for Leave to File Document Under Seal, 47 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. Motion set for hearing on 6/30/2023 at 09:00 AM before Judge John W. Holcomb. (Attachments: # 1 Exhibit A to Padmanabhan Decl., # 2 Exhibit B to Padmanabhan Decl., # 3 Exhibit C to Padmanabhan Decl., # 4 Exhibit D to Padmanabhan Decl.)(Padmanabhan, Krishnan) (Entered: 05/18/2023)	
49	05/19/2023	Text Only ORDER GRANTING APPLICATION of Non-Resident Attorney Brian E. Ferguson to Appear Pro Hac Vice on behalf of Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation 37 , APPLICATION of Non-Resident Attorney Nicholas F. Lenning to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC 46 by Judge John W. Holcomb. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 05/19/2023)	
50	05/22/2023	APPLICATION to file document (Motion to Dismiss, Exhibits A and P to Padmanabhan Declaration, and Declaration of David L. Marcus) under seal filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Proposed Order, # 2 Redacted Document - Motion to Dismiss, # 3 Redacted Document - Exhibit A to Padmanabhan Decl., # 4 Redacted Document - Exhibit P to Padmanabhan Decl., # 5 Redacted Document - Declaration of David Marcus)(Padmanabhan, Krishnan) (Entered: 05/22/2023)	
51	05/22/2023	SEALED DECLARATION IN SUPPORT OF APPLICATION to file document (Motion to Dismiss, Exhibits A and P to Padmanabhan Declaration, and Declaration of David L. Marcus) under seal 50 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Unredacted Document - Motion to Dismiss, # 2 Unredacted Document - Exhibit A to Padmanabhan Decl., # 3 Unredacted Document - Exhibit P to	

#	Date	Proceeding Text	Source
		Padmanabhan Decl., # 4 Unredacted Document - Declaration of David Marcus)(Padmanabhan, Krishnan) (Entered: 05/22/2023)	
52	05/22/2023	NOTICE OF MOTION AND MOTION to Dismiss Under F.R.C.P. 12(b)(1) filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. Motion set for hearing on 6/30/2023 at 09:00 AM before Judge John W. Holcomb. (Attachments: # 1 Declaration of David L. Marcus (Redacted), # 2 Declaration of Krishnan Padmanabhan, # 3 Exhibit A (Redacted), # 4 Exhibit B, # 5 Exhibit C, # 6 Exhibit D, # 7 Exhibit E, # 8 Exhibit F, # 9 Exhibit G, # 10 Exhibit H, # 11 Exhibit I, # 12 Exhibit J, # 13 Exhibit K, # 14 Exhibit L, # 15 Exhibit M, # 16 Exhibit N, # 17 Exhibit O, # 18 Exhibit P (Redacted), # 19 Exhibit Q, # 20 Proposed Order Granting Motion to Dismiss) (Padmanabhan, Krishnan) (Entered: 05/22/2023)	
53	05/22/2023	CERTIFICATE OF SERVICE filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation, re Sealed Declaration in SupportDeclaration,, 51 served on 5/22/2023. (Padmanabhan, Krishnan) (Entered: 05/22/2023)	
54	05/23/2023	APPLICATION to file document (Docket Entries 50-2 and 52) under seal filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Proposed Order)(Padmanabhan, Krishnan) (Entered: 05/23/2023)	
55	05/23/2023	ORDER by Judge John W. Holcomb: Granting 50 Defendants' APPLICATION For Leave to File Under Fed.R.Civ.P 12(B) (1). SEE DOCUMENT FOR FURTHER INFORMATION. (twdb) (Entered: 05/23/2023)	
56	05/23/2023	NOTICE OF MOTION AND MOTION to Dismiss Under F.R.C.P. 12(b)(1) filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. Motion set for hearing on 6/30/2023 at 09:00 AM before Judge John W. Holcomb. (Attachments: # 1 Declaration of David L. Marcus (Redacted), # 2 Declaration of Krishnan Padmanabhan, # 3 Exhibit A (Redacted), # 4 Exhibit B, # 5 Exhibit C, # 6 Exhibit D, # 7 Exhibit E, # 8 Exhibit F, # 9 Exhibit G, # 10 Exhibit H, # 11 Exhibit I, # 12 Exhibit J, # 13 Exhibit K, # 14 Exhibit L, # 15 Exhibit M, # 16 Exhibit N, # 17 Exhibit O, # 18 Exhibit P (Redacted), # 19 Exhibit Q, # 20 Proposed Order Granting Motion to Dismiss) (Padmanabhan, Krishnan) (Entered: 05/23/2023)	
57	05/23/2023	SEALED NOTICE OF MOTION AND MOTION to Dismiss Under Fed. R. Civ. P. 12(B)(1) re Order on Motion for Leave to File Document Under Seal 55 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. Motion set for hearing on 6/30/2023 at 09:00 AM before Judge John W. Holcomb. (Attachments: # 1 Exhibit A to Padmanabhan Decl., # 2 Exhibit P to Padmanabhan Decl., # 3 Declaration of David L. Marcus ISO Motion to Dismiss)(Padmanabhan, Krishnan) (Entered: 05/23/2023)	
58	05/25/2023	ORDER GRANTING DEFENDANTS' APPLICATION TO FILE UNDER SEAL IN CONNECTION WITH DEFENDANTS' MOTION TO DISMISS UNDER FED. R. CIV. P. 12(B)(1) by Judge John W. Holcomb. It is hereby ORDERED that Defendants' sealing application is GRANTED. (SEE DOCUMENT FOR FURTHER DETAILS.) (rolm) (Entered: 05/25/2023)	
59	05/26/2023	STATUS REPORT re Consolidation and Appointment of Special	

#	Date	Proceeding Text	Source
		Master Prepared Jointly by All Parties filed by Plaintiff Entropic Communications, LLC. (Goodrich, Christina) (Entered: 05/26/2023)	
60	05/26/2023	APPLICATION of Non-Resident Attorney George C. Summerfield to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC (Pro Hac Vice Fee - $500 Fee Paid, Receipt No. ACACDC-35393519) filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Order) (Goodrich, Christina) (Entered: 05/26/2023)	
61	05/30/2023	SCHEDULING NOTICE AND ORDER by Judge John W. Holcomb: On its own motion, the Court CONTINUES the Status Conference from June 9, 2023, at 11:00 a.m., to June 9, 2023, at 9:00 a.m. ***TIME CHANGE ONLY*** The parties are DIRECTED to appear in person in Courtroom 9D, on the 9th Floor of the Ronald Reagan Federal Building and United States Courthouse at 411 W. Fourth Street Santa Ana, CA 92701. IT IS SO ORDERED.THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (ev) TEXT ONLY ENTRY (Entered: 05/30/2023)	
62	05/31/2023	Text Only ORDER GRANTING APPLICATION of Non-Resident Attorney George C. Summerfield to Appear Pro Hac Vice on behalf of Plaintiff Entropic Communications, LLC 60 by Judge John W. Holcomb. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (ev) TEXT ONLY ENTRY (Entered: 05/31/2023)	
63	06/05/2023	FIRST AMENDED COMPLAINT against Defendats All Defendants amending Complaint (Attorney Civil Case Opening),, 1 , filed by Plaintiff Entropic Communications, LLC (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3, # 4 Exhibit 4, # 5 Exhibit 5, # 6 Exhibit 6, # 7 Exhibit 7, # 8 Exhibit 8, # 9 Exhibit 9, # 10 Exhibit 10, # 11 Exhibit 11, # 12 Exhibit 12, # 13 Exhibit 13, # 14 Exhibit 14, # 15 Exhibit 15, # 16 Exhibit 16, # 17 Exhibit 17)(Meggs, Connor) (Entered: 06/05/2023)	
64	06/05/2023	APPLICATION to file document First Amended Complaint under seal filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Redacted Document First Amended Complaint, # 2 Proposed Order)(Meggs, Connor) (Entered: 06/05/2023)	
65	06/05/2023	SEALED DECLARATION IN SUPPORT OF APPLICATION to file document First Amended Complaint under seal 64 filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Unredacted Document First Amended Complaint)(Meggs, Connor) (Entered: 06/05/2023)	
66	06/06/2023	NOTICE OF ERRATA filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation, correcting Sealed Declaration in SupportDeclaration,, 39 , SEALED NOTICE OF MOTION AND MOTION TO DISMISS UNDER F.R.C.P. 12(b)(6) re Order on Motion for Leave to File Document Under Seal, 47 48 (specifically as to Exhibit A only at [39-2][48-1]) [(Padmanabhan, Krishnan) (Entered: 06/06/2023)	
67	06/06/2023	SEALED DOCUMENT Corrected Exhibit A to Declaration of Krishnan Padmanabhan re Sealed Declaration in SupportDeclaration,, 39 , SEALED NOTICE OF MOTION AND MOTION TO DISMISS UNDER F.R.C.P. 12(b)(6) re Order on Motion for Leave to File Document Under Seal, 47 48 . Order on Motion for Leave to File Document Under Seal, 47 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Exhibit A to Padmanabhan	

#	Date	Proceeding Text	Source
		Decl.)(Padmanabhan, Krishnan) (Entered: 06/06/2023)	
68	06/06/2023	DECLARATION of Louis Campbell re Errata, 66 in Support of Notice of Errata to Comcast Defendants' Motion to Dismiss Under FRCP 12(b)(6) 40 48 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Padmanabhan, Krishnan) (Entered: 06/06/2023)	
69	06/06/2023	CERTIFICATE OF SERVICE filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation, re Sealed Document., 67 served on 6/6/2023. (Padmanabhan, Krishnan) (Entered: 06/06/2023)	
70	06/06/2023	Joint STIPULATION to Continue Scheduling Conference from 6/30/2023 to 7/21/2023 Re: Initial Order Setting R26 Scheduling Conference - form only 44 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Proposed Order)(Padmanabhan, Krishnan) (Entered: 06/06/2023)	
71	06/06/2023	NOTICE OF LODGING filed re Amended Complaint/Petition., 63 (Attachments: # 1 Exhibit A - Redlined First Amended Complaint)(Goodrich, Christina) (Entered: 06/06/2023)	
72	06/08/2023	Joint STIPULATION for Order to Appoint Special Master filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Affidavit of David M. Keyzer Pursuant to Fed. R. Civ. P. 53(b)(3)(A), # 2 Proposed Order)(Goodrich, Christina) (Entered: 06/08/2023)	
73	06/09/2023	MINUTES OF HEARING RE: STATUS CONFERENCE held before Judge John W. Holcomb. Counsel state their appearances. The Court confers with counsel regarding the posture of the case and case schedule. For the reasons stated on the record, the Court hereby ORDERS as follows: 1. In view of the filing of a First Amended Complaint 63 , Defendants Motion to Dismiss 40 and Defendants Sealed Motion to Dismiss 48 52 57 are DENIED as moot. 2. The parties' Joint Stipulation for Continuance of the Scheduling Conference 65 is APPROVED. The Scheduling Conference is CONTINUED to July 21, 2023, at 11:00 a.m. Court Reporter: Debbie Hino-Spaan. (rolm) (Entered: 06/13/2023)	
74	06/20/2023	APPLICATION to file document (Motion to Dismiss under FRCP 12(b)(1) or 12(b)(6) and Exhibits A, Q, S, T, U and V thereto) under seal filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Proposed Order, # 2 Redacted Document - Motion to Dismiss Under FRCP 12(b)(1) or 12(b)(6) in the Alternative, # 3 Redacted Document - Exhibit A, # 4 Redacted Document - Exhibit Q, # 5 Redacted Document - Exhibit S, # 6 Redacted Document - Exhibit T, # 7 Redacted Document - Exhibit U, # 8 Redacted Document - Exhibit V)(Padmanabhan, Krishnan) (Entered: 06/20/2023)	
75	06/20/2023	SEALED DECLARATION IN SUPPORT OF APPLICATION to file document (Motion to Dismiss under FRCP 12(b)(1) or 12(b)(6) and Exhibits A, Q, S, T, U and V thereto) under seal 74 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Unredacted Document - Motion to Dismiss Under FRCP 12(b)(1) or 12(b)(6), # 2 Unredacted Document - Exhibit A, # 3 Unredacted Document - Exhibit Q, # 4 Unredacted Document - Exhibit S, # 5 Unredacted Document - Exhibit T, # 6 Unredacted Document - Exhibit U, # 7 Unredacted Document - Exhibit V)(Padmanabhan, Krishnan) (Entered: 06/20/2023)	

#	Date	Proceeding Text	Source
76	06/20/2023	NOTICE OF MOTION AND MOTION to Dismiss Under 12(b)(1) or 12(b)(6) in the Alternative filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. Motion set for hearing on 7/21/2023 at 09:00 AM before Judge John W. Holcomb. (Attachments: # 1 Exhibit A (Redacted), # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I, # 10 Exhibit J, # 11 Exhibit K, # 12 Exhibit L, # 13 Exhibit M, # 14 Exhibit N, # 15 Exhibit O, # 16 Exhibit P, # 17 Exhibit Q (Redacted), # 18 Exhibit R, # 19 Exhibit S (Redacted), # 20 Exhibit T (Redacted), # 21 Exhibit U (Redacted), # 22 Exhibit V (Redacted), # 23 Exhibit W, # 24 Exhibit X, # 25 Proposed Order Granting Motion to Dismiss) (Padmanabhan, Krishnan) (Entered: 06/20/2023)	
77	06/21/2023	CERTIFICATE OF SERVICE filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation, re Sealed Declaration in SupportDeclaration,, 75 served on 6/20/2023. (Padmanabhan, Krishnan) (Entered: 06/21/2023)	
78	06/23/2023	ORDER GRANTING DEFENDANTS' APPLICATION FOR LEAVE TO FILE UNDER SEAL IN CONNECTION WITH DEFENDANTS MOTION TO DISMISS UNDER FED. R. CIV. P. 12(B)(1) OR 12(B)(6) IN THE ALTERNATIVE by Judge John W. Holcomb. It is hereby ORDERED that defendant's sealing application is GRANTED. (See document for further details)(yl) (Entered: 06/23/2023)	
79	06/23/2023	EX PARTE APPLICATION to Continue Hearing on Motion to Dismiss from July 21, 2023 to September 22, 2023 Re: NOTICE OF MOTION AND MOTION to Dismiss Under 12(b)(1) or 12(b)(6) in the Alternative 76 filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Declaration of Nicholas F. Lenning, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Proposed Order) (Goodrich, Christina) (Entered: 06/23/2023)	
80	06/23/2023	APPLICATION to file document under seal filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Redacted Document Ex Parte Application, # 2 Proposed Order)(Goodrich, Christina) (Entered: 06/23/2023)	
81	06/23/2023	SEALED DECLARATION IN SUPPORT OF APPLICATION to file document under seal 80 filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Unredacted Document Ex Parte Application)(Goodrich, Christina) (Entered: 06/23/2023)	
82	06/24/2023	OPPOSITION to EX PARTE APPLICATION to Continue Hearing on Motion to Dismiss from July 21, 2023 to September 22, 2023 Re: NOTICE OF MOTION AND MOTION to Dismiss Under 12(b)(1) or 12(b)(6) in the Alternative 76 79 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Declaration of Krishnan Padmanabhan, # 2 Exhibit A to Padmanabhan Decl., # 3 Exhibit B to Padmanabhan Decl., # 4 Exhibit C to Padmanabhan Decl.)(Padmanabhan, Krishnan) (Entered: 06/24/2023)	
83	06/26/2023	ORDER DENYING PLAINTIFF'S EXPARTE APPLICATIONS [ECF No. 87 in the MOCA Case and ECF No. 79 in the Cable Case] (IN CHAMBERS) by Judge John W. Holcomb. For those reasons, the Court hereby ORDERS as follows: For those reasons, the Court hereby ORDERS as follows:For those reasons, the Court hereby ORDERS as follows: Comcast's request to impose sanctions for Entropic's alleged needless multiplication of these proceedings is DENIED. IT IS SO ORDERED. (See document for further details) (yl) (Entered: 06/26/2023)	

#	Date	Proceeding Text	Source
84	06/27/2023	SEALED NOTICE OF MOTION AND MOTION to Dismiss Under FRCP 12(b)(1) or 12(b)(6) in the Alternative, and Sealed Exhibits A, Q, S, T, U, and V in Support Thereof re Order on Motion for Leave to File Document Under Seal, 78 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. Motion set for hearing on 7/21/2023 at 09:00 AM before Judge John W. Holcomb. (Attachments: # 1 Exhibit A, # 2 Exhibit Q, # 3 Exhibit S, # 4 Exhibit T, # 5 Exhibit U, # 6 Exhibit V)(Leiden, Diana) (Entered: 06/27/2023)	
85	06/28/2023	CERTIFICATE OF SERVICE filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation, re SEALED NOTICE OF MOTION AND MOTION to Dismiss Under FRCP 12(b)(1) or 12(b)(6) in the Alternative, and Sealed Exhibits A, Q, S, T, U, and V in Support Thereof re Order on Motion for Leave to File Document Under Seal, 78 84 served on 6/28/2023. (Leiden, Diana) (Entered: 06/28/2023)	
86	06/30/2023	MEMORANDUM in Opposition to NOTICE OF MOTION AND MOTION to Dismiss Under 12(b)(1) or 12(b)(6) in the Alternative 76 filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Objections to Evidence Submitted in Support of Motion to Dismiss, # 2 Proposed Order re Evidentiary Objections)(Goodrich, Christina) (Entered: 06/30/2023)	
87	06/30/2023	APPLICATION to file document under seal filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Redacted Document Opposition to Motion to Dismiss, # 2 Proposed Order)(Goodrich, Christina) (Entered: 06/30/2023)	
88	06/30/2023	SEALED DECLARATION IN SUPPORT OF APPLICATION to file document under seal 87 filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Unredacted Document Opposition to Motion to Dismiss)(Goodrich, Christina) (Entered: 06/30/2023)	
89	07/05/2023	ORDER GRANTING ENTROPIC'S APPLICATION TO FILE OPPOSITION TO MOTION TO DISMISS UNDER SEAL by Judge John W. Holcomb granting 87 APPLICATION (bm) (Entered: 07/05/2023)	
90	07/05/2023	ORDER APPOINTING DAVID KEYZER, ESQ. AS SPECIAL MASTER FOR DISCOVERY PURPOSES by Judge John W. Holcomb, re Stipulation 72 : Pursuant to Fed. R. Civ. P. 53(b)(3)(A), and good cause shown, it is hereby ORDERED as follows: 1. Appointment: The Court determines that the appointment of David Keyzer, Esq. (the "Special Master") is appropriate under Rule 53(a)(1)(C) of the Federal Rules of Civil Procedure to address pretrial matters that cannot be effectively and timely addressed by an available district judge or magistrate judge in this district. (see document for further details) (bm) (Entered: 07/05/2023)	
91	07/07/2023	NOTICE OF ERRATA filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation, correcting NOTICE OF MOTION AND MOTION to Dismiss Under 12(b)(1) or 12(b)(6) in the Alternative 76 (Attachments: # 1 Declaration of Krishnan Padmanabhan ISO Defendants' Motion to Dismiss Under FRCP 12(b)(1) or 12(b)(6))(Padmanabhan, Krishnan) (Entered: 07/07/2023)	
92	07/07/2023	APPLICATION to file document (Comcast's Reply in Support of Motion to Dismiss; and Exhibits 1 and 2 to Declaration of David Marcus in Support Thereof) under seal filed by Defendants	

#	Date	Proceeding Text	Source
		Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Proposed Order Granting Leave to File Under Seal, # 2 Redacted Document - Comcast's Reply ISO Motion to Dismiss, # 3 Redacted Document - Exhibit 1 to Marcus Decl. ISO Motion to Dismiss, # 4 Redacted Document - Exhibit 2 to Marcus Decl. ISO Motion to Dismiss)(Padmanabhan, Krishnan) (Entered: 07/07/2023)	
93	07/07/2023	SEALED DECLARATION IN SUPPORT OF APPLICATION to file document (Comcast's Reply in Support of Motion to Dismiss; and Exhibits 1 and 2 to Declaration of David Marcus in Support Thereof) under seal 92 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Unredacted Document - Comcast's Reply ISO Motion to Dismiss, # 2 Unredacted Document - Exhibit 1 to Marcus Decl. ISO Motion to Dismiss, # 3 Unredacted Document - Exhibit 2 to Marcus Decl. ISO Motion to Dismiss)(Padmanabhan, Krishnan) (Entered: 07/07/2023)	
94	07/07/2023	REPLY in Support of NOTICE OF MOTION AND MOTION to Dismiss Under 12(b)(1) or 12(b)(6) in the Alternative 76 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Comcast's Response to Entropic's Objections to Exhibits Filed ISO Motion to Dismiss, # 2 Declaration of David Marcus ISO Motion to Dismiss, # 3 Exhibit 1 to Marcus Decl. (Redacted), # 4 Exhibit 2 to Marcus Decl. (Redacted))(Padmanabhan, Krishnan) (Entered: 07/07/2023)	
95	07/07/2023	CERTIFICATE OF SERVICE filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation, re Sealed Declaration in SupportDeclaration,, 93 served on 7/7/2023. (Padmanabhan, Krishnan) (Entered: 07/07/2023)	
96	07/07/2023	JOINT REPORT Rule 26(f) Discovery Plan ; estimated length of trial 6 to 8 days, filed by Plaintiff Entropic Communications, LLC.. (Goodrich, Christina) (Entered: 07/07/2023)	
97	07/10/2023	SCHEDULING NOTICE AND ORDER by Judge John W. Holcomb: On its own motion, the Court CONTINUES the hearing on Defendant's Motion to Dismiss [ECF No. 76], Defendant's Sealed Motion to Dismiss [ECF No. 84], and the Scheduling Conference from Friday, July 21, 2023, to Wednesday, August 9, 2023, at 10:00 a.m. The parties are DIRECTED to appear in person in Courtroom 9D, on the 9th Floor of the Ronald Reagan Federal Building and United States Courthouse at 411 W. Fourth Street Santa Ana, CA 92701. IT IS SO ORDERED. THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (cla) TEXT ONLY ENTRY (Entered: 07/10/2023)	
98	07/11/2023	ORDER GRANTING DEFENDANTS' APPLICATION FOR LEAVE TO FILE UNDER SEAL IN CONNECTION WITH DEFENDANTS' REPLY IN SUPPORT OF MOTION TO DISMISS UNDER FED. R. CIV. P. 12(B)(1) OR 12(B)(6) IN THE ALTERNATIVE by Judge John W. Holcomb. It is hereby ORDERED that Defendant's sealing application is GRANTED. IT IS SO ORDERED. (See document for further details) (yl) (Entered: 07/12/2023)	
99	07/12/2023	SEALED REPLY RE NOTICE OF MOTION AND MOTION to Dismiss Under 12(b)(1) or 12(b)(6) in the Alternative 76 , Order on Motion to Dismiss, 98 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Attachments: # 1 Exhibit 1 to Marcus Decl., # 2 Exhibit 2 to Marcus	

#	Date	Proceeding Text	Source
		Decl.)(Padmanabhan, Krishnan) (Entered: 07/12/2023)	
100	07/12/2023	CERTIFICATE OF SERVICE filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation, re Sealed Reply, 99 served on 7/12/2023. (Padmanabhan, Krishnan) (Entered: 07/12/2023)	
101	07/14/2023	Notice of Appearance or Withdrawal of Counsel: for attorney Kenneth Bridges counsel for Plaintiff Entropic Communications, LLC. Adding Kenneth Bridges as counsel of record for Entropic Communications, LLC for the reason indicated in the G-123 Notice. Filed by Plaintiff Entropic Communications, LLC. (Attorney Kenneth Bridges added to party Entropic Communications, LLC(pty:pla))(Bridges, Kenneth) (Entered: 07/14/2023)	
102	07/17/2023	TRANSCRIPT for proceedings held on 6/9/2023 at 9:05 a.m. ****Transcript may be viewed at the court public terminal or purchased through Court Reporter DEBBIE HINO-SPAAN at: WEBSITE www.debbiehinospaan.com; E-mail, dhinospaan@yahoo.com before the deadline for Release of Transcript restriction. After that date, it may be obtained from the Court Reporter or through PACER. Additional formats of the transcript (ASCII, Condensed, and Word Indexing/Concordance) are also available to be purchased at any time through the Court Reporter. Notice of Intent to Redact due within 7 days of this date.** Redaction Request due 8/7/2023. Redacted Transcript Deadline set for 8/17/2023. Release of Transcript Restriction set for 10/16/2023. (dhs) (Entered: 07/17/2023)	
103	07/17/2023	NOTICE OF FILING TRANSCRIPT filed for proceedings 6/9/2023 at 9:05 a.m. re Transcript 102 THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (dhs) TEXT ONLY ENTRY (Entered: 07/17/2023)	
104	07/24/2023	Notice of Special Master Order No. SM-1 filed by Special Master David M Keyzer, pursuant to July 5, 2023 appointment Order, setting special master preliminary conference for July 26, 2023, at 12:00 P.M., by videoconference (Attachments: # 1 Special Master Order No. SM-1)(Keyzer, David) (Entered: 07/24/2023)	
105	07/26/2023	Notice of Special Master Minutes filed by Special Master David M Keyzer, minutes of preliminary conference conducted by the special master on July 26, 2023, pursuant to the Court's July 5, 2023 Order appointing special master (Attachments: # 1 Special Master Minutes)(Keyzer, David) (Entered: 07/26/2023)	
106	08/01/2023	Notice of Appearance or Withdrawal of Counsel: for attorney Cassidy Young counsel for Plaintiff Entropic Communications, LLC. Adding Cassidy Young as counsel of record for Plaintiff Entropic Communications, LLC for the reason indicated in the G-123 Notice. Filed by Plaintiff Entropic Communications, LLC. (Attorney Cassidy Young added to party Entropic Communications, LLC(pty:pla))(Young, Cassidy) (Entered: 08/01/2023)	
107	08/04/2023	Notice of Special Master Order No. SM-2 filed by Special Master David M Keyzer, regarding Discovery Dispute Resolution Procedures (Attachments: # 1 Special Master Order No. SM-2 re Discovery Dispute Resolution Procedures)(Keyzer, David) (Entered: 08/04/2023)	
108	08/08/2023	NOTICE of Appearance filed by attorney Kelsi Robinson on behalf of Plaintiff Entropic Communications, LLC (Attorney Kelsi Robinson added to party Entropic Communications, LLC(pty:pla))(Robinson, Kelsi) (Entered: 08/08/2023)	
109	08/09/2023	NOTICE TO FILER OF DEFICIENCIES in Electronically Filed Document RE: Notice of Appearance 108 . The following error(s)	

#	Date	Proceeding Text	Source
		was/were found: Incorrect event selected. Correct event to be used is: Notice of Appearance or Withdrawal of Counsel G123.. In response to this notice, the Court may: (1) order an amended or correct document to be filed; (2) order the document stricken; or (3) take other action as the Court deems appropriate. You need not take any action in response to this notice unless and until the Court directs you to do so. (ak) (Entered: 08/09/2023)	
110	08/09/2023	NOTICE OF LODGING filed Slides Presented at August 9, 2023 Hearing re MEMORANDUM in Opposition to Motion, 86 (Young, Cassidy) (Entered: 08/09/2023)	
112	08/09/2023	HEARING RE: MOTION OF DEFENDANT DISH NETWORK CORPORATIONS TO DISMISS COUNTS VI AND X OF THE COMPLAINT [ECF No. 50]: SCHEDULING CONFERENCE held before Judge John W. Holcomb. For the reasons stated on the record, the Court takes the motion [ECF No. 50] under submission. Also for the reasons stated in open court, it is hereby ORDERED as follows: Counsel are DIRECTED to meet and confer forthwith regarding the Claim Construction Schedule. The parties are DIRECTED to file no later than August 18, 2023, a Stipulation and Proposed Order setting a Claim Construction Schedule. IT IS SO ORDERED. Court Reporter: Miriam Baird. (yl) (Entered: 08/11/2023)	
111	08/10/2023	NOTICE OF LODGING filed Slides Presented at August 9, 2023 Hearing re NOTICE OF MOTION AND MOTION to Dismiss Under 12(b)(1) or 12(b)(6) in the Alternative 76 (Padmanabhan, Krishnan) (Entered: 08/10/2023)	
113	08/18/2023	TRANSCRIPT for proceedings held on 8/9/23. Court Reporter/Electronic Court Recorder: miriam baird, phone number mvb11893@aol.com. Transcript may be viewed at the court public terminal or purchased through the Court Reporter/Electronic Court Recorder before the deadline for Release of Transcript Restriction. After that date it may be obtained through PACER. Notice of Intent to Redact due within 7 days of this date. Redaction Request due 9/8/2023. Redacted Transcript Deadline set for 9/18/2023. Release of Transcript Restriction set for 11/16/2023. (Baird, Miriam) (Entered: 08/18/2023)	
114	08/18/2023	NOTICE OF FILING TRANSCRIPT filed for proceedings 8/9/23 re Transcript 113 THERE IS NO PDF DOCUMENT ASSOCIATED WITH THIS ENTRY. (Baird, Miriam) TEXT ONLY ENTRY (Entered: 08/18/2023)	
115	08/18/2023	SUPPLEMENT to MEMORANDUM in Opposition to Motion, 86 filed by Plaintiff Entropic Communications, LLC. (Young, Cassidy) (Entered: 08/18/2023)	
116	08/18/2023	STIPULATION for Order Setting Claim Construction Schedule filed by Plaintiff Entropic Communications, LLC. (Attachments: # 1 Proposed Order)(Young, Cassidy) (Entered: 08/18/2023)	
117	08/21/2023	ORDER by Judge John W. Holcomb GRANTING Stipulation Setting Claim Construction Schedule 116 as follows: Claim Construction Hearing set for 7/16/2024 at 10:00 AM. (See document for further information). (jp) (Entered: 08/22/2023)	
118	09/01/2023	SUPPLEMENT to NOTICE OF MOTION AND MOTION to Dismiss Under 12(b)(1) or 12(b)(6) in the Alternative 76 filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation. (Padmanabhan, Krishnan) (Entered: 09/01/2023)	
119	10/16/2023	Joint STIPULATION to Consolidate Cases as to 2:23-cv-01049-JWH-KES, and 2:23-cv-01050-JWH-KES filed by Defendants Comcast Cable Communications Management, LLC, Comcast Cable Communications, LLC, Comcast Corporation.	

#	Date	Proceeding Text	Source
		(Attachments: # 1 Proposed Order)(Padmanabhan, Krishnan) (Entered: 10/16/2023)	
120	10/16/2023	ORDER GRANTING JOINT STIPULATION TO CONSOLIDATE 119 CASES by Judge John W. Holcomb. The Parties Joint Stipulation to Consolidate Cases is GRANTED. The following cases are CONSOLIDATED into a single action for pretrial purposes through the date of the Markman hearing: Case No. 2:23-cv-01049-JWH-KES and Case No. 2:23-cv-01050-JWH-KES. The Clerk is DIRECTED to close the following case administratively: Case No. 2:23-cv-01050-JWH-KES. IT IS SO ORDERED. Cases associated with Lead Case 2:23-cv-01049-JWH-KES (yl) (Entered: 10/17/2023)	

Patents

Number	Title	Issued	Class	Subclass
8,223,775	Architecture for a flexible and high-performance gateway cable modem	07/17/2012	370	401
8,284,690	Receiver determined probe	10/09/2012	370	252
8,792,008	Method and apparatus for spectrum monitoring	07/29/2014	348	192
9,210,362	Wideband tuner architecture	12/08/2015	1	1
9,825,826	Method and apparatus for spectrum monitoring	11/21/2017	1	1
10,135,682	Method and system for service group management in a cable network	11/20/2018	1	1
11,381,866	Cable television device	07/05/2022	1	1
11,399,206	Method for receiving a television signal	07/26/2022	1	1

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End of Document

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/019,255	09/20/2023	9210362	50348.106	5785

23446 7590 11/01/2023

MCANDREWS HELD & MALLOY, LTD
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CHICAGO, IL 60661

EXAMINER	
LIE, ANGELA M	

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
11/01/2023	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Order Granting Request For Ex Parte Reexamination	Control No. 90/019,255	Patent Under Reexamination 9210362	
	Examiner ANGELA M LIE	Art Unit 3992	AIA (FITF) Status No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed 09/20/2023 has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a)☐ PTO-892, b)☑ PTO/SB/08, c)☐ Other: ____

1. ☑ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

/ANGELA M LIE/ Primary Examiner, Art Unit 3992		

cc:Requester (if third party requester)

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

35 USC 325(d)

A review of the post grant history for the underlying patent indicates that there have been no other Office post grant challenges made to the patent (Reexamination Proceedings or *Inter Partes* Review, Post Grant Review, Covered Business Method trials). Accordingly, a discretionary denial of reexamination pursuant to 35 USC 325(d) is not applicable.

Reexamination

Claims 1 and 11 are pending in the Request for Reexamination dated September 20th, 2023.

DECISION ON REQUEST FOR REEXAMINATION

A substantial new question of patentability affecting claims 1 and 11 of US Patent No. 9,210,362 to Reddy et al (the '362 patent, hereafter) is raised by the request for ex parte reexamination.

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The References

(1) "McNeely" WO 2006/119490 to David Lowell McNeely, filed May 4, 2006, published November 9, 2006,

(2) "Pugel" WO 2007/145637 to Michael Anthony Pugel, filed June 16, 2006, published December 21, 2007.

(3) "Gomez" U.S. Patent No. 8,224,274 to Ramon Gomez et al., filed December 17, 2008, and issued July 17, 2012.

Prosecution History

The US Application with a serial number 14/614,543 has been filed on February 5th, 2015. The application included twenty claims with independent claims 1 and 11. On May 14th, 2015, the Examiner has rejected claim 1-20 over claims 1-27 of the US Patent No. 8,526,898 under nonstatutory double patenting. On May 15th, 2015, the Patent Owner filed terminal disclaimer and the Examiner has allowed the claims on August 7th, 2015. As reasons for allowance, the Examiner stated that the prior art made of record teaches a wideband receiver system but does not teach digital circuitry configured to

select a plurality of desired television channels from the digitized plurality of frequencies and output the plurality of television channels to a demodulator as a digital datastream.

Accordingly, the Examiner considers the underlined limitations as the basis for determining whether Substantial New Question of patentability is raised.

Claim 1: A wideband receiver system comprising: a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels; a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels; digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and output said selected plurality of television channels to a demodulator as a digital datastream.

Claim 11: A method comprising: in a wideband receiver system: downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels; digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels; selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.

Substantial New Question of Patentability

SNQ#1. The Request indicates that the Requester believes McNeely in view of Pugel raises a substantial new question of patentability as to claims 1 and 11.

(See Request Pages 14-32)

With respect to the independent claims 1 and 11, McNeely in view of Pugel raises a substantial new question of patentability because McNeely in view of Pugel teaches the following new, non-cumulative technical feature that may raise a substantial new question of patentability:

"... selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies [1]; and outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream. [2]"

McNeely in view of Pugel teach the above features which may raise substantial new question of patentability. The limitation [1] is taught by McNeely in column 9:16-26, wherein "*The A/D converter 220 digitizes the processed L-band signal into a series of samples, each sample containing a group of bits*", wherein L-band signal comprises the plurality of desired television channels. See also 10:1-11, wherein channels are being selected. Figure 2 also depicts element 230 which is "digital channel selector". Moreover, claims 7, 13 and 22 are also directed to selecting channels. Limitation [2] is taught by McNeely and Pugel because they "render obvious outputting, by said digital circuitry (e.g., digital channel selector 230 and digital channel recombiner 240)

of said wideband receiver system (e.g. McNeely's receiver system), the selected plurality of television channels (e.g., McNeely's selected channels) to a demodulator (e.g., Pugel's demodulator) as a digital datastream (e.g., selected digital signal)". See McNeely, 10:12-16. Pugel further teaches "*demodulating the plurality of digital RF channels*" and he also teaches receiving plurality of "*digital cable television channels within a single digital receiver circuit*" (paragraphs [0011] and [0012]). Pugel also discloses that *"each digital channel signal is then coupled to a separate demodulator 141, 142 and 143*" (paragraphs [0027] and [0010]).

Therefore, a reasonable examiner would find combination of McNeely and Pugel teachings to be important in determining the patentability of claims 1 and 11 of the '362 patent. The teachings of McNeely and Pugel discussed herein are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination, and the same question was not the subject of a final holding of invalidity in the Federal Courts.

SNQ#2. The Request indicates that the Requester believes Pugel in view of Gomez raises a substantial new question of patentability as to claims 1 and 11.

(See Request Pages 32-51)

With respect to the independent claims 1 and 11, Pugel in view of Gomez raises a substantial new question of patentability because Pugel in view of Gomez teaches the following new, non-cumulative technical feature that may raise a substantial new question of patentability:

"... selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies [1]; and outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream. [2]"

Limitation [1] is taught by Pugel. He teaches "*selecting (e.g., extracts or selects),by digital circuitry(e.g., digital channel select or of the digital tuner) of said wide band receiver system(e.g., Pugel's apparatus), said plurality of desired television channels (e.g., Pugel's digital channels desired to be recovered) from said digitized plurality of frequencies (e.g., from the digitized analog signals). Specifically, Pugel discloses extracting desired television programs (e.g., particular digital channels desired to be recovered) from the down converted, digitized frequencies (e.g., the "downconvert[ed]... first digital signal and ... second digital signal.")*" paragraph [0038] and Figure 3, wherein tuner 130 corresponds to the selecting unit, and wherein "extracting" corresponds to the step of selection, wherein desired information is extracted to be provided to demodulator. See also paragraphs [0042] – [0045] and Abstract. Limitation [2] is also taught by Pugel in paragraphs [0010], [0024], [0040] and Figure 3. More specifically Pugel teaches that each separate analog signal is converted from analog to digital form in an analog-to-digital converter 121, 122 and 123. Each digital channel signal is coupled to a separate demodulator 141, 142 and 143. Then a plurality of demodulator circuits is coupled to the digital tuner.

Therefore, a reasonable examiner would find Pugel in view of Gomez teaching to be important in determining the patentability of claims 1 and 11 of the '362 patent. The teachings of Pugel in view of Gomez discussed herein are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination, and the same question was not the subject of a final holding of invalidity in the Federal Courts.

NOTICE RE PATENT OWNER'S CORRESPONDENCE ADDRESS

Effective May 16, 2007, 37 CFR 1.33(c) has been revised to provide that: The Patent owner's correspondence address for all communications in an ex parte reexamination is designated as the correspondence address of the patent.

Revisions and Technical Corrections Affecting Requirements for Ex Parte 72 FR 18892 (April, 16, 2007) (Final Rule)

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of this revision to 37 CFR 1.33(c), automatically changed to that of the patent file as of the effective date.

This change is effective for any reexamination proceeding which is pending before the Office as of May 16, 2007, including the present reexamination proceeding, and to any reexamination proceeding which is filed after that date.

Parties are to take this change into account when filing papers, and direct communications accordingly.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of Change of Correspondence Address in the reexamination proceeding and/or the patent (depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone Numbers for reexamination inquiries:

Reexamination	(571) 272-7703
Central Reexam Unit (CRU)	(571) 272-7705
Reexamination Facisimile Transmission No.	(571) 273-9900

Conclusion

Claims 1 and 11 are ordered for reexamination.

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extension of time in reexamination proceedings are provided for in 37 CFR 1.550(c). After the filing of a request for reexamination by a third party requester, any document filed by either the patent owner of the third party requester must be served on the other

party (or parties where two or more third-party-requester proceedings are merged) in the reexamination proceeding in the manner provided in 37 CFR 1.248. See 37 CFR 1.550(f).

The patent owner is reminded of the continued responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP § 2207, 2282 and 2286.

All correspondence relating to this *ex parte* reexamination proceeding should be directed:

By EFS-Web: Registered Users may submit correspondence via EFS-Web, at https://efs.uspto.gov/efile/myportal/efs-registered.

By Mail to: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

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Randolph Building
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EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are "soft-

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Any inquiry concerning this communication should be directed to the Central Reexamination Unit at telephone number 571-272-7705.

/ANGELA M LIE/
Primary Examiner, Art Unit 3992

Conferees:

/LUKE S WASSUM/
Primary Examiner, Art Unit 3992

/ALEXANDER J KOSOWSKI/
Supervisory Patent Examiner, Art Unit 3992

Reexamination	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/019,255	9210362
	Certificate Date	Certificate Number

Requester Correspondence Address: ☐ Patent Owner ☑ Third Party
Haynes and Boone, LLP 2801 N. Harwood St. Suite 2300 Dallas TX 75201

LITIGATION REVIEW ☐	(examiner initials)	(date)
Case Name		Director Initials

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	NUMBER

/ANGELA M LIE/ Primary Examiner, Art Unit 3992	

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	In Ex Parte Reexamination of 9,210,362
				Filing Date	Herewith
				First Inventor Name	Madhukar Reddy et al.
				Art Unit	TBD
				Examiner Name	TBD
SHEET	1	OF	1	Attorney Docket Number	50348.106

U. S. PATENTS				
Examiner's Initials	**Cite No.**	**Document Number**	**Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of Cited Document**
/A.M.L/	Exhibit 1005	8,224,274	07-17-2012	Ramon Gomez et al.

U. S. PATENT APPLICATION PUBLICATIONS				
Examiner's Initials	**Cite No.**	**Document Number**	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of Cited Document**

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	**Cite No.**	**Foreign Patent Document (Country Code – Number – Kind)**	**Publication Date MM-DD-YYYY**	**Patentee or Applicant of Cited Document**	**Translation Y/N**
/A.M.L/	Exhibit 1003	WO 2006/119490	11-09-2006	David Lowell McNeely	
/A.M.L/	Exhibit 1004	WO 2007/145637	12-21-2007	Michael Anthony Pugel	

NON-PATENT LITERATURE DOCUMENTS		
Examiner's Initials	**Cite No.**	**Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published**

Examiner Signature	/ANGELA M LIE/	Date Considered	10/30/2023

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
90/019,255	**03/08/2024 10:18:57 PM Z ET**	**50348.106**

Title of Invention

WIDEBAND TUNER ARCHITECTURE

Application Information

APPLICATION TYPE	Utility / ex parte reexam	PATENT #	9210362
CONFIRMATION #	5785	FILED BY	Xuanjie Wang
PATENT CENTER #	64616943	FILING DATE	09/20/2023
CUSTOMER #	23446	FIRST NAMED INVENTOR	- 9210362
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Hao Tan

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
189005.TR003 90019255 - POA Transmittal for Execution.pdf	5	Power of Attorney	1907 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
189005.TR003 90019255 - POA Transmittal for Execution.pdf	C67BC59ACC92BDA67641F7D630AB92C62FC8BE3EA71077E89FB3C24396EE723E0B5C749EBB15C1D1C73B3411A3A48F6A36F8DAF4E10C6D301B9ECF99F2637B35

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If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

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Control Number(s)	90/019,255
Filing Date(s)	09/20/2023
First Named Inventor	Madhukar Reddy
Title	WIDEBAND TUNER ARCHITECTURE
Patent Number	9210362
Examiner Name	Angela M Lie
Attorney Docket No(s)	189005.TR003

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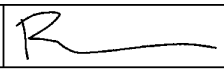
I am the:

☐ Inventor, having ownership of the patent being reexamined.

OR

■ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/AIA/96) submitted herewith or filed on 04/12/2021.

Signature of Inventor or Patent Owner		Date	3/7/2024
Name	Patrick Diaz	Telephone	917-471-4090
Title and Company	Chief Financial Officer / Entropic Communications LLC		

NOTE: Signatures of all the inventors or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

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Application Number	Filing Date

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SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Patrick Diaz		
Title	Chief Financial Officer		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

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If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Additional Uses

Additional USPTO uses of the information in this record may include disclosure to: 1) the International Bureau of the World Intellectual Property Organization, if the record is related to an international application filed under the Patent Cooperation Treaty; 2) the public i) after publication of the application pursuant to 35 U.S.C. 122(b), ii) after issuance of a patent pursuant to 35 U.S.C. 151, iii) if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections, or an issued patent, or iv) without publication of the application or patent under the specific circumstances provided for by 37 CFR 1.14(a)(1)(v)-(vii); and/or 3) the National Archives and Records Administration, for inspection of records.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
90/019,255	09/20/2023	9210362	50348.106

CONFIRMATION NO. 5785

153979
Arch & Lake LLP
203 North LaSalle Street, Suite 2100
Chicago, IL 60601

POA ACCEPTANCE LETTER

OC00000000696511780

Date Mailed: 03/12/2024

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/08/2024.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rbell/

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
90/019,255	09/20/2023	9210362	50348.106

CONFIRMATION NO. 5785

POWER OF ATTORNEY NOTICE



23446
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

Date Mailed: 03/12/2024

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/08/2024.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rbell/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 5785

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
90/019,255	09/20/2023 RULE	455	3992	50348.106

APPLICANTS

ENTROPIC COMMUNICATIONS LLC(OWNER), Residence Not Provided;
RAGHAV BAJAJ, DALLAS, TX;

INVENTORS

9210362, Residence Not Provided;
IP Section Haynes and Boone, LLP, Residence Not Provided;
CURTIS LING, CARLSBAD, CA;
TIM GALLAGHER, CARLSBAD, CA;

**** CONTINUING DATA ***************************

This application is a REX of 14/614,543 02/05/2015 PAT 9210362
which is a CON of 13/962,871 08/08/2013 PAT 9100622
which is a CON of 12/762,900 04/19/2010 PAT 8526898
which claims benefit of 61/170,526 04/17/2009

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

Foreign Priority claimed ❑ Yes ❑ No 35 USC 119(a-d) conditions met ❑ Yes ❑ No Verified and Acknowledged Examiner's Signature	❑ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
				20	2

ADDRESS

Arch & Lake LLP
203 North LaSalle Street, Suite 2100
Chicago, IL 60601
UNITED STATES

TITLE

WIDEBAND TUNER ARCHITECTURE

FILING FEE RECEIVED		
0.00	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

BIB (Rev. 05/07).

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/019,255	09/20/2023	9210362	189005.TR003	5785

153979 7590 03/18/2024

Arch & Lake LLP
203 North LaSalle Street, Suite 2100
Chicago, IL 60601

EXAMINER	
LIE, ANGELA M	

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
03/18/2024	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

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(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

Haynes and Boone, LLP
2801 N. Harwood St.
Suite 2300
Dallas TX 75201

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/019,255* .

PATENT UNDER REEXAMINATION *9210362* .

ART UNIT *3992* .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	**Control No.** 90/019,255	**Patent Under Reexamination** 9210362	
	Examiner ANGELA M LIE	**Art Unit** 3992	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a. ☐ Responsive to the communication(s) filed on _____.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

b. ☐ This action is made FINAL.

c. ☑ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☐ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☑ Claims 1 and 11 are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims _____ are patentable and/or confirmed.
4. ☑ Claims 1 and 11 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a) ☐ approved (7b) ☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the certified copies have
   1 ☐ been received.
   2 ☐ not been received.
   3 ☐ been filed in Application No. _____.
   4 ☐ been filed in reexamination Control No. _____.
   5 ☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Status

Claims 1 and 11 of the US Patent No. 9,210,362 to Reddy et al (the '362 patent, hereinafter) have been ordered for the reexamination.

The References

(1) "McNeely" WO 2006/119490 to David Lowell McNeely, filed May 4, 2006, published November 9, 2006,

(2) "Pugel" WO 2007/145637 to Michael Anthony Pugel, filed June 16, 2006, published December 21, 2007.

(3) "Gomez" U.S. Patent No. 8,224,274 to Ramon Gomez et al., filed December 17, 2008, and issued July 17, 2012.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis (i.e., changing from AIA to pre-AIA) for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 and 11 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over McNeely in view of Pugel.

With respect to claims 1 and 11, McNeely teaches a system and a method comprising: in a wideband receiver system: downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels (**mixer module is disclosed in (9:12-15), RF processing block 210 in Figure 2. Furthemore, McNeely teaches L-band signal input to the RF processing block 210 being in the 1-2 GHz frequency range (7:26-28) and A/D converter acting upon processed L-band signals between frequencies 975 and 1425 MHz (9:16-19), thus McNeely repositions the signals to a lower frequency range and performs down-converting. As recited in the Abstract, "receiver for receiving and digitizing a plurality of first signals, each signal containing channels and for simultaneously recovering a set of selected channels from the plurality of first signals". Accordingly "first signals" correspond to channels that are both desired and not desired and then a selected subset is selected after first signals are received, down-converted and digitized**); digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired

television channels **((9:16-26, the "selected channels" are recovered by the digital channel selector 230 in Figure 2, which occurs after down-conversion of the received signals by mixing circuits 210. Hence the input to the A/D converter 220 includes the selected channels and the unselected channels (i.e. desired and undesired channels)**; selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies (**column 9:16-26, wherein "*The A/D converter 220 digitizes the processed L-band signal into a series of samples, each sample containing a group of bits*", wherein L-band signal comprises the plurality of desired television channels. See also 10:1-11, wherein channels are being selected. Figure 2 also depicts element 230 which is "digital channel selector". Moreover, claims 7, 13 and 22 are also directed to selecting channels**); and outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels as a digital datastream (**10:12-16**).

McNeely, however does not explicitly teach outputting the selected plurality of television channels to a demodulator.

On the other hand, Pugel teaches outputting the selected plurality of television channels as a digital datastream (**Pugel further teaches "*demodulating the plurality of digital RF channels*" and he also teaches receiving plurality of "*digital cable television channels within a single digital receiver circuit*" (paragraphs [0011] and [0012]). Pugel also discloses that *"each digital channel signal is then coupled to a separate demodulator 141, 142 and 143*" (paragraphs [0027] and [0010])**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teachings of McNeely and Pugel and utilize Pugel's demodulator to process a digital datastream of McNeely, in order to efficiently extract information from the modulated (outputted) carrier wave and carry out error corrections.

Claim 1 and 11 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Pugel in view of Gomez

With respect to claims 1 and 11, McNeely teaches a system and a method comprising: in a wideband receiver system (**Abstract, wherein Pugel teaches receiver that processes frequencies in the range between 5MHz and 900 MHz (i.e. wideband receiver system)**: downconverting, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels (**paragraphs [0024] and claim 18, wherein plurality of analog signals in different frequency ranges are converted into digital signals and wherein the signals then are downconverted as explained in claim 18**); digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels (**paragraphs [0009], [0024] and claim 18, wherein entire signal input (i.e. both desired and undesired television channels) are processed and first and second digital signals are formed)**; selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies (**"*selecting (e.g., extracts or selects),by***

digital circuitry(e.g., digital channel select or of the digital tuner) of said wide band receiver system(e.g., Pugel's apparatus), said plurality of desired television channels (e.g., Pugel's digital channels desired to be recovered) from said digitized plurality of frequencies (e.g., from the digitized analog signals). Specifically, Pugel discloses extracting desired television programs (e.g., particular digital channels desired to be recovered) from the down converted, digitized frequencies (e.g., the "downconvert[ed]... first digital signal and ... second digital signal.")" paragraph [0038] and Figure 3, wherein tuner 130 corresponds to the selecting unit, and wherein "extracting" corresponds to the step of selection, wherein desired information is extracted to be provided to demodulator. See also paragraphs [0042] – [0045] and Abstract); and outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels as a digital datastream (**paragraphs [0010], [0024], [0040] and Figure 3. More specifically Pugel teaches that each separate analog signal is converted from analog to digital form in an analog-to-digital converter 121, 122 and 123. Each digital channel signal is coupled to a separate demodulator 141, 142 and 143**).

Pugel, however does not explicitly disclose that the downconverting is performed by a mixer module of the wideband receiver system.

On the other hand, Gomez teaches a tuner which selects and downconverts a desired or selected channel from a RF input signal. More specifically mixer 301 down-converts the desired channel in RF signal (**4:6-19**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teachings of Pugel and Gomez and utilize Gomez's teaching about employing a mixer to perform down-conversion in order to efficiently processing inputted signals. Pugel teaches down-conversion performed after the conversion from analog to digital, performing this step before A/D conversion was well known in the art and thus it would be obvious to one of ordinary skill in the art to change the order of the operations if needed.

NOTICE RE PATENT OWNER'S CORRESPONDENCE ADDRESS

Effective May 16, 2007, 37 CFR 1.33(c) has been revised to provide that: The Patent owner's correspondence address for all communications in an ex parte reexamination or an **inter partes** reexamination is designated as the correspondence address of the patent.

Revisions and Technical Corrections Affecting Requirements for Ex Parte and Inter Partes Reexamination, 72 FR 18892 (April, 16, 2007) (Final Rule)

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of this revision to 37 CFR 1.33(c), automatically changed to that of the patent file as of the effective date.

This change is effective for any reexamination proceeding which is pending before the Office as of May 16, 2007, including the present reexamination proceeding, and to any reexamination proceeding which is filed after that date.

Parties are to take this change into account when filing papers, and direct communications accordingly.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of Change of Correspondence Address in the reexamination proceeding and/or the patent (depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone Numbers for reexamination inquiries:

Reexamination	(571) 272-7703
Central Reexam Unit (CRU)	(571) 272-7705
Reexamination Facisimile Transmission No.	(571) 273-9900

Conclusion

Claims 1 and 11 are rejected under 35 U.S.C. 103(a).

Extensions of Time

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extension of time in reexamination proceedings are provided for in 37 CFR 1.550(c).

After the filing of a request for reexamination by a third party requester, any document filed by either the patent owner of the third party requester must be served on the other party (or parties where two or more third-party-requester proceedings are merged) in the reexamination proceeding in the manner provided in 37 CFR 1.248. See 37 CFR 1.550(f).

Litigation Reminder

The patent owner is reminded of the continued responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP § 2207, 2282 and 2286.

Correspondence

All correspondence relating to this *ex parte* reexamination proceeding should be directed:

Patent Center: Please use Patent Center (https://www.uspto.gov/patents/apply/patent-center) to file and manage your applications and requests.

By Mail to: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents

United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Patent Center

The USPTO is retiring EFS-Web and Private Pair, effective 15 November 2023. Please use Patent Center (https://www.uspto.gov/patents/apply/patent-center) to file and manage your applications and requests. Visit the EFS-Web and Private PAIR Retirement (https://www.uspto.gov/patents/efs-web-and-private-pair-be-retired) and Patent Center Information pages for more information.

Patent Center has 100% of the functionality of EFS-Web and Private PAIR, and is available to all users for electronic filing and management of patent applications. Attend a transition to Patent Center Training session (https://www.uspto.gov/about-us/events/patent-center) to learn more about filing and managing patent applications.

Any inquiry concerning this communication should be directed to the Central Reexamination Unit at telephone number 571-272-7705.

/ANGELA M LIE/
Primary Examiner, Art Unit 3992

Conferees:

/LUKE S WASSUM/
Primary Examiner, Art Unit 3992

/ALEXANDER J KOSOWSKI/
Supervisory Patent Examiner, Art Unit 3992

Notice of References Cited	Application/Control No. 90/019,255	Applicant(s)/Patent Under Reexamination 9210362	
	Examiner ANGELA M LIE	Art Unit 3992	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date YYYY-MM-DD	Name	CPC Classification	US Classification
*	A	US-7899087-B2	2011-03-01	McNeely; David Lowell	H04B7/18526	370/464
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date YYYY-MM-DD	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in YYYY-MM-DD format are publication dates. Classifications may be US or foreign.

Reexamination	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/019,255	9210362
	Certificate Date	Certificate Number

Requester Correspondence Address: ☐ **Patent Owner** ☑ **Third Party**

Haynes and Boone, LLP
2801 N. Harwood St.
Suite 2300
Dallas TX 75201

LITIGATION REVIEW ☑	A.M.L (examiner initials)	14 March 2024 (date)
Case Name		Director Initials
IPR2024-00434		
IPR2024-00433		
IPR2024-00432		
2:23cv1049 Entropic Communications Llc v. Cox Communications, Inc		
2:22cv125 Entropic Communications Llc v. Charter Communications Inc.		

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	**NUMBER**

/ANGELA M LIE/ Primary Examiner, Art Unit 3992	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/019,255	9210362
	Examiner	Art Unit
	ANGELA M LIE	3992

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Litigation Search	03/14/2024	A.M.L
Reviewed prosecution history of the US Patent No. 9,210,362	03/11/2024	A.M.L
Patent Data Portal (PDP) for continuity data	03/14/2024	A.M.L
P-TACTS for AIA proceedings (3 pending IPRs found)	03/14/2024	A.M.L

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/ANGELA M LIE/ Primary Examiner, Art Unit 3992	

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P.O. Box 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
90/019,255	**05/07/2024 11:45:10 PM Z ET**	**189005.TR003**

Title of Invention

WIDEBAND TUNER ARCHITECTURE

Application Information

APPLICATION TYPE	Utility / ex parte reexam	PATENT #	9210362
CONFIRMATION #	5785	FILED BY	Kimberly Ewing
PATENT CENTER #	65415845	FILING DATE	09/20/2023
CUSTOMER #	153979	FIRST NAMED INVENTOR	- 9210362
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Shen Wang

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
189005.TR003_Petition_For_Extension_of_Time_to_Respond_to_OA.docx.pdf	6	Reexam Request for Extension of Time	193 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
189005.TR003_Petition_For_Extension_of_Time_to_Respond_to_OA.docx.pdf	7BF37C7D8150133A55427491CA1FC2382B486DB74CC889671ED7A1D0C145C8152DD480F647DC6B425E99E4FBF7AD5F0ED6AD1E532EA6A3A0B8D51BB0818C6DE8

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
90/019,255	05/07/2024 11:45:10 PM Z ET	189005.TR003

Title of Invention

WIDEBAND TUNER ARCHITECTURE

Application Information

APPLICATION TYPE	Utility / ex parte reexam	PATENT #	9210362
CONFIRMATION #	5785	FILED BY	Kimberly Ewing
PATENT CENTER #	65415845	AUTHORIZED BY	Shen Wang
CUSTOMER #	153979	FILING DATE	09/20/2023
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	- 9210362

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 1299	E202457N45546020	Shen Wang

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1251	EXTENSION FOR RESPONSE WITHIN FIRST MONTH	220.00	1	220.00
			TOTAL AMOUNT:	$220.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C.

371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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CERTIFICATE OF ELECTRONIC SUBMISSION
I hereby certify this document is being electronically filed with the U.S. Patent and Trademark Office on:
Date: May 7, 2024 Name: Shen Wang, Reg. No. 71,847 Signature: /Shen Wang/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Owner: Entropic Communications, LLC

Inventors: Madhukar Reddy et al.

App. No.: 90/019,255

Filed: September 20, 2023

Conf. No.: 5785

Examiner: LIE, ANGELA M.

Art Unit: 3992

Title: WIDEBAND TUNER ARCHITECTURE

Docket No.: 189005.TR003

PATENT OWNER'S PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.550(C)

Dear Examiner Angela M. Lie:

Pursuant to 37 C.F.R. § 1.550(c), Patent Owner Entropic Communications, LLC ("Entropic" or "Patent Owner") petitions for a two (2) month extension of time to reply to the first Office Action ("OA"), mailed March 18, 2024, in the above case. The extension is requested to allow reasonable time to prepare a response to the OA. The extension is also based on the past, continuing, and additional extraordinary circumstances as the response is prepared, including the large number of pending post-grant challenges related to the Patent-at-Issue, related patents, and other patents owned by Patent Owner.

The current shortened deadline to respond with no extension is May 18, 2024 (OA at 3). The requested deadline for response with a two-month extension is July 18, 2024. The present petition is being filed with the fee specified under 37 C.F.R. § 1.17(g).

STATEMENT OF FACTS ("SOF")

1) On December 8 2015, U.S. Patent No. 9,210,362 (the "'362 Patent" or "Patent-at-Issue"), issued with 20 claims, from an application filed on February 5, 2015.

2) The '362 Patent has been asserted in three district court cases, two of which are still pending:

   a) *Entropic Communications, LLC v. Charter Communications, Inc. et al.* (Eastern District of Texas Case No. 2-22-cv-00125 filed April 27, 2022 and dismissed December 10, 2023).

   b) *Entropic Communications, LLC v. Cox Communications, Inc. et al.* (Central District of California Case No. 2-23-cv-01049 filed February 10, 2023 and still pending).

   c) *Entropic Communications, LLC v. Comcast Corporation et al.* (collectively "Comcast") (Central District of California Case No. 2-23-cv-01050 filed February 10, 2023 and still pending).

3) On September 20, 2023, Unified Patents, LLC, in the present reexamination, filed a request for the instant *ex parte* reexamination of '362 Patent claims 1 and 11, which was assigned Control No. 90/019,255.

4) On February 16, 2024, Comcast filed three petitions for *inter partes* review of the '362 Patent (IPR2024-00432, -00433, and -00434). Collectively, Comcast challenged claims 1-20, based on combinations, some including *Pugel.*

   a) On February 16, 2024, Comcast also filed three petitions for *inter partes* review of U.S. Patent No. 11,381,866 (IPR2024-00435, -00436, and -00437), including grounds based on *Pugel.* The '866 Patent is an indirect continuation of the '362 Patent.

   b) On February 16, 2024, Comcast also filed three petitions for *inter partes* review of U.S. Patent No. 11,399,206 (IPR2024-00438, -00439, and -00440), including grounds based on *Pugel.* The '206 Patent is an indirect continuation of the '362 Patent.

5) There are an additional seventeen *inter partes* reviews pending for patents owned by Patent Owner (IPR2024-00373, -00393, -00430, -00431, -00441, 00442, -00444, -00445, -00446, -00452, -00462, -00546, -00555, -00560, -00562, -00578, -00579) as well as two pending *ex parte* reexaminations (Control Nos. 90/019,247, and 90/019,484).

6) On March 18, 2024, in the present reexamination, the Examiner issued a Non-Final Office Action rejecting claims 1 and 11 based on combinations including *Pugel.*

7) Patent Owner's counsel was retained for the present reexamination in late February 2024.

DISCUSSION

An extension of time to respond to an office action in a reexamination may be granted on a showing by the Patent Owner of "sufficient cause." 37 C.F.R. §1.550(c); M.P.E.P. § 2265. In making this determination, the Office balances the statutory requirement that the proceedings be conducted with special dispatch against "the desire to provide the patent owner with a fair opportunity to respond." M.P.E.P. § 2265.

Patent Owner respectfully requests an extension of time to respond to the first Office Action in view of the number of other relevant proceedings involving challenges and other interpretation of the patent rights challenged in this case (SOF ¶¶ 2, 4-5). To ensure consistency and accuracy, Patent Owner's representatives must review the history in all of these proceedings, and will also need to work with Patent Owner's *inter partes* review and district court litigation counsel to ensure consistency and accuracy with respect to positions taken in in *inter partes* review and litigation (SOF ¶ 2, 4-5). Finally, the availability of counsel has been and will continue to be limited by other unavoidable obligations. Despite diligent effort underway, it is clear that additional time is needed to respond to the Office Action.

Patent Owner respectfully specifies that given these circumstances and the course of the present reexamination to date, a reasonable period of extension is two (2) months. No prior extension of time has been requested or granted.

I. There Is Sufficient Cause For Granting An Extension.

This is a third-party requested ex parte reexamination. M.P.E.P. § 2265(V1), states:

> [I]n third party requested ex parte reexaminations, a first request for an extension of time will generally be granted if a sufficient cause is shown, and for a reasonable time specified . . . The reasons stated in the request will be evaluated by the CRU SPRS or TC Director, and the requests will be favorably considered where there is a factual accounting of reasonably diligent behavior by all those responsible for preparing a response within the statutory time period. Second or subsequent requests for an extension of time . . . will only be granted in extraordinary situations.

Because no prior extension of time has been requested, it follows that no "extraordinary situation[]" need be shown for the present first request for an extension to be granted. *Id.* In fact, the situation is amply supportive of a grant of extension. For the reasons stated below, including diligent behavior by those responsible for preparing a response within the statutory time period, it is submitted that the present first request for an extension of time should be favorably considered and granted.

a. *Especially In Light Of Its Recent Retention, Counsel Needs Additional Time to Retain To Analyze The Patent, The Prior Art, The Office Action, And Conduct An Examiner Interview.*

Patent Owner's counsel was retained in late February (SOF ¶ 7). The current deadline for the response to office action is May 18, 2024. During this period, Patent Owner's counsel has been diligently analyzing the patent, the references, and the office action. Patent Owner's counsel also has been evaluating whether to engage an expert to provide a declaration. Patent Owner's counsel also respectfully intends to request an Examiner interview to discuss the rejections.

The necessity of an extension to accommodate the timeline above is further heightened due to the limited availability of Patent Owner's counsel, as discussed in the following section.

b. *Availability Of Counsel Is Limited.*

The availability of counsel is circumscribed by unavoidable factors. Patent Owner's counsel, Arch & Lake LLP, is a small firm of fewer than twelve attorneys. It has been and will continue to be very busy on numerous concurrent matters including a matter scheduled for trial in October before the International Trade Commission necessitating dozens of overseas depositions in the next two months, and over a half dozen active district court cases. These matters cannot be extended except by order of the relevant tribunal or with opposing parties' consent. These activities, in the circumstances, contribute to the need for the requested extension.

c. *Additional Time Is Required To Ensure Appraisal Of Prior And Concurrent Inter Partes Reviews And Litigation Activities Under 37 C.F.R. 1.565(a).*

The effort required in this reexamination by Patent Owner and its counsel in its appraisal of prior and concurrent proceedings is significant because of the past and concurrent inter partes review and litigation activity, including multiple district court litigations and IPRs. (SOF ¶¶ 2, 4-5). Two district court actions and nine IPRs are pending involving the '362 Patent and related patents, as well as one district court action that was pending for nearly 18 months. (SOF ¶¶ 2, 4). Notably, there are also 20 additional pending post-grant matters involving patents owned by Patent Owner.

To prepare Patent Owner's response and satisfy its Rule 11.18(b) and other obligations, it has been necessary for counsel to coordinate with counsel representing Patent Owner in other proceedings, including those involving the '362 Patent, and related patents, in order to review

what, if any, materials bear on the response to the Office Action and must be disclosed to the Office, determine pertinent positions taken, and ensure consistency with such positions.

In short, the complexity of this case due to the past and ongoing litigation and IPR matters involving this patent have led to additional necessary work by Patent Owner's counsel that contributes to the need for an extension of time to respond to the Office Action.

d. *The Patent Owner's Activity To Date Has Been Reasonable and Diligent.*

As noted above, between the mailing of the Non-Final Office Action and today, Patent Owner has worked diligently to coordinate amongst Patent Owner's IPR and litigation counsel, including consideration of an expert declarant. Patent Owner has already done significant work analyzing the reexamination request and Non-Final Office Action.

II. *The Length Of The Extension That Patent Owner Requests Is Reasonable.*

As already noted, Patent Owner requests an extension of time of two (2) months. This length of extension is reasonable under the circumstances in light of the need to prepare testimony and other evidence, and limited witness and counsel availability.

The M.P.E.P. states that a reasonable extension of time in third-party requested reexaminations is "usually one month," and that "requests for an extension of more than one month in third party requested reexaminations will only be granted in extraordinary situations." M.P.E.P. § 2265(VI). In the present reexamination, however, extraordinary circumstances exist as described above. It, is further noted that M.P.E.P. § 2265(VII) states (emphasis added):

> In any *ex parte* reexamination proceeding, *including third party requested reexaminations* . . . , the filing of a timely first response to a *final* rejection *having a shortened statutory period for response* is construed as including a request to extend the shortened statutory period for an additional *two months,* but in no case may the period for response exceed six months from the date of the final action.

The rejections in the present Office Action are not made final (OA at 3), so M.P.E.P. § 2265(VI) is not applicable to Patent Owner's response to the present Office Action or to the present request for extension. However, it remains the case that the M.P.E.P. expressly contemplates a default construction of Patent Owner's response to final rejections in third party requested reexaminations as requesting extension of the shortened statutory period by two months. (It is further noted that "no cause" extensions of time of two months, and for-cause extensions of additional months, are available in patent owner requested or Director ordered *ex parte* reexaminations (M.P.E.P. § 2265(V)). While these provisions do not directly apply to the present request, they suggest that

depending on the circumstances, a reasonable time for extension may be significantly more than one month.

CONCLUSION AND RELIEF REQUESTED

Based on the foregoing, it is respectfully submitted that there is cause under 37 C.F.R. § 1.550(c) for a two (2) month extension of time, extending the time period to at least July 18, 2024, for Patent Owner to prepare its response to the Office Action. If the requested period of extension is not found to be for a reasonable time, M.P.E.P. § 2265(V1), an extension is respectfully requested for a reasonable time. Patent Owner thanks the Examiner for their time and attention in this matter.

Respectfully submitted,

Date: May 7, 2024

/Shen Wang/

Shen Wang, Reg. No. 71,847
Arch & Lake LLP
203 N. LaSalle Street, Suite 2100
Chicago, IL 60601
Tel: 636-236-5390

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PATENT AND TRADEMARK OFFICE

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
90/019,255	**05/08/2024 05:14:55 PM Z ET**	**189005.TR003**

Title of Invention

WIDEBAND TUNER ARCHITECTURE

Application Information

APPLICATION TYPE	Utility / ex parte reexam	PATENT #	9210362
CONFIRMATION #	5785	FILED BY	Kimberly Ewing
PATENT CENTER #	65431384	FILING DATE	09/20/2023
CUSTOMER #	153979	FIRST NAMED INVENTOR	- 9210362
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Shen Wang

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
189005.TR003_Certificate_of_Service.pdf	1	Reexam Certificate of Service	126 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
189005.TR003_Certificate_of_Service.pdf	7F1A882EFDA9553C1AD531A3FC69982FC38CFA462947B5D9F79FC1AA16A14F21C78A79744596A573F795B1C405C24C858B659A55A80C3DCD0004F827E9D3FFCC

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as

described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Owner: Entropic Communications, Inc.

Inventors: Madhukar Reddy et al.

App. No.: 90/019,255

Filed: September 20, 2023

Conf. No.: 5785

Examiner: LIE, Angela M.

Art Unit: 3992

Title: WIDEBAND TUNER ARCHITECTURE

Docket No.: 189005.TR003

CERTIFICATE OF SERVICE

Mail Stop *Ex Parte Reexam*
Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner,

I hereby certify that I served a copy of this Patent Owner's Petition for Extension of Time Under 37 C.F.R. 1.550(C) on the *ex parte* reexamination requestor in accordance with MPEP § 2266, 37 C.F.R. § 1.550 and 35 C.F.R. § 1.248 via first class mail and email on May 8, 2024. The name and address of the party served is:

Raghav Bajaj
Haynes and Boone, LLP
2323 Victory Avenue, Suite 700
Dallas, Texas 75219

Respectfully submitted,

Date: May 8, 2024

/Shen Wang/
Shen Wang, Reg. No. 71,847

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/019,255	09/20/2023	9210362	189005.TR003	5785

153979 7590 05/09/2024

Arch & Lake LLP
203 North LaSalle Street, Suite 2100
Chicago, IL 60601

EXAMINER	
LIE, ANGELA M	

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
05/09/2024	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patents and Trademark Office
P.O.Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

5/9/2024

THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS

HAYNES AND BOONE, LLP
2801 N. HARWOOD STREET
SUITE 2300
DALLAS, TX 75201

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. : 90019255
PATENT NO. : 9210362
ART UNIT : 3992

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above-identified ex parte reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the ex parte reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Decision on Petition for Extension of Time in Reexamination	**Application No.:** 90/019,255	**Applicant(s):** 9,210,362	
	Examiner LIE, ANGELA	**Art Unit** 3992	

1. THIS IS A DECISION ON THE PETITION FILED 05/07/2024 ("May 7, 2024 EOT Petition").

2. THIS DECISION IS ISSUED PURSUANT TO:
   - A. ☒ 37 CFR 1.550(c) – The time for taking any action by a patent owner in a third party requested *ex parte* reexamination proceeding will be extended only for sufficient cause and for a reasonable time specified.
   - B. ☐ 37 CFR 1.550(c) – The time for taking action by a patent owner in a patent owner requested *ex parte* reexamination proceeding will only be extended for more than two months for sufficient cause and for a reasonable time specified.
   - C. ☐ 37 CFR 1.956 – The time for taking any action by a patent owner in an *inter partes* reexamination proceeding will be extended only for sufficient cause and for a reasonable time specified.

   The petition is before the Central Reexamination Unit for consideration.

3. FORMAL MATTERS: Patent Owner requests that the time period for filing a response to the non-final Office action mailed on 03/18/2024, which set a two (2) month shortened statutory period for response, be extended by two (2) months.
   - A. Petition fee per 37 CFR § 1.17(g)):
     - i. ☐ Petition includes authorization to debit a deposit account.
     - ii. ☒ Petition includes authorization to charge a credit card account.
     - iii. ☐ Other: _____.
   - B. ☒ Proper certificate of service was provided. (Not required in reexamination where patent owner is requester).
   - C. ☒ Petition was timely filed.
   - D. ☒ Petition properly signed.

4. DECISION (See MPEP 2265 and 2665)
   - A. ☐ Granted or ☒ Granted-in-part for: one (1) additional month. (See 37 CFR 1.550(c) and 37 CFR 1.956).
     - i. ☒ Other/comment: See page 2 below.
   - B. ☐ Dismissed because:
     - i. ☐ Formal matters (See unchecked box(es) (A, B, C and/or D) in section 3 above).
     - ii. ☐ Petitioner failed to provide a factual accounting of reasonably diligent behavior by all those responsible for preparing a response to the outstanding Office action within the statutory time period.
     - iii. ☐ Petitioner failed to explain why, in spite of the action taken thus far, the requested additional time is needed.
     - iv. ☐ The statements provided fail to establish sufficient cause to warrant extension of the time for taking action (See attached).
     - v. ☐ The petition is moot.
     - vi. ☐ Other/comment: _____.

5. CONCLUSION:

Direct telephone inquiries to either QAS Stephen J. Stein at 571-272-1544 or SPRS Andrew J. Fischer at 571-272-6779.	/Andrew J. Fischer/, Supervisory Patent Reexamination Specialist, Central Reexamination Unit

Patent Owner's May 7, 2024 EOT Petition seeks an extension of time for two (2) additional months (*i.e.*, more than one (1) additional month) to respond to the non-final Office action mailed on March 18, 2024.

In accordance with MPEP § 2265 VI. ¶5, Patent Owner's request for two (2) additional months must be evaluated under the "extraordinary situations" standard.

With respect to the requirements of the "extraordinary situations" standard, the undersigned notes that in the past, situations that have been interpreted by the Office to rise to the level of "extraordinary" were for instance, the death or incapacitation of the Patent Owner and acts of God, such as Hurricane Katrina and the COVID-19 outbreak.

For example, Patent owner argues:

> b. *Availability Of Counsel Is Limited*
>
> The availability of counsel is circumscribed by unavoidable factors. Patent Owner's counsel, Arch & Lake LLP, is a small firm of fewer than twelve attorneys. It has been and will continue to be very busy on numerous concurrent matters including a matter scheduled for trial in October before the International Trade Commission necessitating dozens of overseas depositions in the next two months, and over a half dozen active district court cases. These matters cannot be extended except by order of the relevant tribunal or with opposing parties' consent. These activities, in the circumstances, contribute to the need for the requested extension.
>
> ...
>
> The effort required in this reexamination by Patent Owner and its counsel in its appraisal of prior and concurrent proceedings is significant because of the past and concurrent inter partes review and litigation activity, including multiple district court litigations and IPRs.
>
> - May 7, 2024 EOT Petition, p4.

Patent Owner's statements such as "[i]t has been and will continue to be very busy on numerous concurrent matters," and "its counsel in its appraisal of prior and concurrent proceedings is significant" are statements of resource management. Resource management is not a proper reason why, in spite of actions taken, more time is necessary.

Based upon a review of the entire May 7, 2024 EOT Petition, Patent Owner has not alleged nor shown any "extraordinary situations." Accordingly, the "extraordinary situations" standard has not been met.

Patent Owner also states that "Patent Owner's counsel also respectfully intends to request an Examiner interview to discuss the rejections." *Id.* The undersigned finds this statement weighs in favor of Patent Owner establishing a sufficient explanation why, in spite of the action taken thus far, the requested additional time is needed.

Based upon a review of the entire May 7, 2024 EOT Petition, the undersigned agrees that Patent Owner has provided:

(a) a sufficient factual accounting of reasonably diligent behavior by all those responsible for preparing a response to the outstanding Office action;
(b) a sufficient explanation why, in spite of the action taken thus far, the requested additional time is needed; and
(c) statements that establish sufficient cause to warrant extension of the time for taking action.

Accordingly, May 7, 2024 EOT Petition is hereby granted-in-part for one (1) additional month.

UNITED STATES
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P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
90/019,255	**05/31/2024 06:23:17 PM Z ET**	**189005.TR003**

Title of Invention

WIDEBAND TUNER ARCHITECTURE

Application Information

APPLICATION TYPE	Utility / ex parte reexam	PATENT #	9210362
CONFIRMATION #	5785	FILED BY	Xuanjie Wang
PATENT CENTER #	65755799	FILING DATE	09/20/2023
CUSTOMER #	153979	FIRST NAMED INVENTOR	- 9210362
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	ZHANGYUAN JI

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
189005.TR003-sb0439.pdf	2	Miscellaneous Incoming Letter	182 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
189005.TR003-sb0439.pdf	F4EBB9BE48A0632123940E8AA4E2F024C1ACF5EA02B10779A 4CDE7A04A57C67CD8AAC9D6E50734FF7BFD2BA2E7212B6B1 D47776E99B13B4BDF3AD10B57F0987F

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New Applications Under 35 U.S.C. 111

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Doc Code: ECOMM.AUTH/ECOMM.WTDW
Doc Description: Internet Communications Authorization/Internet Communications Authorization Withdrawal

PTO/SB/439 (11-15)

AUTHORIZATION FOR INTERNET COMMUNICATIONS IN A PATENT APPLICATION OR REQUEST TO WITHDRAW AUTHORIZATION FOR INTERNET COMMUNICATIONS		
	Application No.	90/019,255
	Filing Date	09/20/2023
	First Named Inventor	Madhukar Reddy
	Art Unit	3992
	Examiner Name	ANGELA M LIE
	Practitioner Docket No.	189005.TR003

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. To authorize permission for Internet Communications.

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II. To withdraw authorization for Internet Communications.

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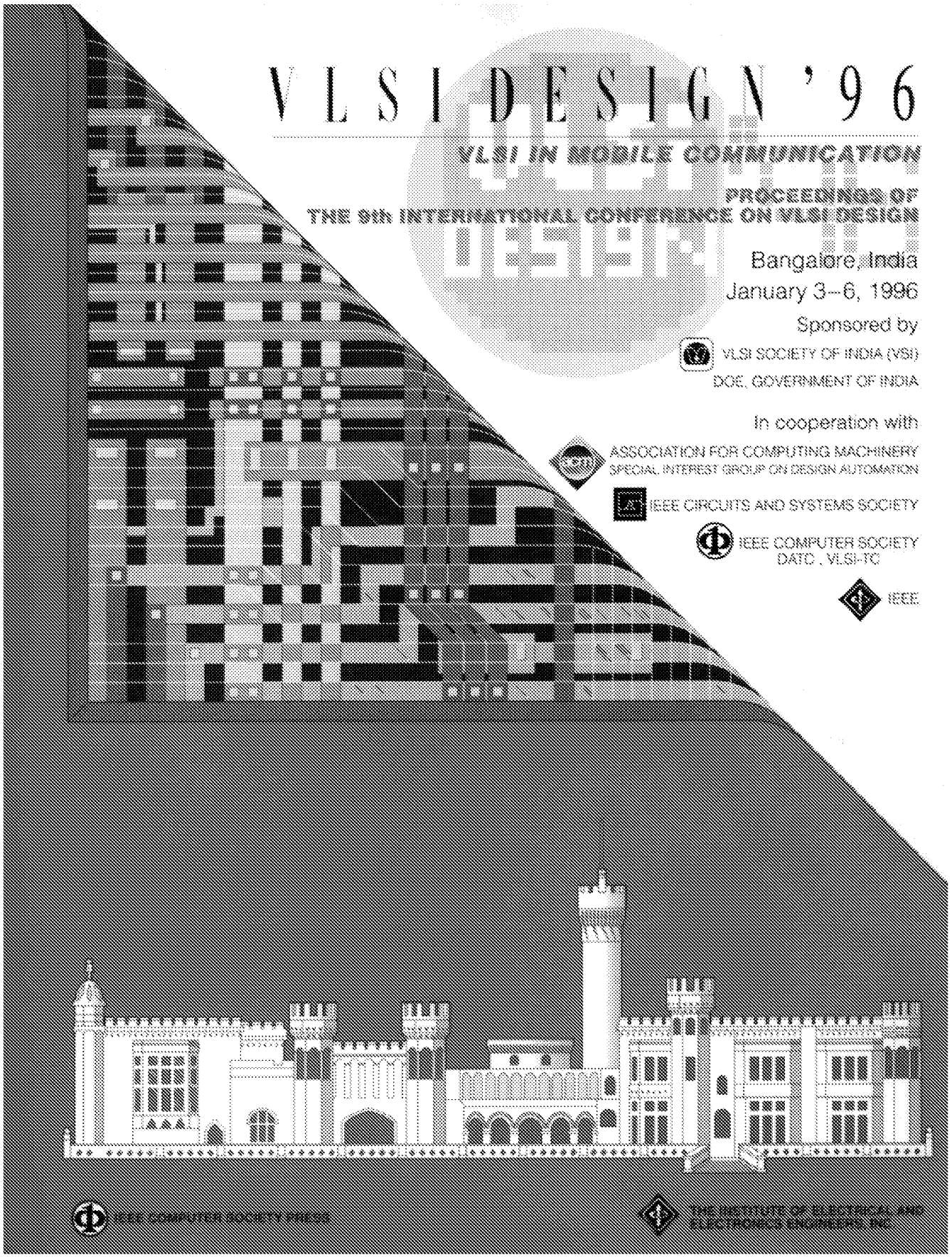
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Ultra Low Power Digital Signal Processing

Anantha P. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

ABSTRACT

The explosive growth of portable wireless devices has elevated power consumption to be one of the most critical design parameters. This paper presents several techniques to implement DSP functions with the lowest possible power consumption. Since power is consumed only when capacitance is being switched, power can be reduced by minimizing this capacitance through operation reduction, choice of data representation, exploitation of spatial and temporal signal correlations, re-synchronization to minimize glitching, and logic, circuit and physical design. Aggressive voltage scaling to 1V and below through circuit and architecture optimization is the key to low-power design. A systems approach to low-power design can result in orders of magnitude power reduction.

1. Introduction

The weight and size of batteries, which are major factors in portable systems, are primarily determined by the power dissipation of electronic circuits. Until recently, there has not been a major focus on a design methodology of digital circuits which directly addresses power reduction, with the focus rather on ever faster clock rates and logic speeds. The emphasis of this work is on minimizing the power consumption in DSP applications, which have two important attributes that make them *different* from general purpose computation: throughput constrained computing and correlation in the data being processed.

The throughput constraint implies that once the required sample rate is met by the hardware, there is no advantage in making the computation faster (unlike general purpose computation where is goal is to compute as fast as possible). This enables a variety of voltage scaling techniques that lower power while maintaining a constant throughput [1]. The second attribute of signal processing systems that can be exploited for low-power is the correlation present in the data being processed. Unlike general purpose computation, the data being processed in many signal processing applications can exhibit high temporal correlation. An important goal of low-power architecture selection is to preserve naturally occurring signal correlations and minimize switching activity.

The focus of this paper is on CMOS circuits and it is well known that power is primarily dissipated in charging and discharging parasitic capacitors and is given by $\alpha_{0->1} * C_L * V_{dd}^2 * f_{clk}$, where C_L is the load capacitance, V_{dd} is the power supply voltage, f_{clk} is the clock frequency, and $\alpha_{0->1}$ is the node transition activity factor (or the fraction of time the node makes a power consuming transition inside a clock period). For example, Figure 1 shows the activity factor, $\alpha_{0->1}$, for a simple 2-input NOR gate as a function of the input signal probabilities, p_a and p_b.

$$\alpha_{0->1} = p_0\, p_1 = (1-(1-p_a)\,(1-p_b))\,(1-p_a)\,(1-p_b) \quad \text{(EQ 1)}$$

The strong influence of signal statistics on power implies that the data statistics must be carefully considered during power optimization. Signal statistics should be considered at all levels of the design including the selection of data representation, resource allocation, operation sequencing, logic structuring, and place and route.

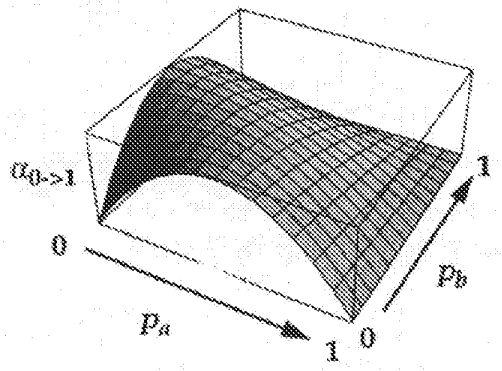


Figure 1: Dependence of power on signal statistics.

2. Optimizing Data Representation

Two's complement is typically chosen to represent numbers in signal processing applications since arithmetic operations are easy to perform. One of the problems with two's complement representation is sign-extension, which causes the msb sign-bits to toggle when a signal changes sign (for example, going from

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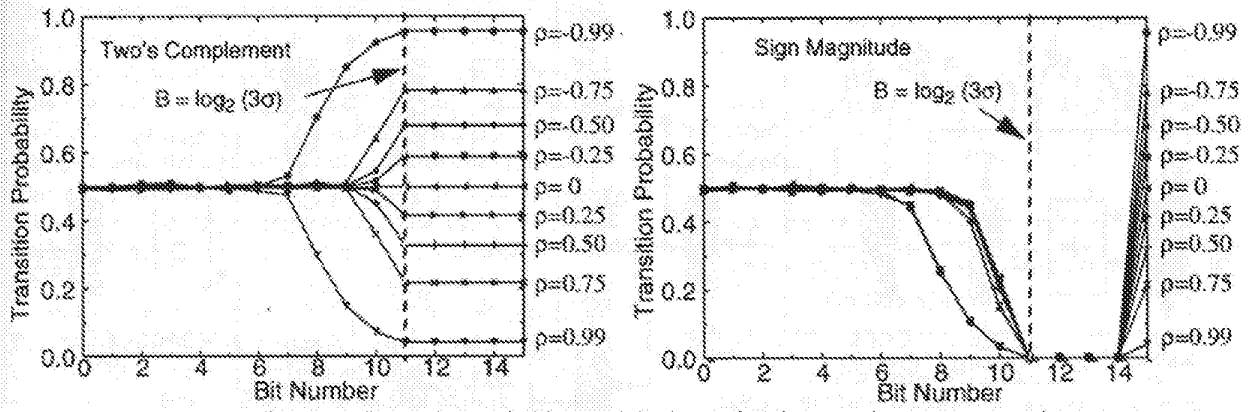


Figure 2: Reducing switching activity by optimizing number representation.

-1 to 0 will result in all of the bits toggling). This is especially significant when the dynamic range of the signals being processed is much smaller than the peak value for the bit-width used since a lot of the msb bits will perform sign-extension. Even when a signal spans the entire bit-width, scaling operations can reduce the dynamic range.

An approach to minimizing the switching activity in the msbs is to use a sign-magnitude representation, in which only one bit is allocated for the sign and the rest to the magnitude [1]. In this case, only one of the msb bits will toggle when the signal switches sign, as opposed to the two's complement representation where due to sign-extension several of the bits will switch. To illustrate this, consider Gaussian data applied to a 16-bit data-bus, which has a mean of 0 and a $3\sigma = 2^{11}$ (the upper breakpoint which represents the dynamic range of the signal lies at $\log_2(3\sigma) = 11$ bits in this case). Figure 2a shows the transition probabilities (both the 0->1 and 1->0) vs. bit position number for two's complement representation as a function of the first order correlation coefficient. A ρ=0 indicates that the data is uncorrelated and therefore the transition probability for the msb's is 1/2 (i.e., there is a 50% chance the output is going to transition between positive and negative). A large positive correlation coefficient implies that the signal changes very slowly and therefore switches sign very infrequently. Similarly, a negative correlation coefficient with a large magnitude implies that the signal changes sign frequently. In two's complement representation, bits 11 to 15 are used for sign-extension. If a sign-magnitude representation is used (Figure 2b), the higher order bits will have a low transition activity and bit 15 (the sign bit) will have the same activity as the two's complement case.

The reduction in the number of transitions for sign-magnitude over two's complement is a function of both the dynamic range of the signal and the signal correlation coefficient. Figure 3 shows the ratio of the number of transitions required in the two's complement representation to that required in the sign-magnitude representation as a function of the signal correlation and normalized dynamic range. The normalized dynamic range of a signal is defined as 3 * σ / Peak Amplitude and the number of transitions is the sum of the transitions for all the bits per clock cycle (i.e., number of transitions = $\sum \alpha_i$, $0 \leq i \leq 15$). The biggest advantage for using sign-magnitude is when the dynamic range is small and the signal has a large negative correlation. Sign-magnitude is clearly useful for driving large busses, where the overhead for converting back to two's complement is quite insignificant compared to the reduction in capacitance switched in the large busses. The scheme presented here is only one example of coding data for reducing power. There are several other schemes which can be used such as log representation, gray-coding [2], conditional inversion coding [3], etc.

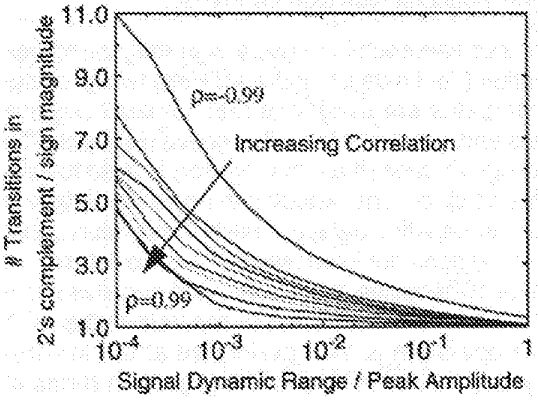


Figure 3: Activity reduction using sign-magnitude.

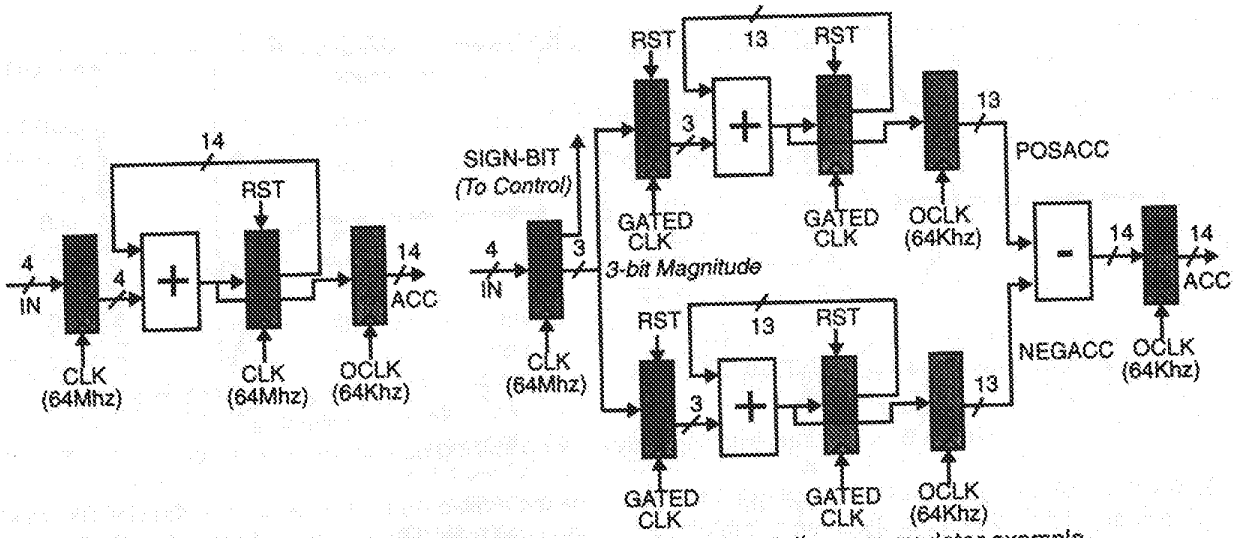


Figure 4: Number Representation trade-off in arithmetic computation: accumulator example.

While sign-magnitude has some advantages in terms of the number of transitions on busses, addition/subtraction operations are difficult to implement. However, in several applications, that require multiple additions inside a sample period (e.g., Multiply Accumulate Units or DSP filters), an architecture optimization can be used that trades silicon area for lower switching activity without altering the throughput. To illustrate this consider a CDMA radio correlator example in which the correlation length is 1024; the samples, whose values ranges from -7 to +7, are accumulated at 64Mhz.

On the left side of Figure 4, is a conventional architecture for an accumulator that uses two's complement representation. The accumulated result is transferred to an accumulator register at 64Khz. In this architecture the msb-bit, bit 3, is tied to bits 4-13 of the adder input for sign-extension and therefore the adder has high switching activity in the msb-bits (due to glitching) when the input changes sign frequently.

Another approach is to use a sign-magnitude representation (right side of Figure 4). Here two accumulator datapaths are used, one that sums all positive numbers and one that sums all negative numbers. The latched sign-bit (from the input register) is used to generate gated clocks that enables the positive datapath latch or the negative datapath latch (this ensures that this scheme does not increase effective clock load). At the end of 1024 cycles, the positive and negative accumulated values are transferred to separate registers. A subtract operation is then performed at the low-frequency and therefore is quite negligible in terms of capacitance overhead. In fact, the higher order bits (3-13) only need an incrementer (as opposed to a full-adder in the two's complement case), reducing the number of gates that are switched in the accumulator. The sign-magnitude implementation, however, requires control circuitry (overhead capacitance) to generate the timing signals for the various latches in the implementation.

By keeping the computation for positive data and negative data separate, the power is not very sensitive to rapid fluctuations in the input data. Table 1 shows the power numbers for various input patterns. Again, the biggest advantage is when the sign toggles frequently. For the case when the input changes very slowly, the sign-magnitude implementation consumes more power (15%) due to the capacitance switched by the control overhead circuitry. For the radio example, data coming in to the accumulator tends to be random.

Table 1. Number representation trade-off for arithmetic.

Input Pattern (1024 cycles)	Two's Complement Power, 3V	Sign Magnitude Power, 3V
Constant (IN= 7)	1.97 mW	2.25 mW
Ramp (-7,-6,...7,-7)	2.13 mW	2.43 mW
Random	3.42 mW	2.51 mW
Min -> Max -> Min (-7, +7,-7,+7,...)	5.28 mW	2.46 mW

3. Time-sharing of Resources

One strategy for implementing signal processing algorithms is the direct mapping approach, where there is a one to one correspondence between the operations on the signal flow graph and operators in the final implementation. Such an architecture style is

conceptually simple and requires a small or no controller. Often, however, due to area constraints or if very high-throughput is not the goal (e.g., speech filtering), time-multiplexed architectures are utilized in which multiple operations on a signal flowgraph can be mapped onto the same functional hardware unit. Given that there is a choice between time-multiplexed and fully-parallel architectures, as is the case in low to medium throughput applications, an important question which arises is what architecture will result in the lowest switching activity. To first order, it would seem that the degree of time-multiplexing would not affect the capacitance switched by the logic elements or interconnect. For example, if a data flowgraph has five additions to be performed inside the sample period, it would seem that there is no difference between an implementation in which one physical adder performs all five additions or an implementation in which there are five adders each performing one addition per sample period. It would seem that the capacitance switched should only be proportional to the number of times the additions were performed but this is not the case since resource sharing can destroy signal correlations and increase switching activity. To demonstrate this trade-off, consider two examples of resource sharing: sharing busses and sharing execution units.

First consider two implementations of two 8-bit counters clocked every cycle one with bus sharing and one without. In the parallel implementation, the two counters are driving two separate busses running at frequency *f* while the time-multiplexed implementation has a single shared bus running at twice the frequency. For the parallel case, the activity is easy to compute. The number of transitions for each bus = $\sum\alpha$ = 1 + 1/2 + 1/4 + ... + 1 / 128 ≈ 2 since the lsb of the counter switches every cycle, the 2nd lsb switches every other cycle, etc. Therefore, the total number of transitions per cycle is approximately 4 for the parallel implementation.

Figure 5 shows the plot of the average number of transitions for the time-shared case as a function of the skew between the counter outputs. The figure also shows the number of transitions for the non-time-shared implementation, which is independent of the counter skew. As seen from this figure, except for one value of the counter skew (when the skew is = 0), the parallel implementation has the lower switching activity. This example illustrates that time-sharing can modify the signal characteristics and cause an increase in the switching activity.

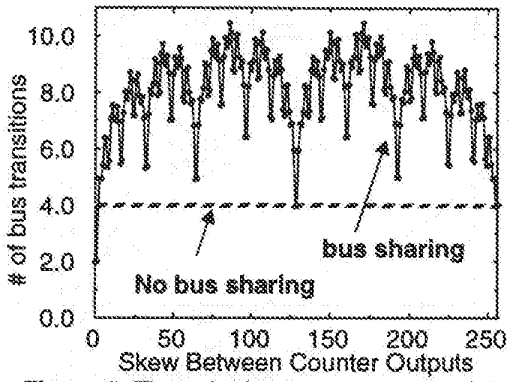


Figure 5: Time-sharing can increase activity.

The second example is a simple second order FIR filter which will demonstrate that time-multiplexing of execution units can increase the switched capacitance. The FIR filter is described as follows:

$$Y = a_0 \bullet X + a_1 \bullet X@1 + a_2 \bullet X@2 = A + B + C \quad \text{(EQ 2)}$$

where @ represents the delay operator and $A = a_0 \bullet X$, $B = a_1 \bullet X@1$ and $C = a_2 \bullet X@2$. Also let $O1 = A + B$. The value of the coefficients are: $a_0 = 0.15625$, $a_1 = 0.015625$, and $a_2 = -0.046875$.

One possible implementation might be to have two physical adders, one performing $A + B = O1$ and the other performing $O1 + C$. An alternate implementation might be to have a single time-multiplexed adder per-

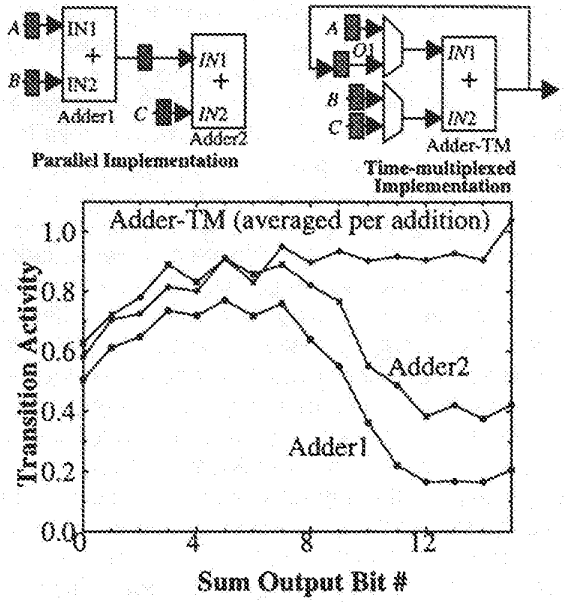


Figure 6: Activity trade-off for time-multiplexed hardware: adder example.

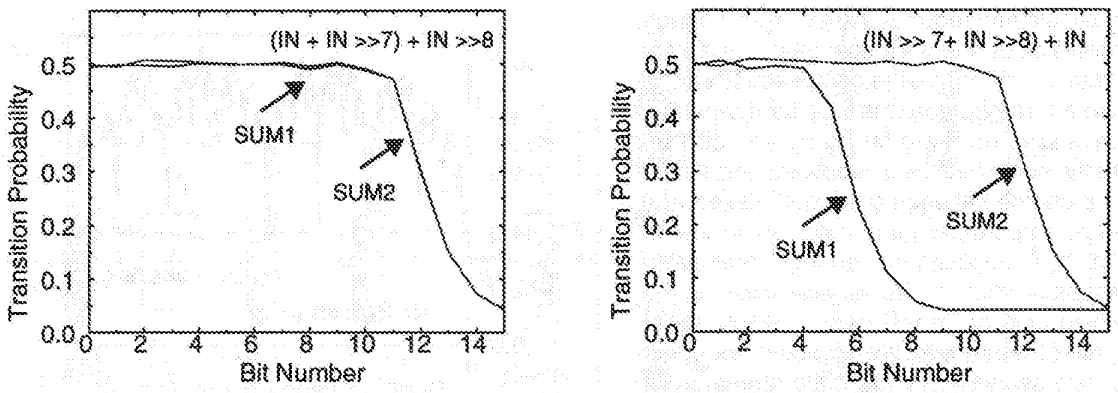


Figure 7: Reducing switching activity by re-ordering inputs.

forming both additions. So, in cycle 1, $A + B$ is performed, and in cycle 2, $O1 + C$ is performed. The topologies for the two cases are shown in Figure 6. In the first implementation, the adders can be chained and therefore the effective critical path can be reduced (chaining two ripple carry adders of N bits has a delay = $(N + 1)$ • Delay of one bit); it is clear that this will result in extra glitching activity but since the objective here is to isolate and illustrate the activity modification only due to time-multiplexing, the first implementation is assumed to be registered. The transition activities (obtained using IRSIM assuming speech input data) for the two adders for the parallel implementation and the average transition activity per addition for the time-multiplexed implementation are shown in Figure 6.

The results once again indicate that time-multiplexing can increase the overall switching activity. The basic idea is that in the fully-parallel implementation, the inputs to the adders change only once every sample period and the source of inputs to the adders are fixed (for example, *IN*1 of adder1 always comes from the output of the multiplier $a_0 * X$). Therefore, if the input changes very slowly (i.e., the input data is very correlated), the activity on the adders become very low. However, in the time multiplexed implementation, the inputs to the adder change twice during the sample period and more importantly arrive from different sources. For example, during the first cycle, *IN*2 of the time-multiplexed adder is set to B and during the second cycle, *IN*2 of the time-multiplexed adder is set to C. Thus, even if the input is constant (which implies that the sign of X, $X@1$ and $X@2$ are the same) or slowly varying, the sign of B and C will be different since the sign of the coefficients a_1 and a_2 are different. This will result in the input to adder switching more often and will therefore result in higher switching activity. That is, even if the input to the filter does not change, the adder can still be switching. For this example, the time multiplexed adder switched 50% extra capacitance per addition compared to the parallel case (even without including the input changes to adders or the multiplexor overhead).

4. Optimizing Ordering of Operation

The switching activity can be reduced by optimizing the ordering of operations in a design. To illustrate this, consider the problem of multiplying a signal with a constant coefficient and assume that the multiplication is decomposed into IN + IN >>7 + IN>>8. Figure 7 shows the results of two alternate implementations for the two required additions. In the first implementation, IN and IN >>7 are added first and the sum (SUM1) is then added to IN >>8. In this case, the SUM1 transition characteristics is very similar to that of the input IN since the amplitude of IN >>7 is much smaller than IN and the 2 inputs have identical sign-bits. Similarly SUM2 is very similar to SUM1 since SUM1 is much larger in magnitude than IN >>8. In the second implementation, the two small number IN>>7 and IN>>8 are added first and the output SUM1 is then added to IN. In this case, the output of the first adder has a small amplitude and therefore lower switching activity. The second implementation switches 30% less capacitance than the first implementation for this data.

5. Voltage Scaling

Since the dominant component of power consumption for a properly designed CMOS circuit is proportional to the square of the supply voltage, operating circuits at the lowest voltage is the key to minimizing the energy consumed per operation. However, the individual circuit elements run slower at lower supply voltages and this must be compensated for through appropriate architectural design. One important class of applications are those which have no advantage in exceeding a bounded computation rate, as found in

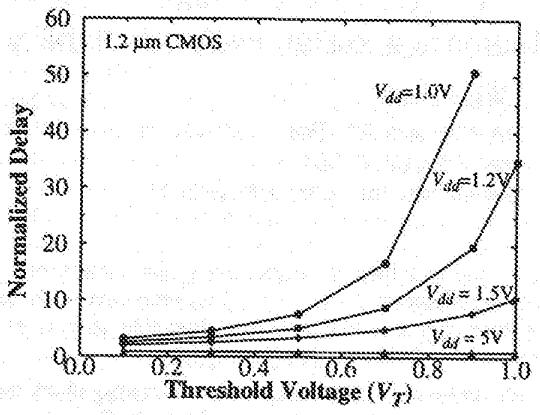


Figure 8: Effect of threshold reduction on the delay for various supply voltages.

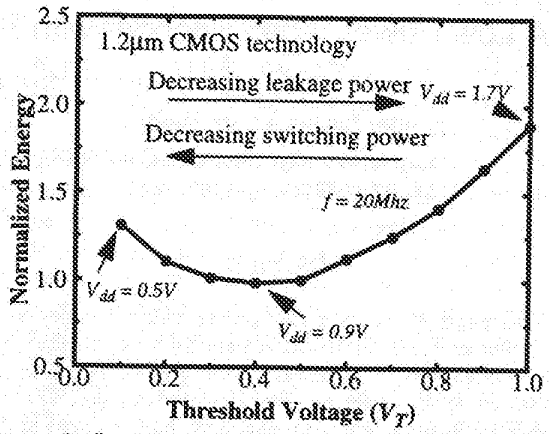


Figure 9: Compromise between dynamic and leakage power dissipation through V_t variation.

real-time signal processing. For such applications, we have previously presented an architecture driven voltage scaling approach in which parallel and pipelined architectures can be used to compensate for increased delays at reduced voltages [4][5]. As the amount of parallelism increases, the amount of overhead circuitry also increases and results in an optimum level of parallelism for low-power. The optimum voltage corresponding to this level of parallelism was found to be close to 1.5V ($\approx 2V_T$) using a standard technology with high threshold devices (V_{TN}=0.7V and V_{TP}=-0.9V).

Reducing the threshold voltage of the device allows the supply voltage to be scaled down (and therefore lower switching power) beyond the architectural optimum without loss in performance. For example, a circuit running at a supply voltage of 1.5V with V_T=1V will have approximately the same performance as the circuit running at a supply voltage of 0.9V and a V_T=0.5V. Figure 8 shows a plot of normalized delay vs. threshold voltage for various supply voltages.

Since significant power improvements can be gained through the use of low-threshold MOS devices, the question of how low the thresholds can be reduced must be addressed. Figure 9 shows a plot of energy vs. threshold voltage for a fixed throughput for a 16-bit datapath ripple carry adder (which essentially represents the power to perform the operation). Here, the power supply voltage is allowed to vary to keep the throughput fixed. For a fixed throughput (e.g., that is obtained at a 20Mhz clock rate), the supply voltage and therefore the switching component of power can be reduced while reducing the threshold voltage. However, at some point, the threshold voltage and supply reduction is offset by an increase in the leakage currents, resulting in an optimal threshold voltage for a given level of logic complexity. That is, the optimum threshold voltage must compromise between improvement of current drive at low supply voltage operation and control of the sub-threshold leakage. Circuits have been designed with power supply voltages as low as 200mV using reduced threshold devices [6].

Acknowledgments

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Title of Invention

WIDEBAND TUNER ARCHITECTURE

Application Information

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PATENT CENTER #	66009955	FILING DATE	09/20/2023
CUSTOMER #	153979	FIRST NAMED INVENTOR	- 9210362
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Hao Tan

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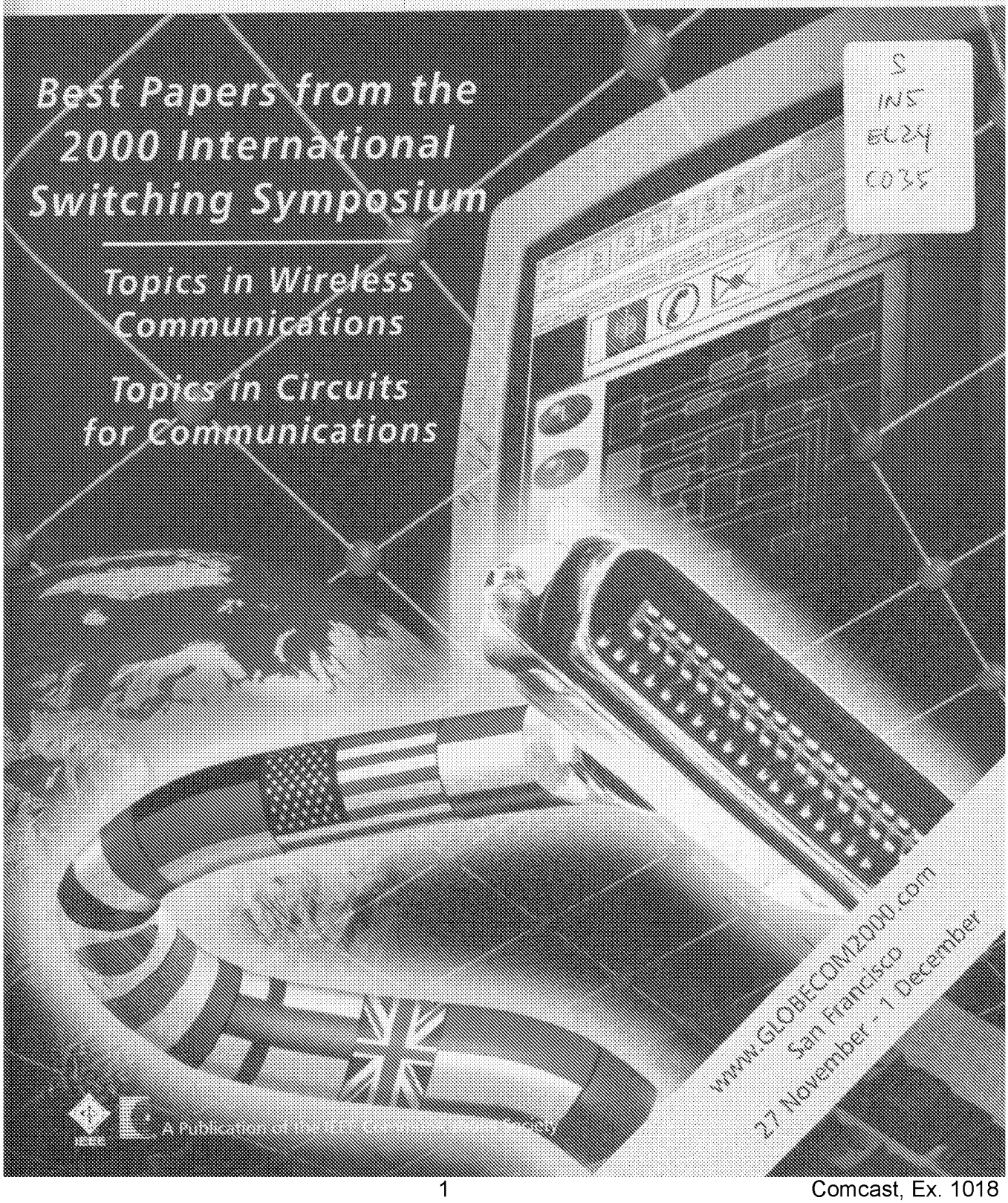
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Classical and Modern Receiver Architectures

Shahriar Mirabbasi and Ken Martin, University of Toronto

ABSTRACT

This article is a review of several classical and modern wireless receiver architectures used in wideband wireless communication systems. The emphasis is on configurations suitable for integration on a single silicon chip. A full understanding of the design trade-offs discussed in this article is necessary for the proper introduction of a new modulation scheme presented in the companion article, "Hierarchical QAM: A Spectrally Efficient DC-Free Modulation Scheme" [1].

INTRODUCTION

The recent surge in applications of radio frequency (RF) transceivers has been accompanied by aggressive design goals such as low cost, low power dissipation, small form factor [2], and high-speed data transfer. These goals are driven by both the need for better portability and affordability, and the ever-increasing demand for higher-speed data communications. Such objectives, together with the usual bandwidth limitations, not only call for highly integrable transceiver architectures, but also for bandwidth-efficient modulation schemes.

To address the demand for better portability and affordability, recent research has been focused toward the development of monolithic transceiver architectures, especially using low-cost complementary metal-oxide semiconductor (CMOS) technology. This approach provides the possibility of integrating analog and digital circuitry on the same chip. In addition, the use of new systems and circuit design techniques facilitates the highest levels of receiver and transmitter integration [3]. Various suitable architectures have been proposed for implementation in deep-submicron CMOS technologies [2–5].

In this article, we review several classical and recently proposed receiver architectures, and discuss their advantages and disadvantages. In a companion article [1], a new spectrally efficient dc-free modulation scheme, suitable for highly integrable receiver architectures, is introduced.

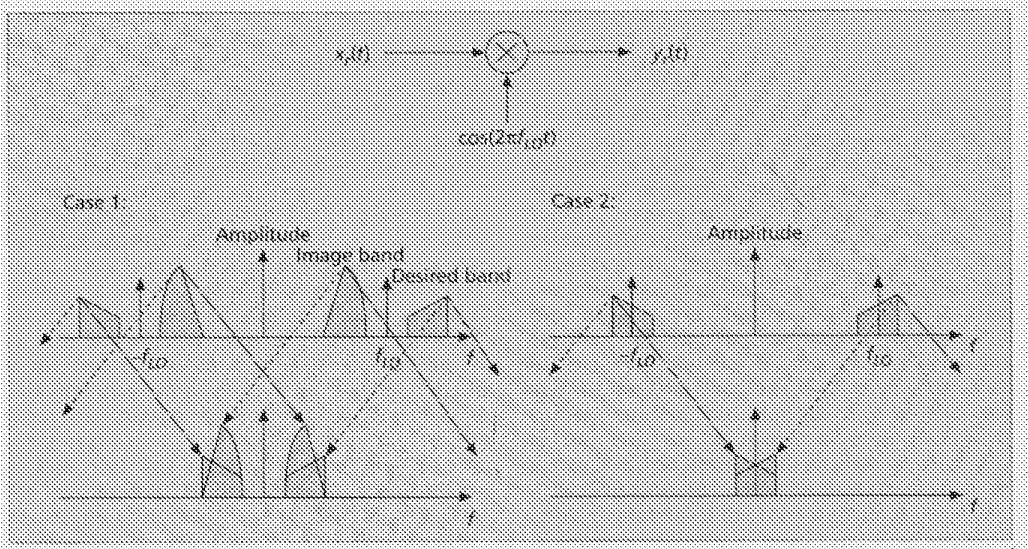


Figure 1. *Mixing a real signal with a real sinusoid for two cases, where f_{LO} is not equal (case 1) and equal (case 2) to the center frequency of the desired signal. The spectra of the inputs of the mixer and the corresponding spectrum of the output of the mixer are shown.*

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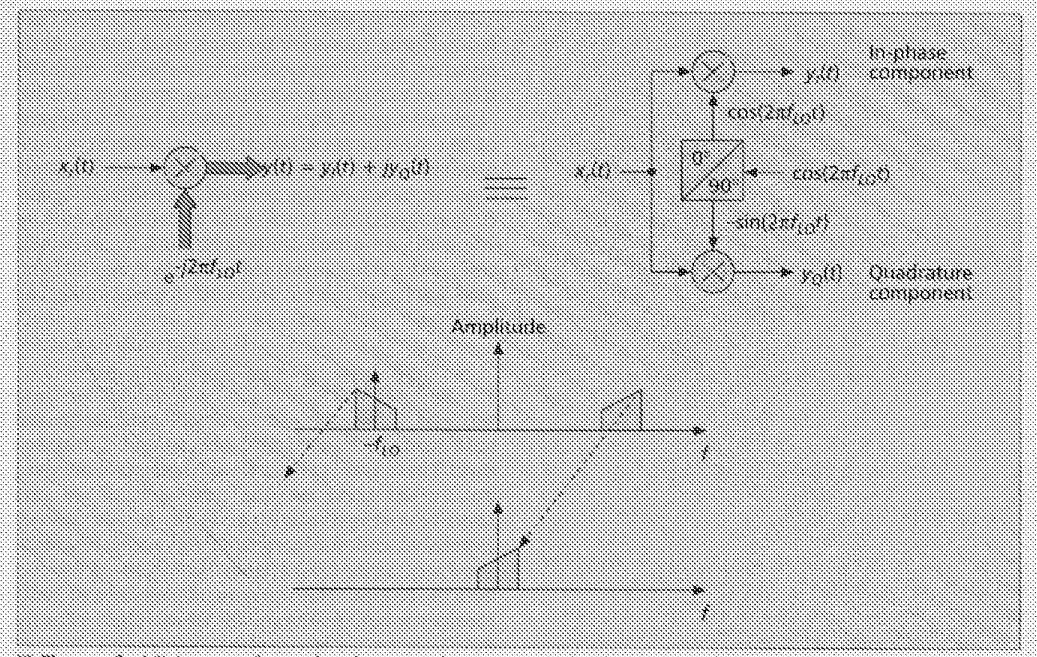


Figure 2. *Mixing a real signal with a complex exponential. The spectra of the real and complex inputs of the mixer, and the spectrum of the complex output of the mixer are shown. Here, complex signals are represented by double lines.*

To address the demand for better portability and affordability, recent research has been focused toward the development of monolithic transceiver architectures, especially using low-cost complementary metal-oxide semiconductor technology.

Background: Real and Complex Mixing

In preparation for the main discussion on receiver architectures, it is useful to review the *image band problem* related to frequency downconversion, an essential operation in any RF receiver. This will be done using complex representation of signals and complex mixing, techniques also useful for the discussions in the companion article [1].

Typically, frequency downconversion of a passband signal is performed by multiplying (mixing) the signal with a sinusoid such as $\cos(2\pi f_{LO}t)$. This is illustrated in Fig. 1 for the two cases in which the frequency of the sinusoid is different from and equal to the center frequency of the signal. Note that for a real signal, the negative and positive Fourier components are complex conjugates of each other. A multiplication in the time domain is equivalent to a convolution in the frequency domain. Since the Fourier transform of a sinusoid contains two equal-amplitude impulses symmetrically placed around zero on the frequency axis, the spectrum of the mixer output signal is the superposition of the positive and negative shifted versions of the spectrum of the input signal. As shown in Fig. 1, two frequency bands symmetric around the multiplying frequency are downconverted to the same output band. The undesired input signal band, which will be superimposed on the desired signal band after mixing, is called the *image band*. It is necessary to suppress any signal in the image band prior to the mixing operation. This is the task of the image-reject (IR) filter which usually precedes the mixer. In the special case where the multiplying frequency is equal to the center frequency of the incoming signal, the image band is the same as the signal band, and the image cannot be eliminated using filtering. Notice that the mixing operation with a real sinusoid generates additional signals above the multiplying frequency. In a typical receiver these high-frequency components (not shown explicitly in Fig. 1) are usually filtered out with a low-pass filter.

The previously discussed image problem arises due to the fact that the frequency spectrum of a real sinusoid contains impulses at both positive and negative frequencies. One way to avoid this problem is to mix the signal with a complex exponential, say $e^{j2\pi f_{LO}t}$, which has only a single frequency component, in this case at a negative frequency ($-f_{LO}$). Although all physical signals are real, complex signals are a convenient mathematical representation for a pair of real signals [5, 6]. A complex signal, $x(t) = x_I(t) + jx_Q(t)$, consists of a real part and an imaginary part, $x_I(t)$ and $x_Q(t)$, respectively, where $x_I(t)$ and $x_Q(t)$ are real signals and

$$j = \sqrt{-1}.$$

Complex signals are processed according to the rules of complex arithmetic. In general, they can have negative and positive frequency components totally different from each other. As an example, the complex exponential $e^{j2\pi f_{LO}t} = \cos(2\pi f_{LO}t) - j\sin(2\pi f_{LO}t)$, has only a single negative-frequency component. Therefore, mixing a real signal with this negative-frequency complex exponential gives a complex signal whose spectrum is a shifted version of the real signal spectrum. *Theoretically*, this eliminates the image problem associated with frequency shifting when mixing with a real sinusoid.

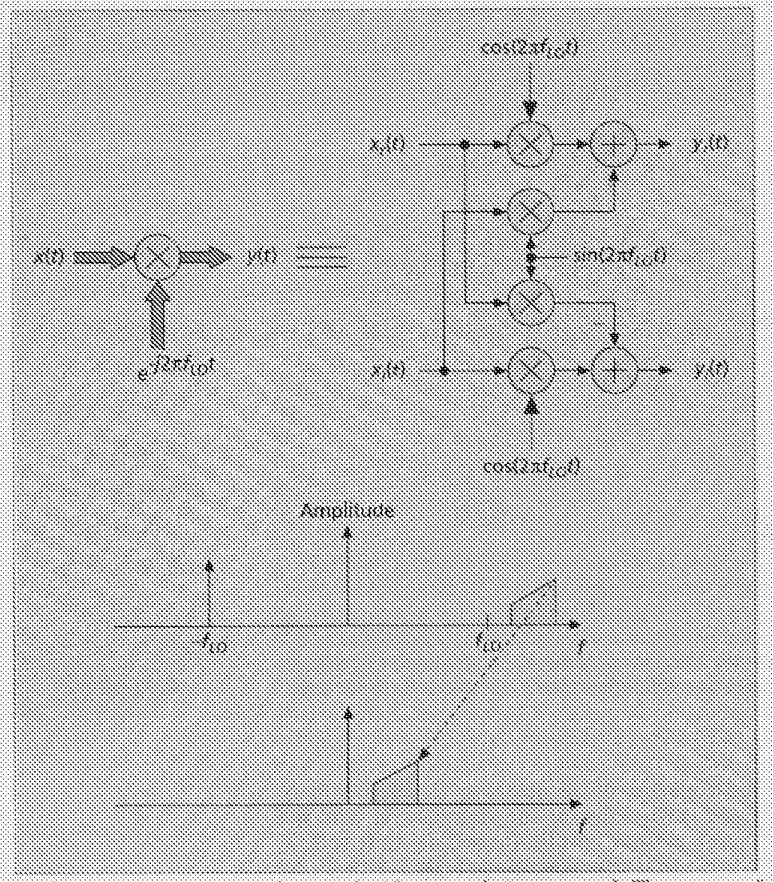


Figure 3. *Mixing a complex signal with a complex exponential. The spectra of the complex inputs of the mixer, and the spectrum of the complex output of the mixer are shown.*

The realization of a multiplier for mixing a real signal with a complex exponential requires two real multipliers, as illustrated in Fig. 2. The real and imaginary parts of the mixer output are called the *in-phase* (I) and *quadrature* (Q) components of the downconverted signal (since cosine and sine are in quadrature). In Fig. 2 the frequency of the complex exponential is chosen to be the same as the center frequency of the passband signal, for comparison with case 3 in Fig. 1. In this case there is no image problem associated with the complex mixer. As discussed in the following section, this fundamental property is used in homodyne receivers.

Now, consider the general case of mixing two complex signals $x(t) = x_r(t) + jx_i(t)$ and $z(t) = z_r(t) + jz_i(t)$: $x(t) \cdot z(t) = (x_r(t) \cdot z_r(t) - x_i(t) \cdot z_i(t)) + j(x_r(t) \cdot z_i(t) + x_i(t) \cdot z_r(t))$. A practical realization of this complex mixer using four real mixers is shown in Fig. 3. Complex mixing is used in IR mixers. These mixers are employed in some recently proposed receiver architectures, discussed later.

In some cases, only the real or imaginary part of a complex mixer output is of interest. One example is the quadrature amplitude modulation (QAM) system modulator [6]. Extracting the real (or imaginary) part of a complex mixer output can be implemented efficiently as shown in Fig. 4. Here, the complex mixer is implemented with two real mixers and one adder.

As a final point, it should be mentioned that in analyzing receivers for undesired image components, it is often necessary to isolate the positive and negative frequency components of the received signal. Figure 5 shows a block diagram of the system for converting an arbitrary complex signal into one that contains only the positive frequency components of the original signal. In this figure, the block with transfer function $-j \cdot \mathrm{sgn}(\omega)$ is the well known Hilbert transformer which shifts its input signal phase by $-90°$ for positive frequencies and $+90°$ for negative frequencies.

Receiver Architectures

Most of the wireless transceivers used so far are based on a conventional heterodyne architecture. These transceivers have good performance, but suffer from high production costs and require a relatively large form factor due to expensive and nonintegrable RF and intermediate frequency (IF) filters. In this section we briefly review the conventional heterodyne receiver topology along with some other recently developed receiver architectures, and discuss their advantages and disadvantages. For each particular receiver architecture, there exists a corresponding transmitter architecture with essentially the same fundamental building blocks. The exception to this regards the transmitter power amplifier, which, although important, is beyond the scope of this article. Therefore, in our review we focus on receiver structures. Further discussions of transmitter architectures can be found in [5, 7].

Conventional Heterodyne Receivers

Most of today's commercially available RF transceivers utilize some variant of conventional heterodyne architecture. In a heterodyne receiver, as shown in Fig. 6, the RF front-end (preselection) filter serves to remove out-of-band signal energy as well as partially reject image band signals. After this prefiltering, the received signal is amplified by a low-noise amplifier (LNA). The IR filter following the LNA further attenuates the undesired signals at the image band frequencies. The desired signal at the output of the IR filter is then downconverted from the carrier frequency to a fixed IF by multiplication (mixing) with the output of a local oscillator (LO). Commonly, in heterodyne receivers, high-performance, low-phase-noise voltage-controlled oscillators (VCOs) employed as LOs are realized with discrete components such as high-quality-factor (Q) inductors and varactor diodes [3].

At the output of the mixer an IF filter, typically followed by a programmable-gain IF amplifier, selects the desired channel and reduces the distortion and dynamic range requirements of the subsequent receiver blocks [3]. The signal can be shifted to baseband and demodulated as shown in Fig. 6, or alternatively further downconverted to lower IFs, and then shifted to baseband and demodulated.

Since, at the carrier frequency, the desired band and image band are separated by twice the IF, it is desirable to choose a high IF to reduce

the requirements on the IR filter. In fact, if the IF is chosen high enough that the preselection RF filter can sufficiently attenuate the image band, it might be possible to directly connect the output of the LNA to the mixer without including an IR filter [7]. On the other hand, since channel selection in a heterodyne system is done at the IF, a low IF allows employment of higher-quality channel-select filters. Therefore, the choice of IF depends on the trade-off between image rejection and channel selection. Other factors influencing the choice of IF are availability and the physical size of commercial filters for different frequencies [2].

Conventionally, all the filters used in the heterodyne system are high-Q discrete component filters, such as surface acoustic wave (SAW) or ceramic filters. Compared to other more integrable receiver architectures, the heterodyne receiver has superior performance with respect to *selectivity*, a measure of a receiver's ability to separate the desired band around the carrier frequency from signals received at other frequencies, and *sensitivity*, the minimal signal at the receiver input for which there is sufficient signal-to-noise ratio (SNR) at the receiver output. This is achieved with the use of high-Q discrete components [3].

Employing high-Q elements does come with some drawbacks. A major limitation is that the off-chip IR filters have low input impedance. This requires a high drive capability for the preceding LNA, inevitably leading to more severe trade-offs between gain, noise figure, stability, and power dissipation in the amplifier [7]. Furthermore, these high-Q filters are difficult and somewhat impractical when realized at high frequencies in an integrated solution, primarily because integrated inductors have at best only moderate Q-factors. In addition, the narrowband discrete-component IF channel-select filter of the heterodyne receiver tailors the particular implementation to a specific standard [3].

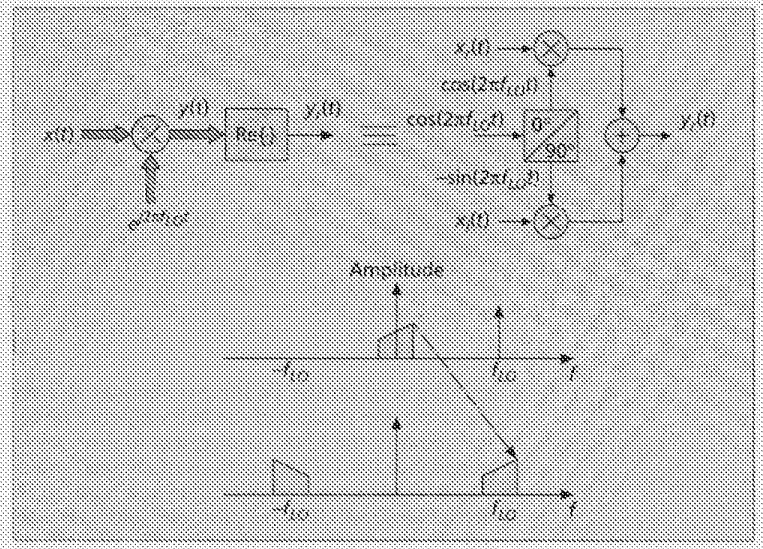


Figure 4. *An efficient implementation for a complex mixer when only a real part of the mixer output is of interest. The spectra of the complex inputs of the mixer, and the spectrum of the real part of the mixer output are shown. Note that since the final output is real signal, its spectrum is complex-conjugate symmetric.*

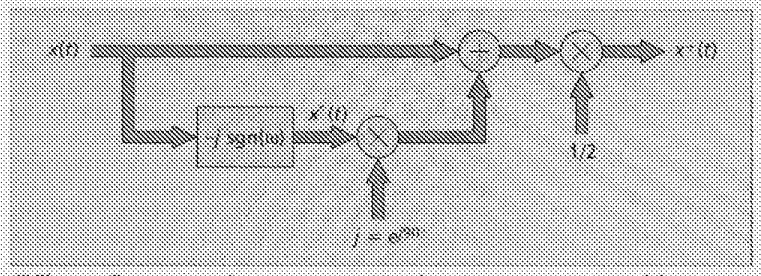


Figure 5. *A system that extracts positive frequency components of the input signal. By changing $e^{j\pi/2}$ to $e^{-j\pi/2}$ (i.e., j to $-j$) in the multiplier, the system would extract the negative frequency components of the input.*

Direct-Conversion Architecture

Direct conversion, also known as *homodyne* or *zero-IF conversion*, is a natural approach to downconverting an RF signal directly to baseband. Alternately, one can think of choosing IF to be zero. This architecture, shown in Fig. 7, employs low-pass filtering in the baseband to suppress nearby interferers and select the desired channel. The quadrature downconversion (I and Q channels) is necessary in typical amplitude and phase or frequency modulated signals because in general the two side-bands of the RF spectrum are different. Mixing with a real sinusoid would result in irreversible corruption of the transmitted information [2]. Note that quadrature downconversion is equivalent to complex mixing, discussed previously (Fig. 2).

The homodyne architecture has several fundamental advantages over the heterodyne counterpart. The intermediary IF stages are removed,

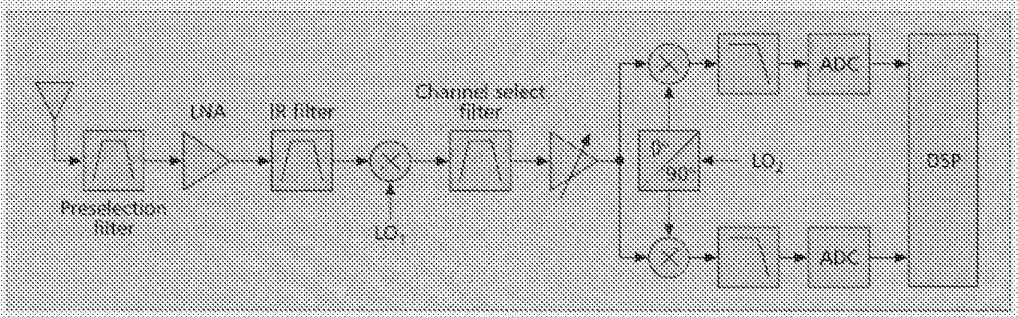


Figure 6. *A generic heterodyne receiver.*

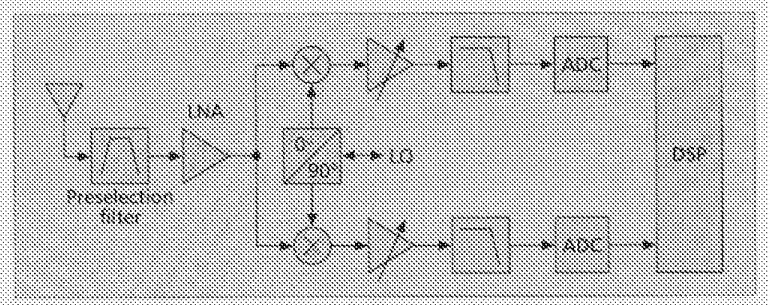


Figure 7. *A generic homodyne receiver.*

and the need for the IR filter is eliminated. Furthermore, the absence of the bulky off-chip IR filters removes the LNA requirement to drive a low impedance load. The functions of channel selection and subsequent amplification at a nonzero IF are replaced with low-pass filtering and baseband amplification, amenable to monolithic integration.

Despite this suitability for higher levels of integration, a homodyne receiver exacerbates a number of issues that either do not exist or are not as serious in a heterodyne receiver. Next, we will briefly review some of these issues.

DC-Offsets — Perhaps the most serious problem is that of dc-offset in the baseband section of the homodyne receiver [4]. These extraneous offset voltages can corrupt the desired signal and/or saturate the following stages. They arise due to the self-mixing phenomenon of the local oscillator or the in-band interferer, aside from the usual element mismatch in the signal path circuitry.

To better understand the origin of these offsets, consider the received signal path shown in Fig. 8. First, the isolation between the LO port and the inputs of the mixer and the LNA is not perfect, and a finite amount of feedthrough exists from the LO port to the other mixer input and to the input of the LNA. Known as *LO leakage*, this effect arises from capacitive and substrate coupling and, if the LO signal is provided externally, through bond-wire coupling. The leakage signal appearing at the inputs of the LNA and the mixer is now mixed with the original LO signal, thus producing a dc component at the output of the mixer. This LO self-mixing can be quite severe, and a time-varying dc-offset occurs when the LO signal leaks out through the antenna, and is radiated and reflected from nearby objects back to the receiver. A similar effect occurs if a large in-band interferer (in the passband of the RF preselection filter) leaks from the LNA output to the mixer LO port and gets multiplied by itself [7]. It should be noted that these dc-offsets exist in heterodyne receivers as well, but are mostly eliminated naturally by the IF band-pass filters.

Thus, direct-conversion receivers require appropriate methods to remove undesired dc offsets. A simple approach is to use ac-coupling in the downconverted signal path. However, since the spectra of all the spectrally efficient modulation schemes currently used exhibit significant energy at dc, such signals are corrupted by ac-coupling filters [4]. A better method is the use of baseband analog and/or digital signal processing (DSP) techniques for offset estimation and cancellation [3][7]. However, these techniques add complexity and do not solve the problems associated with 1/*f* noise at low frequencies in CMOS implementations, a significant issue.

A natural system solution to the dc offset problem in direct-conversion receivers is to minimize the baseband signal energy near dc by choosing a "dc-free" modulation scheme and use ac-coupling for offset elimination. This approach has been successfully used in pager systems with frequency shift keying (FSK) modulation, despite the spectral inefficiency of FSK [4]. In the companion article [1] we introduce a new spectrally efficient dc-free modulation scheme.

LO Leakage — In addition to introducing dc offsets, leakage of the LO signal to the antenna and radiation from there creates in-band interference for other receivers using the same standard [7]. This problem becomes less severe as more sections of RF receivers are fabricated on the same chip. With differential LOs, the net coupling to the antenna can approach acceptably low levels [2].

I/Q Mismatch — As mentioned earlier, for most currently used modulation schemes, a homodyne receiver must incorporate quadrature downconversion. This requires shifting either the RF signal or the LO output by 90°. Since phase-shifting the RF signal generally entails severe noise-power-gain trade-offs [2] and is especially difficult for the wideband signals used in high-data-rate systems, it is often desirable to shift the LO output (Fig. 7). In either case, the errors in the nominally 90° phase shift and mismatches between the amplitudes of the I and Q signal paths corrupt the downconverted signal constellation, thereby increasing the bit error rate. Note that all sections of the circuit in the I and Q paths contribute to gain and phase mismatches.

To gain more insight into the effect of I/Q mismatch, and show the versatility and convenience of using complex formulation, consider the practical case where the quadrature LO generates the complex signal $x_{LO}(t) = \cos(\omega_{LO}t) - j(1+\varepsilon)\sin(\omega_{LO}t + \theta)$. Here, ε and θ represent LO gain and phase errors. One can rewrite the quadrature LO output as

$$x_{LO}(t) = \frac{1}{2}\left[1-(1+\varepsilon)e^{j\theta}\right]e^{j\omega_{LO}t} + \frac{1}{2}\left[1+(1+\varepsilon)e^{-j\theta}\right]e^{-j\omega_{LO}t}.$$

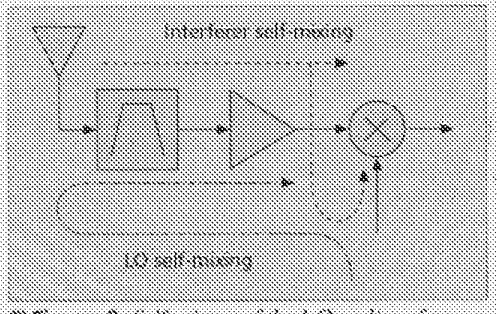


Figure 8. *Self-mixing of the LO and/or of an interferer in homodyne receiver front-end.*

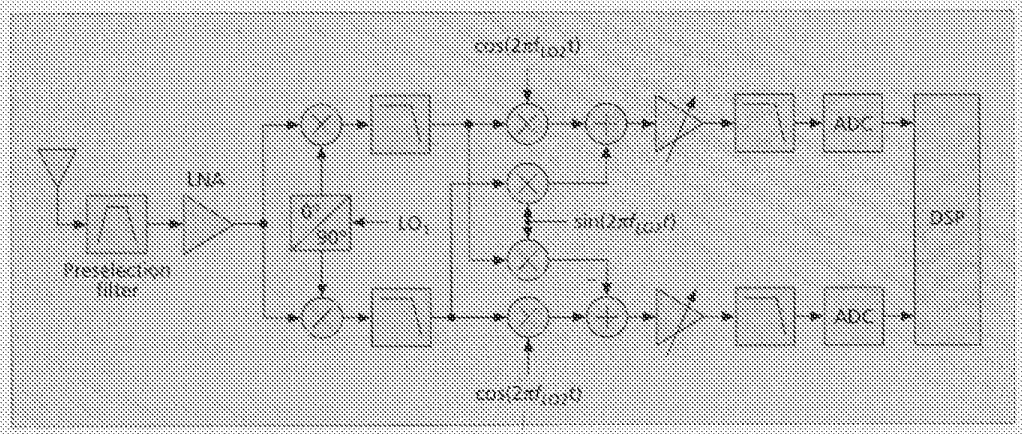


Figure 9. *A double-conversion wideband IF receiver.*

Aside from the problems mentioned here, direct-conversion receivers are sensitive to even-order distortions. Also, since the downconverted spectrum is located around zero frequency, the flicker noise of the devices has a profound effect on the SNR, a severe problem in CMOS implementations.

Ideally, the complex LO output should contain only the negative frequency. However, from the above expression it is apparent that, due to gain and phase errors, there is a positive frequency component with a magnitude of $|1 - (1 + \varepsilon)e^{j\theta}|/2$. This component causes interfering images and, if not compensated for, can deteriorate receiver performance. One can consider the effects of gain and phase mismatches separately. The magnitude of the undesired positive frequency component for gain mismatch is $|\varepsilon|/2$, and for phase mismatch $|\sin(\theta/2)|$, which can be approximated by $|\theta|/2$ when the phase mismatch is small.

Aside from the problems mentioned above, direct-conversion receivers are sensitive to even-order distortions. Also, since the downconverted spectrum is located around zero frequency, the flicker ($1/f$) noise of the devices has a profound effect on the SNR, a severe problem in CMOS implementations [2]. Furthermore, integrating the high-frequency low-phase-noise channel-select frequency synthesizer is difficult to achieve with low-Q VCOs available on integrated circuits [3].

Despite all these problems, direct-conversion transceivers for digital mobile phones using silicon bipolar technology have been in full production at Alcatel since 1991 [8]. The same company recently introduced a direct-conversion transceiver in a silicon germanium BiCMOS process [9] for the Global System for Mobile Communications (GSM) group of standards. In these transceivers, in order to handle the problems associated with static and dynamic dc offsets, DSP algorithms are used. These algorithms rely on the constant-envelope property of the modulation scheme used in GSM. To the best of the authors' knowledge, direct-conversion transceivers have not been used commercially in systems with nonconstant envelope modulation schemes, which are required in high-data-rate communication systems.

Wideband IF with Double-Conversion Receiver Architecture

This alternative architecture [3, 10], well suited to full integration, is shown in Fig. 9. In this receiver, after preselection filtering and amplification, all potential RF channels are complex-mixed and downconverted to IF. As discussed previously related to Fig. 2, there is no image problem. A second complex mixing is done from IF to baseband, using a tunable channel-select frequency-synthesizer. In this complex mixer, by properly adding the outputs of the real multipliers in pairs, the image frequencies are canceled while the desired channels add constructively. If the IF is chosen high enough, additional image rejection may be obtained from the RF front-end preselection filter [3].

Comparing the two integrated solutions discussed so far, in both architectures channel selection is performed at baseband, allowing the possibility of a programmable integrated channel-select filter for multistandard receiver applications. However, the wideband IF architecture has some advantages over the homodyne counterpart, which will now be discussed. Due to the fact that channel tuning is performed not using the first (RF) synthesizer but the lower-frequency (IF) LO, the RF LO can be implemented as a fixed-frequency crystal-controlled oscillator. Several techniques may be utilized to realize a low-phase-noise fixed LO with low-Q on-chip components [3]. Also, since tuning is performed with the IF LO operating at a lower frequency, the phase-noise performance of this oscillator can be significantly better than that of the tunable RF oscillator employed in a homodyne receiver. Furthermore, since in the wideband IF system there is no LO operating at the same frequency as the incoming RF carrier, the potential problems associated with LO leakage and time-varying dc offsets are minimized. Although in the wideband IF system the second LO is at the same frequency as the desired IF channel, the dc offset which results at the baseband from self-mixing is relatively constant and may be cancelled using adaptive signal processing methods [3].

The particular IR mixer used in this architecture, which is similar to the Weaver technique [11], has several advantages. First, lossy passive phase-shifting filters are not required in the signal path to generate the correct phase shift between the image and desired bands. Second, assuming again that the upconverted terms are removed, the image-rejection is very

As in wideband IF systems, if one employs two quadrature downconversion paths in a heterodyne receiver, then all of the required information for the separation of the wanted signal from unwanted signals, such as images, is available in the two IF signals.

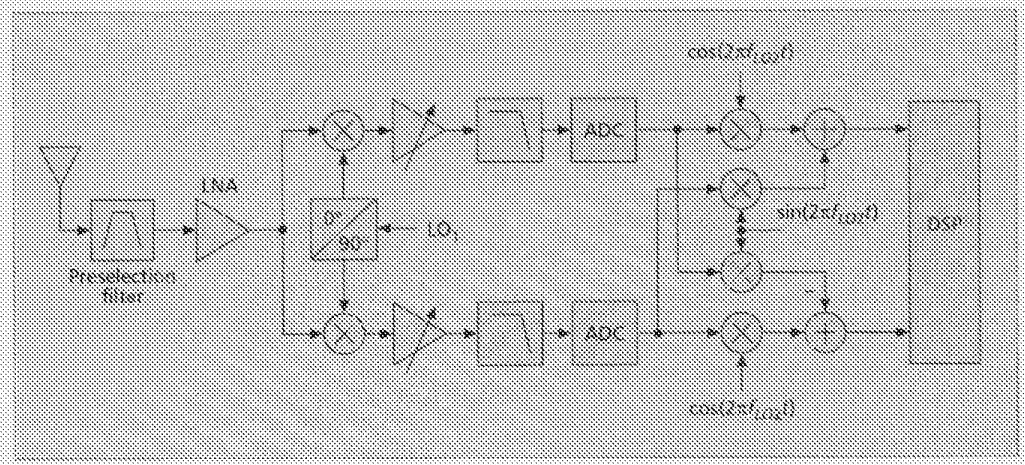


Figure 10. *A low-IF receiver.*

wideband. Also, it can be shown that the edge of the image attenuation band is set by the frequency of the first LO, which leads to the third advantage. If it is assumed that a multistandard-capable receiver is built where the frequency of the first LO can perform a course adjustment to accommodate the carrier frequency of a different standard, the image rejection will follow the first LO, and it can be thought of as a self-aligning IR mixer [3]. Note that the structure of this IR mixer (consisting of four multipliers and two adders) is the same as that of the complex mixer of Fig. 3. A detailed analysis of this IR mixer based on complex signal theory is given in [3].

The limitations of wideband IF receivers are as follows. Since the first LO is fixed in frequency, all channels must pass through the IF stage (the desired channel is selected using a second LO). This has two problematic implications: first, as a result of moving the channel selection to a lower frequency, the IF synthesizer requires a VCO with the capability of tuning across a broader frequency range as a percentage of the nominal operating frequency; second, by removing the channel-select filter at IF, strong adjacent channel interferers are now a concern for the second mixer stage as well as the baseband blocks. This implies a higher dynamic range requirement for these latter receiver stages. Also, as with conventional IR mixers, any I/Q phase and gain mismatch would degrade the performance of the receiver [3].

Low-IF Receiver Architecture

The idea behind low-IF topologies is similar to that of double-conversion wideband IF, and the goal is to combine the advantages of both heterodyne and homodyne receivers [12]. As in wideband IF systems, if one employs two quadrature downconversion paths in a heterodyne receiver, all of the required information for the separation of the wanted signal from unwanted signals, such as images, is available in the two IF signals.

Among the different low-IF topologies mentioned in [5, 10, 12], a preferred version is shown in Fig. 10. This architecture is fairly similar to that of the wideband IF architecture, although there are several subtle differences between the two. First is the choice of IF. While the IF in the wideband IF architecture is typically high, in the low-IF system the IF is chosen as low as one or two times the channel bandwidth. Note that this alleviates the dc offset problem in these two architectures compared to their homodyne counterparts, simply because after the first downconversion the wanted signal is not located around dc. Second, in the low-IF topology it is more feasible to sample the low-IF signal after the first mixer stage with a high resolution analog-to-digital convertor (ADC). Sampling at this point requires an ADC with higher resolution than that required after the IR mixer in wideband IF receivers, because in the former case the wanted signal and unwanted image are sampled. After the first mixer stage, the unwanted image can be much larger than the desired signal.

Although the low-IF architecture requires higher-performance ADCs than does the wideband IF architecture, the signal path to the ADC can be ac-coupled in the low-IF architecture, which in turn eliminates the need for complicated dc offset cancellation circuitry. *Another advantage of this low-IF topology is that part of the complex IR mixer is implemented in the digital domain with no gain and phase I/Q mismatches.* The I/Q imbalances introduced in the preceding analog sections can be corrected using adaptive techniques [13]. Therefore, this strategy shifts the hard specifications from the analog part to the ADCs. Since the performance of integrated ADCs is improving rapidly, this architecture will likely be preferred [12].

Finally, it should be noted that digitizing the received signal at the IF stage can also be employed in conventional heterodyne receiver systems. This approach is sometimes called *digital IF* [7]. In this architecture, the high ADC performance requirements are more challenging to accomplish within a reasonable power dissipation. Despite the advantage of avoiding the I and Q mismatches for typical first IFs in heterodyne receivers, this technique requires a prohibitively fast high-linearity high-dynamic-range ADC, currently limiting its utilization to only base stations [7].

Conclusion

In this tutorial, traditional and recent wireless receiver architectures suitable for a single-chip transceiver are reviewed. To simplify analysis of these architectures and gain more insight into their structures, complex signal representation is used. The advantages and disadvantages of each architecture are discussed with emphasis on practical considerations.

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Low-IF Topologies for High-Performance Analog Front Ends of Fully Integrated Receivers

Jan Crols and Michiel S. J. Steyaert, *Senior Member, IEEE*

***Abstract*— When it comes to integratability, the zero-intermediate frequency (IF) receiver is an alternative for the heterodyne or IF receiver. In recent years, the zero-IF receiver has been introduced in several applications, but its performance cannot be compared to that of the IF receiver yet. This lower performance is closely related to its baseband operation, resulting in filter saturation and distortion, both caused by DC-offsets and self-mixing at the inputs of the mixers. The low-IF receiver has a topology which is closely related to the zero-IF receiver, but it does not operate in the baseband, only *near* the baseband. The consequences are that, as for the zero-IF receiver, the implementation of a low-IF receiver can be done with a high degree of integration, however, its performance can be better. In this paper, the fundamental principles of the low-IF receiver topology are introduced. Different low-IF receiver topologies are synthesized and fully analyzed in this paper. This is done by applying the complex signal technique—a technique used in digital applications to the study of analog receiver front ends.**

I. Introduction

THIS PAPER deals with the design of receivers for telecommunication systems in which phase or frequency modulation is used. It is investigated how these receivers can be realized in a highly integrated way and still show a good quality of signal reception. This is not trivial. Today, most receivers work with an intermediate frequency (IF), and a lot of their components still need to be discrete. Alternative topologies, mainly the zero-IF topologies, can be realized highly integrated, but they tend to have a significantly poorer performance than the discrete realizations.

A typical receiver consist of two important parts which perform its main operations: the downconversion and the demodulation part. In the downconversion part, the wanted signal is filtered and separated from its neighbors, and it is converted from its carrier frequency to a frequency more suited for the demodulator. Due to the high-performance specifications which are required from the downconverter, its implementation is always fully analog. The demodulation is done on a lower frequency. In more and more applications, this demodulation is done in a digital signal processor (DSP). A DSP allows for the use of complicated modulation schemes and complex demodulation algorithm. The result is an overall quality improvement and a high degree of integration. In this paper, only the design of the analog downconversion part of the receiver is discussed. It will be presumed that the demodulation is preferably done with a DSP at baseband. The design of a downconverter will be discussed accordingly.

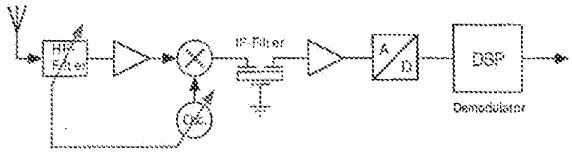


Fig. 1. Schematic representation of the IF receiver topology.

There are two main types of receivers used in telecommunication systems based on phase or frequency modulation: the heterodyne and the homodyne receiver. The difference between them is in whether or not an IF is used. This has great implications on their topology, possibilities, and performance. Heterodyne and homodyne receivers are often called IF and zero-IF receivers, respectively. In this paper, the latter term will be used.

The main advantage of a zero-IF receiver over an IF receiver is the very high integration level that can be achieved. Although full integration is very important for cost reduction, the use of zero-IF receivers was very limited in the past due to the poor performance compared to IF receivers. It is only nowadays that one begins to use zero-IF receivers in systems based on digital communications. In these systems, a lower performance can be accepted in exchange for the higher degree of integration and the ease with which a zero-IF receiver can be combined with a DSP for the baseband demodulation of the digital signal. The recently introduced new wireless digital telecommunication services, like GSM and DECT, are examples of such systems [1], [2].

In this paper, all the advantages and disadvantages concerning integratability and performance of IF and zero-IF receivers are discussed. Starting from the discussion of these two topologies, new receiver topologies, based on the use of a low IF, situated at a few hundred kilohertz, are introduced. It is shown how the advantages of IF and zero-IF, a high performance and a high degree of integration, can be combined. For this purpose, the complex signal technique is introduced to this field of analog circuit design. The complex signal principle brings a higher level of abstraction to, and therefore a clearer insight into, the analysis of multipath signal processing systems. The performance of multipath systems relies, however, on a very good matching, which can only be perfect in digital systems. This paper demonstrates how the complex signal analysis technique can be used to get a better

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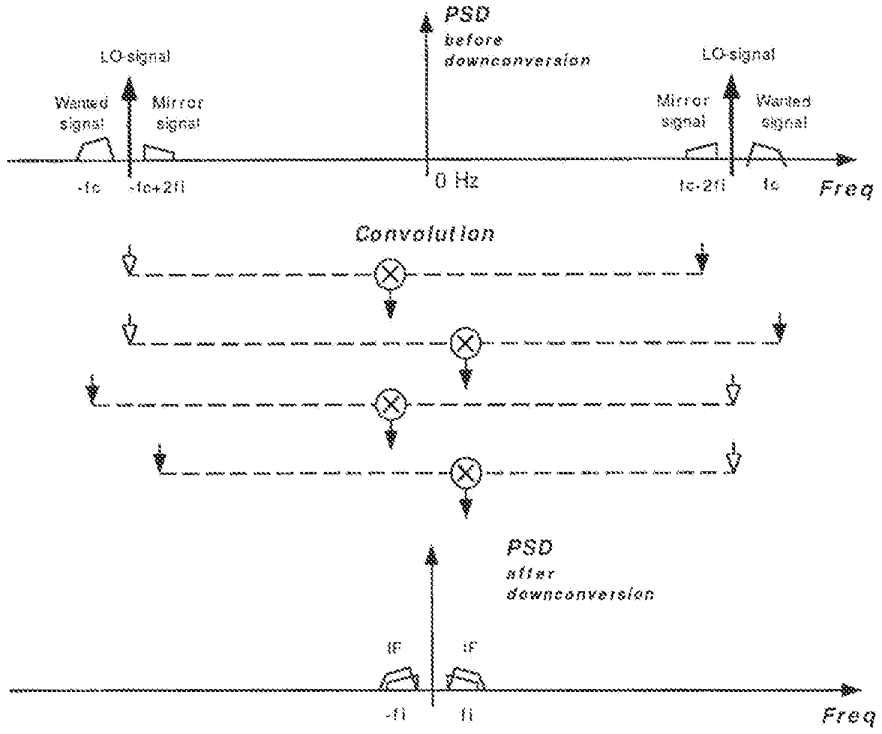


Fig. 2. The downconversion scheme in an IF receiver.

insight into the effect of mismatch in analog multipath signal processing circuits such as zero- and low-IF receivers.

II. Integrated Receivers

A. IF Receivers

IF receivers have been in use for a long time, and their way of operating is very well known [3]. In Fig. 1, the schematic representation of the IF receiver topology is given. The wanted signal is downconverted from its carrier to the IF by multiplying it with a single sinusoidal signal. It can be demodulated on this intermediate frequency or it can be further downconverted after filtering. The main disadvantage here is that apart from the wanted signal, an unwanted signal (called the mirror frequency) is downconverted to the IF. This is illustrated in Fig. 2. When the wanted signal is situated on f_c, the mirror frequency is at $f_c - 2f_i$. This is illustrated with (1). The mixer gives a frequency component on f_i for $f_x = f_c$ and $f_x = f_c - 2f_i$. The antenna signal $a(t)$ is in this case a phase modulated signal and equal to $\cos[2\pi f_x t + m(t) + \phi]$.

$$\begin{aligned} a(t) \times \sin[2\pi(f_c - f_i)t + \varphi] &= \cos[2\pi f_x + m(t) + \phi] \times \sin[2\pi(f_c - f_i)t + \varphi] \\ &= \tfrac{1}{2}\{\sin[2\pi(f_x + f_c - f_i)t + m(t) + \phi + \varphi] \\ &\quad - \sin[2\pi(f_x - f_c + f_i)t + m(t) + \phi - \varphi]\}. \end{aligned} \tag{1}$$

The mirror frequency has to be suppressed before it is mixed down to the IF. This is done by means of a high-frequency (HF) filter. Such an HF filter can only be realized if f_i is high enough because the wanted signal (on f_c) must be relatively far away from the mirror frequency. Even when the ratio f_c/f_i is as small as 10, the specifications for the HF filter are very severe. The HF filter must have a very high Q (up to 50 and more), and it must have an order which is high enough (up to sixth order for high-quality applications, i.e., 60–70-dB mirror frequency suppression); and in some cases, the center frequency must be tunable. A filter with these specifications cannot be integrated. These filters are realized with discrete components. They consist of capacitors and inductors which have to be tuned during production. The tunability of the center frequency is realized by means of a discrete varicap diode. These HF filters are expensive and vulnerable.

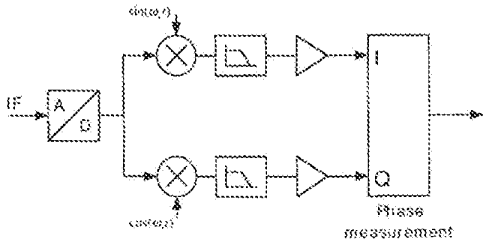


Fig. 3. Demodulation with a DSP of a signal situated on an IF.

Once the signal is downconverted to the IF, it has to be filtered further on in order to extract the wanted signal from its neighbors. This filter too must have a high Q (e.g., 50) and a high order (eighth or tenth order). Integrating these IF filters is also very hard. Although ever more analog integrated IF filters are published [4], [5], for most applications they are still not good enough, and ceramic resonators are still used instead. In [6]–[8], it is shown that the performance (i.e., achievable dynamic range over power consumption) of integrated active bandpass filters is intrinsically Q-times worse than the perfor-

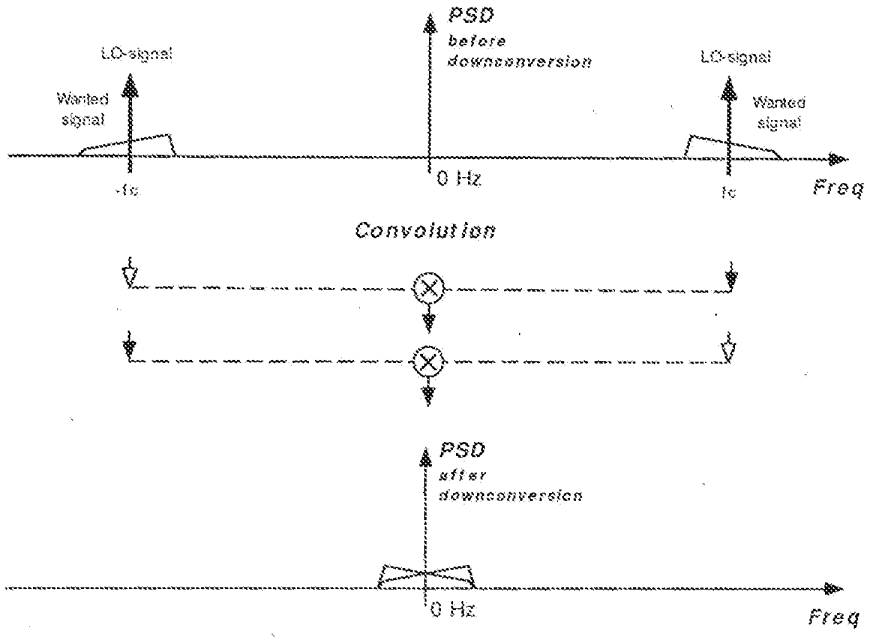


Fig. 4. Direct downconversion by mixing the RF signal with a single sine.

mance of a passive bandpass filter. This means that the discrete passive bandpass filters will always be a lot better than an active integrated version if one is concerned with power and area efficiency. The problem is that, compared to integrated filters, the use of these discrete components is very expensive.

Fig. 3 shows schematically how demodulation can be done with a DSP in an IF receiver. The IF signal is sampled and then downconverted in quadrature. Further demodulation is the same as in zero-IF receivers. The difference is that digitally the quadrature signal can be generated with a very high precision. Often the IF is too high for the A/D-converter, and then one or more extra IF stages are used. The final IF is often situated around 1 MHz [9].

B. Zero-IF Receivers

In zero-IF receivers, the wanted signal is directly downconverted to the baseband. The IF is chosen to be zero. In this case, the signal on the mirror frequency is the wanted signal itself. However, this does not eliminate the problem of the mirror frequency. Both signals—the wanted signal and the signal from the mirror frequency—although they are coming from the same carrier frequency, are not the same. In this case, they are each other's mirror image. Fig. 4 shows that this results in the lower and upper sideband being placed on top of each other in the baseband, which means that they become inseparable.

This problem is solved by doing the downconversion twice—once with a sine and once with a cosine. The topology of a zero-IF receiver is given in Fig. 5. In (2) and (3), the quadrature downconversion of the antenna signal $a(t)$ is calculated.

$$u_i(t) = a(t) \times \cos(2\pi f_c t + \varphi)$$
$$u_q(t) = a(t) \times \sin(2\pi f_c t + \varphi). \tag{2}$$

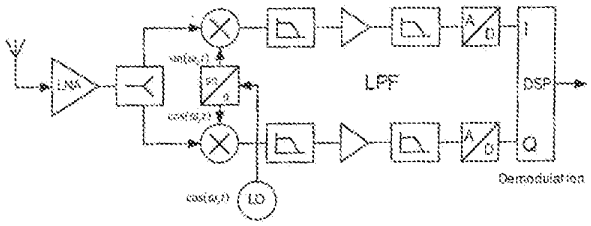


Fig. 5. The zero-IF receiver topology.

The original signal $m(t)$ can, in case of phase modulation, be found as the angle of the vector $[u_i(t), u_q(t)]$, a low-pass filtered version of $[u_i(t), u_q(t)]$.

$$m(t) = \arctan\left[\frac{v_q(t)}{v_i(t)}\right] + \varphi - \phi. \tag{3}$$

The demodulation in a DSP can be done by means of an angle measurement algorithm. The CORDIC algorithm is an example of such an algorithm [10].

The advantages of zero-IF receivers are obvious. There is no need for a high-Q tunable bandpass filter. In most designs, a broadband HF filter which requires no tuning or adjusting is used to reduce the dynamic range requirements for the downconversion part and prevent mixing of the RF signal with harmonic components of the LO signal. The low-pass filters can easily be realized as analog integrated filters.

The precision with which both demodulation paths (I and Q) can be matched determines how good the mirrored signal can be suppressed. The specifications on mirror suppression are not as severe for a zero-IF receiver as they are for an IF receiver. In an IF receiver, extra suppression is needed because the signal on the mirror frequency can be bigger than the wanted signal. However, a suppression of 40 dB is still needed in a good quality zero-IF receiver. The zero-IF receiver

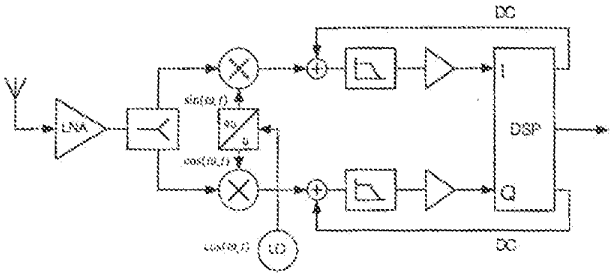


Fig. 6. A zero-IF receiver with a DC compensation feedback path.

is thus very sensitive to matching and to phase and amplitude errors in the quadrature oscillator.

Another problem in zero-IF receivers is the DC-offset which is created during the downconversion. It is mainly a result of the crosstalk between the RF and LO inputs of the mixer. The multiplication of the LO signal with itself gives a DC (or almost DC) signal. This DC-offset is superimposed on the wanted signal in the baseband. It can only be removed be means of very long time constants (at least one-tenth of a second), and it always results in the loss of a part of the wanted signal. This has an effect that is comparable to distortion [11]. The distortion will be lower and of an acceptable level if the time constant is longer (e.g., 1 s), but this long time constant makes the settling time of the complete receiver system too long, and these time constants cannot be analog integrated. For instance, at each change of the carrier frequency, the receiver would have to settle for at least 1 s when a highpass filter of 1 Hz is used. The principle of zero-IF receivers has been known for years. However, it is the DC-offset problem that has kept the zero-IF receiver from use in practical applications. It is only with the introduction of DSP's that this problem has become controllable for system with lower quality specifications (i.e., based on digital signals) [12]. In the DSP a complex nonlinear scheme can be used to determine the DC-level dynamically. This value can then be fed back into the analog part. This is shown in Fig. 6. In this way, saturation of the low-pass filters is prevented and the distortion is kept acceptable.

The crosstalk between LO and RF not only results in a DC voltage; the multiplication of the RF signal with itself results in a broadband baseband signal (twice the bandwidth of the RF signal). A considerable part of the power of this signal is situated in the lower baseband. This is an unwanted effect because this means that this signal is also superimposed on the wanted baseband signal; and once this is done, they cannot be separated anymore.

C. Low-IF Receivers

The development of the low-IF topologies starts from the perception that it must be possible to realize a receiver which combines the advantages of both known receiver types. If one would use two downconversion paths in an IF receiver, all required information for the separation of the wanted signal from the mirror signal would still be available in the two IF signals, as it is in a zero-IF receiver. So in this way it must be possible to postpone the mirror suppression from the HF part to the IF part. A high-quality HF filter would not be necessary anymore. A broadband HF filter, the same as for zero-IF receivers, would be satisfactory. The high IF, necessary to make the HF filter realizable, can now be replaced by a low IF (e.g., one or two times the bandwidth of the wanted signal) and the IF filter becomes now a set of two low Q ($Q = 1$ or 2) bandpass filters whose integration is as easy as the integration of the low-pass filters for a zero-IF receiver.

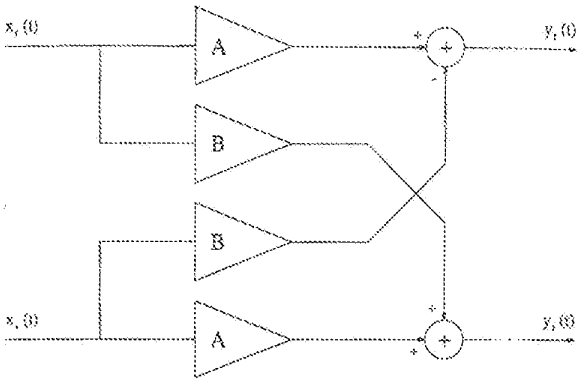


Fig. 7. Block scheme of the amplification of a complex signal with a complex constant.

Although the concept of the low-IF receiver has been proposed in the previous paragraph, it is still not clear how such a receiver can be realized. First, it must be determined how the information available in both IF signals can be used to separate the wanted signal from the mirror signal. Therefore, in the next section of this paper, the complex signal technique is introduced. This is an analysis and synthesis technique which is used in different fields of digital signal processing [13], [14]. Its key concept is the use of multipath signal processing systems which are analyzed as single path systems. The quality of this multipath signal processing depends heavily on how well the operations in each path are matched with each other. In digital systems, this matching can be perfect; in analog systems, a perfect matching is impossible. In this paper, the complex signal technique will be used to analyze the analog zero-IF topology—an obvious multipath system. The limitations of analog integrated systems which use complex signals will be analyzed; and starting from this discussion, the low-IF receiver topologies will be synthesized. A low-IF receiver can be highly integrated and exhibit high performance at the same time.

III. Systems with Complex Signals

A. Polyphase and Complex Signals

A polyphase signal is, by definition, a vector of independent signals. In an n-phase system, these vectors are n-dimensional.

$$u(t) = [u_1(t), u_2(t), \cdots, u_n(t)]$$
$$U(j\omega) = [U_1(j\omega), U_2(j\omega), \cdots, U_n(j\omega)]. \quad (4)$$

These polyphase signals can take any form, and they are therefore not very special. It becomes interesting when they are described as a sum of sequences on which operations

are defined which have sequence specific responses. In the following equations, this is worked out for the special case of two-phase signals. The notation is different from (4). Here the complex notation is used for the two-dimensional vectors and from now on two-phase signals are called complex signals. The j makes sure that the r and i component can be independent components of $u(t)$, and in this way the complex signal, which appears to be one signal, is two-dimensional.

$$u(t) = u_r(t) + ju_i(t)$$
$$U(j\omega) = U_r(j\omega) + jU_i(j\omega). \tag{5}$$

Every frequency component of $u(t)$ can be written as a sum of two sequences. The two sequences of a real signal $[u(t) = u_r(t)]$ always have the same amplitude and the opposite phase.

$$\begin{aligned} &A(\omega)\cdot\cos[\omega t + \varphi(\omega)] \\ &\quad = \frac{A(\omega)}{2}\cdot\{\cos[\omega t + \varphi(\omega)] + j\cdot\sin[\omega t + \varphi(\omega)]\} \\ &\qquad + \frac{A(\omega)}{2}\cdot\{\cos[\omega t + \varphi(\omega)] - j\cdot\sin[\omega t + \varphi(\omega)]\}. \end{aligned} \tag{6}$$

The first sequence has only a positive frequency component, the second only a negative.

$$\begin{aligned} &A(\omega)\cdot\{\cos[\omega t + \varphi(\omega)] + j\cdot\sin[\omega t + \varphi(\omega)]\} \\ &\quad = A(\omega)\cdot e^{j\varphi(\omega)}\cdot e^{j\omega t} \\ &A(\omega)\cdot\{\cos[\omega t + \varphi(\omega)] - j\cdot\sin[\omega t + \varphi(\omega)]\} \\ &\quad = A(\omega)\cdot e^{-j\varphi(\omega)}\cdot e^{-j\omega t}. \end{aligned} \tag{7}$$

In this way, any complex signal, i.e., any ordered set of two independent signals, can be represented as a sum of positive and negative frequency components which in turn are also totally independent. Making a difference between positive and negative frequencies becomes an advantage if one can realize operators which make a difference between positive and negative frequency components.

B. Operations on Complex Signals

The use of complex signals becomes interesting once there are some specific operations defined on them which can be realized in an analog integrated way. The sum of two complex signals is a first and trivial operations. Each component of the sum signal is equal to the sum of the respective components of the signals that are summed. This does of course also mean that frequency components are not transformed to new positions by this operation.

$$\begin{aligned} z(t) = x(t) + y(t) &= [x_r(t) + jx_i(t)] + [y_r(t) + jy_i(t)] \\ &= [x_r(t) + y_r(t)] + j\cdot[x_i(t) + y_i(t)]. \end{aligned} \tag{8}$$

The complex multiplication, defined by $j^2 = -1$, introduces some more interesting operations. The multiplication of a complex signal with a complex constant is not interesting as such. It is, however, a useful building in the synthesis of complex filters.

$$\begin{aligned} y(t) = Z\cdot x(t) &= (Z_r + jZ_i)\cdot[x_r(t) + jx_i(t)] \\ &= [Z_r\cdot x_r(t) - Z_i\cdot x_i(t)] + j[Z_r\cdot x_i(t) + Z_i\cdot x_r(t)]. \end{aligned} \tag{9}$$

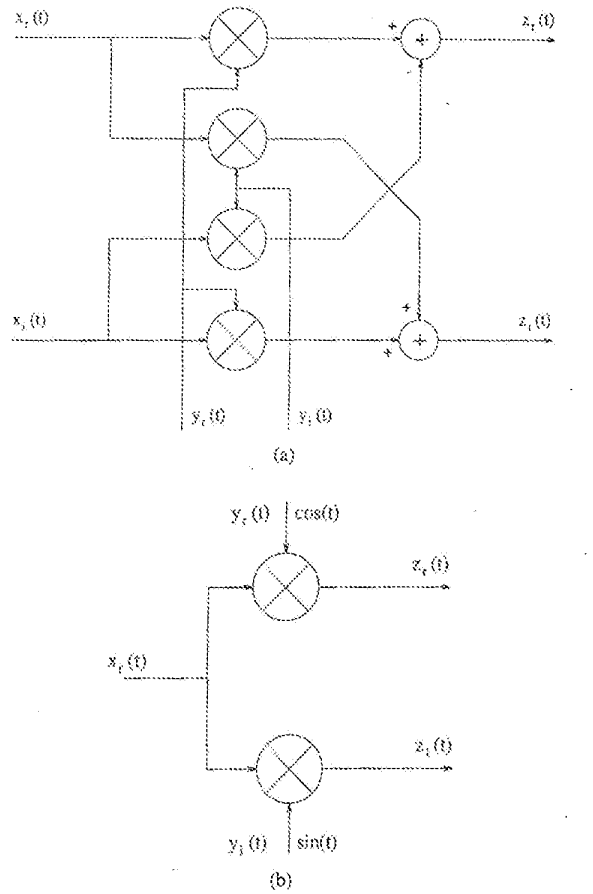


Fig. 8. (a) The multiplication of a complex signal with a complex signal. (b) The special case of the multiplication of a real signal with a complex signal.

Fig. 7 shows how this operation can be realized (with $Z = A + jB$). It is nothing more than the direct implementation of (9). The multiplication of two complex signals is a very important operation in receiver design.

$$\begin{aligned} z(t) = y(t)\cdot x(t) &= [y_r(t) + jy_i(t)]\cdot[x_r(t) + jx_i(t)] \\ &= [y_r(t)\cdot x_r(t) - y_i(t)\cdot x_i(t)] \\ &\quad + j[y_r(t)\cdot x_i(t) + y_i(t)\cdot x_r(t)] \end{aligned} \tag{10}$$

$$\begin{aligned} Z(j\omega) &= Y(j\omega)\otimes X(j\omega) \\ &= [Y_r(j\omega) + jY_i(j\omega)]\otimes[X_r(j\omega) + jX_i(j\omega)] \\ &= [Y_r(j\omega)\otimes X_r(j\omega) - Y_i(j\omega)\otimes X_i(j\omega)] \\ &\quad + j[Y_r(j\omega)\otimes X_i(j\omega) + Y_i(j\omega)\otimes X_r(j\omega)]. \end{aligned} \tag{11}$$

The realization follows again from the worked out equations and is shown in Fig. 8(a). With this complex mixer it is possible to do a downconversion with only a positive or negative frequency. A sine has both, and this leads to the problem of the mirror frequency. The wanted signal is downconverted with the positive frequency component, and the mirror signal is downconverted with the negative frequency component. A special case is the downconversion of a real signal with a positive frequency. The scheme of Fig. 8(a) is reduced to

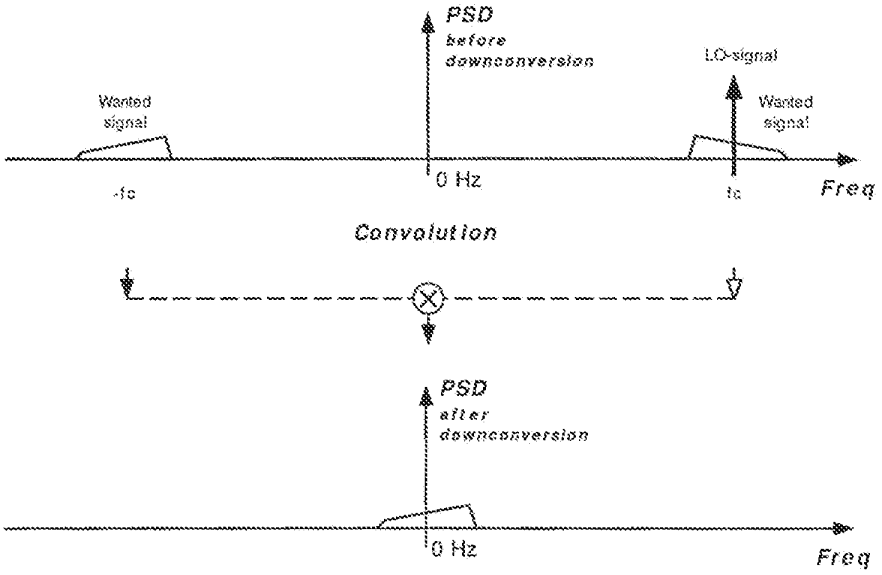


Fig. 9. Downconversion in a zero-IF receiver: mixing with a positive frequency.

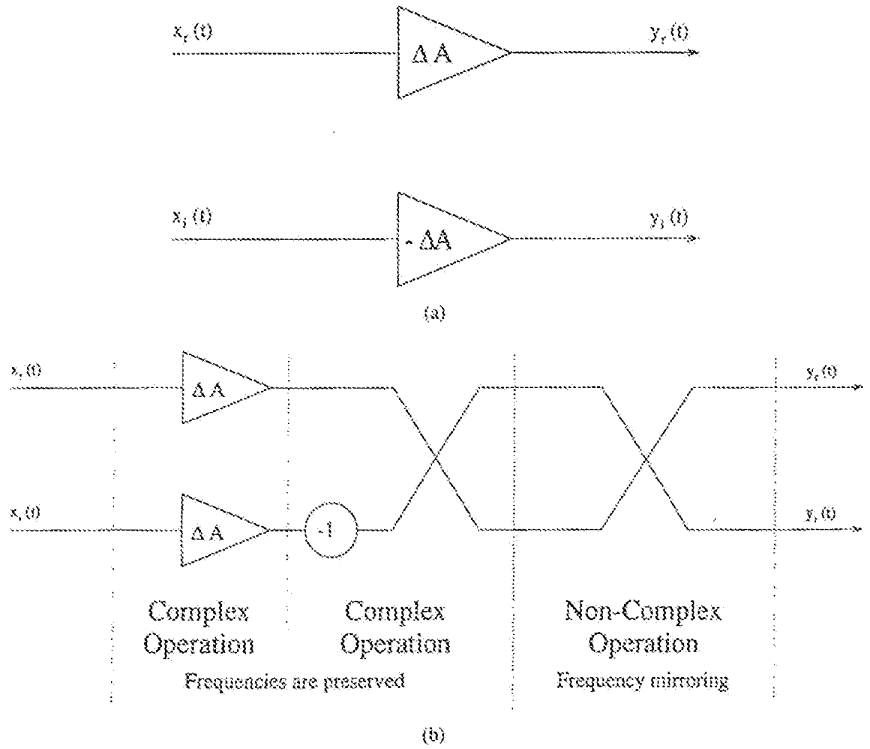


Fig. 10. (a) Mismatch between the amplification in the real and imaginary path. (b) Equivalent scheme.

Fig. 8(b), and it is obvious that this is the mixer which is used in zero-IF receivers. Fig. 9 shows the downconversion of a real signal with a single positive frequency—the downconversion which is used in a zero-IF receiver. Only the signal situated on the negative frequencies is downconverted, and in this way there is no superposition of the lower and upper sideband at baseband.

The most important operation on complex signals is filtering. A complex filter has a transfer characteristic in function of frequency which is sequence dependent. This means that the filtering of positive frequencies is different from the filtering of negative frequencies. Some positive frequencies may be passed, while the same negative frequencies are suppressed. This effect is very handy in receiver design, especially in those cases where the mirror signal is situated on the opposite frequencies of the wanted signal. Once the required transfer function is known, the filter can again be realized from the worked-out equation. The topology is the same as the one of

Fig. 7. In this case, the amplifiers are frequency dependent.

$$\begin{aligned} Y(j\omega) &= H(j\omega)\cdot X(j\omega) \\ &= [H_r(j\omega)+jH_i(j\omega)]\cdot[X_r(j\omega)+jX_i(j\omega)] \\ &= [H_r(j\omega)\cdot X_r(j\omega)-H_i(j\omega)\cdot X_i(j\omega)] \\ &\quad + j[H_r(j\omega)\cdot X_i(j\omega)+H_i(j\omega)\cdot X_r(j\omega)]. \end{aligned} \tag{12}$$

This synthesis technique—the realization of a complex filter with real filters—is, however, very costly. The realization of a first-order filter with a complex pole, for instance, requires the use of four real second-order filters. Direct synthesis is a more appropriate realization method. Direct synthesis is the realization of the complex transfer function with complex summators, amplifiers, and integrators. In the next section of this text, this will be worked out, and the implications of a practical realization will be discussed.

C. Imperfections in Complex Systems

Complex operators are made with pairs of real operators, amplifiers, mixers, and filters. The performance of the system in which these complex operators are used degrades when they are not perfectly matched. In digital systems, matching can be perfect; in analog integrated implementations, mismatch is unavoidable. An example of the effect of mismatch is given in Fig. 10. The amplification of a complex signal with a real constant A normally does not change the frequency distribution of the signal. The mismatched amplification of Fig. 10(a) can, for analysis purposes, be splitted in three different operations: a perfectly matched amplification, a complex multiplication with $-j$, and a switching of the real and imaginary part of the complex signal. This is depicted in Fig. 10(b). The first two operations are complex operations which preserve the frequency distribution. The third operation—the switching of the real and imaginary part—is not a linear operation which preserves the frequencies. Switching the vector components of a complex signal is equal to reversing the vector sequences. A positive sequence becomes a negative sequence and vice versa. In (13) this is written down for a positive and a negative frequency:

$$\begin{aligned} x_r(t)+j\cdot x_i(t) &\rightarrow x_i(t)+j\cdot x_r(t) \\ e^{j\omega_c t} &= \cos(\omega_c t)+j\cdot\sin(\omega_c t) \rightarrow \sin(\omega_c t)+j\cdot\cos(\omega_c t) \\ &= j\cdot e^{-j\omega_c t} \\ e^{-j\omega_c t} &= \cos(\omega_c t)-j\cdot\sin(\omega_c t) \rightarrow \sin(\omega_c t)-j\cdot\cos(\omega_c t) \\ &= -j\cdot e^{j\omega_c t}. \end{aligned} \tag{13}$$

Using this operator for the example of Fig. 10, the total transfer function of the amplifier with mismatch can be calculated. An applied frequency component will be magnified with a factor A, but it will also be mirrored to its opposite frequency and magnified with a factor ΔA. The ratio between the unwanted mirrored signal and the wanted original signal is thus $\Delta A/A$. An amplitude error of 1% gives a −40-dB crosstalk between the positive and negative frequencies.

The result of a phase error between the two signal paths is also an unwanted mirroring of signals to their opposite frequencies. Equation (14) gives the effect of a phase error on a positive frequency component.

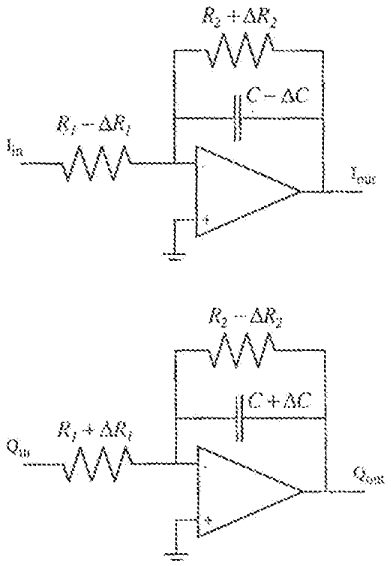


Fig. 11. Mismatch in a low-pass filter for complex signals.

$$\begin{aligned} e^{j\omega_c t} &= \cos(\omega_c t)+j\cdot\sin(\omega_c t) \\ &\rightarrow \cos(\omega_c t+\Delta\varphi)+j\cdot\sin(\omega_c t-\Delta\varphi) \\ &= \cos(\Delta\varphi)\cdot(e^{j\omega_c t}-j\cdot\tan(\Delta\varphi)\cdot e^{-j\omega_c t}). \end{aligned} \tag{14}$$

Apart from the wanted positive frequency, the total transfer function again generates also a negative and unwanted frequency component. The ratio between the unwanted and the wanted signal is $\tan(\Delta\varphi)$, which can be taken equal to $\Delta\varphi$ for small values of $\Delta\varphi$. This means that a phase error of 1° results in a −35-dB crosstalk between positive and negative frequencies.

The relationship between component matching and amplitude and phase errors is illustrated with an example. Fig. 11 gives the realization of an active-RC single pole low-pass filter for complex signals. All passive devices differ from their nominal values. There are three sources of unwanted frequency mirroring in this circuit. One is a constant amplitude error caused by the mismatch on R_1 and R_2. Equation (15) gives a calculation and approximation for this error.

$$\begin{aligned} \frac{\Delta A}{A} &= \left|\frac{A_r-A_i}{2A}\right| = \frac{\dfrac{R_2+\Delta R_2}{R_1-\Delta R_1}-\dfrac{R_2-\Delta R_2}{R_1+\Delta R_1}}{2\dfrac{R_2}{R_1}} \\ &= \frac{1}{2}\cdot\left(\frac{1+\Delta R_2/R_2}{1-\Delta R_1/R_1}-\frac{1-\Delta R_2/R_2}{1+\Delta R_1/R_1}\right) \\ &\approx \frac{1}{2}\cdot\left[\left(1+\frac{\Delta R_1}{R_1}\right)\cdot\left(1+\frac{\Delta R_2}{R_2}\right)\right. \\ &\quad \left.-\left(1-\frac{\Delta R_1}{R_1}\right)\cdot\left(1-\frac{\Delta R_2}{R_2}\right)\right] \\ &\approx [\text{for all } \omega]\ \frac{\Delta R_1}{R_1}+\frac{\Delta R_2}{R_2}. \end{aligned} \tag{15}$$

The other two sources of unwanted frequency mirroring are the frequency dependent amplitude and phase error caused by the

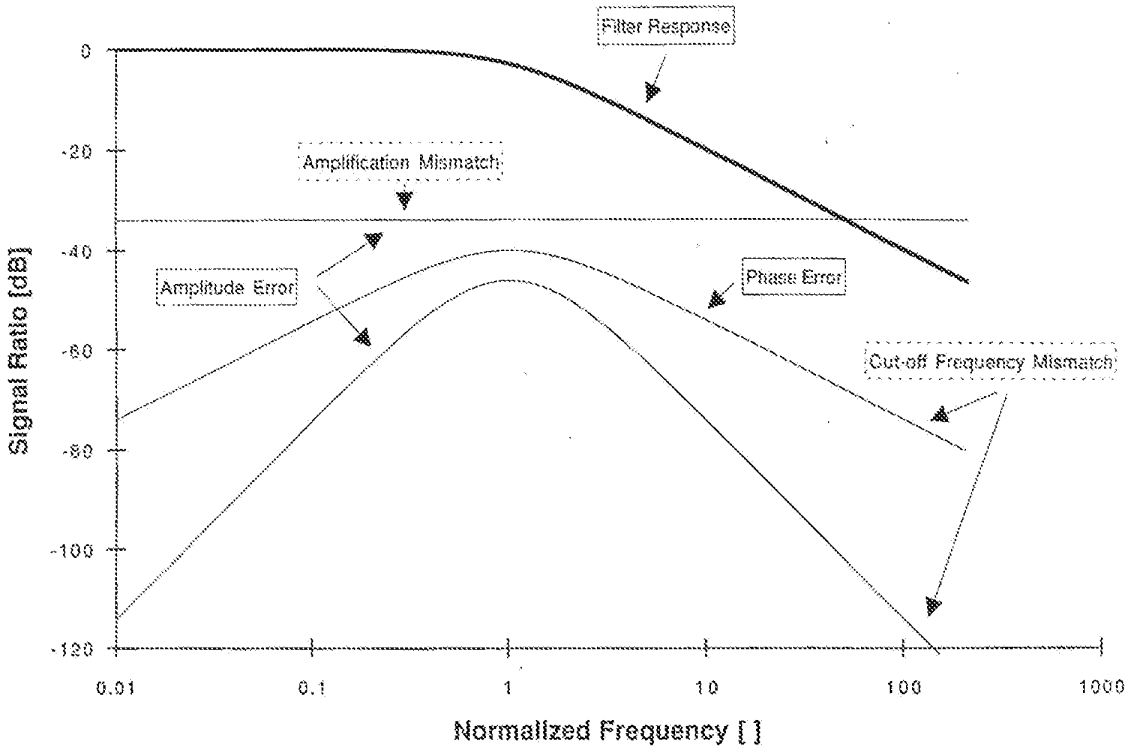


Fig. 12. Signal mirroring caused by mismatch in a low-pass filter for complex signals in function of frequency.

mismatch between the cutoff frequencies of the two low-pass filters. Equations (16) and (17) give these errors in function of frequency for a worst-case situation.

$$\begin{aligned}\tan(\Delta\varphi) &= \tan\left(\frac{\varphi_r-\varphi_i}{2}\right)\\ &= \tan\left\{\frac{1}{2}\cdot\arctan\left[\omega RC\cdot\left(1+\frac{\Delta R_2}{R_2}\right)\cdot\left(1+\frac{\Delta C}{C}\right)\right]-\frac{1}{2}\cdot\arctan\left[\omega RC\cdot\left(1-\frac{\Delta R_2}{R_2}\right)\cdot\left(1-\frac{\Delta C}{C}\right)\right]\right\}\\ &\approx[\text{for }\omega RC\text{ small}]\ \omega RC\cdot\left(\frac{\Delta R_2}{R_2}+\frac{\Delta C}{C}\right)\\ &\approx[\text{for}\omega RC=1]\left(\frac{\Delta R_2}{2R_2}+\frac{\Delta C}{2C}\right).\end{aligned}\tag{17}$$

These three sources of mirroring are plotted versus frequency in Fig. 12. The curves of Fig. 12 are given for a 1% mismatch on each component. For (15)–(17) and Fig. 12, the worst-case analysis technique has been used for the simplicity of the equations. An insight into the total mirror error of a circuit, its mean value, and its variation can be obtained by doing a Monte Carlo simulation. The conclusions that can be drawn from Fig. 12 are the following: amplitude errors caused by pole position mismatch are small (so, capacitor mismatch does not result in amplitude errors); phase errors are caused by resistor and capacitor mismatch (they occur, however, only at the edge of the passband); the amplification mismatch is the main cause of signal mirroring errors in the passband (it completely depends on resistor matching).

The mirror error component that is caused by amplification mismatch can be corrected with the use of two matched AGC's

$$\begin{aligned}\frac{\Delta A}{A} &= \frac{\sqrt{\dfrac{1}{1+(\omega RC)^2\cdot(1+\Delta R_2/R_2)^2\cdot(1+\Delta C/C)^2}}-\sqrt{\dfrac{1}{1+(\omega RC)^2\cdot(1+\Delta R_2/R_2)^2\cdot(1-\Delta R_2/R_2)^2\cdot(1-\Delta C/C)^2}}}{\sqrt{\dfrac{1}{1+(\omega RC)^2}}}\\ &\approx\frac{\sqrt{\dfrac{1}{1+(\omega RC)^2\cdot(1+2\Delta R_2/R_2+2\Delta C/C)}}-\sqrt{\dfrac{1}{1+(\omega RC)^2\cdot(1-2\Delta R_2/R_2-2\Delta C/C)}}}{\sqrt{\dfrac{1}{1+(\omega RC)^2}}}\\ &\approx[\text{for }\omega RC=1]\ \frac{\Delta R_1}{4R_1}+\frac{\Delta R_2}{4R_2}\end{aligned}\tag{16}$$

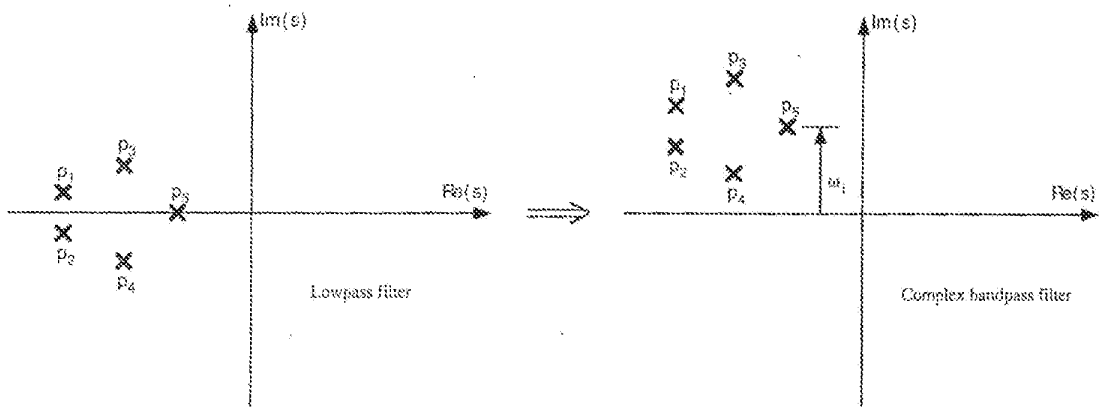


Fig. 13. S-plane representation of the frequency translation of a fifth-order low-pass filter.

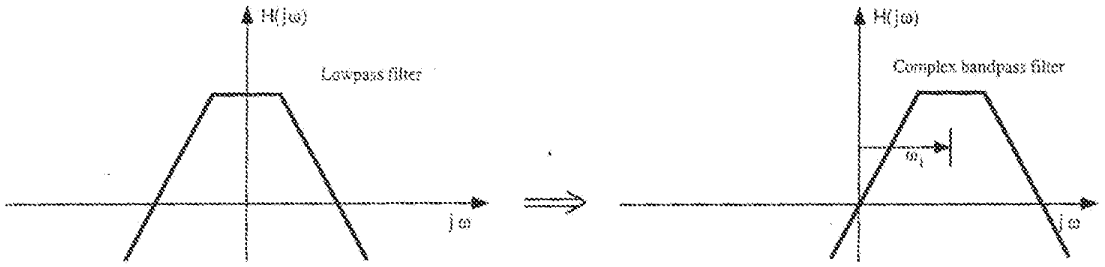


Fig. 14. The effect of a frequency translation on the transfer function.

in the real and imaginary signal path. However, this is only possible for circuits in which there is no physical coupling between the real and the imaginary path. This limits the usability of this technique to circuit topologies in which only real operations are performed on the complex signal. A zero-IF receiver is an example of such a circuit. The amplitude error is then of course determined by the matching between the AGC's; but in a DSP, AGC's can be implemented accurately. The other two types of mismatch error cannot be corrected. Although any phase and amplitude errors can be corrected theoretically, this is practically only possible when they are frequency independent or at least constant in the passband.

In the previous paragraph, the real first-order low-pass filter has been used as an example. The conclusions drawn from this example can be extended to higher order low-pass filters and amplifiers. Bandpass filters, oscillators, and mixers can also be analyzed in the same way. In bandpass filters, pole position matching is dominant. In the passband, the mirror error caused by amplification mismatch of bandpass filters differs not from low-pass filters, but the amplitude and phase errors caused by pole position mismatch are about Q-times worse. Quadrature oscillators often use an RC–CR circuit to obtain the 90° phase shift. The phase shift is a result of comparing the phase shift of a pole and a zero. Therefore, its mirror error highly depends on the matching of this pole and zero and will be dominantly a phase error.

IV. Analog Integrated Complex Filters

A. Complex Filters Synthesis

The transfer function of a real filter is a rational real polynomial function in $j\omega$. An active complex filter can have any rational complex polynomial function in $j\omega$ as transfer function. Most interesting are complex bandpass filters which have a passband only at either positive or negative frequencies [15], [16]. Their transfer function is found by frequency translating a low-pass filter.

$$H_{bp}(j\omega) = H_{lp}(j\omega - j\omega_c). \tag{18}$$

This translation remaps all poles and zero in the s-plane by moving them from their position centered around the zero axis to the center frequency f_c. The translation of poles and zeros in the s-plane is illustrated in Fig. 13. Fig. 14 shows the translation of the filter transfer function from low-pass to bandpass. The translation of a single pole is given in (19).

$$\begin{aligned} H_{lp}(j\omega) &= \frac{1}{1 + j\omega/\omega_o} \\ H_{bp}(j\omega) &= \frac{1}{1 - j\omega_c/\omega_o + j\omega/\omega_o} \\ &= \frac{1}{1 - 2jQ + j\omega/\omega_o}. \end{aligned} \tag{19}$$

A single complex pole cannot be realized with a real filter. Only complex pole pairs can be realized. The result of (19) is a single complex pole. The translated version of a single complex pole is also given with (19). The complex part must just be added to or subtracted from the complex term $2jQ$. Consequently, with this building block for a single complex pole, any translated low-pass filter transfer function can be realized. Fig. 13 depicts this frequency translation operation in the s-plane for a fifth-order low-pass Butterworth filter. After the translation, the poles are not compensated anymore. This is only possible in a complex filter.

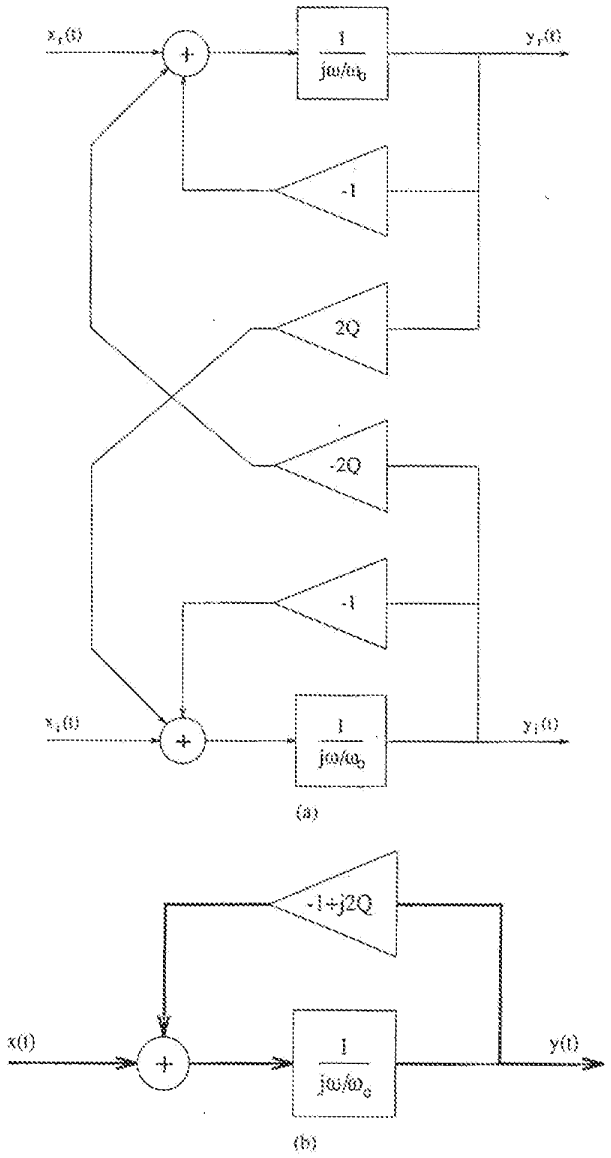


Fig. 15. Block scheme for the realization of a single complex pole. (a) The full notation and (b) the compact notation.

The realization of $H_{bp}(j\omega)$ for a single pole is given in Fig. 15. It is nothing more than the direct synthesis of the transfer function. Fig. 15(a) is the full block schematic with building blocks for real signals. Fig. 15(b) is the same block schematic, but given in a more compact notation which will be used further on throughout this text. A thick arrow stands for a complex signal and it actually represents a bundle of signals (in all our examples, it represents either 2 or 4 signals). The building blocks can stand for complete complex operators. The realization of a translated pole via direct synthesis requires the use of two integrators. This is equal to what a real low-pass filter for complex signals requires, and it is only one-half of what a real bandpass filter for complex signals requires. This makes complex bandpass filter very cost efficient.

Analog integration of a complex filter can be done with all available implementation techniques for filters, as there are active-RC, OTA-C, OTA-RC, MOSFET-C, and Switched-Capacitor. Which technique is most appropriate depends on specifications imposed by the application. Fig. 16 shows an active-RC realization of a complex pole. In Fig. 17, the transfer function of a translated fifth-order low-pass Butterworth filter is given for positive and negative frequencies. The filter has a bandwidth of 220 kHz, and the center frequency is 250 kHz.

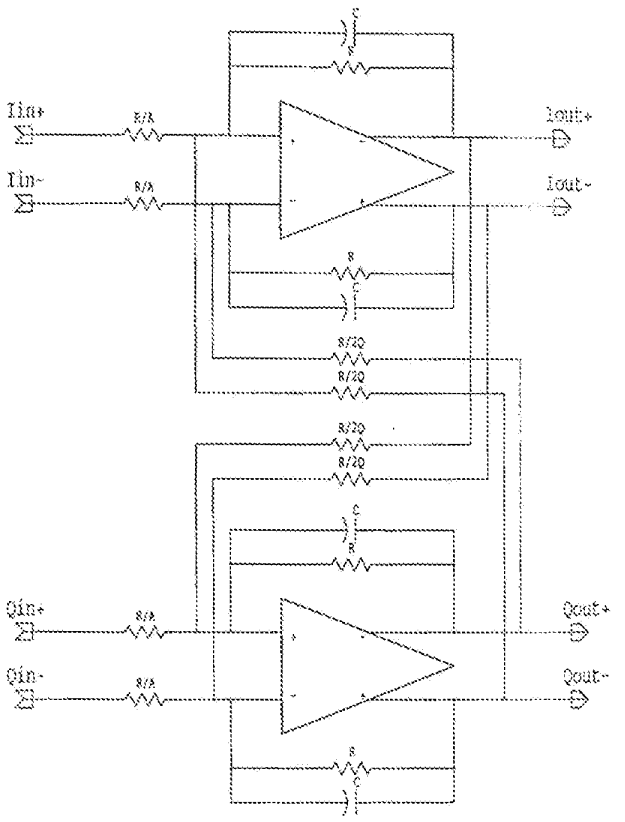


Fig. 16. Realization of a single complex pole with the active-RC filter technique.

B. Sensitivity to Mismatch

In analog integrated implementations, which are different from digital implementations, perfect matching of components like resistors and capacitors is not possible. It is therefore important to choose an implementation technique that depends on components which have a good matching. For the active-RC realization, resistor and capacitor matching is important. Equations (20), (21), and (22) give approximate expressions for the errors at the edges of the passband of the translated low-pass filter of Fig. 15. This is only for frequency mirroring from negative to positive frequencies. The mirroring from wanted to unwanted frequencies is not an unwanted effect.

$$\frac{\Delta A}{A} = \frac{\Delta R}{R} + \frac{\Delta R}{2Q \cdot R} \quad \text{(amplification mismatch)} \tag{20}$$

$$\frac{\Delta A}{A} = \frac{\Delta R}{8R} + \frac{\Delta C}{8C} \quad \text{(pole position mismatch)} \tag{21}$$

$$\Delta\varphi = \frac{\Delta R}{4R} + \frac{\Delta C}{4C} \quad \text{(pole position mismatch).} \tag{22}$$

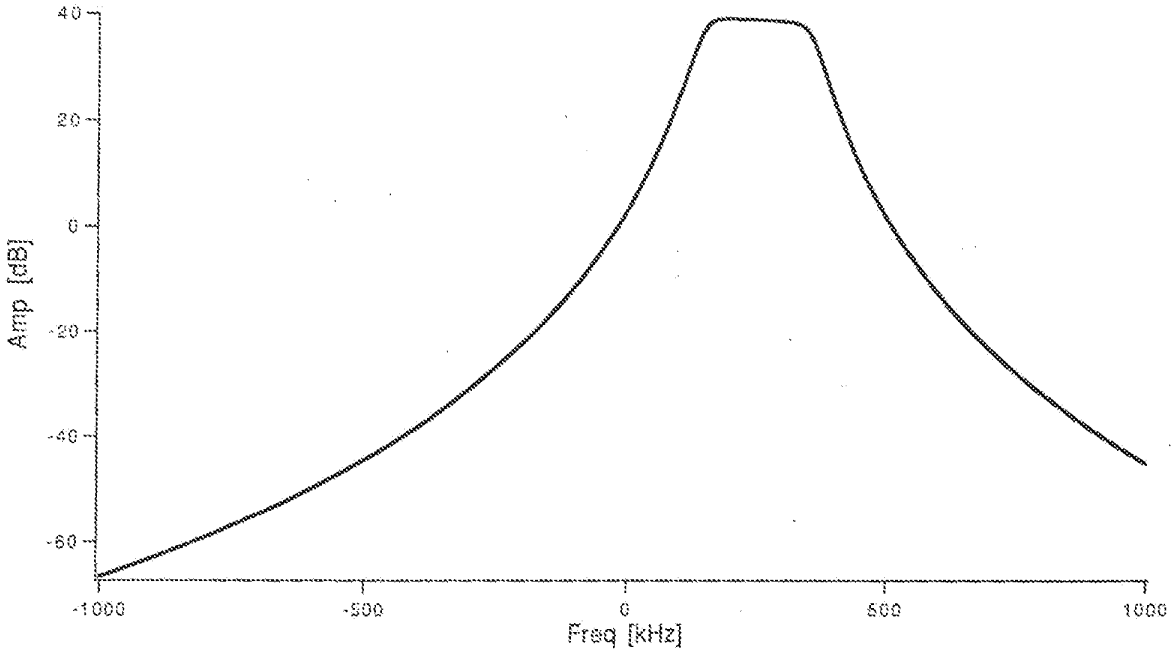


Fig. 17. Transfer function of a frequency translated fifth-order low-pass Butterworth filter.

Fig. 18 gives the crosstalk from negative to positive frequencies for the translated fifth-order Butterworth filter. This crosstalk has been simulated with the Monte Carlo simulation method assuming a random mismatch of 0.2% on every resistor and 0.1% on every capacitor. The crosstalk is equal to −60 dB and depends mainly on the mismatch between the input resistors of the first filter stage.

V. Receivers with Complex Signal Structures

A. Analysis of the Zero-IF Receiver

The obvious example of a receiver topology that uses complex signals is the zero-IF receiver. The topology of a zero-IF receiver is given, in compact notation, in Fig. 19. The RF signal is broadband filtered and then downconverted with a single positive frequency equal to the carrier frequency. The mixing with a positive frequency means that only the negative frequency components of the wanted signal are downconverted and that no mirrored signal is found in the baseband. This has already been illustrated with Fig. 7. After low-pass filtering, the signal is ready for sampling and demodulation.

B. The Low-IF Receiver using a Complex Filter

Fig. 20 shows how the quadrature downconversion mixer can also be used with a LO signal slightly lower then the carrier frequency. The wanted and the mirror signal are downconverted to the IF. However, both signals are not superimposed on each other. The wanted signal is situated at negative frequencies, while the mirror signal is situated at positive frequencies. This receiver topology can be called a low-IF receiver. The IF can be low (a few hundred kilohertz, i.e., one or two times the signal bandwidth), because there is no need for any HF mirror signal suppression.

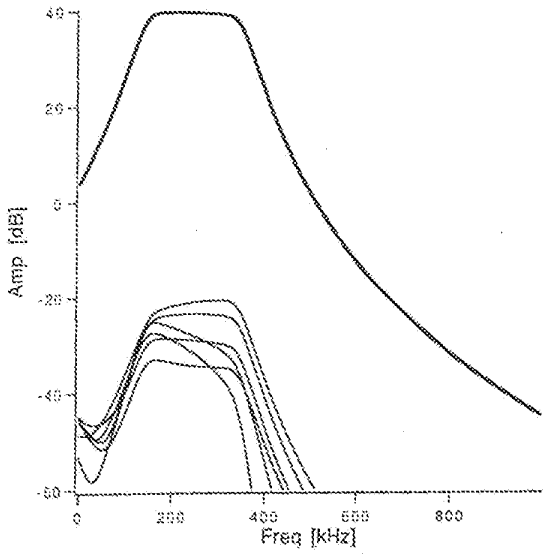


Fig. 18. Monte Carlo simulation of the signal crosstalk from negative to positive frequencies for the translated fifth-order Butterworth filter.

Further downconversion of the IF signal can be done in two ways, both are shown in the full and compact notation in Figs. 21 and 22. In Fig. 21, the mirror signal is first suppressed with a complex bandpass, i.e., shifted low-pass filter, centered around the IF frequency. The final downconversion of the wanted signal to the baseband can then be done by multiplication with a sine. After the LF complex bandpass filter, the wanted signal is separated from its neighbors and is ready for sampling. The required dynamic range of the A/D-converter (number of bits) is the same as for a zero-IF receiver. The same signal is applied, only the center frequency is different. Digital applications require about 6–8 bits, high

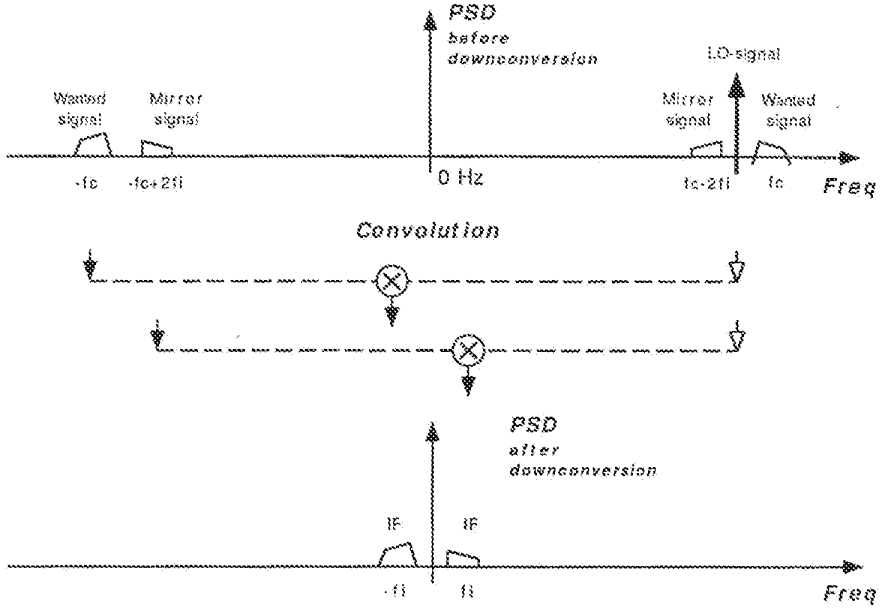


Fig. 19. Downconversion to a low IF.

quality continuous-time applications will require 10 bits. By making the sample frequency, f_s, equal to the IF, the sampling automatically performs the downconversion to the baseband. This means that the speed of the A/D-converter can also be the same as in zero-IF receivers (for the same suppression of aliasing signals with the same, but translated, LF filter). A 400-kHz IF and f_s are suitable values for a signal with a 200-kHz bandwidth (a 100 kHz baseband bandwidth). The same signal can be equally good downconverted with an IF of 200 kHz and an f_s of 400 kHz. In this configuration, every second sample has to be inverted.

C. The Low-IF Receiver Using Real Filters

Fig. 22 shows the alternative approach to the final downconversion. A real bandpass filter is used to separate both the wanted and the mirror signal from their neighbors. Downconversion must be done with a positive frequency equal to the IF. Downconversion with a single sine would bring the mirror signal also to the baseband. After downconversion, a low-pass filter makes sure that the mirror signal, situated at $2 \cdot f_i$ is suppressed sufficiently. Again, after the bandpass filter, the signal is ready for sampling. For easy downconversion, the sample rate has to be four times the IF (e.g., 800 kHz for a 200-kHz signal). This is twice the sample rate which is needed in the version with the complex bandpass filter, but this is no problem for today's A/D-converters. The big difference is found in the required number of bits. In this topology, not only the wanted signal, but the wanted signal together with the mirror signal, is sampled. The mirror signal can be 20–30 dB higher than the wanted signal, and in high-quality applications the wanted signal still has to be sampled with a 10 bit precision. Therefore, 4–5 extra bits are required, resulting in, for the high-quality applications, the need for a 16-bit A/D-converter. Low-cost digital applications will be satisfied with 12 bits, and this value can be further decreased by carefully

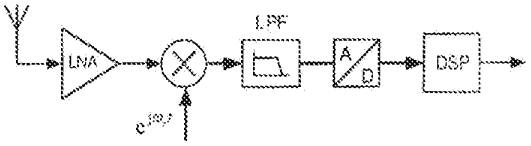


Fig. 20. The zero-IF receiver topology in compact notation.

choosing the position of the IF. The mirror frequency is best situated between two transmitter signals.

Actually, the use of a real bandpass filter is not necessary. Using a 12–16-bit A/D-converter with a good antialiasing filter after the downconversion from RF is enough to make the topology of Fig. 22 work. The big advantage of the use of real filters is the fact that the frequency independent amplitude errors, which is the cause of a finite mirror rejection in the LF part, can be corrected by means of a simple AGC algorithm in the DSP.

D. Comparing Zero-IF and Low-IF Receivers

The advantages of a low-IF receiver compared to a zero-IF receiver are clear. There is absolutely no DC-problem simply because the wanted signal is not situated around DC. This also includes the problem of LO to RF crosstalk. The product of the LO multiplied with itself is situated around DC with a very small bandwidth (less than 1 kHz). The RF-to-LO crosstalk problem is reduced. The product of the RF signal multiplied with itself is broadband, but most of its power is still situated around DC in a band equal to the bandwidth of one transmitted signal (e.g., 200 kHz).

The disadvantage of low-IF receivers is that the suppression of the mirror signal must be higher. In zero-IF receivers, the mirror signal is the same as the wanted signal, and this means that a 40-dB suppression does result in an SNR of 40 dB for the wanted signal. In low-IF receivers, the mirror

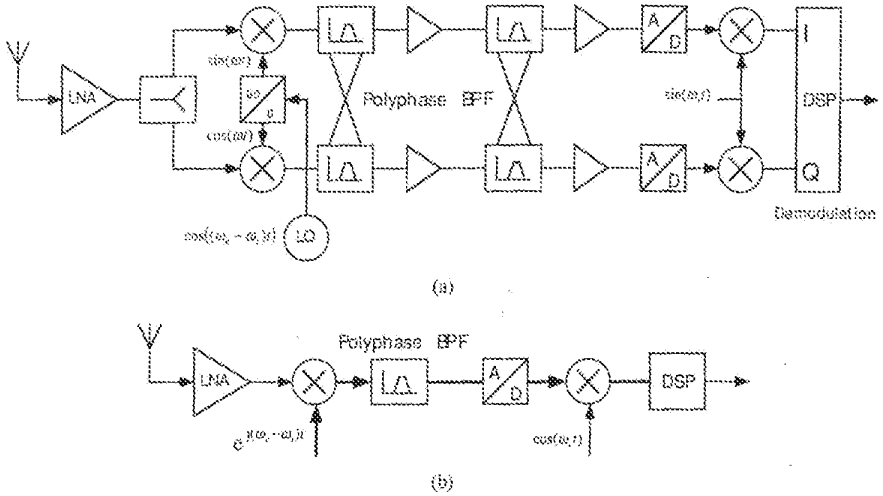


Fig. 21. The topology of a low-IF receiver which uses a complex bandpass filter in the LF part. (a) Full notation and (b) compact notation.

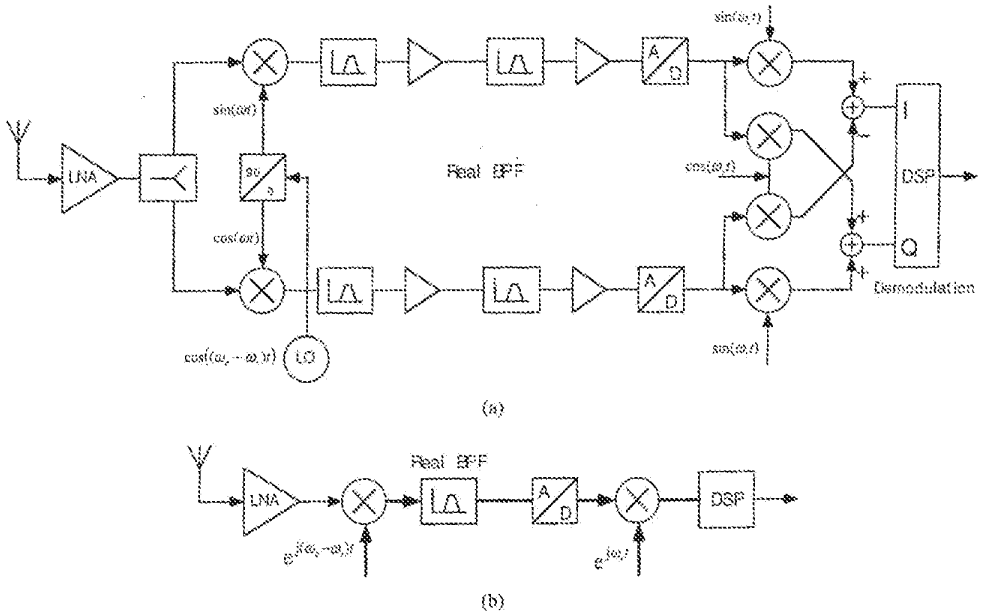


Fig. 22. The topology of a low-IF receiver which uses real filters in the LF part. (a) Full notation and (b) compact notation.

signal can be higher than the wanted signal. A mirror signal suppression of 70 dB is required for an SNR of 40 dB when the mirror signal can be 30 dB higher than the wanted signal. A careful choice of the IF, so that the mirror frequency is situated between two transmission channels, is important. In this way, the suppression specs can be lowered to 50–60 dB.

The achievable suppression is determined by the negative-to-positive frequency crosstalk of the complex building blocks, and this in its turn is determined by matching. A low-frequency complex bandpass filter with a negative-to-positive frequency crosstalk of less than -60 dB can be realized. Lower values, like -70 and -80 dB (required in high-quality applications), cannot be realized. The use of the low-IF topology with limited filtering (only antialiasing) and a 16-bit A/D-converter can offer this performance when a digital amplitude correction is applied. This strategy shifts the high specs from the analog part to the A/D-converter. As the performance of integrated A/D-converters improves rapidly, this is a good way to go. Even at this moment, a 16-bit 1-MHz A/D can already be realized at a reasonable cost of chip area and power consumption [17].

A matching problem that remains in all presented topologies is the phase error which is induced by the quadrature oscillator. Good matching is hard to realize at high frequencies and a phase error of 1° is equal to a mirror suppression as poor as -35 dB. It is this phase error which is the limit to the mirror suppression of todays zero-IF receivers. Further reduction of this phase error is vital, and a new technique has recently been proposed with which this phase error can be reduced to values which are significantly less than 1° [18].

VI. Conclusions

In this paper, the low-IF receiver has been examined as alternative for the IF and zero-IF receiver. Three new topologies have been presented. All three topologies use the same RF and

quadrature downconversion part as in a zero-IF receiver, but different from the zero-IF receiver are all three insensitive to DC offsets and LO to RF crosstalk. The three topologies have been synthesized by means of the complex signal method. With this technique, abstraction can be made of the multipath approach which is used in zero-IF receivers and in the presented low-IF receivers. The complex signal technique has also been used to analyze the effects of mismatch between the paths in the different receiver topologies. Since low-IF receivers are insensitive to DC offsets, mismatch is the main remaining source of decreased performance because it results in a limited mirror signal suppression.

The first low-IF receiver topology which has been proposed is based on the replacement of the low-pass filters of a zero-IF receiver by a complex bandpass filter. Such a filter is a linear frequency translated version of the low-pass filters. However, it has only a passband for positive frequency components, and it is in this way that it can discriminate between the wanted signal and the mirror signal. The RF-part, the downconversion part, the A/D-converters, and the DSP for this low-IF receiver can be exactly the same as in the zero-IF receiver.

The second and third presented low-IF receiver use, respectively, a bandpass filter and a slightly more broadband low-pass filter. In these receivers, the mirror signal suppression is not performed at the low IF, but in the DSP after a four-mixer further downconversion. The consequence is that these low-IF receivers require A/D-converters with a larger number of bits. Their advantage over the first low-IF receiver is that here the amplitude mismatches, which have been introduced in the analog part, can still be corrected in the DSP. The preferred version is the topology with the low-pass filters. It has the most simple structure of all three, and it is the least sensitive to phase errors.

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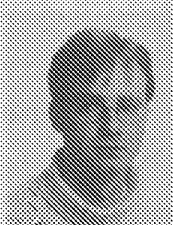
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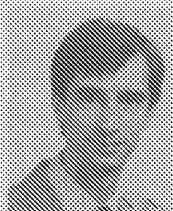
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Aminghasem Safarian
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Silicon-Based RF Front-Ends for Ultra Wideband Radios

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Chapter 1
Introduction

Ultra-wideband (UWB) technology enables high data-rate short-range communication, in excess of hundred megabit-per-seconds and up to multi-gigabit-per-seconds, over a wide spectrum of frequencies, while keeping power consumption at low levels. This low power operation results in a less-interfering co-existence with other existed communication technologies (e.g., UNII bands).

In addition to carrying a huge amount of data over a distance of up to 230 feet at very low power (less than 0.5 mW), the UWB signal has the ability to penetrate through the doors and other obstacles that tend to reflect signals at more limited bandwidths and higher power densities.

The key attributes of UWB technology, therefore, include; high data rates, ranging and communication applications, low equipment cost, and immunity to the multipath fading. These features have motivated the researchers to investigate performance-optimized integrated circuit (IC) solutions for UWB technology.

To best utilize the entire UWB spectrum specified by the FCC from 3.1GHz up to 10.6 GHz, the constituent transceiver should operate across this wide spectral band. On the other hand, designing RF front-end circuits, particularly in CMOS technology, for UWB transceivers entails stringent challenges associated with wideband requirements. In fact, the RF front-end has to exhibit wideband RF characteristics of gain, noise figure, and linearity, as well as low power consumption. The scope of this book includes design and analysis of novel wideband RF front-ends for UWB transceivers in silicon technologies. A great deal of emphasis will be made on the exploration of new performance-optimized distributed integrated circuit topologies for UWB wireless radios.

1.1 Organization of the Book

The book is organized as follows: Chapter 2 provides an introduction to the history and applications of the UWB technology, and reviews the UWB transceiver architectures and design challenges in UWB RF front-end design.

Chapter 3 describes various techniques to design UWB low-noise amplifiers in CMOS technology. Furthermore, we present the systematic design guideline

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and analysis of a CMOS performance-optimized distributed low-noise amplifier (DLNA). A set of comprehensive analysis of the DLNA's gain and noise figure will also be described.

Chapter 4 presents a novel distributed RF front-end which extends the idea of distributed mixers to a distributed RF front-end, incorporating composite cell of low-noise transconductance amplifier (LNTA) and mixer. This distributed RF front-end is mainly designed for dual conversion UWB receivers. Design guidelines and implementation issues of the distributed RF front-end will be discussed, extensively.

Chapter 5 extends the concept of distributed architectures to design a distributed direct-conversion RF front-end (DDC-RF) for the UWB receiver. Such RF front front-end exhibits wideband characteristic, while addressing three important issues in any conventional distributed circuit, namely high power dissipation, large area, and most importantly, the existing delay and loss from one tap-node of the constituent transmission-line to the next which translates to in-phase and quadrature (IQ) phase and gain imbalances. To overcome IQ mismatches, a current equalization technique is illustrated. This chapter also includes the CMOS implementation of the DDC-RF prototype and measurement results.

Chapter 6 employs the distributed architecture in the design of novel active power combiners and splitters with controlled delay and gain. These circuits are key building blocks of multi-antenna UWB (MA-UWB) transceivers.

Finally, Chapter 7 provides concluding remarks.

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Chapter 2
Ultra Wideband Systems

2.1 Wireless World of Technologies

2.1.1 WPAN, WLAN, WWAN

Wireless technologies represent a rapidly emerging area of growth and importance for providing ubiquitous access to the network by mobile users. New standards and technologies are being implemented to allow wireless networks to replace fiber optic and copper lines between fixed points several miles apart. The application domain of wireless networks continues to grow, replacing wires within homes, buildings, metropolitan areas through the deployment of wireless local area networks (WLANs). A WLAN, sometimes referred to as LAWN, is a technology in which mobile users can connect to local area networks through a wireless radio connection. A WLAN also interoperates with other wired LANs. Hence, its behavior must be compatible with other parts of the LAN infrastructure, such as TCP/IP. Two or more LANs then build up the wide area network (WAN). A WAN with wireless radio connection is called wireless WAN (WWAN). An extensive area-coverage for WWAN is generally offered on a nationwide level with wireless network infrastructure provided by a wireless service carrier.

Figure 2.1 demonstrates the world communication technologies, their designated data-rates and potential applications. The MAN stands for the metropolitan area network and the SAN is an abbreviation for the satellite area network.

Of particular interest to this book is wireless personal area network (WPAN), which is a technology for high data-rate communication among the personal devices within relatively short distances. The reach of a PAN is typically a few meters. PANs can be used for communication among portable and mobile computing devices such as PCs, personal digital assistants (PDAs), peripherals, cell phones, pagers, and generally consumer electronics; allowing such devices to communicate and interoperate with one another. Communication environment in WPANs, therefore, favors peer-to-peer connections compared to the ones with infrastructures, such as WLANs. This characteristic of WPANs enables ad-hoc, tiny, low-power and low-cost communication schemes for huge number of devices [1]. The main issue of WPAN standard, however, lies in peaceful co-existence with other existing wired and wireless networking systems with overlapping frequency bands.

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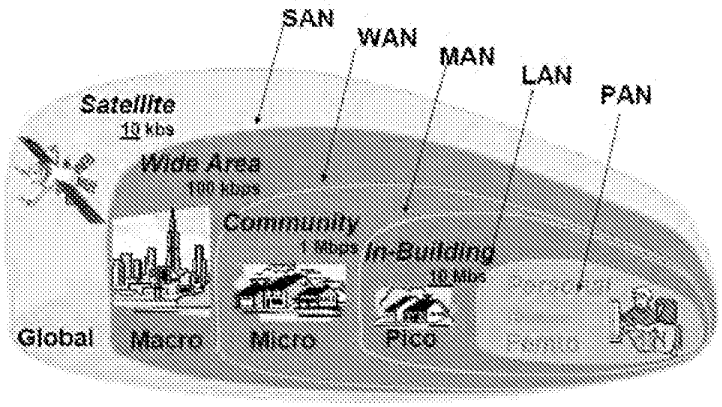


Fig. 2.1 World of communication technologies [2]

UWB falls into the WPAN technology aiming for short-range communication with data rates more than 100Mbps.

From a communications theory perspective, perhaps the most important characteristic of UWB systems is their capability to operate in the power-limited regime. This attribute is comprehended using Shannon's equation for the channel capacity [3]:

$$C = BW \log(1 + SNR) \tag{2.1}$$

where C is the maximum channel capacity (bits/sec), BW is the signal bandwidth and SNR is the signal-to-noise ratio. To increase the channel capacity, and essentially the data rate, one can increase either the signal bandwidth or the signal-to-noise ratio. The channel capacity grows linearly with the signal bandwidth, but only logarithmically with the SNR. Therefore, increasing the signal power to enhance the SNR and essentially channel capacity does not provide a low power solution, and is limited by other factors. In addition, the scaling trend in silicon technologies morphs itself to wireless transceivers that operate in power limited regime. In other words, increasing the power to achieve higher speed communication does not comply well with voltage scaling in silicon technologies. Furthermore, higher transmit powers could interfere strongly with other communication standards. It is thus inferred from Shannon's theory that increasing the signal's bandwidth provides a solution for low-power high data-rate communications. This notion lays the groundwork for UWB technology.

2.1.2 UWB Technology

UWB is a wireless radio technology for use in high speed data transmission or long distance localization applications. Ultra-wide bandwidth communication makes it possible to realize point-to-point, high-speed data transmission between laptops,

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pocket devices and peripheral consumer handhelds within a short distance with low emission. On the other hand, this technology allows the location tracking through low data-rate communication for longer ranges without interfering with existing wireless systems.

UWB technology is defined by the federal communications commission (FCC) as any wireless scheme that occupies either a fractional bandwidth of $BW/f_c > 20\%$, where BW is the communication bandwidth and f_c is the band's center frequency, or more than 500MHz of absolute bandwidth. FCC has also allowed the UWB radio transmissions in the unlicensed frequency range from 3.1 GHz to 10.6 GHz at a limited transmit power of −41.3dBm/MHz, as also shown in Fig. 2.2.

A UWB signal, in fact, occupies extremely wide bandwidth where the RF energy is spread over gigahertz of spectrum. It is wider than any narrowband wireless system by orders of magnitude, and its emitted power seen by other narrowband systems is a fraction of their own power.

If the entire 7.5 GHz band is optimally utilized, the maximum power available to UWB transmitters is approximately 0.556mW or less. This is only a fraction of available transmit power in the industrial, scientific and medical (ISM) bands such as the WLAN IEEE 802.11a/b/g standards. This effectively relegates the UWB scheme to indoor, short-range communications at high data rates or mid-range communications at low data rates, as shown in Fig. 2.3. Applications such as wireless USB and PANs have been proposed with hundreds of Mbps to several Gbps with distances ranging anywhere between 1– to 4–meters. For ranges beyond 20 meters, the achievable data rates by UWB are low compared to existing WLAN systems such as IEEE 802.11a/b/g. [4].

Both UWB and BlueTooth (BT) technologies are used for WPAN. Nevertheless, UWB is capable of delivering data rates in excess of 100 Mbps, while consuming a small amount of power and operating in wide spectral band without interfering with existing communication standards. UWB can also use coaxial cables or twisted-pair cables to communicate data at rates faster than 1 gigabit per second.

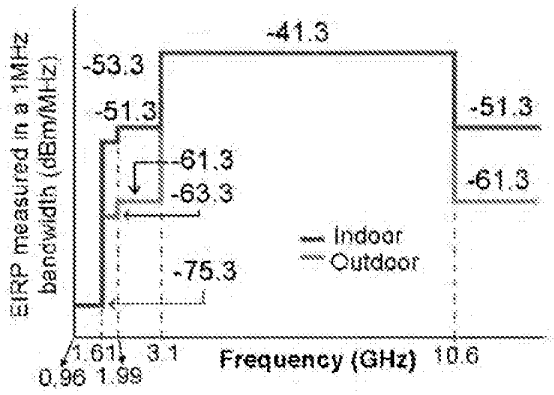


Fig. 2.2 UWB spectral mask and FCC Part 15 limits

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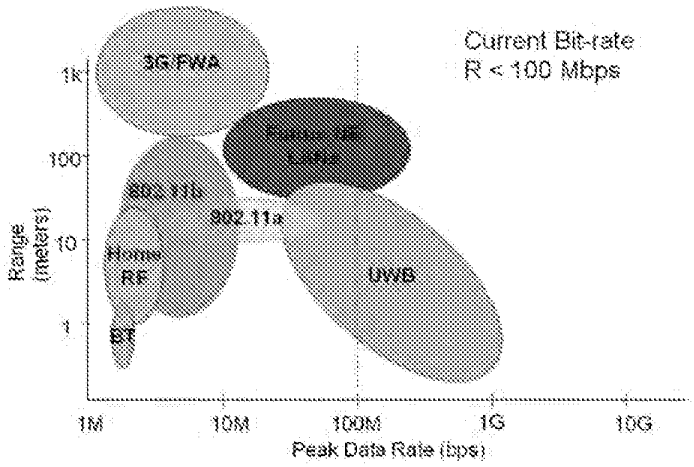


Fig. 2.3 Comparison between UWB and existing WLAN/WPAN systems [5]

2.2 UWB Applications: High Speed Short Range Communication, Long Range Localization

Nowadays "wireless" is an emerging trend in communication networks. While wireless technologies have facilitated a great deal of convenience for users of portable devices within local and wide area networks, they are yet to be extensively used for high speed short-range transmission between PC peripherals and other consumer electronics. UWB technology brings forth the convenience and mobility of wireless access to electronic devices located within few meters inside the home and office; allowing transmission of video, audio and other high-bandwidth data. The potential application in enormous fields where wireless communication network facilitate the work has greatly boosted up the development of UWB. Today, most computer and consumer electronic devices—everything from a digital camcorder and DVD player to a mobile PC and a high-definition TV (HDTV)—require wires to record, play or exchange data. UWB will eliminate these wires, allowing people to "unwire" their lives in new and unexpected ways. For instance, high data rate UWB enables efficient transfer of data from digital camcorders, wireless printing of digital pictures from a camera without the need for an intervening personal computer, and the transfer of files among cell phone handsets and other handheld devices like personal digital audio and video players.

UWB, as a short-range radio technology, complements other radio technologies with longer range coverage, such as WLAN, worldwide interoperability for microwave access (WiMAX), and cellular wide-area communications. It is used to relay data from a host device to other devices in small areas (up to 10–15 meters).

Using UWB:

- An office worker could put a mobile PC on a desk and instantly be connected to a printer, scanner and Voice over IP (VoIP) headset.
- All the components for an entire home entertainment center could be set up and connected to each other without a single wire.

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- A digital camcorder could play a just-recorded video on a friend's HDTV without anyone having to fiddle with wires.
- A portable MP3 player could stream audio to high-quality surround-sound speakers anywhere in the room.
- A mobile computer user could wirelessly connect to a digital projector in a conference room to deliver a presentation.
- Digital pictures could be transferred to a photo print kiosk for instant printing without the need of a cable.

The above advantages have stimulated the researchers to investigate this technology for a performance solution. With the connection speed ranging from 100Mbps to above 1Gbps, UWB systems provide a high data rate connection between devices while keeping power consumption at a low level.

Most of the aforementioned UWB applications target high data-rate communication over short distances (e.g., such as wireless USB), primarily due to extremely low emission level. The spread-spectrum attribute of UWB communication scheme contrives another application domain that requires extremely low-power low data-rate wireless sensing over longer distances, such as localization services, imaging sensors, and RF tags [2]. UWB, therefore, can be used to enable "see-through-the-wall/body" imaging technology and high-precision time-of-arrival-based localization approaches used in medical imaging, remote sensing of objects and motion detection radars with good range resolution. It allows centimeter accuracy in ranging (1GHz BW) as well as in low-power and low-cost implementation of communication systems.

2.3 UWB Signals

UWB technology is at present defined by the FCC as any wireless transmission scheme that occupies a fractional bandwidth of more than 20% (i.e., $BW/f_c \geq 20\%$ where BW is the transmission bandwidth and f_c is the band's center frequency), or and absolute bandwidth of more than 500 MHz. Under this definition, pulse-based systems, wherein each transmitted pulse instantaneously occupies the UWB bandwidth from 3.1- to 10.6 GHz, or an aggregation of at least 500 MHz worth of narrow band carriers, for example in multi-band orthogonal frequency-division multiplexing (MB-OFDM) fashion, can gain access to the UWB spectrum.

Historically, impulse-radio (IR) UWB systems were the first that utilized the concept of wideband communication in power-limited regime. They deploy short-duration pulses with fast rise and fall times, which readily results in wideband spectra. For example, a pulse signal which is centered at 6GHz and occupies a bandwidth of more than 1.2GHz (i.e., 20% fractional bandwidth) is called a UWB pulse. The IR-UWB transceiver architecture promises to be simple and low cost, because many building blocks that exist in conventional transceivers such as off-chip power amplifiers or on-chip driving amplifiers can possibly be eliminated. This

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implies that narrow time duration pulses can directly be transmitted to the antenna. Moreover, in a multipath-dominated environment, larger transmission bandwidths result in increasingly fine resolution of multipath arrivals, thereby leading to reduced fading per resolved path. In the time-domain, the impulsive nature of transmitted UWB waveforms prevents significant overlap, and hence, reduces possibility of destructive combining. Nonetheless, processing such narrow time-duration pulses in an IR-UWB receiver requires high-speed wideband RF building blocks with high sensitivity.

Alternatively, in a MB-OFDM UWB system the 3.1–10.6-GHz band is split into narrow sub-bands. Sophisticated time-frequency codes are used to interleave data sequences in different sub-bands. Each sub-band occupies an absolute bandwidth of 500MHz. A UWB system incorporating MB–OFDM approach exhibits several useful properties, which include:

- Less interfering coexistence and interoperability with existing communication standards
- Less intersymbol interference (ISI) and inter-carrier interference (ICI)
- Easier adoption to different worldwide regulatory environments
- Future scalability and backward compatibility
- Possibility of designing circuits in standard CMOS process to take advantage of all the benefits resulting from technology scaling
- Excellent robustness in multipath environments

As will be seen in Section 2.5.2, the main drawback of MB-OFDM systems is the use of transceiver architectures with complex (de)modulation schemes and sophisticated signal processing units. Another problem is that the peak-to-average power-ratio (PAPR) of OFDM signals tends to be higher than that of narrow pulses in pulse-based UWB. This, in turn, imposes more stringent requirement on MB-OFDM transceiver design, particularly on the power amplifier (PA) in the transmitter.

2.4 Advantages of Ultra Wideband over Narrow-band Systems

UWB technology represent few advantages over the commonly-used narrowband communication systems, such as simpler transceiver architecture, lower cost, lower power consumption, and the capability to resolve multipath fading.

The lower complexity and cost is mainly due to simple transceiver architecture which is different from the conventional narrowband communication systems. In a conventional communication system, a baseband signal is mixed with a higher frequency carrier, producing a radio frequency signal which is transmitted in the desired wireless channel. A power-hungry PA then amplifies this RF signal and delivers required amount of power to the transmit antenna. In the UWB transmitter, the pulse generator can be designed in such a way as to generate UWB-compliance short-duration pulses, which obviates the need for an

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up-conversion mixer or a high-power PA. Similarly, in the receiver path of a UWB system, an analog correlator as a matched filter is used to detect the signal, which essentially substitutes the conventional down-conversion mixers and de-modulators.

Because of the pseudo-random nature of UWB pulse signals with low duty cycles, the signal power is concentrated in a short interval within one repetition period. Hence, the power spectral density of transmitted pulses in the channel looks like that of thermal noise. This indicates that UWB transceivers are capable of communicating undetectable noise-like signals at low energy levels [4, 6]. Accordingly, the impact of UWB interference on the existing wireless networks, such as 802.11a WLAN is negligible [7].

2.5 UWB Transceiver Architecture

2.5.1 Impulse Radio (IR) UWB

IR-UWB is often known as carrier-less technology, wherein the modulated baseband signal is directly transmitted through the antenna into the air, as shown in Fig. 2.4. This attribute greatly reduces the complexity of transceiver architecture, and specifically the RF front-end, compared to narrowband transceivers which employ complex frequency conversion architecture. The low-power emission requirement in the IR-UWB transceiver relaxes the design of antenna pre-drivers on the transmitter side. This is quite opposite to narrowband transceivers where high power PAs are needed to launch the signal with sufficient power to the antenna.

In a receiver structure of an IR-UWB system one could insert the analog-to-digital converter (ADC) just after a low-noise amplifier (LNA) and variable-gain amplifier (VGA), to carry out much of the signal processing in the digital domain [8].

Although the system architecture is seemingly easy to implement, it entails a serious design challenge. The ADC for such system should operate at extremely high sampling rate of at least 15Gsamples/sec with resolution of 4 to 6 bits. Designing such an ADC in currently available nanoscale CMOS process is impossible. Despite encountering serious practical issues when used for 3.1–10.6GHz UWB band, this solution may be suitable for 0–900MHz UWB band dedicated for sensor networks.

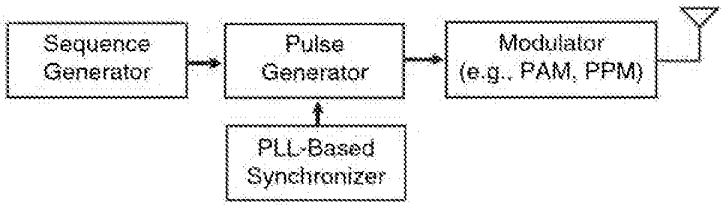


Fig. 2.4 Block diagram of an Impulse Radio-UWB transmitter [8]

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Clearly, the ADC can be moved down the analog chain so that some of the signal processing is carried out in the analog domain, as shown in Fig. 2.5. This is achieved by using a time-integrating analog correlator after LNA/VGA and before the ADC. The analog correlator consists of a wideband multiplier followed by an integrator [9]. The two inputs of the correlator, or the multiplier, are the input signal and the template generated by the pulse generator. The product of these two input signals at the output of the multiplier is further integrated to produce a robust signal level with relatively low frequency content. This signal is fed to the ADC.

The UWB receiver of Fig. 2.5 needs a precise pulse generator, which provides periodic timing signals at the receiver. The local template pulse is triggered by the coded timing signal and produces a series of template signal pulses ideally synchronized with the sequence of all the possible transmitted signals. The correlator then converts the received RF signal to baseband for detection [10]. In a typical spread spectrum receiver, the correlator slides the received signal and correlates it with a reference template pulse. When the received signal and the reference pulse are synchronized in phase, a peak emerges at the output of the correlator.

2.5.2 MB-OFDM UWB

Multi-carrier modulation, also known as OFDM, widely used in the implementation of IEEE 802.11.a, HIPERLAN II, DVB, DAB standards and xDSL technology, performs well in dispersive channels, and enables high rate communication with inexpensive receivers. When combined with guard interval and cyclic prefix, OFDM eliminates ISI/ICI, and overcomes fading by using forward error correction (FEC) coding [11]. The channel equalizer employs the frequency-domain equalization technique that is easily performed using training sequences. Furthermore, the channel estimate can be incorporated into a soft decision Viterbi decoder in a bit-interleaved coded modulation (BICM) fashion to get even more coding gain.

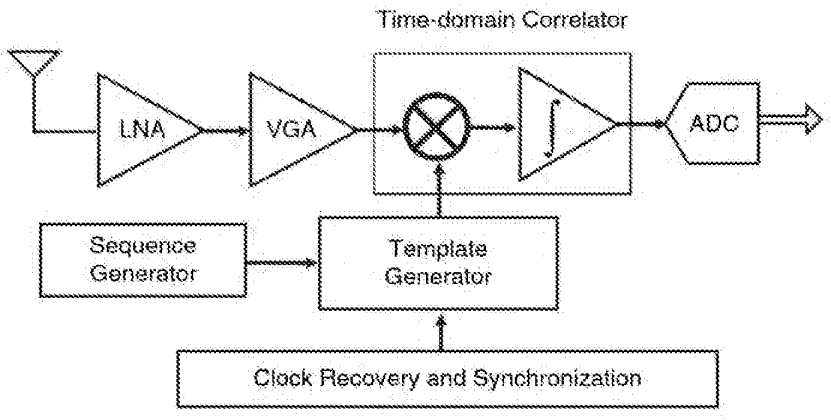


Fig. 2.5 Block diagram of an IR-UWB receiver with a time-domain correlator [8]

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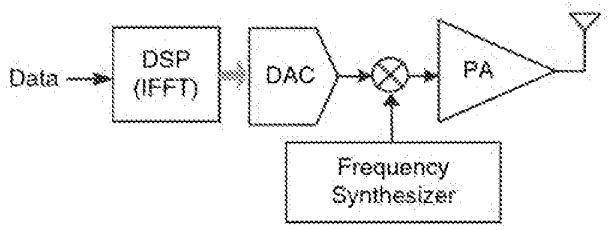


Fig. 2.6 Block diagram of a MB-OFDM UWB transmitter

and have the system operate in lower SNRs. In a multi-band OFDM system, OFDM symbols are interleaved along different frequency bands, hence yielding frequency diversity as well. Another advantage of OFDM is its capability to capture multi-path energy with a simple fast Fourier transform (FFT), in contrast to CDMA and impulse radio, where rake correlator fingers should be used to exploit multi-path diversity. OFDM enables us to adapt our system to avoid using some specific bands to comply with other regulations set forth by other countries. This is easily achieved by modulating "null" on some sub-carriers eliminating the need for narrowband notch filters. Problems with OFDM are the complexity of the transmitter, and high peak-to-average power ratio (PAPR) of OFDM signal causing distortion in power amplifier used in the transmitter. Considering all the pros and cons, a multi-band OFDM still results in a highly satisfactory trade-off between different design criteria.

The block diagram of a MB-OFDM UWB transmitter is shown in Fig. 2.6, where the input data symbols are mapped to the subcarriers of an IFFT to create an OFDM symbol. The digital output of DSP block is converted to an analog signal, which is then upconverted to RF frequencies. Finally, the PA delivers the RF data to the antenna.

A block diagram of a direct conversion MB-OFDM UWB receiver is also shown in Fig. 2.7. The receiver topology can be any of the widely known architectures such as dual conversion or zero/low IF. A pre-select filter immediately after the antenna rejects the out-of-band images, blockers, and out-of-band noise, while passing only the desired UWB signal band. Next, the LNA and quadrature mixers amplify and

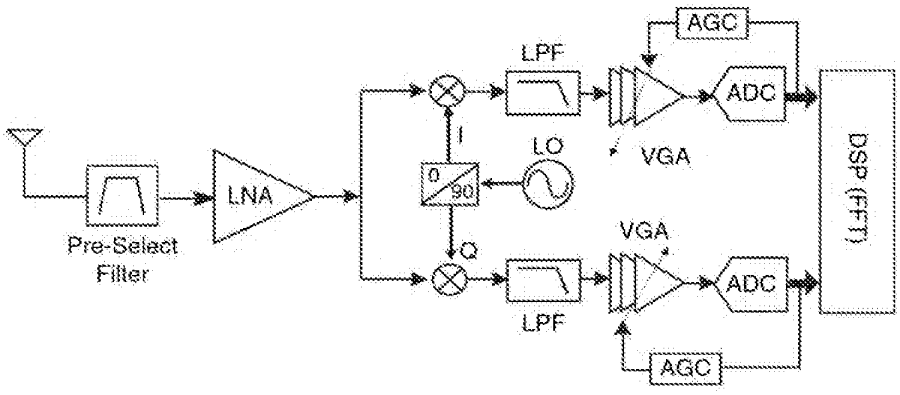


Fig. 2.7 Block diagram of a MB-OFDM UWB direct conversion receiver

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downconvert the received wideband signal to either DC or low-IF. The lowpass filter in companion with VGA filter the out-of-band interferes and set the required amplitude level of the signal for proper analog-to-digital conversion. Finally, the digital signal processing (DSP) unit performs the inverse of the transmitter's baseband operation, which is, taking the FFT from the received baseband signals.

2.6 Challenges

Clearly, designing an RF front-end circuit in UWB transceivers, either IR or MB-OFDM UWB, will face a great challenge in the implementation using low cost CMOS device due to stringent requirements of the UWB technology. Since the bandwidth of UWB licensed by FCC is from 3.1 $\sim$ 10.6GHZ, this implies that RF front-end of UWB transceiver including LNA, down conversion mixers, correlators which are conceptually mixers, should be able to process very wide bandwidth signals spread over the wide range of frequencies. Such a front-end has to exhibit wideband characteristics including gain, noise figure and linearity. This is the key challenge for the RF front-end circuit design besides the low power constraint.

2.7 Link Budget

The link budget for UWB systems is restricted by the FCC rules, signal bandwidth, and the device technology. However, in general the following steps are necessary to calculate the link budget. The average transmit power, *Avg_TX_Power*, is readily expressed as [12]:

$$Avg\_TX\_Power = EIRP \cdot BW \cdot TX_{ON} \tag{2.2}$$

where TX_{ON} denotes the percentage of the time that the transmitter is "ON" in a time duplex (TD) multiplexing system. The *EIRP* stands for *equivalent isotropically radiated power*. It is the amount of power that would have to be emitted by an isotropic antenna that evenly distributes power in all directions to produce the peak power density in the direction of maximum antenna gain.

The path loss between transmitter and receiver is obtained using the well-known Friis equation, i.e,

$$Path\ Loss\ (\text{dB}) = 20\ \log\left(4\pi rf/c\right) \tag{2.3}$$

where c is the light speed, r is the distance between transmitter and receiver, and f is the carrier frequency.

The receiver sensitivity depends on the thermal noise level (-174dBm/Hz), bit rate (r_b), noise figure (NF) of the receiver, and the minimum signal-to-noise ratio ($SNR_{\min}$) which is the required E_b/N_0 to achieve a given *BER* for a certain modulation such as QPSK. Therefore, the receiver sensitivity, *RX_Sensitivity*, is:

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Table 2.1 Link budget for MB-OFDM systems

Data Rate	110Mbps	200Mbps	480Mbps
Avg. TX power	−10.3 dBm	−10.3 dBm	10.3 dBm
Path Loss	64.2 (r=10m)	56.2 (r=4m)	50.2 dB(r = 2m)
RX/TX Antenna Gain	0 dBi	0 dBi	0 dBi
Avg. Rx Power	−74.5 dBm	−66.5 dBm	−60.5 dBm
Noise Power / Bit	−93.6 dBm	−91.0 dBm	−87.2 dBm
CMOS Rx NF	6.6 dB	6.6 dB	6.6 dB
Total Noise Power	−87.0 dB	−84.4 dB	−80.6 dB
Required Eb/No	4.0 dB	4.7 dB	4.9 dB
Implementation Loss	2.5 dB	2.5 dB	3 dB
Rx Sensitivity	−80.5 dBm	−77.2 dBm	−72.7 dBm
Link Margin	6.0 dB	10.7 dB	12.2 dB

$$RX\_Sensitivity = -174\,(\text{dBm/Hz}) + 10\log(BW) + NF + 10\log(r_b) + SNR_{min} \tag{2.4}$$

On the other hand, the received signal power is equal to the total transmit power, including the antenna gain, minus the path loss between transmitter and receiver, i.e.,

$$RX\_Power = Avg\_TX\_Power + Antenna\ Gain\,(\text{dBi}) - Path\ Loss\,(\text{dB}) \tag{2.5}$$

Therefore, the design margin is calculated as:

$$Link\ Margin = RX\_Power\,(\text{dB}) - RX\_Sensitivity\,(\text{dB}) \tag{2.6}$$

For a MB-OFDM signal, Table 2.1 demonstrates the link budget for three data rate values of 110, 220, and 480 Mbps.

Table 2.1 implicitly shows several challenges in designing RF front-end for a MB-OFDM UWB transceiver. Specifically, the receiver NF and sensitivity merits attention. According to calculations of Table 2.1, the entire RX including the RF switches, RF front-end, filters and baseband circuits need to contribute less than 6.6dB of NF.

More examples of link budget calculations for low bit rate application of UWB can be found in [12].

Hereafter, next chapters will extensively discuss circuit solutions that satisfy the design specifications in Table 2.1 for UWB transceivers.

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Chapter 3
UWB Distributed Low Noise Amplifiers (DLNA)

Despite showing several attributes including the enhanced immunity against ISI/ICI and multipath fading, and gigabit wireless connectivity at short ranges; UWB radios should meet severely challenging design specifications, summarized in Table 2.1. More specifically, the requirement of having wideband RF front-end calls for new circuit design techniques. The design of UWB RF chain should naturally start with the low-noise amplifier (LNA), which entails several design challenges due to stringent requirements. A key building block in the UWB receiver's RF front-end, the LNA must retain good performance (i.e., low noise figure and high gain) across the system's wideband frequency spectrum from 3.1- to 10.6-GHz. Importantly, the same set of design requirements should be satisfied in regard to the LNA design regardless of the type of UWB system (i.e., impulse radio or multi-band) being deployed [1]. In fact, the input signal power at the receiver after the UWB antenna and the pre-filter circuit is too low to allow any pre-processing for appropriate sub-band filtering in a multi-band UWB receiver utilizing all available sub-bands. Even if such signal processing was possible, each sub-band would require a distinct LNA circuit, which leads to a bank of LNAs in the receiver. Such design solution is, however, inefficient from both chip area and performance perspectives, demanding alternative circuit design techniques.

In this chapter, first, various techniques for designing UWB low-noise amplifiers in silicon technologies are reviewed. Then the systematic design and analysis of a CMOS performance-optimized distributed low-noise amplifier (DLNA) comprising bandwidth-enhanced cascode cells. Each cascode cell employs an inductor between the common-source and common-gate devices to enhance the bandwidth, while reducing the high-frequency input-referred noise.

The remaining part of this chapter is organized as follows: Section 3.1 overviews the wideband matching techniques. Section 3.2 gives a brief overview of distributed circuits. Section 3.3 describes the circuit topology and a method to calculate the bandwidth-enhancing inductors. This section presents the noise analysis and performance optimization methodology for the proposed DLNA, by first giving a brief overview of the current state of knowledge. The noise analysis and optimization of the DLNA accurately accounts for the impact of thermal noise of line terminations and all device noise sources of each CMOS cascode cell including flicker noise, correlated gate-induced noise and channel thermal noise on the overall

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noise-figure. A three-stage performance-optimized wideband DLNA has been designed and fabricated in a 0.18μm SiGe process, where only MOS transistors were utilized. Measurements of the test chip show a flat noise-figure of 2.9dB, a forward gain of 8dB, and input and output return losses below −12dB and −10dB, respectively, across the 7.5GHz UWB band. The circuit exhibits an average IIP3 of −3.55dBm. The 872μm × 872μm DLNA chip consumes 12mA of current from a 1.8V DC voltage. Section 3.4 provides measurement results of the fabricated DLNA. Finally, Section 3.5 presents conclusions of this chapter.

3.1 Wideband LNA Matching

The LNA is a key building block in a UWB wireless receiver. Challenges in UWB LNA design involves achieving (1) a NF of around 3.5dB, (2) a relatively flat gain of at least 8dB, (3) a minimum reverse isolation of −20dB, and (4) a good linearity (e.g. IIP3>−8dB) [2].

Several techniques have been proposed recently that accomplish required wideband matching at the input of the LNA. Examples of four types of input matching circuits are shown in Fig. 3.1, which includes resistive, $1/g_m$ using common-gate configuration, local shunt-feedback and wideband bandpass termination. These techniques are incremental extensions to the narrowband matching techniques.

The resistive matching is simple and straightforward, but it likely fails to achieve acceptable matching at higher frequencies due to device input capacitances. Moreover, it has a 3dB NF penalty because of the termination resistance, R_G. Interestingly, the distributed circuit architecture, explained later in this chapter, addresses both of these critical issues.

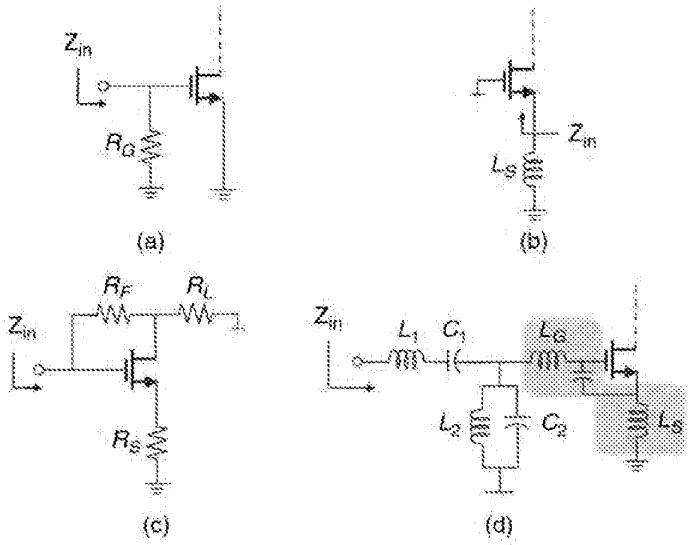


Fig. 3.1 Wideband input matching: (a) Resistive termination, (b) 1/gm termination, (c) passive feedback termination, and (d) bandpass impedance transformation

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A common-gate low-noise amplifier (CG-LNA) [2] and CMOS resistive feedback amplifiers, designed for the UWB lower frequency band (i.e., 3–6 GHz), likely exhibit degrading performance in the UWB upper band due to the device's parasitic capacitances. The inductance of L_s in CG-LNA extends the bandwidth of the input matching. However, the NF of the CG LNA is considerably larger than that of the CMOS common-source or cascode LNAs. Previously employed in common-source LNAs in [3] and [4], the g_m-boosting technique was proposed by [5] to improve the NF performance of a UWB CG LNA.

References [6] and [7] independently designed the first lumped LNA circuits for the UWB radio using a cascode circuit and high-order wideband bandpass filters (BPF)'s to provide wideband input matching. The underlying idea is to use the low-pass impedance matching network used in conventional narrowband RF circuits, and develop a bandpass matching network using lowpass-to-bandpass transformation. Figure 3.2 shows an L-matched and a T-matched network and the corresponding transformed networks.

An important point of concern is that the circuit NF's reported in [6] and [7] were not flat across the 7.5GHz bandwidth and the minimum NF obtained by these works were 4dB, and 2.5dB (in bipolar technology), respectively. The in-band NF of the LNA in [6] increases to as much as 8dB due to inevitable mismatch associated with frequency-dependent 50Ω resistance seen from the transistor's gate terminal.

As an alternative solution, a distributed topology with gain stages distributed along actual or artificial transmission lines (TLs) achieves intrinsically wideband characteristics. This is because the input and output capacitances of gain stages, which are dominant components in bandwidth degradation, will be absorbed to the input and output TLs. Section 3.2 gives a brief overview of distributed circuits. [8, 9, 10, 11] study the analysis and design of various types of distributed circuits in more depth and details.

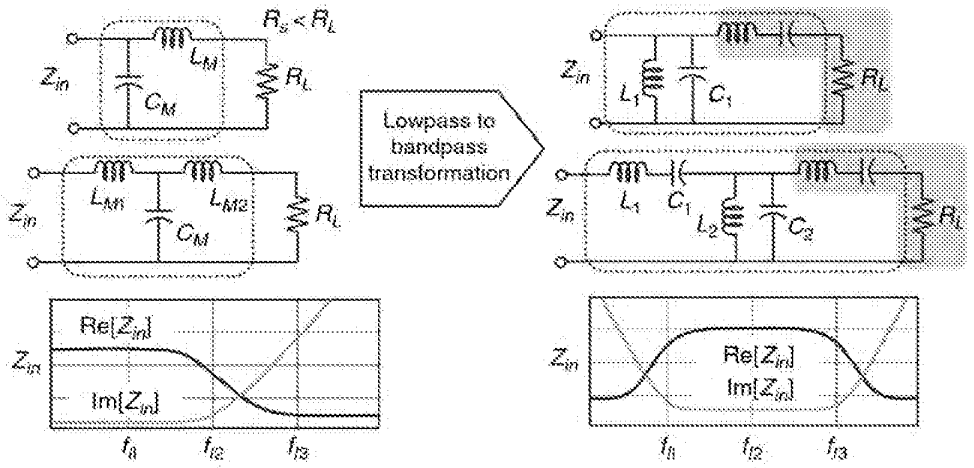


Fig. 3.2 Low pass and band pass impedance transformation

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3.2 Background: Distributed Circuits

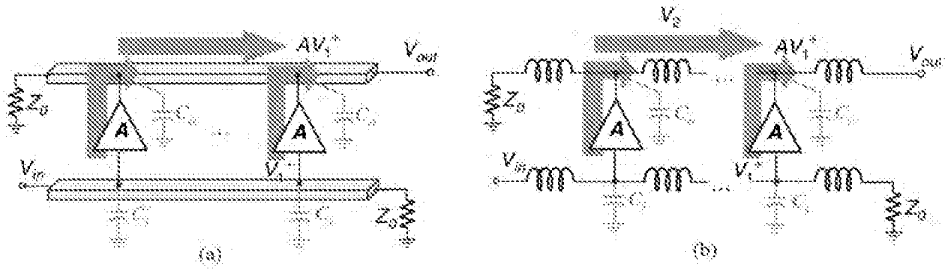
The distributed topology incorporating transmission lines (TL)'s was originally proposed by Ginzton et al. [13]. Insufficient technological capability to design area-efficient distributed circuits delayed the usability of these circuits for a long time. They reappeared in 1980's using a variety of processes, such as GaAs or other III-V technologies, and recently in CMOS process. Examples include distributed amplifiers [9, 10, 11, 12], distributed mixers [14], and distributed oscillators [9, 15]. The renewed interest in distributed circuits is mainly due to the capability of designing on-chip TLs, and high-Q inductors.

Figure 3.3 shows the general block diagram of a DA comprising TLs and gain stages distributed along the TLs, where each gain stage can simply be a common-source (or common-emitter in bipolar technology) stage. The TLs can be realized using either coplanar waveguides (see Fig. 3.3(a)) or cascaded LC circuits (see Fig. 3.3(b)).

As a fundamental property, integrated circuits incorporating on-chip TLs trade delay for bandwidth [8, 16]. In frequency domain, the transistor's parasitic capacitances are absorbed into the constants of the TL [16], as also demonstrated in Figs 3.3(a–b). Hence, the circuit bandwidth is set by the cutoff frequency of the TLs.

An important concern regarding distributed topologies is, however, higher power dissipation and larger chip area compared to lumped circuits. Both the power dissipation and the area of a distributed circuit increase with the number of stages, suggesting a compromise between power dissipation and gain-bandwidth product (GBW). Despite consuming more power than the conventional lumped circuits, the distributed architectures are highly amenable to technology scaling, which makes them a topology of choice for future developments of silicon-based millimeter-wave (MMW) broadband ICs.

The power consumption of a distributed circuit with N number of stages is N times that of a single stage amplifier. We will show that distributed amplifiers provide a better tradeoff between power consumption and the NF compared to lumped amplifiers, in that spending same power results in the lower NF compared to a single stage amplifier.



C_g: Input parasitic capacitance of the gain stage plus external capacitances
C_d: Output parasitic capacitance of the gain stage plus external capacitances

Fig. 3.3 The block diagram of a distributed circuit incorporating (a) actual CPWs, or (b) artificial LC circuits

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Distributed circuits are primarily based on broadband resistive matching, since the source impedance is matched to the termination impedance. This may imply that the minimum achievable NF of a distributed circuit cannot be less than 3dB, which we will show that is not the case and by proper design the NF of a distributed circuit can be less that 3dB.

Consider the g_m stage with resistive matching shown in Fig. 3.1(a). The lower bound noise factor F of the g_m stage with bias current of I is

$$F = \frac{Total\ Output\ Noise}{Total\ Output\ Noise\ due\ to\ Source} = 1 + \frac{R_G}{R_S} + \frac{4\gamma}{\alpha g_m R_S} \tag{3.1}$$

If the g_m stage consumes $N.I$ just to match the current consumption of an N stage distributed amplifier, then g_m increases proportional to $\sqrt{N}$, hence the device noise contribution is reduced by factor of $1/\sqrt{N}$. However, the noise contribution from the R_G remains unchanged, no matter how much power is burned in the g_m stage.

Now consider an N stage distributed amplifier comprising N identical g_m stages, where these stages are distributed along the input/output TLs. The input matching network is again resistive realized by the resistive termination of the TLs. However, in distributed circuits the input/output matching is intrinsically provided by the use of transmission lines.

The noise from R_S travels toward the output from each path and reaches coherently to the output just similar to the main desired signal. Therefore, the total output noise power due to the source resistance is:

$$Total\ Output\ Noise\ due\ to\ Source = \frac{N^2}{4} kTR_S \tag{3.2}$$

But the noise from the resistive matching termination reaches at the output form N paths with different delays. As a result, they all become uncorrelated at the output. One can thus easily calculate the total output noise power due to the resistive termination, which is the sum of the noise powers contributed by each path, i.e.,

$$Total\ Output\ Noise\ due\ to\ R_G = \frac{N}{4} kTR_G \tag{3.3}$$

Thermal noise sources from g_m stages are uncorrelated and will all add up at the output, which results in the following:

$$Total\ Output\ Noise\ due\ to\ g_m = NkT\gamma g_{d0}$$

Therefore, the lower bound of the noise factor of an N stage distributed amplifier is:

$$F_N = \frac{Total\ Output\ Noise}{Total\ Output\ Noise\ due\ to\ Source} = 1 + \frac{1}{N}\left(\frac{R_G}{R_S} + \frac{4\gamma}{\alpha g_m R_S}\right) \tag{3.4}$$

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Table 3.1 Comparison of a DA with a single-stage amplifier with resistive matching

	Resistive Single Stage with I current	Resistive Single Stage with $N.I$current	N-Stage DA
Gain	g_m	$\sqrt{N}g_m$	$\frac{1}{2}Ng_m$
Noise Factor	$1+\frac{R_s}{R_s}+\frac{4\gamma}{\alpha g_m R_s}$	$1+\frac{R_s}{R_s}+\frac{1}{\sqrt{N}}\frac{4\gamma}{\alpha g_m R_s}$	$1+\frac{1}{N}\left(\frac{R_g}{R_s}+\frac{4\gamma}{\alpha g_m R_s}\right)$
Current	I	$N.I$	$N.I$
Matching	Needs extra circuits	Needs extra circuits	Intrinsically wideband

While increasing number of stages lead to more power consumption, it will improve noise factor. Indeed, increasing the number of stages, and hence the power consumption, not only reduces the noise contribution of the active devices, it will also reduce the noise contribution of the matching resistance. For an infinite number of stages, $N\rightarrow\infty$, the N-stage distributed amplifier becomes noiseless! However, in reality for large number of stages (e.g., more than 5 or 6 stages) other noise sources such as thermal noise of the gate resistance and the inductor losses may dominate the NF. Table 3.1 compares three different scenarios that use resistive matching networks. This comparison reveals that, under the same amount of power consumption, distributed amplifiers attain a lower NF than lumped amplifiers

3.3 CMOS Performance-optimized DLNA

In a conventional CMOS DA, where each cell only employs a common-source transistor, the input-output coupling through overlap gate-drain capacitance of each transistor causes the real-part of the DA's propagation constant to become negative, resulting in the amplitude growth of the output waveform at the far-end load termination. The conventional DA is thus potentially unstable. In addition, any voltage/current variation in either gate or drain TL's terminations will be coupled to the other TL through C_{GD} of the common-source transistor. A DA with cascode cell can mitigate these deleterious effects [16, 17, 18]. However, common-gate transistors of each cascode cell begin to contribute significant noise to the output at high frequencies, thereby degrading the circuit's NF.

Indicated in Fig. 3.4 is the schematic of the proposed N-stage UWB DLNA comprising uniform gate and drain artificial LC TLs and identical cascode cells. Each cell employs a cascode configuration to guarantee stability across the entire bandwidth by providing isolation between the cell's input and output terminals. The interstage inductors of the gate (drain) TL along with gate (drain) parasitic capacitances of transistors M_{gk1} (M_{dk2}), $1\leq k\leq N$, constitute cascaded LC ladder circuits with characteristic impedance of $Z_G=\sqrt{L_G/C_{i,cs}}$($Z_D=\sqrt{L_D/C_{o,cg}}$) where $C_{i,cs}$ is the input capacitance of the common-source stage and $C_{o,cg}$ is the output capacitance of the common-gate stage within each cascode cell. Both Z_G and Z_G stay constant over a wide range of frequencies. In this design, both Z_G and Z_D are chosen to match the 50Ω source/load resistances.

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As indicated in Fig. 3.4, each cascode cell incorporates an inductor L_{Ck}, $1 \leq k \leq N$, for the following reason: recall that the gate and drain TLs boost the BW by absorbing the input and output parasitic capacitances of each cell. These TLs do not, however, affect the frequency roll-off due to large parasitic capacitance seen at the internal node of a conventional cascode cell, where the drain of the common-source transistor is short-circuited to the gate of the common-gate transistor. Moreover, the input-referred noise of each cascode cell in the absence of this BW-enhancing inductor may rise considerably at high frequencies, because the internal node's parasitic capacitances will lower the equivalent impedance seen at this node to ground. The above problems are alleviated by using inductors $L_{Ck}1 \leq k \leq N$. The proposed DLNA topology is based on a uniform distributed architecture, therefore, $L_{Ck} = L_{Cr} = L_C$, for all $k \neq r$.

In the absence of L_C, the circuit bandwidth is primarily limited by the pole associated to the internal node of the cascode cells whose value is $p_{cascode} = [g_{m,cg}^{-1}(C_{i,cg}+C_{o,cs})]^{-1}$, where $C_{o,cs}$ is the output capacitance of the common-source transistor, $C_{i,cg}$ is the input capacitance of the common-gate transistor, and $g_{m,cg}$ is the transconductance of the common-gate transistor in each cascode cell (cf. Fig. 3.4). The inductance L_C, which leads to less than 10% of ripple in the passband and a maximum increase of bandwidth, along with this boosted bandwidth are determined using the following analysis.

Figures 3.5 (a) and (b) show the AC equivalent and high-frequency small-signal model of the k-th cascode cell with BW-enhancing inductor L_C, seen from the internal node of the cascode cell. The high-frequency model of Fig. 3.3 (b) is used to obtain the transfer function $V_{ik}(s)/V_{gk}(s)$.

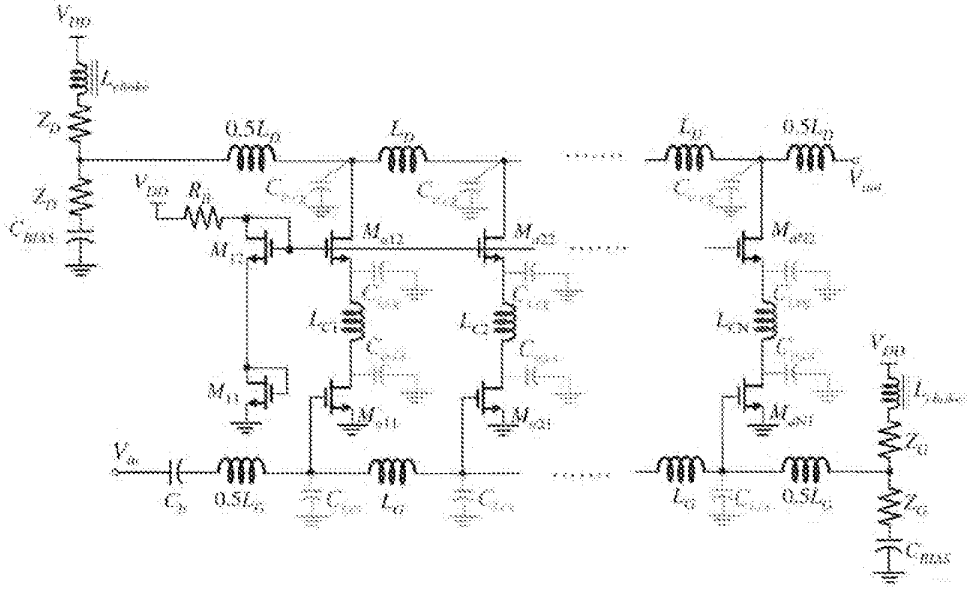


Fig. 3.4 Circuit schematic of the proposed N-stage distributed LNA ($N = 3$ in our design)

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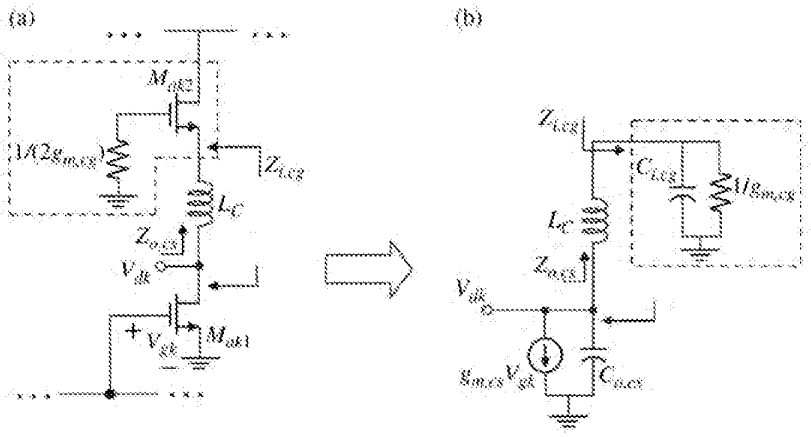


Fig. 3.5 (a) AC equivalent of the BW-enhanced cascode cell, and (b) small-signal model

L_C makes the equivalent impedance $Z_{o,cs}$, seen looking up from V_{dk} and expressed as $Z_{o,cs}(s) = (L_C C_{i,cg} s^2 + g_{m,cg} L_C s + 1)/(g_{m,cg} + C_{i,cg} s)$, behave inductively at high frequencies. This impedance effectively determines the *series resonant* frequency $\omega_{n,z} = (L_C C_{i,cg})^{-1/2}$ of the transfer function $V_{dk}(s)/V_{gk}(s)$ of the k-th cell, and is in parallel with the output impedance of common-source transistor M_{gk1} which is capacitive. Using the circuit model of Fig. 3.5 (b), the transfer function $V_{dk}(s)/V_{gk}(s)$ of the k-th cell is readily obtained as:

$$\frac{V_{dk}}{V_{gk}}(s) = \frac{g_{m,cs} g_{m,cg}^{-1} \left(\frac{s^2}{\omega_{n,z}^2} + \frac{2\xi_z}{\omega_{n,z}} s + 1 \right)}{\frac{s^2}{\omega_{n,p}^2} + \frac{2\xi_p}{\omega_{n,p}} s + 1}$$

$$= \frac{g_{m,cs} g_{m,cg}^{-1} (L_C C_{i,cg} s^2 + g_{m,cg} L_C s + 1)}{(g_{m,cg}^{-1} C_{i,cg} s + 1) L_C C_{o,cs} s^2 + g_{m,cg}^{-1} (C_{i,cg} + C_{o,cs}) s + 1},$$

$$\text{for} 1 \le k \le N \tag{3.5}$$

In the absence of $C_{i,cg}$, the *parallel resonant* frequency of the transfer function $V_{dk}(s)/V_{gk}(s)$ should have been $\omega_{n,p}^{(unloaded)} = (L_C C_{o,cs})^{-1/2}$. $C_{i,cg}$, however, lowers the parallel resonant frequency down to $(1 + g_{m,cg}^{-2} C_{i,cg}^2 \omega^2)^{-1/2} (L_C C_{o,cs})^{-1/2}$ which is smaller than $(L_C C_{o,cs})^{-1/2}$. This *loaded* resonant frequency is frequency-dependent. Because the goal is to obtain L_C so as to maximize the -3dB bandwidth ω_{-3dB}, the frequency offset $\sqrt{1 + g_{m,cg}^{-2} C_{i,cg}^2 \omega^2}$ of the loaded resonant frequency is evaluated at frequencies close to ω_{-3dB}. The parallel resonant frequency $\omega_{n,p}$ thus approximately becomes:

$$\omega_{n,p}^2 \approx \frac{1}{(L_C C_{o,cs})} \cdot \frac{1}{\sqrt{1 + g_{m,cg}^{-2} C_{i,cg}^2 \omega_{-3dB}^2}} \tag{3.6}$$

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To increase the bandwidth while avoiding large frequency peaking, the transfer function $V_{dk}(s)/V_{gk}(s)$ should hold specific characteristics including:

1. The numerator of (3.5) should be in the form of a maximally flat polynomial, implying that the damping factor ζ_z is $1/\sqrt{2}$ (see Fig. 3.6).
2. The denominator of (3.5) should exhibit small peaking in frequency domain, which leads to additional BW increase. A damping factor of ½ (i.e., $\zeta_p = 0.5$) results in a peaking of 1.25dB. Additionally, the parallel resonant frequency $\omega_{n,p}$ becomes equal to the 0-dB frequency, where the magnitude response of the transfer function crosses the 0dB axis after experiencing 1.25dB peaking (see Fig. 3.6).

By choosing $\omega_{n,p}=\omega_{n,z}$, the 0-dB cutoff frequency of the transfer function $V_{dk}(s)/V_{gk}(s)$ is boosted to $\omega_{n,p}$. Moreover, it results in a frequency peaking of less than 10%, as also shown in Fig. 3.6. This criterion along with the above design guidelines 1 and 2 provide sufficient information to calculate the inductance L_C and the new 3-dB bandwidth as follows:

$$L_C = \sqrt{2} g_{m,cg}^{-2}(C_{i,cg} + C_{o,cs}) \tag{3.7}$$

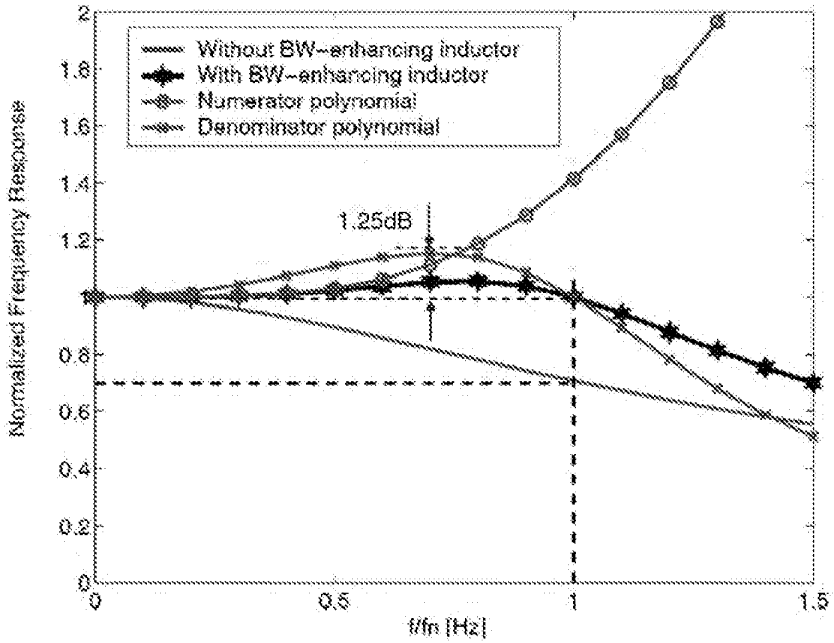


Fig. 3.6 (1) The normalized magnitude response without BW-enhancing inductor, (2) The normalized magnitude response with BW-enhancing inductor, (3) the numerator polynomial, and (4) the denominator of the transfer function

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$$\omega_{-3dB} = \frac{g_{m,cg}\sqrt{(C_{t,cg}/C_{n,cs})^2 - 1}}{C_{t,cg}} \tag{3.8}$$

The bias for cascode transistors in all constituent cells is provided by a single current mirror, as shown in Fig. 3.4. The artificial LC gate line provides the wideband input impedance matching, thereby obviating the need for inductive degeneration for each cascade cell of the DLNA circuit.

The spiral inductors with Q-factors of 10 at 10GHz are designed to realize interstage delay lines because they exhibit a larger inductance per unit length than CPWs or microstrip lines at the UWB frequency range and also avoid the circuit floorplan to spread too much in one dimension. TL inductors are designed such that the same characteristic impedance of 50Ω is obtained at each tap-point of the gate and drain lines so as to maximize the power transfer toward the load termination. The gate line's inductor L_G is larger than the drain line's inductor L_D, because the input capacitance is larger than the output capacitance of each cell. To verify the bandwidth improvement, the DLNA with and without the inductor L_C was simulated. As will be extensively discussed in Section 3.1, a three-stage circuit will result in minimum NF. The simulation result is demonstrated in Fig. 3.7, showing approximately 3.5GHz bandwidth improvement.

The circuit's NF is a function of the load terminations, parasitic capacitances of the cascode stage, the propagation constants of the LC TLs, and the number of stages. A comprehensive noise-figure analysis of the DLNA will be provided in Section 3.1. It intends to address specific issues arising from the analysis presented in [19] by calculating the PSD of noise in the DLNA more accurately.

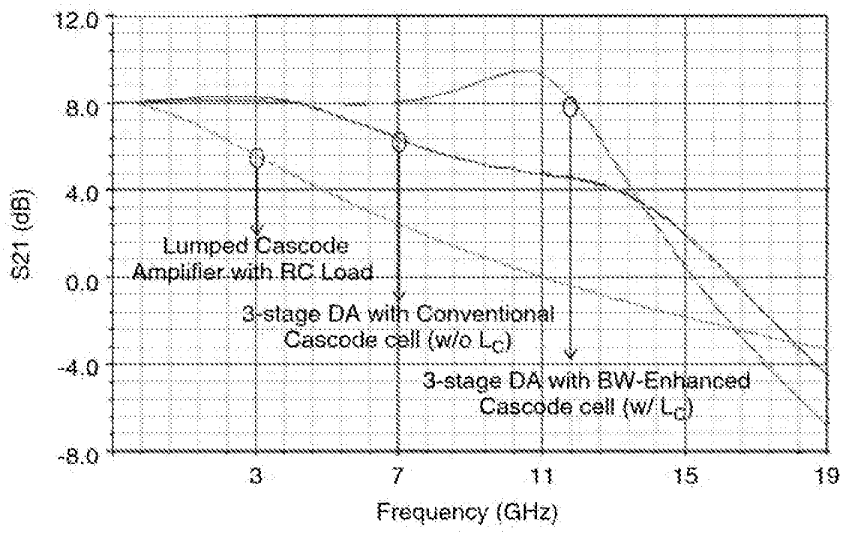


Fig. 3.7 Simulation results of a conventional cascode amplifier, a 3-stage DLNA without L_C, and a 3-stage DLNA with L_C

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3.4 Noise Analysis

The dominant intrinsic noise sources in the DLNA are: (1) thermal noise from the input source impedance ($R_S = Z_G$; Z_G is the gate line's characteristic impedance defined earlier), (2) thermal noise from the gate and drain terminations, and (3) dominant noise sources associated with each MOS transistor including the channel thermal noise, gate-induced noise, and flicker noise. Despite the fact that flicker noise presents negligible impact on a high frequency LNA circuit, for the sake of completeness, its contribution to the overall NF will be accounted for. The distributed structure of the DLNA provides several paths for any given signal/noise source in the circuit. Depending on the traveling direction of the wave toward the far-end termination, wave propagation falls into two classes, namely forward and backward propagation. For the same input and output matching impedances, the in-band forward power gain from the input terminal to the output is maximized when drain and gate TLs have the same propagation constants (i.e., $\beta_d = \beta_g = \beta$). This maximum forward power gain $G_p^{(F)}$ is expressed as (see [19] for more details):

$$G_p^{(F)} = \frac{N^2 g_{m,ck}^2 Z_D Z_G}{4} \tag{3.9}$$

The backward power gain $G_p^{(R)}$ at the near-end drain termination is expressed as [19]:

$$G_p^{(R)} = \frac{g_{m,ck}^2 Z_D Z_G}{4} \left(\frac{\sin N\beta}{\sin \beta} \right)^2 \tag{3.10}$$

To better clarify the forward and backward propagation phenomena, consider Fig. 3.8 showing the block diagram of a four-stage DA with a test current source applied to the input tap of the third cell. This figure clearly demonstrates backward and forward propagations of the wave, generated by I_{test}, toward the load termination.

For convenience, MOS transistors and gate/drain inductors are assumed to be lossless. The use of the inductance L_C in (3.7) allows us to keep the source-terminal impedance of each common-gate transistor large across the UWB frequency range. Therefore, the noise contribution of common-gate transistors $M_{nk}, 1 \leq k \leq N$ can be neglected. Measurement result in Section 3.4 indeed verifies the accuracy of this observation. The voltage across the input capacitance of each cascode cell is amplified by the small-signal gain $g_{m,ck}V_{gk}$ for $1 \leq k \leq N$, and the current from each cell flows in both directions with a phase constant $\beta_d = \beta_g = \beta$ per each LC section of the drain TL (cf. Figs. 3.7 and 3.8). The noise analysis, described in the following, accounts for the impact of high frequency gate-induced noise, and therefore, is an extension of [14]. It is based on a rigorous stochastic modeling with some similarities to the approach presented in [19]. Section 3.4.1 briefly overviews basic concepts of the stationary random process and the procedure introduced in [19] for noise analysis.

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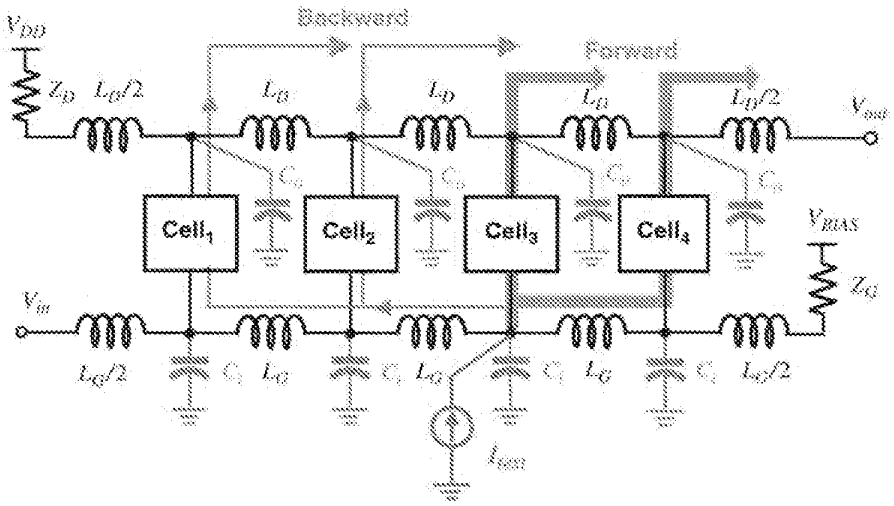


Fig. 3.8 Block diagram schematic of a four-stage DA with a test current source demonstrating the backward and forward propagations

3.4.1 Background and Current State of Knowledge

Device noise sources in electronic circuits are implicitly assumed to fall in the class of wide-sense stationary (WSS) processes [20]. For a WSS random process $x(t)$, the first-order (i.e., mean) statistical average is time-invariant, and the second-order (i.e., autocorrelation function) statistical average at time values t_1 and t_2, defined as $\Phi_x(t_1, t_2) = \overline{x(t_1)x(t_2)}$, depends only on the *difference* between t_1 and t_2 , $t_1 - t_2$. Subsequently, it only needs to be indexed by one variable rather than two variables, i.e., $\Phi_x(t_1, t_2) = \Phi_x(t_1 - t_2)$ (see [20]). Most importantly, the Fourier transform of the autocorrelation of a WSS process, widely known as power spectral density (PSD), is a deterministic function whose integral is the average power of noise. On the other hand, the Fourier transform $X(j\omega)$ of the noise $x(t)$ is defined as $X(j\omega) = \int_t^{x(t)\exp(-j\omega)dt}$ [20]. In contrast to deterministic signals, the Fourier transform of a random process does not carry useful insight with practical implications, as it is a random process by itself.

In an original work presented in [19], the noise-figure of the conventional DA, where each cell is simply a common-source transistor, was calculated. The noise sources that were taken into account in the analysis were channel thermal noise and gate-induced noise of transistors and thermal noise of source and load resistive terminations. For the sake of argument, the analytical procedure in [19] is summarized:

1. The output noise contribution of the r-th stage in an N-stage distributed amplifier is calculated. In doing so:

   (1) It calculates the Fourier transform of the output noise current due to forward and backward amplifications of noise generators of the r-th stage.

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(2) It calculates the magnitude square of the Fourier transform of the total current in the load termination due to the r-th section by combining currents due to forward and backward amplifications, vectorially.
(3) It assumes that the magnitude square of Fourier transform of the total current obtained in step (1.2) is equal to the PSD of the noise current, i.e., $S_{I_d}(\omega) = |I_d(\omega)|^2$, where $S_{I_d}(\omega)$ and $I_d(\omega)$ denote the PSD and the Fourier transform of the noise current I_d, respectively. This is false, as $|I_d(\omega)|^2$ is a random process itself, and cannot be equal to the PSD of noise. In fact, a theorem, proved in [20] and restated in the following, clearly specifies the relationship between a random process and its Fourier transform:
Theorem 1 (p. 515 of [20]). Suppose that $x(t)$ is a stationary random process with autocorrelation $\Phi_x(t_1 - t_2)$ and the PSD $S_x(\omega)$. The Fourier transform of $x(t)$, $X(\omega)$ is non-stationary white random process with autocorrelation expressed as: $\overline{X(\omega)X^*(\omega')} = 2\pi S_x(\omega)\delta(\omega - \omega')$ where $\delta(.)$ is the delta function.

Consequently, $\int_0^\omega \overline{X(\omega)X^*(\omega')}d\omega' = 2\pi S_x(\omega)$, and not $|X(\omega)|^2$ (which is a random process), is equal to $2\pi S_x(\omega)$. More importantly, [19] ignores the partial correlation between the gate-induced and thermal noise sources.

2. Finally, the noise contributions from all N stages are obtained by adding all the noise contributions for all r values from 1 to N.

We address the above problems by developing an analytical approach based on calculation of auto-correlation of the DLNA's output noise. Considering that the properties of Fourier transforms for deterministic signals also hold for random signals, we will first calculate the Fourier transform of the noise current due to forward and backward amplifications. Additionally, we take into account the frequency response of each cell. We will then calculate the autocorrelation functions of the output noise at the load termination. The PSD of noise will then be obtained by taking Fourier transform of the autocorrelation functions for the DLNA circuit of Fig. 3.4. This approach will be illustrated in details in Section 3.4.2.

3.4.2 Noise Contribution of MOS Transistors

Figures 3.7 and 3.8 demonstrate the forward and backward propagations of dominant noise sources of the k-th cell, respectively. To perform the noise analysis of partially correlated channel thermal noise $I_{d,k}$ and gate-induced noise $I_{g,k}$ of the kth stage, the gate-induced noise is first decomposed into its correlated and uncorrelated components [16, 21, 22]; i.e.,

$$\overline{I_{g,k}^2} = \overline{I_{g,uk}^2} + \overline{I_{g,ck}^2} = 4k_BT\delta g_{g,k}(1 - |c|^2) + 4k_BT\delta g_{g,k}|c|^2 \qquad \text{for} \quad 1 \le k \le N \tag{3.11}$$

where k_B is the Boltzmann's constant (1.38065×10^{-23} Joule/°K), T is the absolute temperature, $g_{g,k} = \zeta\omega^2 C_{GS,k}^2/g_{m,k}$ for $1 \le k \le N$, δ is a technology-dependent

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constant, and c is the correlation coefficient [defined as $c = \overline{I_{g,k} I_{d,k}^*} \Big/ (\overline{I_{g,k}^2}\ \overline{I_{d,k}^2})^{1/2}$] whose value for long-channel devices is approximately $j0.395$ [16, 21]. Moreover, $g_{m,k} = g_{m,ck}$ for $1 \le k \le N$.

All the cells distributed along constituent gate and drain TLs of the DLNA in Fig. 3.4 are contributors to the output noise power as well as the overall noise figure. Similar to the approach presented in [19] and summarized in 3.4.1, the noise contribution of MOSFETs of the k-th stage to the output is calculated by accounting for both forward and backward propagations of these noise sources. Because of non-zero correlation between correlated noise sources, the overall average power of additive combination of these noise sources is not equal to sum of the average powers of individual noise sources [20]. This notion will be taken into consideration during the forthcoming noise calculations.

In calculating the noise contribution of MOSFETs, the TLs are assumed to have identical propagation constants. The DLNA's power gain with the same input and output matching impedances will be maximized if the LC TLs have identical propagation constants [8].

First, the forward amplification of noise sources associated with the k-th cell is studied. Besides widening the BW, the inductor L_C reduces the noise contribution of the cascode transistor M_{ak2} of the k-th cell. The dominant noise sources are, therefore, the gate-induced noise, channel thermal noise, and low-frequency flicker noise of the common-source transistors M_{ak1}. Figure 3.9 shows the forward amplification of dominant noise sources of the k-th cell through the signal paths of this cell and $N-k+1$ cells. Using Fig. 3.9, the Fourier transform of the output noise current due to MOSFET noise sources associated with the k-th cell and their forward-propagated replicas is:

$$I_{o,k}^{(F)}(\omega) = \tfrac{1}{2}\,[I_{d,k}(\omega) + (N-k+1)(I_{g,ck}(\omega) + I_{g,uk}(\omega) + I_{1/f,k}(\omega))H_{g,k}(\omega)]e^{-j(N-k+1/2)\beta} \tag{3.12}$$

where $I_{o,k}^{(F)}(\omega)$ denotes the Fourier transform of the output noise current due to forward amplification of MOSFET noise sources of the k-th cell. $I_{d,k}$ and $I_{1/f,k}$ represent the Fourier transforms of the channel thermal noise and flicker noise currents of M_{ak1}, respectively. $I_{g,ck}$ and $I_{g,uk}$ are the Fourier transforms of the correlated and uncorrelated components of the gate-induced noise current of M_{ak1}, respectively. $H_{g,k}(\omega)$ is the input-output transfer function of the k-th cell. With identical cells and identical TL's inductors, the corresponding noise sources of the DLNA will be identical, i.e., $I_{d,k}(\omega) = I_{d,r}(\omega) = I_d(\omega)$; $I_{g,k}(\omega) = I_{g,r}(\omega) = I_g(\omega)$; $I_{1/f,k}(\omega) = I_{1/f,r}(\omega) = I_{1/f}(\omega)$ for $1 \le k, r \le N$. Furthermore, $H_{g,k}(\omega) = H_{g,r}(\omega) = H_g(\omega)$ for $1 \le k, r \le N$.

The backward propagations of gate and flicker noise sources of the k-th cell, shown in Fig. 3.10, contribute to the output noise current. The backward-propagated noises are all correlated with the original noise sources at the gate terminal of the k-th cell. Therefore, the Fourier transform of the noise current is calculated as (cf. Fig. 3.10):

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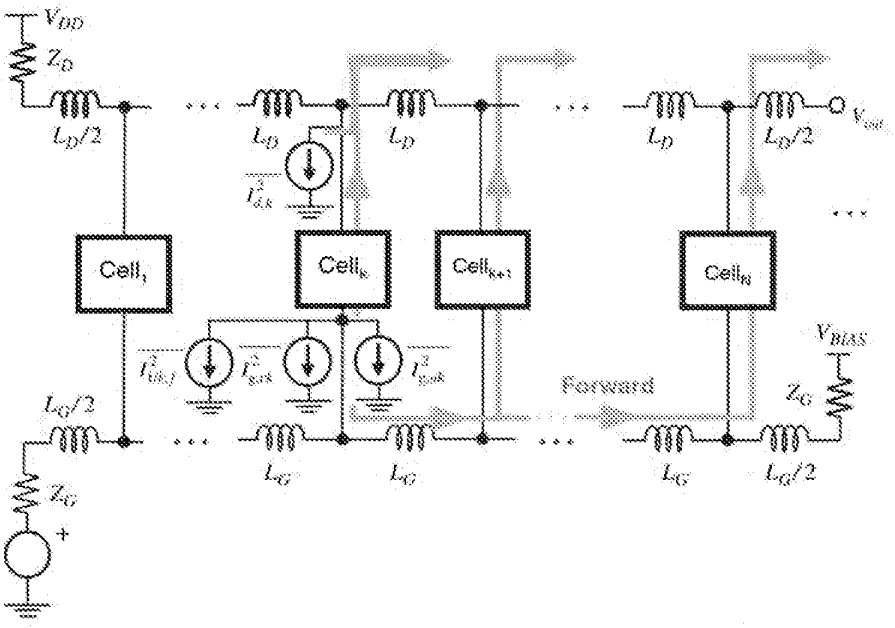


Fig. 3.9 Forward propagation of dominant device noise sources of the k-th cell of the DLNA

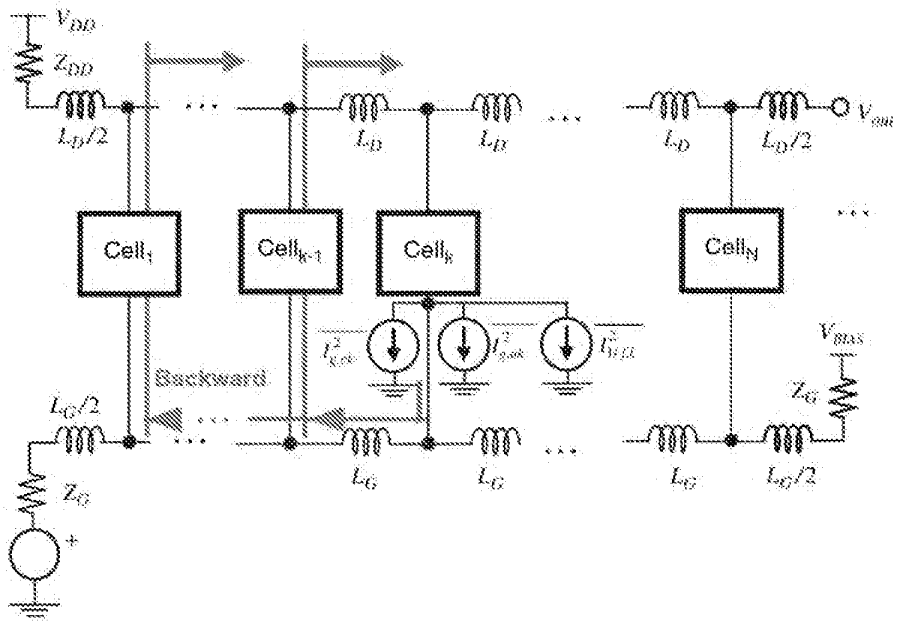


Fig. 3.10 Backward propagation of dominant MOSFET noise sources of the k-th cell of the DLNA

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$$I_{o,k}^{(B)}(\omega) = \frac{1}{2}\left[I_{g,c}(\omega) + I_{g,s}(\omega) + I_{1/f}(\omega)\right] H_g(\omega)\frac{\sin(k-1)\beta}{\sin\beta}e^{-j(N+1/2)\beta} \quad (3.13)$$

The Fourier transform of backward-propagated noise current, $I_{o,k}^{(B)}(\omega)$, reaches its peak when $\sin(k-1)\beta/\sin\beta = k-1$ for $\beta = l\pi$ and $l \in \mathbb{Z}$.

The time-domain noise current at the output, $i_{o,k}(t)$, defined as $i_{o,k}(t) = i_{o,k}^{(F)}(t) + i_{o,k}^{(B)}(t)$, due to MOSFET noise sources of the k-th stage is a random process, meaning that its Fourier transform is a random process itself. On the other hand, as pointed out in Section 3.4.1, the PSD of noise is not equal to the magnitude square of its Fourier transform. The PSD of noise $i_{o,k}(t)$ should therefore be obtained by taking the Fourier transform of its autocorrelation function, $\Phi_{o,k}(m)$, which is defined as:

$$\Phi_{o,k}(m) = \overline{i_{o,k}(t)i_{o,k}(t+m)} \quad (3.14)$$

where

$$\begin{aligned} i_{o,k}(t) = \frac{1}{2}\{&i_d(t) + (N-k+1)\left[i_g(t_1) + i_{1/f}(t_1)\right] * h_g(t_1) \\ &+ (k-1)\left[i_g(t_2) + i_{1/f}(t_2)\right] * h_g(t_2)\} \\ t_1 &= t - (N-k+0.5)\sqrt{LC}, \\ t_2 &= t - (N+0.5)\sqrt{LC}. \end{aligned} \quad (3.15)$$

The symbol $*$ in (3.15) denotes the convolution operation. $h_g(t)$ and $H_g(\omega)$ represent the impulse response and current-gain transfer function of each cell, respectively. After a certain amount of mathematical effort, the upper-bound of the autocorrelation is found using the following expression:

$$\begin{aligned} \Phi_{o,k}(m) = \frac{1}{4}\{&\overline{I_d^2}\delta(m) + \left[(N-k+1)^2 + (k-1)^2\right]\left(\overline{I_g^2} + \overline{I_{1/f}^2}\right) h_g(m) * h_g(-m) \\ &+ (N-k+1)[\Phi_{I_g,I_d}(m-t+t_1) * h_g(m-t+t_1) \\ &+ \Phi_{I_g,I_d}^*(t_1-t-m) * h_g(t_1-t-m)] \\ &+ (k-1)[\Phi_{I_g,I_d}(m-t+t_2) * h_g(m-t+t_2) \\ &+ \Phi_{I_g,I_d}^*(t_2-t-m) * h_g(t_2-t-m)]\} \end{aligned} \quad (3.16)$$

$\Phi_{I_g,I_d}(m)$ is the cross-correlation of stochastic processes $i_g(t)$ and $I_d(t)$ with power spectral density of $S_{I_g,I_d}(\omega)$. The channel thermal noise of transistor is a white noise process, implying that its autocorrelation is an impulse function $\overline{I_d^2}\delta(m)$ (see first term of (3.16)).

The PSD of the output noise current $S_{o,k}(\omega)$ due to the MOSFET noise sources of the k-th stage and all its forward- and backward-propagated replicas is obtained by taking Fourier transform of (3.16), which results in expression (3.17):

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$$S_{o,k}(\omega) = \frac{1}{4}\{\overline{I_d^2} + [(N-k+1)^2 + (k-1)^2]\left(\overline{I_g^2} + \overline{I_{1/f}^2}\right)|H_g(\omega)|^2 + 2(N-k+1)\mathrm{Re}[S_{I_g,I_d}(\omega)H_g(\omega)e^{-j\omega(t-t_0)}] + 2(k-1)\mathrm{Re}[S_{I_g,I_d}(\omega)H_g(\omega)e^{-j\omega(t-t_0)}]\} \quad (3.17)$$

where $Re[.]$ represents the real-part of a complex variable. The input and output capacitances of cascode cells have already been absorbed into the gate and drain TLs. Moreover, L_C has resonated out the effect of parasitic capacitances at the internal node of each cascode cell. Therefore, $H_g(\omega)$ is simplified to the DC current gain $g_m R_{GG}$ of each cell; where $g_m = g_{m,cs}$ and $R_{GG} = Z_G/2+r_{gate}/3[r_{gate}$ is the physical gate resistance]. The 1/3 factor in $r_{gate}/3$ is to model the distributed effect of gate resistance in MOS devices with large widths. The PSD of the output noise current due to the MOSFET noise sources of the k-th stage and all its forward- and backward-propagated replicas thus becomes:

$$S_{o,k}(\omega) = \frac{\overline{I_d^2}}{4}\{1 + [(N-k+1)^2 + (k-1)^2]\left|\frac{\kappa_c}{c}\right|^2(\omega\tau_{GS})^2 + 2N\kappa_c(\omega\tau_{GS})\} + \frac{\overline{I_{1/f}^2}}{4}g_m^2 R_{GG}^2[(N-k+1)^2 + (k-1)^2] \quad (3.18)$$

where $\kappa_c = |c|\sqrt{\delta\xi/\gamma}$($\gamma$ is the channel thermal-noise coefficient and is technology-dependent), $\tau_{GS} = R_{GG}C_{t,cs}$, and $\overline{I_{1/f}^2} = \overline{V_{1/f}^2}\Big/R_{GG}^2$ with $\overline{V_{1/f}^2}$ being the average power of flicker noise voltage [22].

Consequently, the overall PSD of the output noise current,$S_{I_o}^{MOS}(\omega)$, due to MOSFET noise sources is:

$$S_{I_o}^{MOS}(\omega) = \sum_{k=1}^{N} S_{o,k}(\omega) = \frac{\overline{I_d^2}}{4}\{N + \frac{N(2N^2+1)}{3}\left|\frac{\kappa_c}{c}\right|^2(\omega\tau_{GS})^2 + 2N^2\kappa_c(\omega\tau_{GS})\} + \frac{g_m^2\overline{V_{1/f}^2}}{4}\frac{N(2N^2+1)}{3} \quad (3.19)$$

3.4.3 Noise Contribution of Source and Load Impedances

Simple calculations reveal that the noise contributions of the source impedance $R_s = Z_G$, the gate-line termination Z_G, and the drain-line termination Z_D to the output are calculated as follows (see [19]):

$$\overline{V_{n,out}^2}\Big|_{Source\_impedance} = 4k_B T\frac{N^2 Z_G^2 Z_D g_m^2}{4} \quad (3.20)$$

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$$\overline{V_{n,out}^2}\Big|_{Gate\_termination} = 4k_BT\frac{Z_G^2 Z_D g_m^2}{4}\left(\frac{\sin N\beta}{\sin\beta}\right)^2 \tag{3.21}$$

$$\overline{V_{n,out}^2}\Big|_{Drain\_termination} = k_BTZ_D \tag{3.22}$$

3.4.4 Calculation and Optimization of the Overall NF

So far, noise contributions of various noise sources to the output noise power of the DLNA were calculated (cf., (3.19–3.22)). Substituting the results of (3.19–3.22) in the definition of the spot NF yields

$$NF_{lin} = NF_{HF} + \frac{1}{4k_BTZ_T}\cdot\frac{2\pi K_{1/f}}{C_{ox}WL\omega}\cdot\frac{2N^2+1}{3N} \tag{3.23}$$

where

$$NF_{HF} = 1 + \frac{1}{(Ng_mZ_T)^2} + \left(\frac{\sin N\beta}{N\sin\beta}\right)^2 + \frac{\gamma}{Ng_mZ_T}\left[1 + \frac{(2N^2+1)}{3}\left|\frac{\kappa_c}{C}\right|^2(\omega\tau_{GS})^2 + 2N\kappa_c(\omega\tau_{GS})\right] \tag{3.24}$$

and NF_{HF} denotes the high-frequency NF and $Z_T = Z_G = Z_D$.

The flicker noise corner frequency, f_{corner}, is simply determined by equating the mid-range frequency value of NF_{HF} with the low-frequency value of NF_{lin}, resulting in

$$f_{corner} = \frac{K_{1/f}}{C_{ox}WL}\cdot\frac{2N^2+1}{12}\cdot\frac{g_m}{k_BT}\left(\frac{1}{Ng_mZ_T} + \gamma\right) \tag{3.25}$$

where $K_{1/f}$ is the process dependent flicker noise constant with typical values less than $10^{-26}V^2F$ [22]. Equation (3.25) states that the flicker corner frequency increases in proportion with N^2.

Equations (3.23) and (3.24) provide us with interesting design guidelines regarding the distributed LNA circuit of Fig. 3.4. First, the second term of (3.24) is inversely proportional to the forward power-gain of the circuit, which will be significantly reduced by increasing the power gain and increasing the number of stages. The third term represents the contribution of the gate termination. When $N\beta$ is close to zero or π, this term adds an additional factor of one to the circuit's NF, setting the minimum NF to 3dB. However, for other values of $N\beta$, this term is less than unity and decreases with number of stages N. This notion actually implies that for $N\beta \neq l\pi$, $l \in Z$; the noise powers are superimposed at the output incoherently whereas the signal and its propagated replicas are added coherently. As a result, the

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contribution of the gate termination to the overall NF becomes inversely proportional to N^2, and can be made to be smaller than unity.

Both the second and the third terms are inversely proportional to N^2, which can be assumed to be negligible momentarily to simplify the calculations. Differentiating the circuit NF with respect to N yields

$$N_{opt} = \left\{ \frac{1}{2} \left[1 + \frac{3}{\frac{\gamma}{g_{m2}} \left(\left| \frac{g_m}{c} \right| \omega \tau_{GS} \right)^2 + \frac{1}{4kTR_T} \frac{2\pi K_{1/f}}{WLC_{ox}\omega}} \right] \right\}^{1/2} \tag{3.26}$$

As an approximation, the noise contribution of the flicker noise can be neglected, which simplifies (3.26) to

$$N_{opt} \approx \sqrt{\frac{1}{2} \left[1 + \frac{3}{(|\kappa_c/c|\omega\tau_{GS})^2} \right]} \tag{3.27}$$

The device sizes are to be calculated to maximize gain across the UWB frequency band. [23] presented contours of constant gain-bandwidth product as function of gate and drain TLs' attenuations without any consideration for the noise-figure minimization. The design guidelines presented in [8] and [23] to maximize the GBW are primarily based on calculation of optimum gate and drain attenuation factors without providing any quantitative discussion on the impact of number of stages N. In fact, [23] stated that for N greater than 4 the DA's frequency response does not change appreciably.

The design goal of this paper is to maximize the gain and minimize the NF across the UWB band. To achieve this goal, we introduce a design procedure based on the approach proposed in [23] with N being set to optimum number of stages N_{opt} from (3.22). The design optimization procedure utilizes the GBW expression obtained from (3.5) of [23] in terms of the −3dB bandwidth, i.e.,

$$A_0\omega_{-3dB} = 4K_A X_{-3dB}\omega_{max} \tag{3.28}$$

where

A_0 = DC gain
ω_{-3dB} = −3dB cutoff frequency of the amplifier (rad/sec)
ω_{max} = MOSFET's maximum frequency of oscillation (rad/sec)
$K_A = \sqrt{abe^{-b}}$
$a = N\frac{r_{out}C_{ox}}{3\sqrt{L_D C_{ox,g}}} = N\frac{r_{out}\sqrt{C_{ox}/L_G}}{3}; \quad b = N\frac{R_{o,cg}C_{ox}}{\sqrt{L_G C_{ox}}} = NR_{o,cg}\sqrt{C_{ox,g}/L_D}$
$X_{-3dB} = \omega_{-3dB}\sqrt{C_{ox}L_G} = \omega_{-3dB}\sqrt{C_{ox,g}L_D}$

where $R_{o,cg}$ denotes the output resistance of the common-gate stage in each cascode cell.

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To ensure a flat frequency response across the UWB bandwidth, the −3dB cut-off frequency is set to 13GHz. The factors K_A and X_{-3dB} are both functions of gate and drain line attenuations as demonstrated in [8] and [23]. The GBW for our application is several orders of magnitude smaller than ω_{max}, implying that the $K_A X_{-3dB}$ cannot exceed 0.25. For $N = 6$, [23] plotted the normalized gain-bandwidth contours and noticed that there is a single maximum at $a = 0.75$ and $b = 0.32$ and predicted a maximum value of 0.255. This value is about 2% greater than the expected value of 0.25, which is due to approximations used for attenuations of gate and drain TLs in equations used to derive X_{-3db} [23]. To investigate the effect of N on the maximum GBW, the normalized gain-bandwidth contours are simulated for the DLNA of Fig. 3.4 and with N varying from 3 to 6. Fig. 3.11 shows the simulation results.

Table 3.2 shows the $K_A X_{-3dB}$ factors for optimum values of a and b for a specific number of stages N, and compares those with the $K_A X_{-3dB}$ factors obtained for optimum a and b values when $N = 6$. This comparison shows a small sensitivity of the $K_A X_{-3dB}$ factor with respect to a and b values. Based on the assertion of [23] which was also confirmed by simulation data in Table 3.2, GBW will not change with N greater than 4. Therefore, a and b values for $N = 6$ are used. Procedure 1 summarizes the proposed approach for the performance-optimized DLA design.

Procedure 1.

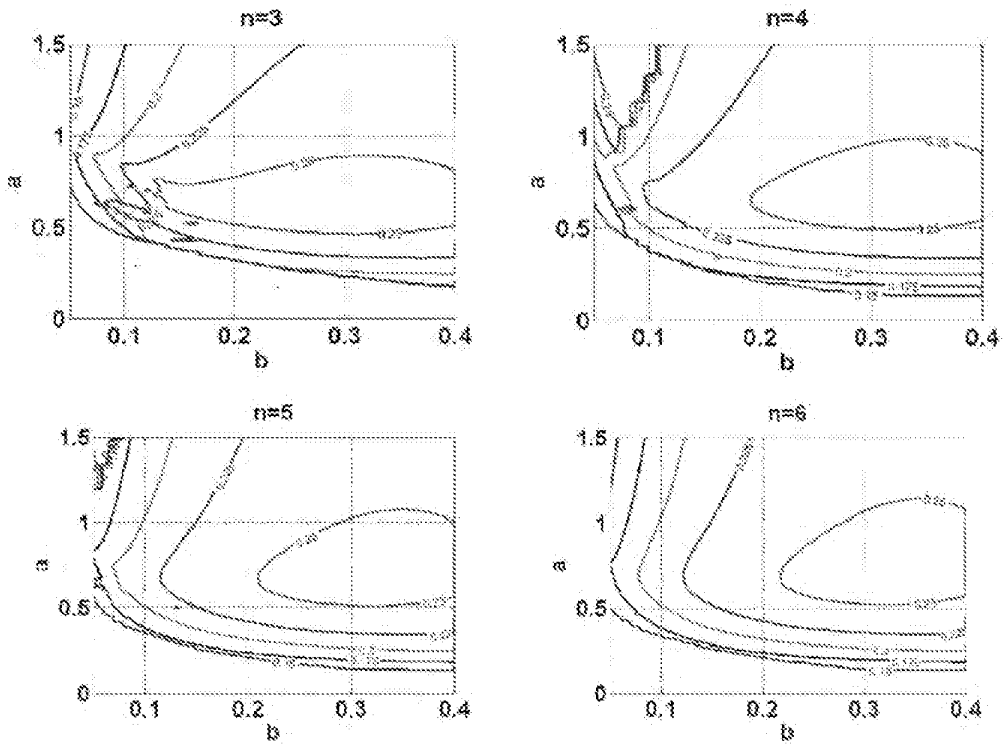


Fig. 3.11 Normalized gain-bandwidth contours for number of stages varying from $N = 3$ to $N = 6$

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Table 3.2 A comparison between the $K_g X_{-3dB,opt}$ for optimum a and b values and $K_g X_{-3dB}$ for a and b values when N=6 (a=0.75; b=0.32 for N=6)

	n = 3	n = 4	n = 5	n = 6
$K_g X_{-3dB}$	0.2570	0.2563	0.2558	0.2555
$K_g X_{-3dB,opt}$	0.2680	0.2568	0.2559	0.2555

1. For a flat magnitude response across the UWB band, set $f_{-3dB} = 13$GHz. The TLs' cutoff frequency, f_c, defined as: $f_c = 2/\left[2\pi\sqrt{L_G C_{i,cs}}\right] = 2/\left[2\pi\sqrt{L_D C_{o,cg}}\right]$ is calculated so as to ensure that $N\beta \neq l\pi$, $l \in Z$. To achieve maximum gain for frequencies up to the UWB upper corner frequency, we set $a = 0.75$ and $b = 0.32$. Moreover, $N = N_{opt}$, and N_{opt} is obtained by (3.26) for minimum NF.
2. The maximum bias current for which the MOS transistors of each cell remain in saturation is calculated for the bias circuit used in the DLNA of Fig. 3.4. This current is readily calculated as $I_{D,max} = V_{TH}/N_{opt} Z_T$.
3. Using (3.28), calculate the maximum DC gain, A_0.
4. Equation (3.6) in [23] gives the DC gain of a conventional distributed amplifier as

$$A_0 = \frac{g_m Z_T^2}{2} \frac{\sinh(b)}{\sinh(b/N_{opt})} e^{-b} \tag{3.29}$$

   This equation holds for the DLNA of Fig. 3.4 with identically matched transistors M_{ak2} and M_{ak1} for the each cascode cell. All the parameters in (3.29) are expressed with respect to gate aspect-ratio of transistors, W/L.
5. Using step 4, calculate the W/L. This W/L results in minimum NF and maximum gain.
6. Using (3.23)–(3.24), obtain minimum NF.

In calculating the NF and gain expression, the device data provided by the foundry have been used. In doing so, a test structure on the same 0.18mm SiGe technology was fabricated to experimentally characterize various individual components including the MOS transistors and varactors, transmission lines, short structures, open structures, and thru structures. Measurement of individual MOSFET transistors in the test structure provides the technology dependent parameters. Applying the design procedure 1 to the DLNA of Fig. 3.4, results in the optimum W/L-ratio of 240μm/0.18μm. Using (3.26), the optimum number of stages for 50 Ω load terminations will be readily calculated, once the optimum (W/L)-ratio is obtained. For the DLNA circuit of Fig. 3.4, $N_{opt} = 3$. To verify these calculations, the DLNA was designed and simulated is Cadence. Four performance-optimized DLNA circuits with number of stages varying from $N = 1$ to $N = 4$ were separately designed and simulated. To capture the gate-induced noise in simulations, the BMIS4 level 54 MOS model has been utilized. Figure 3.12 shows simulated noise-figure with respect to frequency. It shows that the three-stage DLNA achieves a minimum NF of 2.1 across the UWB spectral band. Section 3.4 will summarize measurement results of a three-stage DLNA prototype, which was designed and fabricated in a 0.18μm SiGe process.

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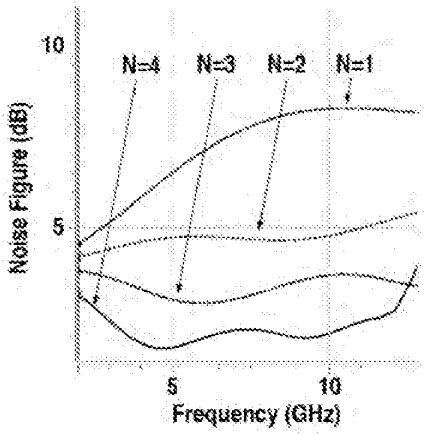


Fig. 3.12 The NF comparison for different number of stages

3.5 Linearity Analysis

A notch filter centered around the 802.11a 5GHz frequency enhances the spurious-free dynamic range (SFDR) of the DLNA. Nevertheless, the proposed UWB DLNA must remain linear when receiving the desired weak wideband signal in the presence of in-band narrowband interfering signals. An analytical study of the circuit's linearity and the 3rd-intercept point (IP3) provides useful insight about the circuit's large-signal performance.

To capture the short-channel effects of submicron CMOS technology including mobility degradation and velocity saturation, the analysis uses the well-known I-V characteristic of the submicron MOS transistor [22], i.e.,

$$I_D = s\frac{1}{2}\mu_0 C_{ox}\left(\frac{W}{L}\right)\frac{(V_{GS}-V_{TH})^2}{1+\left(\frac{\mu_0}{2v_{sat}L}+\theta\right)(V_{GS}-V_{TH})} \tag{3.30}$$

where μ_0 represents the low-field mobility, v_{sat} is the saturated drift velocity, and θ is the process dependent parameter [22]. Assuming the input DC bias voltage to be equal to the threshold voltage, the above equation is simplified to:

$$I_D \approx \frac{1}{2}\mu_0 C_{ox}\left(\frac{W}{L}\right)V_{in}^2\left[1-\eta\left(\frac{\mu_0}{2v_{sat}L}+\theta\right)V_{in}\right] \tag{3.31}$$

where η is a corrective factor ranging from 0.3 to 0.5 to improve the accuracy of the approximation. To estimate the intercept points we determine the DLNA output in response to the input sinusoidal voltage $V_{in}(t) = V_{im}\cos\omega_{in}t$, first. The signal at the near-end input terminal travels down the gate line, while being amplified by each cell once it arrives at that cell's input terminal. The amplified signal will then travel toward the load termination, while being combined with the signals at subsequent tap-points along the drain TL. The signal propagation mechanism is quantified using (3.32):

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$$V_o(t) = \sum_{k=1}^{N} V_{o,k}(t - (N-k+1/2)\sqrt{LC}) \tag{3.32}$$

$V_{o,k}$ is the signal amplified by the k-th stage $V_{o,k}(t) = I_{D,k}(t)Z_D/2$, is related to the input voltage using the I-V characteristic of each cascode cell.

$$V_o(t) = V_{im}\left(1 - \eta(\frac{\mu_0}{2v_{sat}L} + \theta)\frac{V_{im}^2}{4}\right)\cos\omega_{in}(t - N\sqrt{LC}) + \left(\eta(\frac{\mu_0}{2v_{sat}L} + \theta)\frac{V_{im}^3}{4}\right)\cos 3\omega_{in}(t - N\sqrt{LC}) \tag{3.33}$$

The input third-intercept point is thus obtained as

$$IIP_3 = 10\log\left[4 - \eta(\frac{\mu_0}{2v_{sat}L} + \theta)V_{im}^2\right] - 10\log\left[\frac{3}{4}\eta(\frac{\mu_0}{2v_{sat}L} + \theta)V_{im}^2\right] \tag{3.34}$$

Equaton (3.34) states that the IIP3 of the DLNA is equal to that of a lumped LNA that uses the same cascode cell.

3.6 Measurement Results

The UWB DLNA circuit of Fig. 3.4 was fabricated in a 0.18μm SiGe BiCMOS process while only MOS devices were utilized. Square spiral inductors were all fabricated on the top-most metal layer and exhibited a Q-factor of 10 at 10GHz. The LNA test-chip occupies a total area of 872μm × 872μm including the pad ring. The chip was directly mounted on a high-frequency board. Both input and output terminals of the proposed distributed LNA were terminated to on-chip square spiral inductors for matched termination. DC pads incorporate ESD protection. To minimize the parasitic effects of chip-board interface, the chip was solder bumped, and flipped on the board. Figure 3.13 shows the chip micrograph.

A test structure was separately fabricated in the same 0.18mm SiGe technology to experimentally characterize various individual passive and active components including transistors, MOS varactors, transmission lines, short structures, open structures, and thru structures. Of particular interest is characterization of noise parameters of the MOSFET, which was carried out by the foundry. The measured average values of γ, δ, and ζ are 2.21, 4.1, and 5.2, respectively. Calculations using the holistic thermal model developed in BSIM4 model results in $\gamma = 2.14$, $\delta = 3.94$, and $\zeta = 5$.

S-parameter measurements of the circuit were carried out using the Anritsu 37247A vector network analyzer (VNA). Gate biasing was provided by the bias-Tees. Figure 3.14 shows the measured s_{21} and NF of the DLNA under operating conditions of $V_{DD} = 1.8$V and the overall current consumption of 12mA. The DLNA exhibits a flat NF of 2.9dB across the entire 7.5GHz UWB frequency band. As

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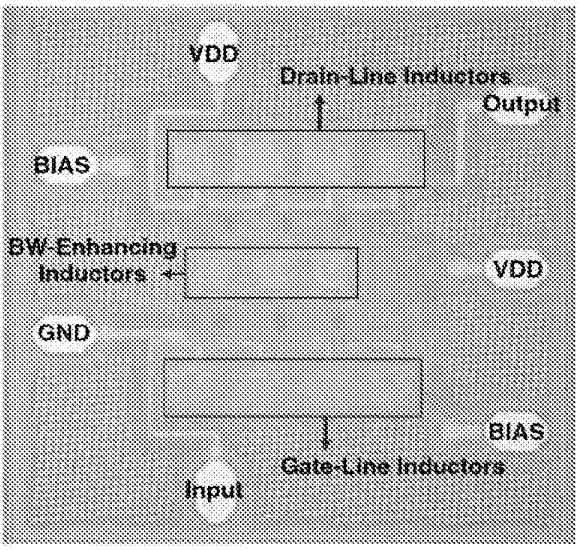


Fig. 3.13 Die photo of the UWB DLNA

explained in Section 3.4.4, at frequencies near or much lower than the lines' cutoff frequency, the far-end termination impedance at the gate load will add 3dB to the total NF, because the second term in (3.24) approaches its maximum value of one. For $N\beta \neq l\pi$, $l \in \mathbb{Z}$ the second term is less than unity and decreases with number of stages N, and the contribution of the gate termination to the overall NF becomes inversely proportional to N^2, and can be made to be smaller than unity. In our design, the gate line's inductance is chosen to be 942pH and the gate input capacitance is 277fF resulting in a line cut-off frequency of $2/[2\pi\sqrt{L_G C_G}] = 19.6$GHz. Consequently, the noise contribution of the gate load resistance becomes negligible. The measured forward gain of the LNA circuit remains at 8dB for frequencies up to 11GHz. It experiences a +1.6dB overshoot at 11.6GHz, as also indicated in Fig. 3.14.

Designing a performance-optimized DLNA with eleven inductors for a wideband frequency operation from 3.1- to 10.6-GHz demands careful layout development

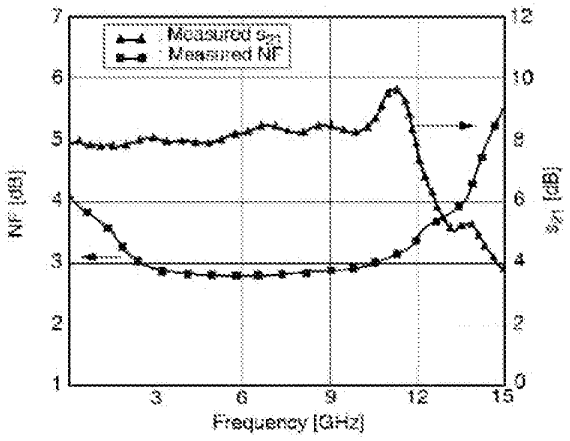


Fig. 3.14 Measured forward gain and noise figure

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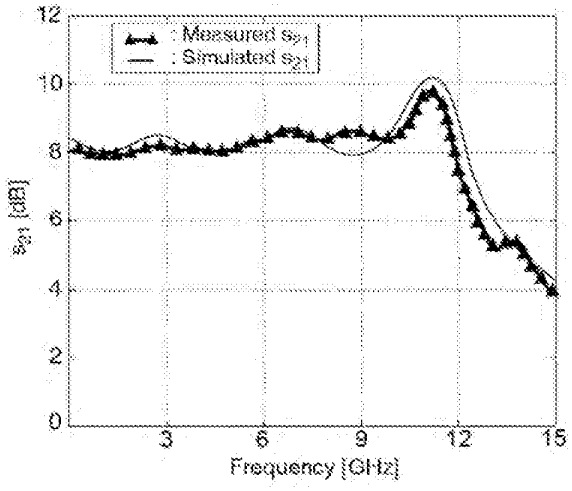


Fig. 3.15 Measured and simulated s_{21} vs. frequency

and post-layout extraction/simulation. Figure 3.15 demonstrate simulated and measured forward gain s_{21}, verifying the accuracy of post-layout simulation. Figure 3.16 compares the measured NF of the DLNA with Eq. (3.23). This comparison verifies an earlier analytical assessment in Section 3.3, which states that (3.23) sets an upper limit for the NF of the DLNA.

Figure 3.17 depicts the measured and simulated input and output return losses, s_{11} (dB) and s_{22} (dB). s_{11} and s_{22} remain below -12dB and -10dB, respectively, across the UWB frequency band. Post-layout simulation driven by electromagnetic extraction of the entire circuit layout allows an accurate simulation result that closely follows the chip measurement. Good return losses from measurement, once again, proves an essential attribute of DAs in exhibiting wideband input/output matching. Simulations predicted slightly better s_{11} and s_{22}. The discrepancy can be attributed to the off-chip flip-chip measurements.

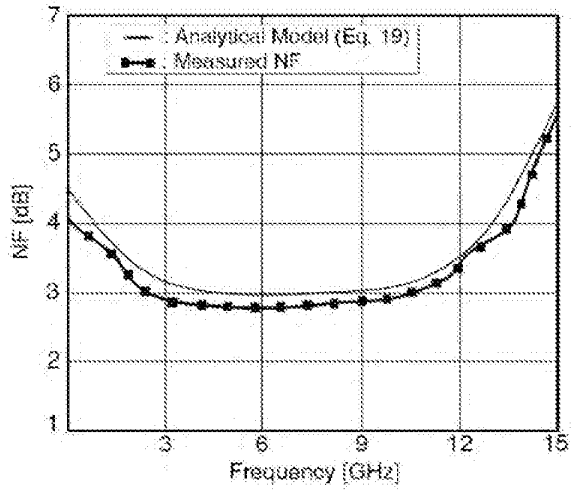


Fig. 3.16 Comparison between the measured NF and (3.23)

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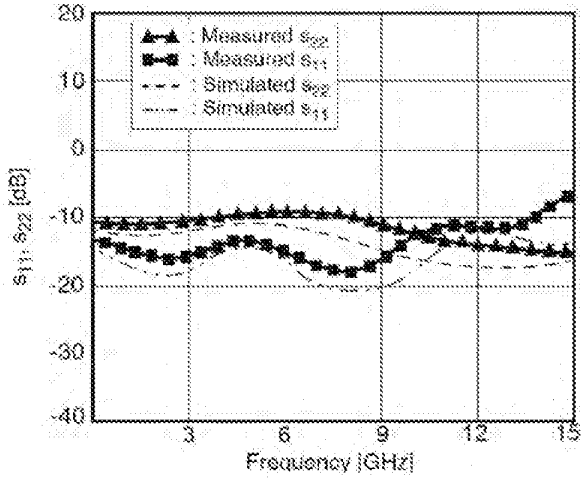


Fig. 3.17 Measured and simulated input and output return losses

Figure 3.18 shows plots of measured and simulated reverse isolation s_{12} (dB) and the LNA's gain s_{21} (dB) vs. frequency. The in-band isolation varies between −50dB and −27dB, which is verified by both simulation and measurement. Figure 3.18 demonstrates the accuracy of s_{12} and s_{21} simulations compared to measurement. The superior input-output isolation is partly due to the utilization of BW-enhanced cascode cells in the proposed DLNA.

The linearity and third-order intercept measurements were performed using the Agilent 8565 spectrum analyzer. The measured input-referred 1dB compression-point ($P_{in,1dB}$) at two input frequencies of 4GHz and 9GHz was −13.1dBm and −12.2dBm, respectively. The result from the two-tone test measurement at 7GHz is shown in Fig. 3.19. The DLNA exhibits an IIP3 of −3.4dBm and an OIP3 of 6.2dBm ay 7GHz frequency. Furthermore, the IP3 measurement was carried out for RF frequencies ranging from 3GHz to 10GHz. Table 3.3 summarizes the result of IP3 measurement, where the average IIP3 is −3.55dBm.

The proposed DLNA retains flat gain and input/output return losses, and relatively constant NF over a wide range of frequencies. It also contains a good linearity

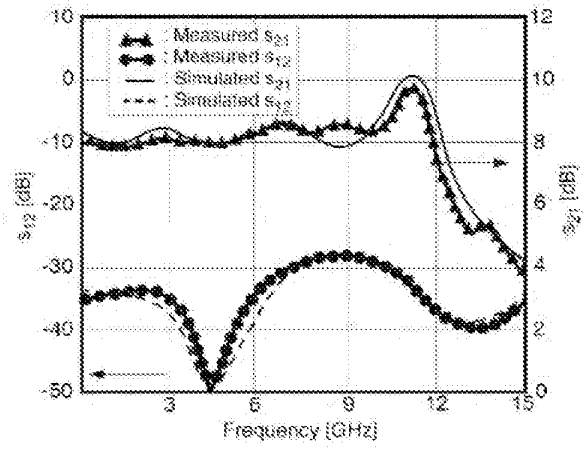


Fig. 3.18 Measured and simulated reverse isolation and gain

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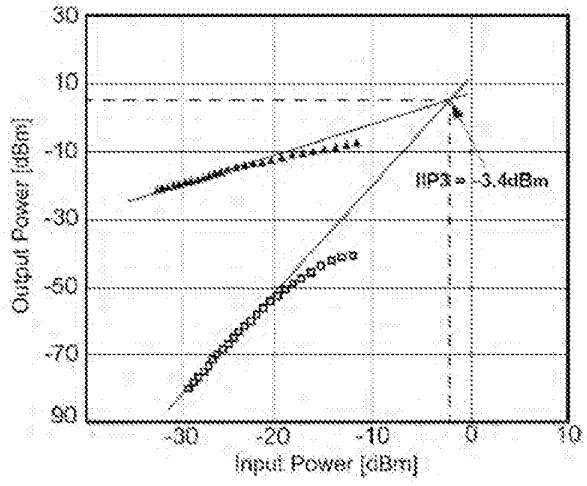


Fig. 3.19 Measured two-tone test at 7-GHz frequency

Table 3.3 Measured IIP3 of the DLNA with respect to frequency

f_{RF} [GHz]	IIP3 [dBm]
3	−4.1
4	−4.0
5	−3.8
6	−3.6
7	−3.4
8	−3.3
9	−3.2
10	−3.0

across the band. Table 3.4 compares the circuit performance of this LNA with some other recently published works.

3.7 Summary

This paper presented the analysis and design of a performance-optimized distributed LNA (DLNA) for UWB receivers. A detailed analysis of noise in the DLNA was provided, which can easily be extended to any other DA topology. A three-stage DLNA using bandwidth-enhancing inductors was fabricated in a 0.18μm SiGe BiCMOS process, where only MOS transistors were used. Measurements of the DLNA show a 2.9dB noise-figure and a forward gain of 8dB over the 7.5GHz UWB bandwidth. The circuit exhibits an average IIP3 of −3.55dBm and an input-referred 1-dB compression point of at least −13.1dB. The overall current consumption is 12mA from a 1.8 supply voltage.

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Table 3.4 Performance comparison of LNA circuits presented in prior work, and the proposed DLNA

Ref	BW (GHz)	s21 (dB)	NF (dB)	s11 (dB)	IIP3 (dBm)	Power (mW)	Topology	Technology
[6]	3–10	9.3	4–8	< −9.9	−6.7	9	Lumped CMOS Cascode	0.18μm CMOS
[7]	3–10	21	2.5–4.2	−14 < s11 < −9	> −3.5	30	Lumped Bipolar Cascode	SiGe BiCMOS, using bipolar
[5]	1.3–12.3	8.2	4.4–5.3	< −7.2	7.6–8.3	4.5	Lumped Differential Common-Gate	0.18μm CMOS
[9]	3dB, ~6GHz	6.5	N/A	< −9	N/A	52	CMOS Distributed Common-Source	0.18μm CMOS
[10]	0.5–4	6.5±1.2	5.4–8	< −6dB	N/A	83.4	CMOS Distributed Common-Source	0.6μm standard CMOS
[24]	0.04–6.2	8 ± 0.6	4.2–6.2	< −16	3	9	CMOS Distributed Cascode	0.18μm CMOS
[16]	0.1–23	14.5 ± 0.9	5	< −9	−0.5	54	Bipolar Distributed Cascode	SiGe BiCMOS Used bipolar
[18]	1–25	7.8 ± 1.3	4.8–7	< −10	4.7	54	CMOS Downsized Distributed	0.18μm SiGe, only CMOS
[23]	0.5–14	10.6dB	3.4–5.4	< −10	10 @ 10GHz	52	CMOS Distributed Cascode	0.18μm CMOS
[26]	3.5–4.5	16dB	3.9–4.2	< −10	−4.5	7.2	Differential LNA w/ Resistive-feedback	0.18μm CMOS
[27]	0.5–10	13	2.9–3.3	< −7	−7.5	9.6	Bipolar Common-Emitter w/ Resistive feedback	0.18μm SiGe Used bipolar
[28]	0–11GHz	10 (high-gain)	3.2–6	< −20	N/A	100	CMOS Distributed Cascode	0.18μm CMOS
[29]	3.1–10.6	10.87–12.02	4.7–5.6	< −11	< −10.6	10.57	Lumped CMOS LNA w/ Dual feedback	0.18μm CMOS
This Work	0.1–11	8	2.9dB *flat*	< −12	−3.55	21.6	Performance-Optimized CMOS Distributed Cascode with BW-Enhancing Inductor	0.18μm SiGe, only CMOS

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Chapter 4
Distributed RF Front-End

The use of distributed topology perfectly lends itself to wideband operation due to its intrinsic wideband matching characteristics.

In a UWB RF front-end (particularly, the one used in an IF transceiver architecture), all building blocks including LNA and downconversion mixers need to provide wideband characteristics. Using a distributed LNA and a distributed mixer is an inefficient approach from both power and area point of view. This chapter presents the design of a new UWB distributed RF front-end, called UWB-DRF, to address the high power dissipation and large area occupation issues of distributed circuits. The proposed UWB-DRF is comprised of *composite cells* distributed along the (artificial or actual) transmission lines (TLs). Each composite cell constitutes a merged low-noise transconductance amplifier (LNTA) and mixer to save the chip area and lower the overall power dissipation of the UWB-DRF. Each composite cell, therefore, combines the linear operation of the accompanying LNTA and the non-linear operation of the current commuting mixer. The UWB-DRF is particularly suitable for zero/low-IF dual conversion receiver (RX) architectures.

The chapter is organized as follows: Section 4.1 gives an overview of the UWB zero/low-IF dual-conversion receiver architecture. Section 4.2 discusses the operation principle of the proposed UWB-DRF. Section 4.3 includes experimental results of a three-stage UWB-DRF prototype fabricated in a 0.13 μm CMOS process. Finally, summary remarks are provided in Section 4.4.

4.1 UWB Zero/Low IF Dual Conversion Receivers

The block diagram of a UWB zero/low IF dual-conversion receiver is shown in Fig. 4.1.

A pre-select filter after the antenna rejects the out-of-band interferences and also out-of-band image frequencies. After being amplified by an UWB LNA, the RF signal is downconverted to the IF band of 2 GHz or less using the first downconversion mixer. The in-band image frequency will be filtered out using the second downconversion stage realized by Weaver-type image-reject architecture in companion with the digital section. The IF signal is then downconverted to zero/low IF using

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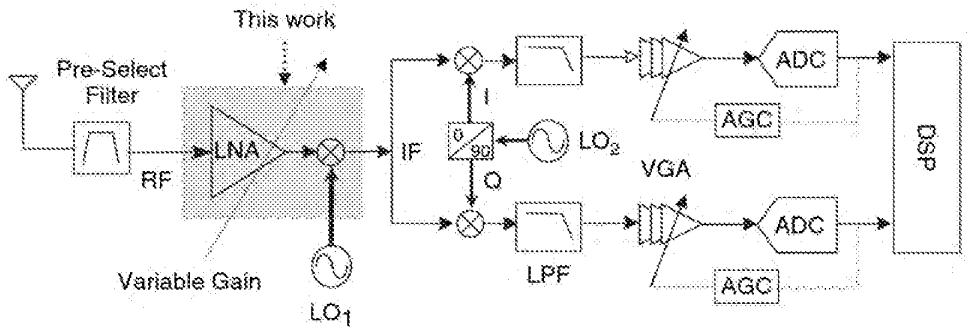


Fig. 4.1 UWB zero/low IF dual-conversion receiver architecture

complex I/Q mixers. The I/Q signals are then passed through low-pass filters (LPF), and variable gain amplifiers (VGA) whose gain is controlled by automatic gain control (AGC) circuitry to set the appropriate signal level for analog-to-digital converter (ADC). Finally, the digital signal processing (DSP) deals with the demodulation and baseband processing of the UWB signal.

The advantage of the dual conversion receiver for UWB application is that they only need quadrature LO signals at 2 GHz or less for the second downconversion mixers. The first LO signal over the multi-GHz spectrum is only single phase, not a quadrature. But in a direct conversion UWB quadrature LO signals should be provided over the entire wide spectrum of 7.5 GHz.

4.2 UWB-DRF

Shown in Fig. 4.2 is the system architecture of the UWB-DRF, where the LNTA and the first downconversion mixer are combined into one cell, and are distributed along TLs.

The UWB-DRF provides wideband matching characteristics at RF, LO, and IF ports. The IF can be any value in the 0.25–2 GHz frequency range. The unique features of the UWB-DRF of Fig. 4.2 are as follows:

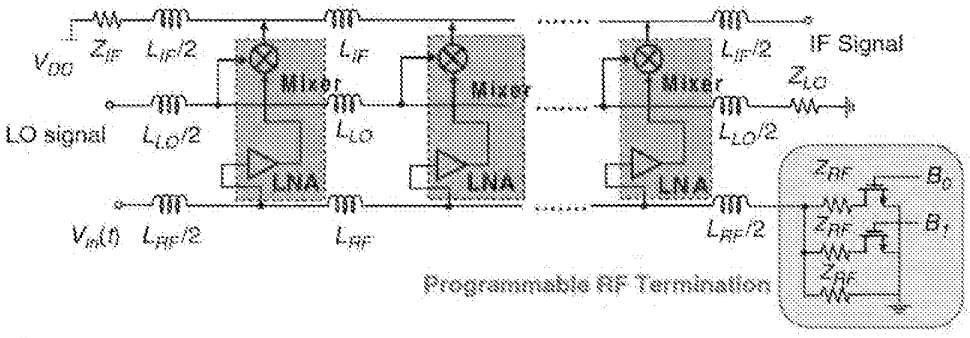


Fig. 4.2 Proposed UWB distributed RF front-end (UWB-DRF) with merged LNTA-mixer cells

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1. Wideband matching at RF, LO, IF ports.
2. Good linearity, flat gain, and small NF across a wide range of frequencies.
3. Re-using the bias current in LNTA/mixer cells to reduce the power consumption of the distributed RF front-end.
4. Provision of programmable matching network to achieve better performance (see control bits of B_0 and B_1 in Fig. 4.2).

Wideband RF, LO, and IF ports provide a needed freedom to choose appropriate frequencies for the LO_1 and LO_2 in the dual conversion receiver of Fig. 4.2. This unique attribute may lead to even smaller number of synthesized LO frequencies and a less complex frequency synthesizer in the receiver.

As mentioned earlier in the introduction, cascading the distributed LNA presented in [1, 2] and a distributed mixer presented in [3] may provide a wideband characteristic at all ports. Nevertheless, it will be an inefficient solution from power consumption and chip area perspectives. The UWB-DRF with distributed composite cells re-use the DC bias currents and share the input wideband TL, thereby significantly lowering the power consumption and saving chip area. In addition, the composite cell exhibits higher linearity, due to elimination of the high-swing node at the output of the LNA and input of the mixer in conventional cascaded LNA and mixer circuits [4].

4.2.1 Composite LNTA/Mixer Cell

The composite cell of merged LNTA/mixer is shown in Fig. 4.3(a). While the input and output parasitic capacitances of each cell are absorbed into the RF and IF TLs, respectively, the large capacitance at the common-source node of each composite cell is not, resulting in roll-off of the circuit's frequency response.

To alleviate this problem an inductor in series with the output of the current-mode LNA is added to reduce the effective capacitance at the common-source

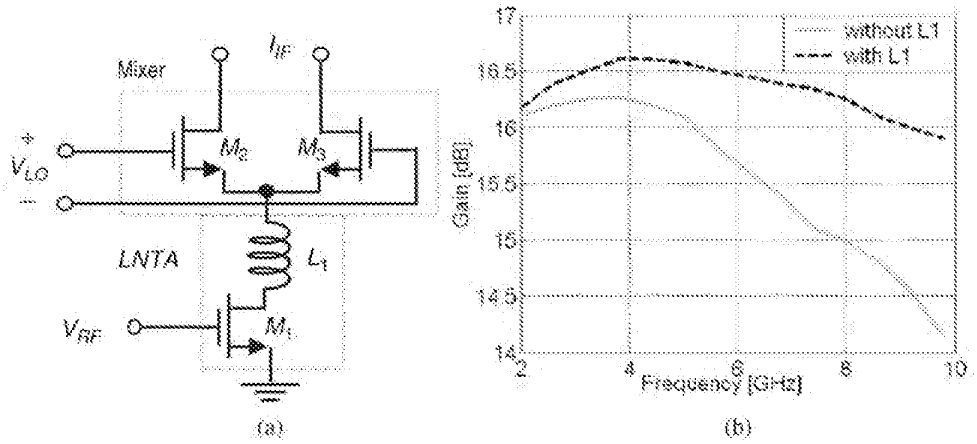


Fig. 4.3 (a) Composite cell, Merged LNA and Mixer, plus the inter-stage inductor (L_1) (b) Simulation results of the UWB-DRF with and without L_1

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node, thereby flattening the UWB-DRF's gain across wide range of frequencies (Fig. 4.3(b)). Moreover, inductor L_f avoids the rise of input-referred noise at higher frequencies [1].

4.2.2 Programmable Input RF TL Termination

The overall voltage-gain of the RX is expressed as [5]

$$\text{Gain} = (1 + \Gamma_L) \times A_v \tag{4.1}$$

where A_V is the front-end's voltage-gain and Γ_L is the reflection coefficient of the RX's input matching network. In a power matched RX, $\Gamma_L = 0$, and the overall gain becomes A_V. The other extreme case represents a power un-matched RX, where $\Gamma_L = 1$ and the total voltage gain of the RX will increase by 6 dB. However, zero power is transferred from the antenna. The 6 dB gain boosting due to input mismatch is a noiseless gain, which means that the noise contribution from the circuit remains unchanged. This implies that the NF will improve by 6 dB as well. Consequently, introducing few decibels of mismatch at the input matching network of the front-end improves the RX's voltage gain and NF. To implement such a variable matching network at the input, the termination resistance of the input RF TL is set to be digitally controlled by two bits of B_0 and B_1 (cf. Fig. (4.1)) in order to achieve variable resistances of Z_{RF}, $Z_{RF}/2$ and $Z_{RF}/3$ (Z_{RF}=150 Ω). Measurement results in Section 4.4 demonstrate a gain increase of 2.2 dB and NF improvement of 1.7 dB for the largest change of the input RF TL termination bits from "11" to "00", while preserving the input return loss (s_{11}) to better than −7.5 dB (i.e., a voltage standing wave ratio "VSWR" of better than 2.45) across the UWB band.

4.2.3 Conversion Gain Calculation

To calculate the conversion gain of the proposed UWB-DRF, a study of signal propagation along the TLs, and nonlinear mixing operation taking place at each cell is provided in this section.

The RF input signal experiences a delay of $(k - 0.5) \times t_{RF}$ along the RF TL to arrive at the kth stage of the distributed RX, which is then converted to current through the LNTA g_m-cell and is mixed with the delayed version of the LO input by the switching pair of the composite cell. The differential IF component of the kth stage's output current flowing toward the load is expressed as:

$$I_{o,k}(t) = \frac{1}{2} g_m V_{RF} \sin\left(\omega_{RF}(t - (k - \frac{1}{2})t_{RF})\right) p_1\left(\omega_{LO}(t - (k - \frac{1}{2})t_{LO})\right) \tag{4.2}$$

where g_m is the small-signal transconductance of the LNTA's tail current transistor, V_{RF} is the input signal amplitude. The 1/2 coefficient comes from the fact that half

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of the IF current travels forward to the load, and the other half travels backward to the IF TL termination. t_{RF} and t_{LO} are the delay of each LC section of RF and LO TLs, respectively. $p_1(t)$ is a periodic waveform with a fundamental component of ω_{LO}, and represents the instantaneous current gain of the switching pair from RF current to differential output IF current. $p_1(t)$ is expressed in terms of the instantaneous g_{m1} and g_{m2} [6]:

$$p_1(t) = \frac{g_{m1}(t) - g_{m2}(t)}{g_{m1}(t) + g_{m2}(t)} \tag{4.3}$$

Assuming sufficiently large LO amplitude and negligible LO TL's loss, the first harmonic of $p_1(t)$ is, $p_{11} \cong 2/\pi$.

The forward IF component of the kth stage experiences another delay of $(n - k + 0.5) \times t_{IF}$ along IF TL to reach to the output load. Therefore, the total output current written in *phasor* domain, neglecting inductor losses, is:

$$I_o = \frac{1}{\pi} g_{mRF} V_{RF} \sum_{k=1}^{n} 1\angle[(\omega_{LO}t_{LO} - \omega_{RF}t_{RF})(k - 0.5) - \omega_{IF}t_{IF}(n - k + 0.5)] \tag{4.4}$$

To maximize the conversion gain, all the current phasors from all n distributed composite cells should arrive at the output with the same phase to add up constructively. Therefore, the argument of (4.4) should be independent of k. This implies that

$$\omega_{RF}t_{RF} - \omega_{LO}t_{LO} = \omega_{IF}t_{IF} \tag{4.5}$$

One simple ***wide-band*** solution to (4.4) is to choose the delay of LC sections of RF, LO, and IF TLs to be equal, which readily results in the conspicuous relationship between the RF, LO, and IF frequencies (i.e., $\omega_{RF} - \omega_{LO} = \omega_{IF}$). Neglecting inductor losses, it is proved that the maximum conversion gain, $G_{c,max}$, is:

$$G_{c,max} = \frac{n}{\pi} g_{mRF} Z_{IF} \tag{4.6}$$

The nominal 50 Ω output termination results in an inadequate gain of approximately 8 dB, as also demonstrated in [7, 1]. $G_{c,max}$ is boosted by increasing either the number of stages, n, or the LNTA's transconductance, g_{mRF}, both of which leading to additional power consumption. Another solution is to increase Z_{IF}, while preserving the cut-off frequency of the IF TL, $\omega_{cut-off} = 2/\sqrt{L_{IF}C_{IF}}$, to sustain the criterion (4.5). However, increasing characteristic impedance of the IF TL, $Z_D = \sqrt{L_{IF}/C_{IF}}$, while keeping $\omega_{cut-off}$ constant, leads to excessively large values of inductors. On the other hand, increasing Z_{IF}, while retaining $\omega_{cut-off}$ and Z_D, results in larger passband ripples. The ripple is roughly equal to gain boosting factor of 20 $\log(Z_{IF}/Z_D)$ compared to the matched load, $Z_{IF} = Z_D$. Fig. 4.4 shows the IF TL's equivalent circuit, where i_2 to i_n are delayed versions of i_1.

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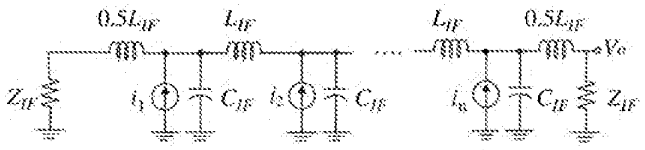


Fig. 4.4 IF transmission line equivalent circuit

At substantially lower frequency than $\omega_{cut-off}$, the inductors L_{IF} have negligible impedances. The circuit is thus simplified to a parallel combination of nC_{IF} and $Z_{IF}/2$. Therefore, the first roll-off of the conversion gain's ripple, ω_{ripple}, takes place at:

$$\omega_{ripple} = \frac{2}{nZ_{IF}C_D} = \frac{Z_D}{Z_{IF}}\frac{\omega_{cut-off}}{n} \tag{4.7}$$

Equation (4.7) states that the gain flatness of the IF TL is traded with the extra gain of the whole RF front-end, as also the simulation result of the circuit of Fig. 4.4, for n=3 is shown in Fig. 4.5.

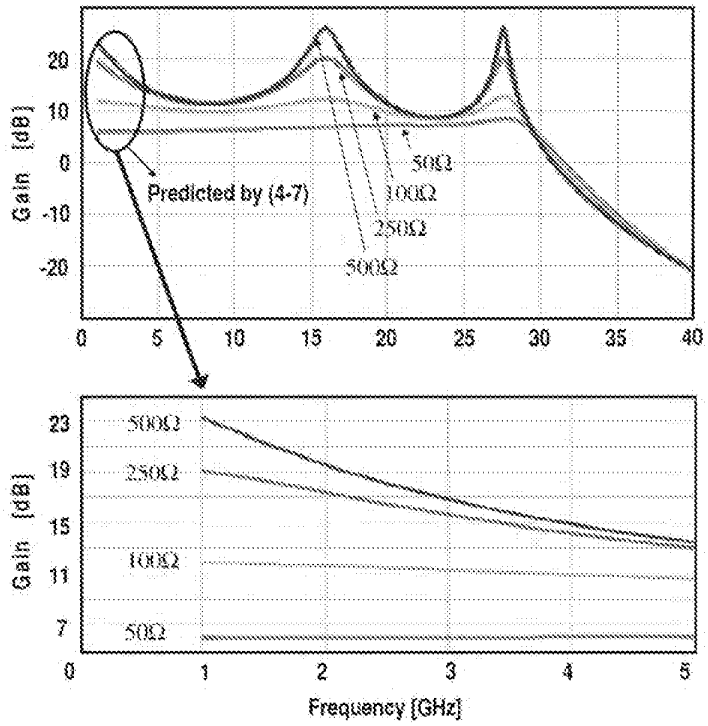


Fig. 4.5 Frequency response of IF TL for different values of Z_{IF}, with fixed $\omega_{cut-off}$

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4.3 Experimental Results

A 3-stage UWB-DRF incorporating composite LNTA/mixer cells along the artificial TLs, shown in Fig. 4.2, was fabricated in a 0.13 μm CMOS process. Fig. 4.6 shows the die micro-photograph of the UWB-DRF. To mitigate high-frequency signal integrity effects, the circuit was laid out carefully to retain symmetry. More precisely, the single-ended RF TL was laid out to be equidistant from LO and IF TLs. Furthermore, the differential LO and IF TLs were placed on both sides of the RF TL. The chip area is 1.5×1 mm.

The s-parameters of the proposed UWB-DRF for different values of the RF TL termination bits (B_0B_1) were measured on wafer using Agilent N5230A network analyzer. Fig. 4.7 shows the s-parameter measurement results. The UWB-DRF shows input return losses of the LO and RF input ports much better than -10 dB across

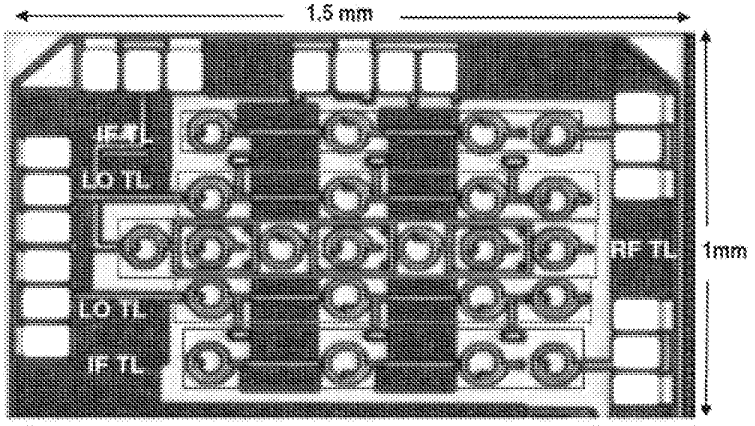


Fig. 4.6 The die photo of the proposed UWB DRF

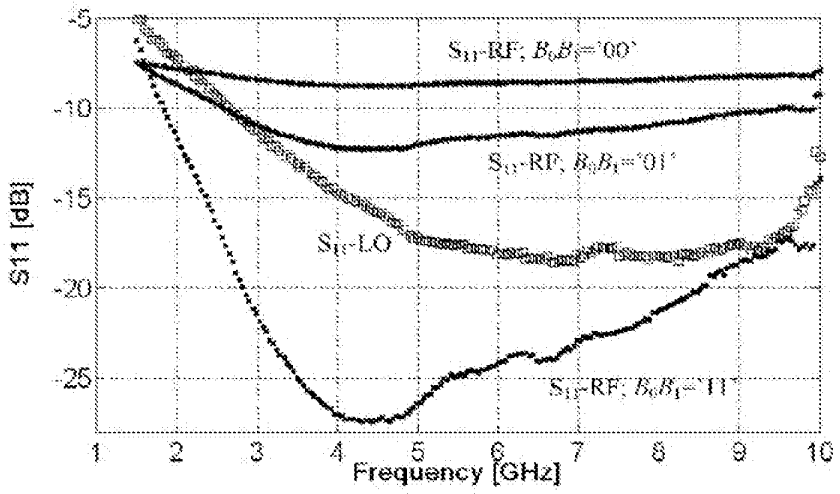


Fig. 4.7 Measured S-parameters

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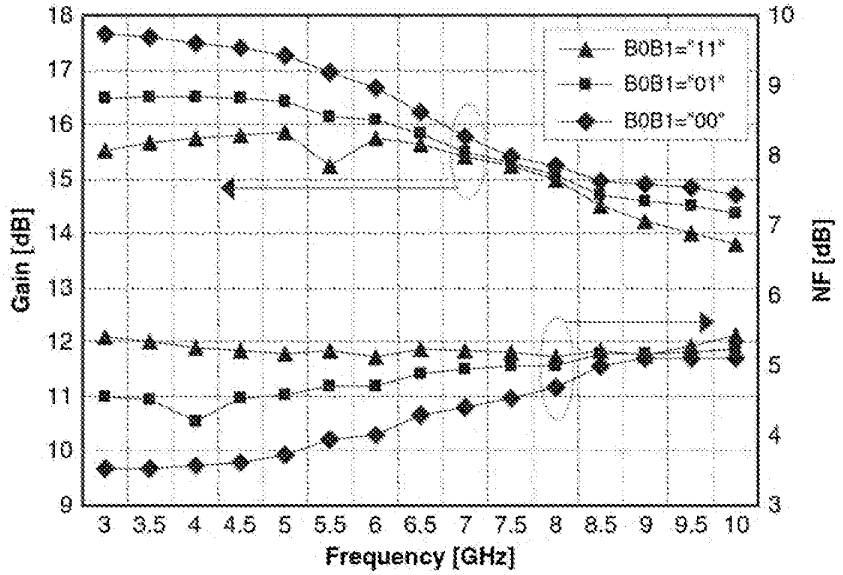


Fig. 4.8 Measured conversion gain and NF of UWB-DRF

the UWB frequency band for the 50 Ω matching case (i.e., B_0B_1="11"). The gain and NF were measured over a wide range of frequencies for different codewords (B_0B_1) of the RF TL termination. Figures 4.7 and 4.8 demonstrate that few decibels of mismatch at the input (B_0B_1="01" or "00") results in almost 2.2 dB increase in conversion gain and 1.7 dB improvement of the front-end NF. This is due to the existence of noiseless gain at the input matching network. The NF and gain were measured for an IF value of 500 MHz. The gain variation of the UWB-DRF (with RF TL of 50 Ω) was measured for different IF values, and for two input RF frequencies of 3 and 10 GHz, as shown in Fig. 4.9, which also exhibits almost flat conversion gain characteristics over the IF bandwidth. Figure 4.10 depicts the measured variable gain of the UWB-DRF, controlled by the common-mode voltage of the switching pair transistors. Lowering the common-mode voltage keeps the tail

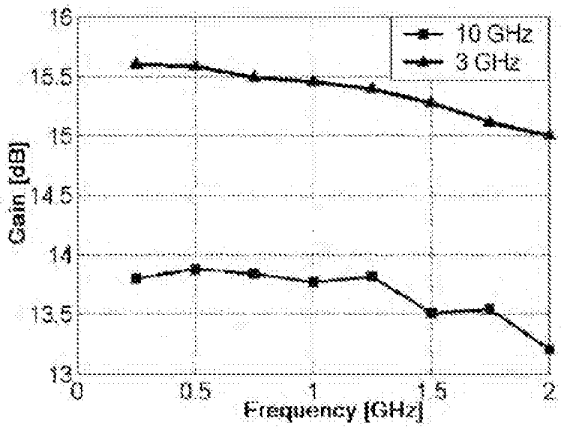


Fig. 4.9 Measured gain for different *IF* and for f_{RF}=3 and 10 GHz with *RF TL* termination of 50 Ω (B_0B_1="11")

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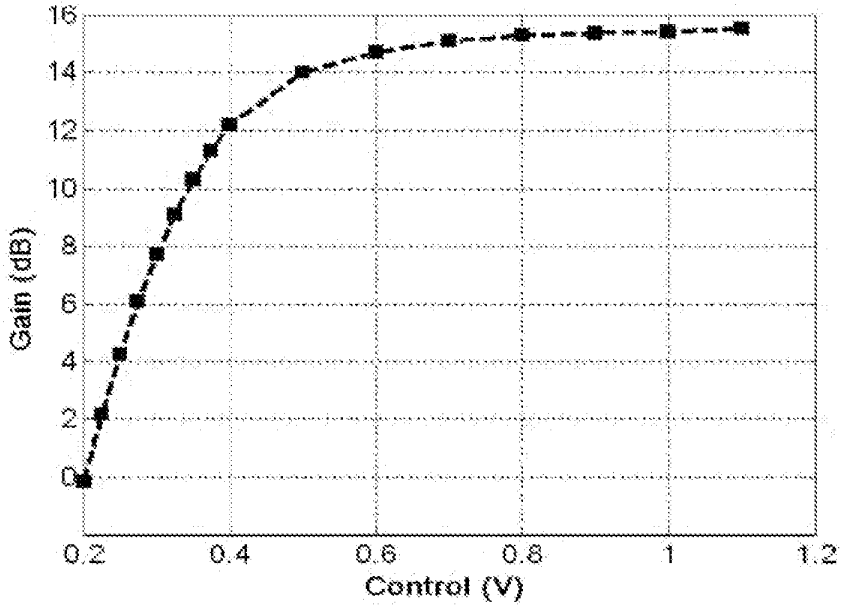


Fig. 4.10 Measured variable gain of UWBDRF for f_{RF} = 3 GHz; f_{IF} = 500 MHz; RF TL Termination of 50 Ω (B_0B_1="11")

current in triode region, thereby decreasing its g_m, and hence, decreasing the gain. Meanwhile, the input capacitance of the tail LNTA varies slightly, therefore, input matching is preserved. The measured IIP3 varies from −6.6 to −4.2 dBm for the input frequencies of 3–10 GHz, verifying a wideband linearity of the UWB-DRF. The measured IIP3 obtained from two-tone tests at frequency pairs of f_{RF}=(3 & 3.01 GHz), (7 & 7.01 GHz), and (10 & 10.01 GHz) for RF TL termination of 50 Ω (B_0B_1="11") is shown in Fig. 4.11(a–c).

Table 4.1 summarizes the measured performance of the UWB-DRF in the power matched case when the RF TL termination is of 50 Ω or (B_0B_1="11") for the entire bandwidth of UWB frequency range.

Table 4.2 compares the UWB-DRF's performance with possible RF TL termination (B_0B_1="11" , "10", and "00", i.e., 50, 75, and 150 Ω, respectively) with two previously published works [8, 9]. The UWB-DRF achieves flatter NF for the *entire* UWB frequency range in the power matched case (B_0B_1="00").

4.4 Summary

This chapter presented a novel distributed RF front-end for UWB receivers (UWB-DRF). A three-stage UWB-DRF incorporating composite LNTA/mixer cells along artificial TLs with controllable gain and programmable input matching network was fabricated in 0.13 μm CMOS process. Measurements of the circuit showed a 3.5–5.4 dB *NF* and a conversion gain of 17.7–13.8 dB over the UWB bandwidth.

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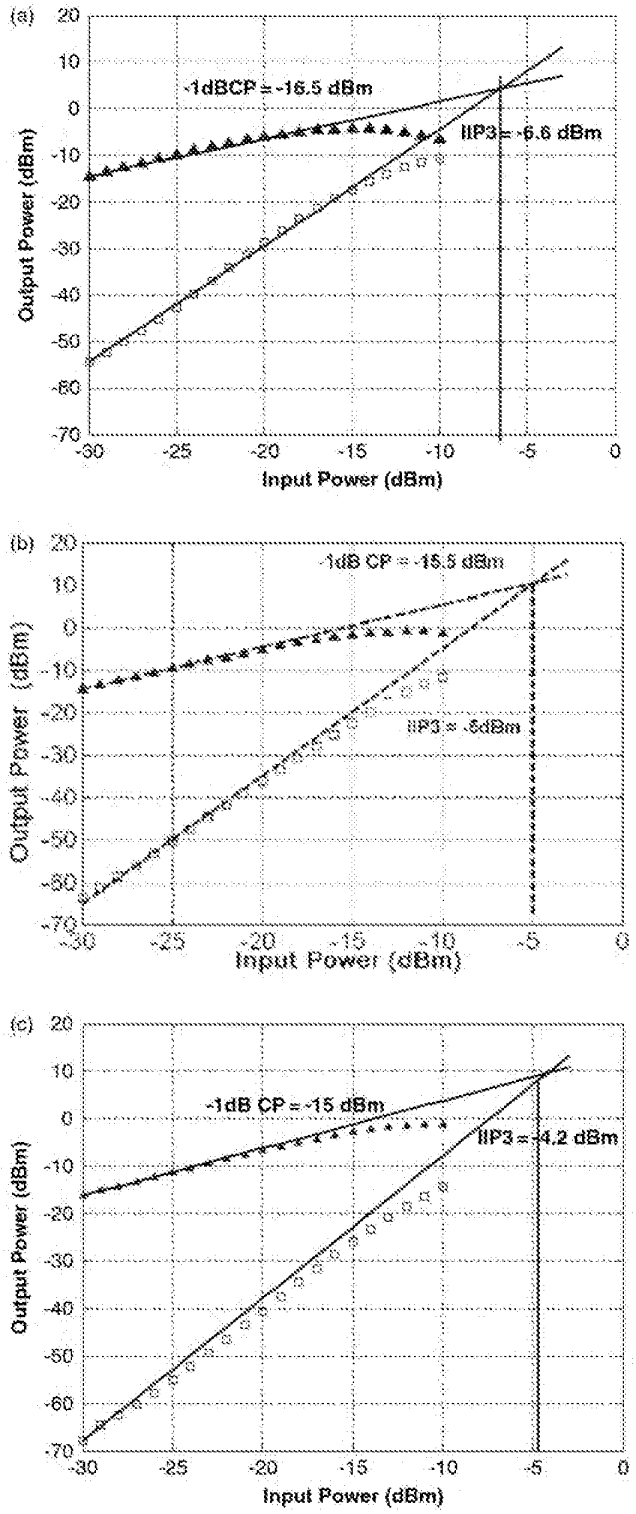


Fig. 4.11 IIP3 measurements: two tone test, f_{BB} = 500 MHz; RF TL Termination = 50 Ω (B_0B_1="11"), high gain mode for (a) f_{RF} = 3 & 3.01 GHz , (b) f_{RF} = 7 & 7.01 GHz, and (c) f_{RF} = 10 & 10.01 GHz

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Table 4.1 Measured summary of the UWB-DRF for RF TL = 50 Ω

f_{RF} [GHz]	3	4	5	6	7	8	9	10
Gain [dB]	15.5	15.8	15.8	15.8	15.4	15	14.2	13.8
NF [dB]	5.4	5.3	5.2	5.1	5.2	5.1	5.2	5.4
IIP3 [dBm]	−6.6	−6.3	−5.9	−5.4	−5	−4.9	−4.5	−4.2

Table 4.2 Performance comparison of UWB-DRF

Reference	Freq. range (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Technology
[9]	3–5	69–73	6.5–8.4	> −17.5	105 (w/ TX)	0.13μm CMOS
[8]	3–8	51–52	3.3–4.1	> −4.5	237.6 (w/ Synthesizer)	SiGe BiCMOS, using bipolar
This Work						
B_0B_1="11"		15.5–13.8	5.2–5.4	> −6.6	14.8	0.13μm CMOS
B_0B_1="10"	3–10.5	16.5–14.4	4.5–5.2	> −7		
B_0B_1="00"		17.7–14.7	3.5–5.1	> −7.5		

The circuit exhibited an average IIP3 of −5 dBm. The UWB-DRF circuit showed wideband performance at the RF, LO, and IF ports. The current consumption was 8.2 mA from a 1.8 V supply voltage.

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Chapter 5
Distributed RF Front-End for UWB Direct Conversion Receiver

Rigorous demand for low-power/low-noise operation and high-level of integration in UWB systems strongly suggests the use of direct conversion architectures. This chapter extends the concept of distributed circuits to design a ***current-equalized minimal-area distributed direct conversion RF front-end***, called DDC-RF, for UWB systems. RF front-end for such receiver, whose block diagram is depicted in Fig. 5.1, must exhibit wideband characteristic while addressing most important issues in any distributed circuit, namely high power dissipation, large area, and most importantly, the existing delay and loss from one tap-node of the constituent TL to the next, which translates to in phase and quadrature (IQ) phase and gain imbalances in the direct conversion receiver of Fig. 5.1.

This chapter is organized as follows: Section 5.1 describes the operation principle of the proposed DDC-RF. Section 5.2 describes the current equalization technique to remove IQ gain/phase imbalances. Section 5.3 includes measurement results of the DDC-RF prototype fabricated in 0.13 μm CMOS process. Finally, concluding remarks are provided in Section 5.4.

5.1 Distributed RF Front-End for Direct Conversion Receiver

The block diagram schematic of the DDC-RF is shown in Fig. 5.2. Similar to the UWB-DRF circuit presented in Chapter 4, this distributed RF front-end employs composite cells distributed along the input artificial RF TL. Each composite cell is comprised of a low-noise transconductance amplifier (LNTA) and a current-commuting mixer. The RF TL absorbs the input parasitic capacitances of the constituent LNTAs, thereby providing wideband input matching. The composite cells' output capacitances partially set the required −3 dB bandwidth of 250MHz required for each sub-band of the MB-OFMD signals at the baseband output. Therefore, the output TL, conventionally used in distributed topologies, is no longer needed. This results in huge reduction of chip area. Moreover, the input resistances seen from the connecting nodes of the LNTA and mixer (cf. S_Q and S_I in Fig. 5.3.) is low. Hence the capacitances of the common-source nodes S_Q and S_I produce high frequency poles. All these attributes enable the proposed DDC-RF to achieve the wideband flat specs.

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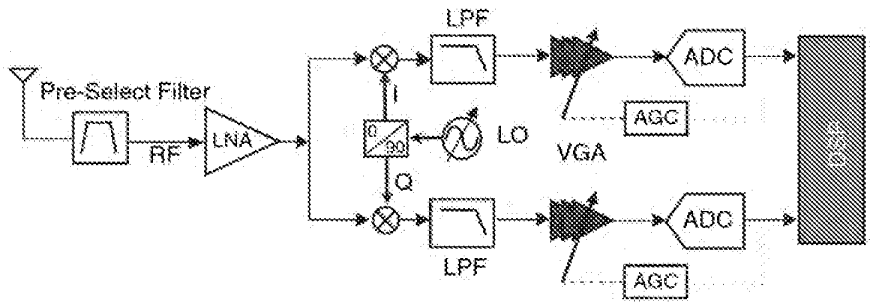


Fig. 5.1 System block diagram of a direct conversion receiver

To address the problems of large area and high power consumption in conventional distributed circuits, the DDC-RF incorporates minimum number of stages; that is, only two stages realized using three inductors. One stage is used for the in-phase component and the other one for the quadrature component of the UWB signal. Similar to the UWB-DRF presented in Chapter 4, this design obviates the need to use two separate distributed receiver paths for each of I and Q components. Furthermore, the composite cell re-uses the bias current for both the LNTA and mixer, resulting in lower power dissipation. Finally, the elimination of the output TL, due to the fact that output voltages Q_{BB} and I_{BB} are zero-IF IQ signals, results in further reduction of the chip area.

The key attributes of this novel DDC-RF are:

1. Wideband matching at input RF port to the antenna and pre-select filter (i.e. matched to 50 Ω).
2. Wideband flat gain, NF, and linearity for both I/Q paths.
3. Elimination of the output TL in conventional distributed architecture, leading to further area reduction.
4. Re-using the bias current for both the LNTA and mixer cells, hence reducing the power consumption of the RF front-end.

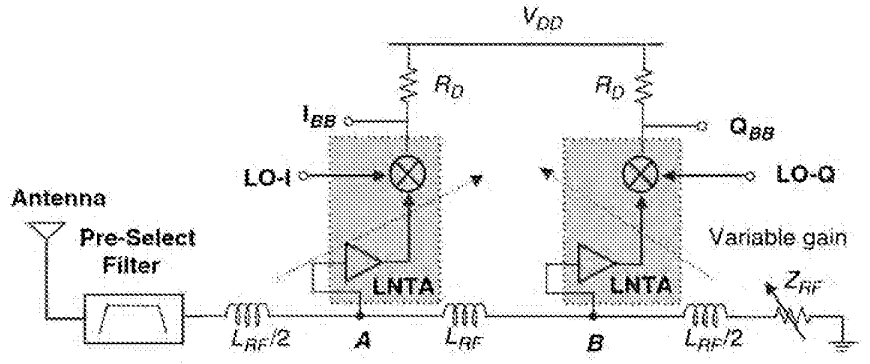


Fig. 5.2 Proposed distributed direct conversion architecture for UWB RF front-end

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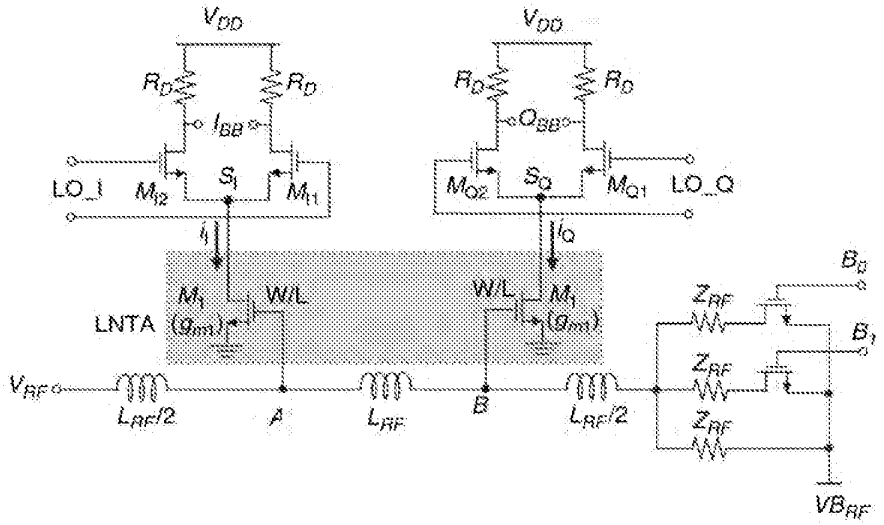


Fig. 5.3 Schematic of the DDC-RF architecture for UWB systems with programmable RF TL termination

5. Provision of variable matching resistance to achieve better noise, power-match performance (see Z_{RF} in Fig. 5.2 and B_0 & B_1 in Fig. 5.3).
6. Provision of variable-gain DDC-RF to accommodate large attenuation of in-band interferes, such as WLAN blockers. By controlling the common mode voltage of $LO_{I,Q}$ signals, the LNTA's transconductance and hence the front-end's gain will change accordingly.

A more detailed circuit schematic of the DDC-RF is shown in Fig. 5.3. The circuit utilizes two paths of composite cells of identical merged LNTA and current commuting mixers, one for I and the other one for Q component of data. The LNTA is a current-mode transconductance and simply comprised of two transistors. The mixers are current-commuting single-balanced cells derived by LO IQ signals. Each cell constitutes a fully differential single-balanced circuit, thereby showing a robust performance in the presence of the common-mode noise. Each mixer of the composite cell multiplies the input RF current with a periodic waveform running at the LO frequency, and produces the low frequency data component.

Similar to the discussion in 4.2.2, the overall receiver's voltage-gain is "$(1 + \Gamma_S) \times A_V$", where A_V is the front-end's voltage-gain and Γ_S is the receiver's input reflection coefficient. Γ_S varies between 0 (power matched RX with gain of A_V) and 1 (power un-matched RX with gain of $2A_V$ and with zero transferred power from antenna). The 6 dB gain boosting due to input mismatch is a noiseless gain, and the noise contribution from the circuit remains unchanged, therefore the NF will improve by 6 dB as well. Therefore, few decibels of mismatch at the RF input port of the front-end improves the receiver's voltage gain and NF. Such a variable RF termination resistance Z_{RF} is implemented using three equal parallel resistances

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of Z_{RF} with two NMOS switches controlled by two bits, B_0 and B_1 realizing RF terminations of Z_{RF}, $Z_{RF}/2$ and $Z_{RF}/3$ ($Z_{RF} = 150$).

5.2 Current Equalization to Remove IQ Gain/Phase Imbalances

As an important concern, the DDC-RF of Fig. 5.3 suffers from IQ gain and phase mismatches. To better understand this problem, consider the RF signal propagation through the input TL in Fig. 5.3. Because of the inherent TL's propagation delay from one tap-node to the next, RF signals at nodes A and B, and subsequently the currents i_I and i_Q, experience a frequency-dependent phase mismatch of ωt_d, where ω is the input radian frequency and t_d is delay of each LC section of the RF TL ($t_d = \sqrt{L_{RF}C_{RF}}$). Furthermore, signals at nodes A and B have amplitude mismatch of $e^{-\alpha}$ (where α is the attenuation constant of the RF TL) due to the existing loss of TL's inductors and poly gate resistances of LNTA transistors. α is indeed frequency dependent and is approximated as [1]:

$$\alpha \approx \frac{X}{4}\left(\frac{1}{Q_{ind}} + \frac{1}{Q_{gate}}\right) \tag{5.1}$$

where $X = \omega/\omega_C$ is the input radian frequency normalized by the RF TL cut-off frequency ($\omega_C = 2/t_d$). Q_{ind} is the quality factor of the TL inductor and $Q_{gate} = 3/r_g C_{gs}\omega$ is the gate quality factor of the LNTA transistor, where $r_g/3$ is the effective polysilicon gate resistance [2] and C_{gs} is the gate-to-channel capacitance.

The RF signals of the I- and Q- mixers, i_I and i_Q, are expressed as follows:

$$\begin{aligned} i_I &= g_{m1}.V_A = g_{m1}.V_{RF}.\sin(\omega t + \theta) \\ i_Q &= g_{m1}.V_B = g_{m1}.V_{RF}.e^{-\alpha}.\sin(\omega t - \omega t_d + \theta) \end{aligned} \tag{5.2}$$

where g_{m1} denotes LNTA's transconductance. Equation (5.2) clearly shows strong presence of systematic IQ gain and phase mismatches of $e^{-\alpha}$ and ωt_d between RF currents of I/Q mixers. One solution to reduce these IQ gain and phase mismatches is to choose the RF TL with a relatively high cut-off frequency ($\omega_c = 1/\sqrt{L_{RF}C_{RF}}$) with respect to the desired frequencies of UWB, i.e. $\omega_c >> \omega$.

To quantify the effect of the IQ mismatch, the proposed DDC-RF is placed into a Weaver-type receiver architecture [3], shown in Fig. 5.4.

The image rejection ratio (*IRR*) of the receiver accounts for both IQ gain and phase mismatches and is calculated as [4]:

$$IRR = \frac{(\Delta A/A)^2 + \theta^2}{2} \tag{5.3}$$

where $\Delta A/A$ is the normalized mismatch to the input amplitude of A, and θ is the phase mismatch. Figure 5.5(a–b) show the simulated *IRR* with respect to different values of RF TL's cut-off frequency across the desired UWB frequency

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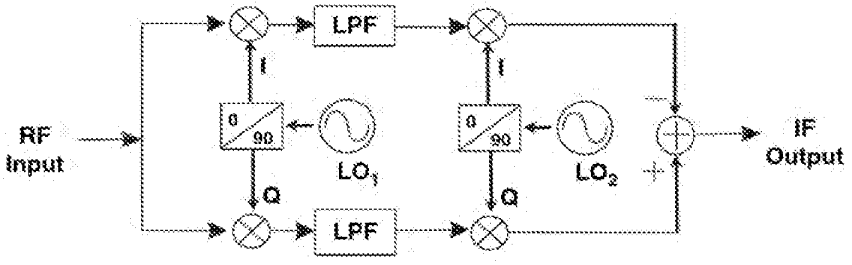


Fig. 5.4 Weaver image-reject receiver

range. As an example, for system-level simulations of the weaver architecture in Fig. 5.4, the following frequencies are chosen: f_{RF}= 10 GHz; f_{LO1}=9.7 GHz; f_{LO2} = 200 MHz. The UWB RF band is downconverted to the IF band of 100MHz, whereas the image band (centered at f_{image}=9.4GHz) is downconverted to the frequency band of 500 MHz. Since the phase mismatch is proportional to the input frequency, it imposes more severe impact at higher corner frequency of UWB, i.e. 10.6 GHz.

Evidently from Fig. 5.5, even with an over-designed cut-off frequency of the RF TL to extend to as high as 40GHz, the image rejection still cannot get better than 15 dB for input frequency of 10 GHz. Typically, an image rejection of 50 dB or better is considered a tolerable level of IQ mismatch in communication systems [4].

To avoid the systematic IQ gain and phase mismatches, one could simply connect the common source nodes of M_{I1-I2} and M_{Q1-Q2}, S_Q and S_I, to each other to feed the I/Q mixers with the same RF signals. However, capacitances seen at these nodes, which by the way are not absorbed by the RF TL, would add up, resulting in significant bandwidth degradation. In fact, simulation results shown in Fig. 5.6,

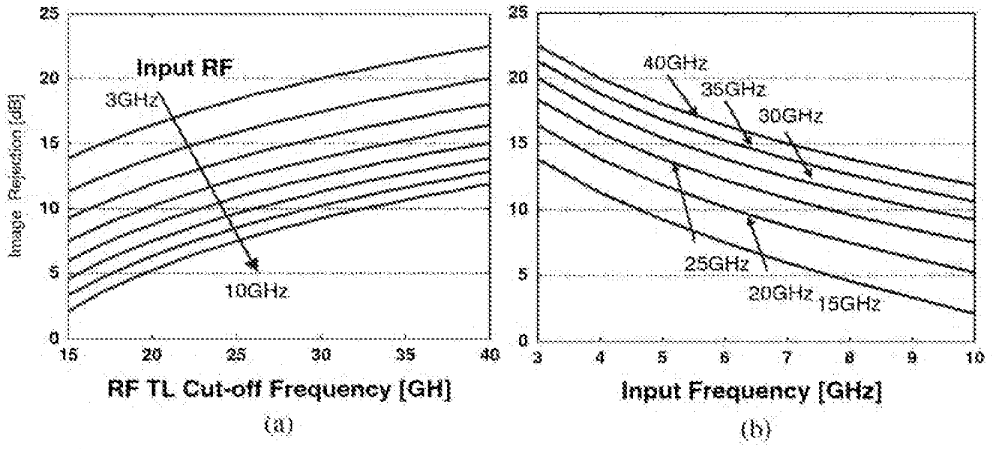


Fig. 5.5 Image rejection degradation due to distributed input matching network, with respect to (a) RF-TL cut-off frequency, ω_C, (b) input frequency

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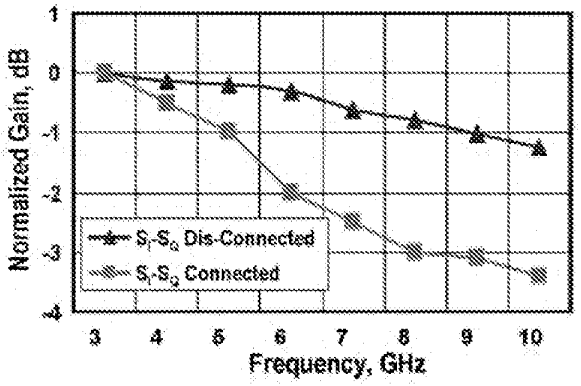


Fig. 5.6 Simulation results of the gain variation of the DDC-RF circuit with and without S_I / S_Q connection

demonstrate more than 3-dB drop in conversion gain across the UWB frequency range.

Therefore, to resolve the systematic mismatch, while retaining wide-band impedance matching at the input RF TL, a *symmetric* DDC-RF of Fig. 5.7 is explored.

The idea is to inject proportional RF currents from nodes A and B to Q- and I-paths, respectively, so as to compensate for gain and phase mismatches. To do so, two LTNA transistors M_1 with aspect-ratios of W/L in Fig. 5.3 are replaced with four transistors $M_{2,3C}$ with aspect-ratios of 0.5W/L in Fig. 5.7. This design provides no changes in capacitances at nodes S_Q and S_I compared to the circuit of Fig. 5.3. The two cross-coupled transistors M_{3C}, therefore, equalize i_I and i_Q for ideally zero gain and phase mismatches while not degrading the bandwidth. Therefore, for

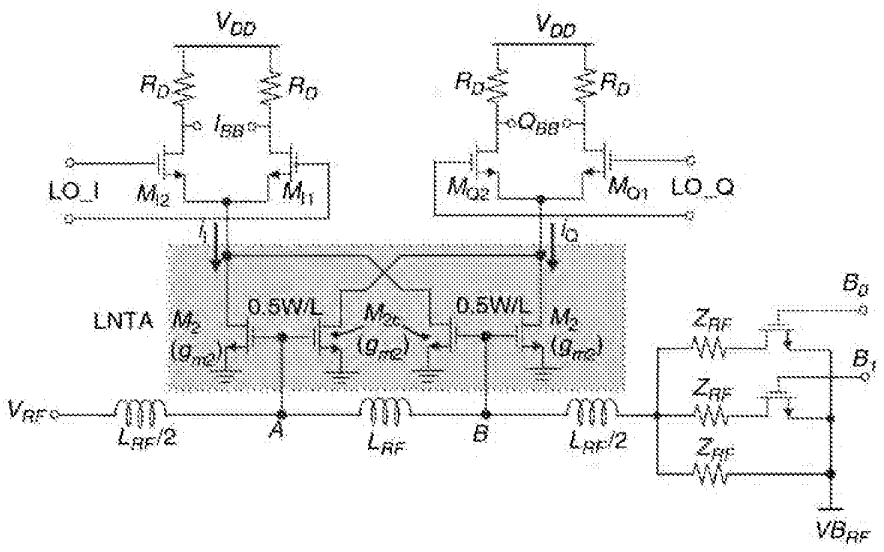


Fig. 5.7 Symmetric DDC-RF architecture for UWB systems with programmable RF TL termination

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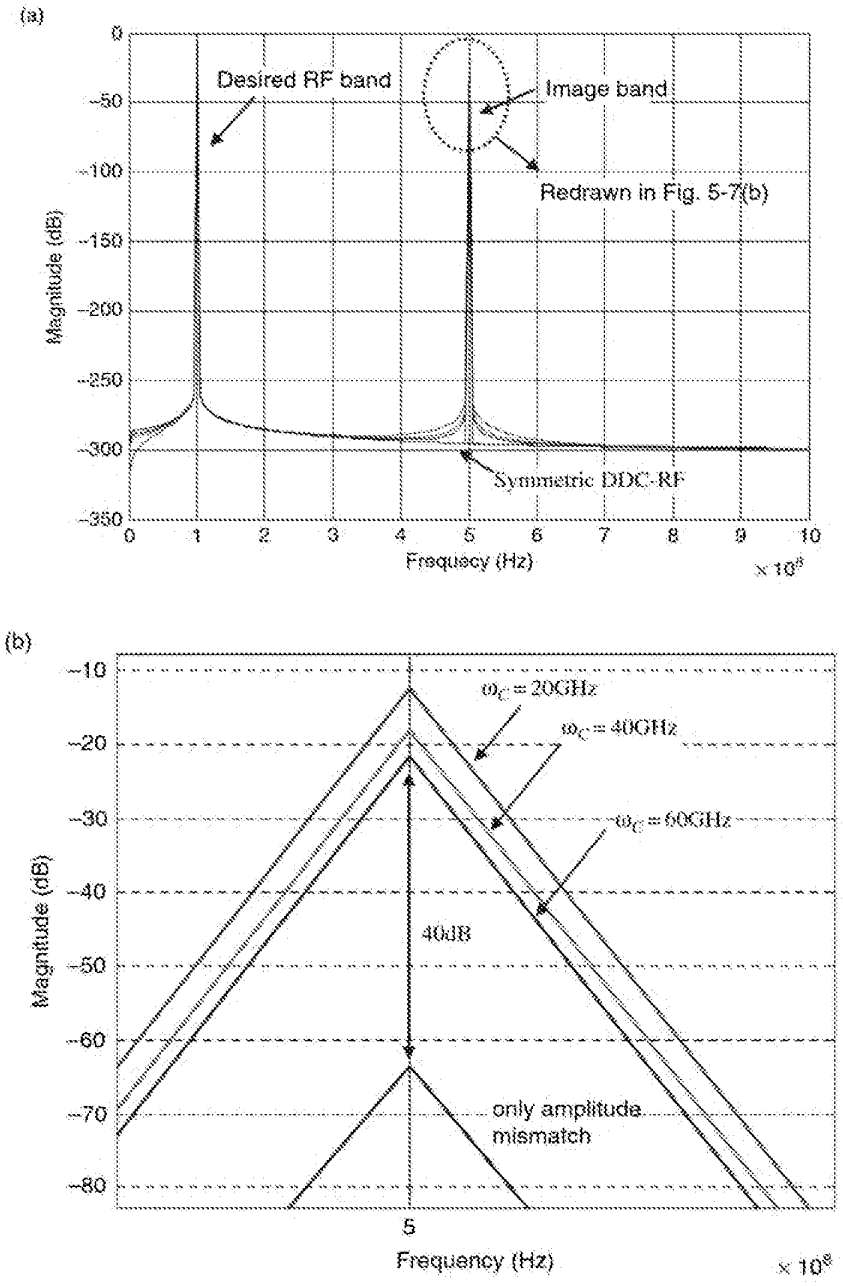


Fig. 5.8 (a) Output spectrum of a weaver receiver for different values of RF TL cut-off frequency. (b) Weaver receiver output spectrum zoomed in at image frequency

the symmetric DDC-RF, the RF currents flowing into the IQ mixers are readily obtained as:

$$i_I = i_Q = g_{m2}.(V_A + V_B) = g_{m2}.V_{RF}[\sin(\omega t + \theta) + e^{-\alpha}.\sin(\omega t - \omega t_d + \theta)] \quad (5.4)$$

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Evidently, (5.4) states that both IQ composite cells of LNTA/mixer cells sample the same RF signal at nodes A and B, thereby introducing no systematic IQ gain and phase mismatches.

The IF output spectrum of the weaver receiver using asymmetric and symmetric DDC-RF is shown in Fig. 5.8a. No image band exists at the output of the weaver receiver that uses the symmetric DDC-RF. On the contrary, the weaver architecture using the asymmetric DDC-RF displays image band.

Furthermore, Fig. 5.8b shows that the receiver achieves an IRR better than 60 dB. As shown in the simulation results of Fig. 5.8b the amplitude mismatch caused by the RF TL non-ideality constitutes a small fraction of the whole IRR.

5.3 Measurement Results

A symmetric DDC-RF, shown in Fig. 5.7, was fabricated in a 0.13 μm CMOS process and the die photo is shown in Fig. 5.9. The chip area excluding the pads and metal fillings is only $500 \times 400\,\mu m^2$, which is the smallest distributed architecture reported to date. Note that the chip area including pads and metal fillings is $1.1 \times 1.1\,mm^2$.

The conversion gain and NF were measured over a wide range of frequencies for different RF TL termination bits (B_0B_1). Figures 5.10 and 5.11 show the measured s_{11} and conversion-gain/NF, respectively. Accordingly, introducing mismatch at the RF TL termination using codeword of B_0B_1 = "00" ("10") degrades s_{11} by 14 dB (9 dB) in average, while improving gain and NF over 2.9 dB (1.2 dB) and 2.2 dB (0.9 dB), respectively. This is because of the existence of the noiseless voltage gain at the input matching network introduced by the programmable RF TL termination.

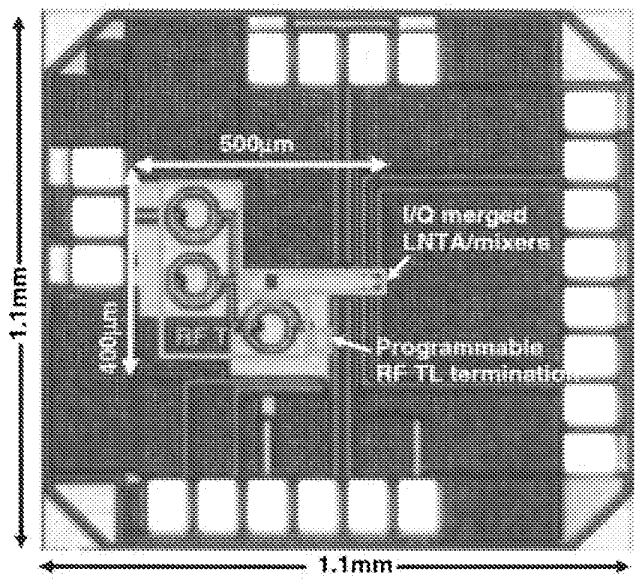


Fig. 5.9 Die photo of the symmetric DDC-RF

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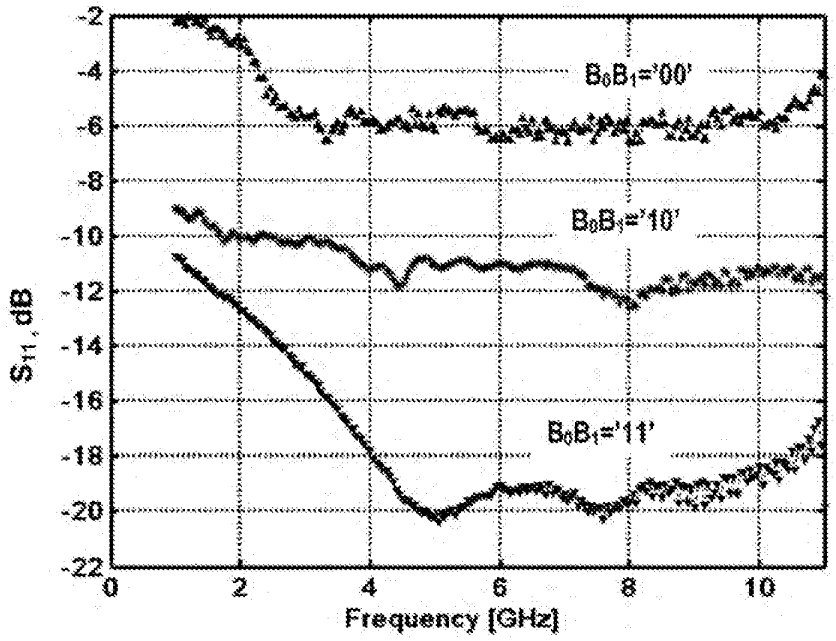


Fig. 5.10 Measured input reflection coefficient of the RF port, s_{11}, for different RF TL codewords

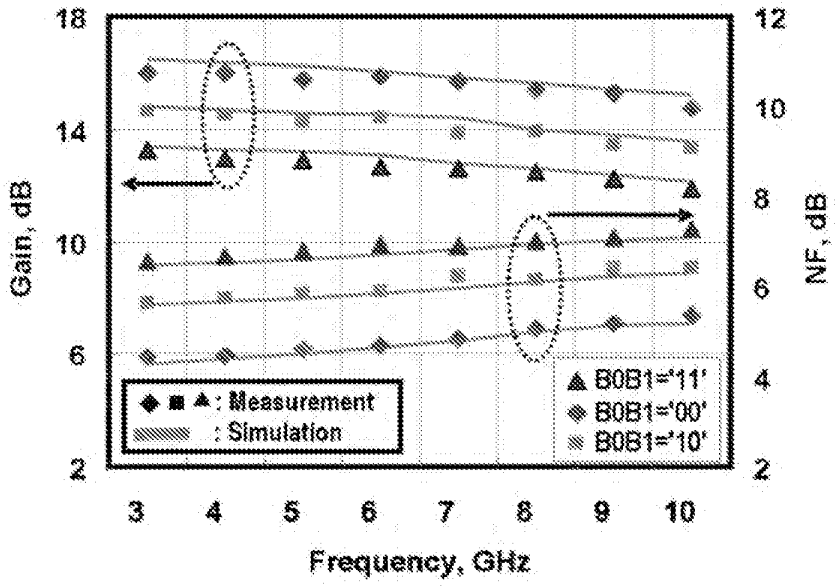


Fig. 5.11 Measured conversion gain and NF of the DDC-RF for different RF TL termination codewords

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The DDC-RF's conversion gain and NF variations across the UWB frequency range are less than 1.3 and 0.9 dB, respectively. The conversion gain and NF degradations are mainly due to the parasitic capacitance of the common source node of the switching pair transistors (M_{I1-I2} and M_{Q1-Q2}).

The baseband output frequency response of the DDC-RF for the RF input band of 3GHz with perfect matched termination (B_0B_1 = "11") is shown in Fig. 5.12. The measured baseband bandwidth of the circuit is 400MHz, with a slope of −20 dB/decade associated with the first-order output RC response of the DDC-RF.

The common-mode voltage $V_{LO,CM}$ of the mixers set the operation region of $M_{2,3C}$ to either saturation or triode, hence changes the LNTA's g_m and gain. Figure 5.13 shows the measured/simulated variable gain of the DDC-RF for the lowest and highest UWB frequencies with respect to $V_{LO,CM}$, setting boundaries for other frequencies (see Fig. 5.11 for gain variation vs. frequency).

Figure 5.14 shows the comparison between the phase/gain mismatches before and after current equalization. The phase mismatch increases proportional with frequency. Hence, for the input frequency band of 10GHz, with the designed TL cut-off frequency (f_C) of 20GHz, the simulated IQ phase imbalance could be as high as 60°. However, the measured results indicate that the current equalization technique effectively reduces the phase mismatch to less than ±2.5°. Furthermore, the measured IQ gain mismatch stays below ±0.5 dB.

The two-tone test was performed to measure the 3rd order input intercept point (IIP3). As an example, Fig. 5.15 shows the power of the fundamental and intermodulation components with −1.5 dBm of IIP3 for 10.5GHz input frequency. The measured IIP3 for matched RF TL termination varies from −3 to −1.5 dBm for the input frequencies of 3.5 to 10.5GHz, showing a wideband linearity of the DDC-RF.

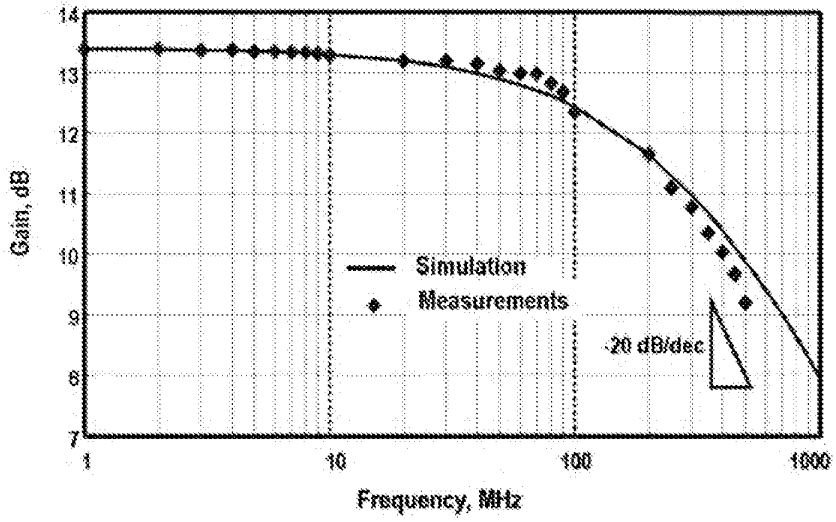


Fig. 5.12 Output IF characteristics: measured and simulated for the band of f_{RF}=3GHz and with RF TL codewords of B_0B_1="11"

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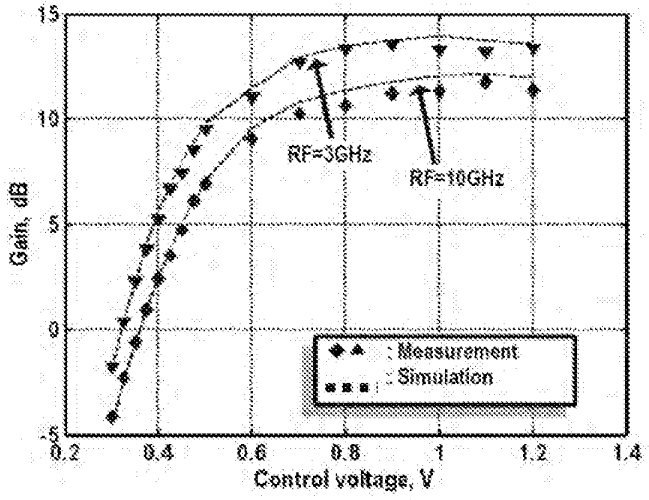


Fig. 5.13 Measured variable gain of the DDC-RF

Table 5.1 summarizes the DDC-RF performance, conversion gain, NF and IIP3 over the wide frequency range of the UWB systems, for RF TL of 50 Ω (B_0B_1 = "11").

The current consumption was 8mA from a 1.8V supply voltage. Table 5.2 compares the UWB-DDC-RF's performance with RF TL termination of 50 and 150 Ω (i.e. B_0B_1="11" and "00", respectively) with [5, 6]. This work achieves almost flat conversion gain and NF across the *entire* UWB frequency range.

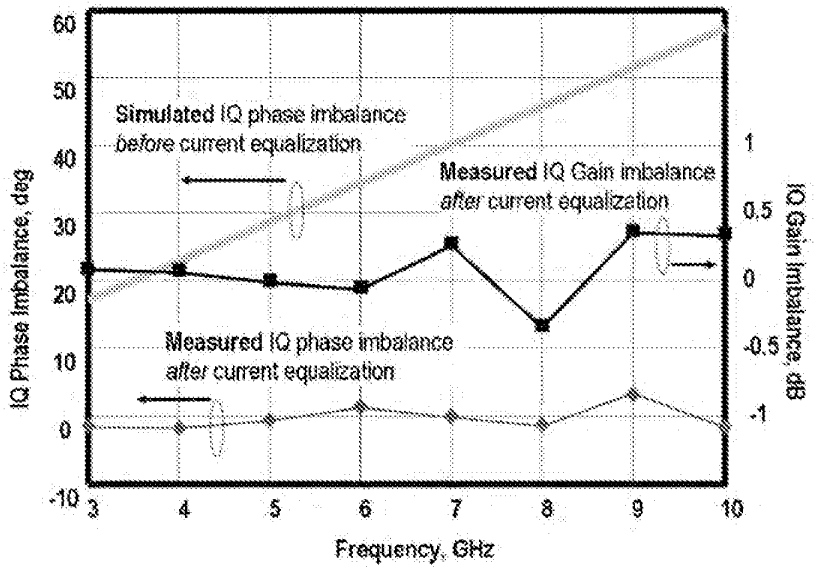


Fig. 5.14 IQ phase mismatch before (simulation) and after (measured) current equalization, also measured IQ gain mismatch

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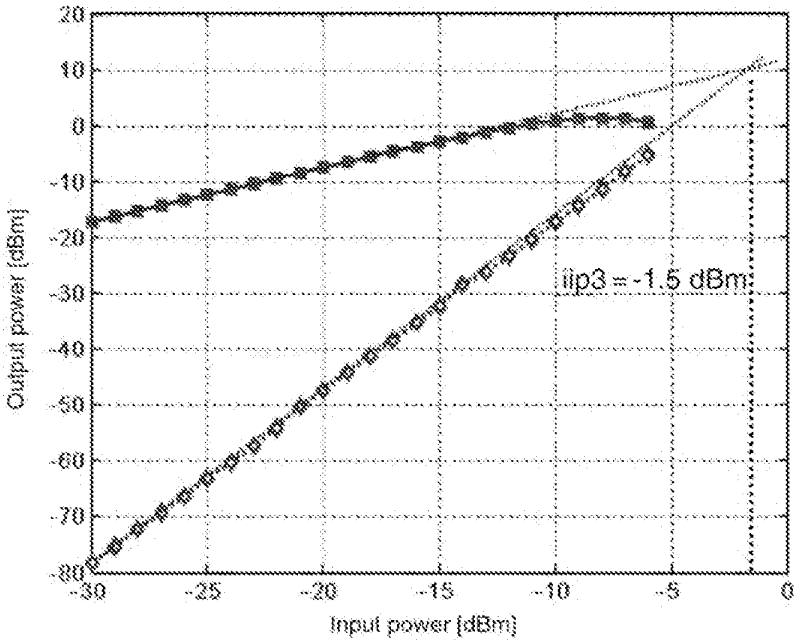


Fig. 5.15 Measured two-tone test for frequency band of 10.5GHz and RF TL termination of Z_{RF}=50Ω (B_0B_1="11")

Table 5.1 Measured summary of the UWB-DRF for RF TL termination of 50 Ω

f_{RF}, GHz	3.5	4.5	5.5	6.5	7.5	8.5	9.5	10.5
Gain, dB	13.4	13.25	13.2	13.1	12.8	12.6	12.4	12.1
NF, dB	6.5	6.5	6.6	6.7	6.8	6.9	7	7.1
IIP3, dBm	−3	−2.8	−2.7	−2.6	−2.2	−2	−1.7	−1.5

Table 5.2 Performance comparison of the recently published UWB DCRs and the proposed DDC-RF

REF.	Freq. (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)
[6]	3–5 0.13μm CMOS	69–73	6.5–8.4	> − 17.5	105 (w/TX)
[5]	3–8 SiGe Bipolar	51–52	3.3–4.1	> − 4.5	237.6 (w/Syn)
B_0B_1="11"	3–10 0.13μm CMOS	13.4–12.1	6.5–7.1	>−3	14.4
B_0B_1="10"		14.6–13.3	5.6–6.4	>−3.7	
B_0B_1="00"		16.5–15.2	4.3–5.2	>−4.4	

5.4 Summary

A novel DDC-RF RF front-end has been proposed in this chapter for UWB systems. Our invention combines the idea of distributed approach which provides wideband functionality of RF front-end, with IQ requirement of direct conversion receivers. The unique distributed architecture uses composite cells of merged LNA and mixer along the input RF TL. The main advantage of the proposed DDC-RF is that instead

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of using two different distributed receiver paths (proposed in Chapter 4) for each in-phase (I) and quadrature-phase (Q) data to achieve wide-band characteristics of RF front-end, an area and power efficient architecture, based on distributed concept for wideband characteristics of RF front-end is been designed and implemented. Also a current equalization technique has been implemented to overcome systematic IQ phase and gain mismatches. Furthermore, deploying merged LNA/mixer enables low-power design of the receiver architecture for UWB systems, while getting superior linearity over the conventional distributed amplifiers.

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Chapter 6
Distributed Active Power Combiners and Splitters for Multi-Antenna UWB Beamforming Transceivers

In a multi-antenna (MA)-UWB beamforming/diversity transceiver, the transmit side transmits a single data stream through multiple transmit antennas, while the receive side combines the received signal from the multiple receive antennas. With sufficient knowledge of the channel characteristic, a beamforming vector can be chosen at the transmitter that will result in full diversity and significant gain for the antenna array. Systems with multi-antennas are well known for their potential of improving system performance under multipath scenarios, while extending communication range [1]. Moreover, the transmit power is now boosted using beamforming mechanism, thereby relaxing the required transmit power for the constituent power amplifier in each transmit path. The MA-UWB systems are, therefore, viable candidates for high-rate mid-range communications in dense multipath environments.

The conventional phased array systems essentially utilize narrowband RF radio. For example, [2] introduced phase-shift around 24GHz center frequency so as to approximate the required delay within a narrow range of frequencies (e.g., 250MHz bandwidth around the 24GHz center frequency). Clearly, this idea cannot be used in MA-UWB beamforming systems, where true *broadband* variable delay is needed to steer the beam. By the same token, one of the most challenging tasks in the implementation of a silicon-based MA-UWB transceiver is the design of power combiners after receiver antennas and power splitters before transmitter antennas. Being able to realize both broadband variable gain and delay is essential in the implementation of power combiners and splitters targeting MA-UWB wireless systems. The wideband combiner and splitters should provide broadband variable gain and delay to steer the beam electrically, not mechanically. Active combiners and splitters exhibit gain (instead of loss) and improve isolation compared to passive counterparts [3]. Previous works on wideband active power combiners and splitters [3, 4, 5] were all fabricated in MMIC GaAs technologies, and were incapable of varying both the delay and gain. Recently, a single path broadband variable gain/delay was implemented in a SiGe BiCMOS technology [6].

One of the unique features of distributed circuits is that they provide wideband delay for the input to the output. In this chapter, we use this idea to design the wideband circuits for MA-UWB transceiver in which variable wideband delay is required for beamforming or gain diversity.

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This chapter mainly focuses on the active power combiners and splitters with wideband variable delay and gain using the distributed architecture. These circuits are the key components for use in MA-UWB point-to-point beamforming communication systems with multiple transmit and receive antennas. In this chapter, few broadband circuit topologies are introduced and studied.

The chapter is organized as follows: Section 6.1 illustrates a new MA-UWB wireless transceiver architecture with beamforming. Section 6.2 discusses the operating principle of the proposed distributed active combiner and splitter with broadband variable gain and delay. Section 6.3 includes measurement results of the fabricated power combiner and splitter in 0.13μm CMOS process. Finally, concluding remarks are provided in Section 6.4.

6.1 MA-UWB Transceiver Architectures with Beamforming

Figures 6.1(a)–(b) show the proposed receiver and transmitter architectures of an $N \times N$ MA-UWB system (in this figure $N = 4$) incorporating active power combiner and splitter.

In general, to achieve beamforming, one can introduce the required delay variability in RF, LO, or IF sections of a transmitter or receiver chain. Nonetheless, introducing controllable delay and combining signal powers in RF path consumes less power, because the power-hungry IF and baseband stages at both the transmitter and the receiver can be shared by all RF paths and antennas. Moreover, combining the signals at the RF stages of the multi-antenna receiver results in a better cancellation of interferes.

In the receiver system of Fig. 6.1(a), the proposed active power combiner with broadband variable gain ($A_{r,1}-A_{r,4}$) and delay ($\tau_{r,1}-\tau_{r,4}$) comes after the multiple antennas to provide beam-steering capability to the receiver. The active power combiner concurrently performs the low-noise pre-amplification, delay- and gain-adjustment, and active power combining. Moreover, a wideband amplifier is placed after the active combiner circuitry and before in-phase (I) and quadrature (Q) down-conversion mixers, to provide additional gain for the RF signal, and essentially to suppress the low-frequency noise of I/Q mixers, particularly flicker noise, thereby improving noise-figure (NF) of the receiver chain. The receiver also employs an RF feedback loop, as depicted in Fig. 6.1(a). The feedback loop comprising the RF detector, a lowpass filter (LPF), and a control unit around the active power combiner and wideband amplifier sets the optimum delay and gain of each path so as to maximize the RF signal's power at the receiver and achieve full diversity characteristics for the receiver antenna-array. The RF detector is a rectifier that, in companion with the subsequent LPF, takes the average power of its input signal. This DC signal then feeds to the control unit, which produces proper control voltages. The control voltages adjust the gain and delay of the active power combiner properly so as to maximize the combined power.

In the transmitter system of Fig. 6.1(b), an active distributed power splitter with broadband variable delay and gain is placed before the antenna array. In addition,

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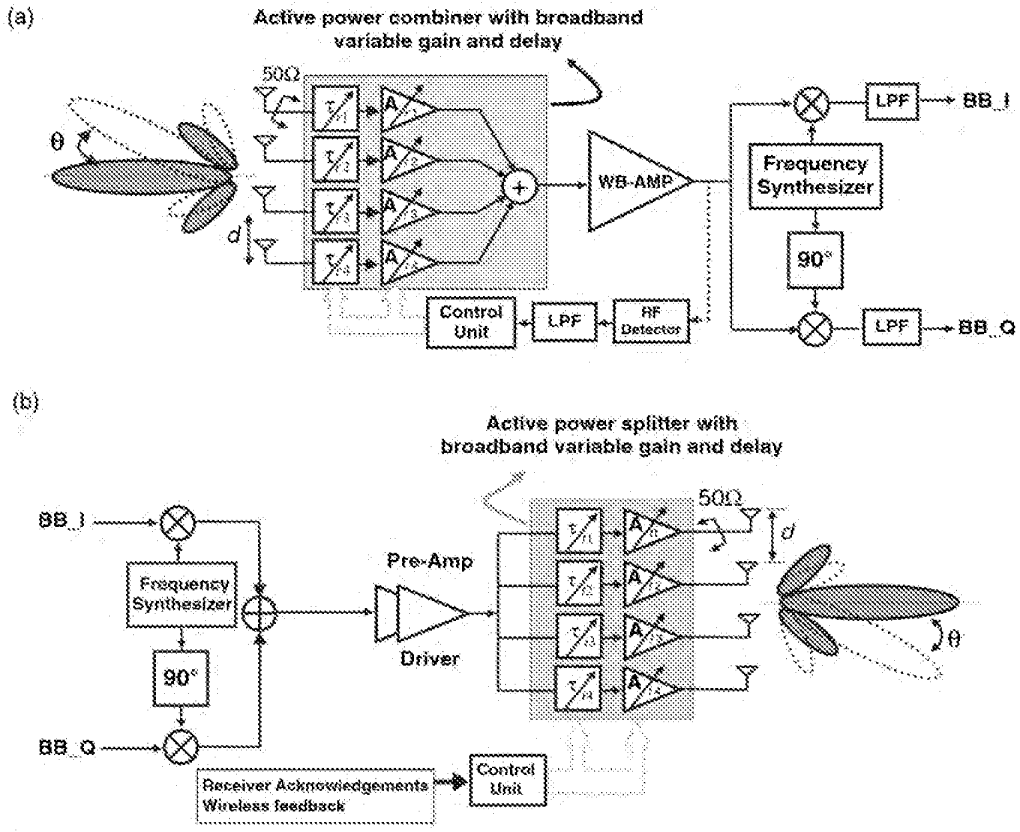


Fig. 6.1 a) The proposed wideband multi-antenna diversity gain receiver with distributed active power combiner. b) The proposed wideband multi-antenna beamforming transmitter with distributed active power splitter

the transmitter incorporates direct conversion architecture to reduce system complexity, and hence, reduce power consumption. The current commuting mixers generate differential RF I/Q components. By properly controlling delay ($\tau_{t1}-\tau_{t4}$) and gain ($A_{t1}-A_{t4}$) of each path to each antenna, the beam pattern of the transmitter's antenna array is directed toward the beam pattern of the intended receiver, which is determined according to acknowledgement signals from the receiver. Therefore, the delay and gain of each path is in fact controlled by a wireless feedback between the receiver/transmitter. As in communication theory of multi-antenna systems, one of the communication channels is allocated for the feedback signal from the receiver [7].

The beamforming phenomenon results in a number of important features in the proposed MA-UWB transceiver:

(1) The transmitter's interference and the receiver's interference-tolerance are both improved, while combating the fading effect.
(2) A fraction of the transmit power is now attained using beamforming, thereby relaxing the required transmit power for the constituent power amplifier in each transmit path. Accordingly, at the receiver with multiple antennas, an active

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power combiner with broadband variable gain and delay is capable of combining the received signal from multiple antennas properly so as to orient the received beam-pattern to the transmitted beam pattern.

Generally, in an *end-fire antenna array* whose antenna elements are spaced apart by at least $\lambda/2$, the direction of the beam's main lobe can be changed at will by introducing the appropriate broadband delay between successive elements of the array [8]. In fact, it is possible to produce a radar beam which sweeps around the horizon, without any mechanical motion of the array, by varying the delay between successive elements of the array electronically.

In wideband systems with a bandwidth of $f_H - f_L$, the wavelength, λ, is primarily determined by the higher corner frequency of the bandwidth [9], f_H, therefore,

$$d = \frac{\lambda}{2} = \frac{c}{2f_H} \tag{6.1}$$

where c is the velocity of light. For a beamforming at an angular phase of θ, the propagation delay τ of the electromagnetic wave from one antenna to the next should be:

$$\tau = \frac{d.\sin\theta}{c} = \frac{\sin\theta}{2f_H} \tag{6.2}$$

If electrical delays of multiple RF paths in the MA-UWB system are set properly using the broadband delay elements, the output signals of the antenna array (either radiated power from the transmitter's antenna array or received signal at the receiver's antenna array) will add up coherently, resulting in a beam formed into the direction of θ. The temporal propagation delay of the electromagnetic wave from the first to the Nth antenna is $(N-1).\tau$; therefore, the relative delay difference in from the first to the Nth antenna should be varying from 0 to $(N-1).\tau$ to achieve continuous beam radiation angle from -90° to $+90^\circ$.

Therefore, the maximum angle of coverage for an N-array antenna system is:

$$\theta_{max} = 2\sin^{-1}\left(\frac{2f_H\tau}{N-1}\right) \tag{6.3}$$

The factor of two before the inverse *sine* function comes from the fact that the coverage spans from $-\theta_{max}$ to $+\theta_{max}$. For example, in a dual antenna UWB system where $N = 2$, and $f_H = 10.6$GHz, the required broadband variable delay for 90° of coverage ($\pm 45^\circ$) is calculated to be 30ps from (6.3).

In an N-antenna array transmitter, it is possible to form a directional beam pattern whose power is a quadratic function of N. Similarly, the coherent addition of the received signals in an N-antenna array receiver results in a *maximum* SNR improvement of $10\log_{10}(N)$, which, in turn, leads to an improvement of the receiver sensitivity.

Having highlighted some of the important attributes of a beamforming MA-WB system, we will be focusing on describing novel circuit topologies for ac-

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tive power combiner and splitter, employed in the proposed MA-UWB transceiver in Fig. 6.1(a)–(b). Specifically, we aim for designing circuits that achieve the following important characteristics:

(1) Provision of broadband variable delay to steer the beam
(2) Provision of wideband matching to the 50Ω antenna impedance

The realization of a broadband variable delay in silicon is quite challenging, since the delay elements need to be extremely low-loss. The inherent wideband matching of distributed circuits together with the acquiescence of these circuits to operate at millimeter-wave frequencies make them a favorable architecture of choice for the realization of variable delay elements, as will be illustrated in Section 6.2 we will present the design of wideband active power combiners and splitters with the ability to vary both the delay and gain. Moreover, designing novel *active* power combiners and splitters with broadband variable delay and gain overcomes the loss of the passive RF delay elements such as passive *LC* networks. Finally, distributed power combiners and splitters provide wideband flat gain, and thus, will not degrade the beam pattern of the MA-UWB system of Fig. 6.1(a)–(b).

6.2 Distributed Power Combiner and Splitter

Recent advances in high-speed integrated circuit design in conjunction with continuous scaling of minimum feature sizes of semiconductor devices have renewed the interest in designing monolithic distributed circuits. In fact, prior research demonstrated the use of distributed architectures in designing distributed VCOs [10], UWB CMOS LNAs [11], UWB CMOS mixers [12], and broadband non-uniform amplifiers [13]. In addition, Chapters 3–5 described the use of new distributed circuit topologies for UWB radios.

The active power combiners and splitters being introduced in this chapter employ artificial transmission lines (TLs) to satisfy the required wideband operation. The remaining of this chapter provides a comprehensive illustration of the proposed active combiners and splitters. The active cells providing variable gain and delay are distributed along the TLs.

6.2.1 Distributed Architecture with Broadband Variable Gain and Delay

The proposed power combiner and splitter constitute a number of identically matched cells that are distributed along the gate and drain TLs, and realize the broadband variable gain and delay. The unit cell achieving broadband variable gain and delay is shown in Fig. 6.2, where the gate and drain *LC* TLs are identical. External capacitances have been added to make the capacitances of the two lines identical.

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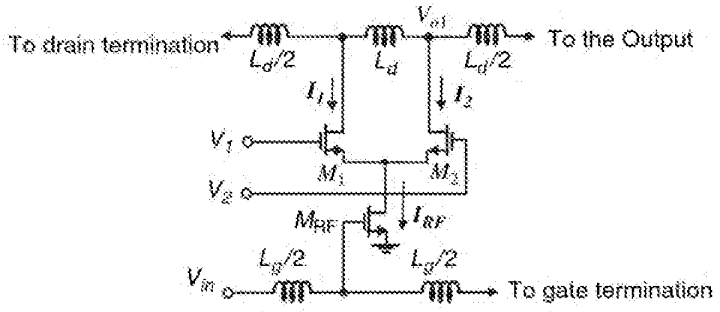


Fig. 6.2 Broadband variable gain and delay unit cell

The bias voltages V_1 and V_2 control gain and delay of the signal path from RF input to the output. The common-mode voltage $V_{CM} = 0.5(V_1 + V_2)$ sets the operation region of the tail current transistors, M_{RF}, to be either in saturation or triode. A change of operation region will subsequently change the transconductance of M_{RF}, thereby controlling the gain from the input to the output. Note that for a large range of V_{CM} variation, the variation in the total gate capacitance remains small, and therefore, good impedance matching is maintained [14].

Considering that each LC section of gate and drain TLs exhibits a propagation delay of $t_d = \sqrt{LC}$ ($L_g = L_d = L$ and $C_g = C_d = C$), if the RF current flows to the output through M_1, it will experience a delay of $2t_d$. On the other hand, the RF current will experience a delay of t_d if transistor M_2 conducts only. This implies that by controlling the differential voltage, $V_d = V_1 - V_2$, the delay from the input to the output varies from t_d and $2t_d$. Generally, the inherent controllable delay of the proposed distributed architecture gives rise to a broadband variable delay from t_d to $2t_d$. Each variable gain and delay unit cell, shown in Fig. 6.2, contributes one t_d, and the half-valued inductors at the input and the output ports together contribute one t_d.

The phasor analysis will be carried out to calculate the variable delay of the unit cell in Fig. 6.2. The phasor of the unit-cell's output voltage (see V_{o1} in Fig. 6.2) is:

$$V_{o1} = \frac{-Z_d}{2} I_1 \angle -\omega t_d + \frac{-Z_d}{2} I_2 = \frac{-Z_d}{2} . I_{RF} . (a_1 \angle -\omega t_d + a_2) \tag{6.4}$$

where

$$\begin{aligned} t_d &= \sqrt{LC} = \frac{2}{\omega_C} \\ a_1 &= \frac{g_{m1}}{g_{m2} + g_{m1}}, \; a_2 = \frac{g_{m2}}{g_{m2} + g_{m1}} \end{aligned} \tag{6.5}$$

where ω is the input frequency and is ω_C is the so-called TL's cut-off frequency, a_1 and a_2 (Note $a_1 + a_2 = 1$) are current gains of the differential pair transistors, which depend on their transconductances, $g_{m1,2}$. The drain termination is Z_d. The $-1/2$ factor in (6.4) comes from the fact that the current at each tap-point of the drain TL

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splits into two equal parts, forward current toward the output and backward current toward Z_d. The amplitude and phase of the V_{o1} phasor will thus be equal to

$$|V_{o1}| = \left|\frac{Z_d}{2}.I_{RF}\right|\sqrt{a_1^2 + a_2^2 + 2a_1a_2\cos(\omega t_d)}$$
$$\angle V_{o1} = -\tan^{-1}\frac{\sin(\omega t_d)}{a_2/a_1 + \cos(\omega t_d)}$$
$$Delay = t_d\frac{1 + a_2/a_1.\cos(\omega t_d)}{1 + (a_2/a_1)^2 + 2a_2/a_1.\cos(\omega t_d)} \tag{6.6}$$

In two extreme cases where the RF current flows entirely through M_1 ($a_1 >> a_2$) or M_2 ($a_2 >> a_1$), the broadband delay will be either t_d or 0 with respect to the input I_{RF}, as also clear from (6.2.1). Current gains a_1 and a_2 are controlled with gate bias voltages of $M_{1,2}$. Accordingly, the delay of the unit cell is controlled *continuously* from t_d to $2t_d$.

Note for delay adjustment from 0 to t_d the output amplitude also changes. One should assure that the amplitude variation during delay adjustment is small, say less than 1 dB, to independently control the delay and gain. The maximum amplitude of V_{o1} happens when $a_1 = 1$ (or 0), and the minimum occurs at $a_1 = a_2 = 0.5$ (see Fig. 6.3 (b)), which can be analytically derived from (6.2.1). The amplitude variation during the delay adjustment process is expressed as follows:

$$\Delta V = 20\log\frac{|V_{o1}|_{a1=1}}{|V_{o1}|_{a1=0.5}} = 20\log\left|\cos(\omega t_d/2)\right| = 20\log\left|\cos(\omega/\omega_C)\right| \tag{6.7}$$

Equation (6.7) states that higher values of TL's cut-off frequency result in less gain variation during delay adjustment, which is verified by simulation results in Fig. 6.3(a–b).

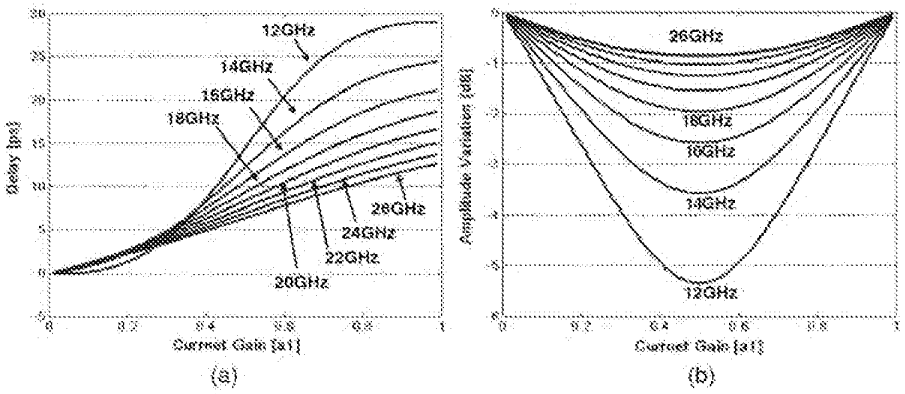


Fig. 6.3 (a) Delay control, (b) amplitude variation during delay adjustment for different values of TL cut-off frequency (ω_C) for input frequency of 11GHz

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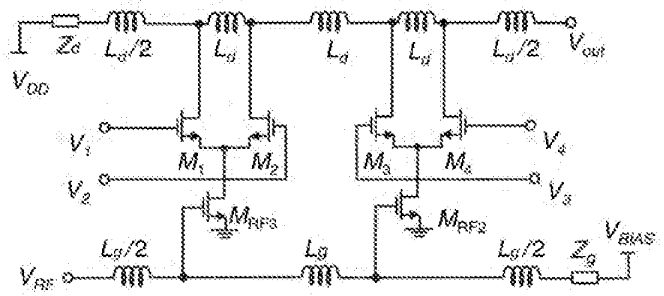


Fig. 6.4 Two-stage broadband variable gain and delay

One way to widen the delay range is to insert more delay in between the two switches of M_1-M_2, meaning more LC sections or more t_d. However, according to (6.2.1), that leads to larger amplitude variation during delay adjustment.

The other alternative to widen the tuning range of the variable delay is to add another identical stage to the unit cell of Fig. 6.2, resulting in the two-stage circuit broadband variable gain and delay of Fig. 6.4.

The delay of the M_1-M_2 path varies from $3t_d$ to $4t_d$ depending on the differential voltage, $V_{d1} = V_1 - V_2$. Similarly, the delay of the M_3-M_4 path is controlled by $V_{d3} = V_3 - V_4$ and varies from $2t_d$ to $3t_d$. Therefore, the delay is controlled first by coarse adjustment, which is the selection either M_1-M_2 or M_3-M_4 path, then fine adjustment by controlling the differential voltages V_{d1} or V_{d3}.

Despite comprising 5 delay elements (i.e., gate and drain LC sections) from the input to the output terminal, the circuit can essentially provide a variable delay from $2t_d$ to $4t_d$, only To achieve the maximum achievable delay's tuning range out of a two stage broadband gain and delay, we propose the new circuit in Fig. 6.5, where two extra cross couple paths are added from the gate TL tap-points to the drain TL tap-points. The additional cross-couple stages, M_5-M_8 with tail current sources M_{RF1} and M_{RF4}, provide the fastest $[t_d, 2t_d]$ and slowest $[4t_d, 5t_d]$ delay paths from the RF input port to the output port. The signal paths through M_{RF2} and M_{RF3} exhibit the same controllable delay as those in the circuit of Fig. 6.4.

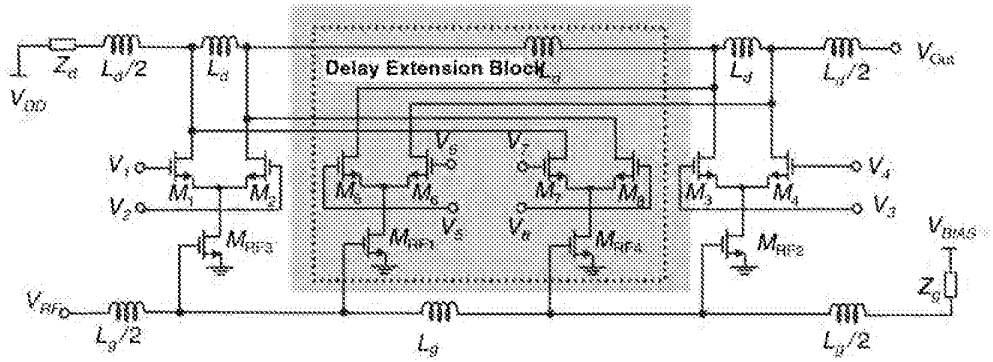


Fig. 6.5 Two-stage broadband variable delay and gain with delay extension block

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respectively. Subsequently, the new two-stage broadband circuit of Fig. 6.5 extends the tuning range by as much as 100% to $[t_d, 5t_d]$ compared to the circuit of Fig. 6.4. This, in turn, results in a wider angle for beam-steering in the proposed MA-UWB beamforming system of Figs. 6.1 and (b). As a result, with the same measured unit delay of 10ps, the range of the variable delay could be extended to 40ps, which is equivalent to over 108° (±54) angular coverage range.

To adjust the delay and gain, control voltages are applied to differential-pair transistors of the constituent power combiner/splitter using a digital-to-analog converter (DAC) fed by digital control unit and a selector circuit. The selector circuit serves as a coarse-tuning stage, setting the local optimal delay value among a number of delays with quantized steps of t_d. The DAC, acting as a fine-tuning system, fine-tunes the delay and gain. The realization of the feedback control path is not included in this chapter.

6.2.2 Distributed Active Power Combiners

A distributed active power combiner utilizes N broadband voltage-controlled gain/delay cells with N input paths, to deliver received signals from N-antenna array to a single output path. Each input path constitutes a distinct input gate TL, which is matched to a separate antenna in the MA-UWB beamforming receiver of Fig. 6.1. The signal combination will take place in the ***current*** domain. An example of a proposed two-stage active power combiner with two input ports is shown in Fig. 6.6.

The use of N input TLs sharing a common output path will readily result in a generalized power combiner for an N-antenna array MA-UWB receiver. The distributed circuit is capable of providing a broadband delay as well as wideband input matching to 50 Ω. The gain and delay of each input port toward the combined output

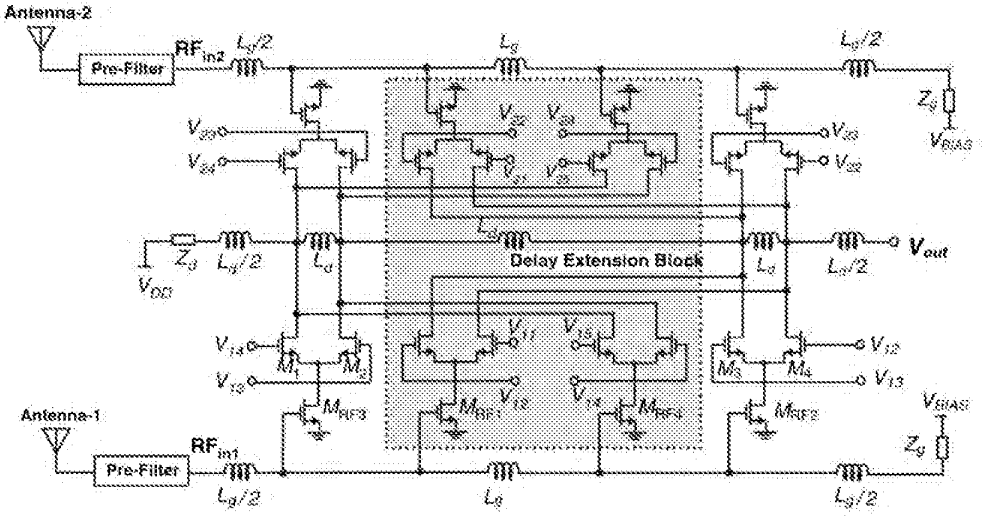


Fig. 6.6 A two-stage distributed active power combiner with delay extension block

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port, V_{out}, is controlled separately by the common-and differential-mode voltages of constituent differential pairs, respectively.

The power combiner is the first building block of the receiver radio; hence, it primarily determines the receiver's NF and the receiver sensitivity. In MA-UWB beamforming systems with signal combination at the receiver, the delayed signals received by N antennas are added coherently in amplitude at the power combiner's output. In contrast, noise powers contributed by N antennas and the power combiner's active devices will be combined in the power domain, because they are uncorrelated. The SNR of the combiner's output will thus be improved by $10\log_{10}(N)$.

It is also helpful to analyze the power combiner's NF. Assuming S_{in} and N_{in} to be the signal and noise powers at each antenna, and N_1 and G_1 to be the intrinsic noise and gain of the active power combiner, the output SNR of a single receiver path receiver will be

$$SNR_{1,out} = SNR_{1,in}/NF_1 \tag{6.8}$$

where

$$NF_1 = \frac{N_1 + N_{in}}{G_1 N_{in}} \tag{6.9}$$

In an N-antenna array system with the coherent power combination, the output signal power can be written as:

$$S_{out} = N^2.G_1.S_{in} \tag{6.10}$$

The uncorrelated noise at the combiner's output is:

$$N_{out} = N(N_{in} + N_1) \tag{6.11}$$

Therefore, one can readily prove that the NF of the N-array antenna, NF_N, using active power combiner is:

$$NF_N = \frac{1}{N} NF_1 \tag{6.12}$$

Equation (6.12) clearly states that the receiver sensitivity will improve by $10\log_{10}(N)$, dB. Although having more active elements means more noise sources in general, but the coherent combination of received signals will improve the NF and sensitivity.

6.2.3 Distributed Active Power Splitter

The core circuit of a power splitter employs the broadband delay/gain unit cell introduced in Fig. 6.5 with extended delay range. Used in MA-UWB transmitter of

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Fig. 6.1(b), a distributed active power splitter is a number of broadband variable gain/delay stages share an input gate TL (rather than output TL in power combiner counterpart), which is wideband-matched to 50 Ω, and connect to the separate output drain TLs, each of which being wideband-matched to 50 Ω. Essentially, each drain TL will be connected to a distinct transmit antenna. An example of a two-stage two output-port active power splitter, incorporating broadband gain and delay stages, is shown in Fig. 6.7.

The delay of each path from the shared input port to the output ports is controlled by the differential voltage of the bias voltages of differential pairs, i.e., V_d.

All the input and output ports of the distributed active combiner and splitter have wideband frequency characteristics, beneficiating from the intrinsic wide-band characteristics of the artificial TLs.

6.2.4 Power Splitters and Combiners with Shunt Peaking Inductors

All input and output ports of the proposed distributed active power combiner in Fig. 6.6 are wideband-matched to 50 Ω. The need to have both input and output matchings is particularly essential in a multi-chip module design. For a fully integrated MA-UWB system, the power combiner's output drives a wideband amplifier inside the chip. The output matching is therefore not required, thereby obviating the need to use bulky passive impedance transformers. This also indicates that the output transmission line may not be needed and less complex bandwidth enhancement techniques such as shunt (and/or series) peaking can be used. A power combiner which exploits this idea is shown in Fig. 6.8 (for simplicity only one path is shown,

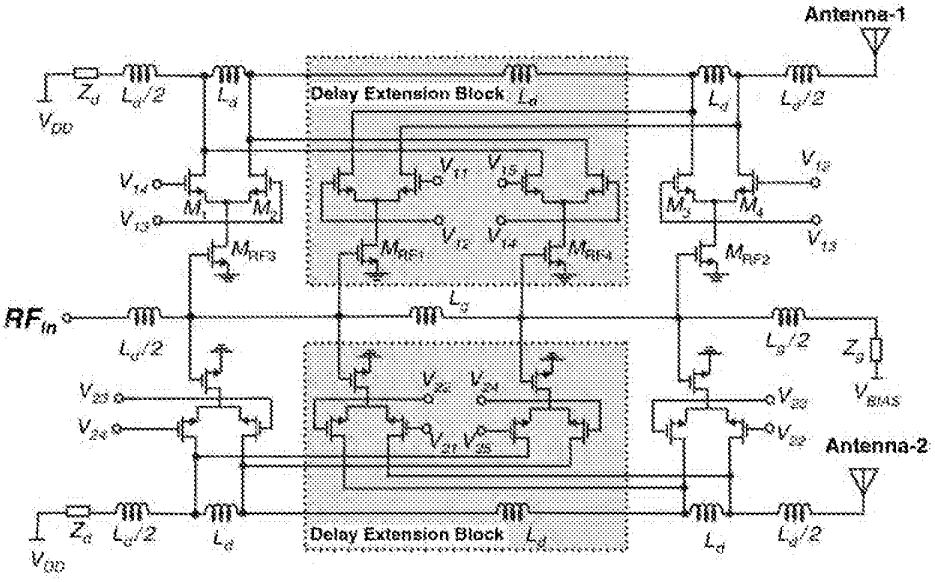


Fig. 6.7 A two-stage distributed active power splitter with delay extension block

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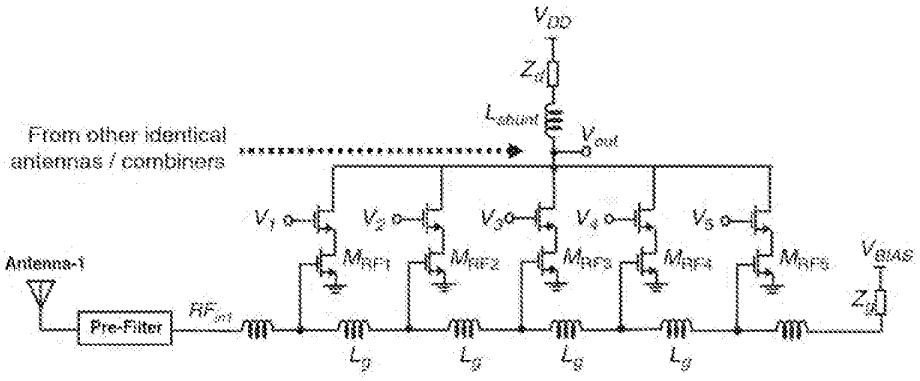


Fig. 6.8 Distributed active power combiner with broadband variable gain and delay using shunt peaking at the output port

the paths from other antennas share L_{shunt} and Z_d), in which the output port uses a shunt peaking, and the power combination is again in current mode.

The shunt-peaking inductor absorbs the capacitances at the output node to provide wideband frequency characteristics. All the broadband delay elements are provided by the input gate transmission lines.

Similarly, the input of a fully integrated power splitter comes from preceding on-chip driver or buffer stage. Therefore, 50Ω wideband input matching may not be needed for the power splitter. Alternatively, the input wideband matching can be utilized by using shunt-peaking in the preceding driver or buffer stage, as the shunt-peaking inductor absorbs the input capacitances of the power splitter. In this case, the broadband delay will be provided by the *LC* delay elements of the output drain transmission lines. The circuit architecture of such a power splitter with broadband variable delay is shown in Fig. 6.9.

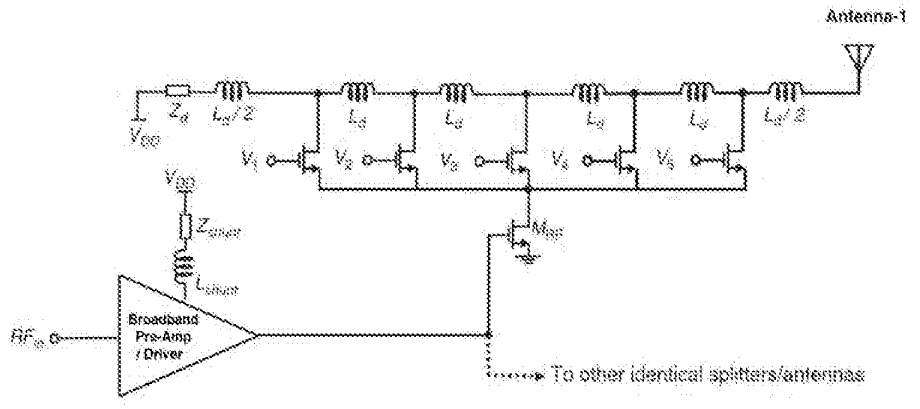


Fig. 6.9 Distributed active power splitter with broadband variable gain and delay using broadband pre-amp / drivers

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6.3 Experimental Results

A two-stage distributed active power combiner and a three-stage distributed active power splitter for a 2×2 MA-UWB beamforming transceiver were designed and fabricated using a 0.13μm CMOS process. Figure 6.10(a–b) show the die photo of combiner and splitter, respectively. The chip area of the combiner and splitter are $1 \times 1\,\text{mm}^2$ and $1.3 \times 0.9\,\text{mm}^2$, respectively.

The fabricated power combiner and splitter constitute of the unit cell of Fig. 6.5. The *interstage* drain inductors between the drains of consecutive active cells (i.e., L_4 between the drains of M_2 and M_3 in Fig. 6.4) and the active devices in delay extension block are omitted in our design, allowing the active cells to share the control bias voltages, i.e. $V_1 = V_3$ and $V_2 = V_4$. As a result, the power gain of each path of the 2-stage power combiner is increased by 3dB. Furthermore a three-stage distributed power splitter similar to the one proposed in Fig. 6.7, but without the *interstage* drain inductors and the active devices in delay extension block, has also been fabricated in a 0.13μm CMOS process. This, in turn, reduces the number of bias pads and makes it easier to carry out on-wafer measurement of the power combiner and splitter chips, and increases the delivered power of each path of a 3-stage power splitter by 6dB. This is achieved at the expense of reducing the range of broadband delay, and hence, the range of angular coverage of the MA-UWB transceiver.

The drain and gate spiral inductors (L_g, L_d) are identical whose value is 590 pH. They are built on three thick top-most metal layers in IBM 0.13μm CMOS process. The half inductors ($L_g/2$, $L_d/2$) at the input, and output ports and at near-end

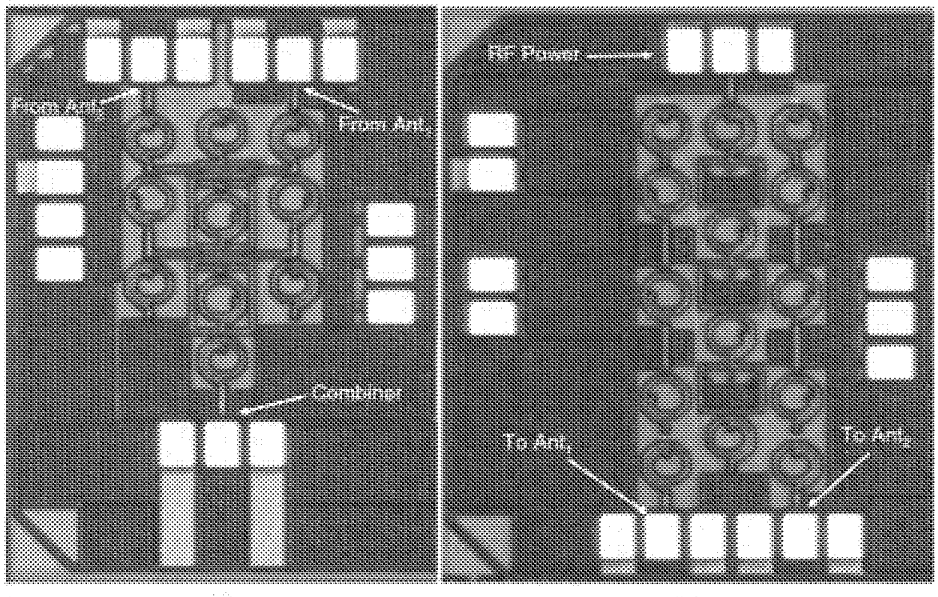


Fig. 6.10 Die photos of (a) power combiner (b) power splitter

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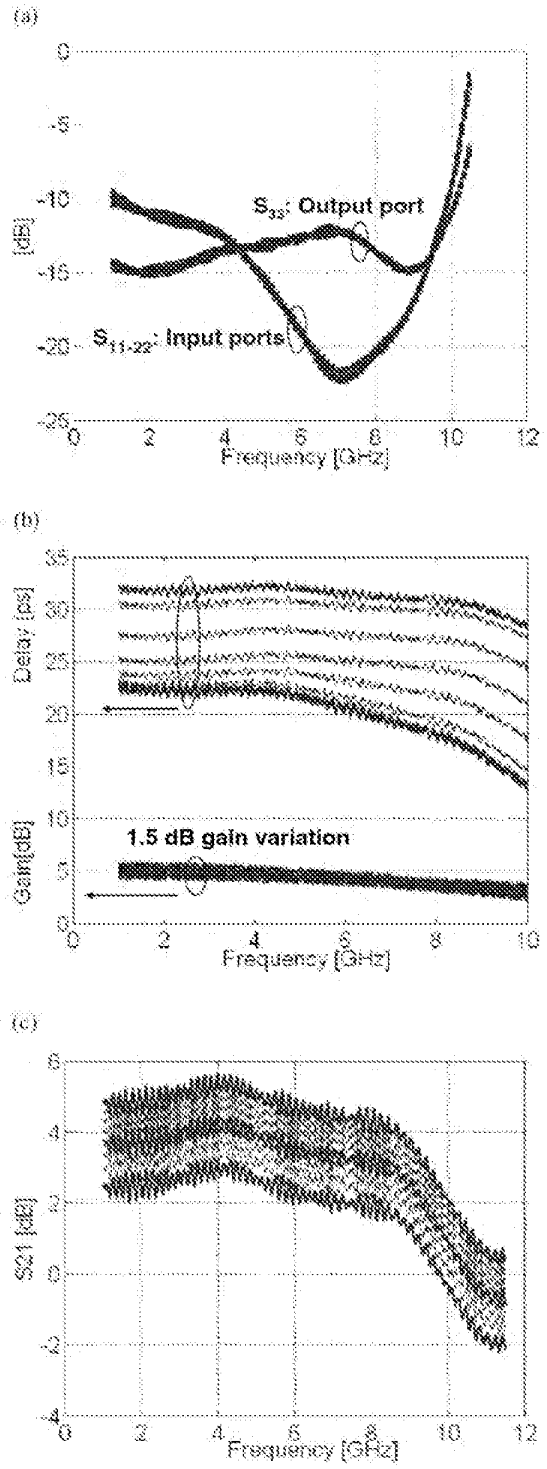


Fig. 6.11 Power combiner measurements: (a) return losses $S_{11,22,33}$, (b) variable delay, and gain variation during delay adjustment, and (c) variable gain S_{21} (or S_{43}) by controlling the common mode voltage

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terminations are 313 *pH*. Additional 100*fF* MiM (Metal-insulator-Metal) capacitors are added to drain tap points to make drain and gate *LC* sections identical. The aspect ratios of tail transistors, M_{RP}, are 100μm/120 nm, and those of the differential-pair transistors are 50μm/120 nm.

The measurements are done using on-wafer testing. Figure 6.11(a–c) show measurement results of the power combiner. Measured return losses of input ports and combined output port are better than −10dB for the entire UWB frequency band. The wideband variable delay of each path of the power combiner is controllable from 32 to 42 ps, and During the delay adjustment, the gain is changed by 1.4 dB, therefore, the delay and gain are controlled almost independently. Fig. 6.11(c) shows wideband variable gain, controlled by the common mode voltage of the switching pair.

Figure 6.12 shows the measured NF of a single path of the power combiner, which is 4.5–5.4 dB for the wide range of frequencies of 1–11 GHz, respectively. Although each single path exhibits relatively high NF, optimum combination of the signals from individual paths due to beamforming can improve the NF *maximally* by $10\log(N)$ (which is equal to 3dB for $N = 2$) in a *flat fading* UWB channel [7].

Similarly, Fig. 6.13(a–c) demonstrate measurement results of the power splitter. Fig. 6.10(a) shows wideband matching at the input port and output ports where the input power is splitted. Again, the broadband delay from input port to each output port is controllable from 43 to 53 ps, while the gain varies 1.5 dB during delay adjustment. The variable gain of each path is also controllable using common-mode voltage of the differential pair, as shown in Fig. 6.13(c).

Figure 6.14 shows the measured variable gain versus the common-mode control voltage of power combiner/splitter. The knee happens when the tail transistor makes a transition from triode to saturation. The controllable gain capability enables power combiner to accommodate large input signals. Moreover, the power splitter has almost 3.5 dB more gain than power combiner because it employs a 3-stage distributed splitter.

Figure 6.15 shows the measured output −1dB compression point (CP) of each path of the power splitter, which is about 7.1dBm. This implies that each path is capable of carrying 7.1dBm RF signal to the transmit antenna load of 50 Ω, and

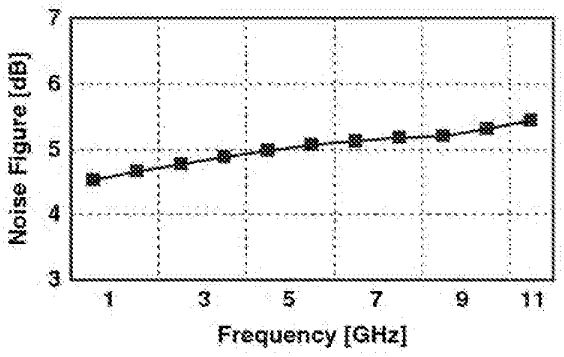


Fig. 6.12 Measured NF of the single path of the power combiner

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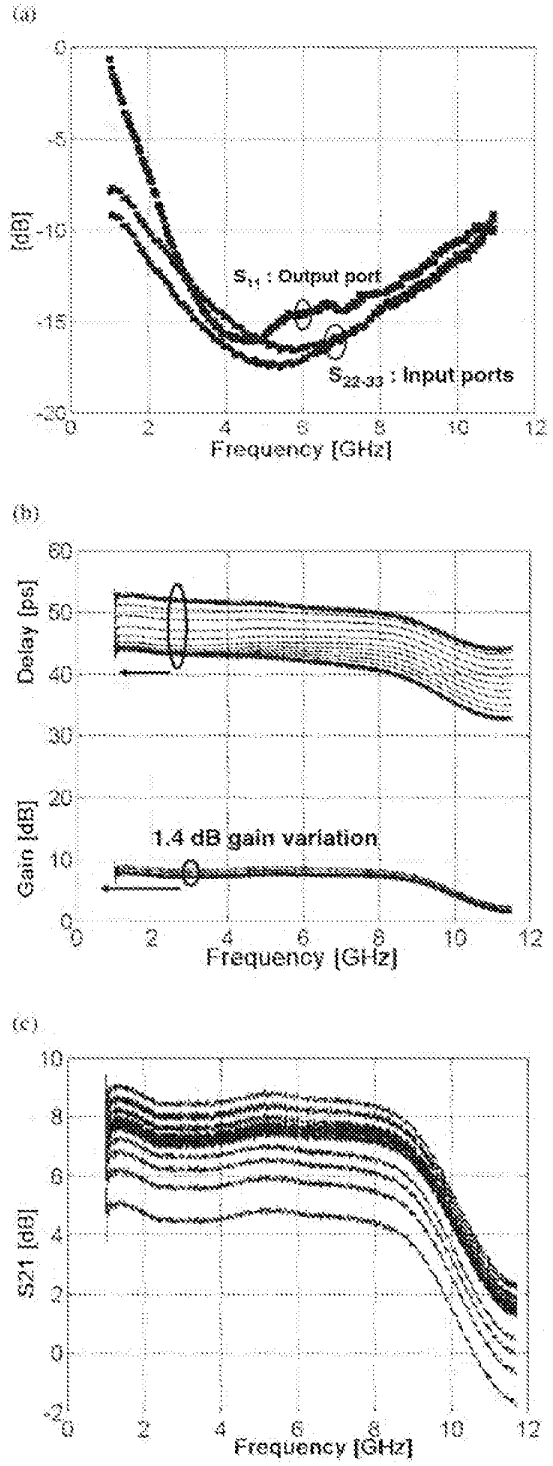


Fig. 6.13 Power splitter measurements: (a) return losses $S_{11,22,33}$ (b) Variable delay and gain variation during delay adjustment, and (c)Variable gain S_{21} (or S_{31}) by controlling the common-mode voltage of differential pair transistors

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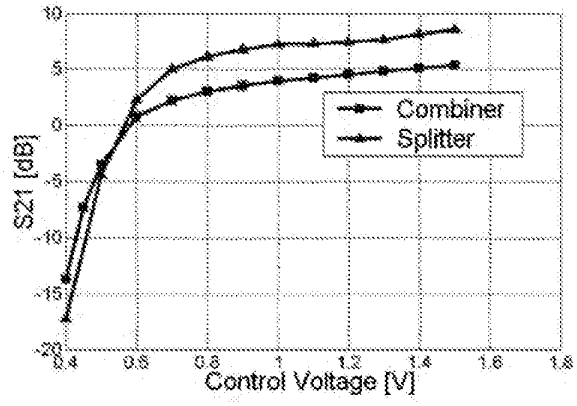


Fig. 6.14 Variable gain of power combiner and splitter

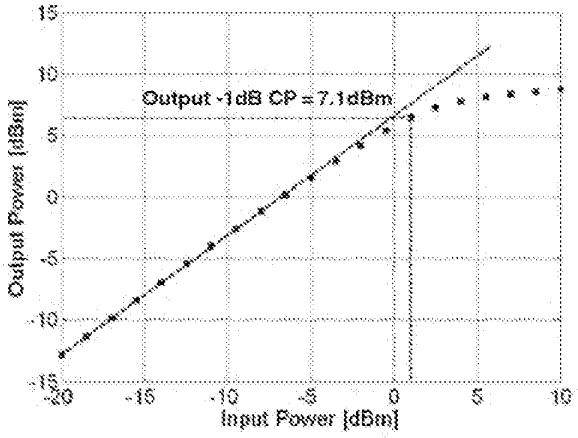


Fig. 6.15 Output–1dB compression point of power splitter

also the total transmitted power could be increased by $10\log(N)$ (which is equal to 3dB for $N = 2$). Therefore, the MA-UWB transmitter is capable of transmitting a total power of 10.1dBm.

Table 6.1 compares the performance of the proposed combiner and splitter with power combiner in [3] and the power splitter in [4], both of which implemented in GaAs MMIC technology. [3] and [4] only combine and split the power with equal delay and gain from each path without the capability of varying the gain and delay of each path independently. [6] implemented a single path variable delay/gain. However, the proposed work is a power combiner/splitter with

Table 6.1 Performance summary of the power combiner and splitter

REF.	RF [GHz]	Variable Gain [dB]	Variable Delay [ps]	Power [mW]	# of stages	Technology
Combiner	1–10.6	$-15 \sim 6$	$32 \sim 42$	15.3	2	CMOS
Splitter	1–10.6	$-16 \sim 9.5$	$43 \sim 53$	20.5	3	CMOS
[3]	4–40	3	N/A	46	2	GaAs
[4]	1–10	$0 \sim -2$	N/A	800	4	GaAs
[6]	1–11.2	$10 \sim 14.2$	$80 \sim 160$	125	8	SiGe

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capability of varying the delay and gain of each path, independently, for a 2 × 2 MA-UWB system. The 2-stage distributed active power combiner draws 8.5mA and the 3-stage distributed active power splitter draws 11.4mA from 1.8V supply voltage.

6.4 Summary

This chapter presented the design of CMOS active power combiners and splitters with wideband variable delay and gain using the distributed architecture. These circuits are the key components for use in multi-antenna MA-UWB point-to-point beamforming communication systems with multiple transmit and receive antennas. Fabricated in a 0.13μm CMOS process, the combiner/splitter's gain was independently controllable from −15 to 6dB and −16 to 9.5dB, respectively. The measured wideband variable delay of each path of the power combiner/splitter was 32 ~ 42 ps, and 43 ~ 53 ps across UWB frequency rang, respectively. The distributed active power combiner and splitter consume 8.5mA and 11.4mA from 1.8V supply voltage, respectively.

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Chapter 7
Conclusions

Ultra-wideband (UWB) is a promising technology for high data rate communication in short distances, as well as low data rate low power communication for object localization and sensor networks. From a communications theory perspective, the most important characteristic of UWB systems is their capability to operate in the power-limited regime while achieving high channel capacity. This attribute is comprehended using well-known Shannon's theory for the channel capacity. Furthermore, the spread-spectrum characteristics of wideband wireless systems and the ability of these systems to highly resolve the signal in multi-path fading channels due to the nature of the short duration of transmitting signals make the UWB systems a desirable wireless system of choice in a wide variety of high-rate, short-range communications including personal area networks. The main challenge lies in designing transceivers that are capable of transmitting and receiving wideband signals.

Distributed integrated circuits provide intrinsic wideband characteristics, which makes them potential candidate for use in UWB transceiver design. Recent advances in high-speed integrated circuit design in conjunction with continuous scaling of minimum feature sizes of semiconductor devices, particularly in CMOS technology, have renewed the interest in designing distributed circuits using on-chip artificial transmission lines. In fact, a comprehensive study in this book demonstrated the use of silicon-based distributed architectures in designing wideband circuits for UWB systems.

First, the design and analysis of a CMOS distributed low noise amplifier (DLNA) was demonstrated in Chapter 3. The performance-optimized DLNA can be employed in RF front-end of UWB receivers. A detailed analysis of noise was also presented, which takes into account all the noise sources and the non-zero correlations between them.

Next in Chapter 4, a novel distributed RF front-end for UWB IF receivers (UWB-DRF) was presented. To save the area and power of the distributed architecture, merged low-noise amplifier and mixers were explored and distributed along the LC transmission lines. A three-stage UWB-DRF incorporating composite LNTA/mixer cells with controllable gain and programmable input matching network was fabricated and the experimental results were presented in this chapter.

Chapter 5 introduced a novel distributed direct conversion RF front-end (DDC-RF) for use in UWB systems. The DDC-RF combines the idea of the distributed

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approach which provides wideband circuits, with IQ requirement of a direct conversion receiver. The unique distributed architecture uses composite cells of merged low-noise transconductance amplifier (LNTA) and mixers along the input RF TL. The main advantage of the proposed DDC-RF is that instead of using two different distributed receiver paths (illustrated in Chapter 4) for each in-phase (I) and quadrature-phase (Q) data to achieve wide-band characteristics of RF front-end, an area and power efficient architecture based on distributed concept for wideband characteristics of RF front-end was designed and implemented. Furthermore, deploying merged LNTA/mixer enables low-power design of the receiver architecture for UWB systems, while achieving superior linearity over the conventional distributed amplifiers. In addition, the baseband output signals are low or zero frequency, hence the output TLs in any conventional distributed circuits were omitted, resulting in less area occupation of the DDC-RF.

To extend the range of high data communication, also to achieve immunity to the multi-path fading, UWB systems can employ multi-antenna configuration at the receiver and the transmitter. Wideband variable delay and gain stages are then required in order to receive and transmit the wireless power in desired direction. To do so, distributed active power combiners and splitters with wideband variable delay and gain were designed and implemented in CMOS technology. Finally the experimental results of the fabricated prototypes were presented in this chapter.

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(54) Broadcast receiver adapted for analog and digital signals

(57) Background:
Digital satellite TV broadcasting systems use an analog IF input followed by an analog QPSK-demodulator and analog lowpass filters prior to A/D conversion. Normally, two A/D converters would be required for digital demodulation of the in phase and of the quadrature component.

Gist of the Invention

A first IF frequency of about 2 GHZ and a second IF of about 140 MHz allows to demodulate FM signals of 27 MHz bandwidth. A subsequent local 70 MHz local oscillator is followed by a lowered resolution A/D converter operating at about 100 MHz sampling frequency in a subsampling mode. A single A/D converter (7) is required only and allows high quality FM demodulation.

Advantages

Allows multi-standard front-end architecture, architecture is suited for digital and analogue input signals, the possible net data rate around 40MBit/s is even higher than required for DirecTV.

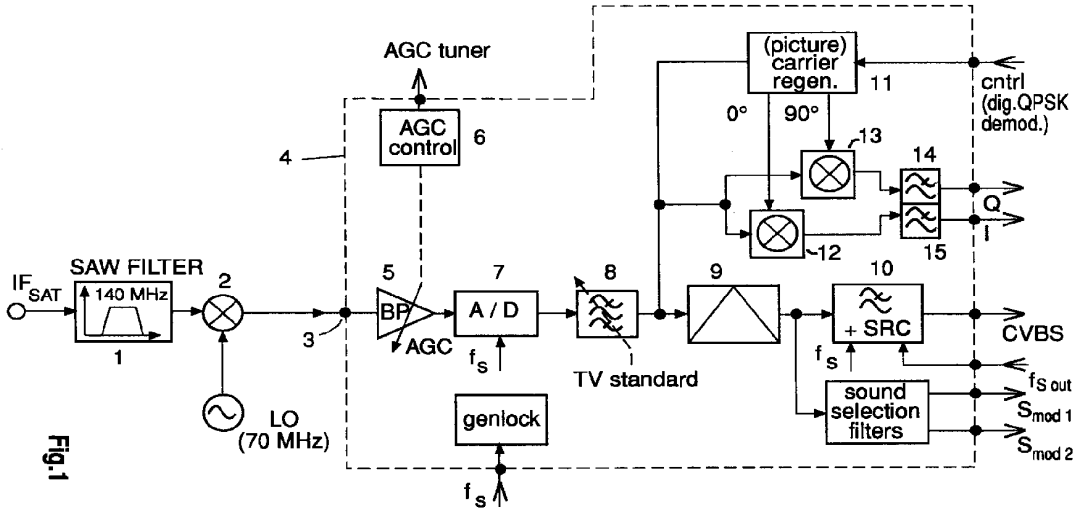


Fig.1

EP 0 696 854 A1

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Description

The invention relates to a broadcast receiver according to the introductory part of claim 1.

Digital TV broadcasting systems that transmit TV signals in digital data form through DBS have been developed aiming at next generation TV systems in several countries. Concerning the transmission the QPSK modulation is one of the most effective digital modulation scheme for high frequency spectrum efficiency. Proposed digital QPSK demodulator are still foreseen to have an analog IF input followed by a quadrature demodulator with lowpass filters prior to the A/D converters for the in phase and quadrature phase component. This approach makes sense in that way that analog IF signals cannot be directly digitised today and that a frequency down-conversion is necessary, anyhow. But on the other hand a quadrature demodulator for a high IF frequency is also difficult to realize. Another important drawback of the outlined digital QPSK demodulator is that it needs two A/D converters with each a high power consumption.

Now direct IF sampling is becoming more cost effective than traditional analog signal processing in some radio applications and it seems that the point has been reached where a digital solution for video IF signals should no longer be excluded in the satellite TV receiver design. This should also include the classical analog satellite reception with FM modulated signals.

It is an object of the invention to provide a broadcast receiver of the kind described which is suited for digital and analog input signals and using a common A/D converter only for analog and digital transmission via satellite.

According to the invention said IF signal is fed to a frequency down converter having its output connected to an A/D converter working with sub-sampling and having its output connected to an FM demodulator and a QPSK demodulator both working in digital signal processing technique.

The main advantages achieved by the present invention are the following:
The proposed architecture allows a digitising of the Sat-IF signals no matter that they are analog or digital ones. The robustness of the chosen modulation schemes allows further the application of an A/D-converter with reduced resolution at higher sampling frequencies in terms of usual video applications. Furthermore, there is only one A/D-converter necessary for the digitising instead of two or three for the classical solution which keeps the power consumption to a minimum. On the other hand by means of the digital signal processing the FM demodulation and also the QPSK demodulation can be realized with a high quality. The necessary analogue component count is nevertheless relatively small.

Nowadays, a multi-standard TV receiver should be able to function also as a satellite braodcast receiver. For that reason the outdoor unit supplies the satellite channels already down-converted in a frequency band covering 950 - 1750 MHz which should be handled by a multi-standard tuner. To take advantage of the double-conversion tuner the 1st-IF frequency should be around 2 GHz. In contrary to the terrestrial and cable transmission, the video signals are FM modulated (in case of the analog DBS transmission) and need, therefore, a significantly higher bandwidth, namely about 27 MHz according the approximation of he Carson formula. Consequently, the fixed bandpass filter in the 1st-IF circuit has to be enlarged by a factor between 2 and 3. If the assumed bandwidth is nearly tripled with respect to the terrestrial or cable reception, the 2nd-IF frequency should also be tripled to keep the relations. Otherwise, either the image frequency components on the 1st-IF band exert harmful influence on the system's performance or the necessary analogue filters become prohibitive expensive. Taking this statement into account, the 2nd-IF frequency should be in the order of 130 - 140 MHz. The assumed multi-standard tuner should, therefore, supply a second output for the 140 MHz Sat-IF signal.

In order that the invention might be better understood, the invention will now be described by using the accompanying drawing. In the drawing

Fig. 1 shows a block diagram of a television receiver working according to the present invention; and

Fig. 2 shows frequency spectra for the conversion of the analogue Sat-IF into a digital IF signal.

In Fig. 1 the incoming IF signal which may come from an outdoor station is fed to SAW(surface acoustic wave) filter 1 and then to a mixer 2 which is fed by oscillator LO having a frequency of 70 MHz. The frequency down-converted signal is fed to input 3 of circuit 4. Circuit 4 includes an amplifier 5 controlled in amplitude by AGC control circuit 6, an A/D converter 7 controlled by sampling frequency fs of 100 MHz, bandpass-filter 8, FM demodulator 9 and low pass filter 10 providing at it's output the CVBS signal. Further are provided a picture carrier regenerator 11 generating carriers with phase of 0° and 90° for QPSK demodulation, synchronous demodulators 12, 13 for QPSK quadrature demodulation and low pass filters 14, 15 providing signal Q,I at outputs of circuit 4.

In the following the operation of said circuit will now be described in combination with Fig. 2.

At first the tuner output signal passes through the SAW filter 1 with a centre frequency of 140 MHz which suppresses a great deal of the adjacent channel signal components (see Fig. 2a, 2b and 2c). This is an important issue because the demodulator input is in general composed of the useful signal plus the co-channel and two adjacent channel interfering signals. The succeeding mixer stage 2 is operated with a local oscillator frequency between 60 and 70 MHz which realizes a frequency transposition into an IF signal of around 75 MHz (see Fig. 2d and 2e). The down-converted If signal then goes into AGC amplifier 5 with an internal bandpass limitation before the IF signal enters the input of A/D-con-

verter 7. The AGC amplifier 5 has to make sure that the full dynamic range of the A/D-converter 7 is exploited to keep the quantizing noise to a minimum. The sampling frequency of the A/D-converter 7 should amount up to 100 MHz to allow sufficient large frequency spaces between the periodic spectra which could be occupied by the remainder of the adjacent channel signals, if the attenuation of the SAW filter 1 is not sufficient (see Fig. 2f). The A/D-converter 7 is operated in the sub-sampling mode, but this does not cause any aliasing problems because of the bandlimited input signal. Owing to the high sampling frequency, the effective dynamic resolution of the A/D-converter 7 may be somewhat reduced with respect to the nominal resolution. It is expected that due to the FM modulation the distortions can be neglected. The following bandpass filter 8 (see Fig. 2g) with an adaptively controlled bandwidth selects the desired signal with a minimal remainder of the adjacent channel signals. The FM demodulator 9 converts the IF signal into the CVBS signal and the subcarrier modulated sound signals, which have to be separated by lowpass and bandpass filters. Especially for the succeeding colour decoding part the sampling rate should be adapted to its clock frequency. The lowpass filter is, therefore, also used as sampling rate converter.

The DBS-band planning was laid down in the WARC '77 specification. It fixes a maximum signal bandwidth of 27 MHz, and the transponder bandwidth of DBS satellites have been designed accordingly. Therefore, it can be assumed a signal bandwidth of about 27 MHz as a stable specification for a D-DBS system allowing a net data rate of around 40 Mbits/s which is more than foreseen in the Direct TV proposal. This figure implies that something like a TCM-8 PSK modulation is used instead of any amplitude modulation schemes (like 16 QAM) which represents a bandwidth- but not power efficient modulation scheme. This point is quite important when a highly non-linear channel like the satellite transponder is used.

For the reception of digitally transmitted video signals the analogue pre-processing blocks can be kept. In the digital part a quadrature mixer and a special carrier regenerator have to be added in order to demodulate QPSK modulated signals. The carrier regenerator can be controlled by the digital QPSK demodulator which is not depicted in Fig. 1. The quadrature demodulator is followed by lowpass filters to produce an in phase and a quadrature symbol pattern at the output. The digital quadrature demodulation offers the advantage that it can be realized without any phase and amplitude matching problems between the I an Q channel. Furthermore, this architecture needs only one A/D-converter instead of two in the classical QPSK demodulator or even three, if also the digitizing of the analog FM transmission is taken into account.

Claims

1. Broadcast receiver adapted for analogue and digital transmitted signals using FM-modulation and QPSK-modulation, said signals being converted into an analogue IF-signal, **characterized in that** said IF signal is fed to a frequency down converter (2) having its output connected to an A/D-converter (7) working with subsampling and having its output connected to an FM-demodulator (9) and a QPSK-demodulator (12, 13) both working in digital signal processing technique.

2. Receiver according to claim 1, **characterized in that** the A/D-converter (7) operates with a sampling frequency of about 100 MHz.

3. Receiver according to claim 1, **characterized in that** the sampling frequency has such a value that two spectra of the signal lie below said sampling frequency.

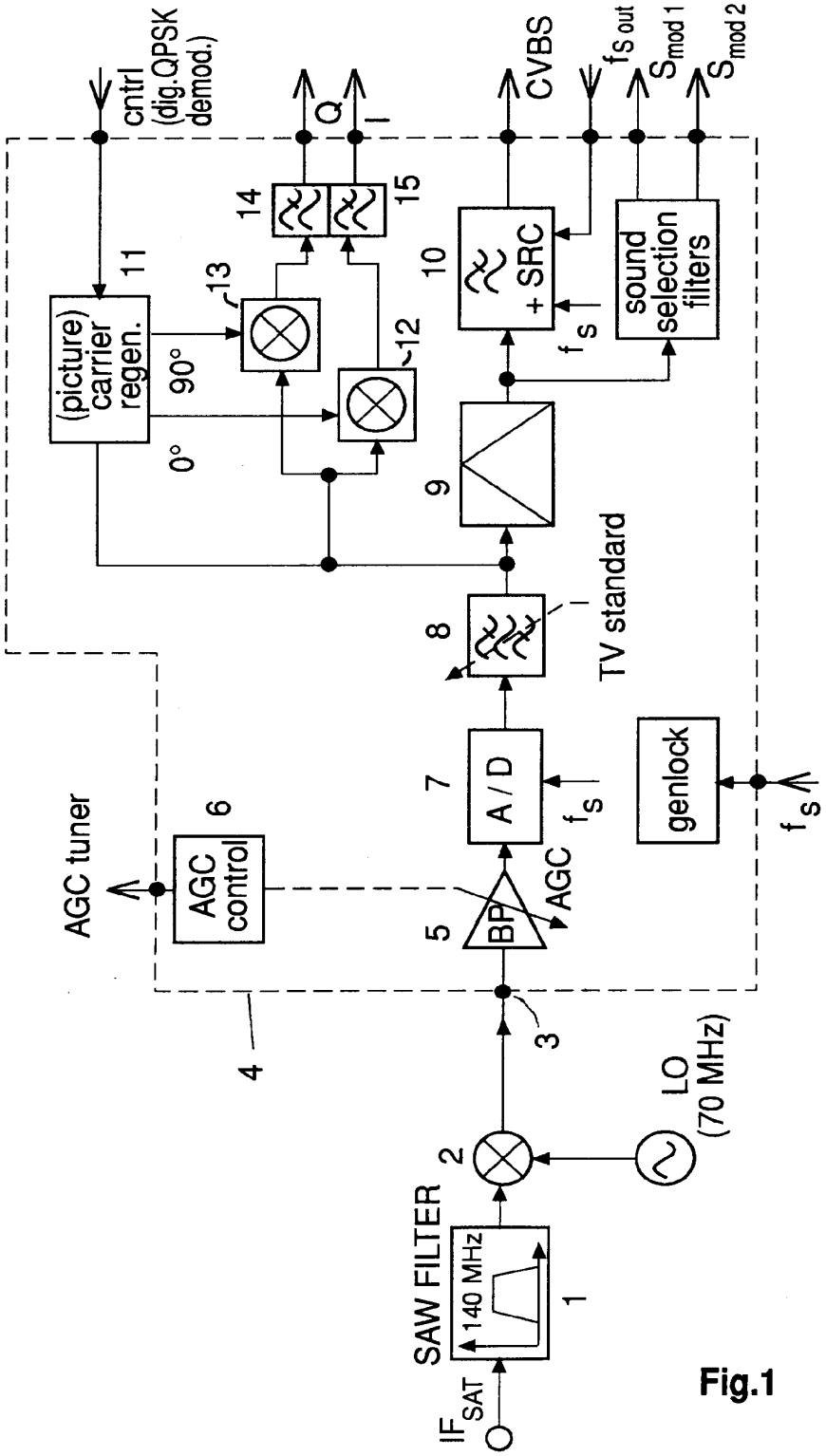

cntrl (dig.QPSK demod.)
Q
I
CVBS
$f_{S\,out}$
$S_{mod\,1}$
$S_{mod\,2}$
14
15
11
13
12
10
+ SRC
sound selection filters
(picture) carrier regen.
90°
0°
f_S
9
8
TV standard
AGC tuner
AGC control
6
7
A / D
genlock
5
BP
AGC
4
3
LO (70 MHz)
2
SAW FILTER
140 MHz
1
IF_{SAT}

Fig.1

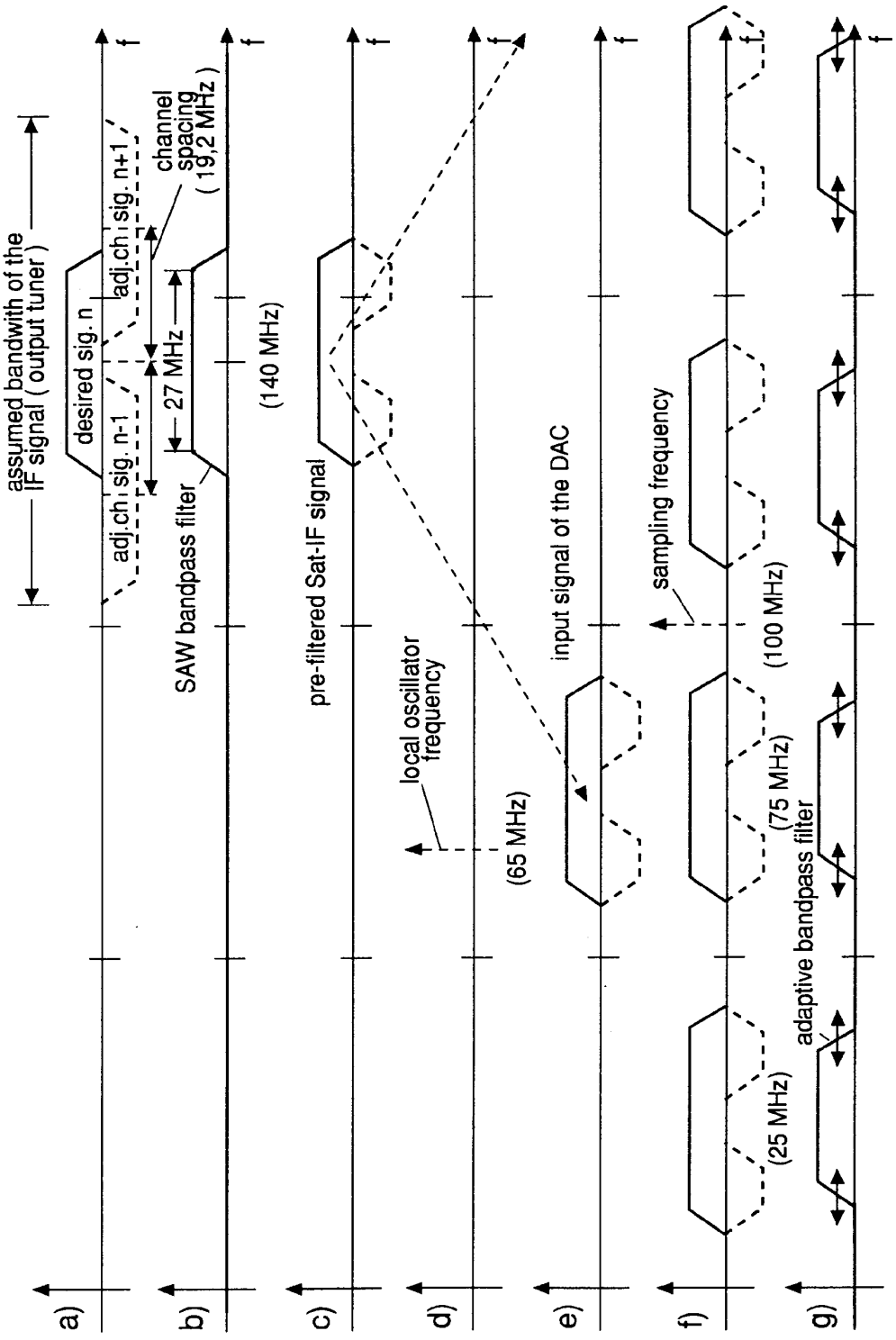

assumed bandwith of the IF signal (output tuner)
desired sig. n
adj.ch. sig. n-1
adj.ch. sig. n+1
channel spacing (19,2 MHz)
27 MHz
SAW bandpass filter
(140 MHz)
pre-filtered Sat-IF signal
local oscillator frequency
(65 MHz)
input signal of the DAC
sampling frequency
(100 MHz)
(75 MHz)
adaptive bandpass filter
(25 MHz)
a)
b)
c)
d)
e)
f)
g)
f

Fig.2

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 11 1940

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	ELECTRONIC DESIGN, vol. 39, no. 10, May 1991 CLEVELAND,OH,US, pages 67-78, XP 000234611 GROSHONG ET AL 'Undersampling Techniques Simplify Digital Radio' * page 68, column 2, line 13 - page 73, column 2, line 4; figure 2 *	1-3	H04B1/26 H04B1/16
A	US-A-5 179 360 (SUZUKI) * column 1, line 1 - column 2, line 63; figure 1 *	1-3	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H04B
H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 August 1995	Andersen, J.G.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

CERTIFICATE OF ELECTRONIC SUBMISSION

I hereby certify this document is being electronically filed with the U.S. Patent and Trademark Office on:

Date: June 18, 2024 Name: Hao Tan Reg. No. 73,711 Signature: / Hao Tan /

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Owner: Entropic Communications, Inc.
Inventors: Madhukar Reddy et al.
App. No.: 90/019,255
Filed: September 20, 2023
Conf. No.: 5785
Examiner: LIE, ANGELA M
Art Unit: 3992
Title: WIDEBAND TUNER ARCHITECTURE
Docket No.: 189005.TR003

SUMMARY OF TELEPHONE INTERVIEW

Patent Owner thanks the Examiners for their time and attention in this matter. During the interview conducted on June 6, 2024 at 10 am (Easten). Patent Owner and Examiners discussed the following:

1. The rejection of claims 1 and 11 under pre-AIA 35 U.S.C. 103(a) as allegedly being unpatentable over McNeely (WO 2006/119490) in view of Pugel (WO 2007/145637).

2. The rejection of claims 1 and 11 under pre-AIA 35 U.S.C. 103(a) as allegedly being unpatentable over Pugel (WO 2007/145637) in view of Gomez (US 8,224,274).

To overcome claim rejections under pre-AIA 35 U.S.C. 103(a), Patent Owner presented arguments on differences between the claims and the cited references and that the combinations of references are not operable. The Examiner advised the Patent Owner to explain those arguments in more detail and emphasize why the combinations would not be successful and/or not operational concerning the motivation to combine. No agreement was reached regarding patentability of the claims.

Respectfully submitted,

Date: June 18, 2024

/ Hao Tan/

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CERTIFICATE OF ELECTRONIC SUBMISSION
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Owner: Entropic Communications, Inc.

Inventors: Madhukar Reddy et al.

App. No.: 90/019,255

Filed: 09/20/2023

Conf. No. 5785

Examiner: LIE, ANGELA M

Art Unit: 3992

Title: WIDEBAND TUNER ARCHITECTURE

Docket No.: 189005.TR003

RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop *Ex Parte Reexam*
Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner,

In response to the Non-Final Office Action dated March 18, 2024, please consider the following remarks.

A **Listing of Claims** begins on page 2 of this paper.

Applicant's **Remarks** begin on page 6 of this paper.

LISTING OF CLAIMS

No claim is amended. The listing of all claims of the Patent is provided for reference only. Only two claims, Claims 1 and 11, are rejected in the OA:

1. A wideband receiver system comprising:

a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

digital circuitry configured to:

select said plurality of desired television channels from said digitized plurality of frequencies; and

output said selected plurality of television channels to a demodulator as a digital datastream.

2. The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface.

3. The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface.

4. The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.

5. The wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises:

a first ADC configured to generate a digital in-phase signal; and

a second ADC configured to generate a digital quadrature signal.

6. The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.

7. The wideband receiver system of claim 6, wherein:

prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and

after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.

8. The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.

9. The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter.

10. The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels.

11. A method comprising:

in a wideband receiver system:

downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and

outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.

12. The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface.

13. The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface.

14. The method of claim 11, comprising:

generating, by a first mixer of said mixer module, an in-phase signal; and

generating, by a second mixer of said mixer module, a quadrature signal.

15. The method of claim 11, comprising:

generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and

generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.

16. The method of claim 15, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry.

17. The method of claim 16, wherein:

prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and

after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum.

18. The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.

19. The method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter.

20. The method of claim 11, comprising decimating, by said digital circuitry, one or more of said selected plurality of desired television channels prior to said outputting of said selected plurality of television channels.

REMARKS

Claims 1 and 11 are subject to reexamination. No new matter has been added. Patent Owner respectfully requests reconsideration of the claims in view of the following remarks. Patent Owner respectfully thanks the Examiner for the opportunity to discuss the rejection telephonically on June 6, 2024.

References Relied Upon in First Rejection

McNeely

World Intellectual Property Organization Publication No. WO 2006/119490 ("McNeely") relates to "an apparatus and method for performing frequency translation." (McNeely at Abstract). In particular, McNeely "describes a circuit used for processing satellite signals." (*Id.* at 5:27–28). McNeely explains that during receipt of signals in a typical satellite system installation at a customer home, satellite transponders located on satellites 102a–c transmit satellite signals to satellite dishes 104a–c located at or near the customer's home. (*Id.* at 6:10–18; Fig. 1). LNBs in the satellite dishes amplify and convert the satellite signal from an 11–13 GHz range to an "L-band signal" in the 1–2 GHz range. (*Id.* at 6:26–28).

McNeely explains that the L-band signals in their entirety cannot be supplied through a single coaxial cable for delivery into the customer home because the L-band signals occupy too much frequency bandwidth. (*Id.* at 7:6–9). Accordingly, McNeely discloses a frequency translation module (FTM) 110 located outside or very near to the entry point into the customer home, which performs a "preselection" of certain physical channels and outputs a signal comprising multiple channels over a single coaxial cable into the customer home. (*Id.* at 7:11–26). From there, the signal is provided to terminals and/or set-top boxes within the customer home, each of which receives the signal comprising multiple channels, tunes to the desired physical channel within the

signal, demodulates the physical channel to produce a transport stream, and extracts the desired bitstream(s) from the transport stream. (*Id.* at 7:26–8:7).

Notably, McNeely is directed to improvements within the FTM itself. McNeely explains that "a conventional FTM contains analog signal processing used for the filtering, mixing, and recombining of the L-band signals," but "[t]he utilization of digital signal processing within the FTM structure permits greater flexibility and removes some of the limitations of analog signal processing." (*Id.* at 8:24–31). McNeely does ***not*** teach any improvements to the tuning of television channels, but rather relies upon the use of conventional set-top boxes within the customer home (downstream from the FTM) to perform the tuning and demodulation. (*Id.* at 8:3–7). McNeely specifically notes that "the process used by the FTM 110 ***is different from a direct tuning*** of those certain physical channels since other energy besides the selected channel may be present, and ***the channels are then recombined*** to form a new signal for further distribution." (*Id.* at 7:17–21 (all emphasis added unless otherwise noted)).

Pugel

World Intellectual Property Organization Publication No. WO 2007/145637 ("Pugel") relates to a "multichannel digital cable tuner." (Pugel at Title). In one embodiment, a multichannel receiver circuit includes a plurality of amplifier-filter circuits, a plurality of analog-to-digital converters, a digital tuner, and a plurality of demodulator circuits. (*Id.* at [0023]). Pugel discloses that the plurality of amplifier-filter circuits segregates the analog input signal into a plurality of separate analog signals of differing frequency ranges, or "bands." (*Id.* at [0024]). For example, an arrangement of three amplifier-filter circuits might be used, wherein the three circuits are configured to process frequencies from 5–300 MHz, 300–600 MHz, and 600–900 MHz respectively. (*Id.* at [0028]). Each separate analog signal band is then converted from analog to digital form by an analog-to-digital converter (ADC). (*Id.* at [0024]).

Pugel next discloses that the converted digital signals are coupled to digital tuner 130, which demultiplexes the converted digital signals to generate a plurality of digital channel signals. (*Id.* at [0027]). Pugel notes in particular that "[t]he digital tuner 130 may include a channel selector 315 to permit selection of one or more particular digital channels desired to be recovered." (*Id.* at [0038]). Each digital channel signal is then coupled to a separate demodulator, which performs demodulation and forward-error-correction (FEC) operations appropriate for the content of that digital channel. (*Id.* at [0027]).

Response to First Rejection under 35 U.S.C. § 103

Claims 1 and 11 are rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over McNeely in view of Pugel.

McNeely Is Not Analogous Art

The OA fails to demonstrate that McNeely is analogous art. "A reference qualifies as prior art for an obviousness determination . . . only when it is analogous to the claimed invention." *In re Klein*, 647 F.3d 1343, 1348 (Fed. Cir. 2011). An obviousness ground that relies upon non-analogous art fails. *Id.*, 1352. To be analogous, a reference must be either (1) from the same field of endeavor as the patent-at-issue, or (2) reasonably pertinent to the particular problem with which the inventor of the challenged patent is involved. *In re Clay*, 966 F.2d 656, 658-59 (Fed. Cir. 1992). McNeely meets neither criterion.

As its title suggests, the '362 Patent is directed to a "wideband tuner architecture." *See Airbus S.A.S. v. Firepass Corp.*, 941 F.3d 1374, 1380-81 (Fed. Cir. 2019) (affirming Board's finding of field of endeavor based on "the title of the [] patent and the preamble of a . . . claim"). The '362 Patent explains that tuners are "[r]eceivers used to down-convert and selectively filter TV channels." (1:24-27). This is why, for example, Claim 1 recites "[a] wideband receiver system

comprising . . . digital circuitry configured to: ***select*** said plurality of desired television channels." The '362 Patent further states:

> Existing tuners for these applications down-convert a swath of channels to an intermediate frequency, which are then sent to a demodulator. Because the swath of channels is not contiguous, this swath includes the desired channels as well as undesired channels. The demodulator employs a high-speed data converter to capture this swath of desired and undesired channels in the digital domain and subsequently filters out the desired channels.

(1:27-34). The '362 Patent explains that one disadvantage of existing tuners is that achieving a high bandwidth "would require a very expensive digital processing circuitry such as very high-speed analog to digital conversion and high-speed processor in the demodulator." (2:20-23). Accordingly, the '362 Patent aims to improve upon wideband tuner architecture by "eliminat[ing] the need of expensive data conversion, filtering and channel selection on the demodulator side" and by "remov[ing] undesired channels from the signal path at an early stage, thus reliev[ing] the large dynamic range requirement in the demodulator." (6:60-64).

McNeely is not directed to a tuner, nor does it attempt to solve the problem of eliminating expensive data conversion, filtering, and channel selection from the demodulator side of a tuner. As explained above, McNeely is directed to an improved frequency translation module (FTM). McNeely explains that an FTM is used in satellite television systems because the signals travelling from the satellite dishes into the customer home occupy too much frequency for delivery over a single coaxial cable. (McNeely, 7:6-9). The FTM addresses this problem by performing what McNeely calls a "preselection" of certain physical channels, a process even McNeely acknowledges is different than tuning. (*Id.* at 7:11–26).

McNeely makes it explicitly clear that its FTM is ***not*** a tuner. This is because "the process used by the FTM 110 is ***different from a direct tuning*** of those certain physical channels since ***other energy besides the selected channel may be present***, and the channels are then recombined

to form a new signal for further distribution." (*Id.* at 7:17–21 (emphasis added)). In other words, McNeely's FTM filters out some—but not all—of the undesired channels and outputs a combination of desired and undesired channels. And this is because McNeely is only concerned with making sure the signal bandwidth is narrow enough for delivery into the home on a single coaxial cable, rather than making sure that only the selected channels arrive at the demodulator side of a tuner. This is also why McNeely still relies on the use of conventional terminals and/or set-top boxes to perform tuning prior to demodulation, and why it is silent as to the architecture of those boxes (confirming that the set top boxes would still be responsible for tuning). (*Id.* at 8:1-7).

Thus, McNeely and the '362 Patent are directed towards entirely different problems, and the issues addressed by McNeely have no bearing upon the tuning of selected channels, nor the elimination of expensive data conversion, filtering, and channel selection circuitry from the demodulator side of a wideband tuner.

Thus, the OA fails to demonstrate that McNeely is analogous art to the '362 Patent.

McNeely Does Not Disclose or Suggest "Select[ing] Said Plurality of Desired Television Channels"

Claim 1 requires digital circuitry configured to "select said plurality of desired television channels from said digitized plurality of frequencies." Likewise, claim 11 requires "selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies." The Examiner appears to take the position that this "selecting" is performed by McNeely's digital channel selector 230 (*See* OA at 4), which is a component of frequency translation module (FTM) 110. (McNeely at 9:1–5).

However, McNeely makes it expressly clear that FTM 110 does not "select said plurality of desired television channels" as required by the claims. As McNeely explains:

> The FTM 110 extracts certain ranges of frequencies containing selected physical channels as portions of the three L-band signals provided. . . . The process used by

> the FTM 110 may be described as a preselection of certain physical channels. However, the process used by the FTM 110 is different from a direct tuning of those certain physical channels since other energy besides the selected channel may be present, and the channels are then recombined to form a new signal for further distribution.

(*Id.* at 7:11–21). In other words, rather than selecting (and outputting) the desired television channels, McNeely's FTM selects ***ranges of frequencies containing the desired channels*** (and undesired channels). (*Id.* at 7:11–13). McNeely itself characterizes this as only a "preselection" because the outgoing signal still contains a mix of desired and undesired channels. (*Id.* at 7:15–19). This is why McNeely still relies on the set-top boxes to actually tune to the desired channels before those channels can be demodulated. (*Id.* at 8:3–7).

Therefore, the Examiner has not shown that the alleged combination discloses or renders obvious "select[ing] said plurality of desired television channels."

The OA Fails to Allege a Rational Basis to Modify McNeely Based On Pugel's Alleged Teaching of "Outputting the Selected Plurality of Television Channels to a Demodulator"

The Examiner acknowledges that McNeely "does not explicitly teach outputting the selected plurality of television channels to a demodulator." (OA at 4). In fact, McNeely discloses *neither* outputting to a demodulator *nor* outputting a digital datastream, both of which are required by claims 1 and 11.

As depicted in Figure 2, McNeely's FTM outputs an analog signal. (McNeely at Fig. 2).

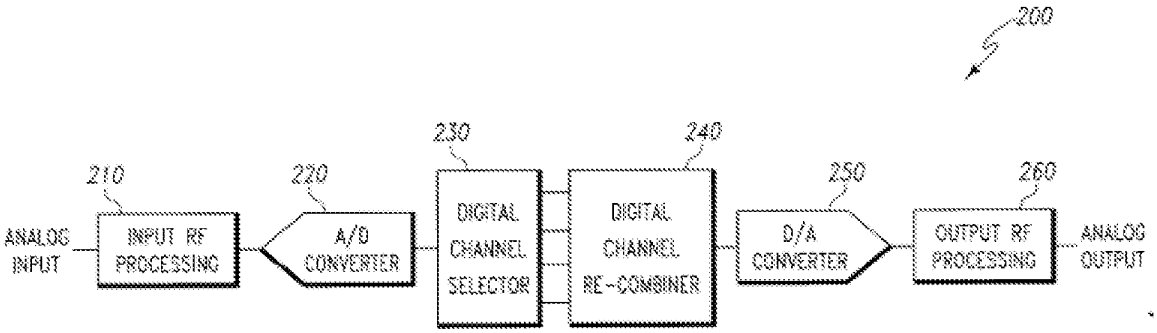


Fig. 2

Reproduced Fig. 2 of McNeely

This is because, as explained above, McNeely is not concerned with tuning the desired channels so that they are ready for demodulation. Rather, McNeely is concerned with reducing the bandwidth of the analog signal travelling from the satellite dishes into the home, so it is narrow enough to transmit across a single coaxial cable. Once inside the home, the signal is transmitted to tuner devices (*e.g.*, set-top boxes). (*Id.* at 19:25–28). But McNeely does not teach anything about the architecture of these set-top boxes. (*See id.* at 8:3–7).

The Examiner asserts that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of McNeely and Pugel and utilize Pugel's demodulator ***to process a digital datastream of McNeely***." (OA at 5). This assertion ignores the actual teachings of *McNeely*, which confirm that there is no "digital datastream of McNeely;" instead *McNeely* outputs an analog data stream.

However, the OA does not establish a rational basis for combining the teachings of these two references. As an initial matter, McNeely relates to an FTM that explicitly does not perform

tuning. (McNeely at 7:17–21). Therefore, it is unclear why a person of ordinary skill in the art would be motivated to combine McNeely's teachings with Pugel, which relates to a "multichannel ***digital cable tuner***." (Pugel at Title). Notably, the Applicant for both McNeely and Pugel is Thompson Licensing, yet there is no incorporation of McNeely's satellite FTM into the later filed Pugel.

Secondly, because McNeely's FTM does not perform tuning, it is unclear how a person of skill in the art could expect to modify McNeely so that it outputs a digital signal directly to a demodulator, as allegedly taught by Pugel. This would skip the tuning step altogether. Moreover, it would go against the entire purpose of McNeely, which is to transmit a signal into the home on a single coaxial (*i.e.*, analog) cable. The OA does not address how a person skilled in the art would be motivated to look past that issue in combining McNeely with Pugel.

Therefore, the Examiner has not shown that it would be obvious to combine McNeely with Pugel's alleged teaching of "output[ting] said selected plurality of television channels to a demodulator as a digital datastream."

Therefore, the combination of McNeely and Pugel fails to teach or suggest all features recited in independent claims 1 and 11 for at least the reasons above. A person of ordinary skill in the art would not have combined McNeely and Pugel. Even if the combination were proper, it still would not teach the claimed wideband receiver system and method. Therefore, claims 1 and 11 are allowable over the cited art.

References Relied Upon in Second Rejection

Pugel

Pugel is described above with respect to the first rejection.

Gomez

U.S. Patent No. 8,224,274 ("Gomez") relates to a scalable architecture for a satellite channel switch. (Gomez at Title). More specifically, Gomez "relates to processing one or more input channels to a frequency translation module through a scalable switch architecture." (*Id.* at 1:17–20). Gomez explains that "[a] frequency translation module (FTM) enables a user to selectively switch the signals received from each satellite antenna and deliver these signals to an IRD located within a household." (*Id.* at 1:38–41). Gomez states there is a need for "a method or apparatus for implementing a scalable switch architecture for a FTM that minimizes circuit area and power consumption." (*Id.* at 1:55–57). Accordingly, Gomez discloses "digital frequency converters and filters, which are compact in modern integrated circuit technology and consume less power than their analog counterparts, may be used to implement a scalable FTM architecture." (*Id.* at 1:61–65).

Response to Second Rejection under 35 U.S.C. § 103

Claims 1 and 11 are rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Pugel in view of Gomez.

The OA Fails to Allege a Rational Basis to Modify Pugel Based on Gomez's Alleged Teaching of "A Mixer Module"

Independent claim 1 recites "a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels." Independent claim 11 similarly recites "downconvertering, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of

desired television channels and a plurality of undesired television channels." The Examiner acknowledges that Pugel "does not explicitly disclose that the downconverting is performed by a mixer module of the wideband receiver system." (OA at 6). The Examiner asserts that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Pugel and Gomez and utilize Gomez's teaching about employing a mixer to perform down-conversion in order to efficiently processing [*sic*] inputted signals." (OA at 7). However, the OA does not establish a rational basis for combining these two references.

As an initial matter, the OA does not explain why a person skilled in the art would initially look to modify Pugel in view of Gomez. Pugel relates to a "multichannel digital cable tuner." (Pugel, Title). Specifically, Pugel aims to "permit[] substantially simultaneous reception of multiple digital cable channels ***within a single digital receiver circuit*** suitable for use with conventional cable delivery systems and at a reasonable cost." (*Id.* at Abstract). Accordingly, Pugel's "single digital receiver circuit" includes both a tuner and demodulators. (Pugel, Fig. 1). In contrast, Gomez relates to channel switching in a satellite FTM. (Gomez at 1:15–57). Although Gomez discloses that its FTM may contain one or more tuners (*Id.* at 1:41), Gomez teaches that its FTM is separate from the receivers, which Gomez refers to as integrated receiver decoder(s) [IRD], and which Gomez confirms are located within the home ("IRD located within a household"). (*Id.* at 1:38-41). Gomez does not concern itself with the architecture or features of the receiver, instead describing functionality that exists elsewhere in the signal delivery system. And in fact, Gomez goes against the very idea of Pugel, which is directed to a single digital receiver circuit that performs both tuning and demodulation. As such, there is no basis to look to Gomez to modify Pugel.

Next, the Examiner appears to specifically rely on "mixer 301" in Gomez as allegedly "downconvert[ing] the desired channel in RF signal." (OA at 6 (citing Gomez at 4:6-19)). However, there are a number of problems with this reading of Gomez.

First, the claim language requires "downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels." The relied upon mixer 301 of Gomez downconverts ***only*** the desired channel(s), as the down-conversion happens ***after*** the tuning to the desired frequency has occurred:

> Mixer 301 receives RF input signal 101 from amplifier 300 and also receives a local oscillator (LO) signal from PLL 304. For direct conversion, the frequency of PLL 304 is tuned to the frequency of the desired channel in RF input signal 101 so that it is down-converted to baseband, for further processing. For example, if the desired channel in RF input signal 101 is at 100 MHz, then PLL 304 is tuned to 100 MHz, so that mixer 301 down-converts the desired channel in RF signal 101 to DC.

(Gomez at 4:10–19 (emphasis added)). There is simply no basis to modify any teaching of Pugel in view of Gomez's specific form of down-conversion, without relying on the '362 Patent as a roadmap.

The OA does not explain why a person of ordinary skill in the art would be motivated to combine Pugel with Gomez to achieve the claim language. If anything, the combination of Pugel and Gomez would lead the person skilled in the art ***away*** from the claim language by directing them to downconvert only the desired channels.

Second, the Examiner relies on Pugel's disclosure of downconverting a digital signal. (Pugel at Cl. 18; OA at 5). However, Gomez does not teach the use of a mixer to perform digital downconversion. Rather, Gomez teaches that mixer 301 is an ***analog*** mixer. This is evident because mixer 301 receives an RF input signal (4:10-12) and because Figure 3 of Gomez does not disclose any digitization of the RF signal. (*Id.* at Fig. 3, 4:4-46). Gomez also characterizes mixers

generally as an example of an "analog component." (*Id.* at 1:47-49). And indeed, Gomez elsewhere discloses mixers that explicitly convert an analog signal (*e.g. id.* at Abstract, 2:11-13, 9:23-25, 10:54-56). While Gomez does disclose that "Mixer 1201 receives digital data" and that "Mixer 1205 up-converts the frequency of the digital signal," Gomez does not indicate that either of these two mixers performs ***down***-converting. (*Id.* at 7:66, 8:46-47). The OA does not explain why a person skilled in the art would find it obvious to modify Pugel based on Gomez to arrive at the claim language, when Gomez does not teach the use of a mixer to perform the digital downconversion that occurs in Pugel.

Third, Gomez actually teaches that there are ***disadvantages*** with using analog components such as mixers, and one of the stated goals of Gomez is to minimize the number of such analog components that are used:

> Conventional approaches to the design of tuners employ analog components, such as fixed-frequency filters, mixers, and local oscillators. Consequently, FTMs require extensive hardware, including at least one oscillator and one mixer for each tuner, making the module costly and too large for some applications. Furthermore, as the channel capacity of a FTM grows, the module consumes more power due to the increase in analog components. What is needed is a method or apparatus for implementing a scalable switch architecture for a FTM that minimizes circuit area and power consumption.

(Gomez at 1:47-57). In this regard, contrary to the OA, Gomez actually suggests against the proposed combination that the OA advances. *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) (A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention). The OA does not explain why a person skilled in the art, apprised of this language, would be motivated to introduce mixers into Pugel's multichannel digital cable tuner.

Therefore, the Examiner has not shown that it would be obvious to combine Pugel with Gomez's alleged teaching of "a tuner which selects and downconverts a desired or selected channel

from a RF input signal" (OA at 6), or that the proposed combination would render obvious this claim element. A person of ordinary skill in the art would not have combined Pugel and Gomez as the OA suggests. Therefore, claims 1 and 11 are allowable over the cited art.

Conclusion

Thus, withdrawal of the rejections under 35 U.S.C. 103 are respectfully requested. These remarks are believed to address all of the rejections in the instant Office Action. Applicant respectfully requests that the rejections be withdrawn and that a Notice of Allowance be granted. The Examiner is respectfully requested to contact the undersigned in the event that a telephone interview would expedite consideration of the application. Should any fee be required in this response, please charge the fee due to Deposit Account 60-2239.

Respectfully submitted,

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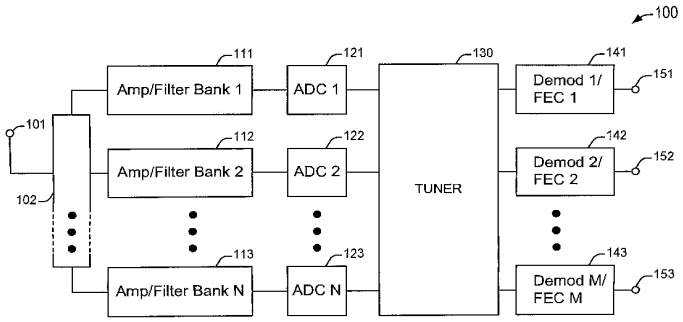
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(54) Title: MULTICHANNEL DIGITAL CABLE TUNER



(57) Abstract: A method and apparatus is presented for simultaneous reception of a plurality of digital RF channels. Specifically, N amplifier-filter circuits (111, 112, 113) are configured to receive and separate a multichannel analog RF input signal into N analog signals, each including a different frequency band. N analog-to-digital converters (121, 122, 123) are provided, each respectively coupled to one of the N amplifier-filter circuits (111, 112, 113) and configured to receive an analog signal and generate a respective digital signal. A digital tuner (130) is coupled to receive and demultiplex the N digital signals generated by the N analog-to-digital converters (121, 122, 123), thereby recovering M digital RF channels. M demodulation circuits (141, 142, 143) are provided for performing demodulation and forward-error-correction of the M digital RF channels (see FIG. 1). This combination of components permits substantially simultaneous reception of multiple digital cable channels within a single digital receiver circuit suitable for use with conventional cable delivery systems and at a reasonable cost.

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MULTICHANNEL DIGITAL CABLE TUNER

Field of the Invention

[0001] The present invention relates to television communications and, in particular, to an apparatus and method for multi-channel television reception.

Background of the Invention

[0002] In order to accommodate the increasing demands of television consumers, cable television (cable TV or CATV) broadcasters have transformed themselves in recent years to provide digital (as opposed to traditional analog) channels among their broadcast content. Cable TV broadcasters have employed digital technology to, for example, increase the number of offered channels, add per-channel programming information, and provide remote-interaction functionality such as pay-per-view (PPV) movies and sporting events.

[0003] As the benefits of digital cable television have become known, consumer demand has continued to rise, along with demand for increased variety of content. This demand for increased variety has reached the end-user level, where several users within a single household may prefer to enjoy different cable television programs simultaneously. Because digital cable television receivers, or set top boxes (STBs), were previously designed to receive only a single channel at a time, multiple simultaneous channel reception presented a problem for multi-user households.

[0004] Traditional solutions to this problem have included the provision of several receivers or STBs, each located in different rooms of the household. In this way, each television reception device, for example a television set, could be coupled to its own STB, and each user could independently receive and control reception of different cable television programs. These traditional solutions suffered from several disadvantages including increased cost of acquiring a plurality of STBs, increased space requirements for the additional STBs, need for additional household coaxial cable wiring, etc.

[0005] In addition to the above-mentioned disadvantages, traditional solutions lack the flexibility required to keep pace with new developments in consumer demand and diversification of that demand. For example, consumers now demand

support for simultaneous reception and display of multiple television channels on a single television screen (e.g., picture-in-picture (PiP)). In addition, the emergence of personal video recorder (PVR) technology increases the demand for multi-channel reception capability. Many PVR's include the ability to tune one or more channels for viewing, while simultaneously tuning one or more additional channels for recording to a recording medium. The information on the recorded channels is then available for later playback or other processing.

[0006] Along with the ability to simultaneously tune multiple channels it would be advantageous for tuning equipment to include a networking functionality that would allow distribution of received content to various locations, such as various rooms within a residence. It would therefore be desirable to have a distribution network coupled to a multichannel tuner device. Furthermore, it would be advantageous if such a distribution network included a networking device that was integral to a tuner system, thus simplifying setup and maintenance of a network for the redistribution of cable channel content.

[0007] Consumers have begun to demand additional flexibility in the location of reception devices, including handheld personal media devices capable of remotely receiving digital television programs as well as digital music programs, without the increased cost of a plurality of STBs.

Summary of the Invention

[0008] Given consumer demand for increased flexibility and convenience, there is a need for a digital television receiver capable of simultaneously receiving a plurality of channels, designed for delivery of a variety of digital content, and suitable for use with conventional cable television delivery systems.

[0009] The present invention is directed to a method and apparatus for simultaneous reception of a plurality of digital television channels. Specifically, the apparatus of the present invention is directed to a multichannel receiver circuit including a plurality of amplifier-filter circuits configured to receive a multichannel analog RF input signal, the plurality of amplifier-filter circuits including at least a first amplifier-filter circuit configured to generate a first analog signal including a first band of frequencies and a second amplifier-filter circuit configured to generate a second analog signal including a second band of frequencies. A plurality of analog-to-digital

converters is provided, each respectively coupled to one of the plurality of amplifier-filter circuits, the plurality of analog-to-digital converters including at least a first analog-to-digital converter configured to receive the first analog signal and generate a first digital signal and a second analog-to-digital converter configured to receive the second analog signal and generate a second digital signal. A digital tuner is provided, coupled to receive at least the first and second digital signals generated by the plurality of analog-to-digital converters, the digital tuner configured to recover a plurality of digital RF channels.

[0010] In an alternate embodiment, in addition to the above a plurality of demodulator circuits is coupled to the digital tuner, the plurality of demodulator circuits including at least a first demodulator circuit configured to receive and demodulate a first channel of the plurality of digital RF channels and a second demodulator circuit being configured to receive and demodulate a second channel of the plurality of digital RF channels. The plurality of demodulator circuits includes circuitry configured for forward error correction.

[0011] The method of the present invention includes receiving at least one multichannel analog RF input signal; separating the multichannel analog RF input signal into at least two analog signals including a first analog signal including a first band of frequencies and a second analog signal including a second band of frequencies; converting the at least two analog signals into at least two respective digital signals, including converting the first analog signal into a first digital signal and converting the second analog signal into a second digital signal; and demultiplexing the at least two digital signals to recover the plurality of digital RF channels.

[0012] In an alternative embodiment, in addition to the above steps the method includes demodulating the plurality of digital RF channels, including at least demodulating a first digital RF channel and demodulating a second digital RF channel; and forward-error-correcting the plurality of digital RF channels, including at least performing a first forward-error-correction of the first digital RF channel and performing a second forward-error-correction of the second digital RF channel.

[0013] This combination of components, when employed in the configuration of the present invention, permits substantially simultaneous reception of a plurality of digital cable television channels within a single digital receiver circuit. These

advantages can be provided in a form suitable for use with conventional cable television delivery systems and at a reasonable cost.

Brief Description of the Drawings

[0014] In the drawings:

[0015] Fig. 1 is a simplified block diagram illustrating an exemplary multichannel receiver circuit in accordance with the present invention;

[0016] Fig. 2 is a simplified block diagram illustrating a portion of the exemplary multichannel receiver circuit shown in Fig. 1;

[0017] Fig. 3 is a simplified block diagram illustrating another portion of the exemplary multichannel receiver circuit shown in Fig. 1;

[0018] Fig. 4 is a flow diagram illustrating an exemplary method of receiving a plurality of digital RF channels in accordance with an alternate embodiment of the present invention.

Detailed Description

[0019] The following discussion of the method and apparatus directed to a multichannel receiver circuit will help illuminate the features and advantages of the present invention, including its ease of formation using conventional techniques of constructing electronic devices and circuits which are well known in the art.

[0020] In the following discussion, the singular term "signal" and plural term "signals" are used interchangeably and are to be understood as including analog or digital information, at a single frequency or a plurality of frequencies, and may or may not include coding, modulation, sideband information, or other features of signals or waveforms well known in the art. Furthermore, when reference is made to a "receiver," "transmitter," "output," or "input," previous process steps may have been utilized to form signals or waveforms compatible with these features.

[0021] In addition, no particular order is required for the method steps described below, with the exception of those logically requiring the results of prior steps, for example converting of the first and second analog signals into first and second digital signals logically requires the prior generation of first and second analog signals. Otherwise, enumerated steps are provided below in an exemplary order which may

be altered. For instance, the several demodulation steps may be rearranged or performed simultaneously.

[0022] An exemplary embodiment of the invention will now be described with reference to FIG. 1. Although the invention will be described using the environment of reception of cable television signals, it should be apparent that the invention may be used in other types of radio-frequency communications systems as well, including reception of digital television channels via satellite and terrestrial television transmission systems. In contrast to the scheme described above, exemplary embodiments of the present invention provide substantially simultaneous recovery of a plurality of digital RF channels within a single multichannel receiver circuit, thereby reducing cost and increasing system flexibility.

[0023] FIG. 1 shows a simplified block diagram representation of a multichannel receiver circuit generally designated 100 in accordance with an aspect of the present invention. The multichannel receiver circuit 100 includes a plurality of amplifier-filter banks or circuits 111, 112, 113, a plurality of analog-to-digital converters 121, 122, 123, a digital tuner 130, and a plurality of demodulator circuits 141, 142, 143. It should be apparent from FIG. 1 that, although three instances of each plurality are shown, the present invention is not so limited and any number of amplifier-filter circuits, analog-to-digital converters, and/or demodulator circuits may be used in accordance with the present invention. In addition, the number (1 . . . M) of demodulator circuits provided is not necessarily related to the number (1 . . . N) of amplifier-filter circuits and/or analog-to-digital converters provided, and accordingly the present invention should not be so limited.

[0024] In operation, according to one embodiment, a multichannel analog RF input signal received at input coupler 101 is split into a plurality of substantially identical signals at splitter 102. Splitter 102 may include one or more amplifiers, filters, or other components (not shown) which reduce or overcome insertion loss or other adverse effects of the split, as should be apparent to one of ordinary skill in the art. The plurality of amplifier-filter circuits 111, 112, 113 then segregates the multichannel analog input signal into a plurality of separate analog signals of differing frequency ranges, or "bands." Each separate analog signal is then converted from analog to digital form in an analog-to-digital converter 121, 122, 123.

[0025] It should be noted that, in one embodiment of the invention, the splitter 102 is omitted. In this embodiment,the respective inputs of the amplifier/filter banks 111, 112, 113 are mutually directly connected to the input coupler 101. The amplifier/filter banks 111, 112, 113 serve as a demultiplexer to demultiplex the incoming signal received at the input coupler 101. In one embodiment, each amplifier/filter bank has particular characteristics that permit the passage of a specific range of frequencies substantially independent of the frequency selection characteristics of the other amplifier/filter banks. For example, one filter might have a pass-band of about 5 to about 300 MHz, while another filter might have a pass band of about 300 to about 600 MHz.

[0026] In one embodiment, the band break edges would be passed through two amplifier sets, e.g., amplifier/filter banks 111, 112. Thus, for example, the channels present just above a distal 300 MHz would pass through both the the 5 to 300 MHz filter and the 300 to 600 MHz filter. This helps to ensure the continuous coverage of all channel despite non-ideal filter characteristics.

[0027] The converted digital signals are coupled to the digital tuner 130, which demultiplexes the converted digital signals to generate a plurality of digital channel signals. Each digital channel signal is then coupled to a separate demodulator 141, 142, 143, which performs demodulation and forward-error-correction (FEC) operations appropriate for the content of that digital channel. Finally, in one embodiment, the resulting digital channel signals are each coupled to a separate output coupler 151, 152, 153 for further processing including for example MPEG transport processing.

[0028] Each of the plurality of amplifier-filter banks or circuits 111, 112, 113 is configured to process frequencies within a specified band. For example, a first amplifier-filter circuit 111 may be configured to process frequencies from about 5 MHz to about 300 MHz, a second amplifier-filter circuit 112 may be configured for frequencies between about 300 MHz and about 600 MHz, and a third amplifier-filter circuit 113 may be configured for frequencies from about 600 MHz to about 900 MHz. In such an example, the present invention may be used to recover a plurality of digital cable television channels from a multichannel analog RF input signal which includes frequencies ranging from about 5 MHz to about 900 MHz.

[0029] Referring now to FIG. 2, each amplifier-filter circuit 111, 112, 113 includes at least an amplifier 201, 203, 205 and a filter 202, 204, 206, respectively. Each of the amplifiers 201, 203, 205 may be a low-noise amplifier (LNA) or other amplifier suitable for use in analog RF front-end applications.

[0030] Each of the filters 202, 204, 206 may be band-pass filters (BPF) or other devices suitable for passing a range or band of frequencies while simultaneously filtering out or attenuating other frequencies outside the range or band. Each of the amplifier-filter circuits 111, 112, 113 may include one or more additional components (not shown) for accomplishing segregation of the analog input signal as described above.

[0031] In addition, each of the filters 202, 204, 206 may include a gain controlled amplifier. In an exemplary embodiment, each of the filters 202, 204, 206 includes a gain control input that allows adjustment of the respective gain of the filter. The system may thus be configured to allow adjustment of the filters to correspond to a range of possible received signal levels from the system while maintaining desirable signal levels at the inputs of the A/D converters. In one embodiment of the invention, a device is provided for comparing an output of the filter to a set-point value and controlling filter gain in a feedback loop.

[0032] Each amplifier-filter circuit 111, 112, 113 should preferably be physically separate and may be configured to amplify a particular range of frequencies without producing substantial intermodulation distortion effects. Alternatively, the amplifier-filter circuits 111, 112, 113 may be co-located in a single package configured to permit processing of signals within each band separately and independently (e.g., substantially free of intermodulation distortion attributable to simultaneous amplification of a wide range of frequencies). The amplifier-filter circuits 111, 112, 113 should preferably be configured to minimize degradation of one or more signal characteristics particularly susceptible to front end effects, such as noise figure, sensitivity, and dynamic range.

[0033] By employing undersampling techniques, various embodiments of the present invention may be economically implemented. As would be understood by one of ordinary skill in the art, the Nyquist criterion is met as long as the bandwidth of a signal is less than half of the sampling frequency. In one embodiment of the invention, each band has a bandwidth of about 300 MHz. Accordingly, each of the

A/D converters 121, 122, 123 can recover a respective target frequency if operated at a sampling frequency of 600 MHz. In addition, since each of the bands has substantially the same bandwidth, a single 600 MHz clock is sufficient to provide a clock frequency for all of the analog-to-digital converters. Consequently, in one embodiment, a single clock device can provide the requisite clock signal for all of the A/D converters. Moreover, the required frequency is not remarkably high, facilitating design and implementation of the clock device.

[0034] Without the use of undersampling the system would require, for example, a first analog-to-digital converter 121 operating with a sampling frequency of about 600 MHz for processing frequencies in a band from about 5 MHz to about 300 MHz , a second analog-to-digital converter 122 operating with a sampling frequency of about 1.2 GHz for processing frequencies in a band between about 300 MHz and about 600 MHz, a third analog-to-digital converter 123 operating with a sampling frequency of about 1.8 GHz, for processing frequencies in a band from about 600 MHz to about 900 MHz, etc.

[0035] In accordance with an aspect of the invention, each analog-to-digital converter 121, 122, 123 may include a frequency selector 211, 212, 213 for setting the sampling frequency and/or input frequency corresponding to the desired band. For example, a first analog-to-digital converter 121 may include a first frequency selector 211 including a clock input coupler on which a clock signal is transmitted, indicating the desired sampling frequency of the first analog-to-digital converter 121. Other forms of communicating a desired sampling frequency of each of the analog-to-digital converters 121, 122, 123 may be utilized in accordance with the present invention, as would be appreciated by one of ordinary skill in the art.

[0036] Each analog-to-digital converter 121, 122, 123 should have resolution and linearity characteristics sufficient for satisfactorily processing digital television signals and associated signals intended for end users in a conventional cable television broadcast system. For example, each analog-to-digital converter 121, 122, 123 may produce from about 1024 to about 65536 discrete values, corresponding to a resolution of 10 (i.e., $2^{10} = 1024$) to 16 (i.e., $2^{16} = 65536$) bits.

[0037] Referring now to FIG. 3, a digital tuner 130 is provided for processing the digital signals converted by the plurality of analog-to-digital converters 121, 122, 123. The digital tuner 130 may include one or more digital multiplexers or demultiplexers

capable of generating a plurality of digital channel signals from the converted digital band signals. The digital tuner 130 may include a multitude of components configured as is well known in the art to recover a plurality of digital channel signals substantially simultaneously using a plurality of separate digital processors or a single digital processor.

[0038] The digital tuner 130 may include a channel selector 315 to permit selection of one or more particular digital channels desired to be recovered. For example, a selected set of digital cable television channels may be communicated to the digital tuner 130 via the channel selector 315 corresponding to a plurality of pay-per-view selections desired by members of a household; the digital tuner 130 may demultiplex only the digital channel signals corresponding to those digital cable television channels. Alternatively, the digital tuner 130 may be configured to demultiplex and recover all of the available digital channel signals.

[0039] It should be appreciated that the digital tuner 130 in accordance with the present invention is not limited to the above-described operations, but the digital tuner 130 may also perform a variety of other processing operations prior to providing digital channel signals suitable for use in each of the demodulation circuits 141, 142, 143. For example, the digital tuner 130 may perform coding, decoding, scrambling, descrambling, rotating, and/or derotating operations prior to passing the digital channel signals to demodulation circuits 141, 142, 143.

[0040] Each of the demodulation circuits 141, 142, 143 may include one or more demodulators 301, 303, 305 and forward-error-correction (FEC) circuitry 302, 304, 306, respectively. Each of the demodulation circuits 141, 142, 143 may include demodulators 301, 303, 305 configured to perform a particular demodulation function or set of functions corresponding to the type of digital content expected to be found within a corresponding digital channel signal. For example, a first demodulator 301 may be configured to perform quadrature amplitude modulation (QAM) demodulation of digital cable television signals; a second demodulator 303 may be configured to perform quadrature phase shift keying (QPSK) demodulation of digital audio signals; and a third demodulator 305 may be configured to perform vestigial sideband (VSB) demodulation of high-definition television (HDTV) signals. Of course, it should be appreciated that more than one of the plurality of demodulation circuits 141, 142, 143

may be configured to perform similar or identical functions or operations on separate digital channel signals substantially simultaneously.

[0041] Forward-error-correction (FEC) circuits 302, 304, 306 may include one or more components configured for coding or decoding, for example a Reed-Solomon decoder. It should be appreciated that each of the demodulation circuits 141, 142, 143 and/or the digital tuner 130 may include circuitry for providing additional functions, for example adaptive filters for removing multi-path propagation effects, co-channel interference, and other types of radio frequency interference (RFI) well known in the art.

[0042] FIG. 4 shows a flow diagram representation of a method of receiving a plurality of digital RF channels generally designated 400 in accordance with an aspect of the present invention. The method 400 includes a separating step 402, a first converting step 403, a second converting step 404, a demultiplexing step 405, a first demodulating step 406, and a second demodulating step 407.

[0043] The method 400 begins at step 401 and proceeds to step 402 in which a multichannel analog RF input signal is separated into a plurality of analog signals including at least first and second analog signals. The first analog signal includes a first band of frequencies and the second analog signal includes a second band of frequencies. It should be appreciated that the input signal may also be separated into at least a third analog signal including a third band of frequencies, and the first, second, and third bands of frequencies may not necessarily be contiguous.

[0044] In step 403, the first analog signal is converted into a first digital signal using a first analog-to-digital converter. In step 404, the second analog signal is converted into a second digital signal using a second analog-to-digital converter independently of the conversion performed in the first analog-to-digital converter. The first and second analog-to-digital converters may convert different frequency bands from analog to digital form, similar to analog-to-digital converters 121, 122, 123 described above with reference to FIGS. 1 and 2, and each should have a sampling frequency of at least twice the bandwidth of the respective frequency band in accordance with the Shannon-Nyquist sampling theorem. The first and second analog-to-digital converters should perform such conversions with resolution and linearity characteristics sufficient for satisfactorily processing digital television signals

and associated signals intended for end users in a conventional cable television broadcast system.

[0045] In step 405, the first digital signal (converted in the first analog-to-digital converter) and the second digital signal (converted in the second analog-to-digital converter) are demultiplexed to generate a plurality of digital RF channel signals including at least first and second digital RF channel signals. Each of the plurality of digital RF channel signals is typically characterized by a different carrier frequency and a bandwidth or range of frequencies assigned to a particular application or type of content to be carried on that channel. It should be apparent that each digital RF channel signal may in turn carry or provide a plurality of data streams, e.g., audio, video, program information, or interactive content.

[0046] In step 406, the first digital RF channel signal is demodulated and forward-error-corrected. In step 407, the second digital RF channel signal is demodulated and forward-error-corrected. Steps 406 and 407 may be accomplished using demodulation circuits 141, 142, 143 described above with reference to FIGS. 1 and 3. However, the present invention is not so limited and steps 406 and 407 may alternatively be accomplished in any of several other ways known in the art, for example demodulation and forward-error correction steps 406 and 407 may be performed within one or more digital processors temporarily or semi-permanently programmed to perform such operations.

[0047] The method then proceeds to step 407, where it ends until another multichannel analog RF input signal is received from which one or more digital RF channels are desired to be recovered.

[0048] As illustrated in the preceding discussion and accompanying figures, the method and apparatus of the present invention represent an improvement in the state of the art for multichannel digital cable receivers and associated methods. The present invention provides a multichannel receiver circuit and method that accomplishes substantially simultaneous reception of a plurality of digital cable television channels at a reasonable cost. These advantages can be embodied in a single digital receiver circuit capable of recovering a wide variety of digital content, and may be configured for use with conventional cable television delivery systems.

[0049] One of skill in the art will appreciate that the invention, as described above, allows a single device to receive a modulated signal at an input and produce

a plurality of video signals, or other information signals, related to the modulated signal. This plurality of video signals may then be received at respective devices such as, for example, a television display device, a PVR device, a videocassette recorder device, or any other appropriate signal receiving device. These devices may be disposed at respective locations which may or may not be remote from one another. Accordingly, for example, a plurality of television receivers, PVR's, or other devices, may be disposed in respective rooms of a house or multi-unit dwelling, in a respective plurality of offices, or in otherwise separated locations while concurrently receiving signals from a common modulated signal input.

[0050] While the invention has been described in detail in connection with the preferred embodiments known at the time, it should be readily understood that the invention is not limited to such disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions, or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. Accordingly, the invention is not to be seen as limited by the foregoing description, but is only limited by the scope of the appended claims.

CLAIMS

1. An apparatus (100), comprising:

first means for processing (111) an input signal comprising signals in a first frequency band and signals in a second frequency band to produce a first analog signal including signals in the first frequency band and substantially excluding the signals in the second frequency band;

second means for processing (112) the input signal comprising signals in a first frequency band and signals in a second frequency band to produce a second analog signal including signals in the second frequency band and substantially excluding the signals in the first frequency band;

a first analog-to-digital converter (121) for processing the first analog signal to produce a first digital signal representing the signals in the first frequency band;

a second analog-to-digital converter (122) for processing the second analog signal to produce a second digital signal representing the signals in the second frequency band; and

a means for processing (130) the first and second digital signals to simultaneously produce a first output signal representing a first digital channel included in the first frequency band and a second output signal representing a second digital channel included in the second frequency band.

2. The apparatus (100) of claim 1 further comprising a third amplifier-filter circuit (113) configured to process signals within a third frequency band and a third analog-to-digital converter (121) configured generate a third digital signal comprising a representation of said processed signals within said third frequency band.

3. The apparatus (100) of claim 2 wherein said first frequency band includes frequencies from about 5 MHz to about 300 MHz, said second band includes frequencies between about 300 MHz and about 600 MHz, and said third band includes frequencies from about 600 MHz to about 900 MHz.

4. The apparatus (100) of claim 3 wherein said first second and third analog-to-digital converters (121, 122, 123) have sampling frequencies of at least 600 MHz.

5. The apparatus (100) of claim 3 wherein said first second and third analog-to-digital converters (121, 122, 123) are configured for an input frequency of up to about 900 MHz.

6. The apparatus (100) of claim 1 wherein the digital processor (130) includes a frequency selector for selecting a desired sampling frequency.

7. The apparatus (100) of claim 1 wherein each of said first, second, and third analog-to-digital converters (121, 122, 123) have a resolution of at least about 10 bits.

8. The apparatus (100) of claim 1 wherein each of said first, second, and third analog-to-digital converters (121, 122, 123) have a resolution from about 10 to about 16 bits.

9. The apparatus (100) of claim 1 wherein said digital processor (130) is configured to recover substantially all signals with said first and second frequency bands.

10. The apparatus (100) of claim 1 wherein said digital processor (130) is configured to recover a selected set of signals with said first and second frequency bands.

11. The apparatus (100) of claim 10 wherein said digital processor (130) is configured to recover said selected set of signals with said first and second frequency bands substantially simultaneously.

12. The apparatus (100) of claim 1 further comprising a first demodulator circuit (141) coupled to said digital processor (130) and a second demodulator circuit (142) coupled to said digital processor (130).

13. The apparatus (100) of claim 12 wherein said first and second demodulator circuits (141, 142) include circuitry configured for forward error correction (302, 304, 306).

14. The apparatus (100) of claim 12 where said digital processor (130) multiplexes said first, second, and third digital signals, downconverts said multiplexed signal and extracts desired information to be coupled to said first and second demodulator circuits (141, 142).

15. The apparatus (100) of claim 12 where said digital processor (130) downconverts and extracts desired information to be coupled to said first and second demodulator circuits (141, 142) from each of said first, second, and third digital signals individually.

16. The apparatus (100) of claim 1 wherein said apparatus (100) processes frequencies between about 5 MHz and about 900 MHz.

17. The apparatus (100) of claim 1 wherein apparatus (100) processes cable television channels.

18. A method (400) processing signals comprising the steps of:

(a) separating an input signal into a first analog signal and a second analog signal;

(b) digitizing said first analog signal to generate a first digital signal;

(c) digitizing said second analog signal to generate a second digital signal;

(d) downconverting said first digital signal and said second signal; and

(e) extracting desired television program information from said downconverted first digital signal and said second digital signal.

19. The method (400) of claim 18, further comprising the steps of:

(a) demodulating (406, 407) said extracted television program information;

(b) forward-error-correcting (406, 407) said extracted television program information;

20. The method (400) of claim 18 further comprising the steps of:

(a) multiplexing said first digital signal and said second digital signal after said digitizing steps and before said downconverting step.

21. The method (400) of claim 18 further where said downconverting step comprises downconverting each of said first and second set of signals individually.

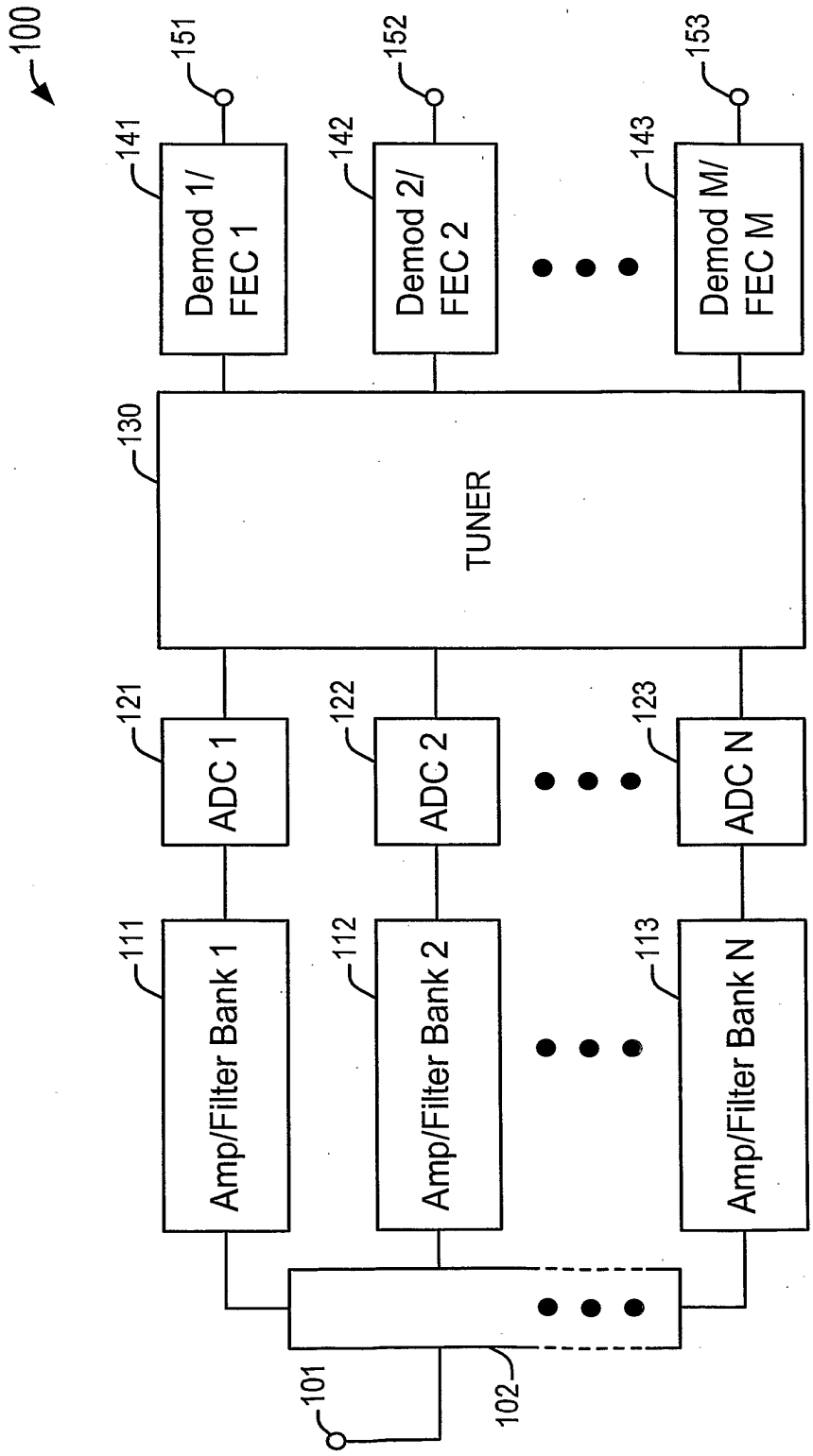

100
151
152
153
141
142
143
Demod 1/ FEC 1
Demod 2/ FEC 2
Demod M/ FEC M
130
TUNER
121
122
123
ADC 1
ADC 2
ADC N
111
112
113
Amp/Filter Bank 1
Amp/Filter Bank 2
Amp/Filter Bank N
101
102

FIG. 1

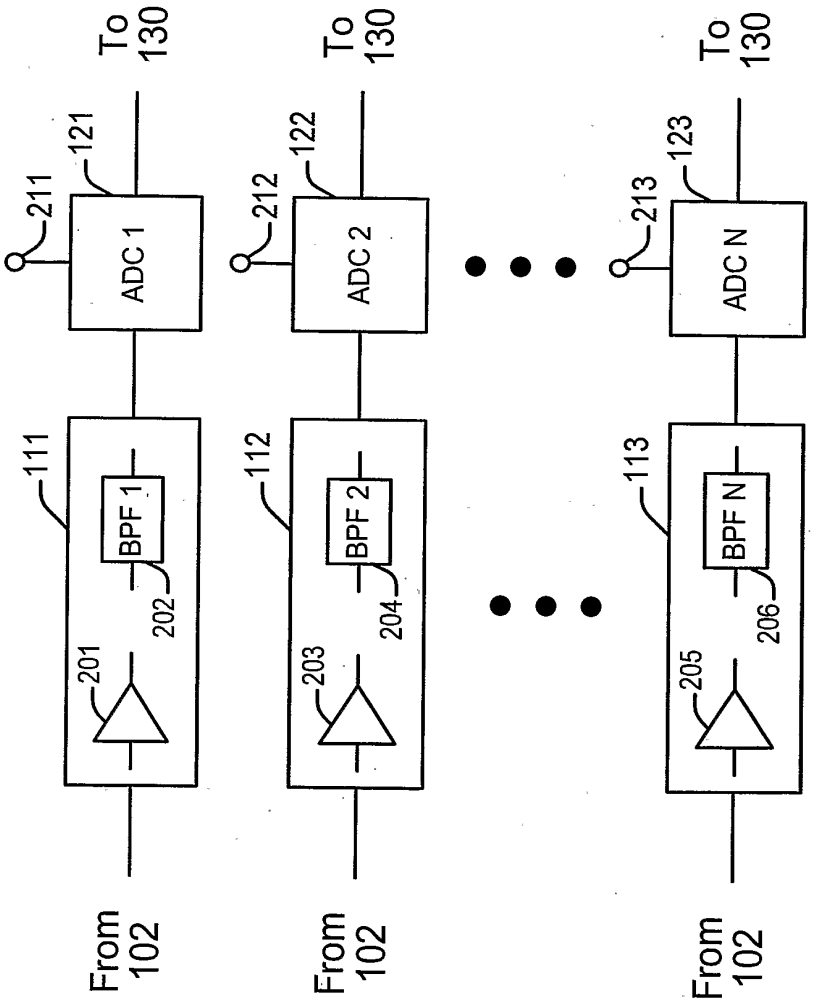

From 102
From 102
From 102
111
112
113
BPF 1
BPF 2
BPF N
201
202
203
204
205
206
211
212
213
ADC 1
ADC 2
ADC N
121
122
123
To 130
To 130
To 130

FIG. 2

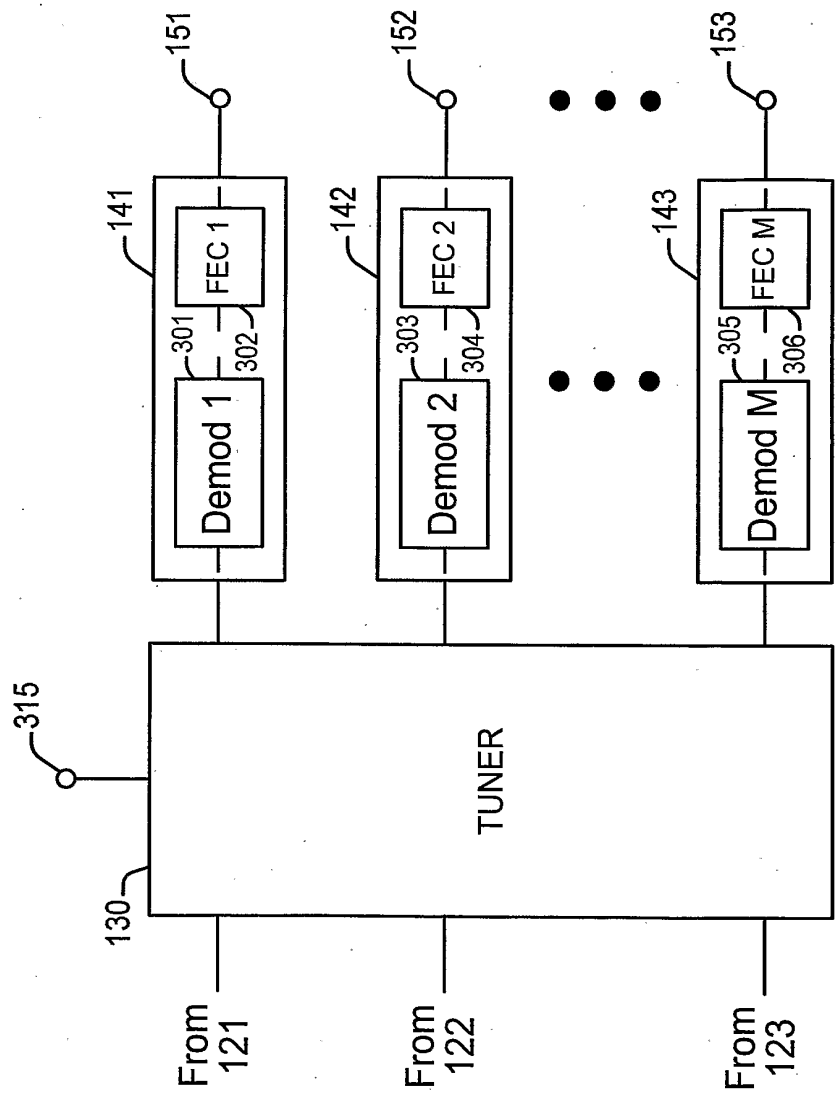

151
152
153
141
142
143
FEC 1
FEC 2
FEC M
301
302
303
304
305
306
Demod 1
Demod 2
Demod M
315
TUNER
130
From 121
From 122
From 123

FIG. 3

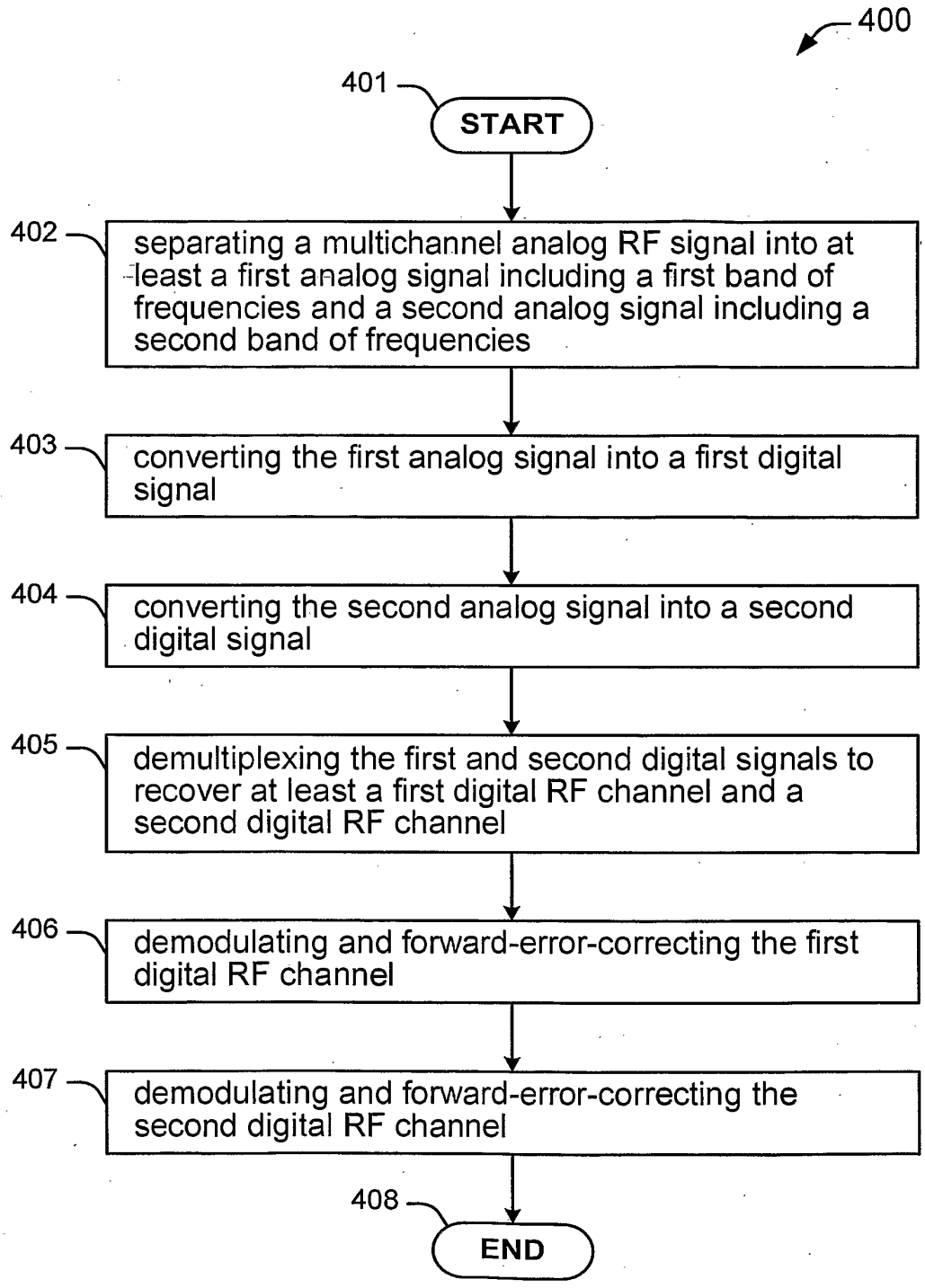

400
401
START
402
separating a multichannel analog RF signal into at least a first analog signal including a first band of frequencies and a second analog signal including a second band of frequencies
403
converting the first analog signal into a first digital signal
404
converting the second analog signal into a second digital signal
405
demultiplexing the first and second digital signals to recover at least a first digital RF channel and a second digital RF channel
406
demodulating and forward-error-correcting the first digital RF channel
407
demodulating and forward-error-correcting the second digital RF channel
408
END

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/023664

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N5/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/204034 A1 (HANRAHAN ROBERT MASON [US]) 14 October 2004 (2004-10-14)	1,2, 9-12,14, 15,17, 18,20,21
Y	the whole document	3-8,13, 16,19
Y	WO 01/20792 A1 (SARNOFF CORP [US]; MALKEMES ROBERT [US]) 22 March 2001 (2001-03-22) page 4, line 19 - page 5, line 27 page 6, line 29 page 8, line 16 - line 22	3-8,16
Y	US 2005/012869 A1 (AKIYAMA TOSHIFUMI [JP]) 20 January 2005 (2005-01-20) figures 4,5	13,19

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 February 2007	26/02/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Yvonnet, Joel

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/023664

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005/190777 A1 (HESS KENDAL M [US] ET AL) 1 September 2005 (2005-09-01) figures 6,7	1,18
A	US 5 068 918 A (VERHEIJEN PAULUS A M [NL] ET AL) 26 November 1991 (1991-11-26) column 3, line 20 - line 26	1,18

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2006/023664

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 2005012869 A1	20-01-2005	CN 1578437 A	09-02-2005
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		NL 8901460 A	02-01-1991

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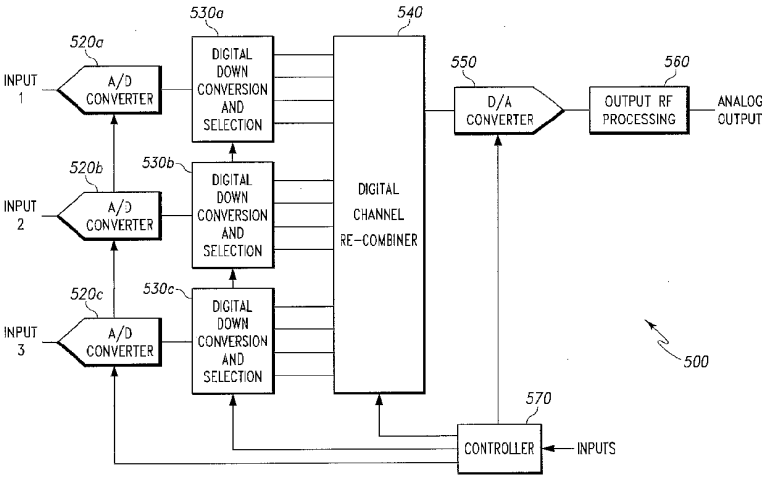
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Published:
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: APPARATUS AND METHOD FOR FREQUENCY TRANSLATION



(57) Abstract: The disclosed embodiments relate to an apparatus and method for performing frequency translation. The apparatus includes a receiver (520a-c, 530a-c) for receiving and digitizing a plurality of first signals, each signal containing channels and for simultaneously recovering a set of selected channels from the plurality of first signals. The apparatus also includes a transmitter (540, 550, 560) for combining the set of selected channels to produce a second signal. The method of the present invention includes receiving a first signal (602) containing a plurality of different channels, selecting a set of selected channels (606) from the plurality of different channels, combining the set of selected channels (608) to form a second signal and transmitting the second signal (612).

WO 2006/119490 A2

Apparatus and Method for Frequency Translation

This application claims the benefit under 35 U.S.C.§ 119 of a provisional application 60/677563 filed in the United States on May 4, 2005.

FIELD OF THE INVENTION

The present invention generally relates to communications systems. More specifically, the present invention relates to the receiving and retransmission of content within a communications system.

BACKGROUND OF THE INVENTION

This section is intended to introduce the reader to various aspects of art, which may be related to various aspects of the present invention that are described and/or claimed below. This discussion is believed to be helpful in providing the reader with background information to facilitate a better understanding of the various aspects of the present invention. Accordingly, it should be understood that these statements are to be read in this light, and not as admissions of prior art.

In today's data communication systems such as used in satellite TV, data of different types often reside in what are known as virtual channels. The data from these virtual channels is separately disassembled into data packets, aggregated within and across different data types into bit streams and conveyed by packet delivery systems. Data consumer appliances, such as satellite receivers, select from physical channels available to them, convert the signals on these channels to digital form (packets) and collect the data packets required to re-assemble the desired virtual channels of information (e.g., audio, video, program guide, transactional data, etc.). At different points along the data path between a content provider and a content consumer data

management opportunities occur. A piece of data may come from one of many sources, be routed through one of many satellites, pass through several of many transponders aboard the satellite, be received by a consumer antenna, and be distributed to places of consumption.

Consumer receivers are often capable of receiving only one of the physical channels from the satellite at a time for display. However, new receivers may contain advanced features the consumer can use. For instance, a receiving device may contain more than one tuner for use in either two picture simultaneous display systems or content recording. Additionally, consumer households often include multiple receivers, each receiver requiring the tuning of one or more channels for use.

The ever-expanding amount of content for delivery has made it very difficult to deliver that content to all places at all times. Systems receiving data from up to four separate satellites to deliver programming to the home can no longer deliver all of the content on one coaxial cable connection. Various approaches have been adapted including the use of multiple cables or complex switching arrangements. Many of these approaches are in some manner suboptimal for a home installation due to high cost or high complexity.

Another solution may be to employ a system of preselecting, combining, and redistributing the incoming content based on the physical channels requested by the user(s) using analog signal processing. As a result, only the channels required for delivery to the receivers in a household are selected from the initial available content. The desired channels may then be provided on a single cable that is relatively easy to distribute around the household. The solution relies on coarse analog signal tuning and re-mixing to move channels or frequency regions of signals from an original spectral location in frequency at the input to another spectral location in frequency on a common signal at the output. Further, channels or signal regions at the same frequency but on different satellites may be combined by moving one or both of the

original channels or regions. These relocated signals containing the desired channels are then provided on the single cable, eliminating the need for any additional switching and multiple cable connections.

The analog solution involving preselection, combination, and redistribution remains limited in the number of channels that can be provided due to the inherent shortcomings of performing the processing in the analog domain. Narrow band filters used to select individual physical channels while rejecting others are impractical at frequencies above the range of one gigahertz (GHz). Available filters having a practical bandwidth require additional channel separation in order to prevent undesired interferences in the output signal. Additionally as the desire to deliver more requested channels to the home increases, the subsequent increase in analog circuit complexity results in an expensive and inefficient design with potential problems due to analog crosstalk. Therefore there is a desire to have a solution providing receiving and re-synthesizing of channels for distribution in a more optimal manner.

SUMMARY OF THE INVENTION

The present invention relates to an apparatus and method for performing frequency translation. The apparatus includes a receiver for receiving and digitizing a plurality of first signals, each signal containing channels and for simultaneously recovering a set of selected channels from the plurality of first signals. The apparatus also includes a transmitter for combining the set of selected channels to produce a second signal.

The method of the present invention includes receiving a first signal containing a plurality of different channels, selecting a set of selected channels from the plurality of different channels, combining the set of selected channels to form a second signal and transmitting the second signal.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a block diagram of an exemplary system using the present invention.

FIG. 2 is a block diagram of an embodiment of the present invention

FIG. 3 is a block diagram of another embodiment of the present invention.

FIG. 4 is a block diagram of yet another embodiment of the present invention.

FIG. 5 is a block diagram of a further embodiment of the present invention.

FIG. 6 is a flow chart illustrating a method of the present invention.

The characteristics and advantages of the present invention may become more apparent from the following description, given by way of example.

DETAILED DESCRIPTION

One or more specific embodiments of the present invention will be described below. In an effort to provide a concise description of these embodiments, not all features of an actual implementation are described in the specification. It should be appreciated that in the development of

any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming, but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

It is noted that familiarity with television broadcasting and receivers is assumed and is not described in detail herein. For example, other than the inventive concept, familiarity with current and proposed recommendations for TV standards such as National Television Systems Committee (NTSC), Phase Alternation Lines (PAL), Sequential Couleur Avec Memoire (SECAM), Advanced Television Systems Committee (ATSC), and Direct Broadcast Satellite (DBS) is assumed. Likewise, other than the inventive concept, transmission concepts such as satellite transponders, down-link signals, eight-level vestigial sideband (8-VSB), Quadrature Amplitude Modulation (QAM), and receiver components such as a radio-frequency (RF) front-end, or receiver section, such as a low noise block, tuners, and demodulators is assumed. Similarly, formatting and encoding methods (such as Moving Picture Expert Group (MPEG)-2 Systems Standard (ISO/IEC 13818-1)) for generating transport bit streams are well-known and not described herein. In addition, the inventive concept may be implemented using conventional programming techniques which, as such, will not be described herein.

The following describes a circuit used for processing satellite signals. Other systems utilized to receive other types of signals where the signal input may be supplied by some other means may include very similar structures. Those of ordinary skill in the art will appreciate that the embodiment of the circuits described herein is merely one potential

embodiment. As such, in alternate embodiments, the components of the circuit may be rearranged or omitted, or additional components may be added. For example, with minor modifications, the circuits described may be configured to for use in non-satellite video and audio services such as those delivered from a cable network. Further, the invention described could be used in conjunction with a home networking system. The device may receive inputs from a satellite or cable network, process them, and provide them as an output to the home network system. The output may in the form of a wired or wireless transmission.

Turning now to the drawings and referring initially to FIG. 1, an overall block diagram 100 of a system using the present invention is shown. FIG. 1 represents a typical satellite system installation at a customer home. A similar installation may also exist at an apartment complex or hotel where the system may be augmented with additional equipment often incorporated in multi-dwelling unit applications. Satellite transponders located on satellites 102a-c transmit satellite signals to satellite dishes 104a-c. Each satellite dish contains a reflector, a feed horn and a low noise block converter (LNB).

Each of the satellite signals may represent one or more individual physical channels. Each of the physical channels may in turn represent one or more preferably digital data streams of information combined together, encoded, and modulated using various analog and/or digital modulation techniques. The physical channels are often grouped to cover a limited frequency range such as 500 to 1000 MHz of bandwidth. The satellite signals are often located in the microwave frequency range, for instance 11-13 Gigahertz (GHz). The LNBs in the satellite dishes 104a-c will amplify and convert the satellite signal in the 11-13 GHz range to an L-band signal in the 1-2 GHz frequency range. Although three satellite dishes are shown, the orbital locations of the satellites 102a-c may permit using one satellite dish containing one reflector and three feed horns and LNBs. Also, systems may utilize more or fewer

than the three satellites signals illustrated here. The systems may additionally use techniques such as polarization diversity to increase the number of satellite signals delivered from each satellite.

Each of the three L-band signals from the satellite dishes 104a-c are provided through separate coaxial cables to a frequency translation module (FTM) 110. The three L-band signals in their entirety cannot be supplied through a single coaxial cable for delivery into the customer home, because the L-band signals occupy too much frequency bandwidth. As previously described, each L-band signal may occupy 1 GHz of bandwidth, and a typical customer premises cable installation may only support less than 2 GHz of total signal bandwidth. The FTM 110 extracts certain ranges of frequencies containing selected physical channels as portions of the three L-band signals provided. The FTM 110 also frequency translates the extracted ranges as needed and re-combines them to form a new single selected L-band signal. The process used by the FTM 110 may be described as a preselection of certain physical channels. However, the process used by the FTM 110 is different from a direct tuning of those certain physical channels since other energy besides the selected channel may be present, and the channels are then recombined to form a new signal for further distribution. Note that the FTM 110 may reside physically outside the customer home as shown, or may reside very near to the entry point into the customer home.

Once the FTM 110 has preselected the physical channels for use, the selected signal is provided over a single coaxial cable to the customer's premises 120. The selected signal may pass through a set of signal splitters 122a-c, as needed, to supply each of the locations for the premises installation. The splitters 122a-c may contain passive circuits such as transformers and resistors or may also contain amplifiers in order to increase the signal level at the installation location.

At each installation location in the premises 120, the selected signal is provided to a standalone terminal 130 or to a combination settop box 140a-c and display device 150a-c. The terminal 130 and settop box 140a-c operate in a similar manner. Each of them receive the selected signal, tune to the desired physical channel within the selected signal, demodulate the physical channel to produce a transport stream, and extract the desired bit stream(s) from the transport stream. The terminal 130 may be used for local storage of various bit streams or for distribution of these bitstreams over a different network such as a wireless network or an Ethernet connection. The settop box 140a-c converts the desired bitstream(s) into video and audio signals for display on the display device 150a-c.

The terminal 130 and settop boxes 140a-c may provide one or more control signals back onto the cable to the FTM 110. The control signal is generated based on inputs provided, for instance by a customer. The control signal sent to FTM 110 contains information necessary to perform the preselection of frequency ranges and physical channels from each of the L-band signals. The communication protocol to the FTM 110 may be done in a manner suitable for delivery as is known in the art, such as frequency shift keying FSK protocol. The control signal may alternately be supplied through a wireless link. Electrical power may also be passed through the coaxial cable to the FTM 110 and further on to the satellite dishes 104a-c.

As described earlier, a conventional FTM contains analog signal processing used for the filtering, mixing, and recombining of the L-band signals. Analog signal processing contains limitations when operating at high frequencies in the 1GHz range, and the complexity of the analog signal processor increases significantly with an increase of the number of selected physical channels. The utilization of digital signal processing within the FTM structure permits greater flexibility and removes some of the limitations of analog signal processing.

Turning now to FIG. 2 a block diagram 200 of an embodiment of the present invention is shown. The diagram shows an implementation of the FTM 110 that includes digital signal processing in order to increase the performance and available bandwidth for selected channels. In order to facilitate a further understanding of the invention, an FTM 110 will be described here using only a single L-band signal as an input. The single L-band signal, as an analog input, is processed through an RF processing block 210. The RF processing block 210 may contain circuitry for filtering undesired energy outside the signal frequency range, may correct for any frequency response errors introduced, and may amplify the signal to a level necessary for input to the analog to digital (A/D) converter 220. The input RF processing block 210 may also contain any mixing circuits necessary to position the L-band signal in the correct frequency range for operation of the A/D converter 220.

The A/D converter 220 digitizes the processed L-band signal into a series of samples, each sample containing a group of bits. In an exemplary embodiment, the processed satellite signal is located between the frequencies of 975 and 1425 MHz. The A/D converter 220 samples the processed L-band signal at a rate of 933 megasamples per second (MSPS) generating a digital signal containing a series of samples, each sample represented by 8 bits. The A/D converter 220 may also generate a translated frequency image of the L-band signal essentially translating the signal from an initial frequency range in the analog domain to a different frequency range based on sampling principles. A clock signal, not shown, is supplied to the A/D converter for performing the sampling. The clock signal may be generated by a crystal or as part of a voltage controlled oscillator. The clock signal may also directly, or through additional multipliers and dividers, supply signals to other blocks within the FTM 110.

The digital channel selector 230 receives the sampled signal and proceeds to select and down-convert each of the individual physical channels that have been selected. After processing, each of the selected individual channels are located within the same frequency range at or near to baseband, but are contained as individual signals on separate signal lines. The number of bits representing each selected individual channel may be different from the original sampled signal based on the processing method employed. The use of digital signal processing and processing of the signal in parallel permits narrower filtering constraints and more efficient channel selection within the FTM 110.

Each of the individual selected channels is provided to the digital channel re-combiner 240. The digital channel re-combiner 240 frequency translates the individual selected channels each to a different and separate frequency range and combines these signals together to form a single selected digital signal. The selected digital signal is supplied to a digital to analog (D/A) converter 250. The D/A converter 250 converts the selected digital signal to a selected analog signal. In a preferred embodiment, the selected digital signal provided to the D/A converter 250 is a series of 10 bit samples at a rate of 950 MSPS. The D/A converter 250 outputs a selected analog signal within a frequency range of DC to 475 MHz.

The selected analog signal is passed to the RF processing block 260. The RF processing block 260 provides any analog signal processing necessary to properly send the selected analog signal on the coaxial cable to the customer home. The RF processing block 260 may contain circuitry for filtering undesired signal energy outside the signal frequency range, such as the images produced by the sampling process in D/A converter 250. The RF processing block 260 may also correct for any other frequency response errors introduced, and may amplify the signal as necessary to provide the signal onto a coaxial cable. The RF

processing block 260 may also contain a mixing circuit necessary to position the selected analog signal in the correct L-band frequency range, for instance 975 - 1425 MHz.

Some additional circuitry may also be included such as circuitry for controlling the blocks, receiving and processing user inputs, and additional signal processing, although this circuitry is not shown here.

Turning now to FIG. 3, an illustrative block diagram of a circuit 300 of an embodiment of a portion of the present invention is shown. Circuit 300 represents circuitry contained with the digital channel converter block 230. A sampled signal, converted from an L-band signal by A/D converter 220, is provided to the sample demultiplexer 310. Sample demultiplexer 310 resamples at a demultiplexer sampling rate, F_F, (or post-decimation sampling rate) to provide a number of decimated sample streams in parallel.

Each of the decimated sample streams represents a sampled and time shifted version of the original signal with each of the folded spectra, from the decimation, aliased into the same decimated frequency space. The number of decimated sample streams, N, may be integrally related to the number of virtual channels in the original signal. In a preferred embodiment, the number of physical channels is sixteen. Further, the sample demulitplexer 310 sampling rate is preferably two times the data rate of one of the physical channels, or $F_F = 2F_S$ where F_s is the data rate of the physical channel. Each of the decimated sample streams passes through a sampling interface block 320. The sampling interface block 320 provides any sampling domain adjustments necessary in moving the signal from the A/D converter 220 and sample demulitplexer 310 to the filter bank 330a-N, connected to the sampling interface block 320. The filter bank 330a-N may provide a number of process steps including filtering the physical channels that are distributed within the decimated sample streams prior to the physical channels being separated. The filtering provides rejection of any energy not within a

physical channel while generating a reconstructive set of base signals for selecting out the physical channels in further downstream processing. The filter bank 330a-N may also provide a time realignment of each of the decimated sample streams. In a preferred embodiment, the filter bank 330a-N consists of a bank of bifurcated filters that collectively generate a filtered signal vector. Since all the bifurcated filters have a similar structure, only one bifurcated filter is described in detail herein.

A bifurcated filter may typically consist of two parallel branches of coefficient multiply and delay operations with the operations in each of the branches separately summed together. Each branch is designated as either an even output signal or an odd output signal. The number of multiply and delay operations in each branch may vary based on design criteria. For instance, sixteen weighted multiply and a number of coefficient multipliers may be used in each bifurcated filter. The delay element is controlled by a decimated sample clock signal, not shown, at a frequency F_f. The summing node separately adds together the values from each of the odd weighted multipliers and even weighted multipliers to form the odd and even output signal. The orientation of the filter branches and operations within the branches allows special properties to exist. These properties include amplitude inversion of the signal or time reversing the signal within the branch. As noted, other filter structures may be used, as known by those skilled in the art, in conjunction with the various techniques of simultaneous channel reception techniques.

The output signal, a filter signal vector containing 2N signal streams, from the filter bank 330a-N connects to a bank of summing nodes 340a-N. Referring to the preferred embodiment, the even and odd outputs from each of the different bifurcated filters may be combined in a cross-coupling pattern. The even output of filter 0 is summed with the odd output of filter N-1, even output of filter 1 with the odd output of filter N-2, and so on as shown. The summing nodes 340a-N generate a set of filtered sample streams.

The filtered sample streams at the output of summing nodes 340a-N connect to a distributor block 350. The main purpose of the distributor block 350 is to process the filtered sample streams generated by the filter block 330a-N and summing nodes 340a-N to reconstruct the set of physical channels, originally provided in the L-band signal, from the decimated and filtered sample streams. The processing may include recombining the streams in a manner using mathematical operations. In a preferred embodiment the distributor block 350 uses a type IV Discrete Cosine Transform (DCT) for processing the filtered sample streams. The bifurcated filter structure described previously further permits a small DCT structure in implementation by making use of the inversion and time reversal properties of the filter. The bifurcated filter structure may also permit use of a DCT employing a sparse matrix decomposition structure.

The combination of the filter bank 330a-N, summing node 340a-N, and distributor 350 results in generating a set of output streams, each representing the separated data content from a physical channel. The set of individual physical channels from the distributor 350 are generated from the set of decimated sample streams where each stream contains content from each of the physical channels in a sample aliased condition. It should be noted that other methods may be employed for accomplishing recovery of separate physical channels simultaneously from a single signal.

The output of distributor block 350 represents N individual physical channels positioned at or near to baseband frequency. Each physical channel, in digital signal form, may be located on a separate signal line at the output of distributor block 350. Each of the separate signal lines connect to a channel selector block 360. The channel selector block 360 may select a set of physical channels from the original N input channels provided. Any number of channels up to the full number N may be selected. For instance, four channels may be selected. The number of channels permitted for selection in channel selector block 360 is a

design choice, and the full number of permitted channels for selection does not have to be selected at any one time. Additionally, any further physical channel separation may be performed, such as removing any aliasing components present due to the complex form of the signal as a result of the previously described processing.

The channel selector block 360 receives inputs from a controller 370 regarding which, if any, of the originally received physical channels is currently requested by the customer. The controller 370 may connect to the sample demultiplexer 310, interface 320, filter bank 330a-N, and distributor 350 in addition to connecting to channel selector 360. The controller 370 may also provide an interface for user inputs or a communications input in order to receive and convey the user requested channel information from multiple locations. As described previously, the user inputs may be supplied through the signal cable or through some other communications means. Also, as described previously, a home or customer premises may supply more than one customer input. In addition, controller 370 may provide additional functions for operation of the demultiplexer 310, interface 320, filter bank 330a-N, and assembler 350, such as clock functions, as necessary. The controller 370 may also be embodied as a portion of a larger controller function responsible for controlling and managing, for instance, the entire FTM device.

Turning now to FIG. 4, a block diagram 400 of a further embodiment of the present invention is shown. FIG. 4 illustrates an implementation of the digital channel re-combiner 240. The M outputs, representing a set of selected physical channels, of channel selector 360 are provided to the assembler 410. As described previously, the M outputs of the channel selector 360 may be equal to or less than the N physical channels present in the original L-band signal. In a preferred embodiment, the assembler 410 may receive up to N inputs. If the number of signals provided from channel selector 360 is less than N, the remaining inputs of channel assembler 410 are placed in a condition of

"null" or no input. Additionally, the assembler 410 may also provide the ability to re-order the M input signals. For instance, if the M signals provided to the assembler 410 are physical channels in positions 1, 2, 3, and 4 from selection of the original N channels, the assembler 410 may re-position the M signals by addressing them as inputs 1, 5, 9, and N-1. In this manner, further processing, including internal or external filtering may be simplified. Also, the re-positioning permits re-spacing of the M signals.

The assembler 410 provides processing for converting the selected channels into a set of signals forming a base set of parallel data streams that can then be filtered prior to remultiplexing and converting to an analog signal. The channel re-combiner 410 provides N outputs as a set of converted sample streams to inverse filter bank 420a-N. The inverse filter bank 420a-N provides filtering and/or time delay operations necessary to permit signal remultiplexing. The output of the inverse filter bank 420a-N provides a set of inverse filtered sample streams.

The inverse filtered sample streams at the output of the inverse filter bank 420a-N are provided to the sample multiplexer 430. The sample multiplexer 430 re-combines the samples, in a time multiplexing fashion, into a single sample stream. The sampling rate of the new single sample stream is preferably $2NF_s$ (F_s is the data rate of one channel). Clock signals representing both the input parallel sample stream rate and the new sampling rate at the output of the sample multiplexer 430 are also provided.

In a preferred embodiment, the assembler 410 is realized as an inverse type IV DCT, and the filter bank 420a-N is realized as an effective inverse bifurcated filter bank with respect to filter bank 330a-N as previously described. In this and other possible approaches, advantages exist due to the sparse matrix factorization stages containing a defined sparse inverse as well as the complementary form of the filtering stages. For example, the Type IV DCT is its own inverse i.e.,

(DCT IV)^2=I (identity matrix), and the bifurcated filters work with the transform elements to shape the bands of independent physical channels. Also, the inverse filter bank 420a-N, shown as a bifurcated filter structure has a signal splitting at its input for providing a cross coupling of signals to the even and odd branches of the individual filters. After each branch in the individual filters has completed processing, the even and odd branches of each individual filter are summed together to form the individual output signal.

Alternatively, since the type IV DCT function in both the distributor 350 and assembler 410 may be the same, only one block for both operations may be used. For example, a single block may, in conjunction with a signal multiplexer (not shown), provide either an output signal representing the set of individual physical channels or the base set of parallel data streams in alternating operations.

A controller 470 may connect to the assembler 410, filter bank 420a-N, and sample multiplexer 430. The controller 470 may control the final selection process and ordering of selected physical channels in assembler 410. The controller 470 may follow a pre-programmed allocation and ordering algorithm, or may process user inputs to determine the allocation and ordering. The controller 470 may also provide an interface for user inputs or a communications input in order to receive and convey the user requested channel information from multiple locations. As described earlier, a home or customer premises may supply more than one customer input. In addition, controller 470 may provide additional functions for operation of the assembler 410, filter bank 420a-N, and multiplexer 430 such as clock functions, as necessary. The controller 470 may also be embodied as a portion of a larger controller function responsible for controlling and managing, for instance, the entire FTM device.

Additionally, if the M signals at the input to the assembler 410 are less than the N original channels, the channel re-combiner may also

change the overall sampling rate. The assembler 410 may be reconfigured to process the M signals in an M point transform, producing M parallel data streams. The filter bank may subsequently contain only M branches and the sample multiplexer process only M inputs. The clocks, supplied to the D/A converter as well as other blocks with diagram 400 may also be a scaled version of the clock used for digital channel selector 230. For instance, if M is one half the number N, then the clock signal for the digital channel re-combiner 240 may be one half the frequency of the clock signal for the digital channel selector 230. Note that the clock signal supplied to the other blocks working on parallel data streams may remain unaffected.

Further, the choice of value of M may be chosen to permit a maximum of allowable channels at any time. However, in actual operation, a number less than M channels may actually be in use.

Turning now to FIG. 5, a block diagram of another embodiment of the present invention is shown. FIG. 5 illustrates a three L-band signal input FTM utilizing the inventive concept described herein. Each L-band input signal is processed through RF input processing, not shown. Each L-band signal is further processed in A/D converter 520a-c, and digital channel selectors 530a-c as described previously. Also, D/A converter 550 and output RF processing block 560 operate as described previously.

Each digital channel selector 530a-c is capable of producing M outputs representing M physical channels where M is less than or equal to the N original physical channels from an L-band signal. Each L-band signal may provide a different number of physical channels.

The digital channel re-combiner 540 may process up to N channels in its assembler block as described above. The assembler in the digital channel re-combiner 540 also includes switching and selection circuits to manage which of the M inputs from each of the digital channel selectors 530a-c are processed in the digital channel re-combiner 540.

The management and switching function is controlled by the controller 570.

The controller 570 provides functions to ensure that a selected combination of the M outputs from the selectors 530a-c does not exceed the N inputs for selected channels possible for processing in digital channel re-combiner 540. The controller 570 receives inputs from the one or more users and processes the inputs to determine the correct combination of inputs. In a preferred embodiment, each of the digital channel selectors 530a-c may provide up to six signals to the digital channel re-combiner. The digital channel re-combiner 540 may accept only sixteen signals. The controller 570 may determine, for instance based on inputs from users, that only five inputs will be used from digital channel selectors 530a and 530b, and all six will be used from digital channel selector 530c. Additional user inputs may then require a change to this apportionment. The controller 570 may also provide control or other necessary signals such as clock signals to A/D converters 520a-c, digital channel selectors 530a-c and D/A converter 550.

The digital channel re-combiner 540 may also contain signal processing such as digital signal level adjustment applied to each of the selected channels. Level adjustment may allow all selected channels to be delivered at approximately the same signal level improving the operation of home equipment such as settop boxes.

Block diagram 500 forms a multi-input, single output channel selection, translation, and distribution device. The device produces an output of up to N channels in a single signal for delivery over a single coaxial cable, from an input containing up to three times N possible input channels presented in three separate signals. The use of three inputs is illustrative, and a greater or fewer number of inputs containing a greater or fewer number of possible input channels may be used.

Turning now to FIG. 6, a flow chart 600 showing an embodiment of the method of the present invention is shown. At step 602, one or more

incoming satellite signals are received by a device, such as the FTM device described previously in block diagram 500. Next, at 604, the incoming satellite signals are converted to digital signals. The conversion is preferably performed by A/D converters 530a-c, and may further include a processing means for separating the individual physical channels after the conversion such as described in digital channel selectors 530a-c.

Next, at step 606, the desired physical channels are selected to form a group of selected physical digital channels in parallel. The selected physical channels are selected in the digital channel selectors 530a-c based on requests by the customer's home equipment processes and managed by, for instance, controller 570. The controller 570 may be responsible for receiving and managing multiple requests and providing the proper information to the digital channel selectors 530a-c as well as the digital channel re-combiner 540.

The group of selected digital channels, at step 608, are re-combined in a frequency diverse manner to form a signal occupying a range of frequencies and containing the selected digital channels at separate frequencies. The recombination may include a means for processing the group of selected digital channels such as described for digital channel re-combiner 540. At step 610, the recombined frequency diverse signals are converted back into an analog signal containing the selected channels at separate frequencies. The conversion may be done using a D/A converter 550 and may also include any additional processing as described for output RF processing block 560. Finally, at step 612, the analog signal is sent or transmitted to additional devices, for instance devices found in customer premises connected by a single coaxial cable.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. The

foregoing merely illustrates the principles of the invention and it will thus be appreciated that those skilled in the art will be able to devise numerous alternative arrangements which, although not explicitly described herein, embody the principles of the invention and are within its spirit and scope. For example, although illustrated in the context of separate functional elements, these functional elements may be embodied on one or more integrated circuits (ICs). Similarly, although shown as separate elements, any or all of the elements of may be implemented in hardware, software, or a combination of both. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the scope of the present invention as defined by the appended claims.

What is claimed is:

1. An apparatus (500) comprising:

a receiver (520a-c, 530a-c) for receiving and digitizing a plurality of first signals, each signal containing one or more different channels and for simultaneously recovering a plurality of selected channels from said plurality of first signals; and

a transmitter (540, 550, 560) for combining said plurality of selected channels and producing a second signal.

2. The apparatus (500) set forth in claim 1, wherein said receiver (520a-c, 530a-c) further comprises:

a sampler (310, 320, 330a-N) for sampling said plurality of first signals to provide a plurality of decimated sample streams; and

a distributor (350) operatively connected to said sampler (310, 320, 330a-N) for processing said plurality of decimated sample streams to provide output signals representative of said one or more different physical channels.

3. The apparatus (500) of claim 2, wherein said distributor (350) includes a transform element.

4. The apparatus (500) of claim 3, wherein said transform element performs matrix-based processing on said plurality of decimated sample steams using a sparse matrix factorization of a type IV discrete cosine transform.

5. The apparatus (500) of claim 2, wherein said sampler (310, 320, 330a-N) further comprises:

a demultiplexer (310) for demultiplexing the signal into said plurality of decimated sample streams; and

a plurality of filters (330a-N) operatively connected to said demultiplexer (310) for processing said plurality of decimated sample streams.

6. The apparatus (500) of claim 5, wherein said plurality of filters (330a-N) includes a plurality of bifurcated filters.

7. The apparatus (500) of claim 1, wherein said receiver (530a-c) further comprises a selector (360) operatively connected to said distributor (350) for selecting said plurality of selected channels.

8. The apparatus (500) of claim 1, wherein said transmitter (540, 550, 560) further comprises:

an assembler (410) that assembles said plurality of selected channels to provide a set of parallel data streams representing the combination of said plurality of channels; and

a converter (420a-N, 430) for converting said parallel data streams into said second signal.

9. The apparatus (500) of claim 8, wherein said assembler (410) includes a transform element.

10. The apparatus (500) of claim 9, wherein said transform element performs matrix-based processing on said plurality of selected channels using a sparse matrix factorization of type IV discrete cosine transform.

11. The apparatus (500) of claim 8, wherein said converter further comprises:

a plurality of filters (420a-N) for processing said plurality of parallel data streams; and

a multiplexer connected to said plurality of filters for multiplexing said plurality of parallel data streams into a single sample stream.

12. The apparatus (500) of claim 11, wherein said plurality of filters (420a-N) includes a plurality of bifurcated filters.

13. A method (600) for providing frequency translation comprising:

receiving (602) a first signal having a plurality of different frequency channels;

selecting (606) a set of frequency channels from said plurality of different frequency channels;

combining (608) said set of frequency channels to form a second signal; and

transmitting (612) said second signal.

14. The method (600) of claim 13, wherein the step of selecting further comprises:

processing (604) said first signal to provide a plurality of decimated sample streams; and

performing (606) a transform on said number of decimated sample streams to provide transform output signals.

15. The method (600) of claim 14, wherein the step of processing (604) includes:

demultiplexing the signal into the number of decimated sample streams; and

filtering said number of decimated sample streams with a plurality of filters for matching said transform.

16. The method (600) of claim 15, wherein said plurality of filters include a plurality of bifurcated filters and said transform is a type IV discrete cosine transform.

17. The method (600) of claim 13, wherein the step of selecting further comprises re-ordering said set of frequency channels.

18. The method (600) of claim 13, wherein said step of combining (608) further comprises:

performing transform-based processing on said set of different frequency channels to provide a plurality of parallel data streams; and

processing said plurality of parallel data streams to provide said second signal.

19. An integrated circuit (500) for use in a receiving system, which receives signals representing a plurality of channels, the integrated circuit comprising:

a demultiplexing element (310) for demultiplexing a received sampled signal to produce a plurality of first data streams;

a transform element (350, 410) for transforming said plurality of first data streams into a plurality of transform output signals, and for transforming at least two of said plurality of transform output signals into a plurality of second data streams; and

a multiplexing element (430) for mulitplexing said plurality of second data streams and outputting a sampled signal.

20. The integrated circuit (500) of claim 19, wherein said transform element (350, 410) uses a type IV discrete cosine transform.

21. The integrated circuit (500) of claim 20, further comprising:

a first filter element (330a-N) operative to filter said plurality of first data streams prior to providing said plurality of first data streams to said transform element; and

a second filter element (420a-N) operative to filter said plurality of second data streams prior to providing said plurality of second data streams to said multiplexing element.

22. An apparatus (500) for frequency translation comprising:

means for receiving (520a-c) a first signal having a plurality of different frequency channels;

means for translating (530a-c) said first signal into a set of signals representing said plurality of different frequency channels;

means for selecting (530a-c) a set of channels from said set of signals;

means for combining (540) said set of channels to form a second signal; and

means for transmitting (550, 560) said second signal.

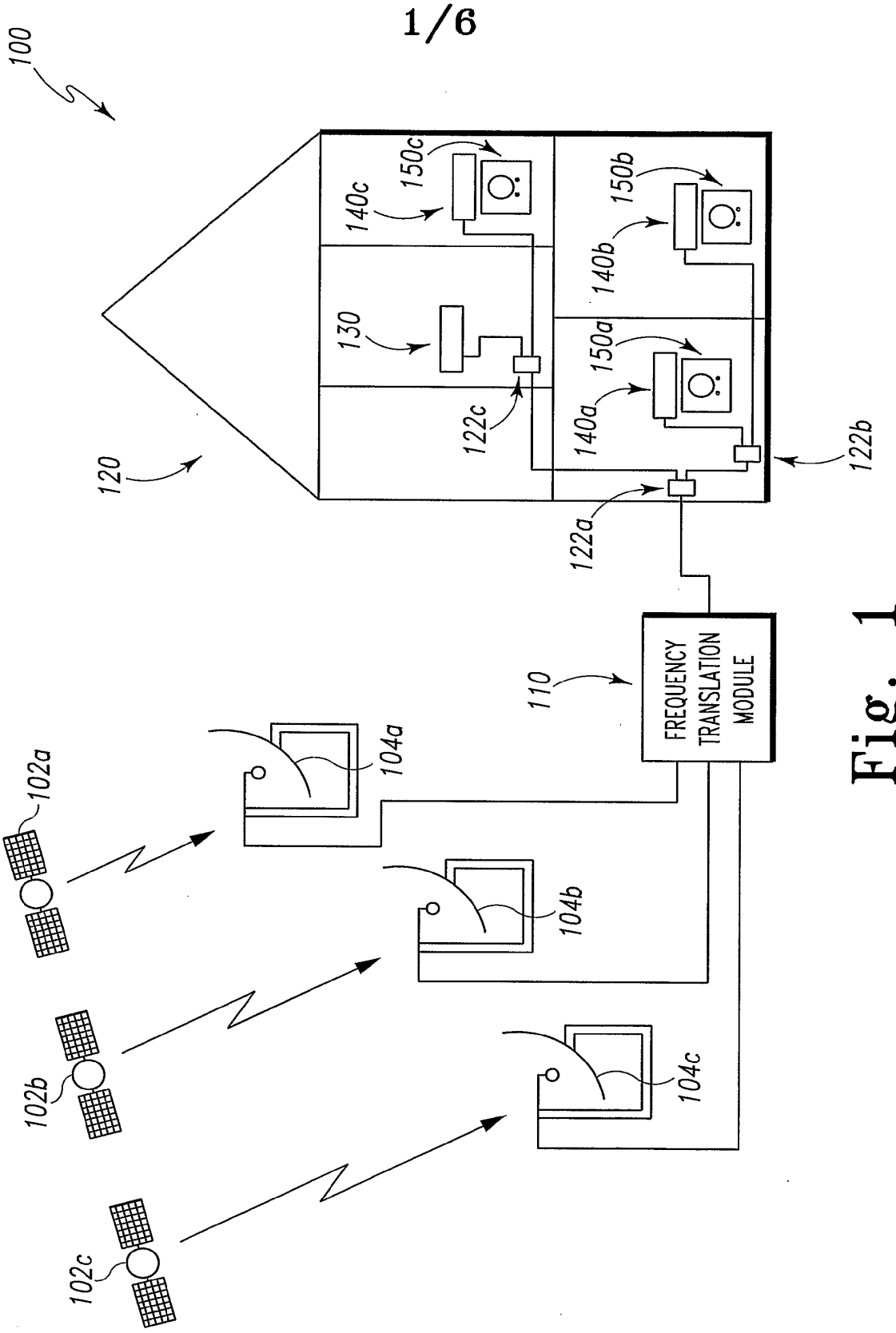

100
120
140c
150c
130
122c
140b
150b
140a
150a
122b
122a
110
FREQUENCY TRANSLATION MODULE
102a
104a
104b
102b
104c
102c

Fig. 1

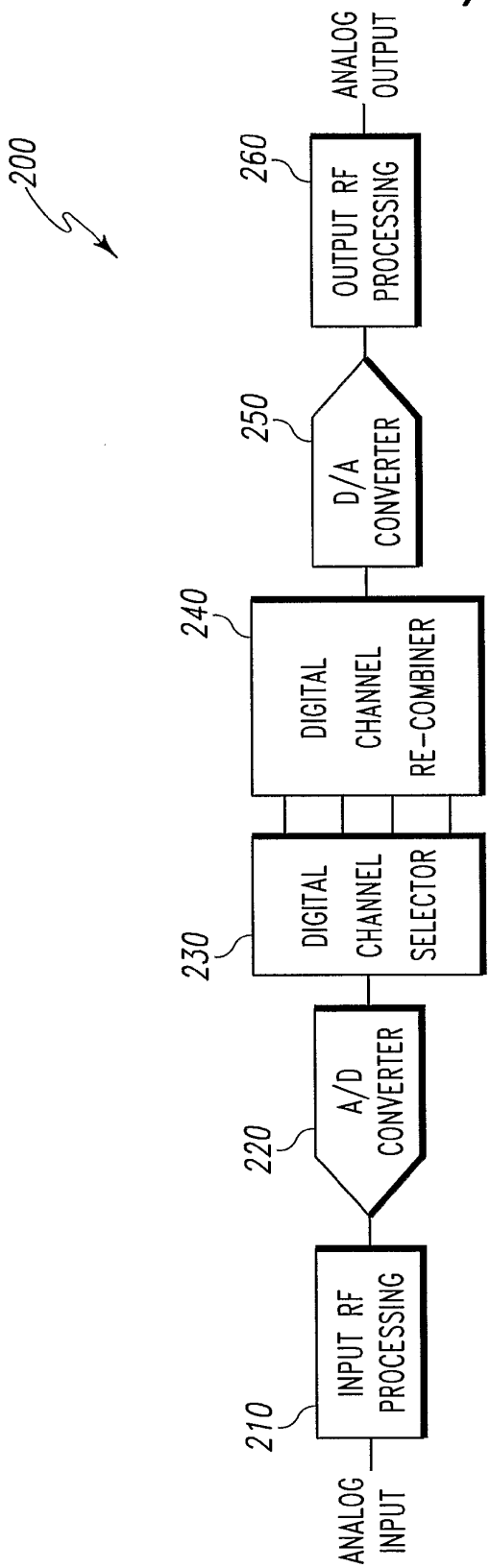

200
ANALOG INPUT
210
INPUT RF PROCESSING
220
A/D CONVERTER
230
DIGITAL CHANNEL SELECTOR
240
DIGITAL CHANNEL RE-COMBINER
250
D/A CONVERTER
260
OUTPUT RF PROCESSING
ANALOG OUTPUT

Fig. 2

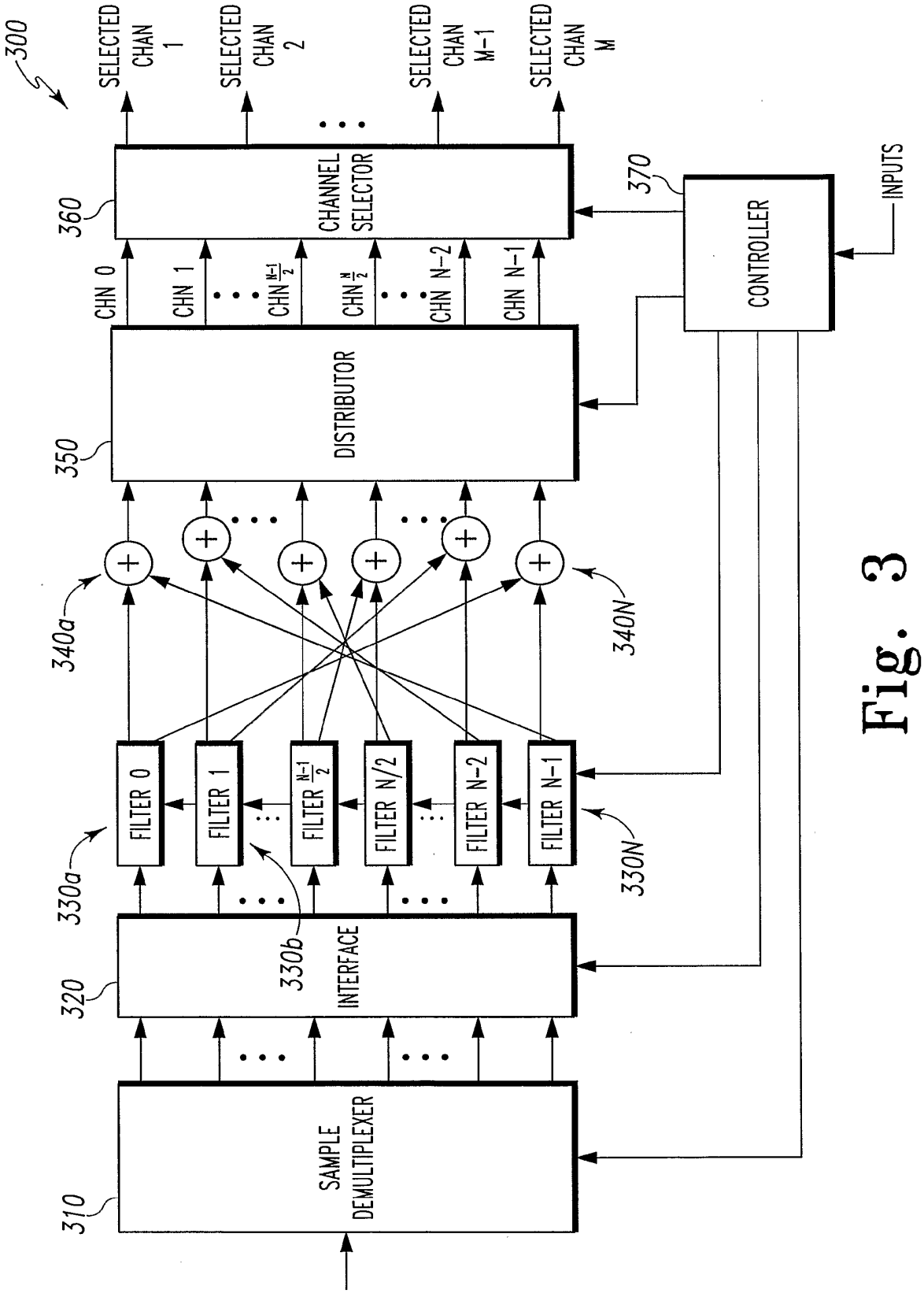

300
SELECTED CHAN 1
SELECTED CHAN 2
SELECTED CHAN M-1
SELECTED CHAN M
360
CHANNEL SELECTOR
370
CONTROLLER
INPUTS
CHN 0
CHN 1
CHN (N-1)/2
CHN N/2
CHN N-2
CHN N-1
350
DISTRIBUTOR
340a
340N
FILTER 0
FILTER 1
FILTER (N-1)/2
FILTER N/2
FILTER N-2
FILTER N-1
330a
330b
330N
320
INTERFACE
310
SAMPLE DEMULTIPLEXER

Fig. 3

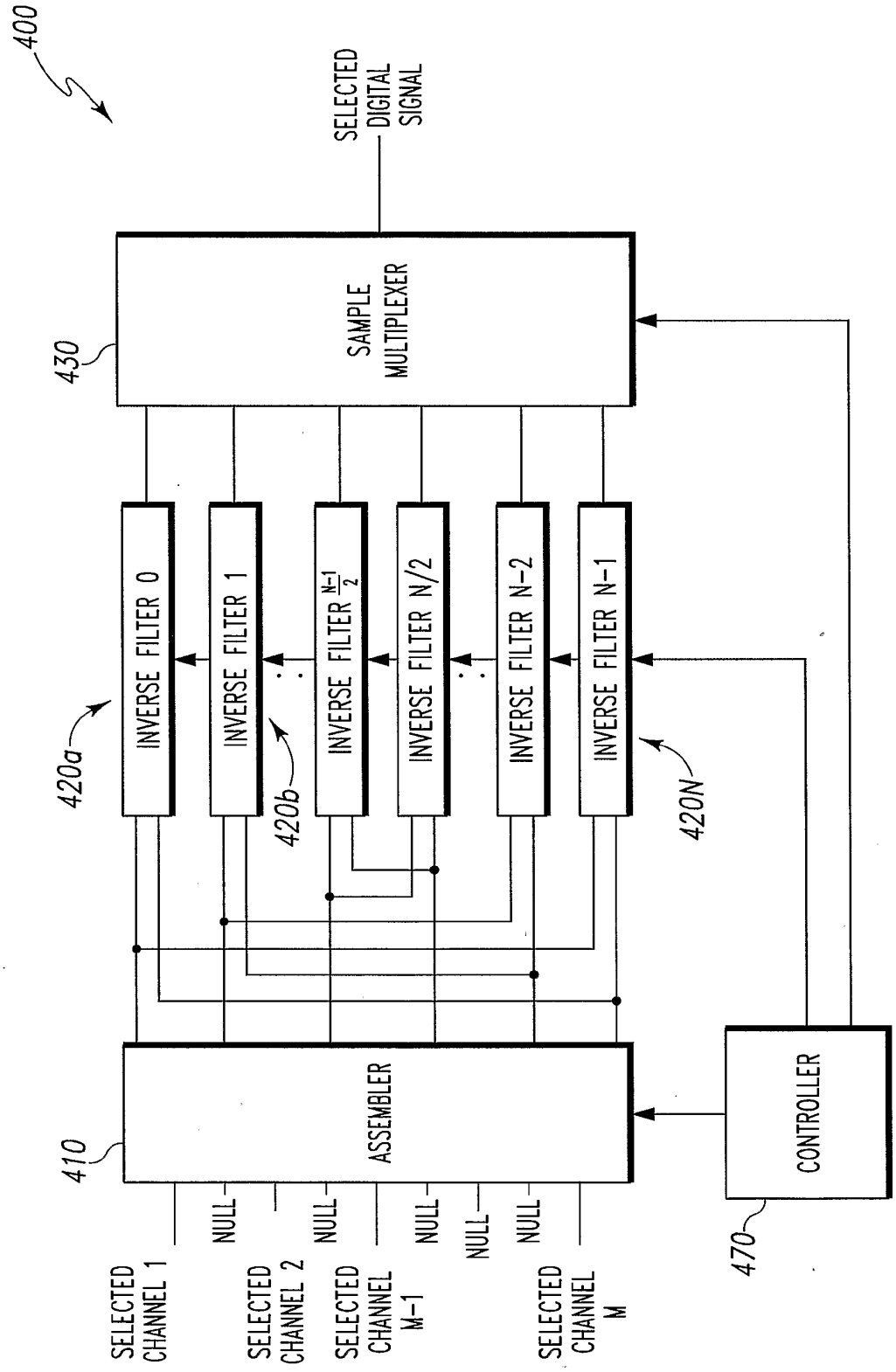

400
SELECTED DIGITAL SIGNAL
SAMPLE MULTIPLEXER
430
INVERSE FILTER 0
INVERSE FILTER 1
INVERSE FILTER $\frac{N-1}{2}$
INVERSE FILTER N/2
INVERSE FILTER N-2
INVERSE FILTER N-1
420a
420b
420N
ASSEMBLER
410
CONTROLLER
470
SELECTED CHANNEL 1
NULL
SELECTED CHANNEL 2
NULL
SELECTED CHANNEL M-1
NULL
NULL
NULL
SELECTED CHANNEL M

Fig. 4

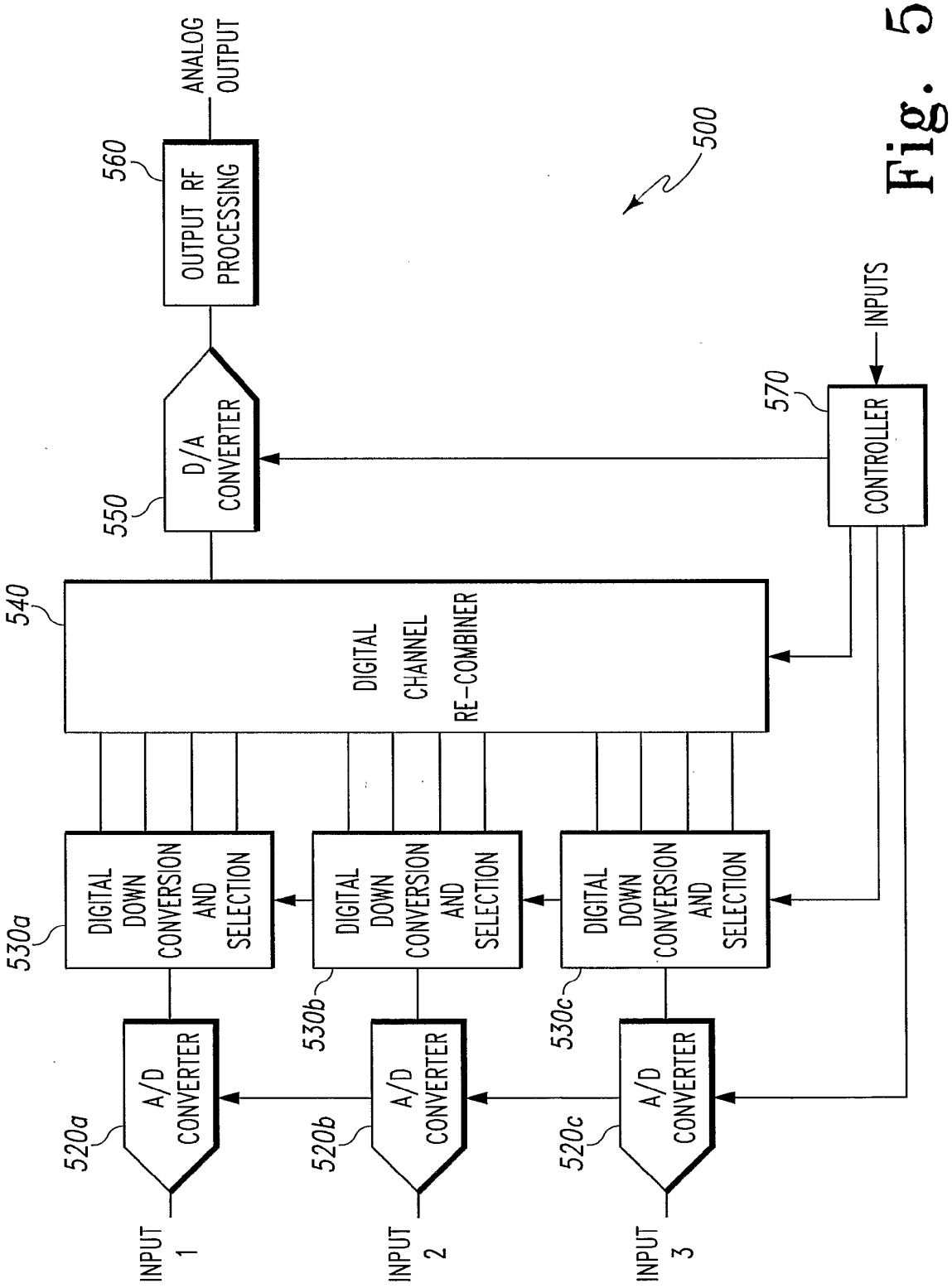

500
ANALOG OUTPUT
560
OUTPUT RF PROCESSING
D/A CONVERTER
550
INPUTS
570
CONTROLLER
540
DIGITAL CHANNEL RE-COMBINER
530a
DIGITAL DOWN CONVERSION AND SELECTION
530b
DIGITAL DOWN CONVERSION AND SELECTION
530c
DIGITAL DOWN CONVERSION AND SELECTION
520a
A/D CONVERTER
520b
A/D CONVERTER
520c
A/D CONVERTER
INPUT 1
INPUT 2
INPUT 3

Fig. 5

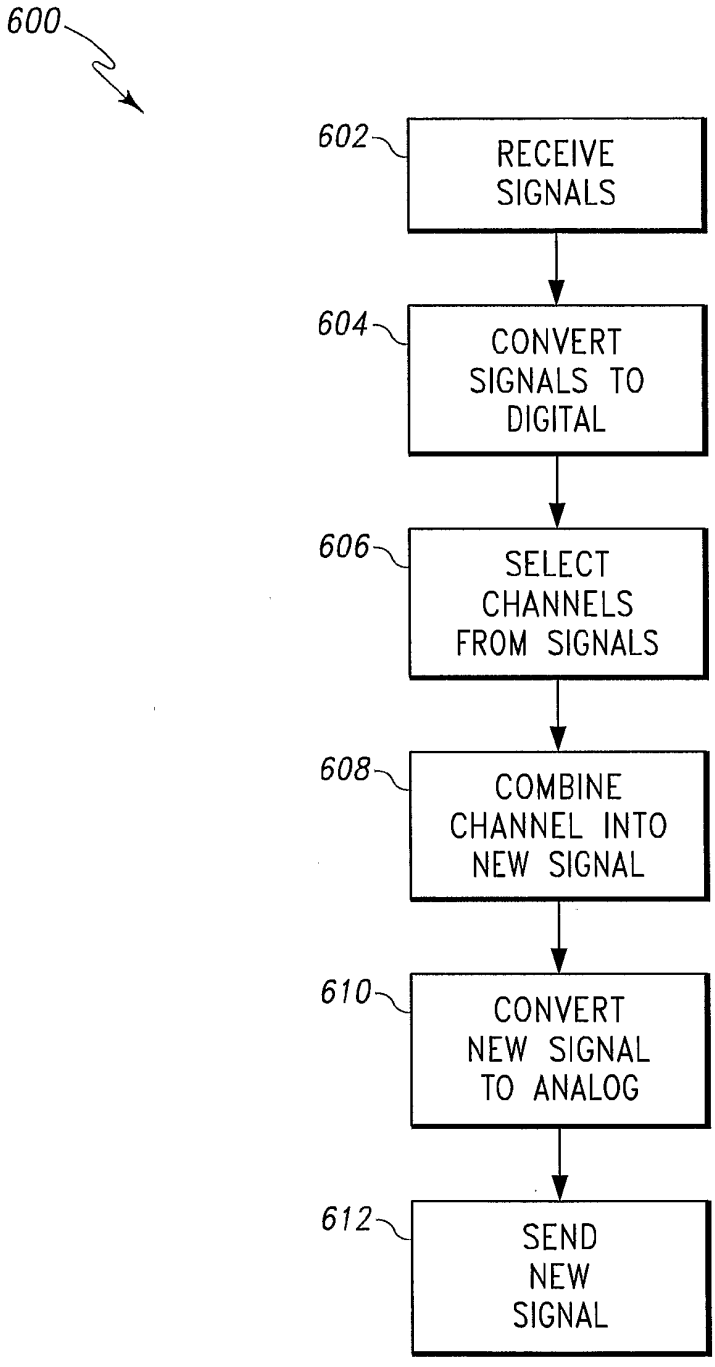
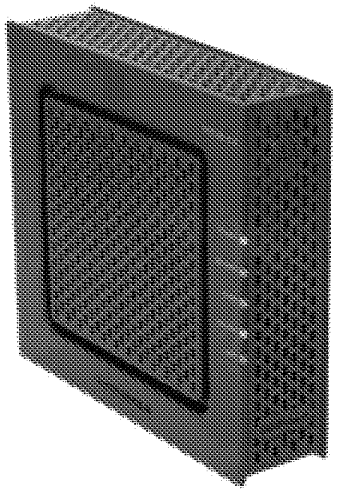

600
602
RECEIVE SIGNALS
604
CONVERT SIGNALS TO DIGITAL
606
SELECT CHANNELS FROM SIGNALS
608
COMBINE CHANNEL INTO NEW SIGNAL
610
CONVERT NEW SIGNAL TO ANALOG
612
SEND NEW SIGNAL

Fig. 6

DATA SHEET





SURFboard® SB6120
Cable Modem

Strengthen your broadband leadership — Count on Motorola's SURFboard DOCSIS® / EuroDOCSIS 3.0 CPE to help you deliver innovative, ultra broadband data services to your premium customers.

Highlights

Compatible with Windows®, Macintosh®, and UNIX® computers

DOCSIS 3.0 and EuroDOCSIS 3.0 Certified, featuring:

- Channel bonding of up to 4 downstream channels and 4 upstream channels increasing data rates of well over 100 Mbps in each direction
- Supports IPv4 and IPv6 to expand network addressing capabilities
- Enhanced security: supports AES traffic encryption

Enhanced network management

Ability to provision and manage IP multicast

GigE (RJ-45) data port with Auto Negotiate and Auto MDIX

Front Panel LEDs indicate status and simplify troubleshooting

User-friendly online diagnostics

Remotely configurable and monitorable using SNMP and TFTP

High Value and Increased Data Rates

Motorola's easy-to-use SB6120 SURFboard DOCSIS 3.0 Cable Modem unlocks the potential of offering innovative high-bandwidth data and multimedia services to customers.

Utilizing the power of DOCSIS 3.0, the SB6120 enables channel bonding of up to 4 downstream channels and 4 upstream channels – which allows an operator to offer their customers advanced multimedia services with data rates of well over 100 Mbps in each direction. The SB6120's higher-speed services enable operators to:

- Protect their installed base of high-speed data customers
- Deliver high-bandwidth, multimedia services
- Deliver competitive, high-capacity commercial services to their business customers

Economic and Flexible

The Motorola SB6120 SURFboard DOCSIS 3.0 Cable Modem provides operators with an economic option for providing Ultra-Broadband services, with 4X the current maximum user data throughput approximating 160 Mbps in DOCSIS mode and 195 Mbps in EuroDOCSIS mode*, without the need for hybrid fiber coax (HFC) plant upgrade. Maximizing an operator's current infrastructure investment, the SB6120 can be deployed without service interruption.

Backwards compatible to DOCSIS 1.0, 1.1 and 2.0, the SB6120 also supports both IPv4 and IPv6, Advanced Encryption Services, and all other DOCSIS 3.0 standards.

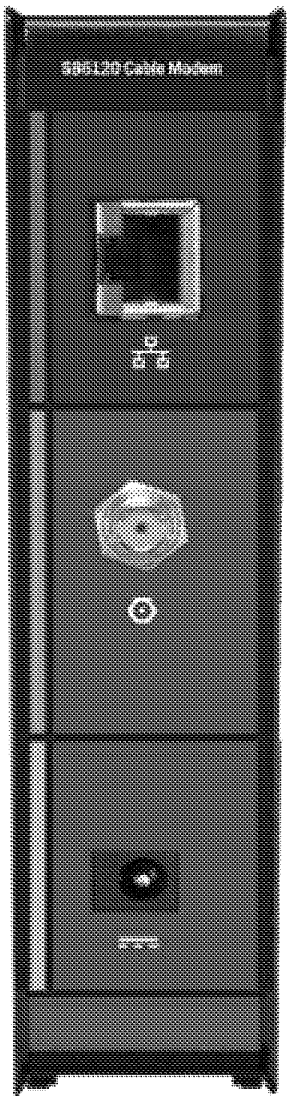
As part of Motorola DOCSIS 3.0 Ultra-Broadband family of products, the SB6120 includes an enhanced tuner that supports up to a 1 GHz downstream input allowing operators to increase the frequency spectrum for deployment of new high-value services such as bandwidth on-demand, commercial services, interactive gaming and IPTV to their customers.

The SB6120 features a 10/100/1000Base-T Ethernet (RJ-45) port, as well as intuitive, easy to read front-panel operational status LEDs. Operators can optionally activate dual colored LEDs for their customer to have visual verification of bonded channels and GigE link use.

With Motorola's cable modems, high-speed Internet access has always been at your fingertips – always on and always connected. The SB6120 is the ideal competitive solution for the high-end residential user, the small home office owner, as well as the medium to large business enterprise.

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DATA SHEET
SURFboard® SB6120
Cable Modem



Motorola's Service Assured DOCSIS® 3.0 Solutions enable you to deliver increased bandwidth, enhance security, and cost-effectively deploy data services to your bandwidth-demanding consumers — all while maximizing current infrastructure investment and lowering capital spend.

ECOMOTO™

Motorola's SB6120 SURFboard® Cable Modems are helping service providers lower their carbon footprint by helping them lower energy consumption. Motorola has a global commitment to be part of the solution to climate change, working for years to continually improve the environmental profile of our products, operations and supply chain. We work in step with our customers and their increasing interest in partnering with a company that will help them reduce their environmental impact, while offering compelling products that will help them grow their end-consumer customer base.

Motorola designed the next generation of SURFboard products of customer premises equipment (CPE) to minimize its impact on the environment. Motorola's CPE comply with international environmental and energy efficient standards. The portfolio uses ENERGY STAR qualified power supplies and its devices and power supplies are compliant with European Code of Conduct requirements. In addition, the devices and power supplies are lead-free and RoHS compliant. Finally, all new SB6120 SURFboard Cable Modems use environmentally friendly package designs. The SB6120 cable modems are available in single box pack boxes – eliminating the use of styrofoam plastic and reducing box size – thereby reducing waste and transport costs. Motorola SB6120 cable modem packaging is 100% recyclable and is marked with standard recycling codes to make it easier for our customers to identify recycling opportunities.

General Specifications

Cable Interface	75 Ω F-connector
CPE Network Interface	10/100/1000Base-T Ethernet (RJ-45)
Data Protocol	TCP/IP
Dimensions	5.7 in H x 5.7 in W x 1.5 in D (146 mm x 146 mm x 38 mm)
Power	9W (nominal)
Input Power	
North America	105 to 125 VAC, 60 Hz
Outside North America	100 to 240 VAC, 50 to 60 Hz
Regulatory	Unit is RoHS compliant, ENERGY STAR V2 , COC V3, Compliant per the "Code of Conduct on Energy Consumption of Broadband Equipment", CMM, MEPS

Environmental

Operating Temperature	32 °F to 104 °F (0 °C to 40 °C)
Storage Temperature	–22 °F to 158 °F (–30 °C to 70 °C)
Operating Humidity	5 to 95% R.H. (non-condensing)

Downstream

Modulation	64 or 256 QAM
Capture Bandwidth	100 MHz (edge to edge)
Maximum Theoretical Data Rate**	
DOCSIS	171.537 Mbps (4 channels) / 42.884 (single channel) @ 256 QAM at 5.36 Msym/s
EuroDOCSIS	222.464 Mbps (4 channels) / 55.616 (single channel) @ 256 QAM at 6.952 Msym/s
Bandwidth	
DOCSIS	≤ 24 MHz
EuroDOCSIS	≤ 32 MHz
Symbol Rate	
DOCSIS	64 QAM 5.057 Msym/s; 256 QAM 5.361 Msym/s
EuroDOCSIS	64 QAM 6.952 Msym/s; 256 QAM 6.952 Msym/s
Operating Level Range	–15 to 15 dBmV
Bonded Channel RF Level Tolerance	10dBmV
Input Impedance	75 Ω (nominal)
Frequency Range	DOCSIS and EuroDOCSIS 108 to 1002 MHz (edge to edge), Optional 81 to 1002 MHz (edge to edge)
Frequency Plan	
EuroDOCSIS	Annex A
DOCSIS	Annex B
J-DOCSIS	Annex B, modified for Japan Frequencies
Security	DOCSIS 3.0 Security (BPI+, EAE, SSD)
Network Management	SNMP v2 & v3
Provisioning	Supports IP addressing using IPv4 and/or IPv6 (dual stack)

DATA SHEET
SURFboard® SB6120
Cable Modem

Upstream

Modulation		QPSK and 8, 16, 32, 64, 128 QAM
Maximum Channel Rate**		
	DOCSIS	131.072 Mbps (4 channels) / 32.768 Mbps (single channel)* @ 128 QAM at 6.4 MHz
	EuroDOCSIS	131.072 Mbps (4 channels) / 32.768 Mbps (single channel)* @ 128 QAM at 6.4 MHz
Channel Width		200 kHz, 400 kHz, 800 kHz, 1.6 MHz, 3.2 MHz, 6.4*** MHz
Symbol Rates		160, 320, 640, 1280, 2560, 5120*** ksym/s
Operating Level Range		Level range per channel (Multiple Transmit Channel mode disabled, or only Multiple Transmit Channel mode enabled with one channel in the TCS)
	DOCSIS/EuroDOCSIS	
	TDMA	Pmin to +57 dBmV (32 QAM, 64 QAM) Pmin to +58 dBmV (8 QAM, 16 QAM) Pmin to +61 dBmV (QPSK)
	S-CDMA	Pmin to +56 dBmV (all modulations), where: Pmin = +17 dBmV, 1280 kHz modulation rate Pmin = +20 dBmV, 2560 kHz modulation rate Pmin = +23 dBmV, 5120 kHz modulation rate
	Level range per channel (two channels in the TCS)	
	TDMA	Pmin to +54 dBmV (32 QAM, 64 QAM) Pmin to +55 dBmV (8 QAM, 16 QAM) Pmin to +58 dBmV (QPSK)
	S-CDMA	Pmin to +53 dBmV (all modulations), where: Pmin = +17 dBmV, 1280 kHz modulation rate Pmin = +20 dBmV, 2560 kHz modulation rate Pmin = +23 dBmV, 5120 kHz modulation rate
	Level range per channel (three or four channels in the TCS)	
	TDMA	Pmin to +51 dBmV (32 QAM, 64 QAM) Pmin to +52 dBmV (8 QAM, 16 QAM) Pmin to +55 dBmV (QPSK)
	S-CDMA	Pmin to +50 dBmV (all modulations), where: Pmin = +17 dBmV, 1280 kHz modulation rate Pmin = +20 dBmV, 2560 kHz modulation rate Pmin = +23 dBmV, 5120 kHz modulation rate
Output Impedance		75 Ω (nominal)
Frequency Range		DOCSIS 5-42 MHz (edge to edge), EuroDOCSIS and optional DOCSIS 5 to 65 MHz (edge to edge)
Compatibility		PC: 80486, Pentium, or later; Windows Vista™, 2000, or XP or Linux® with Ethernet connection (older versions of Windows, although not specifically supported, will work with this cable modem) Macintosh: Power PC or later, OS 9 or higher, Ethernet connection UNIX: Ethernet connection Home Networking: Ethernet router or wireless access point

* Actual speeds will vary, and are often less than the maximum possible. Data transmission speed is approximate and depends on the configuration and capacity of your network, as well as the amount of traffic on the network.

** Actual data throughput will be less due to physical layer overhead (error correction coding, burst preamble, and guard interval).

*** With A-TDMA- or S-CDMA-enabled CMTS.

**** With S-CDMA-enabled CMTS.

Certain features may not be activated by your service provider, and/or their network settings may limit the feature's functionality. Additionally, certain features may require a subscription. Contact your service provider for details.

All features, functionality, and other product specifications are subject to change without notice or obligation. DOCSIS 3.0 modem capabilities are dependant on the services available through the CMTS. Please verify with your CMTS vendor their specific DOCSIS 3.0 implementation roadmap.

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Total Number of Pages in This Submission

Application Number	90/019,255
Filing Date	09/20/2023
First Named Inventor	Madhukar Reddy
Art Unit	3992
Examiner Name	ANGELA M LIE
Attorney Docket Number	189005.TR003

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- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
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- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):
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  2. IDS along with Cover letter
  3. Applicant Summary of Interview

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	Application Number	90019255
	Filing Date	2023-09-20
	First Named Inventor	Madhukar Reddy
	Art Unit	3992
	Examiner Name	LIE, ANGELA M
	Attorney Docket Number	189005.TR003

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	Examiner Name	LIE, ANGELA M
	Attorney Docket Number	189005.TR003

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	90019255
	Filing Date	2023-09-20
	First Named Inventor	Madhukar Reddy
	Art Unit	3992
	Examiner Name	LIE, ANGELA M
	Attorney Docket Number	189005.TR003

	1	JEFFREY A. WELDON, et al. "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter With Harmonic-Rejection Mixers," IEEE Journal of Solid-Slate Circuits, December 2001, pages: 2003-2015, Vol. 36, No. 12, Seattle, WA, USA.	☐
	2	FRANCESCO GATTA, et al. "An embedded 65nm CMOS low-IF 48 MHz to 1 GHz dual tuner for DOCSIS 3.0," 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, Feb. 12, 2009,pages: 122-123, San Francisco, CA, USA.	☐
	3	System Art - Broadcom BCM 3380 Broadcom Jun. 10, 2008	☐
	4	Silicon-based RF front-ends for ultra wideband radios UWB textbook Jan. 2008	☐
	5	System Art - Motorola SURFboard cable modem SB6120 Motorola / Arris 2007	☐
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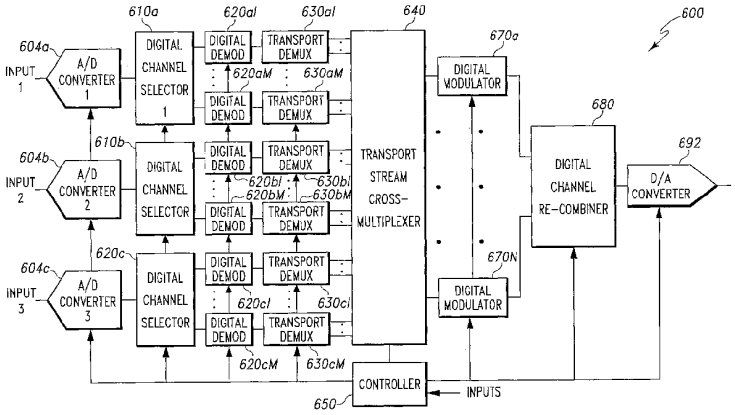
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(54) Title: APPARATUS AND METHOD FOR RE-SYNTHESIZING SIGNALS



(57) Abstract: The disclosed embodiments relate to an apparatus (600) and a method (700) for re-synthesizing signals. The apparatus (600) includes a receiver (604a-c, 610a-c) for receiving a plurality of digitally multiplexed signals, each digitally multiplexed signal associated with a different physical transmission channel, and for simultaneously recovering from at least two of the digital multiplexes a plurality of bit streams. The apparatus also includes a transmitter (640, 67Oa-N, 680) for inserting the plurality of bit streams into different digital multiplexes and for modulating the different digital multiplexes for transmission on different transmission channels. The method (700) involves receiving a first signal (702) having a plurality of different program streams in different frequency channels, selecting (706) a set of program streams from the plurality of different frequency channels, combining (712) the set of program streams to form a second signal, and transmitting (720) the second signal.

WO 2006/119489 A2

Apparatus and Method for Re-Synthesizing Signals

This application claims the benefit under 35 U.S.C.§ 119 of a provisional application 60/677563 filed in the United States on May 4, 2005.

FIELD OF THE INVENTION

The present invention generally relates to communications systems. More specifically, the present invention relates to the receiving and retransmission of content within a communications system.

BACKGROUND OF THE INVENTION

This section is intended to introduce the reader to various aspects of art, which may be related to various aspects of the present invention that are described and/or claimed below. This discussion is believed to be helpful in providing the reader with background information to facilitate a better understanding of the various aspects of the present invention. Accordingly, it should be understood that these statements are to be read in this light, and not as admissions of prior art.

In today's data communication systems such as used in satellite TV, data of different types often reside in what are known as virtual channels. The data from these virtual channels is separately disassembled into data packets, aggregated within and across different data types into bit streams and conveyed by packet delivery systems. Data consumer appliances, such as satellite receivers, select from physical channels available to them, convert the signals on these channels to digital form (packets) and collect the data packets required to re-assemble the desired virtual channels of information (e.g., audio, video, program guide, transactional data, etc.). At different points along the data path between a content provider and a content consumer data

management opportunities occur. A piece of data may come from one of many sources, be routed through one of many satellites, pass through several of many transponders aboard the satellite, be received by a consumer antenna, and be distributed to places of consumption.

Consumer receivers are often capable of receiving only one of the physical channels from the satellite at a time for display. However, new receivers may contain advanced features the consumer can use. For instance, a receiving device may contain more than one tuner for use in either two picture simultaneous display systems or content recording. Additionally, consumer households often include multiple receivers, each receiver requiring the tuning of one or more channels for use.

The ever-expanding amount of content for delivery has made it very difficult to deliver that content to all places at all times. Systems receiving data from up to four separate satellites to deliver programming to the home can no longer deliver all of the content on one coaxial cable connection. Various approaches have been adapted including the use of multiple cables or complex switching arrangements. Many of these approaches are in some manner suboptimal for a home installation due to high cost or high complexity.

Another solution may be to employ a system of preselecting, combining, and redistributing the incoming content based on the physical channels requested by the user(s) using analog signal processing. As a result, only the content required for delivery to the receivers in a household are selected from the initial available content. The desired content may then be provided on a single cable that is relatively easy to distribute around the household. The solution relies on coarse analog signal tuning and re-mixing to move channels or frequency regions of signals from an original spectral location in frequency at the input to another spectral location in frequency on a common signal at the output. Further, channels or signal regions at the same frequency but on different satellites may be combined by moving one or both of the

original channels or regions. These relocated signals containing the desired channels are then provided on the single cable, eliminating the need for any additional switching and multiple cable connections.

The analog solution involving preselection, combination, and redistribution remains limited in the number of channels that can be provided due to the inherent shortcomings of performing the processing in the analog domain. Narrow band filters used to select individual physical channels while rejecting others are impractical at frequencies above the range of one gigahertz (GHz). Available filters having a practical bandwidth require additional channel separation in order to prevent undesired interferences in the output signal. Additionally as the desire to deliver more requested channels to the home increases, the subsequent increase in analog circuit complexity results in an expensive and inefficient design with potential problems due to analog crosstalk. Further, the analog solution does not include additional capabilities involving channel data re-mulitplexing that may prove useful. The ability to manipulate the data streams in the digital domain increases the value and feature set of the network. Therefore, an apparatus and process for receiving and re-synthesizing of channels for distribution in a more optimal manner is desired.

SUMMARY OF THE INVENTION

The present invention relates to an apparatus and a method for re-synthesizing signals. The apparatus includes a receiver for receiving a plurality of digitally multiplexed signals, each digitally multiplexed signal associated with a different physical transmission channel, and for simultaneously recovering from at least two of the digital multiplexes a plurality of bit streams. The apparatus also includes a transmitter for inserting the plurality of bit streams into different digital multiplexes and

for modulating the different digital multiplexes for transmission on different transmission channels.

The method involves receiving a first signal having a plurality of different program streams in different frequency channels, selecting a set of program streams from the plurality of different frequency channels, combining the set of program streams to form a second signal, and transmitting the second signal.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a block diagram of an exemplary system using the present invention.

FIG. 2 is a block diagram of an embodiment of the present invention

FIG. 3 is a block diagram of another embodiment of the present invention.

FIG. 4 is a block diagram of yet another embodiment of the present invention.

FIG. 5 is a block diagram of yet another embodiment of the present invention.

FIG. 6 is a block diagram of a further embodiment of the present invention.

FIG. 7 is a flow chart illustrating a method of the present invention.

The characteristics and advantages of the present invention may become more apparent from the following description, given by way of example.

DETAILED DESCRIPTION

One or more specific embodiments of the present invention will be described below. In an effort to provide a concise description of these embodiments, not all features of an actual implementation are described in the specification. It should be appreciated that in the development of any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming, but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

It is noted that familiarity with television broadcasting and receivers is assumed and is not described in detail herein. For example, other than the inventive concept, familiarity with current and proposed recommendations for TV standards such as National Television Systems Committee (NTSC), Phase Alternation Lines (PAL), Sequential Couleur Avec Memoire (SECAM), Advanced Television Systems Committee (ATSC), and Direct Broadcast Satellite (DBS) is assumed. Likewise, other than the inventive concept, transmission concepts such as satellite transponders, down-link signals, eight-level vestigial sideband (8-VSB), Quadrature Amplitude Modulation (QAM), and receiver components such as a radio-frequency (RF) front-end, or receiver section, such as a low noise block, tuners, and demodulators is assumed. Similarly,

formatting and encoding methods (such as Moving Picture Expert Group (MPEG)-2 Systems Standard (ISO/IEC 13818-1)) for generating transport bit streams are well-known and not described herein. In addition, the inventive concept may be implemented using conventional programming techniques which, as such, will not be described herein.

The following describes a circuit used for processing satellite signals. Other systems utilized to receive and transmit other types of signals where the signal input may be supplied by some other means may include very similar structures. Those of ordinary skill in the art will appreciate that the embodiment of the circuits described herein is merely one potential embodiment. As such, in alternate embodiments, the components of the circuit may be rearranged or omitted, or additional components may be added. For example, with minor modifications, the circuits described may be configured to for use in non-satellite video and audio services such as those delivered from a cable network. Further, the re-synthesizer described could be used in conjunction with a home networking system. The re-synthesizer may receive inputs from a satellite or cable network, process them, and provide them as an output to the home network system. The output may in the form of a wired or wireless transmission.

Turning now to the drawings and referring initially to FIG. 1, an overall block diagram 100 of a system using the present invention is shown. FIG. 1 represents a typical satellite system installation at a customer home. A similar installation may also exist at an apartment complex or hotel where the system may be augmented with additional equipment often incorporated in multi-dwelling unit applications. Satellite transponders located on satellites 102a-c transmit satellite signals to satellite dishes 104a-c. Each satellite dish contains a reflector, a feed horn and a low noise block converter (LNB).

Each of the satellite signals may represent one or more individual physical channels. Each of the physical channels may in turn represent

one or more preferably digital bit streams of information combined together as a digital multiplex, encoded, and modulated using various analog and/or digital modulation techniques. The digital data streams are usually called program streams and may be streams of audio, video, or other data including program guide information. The physical channels are often grouped to cover a limited frequency range such as 500 to 1000 MHz of bandwidth. The satellite signals are often located in the microwave frequency range, for instance 11-13 Gigahertz (GHz). The LNBs in the satellite dishes 104a-c will amplify and convert the satellite signal in the 11-13 GHz range to an L-band signal in the 1-2 GHz frequency range. Although three satellite dishes are shown, the orbital locations of the satellites 102a-c may permit using one satellite dish containing one reflector and three feed horns and LNBs. Also, systems may utilize more or fewer than the three satellites signals illustrated here. The systems may additionally use techniques such as polarization diversity to increase the number of satellite signals delivered from each satellite.

Each of the three L-band signals from the satellite dishes 104a-c are provided through separate coaxial cables to a re-synthesizer 110. The three L-band signals in their entirety cannot be supplied through a single coaxial cable for delivery into the customer home, because the L-band signals occupy too much frequency bandwidth. As previously described, each L-band signal may occupy 1 GHz of bandwidth, and a typical customer premises cable installation may only support less than 2 GHz of total signal bandwidth. The re-synthesizer 110 extracts certain ranges of frequencies containing selected physical channels as portions of the three L-band signals provided. The re-synthesizer 110 also frequency translates the extracted ranges as needed and re-combines them to form a new single selected L-band signal. The process used by the re-synthesizer 110 may be described as a preselection of certain physical channels. However, the process used by the re-synthesizer

110 is different from a direct tuning of those certain physical channels since other energy besides the selected channel may be present, and the channels are then recombined to form a new signal for further distribution. Further, the re-synthesizer 110 also provides processing to recover the individual program streams from the physical channels present. The re-synthesizer 110 may also allow adding or removing of streams as well as re-arrangement of streams to form new physical channels of information. Note that the FTM 110 may reside physically outside the customer home as shown, or may reside very near to the entry point into the customer home or a multi-dwelling unit. For example, the re-synthesizer may be located in a room adjacent to the entry point for the cabling from the satellite dishes 104a-c. The room may include additional control devices for use with the network and the re-synthesizer 110.

Once the re-synthesizer 110 has preselected and processed the physical channels for use, the selected signal is provided over a single coaxial cable to the customer's premises 120. The selected signal may pass through a set of signal splitters 122a-c, as needed, to supply each of the locations for the premises installation. The splitters 122a-c may contain passive circuits such as transformers and resistors or may also contain amplifiers in order to increase the signal level at the installation location.

At each installation location in the premises 120, the selected signal is provided to a standalone terminal 130 or to a combination settop box 140a-c and display device 150a-c. The terminal 130 and settop box 140a-c operate in a similar manner. Each of them receive the selected signal, tune to the desired physical channel within the selected signal, demodulate the physical channel to produce a transport stream, and extract the desired bit stream(s) from the transport stream. The terminal 130 may be used for local storage of various bit streams or for distribution of these bitstreams over a different network such as a

wireless network or an Ethernet connection. The settop box 140a-c converts the desired bitstream(s) into video and audio signals for display on the display device 150a-c.

The terminal 130 and settop boxes 140a-c may provide one or more control signals back onto the cable to the re-synthesizer 110. The control signal is generated based on inputs provided, for instance by a customer. The control signal sent to re-synthesizer 110 contains information necessary to perform the preselection and processing of frequency ranges, physical channels, and program streams from each of the L-band signals. The communication protocol to the re-synthesizer 110 may be done in a manner suitable for delivery as is known in the art, such as frequency shift keying FSK protocol. The control signal may alternately be supplied through a wireless link. Electrical power may also be passed through the coaxial cable to the re-synthesizer 110 and further on to the satellite dishes 104a-c.

As described earlier, a conventional re-synthesizer, sometimes known as a frequency translation module, contains analog signal processing used for the filtering, mixing, and recombining of the L-band signals. Analog signal processing contains limitations when operating at high frequencies in the 1GHz range, and the complexity of the analog signal processing increases significantly with an increase of the number of selected physical channels. The utilization of digital signal processing within the re-synthesizer structure permits greater flexibility and removes some of the limitations of analog signal processing. The digital processing further permits recovery and processing of the program streams permitting additional flexibility and efficiency.

Turning now to FIG. 2 a block diagram 200 of an embodiment of the present invention is shown. The diagram shows an implementation of the re-synsthesizer 110 that includes digital signal processing in order to increase the performance and available bandwidth for selected channels. In order to facilitate a further understanding of the invention, a

re-synthesizer 110 will be described here using only a single L-band signal as an input. Further, the re-synthesizer 110 described here will include the capabilities only to translate frequency ranges or physical channels from the input to the output. The single L-band signal, as an analog input, is processed through an RF processing block 210. The RF processing block 210 may contain circuitry for filtering undesired energy outside the signal frequency range, may correct for any frequency response errors introduced, and may amplify the signal to a level necessary for input to the analog to digital (A/D) converter 220. The input RF processing block 210 may also contain any mixing circuits necessary to position the L-band signal in the correct frequency range for operation of the A/D converter 220.

The A/D converter 220 digitizes the processed L-band signal into a series of samples, each sample containing a group of bits. In an exemplary embodiment, the processed satellite signal is located between the frequencies of 975 and 1425 MHz. The A/D converter 220 samples the processed L-band signal at a rate of 933 megasamples per second (MSPS) generating a digital signal containing a series of samples, each sample represented by 8 bits. The A/D converter 220 may also generate a translated frequency image of the L-band signal essentially translating the signal from an initial frequency range in the analog domain to a different frequency range based on sampling principles. A clock signal, not shown, is supplied to the A/D converter for performing the sampling. The clock signal may be generated by a crystal or as part of a voltage controlled oscillator. The clock signal may also directly, or through additional multipliers and dividers, supply signals to other blocks within the re-synthesizer 110.

The digital channel selector 230 receives the sampled signal and proceeds to select and down-convert each of the individual physical channels that have been selected. After processing, each of the selected individual channels are located within the same frequency

range at or near to baseband, but are contained as individual signals on separate signal lines. The number of bits representing each selected individual channel may be different from the original sampled signal based on the processing method employed. The use of digital signal processing and processing of the signal in parallel permits narrower filtering constraints and more efficient channel selection within the re-synthesizer 110.

Each of the individual selected channels is provided to the digital channel re-combiner 240. The digital channel re-combiner 240 frequency translates the individual selected channels each to a different and separate frequency range and combines these signals together to form a single selected digital signal. The selected digital signal is supplied to a digital to analog (D/A) converter 250. The D/A converter 250 converts the selected digital signal to a selected analog signal. In a preferred embodiment, the selected digital signal provided to the D/A converter 250 is a series of 10 bit samples at a rate of 950 MSPS. The D/A converter 250 outputs a selected analog signal within a frequency range of DC to 475 MHz.

The selected analog signal is passed to the RF processing block 260. The RF processing block 260 provides any analog signal processing necessary to properly send the selected analog signal on the coaxial cable to the customer home. The RF processing block 260 may contain circuitry for filtering undesired signal energy outside the signal frequency range, such as the images produced by the sampling process in D/A converter 250. The RF processing block 260 may also correct for any other frequency response errors introduced, and may amplify the signal as necessary to provide the signal onto a coaxial cable. The RF processing block 260 may also contain a mixing circuit necessary to position the selected analog signal in the correct L-band frequency range, for instance 975 - 1425 MHz.

Some additional circuitry may also be included such as for controlling the blocks, receiving and processing user inputs, and additional signal processing, although this circuitry is not shown here.

Turning now to FIG. 3, an illustrative block diagram of a circuit 300 of an embodiment of a portion of the present invention is shown. Circuit 300 represents circuitry contained with the digital channel converter block 230. A sampled signal, converted from an L-band signal by A/D converter 220, is provided to the sample demultiplexer 310. Sample demultiplexer 310 resamples at a demultiplexer sampling rate, F_F, (or post-decimation sampling rate) to provide a number of decimated sample streams in parallel.

Each of the decimated sample streams represents a sampled and time shifted version of the original signal with each of the folded spectra, from the decimation, aliased into the same decimated frequency space. The number of decimated sample streams, N, may be integrally related to the number of virtual channels in the original signal. In a preferred embodiment, the number of physical channels is sixteen. Further, the sample demulitplexer 310 sampling rate is preferably two times the data rate of one of the physical channels, or $F_F = 2F_S$ where F_s is the data rate of the physical channel. Each of the decimated sample streams passes through a sampling interface block 320. The sampling interface block 320 provides any sampling domain adjustments necessary in moving the signal from the A/D converter 220 and sample demulitplexer 310 to the filter bank 330a-N, connected to the sampling interface block 320. The filter bank 330a-N may provide a number of process steps including filtering the physical channels that are distributed within the decimated sample streams prior to the physical channels being separated. The filtering provides rejection of any energy not within a physical channel while generating a reconstructive set of base signals for selecting out the physical channels in further downstream processing. The filter bank 330a-N may also provide a time realignment of each of

the decimated sample streams. In a preferred embodiment, the filter bank 330a-N consists of a bank of bifurcated filters that collectively generate a filtered signal vector. Since all the bifurcated filters have a similar structure, only one bifurcated filter is described in detail herein.

A bifurcated filter may typically consist of two parallel branches of coefficient multiply and delay operations with the operations in each of the branches separately summed together. Each branch is designated as either an even output signal or an odd output signal. The number of multiply and delay operations in each branch may vary based on design criteria. For instance, sixteen weighted multiply and a number of coefficient multipliers may be used in each bifurcated filter. The delay element is controlled by a decimated sample clock signal, not shown, at a frequency F_f. The summing node separately adds together those values from each of the odd weighted multipliers and even weighted multipliers to form the odd and even output signal. The orientation of the filter branches and operations within the branches allows special properties to exist. These properties include amplitude inversion of the signal or time reversing the signal within the branch. As noted, other filter structures may be used, as known to those skilled in the art, in conjunction with the various techniques of simultaneous channel reception techniques.

The output signal, a filter signal vector containing 2N signal streams, from the filter bank 330a-N connects to a bank of summing nodes 340a-N. Referring to the preferred embodiment, the even and odd outputs from each of the different bifurcated filters may be combined in a cross-coupling pattern. The even output of filter 0 is summed with the odd output of filter N-1, even output of filter 1 with the odd output of filter N-2, and so on as shown. The summing nodes 340a-N generate a set of filtered sample streams.

The filtered sample streams at the output of summing nodes 340a-N connect to a distributor block 350. The main purpose of the distributor

block 350 is to process the filtered sample streams generated by the filter block 330a-N and summing nodes 340a-N to reconstruct the set of physical channels, originally provided in the L-band signal, from the decimated and filtered sample streams. The processing may include recombining the streams in a manner using mathematical operations. In a preferred embodiment the distributor block 350 uses a type IV Discrete Cosine Transform (DCT) for processing the filtered sample streams. The bifurcated filter structure described previously further permits a small DCT structure in implementation by making use of the inversion and time reversal properties of the filter. The bifurcated filter structure may also permit use of a DCT employing a sparse matrix decomposition structure.

The combination of the filter bank 330a-N, summing node 340a-N, and distributor 350 results in generating a set of output streams, each representing the separated data content from a physical channel. The set of individual physical channels from the distributor 350 are generated from the set of decimated sample streams where each stream contains content from each of the physical channels in a sample aliased condition. It should be noted that other methods may be employed for accomplishing recovery of separate physical channels simultaneously from a single signal.

The output of distributor block 350 represents N individual physical channels positioned at or near to baseband frequency. Each physical channel, in digital signal form, may be located on a separate signal line at the output of distributor block 350. Each of the separate signal lines connect to a channel selector block 360. The channel selector block 360 may select a set of physical channels from the original N input channels provided. Any number of channels up to the full number N may be selected. For instance, four channels may be selected. The number of channels permitted for selection in channel selector block 360 is a design choice, and the full number of permitted channels for selection does not have to be selected at any one time. Additionally, any further

physical channel separation may be performed, such as removing any aliasing components present due to the complex form of the signal as a result of the previously described processing.

The channel selector block 360 receives inputs from a controller 370 regarding which, if any, of the originally received physical channels is currently requested by the customer. The controller 370 may connect to the sample demultiplexer 310, interface 320, filter bank 330a-N, and distributor 350 in addition to connecting to channel selector 360. The controller 370 may also provide an interface for user inputs or a communications input in order to receive and convey the user requested channel information from multiple locations. As described previously, the user inputs may be supplied through the signal cable or through some other communications means. Also, as described previously, a home or customer premises may supply more than one customer input. In addition, controller 370 may provide additional functions for operation of the demultiplexer 310, interface 320, filter bank 330a-N, and assembler 350, such as clock functions, as necessary. The controller 370 may also be embodied as a portion of a larger controller function responsible for controlling and managing, for instance, the entire FTM device.

Turning now to FIG. 4, a block diagram 400 of a further embodiment of the present invention is shown. FIG. 4 illustrates an implementation of the digital channel re-combiner 240. The M outputs, representing a set of selected physical channels, of channel selector 360 are provided to the assembler 410. As described previously, the M outputs of the channel selector 360 may be equal to or less than the N physical channels present in the original L-band signal. In a preferred embodiment, the assembler 410 may receive up to N inputs. If the number of signals provided from channel selector 360 is less than N, the remaining inputs of channel assembler 410 are placed in a condition of "null" or no input. Additionally, the assembler 410 may also provide the ability to re-order the M input signals. For instance, if the M signals

provided to the assembler 410 are physical channels in positions 1, 2, 3, and 4 from selection of the original N channels, the assembler 410 may re-position the M signals by addressing them as inputs 1, 5, 9, and N-1. In this manner, further processing, including internal or external filtering may be simplified. Also, the re-positioning permits re-spacing of the M signals.

The assembler 410 provides processing for converting the selected channels into a set of signals forming a base set of parallel data streams that can then be filtered prior to remultiplexing and converting to an analog signal. The channel re-combiner 410 provides N outputs as a set of converted sample streams to inverse filter bank 420a-N. The inverse filter bank 420a-N provides filtering and/or time delay operations necessary to permit signal remultiplexing. The output of the inverse filter bank 420a-N provides a set of inverse filtered sample streams.

The inverse filtered sample streams at the output of the inverse filter bank 420a-N are provided to the sample multiplexer 430. The sample multiplexer 430 re-combines the samples, in a time multiplexing fashion, into a single sample stream. The sampling rate of the new single sample stream is preferably $2NF_s$ (F_s is the data rate of one channel). Clock signals representing both the input parallel sample stream rate and the new sampling rate at the output of the sample multiplexer 430 are also provided.

In a preferred embodiment, the assembler 410 is realized as an inverse type IV DCT, and the filter bank 420a-N is realized as an effective inverse bifurcated filter bank with respect to filter bank 330a-N as previously described. In this and other possible approaches, advantages exist due to the sparse matrix factorization stages containing a defined sparse inverse as well as the complementary form of the filtering stages. For example, the Type IV DCT is its own inverse i.e., $(\text{DCT IV})^2=I$ (identity matrix), and the bifurcated filters work with the transform elements to shape the bands of independent physical

channels. Also, the inverse filter bank 420a-N, shown as a bifurcated filter structure has a signal splitting at its input for providing a cross coupling of signals to the even and odd branches of the individual filters. After each branch in the individual filters has completed processing, the even and odd branches of each individual filter are summed together to form the individual output signal.

Alternatively, since the type IV DCT function in both the distributor 350 and assembler 410 may be the same, only one block for both operations may be used. For example, a single block in conjunction with a signal multiplexer (not shown) may provide either a signal representing the set of individual physical channels or the base set of parallel data streams in alternating operations.

A controller 470 may connect to the assembler 410, filter bank 420a-N, and sample multiplexer 430. The controller 470 may control the final selection process and ordering of selected physical channels in assembler 410. The controller 470 may follow a pre-programmed allocation and ordering algorithm, or may process user inputs to determine the allocation and ordering. The controller 470 may also provide an interface for user inputs or a communications input in order to receive and convey the user requested channel information from multiple locations. As described earlier, a home or customer premises may supply more than one customer input. In addition, controller 470 may provide additional functions for operation of the assembler 410, filter bank 420a-N, and multiplexer 430 such as clock functions, as necessary. The controller 470 may also be embodied as a portion of a larger controller function responsible for controlling and managing, for instance, the entire re-synthesizer device.

Additionally, if the M signals at the input to the assembler 410 are less than the N original channels, the channel re-combiner may also change the overall sampling rate. The assembler 410 may be reconfigured to process the M signals in an M point transform, producing

M parallel data streams. The filter bank may subsequently contain only M branches and the sample multiplexer process only M inputs. The clocks, supplied to the D/A converter as well as other blocks with diagram 400 may also be a scaled version of the clock used for digital channel selector 230. For instance, if M is one half the number N, then the clock signal for the digital channel re-combiner 240 may be one half the frequency of the clock signal for the digital channel selector 230. Note that the clock signal supplied to the other blocks working on parallel data streams may remain unaffected.

Further, the choice of value of M may be chosen for instance to permit a maximum of allowable channels at any time. However, in actual operation, a number less than M channels may actually be in use.

Turning now to FIG. 5, a block diagram 500 of a further embodiment of the present invention is shown. The diagram shows an implementation of the re-synthesizer 110 that includes digital signal processing and further includes program stream processing in order to increase the performance and available bandwidth for selected channels. In order to facilitate a further understanding of the invention, a re-synthesizer 110 will be described here using only a single L-band signal as an input. An input RF processing block 502 is connected to an A/D converter 504. The output of the A/D converter is connected to a digital channel selector 510. The outputs of the digital channel selector 510 each individually connect to a digital demodulator (demod) 520a-M. Each digital demod 520a-M connects to a transport demultiplexer (demux) 530a-M. The outputs of each transport demux 530a-M connect to a stream insert and extract block 540. The outputs of the stream insert and extract block connect to a set of transport remultiplexer (remux) blocks 560a-N. Each transport remux 560a-N connects to a digital modulator 570a-N. The outputs of the digital modulators 570a-N connect into a digital channel re-combiner 580. The output of the digital channel re-combiner 580 connects into a D/A converter 592. The output

of the D/A converter 593 connects into an output RF processing block 594. A controller 550 also connects to all of the other blocks including the stream insert and extract block 540.

The operation of blocks identified as input RF processing block 502, A/D converter 504, digital channel selector 510, digital channel re-combiner 580, D/A converter 592, and output RF processing block 594 are similar in operation to blocks having the same name described previously. Except as noted, these blocks will not be further described.

The digital channel selector 510 provides a set of selected channels to the digital demods 520a-M. The digital demods 520a-M contain digital signal processing for the demodulation, transmission equalization, and error correction of the selected channels according to the required transmission standard prescribed for the selected channel. In a preferred embodiment, digital demods 520a-M include processing necessary to demodulate and decode transport streams sent in either Motion Picture Entertainment Group standard MPEG 2 or Joint Video Team (JVT) format using either a Quaternary Phase Shift Keying (QPSK) modulation format or 8-PSK modulation format. The digital demods 520a-N also perform error correction using either Viterbi, Reed Solomon, and/or Low Density Parity Check (LDPC) error correction techniques. Further details regarding the individual detailed operation of the digital demods 520a-M are well known by those skilled in the art.

Each of the digital demods 520a-M produces a transport stream representing one or more individual program streams multiplexed with additional identification data. As described previously, a transport stream contains one or more program streams usually in multiplexed and packetized form. A program stream may represent an audio or video signal or may represent data such as a program guide. Each transport stream is provided to one of the transport demuxes 530a-M. The transport demuxes 530a-M process the transport streams by first recovering and separating the identification data for the transport stream.

The transport demuxes 530a-N use the identification data or program identifiers (PIDs) to separate out the program stream data in the transport stream into packets for each of the individual program streams. The transport demuxes 530a-M assemble the packets into separate individual program streams. The output of the transport demuxes 530a-M may supply the individual program streams on separate signal lines as shown, or may alternately provide the program streams along with the PIDs over a communications bus. In addition, stream identifiers are provided. These stream identifiers may include the PIDs supplied originally or may include new identification information sent along with the program streams. The stream identifiers may be used in further processing including reassembling the program streams back into transport streams.

The individual program streams are provided to the stream insert and extract block 540. The stream insert and extract block 540 allows removal and insertion of individual program streams into the set of individual streams present. The stream insert and extract block 540 may be able to remove program streams that are not required at the output and insert new program streams in place of the removed program streams. The new program streams may, for instance, represent content not present in the original signal. In a preferred embodiment, the new program stream represents local advertising and news content inserted in place of content in the original signal. The stream insert and extract block 540 may also be able to remove or introduce more than one stream at a time, and may include the ability to remove or introduce segments of program streams based on, for instance, time stamp identifiers present with the PIDs or stream identifiers.

The removal and insertion operations do not need to be matched and removed program streams are not required to be replaced in complete fashion by the insertion of new streams. However, the addition of new streams may not be possible without removing existing program

streams. The new program streams may utilize the stream identifier information such as the PIDs from the removed program streams. Additionally, the PID information may be modified in order to facilitate new program guide data while the stream identifier may remain the same, in order to allow the new program stream to be processed correctly downstream.

The stream insert and extract block 540 is controlled by controller 550. The controller 550 provides the signal management for the stream insert and extract block 540 as well as providing a signal path for removing and introducing the program streams. In addition, the controller 550 provides connections to external circuitry (not shown) for supplying the removed program streams to other devices, or for inputting the new program streams from other devices. The controller 550 also manages inputs provided by users either directly or remotely. The controller 550 provides management of the program stream identifiers during the insertion and extraction used in processing the program streams. The controller 550 may also include the ability to generate and supply new program identification information including new program guide data for identifying the new program streams.

The output of the insert and extract block 540 contains groups of program streams that are provided to the transport remuxes 560a-N. The transport remuxes 560a-N process the groups of program streams, using the stream identifiers, and multiplex the streams back into remuxed transport streams. These remixed transport streams include any new program streams that were added replacing the removed program streams processed in the stream insert and extract block 540. In a preferred embodiment, streams containing the stream identifiers originally grouped in transport streams at the output of digital demods 520a-M are remulitplexed together in each of the transport remuxes 560a-N. As with the program streams at the output of the transport muxes 530a-M, the output of the insert and extract block 540 may supply

the individual program streams on separate signal lines, as shown, or may alternately provide the program streams along with the stream identifiers over a communications bus. The transport remuxes 560a-N process the individual program streams along with the stream identifiers to form a single packetized and multiplexed transport data stream containing identification data and program stream information.

Each output of the transport remuxes 560a-N is supplied to digital modulators 570a-N. In the digital modulators 570a-N, the transport streams are transformed into digital communications signals. The digital modulators 570a-N typically provide error correction processing to incorporate error correction into the signal. Additionally the digital modulators 570a-N include data to symbol mapping for creating a particular modulation signal format. In a preferred embodiment, digital modulators 570a-N include processing necessary to code and modulate transport streams for sending in either Motion Picture Entertainment Group standard (MPEG 2) or Joint Video Team (JVT) format using either a Quaternary Phase Shift Keying (QPSK) modulation format or an 8-PSK modulation format. The digital modulators 570a-N also generate and insert error correction information using either Viterbi, Reed Solomon, and/or Low Density Parity Check (LDPC) error correction techniques. Further details regarding the individual detailed operation of the digital modulators 570a-N are well known by those skilled in the art.

It is important to note that the digital modulation format provided by the digital modulators 570a-N may be the same as the format used in processing the signals in the digital demods 520a-M. However, the modulators 570a-N may provide output signals in an alternate format, including formats such as 64 point Quadrature Amplitude Modulation (64QAM). It is important to note that the format chosen in modulator 570a-N may most likely match a format that can be processed in the downstream customer equipment including settop boxes.

Turning now to FIG. 6, a block diagram 600 of another embodiment of the present invention is shown. FIG. 6 illustrates a three L-band signal input re-synthesizer utilizing the inventive concept described herein. Each L-band input signal is processed through RF input processing, not shown.

The processed L-band input signals are connected to A/D converters 604a-c. The outputs of the A/D converters 604a-c are connected to digital channel selectors 610a-c. The outputs of the digital channel selectors 610a-c each individually connect to groups of digital demods 620a1-aM, 620b1-bM, and 620c1-cM. Each of the digital demods 620a1-aM, 620b1-bM, and 620c1-cM connects to groups of transport demuxes 630a1-aM, 630b1-bM, and 630c1-cM. The one or more outputs of each of the transport demuxes 630a1-aM, 630b1-bM, and 630c1-cM connects to a transport stream cross-multiplexer 640. The outputs of the transport stream cross-multiplexer 640 connect to a set of digital modulators 670a-N. The outputs of the digital modulators 670a-N connect into a digital channel re-combiner 680. The output of the digital channel re-combiner 680 connects into a D/A converter 692. The output of the D/A converter 692 may connect to further RF processing (not shown) prior to providing an output for transmitting on a coaxial cable. A controller 650 also connects to all of the other blocks including the transport stream cross-multiplexer 640.

The operation of blocks identified as A/D converters 604a-c, digital channel selectors 610a-c, digital demods 620a1-aM, 620b1-bM, and 620c1-cM, transport de-muxes 630a1-aM, 630b1-bM, and 630c1-cM, digital modulators 670a-N, digital channel re-combiner 680, and D/A converter 692 are similar in operation to blocks having the same name and described previously. Except as noted, these blocks will not be further described.

Each digital channel selector 610a-c is capable of producing M outputs representing M physical channels where M is less than or equal

to the N original physical channels from an L-band signal. Each L-band signal may provide a different number of physical channels for eventual use in the final output signal as was described previously.

Each of the selected channels from digital channel selectors 610a-c is then further demodulated in the digital demod blocks 620a1-aM, 620b1-bM, and 620c1-cM. The output transport streams are then processed in the transport demuxes 630a1-aM, 630b1-bM, and 630c1-cM. Each transport demux 630a1-aM, 630b1-bM, and 630c1-cM. produce one or more individual program streams along with stream identifiers as described previously. The stream identification will permit further processing including the reassembling into a new transport stream described below.

The individual programs streams, along with the stream identifiers, are provided to the transport stream cross-multiplexer 640. The transport stream cross-multiplexer 640 allows programs streams from different transport originally streams to be combined or multiplexed together to form new transport streams. The transport stream cross-multiplexer 640 further selects and groups the selected program streams for processing to form transport streams. Each group of selected program streams, along with the stream identifiers is packetized and further multiplexed together to form new transport streams. For example, program streams one and two are requested from a particular channel delivered as a multiplex of channels from a first satellite but not a program stream three. Also, program stream one is requested from a particular channel delivered as a multiplex of channels from a second satellite, but not program streams two, three, and four. The transport stream cross-multiplexer 640 may assign program stream one from the second satellite channel as program stream three of the first satellite channel and also make the necessary stream identification changes. The transport stream cross-multiplexer 640 may then remultiplex the three program streams to create a new transport stream.

The selected program streams and stream identifiers are re-multiplexed or packaged to permit more efficient delivery of the selected program content by the user. The number of new transport streams, N, may be different from the number of transport streams that were supplied to the transport stream cross-multiplexer 640. The number of transport streams used is a matter of design choice, but may not exceed the number of available channels in the final output signal. Further, as described previously, the order of the transport streams may be changed by the transport stream cross-multiplexer 640 from the order of the transport streams provided by the digital demods 620a1-aM, 620b1-bM, and 620c1-cM.

The transport stream cross-multiplexer 640 is controlled by controller 650. The controller 650 provides the signal management for the transport stream cross-multiplexer 640 such as managing the packetization and time stamp indicators provided as part of the stream identification. The controller also provides new stream identification information, for instance, in the form of new PIDs. The new identification information is used in the formation of the new transport streams in the transport stream cross-mulitplexer 640. The controller 670 also manages inputs provided by users, provided either directly or remotely. The controller 670 may also include the ability to generate and supply new program identification information including new program guide data for identifying the program streams within the new transport streams.

Each of the new transport streams from the transport stream cross-multiplexer 640 is provided to the digital modulators 670a-N. As described previously, the digital modulators 650a-N modulate the transport streams using a particular encoding and modulation format to form modulated channels of information. Additionally, the format provided by the modulator may be the same as the format used in processing the signals in the digital demods 620a1-aM, 620b1-bM, 620c1-cM. However, the modulator may provide the output signals in an

alternate format, including formats such as 64 QAM. It is important to note that the format chosen in the modulator should match a format that can be processed the downstream customer equipment such as settop boxes or other network equipment.

Each of the modulated channels from the digital modulators 670a-N is provided to the digital channel re-combiner 680. The digital channel re-combiner 680 may process up to N channels in its assembler block as described above. The assembler in the digital channel re-combiner 680 may also includes switching and selection circuits to manage which of the M inputs originally provided from each of the digital channel selectors 530a-c are processed in the digital channel re-combiner 680. The management and switching function is controlled by the controller 650.

The digital channel re-combiner 680 may also contain signal processing such as digital signal level adjustment applied to each of the selected channels. Level adjustment may allow all selected channels to be delivered at approximately the same signal level improving the performance of the home equipment.

Block diagram 600 forms a multi-input, single output channel selection, translation, stream processing, and distribution device. The device produces an output of up to N channels in a single signal for delivery over a single coaxial cable, from an input containing up to three times N possible input channels presented in three separate signals. The selected channels are then digitally demodulated to the bit packet level and disassembled into program streams. The various program streams and their associated identifiers may then be re-combined into new physical channels, with new identifiers if needed, and digitally re-modulated into a single signal. The re-synthesizer would create a new cross-signal re-multiplexed RF output. The re-synthesizer allows collecting sets of programs to be simultaneously viewed on the same set of channels that is different and more efficiently presented to the user

than providing the original set of signals. Note, that the use of three inputs is illustrative, and a greater or fewer number of inputs containing a greater or fewer number of possible input channels may be used.

It is also possible that the functions described in the stream insert and extract block 540 and the transport stream cross-multiplexer 640 may be combined and used in the same re-synthesizer. For instance, in a multi-dwelling unit installation, the combined transport cross-multiplexer and stream insert and extract block may be used to provide a signal containing program streams arranged into new channels as requested by the various occupants of the dwelling units as well as provide local community events in a program stream provided to all occupants.

Turning now to FIG. 7, a flow chart 700 utilizing the present invention is shown. At step 702, one or more incoming satellite signals are received by a device, such as the re-synthesizer described in block diagram 600. Next at 704, the one or more incoming satellite signals are converted to digital signals. The conversion is preferably performed by A/D converters 604a-c, and may further include processing for separating the individual physical channels after the conversion such as described in digital channel selectors 610a-c. Next, at step 706, the desired physical channels are selected to form a group of selected frequency channels. The selected frequency channels may be outputs from digital channel selectors 610a-c. The selected frequency channels may be selected in digital channel selectors 610a-c based on requests by the customer's home equipment. The selection process may be managed by controller 650. The controller 650 may be responsible for receiving and managing multiple requests and providing the proper information to the digital channel selectors 610a-c.

Next, at step 708, the selected digital channels are demodulated. The demodulation may occur in digital demods 620a1-aM, 620b1-bM, and 620c1-cM. At step 710, the demodulated channels, now

represented as transport streams, are demultiplexed into individual program streams. The demultiplexing may take place in the transport demuxes 630a1-aM, 630b1-bM, and 630c1-cM. Next at step 712, the individual program streams are processed to form new transport streams. Step 712 may involve removing existing program streams and inserting new programs for use in the in the new transport streams such as described in the stream insert and extract block 540. Step 712 may also provide the ability to re-arrange and recombine the program streams to form new transport streams such as described in transport stream cross-multiplexer 640.

Next, at step 714, the new transport streams are modulated into new channels. The modulation may be accomplished in digital modulators 670a-N. The modulation format used in modulators 670a-N may be the same as the format the original L-band signals were provided in. However, the format may also be different and may instead match a format that can be processed by downstream equipment such as settop boxes.

Next, at step 716, the group of new channels is re-combined in a frequency diverse manner to form a signal occupying a range of frequencies and containing the channels at separate frequencies. The recombination may include a means for processing the group of selected digital channels such as described in digital channel re-combiner 680. At step 718, the recombined frequency diverse digital signal is converted back into an analog signal containing the selected channels at separate frequencies. The conversion may be performed in D/A converter 692. Finally, at step 720, the analog signal, representing the selected program streams from the selected channels is provided as an output supplied for transmission to other devices such as settop boxes and/or home network equipment.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of

example in the drawings and have been described in detail herein. The foregoing merely illustrates the principles of the invention and it will thus be appreciated that those skilled in the art will be able to devise numerous alternative arrangements which, although not explicitly described herein, embody the principles of the invention and are within its spirit and scope. For example, although illustrated in the context of separate functional elements, these functional elements may be embodied on one or more integrated circuits (ICs). Similarly, although shown as separate elements, any or all of the elements of may be implemented in hardware, software, or a combination of both. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the scope of the present invention as defined by the appended claims.

What is claimed is:

1. An apparatus (600) comprising:

a receiver (604a-c, 610a-c) for receiving a plurality of digitally multiplexed signals, each digitally multiplexed signal associated with a different physical transmission channel, and for simultaneously recovering from at least two of the digital multiplexes a plurality of bit streams; and

a transmitter (640, 670a-N, 680) for inserting the plurality of bit streams into different digital multiplexes and for modulating the different digital multiplexes for transmission on different transmission channels.

2. The apparatus (600) set forth in claim 1, wherein said receiver (604a-c, 610a-c) further comprises:

a sampler (604a-c) for sampling the signal to provide a plurality of decimated sample streams; and

a distributor (350) operatively connected to said sampler for processing said plurality of decimated sample streams to provide output signals representative of said one or more different physical channels.

3. The apparatus (600) of claim 2, wherein said distributor (350) includes a transform element.

4. The apparatus (600) of claim 2, wherein said sampler (604a-c) further comprises:

a demultiplexer (310) for demultiplexing the signal into said plurality of decimated sample streams; and

a plurality of filters (330a-N) connected to said demultiplexer (310) for processing said plurality of decimated sample streams.

5. The apparatus (600) of claim 2, wherein said receiver (604a-c, 610a-c) further comprises a selector (360) operatively connected to said

distributor (350) for selecting a subset of output signals representative of said one or more different physical channels.

6. The apparatus (600) of claim 2, wherein said receiver (604a-c, 610a-c) further comprises a demodulator (620a1-aM, 620b1-bM, 620c1-cM) operatively coupled to said selector (360) for processing said subset of output signals and generating said plurality of bit streams.

7. The apparatus (600) of claim 6, wherein said demodulator (620a1-aM, 620b1-bM, 620c1-cM) is a demodulator capable of demodulating signals from a satellite system.

8. The apparatus (600) of claim 1, wherein said transmitter (640, 670a-N, 680) further comprises:

a bit stream processor (640) for processing said plurality of bit streams into said new digital multiplexes; and

a modulator (670a-N) connected to said bit stream processor (640) for modulating said new digital multiplexes into a set of selected physical channels.

9. The apparatus (600) of claim 8, wherein said bit stream processor (640) includes a processor for inserting new bit streams into said new digital multiplexes not present in said plurality of digital multiplexes.

10. The apparatus (600) of claim 8, wherein said bit stream processor (640) includes a processor for re-arranging said bit streams between said plurality of digital multiplexes and said new digital multiplexes.

11. The apparatus (600) of claim 1, wherein said modulator (670a-N) is a modulator capable of modulating signals for reception by a satellite signal receiver.

12. The apparatus (600) of claim 1, wherein said transmitter (640, 670a-c, 680) further comprises:

an assembler (410) operative on said selected physical channels to provide a set of parallel data streams representing the combination of said selected physical channels; and

a converter (420a-N, 430) for converting said parallel data streams into said different physical transmission channels.

13. The apparatus (600) of claim 12, wherein said assembler (410) includes a transform element.

14. The apparatus (600) of claim 12, wherein said converter (420a-N, 430) further comprises:

a plurality of filters (420a-N) for processing said plurality of parallel data streams; and

a multiplexer (430) connected to said plurality of filters (420a-N) for multiplexing said plurality of parallel data streams into a single sample stream containing said different physical transmission channels.

15. The apparatus (600) of claim 1, wherein said different transmission channels are included in one signal.

16. The apparatus (600) of claim 1, wherein said plurality of digitally multiplexed signals are a plurality of transport streams.

17. The apparatus (600) of claim 1, wherein said plurality of bit streams include a plurality of program streams containing audio, video, or data information.

18. A method (700) for re-synthesizing signals comprising:

receiving (702) a first signal having a plurality of different program streams in different frequency channels;

selecting (706) a set of program streams from said plurality of different frequency channels;

combining (712) said set of program streams to form a second signal; and

transmitting (720) said second signal.

19. The method (700) of claim 18, wherein the step of selecting (706) further comprises:

decimating said first signal into a plurality of decimated sample streams;

performing a transform on said number of decimated sample streams to provide transform output signals.

20. The method (700) claim 19, wherein the step of decimating includes:

demultiplexing the signal into the number of decimated sample streams; and

processing the number of decimated sample streams with a plurality of filters for matching the discrete cosine transform.

21. The method (700) of claim 18, wherein the step of selecting (706) includes re-ordering said set of program streams.

22. The method (700) of claim 18, wherein the step of combining (712) further comprises:

performing transform-based processing on said set of different frequency channels to provide a plurality of parallel data streams; and

processing said plurality of parallel data streams to provide said second signal.

23. An integrated circuit (600) for use in a receiving system, which receives signals representing a plurality of channels, the integrated circuit comprising:

a demultiplexing element (310) for demultiplexing a received sampled signal to produce a plurality of first data streams;

a transform element (350, 410) for transforming said plurality of first data streams into a plurality of transform output signals, and for transforming at least two of said plurality of transform output signals into a plurality of second data streams;

a bit stream processing element (640) for processing said plurality of transform output signals to select a set of bit streams and to combine said selected bit streams into said at least two transform output signals; and

a multiplexing element (430) for mulitplexing said plurality of second data streams and outputting a sampled signal.

24. The integrated circuit (600) of claim 23, wherein said transform element (350, 410) uses a type IV discrete cosine transform.

25. The integrated circuit (600) of claim 23, further comprising:

a first filter element (330a-N) operative to filter said plurality of first data streams prior to providing said plurality of first data streams to said transform element (350, 410); and

a second filter element (420a-N) operative to filter said plurality of second data streams prior to providing said plurality of second data streams to said multiplexing element (430).

26. The integrated circuit (600) of claim 23, further comprising:

a demodulator element (620a1-aM, 620b1-bM, 620c1-cM) for demodulating said plurality of transform output signals prior to providing

said plurality of transform output signals to said bit stream processing element (640); and

a modulator element (670a-N) for modulating said at least two transform output signals prior to providing said least two transform output signals to said transform element (350, 410).

27. An apparatus (600) for re-synthesizing signals comprising:

means for receiving (604a) a first signal having a plurality of bit streams from different frequency channels;

means for translating (610a-c) said first signal into a set of signals representing said plurality of different frequency channels;

means for selecting (640) a set of bit streams from said set of signals;

means for combining (680) said set of bit streams to form a second signal; and

means for transmitting (692) said second signal.

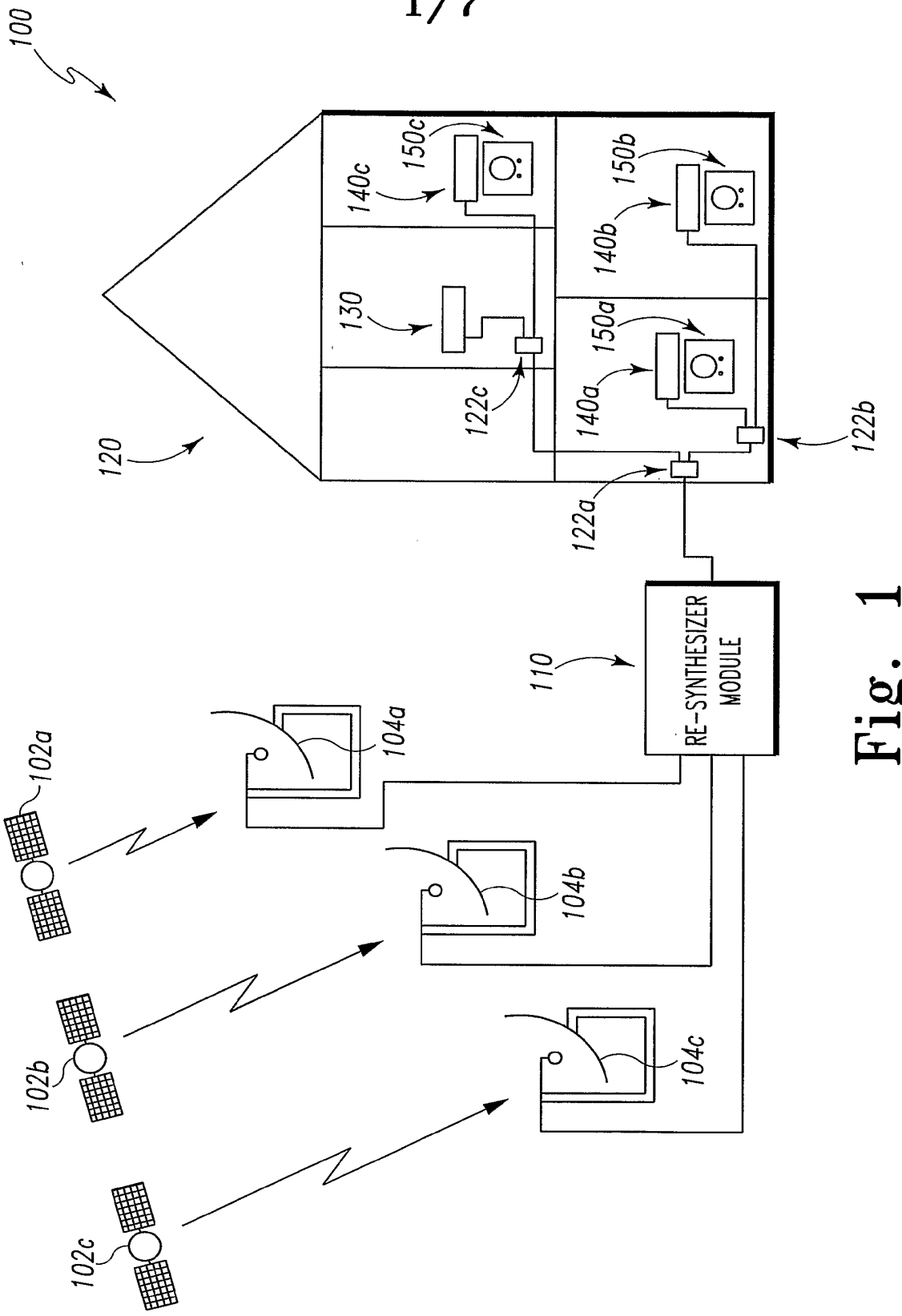

100
120
130
140c
150c
140b
150b
140a
150a
122c
122a
122b
110
RE-SYNTHESIZER MODULE
102a
102b
102c
104a
104b
104c

Fig. 1

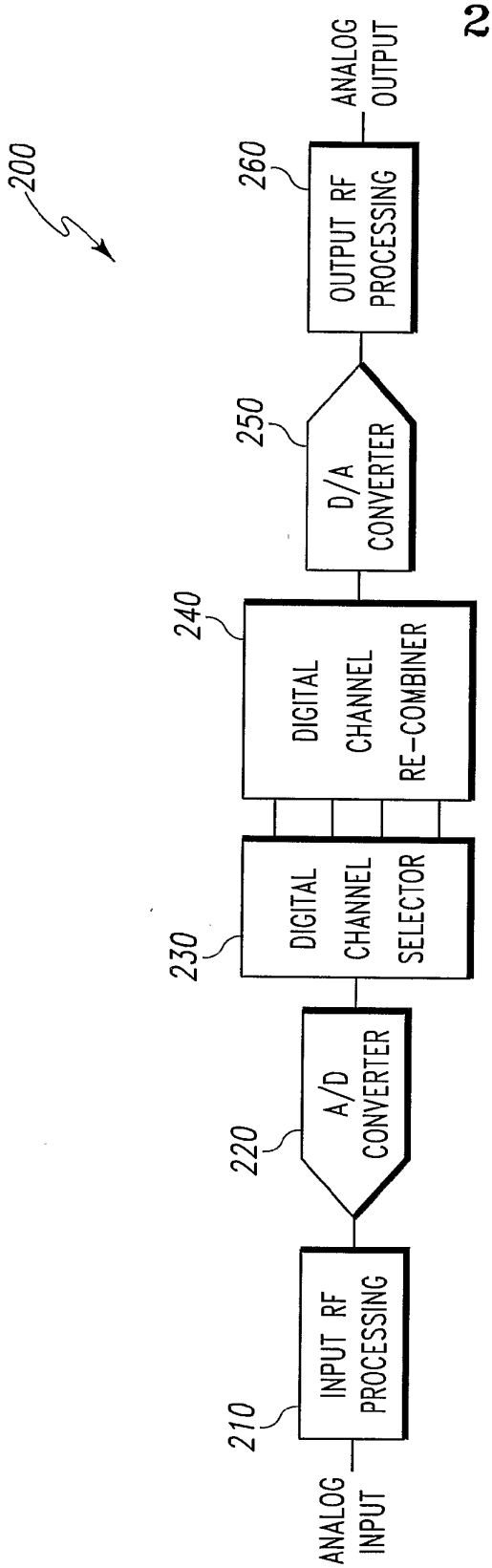

200
ANALOG INPUT
210
INPUT RF PROCESSING
220
A/D CONVERTER
230
DIGITAL CHANNEL SELECTOR
240
DIGITAL CHANNEL RE-COMBINER
250
D/A CONVERTER
260
OUTPUT RF PROCESSING
ANALOG OUTPUT

Fig. 2

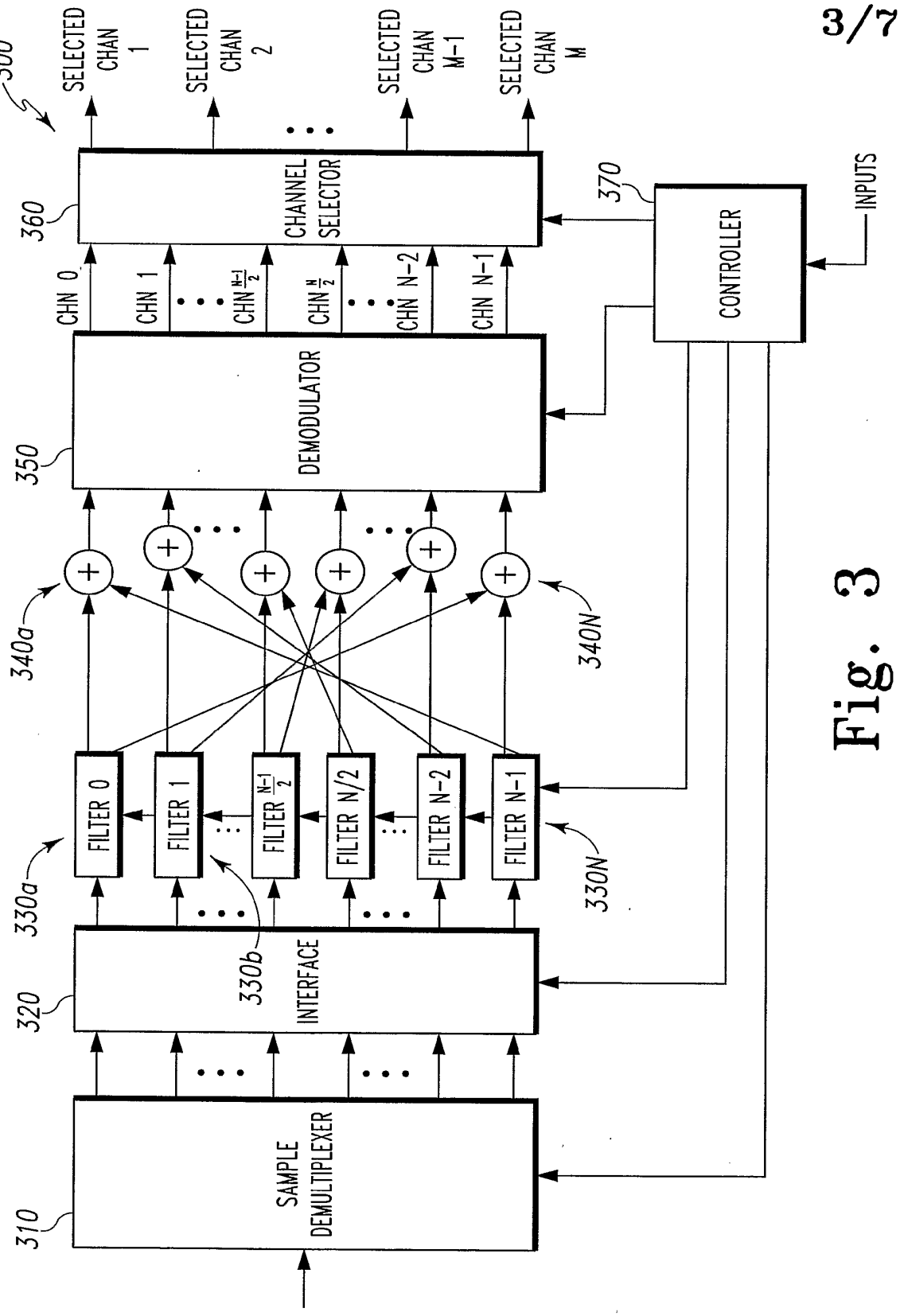

300
SELECTED CHAN 1
SELECTED CHAN 2
SELECTED CHAN M-1
SELECTED CHAN M
360
CHANNEL SELECTOR
370
CONTROLLER
INPUTS
CHN 0
CHN 1
CHN (N-1)/2
CHN N/2
CHN N-2
CHN N-1
350
DEMODULATOR
340a
340N
FILTER 0
FILTER 1
FILTER (N-1)/2
FILTER N/2
FILTER N-2
FILTER N-1
330a
330b
330N
320
INTERFACE
310
SAMPLE DEMULTIPLEXER

Fig. 3

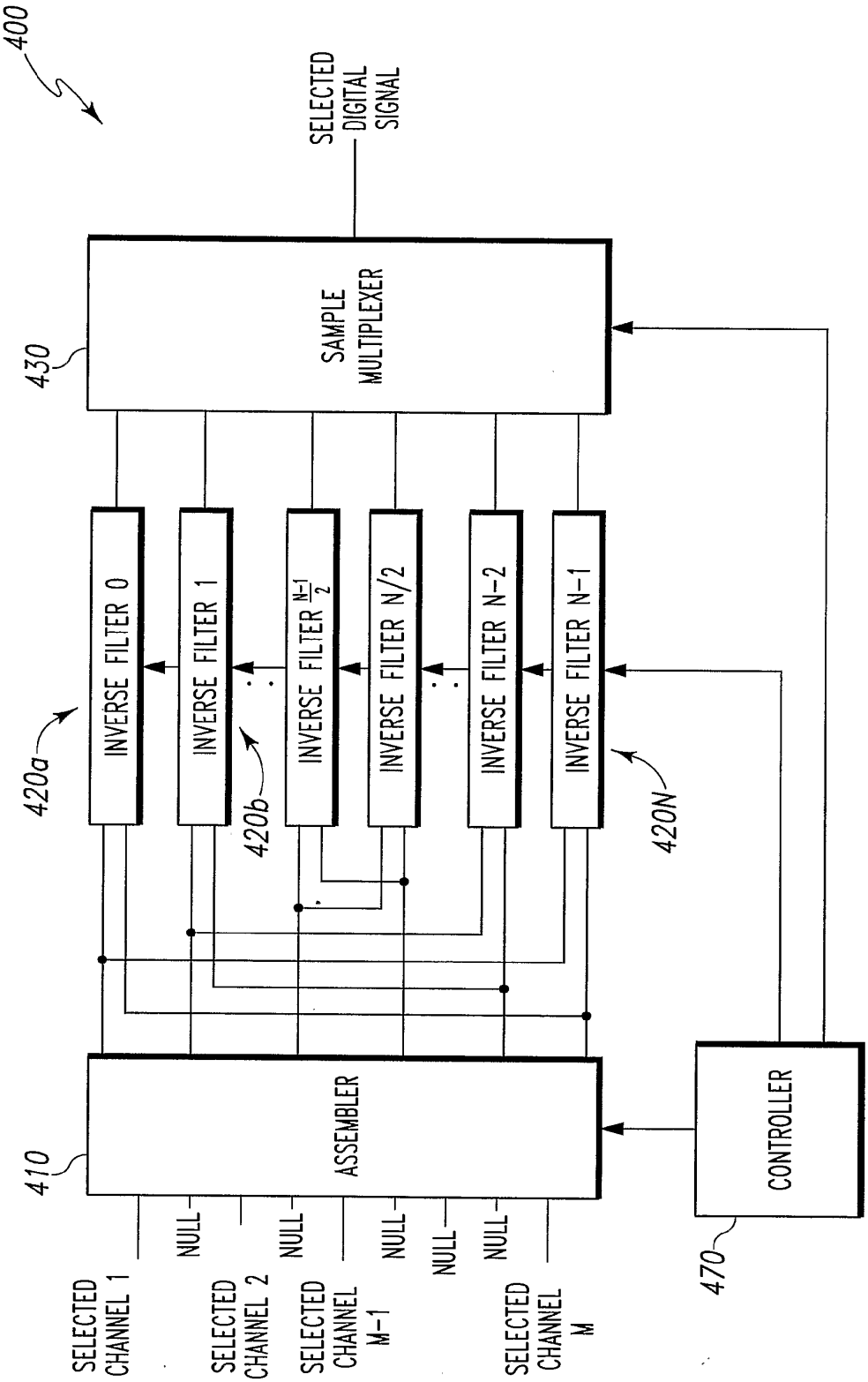

400
SELECTED DIGITAL SIGNAL
SAMPLE MULTIPLEXER
430
INVERSE FILTER 0
INVERSE FILTER 1
INVERSE FILTER $\frac{N-1}{2}$
INVERSE FILTER N/2
INVERSE FILTER N-2
INVERSE FILTER N-1
420a
420b
420N
ASSEMBLER
410
CONTROLLER
470
SELECTED CHANNEL 1
NULL
SELECTED CHANNEL 2
NULL
SELECTED CHANNEL M-1
NULL
NULL
SELECTED CHANNEL M

Fig. 4

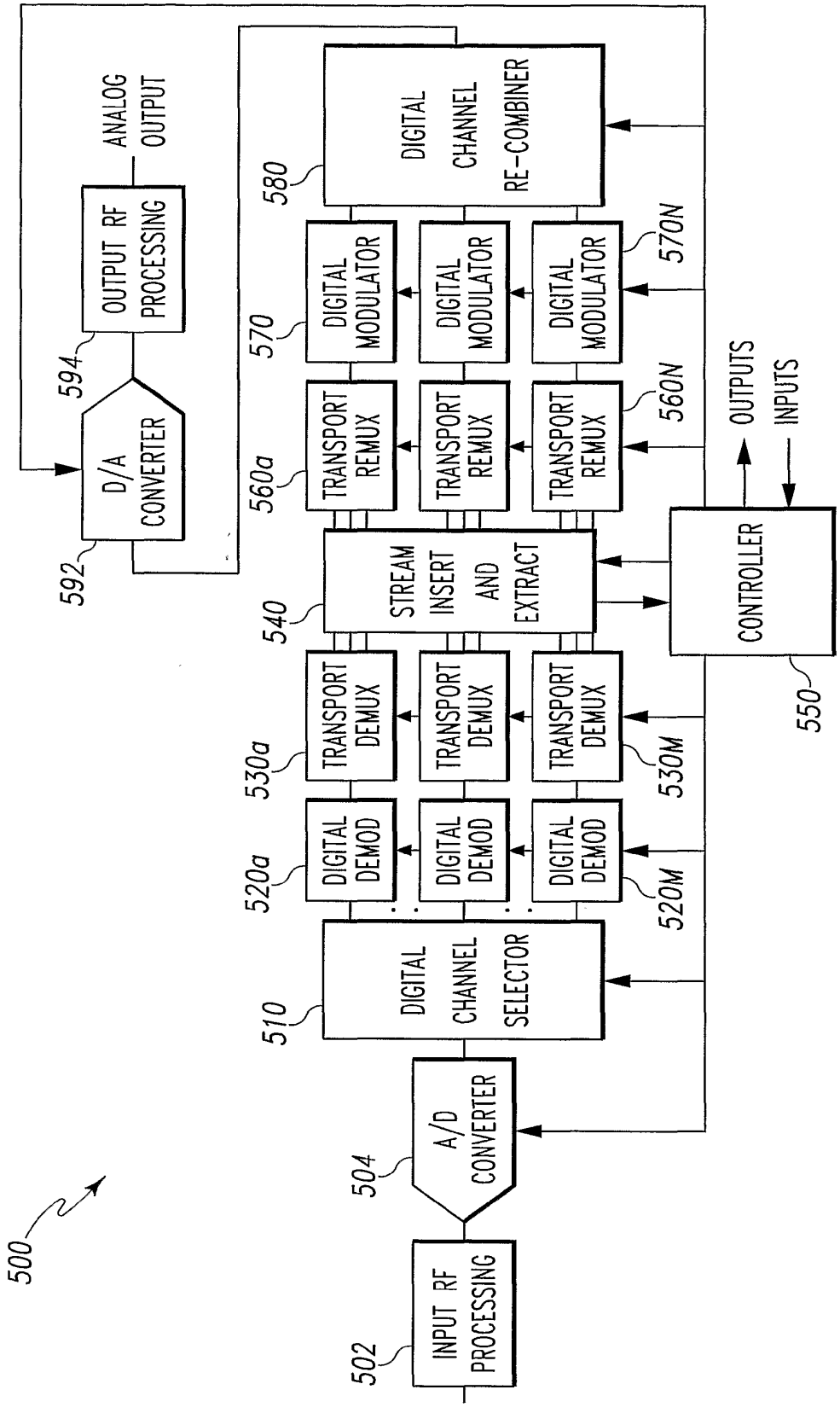

500
INPUT RF PROCESSING
502
A/D CONVERTER
504
DIGITAL CHANNEL SELECTOR
510
DIGITAL DEMOD
520a
DIGITAL DEMOD
520M
TRANSPORT DEMUX
530a
TRANSPORT DEMUX
530M
STREAM INSERT AND EXTRACT
540
TRANSPORT REMUX
560a
TRANSPORT REMUX
560N
DIGITAL MODULATOR
570
DIGITAL MODULATOR
570N
DIGITAL CHANNEL RE-COMBINER
580
D/A CONVERTER
592
OUTPUT RF PROCESSING
594
ANALOG OUTPUT
CONTROLLER
550
OUTPUTS
INPUTS

Fig. 5

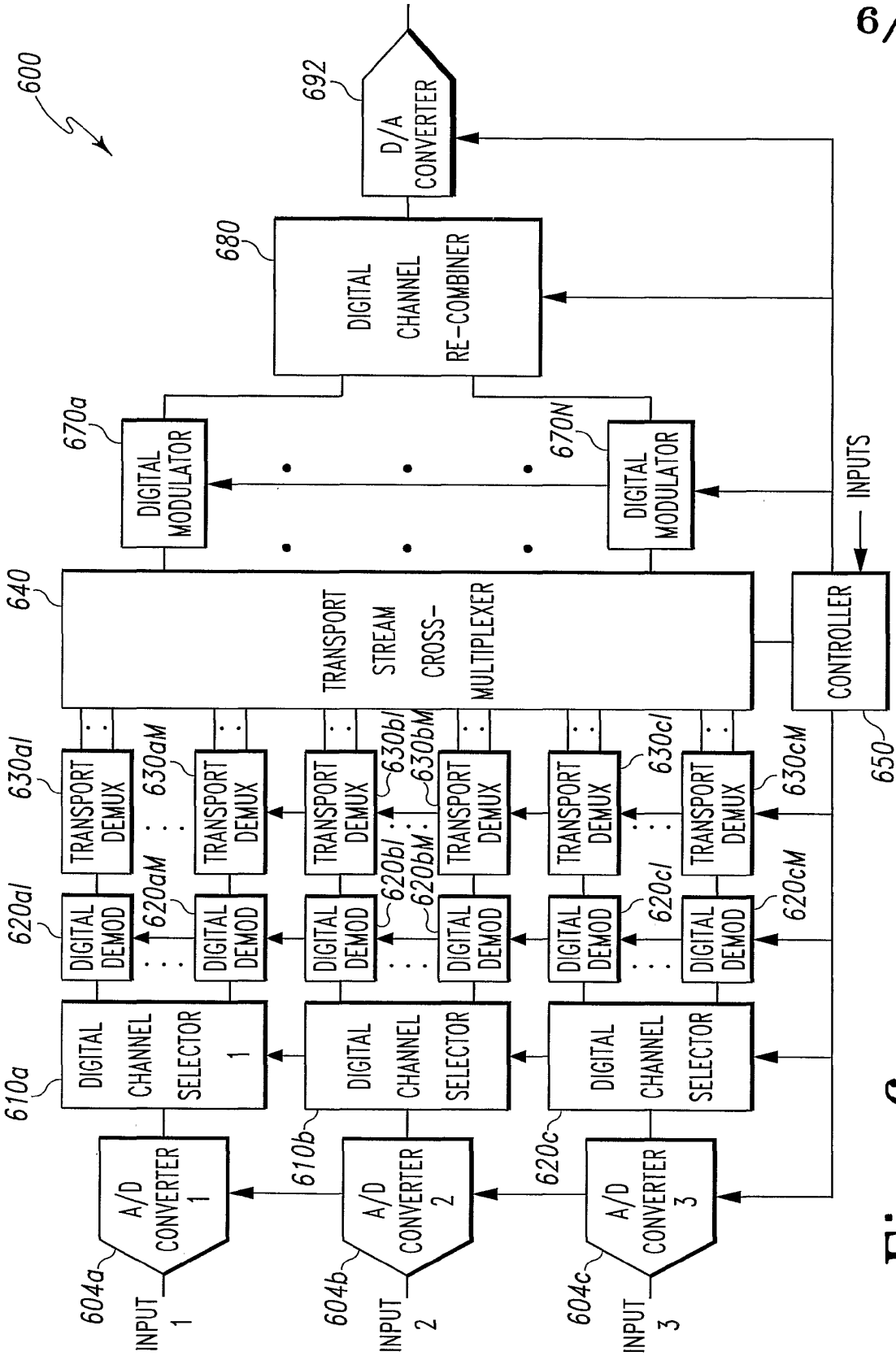

600
692
D/A CONVERTER
680
DIGITAL CHANNEL RE-COMBINER
670a
DIGITAL MODULATOR
670N
DIGITAL MODULATOR
INPUTS
640
TRANSPORT STREAM CROSS-MULTIPLEXER
CONTROLLER
650
630a1
630aM
630b1
630bM
630c1
630cM
TRANSPORT DEMUX
620a1
620aM
620b1
620bM
620c1
620cM
DIGITAL DEMOD
610a
610b
620c
DIGITAL CHANNEL SELECTOR 1
DIGITAL CHANNEL SELECTOR
604a
604b
604c
A/D CONVERTER 1
A/D CONVERTER 2
A/D CONVERTER 3
INPUT 1
INPUT 2
INPUT 3

Fig. 6

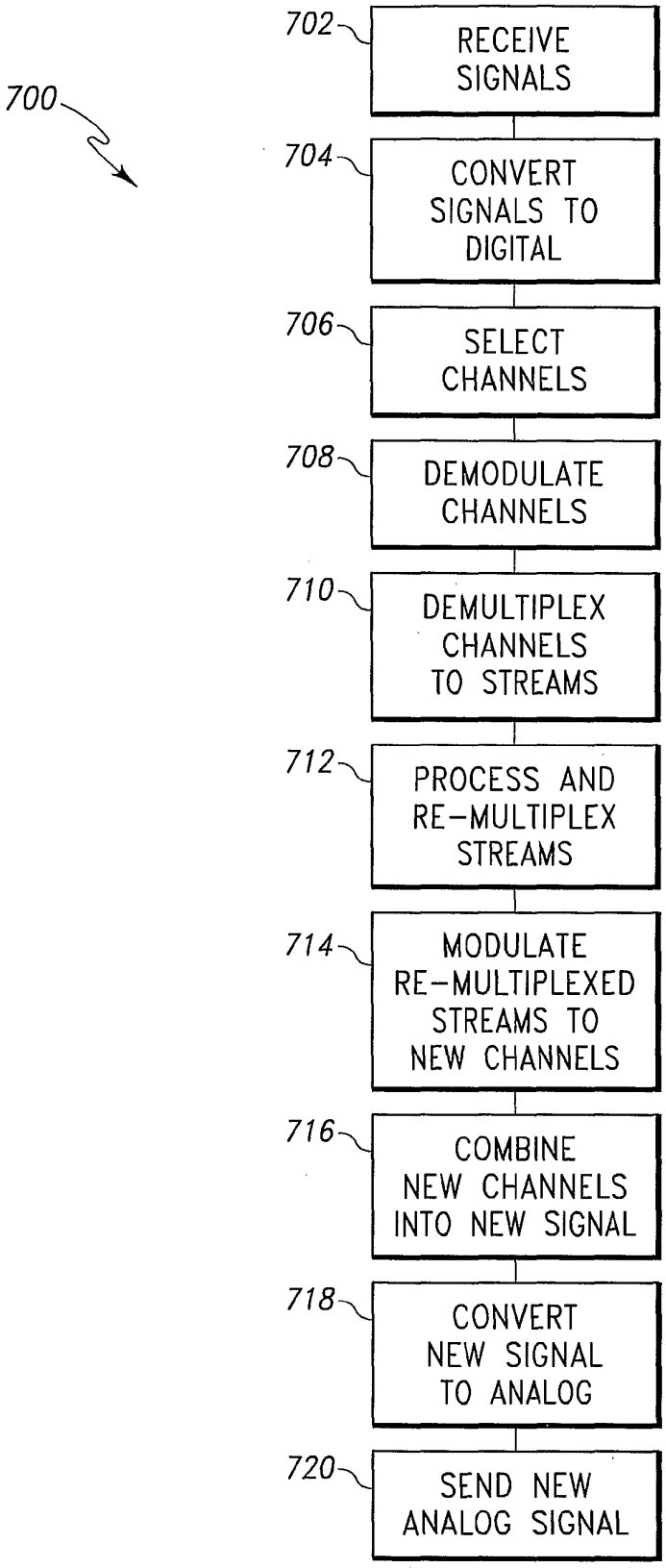

700
702
RECEIVE SIGNALS
704
CONVERT SIGNALS TO DIGITAL
706
SELECT CHANNELS
708
DEMODULATE CHANNELS
710
DEMULTIPLEX CHANNELS TO STREAMS
712
PROCESS AND RE-MULTIPLEX STREAMS
714
MODULATE RE-MULTIPLEXED STREAMS TO NEW CHANNELS
716
COMBINE NEW CHANNELS INTO NEW SIGNAL
718
CONVERT NEW SIGNAL TO ANALOG
720
SEND NEW ANALOG SIGNAL

Fig. 7

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A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter With Harmonic-Rejection Mixers

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***Abstract*—A highly integrated 1.75-GHz 0.35-μm CMOS transmitter is described. The I/Q modulator-based transmitter facilitates integration through the use of a unique mixer, termed a harmonic-rejection mixer, and a wide loop bandwidth phase-locked loop (PLL) for the RF synthesizer. The harmonic-rejection mixers are used to eliminate the need for a discrete IF filter and the use of a wide loop bandwidth PLL allowed for the complete integration of the synthesizers using low-Q components while achieving low phase noise. The entire transmit signal path from the digital-to-analog converters to the power amplifier, including two fully integrated frequency synthesizers, is integrated into a single-chip solution. The transmitter was tested with a testing buffer before the power amplifier (PA) and achieved less than 1.3° rms phase error when modulating a DCS-1800 GMSK signal. The prototype consumed 151 mA from a 3-V supply. A class-C PA, capable of driving 25 dBm off-chip, was included and the output was compared to the testing buffer with little change in the transmitter performance.**

***Index Terms*—Class-C power amplifier, CMOS RF, digital-to-analog converter, frequency synthesizer, harmonic-rejection mixer, harmonic-rejection transmitter, image-rejection mixer, low-pass filter, phase-locked loop, power amplifier, quadrature generation, radio architectures, radio transmitter, wireless communications.**

I. Introduction

THE DEMAND for wireless connectivity supporting both voice and data has dramatically increased in recent years. Advancements in wireless technology have largely been driven by the desire for lower cost solutions. One method of achieving this price reduction is through increased levels of integration in both the transmitter and the receiver. In addition to reducing the number of ICs needed, eliminating the need for costly discrete components can also lower the overall cost. Consequently, methods of integration have received considerable attention over the last few years [1], with the goal of complete integration of both the digital and analog circuits onto a single chip. CMOS is amenable to high integration due to the fact that the vast majority of digital integrated circuits as well as many analog integrated circuits [2] are implemented in CMOS technologies. However, maintaining high performance in a wireless system, with an integrated CMOS solution, requires advances at both the architectural and circuit level because many current implementations are not amenable to integration in CMOS.

Recently, significant effort has been directed toward the implementation of integrated CMOS receivers [3], [4]. The focus of this work is to demonstrate techniques that would allow for a highly integrated high-performance CMOS transmitter and eliminate the need for costly discrete components. The challenge was to maintain the high performance needed by cellular communications systems while using low-Q on-chip components inherent to standard CMOS. A prototype was fabricated using a 0.35-μm double-poly five-layer metal CMOS technology. The transmitter operated at 1.75 GHz and was designed for a narrow-band cellular standard, DCS-1800, an up-banded version of GSM. Although the prototype was only tested with one standard, the architecture was chosen to facilitate multistandard operation. The transmitter integrated the entire signal path from the digital-to-analog converters (DACs) to the power amplifier (PA) including two frequency synthesizers. The full integration of the transmitter was facilitated by a number of techniques including the harmonic-rejection mixer (HRM) and a wide-loop-bandwidth phase-locked loop (PLL).

Section II discusses relevant transmitter architectures and their potential for integration in CMOS and multistandard operation. Section III focuses on the harmonic-rejection transmitter in more detail while addressing a few of the key concepts and circuit blocks. Section IV examines the CMOS prototype transmitter used to demonstrate the previously discussed concepts, and Section V presents the measured results from this transmitter. Finally, some conclusions are made in Section VI.

II. Transmitter Architectures

Transmitter implementations to date have used a variety of architectures, each of which exhibits features making them well suited for implementing a specific standard. However, if the goal is multistandard operation, a transmitter architecture with high flexibility is desired. Furthermore, high performance is required if a difficult standard is among the targeted applications. In particular, RF systems with large cell sizes, such as cellular communication systems, generally require higher performance than short-range systems such as Bluetooth. The issue is further complicated by the fact that CMOS integration using low-Q components limits the performance of many circuit techniques. As

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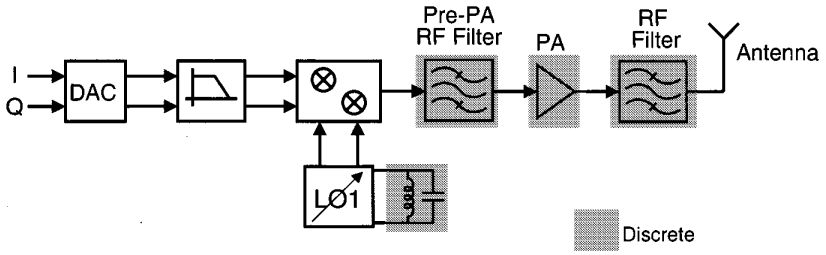


Fig. 1. Direct upconversion transmitter block diagram.

a result, new architectures and circuit techniques must be investigated if the goal is high-performance multistandard operation using CMOS and its inherently low-Q devices.

The vast majority of transmitters fall into two classes: I/Q modulator-based transmitters and voltage-controlled oscillator (VCO)-based transmitters. Although VCO-based transmitters have shown promise with respect to the elimination of discrete components [5], [6], they are fundamentally limited to constant-envelope modulation schemes. In contrast, I/Q modulator-based transmitters can operate with both constant and nonconstant envelope modulation, making them well suited for multistandard operation. To begin the discussion of I/Q modulator-based transmitters, a homodyne or direct upconversion transmitter is evaluated, followed by a discussion of the traditional heterodyne or indirect upconversion transmitter. Finally, a modified heterodyne transmitter is presented called the harmonic-rejection transmitter.

A. Direct-Upconversion Transmitter (Homodyne)

The direct-upconversion transmitter, shown in Fig. 1, is attractive because of the simplicity of the signal path. The in-phase (I) and quadrature (Q) baseband digital signals pass through a DAC and a baseband filter before the signal is upconverted to RF in a single step. The I and Q signals are then combined before passing through a pre-PA RF filter, a PA, and a second RF filter. Channel tuning is typically performed with a single RF channel-select frequency synthesizer. The shaded components in Fig. 1 would likely remain discrete if CMOS integration with low-Q components was attempted for a number of reasons. In particular, integrating a low-phase noise RF channel-select frequency synthesizer using low-Q components would be particularly difficult for narrow-band cellular standards such as GSM. This would lead to the use of a discrete VCO tank circuit to meet the required phase-noise performance with reasonable power consumption. Aside from the tank circuit, a discrete pre-PA RF filter is needed for two reasons. First, the filter reduces potential third-order intermodulation in the PA that could degrade modulation accuracy. This can be seen in Fig. 2 when the third harmonic of the desired signal intermodulates with the desired signal to produce an unwanted third harmonic of the baseband signal. The pre-PA RF filter is also needed to attenuate transmitted noise that in turn reduces the filtering requirement after the PA. This allows the use of a single filter after the PA with potentially lower loss than if a pre-PA filter was not used. Aside from the need for discrete components, the direct upconversion transmitter suffers from some well-known problems. First, the local oscillator (LO) feedthrough is relatively large because of the high frequency used in the I/Q modulator. The second, and potentially more severe, problem is LO pulling which occurs because the transmitted signal is running at the same frequency as the LO. This condition would only get worse with PA integration. One method to reduce LO pulling is offset mixing [7], [8], but this technique does not address any of the other integration issues. To further improve transmitter performance, an indirect upconversion transmitter is often used.

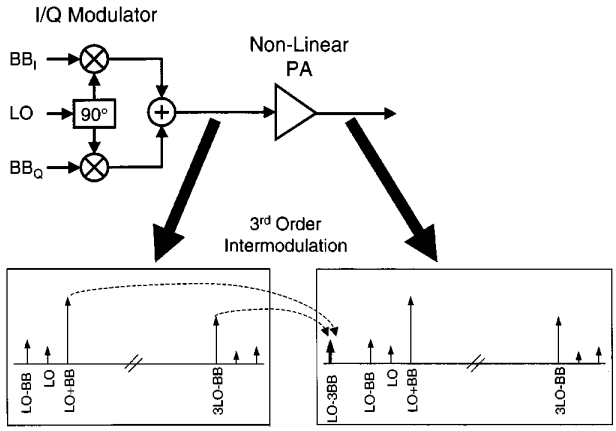


Fig. 2. Third-order intermodulation in PA.

B. Indirect Upconversion Transmitter (Heterodyne)

The indirect upconversion transmitter, shown in Fig. 3, can be viewed as the transmitter version of the superheterodyne receiver. Like the homodyne transmitter, an I/Q modulator is used; however, now the baseband signal is frequency translated to a fixed IF. The signal is then typically filtered to remove unwanted IF harmonics. The IF signal is then upconverted to RF before it passes through a pre-PA RF filter, the PA, and a final RF filter. Like the direct upconversion transmitter, channel tuning is performed with a single RF channel-select frequency synthesizer, and again, the shaded components would likely remain discrete if CMOS integration with low-Q components was attempted. In addition, yet another discrete component, the IF filter, has been added. Furthermore, little has been done to ease the requirements of the RF VCO tank circuit or the pre-PA RF filter. However, this transmitter does have a number of performance advantages. First, LO feedthrough is reduced because of the lower frequency used in the I/Q modulator, and second, LO pulling is reduced because neither oscillator is operating at the transmitted frequency. To further improve performance a modi-

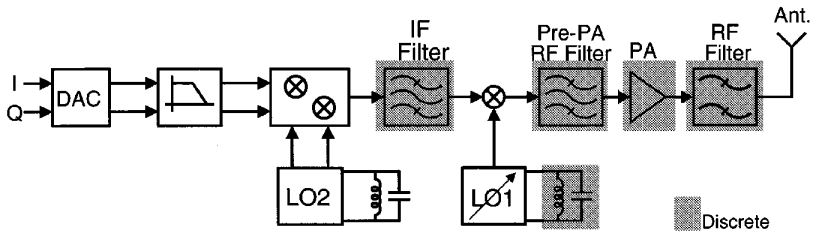


Fig. 3. Indirect upconversion transmitter block diagram.

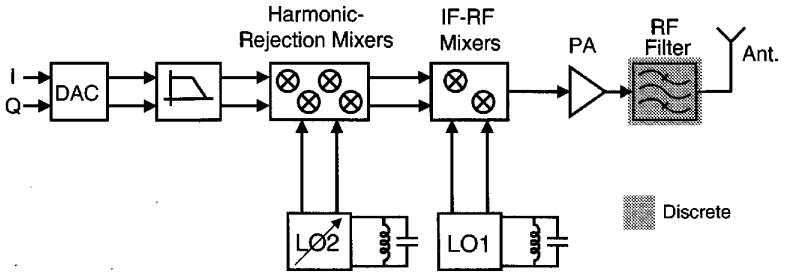


Fig. 4. Harmonic-rejection transmitter block diagram.

fied indirect-upconversion transmitter was used, called the harmonic-rejection transmitter.

C. Harmonic-Rejection Transmitter

The two-step transmitter shown in Fig. 4 is called the harmonic-rejection transmitter (HRT) because of the unique mixers used in the baseband to IF upconversion. This transmitter maintains the performance advantages of the traditional indirect upconversion transmitter in that both LO pulling and LO feedthrough are reduced. In addition, for reasons shown later, the dependency on discrete components has been reduced. For a given performance metric, removal of the IF filter and pre-PA filter may now be possible, as well as complete integration of the RF VCO tank circuit. Integration of the tank circuit is achieved by switching the roles of the synthesizers as compared to a conventional heterodyne transmitter. Channel tuning is now performed with the IF synthesizer while the RF synthesizer is fixed in frequency. By reversing the roles of the two synthesizers, the total phase noise of both synthesizers can be reduced when using low-Q on-chip components for the VCO tank circuitry.

The IF filtering requirement is relaxed by the use of HRMs for the baseband to IF upconversion. As previously mentioned, conventional switching mixers introduce relatively large harmonics at multiples of the IF frequency that require the use of a high-Q filter not amenable to CMOS integration. In contrast, the HRM not only frequency translates the baseband signal to IF but also avoids the need for a discrete filter by attenuating the third and fifth IF harmonics. This attenuation is achieved by effectively multiplying the baseband signal by a 3-bit, amplitude-quantized sinusoid. The details of the HRM will be discussed in more detail in Section III.

In addition to the relaxation of the IF filtering requirement, the requirements on the pre-PA RF filter have also been relaxed. The pre-PA filter is needed to reduce potential third-order intermodulation and to attenuate transmitted noise and spurs. Since the transmitted noise is typically dominated by the phase noise of the synthesizers, switching the roles of the synthesizers potentially allows for low-phase-noise integrated synthesizers which in turn reduce the pre-PA filtering requirement. Also, as previously mentioned, energy located at three times the carrier frequency can intermodulate and degrade the modulation accuracy. In an indirect upconversion transmitter, energy is generated at three times the carrier frequency from the 3LO2 $\times$ 3LO1 mixing product. However, due to the rejection of the third IF harmonic, third-order intermodulation is a less significant problem in the HRT. Consequently, the pre-PA RF filter is no longer needed to prevent significant third-order intermodulation. As a result, PA integration is now possible, because the RF filtering can be performed with one RF filter after the PA.

The next section will discuss some of the important details of the HRT, focusing on the HRM and frequency synthesizers.

III. Transmitter Details

A. Harmonic-Rejection Mixer

A key building block in the HRT is the harmonic-rejection mixer (HRM). Switching mixers are commonly used in RF transceivers because of their numerous advantages compared to other mixer topologies [9]. However, these mixers generate harmonics of the local oscillator frequency, which consequently need filtering. The top half of Fig. 5(a) shows a conventional switching mixer in which the baseband signal is effectively multiplied by a square-wave LO2 signal. The resulting upconverted signal now has relatively large copies of the baseband signal located at odd multiples of the LO frequency. Typically, a high-Q filter is needed to attenuate these copies. Alternatively, an HRM could be used to attenuate the third and fifth LO harmonics, reducing the IF filtering requirement. The fundamental concept of the HRM, shown in Fig. 5(b), is to multiply the baseband signal by a 3-bit, amplitude-quantized sinusoid, $f_{\mathrm{LO2h}}(t)$. Because the first harmonic of $f_{\mathrm{LO2h}}(t)$ is located

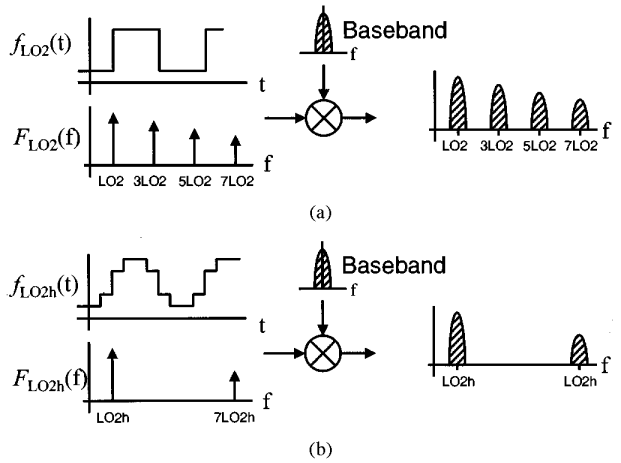


Fig. 5. (a) Conventional switching mixer. (b) Harmonic-rejection fundamentals.

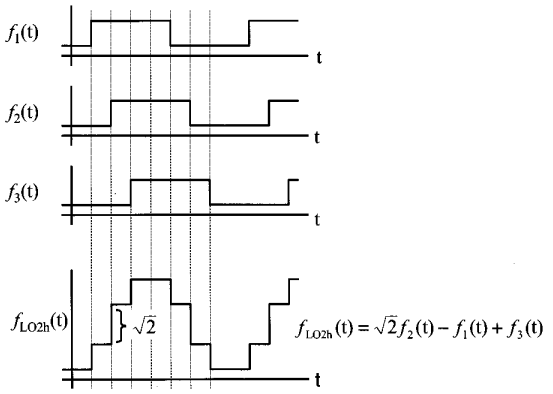


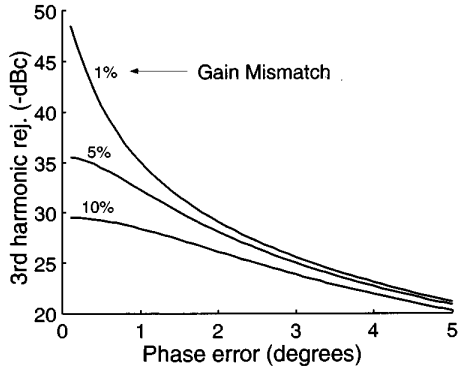
Fig. 6. Harmonic-rejection signal generation.

at seven times the fundamental frequency, the first significant copy of the upconverted baseband signal is also located at seven times the fundamental frequency. Consequently, the IF filtering requirement is greatly relaxed, leading to removal of the IF filter. The next challenge was to generate $f_{\mathrm{LO2h}}(t)$ while maintaining the advantages of using a current-commutating switching mixer. Current-commutating switching mixers allow for a relatively low LO swing, which is critical for integration using low-Q components.

To generate $f_{\mathrm{LO2h}}(t)$, three square waves are summed as shown in Fig. 6. To accurately represent a quantized sinusoid, the magnitude of $f_2(t)$ is scaled by $\sqrt{2}$. To better understand the rejection of the third and fifth harmonics, it is instructive to expand the three square waves using a Fourier series. The Fourier series representation of the three square waves up to the fifth-order component is given by

$$f_1(t) = \frac{\sqrt{2}}{\pi}\left[(\cos(\omega t) - \sin(\omega t)) + \frac{1}{3}(\cos(3\omega t) + \sin(3\omega t)) - \frac{1}{5}(\cos(5\omega t) - \sin(5\omega t))\ldots\right] \quad (1)$$

$$f_2(t) = \frac{2}{\pi}\left[\cos(\omega t) - \frac{1}{3}\cos(3\omega t) + \frac{1}{5}\cos(5\omega t)\ldots\right] \quad (2)$$



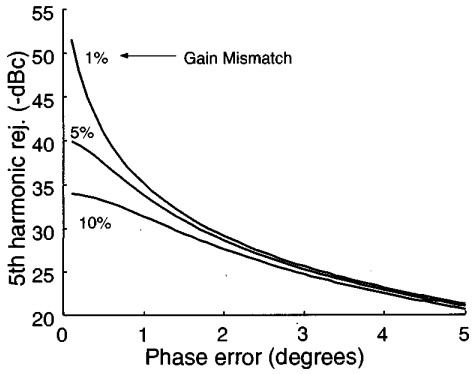


Fig. 7. Harmonic-rejection with mismatch. (a) For third harmonic. (b) For fifth harmonic.

$$f_3(t) = \frac{\sqrt{2}}{\pi}\left[(\cos(\omega t) + \sin(\omega t)) + \frac{1}{3}(\cos(3\omega t) - \sin(3\omega t)) - \frac{1}{5}(\cos(5\omega t) + \sin(5\omega))\ldots\right]. \quad (3)$$

Summing the three ideal square waves with $f_2(t)$ scaled by $\sqrt{2}$ results in the total rejection of the third and fifth harmonics. However, similar to a single-sideband mixer, gain and phase mismatch result in nonideal cancellation of the third and fifth harmonics. The rejection of the third and fifth harmonic are given by

$$\mathrm{HRM}_3 = \left(\frac{1}{9}\right)((1 - \cos(3\theta)(1+\Delta))^2 + ((1+\Delta)\sin(3\theta))) \quad (4)$$

$$\mathrm{HRM}_5 = \left(\frac{1}{25}\right)((1 - \cos(5\theta)(1+\Delta))^2 + ((1+\Delta)\sin(5\theta))) \quad (5)$$

where Δ is the gain mismatch and θ is the phase mismatch. The rejection depends strongly on the phase error in the original signal. Shown in Fig. 7 is the harmonic rejection plotted as a function of phase error for different gain errors. Fig. 7(a) shows the rejection of the third harmonic while Fig. 7(b) shows the rejection of the fifth harmonic. Note that as the phase and gain error increase the rejection of the third harmonic approaches 9.5 dBc while the rejection of the fifth harmonic approaches 14 dBc, which are the levels of an ideal square wave. For one-

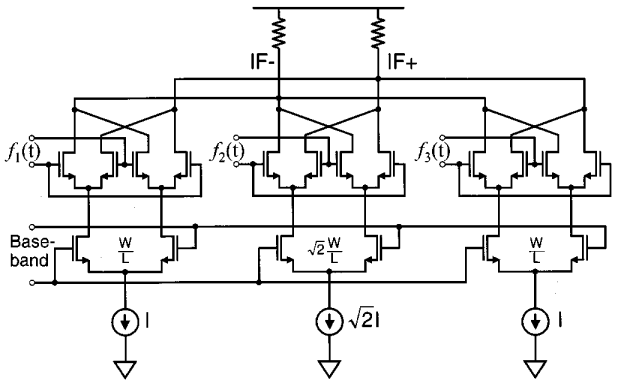


Fig. 8. Harmonic-rejection mixer circuit diagram.

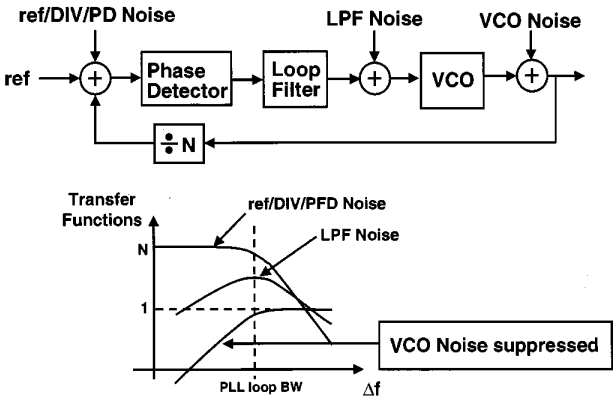


Fig. 9. VCO phase-noise suppression in wide-loop-bandwidth PLL.

degree phase error and 1% matching, approximately 35 dB of rejection is achieved for both the third and fifth harmonics.

To implement the HRM, each square wave, $f_1(t)$, $f_2(t)$, and $f_3(t)$, is mixed with the baseband signal and then the three outputs are summed. The advantage of this approach is that a low-noise switching mixer can now be used. However, a potential disadvantage is that scaling the LO voltage, by $\sqrt{2}$ in this case, will not proportionally scale the output voltage swing. The simplified circuit schematic for the HRM is shown in Fig. 8. The HRM consists of three current-commutating submixers. The transconductance stage of each submixer is driven with the identical baseband signal. However, the switches are driven by the three phase-shifted square waves. The current output of the three submixers is summed to generate the final output signal. Consequently, the baseband signal is effectively multiplied by a 3-bit amplitude-quantized sinusoid. To scale $f_2(t)$ by $\sqrt{2}$, the current switched in the middle submixer was increased by $\sqrt{2}$ by scaling the tail current source. Furthermore, to maintain an equivalent linearity performance in the three submixer transconductance stages, the input transistors were also scaled in the middle submixer to give a V_{dsat} that is equal in the three submixers.

B. Frequency Synthesizers

This transmitter architecture offers advantages with respect to full integration of the frequency synthesizer with on-chip low-Q VCOs. As previously mentioned, channel tuning is now performed with the low frequency synthesizer while the RF synthesizer is fixed in frequency. This achieves lower phase noise than the standard configuration because it allows for the use of a wide loop bandwidth for the RF synthesizer.

Performing channel-tuning with the lower frequency IF synthesizer allows the RF synthesizer to have an extended loop bandwidth, which has the effect of suppressing the close-to-carrier phase noise produced by the VCO. This may be better understood by evaluating the phase-noise transfer functions of the various components within a PLL to the output of the synthesizer, as illustrated in Fig. 9. Here, the phase-noise transfer function from the VCO to the PLL output has a high-pass characteristic relative to the carrier. Because the channel tuning is performed using the lower frequency IF synthesizer, the comparison frequency of the RF synthesizer can be significantly raised,

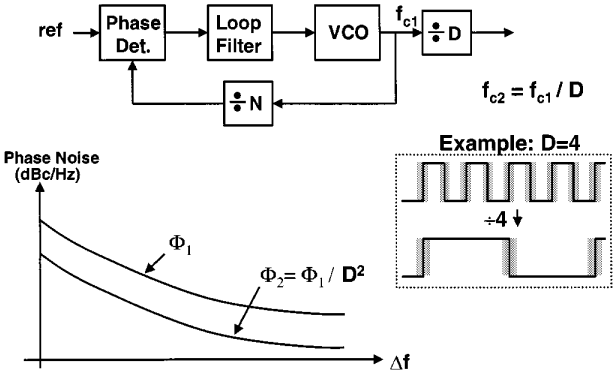


Fig. 10. Phase noise of low-frequency synthesizer.

by as much as a few orders of magnitude. Typically, for reasons related to the stability of a second-order PLL, the loop bandwidth must be anywhere from a fourth to a tenth of the comparison frequency. Therefore, the higher comparison frequency allows an increased loop bandwidth for the RF synthesizer, significantly extending the close-to-carrier bandwidth where VCO phase-noise suppression will occur. The overall RF synthesizer close-to-carrier phase-noise performance can then be designed such that the phase-noise performance is no longer dominated by a noisy integrated VCO using low-Q components in the tank circuit.

Although the lower frequency synthesizer must now perform channel tuning, lower phase noise, relative to the carrier power, can inherently be achieved due to the lower operating frequency. In this transmitter system, narrow channel tuning must be performed. Consequently, the maximum reference frequency and PLL loop bandwidth are limited, ultimately reducing the band of close-to-carrier VCO phase-noise suppression. The concept of inherently lower phase noise at lower frequencies may be understood with a time-domain interpretation, which is illustrated in Fig. 10. Assume for the moment that the PLL used to synthesize the channel spacing required by a narrow-band system produces an output at RF, instead of IF (again, the loop bandwidth would be small). If the output of this synthesizer is divided down to the IF frequency, there is an inherent lowering in both the rms jitter and phase noise as compared to the carrier.

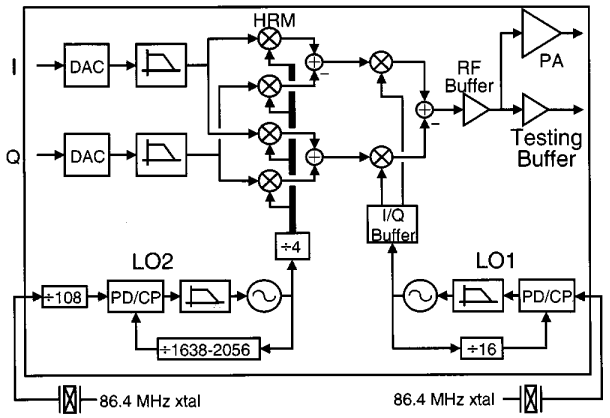


Fig. 11. CMOS prototype HRT block diagram.

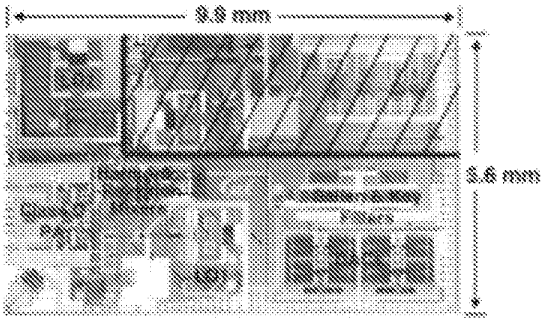


Fig. 12. Die photo.

This is illustrated in Fig. 10 for $D = 4$, where the time-domain waveform at the output of the synthesizer is shown at the bottom. Before the divider, each edge of the waveform contains jitter, resulting from noise generated inside the PLL. If it is assumed that an idealized noiseless divider is used to lower the frequency by a divider ratio D, then the divider will only capture the timing jitter from one of D edges, yet the period of the fundamental waveform increases by a factor of D. Stated differently, the rms timing jitter on the lower frequency LO, at the divider D output, will have the same timing jitter on each edge, however, the period of the waveform is increased by a factor of D. Thus, the jitter relative to the fundamental period has decreased by a factor D. For close-to-carrier phase noise, the timing error created from edge to edge is correlated at the output of the divider. Because of this correlation in timing error from edge to edge, the effect of a noiseless divider is to reduce the close-to-carrier phase noise by the square of the division ratio, in this case D. In the actual implementation of the IF synthesizer used in the transmitter prototype, the channel-tuning synthesizer produces an output in the range of 1.3104 to 1.4704 GHz, in 800-kHz steps. The IF synthesizer output is then divided down by a factor of 4; thus, the close-to-carrier phase noise produced at the output of the synthesizer is reduced by a factor of 16.

The RF synthesizer used by this prototype transmitter has been previously described in [10] and realizes a 1.3824-GHz oscillator with a loop bandwidth of 8 MHz. The IF synthesizer produces frequencies from 327.6 to 367.6 MHz in 200-kHz steps and has a 40-kHz loop bandwidth.

IV. CMOS Prototype

A CMOS prototype HRT was fabricated in a 0.35-μm double-poly five-layer metal process. A block diagram of the HRT is shown in Fig. 11. The HRT integrated the entire transmit signal path from the DACs to the PA, including two frequency synthesizers. Ten-bit digital I and Q baseband signals are brought on chip and passed through two 10-bit resistor string DACs and then filtered by two Sallen & Key third-order low-pass filters. The signals are then upconverted to a variable IF using four HRMs. Four mixers are used to provide image rejection for the baseband signal and to generate both I and Q IF signals. The IF signals are then upconverted to RF using two inductively loaded current-commutating mixers. The RF signal is then buffered before being driven off-chip with either a testing buffer or an integrated class-C PA. The testing buffer is capable of driving 0 dBm into 50 Ω, while the PA is capable of delivering 25 dBm. A die micrograph is shown in Fig. 12.

With the high level of integration implemented in this work, coupling between circuits and circuit blocks can severely degrade performance. The chip was fabricated in an epitaxial process; the epitaxial layer had a resistivity of 10 Ω·cm, while the substrate had a resistivity of 0.01 Ω·cm. With such a low substrate resistivity, it is quite possible that large signals injected into the substrate from the digital circuits or from the power amplifier (PA) can couple back into the sensitive analog sections. To reduce the effects of substrate coupling, three general techniques were used throughout the chip. First, a fully differential signal path was used from the output of the DACs through the output of both the PA and the testing buffer. Ideally, a differential circuit will see coupling from the substrate, due to other circuit blocks, as common-mode noise, and will reject those signals. Both frequency synthesizers were also implemented in a fully differential fashion, including the VCO control voltages. Differential control voltages were used to maximize the immunity of the frequency synthesizers to coupling through the substrate, from other blocks as well as each other. Second, independent supplies, which were heavily bypassed both on and off chip, were used for each of the circuit blocks. This was done so that the local supply and ground would move together; any voltage fluctuations on either the ground or supply nodes would ideally not impact the signals as they moved through the signal path. Third, multiple substrate contacts were placed around the transistors so that the body would move in unison with the local supply and ground. Therefore, any substrate coupling would also be coupled into the supply and ground local to a given circuit block, and would therefore minimize the effect of that coupling on the differential signal path.

To better understand the circuit implementation, a more detailed description of some of the key circuit blocks will follow. The blocks to be discussed include the DAC, the Sallen & Key filter, the RF quadrature generator, and the PA.

A. DAC

Fig. 13 shows the basic structure of the resistor string DAC used in the transmitter. The digital-to-analog conversion is made

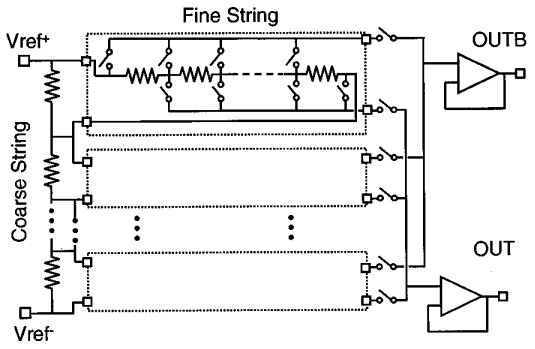


Fig. 13. Dual resistor string DAC schematic.

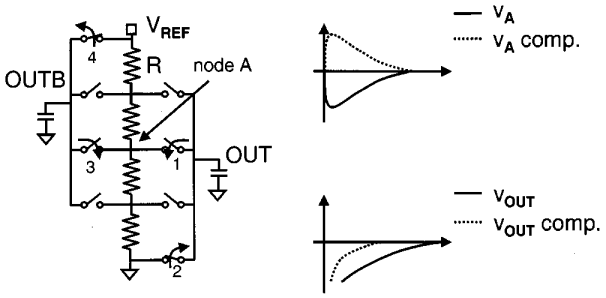


Fig. 14. Glitch reduction circuit technique for DAC.

in two steps using two 5-bit resistor strings that select the appropriate output analog level. In the design of a resistor-string DAC, there is usually a tradeoff between the maximum speed of the DAC and its power consumption. As the total value of the resistance in the resistor string increases, the overall power consumption is reduced, but the time needed for the output voltage to settle is also increased. A critical factor in the settling time is the issue of capacitive coupling between the output and the intermediate nodes in the resistor string. The intermediate nodes in the resistor string should stay at a fixed voltage at all times, but as switches close and open and different intermediate nodes are tied to the output, there is an instantaneous change on the intermediate nodes (for example, node A in Fig. 14) that causes an increase in the settling time of the output. This problem can be reduced through the use of a set of replica switches and a dummy capacitor, as shown in Fig. 14. Switches 3 and 4 switch in opposition to switches 1 and 2, respectively, and thereby induce an equal and opposite effect on the intermediate node voltage A. The uncompensated voltage at node A is summed with the glitch reduction due to the switches 3 and 4, resulting in a reduced fluctuation voltage at node A, as shown in Fig. 14. This allows the voltage at the output to settle more quickly to its desired value; furthermore, in simulation, the power consumption can be reduced as much as 30% for a given settling time. Moreover, the use of complementary switches performs the operation of single-ended to differential conversion. In the actual implementation, the function of the dummy capacitor was performed with the complementary output buffer.

B. Sallen & Key Filter

After the DACs, the I and Q baseband signals are filtered before upconversion. The filtering is performed with a third-order Sallen & Key low-pass filter. The filter uses a buffer in the feedback path to improve the rejection. Shown on the left side of Fig. 15 is a conventional Sallen & Key filter. The feedback capacitor C_1 introduces a zero in the transfer function which decreases the attenuation at higher frequencies. However, the wide-band noise is critical in transmitters, because it may corrupt the highly sensitive receivers nearby. One method of improving the attenuation, at the cost of increased power, is to increase the bandwidth of the forward buffer used in the filter. Alternatively, the effect of the zero may be reduced by adding a buffer in the feedback path as shown in the right side of the Fig. 15. The buffer blocks the zero introduced by the capacitor allowing for a lower bandwidth in the forward buffer. The plot shows the expected attenuation for the two configurations with equal power consumption. At higher frequencies, approximately a 30-dB improvement in the high-frequency attenuation is predicted by simulation with the feedback amplifier, as compared to a conventional Sallen & Key filter consuming equal power.

C. RF Quadrature Generator

The amount of sideband suppression obtained by an image-rejection mixer is highly dependent on the phase accuracy of the I and Q LO signals. For this transmitter system, the quadrature accuracy of the I and Q LO signals further relax the RF filtering requirement of the IF image. Additional and specific requirements of the quadrature generation circuitry used by this transmitter are that both the loading at the output of the synthesizer (or VCO) and the degradation in the VCO tank Q be minimized. Traditional methods of generating quadrature from a single phase include frequency dividers and passive filters realized with resistors and capacitors. The first LO (RF synthesizer) directly generates the frequency required for upconversion by the corresponding mixers, eliminating the possibility of using a frequency divider to generate quadrature LOs. Two common passive filter approaches include using an RC-CR filter or an asymmetric polyphase filter [11]. These passive methods for generating quadrature suffer from a variety of drawbacks, which can include both phase and amplitude frequency dependence, phase error from either component mismatch or process variations, and loss in LO carrier power.

Despite the well-known problems, polyphase filters are still an effective method for generating highly accurate quadrature signals from a single phase. However, there are several mechanisms of loss in this filter that typically require power-consuming buffers at the input and output of the filter. Polyphase filters generate quadrature from a single phase by passing the signal through multiple stages of an RC network when the signal frequency is near the 3-dB frequency of the RC network. Other contributing factors to loss in a polyphase filter include the parasitics associated with bottom plate capacitance used to create the capacitors. If the output is directly coupled to the mixer input, then an ac-coupling capacitor might be needed, which introduces additional parasitics and loss in LO carrier power.

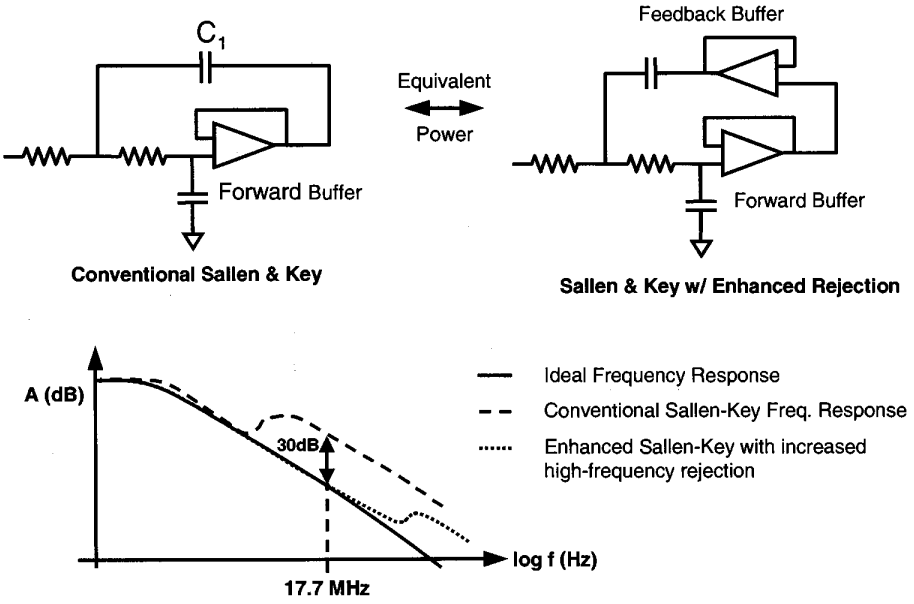


Fig. 15. Improved rejection from Sallen & Key filter.

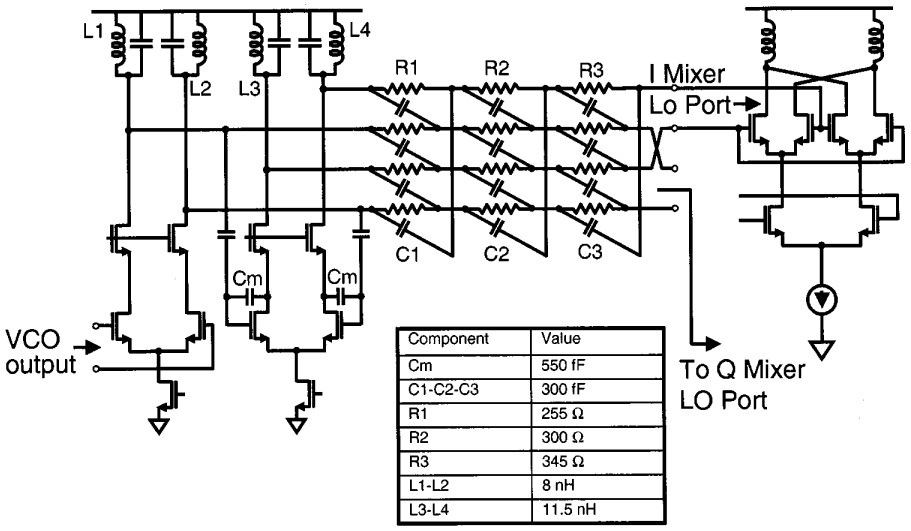


Fig. 16. High-frequency (LO1) VCO buffer quadrature generator circuit schematic.

The circuit shown in Fig. 16 reduces one mechanism of loss in the polyphase filter by using a buffer which drives the input of the filter with signals roughly in quadrature and thus eliminates the inherent 3-dB loss associated with converting a single phase to quadrature phases. Two common source buffers before the polyphase generate signals which are roughly 90° out of phase at the inductively loaded nodes when the operating frequency is near the g_m/C_m of the second buffer [12]. In addition, the input impedance looking into the buffer is capacitive with the exception of the gate resistance r_g, therefore minimizing the reduction in the VCO tank Q and loading. The Q of the LC tank at the buffer output, shown as L1-L4 in Fig. 16, is approximately 1.5 when loaded with the polyphase filter. The mixer LO input was designed to have a common mode at V_{dd} and thus the need for an ac-coupling capacitor has been eliminated as well as its associated loss.

D. Power Amplifier

Previous sections detailed the transmitter architecture, including the benefits of the harmonic rejection architecture with respect to the filtering required before the PA. These benefits allow for the use of an integrated highly nonlinear PA when a constant-envelope modulation scheme is used. Recent efforts that have investigated nonlinear PAs have focused primarily on switch-mode nonlinear PAs, such as class-D and class-E PAs [13], [14]. One drawback to switch-mode PAs, especially with respect to their potential for integration, is the need for a dc–dc converter in order to perform power control, which is

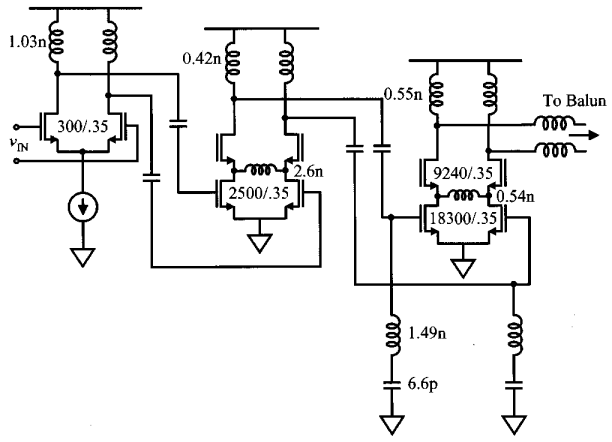


Fig. 17. Class-C power amplifier circuit schematic.

required in most cellular communications systems. In general, the only way to vary the output power level of a switch-mode PA is to vary the power supply; thus the need for the dc–dc converter, which can be difficult to integrate. Therefore, a different solution was explored.

In this work, a class-C architecture was used for the PA. The class-C architecture is an extension of the class-A and class-B architectures. In the class-C architecture, the angle of conduction (the portion of the cycle when the device is on) is less than 180°; the device is biased such that it is off for more than one-half the cycle by setting the dc bias below the threshold voltage of the device. Consequently, the input signal turns the device on for only a fraction of the period. This reduction in the period when the device conducts current serves to reduce the power consumed in the device and thus potentially raises the efficiency of the PA.

In the design of submicron CMOS PAs, a key limitation is the oxide breakdown voltage, which limits the available voltage swing at the drain of the transistor. As a result, the load impedance seen by the device needs to be extremely low in order to deliver the required amount of power without damaging the device. Furthermore, the current level must rise in proportion with the reduced voltage swing. Since CMOS generally has a poor transconductance when compared with silicon bipolar or Gallium Arsenide technologies, the device sizes required can be quite large in order to generate the required output power.

Fig. 17 shows the circuit diagram of the three-stage fully differential class-C PA used in this work. The stages are ac-coupled in order to allow the input device of each stage to be biased independent of the output of the previous stage. Since the PA was to be used in an integrated environment, the previous stages would likely not be able drive a heavy load; therefore, three stages were used in order that the first stage would not load down the output of the mixer. The first stage was biased in a class-A fashion, with a variable tail current source that controls the gain and thus the output power level. The final two stages are biased in a class-C fashion and use a cascode structure with the top devices biased at the supply in order to reduce the stress on the oxide due to voltage excursions at the outputs of those stages. At the input to the final stage, a different tuning technique was used to peak the gain at the desired frequency. Due to the high current drive required and the poor transconductance of CMOS, the output transistor size was extremely large (18300 μm/0.35 μm); using a single spiral inductor to tune out all the capacitance between the second and third stages required an extremely small value inductor (on the order of 0.1 nH). That inductor was quite difficult to implement without parasitic trace inductance affecting the tuning at that node. Instead, a series LC was used in parallel with the gate capacitance of the final stage in order to provide a peaking of the impedance at that node. Furthermore, inductors were used across the differential cascode node in the second and third stages, in order to reduce the current required to charge and discharge the capacitors at those nodes and boost the efficiency. The inductors used at the output of the first and second stages as well as those at the cascode nodes were implemented as spiral inductors on chip; the other inductors used in this circuit were implemented as bond wires, in order to take advantage of their higher Q. The inputs of the second and third stages were biased at 0.35 V with a bias voltage generated on chip.

V. Results

Although the HRT was designed to facilitate multistandard operation, the performance of the transmitter was tested with the DCS 1800 specifications. This up-banded version of GSM was chosen for a number of reasons. First, it requires very high modulation accuracy from the transmitter. Second, DCS 1800 requires very low unwanted spurious transmission especially in the receive band. Finally, DCS 1800 uses a constant envelope modulation scheme making it well suited for use with a highly nonlinear class-C power amplifier.

A. Measured Results With Testing Buffer

The results in this section were measured using a testing buffer after the mixers, in parallel with the PA, as opposed to the PA itself. The next section will compare some of this data when the measurements were taken at the output of the PA instead of the testing buffer.

A critical test for all transmitters is the single-sideband test in which a single baseband tone is upconverted to RF. Although I/Q modulator-based transmitters are ideal for multistandard operation, gain mismatch and phase error in the modulator generally limit the modulation accuracy. Shown in Fig. 18 is the output of the transmitter when a 50-kHz baseband tone is upconverted to RF. The unwanted image suppression was measured at −56 dBc, implying that the gain and phase were matched very well throughout the transmitter. This was accomplished with careful layout techniques and the measurement transmitter has no external tuning. The carrier suppression was measured at −38 dBc while the third-order distortion was measured at −46 dBc. The third-order distortion was dominated by the baseband inputs of the HRMs.

Another key transmitter performance test is measuring the output when a modulated baseband signal is used as opposed to a single tone. Typically, different RF standards provide a spectral mask under which the transmitted signal must fall. Meeting

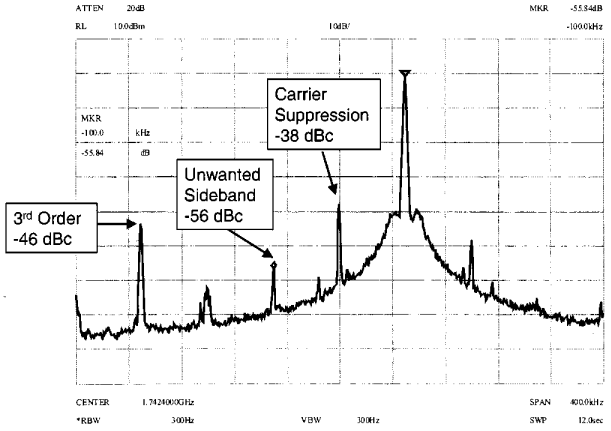


Fig. 18. Transmitter output with single-sideband test.

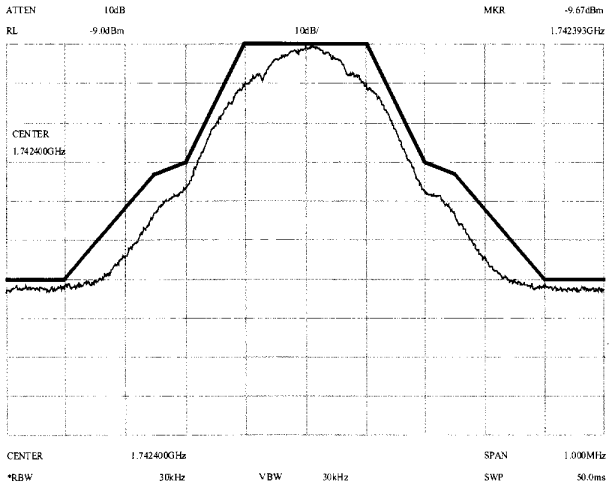


Fig. 19. Transmitter output with modulated baseband signal.

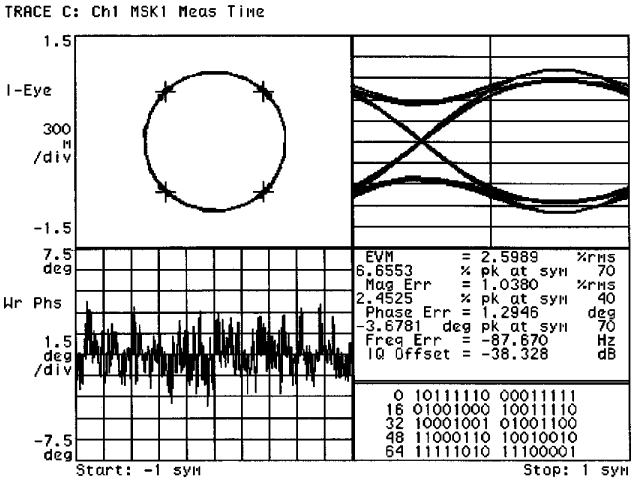


Fig. 20. Modulation accuracy of transmitter.

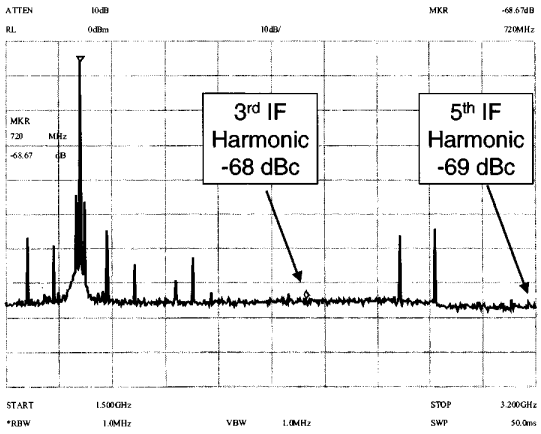


Fig. 21. Wide-band spectrum at transmitter output.

this specification requires low phase noise from the frequency synthesizer and high linearity in the baseband circuits. To test the HRT a DCS 1800 GMSK modulated baseband signal was used. Shown in Fig. 19 is the measured output spectrum along with the DCS-1800 spectral mask requirement. The measured results are limited by the phase noise of the frequency synthesizers.

Although the spectral mask limits the transmitted noise and unwanted spectral emissions, it does not measure the modulation accuracy. This test is typically performed using a modulated baseband signal and comparing the transmitted signal with the ideal signal. The DCS-1800 standard requires that the rms phase error is less than 5° with a peak phase error no larger than 20°. The measured results for the HRT are shown in Fig. 20 and the rms phase error is 1.3° while the peak phase error is 3.7°. This error was probably caused by the nonidealities in the I/Q modulator along with the phase noise of the synthesizers.

In addition to the close-in spectral mask requirements, DCS 1800 limits the unwanted transmissions that could potentially fall in the receive band. Consequently, the limit for the transmitted noise measured at 20-MHz offset from the carrier is -151 dBc/Hz. This transmitter was measured at -126 dBc/Hz. This noise was primarily caused by the phase noise of the frequency synthesizers. To meet the DCS 1800 specification, an RF filter is needed with 25 dB of attenuation at a 20-MHz offset. Such attenuation is achievable with a single RF filter allowing for a highly integrated transmitter requiring only one filter afterwards.

Finally, as a test of the HRM, a wide-band output spectrum was measured. The results are shown in Fig. 21. The suppression of the third IF harmonic was measured to be -68 dBc while the fifth IF harmonic suppression was measured to be -69 dBc. Although the third IF harmonic was further suppressed by the IF–RF image-reject mixer, the fifth IF harmonic was only suppressed by the HRM. The third IF harmonic on the low side of the carrier frequency was only suppressed by the HRM, and it was below the noise floor of the spectrum analyzer.

B. Measured Results With PA

The transmitter was also tested with the class-C PA. Shown in Fig. 22 are the results of a single-sideband test using the same 50-kHz signal. The test setup introduced approximately 2 dB of

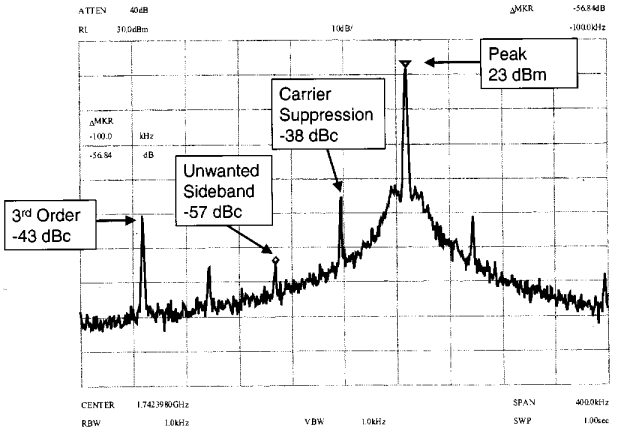


Fig. 22. Single-sideband test with PA output.

TABLE I
SUMMARY OF MEASURED RESULTS

VDD = 3 Volts Temp.= 25°C

	Testing Buffer	PA
Single Sideband Suppression	-56 dBc	-57 dBc
LO2 3rd Harmonic Spur	-68 dBc	-68 dBc
LO2 5th Harmonic Spur	-69 dBc	-69 dBc
IF Image Suppression	-60 dBc	-60 dBc
RF Carrier Suppression	-38 dBc	-38 dBc
RMS Phase Error	1.3°	N/A
Peak Phase Error	3.7°	N/A
20 MHz Carrier Offset Noise	-126 dBc/Hz	-121 dBc/Hz
3rd Order Distortion	-46 dBc	-43 dBc
Output Power	0 dBm	25 dBm
Active Chip Area	20 mm²	24 mm²
Technology	0.35 µm DP-5M CMOS	0.35 µm DP-5M CMOS

loss between the output of the PA and the measurement equipment. The differential to single-ended conversion was accomplished using a microstrip balun similar to the balun described in [14]. Comparing Fig. 22 with Fig. 18 shows very little difference. The integrated PA had little effect on the transmitter output when a single-sideband test was performed. Furthermore, although not shown here, the wide-band spectrum also showed little change compared to the wide-band output measured at the testing buffer. Although the integrated PA had little effect on the modulation performance, the noise at 20-MHz offset was affected by the PA. As previously mentioned, the noise measured with the testing buffer was −126 dBc/Hz while the noise measured with the PA was −121 dBc/Hz. Substrate coupling is the likely cause of the increased noise.

The integrated class-C PA was designed for 1.5-W peak power and was tested as standalone component. The peak measured power of the standalone PA was measured at 1.2 W. This power was not achieved in the integrated version because of the lower than expected gain in the transmitter. This was due to lower than expected Qs for the on-chip spiral inductors which are critical for gain.

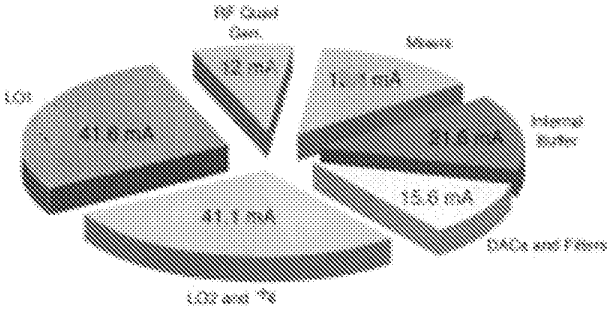


Fig. 23. Transmitter current consumption.

C. Results Summary

A summary of the measured results is shown in Table I. The table shows the results when measured with the testing buffer and the PA. Shown in Fig. 23 is the power consumption of the transmitter excluding the testing buffer and the PA. The lower than expected Qs negatively impacted the power consumption. The current for certain circuit blocks was increased to achieve the desired output power. Because the gain was lower than expected in the transmit path, the power output and the efficiency of the PA were significantly lower than expected.

VI. CONCLUSION

A fully integrated CMOS transmitter has been demonstrated. The entire transmit signal path including the PA and the frequency synthesizers were integrated in a 0.35-μm double-poly five-layer metal CMOS process. The transmitter demonstrated cellular performance requiring only a single RF filter after the PA. The need for pre-PA filtering was removed through the use of a harmonic-rejection transmitter and a wide-loop-bandwidth RF synthesizer. The performance met many of the key requirements of DCS 1800, an up-banded version of GSM. Furthermore, due to careful planning, the effect of on-chip coupling was minimized. This was evident by the fact that the chip incorporated two frequency synthesizers, two DACs, and a 25-dBm PA. Furthermore, the PA had a minimal effect on the performance when the PA output was compared to the output from a post-mixer testing buffer.

ACKNOWLEDGMENT

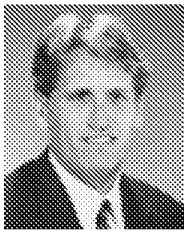
The authors would like to thank STMicroelectronics for their support and for chip fabrication services. Further, the authors are grateful to Agilent Technologies, Atmel, Conexant Systems, National Semiconductor, Nokia Mobile Phones, Nortel Networks, and Philips Research for their valued contributions.

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His research focuses on wireless transmitter architectures well suited for high levels of integration in CMOS. In addition, he is investigating CMOS mixers for wireless applications.

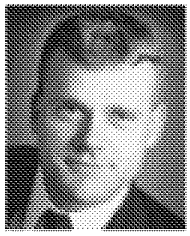
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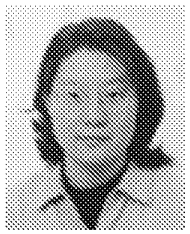
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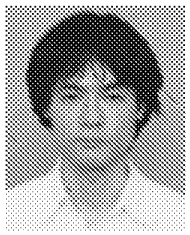
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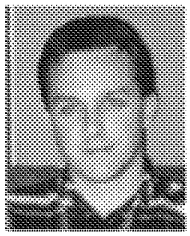
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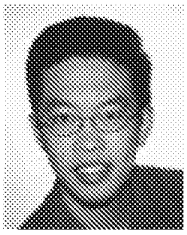
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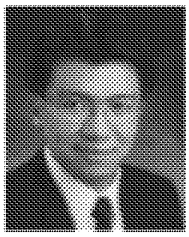
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From 1993 until 1998, he was with STMicroelectronics Central R&D, France, as an Analog Design Engineer in the field of phase-locked loops and clock recovery for ATM (SDH/SONET) and GSM/DCS1800 applications. From 1998 to 1999, he was a Visiting Industrial Fellow in Dr. P. Gray's research group at the University of California, Berkeley. During his stay, he implemented a variable gain amplifier and active filters for a fully integrated RF transceiver. Since 1999, he worked at STMicroelectronics, Crolles, France, on phase quadrature locked loop for digital and cable TV receivers. He is currently developing synthesizers for HiperLAN/2 and 802.11applications. His research interests include mixed RF and analog VLSI circuit design in wireless and cable communications.



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He has been a Teaching Assistant in a number of circuit design classes at the University of California, Berkeley. In the summer of 1998, he was with the Silicon Circuits Research Department at Bell Laboratories, Lucent Technologies, where he conducted research in microwave balun design. He joined Marvell Semiconductor Inc. in 2001, where he continued his work in designing RF ICs for wireless applications.

Mr. Tsai was recognized as an Outstanding Graduate Student Instructor at the University of California, Berkeley, in 1996.



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In 1996 and 1997, he investigated and developed a hardware system for 600-dpi color scanner with Thymedia Company Ltd., Seoul, Korea. In 1999, he designed a board to test the multistandard RF monolithic chip at RF research group in the department of electrical engineering at the University of California, Berkeley.



Paul R. Gray (M'69–SM'76–F'80) was born in Jonesboro, AR, on December 8, 1942. He received the B.S., M.S., and Ph.D. degrees from the University of Arizona, Tucson, in 1963, 1965, and 1969, respectively.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Owner: Entropic Communications, Inc.
Inventors: Madhukar Reddy et al.
App. No.: 90/019,255
Filed: 09/20/2023
Conf. No. 5785
Examiner: LIE, ANGELA M
Art Unit: 3992
Title: WIDEBAND TUNER ARCHITECTURE
Docket No.: 189005.TR003

INFORMATION DISCLOSURE STATEMENT

Dear Examiner Angela M. Lie:

As detailed in Patent Owner's Petition For Extension of Time, the '362 patent has been asserted in three district court cases, two of which are still pending:

a) *Entropic Communications, LLC v. Charter Communications, Inc. et al.* (Eastern District of Texas Case No. 2-22-cv-00125 filed April 27, 2022 and dismissed December 10, 2023).

b) *Entropic Communications, LLC v. Cox Communications, Inc. et al.* (Central District of California Case No. 2-23-cv-01049 filed February 10, 2023 and still pending).

c) *Entropic Communications, LLC v. Comcast Corporation et al.* (collectively "Comcast") (Central District of California Case No. 2-23-cv-01050 filed February 10, 2023 and still pending).

Please let us know if there are any specific documents or types of information, such as invalidity contentions, relevant court rulings, or any other litigation materials you would like us to submit. We are committed to ensuring you have all the necessary information for a thorough reexamination, but do not want to be seen as obfuscating any potentially relevant information by submitting the entire litigation docket. To the extent any of this information would be helpful, please contact the undersigned.

The '362 patent is also involved in the following IPR proceedings. The prior art asserted in the various grounds to the extent not already in the reexamination record is listed under each proceeding number:

a) IPR2024-00432

1) U.S. Patent No. 7,237,214 ("Pandey")

2) U.S. Pub. No. 2006/0233147 ("Karabinis")

3) S. Mirabbasi and K. Martin, "Classical and Modern Receiver Architectures," IEEE Communications Magazine, vol. 38, no. 11, pp. 132-139, November 2000" ("Mirabbasi")

b) IPR2024-00433

4) U.S. Patent No. 7,783,958 ("Eidson")

5) U.S. Pub. No. 2006/0256216 ("Takahiko")

6) Excerpts of Jan M Rabaey, "Digital Integrated Circuits: A Design Perspective" (Pearson, 2nd ed. 2002) ("Rabaey")

c) IPR2024-00434

7) U.S. Pub. No. 2006/0029170 ("Jensen '170")

8) J. Crols and M. S. J. Steyaert, "Low-IF topologies for high-performance analog front ends of fully integrated receivers," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998 ("Crols")

9) A. P. Chandrakasan, "Ultra low power digital signal processing," Proceedings of 9th International Conference on VLSI Design, Bangalore, India, 1996, pp. 352-357 ("Chandrakasan")

We are, herewith, submitting the petitions, declarations, and prior art asserted in the various grounds to the extent not already in the reexamination record and believe the information submitted to be the extent of the information that could be considered material to patentability. However, the identification of this information shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b). To the extent the Office believes any additional information would be helpful to consider, we can provide it upon request.

Respectfully submitted,

Date: June 18, 2024

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6.6 An Embedded 65nm CMOS Low-IF 48MHz-to-1GHz Dual Tuner for DOCSIS 3.0

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Broadcom, Irvine, CA

The increased competition to deliver broadband data to the home (including GPON and VDSL) is motivating cable providers to deliver data rates which far exceed what is presently available based on the DOCSIS 1.x and DOCSIS 2.0 standards. The DOCSIS 3.0 standard provides this bandwidth increase as well as additional flexibility, where higher data throughput can be obtained by bonding together multiple downstream (DS) channels. This standard calls for the ability to bond any 4 channels in a 64MHz contiguous RF bandwidth. Solutions that allow even more channel bonding and provide more flexibility in the allocated frequency spectrum are preferred. This paper reports an embedded dual-tuner architecture able to select two independent 32MHz frequency bands, allowing for a maximum of 16 demodulated 6MHz Annex B DS channels. In Fig. 6.6.1 the top level block diagram is shown: an external LNA amplifies the RF signal which drives an internal splitter, followed by the two low-IF tuners. Each tuner downconverts 5 DS channels to IF frequencies centered at 0MHz (CH 0), +6MHz (CH +1), +12MHz (CH +2), -6MHz (CH -1) and -12MHz (CH -2). Channels +1 and +2 lie at the images of channels -1 and -2 respectively. Any or all channels can be selected for demodulation by the SoC, up to a maximum of eight. Image rejection is enhanced digitally, taking advantage of the tuner integration into the SoC.

Tuner Core Description

Each of the two tuner cores included in this RF front-end is designed to meet both DOCSIS and SCTE 40 performance over a 48MHz-to-1GHz extended cable plant. Previous silicon tuners have been RF stand-alone chips that use high-quality external filters or BiCMOS technology [1, 2]. However, both approaches prevent cost-effective tuner integration with complex SoCs. SCTE 40 adjacent- and plant-loading profiles are 10dB higher than DOCSIS [4, 5], and impose very stringent demands on linearity, phase noise, PLL spurs, harmonic rejection (HR) and image rejection (IR). An innovative PLL architecture achieves low phase noise and low reference spurs, without sacrificing frequency resolution, while a Harmonic Rejection Mixer (HRM) combined with a highly linear tracking filter suppresses LO harmonics.

System Architecture and Signal Path

The dual tuner core has been integrated in a DOCSIS 3.0 cable modem SoC in 65nm CMOS technology, which includes 8 DS receivers with 64-256-1024-QAM demodulators, a 400MHz MIPS, 166MHz DDR I, PCIE and GPHY interfaces, 11dBm output power upstream DAC and 10 PLLs.

Embedding a noise-sensitive 48MHz-to-1GHz tuner is particularly challenging because the RF signals are in the same band as the DDR clock and data. A significant amount of noise pickup occurs in the package leads and bond wires. By moving the LNA off-chip, the signal level is raised at the noisy boundary and pickup suppression requirements are relaxed. The LNA provides up to 20dB of gain with 5dB NF. A 30dB continuous VGA with internal RSSI guarantees a constant power at the tuner input compensating for cable-plant power variations. A cable-tilt detector detects cable high frequency roll-off and compensates with a high-frequency gain boost.

PLL Architecture

Fractional-N PLLs have been commonly used to widen loop bandwidth and obtain fine-frequency resolution, but they have the potential to produce fractional spurs. Fig. 6.6.2 shows the PLL architecture that combines high frequency resolution with a wide loop bandwidth, without introducing reference spurs. A differential crystal oscillator generates the reference clock for a 6MHz-bandwidth (BW) fixed-frequency PLL, which creates the 1200MHz reference for the 32b DDFS and an 8b DAC. The DDFS and DAC combination produces the reference clock for an integer-N PLL which drives the downconversion mixer. This architecture enables sub-kHz LO frequency resolution while providing a high-frequency reference, allowing the PLL bandwidth to be increased. A larger loop BW reduces phase noise and shrinks loop-filter size, thereby eliminating the need for any external components. An active anti-alias filter following the DAC attenuates unwanted spurs and the DAC images. The PLL 2-to-4.8GHz LC VCO frequency is divided by 4-8-16-32 to cover 48MHz to 1GHz, and to create the quadrature and the three phases used in the mixers. The 1200MHz reference PLL is shared between the two tuners and also provides low-jitter references for common high-speed interfaces such as PCIE and GPHY SERDES, resulting in power and area savings at the system level.

Harmonic Rejection Front-End

In a conventional Gilbert-cell mixer the LO switches are hard driven to improve linearity and optimize noise figure. However this generates LO harmonics. Channels present at the LO harmonics are folded on top of the desired one, degrading SNR. Our design incorporates harmonic-rejection mixers, which suppress the 3rd and 5th LO harmonics [6]. Harmonic suppression is limited by LO phase inaccuracies and gain mismatch, but careful design and 65nm logic speed guarantee a minimum HR of 40dB. The RF tracking filter rejects the 7th and 9th harmonics and guarantees total rejection greater than 65dB. This filter is exposed to the full RF input power, thus requiring extremely high linearity and low noise figure. In Fig. 6.6.3 the HR RF front-end with active splitter is shown. The source follower isolates the two tuners, reducing the cross-LO leakage. Below 330MHz the 3rd-order tracking filter is selected. A wide-bandwidth first-order pole reduces the input power and implements a programmable gain optimizing the dynamic range. An active RC approach is preferred to GM-C for its higher linearity, while the 3GHz required UGB is obtained by using short channel devices.

Image Rejection

In order to demodulate each channel the corresponding image needs to be cancelled. SCTE 40 specifies a maximum adjacent power 16 to 21dB higher than the desired channel. Following the baseband ADC, two correction circuits eliminate the gain imbalance (driven by an I^2 (in-phase) -Q^2 (quadrature) error detector) and phase imbalance (driven by an I*Q error detector). Gain- and phase-imbalance correction each consist of the error detector, a first-order loop and correction logic.

Measurements

A micrograph of the tuner is shown in Fig. 6.6.7. Each tuner core occupies 5mm^2 and consumes 750mW from 2.5V in SCTE 40 mode and 480mW in DOCSIS mode. The LNA dissipates 450mW and 180mW in the two modes, respectively. In Fig. 6.6.4 the measured 256-QAM slicer SNR for min, mid and high power across the 50-to-1000MHz band is shown. Fig. 6.6.5 shows the SNR for 5 channels demodulated simultaneously with +10dBc adjacent and +16dBc higher image. PLL reference spurs are below -75dBc. At 1GHz, integrated phase noise from 5kHz to 10MHz is 0.2°. Achieved 256-QAM sensitivity is -73dBm. The dual tuner achieves 30dB SNR in the worst case 256-QAM SCTE40 Table E.7 [4] tests with +16dBc analog adjacent, and +16dBc full-loaded plant, 33dB input SNR and -12dBmV input power. With 135 +15dBmV (-32dBm) analog channels, measured CTB, CSO and XMOD are better than -66dBc, -64dBc and -60dBc respectively.

Acknowledgments.

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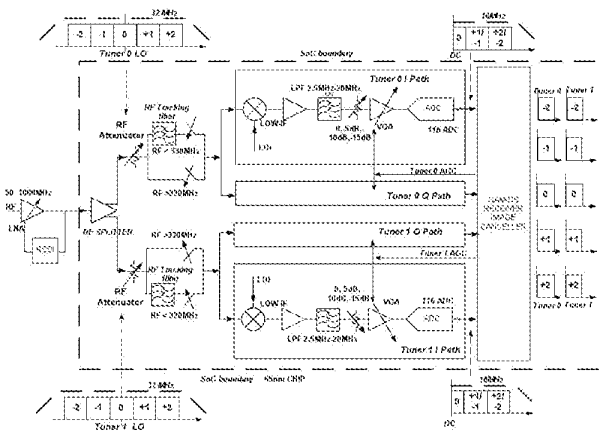


Figure 6.6.1: Embedded dual tuner block diagram.

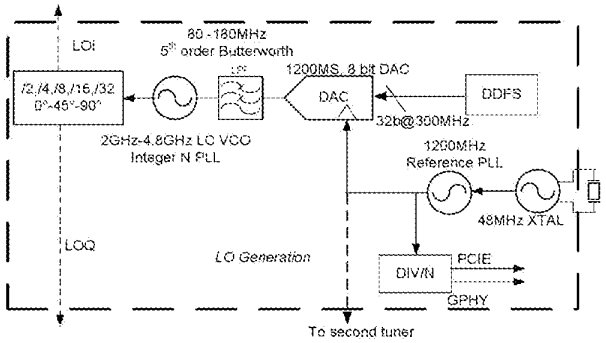


Figure 6.6.2: PLL block diagram.

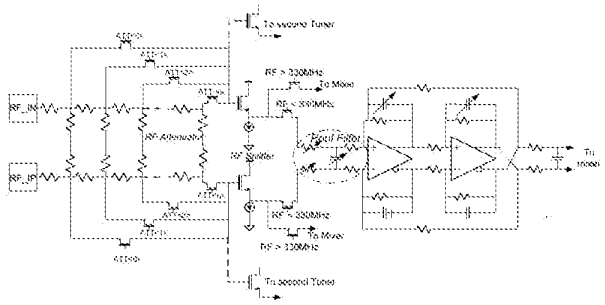


Figure 6.6.3: Harmonic rejection front-end with RF splitter and attenuator.

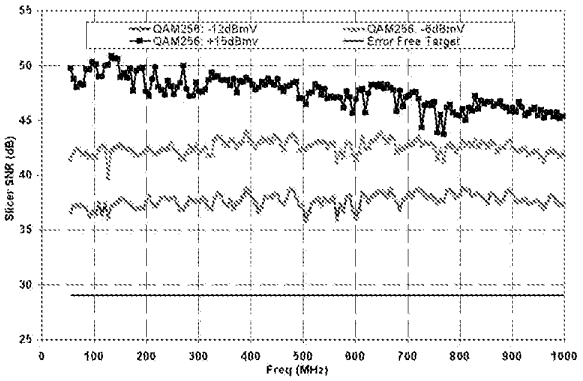


Figure 6.6.4: Single channel 256-QAM measured slicer SNR.

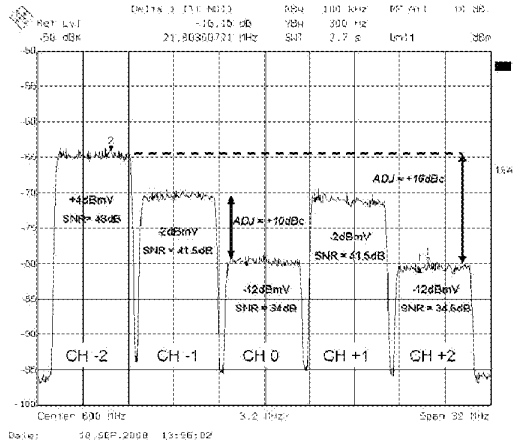


Figure 6.6.5: 5-channel block SNR with +10dBc and +16dBc adjacent-channel power (simultaneous reception).

Input Range	48MHz ~ 1000MHz
Sensitivity (256 QAM)	-73dBm
RF AGC Gain Range	80dB
NF @ Max Gain (tilt on-off)	5-7dB
LO Phase Noise (10kHz)	<-100dBc/Hz
LO RMS Noise @850MHz	0.2 degrees
CTB (Composite Triple Beat)	< -66dBc (SCTE40 Mode)
CSO (Composite Second Order)	< -64dBc (SCTE40 Mode)
XMOD	<-60dBc (SCTE40 Mode)
Max Input Level	-5dBm
Low Input Power SNR (256QAM)	> 36dB
Carrier Peak SNR	51dB
Image Rejection	> 60dB
Single Tuner Power (DOCSIS Mode)	480mW (Tuner + LNA = 640mW)
Single Tuner Power (SCTE40 Mode)	750mW (Tuner + LNA = 1150mW)
Reference PLL Power	60mW
Area (dual tuner)	10mm^2
Process	65nm CMOS

Figure 6.6.6: Performance Summary.

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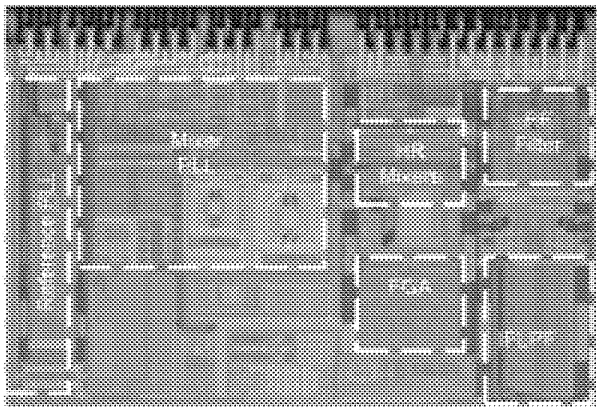


Figure 5.6.7: Tuner die micrograph.

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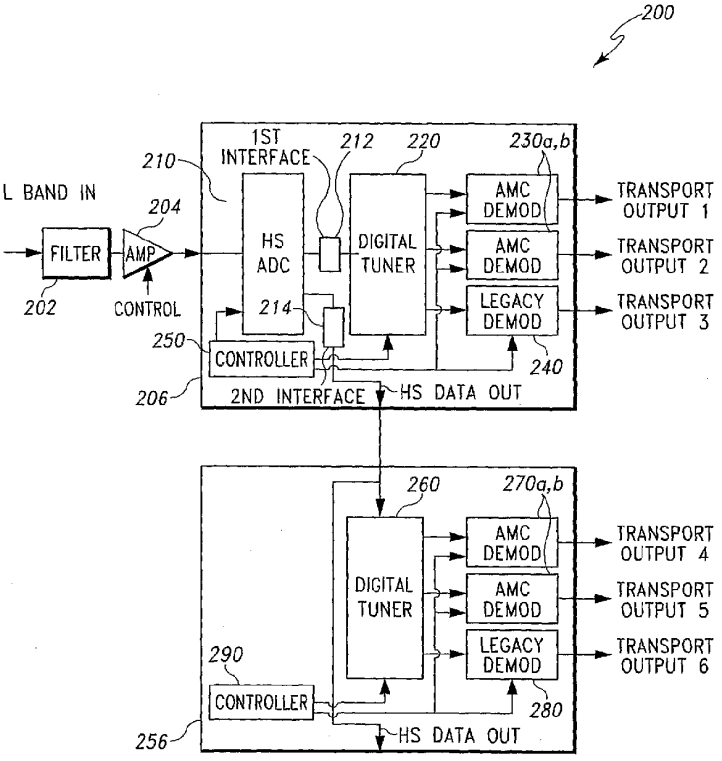
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[Continued on next page]

(54) Title: SYSTEM AND METHOD FOR RECEIVING MULTIPLE CHANNELS



(57) Abstract: The disclosed embodiments relate to a system (200) and method (400) for receiving multiple channels in a communications receiver. The system (200) includes a first module (206) further including an analog to digital converter (210) for converting an input signal to a first and second digital signal and a first processor (220, 230, 240) for processing the first digital signal, and a second module (256) further including a second processor (260, 270, 280) to process the second digital signal. The method (400) involves receiving an analog signal (402), converting the analog signal to a first and second digital signal (404), passing the first digital signal through a first interface (406), processing the first digital signal to a produce a first plurality of output signals (408), passing the second digital signal through a second interface (410), and processing the second digital signal to produce a second plurality of output signals (412).

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System and Method For Receiving Multiple Channels

This application claims the benefit under 35 U.S.C.§ 119 of a provisional application 60/677,501 filed in the United States on May 4, 2005.

FIELD OF THE INVENTION

The invention relates generally toward a communications receiver. The invention more specifically relates to a system and associated method for tuning multiple channels using signal splitting performed after analog to digital conversion.

BACKGROUND OF THE INVENTION

This section is intended to introduce the reader to various aspects of art, which may be related to various aspects of the present invention that are described and/or claimed below. This discussion is believed to be helpful in providing the reader with background information to facilitate a better understanding of the various aspects of the present invention. Accordingly, it should be understood that these statements are to be read in this light, and not as admissions of prior art.

In recent years, media delivery to the home has incurred a rapid change. Today, the consumer may be capable of receiving over 100 different programs of material simultaneously in the home from a number of sources, including satellites systems, cable systems, and the internet. It is evident that the consumer can now choose from a greater number of programming options than ever before.

Consumer products are also undergoing a change to cope with the new demands of the consumer, based on the large number of programming options available. New consumer devices will often allow viewing of at least two programs at once, through picture-in-picture, and may further allow recording of more than one program for later viewing. Some devices may even include the ability to redistribute programs throughout an entire household.

The devices that actually receive the signal have, however, undergone very little change throughout this period. Traditional tuners are typically only capable of tuning to a single physical channel frequency of information. If more than one channel of information is desired, then the traditional approach is to split the power of the radio frequency (RF) signal and provide each of the split signals to a separate tuner. When the RF signal is split, a loss of signal energy and overall signal performance is experienced at each separate tuner. In some cases, more than one RF split is necessary which further degrades the signal available to each tuner. This would be necessary if, for example, four tuners are required for an application. In order to overcome the loss of signal energy, the signal(s) could be actively amplified, either before or after the RF split, but amplification may introduce additional noise and distortion into the signal. Therefore, the split signal may have lower signal quality than the signal received prior to the first signal split.

A system currently using multiple tuner receivers is the digital satellite television service. Indeed, it is now more common to find satellite receivers with at least two tuners included. In the future, satellite receivers may have as many as five tuners. Furthermore, changes in system specifications may require that an extra tuner always be available for receiving control information such as the program guide or other downloadable features.

Recent advances in receiver front end technology are beginning to alter the landscape of the satellite receiver design by shifting more and more circuitry into the digital signal processing domain. Many of the conventional analog functions found in the tuner are now migrating into digital circuitry. An advantage of moving the circuitry to the digital domain is that it may be possible to mitigate the potential signal degradation associated with analog devices such as RF splitters.

However, a further complicating factor for receivers capable of receiving multiple channels is that the data for each channel must be individually demodulated to provide the data that can then be used in further processing such as video and audio decoding. A demodulation process typically involves demodulating an encoded signal and performing error-correction to repair or identify any errors incurred during transmission. The demodulation process may also include equalization to aid reception given current channel impairments. Because of physical limitations in the design and implementation of circuits such as silicon integrated circuits, it may not be possible to include more than a small number of demodulation systems on a single silicon die. Again, a traditional approach would be to include a separate tuner system for every demodulation system in the overall design. However, this approach suffers from the performance degradation discussed above. It is therefore desirable to have a system capable of multiple channel reception that minimizes signal performance degradation and takes advantage of scaling afforded by advancing digital circuit designs.

SUMMARY OF THE INVENTION

The disclosed embodiments relate to a system and method for receiving multiple channels in a communications receiver. The system

includes a first module including an analog to digital converter for converting an input signal to a first and second digital signal and a first processor for processing the first digital signal, and a second module including a second processor to process the second digital signal.

The method involves receiving an analog signal, converting the analog signal to a first and second digital signal, passing the first digital signal through a first interface, processing the first digital signal to a produce a first plurality of output signals, passing the second digital signal through a second interface, and processing the second digital signal to produce a second plurality of output signals.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a block diagram of a preferred embodiment of the present invention.

FIG. 2 is a block diagram of a preferred embodiment of a system utilizing the present invention.

FIG. 3 is a block diagram of another preferred embodiment of a system utilizing the present invention.

FIG. 4 is a flow chart of an exemplary method of the present invention.

The characteristics and advantages of the present invention may become more apparent from the following description, given by way of example.

DETAILED DESCRIPTION

One or more specific embodiments of the present invention will be described below. In an effort to provide a concise description of these embodiments, not all features of an actual implementation are described

in the specification. It should be appreciated that in the development of any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming, but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

The following describes a circuit used for receiving satellite signals. Other systems utilized to receive other types of signals where the signal input may be supplied by some other means may include very similar structures. Those of ordinary skill in the art will appreciate that the embodiment of the circuits described herein is merely one potential embodiment. As such, in alternate embodiments, the components of the circuit may be rearranged or omitted, or additional components may be added. For example, with minor modifications, the circuits described may be configured to for use in non-satellite video and audio services such as those delivered from a cable network.

Referring now to Fig. 1, a block diagram of a preferred embodiment of the invention is shown. Fig. 1 shows a tuner demodulator circuit 100 used in a receiver in a satellite signal receiving system. The tuner demodulator circuit 100 may generally be

incorporated within a single electrically operative module such as an integrated circuit (IC). An analog RF input signal is supplied to the tuner demodulator circuit 100. The RF input signal represents the transmitted satellite signal downconverted to an intermediate frequency (IF) in the L-band frequency range between one and two gigahertz (GHz). The L-Band signal contains the entire spectrum and associated data corresponding to a particular polarized signal from a particular satellite within the system. For instance, the L-band signal may contain sixteen specific physical channels of information all frequency division multiplexed together and occupying a frequency range between approximately 950 and 1450 MHz. Each channel may be approximately 20 MHz in bandwidth and carry many individual programming streams.

The input signal, representing more than one individual channel, is input to the tuner demodulator circuit 100 and passed to a high speed analog to digital (A/D) converter 110. The input signal may be processed by circuitry, such as amplifiers and filters, not shown, prior to being input into the the tuner demodulator circuit 100. The high speed A/D converter 110 samples the L-band signal to generate a digital output. A sampling clock, not shown, is also input into the high speed A/D converter 110. The sampling clock may be a fixed clock source from a crystal or may be generated from another source using a phase locked loop (PLL) oscillator. The sampling clock frequency may be chosen so as to allow proper sampling of the entire L-band signal. In one embodiment, the sampling frequency of 933 Megahertz (MHz) is chosen to sample an L-band signal in the frequency range of 960 MHz to 1440 MHz. The output of the A/D converter 110 represents a set of time samples of the L-band signal where each sample may be a digital word represented by a number of bits. In a preferred embodiment, the sample at the output of the A/D converter 110 is a digital word represented by 8 bits. Due to the sampling process employed, the

frequency spectrum of the sampled digital output of the output of the A/D converter 110 may be frequency shifted and/or transposed relative to its original position in frequency as an analog signal at the input.

The signal from the output of the A/D converter 110 connects to the digital tuner block 120. The signal at the output of the A/D converter is a very high speed digital signal representing, for instance, as much as 8 bits of data at 933 Megasamples per second. Difficulty may arise in providing a signal at such high speed to other functions within the module. The very high speed digital signal may be demultiplexed into two or more signals representing, for instance, two sets of 8 bit signals at 466.5 MHz. The demultiplexing and other timing function may be found within the A/D converter 110. The signal may then be provided over first interface 112. Since the very high speed digital signal is contained within a module, a nonstandard signal format and interface method may be used in connecting the very high speed digital signal to the digital tuner block 120. The first interface 112 may simply provide an electrical connection between the A/D converter 110 and the digital tuner block 120. In one embodiment the very high speed signal is provided on first interface 112 over a controlled impedance interface of a controlled electrical length as a set of signals referenced only to the ground plane.

The digital tuner block 120 provides digital signal processing of the entire spectrum to down-convert and generate one or more specific channels of baseband digital data necessary for further individual channel demodulation and processing. The term baseband as used here is used to represent a signal that is located at baseband or is located in a frequency range that is near to baseband. In one embodiment, three different digital baseband signals are provided as outputs from the digital tuner block 120. In practice, the number of digital baseband signals provided is limited by the number of channels provided in the original L-band signal input, the number of simultaneous

channels the digital tuner block 120 can downconvert and generate, and/or the number of demodulators that can follow.

The one or more baseband digital signals are still coded for transmission and therefore must be further demodulated and corrected for transmission errors before the actual programming information becomes available. Demodulation and decoding is carried out in ether the advanced modulation and compression (AMC) demodulators 130a, b or the legacy demodulator 140 depending on the transmission standard the individual channel signal has employed. The type and number of demodulators used is a matter of design choice, and in a preferred emobodiment two AMC demodulators and one legacy demodulator have been included.

The AMC demodulators 130a, b and legacy demodulator 140 contain digital signal processing for the demodulation, transmission equalization, and error correction of the signals according to the required transmission standard. In particular, a legacy demodulator includes processing necessary to demodulate and decode transport streams sent in Motion Picture Entertainment Group standard MPEG 2 format with a Quaternary Phase Shift Keying (QPSK) modulation format. An AMC demodulator includes the processing necessary to demodulate signals sent in MPEG Joint Video Team (JVT) format with 8-PSK modulation and Low Density Parity Check (LDPC) error correction, in addition to the processing included in the legacy demodulator. The AMC demodulator may also include an equalization system to further enhance signal recovery of the more complex format. Further details regarding the individual detailed operation of either of these types of demodulator is beyond the scope of this specification.

The AMC demodulators 130a, b and legacy demodulator 140 provide outputs labeled as transport outputs 1, 2, and 3 respectively. The transport outputs contain individual or multiple program streams of

audio, video or data information and may be provided to digital audio/video decoding processes for actual display of the programs and information.

Collectively, the digital tuner block 120, AMC demodulators 130a, b and legacy demodulator 140 make up the processing for the first signal supplied through the first interface 112. Other processing may be included as is known in the art. Other functions and blocks may also be present, but not shown, in the tuner demodulator circuit 100 including a controller for controlling the tuning and signal processing functions. Also, control circuitry may be present in the tuner demodulator for controlling the satellite system's external processing module, often referred to as the outdoor unit. The outdoor unit may include circuitry and processing for switching between different satellites or polarizations. The tuner demodulator circuit 100 may also include control for external circuitry capable of providing some preselection of channels in order to allow the preselected set of channels to be delivered on one cable to the receiver and further to the tuner demodulator as described.

Because of the limitations of physical silicon processes discussed earlier, only a small number of demodulators such as the AMC demodulators 130a, b or legacy demodulator 140 may be present on any single module or integrated circuit. For example, three such circuits may be present. However, it may be necessary or desirable to demodulate, for example, all of the available signal channels simultaneously within one system. In order to accommodate additional demodulators, it may be desirable to split the signal before tuning occurs.

In order to accommodate splitting the signal, a high speed data output and second interface 114 is shown connected to the A/D converter 110. The high speed data output through second interface 114 may represent a digital data signal before digital tuning and demodulation. The high speed data output may be presented externally

from the tuner demodulator 100 using some high-speed serial or parallel bus system. For example, in one embodiment the second interface 114 may utilize the low voltage differential signaling (LVDS) protocol on a parallel eight bit bus. Other interface types and formats are possible, as are well known to those skilled in the art. Further, as described for first interface 112, the high speed data output may be multiplexed in order to reduce the operating data speed. The high speed data output signal may be demultiplexed in a manner acceptable for distribution using LVDS in the second interface 114 and may be different than the manner of first interface 112. In one embodiment, the signal is demultiplexed by a factor of four, resulting in four sets of eight bit signals in parallel operating at a bus speed of 233.25 MHz.

Additionally, due to the unknown external nature of the interface, it may be desirable to provide at least one synchronizing signal. The synchronizations signal(s) may be the original high speed clock as well as a demultiplexing clock or other synchronizing signal as is known in the art. All of the demultiplexing and synchronization may further be generated within the A/D converter 110 and supplied through the second interface 114. In this manner, the A/D converter 110 provides two separate signals in two separate formats over two separate interfaces to two separate tuning and demodulating functions. The A/D converter 110 provides a signal containing essentially all of the channels from the original signal through a first interface to the digital tuner 120, and provides substantially this same signal through a second interface in a second format to additional circuits located outside tuner demodulator 100. The interface may serve as an input to a second module or IC containing additional demodulators, such as AMC demodulators or legacy demodulators, as described in more detail below.

Referring now to Fig. 2, a preferred embodiment of a system, 200, incorporating the invention using two tuner demodulator circuits, such as

that shown in Fig. 1 is shown. The L-band analog signal, containing a plurality of satellite channels delivered from an outdoor satellite unit not shown, is processed prior to entering tuner demodulator 206. In a preferred embodiment, the L-band signal is first filtered in L-band filter 202 to remove unnecessary signals present outside the desired L-band frequency range. The output of the L-band filter is connected to a gain controllable amplifier 204. The gain controllable amplifier 204 adjusts the L-band signal level, by means of a control signal, to best optimize the signal for inputting to the A/D converter 210 in tuner demodulator 206. The control signal for the gain controllable amplifier 204 may be generated by circuitry on the tuner demodulator circuit 206. In a preferred embodiment, the control signal may be generated by determining the signal power in the digital data signal from the output of the A/D converter 210. It is important to note that other processing may be possible before the signal enters the tuner demodulator 206.

Tuner demodulator 206 contains an A/D converter 210, first and second interfaces 212 and 214, digital tuner 220, demodulators 230a, b and 240 as described above. The tuner demodulator 206 provides transport outputs 1, 2, and 3 for further information processing as described above. A controller 250 provides control for the operation of the digital tuner 220 and the demodulators 230a, b and 240. The controller 250 connects to all of the existing blocks in the tuner demodulator 206. The controller 250 operatively receives inputs from external circuitry, not shown, representing, for instance, requests from a user for channels to be received and tuned. The controller 250 processes these inputs to generate the control information and provides this control information to the digital tuner 220 for selecting and tuning the particular channel from the group of channels present. The controller 250 may also generate the control information used by the demodulators 230 a, b and 240 for selecting particular channel

demodulation characteristics, such as the type of modulation or error correction that may be used with the particular channel.

The tuner demodulator 206 also contains a high speed data output through second interface 214 providing an output signal representative of the digital signal at the output of the A/D converter. The high speed data output connects to tuner demodulator 256. Tuner demodulator 256 does not contain an A/D converter and utilizes the signal supplied by the high speed data output as the input signal to the digital tuner 260 within the tuner demodulator 256. Collectively, the digital tuner block 260, AMC demodulators 270a, b and legacy demodulator 280 make up the processing for the second signal supplied through the second interface 214. Additional processing may also be included as is known in the art. The tuner demodulator 256 may choose the particular information about the signal necessary to demodulate one or more channels, which would likely be different than the channels tuned in tuner demodulator 206.

The tuner demodulator 256 provides transport outputs 4, 5, and 6 for further information processing as described above. A controller 290 connects to all of the existing blocks in the tuner demodulator 256. The controller 290 may operatively receive inputs from external circuitry, not shown, representing, for instance, requests from a user for channels to be received and tuned. The controller 290 processes these inputs to generate the control information and provides this information to the digital tuner 260 for selecting and tuning the particular channel from the group of channels present. The controller 290 may also generate the control information used by the demodulators 270a, b and 280 for selecting particular channel demodulation characteristics, such as the type of modulation or error correction that may be used with the particular channel.

The tuner demodulator 256 may also contain a high speed data output similar to tuner demodulator 206. It may also contain an

interface, not shown, similar to second interface 214. The high-speed data output stream may be again routed externally and provided to another tuner demodulator. The signal splitting and distribution operation may continue until as many channels of information as necessary may be processed and demodulated.

In one embodiment, the analog-digital converter 210 may reside on a separate integrated circuit die packaged within a multi-chip module integrated circuit. The integrated circuit die containing the digital tuner and demodulators used in both tuner demodulator 206 and tuner demodulator 256 may be identical. The high-speed A/D converter may be present in only one integrated circuit and not be present on subsequent integrated circuits used in the system. As a result, a single circuit for the tuner and demodulator may be designed and the system design may be scaled externally corresponding to the number of channels desired for simultaneous demodulation, and require that only one A/D converter be used in a particular system. The ability to depopulate or eliminate the A/D converter circuits would save cost on the overall implementation, provide an effective method for signal splitting, and yet still provide the convenience of a single circuit design.

Turning now to Fig. 3, a preferred embodiment of a system, 300, incorporating the invention using two tuner demodulator circuits is shown. The L-band analog signal is processed through L-band filter 302 and gain controllable amplifier 304 as described above. It is important to note that other processing may be possible before the signal enters the tuner demodulator 306.

Tuner demodulator 306 contains an A/D converter 310, first and second interfaces 312 and 314, digital tuner 320, demodulators 330a, b and 340, and controller 350 as described above. The tuner demodulator 306 provides transport outputs 1, 2, and 3 for further information processing as described above. The tuner demodulator 306 also

contains a high speed data output for providing an output signal to the input of tuner demodulator 356.

Tuner demodulator 356 does not contain an A/D converter and utilizes the signal supplied by the high speed data output as the input signal to the digital tuner 370 inside of the tuner demodulator 356. The high speed data output is connected internally to the digital tuner block 320. In this manner, the split signal from A/D converter 310 may be modified by utilizing a portion of the processing in the digital tuner block 320 before splitting and transferring the signal to tuner demodulator 356. The tuner demodulator 356 may choose the particular information about the signal necessary to demodulate one or more channels, which would likely be different than the channels tuned in tuner demodulator 306. The controller 390 within tuner demodulator 356 provides a control signal for controlling what information is provided from tuner demodulator 306 to tuner demodulator 356. For instance, a control signal, supplied by a separate connection as shown, may be supplied from tuner demodulator 356 to tuner demodulator 306 for controlling the specific processing needed in the digital tuner block 320. The controller 390 also connects, and provides control, to all of the existing blocks in the tuner demodulator 356, as described above.

The processed signal output from digital tuner 320 may be routed through second interface 314 as the high speed data output and provided as an input in tuner demodulator 356. An advantage of using such an approach would be to allow the high speed data output to operate at a lower operating speed because only a specified portion of the original signal would be transferred to tuner demodulator 356, rather than the entire signal containing all channels. In one embodiment, the digital tuner 320 may generate more than one signal for delivery to tuner demodulator 356 based on the control signal. Each of these signals may represent one or more individual channels as required for the

operation of tuner demodulator 356. Each signal transferred between tuner demodulator 306 and tuner demodulator 356 may then utilize separate physical connections. The tuner demodulator 356 also provides transport outputs 4,5, and 6 for further information processing as described above. In this embodiment, it may be possible that either controller 350 or controller 390 may serve as a master controller for receiving inputs from external sources, such as user inputs for controlling the channels to tune.

In another embodiment, the tuner demodulator 356 may also contain a high speed data output similar to tuner demodulator 306. The high-speed data output stream may be again routed externally and provided to another tuner demodulator. The signal splitting and distribution operation may continue until as many channels of information as necessary may be processed and demodulated.

In another embodiment, the high speed data output may be modified by allowing more than one signal processed by the digital tuner block 320 to be multiplexed onto the same interface connection. Multiplexing the signals to be transferred may result in reducing the number of separate connections between tuner demodulator 306 and tuner demodulator 356 by combining all of the signals processed by digital tuner block 320 and provided to tuner demodulator 356 onto one bus connection.

Turning now to Fig. 4, an exemplary method, 400, utilizing the present invention is shown. At step 402, an analog input signal is received. The analog input signal may represent, for instance, a plurality of channels located at different frequencies delivered from a satellite system.

Next, at step 404 the analog input signal is converted from its analog form to a digital form in a circuit such as A/D converter 210, as

described in Fig. 2. The converted signal is now a digital signal representing a plurality of or channels.

Next, at step 406, the digital signal is passed through a first interface 212. This first interface may primarily be an interface that is internal to a module. After passing through the first interface, at step 408, the signal is tuned in digital tuner 220, and the selected tuned channels are then demodulated in demodulators 230a, b and 240 respectively to produce one or more transport outputs.

In parallel to steps 406, at step 410, the digital signal passes through a second interface 214. The second interface may utilize the high speed output that may additionally provide a signal external to a module where the A/D converter 210 is located. Finally at step 412, the converted signal, having passed through the second interface 212, tuned in digital tuner 260, and the selected tuned channels are then demodulated in demodulators 270a, b and 280 respectively to produce one or more transport outputs.

As described earlier in Fig. 3, the signal that is provided through the first interface 312 and the signal that is provided through the second interface 314 may or may not be substantially the same. For instance, the signal provided through the second interface 314 may include some additional processing performed within the digital tuner 320 connected to the first interface 312.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and will be described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

What is claimed is:

1. A system (200) for processing multiple channels in a communications receiver comprising:

a first module (206) including an analog to digital converter (210) for converting a first input signal to a first digital signal and a second digital signal and a first processor (220, 230, 240) for processing said first digital signal; and

a second module (256) including a second processor (260, 270. 280) to process said second digital signal.

2. The system (200) set forth in claim 1, wherein said first module (206) further includes a first interface (212) between said analog to digital converter (210) and said first processor (220, 230, 240) to provide said first digital signal in a first format to said first processor (220, 230, 240).

3. The system (200) set forth in claim 2, wherein said first module (206) further includes a second interface (214) connected to said analog to digital converter (210) to provide said second digital signal in a second format to said second processor (260, 270. 280) of said second module (256).

4. The system (200) set forth in claim 3, wherein said second interface (214) provides said second digital signal outside of said first module (206).

5. The system (200) set forth in claim 1, wherein said first processor (220, 230, 240) further includes a tuner (220).

6. The system (200) set forth in claim 5, wherein said tuner (220) is a digital tuner capable of tuning and outputting a plurality of channels simultaneously.

7. The system (200) set forth in claim 1, wherein said second processor (260, 270. 280) further includes a demodulator (270, 280).

8. The system (200) set forth in claim 7, wherein said demodulator (270, 280) is capable of demodulating a QPSK signal.

9. The system (200) set forth in claim 1, wherein said second signal represents a plurality of channels.

10. The system (200) set forth in claim 1, wherein said first module (206) outputs a plurality of first output signals.

11. The system (200) set forth in claim 10, wherein said second module (256) outputs a plurality of second output signals.

12. The system (200) set forth in claim 11, wherein said plurality of first output signals and said plurality of second output signals are transport signals.

13. The system (200) set forth in claim 1, wherein said first input signal contains a plurality of analog channels.

14. The system (200) set forth in claim 13, wherein said analog to digital converter (210) processes said plurality of analog channels simultaneously.

15. The system (200) of claim 13, where said plurality of analog channels are frequency division multiplexed.

16. The system (200) set forth in claim 13, wherein said plurality of analog channels are a set of satellite channels.

17. The system (200) set forth in claim 1 wherein said second module (256) further includes a controller (290) operatively coupled between said second module (256) and said first module (206) for controlling said second digital signal.

18. The system (200) set forth in claim 1, wherein said first module (206) and said second module (256) are integrated circuits.

19. A method (400(for providing multiple outputs from a single input, the method comprising the steps of:

receiving an analog signal (402);

converting said analog signal to a first digital signal and a second digital signal (404);

passing said first digital signal through a first interface (406);

processing said first digital signal passed through said first interface to produce a first plurality of output signals (408);

passing said second digital signal through a second interface (410); and

processing said second digital signal passed through said second interface to produce a second plurality of output signals (412).

20. The method (400) set forth in claim 19, wherein in the step of processing said first digital signal passing through said first interface (408) further comprises the steps of tuning said first digital signal.

21. The method (400) set forth in claim 19, wherein the step of processing said second digital signal passing through said second interface (412) further comprises the steps of demodulating said second digital signal to produce a plurality of transport streams.

22. The method (400) set forth in claim 19, wherein said first interface and said second interface are not the same.

23. The method (400) set forth in claim 19, wherein said first interface is an interface for passing said first digital signal internal to a module.

24. The method (400) set forth in claim 19, wherein said second interface is an interface for passing said second digital signal to the outside of a module.

25. A system (200) for receiving multiple channels, the system comprising:
means for receiving an analog signal;
means for converting said analog signal to a first digital signal and a second digital signal (210);
means for passing said first digital signal through a first interface (212);
means for processing said first digital signal passed through said first interface to produce a first plurality of output signals (220, 230, 240);
means for passing said second digital signal through a second interface (214); and
means for processing said second digital signal passed through said second interface to produce a second plurality of output signals (260, 270. 280).

26. A system (200) for processing multiple channels in a communications receiver comprising:

a first module (206) including an analog to digital converter (210) for converting a first input signal, containing a plurality of analog channels, to a first digital signal and a second digital signal, a first interface (212) connected to said analog to digital converter (210) to internally provide said first digital signal in a first format, a first processor (220, 230, 240) connected to said first interface (212) to tune and demodulate said first digital signal provided by first interface (212), and a second interface (214) connected to said analog to digital converter (210) to externally provide said second digital signal in a second format; and

a second module (256) connected to said second interface (214) including a second processor (260, 270. 280) to tune and demodulate said second digital signal.

1/4

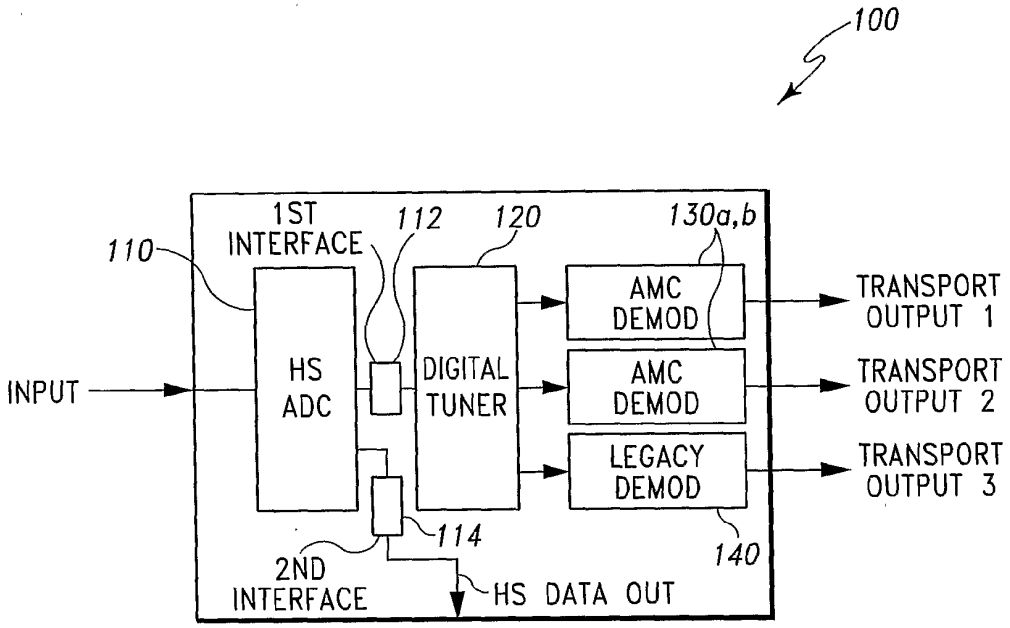

100
110
1ST INTERFACE
112
120
130a,b
INPUT
HS ADC
DIGITAL TUNER
AMC DEMOD
AMC DEMOD
LEGACY DEMOD
TRANSPORT OUTPUT 1
TRANSPORT OUTPUT 2
TRANSPORT OUTPUT 3
114
140
2ND INTERFACE
HS DATA OUT

Fig. 1

2/4

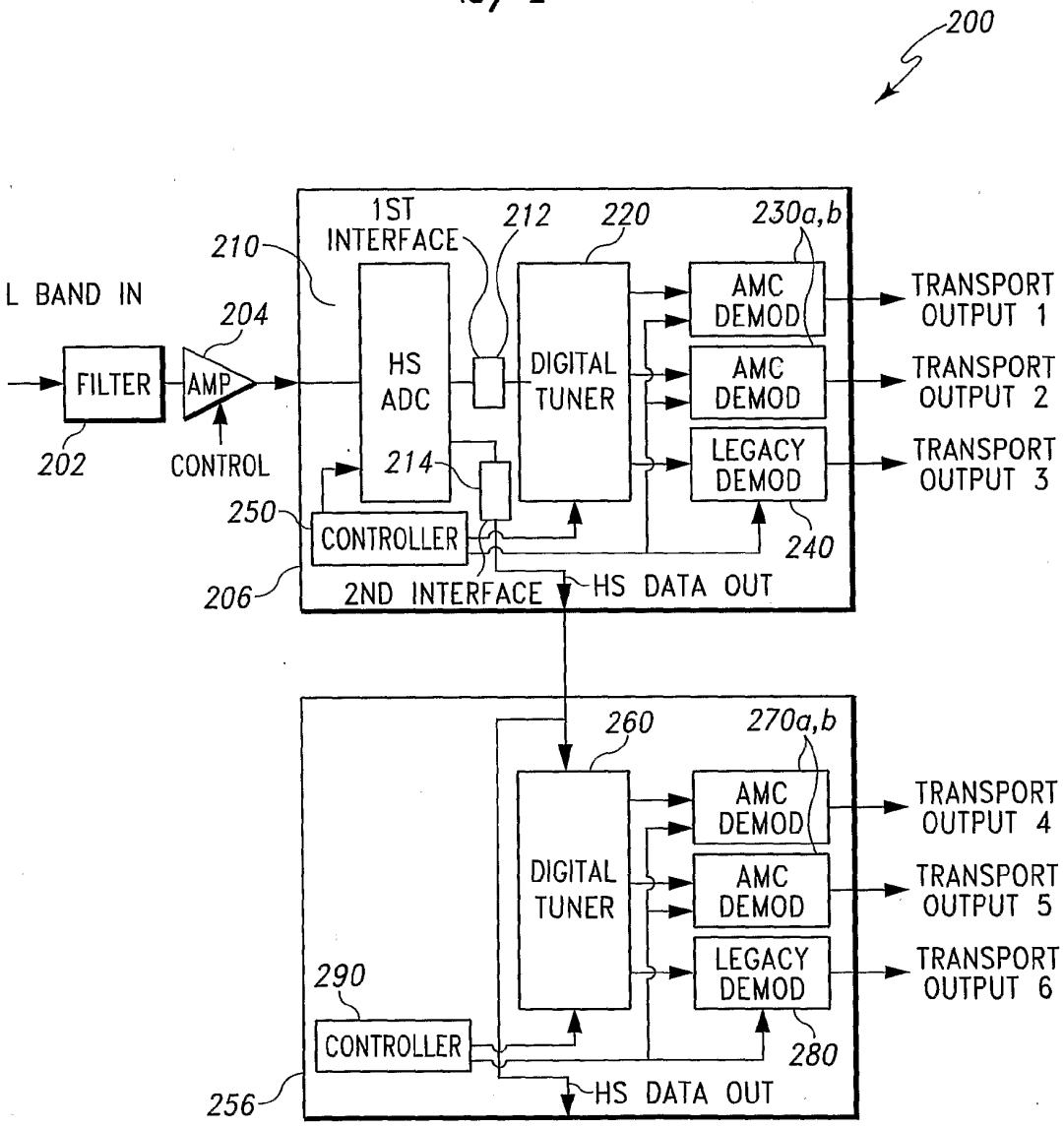

200
1ST INTERFACE
212
220
230a,b
210
L BAND IN
204
HS ADC
DIGITAL TUNER
AMC DEMOD
AMC DEMOD
LEGACY DEMOD
TRANSPORT OUTPUT 1
TRANSPORT OUTPUT 2
TRANSPORT OUTPUT 3
FILTER
AMP
202
CONTROL
214
250
CONTROLLER
240
206
2ND INTERFACE
HS DATA OUT
260
270a,b
DIGITAL TUNER
AMC DEMOD
AMC DEMOD
LEGACY DEMOD
TRANSPORT OUTPUT 4
TRANSPORT OUTPUT 5
TRANSPORT OUTPUT 6
290
CONTROLLER
280
256
HS DATA OUT

Fig. 2

3/4

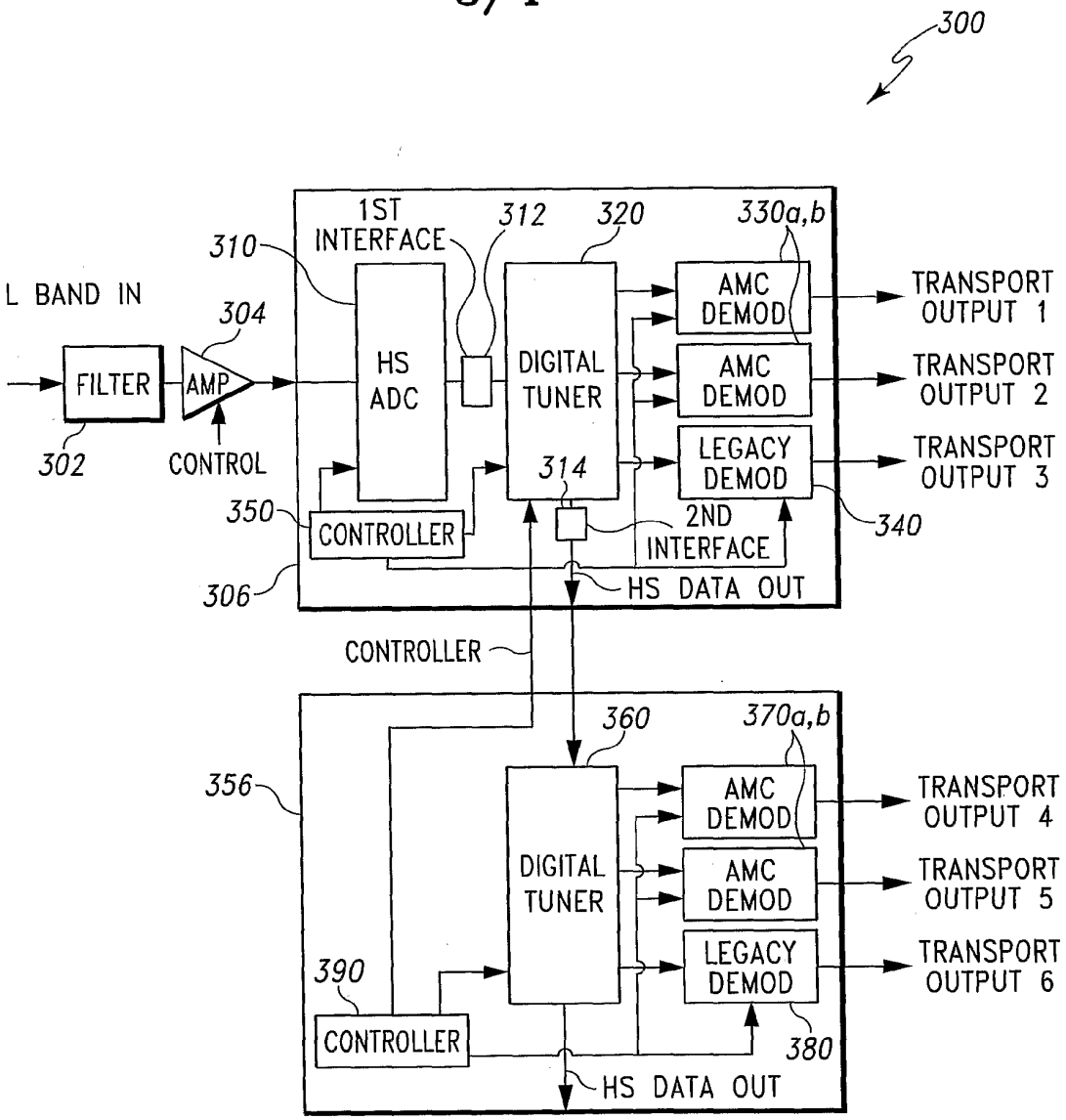

300
L BAND IN
FILTER
AMP
CONTROL
302
304
310
1ST INTERFACE
312
320
330a,b
HS ADC
DIGITAL TUNER
AMC DEMOD
AMC DEMOD
LEGACY DEMOD
TRANSPORT OUTPUT 1
TRANSPORT OUTPUT 2
TRANSPORT OUTPUT 3
314
340
350
CONTROLLER
2ND INTERFACE
306
HS DATA OUT
CONTROLLER
360
370a,b
356
DIGITAL TUNER
AMC DEMOD
AMC DEMOD
LEGACY DEMOD
TRANSPORT OUTPUT 4
TRANSPORT OUTPUT 5
TRANSPORT OUTPUT 6
390
CONTROLLER
380
HS DATA OUT

Fig. 3

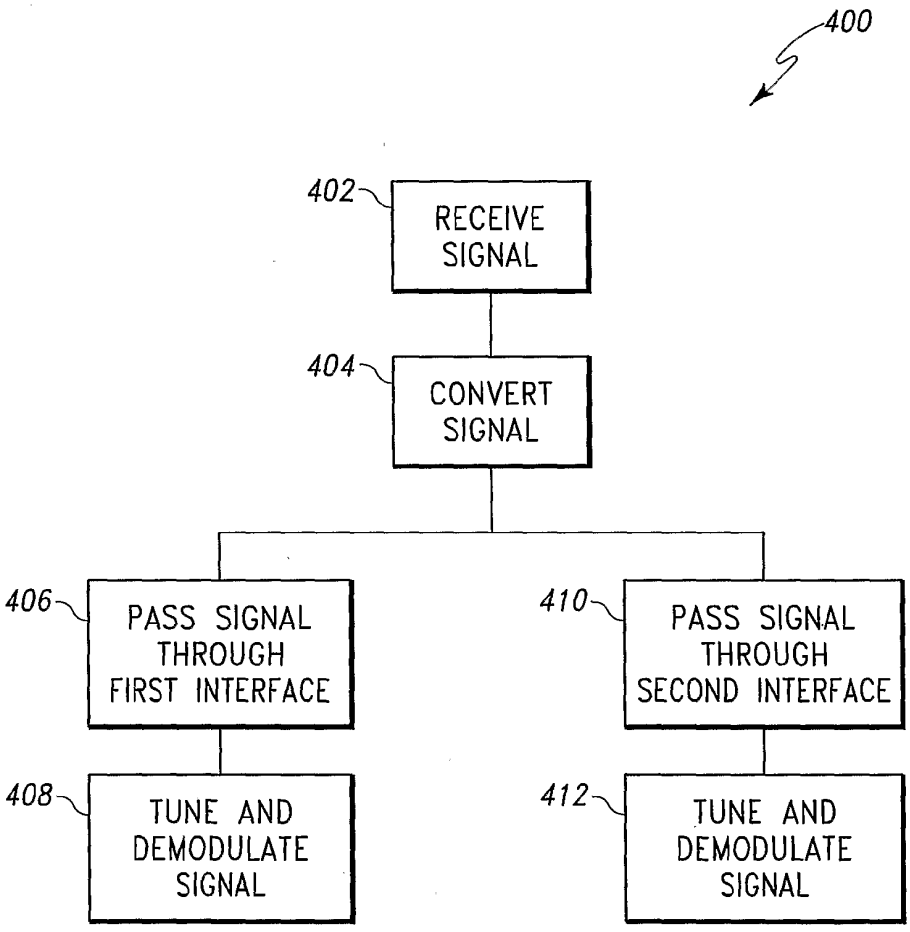

400
402
RECEIVE SIGNAL
404
CONVERT SIGNAL
406
PASS SIGNAL THROUGH FIRST INTERFACE
408
TUNE AND DEMODULATE SIGNAL
410
PASS SIGNAL THROUGH SECOND INTERFACE
412
TUNE AND DEMODULATE SIGNAL

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/011818

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04B1/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 282 184 B1 (LEHMAN BRIAN JAMES ET AL) 28 August 2001 (2001-08-28) abstract; claim 1; figure 2 column 5, line 48 - line 67	1-26
X	US 2002/118784 A1 (TEO KOON H ET AL) 29 August 2002 (2002-08-29) abstract; claim 1; figure 1	1,19,25, 26
X	EP 1 437 837 A (SAMSUNG ELECTRONICS CO., LTD) 14 July 2004 (2004-07-14) abstract; claim 1; figure 1	1,19,25, 26
A	US 5 859 878 A (PHILLIPS ET AL) 12 January 1999 (1999-01-12) abstract; claim 1; figure 1	1,19,25, 26

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
13 July 2006	26/07/2006

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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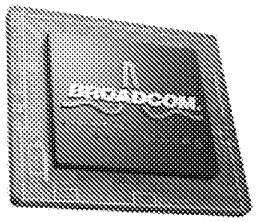
Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		EP 0847631 A1	17-06-1998
		WO 9708843 A2	06-03-1997

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Connecting everything®

BCM3380 PRODUCT Brief



INTEGRATED DOCSIS®/ EURODOCSIS™ 3.0 CABLE MODEM SOC

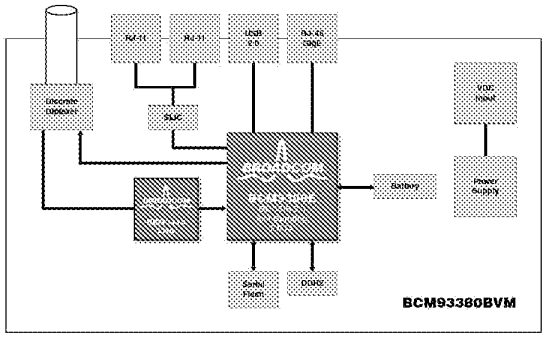
FEATURES

- **DOCSIS®/EuroDOCSIS™ 3.0 compliant MAC**
  - Eight channels downstream
  - Four channels upstream
  - Integrated octal demod and quad modulator
- **Integrated 64-MHz wideband receiver**
  - Two independent 32-MHz blocks
  - 1-GHz plant support
- **Integrated quad power amp**
- **Advanced Processor Architecture**
  - 1000 DMIPS VIPER™ Processor Core
  - Four hardware assist engines
  - High speed DDR2 interface
  - Total processing capability of 500 kpps
- **Integrated IPTV Solution**
  - Complete QAM to IP processing on chip
  - Hardware MPEG to IP conversion engine
  - Dedicated connectivity to IP-STB
- **Complete set of advanced peripheral interfaces**
  - Two USB 2.0 Host/Device ports with integrated PHY
  - Two 10/100/1000 Mbps Ethernet ports with Ethernet^{AV}, 1 with integrated PHY
  - One PCI Express® interface
  - Two SIM card interfaces for fixed mobile convergence
- **Advanced VoIP Subsystem**
  - 2-line Audio Processing Module with integrated codec and HVG
  - Direct interface to low-cost external dual SLIC
  - PCM interface for expansion beyond two voice lines
  - Battery Management Unit
  - CablexChange® software support

SUMMARY OF BENEFITS

- **Highest speed DOCSIS/EuroDOCSIS 3.0 solution available with downstream up to 320 Mbps and upstream up to 160 Mbps enables competitive MSO offering.**
- **Unmatched, powerful processing architecture enables line speed data rates and ability to maximize total system performance of a DOCSIS/ EuroDOCSIS 3.0 system.**
- **Flexible integrated receiver or independent external tuners do not put additional burden on MSO channel lineup.**
- **1-GHz receiver support enables MSOs to expand their usable spectrum.**
- **Maximum integration reduces total system cost, eliminating the need for external tuners, power amps, or PHY devices.**
- **Integrated IPTV solution creates an end-to-end IPTV solution, enabling MSO to utilize reduced cost IP-STB without investment on the headend.**
- **Integrated highest speed interfaces enable maximum DOCSIS/ EuroDOCSIS 3.0 speeds without additional cost, and provides maximum flexibility in application including Wi-Fi® Gateways, IPTV, Media Server Gateways, Fixed Mobile Convergence platforms, etc.**
- **Complete VoIP subsystem leverages proven CablexChange software for full PacketCable™ and SIP support.**
- **System compatible configurations enable multiple end products with marginal additional investment.**
- **10th generation DOCSIS technology ensures a proven, robust, and reliable solution.**

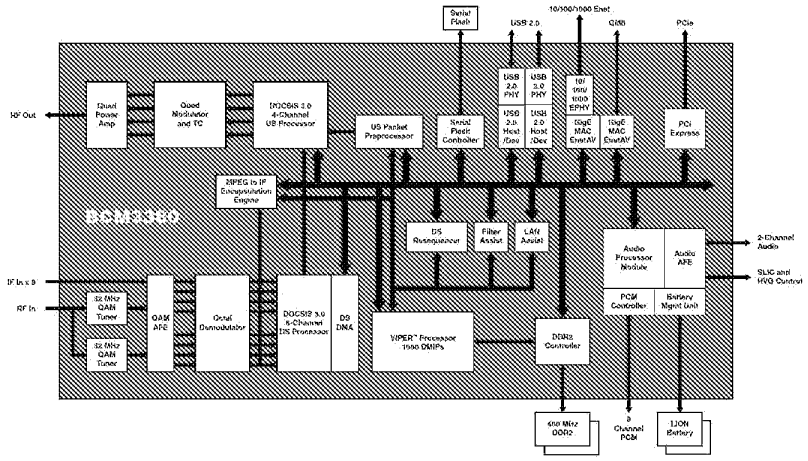
DOCSIS/EuroDOCSIS 3.0 Embedded Multimedia Terminal Adapter (eMTA)



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DEF_ENTROPIC_PRIOR ART 00020757

OVERVIEW



BCM3380 Block Diagram

The BCM3380 is the industry's first fully integrated solution for DOCSIS/EuroDOCSIS 3.0 applications. With advanced support for eight downstream channels, the BCM3380 is the world's fastest cable modem SoC enabling cable operators to deliver competitive high-speed services. The BCM3380 integrates all of the necessary functionality to enable cost-optimized solutions for data modems, eMTAs, gateways, media servers, and fixed mobile convergence platforms.

Delivering over 1000 DMIPS, the advanced VIPER processor and the four independent hardware assist engines deliver unmatched packet processing power. With total capability of over 500 kpps, the BCM3380 enables line speed rates, maximizes the eight downstream and four upstream channels of DOCSIS/EuroDOCSIS 3.0, with plenty of processing power to handle gateway and other advanced applications such as WiFi or VoIP.

The BCM3380 incorporates a complete IPTV solution. By performing QAM to IP conversion on chip, the BCM3380 enables operators to offer IPTV service and directly take advantage of lower cost IP-STB hardware. The MPEG to IP integrated hardware engine within the BCM3380 encapsulates MPEG data coming from the RF interface into IP format and passes it along to any interface, such as Ethernet, USB, WiFi, etc., all without any added jitter. Further QoS is provided by patented Ethernet^{AV} technology, which provides QoS within the Ethernet network. With a second Ethernet interface integrated on chip, BCM3380-based IPTV applications are not burdened with additional costs of external Ethernet switches. The eight downstream channel capability of the BCM3380 supports IPTV without jeopardizing the simultaneous support of a full 4-channel DOCSIS 3.0 modem.

With an integrated VoIP subsystem similar to that deployed through multiple previous generations of Broadcom voice cable modem SoC, the BCM3380 delivers a proven, robust VoIP system. By incorporating a complete 2-channel voice system, the BCM3380 relies only on an external, low-cost SLIC device to complete the VoIP subsystem. The BCM3380 provides codec functionality, battery management, as well as high-voltage generation for lowest cost VoIP implementation. Expandability beyond two voice lines is supported via PCM interface.

The BCM3380 is intended for use in a variety of applications, such as data modems, voice modems, gateways, media servers, and fixed mobile convergence platforms. With a wide variety of high-speed standard interfaces, including USB 2.0, 10/100/1000 Mbps Ethernet, and PCI Express, the BCM3380 is optimized for each application.

BCM3380 Product Configurations

	Primary Application	*External Tuner Support*	*PCI e™*	*USB Port1*	*USB Port2*	*GMII*	*Voice*	*SIM Card*	*IPTV*
BCM3380D	Data Modem	N	N	DEV	N	N	N	N	Y
BCM3380E	2-Line EMTA	N	N	DEV	N	N	Y	N	Y
BCM3380Z	Gateway	Y	Y	HOST/DEV	HOST/DEV	Y	Y	Y	Y

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Digital Integrated Circuits

A Design Perspective

SECOND EDITION



JAN M. RABAEY
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To Kathelijn, Karthiyayani, Krithivasan, and our Parents

"Qu'est-ce que l'homme dans la nature?
Un néant a l'égard de l'infini,
un tout al l'égard du néant,
un milieu entre rien et tout."

"What is man in nature?
Nothing in relation to the infinite,
everything in relation to nothing,
a mean between nothing and everything."

Blaise Pascal, *Pensées*, n. 4, 1670.

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PART

1

The Fabrics

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term, this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000."

Gordon Moore,
Cramming more Components onto
Integrated Circuits, (1965).

CHAPTER

1

Introduction

The evolution of digital circuit design

Compelling issues in digital circuit design

How to measure the quality of a design

Valuable references

1.1 A Historical Perspective
1.2 Issues in Digital Integrated Circuit Design
1.3 Quality Metrics of a Digital Design
  1.3.1 Cost of an Integrated Circuit
  1.3.2 Functionality and Robustness
  1.3.3 Performance
  1.3.4 Power and Energy Consumption
1.4 Summary
1.5 To Probe Further

1.1 A Historical Perspective

The concept of digital data manipulation has made a dramatic impact on our society. One has long grown accustomed to the idea of digital computers. Evolving steadily from mainframe and minicomputers, personal and laptop computers have proliferated into daily life. More significant, however, is a continuous trend towards digital solutions in all other areas of electronics. Instrumentation was one of the first noncomputing domains where the potential benefits of digital data manipulation over analog processing were recognized. Other areas such as control were soon to follow. Only recently have we witnessed the conversion of telecommunications and consumer electronics into the digital format. Increasingly, telephone data is transmitted and processed digitally over both wired and wireless networks. The compact disk has revolutionized the audio world, and digital video is following in its footsteps.

The idea of implementing computational engines using an encoded data format is by no means an idea of our times. In the early 19th century, Babbage envisioned large-scale mechanical computing devices, which he called *Difference Engines* [Swade93]. Although these engines use the decimal number system rather than the binary representation now common in modern electronics, the underlying concepts are very similar. The Analytical Engine, developed in 1834, was perceived as a general-purpose computing machine, with features strikingly close to modern computers. Besides executing the basic repertoire of operations (addition, subtraction, multiplication, and division) in arbitrary sequences, the machine operated in a two-cycle sequence, called "store" and "mill" (execute), not unlike today's computers. It even used pipelining to speed up the execution of the addition operation! Unfortunately, the complexity and the cost of the designs made the concept impractical. For instance, the design of Difference Engine I (part of which is shown in Figure 1-1) required 25,000 mechanical parts at a total cost of £17,470 (in 1834!).

The electrical solution turned out to be more cost effective. Early digital electronics systems were based on magnetically controlled switches (or relays). They were mainly used in the implementation of very simple logic networks. Such systems are still used in train safety systems. The age of digital electronic computing only started in full with the introduction of the vacuum tube. While originally used almost exclusively for analog processing, it soon was recognized that the vacuum tube was useful for digital computations as well. Not long thereafter, the first complete computers were realized. The era of the vacuum-tube-based computer culminated in the design of machines like the ENIAC (intended for computing artillery firing tables) and the UNIVAC I (the first successful commercial computer). To get an idea about *integration density*, the ENIAC was 80 feet long, 8.5 feet high, and several feet wide; it also incorporated 18,000 vacuum tubes. It became rapidly clear, however, that this design technology had reached its limits. Reliability problems and excessive power consumption made the implementation of larger engines economically and practically infeasible.

All changed with the invention of the *transistor* at Bell Telephone Laboratories in 1947 [Bardeen48], followed by the introduction of the bipolar junction transistor by Schockley in

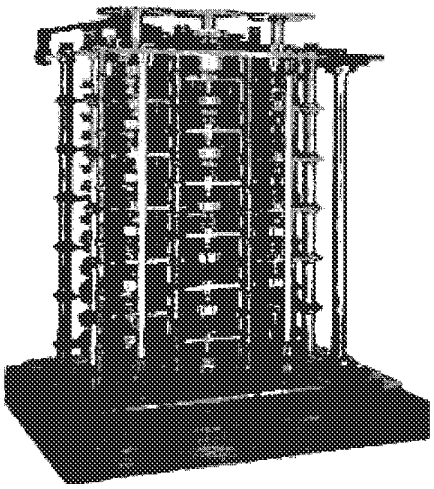


Figure 1-1 Working part of Babbage's Difference Engine I (1832), the first known automatic calculator (from [Swade93], courtesy of the Science Museum of London).

1949 [Schockley49].[1] It took until 1956 before this led to the first bipolar digital logic gate, made of discrete components introduced by Harris [Harris56]. In 1958, Jack Kilby at Texas Instruments conceived the *integrated circuit (IC)*, in which all components, passive and active, are integrated on a single semiconductor substrate—he was awarded the Nobel prize for this breakthrough. It led to the introduction of the first set of integrated-circuit commercial logic gates, called the *Fairchild Micrologic family* [Norman60]. The first truly successful IC logic family, *TTL (Transistor-Transistor Logic)* was pioneered in 1962 [Beeson62]. Other logic families were devised with higher performance in mind. Examples of these are the current switching circuits that produced the first subnanosecond digital gates and culminated in the *ECL (Emitter-Coupled Logic)* family [Masaki74]. TTL had the advantage, however, of offering a higher integration density and was the basis of the first integrated circuit revolution. In fact, the manufacturing of TTL components is what spearheaded the first large semiconductor companies such as Fairchild, National, and Texas Instruments. The family was so successful that it composed the largest fraction of the digital semiconductor market until the 1980s.

Ultimately, bipolar digital logic lost the battle for hegemony in the digital design world for exactly the reasons that haunted the vacuum tube approach: the large power consumption per gate puts an upper limit on the number of gates that can be reliably integrated on a single die,

[1] An intriguing overview of the evolution of digital integrated circuits can be found in [Murphy93]. (Most of the data in this overview has been extracted from this reference). It is accompanied by some of the historically ground-breaking publications in the domain of digital ICs.

package, housing, or box. Although attempts were made to develop high integration density, low-power bipolar families (such as I^2L—*Integrated Injection Logic* [Hart72]), the MOS digital integrated circuit approach eventually held sway.

The basic principle behind the MOSFET transistor (originally called IGFET) was proposed in a patent by J. Lilienfeld (Canada) as early as 1925, and, independently, by O. Heil in England in 1935. Insufficient knowledge of the materials and gate stability problems, however, delayed the practical usability of the device for a long time. Once these were solved, MOS digital integrated circuits started to take off in full in the early 1970s. Remarkably, the first MOS logic gates introduced were of the CMOS variety [Wanlass63], and this trend continued until the late 1960s. The complexity of the manufacturing process delayed the full exploitation of these devices for two more decades. Instead, the first practical MOS integrated circuits were implemented in PMOS-only logic and were used in applications such as calculators. The second age of the digital integrated circuit revolution was inaugurated with the introduction of the first microprocessors by Intel in 1972 (the 4004) [Faggin72] and 1974 (the 8080) [Shima74]. These processors were implemented in NMOS-only logic, which has the advantage of higher speed over the PMOS logic. Simultaneously, MOS technology enabled the realization of the first high-density semiconductor memories. For instance, the first 4Kbit MOS memory was introduced in 1970 [Hoff70].

These events were at the start of a truly astounding evolution towards ever higher integration densities and speed performances, a revolution that currently is still in full swing. The road to the current levels of integration has not been without hindrances, however. In the late 1970s, NMOS-only logic started to suffer from the same plague that made high-density bipolar logic unattractive or infeasible: power consumption. This realization, combined with progress in manufacturing technology, finally tilted the balance towards the CMOS technology, and this is where it remains today. Interestingly enough, power consumption concerns are rapidly becoming dominant in CMOS design as well, and this time there does not seem to be a new technology around the corner to alleviate the problem.

Although the large majority of the current integrated circuits are implemented in the MOS technology, other technologies come into play when very high performance is at stake. An example of this is the BiCMOS technology that combines bipolar and MOS devices on the same die. When even higher performance is necessary, other technologies emerge such as silicon-germanium, and even superconducting technologies. These technologies only play a very small role in the overall digital integrated circuit design scene. With the ever increasing performance of CMOS, this role is bound to be reduced further with time—hence, the focus of this textbook is on CMOS only.

1.2 Issues in Digital Integrated Circuit Design

Integration density and performance of integrated circuits have gone through an astounding revolution in the last two decades. In the 1960s, Gordon Moore, then with Fairchild Corporation and later cofounder of Intel, predicted that the number of transistors that can be integrated on a

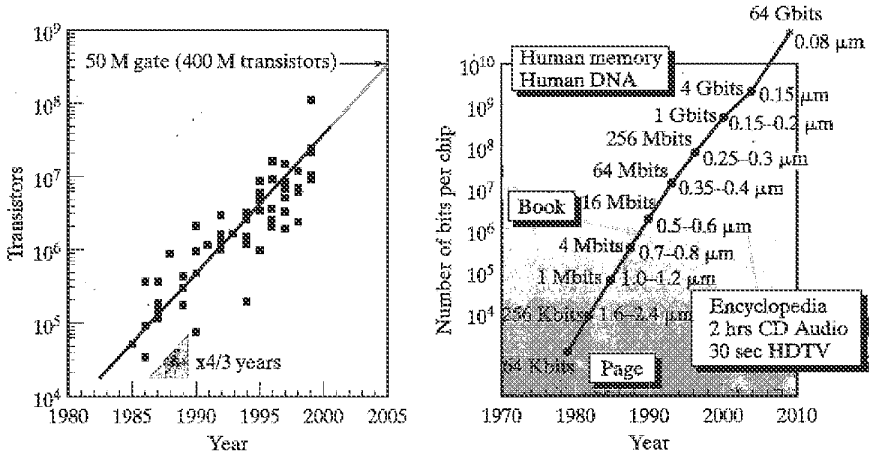


Figure 1-2 Evolution of integration complexity of logic ICs and memories as a function of time.

single die would grow exponentially with time. This prediction, later called *Moore's law*, has proven to be amazingly visionary [Moore65]. Its validity is best illustrated with the aid of a set of graphs. Figure 1-2 plots the integration density of both logic ICs and memory as a function of time. As can be observed, integration complexity doubles approximately every one to two years. As a result, memory density has increased by more than a thousandfold since 1970.

An intriguing case study is offered by the microprocessor. From its inception in the early 1970s, the microprocessor has grown in performance and complexity at a steady and predictable pace. The transistor counts for a number of landmark designs that are collected in Figure 1-3.

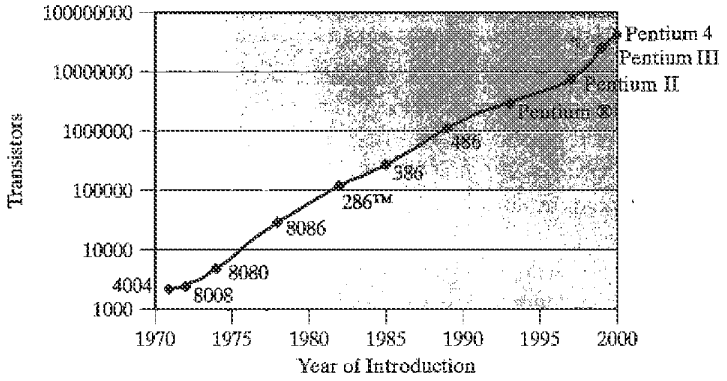


Figure 1-3 Historical evolution of microprocessor transistor count (from [Intel01]).

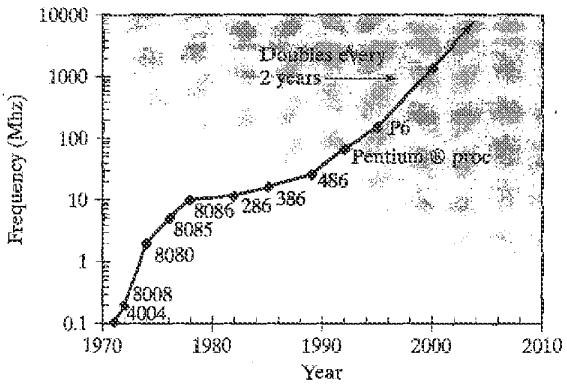


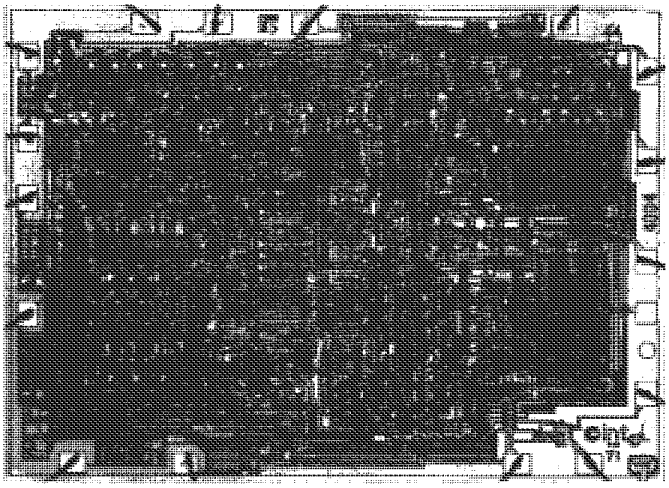
Figure 1-4 Microprocessor performance trends at the beginning of the 21st century. (Courtesy of Intel.)

The million-transistor/chip barrier was crossed in the late 1980s. Clock frequencies double every three years in the past decade and have reached into the GHz range. This is illustrated in Figure 1-4, which plots the microprocessor trends in terms of performance at the beginning of the 21st century. An important observation is that, as of now, these trends have not shown any signs of a slowdown.

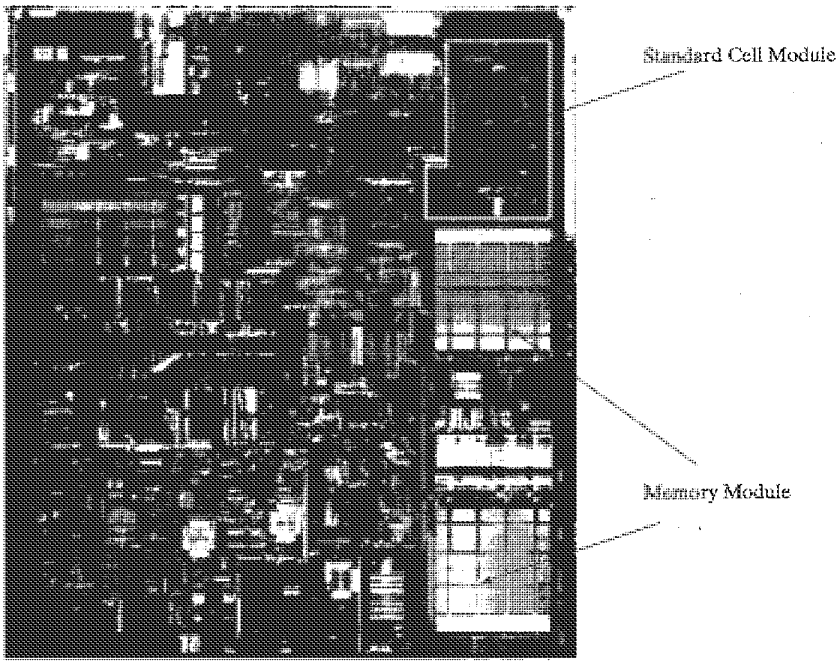
It should not surprise the reader that this revolution has had a profound impact on how digital circuits are designed. Early designs were truly handcrafted. Every transistor was laid out and optimized individually and carefully fitted into its environment. This is adequately illustrated in Figure 1-5a, which shows the design of the Intel 4004 microprocessor. Obviously, this approach is not appropriate when more than a million devices have to be created and assembled. With the rapid evolution of the design technology, time to market is one of the crucial factors in the ultimate success of a component.

As a result, designers have increasingly adhered to rigid design methodologies and strategies that are more amenable to design automation. The impact of this approach is apparent from the layout of one of the later Intel microprocessors, the Pentium® 4, shown in Figure 1-5b. Instead of the individualized approach of the earlier designs, a circuit is constructed in a hierarchical way: a processor is a collection of modules, each of which consists of a number of cells on its own. Cells are reused as much as possible to reduce the design effort and to enhance the chances for a first-time-right implementation. The fact that this hierarchical approach is at all possible is the key ingredient for the success of digital circuit design and also explains why, for instance, very large-scale analog design has never caught on.

The obvious next question is why such an approach is feasible in the digital world and not (or to a lesser degree) in analog designs. The crucial concept here, and the most important one in dealing with the complexity issue, is *abstraction*. At each design level, the internal details of a complex module can be abstracted away and replaced by a *black-box view* or *model*. This model contains virtually all the information needed to deal with the block at the next level of hierarchy.



(a) The 4004 microprocessor



(b) The Pentium ® 4 microprocessor

Figure 1-5 Comparing the design methodologies of the Intel 4004 (1971) and Pentium® 4 (2000) microprocessors (reprinted with permission from Intel).

For instance, once a designer has implemented a multiplier module, its performance can be defined very accurately and can be captured in a model. In general, the performance of this multiplier is only marginally influenced by the way it is utilized in a larger system. For all purposes, therefore, it can be considered a black box with known characteristics. As there exists no compelling need for the system designer to look inside this box, design complexity is substantially reduced. The impact of this *divide-and-conquer* approach is dramatic. Instead of having to deal with a myriad of elements, the designer has to consider only a handful of components, each of which are characterized in performance and cost by a small number of parameters.

This is analogous to a software designer using a library of software routines such as input/output drivers. Someone writing a large program does not bother to look inside those library routines. The only thing he cares about is the intended result of calling one of those modules. Imagine what writing software programs would be like if you had to fetch every bit individually from the disk and ensure its correctness instead of relying on handy "file open" and "get string" operators.

Abstraction levels typically used in digital circuit design are, in order of increasing abstraction, the device, circuit, gate, functional module (e.g., adder) and system levels (e.g., processor), as illustrated in Figure 1-6. A semiconductor device is an entity with a very complex behavior. No circuit designer will ever seriously consider the solid-state physics equations governing the behavior of the device when designing a digital gate. Instead, he will use a simplified model that adequately describes the input/output behavior of the transistor. For instance, an AND gate is adequately described by its Boolean expression ($Z = A.B$), its bounding box, the position of the input and output terminals, and the delay between the inputs and the output.

This design philosophy has been the enabler for the emergence of elaborate *computer-aided design* (CAD) frameworks for digital integrated circuits—without it the current design complexity would not have been achievable. Design tools include simulation at the various complexity levels, design verification, layout generation, and design synthesis. An overview of these tools and design methodologies is given in Chapter 8.

Furthermore, to avoid the redesign and reverification of frequently used cells, such as basic gates and arithmetic and memory modules, designers most often resort to *cell libraries*. These libraries not only contain the layouts, but also provide complete documentation and characterization of the behavior of the cells. The use of cell libraries is, for instance, apparent in the layout of the Pentium® 4 processor (Figure 1-5b). The integer and floating-point unit, just to name a few, contain large sections designed using one particular cell-based approach, called *standard cell*. Logic gates are placed in rows of cells of equal height and interconnected using routing channels. The layout of such a block can be generated automatically given that a library of cells is available.

The preceding analysis demonstrates that design automation and modular design practices have effectively addressed some of the complexity issues incurred in contemporary digital design. This leads to the following pertinent question: If design automation solves all our design problems, why should we be concerned with digital circuit design at all? Will the next-generation

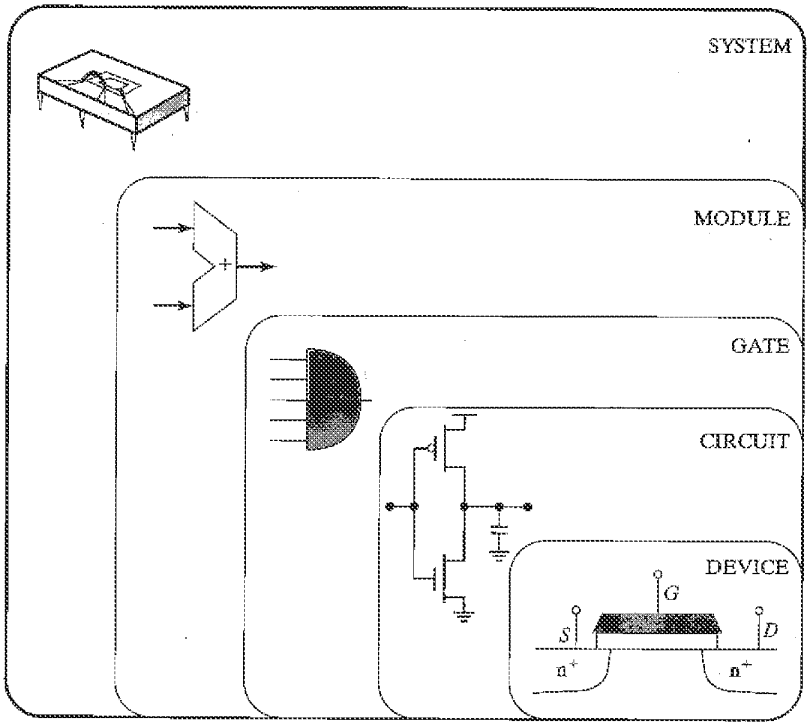


Figure 1-6 Design abstraction levels in digital circuits.

digital designer ever have to worry about transistors or parasitics, or is the smallest design entity he will ever consider be the gate and the module?

The truth is that the reality is more complex, and various reasons exist as to why an insight into digital circuits and their intricacies will still be an important asset for a long time to come:

- First, someone still has to *design and implement* the module libraries. Semiconductor technologies continue to advance from year to year. Until one has developed a foolproof approach towards "porting" a cell from one technology to another, each change in technology—which happens approximately every two years—requires a redesign of the library.
- Creating an adequate *model* of a cell or module requires an in-depth understanding of its internal operation. For instance, to identify the dominant performance parameters of a given design, one has to recognize the critical timing path first.
- The library-based approach works fine when the design constraints (speed, cost, or power) are not stringent. This is the case for a large number of *application-specific designs*, where

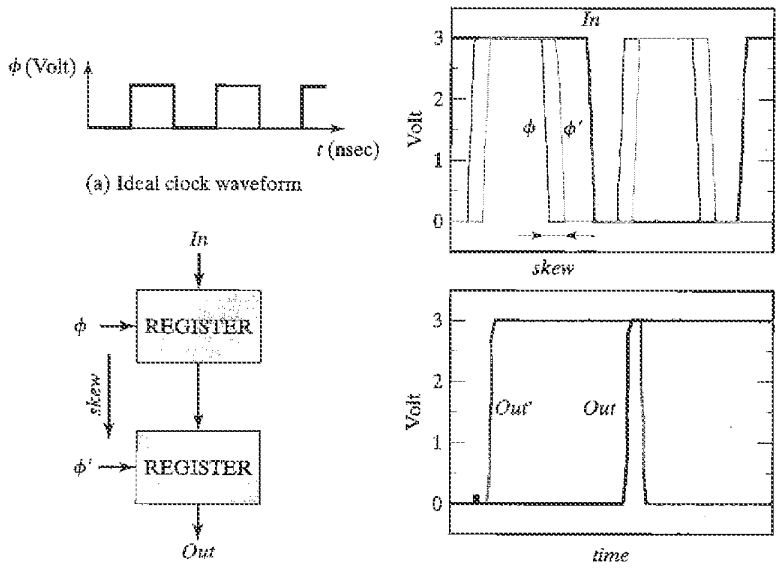
the main goal is to provide a more integrated system solution, and performance requirements are easily within the capabilities of the technology. Unfortunately, for a large number of other products such as microprocessors, success hinges on high performance, and designers therefore tend to push technology to its limits. At that point, the hierarchical approach tends to become somewhat less attractive. To resort to our previous analogy to software methodologies, a programmer tends to "customize" software routines when execution speed is crucial; compilers—or design tools—are not yet to the level of what human sweat or ingenuity can deliver.

- Even more important is the observation that the abstraction-based approach is only correct to a certain degree. The performance of, for instance, an adder can be substantially influenced by the way it is connected to its environment. The interconnection wires themselves contribute to delay because they introduce parasitic capacitances, resistances, and even inductances. The impact of the *interconnect parasitics* is bound to increase in the years to come with the scaling of the technology.
- Scaling tends to emphasize some other deficiencies of the abstraction-based model. Some design entities tend to be *global or external*. Examples of global factors are the clock signals, used for synchronization in a digital design, and the supply lines. Increasing the size of a digital design has a profound effect on these global signals. For instance, connecting more cells to a supply line can cause a voltage drop over the wire, which, in turn, can slow down all the connected cells. Issues such as clock distribution, circuit synchronization, and supply-voltage distribution are becoming more and more critical. Coping with them requires a profound understanding of the intricacies of digital circuit design.
- Another impact of technology evolution is that *new design issues* and constraints tend to emerge over time. A typical example of this is the periodical reemergence of power dissipation as a constraining factor, as was already illustrated in the historical overview. Another example is the changing ratio between device and interconnect parasitics. To cope with these unforeseen factors, one must at least be able to model and analyze their impact, requiring once again a profound insight into circuit topology and behavior.
- Finally, when things can go wrong, they often do. A fabricated circuit does not always exhibit the exact waveforms one might expect from advance simulations. Deviations can be caused by variations in the fabrication process parameters, or by the inductance of the package, or by a badly modeled clock signal. *Troubleshooting* a design requires circuit expertise.

For all these reasons, it is our profound belief that an in-depth knowledge of digital circuit design techniques and approaches is an essential asset for a digital-system designer. Even though she might not have to deal with the details of the circuit on a daily basis, the understanding will help her cope with unexpected circumstances and determine the dominant effects when analyzing a design.

Example 1.1 Clocks Defy Hierarchy

To illustrate some of the issues raised in the preceding discussion, let us examine the impact of deficiencies in one of the most important global signals in a design, the *clock*. The function of the clock signal in a digital design is to order the multitude of events happening in the circuit. This task can be compared to the function of a traffic light that determines which cars are allowed to move. It also makes sure that all operations are completed before the next one starts—a traffic light should be green long enough to allow a car or a pedestrian to cross the road. Under ideal circumstances, the clock signal is a periodic step waveform with transitions synchronized throughout the designed circuit (Figure 1-7a). In light of our analogy, changes in the traffic lights should be synchronized to maximize throughput while avoiding accidents. The importance of the *clock alignment* concept is illustrated with the example of two cascaded registers, both operating on the rising edge of the clock ϕ (Figure 1-7b). Under normal operating conditions, the input *In* gets sampled into the first register on the rising edge of ϕ and appears at the output exactly one clock period later. This is confirmed by the simulations shown in Figure 1-7c (signal *Out*).



(a) Ideal clock waveform

(b) Two cascaded registers

(c) Simulated waveforms

Figure 1-7 Impact of clock misalignment.

Due to delays associated with routing the clock wires, it may happen that the clocks become misaligned with respect to each other. As a result, the registers are interpreting time indicated by the clock signal differently. Consider the case in which the clock signal

for the second register is delayed—or skewed—by a value δ. The rising edge of the delayed clock ϕ' will postpone the sampling of the input of the second register. If the time it takes to propagate the output of the first register to the input of the second register is smaller than the clock delay, the latter will sample the wrong value. This causes the output to change prematurely, as clearly illustrated in the simulation, where the signal *Out'* goes high at the first rising edge of ϕ' instead of the second one. In terms of our traffic analogy, cars leaving the first traffic light hit the cars at the next light that have not yet left.

Clock misalignment, or *clock skew*, is an important example of how global signals may influence the functioning of a hierarchically designed system. Clock skew is actually one of the most critical design problems facing the designers of large high-performance systems.

Example 1.2 Power Distribution Networks Defy Hierarchy

While the clock signal is one example of a global signal that crosses the chip hierarchy boundaries, the power distribution network represents another. A digital system requires a stable DC voltage to be supplied to the individual gates. To ensure proper operation, this voltage should be stable within a few hundred millivolts. The power distribution system has to provide this stable voltage in the presence of very large current variations. The resistive nature of the on-chip wires and the inductance of the IC package pins make this a difficult proposition. For example, the average DC current to be supplied to a 100 W-1V microprocessor equals 100 A! The peak current can easily be twice as large, and current demand can readily change from almost zero to this peak value over a short time—in the range of 1 nsec or less. This leads to a current variation of 100 GA/s, which is a truly astounding number.

Consider the problem of the resistance of power distribution wires. For a current of 100 A, a wire resistance of merely 1.25 mΩ leads to a 5% drop in supply voltage (for a 2.5 V supply). Making the wires wider reduces the resistance and thus the voltage drop. While this sizing of the power network is relatively simple in a flat design approach, it is a lot more complex in a hierarchical design. For example, consider the two blocks shown in Figure 1-8a [Saleh01]. If power distribution for Block A is examined in isolation, the additional loading due to the presence of Block B is not taken into account. If power is routed through Block A to Block B, a larger IR drop will occur in Block B, since power is also being consumed by Block A before it reaches Block B.

Since the total IR drop is based on the resistance seen from the pin to the block, one could route around the block and feed power to each block separately, as shown in Figure 1-8b. Ideally, the main trunks should be large enough to handle all the current flowing through separate branches. Although routing power this way is easier to control and maintain, it also requires more area to implement. The large metal trunks of power have to

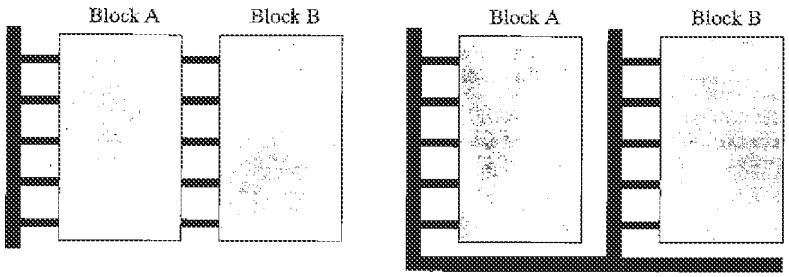


Figure 1-8 Power distribution network design.

be sized to handle all the current for each block. This requirement forces designers to set aside area for power busing that takes away from the available routing area.

As more and more blocks are added, the complex interactions between the blocks determine the actual voltage drops. For instance, it is not always easy to determine which way the current will flow when multiple parallel paths are available between the power source and the consuming gate. Also, currents into the different modules do rarely peak at the same time. All these considerations make the design of the power distribution a challenging job. It requires a design methodology approach that supersedes the artificial boundaries imposed by hierarchical design.

The purpose of this book is to provide *a bridge between the abstract vision of digital design and the underlying digital circuit and its peculiarities*. While starting from a solid understanding of the operation of electronic devices and an in-depth analysis of the nucleus of digital design—the inverter—we will gradually channel this knowledge into the design of more complex entities, such as complex gates, datapaths, registers, controllers, and memories. The persistent quest for a designer when designing each of the mentioned modules is to identify the dominant design parameters, to locate the section of the design he should focus his optimizations on, and to determine the specific properties that make the module under investigation (e.g., a memory) different from any others.

We also address other compelling (global) issues in modern digital circuit design such as *power dissipation, interconnect, timing,* and *synchronization*.

1.3 Quality Metrics of a Digital Design

This section defines a set of basic properties of a digital design. These properties help to quantify the quality of a design from different perspectives: cost, functionality, robustness, performance, and energy consumption. Which one of these metrics is most important depends upon the application. For instance, pure speed is a crucial property in a computer server. On the other hand, energy consumption is a dominant metric for hand heldmobile applications such as cell

phones. The introduced properties are relevant at all levels of the design hierarchy—system, chip, module, and gate. To ensure consistency in the definitions throughout the design hierarchy stack, we propose a bottom-up approach: We start with defining the basic quality metrics of a simple inverter, and gradually expand these to the more complex functions such as gate, module, and chip.

1.3.1 Cost of an Integrated Circuit

The total cost of any product can be separated into two components: the recurring expenses or the *variable cost*, and the nonrecurring expenses or the *fixed cost*.

Fixed Cost

The fixed cost is independent of the sales volume or the number of products sold. An important component of the fixed cost of an integrated circuit is the effort in time and manpower it takes to produce the design. This design cost is strongly influenced by the complexity of the design, the aggressiveness of the specifications, and the productivity of the designer. Advanced design methodologies that automate major parts of the design process can help to boost the latter. Bringing down the design cost in the presence of an ever-increasing IC complexity is one of the major challenges always facing the semiconductor industry.

Additionally, one has to account for the *indirect costs*, the company overhead that cannot be billed directly to one product. It includes the company's research and development (R&D) costs, manufacturing equipment, marketing and sales costs, and building infrastructure, among others.

Variable Cost

The variable cost accounts for the cost that is directly attributable to a manufactured product, and is hence proportional to the product volume. Variable costs include the costs of the parts used in the product, assembly costs, and testing costs. The total cost of an integrated circuit is

$$\text{cost per IC} = \text{variable cost per IC} + \left(\frac{\text{fixed cost}}{\text{volume}}\right) \tag{1.1}$$

The impact of the fixed cost is more pronounced for small-volume products. This helps explain why it makes sense to have large design teams working for several years on a hugely successful product such as a microprocessor.

While the cost of producing a single transistor has dropped exponentially over the past few decades, the basic variable-cost equation has not changed:

$$\text{variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}} \tag{1.2}$$

As will be discussed further in Chapter 2, the IC manufacturing process groups a number of identical circuits onto a single *wafer* (see Figure 1-9). Upon completion of the fabrication, the wafer is chopped into *dies*, which are then individually packaged after being *tested*. We will

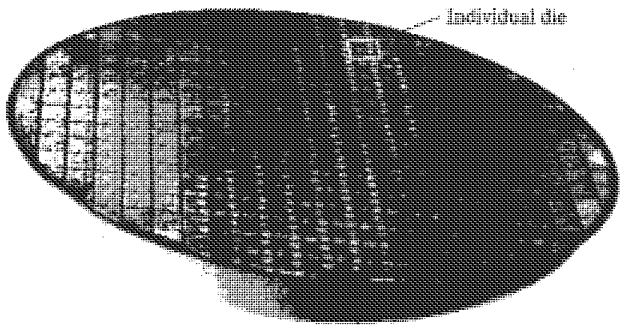


Figure 1-9 Finished wafer. Each square represents a die—in this case the AMD Duron™ microprocessor (reprinted with permission from AMD).

focus on the cost of the die in this discussion. The cost of packaging and testing is the topic of later chapters.

The die cost depends on the number of good dies on a wafer, and the percentage of those that are functional. The latter factor is called the *die yield*, given by

$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}} \tag{1.3}$$

The number of dies per wafer is, in essence, the area of the wafer divided by the die area. The actual situation is somewhat more complicated as wafers are round, and chips are square. Dies around the perimeter of the wafer are therefore lost. The size of the wafer has been steadily increasing over the years, yielding more dies per fabrication run. Equation (1.3) also presents the first indication that the cost of a circuit is dependent upon the chip area—increasing the chip area simply means that fewer dies fit on a wafer.

The actual relation between cost and area is more complex, and depends upon the die yield. Both the substrate material and the manufacturing process introduce faults that can cause a chip to fail. Assuming that the defects are randomly distributed over the wafer and that the yield is inversely proportional to the complexity of the fabrication process, we obtain the equation

$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha} \tag{1.4}$$

where α is a parameter that depends upon the complexity of the manufacturing process, and it is roughly proportional to the number of masks. A good estimate for today's complex CMOS processes is $\alpha = 3$. The defects per unit area is a measure of the material and process-induced faults. A value between 0.5 and 1 defects/cm^2 is typical these days, but depends strongly upon the maturity of the process.

Example 1.3 Die Yield

Assume a wafer size of 12 inches, a die size of 2.5 cm^2, 1 defects/cm^2, and $\alpha = 3$. Determine the die yield of this CMOS process run.

The number of dies per wafer can be estimated with the following expression, which takes into account the lost dies around the perimeter of the wafer:

$$\text{dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}$$

This means there are 252 (= 296 – 44) potentially operational dies for this particular example. The die yield can be computed with the aid of Eq. (1.4), and equals 16%! This means that, on average only 40 of the dies will be fully functional.

The bottom line is that the number of functional dies per wafer, and hence the cost per die, is a strong function of the die area. While the yield tends to be excellent for the smaller designs, it drops rapidly once a certain threshold is exceeded. Bearing in mind the equations derived previously and the typical parameter values, we can conclude that die costs are proportional to the fourth power of the area:

$$\text{cost of die} = f(\text{die area})^4 \tag{1.5}$$

The area is a function that is directly controllable by the designer(s), and it is the prime metric for cost. Small area is thus a desirable property for a digital gate. The smaller the gate, the higher the integration density and the smaller the die size. Smaller gates also tend to be faster and consume less energy—the total gate capacitance, which is one of the dominant performance parameters, often scales with the area.

The *number of transistors* in a gate is indicative of the expected implementation area but other parameters may have an impact. For instance, a complex interconnect pattern between the transistors can cause the wiring area to dominate. The *gate complexity*, as expressed by the number of transistors and the regularity of the interconnect structure, also has an impact on the design cost. Complex structures are more difficult to implement and tend to take more of the designer's valuable time. Simplicity and regularity is a precious property in cost-sensitive designs.

1.3.2 Functionality and Robustness

A prime requirement for a digital circuit is, obviously, that it performs the function it is designed for. The measured behavior of a manufactured circuit normally deviates from the expected response. One reason for this aberration is due to the variations in the manufacturing process. The dimensions and device parameters vary between runs or even on a single wafer or die. The electrical behavior of a circuit can be profoundly affected by those variations. The presence of disturbing noise sources on or off the chip is another source of deviations in circuit response.

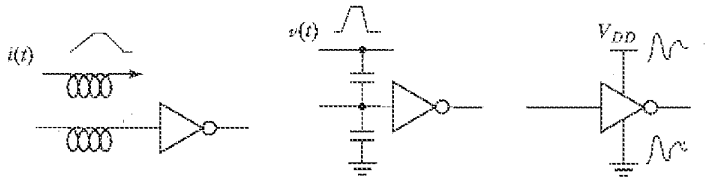


Figure 1-10 Noise sources in digital circuits.

The word *noise*, in the context of digital circuits, means *unwanted variations of voltages and currents at the logic nodes*. Noise signals can enter a circuit in many ways. Some examples of digital noise sources are depicted in Figure 1-10. For instance, two wires placed side by side in an integrated circuit form a coupling capacitor and a mutual inductance. Hence, a change in voltage or current on one of the wires can influence the signals on the neighboring wire. Noise on the power and ground rails of a gate also influences the signal levels in the gate.

Most noise in a digital system is internally generated, and the noise value is proportional to the signal swing. Capacitive and inductive cross talk, and the internally generated power supply noise are examples of such. Other noise sources such as input power supply noise are external to the system, and their value is not related to the signal levels. For these sources, the noise level is directly expressed in volts or amperes. Noise sources that are a function of the signal level are better expressed as a fraction or percentage of the signal level. Noise is a major concern in the engineering of digital circuits. How to cope with all these disturbances is one of the main challenges in the design of high-performance digital circuits and is a recurring topic in this book.

The steady-state parameters (also called the *static behavior*) of a gate measure how robust the circuit is with respect to both variations in the manufacturing process and noise disturbances. The definition and derivation of these parameters requires a prior understanding of how digital signals are represented in the world of electronic circuits.

Digital circuits (DC) perform operations on *logical* (or *Boolean*) variables. A logical variable x can only assume two discrete values:

$$x \in \{0,1\}$$

As an example, the inversion (i.e., the function that an inverter performs) implements the following compositional relationship between two Boolean variables x and y:

$$y = \bar{x}: \{x = 0 \Rightarrow y = 1; x = 1 \Rightarrow y = 0\} \tag{1.6}$$

A logical variable is, however, a mathematical abstraction. In a physical implementation, such a variable is represented by an electrical quantity. This is most often a node voltage that is not discrete, but can adopt a continuous range of values. This electrical voltage is turned into a discrete variable by associating *a nominal voltage level* with each logic state: $1 \Leftrightarrow V_{OH}$, $0 \Leftrightarrow V_{OL}$, where V_{OH} and V_{OL} represent the *high* and the *low* logic levels, respectively. Applying V_{OH}

to the input of an inverter yields V_{OL} at the output and vice versa. The difference between the two is called the *logic* or *signal swing* V_{sw}.

$$V_{OH} = \overline{(V_{OL})}$$
$$V_{OL} = \overline{(V_{OH})} \tag{1.7}$$

The Voltage-Transfer Characteristic

Assume now that a logical variable *in* serves as the input to an inverting gate that produces the variable *out*. The electrical function of a gate is best expressed by its *voltage-transfer characteristic* (VTC) (sometimes called the *DC transfer characteristic*), which plots the output voltage as a function of the input voltage $V_{out} = f(V_{in})$. An example of an inverter VTC is shown in Figure 1-11. The high and low nominal voltages, V_{OH} and V_{OL}, can readily be identified—$V_{OH} = f(V_{OL})$ and $V_{OL} = f(V_{OH})$. Another point of interest of the VTC is the *gate* or *switching threshold voltage* V_M (not to be confused with the threshold voltage of a transistor), that is defined as $V_M = f(V_M)$. V_M can also be found graphically at the intersection of the VTC curve and the line given by $V_{out} = V_{in}$. The gate threshold voltage presents the midpoint of the switching characteristics, which is obtained when the output of a gate is short-circuited to the input. This point will prove to be of particular interest when studying circuits with feedback (also called *sequential circuits*).

Even if an ideal nominal value is applied at the input of a gate, the output signal often deviates from the expected nominal value. These deviations can be caused by noise or by the loading on the output of the gate (i.e., by the number of gates connected to the output signal). Figure 1-12a illustrates how a logic level is represented in reality by a range of acceptable voltages, separated by a region of uncertainty, rather than by nominal levels alone. The regions of acceptable high and low voltages are delimited by the V_{IH} and V_{IL} voltage levels, respectively. By definition, these represent the points where the gain ($= dV_{out} / dV_{in}$) of the VTC equals –1 as shown in Figure 1-12b. The region between V_{IH} and V_{IL} is called the *undefined region*

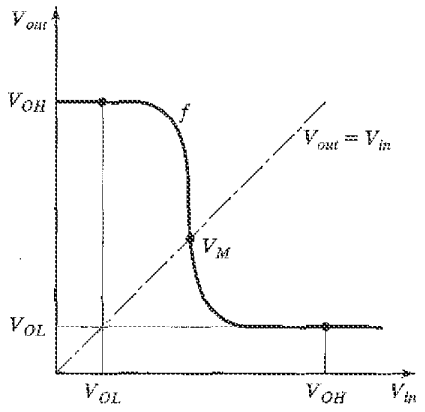
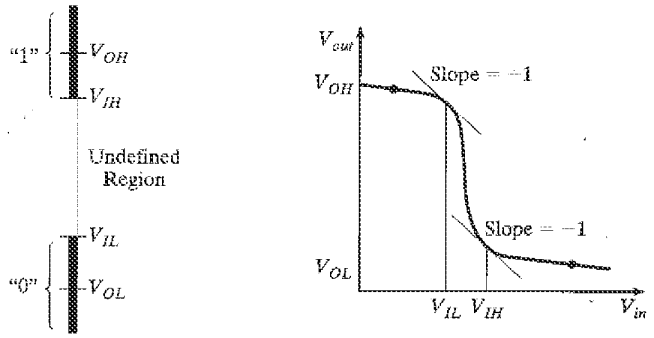


Figure 1-11 Inverter voltage-transfer characteristic.



(a) Relationship between voltage and logic levels (b) Definition of V_{IH} and V_{IL}

Figure 1-12 Mapping logic levels to the voltage domain.

(sometimes also called the *transition width*, or *TW*). Steady-state signals should avoid this region if proper circuit operation is to be ensured.

Noise Margins

For a gate to be robust and insensitive to noise disturbances, it is essential that the "0" and "1" intervals be as large as possible. A measure of the sensitivity of a gate to noise is given by the noise margins NM_L (*noise margin low*) and NM_H (*noise margin high*), which quantize the size of the legal "0" and "1," respectively, and set a fixed maximum threshold on the noise value:

$$\begin{aligned} NM_L &= V_{IL} - V_{OL} \\ NM_H &= V_{OH} - V_{IH} \end{aligned} \tag{1.8}$$

The noise margins represent the levels of noise that can be sustained when gates are cascaded as illustrated in Figure 1-13. It is obvious that the margins should be larger than 0 for a digital circuit to be functional, and by preference, they should be as large as possible.

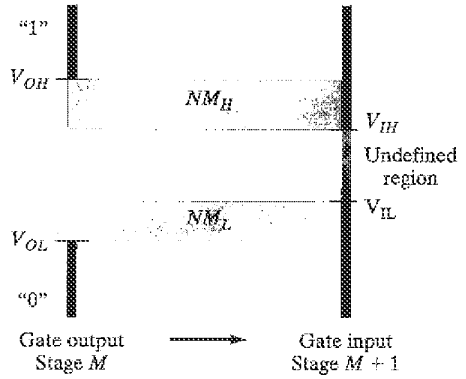
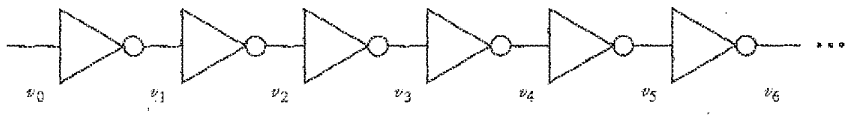
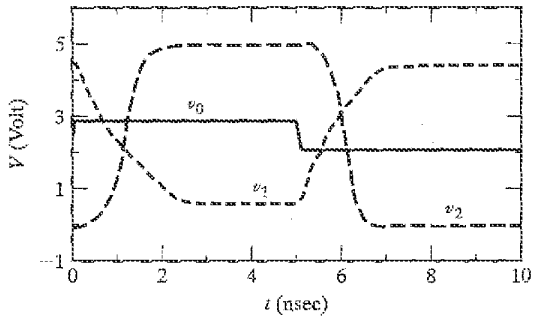


Figure 1-13 Cascaded inverter gates: definition of noise margins.



(a) A chain of inverters



(b) Simulated response of chain of MOS inverters

Figure 1-14 The regenerative property.

Regenerative Property

A large noise margin is desirable, but it is not the only requirement. Assume that a signal is disturbed by noise and differs from the nominal voltage levels. As long as the signal is within the noise margins, the gate that follows continues to function correctly, although its output voltage varies from the nominal one. This deviation is added to the noise injected at the output node and passed to the next gate. The effect of different noise sources may accumulate and eventually force a signal level into the undefined region. Fortunately, this does not happen if the gate possesses the *regenerative property*, which ensures that a disturbed signal gradually converges back to one of the nominal voltage levels after passing through a number of logical stages. This property can be understood as follows:

An input voltage v_{in} ($v_{in} \in$ "0") is applied to a chain of N inverters (Figure 1-14a). Assuming that the number of inverters in the chain is even, the output voltage v_{out} ($N \rightarrow \infty$) will equal V_{OL} if and only if the inverter possesses the regenerative property. Similarly, when an input voltage v_{in} ($v_{in} \in$ "1") is applied to the inverter chain, the output voltage will approach the nominal value V_{OH}

Example 1.4 Regenerative Property

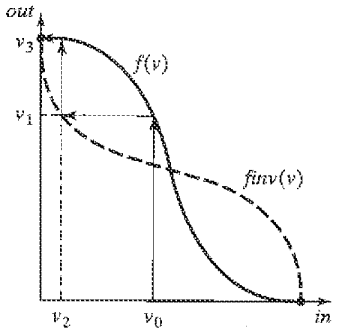
The concept of regeneration is illustrated in Figure 1-14b, which plots the simulated transient response of a chain of CMOS inverters. The input signal to the chain is a step wave-

form with a degraded amplitude, which could be caused by noise. Instead of swinging from rail to rail, v_0 only extends between 2.1 and 2.9 V. From the simulation, it can be observed that this deviation rapidly disappears while progressing through the chain; v_1, for instance, extends from 0.6 V to 4.45 V. Even further, v_2 already swings between the nominal V_{OL} and V_{OH}. The inverter used in this example clearly possesses the regenerative property.

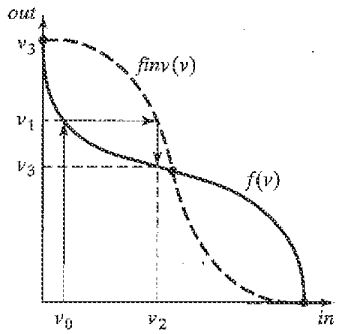
The conditions under which a gate is regenerative can be intuitively derived by analyzing a simple case study. Figure 1-15a plots the VTC of an inverter $V_{out} = f(V_{in})$ as well as its inverse function *finv*(), which reverts the function of the x- and y-axis and is defined as

$$in = f(out) \Rightarrow in = finv(out) \tag{1.9}$$

Assume that a voltage v_0, deviating from the nominal voltages, is applied to the first inverter in the chain. The output voltage of this inverter equals $v_1 = f(v_0)$ and is applied to the next inverter. Graphically, this corresponds to $v_1 = finv(v_2)$. The signal voltage gradually converges to the nominal signal after a number of inverter stages, as indicated by the arrows. In Figure 1-15b the signal does not converge to any of the nominal voltage levels, but to an intermediate voltage level. Hence, the characteristic is nonregenerative. The difference between the two cases is due to the gain characteristics of the gates. To be regenerative, the VTC should have a transient region (or undefined region) with a gain *greater than* 1 in absolute value, bordered by the two legal zones, where the gain should be *less than* 1. Such a gate has two stable operating points. This clarifies the definition of the V_{IH} and the V_{IL} levels that form the boundaries between the legal and the transient zones.



(a) Regenerative gate



(b) Nonregenerative gate

Figure 1-15 Conditions for regeneration.

Noise Immunity

While the noise margin is a meaningful means for measuring the robustness of a circuit against noise, it is not sufficient. It expresses the capability of a circuit to "overpower" a noise source. *Noise immunity*, on the other hand, expresses the ability of the system to process and transmit information correctly in the presence of noise [Dally98]. Many digital circuits with low noise margins have very good noise immunity because they *reject a noise source* rather than overpower it. These circuits have the property that only a small fraction of a potentially damaging noise source is coupled to the important circuit nodes. More precisely, the transfer function between noise source and signal node is far less than 1. Circuits that do not posses this property are *susceptible* to noise.

To study the noise immunity of a gate, we have to construct a noise budget that allocates the power budget to the various noise sources. As discussed earlier, the noise sources can be divided into the following types of sources:

- those that are *proportional* to the signal swing V_{sw}. The impact on the signal node is expressed as $g\ V_{sw}$; and
- those that are *fixed*. The impact on the signal node equals $f\ V_{Nf}$, with V_{nf} the amplitude of the noise source, and f the transfer function *from noise* to signal node.

We assume, for the sake of simplicity, that the noise margin equals half the signal swing (for both H and L). To operate correctly, the noise margin has to be larger than the sum of the coupled noise values:

$$V_{NM} = \frac{V_{sw}}{2} \geq \sum_i f_i V_{Nfi} + \sum_j g_j V_{sw} \tag{1.10}$$

Given a set of noise sources, we can derive the minimum signal swing necessary for the system to be operational:

$$V_{sw} \geq \frac{2\sum_i f_i V_{Nfi}}{1 - 2\sum_j g_j} \tag{1.11}$$

This makes it clear that the signal swing (and the noise margin) has to be large enough to overpower the impact of the fixed sources ($f\ V_{Nf}$). On the other hand, the sensitivity to internal sources depends primarily upon the noise suppressing capabilities of the gate, this is the proportionality or gain factors g_j. In the presence of large gain factors, increasing the signal swing does not do any good to suppress noise, as the noise increases proportionally. In later chapters, we will discuss some differential logic families that suppress most of the internal noise, and thus can get away with very small noise margins and signal swings.

Directivity

The directivity property requires a gate to be *unidirectional*—that is, changes in an output level should not appear at any unchanging input of the same circuit. Otherwise, an output-signal transition reflects to the gate inputs as a noise signal, affecting the signal integrity.

In real gate implementations, full directivity can never be achieved. Some feedback of changes in output levels to the inputs cannot be avoided. Capacitive coupling between inputs and outputs is a typical example of such a feedback. It is important to minimize these changes so that they do not affect the logic levels of the input signals.

Fan-In and Fan-Out

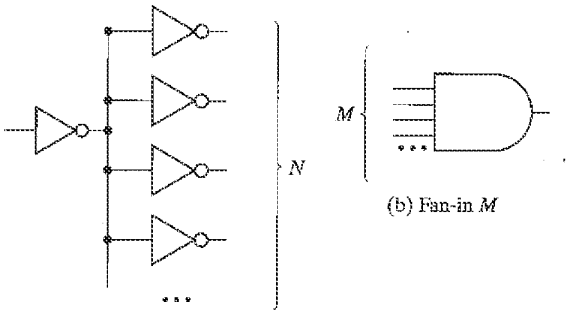
The *fan-out* denotes *the number of load gates N that are connected to the output of the driving gate* (see Figure 1-16). Increasing the fan-out of a gate can affect its logic output levels. From the world of analog amplifiers, we know that this effect is minimized by making the input resistance of the load gates as large as possible (minimizing the input currents) and by keeping the output resistance of the driving gate small (reducing the effects of load currents on the output voltage). When the fan-out is large, the added load can deteriorate the dynamic performance of the driving gate. For these reasons, many generic and library components define a *maximum fan-out* to guarantee that the static and dynamic performance of the element meet specification.

The *fan-in* of a gate is defined as the *number of inputs* to the gate (see Figure 1-16b). Gates with large fan-in tend to be more complex, which often results in inferior static and dynamic properties.

The Ideal Digital Gate

Based on these observations, we can define the *ideal* digital gate from a static perspective. The ideal inverter model is important because it gives us a metric by which we can judge the quality of actual implementations.

Its VTC is shown in Figure 1-17 and has the following properties: infinite gain in the transition region, and gate threshold located in the middle of the logic swing, with high and low



(a) Fan-out N (b) Fan-in M

Figure 1-16 Definition of fan-out and fan-in of a digital gate.

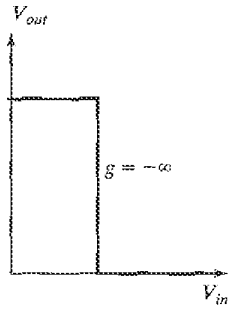


Figure 1-17 Ideal voltage-transfer characteristic.

noise margins equal to half the swing. The input and output impedances of the ideal gate are infinity and zero, respectively (i.e., the gate has unlimited fan-out). While this ideal VTC is unfortunately impossible in real designs, some implementations, such as the static CMOS inverter, come close.

Example 1.5 Voltage-Transfer Characteristic

Figure 1-18 shows an example of a voltage-transfer characteristic of an actual, but outdated, gate structure. The values of the dc parameters are derived from inspection of the graph.

$$V_{OH} = 3.5\text{ V}; \qquad V_{OL} = 0.45\text{ V}$$
$$V_{IH} = 2.35\text{ V}; \qquad V_{IL} = 0.66\text{ V}$$
$$V_M = 1.64\text{ V}$$
$$NM_H = 1.15\text{ V}; \qquad NM_L = 0.21\text{ V}$$

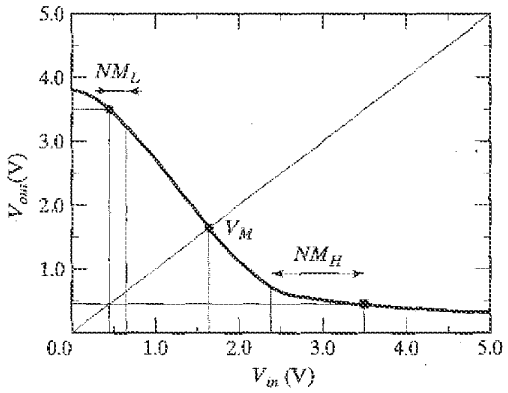


Figure 1-18 Voltage-transfer characteristic of an NMOS inverter of the 1970s.

The observed transfer characteristic, obviously, is far from ideal: it is asymmetrical, has a very low value for NM_L, and the voltage swing of 3.05 V is substantially below the maximum obtainable value of 5 V (which is the value of the supply voltage for this design).

1.3.3 Performance

From a system designer's perspective, the performance of a digital circuit expresses its computational ability. For instance, a microprocessor often is characterized by the number of instructions it can execute per second. This performance metric depends both on the architecture of the processor—for instance, the number of instructions it can execute in parallel—and the actual design of logic circuitry. While the former is crucially important, it is not the focus of this text. The reader may refer to the many excellent books on this topic [for instance, Hennessy02]. When focusing on the pure design, performance is most often expressed by the duration of the clock period (*clock cycle time*), or its rate (*clock frequency*). The minimum value of the clock period for a given technology and design is set by a number of factors such as the time it takes for the signals to propagate through the logic, the time it takes to get the data in and out of the registers, and the uncertainty of the clock arrival times. Each of these topics will be discussed in detail in this book. The performance of an individual gate lies at the core of the whole performance analysis, however.

The *propagation delay* t_p of a gate defines how quickly it responds to a change at its input(s). It expresses *the delay experienced by a signal when passing through a gate*. It is measured between the 50% transition points of the input and output waveforms, as shown in Figure 1-19 for

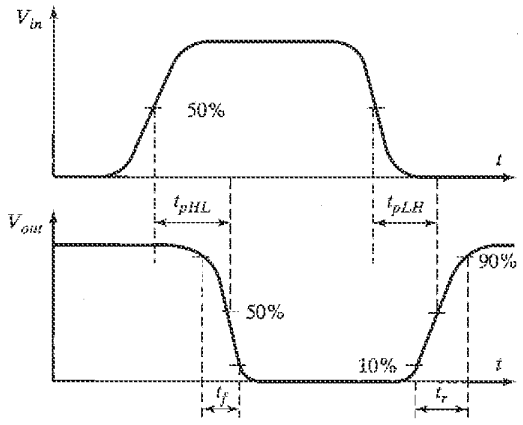


Figure 1-19 Definition of propagation delays and rise and fall times.

an inverting gate.[2] Because a gate displays different response times for rising or falling input waveforms, two definitions of the propagation delay are necessary. The t_{pLH} defines the response time of the gate for a *low-to-high* (or positive) output transition, while t_{pHL} refers to a *high-to-low* (or negative) transition. The propagation delay t_p is defined as the average of the two:

$$t_p = \frac{t_{pLH} + t_{pHL}}{2} \tag{1.12}$$

CAUTION: Observe that the propagation delay t_p, in contrast to t_{pLH} and t_{pHL}, is an artificial gate quality metric, and has no physical meaning per se. It is mostly used to compare different semiconductor technologies, circuit, or logic design styles.

The propagation delay is not only a function of the circuit technology and topology, but depends upon other factors as well. Most importantly, the delay is a function of the *slopes* of the input and output signals of the gate. To quantify these properties, we introduce the *rise and fall times*, t_r and t_f, which are metrics that apply to individual signal waveforms rather than to gates (see Figure 1-19), and they express how fast a signal transits between the different levels. The uncertainty over when a transition actually starts or ends is avoided by defining the rise and fall times between the 10% and 90% points of the waveforms, as shown in the figure. The rise/fall time of a signal is largely determined by the strength of the driving gate, and the load presented to it.

When comparing the performance of gates implemented in different technologies or circuit styles, it is important not to confuse the picture by including parameters such as load factors, fan-in, and fan-out. A uniform way of measuring the t_p of a gate so that technologies can be judged on an equal footing is desirable. The de facto standard circuit for delay measurement is the *ring oscillator*, which consists of an odd number of inverters connected in a circular chain (see Figure 1-20.) Due to the odd number of inversions, this circuit does not have a stable operating point and oscillates. The period T of the oscillation is determined by the propagation time of a signal transition through the complete chain, or $T = 2 \times t_p \times N$ with N the number of inverters in the chain. The factor 2 results from the observation that a full cycle requires both a low-to-high and a high-to-low transition. Note that this equation is only valid for $2Nt_p >> t_f + t_r$. If this condition is not met, the circuit might not oscillate—one "wave" of signals propagating through the ring will overlap with a successor and eventually dampen the oscillation. Typically, a ring oscillator needs at least five stages to be operational.

[2]The 50% definition is inspired by the assumption that the switching threshold V_M is typically located in the middle of the logic swing.

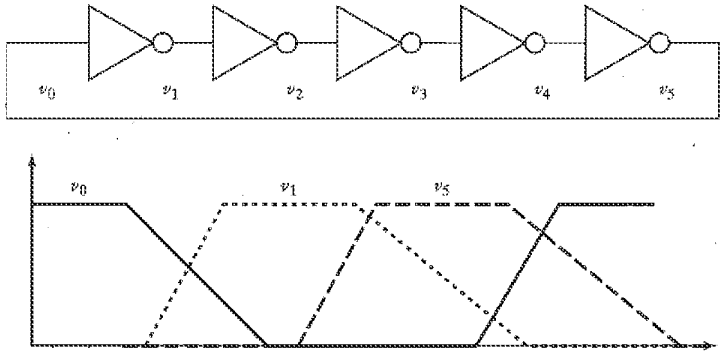


Figure 1-20 Ring oscillator circuit for propagation-delay measurement.

CAUTION: We must be extremely careful with results obtained from ring oscillator measurements. A t_p of 20 ps by no means implies that a circuit built with those gates will operate at 50 GHz. The oscillator results are primarily useful for quantifying the differences between various manufacturing technologies and gate topologies. The oscillator is an idealized circuit in which each gate has a fan-in and fan-out of exactly 1 and parasitic loads are minimal. In more realistic digital circuits, fan-ins and fan-outs are higher, and interconnect delays are non-negligible. The gate functionality is also substantially more complex than a simple invert operation. As a result, the achievable clock frequency, on average, is 50 to 100 times slower than the frequency obtained from ring oscillator measurements. This is an average observation; carefully optimized designs might approach use ideal frequency more closely.

Example 1.6 Propagation Delay of First-Order *RC* Network

Digital circuits are often modeled as first-order *RC* networks of the type shown in Figure 1-21. The propagation delay of such a network is thus of considerable interest.

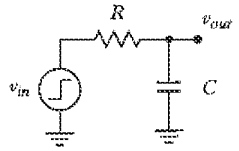


Figure 1-21 First-order *RC* network.

When applying a step input (with v_{in} going from 0 to V), the transient response of this circuit is known to be an exponential function, and is given by the following expression (where $\tau = RC$, the time constant of the network):

$$v_{out}(t) = (1 - e^{-t/\tau})\, V \tag{1.13}$$

The time to reach the 50% point is easily computed as $t = \ln(2)\tau = 0.69\tau$. Similarly, it takes $t = \ln(9)\tau = 2.2\tau$ to get to the 90% point. It is worth memorizing these numbers because they are used extensively throughout this text.

1.3.4 Power and Energy Consumption

The power consumption of a design determines how much energy is consumed per operation, and how much heat the circuit dissipates. These factors influence a great number of critical design decisions, such as the power supply capacity, the battery lifetime, supply line sizing, packaging and cooling requirements. Therefore, power dissipation is an important property of a design that affects feasibility, cost, and reliability. In the world of high-performance computing, power consumption limits, dictated by the chip package and the heat removal system, determine the number of circuits that can be integrated onto a single chip, and how fast they are allowed to switch. With the increasing popularity of mobile and distributed computation, energy limitations put a firm restriction on the number of computations that can be performed given a minimum time between battery recharges.

Depending on the design problem at hand, different dissipation measures must be considered. For instance, the peak power P_{peak} is important when studying supply line sizing. When addressing cooling or battery requirements, one is predominantly interested in the average power dissipation P_{av}. The measures are defined as

$$P_{peak} = i_{peak} V_{supply} = max[p(t)]$$
$$P_{av} = \frac{1}{T}\int_0^T p(t)dt = \frac{V_{supply}}{T}\int_0^T i_{supply}(t)dt \tag{1.14}$$

where $p(t)$ is the instantaneous power, i_{supply} is the current being drawn from the supply voltage V_{supply} over the interval $t \in [0,T]$, and i_{peak} is the maximum value of i_{supply} over that interval.

The dissipation can further be decomposed into *static* and *dynamic* components. The latter occurs only during transients, when the gate is switching. It is attributed to the charging of capacitors and temporary current paths between the supply rails; therefore it is proportional to the switching frequency: *the higher the number of switching events, the greater the dynamic power consumption.* On the other hand, the static component is present even when no switching occurs and is caused by static conductive paths between the supply rails or by leakage currents. It is always present, even when the circuit is in standby. Minimization of this consumption source is a worthwhile goal.

The propagation delay and the power consumption of a gate are related—the propagation delay is mostly determined by the speed at which a given amount of energy can be stored on the gate capacitors. The faster the energy transfer (or the higher the power consumption), the faster the gate. For a given technology and gate topology, the product of power consumption and propagation delay is generally a constant. This product is called the *power-delay product* (or PDP),

and can be considered as a quality measure for a switching device. The PDP is simply the *energy* consumed by the gate *per switching event*. The ring oscillator is again the circuit of choice for measuring the PDP of a logic family.

An ideal gate is one that is fast and consumes little energy. The *energy-delay* product (E-D) is a combined metric that brings those two elements together, and is often used as the ultimate quality metric. Thus, it should be clear that the E-D is equivalent to *power-delay*^{2}.

Example 1.7 Energy Dissipation of First-Order *RC* Network

Let us again consider the first-order *RC* network (shown in Figure 1-21). When applying a step input (with V_{in} going from 0 to V), an amount of energy is provided by the signal source to the network. The total energy delivered by the source (from the start of the transition to the end) can be readily computed:

$$E_{in} = \int_0^\infty i_{in}(t)v_{in}(t)dt = V\int_0^\infty C\frac{dv_{out}}{dt}dt = (CV)\int_0^V dv_{out} = CV^2 \tag{1.15}$$

It is interesting to observe that the energy needed to charge a capacitor from 0 to V volts with a step input is a function of the size of the voltage step and the capacitance, but is independent of the value of the resistor. We can also compute how much of the delivered energy gets stored on the capacitor at the end of the transition.

$$E_C = \int_0^\infty i_C(t)v_{out}(t)dt = \int_0^\infty C\frac{dv_{out}}{dt}v_{out}dt = C\int_0^V v_{out}dv_{out} = \frac{CV^2}{2} \tag{1.16}$$

This is exactly half of the energy delivered by the source. For those who wonder what happened to the other half—a simple analysis shows that an equivalent amount gets dissipated as heat in the resistor during the transaction. It is left to the reader to demonstrate that during the discharge phase (for a step from V to 0), the energy originally stored on the capacitor gets dissipated in the resistor as well, and then turned into heat.

1.4 Summary

In this introductory chapter, we learned about the history and the trends in digital circuit design. We also introduced the important quality metrics used to evaluate the quality of a design: cost, functionality, robustness, performance, and energy/power dissipation.

1.5 To Probe Further

The design of digital integrated circuits has been the topic of many textbooks and monographs. To help the reader find more information on some selected topics, an extensive list of references

follows. The state-of-the-art developments in the area of digital design are generally reported in technical journals or conference proceedings, the most important of which are listed.

Journals and Proceedings

IEEE Journal of Solid-State Circuits
IEICE Transactions on Electronics (Japan)
Proceedings of The International Solid-State and Circuits Conference (ISSCC)
Proceedings of the VLSI Circuits Symposium
Proceedings of the Custom Integrated Circuits Conference (CICC)
European Solid-State Circuits Conference (ESSCIRC)

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Exercises

Please refer to **http://bwrc.eecs.berkeley.edu/IcBook** for up-to-date problem sets and exercises. By making the exercises electronically available rather than in print, we can provide a dynamic environment that tracks the rapid evolution of today's digital integrated circuit design technology.

CHAPTER

4

The Wire

Determining and quantifying interconnect parameters

Introducing circuit models for interconnect wires

Detailed wire models for SPICE

Technology scaling and its impact on interconnect

4.1 Introduction

4.2 A First Glance

4.3 Interconnect Parameters—Capacitance, Resistance, and Inductance
- 4.3.1 Capacitance
- 4.3.2 Resistance
- 4.3.3 Inductance

4.4 Electrical Wire Models
- 4.4.1 The Ideal Wire
- 4.4.2 The Lumped Model
- 4.4.3 The Lumped *RC* Model
- 4.4.4 The Distributed *rc* Line
- 4.4.5 The Transmission Line

4.5 SPICE Wire Models
- 4.5.1 Distributed rc Lines in SPICE
- 4.5.2 Transmission Line Models in SPICE
- 4.5.3 Perspective: A Look into the Future

4.6 Summary

4.7 To Probe Further

4.1 Introduction

Throughout most of the history of integrated circuits, on-chip interconnect wires were almost like second class citizens, only considered in special cases or when performing high-precision analysis. With the introduction of deep submicron semiconductor technologies, this picture has undergone rapid changes. The parasitic effects introduced by the wires display a scaling behavior that differs from the active devices such as transistors, and they tend to gain in importance as device dimensions are reduced and circuit speed is increased. In fact, they start to dominate some of the relevant metrics of digital integrated circuits such as speed, energy consumption, and reliability. This situation is aggravated by the fact that improvements in technology make the production of ever larger die sizes economically feasible, which results in an increase in the average length of an interconnect wire and in the associated parasitic effects. A careful and in-depth analysis of the role and behavior of the interconnect wire in a semiconductor technology is, therefore, not only desirable, but essential.

4.2 A First Glance

The designer of an electronic circuit has multiple choices in realizing the interconnections between the various devices that make up the circuit. State-of-the-art processes offer multiple layers of aluminum or copper, and at least one layer of polysilicon. Even the heavily doped n^+ or p^+ diffusion layers typically used for the realization of source and drain regions can be employed for wiring purposes. These wires appear in the schematic diagrams of electronic circuits as simple lines with no apparent impact on the circuit performance. From our discussion of the integrated circuit manufacturing process, it should be clear that this picture is too simplistic, and that the wiring of today's integrated circuits forms a complex geometry that introduces capacitive, resistive, and inductive parasitics. All three have multiple effects on the circuit's behavior:

1. They all cause an increase in propagation delay, or, equivalently, a drop in performance.
2. They all have an impact on the energy dissipation and the power distribution.
3. They all cause the introduction of extra noise sources, which affect the reliability of the circuit.

A designer can decide to play it safe and include all these parasitic effects in her analysis and design optimization process. This conservative approach is not very constructive, however, and most often it is not even feasible. First of all, a "complete" model is dauntingly complex and is only applicable to very small topologies. Hence, it is totally useless for today's integrated circuits, with their millions of circuit nodes. Furthermore, this approach has the disadvantage of "not seeing the forest for the trees," so to speak. The circuit behavior at a given circuit node is only determined by a few dominant parameters. Bringing all possible effects to bear may obscure the picture and turn the optimization and design process into a "trial-and-error" operation, rather than an enlightened and focused search.

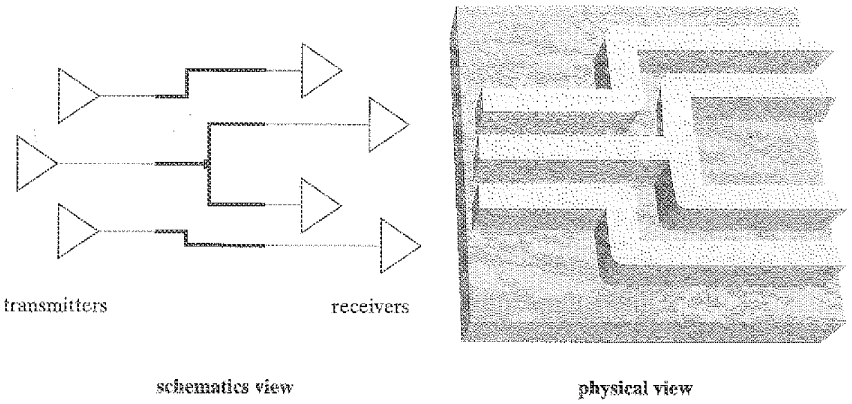


Figure 4-1 Schematic and physical views of wiring of bus network. The latter shows only a limited area (as indicated by the emphasis in the schematics).

Thus, it is important for the designer to have a clear insight into the parasitic wiring effects, their relative importance, and their models. This is best illustrated with a simple example, as shown in Figure 4-1. Each wire in a bus network connects a transmitter (or transmitters) to a set of receivers and is implemented as a chain of wire segments of various lengths and geometries. Assume that all segments are implemented on a single interconnect layer and isolated from the silicon substrate and from each other by a layer of dielectric material. (Be aware that the reality may be far more complex.)

A full-fledged circuit model, that takes into account the parasitic capacitance, resistance, and the inductance of the interconnections is shown in Figure 4-2a. Observe that these extra circuit elements are not located in a single physical point, but are distributed over the length of the wire. This is necessary when the length of the wire becomes significantly greater than its width. In addition, interwire parasitics are present, creating coupling effects between the different bus signals that were not present in the original schematics.

Analyzing the behavior of this schematic, which only models a small part of the circuit, is slow and cumbersome. Fortunately, substantial simplifications often can be made, including the following:

- Inductive effects can be ignored if the resistance of the wire is substantial enough—this is the case for long aluminum wires with a small cross section, for example, or if the rise and fall times of the applied signals are slow.
- When the wires are short, the cross section of the wire is large, or the interconnect material used has a low resistivity, a capacitance-only model can be used (see Figure 4-2b).
- Finally, when the separation between neighboring wires is large, or when the wires only run together for a short distance, interwire capacitance can be ignored, and all the parasitic capacitance can be modeled as capacitance to ground.

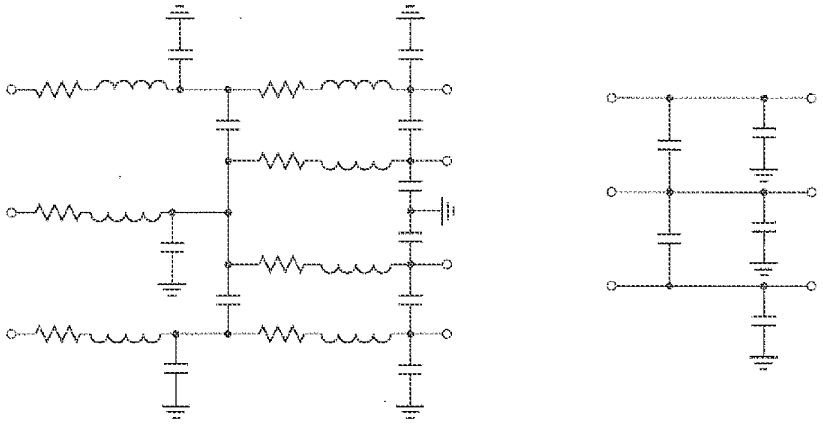


Figure 4-2 Wire models for the circuit of Figure 4-1. Model (a) considers most of the wire parasitics (with the exception of interwire resistance and mutual inductance), while model (b) only considers capacitance.

Obviously, the latter cases are the easiest to model, analyze, and optimize. The experienced designer knows to differentiate between dominant and secondary effects. The goal of this chapter is to present the basic techniques of estimating the values of the various interconnect parameters, simple models to evaluate their impact, and a set of rules of thumb for deciding when and where a particular model or effect should be considered.

4.3 Interconnect Parameters—Capacitance, Resistance, and Inductance

4.3.1 Capacitance

An accurate modeling of the wire capacitance(s) in a state-of-the-art integrated circuit is a nontrivial task, and even today it is the subject of advanced research. The task is further complicated by the fact that the interconnect structure of contemporary integrated circuits is three-dimensional, as was clearly demonstrated in the integrated-circuit cross section of Figure 2-8. The capacitance of such a wire is a function of its shape, its environment, its distance to the substrate, and the distance to surrounding wires. Rather than getting lost in complex equations and models, a designer typically will use an advanced extraction tool to get precise values of the interconnect capacitances of a completed layout. Most semiconductor manufacturers also provide empirical data for the various capacitance contributions, as measured from a number of test dies. Yet, some simple, first-order models come in handy to provide a basic understanding of the nature of interconnect capacitance and its parameters, and of how wire capacitance will evolve with future technologies.

Consider first a simple rectangular wire placed above the semiconductor substrate, as shown in Figure 4-3. If the width of the wire is substantially larger than the thickness of the

CHAPTER

6

Designing Combinational Logic Gates in CMOS

In-depth discussion of logic families in CMOS—static and dynamic, pass-transistor, nonratioed and ratioed logic

Optimizing a logic gate for area, speed, energy, or robustness

Low-power and high-performance circuit-design techniques

6.1 Introduction
6.2 Static CMOS Design
  6.2.1 Complementary CMOS
  6.2.2 Ratioed Logic
  6.2.3 Pass-Transistor Logic
6.3 Dynamic CMOS Design
  6.3.1 Dynamic Logic: Basic Principles
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  6.4.1 How to Choose a Logic Style?
  6.4.2 Designing Logic for Reduced Supply Voltages
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6.1 Introduction

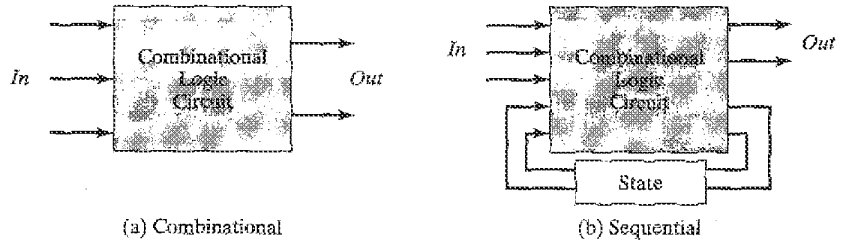
The design considerations for a simple inverter circuit were presented in the previous chapter. We now extend this discussion to address the synthesis of arbitrary digital gates, such as NOR, NAND, and XOR. The focus is on *combinational logic* or *nonregenerative* circuits—that is, circuits having the property that at any point in time, the output of the circuit is related to its current input signals by some Boolean expression (assuming that the transients through the logic gates have settled). No intentional connection from outputs back to inputs is present.

This is in contrast to another class of circuits, known as *sequential* or *regenerative*, for which the output is not only a function of the current input data, but also of previous values of the input signals (see Figure 6-1). This can be accomplished by connecting one or more outputs intentionally back to some inputs. Consequently, the circuit "remembers" past events and has a sense of *history*. A sequential circuit includes a combinational logic portion and a module that holds the state. Example circuits are registers, counters, oscillators, and memory. Sequential circuits are the topic of the next chapter.

There are numerous circuit styles to implement a given logic function. As with the inverter, the common design metrics by which a gate is evaluated are area, speed, energy, and power. Depending on the application, the emphasis will be on different metrics. For example, the switching speed of digital circuits is the primary metric in a high-performance processor, while in a battery operated circuit, it is energy dissipation. Recently, power dissipation also has become an important concern and considerable emphasis is placed on understanding the sources of power and approaches to dealing with power. In addition to these metrics, robustness to noise and reliability are also very important considerations. We will see that certain logic styles can significantly improve performance, but they usually are more sensitive to noise.

6.2 Static CMOS Design

The most widely used logic style is static complementary CMOS. The static CMOS style is really an extension of the static CMOS inverter to multiple inputs. To review, the primary advantage of the CMOS structure is robustness (i.e., low sensitivity to noise), good performance, and low power consumption with no static power dissipation. Most of those properties are carried over to large fan-in logic gates implemented using a similar circuit topology.



(a) Combinational (b) Sequential

Figure 6-1 High-level classification of logic circuits.

The complementary CMOS circuit style falls under a broad class of logic circuits called *static* circuits in which **at every point in time, each gate output is connected to either V_{DD} or V_{SS} via a low-resistance path**. Also, the outputs of the gates assume at all times the value of the Boolean function implemented by the circuit (ignoring, the transient effects during switching periods). This is in contrast to the *dynamic* circuit class, which relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes. The latter approach has the advantage that the resulting gate is simpler and faster. Its design and operation are, however, more involved and prone to failure because of increased sensitivity to noise.

In this section, we sequentially address the design of various static circuit flavors, including complementary CMOS, ratioed logic (pseudo-NMOS and DCVSL), and pass-transistor logic. We also deal with issues of scaling to lower power supply voltages and threshold voltages.

6.2.1 Complementary CMOS

Concept

A static CMOS gate is a combination of two networks—the *pull-up network* (PUN) and the *pull-down* network (PDN), as shown in Figure 6-2. The figure shows a generic N-input logic gate where all inputs are distributed to both the pull-up and pull-down networks. The function of the PUN is to provide a connection between the output and V_{DD} anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output to V_{SS} when the output of the logic gate is meant to be 0. The PUN and PDN networks are constructed in a mutually exclusive fashion such that *one and only one* of the networks is conducting in steady state. In this way, once the transients have settled, a path always exists between V_{DD} and the output F for a high output ("one"), or between V_{SS} and F for a low output ("zero"). This is equivalent to stating that the output node is always a *low-impedance* node in steady state.

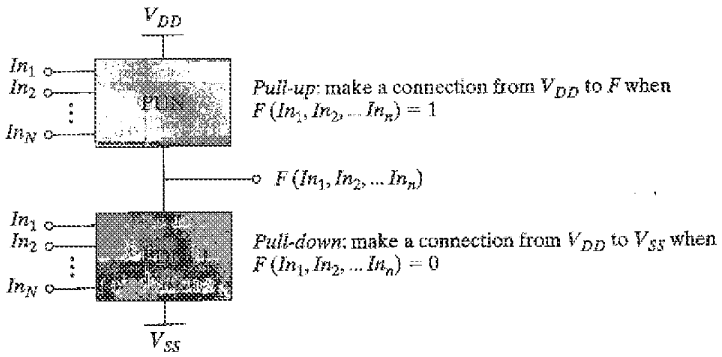
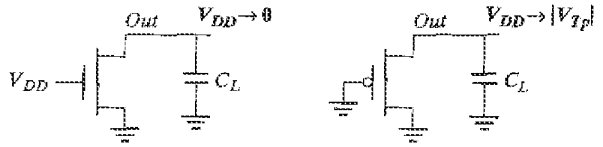


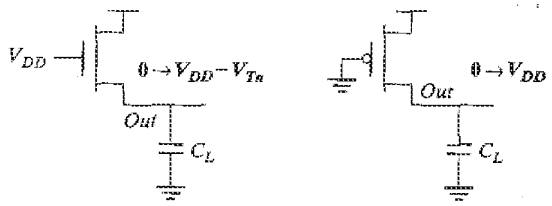
Figure 6-2 Complementary logic gate as a combination of a PUN (pull-up network) and a PDN (pull-down network).

In constructing the PDN and PUN networks, the designer should keep the following observations in mind:

- A transistor can be thought of as a switch controlled by its gate signal. An NMOS switch is *on* when the controlling signal is high and is *off* when the controlling signal is low. A PMOS transistor acts as an inverse switch that is *on* when the controlling signal is low and *off* when the controlling signal is high.
- The PDN is constructed using NMOS devices, while PMOS transistors are used in the PUN. The primary reason for this choice is that NMOS transistors produce "strong zeros," and PMOS devices generate "strong ones." To illustrate this, consider the examples shown in Figure 6-3. In Figure 6-3a, the output capacitance is initially charged to V_{DD}. Two possible discharge scenarios are shown. An NMOS device pulls the output all the way down to GND, while a PMOS lowers the output no further than $|V_{Tp}|$—the PMOS turns *off* at that point and stops contributing discharge current. NMOS transistors are thus the preferred devices in the PDN. Similarly, two alternative approaches to charging up a capacitor are shown in Figure 6-3b, with the output initially at GND. A PMOS switch succeeds in charging the output all the way to V_{DD}, while the NMOS device fails to raise the output above $V_{DD} - V_{Tn}$. This explains why PMOS transistors are preferentially used in a PUN.
- A set of rules can be derived to construct logic functions (see Figure 6-4). NMOS devices connected in series correspond to an AND function. With all the inputs high, the series combination conducts and the value at one end of the chain is transferred to the other end. Similarly, NMOS transistors connected in parallel represent an OR function. A conducting path exists between the output and input terminal if at least one of the inputs is high. Using similar arguments, construction rules for PMOS networks can be formulated. A series con-



(a) Pulling down a node by using NMOS and PMOS switches



(b) Pulling down a node by using NMOS and PMOS switches

Figure 6-3 Simple examples illustrate why an NMOS should be used as a pull-down, and a PMOS should be used as a pull-up device.

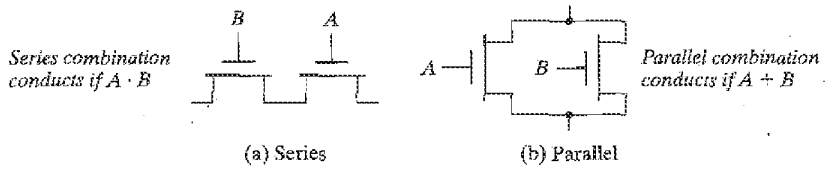


Figure 6-4 NMOS logic rules—series devices implement an AND, and parallel devices implement an OR.

nection of PMOS conducts if both inputs are low, representing a NOR function ($\overline{A} \cdot \overline{B} = \overline{A + B}$), while PMOS transistors in parallel implement a NAND ($\overline{A} + \overline{B} = \overline{A \cdot B}$).

- Using De Morgan's theorems ($\overline{A + B} = \overline{A} \cdot \overline{B}$ and $\overline{A \cdot B} = \overline{A} + \overline{B}$), it can be shown that the pull-up and pull-down networks of a complementary CMOS structure are *dual* networks. This means that a parallel connection of transistors in the pull-up network corresponds to a series connection of the corresponding devices in the pull-down network, and vice versa. Therefore, to construct a CMOS gate, one of the networks (e.g., PDN) is implemented using combinations of series and parallel devices. The other network (i.e., PUN) is obtained using the duality principle by walking the hierarchy, replacing series subnets with parallel subnets, and parallel subnets with series subnets. The complete CMOS gate is constructed by combining the PDN with the PUN.
- The complementary gate is naturally *inverting*, implementing only functions such as NAND, NOR, and XNOR. The realization of a noninverting Boolean function (such as AND OR, or XOR) in a single stage is not possible, and requires the addition of an extra inverter stage.
- The number of transistors required to implement an N-input logic gate is $2N$.

Example 6.1 Two-Input NAND Gate

Figure 6-5 shows a two-input NAND gate ($F = \overline{A \cdot B}$). The PDN network consists of two NMOS devices in series that conduct when both A and B are high. The PUN is the dual

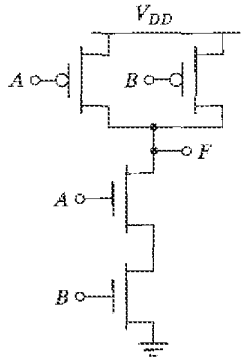


Figure 6-5 Two-input NAND gate in complementary static CMOS style.

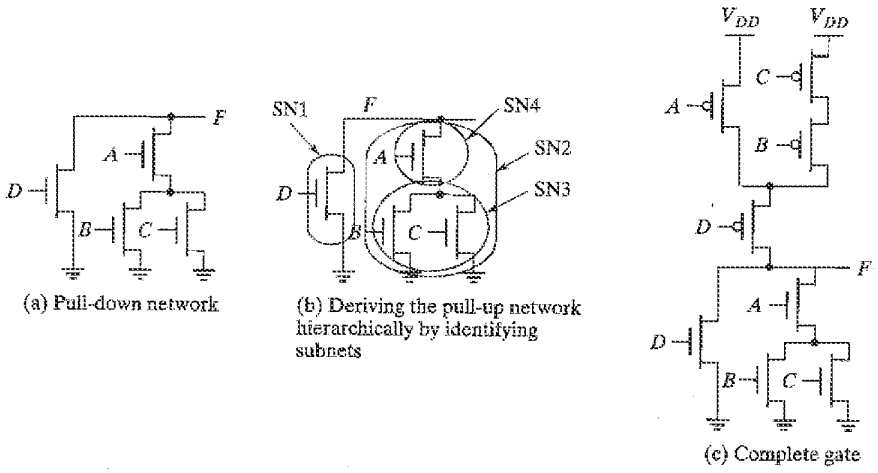
network, and it consists of two parallel PMOS transistors. This means that F is 1 if $A = 0$ or $B = 0$, which is equivalent to $F = \overline{A \cdot B}$. The truth table for the simple two input NAND gate is given in Table 6-1. It can be verified that the output F is always connected to either V_{DD} or GND, but never to both at the same time.

Table 6-1 Truth Table for two-input NAND.

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Example 6.2 Synthesis of Complex CMOS Gate

Using complementary CMOS logic, consider the synthesis of a complex CMOS gate whose function is $F = \overline{D + A \cdot (B + C)}$. The first step in the synthesis of the logic gate is to derive the pull-down network as shown in Figure 6-6a by using the fact that NMOS devices in series implements the AND function and parallel device implements the OR function. The next step is to use duality to derive the PUN in a hierarchical fashion. The PDN network is broken into smaller networks (i.e., subset of the PDN) called subnets that simplify the derivation of the PUN. In Figure 6-6b, the subnets (SN) for the pull-down net-



(a) Pull-down network

(b) Deriving the pull-up network hierarchically by identifying subnets

(c) Complete gate

Figure 6-6 Complex complementary CMOS gate.

work are identified. At the top level, SN1 and SN2 are in parallel, so that in the dual network they will be in series. Since SN1 consists of a single transistor, it maps directly to the pull-up network. On the other hand, we need to sequentially apply the duality rules to SN2. Inside SN2, we have SN3 and SN4 in series, so in the PUN they will appear in parallel. Finally, inside SN3, the devices are in parallel, so they appear in series in the PUN. The complete gate is shown in Figure 6-6c. The reader can verify that for every possible input combination, there always exists a path to either V_{DD} or GND.

Static Properties of Complementary CMOS Gates

Complementary CMOS gates inherit all the nice properties of the basic CMOS inverter. They exhibit rail-to-rail swing with $V_{OH} = V_{DD}$ and $V_{OL} = \text{GND}$. The circuits also have no static power dissipation, since the circuits are designed such that the pull-down and pull-up networks are mutually exclusive. The analysis of the DC voltage transfer characteristics and the noise margins is more complicated than for the inverter, as these parameters **depend upon the data input patterns** applied to gate.

Consider the static two-input NAND gate shown in Figure 6-7. Three possible input combinations switch the output of the gate from high to low: (a) $A = B = 0 \rightarrow 1$, (b) $A = 1, B = 0 \rightarrow 1$, and (c) $B = 1, A = 0 \rightarrow 1$. The resulting voltage transfer curves display significant differences. The large variation between case (a) and the others (b and c) is explained by the fact that in the former case, both transistors in the pull-up network are on simultaneously for $A = B = 0$, representing a strong pull-up. In the latter cases, only one of the pull-up devices is on. The VTC is shifted to the left as a result of the weaker PUN.

The difference between (b) and (c) results mainly from the state of the internal node *int* between the two NMOS devices. For the NMOS devices to turn on, both gate-to-source voltages

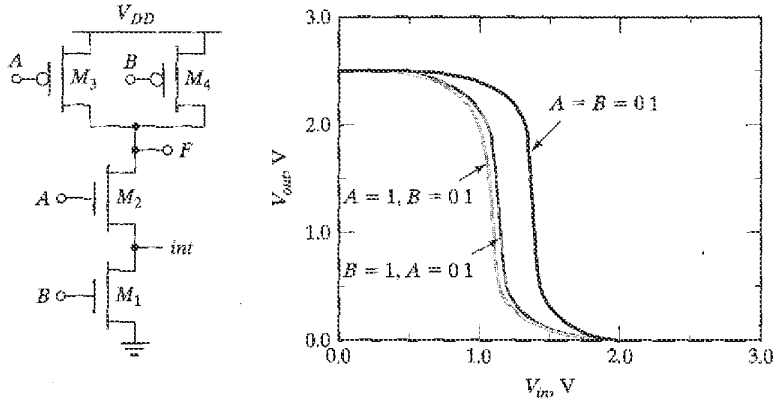


Figure 6-7 The VTC of a two-input NAND is data dependent. NMOS devices are 0.5 µm/0.25 µm while the PMOS devices are sized at 0.75 µm/0.25 µm.

must be above V_{Tn}, with $V_{GS2} = V_A - V_{DS1}$ and $V_{GS1} = V_B$. The threshold voltage of transistor M_2 will be higher than transistor M_1 due to the body effect. The threshold voltages of the two devices are given by the following equations:

$$V_{Tn2} = V_{Tn0} + \gamma(\sqrt{|2\phi_f| + V_{int}} - \sqrt{|2\phi_f|}) \tag{6.1}$$

$$V_{Tn1} = V_{Tn0} \tag{6.2}$$

For case (b), M_3 is turned *off*, and the gate voltage of M_2 is set to V_{DD}. To a first order, M_2 may be considered as a resistor in series with M_1. Since the drive on M_2 is large, this resistance is small and has only a small effect on the voltage transfer characteristics. In case (c), transistor M_3 acts as a resistor, causing a V_T increase in M_2 due to body effect. The overall impact is quite small, as seen from the plot.

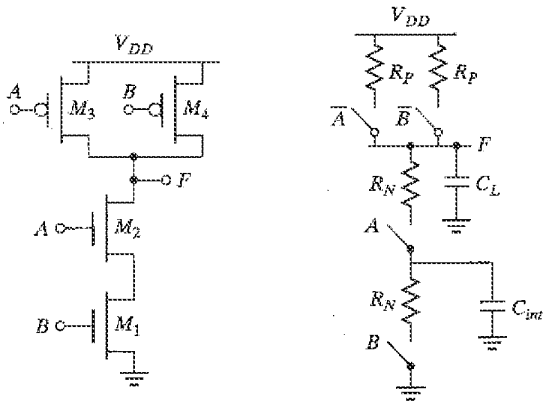
Design Consideration

The important point to take away from the preceding discussion is that the **noise margins are input/pattern dependent**. In Example 6.2, a glitch on only one of the two inputs has a larger chance of creating a false transition at the output than if the glitch were to occur on both inputs simultaneously. Therefore, the former condition has a lower low-noise margin. A common practice when characterizing gates such as NAND and NOR is to connect all the inputs together. Unfortunately, this does not represent the worst case static behavior; the data dependencies should be carefully modeled. ■

Propagation Delay of Complementary CMOS Gates

The computation of propagation delay proceeds in a fashion similar to the static inverter. For the purpose of delay analysis, each transistor is modeled as a resistor in series with an ideal switch. The value of the resistance is dependent on the power supply voltage and an equivalent large signal resistance, scaled by the ratio of device width over length, must be used. The logic is transformed into an equivalent *RC* network that includes the effect of internal node capacitances. Figure 6-8 shows the two-input NAND gate and its equivalent *RC* switch level model. Note that the internal node capacitance C_{int}—attributable to the source/drain regions and the gate overlap capacitance of M_2 and M_1—is included here. While complicating the analysis, the capacitance of the internal nodes can have quite an impact in some networks such as large fan-in gates. In a first pass, we ignore the effect of the internal capacitance.

A simple analysis of the model shows that, similarly to the noise margins, **the propagation delay depends on the input patterns**. Consider, for instance, the low-to-high transition. Three possible input scenarios can be identified for charging the output to V_{DD}. If both inputs are driven low, the two PMOS devices are on. The delay in this case is $0.69 \times (R_p/2) \times C_L$, since the two resistors are in parallel. This is not the worst case low-to-high transition, which occurs when only one device turns on, and is given by $0.69 \times R_p \times C_L$. For the pull-down path, the output is discharged only if both A and B are switched high, and the delay is given by $0.69 \times (2R_N) \times C_L$ to a first order. In other words, adding devices in series slows down the circuit, and devices must be made wider to avoid a performance penalty. When sizing the transistors in a gate with multiple inputs, we should pick the combination of inputs that triggers the worst case conditions.



(a) Two-input NAND (b) *RC*-equivalent model

Figure 6-8 Equivalent *RC* model for a two-input NAND gate.

For the NAND gate to have the same pull-down delay (t_{phl}) as a minimum-sized inverter, the NMOS devices in the PDN stack must be made twice as wide so that the equivalent resistance of the NAND pull-down network is the same as the inverter. The PMOS devices can remain unchanged.[1]

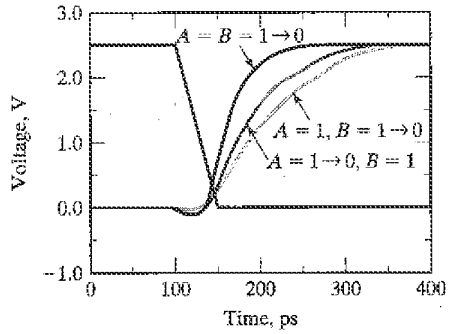
This first-order analysis assumes that the extra capacitance introduced by widening the transistors can be ignored. This is not a good assumption, in general, but it allows for a reasonable first cut at device sizing.

Example 6.3 Delay Dependence on Input Patterns

Consider the NAND gate of Figure 6-8a. Assume NMOS and PMOS devices of 0.5 µm/0.25 µm and 0.75 µm/0.25 µm, respectively. This sizing should result in approximately equal worst case rise and fall times (since the effective resistance of the pull-down is designed to be equal to the pull-up resistance).

Figure 6-9 shows the simulated low-to-high delay for different input patterns. As expected, the case in which both inputs transition go low ($A = B = 1 \rightarrow 0$) results in a smaller delay, compared with the case in which only one input is driven low. Notice that the worst case low-to-high delay depends upon which input (A or B) goes low. The reason for this involves the internal node capacitance of the pull-down stack (i.e., the source of M_2). For the case in which $B = 1$ and A transitions from $1 \rightarrow 0$, the pull-up PMOS device only has to charge up the output node capacitance (M_2 is turned off). On the other hand, for the case in which $A = 1$ and B transitions from $1 \rightarrow 0$, the pull-up PMOS device

[1] In deep-submicron processes, even larger increases in the width are needed due to the on-set of velocity saturation. For a two-input NAND, the NMOS transistors should be made 2.5 times as wide instead of 2 times.



Input Data Pattern	Delay (ps)
$A = B = 0 \rightarrow 1$	69
$A = 1, B = 0 \rightarrow 1$	62
$A = 0 \rightarrow 1, B = 1$	50
$A = B = 1 \rightarrow 0$	35
$A = 1, B = 1 \rightarrow 0$	76
$A = 1 \rightarrow 0, B = 1$	57

Figure 6-9 Example showing the delay dependence on input patterns.

has to charge up the sum of the output and the internal node capacitances, which slows down the transition.

The table in Figure 6-9 shows a compilation of various delays for this circuit. The first-order transistor sizing indeed provides approximately equal rise and fall delays. An important point to note is that the high-to-low propagation delay depends on the initial state of the internal nodes. For example, when both inputs transition from $0 \rightarrow 1$, it is important to establish the state of the internal node. The worst case happens when the internal node is initially charged up to $V_{DD} - V_{Tn}$, which can be ensured by pulsing the A input from $1 \rightarrow 0 \rightarrow 1$, while input B only makes the $0 \rightarrow 1$ transition. In this way, the internal node is initialized properly.

The important point to take away from this example is that estimation of delay can be fairly complex, and requires a careful consideration of internal node capacitances and data patterns. Care must be taken to model the worst case scenario in the simulations. A brute force approach that applies all possible input patterns may not always work, because it is important to consider the state of internal nodes.

The CMOS implementation of a NOR gate ($F = \overline{A + B}$) is shown in Figure 6-10. The output of this network is high, if and only if both inputs A and B are low. The worst case pull-down transition happens when only one of the NMOS devices turns on (i.e., if either A or B is high). Assume that the goal is to size the NOR gate such that it has approximately the same delay as an inverter with the following device sizes: NMOS of 0.5 µm/0.25 µm and PMOS of 1.5 µm/0.25 µm. Since the pull-down path in the worst case is a single device, the NMOS devices (M_1 and M_2) can have the same device widths as the NMOS device in the inverter. For the output to be pulled high, both devices must be turned on. Since the resistances add, the devices must be made two times larger compared with the PMOS in the inverter (i.e., M_3 and M_4 must have a size of 3 µm/0.25 µm). Since PMOS devices have a lower mobility relative to NMOS devices, stacking devices in series must be avoided as much as possible. A NAND implementation is clearly preferred over a NOR implementation for implementing generic logic.

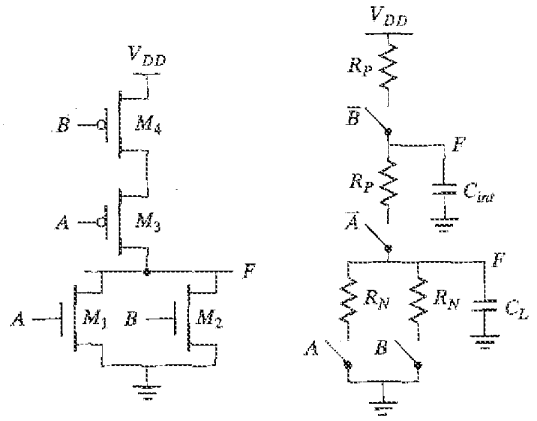


Figure 6-10 Sizing of a NOR gate.

Problem 6.1 Transistor Sizing in Complementary CMOS Gates

Determine the sizes of the transistors in Figure 6-6c such that it has approximately the same t_{plh} and t_{phl} as an inverter with the following sizes: NMOS: 0.5 μm/0.25 μm and a PMOS: 1.5 μm/0.25 μm.

So far in the analysis of propagation delay, we have ignored the effect of internal node capacitances. This is often a reasonable assumption for a first-order analysis. However, in more complex logic gates with large *fan-ins*, the internal node capacitances can become significant. Consider a four-input NAND gate, as drawn in Figure 6-11, which shows the equivalent *RC* model of the gate, including the internal node capacitances. The internal capacitances consist of the junction capacitances of the transistors, as well as the gate-to-source and gate-to-drain capacitances. The latter are turned into capacitances to ground using the Miller equivalence. The delay analysis for such a circuit involves solving distributed *RC* networks, a problem we already encountered when analyzing the delay of interconnect networks. Consider the pull-down delay of the circuit. The output is discharged when all inputs are driven high. The proper initial conditions must be placed on the internal nodes (i.e., the internal nodes must be charged to $V_{DD} - V_{TN}$) before the inputs are driven high.

The propagation delay can be computed by using the Elmore delay model:

$$t_{pHL} = 0.69(R_1 \cdot C_1 + (R_1 + R_2) \cdot C_2 + (R_1 + R_2 + R_3) \cdot C_2 + (R_1 + R_2 + R_3 + R_4) \cdot C_L) \quad (6.3)$$

Notice that the resistance of M_1 appears in all the terms, which makes this device especially important when attempting to minimize delay. Assuming that all NMOS devices have an equal size, Eq. (6.3) simplifies to

$$t_{pHL} = 0.69R_N(C_1 + 2 \cdot C_2 + 3 \cdot C_3 + 4 \cdot C_L) \quad (6.4)$$

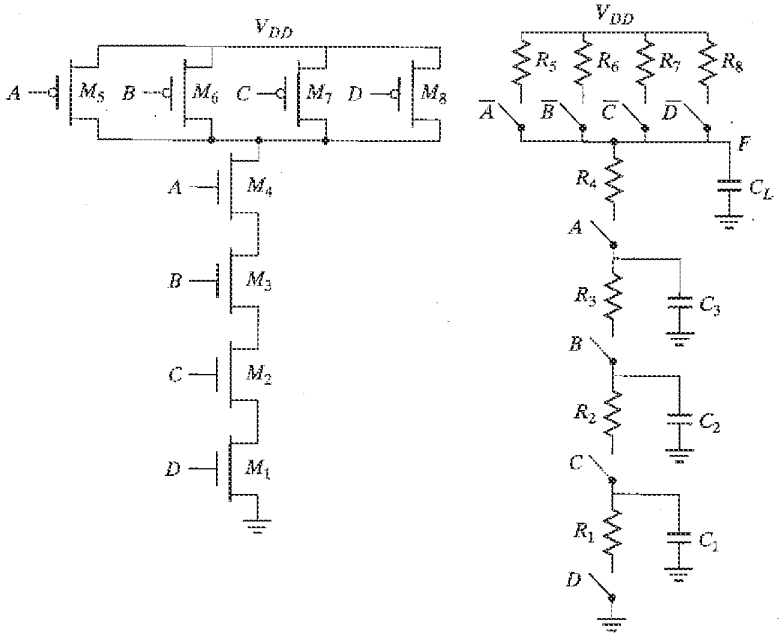


Figure 6-11 Four-input NAND gate and its *RC* model.

Example 6.4 A Four-Input Complementary CMOS NAND Gate

In this example, we evaluate the *intrinsic (or unloaded) propagation delay* of a four-input NAND gate (without any loading) is evaluatedusing hand analysis and simulation. The layout of the gate is shown in Figure 6-12. Assume that all NMOS devices have a W/L of 0.5 μm/0.25 μm, and all PMOS devices have a device size of 0.375 μm/0.25 μm. The devices are sized such that the worst case rise and fall times are approximately equal to a first order (ignoring the internal node capacitances).

By using techniques similar to those employed for the CMOS inverter in Chapter 5, the capacitance values can be computed from the layout. Notice that in the pull-up path, the PMOS devices share the drain terminal, in order to reduce the overall parasitic contribution. Using our standard design rules, we find that the area and perimeter for various devices can be easily computed, as shown in Table 6-2.

In this example, we focus on the pull-down delay, and the capacitances will be computed for the high-to-low transition at the output. While the output makes a transition from V_{DD} to 0, the internal nodes only transition from $V_{DD} - V_{Tn}$ to GND. We need to linearize the internal junction capacitances for this voltage transition, but, to simplify the analysis, we use the same K_{eq} for the internal nodes as for the output node.

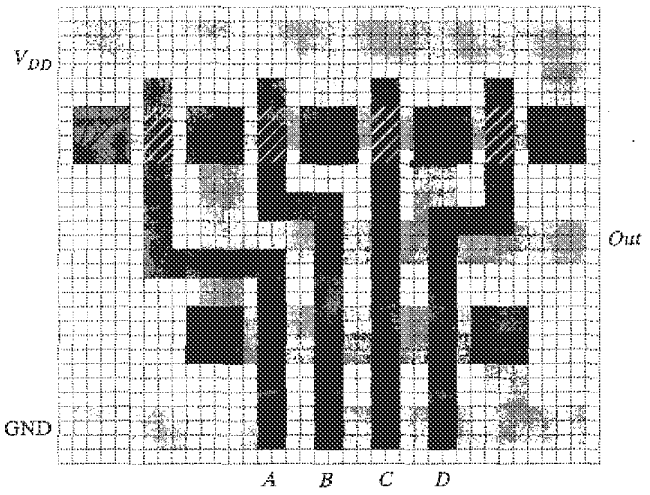


Figure 6-12 Layout a four-input NAND gate in complementary CMOS. See also Colorplate 7.

Table 6-2 Area and perimeter of transistors in four-input NAND gate.

Transistor	W (μm)	AS (μm²)	AD (μm²)	PS (μm)	PD (μm)
1	0.5	0.3125	0.0625	1.75	0.25
2	0.5	0.0625	0.0625	0.25	0.25
3	0.5	0.0625	0.0625	0.25	0.25
4	0.5	0.0625	0.3125	0.25	1.75
5	0.375	0.297	0.172	1.875	0.875
6	0.375	0.172	0.172	0.875	0.875
7	0.375	0.172	0.172	0.875	0.875
8	0.375	0.297	0.172	1.875	0.875

It is assumed that the output connects to a single, minimum-size inverter. The effect of intracell routing, which is small, is ignored. The various contributions are summarized in Table 6-3. For the NMOS and PMOS junctions, we use $K_{eq} = 0.57$, $K_{eqsw} = 0.61$, and $K_{eq} = 0.79$, $K_{eqsw} = 0.86$, respectively. Notice that the gate-to-drain capacitance is multiplied by a factor of two for all internal nodes as well as the output node, to account for the Miller effect. (This ignores the fact that the internal nodes have a slightly smaller swing due to the threshold drop.)

Table 6-3 Computation of capacitances for high-to-low transition at the output. The table shows the intrinsic delay of the gate without extra loading. Any *fan-out* capacitance would simply be added to the C_L term.

Capacitor	Contributions (H → L)	Value (fF) (H → L)
C1	$C_{d1} + C_{s2} + 2 * C_{gd1} + 2 * C_{gs2}$	(0.57 * 0.0625 * 2 + 0.61 * 0.25 * 0.28) + (0.57 * 0.0625 * 2 + 0.61 * 0.25* 0.28) + 2 * (0.31 * 0.5) + 2 * (0.31 * 0.5) = 0.85 fF
C2	$C_{d2} + C_{s3} + 2 * C_{gd2} + 2 * C_{gs3}$	(0.57 * 0.0625 * 2 + 0.61 * 0.25 * 0.28) + (0.57 * 0.0625 * 2 + 0.61 * 0.25* 0.28) + 2 * (0.31 * 0.5) + 2 * (0.31 * 0.5) = 0.85 fF
C3	$C_{d3} + C_{s4} + 2 * C_{gd3} + 2 * C_{gs4}$	(0.57 * 0.0625 * 2+ 0.61 * 0.25 * 0.28) + (0.57 * 0.0625 * 2+ 0.61 * 0.25* 0.28) + 2 * (0.31 * 0.5) + 2 * (0.31 * 0.5) = 0.85 fF
CL	$C_{d4} + 2 * C_{gd4} + C_{d5} + C_{d6} + C_{d7} + C_{d8} + 2 * C_{gd5} + 2 * C_{gd6} + 2 * C_{gd7} + 2 * C_{gd8} = C_{d4} + 4 * C_{d5} + 4 * 2 * C_{gd6}$	(0.57 * 0.3125 * 2 + 0.61 * 1.75 *0.28) + 2 * (0.31 * 0.5)+ 4 * (0.79 * 0.171875* 1.9+ 0.86 * 0.875 * 0.22)+ 4 * 2 * (0.27 * 0.375) = 3.47 fF

Using Eq. (6.4), we compute the propagation delay, as follows:

$$t_{pHL} = 0.69\left(\frac{13\text{K}\Omega}{2}\right)(0.85\text{ fF} + 2 \cdot 0.85\text{ fF} + 3 \cdot 0.85\text{ fF} + 4 \cdot 3.47\text{ fF}) = 85\text{ ps}$$

The simulated delay for this particular transition was found to be 86 ps! The hand analysis gives a fairly accurate estimate, given all of the assumptions and linearizations that were made. For example, we assume that the gate–source (or gate–drain) capacitance only consists of the overlap component. This is not entirely the case, because, during the transition, some other contributions come in place depending upon the operating region. Once again, the goal of hand analysis is not to provide a totally accurate delay prediction, but rather to give intuition into what factors influence the delay and to aid in initial transistor sizing. Accurate timing analysis and transistor optimization is usually done using SPICE. The simulated worst case low-to-high delay time for this gate was 106 ps.

While complementary CMOS is a very robust and simple approach for implementing logic gates, there are two major problems associated with using this style as the complexity of the gate (i.e., *fan-in*) increases. First, the number of transistors required to implement an N fan-in gate is $2N$. This can result in a significantly large implementation area.

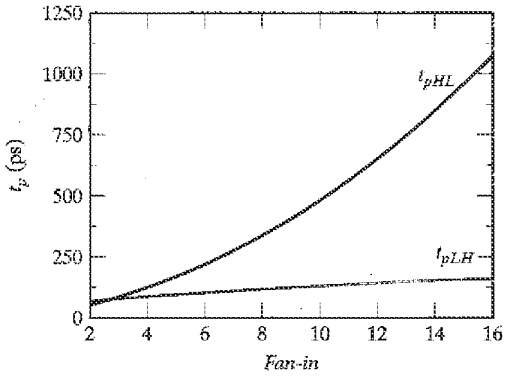


Figure 6-13 Propagation delay of CMOS NAND gate as a function of fan-in. A fan-out of one inverter is assumed, and all pull-down transistors are minimal size.

The second problem is that propagation delay of a complementary CMOS gate deteriorates rapidly as a function of the fan-in. In fact, the *unloaded intrinsic delay* of the gate is, at worst, a *quadratic function of the fan-in.*

- The large number of transistors ($2N$) increases the overall capacitance of the gate. For an N-input gate, the *intrinsic capacitance* increases linearly with the fan-in. Consider, for instance, the NAND gate of Figure 6-11. Given the linear increase in the number of PMOS devices connected to the output node, we expect the low-to-high delay of the gate to increase linearly with fan-in—while the capacitance goes up linearly, the pull-up resistance remains unchanged.
- The series connection of transistors in either the PUN or PDN of the gate causes an additional slowdown. We know that the *distributed RC network* in the PDN of Figure 6-11 comes with a delay that is quadratic in the number of elements in the chain. The high-to-low delay of the gate should hence be a quadratic function of the fan-in.

Figure 6-13 plots the (intrinsic) propagation delay of a NAND gate as a function of fan-in assuming a fixed fan-out of one inverter (NMOS: 0.5 μm and PMOS: 1.5 μm). As predicted, t_{pLH} is a linear function of fan-in, while the simultaneous increase in the pull-down resistance and the load capacitance cause an approximately quadratic relationship for t_{pHL}. Gates with a *fan-in* greater than or equal to 4 become excessively slow and must be avoided.

Design Techniques for Large Fan-in

The designer has a number of techniques at his disposition to reduce the delay of large fan-in circuits:

- **Transistor Sizing** The most obvious solution is to increase the transistor sizes. This lowers the resistance of devices in series and lowers the time constants. However, increasing the transistor sizes results in larger parasitic capacitors, which not only affect the *propagation delay* of the gate in question, but

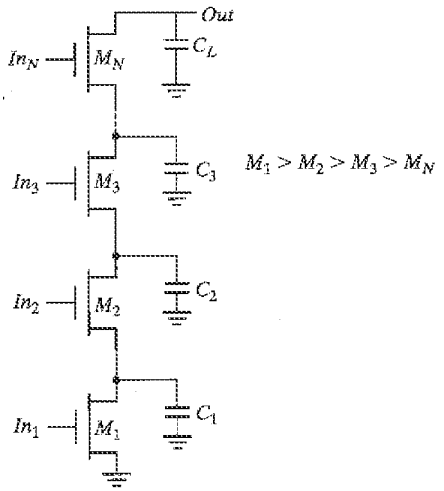


Figure 6-14 Progressive sizing of transistors in large transistor chains copes with the extra load of internal capacitances.

also present a larger load to the preceding gate. This technique should therefore be used with caution. If the load capacitance is dominated by the intrinsic capacitance of the gate, widening the device only creates a "self-loading" effect, and the *propagation delay* is unaffected. Sizing is only effective when the load is dominated by the fan-out. A more comprehensive approach toward sizing transistors in complex CMOS combinational networks is discussed in the next section.

- **Progressive Transistor Sizing** An alternate approach to uniform sizing (in which each transistor is scaled up uniformly), is to use progressive transistor sizing (Figure 6-14). Referring back to Eq. (6.3), we see that the resistance of M_1 (R_1) appears N times in the delay equation, the resistance of M_2 (R_2) appears $N-1$ times, etc. From the equation, it is clear that R_1 should be made the smallest, R_2 the next smallest, etc. Consequently, a progressive scaling of the transistors is beneficial: $M_1 > M_2 > M_3 > M_N$. This approach reduces the dominant resistance, while keeping the increase in capacitance within bounds. For an excellent treatment on the optimal sizing of transistors in a complex network, we refer the interested reader to [Shoji88, pp. 131–143]. You should be aware, however, of one important pitfall of this approach. While progressive resizing of transistors is relatively easy in a schematic diagram, it is not as simple in a real layout. Very often, design-rule considerations force the designer to push the transistors apart, which causes the internal capacitance to grow. This may offset all the gains of the resizing!
- **Input Reordering** Some signals in complex combinational logic blocks might be more critical than others. Not all inputs of a gate arrive at the same time (due, for instance, to the propagation delays of the preceding logical gates). An input signal to a gate is called *critical* if it is the last signal of all inputs to assume a stable value. The path through the logic which determines the ultimate speed of the structure is called the *critical path*.

  Putting the critical-path transistors closer to the output of the gate can result in a speed up, as demonstrated in Figure 6-15. Signal In_1 is assumed to be a critical signal. Suppose further that In_2 and In_3 are high, and that In_1 undergoes a $0 \rightarrow 1$ transition. Assume also that C_L is initially charged high. In case (a), no path to GND exists until M_1 is turned on, which, unfortunately, is the last event to happen. The delay between the arrival of In_1 and the output is therefore determined by the time it takes to discharge C_L, C_1, and C_2. In the second case, C_1 and C_2 are already

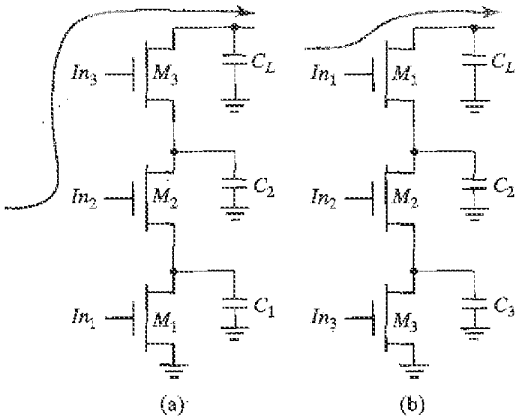


Figure 6-15 Influence of transistor ordering on delay. Signal In_1 is the critical signal.

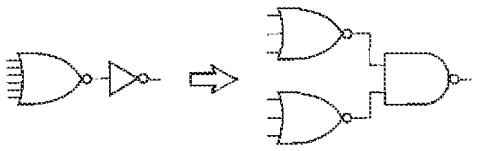


Figure 6-16 Logic restructuring can reduce the gate fan-in.

discharged when In_1 changes. Only C_L still has to be discharged, resulting in a smaller delay.

- **Logic Restructuring** Manipulating the logic equations can reduce the fan-in requirements and thus reduce the gate delay, as illustrated in Figure 6-16. The quadratic dependency of the gate delay on *fan-in* makes the six-input NOR gate extremely slow. Partitioning the NOR gate into two three-input gates results in a significant speedup, which by far offsets the extra delay incurred by turning the inverter into a two-input NAND gate. ■

Optimizing Performance in Combinational Networks

Earlier, we established that minimization of the propagation delay of a gate in isolation is a purely academic effort. The sizing of devices should happen in its proper context. In Chapter 5, we developed a methodology to do so for inverters. We also found that an optimal fan-out for a chain of inverters driving a load C_L is $(C_L/C_{in})^{1/N}$, where N is the number of stages in the chain, and C_{in} the input capacitance of the first gate in the chain. If we have an opportunity to select the number of stages, we found out that we would like to keep the fan-out per stage around 4. Can this result be extended to determine the size of any combinational path for minimal delay? By extending our previous approach to address complex logic networks, we find out that this is indeed possible [Sutherland99].[2]

[2]The approach introduced in this section is commonly called logical effort, and was formally introduced in [Sutherland99], which presents an extensive treatment of the topic. The treatment offered here represents only a glance over of the overall approach.

Table 6-4 Estimates of intrinsic delay factors of various logic types, assuming simple layout styles, and a fixed PMOS–NMOS ratio.

Gate type	p
Inverter	1
n-input NAND	n
n-input NOR	n
n-way multiplexer	$2n$
XOR, NXOR	$n2^{n-1}$

To do so, we modify the basic delay equation of the inverter that we introduced in Chapter 5, namely,

$$t_p = t_{p0}\left(1 + \frac{C_{ext}}{\gamma C_g}\right) = t_{p0}(1 + f/\gamma) \tag{6.5}$$

to

$$t_p = t_{p0}(p + gf/\gamma) \tag{6.6}$$

with t_{p0} still representing the intrinsic delay of an inverter and f the *effective fan-out*, defined as the ratio between the external load and the input capacitance of the gate. In this context, f is also called the *electrical effort*, and p represents the ratio of the intrinsic (or unloaded) delays of the complex gate and the simple inverter, and is a function of gate topology, as well as layout style. The more involved structure of the multiple-input gate causes its intrinsic delay to be higher than that of an inverter. Table 6-4 enumerates the values of p for some standard gates, assuming simple layout styles, and ignoring second-order effects such as internal node capacitances.

The factor g is called the *logical effort*, and represents the fact that, for a given load, complex gates have to work harder than an inverter to produce a similar response. In other words, the logical effort of a logic gate tells how much worse it is at producing output current than an inverter, given that each of its inputs may present only the same input capacitance as the inverter. Equivalently, logical effort is how much more input capacitance a gate presents to deliver the same output current as an inverter. Logical effort is a useful parameter, because it depends only on circuit topology. The logical efforts of some common logic gates are given in Table 6-5.

Table 6-5 Logic efforts of common logic gates, assuming a PMOS–NMOS ratio of 2.

Gate Type	Number of Inputs			
	1	2	3	n
Inverter	1			
NAND		4/3	5/3	(n + 2)/3
NOR		5/3	7/3	(2n + 1)/3
Multiplexer		2	2	2
XOR		4	12	

Example 6.5 Logical Effort of Complex Gates

Consider the gates shown in Figure 6-17. Assuming PMOS–NMOS ratio of 2, the input capacitance of a minimum-sized symmetrical inverter equals three times the gate capacitance of a minimum-sized NMOS (called C_{unit}). We size the two-input NAND and NOR such that their equivalent resistances equal the resistance of the inverter (using the techniques described earlier). This increases the input capacitance of the two-input NAND to 4 C_{unit}, or 4/3 the capacitance of the inverter. The input capacitance of the two-input NOR is 5/3 that of the inverter. Equivalently, for the same input capacitance, the NAND and NOR gate have 4/3 and 5/3 less driving strength than the inverter. This affects the delay component that corresponds to the load, increasing it by this same factor, called the *logical effort*. Hence, $g_{NAND} = 4/3$, and $g_{NOR} = 5/3$.

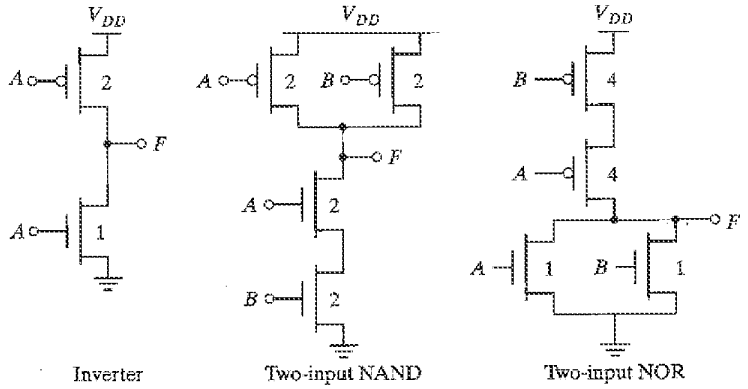


Figure 6-17 Logical effort of two-input NAND and NOR gates.

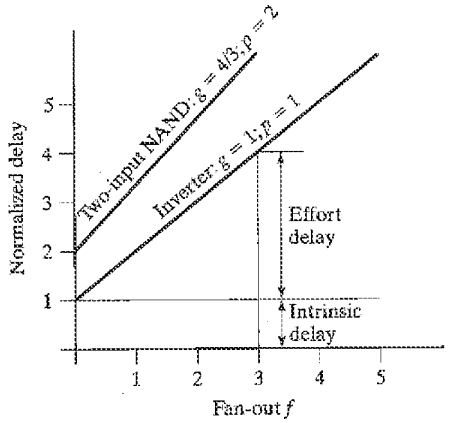


Figure 6-18 Delay as a function of fan-out for an inverter and a two-input NAND.

The delay model of a logic gate, as represented in Eq. (6.6), is a simple linear relationship. Figure 6-18 shows this relationship graphically: the delay is plotted as a function of the fan-out for an inverter and for a two-input NAND gate. The slope of the line is the logical effort of the gate; its intercept is the intrinsic delay. The graph shows that we can adjust the delay by adjusting the effective fan-out (by transistor sizing) or by choosing a logic gate with a different logical effort. Observe also that fan-out and logical effort contribute to the delay in a similar way. We call the product of the two $h = fg$, the *gate effort*.

The total delay of a path through a combinational logic block can now be expressed as

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{j=1}^{N} \left(p_j + \frac{f_j g_j}{\gamma} \right) \tag{6.7}$$

We use a similar procedure as we did for the inverter chain in Chapter 5 to determine the minimum delay of the path. By finding $N-1$ partial derivatives and setting them to zero, we find that **each stage should bear the same gate effort:**

$$f_1 g_1 = f_2 g_2 = \ldots = f_N g_N \tag{6.8}$$

The logical effort along a path in the network compounds by multiplying the logical efforts of all the gates along the path, yielding the *path logical effort* G:

$$G = \prod_{1}^{N} g_i \tag{6.9}$$

We also can define a *path effective fan-out* (or *electrical effort*) F, which relates the load capacitance of the last gate in the path to the input capacitance of the first gate:

$$F = \frac{C_L}{C_{g1}} \tag{6.10}$$

To relate F to the effective fan-outs of the individual gates, we must introduce another factor to account for the logical fan-out within the network. When fan-out occurs at the output of a node, some of the available drive current is directed along the path we are analyzing, and some is directed off the path. We define the *branching effort* b of a logical gate on a given path to be

$$b = \frac{C_{\text{on-path}} + C_{\text{off-path}}}{C_{\text{on-path}}} \tag{6.11}$$

where $C_{\text{on-path}}$ is the load capacitance of the gate along the path we are analyzing and $C_{\text{off-path}}$ is the capacitance of the connections that lead off the path. Note that the branching effort is, if the path does not branch (as in a chain of gates). The *path branching effort* is defined as the product of the branching efforts at each of the stages along the path, or

$$B = \prod_{1}^{N} b_i \tag{6.12}$$

The path electrical effort can now be related to the electrical and branching efforts of the individual stages:

$$F = \prod_{1}^{N} \frac{f_i}{b_i} = \frac{\prod f_i}{B} \tag{6.13}$$

Finally, the total path effort H can be defined. Using Eq. (6.13), we write

$$H = \prod_{1}^{N} h_i = \prod_{1}^{N} g_i f_i = GFB \tag{6.14}$$

From here on, the analysis proceeds along the same lines as the inverter chain. The gate effort that minimizes the path delay is

$$h = \sqrt[N]{H} \tag{6.15}$$

and the minimum delay through the path is

$$D = t_{p0}\left(\sum_{j=1}^{N} p_j + \frac{N(\sqrt[N]{H})}{\gamma}\right) \tag{6.16}$$

Note that the path intrinsic delay is a function of the types of logic gates in the path and is not affected by the sizing. The size factors of the individual gates in the chain s_i can then be derived by working from front to end (or vice versa). We assume that a unit-size gate has a driving capability equal to a minimum-size inverter. Based on the definition of the logical effort, this means that its input capacitance is g times larger than that of the reference inverter, which equals C_{ref}. With s_1 the sizing factor of the first gate in the chain, the input capacitance of the chain C_{g1}

equals $g_1 s_1 C_{ref}$. Including the branching effort, we know that the input capacitance of gate 2 is (f_1/b_1) larger, or

$$g_2 s_2 C_{ref} = \left(\frac{f_1}{b_1}\right) g_1 s_1 C_{ref} \tag{6.17}$$

For gate i in the chain, this yields

$$s_i = \left(\frac{g_1 s_1}{g_i}\right) \prod_{j=1}^{i-1} \left(\frac{f_j}{b_j}\right) \tag{6.18}$$

Example 6.6 Sizing Combinational Logic for Minimum Delay

Consider the logic network of Figure 6-19, which may represent the critical path of a more complex logic block. The output of the network is loaded with a capacitance which is five times larger than the input capacitance of the first gate, which is a minimum-sized inverter. The effective fan-out of the path thus equals $F = C_L/C_{g1} = 5$. Using the entries in Table 6-5, we find the path logical effort as follows:

$$G = 1 \times \frac{5}{3} \times \frac{5}{3} \times 1 = \frac{25}{9}$$

Since there is no branching, $B = 1$. Hence, $H = GFB = 125/9$, and the optimal stage effort h is $\sqrt[4]{H} = 1.93$. Taking into account the gate types, we derive the following fan-out factors: $f_1 = 1.93$; $f_2 = 1.93 \times (3/5) = 1.16$; $f_3 = 1.16$; $f_4 = 1.93$. Notice that the inverters are assigned larger than the more complex gates because they are better at driving loads.

Finally, we derive the gate sizes (with respect to the minimum-sized versions) using Eq. (6.18). This leads to the following values: $a = f_1 g_1/g_2 = 1.16$; $b = f_1 f_2 g_1/g_3 = 1.34$; and $c = f_1 f_2 f_3 g_1/g_4 = 2.60$.

These calculations do not have to be very precise. As discussed in Chapter 5, sizing a gate too large or too small by a factor of 1.5 still results in circuits within 5% of minimum delay. Therefore, the "back of the envelope" hand calculations using this technique are quite effective.

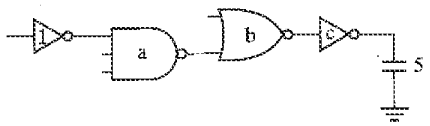


Figure 6-19 Critical path of combinational network.

Problem 6.2 Sizing an Inverter Network

Revisit Problem 5.5, but this time around use the branching-effort approach to produce the solution.

Power Consumption in CMOS Logic Gates

The sources of power consumption in a complementary CMOS inverter were discussed in detail in Chapter 5. Many of these issues apply directly to complex CMOS gates. The power dissipation is a strong function of transistor sizing (which affects physical capacitance,) input and output rise–fall times (which determine the short-circuit power,) device thresholds and temperature (which impact leakage power,) and switching activity. The dynamic power dissipation is given by $\alpha_{0\to1} C_L V_{DD}^2 f$. Making a gate more complex mostly affects the *switching activity* $\alpha_{0\to1}$, which has two components: a static component that is only a function of the topology of the logic network, and a dynamic one that results from the timing behavior of the circuit. (The latter factor is also called glitching.)

Logic Function The transition activity is a strong function of the logic function being implemented. For static CMOS gates with statistically independent inputs, the static transition probability is the probability p_0 that the output will be in the *zero* state in one cycle, multiplied by the probability p_1 that the output will be in the *one* state in the next cycle:

$$\alpha_{0\to1} = p_0 \cdot p_1 = p_0 \cdot (1 - p_0) \tag{6.19}$$

Assuming that the inputs are independent and uniformly distributed, any N-input static gate has a transition probability given by

$$\alpha_{0\to1} = \frac{N_0}{2^N} \cdot \frac{N_1}{2^N} = \frac{N_0 \cdot (2^N - N_0)}{2^{2N}} \tag{6.20}$$

where N_0 is the number of *zero* entries, and N_1 is the number of *one* entries in the output column of the truth table of the function. To illustrate, consider a static two-input NOR gate whose truth table is shown in Table 6-6. Assume that only one input transition is possible during a clock cycle and that the inputs to the NOR gate have a uniform input distribution (in other words, the four possible states for inputs A and B—00, 01, 10, 11—are equally likely).

Table 6-6 Truth table of a two-input NOR gate.

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

From Table 6-6 and Eq. (6.20), the output transition probability of a two-input static CMOS NOR gate can be derived:

$$\alpha_{0\to 1} = \frac{N_0 \cdot (2^N - N)}{2^{2N}} = \frac{3 \cdot (2^2 - 3)}{2^{2 \cdot 2}} = \frac{3}{16} \tag{6.21}$$

Problem 6.3 *N*-Input XOR Gate

Assuming the inputs to an *N*-input XOR gate are uncorrelated and uniformly distributed, derive the expression for the switching activity factor.

Signal Statistics The switching activity of a logic gate is a strong function of the input signal statistics. Using a uniform input distribution to compute activity is not a good technique, since the propagation through logic gates can significantly modify the signal statistics. For example, consider once again a two-input static NOR gate, and let p_a and p_b be the probabilities that the inputs A and B are *one*. Assume further that the inputs are not correlated. The probability that the output node is 1 is given by

$$p_1 = (1 - p_a)(1 - p_b) \tag{6.22}$$

Therefore, the probability of a transition from 0 to 1 is

$$\alpha_{0\to 1} = p_0 p_1 = (1 - (1 - p_a)(1 - p_b))(1 - p_a)(1 - p_b) \tag{6.23}$$

Figure 6-20 shows the transition probability as a function of p_a and p_b. Observe how this graph degrades into the simple inverter case when one of the input probabilities is set to 0. From

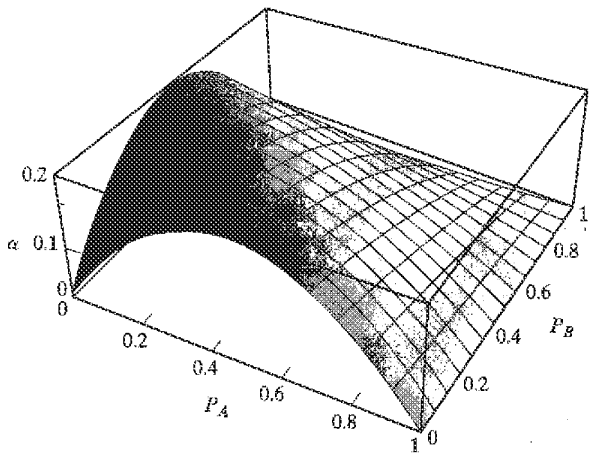


Figure 6-20 Transition activity of a two-input NOR gate as a function of the input probabilities (p_A, p_B).

this plot, it is clear that understanding the signal statistics and their impact on switching events can be used to significantly impact the power dissipation.

Problem 6.4 Power Dissipation of Basic Logic Gates

Derive the $0 \rightarrow 1$ output transition probabilities for the basic logic gates (AND, OR, XOR). The results to be obtained are given in Table 6-7.

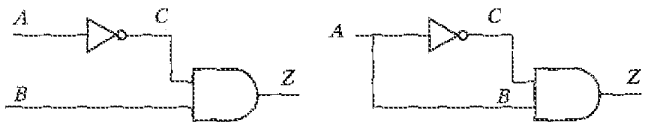
Table 6-7 Output transition probabilities for static logic gates.

	$\alpha_{0\rightarrow1}$
AND	$(1-p_A p_B)p_A p_B$
OR	$(1-p_A)(1-p_B)[1-(1-p_A)(1-p_B)]$
XOR	$[1-(p_A+p_B-2p_A p_B)](p_A+p_B-2p_A p_B)$

Intersignal Correlations The evaluation of the switching activity is further complicated by the fact that signals exhibit correlation in space and time. Even if the primary inputs to a logic network are uncorrelated, the signals become correlated or "colored," as they propagate through the logic network. This is best illustrated with a simple example. Consider first the circuit shown in Figure 6-21a, and assume that the primary inputs A and B are uncorrelated and uniformly distributed. Node C has a **1** (**0**) probability of 1/2, and a $0 \rightarrow 1$ transition probability of 1/4. The probability that the node Z undergoes a power consuming transition is then determined using the AND-gate expression of Table 6-7:

$$P_{0\rightarrow1} = (1 - p_a p_b)\, p_a\, p_b = (1 - 1/2 \cdot 1/2)\; 1/2 \cdot 1/2 = 3/16 \tag{6.24}$$

The computation of the probabilities is straightforward: signal and transition probabilities are evaluated in an ordered fashion, progressing from the input to the output node. This approach, however, has two major limitations: (1) it does not deal with circuits with feedback as found in sequential circuits, and (2) it assumes that the signal probabilities at the input of each gate are independent. This is rarely the case in actual circuits, where reconvergent fan-out often causes intersignal dependencies. For instance, the inputs to the AND gate in Figure 6-21b (C and B) are interdependent because both are a function of A. The approach to computing



(a) Logic circuit without reconvergent fan-out

(b) Logic circuit with reconvergent fan-out

Figure 6-21 Example illustrating the effect of signal correlations.

probabilities that we presented previously fails under these circumstances. Traversing from inputs to outputs yields a transition probability of 3/16 for node Z, similar to the previous analysis. This value clearly is false, as logic transformations show that the network can be reduced to $Z = C \cdot B = A \cdot \overline{A} = 0$, and thus no transition will ever take place.

To get the precise results in the progressive analysis approach, its is essential to take signal interdependencies into account. This can be accomplished with the aid of conditional probabilities. For an AND gate, Z equals 1 if and only if B and C are equal to 1. Thus,

$$p_Z = p(Z = 1) = p(B = 1, C = 1) \tag{6.25}$$

where $p(B = 1, C = 1)$ represents the probability that B and C are equal to 1 simultaneously. If B and C are independent, $p(B = 1, C = 1)$ can be decomposed into $p(B = 1) \cdot p(C = 1)$, and this yields the expression for the AND gate derived earlier: $p_Z = p(B = 1) \cdot p(C = 1) = p_B p_C$. If a dependency between the two exists (as is the case in Figure 6-21b), a conditional probability has to be employed, such as the following:

$$p_Z = p(C = 1|B = 1) \cdot p(B = 1) \tag{6.26}$$

The first factor in Eq. (6.26) represents the probability that $C = 1$ given that $B = 1$. The extra condition is necessary because C is dependent upon B. Inspection of the network shows that this probability is equal to 0, since C and B are logical inversions of each other, resulting in the signal probability for Z, $p_Z = 0$.

Deriving those expressions in a structured way for large networks with reconvergent fanout is complex, especially when the networks contain feedback loops. Computer support is therefore essential. To be meaningful, the analysis program has to process a typical sequence of input signals, because the power dissipation is a strong function of statistics of those signals.

Dynamic or Glitching Transitions When analyzing the transition probabilities of complex, multistage logic networks in the preceding section, we ignored the fact that the gates have a nonzero propagation delay. In reality, the finite propagation delay from one logic block to the next can cause spurious transitions known as *glitches or dynamic hazards* to occur: a node can exhibit multiple transitions in a single clock cycle before settling to the correct logic level.

A typical example of the effect of glitching is shown in Figure 6-22, which displays the simulated response of a chain of NAND gates for all inputs going simultaneously from 0 to 1. Initially, all the outputs are 1 since one of the inputs was 0. For this particular transition, all the odd bits must transition to 0, while the even bits remain at the value of 1. However, due to the finite propagation delay, the even output bits at the higher bit positions start to discharge, and the voltage drops. When the correct input ripples through the network, the output goes high. The glitch on the even bits causes extra power dissipation beyond what is required to strictly implement the logic function. Although the glitches in this example are only partial (i.e., not from rail to rail), they contribute significantly to the power dissipation. Long chains of gates often occur in important structures such as adders and multipliers, and the glitching component can easily dominate the overall power consumption.

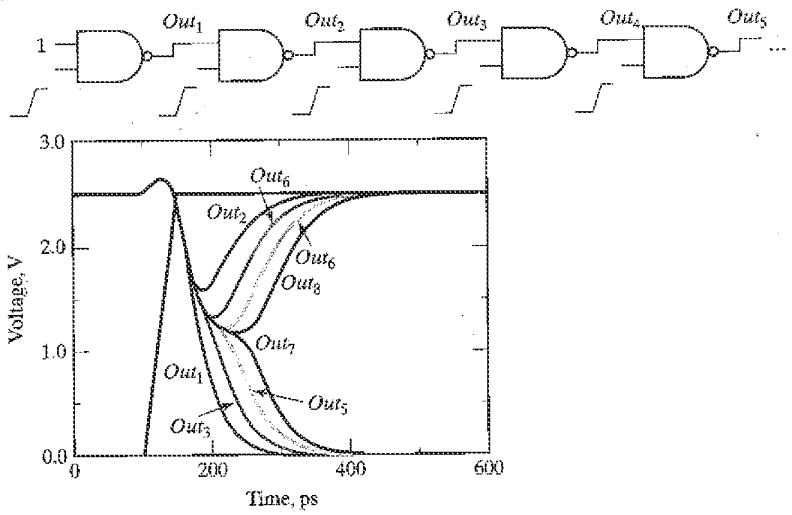


Figure 6-22 Glitching in a chain of NAND gates.

Design Techniques to Reduce Switching Activity

The dynamic power of a logic gate can be reduced by minimizing the physical capacitance and the switching activity. The physical capacitance can be minimized in a number ways, including circuit style selection, transistor sizing, placement and routing, and architectural optimizations. The switching activity, on the other hand, can be minimized at all levels of the design abstraction, and is the focus of this section. Logic structures can be optimized to minimize both the fundamental transitions required to implement a given function and the spurious transitions.

1. **Logic Restructuring** Changing the topology of a logic network may reduce its power dissipation. Consider, for example, two alternative implementations of $F = A \cdot B \cdot C \cdot D$, as shown in Figure 6-23. Ignore glitching and assume that all primary inputs (A,B,C,D) are uncorrelated and uniformly distributed (this is, $p_{1\,(a,b,c,d)} = 0.5$). Using the expressions from Table 6-7, the activity can be computed for the two topologies, as shown in Table 6-8. The results indicate that the chain implementation has an overall lower switching activity than the tree implementation for random inputs. However, as mentioned before, it is also important to consider the timing behavior to

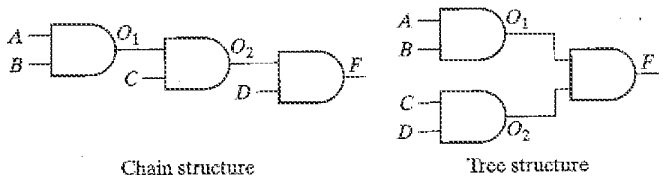


Figure 6-23 Simple example to demonstrate the influence of circuit topology on activity.

Table 6-8 Probabilities for tree and chain topologies.

	O_1	O_2	F
p_1 (chain)	1/4	1/8	1/16
$p_0 = 1\text{-}p_1$ (chain)	3/4	7/8	15/16
$p_{0\to1}$ (chain)	3/16	7/64	15/256
p_1 (tree)	1/4	1/4	1/16
$p_0 = 1\text{-}p_1$ (tree)	3/4	3/4	15/16
$p_{0\to1}$ (tree)	3/16	3/16	15/256

accurately make power trade-offs. In this example, the tree topology experiences (virtually) no glitching activity since the signal paths are balanced to all the gates.

2. **Input ordering** Consider the two static logic circuits of Figure 6-24. The probabilities that *A*, *B*, and C are equal to **1** are listed in the Figure. Since both circuits implement identical logic functionality, it is clear that the activity at the output node Z is equal in both cases. The difference is in the activity at the intermediate node. In the first circuit, this activity equals $(1 - 0.5 \times 0.2)\ (0.5 \times 0.2) = 0.09$. In the second case, the probability that a $0 \to 1$ transition occurs equals $(1 - 0.2 \times 0.1)\ (0.2 \times 0.1) = 0.0196$, a substantially lower value. From this, we learn that it is beneficial to postpone the introduction of signals with a high transition rate (i.e., signals with a signal probability close to 0.5). A simple reordering of the input signals is often sufficient to accomplish that goal.

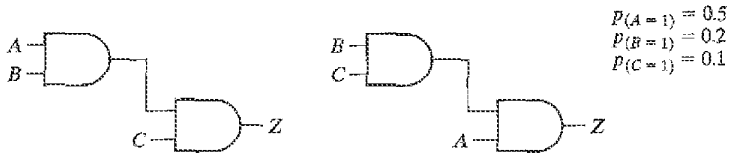
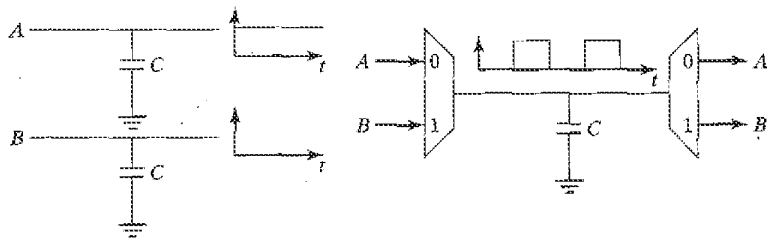


Figure 6-24 Reordering of inputs affects the circuit activity.

3. **Time-multiplexing resources** Time-multiplexing a single hardware resource—such as a logic unit or a bus—over a number of functions is a technique often used to minimize the implementation area. Unfortunately, the minimum area solution does not always result in the lowest switching activity. For example, consider the transmission of two input bits (*A* and *B*) using either dedicated resources or a time-multiplexed approach, as shown in Figure 6-25. To the first order, ignoring the multiplexer overhead, it would seem that the degree of time multiplexing should not affect the switched capacitance, since the time-multiplexed solution has half the physical capacitance switched at twice the frequency (for a fixed throughput).

If the data being transmitted are random, it will make no difference which architecture is used. However, if the data signals have some distinct properties (such as temporal correlation), the power dissipation of the time-multiplexed solution can be significantly higher. Suppose, for instance, that *A* is always (or mostly) 1, and *B* is (mostly) 0. In the parallel solution, the switched capacitance is very low since there are very few transitions on the data bits. However, in the time-multiplexed solution,

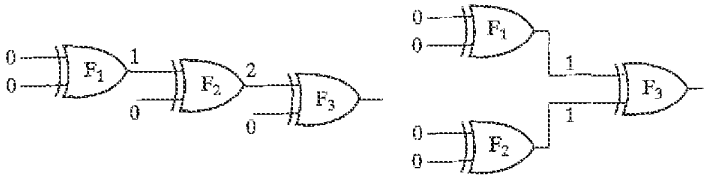


(a) Parallel data transmission (b) Serial data transmission

Figure 6-25 Parallel versus time-multiplexed data busses.

the bus toggles between 0 and 1. Care must be taken in digital systems to avoid time-multiplexing data streams with very distinct data characteristics.

4. **Glitch Reduction by balancing signal paths** The occurrence of glitching in a circuit is mainly due to a mismatch in the path lengths in the network. If all input signals of a gate change simultaneously, no glitching occurs. On the other hand, if input signals change at different times, a dynamic hazard might develop. Such a mismatch in signal timing is typically the result of different path lengths with respect to the primary inputs of the network. This is illustrated in Figure 6-26. Assume that the XOR gate has a unit delay. The first network (a) suffers from glitching as a result of the wide disparity between the arrival times of the input signals for a gate. For example, for gate F_3, one input settles at time 0, while the second one only arrives at time 2. Redesigning the network so that all arrival times are identical can dramatically reduce the number of superfluous transitions (network b).



(a) Network sensitive to glitching (b) Glitch-free network

Figure 6-26 Glitching is influenced by matching of signal path lengths. The annotated numbers indicate the signal arrival times.

Summary

The CMOS logic style described in the previous section is highly robust and scalable with technology, but requires $2N$ transistors to implement an N-input logic gate. Also, the load capacitance is significant, since each gate drives two devices (a PMOS and an NMOS) per *fan-out*. This has opened the door for alternative logic families that either are simpler or faster.

6.2.2 Ratioed Logic

Concept

Ratioed logic is an attempt to reduce the number of transistors required to implement a given logic function, often at the cost of reduced robustness and extra power dissipation. The purpose

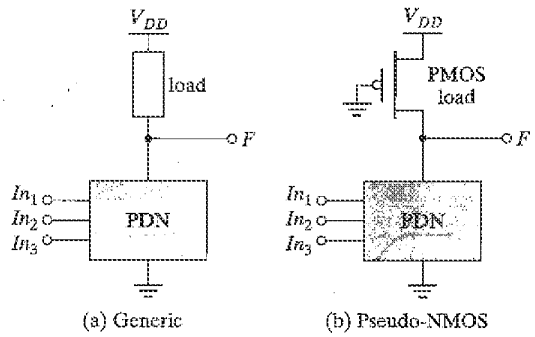


Figure 6-27 Ratioed logic gate.

of the PUN in complementary CMOS is to provide a conditional path between V_{DD} and the output when the PDN is turned *off*. In ratioed logic, the entire PUN is replaced with a single unconditional load device that pulls up the output for a high output as in Figure 6-27a. Instead of a combination of active pull-down and pull-up networks, such a gate consists of an NMOS pull-down network that realizes the *logic function*, and a simple *load device*. Figure 6-27b shows an example of ratioed logic, which uses a grounded PMOS load and is referred to as a pseudo-NMOS gate.

The clear advantage of a pseudo-NMOS gate is the reduced number of transistors ($N + 1$, versus $2N$ for complementary CMOS). The nominal high output voltage (V_{OH}) for this gate is V_{DD} since the pull-down devices are turned *off* when the output is pulled high (assuming that V_{OL} is below V_{Tn}). On the other hand, **the nominal low output voltage is not 0 V**, since there is contention between the devices in the PDN and the grounded PMOS load device. This results in reduced noise margins and, more importantly, static power dissipation. The sizing of the load device relative to the pull-down devices can be used to trade off parameters such as *noise margin*, *propagation delay*, and *power dissipation*. Since the voltage swing on the output and the overall functionality of the gate depend on the ratio of the NMOS and PMOS sizes, the circuit is called *ratioed*. This is in contrast to the *ratioless* logic styles, such as complementary CMOS, where the low and high levels do not depend on transistor sizes.

Computing the dc-transfer characteristic of the pseudo-NMOS proceeds along paths similar to those used for its complementary CMOS counterpart. The value of V_{OL} is obtained by equating the currents through the driver and load devices for $V_{in} = V_{DD}$. At this operation point, it is reasonable to assume that the NMOS device resides in linear mode (since, ideally, the output should be close to 0V), while the PMOS load is saturated:

$$k_n\left((V_{DD} - V_{Tn})V_{OL} - \frac{V_{OL}^2}{2}\right) + k_p\left((-V_{DD} - V_{Tp}) \cdot V_{DSATp} - \frac{V_{DSATp}^2}{2}\right) = 0 \qquad (6.27)$$

Assuming that V_{OL} is small relative to the gate drive ($V_{DD} - V_T$), and that V_{Tn} is equal to V_{Tp} in magnitude, V_{OL} can be approximated as

$$V_{OL} \approx \frac{k_p(V_{DD} + V_{Tp}) \cdot V_{DSATp}}{k_n(V_{DD} - V_{Tn})} \approx \frac{\mu_p \cdot W_p}{\mu_n \cdot W_n} \cdot V_{DSATp} \tag{6.28}$$

In order to make V_{OL} as small as possible, the PMOS device should be sized much smaller than the NMOS pull-down devices. Unfortunately, this has a negative impact on the *propagation delay* for charging up the output node since the current provided by the PMOS device is limited.

A major disadvantage of the pseudo-NMOS gate is the static power that is dissipated when the output is low through the direct current path that exists between V_{DD} and GND. The static power consumption in the low-output mode is easily derived:

$$P_{low} = V_{DD} I_{low} \approx V_{DD} \cdot \left| k_p \left((-V_{DD} - V_{Tp}) \cdot V_{DSATp} - \frac{V_{DSATp}^2}{2} \right) \right| \tag{6.29}$$

Example 6.7 Pseudo-NMOS Inverter

Consider a simple pseudo-NMOS inverter (where the PDN network in Figure 6-27 degenerates to a single transistor) with an NMOS size of 0.5 μm/0.25 μm. In this example, we study the effect of sizing the PMOS device to demonstrate the impact on various parameters. The *W*–*L* ratio of the grounded PMOS is varied over values from 4, 2, 1, 0.5 to 0.25. Devices with a W–$L < 1$ are constructed by making the length greater than the width. The voltage transfer curve for the different sizes is plotted in Figure 6-28.

Table 6-9 summarizes the nominal output voltage (V_{OL}), static power dissipation, and the low-to-high propagation delay. The low-to-high delay is measured as the time it takes to reach 1.25 V from V_{OL} (which is not 0V for this inverter)—by definition. The trade-off between the static and dynamic properties is apparent. A larger pull-up device not only improves performance, but also increases static power dissipation and lowers noise margins by increasing V_{OL}.

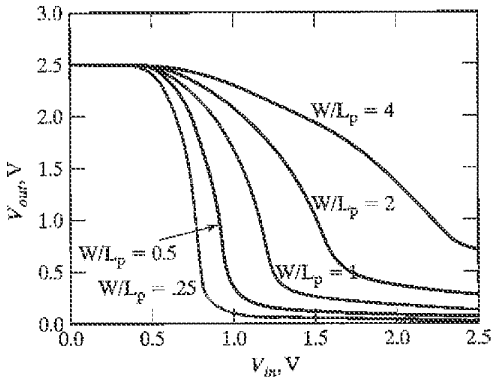


Figure 6-28 Voltage-transfer curves of the pseudo-NMOS inverter as a function of the PMOS size.

Table 6-9 Performance of a pseudo-NMOS inverter.

Size	V_{OL}	Static Power Dissipation	t_{plh}
4	0.693 V	564 μW	14 ps
2	0.273 V	298 μW	56 ps
1	0.133 V	160 μW	123 ps
0.5	0.064 V	80 μW	268 ps
0.25	0.031 V	41 μW	569 ps

Notice that the simple first-order model to predict V_{OL} is quite effective. For a PMOS W–L of 4, V_{OL} is given by (30/115) (4) (0.63V) = 0.66V.

The static power dissipation of pseudo-NMOS limits its use. When area is most important however, its reduced transistor count compared with complementary CMOS is quite attractive. Pseudo-NMOS thus still finds occasional use in large fan-in circuits. Figure 6-29 shows the schematics of pseudo-NMOS NOR and NAND gates.

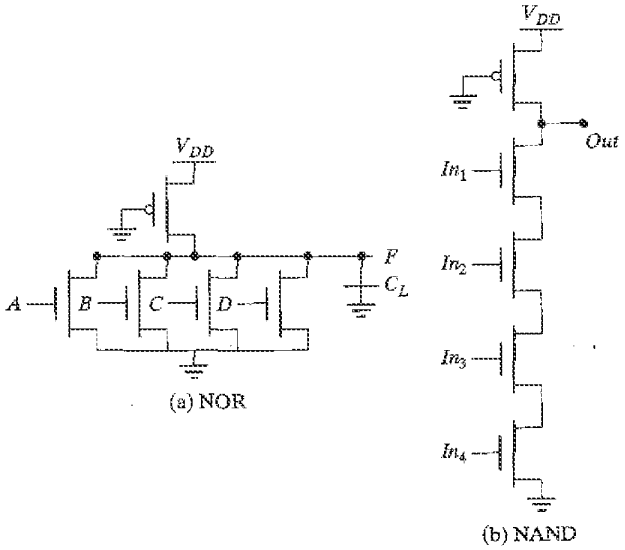


Figure 6-29 Four-input pseudo-NMOS NOR and NAND gates.

Problem 6.5 NAND versus NOR in Pseudo-NMOS

Given the choice between NOR or NAND logic, which one would you prefer for implementation in pseudo-NMOS?

How to Build Even Better Loads

It is possible to create a ratioed logic style that completely eliminates static currents and provides rail-to-rail swing. Such a gate combines two concepts: *differential logic* and *positive feedback*. A differential gate requires that each input is provided in complementary format, and it produces complementary outputs in turn. The feedback mechanism ensures that the load device is turned off when not needed. An example of such a logic family, called *Differential Cascode Voltage Switch Logic* (or DCVSL), is presented conceptually in Figure 6-30a [Heller84].

The pull-down networks PDN1 and PDN2 use NMOS devices and are mutually exclusive—that is, when PDN1 conducts, PDN2 is off, and when PDN1 is off, PDN2 conducts—such that the required logic function and its inverse are simultaneously implemented. Assume now that, for a given set of inputs, PDN1 conducts while PDN2 does not, and that *Out* and $\overline{Out}$ are initially high and low, respectively. Turning *on PDN1*, causes *Out* to be pulled down, although there is still contention between M_1 and PDN1. $\overline{Out}$ is in a high impedance state, as M_2 and PDN2 are both turned *off*. PDN1 must be strong enough to bring *Out* below $V_{DD} - |V_{Tp}|$, the point at which M_2 turns *on* and starts charging $\overline{Out}$ to V_{DD}, eventually turning off M_1. This in turn enables *Out* to discharge all the way to GND. Figure 6-30b shows an example of an XOR–XNOR gate. Notice that it is possible to share transistors among the two pull-down networks, which reduces the implementation overhead.

The resulting circuit exhibits a rail-to-rail swing, and the static power dissipation is eliminated: in steady state, none of the stacked pull-down networks and load devices are

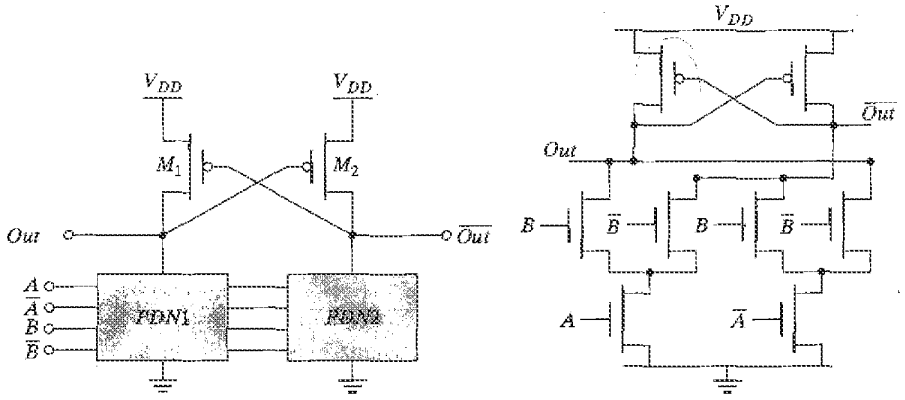


Figure 6-30 DCVSL logic gate.

simultaneously conducting. However, the circuit is still ratioed since the sizing of the PMOS devices relative to the pull-down devices is critical to functionality, not just performance. In addition to the problem of increased design complexity, this circuit style has a power-dissipation problem that is due to cross-over currents. During the transition, there is a period of time when PMOS and PDN are turned on simultaneously, producing a short circuit path.

Example 6.8 DCVSL Transient Response

An example transient response is shown in Figure 6.31 for an AND/NAND gate in DCVSL. Notice that as *Out* is pulled down to $V_{DD} - |V_{Tp}|$, $\overline{Out}$ starts to charge up to V_{DD} quickly. The delay from the input to *Out* is 197 ps and to $\overline{Out}$ is 321 ps. A static CMOS AND gate (NAND followed by an inverter) has a delay of 200 ps.

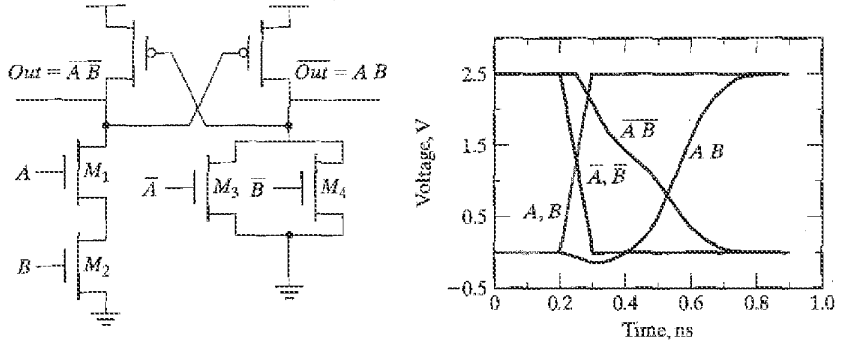


Figure 6-31 Transient response of a simple AND/NAND DCVSL gate. M_1 and M_2 1 μm/0.25 μm, M_3 and M_4 are 0.5 μm/0.25 μm and the cross-coupled PMOS devices are 1.5 μm/0.25 μm.

Design Consideration—Single-Ended versus Differential

The DCVSL gate provides *differential* (or *complementary*) *outputs*. Both the output signal (V_{out}) and its inverted value ($\overline{V}_{out}$) are simultaneously available. This is a distinct advantage, because it eliminates the need for an extra inverter to produce the complementary signal. It has been observed that a differential implementation of a complex function may reduce the number of gates required by a factor of two! The number of gates in the critical timing path is often reduced as well. Finally, the approach prevents some of the time-differential problems introduced by additional inverters. For example, in logic design, it often happens that both a signal and its complement are needed simultaneously. When the complementary signal is generated using an inverter, the inverted signal is delayed with respect to the original (Figure 6-32a). This causes timing problems, especially in very high-speed designs. Logic families with differential output capability avoid this problem to a major extent, if not completely (Figure 6-32b).

With all these positive properties, why not always use differential logic? The reason is that the differential nature virtually doubles the number of wires that have to be routed, often leading to unwieldy designs on top of the additional implementation overhead in the individual gates. The dynamic power dissipation also is high.

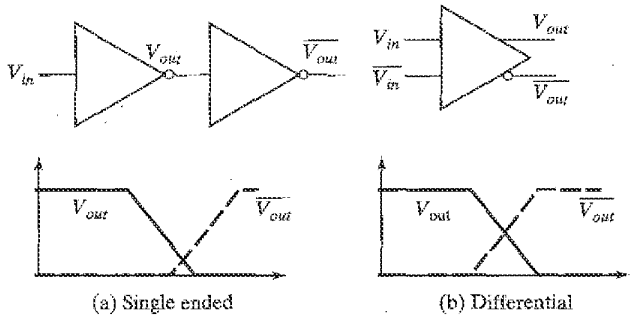


Figure 6-32 Advantage of over single-ended (a) differential (b) gate. ■

6.2.3 Pass-Transistor Logic

Pass-Transistor Basics

A popular and widely used alternative to complementary CMOS is *pass-transistor logic*, which attempts to reduce the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source–drain terminals [Radhakrishnan85]. This is in contrast to logic families that we have studied so far, which only allow primary inputs to drive the gate terminals of MOSFETS.

Figure 6-33 shows an implementation of the AND function constructed that way, using only NMOS transistors. In this gate, if the B input is high, the top transistor is turned on and copies the input A to the output F. When B is low, the bottom pass-transistor is turned on and passes a 0. The switch driven by $\overline{B}$ seems to be redundant at first glance. Its presence is essential to ensure that the gate is static—a low-impedance path must exist to the supply rails under all circumstances (in this particular case, when B is low).

The promise of this approach is that fewer transistors are required to implement a given function. For example, the implementation of the AND gate in Figure 6-33 requires 4 transistors (including the inverter required to invert B), while a complementary CMOS implementation would require 6 transistors. The reduced number of devices has the additional advantage of lower capacitance.

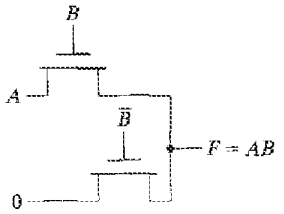


Figure 6-33 Pass-transistor implementation of an AND gate.

Unfortunately, as discussed earlier, an NMOS device is effective at passing a 0, but it is poor at pulling a node to V_{DD}. When the pass-transistor pulls a node high, the output only charges up to $V_{DD} - V_{Tn}$. In fact, the situation is worsened by the fact that the devices experience body effect, because a significant source-to-body voltage is present when pulling high. Consider the case in which the pass-transistor is charging up a node with the gate and drain terminals set at V_{DD}. Let the source of the NMOS pass-transistor be labeled x. The node x will charge up to $V_{DD} - V_{Tn}(V_x)$. We obtain

$$V_x = V_{DD} - (V_{tn0} + \gamma((\sqrt{|2\phi_f| + V_x}) - \sqrt{|2\phi_f|})) \tag{6.30}$$

Example 6.9 Voltage Swing for Pass-Transistors Circuits

The transient response of Figure 6-34 shows an NMOS charging up a capacitor. The drain voltage of the NMOS is at V_{DD}, and its gate voltage is being ramped from 0 V to V_{DD}. Assume that node x is initially at 0 V. We observe that the output initially charges up quickly, but the tail end of the transient is slow. The current drive of the transistor (gate-to-source voltage) is reduced significantly as the output approaches $V_{DD} - V_{Tn}$, and the current available to charge up node x is reduced drastically. Manual calculation using Eq. (6.30) results in an output voltage of 1.8 V, which is close to the simulated value.

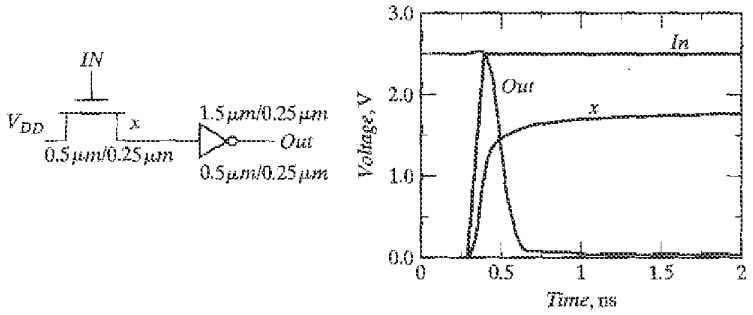


Figure 6-34 Transient response of charging up a node using an *N* device. Notice the slow tail after an initial quick response. $V_{DD} = 2.5$ V.

WARNING: The preceding example demonstrates that **pass-transistor gates cannot be cascaded by connecting the output of a pass gate to the gate input of another pass-transistor.** This is illustrated in Figure 6-35a, where the output of M_1 (node x) drives the gate of another MOS device. Node x can charge up to $V_{DD} - V_{Tn1}$. If node C has a rail-to-rail swing, node Y only charges up to the voltage on node $x - V_{Tn2}$, which works out to $V_{DD} - V_{Tn1} - V_{Tn2}$. Figure 6-35b, on the other hand, has the output of M_1 (x) driving the junction of M_2, and there is only one threshold drop. This is the proper way of cascading pass gates.

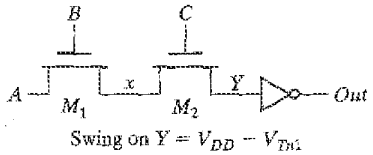


Figure 6-35 Pass-transistor output (drain–source) terminal should not drive other gate terminals to avoid multiple threshold drops.

Example 6.10 VTC of the Pass-Transistor AND Gate

The voltage transfer curve of a pass-transistor gate shows little resemblance to complementary CMOS. Consider the AND gate shown in Figure 6-36. Similar to complementary CMOS, the VTC of pass-transistor logic is data dependent. For the case when $B = V_{DD}$, the top pass-transistor is turned *on*, while the bottom one is turned *off*. In this case, the output just follows the input A until the input is high enough to turn *off* the top pass-transistor (i.e., reaches $V_{DD} - V_{Tn}$). Next, consider the case in which $A = V_{DD}$, and B makes a transition from $0 \rightarrow 1$. Since the inverter has a threshold of $V_{DD}/2$, the bottom pass-transistor is turned *on* until then and the output remains close to zero. Once the bottom pass-transistor turns *off*, the output follows the input B minus a threshold drop. A similar behavior is observed when both inputs A and B transition from $0 \rightarrow 1$.

Observe that a pure pass-transistor gate is not regenerative. A gradual signal degradation will be observed after passing through a number of subsequent stages. This can be remedied by the occasional insertion of a CMOS inverter. With the inclusion of an inverter in the signal path, the VTC resembles one of the CMOS gates.

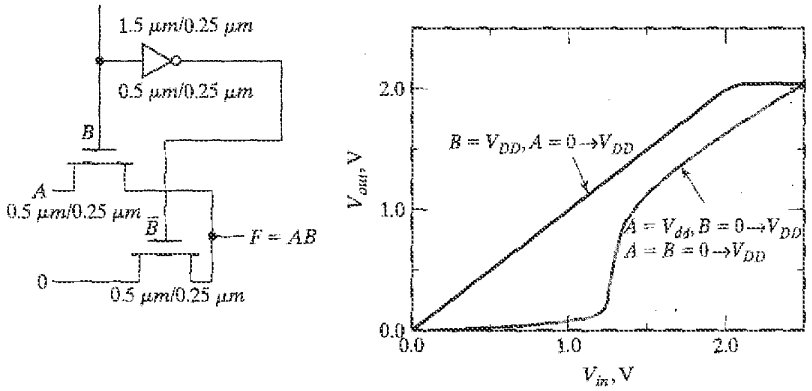


Figure 6-36 Voltage transfer characteristic for the pass-transistor AND gate of Figure 6-33.

Pass-transistors require lower switching energy to charge up a node, due to the reduced voltage swing. For the pass-transistor circuit in Figure 6-34, assume that the drain voltage is at

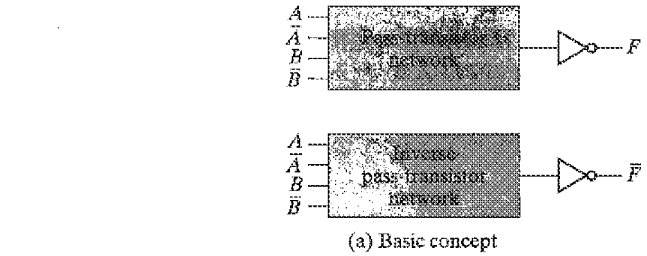
V_{DD} and the gate voltage transitions to V_{DD}. The output node charges from 0V to $V_{DD} - V_{Tn}$ (assuming that node x was initially at 0V), and the energy drawn from the power supply for charging the output of a pass-transistor is given by

$$E_{0\to 1} = \int_0^T P(t)dt = V_{DD}\int_0^T i_{supply}(t)dt$$
$$= V_{DD}\int_0^{(V_{DD}-V_{Tn})} C_L dV_{out} = C_L \cdot V_{DD}\cdot(V_{DD}-V_{Tn}) \tag{6.31}$$

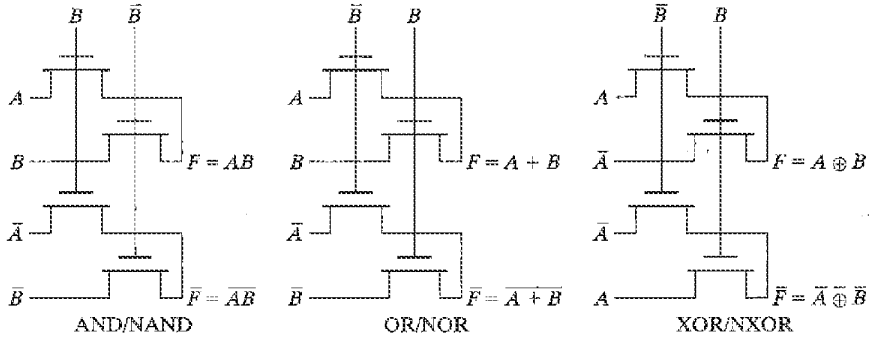
While the circuit exhibits lower switching power, it may also consume static power when the output is high—the reduced voltage level may be insufficient to turn off the PMOS transistor of the subsequent CMOS inverter.

Differential Pass-Transistor Logic

For high performance design, a differential pass-transistor logic family, called *CPL* or *DPL*, is commonly used. The basic idea (similar to DCVSL) is to accept true and complementary inputs and produce true and complementary outputs. Several CPL gates (AND/NAND, OR/NOR, and XOR/NXOR) are shown in Figure 6-37. These gates possess some interesting properties:



(a) Basic concept



(b) Example pass-transistor networks

Figure 6-37 Complementary pass-transistor logic (CPL).

- Since the circuits are *differential*, complementary data inputs and outputs are always available. Although generating the differential signals requires extra circuitry, the differential style has the advantage that some complex gates such as XORs and adders can be realized efficiently with a small number of transistors. Furthermore, the availability of both polarities of every signal eliminates the need for extra inverters, as is often the case in static CMOS or pseudo-NMOS.
- CPL belongs to the class of *static* gates, because the output-defining nodes are always connected to either V_{DD} or GND through a low-resistance path. This is advantageous for the noise resilience.
- The design is very modular. In effect, all gates use exactly the same topology. Only the inputs are permutated. This makes the design of a library of gates very simple. More complex gates can be built by cascading the standard pass-transistor modules.

Example 6.11 Four-Input NAND in CPL

Consider the implementation of a four-input AND/NAND gate using CPL. Based on the associativity of the boolean AND operation $[A \cdot B \cdot C \cdot D = (A \cdot B) \cdot (C \cdot D)]$, a two-stage approach has been adopted to implement the gate (Figure 6-38). The total number of transistors in the gate (including the final buffer) is 14. This is substantially higher than previously discussed gates.[3] This factor, combined with the complicated routing requirements, makes this circuit style not particularly efficient for this gate. One should, however, be aware of the fact that the structure simultaneously implements the AND and the NAND functions, which might reduce the transistor count of the overall circuit.

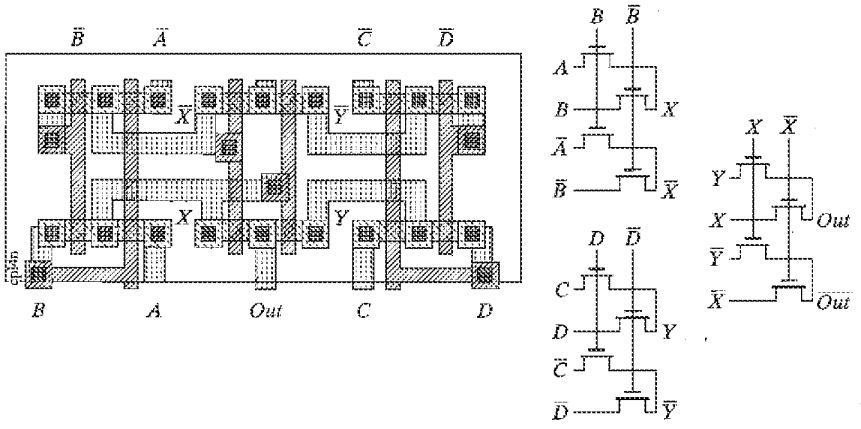


Figure 6-38 Layout and schematics of four-input NAND gate using CPL. The final inverter stage is omitted.

[3]This particular circuit configuration is only acceptable when zero-threshold pass-transistors are used. If not, it directly violates the concepts introduced in Figure 6-35.

In sum, CPL is a conceptually simple and modular logic style. Its applicability depends strongly on the logic function to be implemented. The availability of a simple XOR and the ease of implementing multiplexers makes it attractive for structures such as adders and multipliers. Some extremely fast and efficient implementations have been reported in that application domain [Yano90]. When considering CPL, the designer should not ignore the implicit routing overhead of the complementary signals, which is apparent in the layout of Figure 6-38.

Robust and Efficient Pass-Transistor Design

Unfortunately, differential pass-transistor logic, like single-ended pass-transistor logic, suffers from static power dissipation and reduced noise margins, since the high input to the signal-restoring inverter only charges up to $V_{DD} - V_{Tn}$. There are several solutions proposed to deal with this problem, outlined as follows:

Solution 1: Level Restoration A common solution to the voltage drop problem is the use of a *level restorer*, which is a single PMOS configured in a feedback path (see Figure 6-39). The gate of the PMOS device is connected to the output of the inverter its drain is connected to the input of the inverter and the source is connected to V_{DD}. Assume that node X is at 0V (*out* is at V_{DD} and the M_r is turned *off*) with $B = V_{DD}$ and $A = 0$. If input A makes a 0 to V_{DD} transition, M_n only charges up node X to $V_{DD} - V_{Tn}$. This is, however, enough to switch the output of the inverter low, turning on the feedback device M_r and pulling node X all the way to V_{DD}. This eliminates any static power dissipation in the inverter. Furthermore, no static current path can exist through the level restorer and the pass-transistor, since the restorer is only active when A is high. In sum, this circuit has the advantage that all voltage levels are either at GND or V_{DD}, and no static power is consumed.

While this solution is appealing in terms of eliminating static power dissipation, it adds complexity since the circuit is ratioed. The problem arises during the transition of node X from high to low (seeFigure 6-40). The pass-transistor network attempts to pull down node X, while

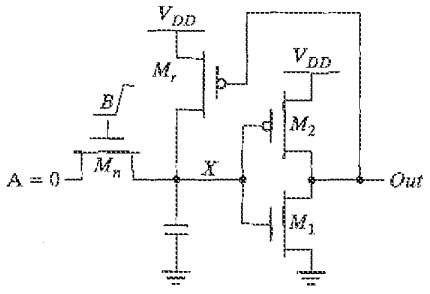


Figure 6-39 Transistor-sizing problem in level-restoring circuits.

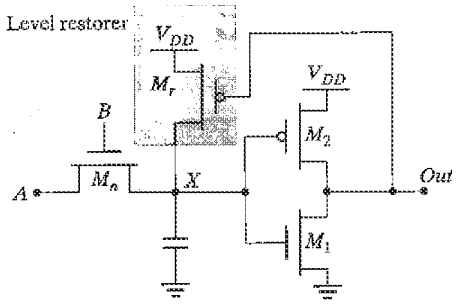


Figure 6-40 Level-restoring circuit.

the level restorer pulls X to V_{DD}. Therefore, the pull-down network, represented by M_n, must be stronger than the pull-up device Mr to switch node X (and the output). Careful transistor sizing is necessary to make the circuit function correctly. Assume the notation R_1 to denote the equivalent on-resistance of transistor M_1, R_2 for M_2, and R_r for M_r. When R_r is too small, it is impossible to bring the voltage at node X below the switching threshold of the inverter. Hence, the inverter output never switches to V_{DD}, and the gate is locked in a single state. The problem can be resolved by sizing transistors M_n and M_r such that the voltage at node X drops below the threshold of the inverter V_M, which is a function of R_1 and R_2. This condition is sufficient to guarantee the switching of the output voltage V_{out} to V_{DD} and the turning off of the level-restoring transistor.

Example 6.12 Sizing of a Level Restorer

Analyzing the circuit as a whole is nontrivial, because the restoring transistor acts as a feedback device. One way to simplify the circuit for manual analysis is to open the feedback loop and to ground the gate of the restoring transistor when determining the switching point (this is a reasonable assumption, as the feedback only becomes active once the inverter starts to switch). Hence, M_r and M_n form a configuration that resembles pseudo-NMOS with M_r the load transistor, and M_n acting as a pull-down network to GND. Assume that the inverter M_1, M_2 is sized to have its switching threshold at $V_{DD}/2$ (NMOS: 0.5 µm/0.25 µm and PMOS: 1.5 µm/0.25 µm). Therefore, node X must be pulled below $V_{DD}/2$ to switch the inverter and to shut off M_r.

This is confirmed in Figure 6-41, which shows the transient response as the size of the level restorer is varied, while keeping the size of M_n fixed (0.5 µm/0.25 µm). As the simulation indicates, for sizes above 1.5 µm/0.25 µm, node X cannot be brought below the switching threshold of the inverter, and can't switch the output.

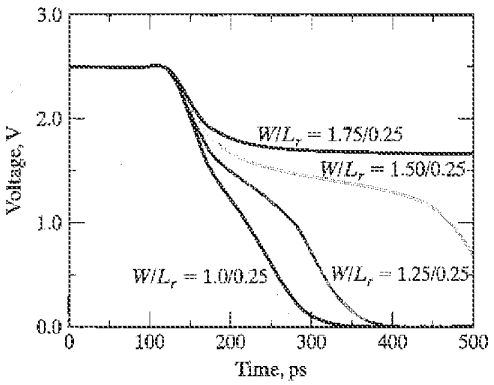


Figure 6-41 Transient response of the circuit in Figure 6-39. A level restorer that is too large results in incorrect evaluation.

Another concern is the influence of the level restorer on the switching speed of the device. Adding the restoring device increases the capacitance at the internal node X, slowing down the gate. In addiction, the rise time of the gate is affected negatively. The level restoring transistor M_r fights the decrease in voltage at node X before being switched off. On the other hand, the level restorer reduces the fall time, since the PMOS transistor, once turned on, accelerates the pull-up action.

Problem 6.6 Device Sizing in Pass-Transistors

For the circuit shown in Figure 6-39, assume that the pull-down device consists of six pass-transistors in series each with a device size of 0.5 μm/0.25 μm (replacing transistor M_n). Determine the maximum W–L size for the level restorer transistor for correct functionality.

A modification of the level restorer concept is shown in Figure 6-42. It is applicable in differential networks and is known as *swing-restored pass-transistor logic*. Instead of a simple inverter at the output of the pass-transistor network, two back-to-back inverters configured in a cross-coupled fashion are used for level restoration and performance improvement. Inputs are fed to both the gate and source–drain terminals, as in the case of conventional pass-transistor networks. Figure 6-42 shows a simple XOR/XNOR gate of three variables A, B, and C. The complementary network can be optimized by sharing transistors between the true and complementary outputs. This logic family comes with a major caveat: When cascading gates, buffers may have to be included in between the gates. If not, contention between the level-restoring devices of the cascaded gates negatively impacts the performance.

Solution 2: Multiple-Threshold Transistors A technology solution to the voltage-drop problem associated with pass-transistor logic is the use of multiple-threshold devices. Using *zero-*

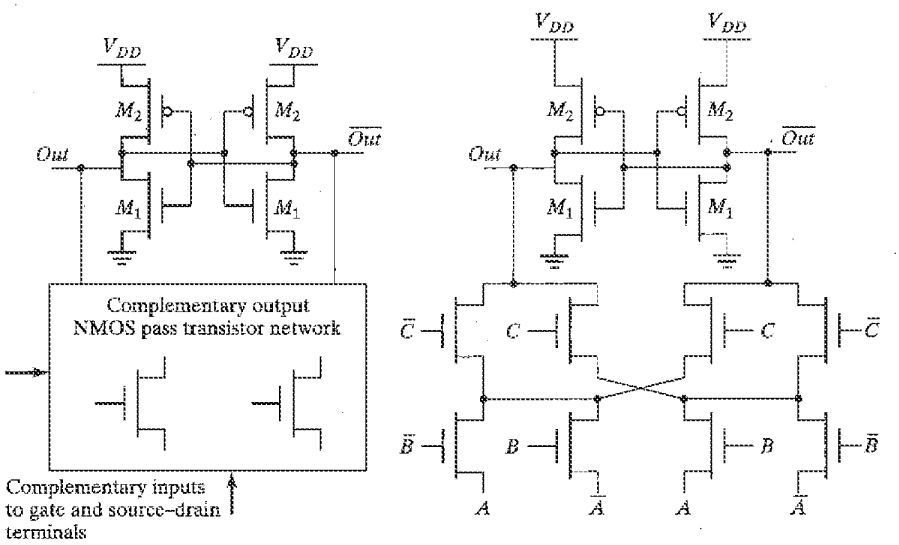


Figure 6-42 Swing-restored pass-transistor logic [Landman91, Parameswar96].

threshold devices for the NMOS pass-transistors eliminates most of the threshold drop, and passes a signal close to V_{DD}. All devices other than the pass-transistors (i.e., the inverters) are implemented using standard high-threshold devices. The use of multiple-threshold transistors is becoming more common, and involves simple modifications to existing process flows. Observe that even if the device implants were carefully calibrated to yield thresholds of exactly zero, the body effect of the device still would prevent a full swing to V_{DD}.

The use of zero-threshold transistors has some negative impact on the power consumption due to the subthreshold currents flowing through the pass-transistors, even if V_{GS} is below V_T. This is demonstrated in Figure 6-43, which points out a potential sneak dc-current path. While these leakage paths are not critical when the device is switching constantly, they do pose a significant energy overhead when the circuit is in the idle state.

Solution 3: Transmission-Gate Logic The most widely used solution to deal with the voltage-drop problem is the use of *transmission gates*.[4] This technique builds on the complementary properties of NMOS and PMOS transistors: NMOS devices pass a strong 0, but a weak 1, while PMOS transistors pass a strong 1 but a weak 0. The ideal approach is to use an NMOS to pull down and a PMOS to pull up. The transmission gate combines the best of both device flavors by placing an NMOS device in parallel with a PMOS device as in Figure 6-44a. The control

[4]The transmission gate is only one of the possible solutions. Other styles of pass-transistor networks that combine NMOS and PMOS transistors have been devised. Double pass-transistor logic (DPL) is an example of such [Bernstein98, pp. 84].

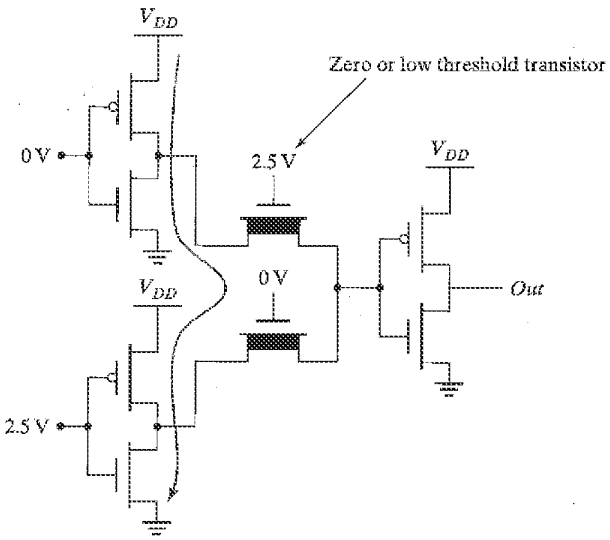
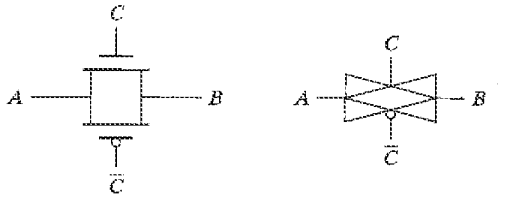


Figure 6-43 Static power consumption when using zero-threshold pass-transistors.



(a) Circuit (b) Symbolic representation

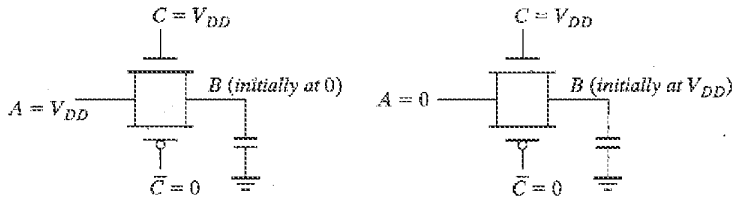
Figure 6-44 CMOS transmission gate.

signals to the transmission gate (C and $\overline{C}$) are complementary. The transmission gate acts as a bidirectional switch controlled by the gate signal C. When $C = 1$, both MOSFETs are on, allowing the signal to pass through the gate. In short,

$$A = B \quad \text{if} \quad C = 1 \tag{6.32}$$

On the other hand, $C = 0$ places both transistors in cutoff, creating an open circuit between nodes A and B. Figure 6-44b shows a commonly used transmission-gate symbol.

Consider the case of charging node B to V_{DD} for the transmission-gate circuit in Figure 6-45a. Node A is set at V_{DD}, and the transmission gate is enabled ($C = 1$ and $\overline{C} = 0$). If only the NMOS pass device were present, node B would only charge up to $V_{DD} - V_{Tn}$, at which point the NMOS device would turn off. However, since the PMOS device is present



(a) Charging node B (b) Discharging node B

Figure 6-45 Transmission gates enable rail-to-rail switching.

and is "on" ($V_{GSp} = -V_{DD}$), the output charges all the way up to V_{DD}. Figure 6-45b shows the opposite case—that is, discharging node B to 0. B is initially at V_{DD} when node A is driven low. The PMOS transistor by itself can only pull-down node B to V_{Tp} at which point it turns *off*. The parallel NMOS device stays turned on, however (since its $V_{GSn} = V_{DD}$), and pulls node B all the way to GND. Although the transmission gate requires two transistors and more control signals, it enables rail-to-rail swing.

Transmission gates can be used to build some complex gates very efficiently. Figure 6-46 shows an example of a simple inverting two-input multiplexer. This gate either selects input A or B on the basis of the value of the control signal S, which is equivalent to implementing the following Boolean function:

$$\overline{F} = (A \cdot S + B \cdot \overline{S}) \tag{6.33}$$

A complementary implementation of the gate requires eight transistors instead of six.

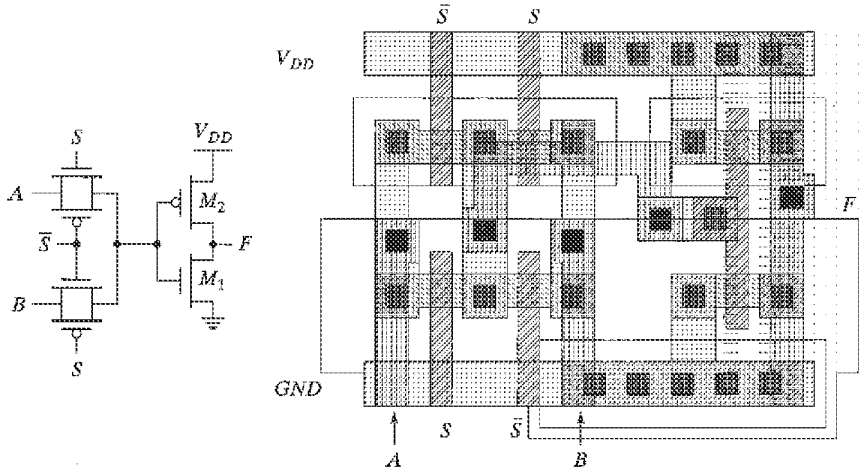


Figure 6-46 Transmission-gate multiplexer and its layout.

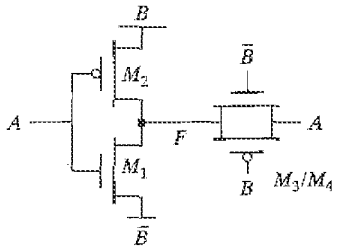


Figure 6-47 Transmission-gate XOR.

Another example of the effective use of transmission gates is the popular XOR circuit shown in Figure 6-47. The complete implementation of this gate requires only 6 transistors (including the inverter used for the generation of $\overline{B}$), compared with the 12 transistors required for a complementary implementation. To understand the operation of this circuit, we need only analyze the $B = 0$ and $B = 1$ cases separately. For $B = 1$, transistors M_1 and M_2 act as an inverter, while the transmission gate M_3/M_4 is off; hence, $F = \overline{A}B$. In the opposite case, M_1 and M_2 are disabled, and the transmission gate is operational, or $F = A\overline{B}$. The combination of both leads to the XOR function. Notice that regardless of the values of A and B, node F always has a connection to either V_{DD} or GND and thus is a low-impedance node. When designing static-pass-transistor networks, it is essential to adhere to the low-impedance rule under all circumstances. Other examples in which transmission-gate logic is effectively used are fast adder circuits and registers.

Performance of Pass-Transistor and Transmission-Gate Logic

The pass-transistor and the transmission gate are, unfortunately, not ideal switches, and they have a series resistance associated with them. To quantify the resistance, consider the circuit in Figure 6-48, which involves charging a node from 0 V to V_{DD}. In this discussion, we use the large-signal definition of resistance, which involves dividing the voltage across the switch by the drain current. The effective resistance of the switch is modeled as a parallel connection of the resistances R_n and R_p of the NMOS and PMOS devices, defined as $(V_{DD} - V_{out})/I_{Dn}$ and $(V_{DD} - V_{out})/(-I_{Dp})$, respectively. The currents through the devices obviously are dependent on the value of V_{out} and the operating mode of the transistors. During the low-to-high transition, the pass-transistors traverse through a number of operation modes. For low values of V_{out}, the NMOS device is saturated and the resistance is approximated as

$$R_p = \frac{V_{out} - V_{DD}}{I_{Dp}} = \frac{V_{out} - V_{DD}}{k_p \cdot \left((-V_{DD} - V_{Tp})(V_{out} - V_{DD}) - \dfrac{(V_{out} - V_{DD})^2}{2}\right)} \simeq \frac{1}{k_p(-V_{DD} - V_{Tp})} \tag{6.34}$$

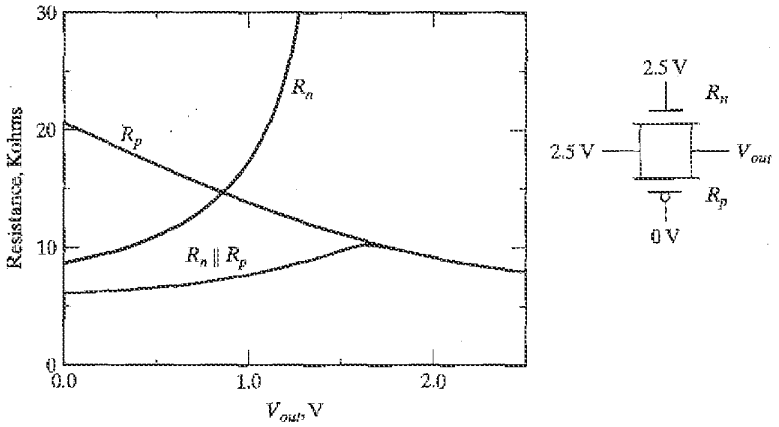


Figure 6-48 Simulated equivalent resistance of transmission gate for low-to-high transition (for $(W/L)_n = (W/L)_p = 0.5\ \mu m/0.25\ \mu m$). A similar response for overall resistance is obtained for the high-to-low transition.

The resistance goes up for increasing values of V_{out} and approaches infinity when V_{out} reaches $V_{DD} - V_{Tn}$ and the device shuts off. Similarly, we can analyze the behavior of the PMOS transistor. When V_{out} is small, the PMOS is saturated, but it enters the linear mode of operation for V_{out} approaching V_{DD}. This gives the following approximated resistance:

$$R_p = \frac{V_{out} - V_{DD}}{I_{Dp}} = \frac{V_{out} - V_{DD}}{k_p \cdot \left((-V_{DD} - V_{Tp})(V_{out} - V_{DD}) - \frac{(V_{out} - V_{DD})^2}{2} \right)} \tag{6.35}$$

$$= \frac{1}{k_p(-V_{DD} - V_{Tp})}$$

The simulated value of $R_{eq} = R_p \parallel R_n$ as a function of V_{out} is plotted in Figure 6-48. It can be observed that R_{eq} is relatively constant ($\approx 8\ k\Omega$ in this particular case). The same is true in other design instances (for example, when discharging C_L). When analyzing transmission-gate networks, the simplifying assumption that the switch has a constant resistive value is therefore acceptable.

Problem 6.7 Equivalent Resistance during Discharge

Determine the equivalent resistance by simulation for the high-to-low transition of a transmission gate. (In other words, produce a plot similar to the one presented in Figure 6-48).

An important consideration is the delay associated with a chain of transmission gates. Figure 6-49 shows a chain of n transmission gates. Such a configuration often occurs in circuits such as adders or deep multiplexors. Assume that all transmission gates are turned on and a step

Obviously, the number of switches per segment grows with increasing values of t_{buf}. In current technologies, m_{opt} typically equals 3 or 4. The presented analysis ignores that tp_{buf} itself is a function of the load m. A more accurate analysis taking this factor into account is presented in Chapter 9.

Example 6.14 Transmission-Gate Chain

Consider the same 16-transmission-gate chain. The buffers shown in Figure 6-51 can be implemented as inverters (instead of two cascaded inverters). In some cases, it might be necessary to add an extra inverter to produce the correct polarity. Assuming that each inverter is sized such that the NMOS is 0.5 µm/0.25 µm and PMOS is 0.5 µm /0.25 µm, Eq. (6.39) predicts that an inverter must be inserted every 3 transmission gates. The simulated delay when placing an inverter every two transmission gates is 154 ps; for every three transmission gates, the delay is 154 ps; and for four transmission gates, it is 164 ps. The insertion of buffering inverters reduces the delay by a factor of almost 2.

CAUTION: Although many of the circuit styles discussed in the previous sections sound very interesting, and might be superior to static CMOS in many respects, none has the *robustness and ease of design* of complementary CMOS. Therefore, use them sparingly and with caution. For designs that have no extreme area, complexity, or speed constraints, complementary CMOS is the recommended design style.

6.3 Dynamic CMOS Design

It was noted earlier that static CMOS logic with a fan-in of N requires $2N$ devices. A variety of approaches were presented to reduce the number of transistors required to implement a given logic function including pseudo-NMOS, pass-transistor logic, etc. The pseudo-NMOS logic style requires only $N + 1$ transistors to implement an N input logic gate, but unfortunately it has static power dissipation. In this section, an alternate logic style called *dynamic logic* is presented that obtains a similar result, while avoiding static power consumption. With the addition of a clock input, it uses a sequence of *precharge* and conditional *evaluation* phases.

6.3.1 Dynamic Logic: Basic Principles

The basic construction of an (n-type) dynamic logic gate is shown in Figure 6-52a. The PDN (pull-down network) is constructed exactly as in complementary CMOS. The operation of this circuit is divided into two major phases—*precharge* and *evaluation*—with the mode of operation determined by the *clock signal CLK*.

Precharge

When $CLK = 0$, the output node *Out* is precharged to V_{DD} by the PMOS transistor M_p. During that time, the evaluate NMOS transistor M_e is off, so that the pull-down path is disabled. The

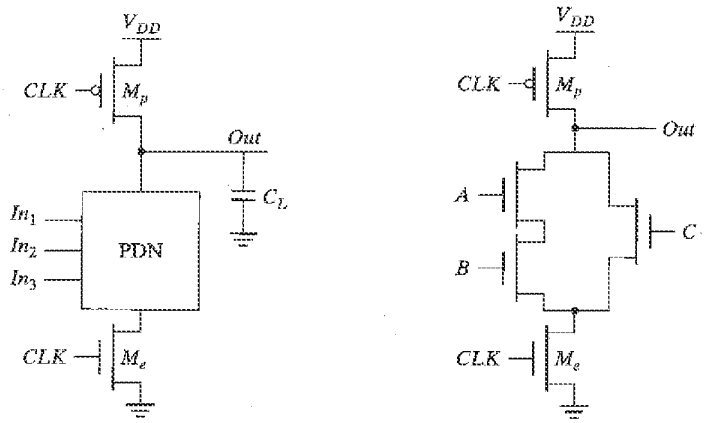


Figure 6-52 Basic concepts of a dynamic gate.

evaluation FET eliminates any static power that would be consumed during the precharge period (i.e., static current would flow between the supplies if both the pull-down and the precharge device were turned on simultaneously).

Evaluation

For $CLK = 1$, the precharge transistor M_p is off, and the evaluation transistor M_e is turned on. The output is conditionally discharged based on the input values and the pull-down topology. If the inputs are such that the PDN conducts, then a low resistance path exists between *Out* and GND, and the output is discharged to GND. If the PDN is turned off, the precharged value remains stored on the output capacitance C_L, which is a combination of junction capacitances, the wiring capacitance, and the input capacitance of the fan-out gates. During the evaluation phase, the only possible path between the output node and a supply rail is to GND. Consequently, once *Out* is discharged, it cannot be charged again until the next precharge operation. **The inputs to the gate can thus make at most one transition during evaluation.** Notice that the output can be in the *high-impedance state* during the evaluation period if the pull-down network is turned off. This behavior is fundamentally different from the static counterpart that always has a low resistance path between the output and one of the power rails.

As an example, consider the circuit shown in Figure 6-52b. During the precharge phase ($CLK = 0$), the output is precharged to V_{DD} regardless of the input values, because the evaluation device is turned off. During evaluation ($CLK = 1$), a conducting path is created between *Out* and GND if (and only if) $A \cdot B + C$ is TRUE. Otherwise, the output remains at the precharged state of V_{DD}. The following function is thus realized:

$$Out = \overline{CLK} + \overline{(A \cdot B + C)} \cdot CLK \tag{6.40}$$

A number of important properties can be derived for the dynamic logic gate:

- The logic function is implemented by the NMOS pull-down network. The construction of the PDN proceeds just as it does for static CMOS.
- The *number of transistors* (for complex gates) is substantially lower than in the static case: $N + 2$ versus $2N$.
- It is *nonratioed*. The sizing of the PMOS precharge device is not important for realizing proper functionality of the gate. The size of the precharge device can be made large to improve the low-to-high transition time (of course, at a cost to the high-to-low transition time). There is, however, a trade-off with power dissipation, since a larger precharge device directly increases clock-power dissipation.
- It only consumes *dynamic power*. Ideally, no static current path ever exists between V_{DD} and GND. The overall power dissipation, however, can be significantly higher compared with a static logic gate.
- The logic gates have *faster switching speeds*, for two main reasons. The first (obvious) reason is due to the reduced load capacitance attributed to the lower number of transistors per gate and the single-transistor load per *fan-in*. This translates in a *reduced logical effort*. For instance, the logical effort of a two-input dynamic NOR gate equals 2/3, which is substantially smaller than the 5/3 of its static CMOS counterpart. The second reason is that the dynamic gate does not have short circuit current, and all the current provided by the pull-down devices goes towards discharging the load capacitance.

The low and high output levels of V_{OL} and V_{OH} are easily identified as GND and V_{DD}, and they are not dependent on the transistor sizes. The other VTC parameters are dramatically different from static gates. Noise margins and switching thresholds have been defined as static quantities that are not a function of time. To be functional, a dynamic gate requires a periodic sequence of precharges and evaluations. Pure static analysis, therefore, does not apply. During the evaluation period, the pull-down network of a dynamic inverter starts to conduct when the input signal exceeds the threshold voltage (V_{Tn}) of the NMOS pull-down transistor. Therefore, it is reasonable to assume that the switching threshold (V_M) as well as V_{IH} and V_{IL} are equal to V_{Tn}. This translates to a low value for the NM_L.

Design Consideration

It is also possible to implement dynamic logic using the dual approach, where the output node is connected by a predischarge NMOS transistor to GND, and the evaluation PUN network is implemented in PMOS. The operation is similar: During precharge, the output node is discharged to GND; during evaluation, the output is conditionally charged to V_{DD}. This p-type dynamic gate has the disadvantage of being slower than the n-type because of the lower current drive of the PMOS transistors. ■

6.3.2 Speed and Power Dissipation of Dynamic Logic

The main advantages of dynamic logic are increased speed and reduced implementation area. Fewer devices to implement a given logic function implies that the overall load capacitance is much smaller. The analysis of the switching behavior of the gate has some interesting peculiarities to it. After the precharge phase, the output is high. For a low input signal, no additional switching occurs. As a result, $t_{pLH} = 0$! The high-to-low transition, on the other hand, requires the discharging of the output capacitance through the pull-down network. Therefore, t_{pHL} is proportional to C_L and the current-sinking capabilities of the pull-down network. The presence of the evaluation transistor slows the gate somewhat, as it presents an extra series resistance. Omitting this transistor, while functionally not forbidden, may result in static power dissipation and potentially a performance loss.

The preceding analysis is somewhat unfair because it ignores the influence of the precharge time on the switching speed of the gate. The precharge time is determined by the time it takes to charge C_L through the PMOS precharge transistor. During this time, the logic in the gate cannot be utilized. Very often, however, the overall digital system can be designed in such a way that the precharge time coincides with other system functions. For instance, the precharge of the arithmetic unit in a microprocessor could coincide with the instruction decode. The designer has to be aware of this "dead zone" in the use of dynamic logic and thus should carefully consider the pros and cons of its usage, taking the overall system requirements into account.

Example 6.15 A Four-Input Dynamic NAND Gate

Figure 6-53 shows the design of a four-input NAND example designed using the dynamic-circuit style. Due to the dynamic nature of the gate, the derivation of the voltage-transfer

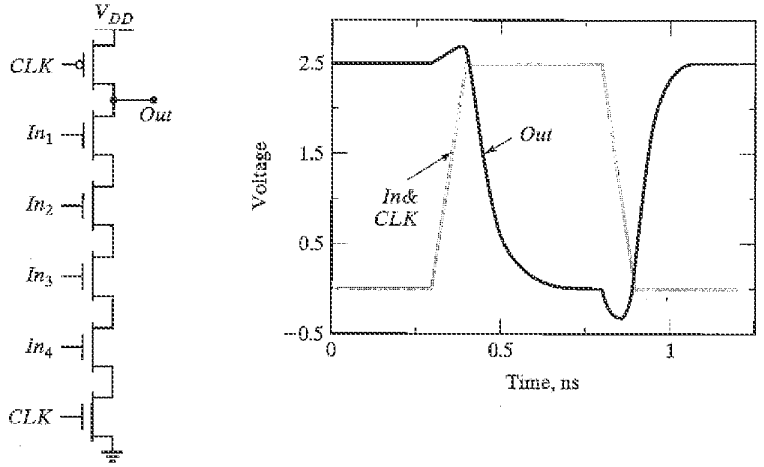


Figure 6-53 Schematic and transient response of a four-input dynamic NAND gate.

characteristic diverges from the traditional approach. As discussed earlier, we assume that the switching threshold of the gate equals the threshold of the NMOS pull-down transistor. This results in asymmetrical noise margins, as shown in Table 6-10.

Table 6-10 The dc and ac parameters of a four-input dynamic NAND.

Transistors	V_{OH}	V_{OL}	V_M	NM_H	NM_L	t_{pHL}	t_{pLH}	t_{pre}
6	2.5 V	0 V	V_{TN}	$2.5 - V_{TN}$	V_{TN}	110 ps	0 ps	83 ps

The dynamic behavior of the gate is simulated with SPICE. It is assumed that all inputs are set high when the clock goes high. On the rising edge of the clock, the output node is discharged. The resulting transient response is plotted in Figure 6-53, and the propagation delays are summarized in Table 6-10. The duration of the precharge cycle can be adjusted by changing the size of the PMOS precharge transistor. Making the PMOS too large should be avoided, however, as it both slows down the gate and increases the capacitive load on the clock line. For large designs, the latter factor might become a major design concern because the clock load can become excessive and hard to drive.

As mentioned earlier, the static gate parameters are time dependent. To illustrate this, consider a four-input NAND gate with all the partial inputs tied together, and are making a low-to-high transition. Figure 6-54 shows a transient simulation of the output voltage for three different input transitions—from 0 to 0.45 V, 0.5 V and 0.55 V, respectively. In the preceding discussion, we have defined the switching threshold of the dynamic gate as the device threshold. However, notice that the amount by which the output voltage drops is a strong function of the input voltage and the *available evaluation time*. The noise voltage needed to corrupt the signal has to be larger if the evaluation time is short. In other words, the switching threshold is truly time dependent.

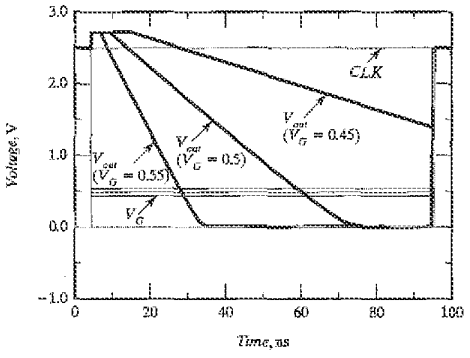


Figure 6-54 Effect of an input glitch on the output. The switching threshold depends on the time for evaluation. A larger glitch is acceptable if the evaluation phase is shorter.

It would appear that dynamic logic presents a significant advantage from a power perspective. There are three reasons for this. First, the physical capacitance is lower since dynamic logic uses fewer transistors to implement a given function. Also, the load seen for each fan-out is one transistor instead of two. Second, dynamic logic gates *by construction* can have at most one transition per clock cycle. Glitching (or dynamic hazards) does not occur in dynamic logic. Finally, dynamic gates do not exhibit short-circuit power since the pull-up path is not turned on when the gate is evaluating.

While these arguments generally are true, they are offset by other considerations: (1) the clock power of dynamic logic can be significant, particularly since the clock node has a guaranteed transition on every single clock cycle; (2) the number of transistors is greater than the minimal set required for implementing the logic; (3) short-circuit power may exist when leakage-combatting devices are added (as will be discussed further); and (4), most importantly, dynamic logic generally displays a higher switching activity due to the periodic *precharge* and *discharge* operations. Earlier, the transition probability for a static gate was shown to be $p_0 p_1 = p_0 (1 - p_0)$. For dynamic logic, the output transition probability does not depend on the state (history) of the inputs, but rather on the signal probabilities. For an n-tree dynamic gate, the output makes a $0 \rightarrow 1$ transition during the precharge phase only if the output was discharged during the preceding evaluate phase. Hence, the $0 \rightarrow 1$ transition probability for an n-type dynamic gate is given by

$$a_{0 \rightarrow 1} = p_0 \tag{6.41}$$

where p_0 is the probability that the output is zero. This number is always greater than or equal to $p_0 p_1$. For uniformly distributed inputs, the transition probability for an N-input gate is

$$a_{0 \rightarrow 1} = \frac{N_0}{2^N} \tag{6.42}$$

where N_0 is the number of zero entries in the truth table of the logic function.

Example 6.16 Activity Estimation in Dynamic Logic

To illustrate the increased activity for a dynamic gate, consider again a two-input NOR gate. An n-tree dynamic implementation is shown in Figure 6-55, along with its static counterpart. For equally probable inputs, there is a 75% probability that the output node of the dynamic gate discharges immediately after the precharge phase; implying that the activity for such a gate equals 0.75 (i.e., $P_{NOR} = 0.75\ C_L V_{dd}^2 f_{clk}$). The corresponding activity is a lot smaller, 3/16, for a static implementation. For a dynamic NAND gate, the transition probability is 1/4 (since there is a 25% probability the output will be discharged) while it is 3/16 for a static implementation. Although these examples illustrate that the switching activity of dynamic logic is generally higher, it should be noted that dynamic logic has lower physical capacitance. Both factors must be accounted for when analyzing dynamic power dissipation.

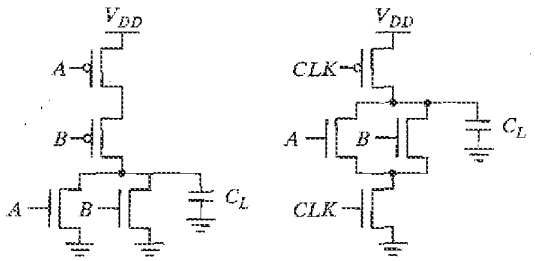


Figure 6-55 Static NOR versus *n*-type dynamic NOR.

Problem 6.8 Activity Computation

For the four-input dynamic NAND gate, compute the activity factor with the following assumption for the inputs: They are independent, and $p_{A=1} = 0.2$, $p_{B=1} = 0.3$, $p_{C=1} = 0.5$, and $p_{D=1} = 0.4$.

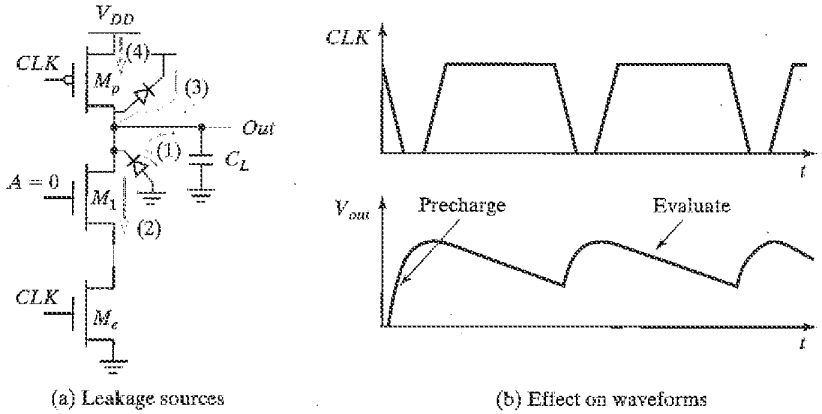
6.3.3 Signal Integrity Issues in Dynamic Design

Dynamic logic clearly can result in high-performance solutions compared to static circuits. However, there are several important considerations that must be taken into account if one wants dynamic circuits to function properly. These include charge leakage, charge sharing, capacitive coupling, and clock feedthrough. These issues are discussed in some detail in this section.

Charge Leakage

The operation of a dynamic gate relies on the dynamic storage of the output value on a capacitor. If the pull-down network is *off*, ideally, the output should remain at the precharged state of V_{DD} during the evaluation phase. However, this charge gradually leaks away due to leakage currents, eventually resulting in a malfunctioning of the gate. Figure 6-56a shows the sources of leakage for the basic dynamic inverter circuit.

Source 1 and 2 are the *reverse-biased diode* and *subthreshold leakage* of the NMOS pull-down device M_1, respectively. The charge stored on C_L will slowly leak away through these leakage channels, causing a degradation in the high level (Figure 6-56b). Dynamic circuits therefore require a minimal clock rate, which is typically on the order of a few kHz. This makes the usage of dynamic techniques unattractive for low-performance products such as watches, or processors that use conditional clocks (where there are no guarantees on minimum clock rates). Note that the PMOS precharge device also contributes some leakage current due to the reverse bias diode (source 3) and the subthreshold conduction (source 4). To some extent, the leakage current of the PMOS counteracts the leakage of the pull-down path. As a result, the output voltage is going to be set by the resistive divider composed of the pull-down and pull-up paths.



(a) Leakage sources (b) Effect on waveforms

Figure 6-56 Leakag e issues in dynamic circuits.

Example 6.17 Leakage in Dynamic Circuits

Consider the simple inverter with all devices set at 0.5 μm/0.25 μm. Assume that the input is low during the evaluation period. Ideally, the output should remain at the precharged state of V_{DD}. However, as seen from Figure 6-57, the output voltage drops. Once the output drops below the switching threshold of the fan-out logic gate, the output is interpreted as a low voltage. Notice that the output settles to an intermediate voltage, due to the leakage current provided by the PMOS pull-up.

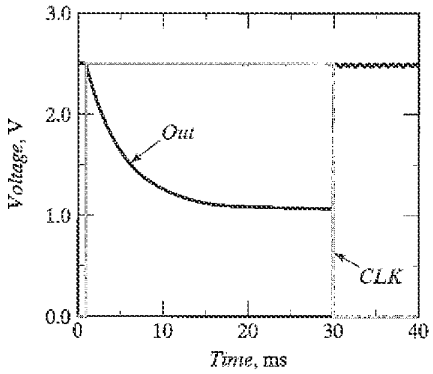


Figure 6-57 Impact of charge leakage. The output settles to an intermediate voltage determined by a resistive divider of the pull-down and pull-up devices.

Leakage is caused by the high-impedance state of the output node during the evaluate mode, when the pull-down path is turned off. The leakage problem may be counteracted by reducing the output impedance on the output node during evaluation. This often is done by

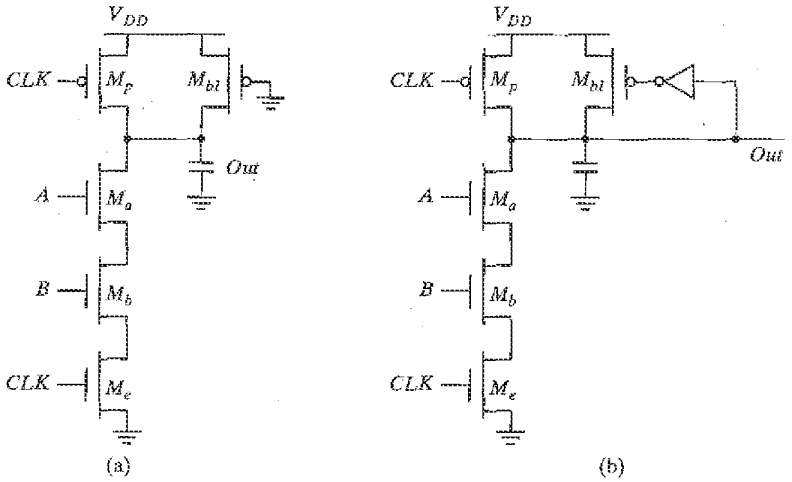


Figure 6-58 Static bleeders compensate for the charge leakage.

adding a *bleeder transistor*, as shown in Figure 6-58a. The only function of the bleeder—an NMOS style pull-up device—is to compensate for the charge lost due to the pull-down leakage paths. To avoid the ratio problems associated with this style of circuit and the associated static power consumption, the bleeder resistance is made high (in other words, the device is kept small). This allows the (strong) pull-down devices to lower the *Out* node substantially below the switching threshold of the next gate. Often, the bleeder is implemented in a feedback configuration to eliminate the static power dissipation altogether (Figure 6-58b).

Charge Sharing

Another important concern in dynamic logic is the impact of charge sharing. Consider the circuit in Figure 6-59. During the precharge phase, the output node is precharged to V_{DD}. Assume that all inputs are set to 0 during precharge, and that the capacitance C_a is discharged. Assume further that input B remains at 0 during evaluation, while input A makes a $0 \rightarrow 1$ transition, turning transistor M_a on. The charge stored originally on capacitor C_L is redistributed over C_L and C_a. This causes a drop in the output voltage, which cannot be recovered due to the dynamic nature of the circuit.

The influence on the output voltage is readily calculated. Under the assumptions given previously, the following initial conditions are valid: $V_{out}(t = 0) = V_{DD}$ and $V_X(t = 0) = 0$. As a result, two possible scenarios must be considered:

1. $\Delta V_{out} < V_{Tn}$. In this case, the final value of V_X equals $V_{DD} - V_{Tn}(V_X)$. Charge conservation then yields

$$C_L V_{DD} = C_L V_{out}(\text{final}) + C_a[V_{DD} - V_{Tn}(V_X)]$$

or

$$\Delta V_{out} = V_{out}(\text{final}) + (-V_{DD}) = -\frac{C_a}{C_L}[V_{DD} - V_{Tn}(V_X)] \tag{6.43}$$

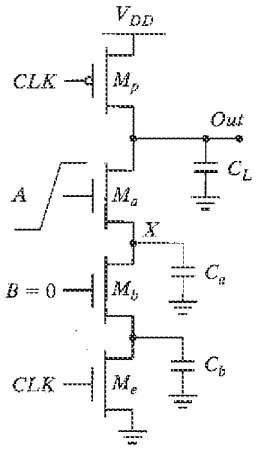


Figure 6-59 Charge sharing in dynamic networks.

2. $\Delta V_{out} > V_{Tn}$. V_{out} and V_X then reach the same value:

$$\Delta V_{out} = -V_{DD}\left(\frac{C_a}{C_a + C_L}\right) \tag{6.44}$$

We determine which of these scenarios is valid by the capacitance ratio. The boundary condition between the two cases can be determined by setting ΔV_{out} equal to V_{Tn} in Eq. (6.44), yielding

$$\frac{C_a}{C_L} = \frac{V_{Tn}}{V_{DD} - V_{Tn}} \tag{6.45}$$

Case 1 holds when the (C_a/C_L) ratio is smaller than the condition defined in Eq. (6.45). If not, Eq. (6.44) is valid. Overall, it is desirable to keep the value of ΔV_{out} below $|V_{Tp}|$. The output of the dynamic gate might be connected to a static inverter, in which case the low level of V_{out} would cause static power consumption. One major concern is a circuit malfunction if the output voltage is brought below the switching threshold of the gate it drives.

Example 6.18 Charge Sharing

Let us consider the impact of charge sharing on the dynamic logic gate shown in Figure 6-60, which implements a three-input EXOR function $y = A \oplus B \oplus C$. The first question to be resolved is what conditions cause the worst case voltage drop on node y. For simplicity, ignore the load inverter, and assume that all inputs are low during the precharge operation and that all isolated internal nodes (V_a, V_b, V_c, and V_d) are initially at 0 V.

Inspection of the truth table for this particular logic function shows that the output stays high for 4 out of 8 cases. The worst case change in output is obtained by exposing the maximum amount of internal capacitance to the output node during the evaluation

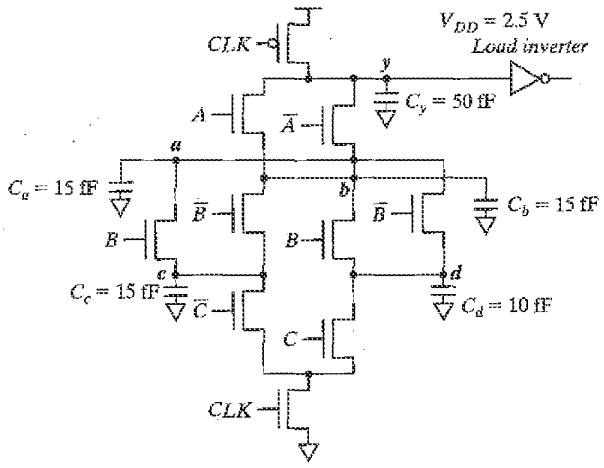


Figure 6-60 Example illustrating the charge-sharing effect in dynamic logic.

period. This happens for $\overline{A}\ B\ C$ or $A\ \overline{B}\ C$. The voltage change can then be obtained by equating the initial charge with the final charge as done with equation Eq. (6.44), yielding a worst case change of 30/(30 + 50) * 2.5 V = 0.94 V. To ensure that the circuit functions correctly, the switching threshold of the connecting inverter should be placed below 2.5 – 0.94 = 1.56 V.

The most common and effective approach to deal with the charge redistribution is to also precharge critical internal nodes, as shown in Figure 6-61. Since the internal nodes are charged

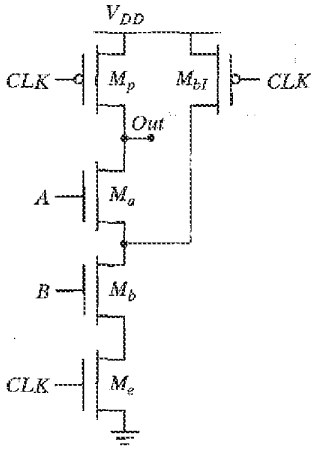


Figure 6-61 Dealing with charge sharing by precharging internal nodes. An NMOS precharge transistor may also be used, but this requires an inverted clock.

to V_{DD} during precharge, charge sharing does not occur. This solution obviously comes at the cost of increased area and capacitance.

Capacitive Coupling

The relatively high impedance of the output node makes the circuit very sensitive to crosstalk effects. A wire routed over or next to a dynamic node may couple capacitively and destroy the state of the floating node. Another equally important form of capacitive coupling is *backgate (*or *output-to-input) coupling*. Consider the circuit shown in Figure 6-62a, in which a dynamic two-input NAND gate drives a static NAND gate. A transition in the input *In* of the static gate may cause the output of the gate (Out_2) to go low. This output transition couples capacitively to the other input of the gate (the dynamic node Out_1) through the gate–source and gate–drain capacitances of transistor M_4. A simulation of this effect is shown in Figure 6-62b. It demonstrates how the coupling causes the output of the dynamic gate Out_1 to drop significantly. This further causes the output of the static NAND gate not to drop all the way down to 0 V and a small amount of static power to be dissipated. If the voltage drop is large enough, the circuit can evaluate incorrectly, and the NAND output may not go low. When designing and laying out dynamic circuits, special care is needed to minimize capacitive coupling.

Clock Feedthrough

A special case of capacitive coupling is clock feedthrough, an effect caused by the capacitive coupling between the clock input of the precharge device and the dynamic output node. The coupling capacitance consists of the gate-to-drain capacitance of the precharge device, and includes both the overlap and channel capacitances. This capacitive coupling causes the output of the dynamic node to rise above V_{DD} on the low-to-high transition of the clock, assuming that the pull-down network is turned off. Subsequently, the fast rising and falling edges of the clock couple onto the signal node, as is quite apparent in the simulation of Figure 6-62b.

The danger of clock feedthrough is that it may cause the normally reverse-biased junction diodes of the precharge transistor to become forward biased. This causes electron injection into the substrate, which can be collected by a nearby high-impedance node in the 1 state, eventually resulting in faulty operation. CMOS latchup might be another result of this injection. For all purposes, high-speed dynamic circuits should be carefully simulated to ensure that clock feedthrough effects stay within bounds.

All of the preceding considerations demonstrate that the design of dynamic circuits is rather tricky and requires extreme care. It should therefore be attempted only when high performance is required, or high quality design-automation tools are available.

6.3.4 Cascading Dynamic Gates

Besides the signal integrity issues, there is one major catch that complicates the design of dynamic circuits: Straightforward cascading of dynamic gates to create multilevel logic structures does not work. The problem is best illustrated with two cascaded *n*-type dynamic

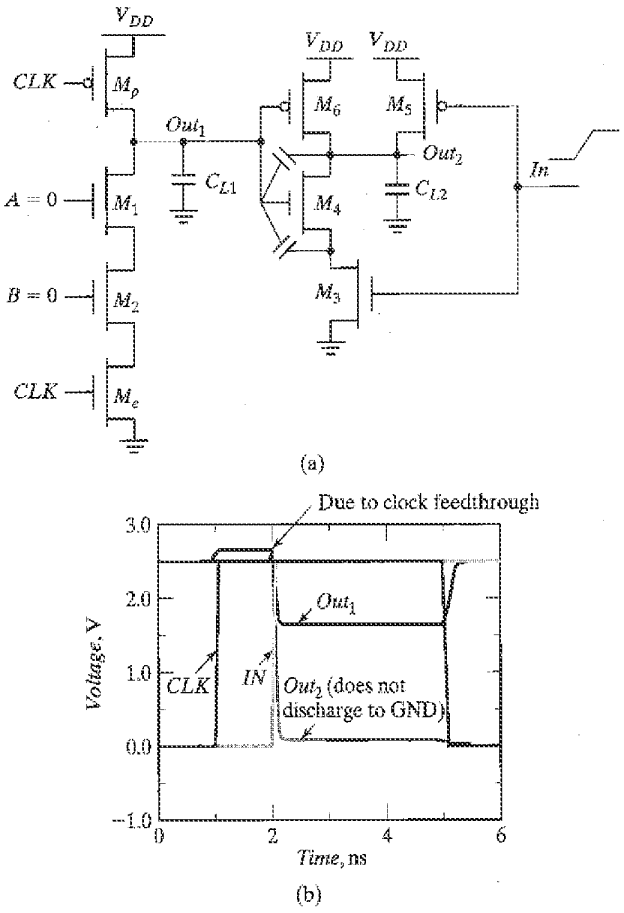


Figure 6-62 Example demonstrating the effect of backgate coupling: (a) circuit schematics; (b) simulation results.

inverters, shown in Figure 6-63a. During the precharge phase (i.e., $CLK = 0$), the outputs of both inverters are precharged to V_{DD}. Assume that the primary input *In* makes a $0 \rightarrow 1$ transition (Figure 6-63b). On the rising edge of the clock, output Out_1 starts to discharge. The second output should remain in the precharged state of V_{DD} as its expected value is 1 (Out_1 transitions to 0 during evaluation). However, there is a finite propagation delay for the input to discharge Out_1 to GND. Therefore, the second output also starts to discharge. As long as Out_1 exceeds the switching threshold of the second gate, which approximately equals V_{Tn}, a conducting path exists between Out_2 and GND, and precious charge is lost at Out_2. The conducting path is only disabled once Out_1 reaches V_{Tn}, and turns off the NMOS pull-down transistor. This leaves Out_2 at an intermediate voltage level. The correct level will not be recovered, because dynamic gates rely on capacitive storage, in contrast to static gates, which have dc restoration. The charge loss leads to reduced noise margins and potential malfunctioning.

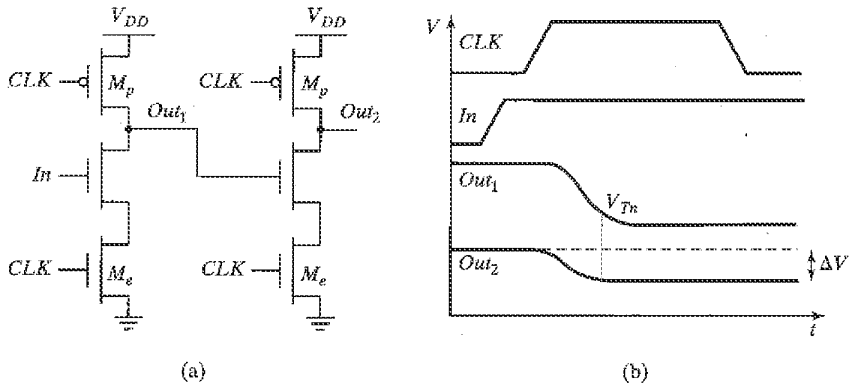


Figure 6-63 Cascade of dynamic *n*-type blocks.

The cascading problem arises because the outputs of each gate—and thus the inputs to the next stages—are precharged to 1. This may cause inadvertent discharge in the beginning of the evaluation cycle. Setting all the inputs to 0 during precharge addresses that concern. When doing so, all transistors in the pull-down network are turned off after precharge, and no inadvertent discharging of the storage capacitors can occur during evaluation. In other words, correct operation is guaranteed as long as **the inputs can only make a single 0 → 1 transition during the evaluation period.**[5] Transistors are turned on only when needed—and at most, once per cycle. A number of design styles complying with this rule have been conceived, but the two most important ones are discussed next.

Domino Logic

Concept A domino logic module [Krambeck82] consists of an *n*-type dynamic logic block followed by a static inverter (Figure 6-64). During precharge, the output of the *n*-type dynamic gate is charged up to V_{DD}, and the output of the inverter is set to 0. During evaluation, the dynamic gate conditionally discharges, and the output of the inverter makes a conditional transition from 0 → 1. If one assumes that all the inputs of a domino gate are outputs of other domino gates,[6] then it is ensured that all inputs are set to 0 at the end of the precharge phase, and that the only transitions during evaluation are 0 → 1 transitions. Hence, the formulated rule is obeyed. The introduction of the static inverter has the additional advantage that the fan-out of the gate is driven by a static inverter with a low-impedance output, which increases noise immunity. Also, the buffer reduces the capacitance of the dynamic output node by separating internal and load capacitances. Finally, the inverter can be used to drive a bleeder device to combat leakage and charge redistribution, as shown in the second stage of Figure 6-64.

[5]This ignores the impact of charge distribution and leakage effects, discussed earlier.

[6]It is required that all other inputs that do not fall under this classification (for instance, primary inputs) stay constant during evaluation.

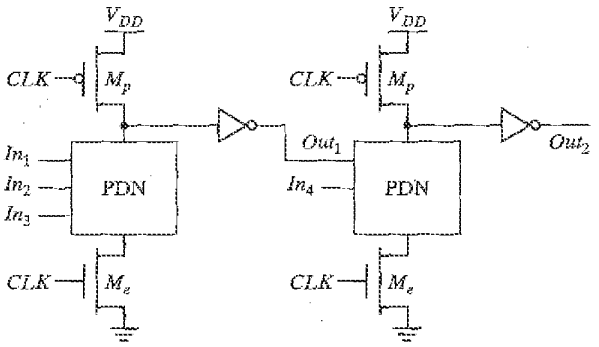


Figure 6-64 Domino CMOS logic.

Consider now the operation of a chain of domino gates. During precharge, all inputs are set to 0. During evaluation, the output of the first domino block either stays at 0 or makes a $0 \rightarrow 1$ transition, affecting the second gate. This effect might ripple through the whole chain, one after the other, similar to a line of falling dominoes—hence the name. Domino CMOS has the following properties:

- Since each dynamic gate has a static inverter, only noninverting logic can be implemented. Although there are ways to deal with this, as discussed in a subsequent section, this is a major limiting factor, and pure domino design has thus become rare.
- Very high speeds can be achieved: only a rising edge delay exists, while t_{pHL} equals zero. The inverter can be sized to match the *fan-out*, which is already much smaller than in the complimentary static CMOS case, as only a single gate capacitance has to be accounted for per fan-out gate.

Since the inputs to a domino gate are low during precharge, it is tempting to eliminate the evaluation transistor because this reduces clock load and increases pull-down drive. However, eliminating the evaluation device extends the precharge cycle—the precharge now has to ripple through the logic network as well. Consider the logic network shown in Figure 6-65, where the evaluation devices have been eliminated. If the primary input In_1 is 1 during evaluation, the output of each dynamic gate evaluates to 0, and the output of each static inverter is 1. On the falling edge of the clock, the precharge operation is started. Assume further that In_1 makes a high-to-low transition. The input to the second gate is initially high, and it takes two gate delays before In_2 is driven low. During that time, the second gate cannot precharge its output, as the pull-down network is fighting the precharge device. Similarly, the third gate has to wait until the second gate precharges before it can start precharging, etc. Therefore, the time taken to precharge the logic circuit is equal to its critical path. Another important negative is the extra power dissipation when both pull-up and pull-down devices are on. Therefore, it is good practice to always utilize evaluation devices.

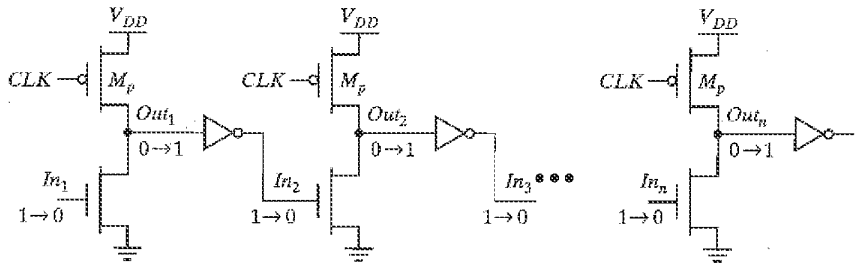


Figure 6-65 Effect of ripple precharge when the evaluation transistor is removed. The circuit also exhibits static power dissipation.

Dealing with the Noninverting Property of Domino Logic A major limitation in domino logic is that only noninverting logic can be implemented. This requirement has limited the widespread use of pure domino logic. There are several ways to deal with it, though. Figure 6-66 shows one approach to the problem—reorganizing the logic using simple boolean transforms such as De Morgan's Law. Unfortunately, this sort of optimization is not always possible, and more general schemes may have to be used.

A general (but expensive) approach to solving the problem is the use of differential logic. *Dual-rail domino* is similar in concept to the DCVSL structure discussed earlier, but it uses a precharged load instead of a static cross-coupled PMOS load. Figure 6-67 shows the circuit schematic of an AND/NAND differential logic gate. Note that all inputs come from other differential domino gates. They are low during the precharge phase, while making a conditional $0 \rightarrow 1$ transition during evaluation. Using differential domino, it is possible to implement any arbitrary function. This comes at the expense of an increased power dissipation, since a transition is guaranteed every single clock cycle regardless of the input values—either O or $\overline{O}$ must make a $0 \rightarrow 1$ transition. The function of transistors M_{f1} and M_{f2} is to keep the circuit static when the clock is high for extended periods of time (*bleeder*). Notice that this circuit is not ratioed, even in the presence of the PMOS pull-up devices! Due to its high performance, this differential approach is very popular, and is used in several commercial microprocessors.

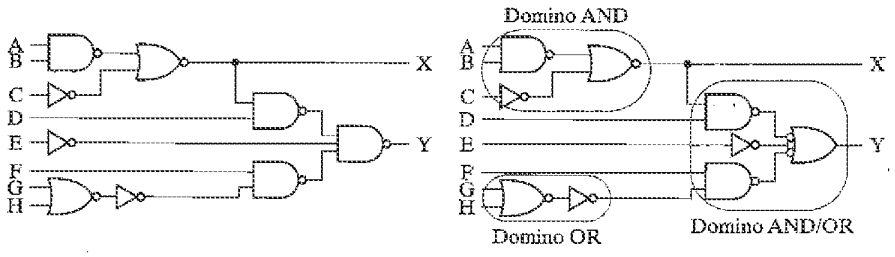


Figure 6-66 Restructuring logic to enable implementation by using noninverting domino logic.

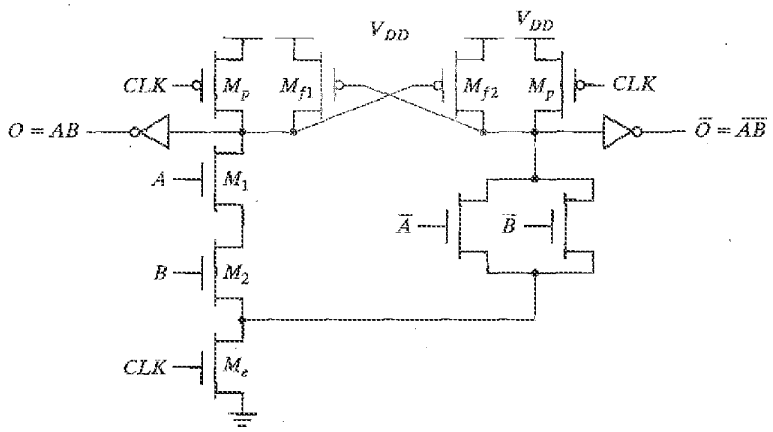


Figure 6-67 Simple dual rail (differential) domino logic gate.

Optimization of Domino Logic Gates Several optimizations can be performed on domino logic gates. The most obvious performance optimization involves the sizing of the transistors in the static inverter. With the inclusion of the evaluation devices in domino circuits, all gates precharge in parallel, and the precharge operation takes only two gate delays—charging the output of the dynamic gate to V_{DD}, and driving the inverter output low. The critical path during evaluation goes through the pull-down path of the dynamic gate and through the PMOS pull-up transistor of the static inverter. Therefore, to speed up the circuit during evaluation, the beta ratio of the static inverter should be made high so that its switching threshold is close to V_{DD}. This can be accomplished by using a small (minimum-sized) NMOS and a large PMOS device. The minimum-sized NMOS only affects the precharge time, which is generally limited due to the parallel precharging of all gates. The only disadvantage of using a large beta ratio is a reduction in noise margin. Hence, a designer should consider reduced noise margin and performance impact simultaneously during the device sizing.

Numerous variations of domino logic have been proposed [Bernstein98]. One optimization that reduces area is *multiple-output domino logic*. The basic concept is illustrated in Figure 6-68. It exploits the fact that certain outputs are subsets of other outputs to generate a number of logical functions in a single gate. In this example, $O3 = C + D$ is used in all three outputs, and thus it is implemented at the bottom of the pull-down network. Since $O2$ equals $B \cdot O3$, it can reuse the logic for $O3$. Notice that the internal nodes have to be precharged to V_{DD}, to produce the correct results. Given that the internal nodes precharge to V_{DD}, the number of devices driving precharge devices is not reduced. However, the number of evaluation transistors is drastically reduced because they are amortized over multiple outputs. Additionally, this approach results in a reduction of the fan-out factor, again due to the reuse of transistors over multiple functions.

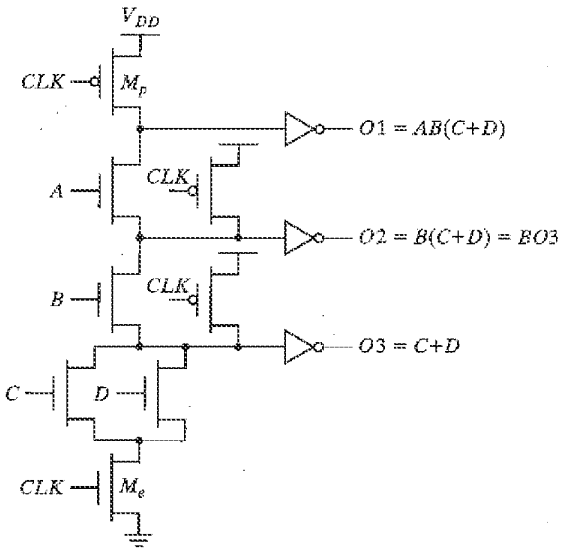


Figure 6-68 Multiple-output domino.

Compound domino (Figure 6-69) represents another optimization of the generic domino gate, once again minimizing the number of transistors. Instead of each dynamic gate driving a static inverter, it is possible to combine the outputs of multiple dynamic gates with the aid of a complex static CMOS gate, as shown in Figure 6-69. The outputs of three dynamic structures (implementing $O1 = \overline{A\,B\,C}$, $O2 = \overline{D\,E\,F}$ and $O3 = \overline{G\,H}$) are combined using a single complex CMOS static gate that implements $O = \overline{(O1 + O2)\,O3}$. The total logic function realized this way is $O = A\,B\,C\,D\,E\,F + GH$.

Compound domino is a useful tool for constructing complex dynamic logic gates. Large dynamic stacks are replaced by parallel structures with small fan-in and complex CMOS gates. For example, a large *fan-in* domino AND can be implemented as a set of parallel dynamic NAND structures with lower *fan-in*, combined with a static NOR gate. One important consideration in Compound domino is the problem associated with backgate coupling. Care must be taken to ensure that the dynamic nodes are not affected by the coupling between the output of the static gates and the output of dynamic nodes.

np-CMOS

An alternative approach to cascading dynamic logic is provided by *np*-CMOS, which uses two flavors (*n*-tree and *p*-tree) of dynamic logic, and avoids the extra static inverter in the critical path that comes with domino logic. In a *p*-tree logic gate, PMOS devices are used to build a pull-up logic network, including a PMOS evaluation transistor ([Gonçalvez83, Friedman84, Lee86]).

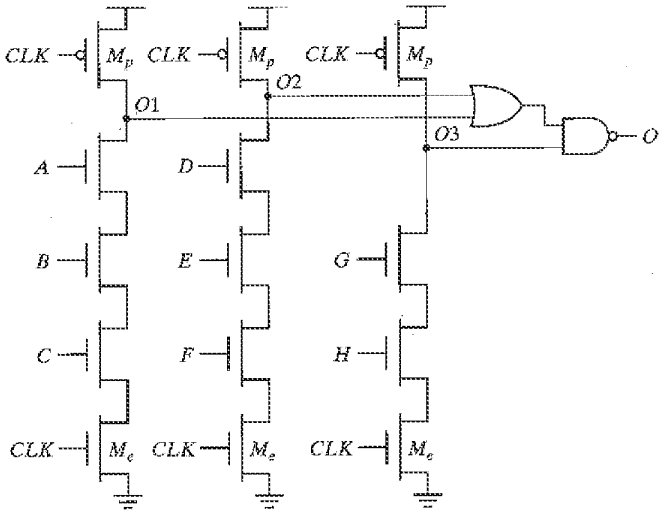


Figure 6-69 Compound domino logic uses complex static gates at the output of the dynamic gates.

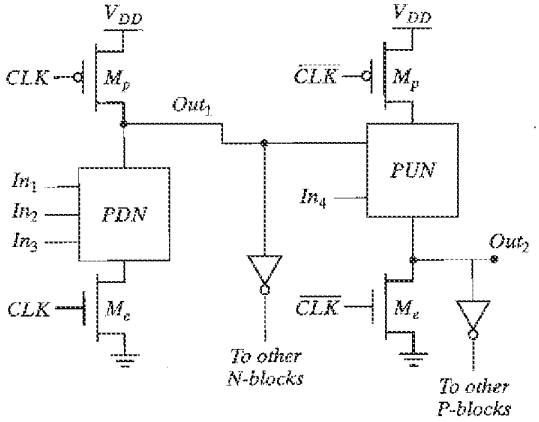


Figure 6-70 The *np*-CMOS logic circuit style.

(see Figure 6-70). The NMOS predischarge transistor drives the output low during precharge The output conditionally makes a $0 \rightarrow 1$ transition during evaluation depending on its inputs.

np-CMOS logic exploits the duality between *n*-tree and *p*-tree logic gates to eliminate the cascading problem. If the *n*-tree gates are controlled by *CLK*, and *p*-tree gates are controlled using $\overline{CLK}$, *n*-tree gates can directly drive *p*-tree gates, and vice versa. Similar to domino, *n*-tree outputs must go through an inverter when connecting to another *n*-tree gate. During the

precharge phase ($CLK = 0$), the output of the n-tree gate, Out_1, is charged to V_{DD}, while the output of the p-tree gate, Out_2, is predischarged to 0 V. Since the n-tree gate connects PMOS pull-up devices, the PUN of the p-tree is turned off at that time. During evaluation, the output of the n-tree gate can only make a $1 \rightarrow 0$ transition, conditionally turning on some transistors in the p-tree. This ensures that no accidental discharge of Out_2 can occur. Similarly, n-tree blocks can follow p-tree gates without any problems, because the inputs to the n-gate are precharged to 0. A disadvantage of the np-CMOS logic style is that the p-tree blocks are slower than the n-tree modules, due to the lower current drive of the PMOS transistors in the logic network. Equalizing the propagation delays requires extra area. Also, the lack of buffers requires that dynamic nodes are routed between gates.

6.4 Perspectives

6.4.1 How to Choose a Logic Style?

In the preceding sections, we have discussed several gate-implementation approaches using the CMOS technology. Each of the circuit styles has its advantages and disadvantages. Which one to select depends upon the primary requirement: ease of design, robustness, area, speed, or power dissipation. No single style optimizes all these measures at the same time. Even more, the approach of choice may vary from logic function to logic function.

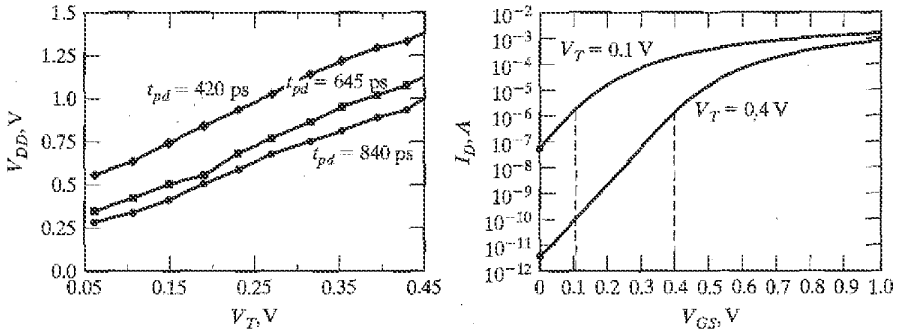
The static approach has the advantage of being robust in the presence of noise. This makes the design process rather trouble free and amenable to a high degree of automation. It is clearly the best general-purpose logic design style. This ease of design does come at a cost: For complex gates with a large fan-in, complementary CMOS becomes expensive in terms of area and performance. Alternative static logic styles have therefore been devised. Pseudo-NMOS is simple and fast at the expense of a reduced noise margin and static power dissipation. Pass-transistor logic is attractive for the implementation of a number of specific circuits, such as multiplexers and XOR-dominated logic like adders.

Dynamic logic, on the other hand, makes it possible to implement fast and small complex gates. This comes at a price, however. Parasitic effects such as charge sharing make the design process a precarious job. Charge leakage forces a periodic refresh, which puts a lower bound on the operating frequency of the circuit.

The current trend is towards an increased use of complementary static CMOS. This tendency is inspired by the increased use of design-automation tools at the logic design level. These tools emphasize optimization at the logic level, rather than at the circuit level, and they put a premium on robustness. Another argument is that static CMOS is more amenable to voltage scaling than some of the other approaches discussed in this chapter.

6.4.2 Designing Logic for Reduced Supply Voltages

In Chapter 3, we projected that the supply voltage for CMOS processes will continue to drop over the coming decade, and may go as low as 0.6 V by 2010. To maintain performance under



(a) V_{DD}/V_T *for fixed performance* (b) *Leakage as a function of* V_T

Figure 6-71 Voltage Scaling (V_{DD}/V_T on delay and leakage).

those conditions, it is essential that the device thresholds scale as well. Figure 6-71a shows a plot of the (V_T, V_{DD}) ratio required to maintain a given performance level (assuming that other device characteristics remain identical).

This trade-off is not without penalty. Reducing the threshold voltage increases the subthreshold leakage current exponentially, as we derived in Eq. (3.39) (repeated here for the sake of clarity):

$$I_{leakage} = I_S 10^{\frac{V_{GS}-V_{th}}{S}} \left(1 - 10^{\frac{-nV_{DS}}{S}}\right) \tag{6.46}$$

In Eq. (6.46), S is the *slope factor* of the device. The subthreshold leakage of an inverter is the current of the NMOS for $V_{in} = 0$ V and $V_{out} = V_{DD}$ (or the PMOS current for $V_{in} = V_{DD}$ and $V_{out} = 0$). The exponential increase in inverter leakage for decreasing thresholds is illustrated in Figure 6-71b.

These leakage currents are a concern particularly for designs that feature intermittent computational activity separated by long periods of inactivity. For example, the processor in a cellular phone remains in idle mode for a majority of the time. While the processor is in idle mode, ideally, the system should consume zero or near-zero power. This is only possible if leakage is low—that is, the devices have a high threshold voltage. This is in contrast to the scaling scenario that we just depicted, where high performance under low supply voltage means reduced thresholds. To satisfy the contradicting requirements of high performance during active periods and low leakage during standby, several process modifications or leakage-control techniques have been introduced in CMOS processes. Most processes with feature sizes at or below 0.18 μm CMOS support devices with different thresholds—typically a device with low threshold for high-performance circuits, and a transistor with high threshold for leakage control. Another approach gaining popularity is the

dynamic control of the threshold voltage of a device by exploiting the body effect of the transistor. Use of this approach to control individual devices requires a dual-well process (see Figure 2-2).

Clever circuit design can also help reduce the leakage current, which is a function of the circuit topology and the value of the inputs applied to the gate. Since V_T depends on body bias (V_{BS}), the subthreshold leakage of an MOS transistor depends not only on the gate drive (V_{GS}), but also on the body bias. In an inverter with $In = 0$, the subthreshold leakage of the inverter is set by the NMOS transistor with its $V_{GS} = V_{BS} = 0$ V. In more complex CMOS gates, such as the two-input NAND gate of Figure 6-72, the leakage current depends on the input vector. The subthreshold leakage current of this gate is the least when $A = B = 0$. Under these conditions, the intermediate node X settles to

$$V_X = V_{th} \ln(1 + n) \tag{6.47}$$

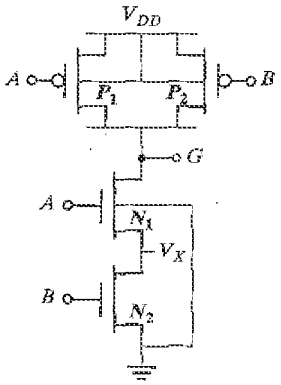
The leakage current of the gate is then determined by the topmost NMOS transistor with $V_{GS} = V_{BS} = -V_X$. Clearly, the subthreshold leakage under this condition is smaller than that of the inverter. This reduction due to stacked transistors is called the *stack effect*. The Table in Figure 6-72 analyzes the leakage components for the two-input NAND gate under different input conditions.

The reality is even better. In short-channel MOS transistors, the subthreshold leakage current depends not only on the gate drive (V_{GS}) and the body bias (V_{BS}), but also on the drain voltage (V_{DS}). The threshold voltage of a short-channel MOS transistor decreases with increasing V_{DS} due to *drain-induced barrier lowering* (DIBL). Typical values for DIBL can range from a 20- to a 150-mV change in V_T per voltage change in V_{DS}. Because of this, the impact of the stack effect is even more significant for short-channel transistors. The intermediate voltage reduces the drain–source voltage of the topmost device, increases its threshold, and thus lowers its leakage.

Example 6.19 Stack Effect in Two-Input NAND Gate

Consider again the two-input NAND gate of Figure 6-72a, when both N_1 and N_2 are *off* ($A = B = 0$). From the simulated load lines shown in Figure 6-72c, we see that V_X settles to approximately 100 mV in steady state. The steady-state subthreshold leakage in the gate is therefore due to $V_{GS} = V_{BS} = -100$ mV and $V_{DS} = V_{DD} - 100$ mV, which is 20 times smaller than the leakage of a stand-alone NMOS transistor with $V_{GS} = V_{BS} = 0$ mV and $V_{DS} = V_{DD}$ [Ye98].

In sum, the subthreshold leakage in complex stacked circuits can be significantly lower than in individual devices. Observe that the maximum leakage reduction occurs when all the transistors in the stack are *off*, and the intermediate node voltage reaches its steady-state value. Exploiting this effect requires a careful selection of the input signals to every gate during standby or sleep mode.



A	B	V_X	I_{SUB}
0	0	$V_{th} \ln(1+n)$	$I^N_{SUB}(V_{GS} = V_{BS} = -V_X)$
0	1	0	$I^N_{SUB}(V_{GS} = V_{BS} = 0)$
1	0	$V_{dd} - V_T$	$I^N_{SUB}(V_{GS} = V_{BS} = 0)$
1	1	0	$2\,I^P_{SUB}(V_{SG} = V_{SB} = 0)$

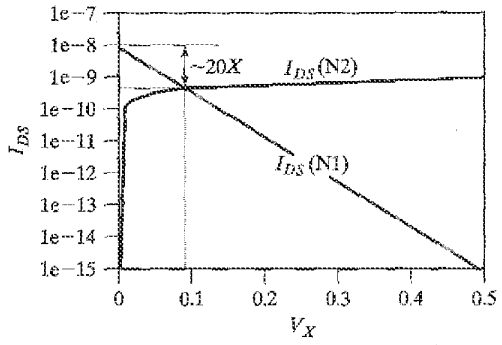


Figure 6-72 Subthreshold leakage reduction in a two-input NAND gate (a) due to stack effect for different input conditions (b). Figure (c) plots the simulated load lines of the gate for $A = B = 0$.

Problem 6.9 Computing V_X

Equation (6.47) calculates the intermediate node voltage for a two-input NAND with less than 10% error, for $A = B = 0$. Derive Eq. (6.47) assuming (1) V_T and I_S of N_1 and N_2 are approximately equal, (2) NMOS transistors are identically sized, and (3) $n < 1.5$.

6.5 Summary

In this chapter, we have extensively analyzed the behavior and performance of combinational CMOS digital circuits with regard to area, speed, and power. We summarize the major points as follows:

- *Static complementary* CMOS combines dual pull-down and pull-up networks, only one of which is enabled at any time.

- The performance of a CMOS gate is a strong function of the *fan-in*. Techniques to deal with fan-in include transistor sizing, input reordering, and partitioning. The speed is also a linear function of the fan-out. Extra buffering is needed for large fan-outs.
- The *ratioed logic* style consists of an active pull-down (-up) network connected to a load device. This results in a substantial reduction in gate complexity at the expense of static power consumption and an asymmetrical response. Careful transistor sizing is necessary to maintain sufficient noise margins. The most popular approaches in this class are the pseudo-NMOS techniques and differential DCVSL, which require complementary signals.
- *Pass-transistor logic* implements a logic gate as a simple switch network. This results in very simple implementations for some logic functions. Long cascades of switches are to be avoided due to a quadratic increase in delay with respect to the number of elements in the chain. NMOS-only pass-transistor logic produces even simpler structures, but might suffer from static power consumption and reduced noise margins. This problem can be addressed by adding a level-restoring transistor.
- The operation of *dynamic logic* is based on the storage of charge on a capacitive node and the conditional discharging of that node as a function of the inputs. This calls for a two-phase scheme, consisting of a precharge followed by an evaluation step. Dynamic logic trades off noise margin for performance. It is sensitive to parasitic effects such as leakage, charge redistribution, and clock feedthrough. Cascading dynamic gates can cause problems and thus should be addressed carefully.
- The *power consumption* of a logic network is strongly related to the switching activity of the network. This activity is a function of the input statistics, the network topology, and the logic style. Sources of power consumption such as glitches and short-circuit currents can be minimized by careful circuit design and transistor sizing.
- Threshold voltage scaling is required for *low-voltage operation*. Leakage control is critical for low-voltage operation.

6.6 To Probe Further

The topic of (C)MOS logic styles is treated extensively in the literature. Numerous texts have been devoted to the issue. Some of the most comprehensive treatments can be found in [Weste93] and [Chandrakasan01]. Regarding the intricacies of high-performance design, [Shoji96] and [Bernstein98] offer the most in-depth discussion of the optimization and analysis of digital MOS circuits. The topic of power minimization is relatively new, but comprehensive reference works are available in [Chandrakasan95], [Rabaey95], and [Pedram02].

Innovations in the MOS logic area are typically published in the proceedings of the ISSCC Conference and the VLSI circuits symposium, as well as the *IEEE Journal of Solid State Circuits* (especially the November issue).

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Exercises

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DESIGN METHODOLOGY INSERT

C

How to Simulate Complex Logic Circuits

Timing- and Switch-Level Simulation

Logic and Functional Simulation

Behavioral Simulation

Register-Transfer Languages

While circuit simulation in the SPICE style proves to be an extremely valuable element of the designers tool box, it has one major deficiency. By taking into account all the peculiarities and second-order effects of the semiconductor devices, it tends to be time consuming. It rapidly becomes unwieldy when designing complex circuits, unless one is willing to spend days of computer time. Even though computers are always getting faster and simulators are getting better, circuits are getting complex even faster. The designer can address the complexity issue by giving up modeling accuracy and resorting to higher representation levels. A discussion of the different abstraction levels available to the designer and their impact on simulation accuracy is the topic of this insert.

The best way of differentiating among the myriad of simulation approaches and abstraction levels is to identify how the data and time variables are represented—as analog, continuous variables, as discrete signals, or as abstract data models.

C.1 Representing Digital Data as a Continuous Entity

Circuit Simulation and Derivatives

In Design Methodology Insert B, we established that a circuit simulator is "digitallyagnostic," meaning that it is, in essence, an analog simulator. Voltage, current, and time are treated as analog variables. This accurate modeling, combined with the nonlinearity of most of the devices leads to a high overhead in simulation time.

Substantial effort has been invested to decrease the computation time at the expense of generality. Consider an MOS digital circuit. Due to the excellent isolation property of the MOS gate, it is often possible to partition the circuit into a number of sections that have limited interaction. A possible approach is to solve each of these partitions individually over a given period, assuming that the inputs from other sections are known or constant. The resulting waveforms can then be iteratively refined. This *relaxation-based* approach has the advantage of being computationally more effective than the traditional technique by avoiding expensive matrix inversions, but it is restricted to MOS circuits [White87]. When the circuit contains feedback paths, the partitions can become large, and simulation performance degrades.

Another approach is to reduce the complexity of the transistor models used. For example, linearization of the model leads to a dramatic reduction in the computational complexity. Yet another approach is to employ a simplified table-lookup model. While this approach, by necessity, leads to a decreased accuracy of the waveforms, it still allows for a good estimation of timing parameters such as propagation delay and rise and fall times. This explains why these tools often are called *timing simulators*. The big advantage is in the execution speed, which can be one or two orders of magnitude higher than that of SPICE-like tools. Another advantage is that, in contrast to the tools that are discussed next, timing simulators still can incorporate second-order effects such as leakage, threshold drops, and signal glitches. Examples of an offering in this class is the NanoSim (formerly TimeMill/PowerMill) tool set from Synopsys [TimeMill]. As a point of reference, simulators in this class typically give up 5 to 10% in accuracy on timing parameters, with respect to full-blown circuit simulators.

C.2 Representing Data as a Discrete Entity

In digital circuits, we generally are not interested in the actual value of the voltage variable, but only in the digital value it represents. Therefore, it is possible to envision a simulator in which data signals are either in the 0 or 1 range. Signals that do no comply with either condition are denoted as X, or undefined.

This tertiary representation $\{0, 1, X\}$ is used extensively in simulators at both the device and gate level. By augmenting this set of allowable data values, we can obtain more detailed information, while retaining the capability of handling complex designs. Possible extensions are the Z-value for a tristate node in the high-impedance state, and R- and F-values for the rising and falling transients. Some commercially offered simulators provide as many as a dozen possible signal states.

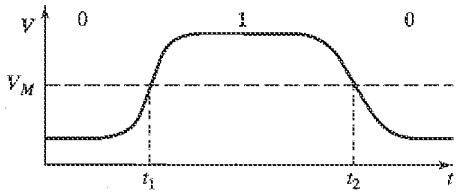


Figure C-1 Discretizing the time variable.

While substantial performance improvement is obtained by making the data representation space discrete, similar benefits can be obtained by making time a discrete variable as well. Consider the voltage waveform of Figure C-1, which represents the signal at the input of an inverter with a switching threshold V_M. It is reasonable to assume that the inverter output changes its value one propagation delay after its input crossed V_M. When one is not strictly interested in the exact shape of the signal waveforms, it is sufficient to evaluate the circuit only at the interesting time points, t_1 and t_2.

Similarly, the interesting points of the output waveform are situated at $t_1 + t_{pHL}$ and $t_2 + t_{pLH}$. A simulator that only evaluates a gate at the time an event happens at one of its inputs is called an *event-driven* simulator. The evaluation order is determined by putting projected events on a time queue and processing them in a time-ordered fashion. Suppose that the waveform of Figure C-1 acts as the input waveform to a gate. An event is scheduled to occur at time t_1. Upon processing that event, a new event is scheduled for the fan-out nodes at $t_1 + t_{pHL}$ and is put on the time queue. This event-driven approach is evidently more efficient than the time-step-driven approach of the circuit simulators. To take the impact of fan-out into account, the propagation delay of a circuit can be expressed in terms of an intrinsic delay (t_{in}) and a load-dependent factor (t_l), and it can differ over edge transitions:

$$t_{pLH} = t_{inLH} + t_{lLH} \times C_L \tag{C.1}$$

The load C_L can be entered in absolute terms (in pF) or as a function of the number of fan-out gates. Observe how closely this equation resembles the *logical-effort* model we introduced in the preceding chapter.

While offering a substantial performance benefit, the preceding approach still has the disadvantage that events can happen any time. Another simplification could be to make the time even more discrete and allow events to happen only at integer multiples of a *unit time* variable. An example of such an approach is the *unit-delay* model, where each circuit has a single delay of one unit. Finally, the simplest model is the *zero-delay model*, in which gates are assumed to be free of delay. Under this paradigm, time proceeds from one clock event to the next, and all events are assumed to occur instantaneously upon arrival of a clocking event. These concepts can be applied on a number of abstraction levels, resulting in the simulation approaches discussed next.

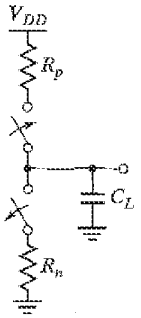


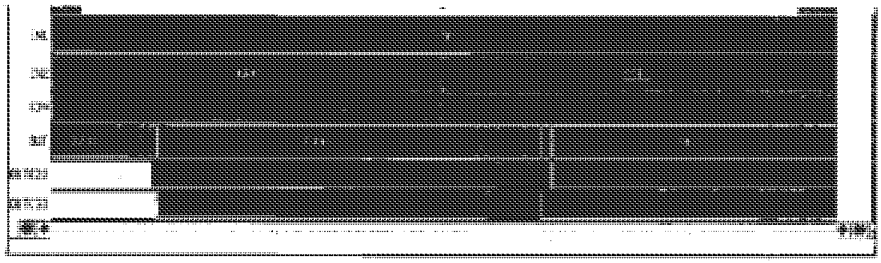
Figure C-2 Switch-level model of CMOS inverter.

Switch-Level Simulation

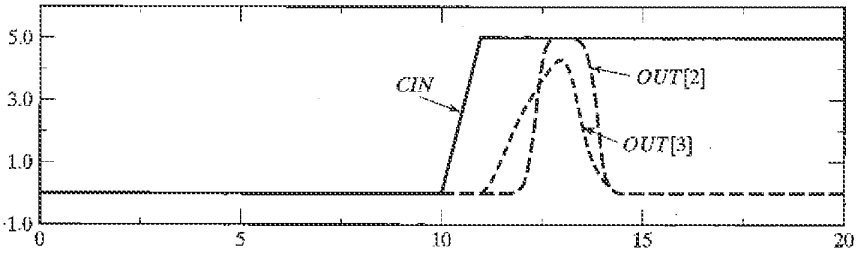
The nonlinear nature of semiconductor devices is one of the major impediments to higher simulation speeds. The switch-level model [Bryant81] overcomes this hurdle by approximating the transistor behavior with a linear resistance whose value is a function of the operating conditions. In the off-mode, the resistance is set to infinity, while in the on-mode, it is set to the average "on" resistance of the device (Figure C-2). The resulting network is a time-variant, linear network of resistors and capacitors that can be more efficiently analyzed. Evaluation of the resistor network determines the steady-state values of the signals and typically employs a {0, 1, *X*} model. For instance, if the total resistance between a node and GND is substantially smaller than the resistance to V_{DD}, the node is set to the 0-state. The timing of the events can be resolved by analyzing the *RC* network. Simpler timing models such as the unit-delay model are also employed.

Example C.1 Switch versus Circuit-Level Simulation

A four-bit adder is simulated using the switch-level simulator IRSIM ([Salz89]). The simulation results are plotted in Figure C-3. Initially, all inputs (*IN*1 and *IN*2) and the carry-input *CIN* are set to 0. After 10 nsec, all inputs *IN*2 as well as *CIN* are set to 1. The display window plots the input signals, the output vector *OUT*[0–3], and the most significant output bits *OUT*[2] and *OUT*[3]. The output converges to the correct value 0000 after a transition period. Notice how the data assumes only 0 and 1 levels. The glitches in the output signals go rail to rail, although in reality they might represent only partial excursions. During transients, the signal is marked *X*, which means "undefined." To put this result in perspective, Figure C-3 plots the SPICE results for the same input vectors. Notice the partial glitches. Also, it shows that the IRSIM timing, which is based on an *RC* model, is relatively accurate and sufficient to get a first-order impression.



(a) IRSIM results.



(b) SPICE results.

Figure C-3 Comparison between circuit and switch-level simulations.

Gate-Level (or Logic) Simulation

Gate-level simulators use the same signal values as the switch-level tools, but the simulation primitives are gates instead of transistors. This approach enables the simulation of more complex circuits at the expense of detail and generality. For example, some common VLSI structures such as tristate busses and pass transistors are hard to deal with at this level. Since gate level is the preferred entry level for many designers, this simulation approach remained extremely popular until the introduction of logic synthesis tools, which moved the focus to the functional or behavioral abstraction layer. The interest in logic simulation was so great that special and expensive hardware accelerators were developed to expedite the simulation process (e.g., [Agrawal90]).

Functional Simulation

Functional simulation can be considered as a simple extension of logic simulation. The primitive elements of the input description can be of an arbitrary complexity. For instance, a simulation element can be a NAND gate, a multiplier, or an SRAM memory. The functionality of one of these complex units can be described using a modern programming language or a dedicated hardware description language. For instance, the THOR simulator uses the C programming language to determine the output values of a module as a function of its inputs [Thor88].

The *SystemC* language [SystemC] uses most of the syntax and semantics of C, but adds a number of constructs and data types to deal with the peculiarities of hardware design—such as the presence of concurrency. On the other hand, *VHDL (VHSIC Hardware Description Language)* [VHDL88] is a specially developed language for the description of hardware designs.

In the *structural mode*, VHDL describes a design as a connection of functional modules. Such a description often is called a *netlist*. For example, Figure C-4 shows a description of a 16-bit accumulator consisting of a register and adder.

The adder and register can in turn be described as a composition of components such as full-adder or register cells. An alternative approach is to use the *behavioral mode* of the language that describes the functionality of the module as a set of input/output relations regardless of the chosen implementation. As an example, Figure C-5 describes how the output of the adder is the two's-complement sum of its inputs.

```
entity accumulator is
    port ( -- definition of input and output terminals
        DI: in bit_vector(15 downto 0) -- a vector of 16 bit wide
        DO: inout bit_vector(15 downto 0);
        CLK: in bit
    );
end accumulator;

architecture structure of accumulator is
    component reg -- definition of register ports
        port (
            DI : in bit_vector(15 downto 0);
            DO : out bit_vector(15 downto 0);
            CLK : in bit
        );
    end component;
    component add -- definition of adder ports
        port (
            IN0 : in bit_vector(15 downto 0);
            IN1 : in bit_vector(15 downto 0);
            OUT0 : out bit_vector(15 downto 0)
        );
    end component;
-- definition of accumulator structure
signal X : bit_vector(15 downto 0);
begin
    add1 : add
        port map (DI, DO, X); -- defines port connectivity
    reg1 : reg
        port map (X, DO, CLK);
end structure;
```

Figure C-4 Functional description of an accumulator in VHDL.

```
entity add is
    port (
        IN0 : in bit_vector(15 downto 0);
        IN1 : in bit_vector(15 downto 0);
        OUT0 : out bit_vector(15 downto 0)
    );
end add;

architecture behavior of add is
begin
    process(IN0, IN1)
        variable C : bit_vector(16 downto 0);
        variable S : bit_vector(15 downto 0);
    begin
        loop1:
        for i in 0 to 15 loop
            S(i) := IN0(i) xor IN1(i) xor C(i);
            C(i+1):= IN0(i) and IN1(i) or C(i) and (IN0(i) or IN1(i));
        end loop loop1;
        OUT0 <= S;
    end process;
end behavior;
```

Figure C-5 Behavioral description of 16-bit adder.

The signal levels of the functional simulator are similar to the switch and logic levels. A variety of timing models can be used—for example, the designer can describe the delay between input and output signals as part of the behavioral description of a module. Most often the zero-delay model is employed, since it yields the highest simulation speed.

C.3 Using Higher-Level Data Models

When conceiving a digital system such as a compact disk player or an embedded microcontroller, the designer rarely thinks in terms of bits. Instead, she envisions data moving over busses as integer or floating-point words, and patterns transmitted over the instruction bus as members of an enumerated set of instruction words (such as {*ACC*, *RD*, *WR*, or *CLR*}). Modeling a discrete design at this level of abstraction has the distinct advantage of being more understandable, and it also results in a substantial benefit in simulation speed. Since a 64-bit bus is now handled as a single object, analyzing its value requires only one action instead of the 64 evaluations it formerly took to determine the current state of the bus at the logic level. The disadvantage of this approach is another sacrifice of timing accuracy. Since a bus is now considered to be a single entity, only one global delay can be annotated to it, while the delay of bus elements can vary from bit to bit at the logic level.

It also is common to distinguish between *functional* (or *structural*) and *behavioral* descriptions. In a functional-level specification, the description mirrors the intended hardware

structure. Behavioral-level specifications only mimic the input/output functionality of a design. Hardware delay loses its meaning, and simulations are normally performed on a per clock-cycle (or higher) basis. For instance, the behavioral models of a microprocessor that are used to verify the completeness and the correctness of the instruction set are performed on a per instruction basis.

The most popular languages at this level of abstraction are the VHDL and VERILOG hardware-description languages. VHDL allows for the introduction of user-defined data types such as 16-bit, two's-complement words or enumerated instruction sets. Many designers tend to use traditional programming approaches such as C or C++ for their first-order behavioral models. This approach has the advantage of offering more flexibility, but it requires the user to define all data types and to essentially write the complete simulation scenario.

Example C.2 Behavioral-Level VHDL Description

To contrast the functional and behavioral description modes and the use of higher level data models, consider again the example of the accumulator (see Figure C-6). In this case, we use a fully behavioral description that employs integer data types to describe the module operation.

Figure C-7 shows the results of a simulation performed at this level of abstraction. Even for this small example, the simulation performance in terms of CPU time is three times better than what is obtained with the structural description of Figure C-4.

```
entity accumulator is
    port (
        DI : in integer;
        DO : inout integer := 0;
        CLK : in bit
    );
end accumulator;

architecture behavior of accumulator is
begin
    process(CLK)
    variable X : integer := 0; -- intermediate variable
    begin
        if CLK = '1' then
            X <= DO + DI;
            DO <= X;
        end if;
    end process;
end behavior;
```

Figure C-6 Accumulator for Example C.2.

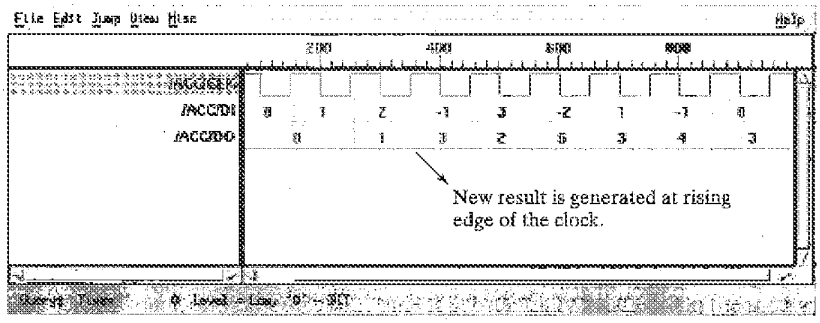


Figure C-7 Display of simulation results for accumulator example as obtained at the behavioral level. The WAVES display tool (and VHDL simulator) are part of the Synopsis VHDL tool suite (Courtesy of Synopsys.).

References

[Agrawal90] P. Agrawal and W. Dally, "A Hardware Logic Simulation System," *IEEE Trans. Computer-Aided Design*, CAD-9, no. 9, pp. 19–29, January 1990.

[Bryant81] R. Bryant, *A Switch-Level Simulation Model for Integrated Logic Circuits*, Ph. D. diss., MIT Laboratory for Computer Science, report MIT/LCS/TR-259, March 1981.

[Salz89] A. Salz and M. Horowitz, "IRSIM: An Incremental MOS Switch-Level Simulator," *Proceedings of the 26th Design Automation Conference*, pp. 173–178, 1989.

[SystemC] *Everything You Wanted to Know about SystemC, http://www.systemc.org/*

[Thor88] R. Alverson et al., "THOR User's Manual," Technical Report CSL-TR-88-348 and 349, Stanford University, January 1988.

[TimeMill] *http://www.synopsys.com/products/mixedsignal/mixedsignal.html*

[VHDL88] VHDL Standards Committee, IEEE Standard VHDL Language Reference Manual, IEEE standard 1076–1077, 1978.

[White87] J. White and A. Sangiovanni-Vincentelli, *Relaxation Techniques for the Simulation of VLSI Circuits*, Kluwer Academic, 1987.

DESIGN METHODOLOGY INSERT

D

Layout Techniques for Complex Gates

Weinberger and standard-cell layout techniques

Euler graph approach

In Chapter 6, we discussed in detail how to construct the schematics of complex gates and how to size the transistors. The last step in the design process is to derive a layout for the gate or cell; in other words, we must determine the exact shape of the various polygons composing the gate layout. The composition of a layout is strongly influenced by the *interconnect approach*. How does the cell fit in the overall chip layout, and how does it communicate with neighboring cells? Keeping these questions in mind from the start results in denser designs with less parasitic capacitance.

Weinberger and Standard-Cell Layout Techniques

We now examine two important layout approaches, although many others can be envisioned. In the *Weinberger approach* [Weinberger67], the data wires (inputs and outputs) are routed (in metal) parallel to the supply rails and perpendicular to the diffusion areas, as illustrated in Figure D-1. Transistors are formed at the cross points of the polysilicon signal wires (connected to the horizontal metal wires) and the diffusion zones. The "over-the-cell" wiring approach makes the Weinberger technique particularly suited for bit-sliced datapaths. While it is still used on an occasional base, the Weinberger technique has lost its appeal over the years in favor of the standard-cell style.

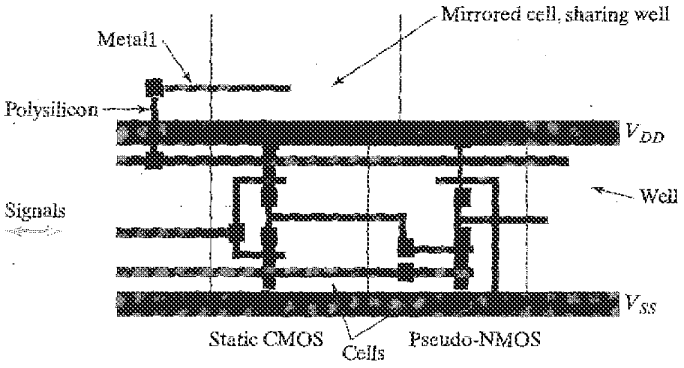


Figure D-1 The Weinberger approach for complex gate layout (using a single metal layer).

In the *standard-cell technique*, signals are routed in polysilicon perpendicular to the power distribution (Figure D-2). This approach tends to result in a dense layout for static CMOS gates, as the vertical polysilicon wire can serve as the input to both the NMOS and the PMOS transistors. An example of a cell implemented using the standard-cell approach is shown in Figure 6-12. Interconnections between cells generally are established in so-called routing channels, as demonstrated in Figure D-2. The standard-cell approach is very popular at present due to its high degree of automation. (For a detailed description of the design automation tools supporting the standard-cell approach, see Chapter 8.)

Layout Planning using the Euler Path Approach

The common use of this layout strategy makes it worth analyzing how a complex Boolean function can be mapped efficiently onto such a structure. For density reasons, it is desirable to realize the NMOS and PMOS transistors as an unbroken row of devices with abutting source–drain con-

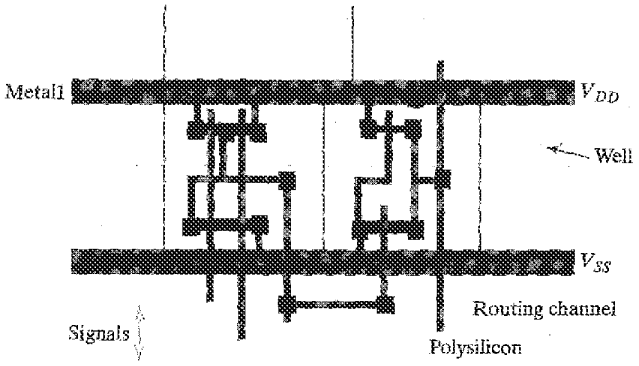


Figure D-2 The standard-cell approach for complex gate layout.

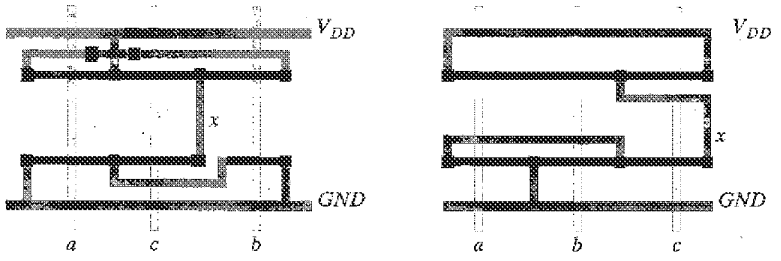
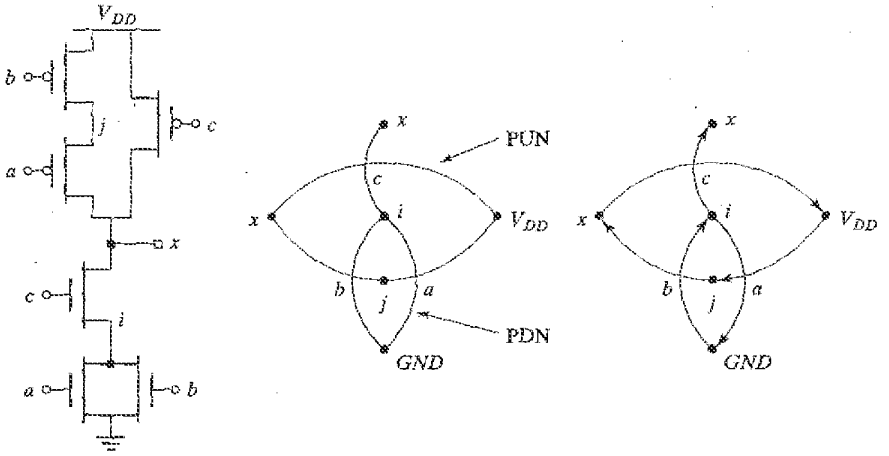


Figure D-3 Stick Diagram for $x = (a + b) \cdot c$.

nections, and with the gate connections of the corresponding NMOS and PMOS transistors aligned. This approach requires only a single strip of diffusion in both wells. To achieve this goal, a careful ordering of the input terminals is necessary. This is illustrated in Figure D-3, where the logical function $\bar{x} = (a + b) \cdot c$ is implemented. In the first version, the order $\{a\ c\ b\}$ is adopted. It can easily be seen that no solution will be found using only a single diffusion strip. A reordering of the terminals (for instance, using $\{a\ b\ c\}$), generates a feasible solution, as shown in Figure D-3b. Observe that the "layouts" in Figure D-3 do not represent actual mask geometries, but are rather symbolic diagrams of the gate topologies. Wires and transistors are represented as dimensionless objects, and positioning is relative, not absolute. Such conceptual representations are called *stick diagrams*, and often are used at the conception time of the gate, before determining the actual dimensions. We use stick diagrams whenever we want to discuss gate topologies or layout strategies.

Fortunately, a systematic approach has been developed to derive the permutation of the input terminals so that complex functions can be realized by uninterrupted diffusion strips that minimize the area [Uehara81]. The systematic nature of the technique also has the advantage that it is easily automated. It consists of the following two steps:

1. **Construction of *logic graph*.** The logic graph of a transistor network (or a switching function) is the graph of which the vertices are the nodes (signals) of the network, and the edges represent the transistors. Each edge is named for the signal controlling the corresponding transistor. Since the PUN and PDN networks of a static CMOS gate are dual, their corresponding graphs are dual as well—that is, a parallel connection is replaced by a series one and vice versa. This is demonstrated in Figure D-4, where the logic graphs for the PDN and PUN networks of the Boolean function $\bar{x} = (a + b) \cdot c$ are overlaid (notice that this approach can be used to derive dual networks).
2. **Identification of Euler paths.** An Euler path in a graph is defined as a path through all nodes in the graph such that each edge in the graph is only visited once. Identification of such a path is important, because an ordering of the inputs leading to an uninterrupted diffusion strip of NMOS (PMOS) transistors is possible only if there exists an Euler path in



(a) Schematic diagram (b) Logic graphs for PDN and PUN (c) Consistent Euler paths for PDN and PUN

Figure D-4 Schematic diagram, logic graph, and Euler paths for $x = (a + b) \cdot c$.

the logic graph of the PDN (PUN) network. The reasoning behind this finding is as follows:

To form an interrupted strip of diffusion, all transistors must be visited in sequence; that is, the drain of one device is the source of the next one. This is equivalent to traversing the logic graph along an Euler path. Be aware that Euler paths are not unique: many different solutions may exist.

The sequence of edges in the Euler path equals the ordering of the inputs in the gate layout. To obtain the same ordering in both the PUN and PDN networks, as is necessary if we want to use a single poly strip for every input signal, the Euler paths must be *consistent*—that is, they must have the same sequence.

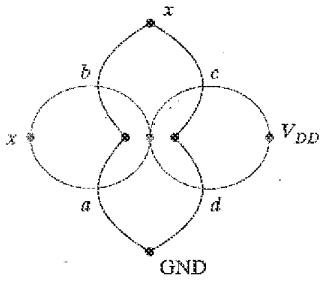
Consistent Euler paths for the example of Figure D-4a are shown in Figure D-4c. The layout associated with this solution is shown in Figure D-3b. An inspection of the logic diagram of the function shows that $\{a\ c\ b\}$ is an Euler path for the PUN, but not for the PDN. A single-diffusion-strip solution is, hence, nonexistent (Figure D-3a).

Example D.1 Derivation of Layout Topology of Complex Logic Gate

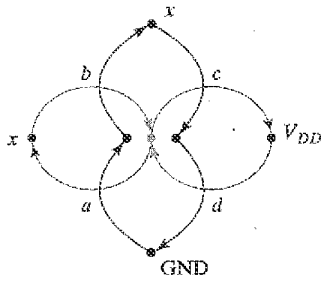
As an example, let us derive the layout topology of the following logical function:

$$x = \overline{ab + cd}$$

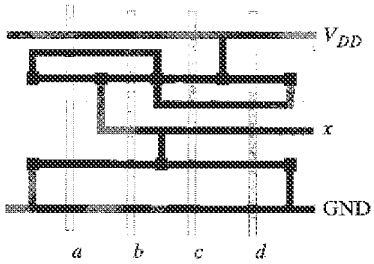
The logical function and one consistent Euler path are shown in Figure D-5a and Figure D-5b. The corresponding layout is shown in Figure D-5c.



(a) Logic graphs for $\overline{(ab + cd)}$



(b) Euler paths {a b c d}



(c) Stick diagram for ordering {a b c d}

Figure D-5 Deriving the layout topology for $x = (ab + cd)$.

The reader should be aware that the existence of consistent Euler paths depends on the way the Boolean expressions (and the corresponding logic graphs) are constructed. For example, no consistent Euler paths can be found for $\overline{x} = a + b \cdot c + d \cdot e$, but the function $\overline{x} = b \cdot c + a + d \cdot e$ has a simple solution (confirm that this is true by preserving the ordering of the function when constructing the logic graphs). A restructuring of the function is sometimes necessary before a set of consistent paths can be identified. This could lead to an exhaustive search over all possible path combinations. Fortunately, a simple algorithm to avoid this plight has been proposed [Uehara81]. A discussion of this is beyond our scope, however, and we refer the interested reader to that text.

Finally, it is worth mentioning that the layout strategies presented are not the only possibilities. For example, sometimes it might be more effective to provide multiple diffusion strips stacked vertically. In this case, a single polysilicon input line can serve as the input for multiple transistors. This might be beneficial for certain gate structures, such as the NXOR gate, and therefore, case-by-case analysis is recommended.

To Probe Further

A good overview of cell-generation techniques can be found in [Rubin87, pp. 116–128]. Some of the landmark papers in this area include the following:

[Clein00] D. Clein, *CMOS IC Layout*, Newnes, 2000.

[Rubin87] S. Rubin, *Computer Aids for VLSI Design*, Addison-Wesley, 1987.

[Uehara81] T. Uehara and W. Van Cleemput, "Optimal Layout of CMOS Functional Arrays," *IEEE Trans. on Computers*, vol. C-30, no. 5, pp. 305–311, May 1981.

[Weinberger67] A. Weinberger, "Large Scale Integration of MOS Complex Logic: A Layout Method," *IEEE Journal of Solid State Circuits*, vol. 2, no. 4, pp. 182–190, 1967.

SECOND EDITION

DIGITAL INTEGRATED CIRCUITS

A DESIGN PERSPECTIVE

JAN M. RABAEY • ANANTHA CHANDRAKASAN
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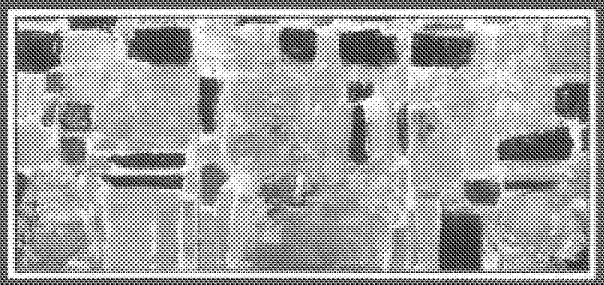
Since the publication of the first edition of this book in 1996, CMOS manufacturing technology has continued its relentless pace, scaling to ever smaller dimensions. Minimum feature sizes are now reaching the 100 nm realm. Circuits are becoming more complex, challenging the productivity of the designer, while the plunge into the deep submicron space causes designers to behave differently and brings to the forefront a number of new issues that impact the reliability, cost, performance, power dissipation, and robustness of the digital IC. This updated text reflects the ongoing revolution in the world of digital integrated circuit design caused by this move into the deep submicron realm. The author has increased importance of deep submicron interconnect effects, microarchitecture, circuit integrity, high performance and low power design, timing, and clock distribution. In contrast to the first edition, the present text focuses entirely on CMOS ICs.

http://bwrc.eecs.berkeley.edu/Publications/—A Dynamic Companion

From more than the first edition, this book goes to companion website to evolve and grow over time. It contains complete Microsoft PowerPoint presentations covering all the material, updates, corrections, design projects and extensive instructor material. Most importantly, all problems will are now available on the website (and have been removed from the text).

Outstanding Features of the Text

- It focuses entirely on deep submicron CMOS devices, the workhorses of today's digital integrated circuits. A simple transistor model for manual analysis, called the unified MOS model, has been developed and is used throughout.
- Design Examples across the chapters of Digital ICs from a real-world perspective. Design challenges and guidelines are highlighted as a function of CMOS technology is used for all the examples and problems.
- Design Methodology issues are interspersed throughout the text, highlighting the importance of methodology and tools in today's design process.
- A Perspective section at the end of each chapter gives an insight into future architectures.



Above the Cover: Detail of "Web Bridge" by Jean Mitchell Arrowsmith (1929-2002). Oil on canvas, 117 x 245 in. (284.5 x 622.3 cm). Carnegie Museum of Art, Pittsburgh, PA.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 90/019,255	Filing Date 09/20/2023	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	06/18/2024	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/RHONDA BELL/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
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This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Owner: Entropic Communications, Inc.
Inventors: Madhukar Reddy et al.
App. No.: 90/019,255
Filed: September 20, 2023
Conf. No.: 5785
Examiner: LIE, ANGELA M
Art Unit: 3992
Title: WIDEBAND TUNER ARCHITECTURE
Docket No.: 189005.TR003

CERTIFICATE OF SERVICE

Mail Stop *Ex Parte Reexam*
Central Reexamination Unit
Commissioner for Patents
P O Box 1450
Alexandria, VA 22313-1450

Dear Commissioner,

I hereby certify that I served a copy of the Response to the Office Action of March 18, 2024 in the *ex parte* reexamination requestor in accordance with MPEP § 2266, 37 C.F.R. § 1.550 and 35 C.F.R. 1.248 via first class mail on July 16, 2024. The name and address of the party served is:

Raghav Bajaj
Haynes and Boone, LLP
2323 Victory Avenue, Suite 700
Dallas, Texas 75219

Respectfully submitted,

Date: July 16, 2024 / Hao Tan/
Hao Tan, Reg. No. 73,711

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
90/019,255	**07/16/2024 04:14:02 PM Z ET**	**189005.TR003**

Title of Invention

WIDEBAND TUNER ARCHITECTURE

Application Information

APPLICATION TYPE	Utility / ex parte reexam	PATENT #	9210362
CONFIRMATION #	5785	FILED BY	ZHANGYUAN JI
PATENT CENTER #	66391109	FILING DATE	09/20/2023
CUSTOMER #	153979	FIRST NAMED INVENTOR	- 9210362
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Certificate of Service.pdf	1	Reexam Certificate of Service	121 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
Certificate of Service.pdf	C0F1B4EFDED49CF511A8A6352393A3126F2AA69FA6A16911E E9D2BE7E41762DF6989C133CBC74C9D45BDF63BBB48FA028 AAF24130EB3A2456EB24206CE361485

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/019,255	09/20/2023	9210362	189005.TR003	5785

153979 7590 08/07/2024

Arch & Lake LLP
203 North LaSalle Street, Suite 2100
Chicago, IL 60601

EXAMINER	
LIE, ANGELA M	

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
08/07/2024	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

Haynes and Boone, LLP
2801 N. Harwood St.
Suite 2300
Dallas TX 75201

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/019,255* .

PATENT UNDER REEXAMINATION *9210362* .

ART UNIT *3992* .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Status

Claims 1 and 11 of the US Patent No. 9,210,362 to Reddy et al (the '362 patent, hereinafter) have been ordered for the reexamination.

The References

(1) "McNeely" WO 2006/119490 to David Lowell McNeely, filed May 4, 2006, published November 9, 2006,

(2) "Pugel" WO 2007/145637 to Michael Anthony Pugel, filed June 16, 2006, published December 21, 2007.

(3) "Gomez" U.S. Patent No. 8,224,274 to Ramon Gomez et al., filed December 17, 2008, and issued July 17, 2012.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis (i.e., changing from AIA to pre-AIA) for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 and 11 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Pugel in view of Gomez

With respect to claims 1 and 11, Pugel teaches a system and a method comprising: in a wideband receiver system (**Abstract, wherein Pugel teaches receiver that processes frequencies in the range between 5MHz and 900 MHz (i.e. wideband receiver system)**: downconverting, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels (**paragraphs [0024] and claim 18, wherein plurality of analog signals in different frequency ranges are converted into digital signals and wherein the signals then are downconverted as explained in claim 18**); digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels (**paragraphs [0009], [0024] and claim 18, wherein entire signal input (i.e. both desired and undesired television channels) are processed and first and second digital signals are formed)**; selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies (**"*selecting (e.g., extracts or selects),by***

digital circuitry(e.g., digital channel select or of the digital tuner) of said wide band receiver system(e.g., Pugel's apparatus), said plurality of desired television channels (e.g., Pugel's digital channels desired to be recovered) from said digitized plurality of frequencies (e.g., from the digitized analog signals). Specifically, Pugel discloses extracting desired television programs (e.g., particular digital channels desired to be recovered) from the down converted, digitized frequencies (e.g., the "downconvert[ed]... first digital signal and ... second digital signal.")" paragraph [0038] and Figure 3, wherein tuner 130 corresponds to the selecting unit, and wherein "extracting" corresponds to the step of selection, wherein desired information is extracted to be provided to demodulator. See also paragraphs [0042] – [0045] and Abstract); and outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels as a digital datastream (**paragraphs [0010], [0024], [0040] and Figure 3. More specifically Pugel teaches that each separate analog signal is converted from analog to digital form in an analog-to-digital converter 121, 122 and 123. Each digital channel signal is coupled to a separate demodulator 141, 142 and 143**).

Pugel, however does not explicitly disclose that the downconverting is performed by a mixer module of the wideband receiver system.

On the other hand, Gomez teaches a tuner which selects and downconverts a desired or selected channel from a RF input signal. More specifically mixer 301 down-converts the desired channel in RF signal (**4:6-19**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teachings of Pugel and Gomez and utilize Gomez's teaching about employing a mixer to perform down-conversion in order to efficiently processing inputted signals. Pugel teaches down-conversion performed after the conversion from analog to digital, performing this step before A/D conversion was well known in the art and thus it would be obvious to one of ordinary skill in the art to change the order of the operations if needed.

Response to Arguments

Applicant's arguments filed June 18th, 2024 have been fully considered but they are not persuasive.

Argument #1: In the first argument, on pages 7-9, the Patent Owner contends "*McNeely specifically notes that "the process used by the FTM 110 is different from a direct tuning of those certain physical channels since other energy besides the selected channel may be present, and the channels are then recombined to form a new signal for further distribution." (7:17—21) … Pugel next discloses that the converted digital signals are coupled to digital tuner 130, which demultiplexes the converted digital signals to generate a plurality of digital channel signals … Each digital channel signal is then coupled to a separate demodulator, which performs demodulation and forward-error-correction (FEC) operations appropriate for the content of that digital channel … McNeely makes it explicitly clear that its FTM is not a tuner. This is because "the process used by the FTM 110 is different from a direct tuning of those certain physical channels since other energy besides the selected channel may be present, and the*

channels are then recombined to form a new signal for further distribution." (7:17—21). In other words, McNeely's FTM filters out some—but not all—of the undesired channels and outputs a combination of desired and undesired channels."

***Examiner's Response**:* The Examiner did not find the Patent Owner's argument persuasive. It is important to note that since US Patent No. 9,210,362 is not expired, thus claims are interpreted according to the broadest reasonable interpterion standard explained in MPEP 2111:

"The broadest reasonable interpretation does not mean the broadest possible interpretation. Rather, the meaning given to a claim term must be consistent with the ordinary and customary meaning of the term (unless the term has been given a special definition in the specification), and must be consistent with the use of the claim term in the specification and drawings. Further, the broadest reasonable interpretation of the claims must be consistent with the interpretation that those skilled in the art would reach".

More specifically claims 1 and 11 are directed to a receiver including a mixer module, analog to digital converter (ADC) module and circuitry to select a desired television channels and forward those channels to a demodulator. There is no mention in the claim language of a tuner and specific function that this unit would perform. As demonstrated in the rejection, all of the modules recited above are taught by the cited prior art. For instance, Patent Owner argue that McNeely teaches that some but not all undesired channels are filtered and a combination of desired and undesired channels is output for further processing. The Examiner disagrees with this interpretation. For instance, Figure 2 denotes that signal containing both desired ("selected") and undesired ("not selected") channels, is inputted into the unit 210 which as explained on page 9, lines 8-15, can filter frequencies and it also includes mixing circuits necessary to position band signal in the correct frequency range for operation of the A/D converter.

Furthermore, down-conversion takes place when a higher frequency signal is converted to a lower frequency signal. As explained by McNeely, the signal frequency is in the 1-2GHz frequency range and input into the A/D is at the frequency range of 975 and 1425MHz, thus the original signal is down-converted by the mixer 210 to feed the signal at the lower frequency band into A/D.

At this point the signal is sent over to element 220 where the analog signal is digitized. Subsequently, element 230 receives the output from the converter and selects certain channels (i.e. desired channels). On contrary, to what the Patent Owner alleges the re-combined signal does not include both desired and not desired signals but instead it can be an aggregate of the desired signals. For instance, page 10, lines 12-16 explains:

> "*The digital channel re-combiner 240 frequency translates the individual selected channels each to a different 15 and separate frequency range and combines these signals together to form a single selected digital signal*".

Argument #2: In the second argument on page 10, the Patent Owner alleges that "*The OA fails to demonstrate that McNeely is analogous art … To be analogous, a reference must be either (1) from the same field of endeavor as the patent-at-issue, or (2) reasonably pertinent to the particular problem with which the inventor of the challenged patent is involved … The '362 Patent explains that tuners are "[r]eceivers used to down-convert and selectively filter TV channels." (1:24-27). This is why, for example, Claim 1 recites "[a] wideband receiver system channels is not contiguous, this swath includes the desired channels as well as undesired channels. Accordingly, the*

'362 Patent aims to improve upon wideband tuner architecture by "eliminat[ing] the need of expensive data conversion, filtering and channel selection on the demodulator side" and by "remov[ing] undesired channels from the signal path at an early stage, thus reliev[ing] the large dynamic range requirement in the demodulator." (6:60-64).

McNeely is not directed to a tuner, nor does it attempt to solve the problem of eliminating expensive data conversion, filtering, and channel selection from the demodulator side of a tuner. As explained above, McNeely is directed to an improved frequency translation module (FTM). McNeely explains that an FTM is used in satellite television systems because the signals travelling from the satellite dishes into the customer home occupy too much frequency for delivery over a single coaxial cable. (McNeely, 7:6-9). The FTM addresses this problem by performing what McNeely calls a "preselection" of certain physical channels, a process even McNeely acknowledges is different than tuning. (/d. at 7:11-26). McNeely makes it explicitly clear that its FTM is not a tuner.".

***Examiner's Response**: The Examiner did not find the above argument persuasive.* In response to applicant's argument that McNeely is nonanalogous art, it has been held that a prior art reference must either be in the field of the inventor's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, McNeely teaches a system which includes a receiver for receiving and digitizing plurality of signals and recovering a set of selected channels from plurality

of signals (page 3, lines 21-26). Accordingly, McNeely and '362 Patent both receive and process signals (i.e. field of endeavor) and thus are deemed analogous arts.

Argument #3: Then on page 10, the Patent Owner contends "*McNeely's FTM filters out some—but not all—of the undesired channels and outputs a combination of desired and undesired channels. And this is because McNeely is only concerned with making sure the signal bandwidth is narrow enough for delivery into the home on a single coaxial cable, rather than making sure that only the selected channels arrive at the demodulator side of a tuner … McNeely Does Not Disclose or Suggest "Select{ing] Said Plurality of Desired Television Channels … McNeely makes it expressly clear that FTM 110 does not "select said plurality of desired television channels" as required by the claims. As McNeely explains:*

> *The FTM 110 extracts certain ranges of frequencies containing selected physical channels as portions of the three L-band signals provided. . . . The process used by the FTM 110 may be described as a preselection of certain physical channels. However, the process used by the FTM 110 is different from a direct tuning of those certain physical channels since other energy besides the selected channel may be present, and the channels are then recombined to form a new signal for further distribution."*

In other words, rather than selecting (and outputting) the desired television channels, McNeely's FTM selects ranges of frequencies containing the desired channels (and undesired channels). (/d. at 7:11-13). McNeely itself characterizes this as only a "preselection" because the outgoing signal still contains a mix of desired and undesired channels. (/d. at 7:15— 19). This is why McNeely still relies on the set-top boxes to actually tune to the desired channels before those channels can be demodulated … The OA Fails to Allege a Rational Basis to Modify McNeely Based On

Pugel's Alleged Teaching of "Outputting the Selected Plurality of Television Channels to a Demodulator".

***Examiner's Response**:* The Examiner found the above argument persuasive. *Accordingly, the Rejection of claims 1 and 11 under 35 U.S.C. 103(a) over McNeely in view of Pugel are withdrawn.*

***Argument #4**: On page 12, the Patent Owner alleges that "The Examiner asserts that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of McNeely and Pugel and utilize Pugel's demodulator to process a digital datastream of McNeely." (OA at 5). This assertion ignores the actual teachings of McNeely, which confirm that there is no "digital datastream of McNeely," instead McNeely outputs an analog data stream".*

Examiner's Response: This argument is moot because the Examiner has found the previous argument #3 persuasive.

Argument #5: On page 15, the Patent Owner asserts "*As an initial matter, the OA does not explain why a person skilled in the art would initially look to modify Pugel in view of Gomez … Pugel's "single digital receiver circuit" includes both a tuner and demodulators. (Pugel, Fig. 1). In contrast, Gomez relates to channel switching in a satellite FTM. (Gomez at 1:15-57). Although Gomez discloses that its FTM may contain one or more tuners (/d. at 1:41), Gomez teaches that its FTM is separate from the receivers, which Gomez refers to as integrated receiver decoder(s) [IRD], and which*

Gomez confirms are located within the home ("IRD located within a household"). /d. at 1:38-41). Gomez does not concern itself with the architecture or features of the receiver, instead describing functionality that exists elsewhere in the signal delivery system. And in fact, Gomez goes against the very idea of Pugel, which is directed to a single digital receiver circuit that performs both tuning and demodulation".

***Examiner's Response**: The Examiner did not find the above argument persuasive because Pugel and Gomez are considered analogous arts because they belong the same field of endeavor covering receiving and processing signals and tuners.*

Furthermore, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See In re McLaughlin, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In this instance, down converting data was well known in the art as lowering frequency is often a necessary step in simplifying subsequent radio stages. In addition, the Examiner wishes to point out that Gomez reference has been used as a secondary reference to show that down converting step was well known in the art at the time the invention was made and thus it is not required for Gomez reference to teach a receiver as described in the claims 1 and 11.

Argument #6: On page 16, the Patent Owner further contends "*First, the claim language requires "downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels." The relied upon mixer 301 of Gomez downconverts only the desired channel(s), as the down-conversion happens after the tuning to the desired frequency has occurred*".

***Examiner's Response**:* The Examiner did not find the above argument persuasive because Pugel's teaching has been relied upon for processing plurality of frequencies comprising both desired and undesired channels. More specifically paragraph [0024] teaches processing multiple frequency bands comprising both channels. As later taught in paragraph [0038], a selection step takes place where desired channels can be selected and only those will further pass on for further processing. Gomez's reference has been introduced to show that down-converting by a mixer module was well known in the art, thus one of ordinary skill in the art at the time the invention was made would be capable of incorporating a down-conversion step of the data (i.e. frequency band comprising both desired and undesired channels) provided by Pugel. In other words, mere down-conversion step in signal processing would not be considered an inventive step at the time the invention was made.

Argument #7: Continuing on pages 16 and 17, the Patent Owner also submits that "*the Examiner relies on Pugel's disclosure of downconverting a digital signal.*

(Pugel at Cl. 18; OA at 5). However, Gomez does not teach the use of a mixer to perform digital downconversion. Rather, Gomez teaches that mixer 301 is an analog mixer. This is evident because mixer 301 receives an RF input signal (4:10-12) and because Figure 3 of Gomez does not disclose any digitization of the RF signal … While Gomez does disclose that "Mixer 1201 receives digital data" and that "Mixer 1205 up-converts the frequency of the digital signal," Gomez does not indicate that either of these two mixers performs down-converting. (/d. at 7:66, 8:46-47). The OA does not explain why a person skilled in the art would find it obvious to modify Pugel based on Gomez to arrive at the claim language, when Gomez does not teach the use of a mixer to perform the digital downconversion that occurs in Pugel.".

Examiner's Response: The Examiner did not find the above argument persuasive. While Pugel teaches doewnconverting a signal, it has been noted on page 6 that he doesn't teach downconverting the analog signal by the mixer (i.e. before conversion of analog to digital). Accordingly, the Examiner introduced the secondary reference, Gomez to demonstrate that downconverting an RF analog signal prior to conversion to digital was well known in the art (column 4, lines 4-7). Consequently, Gomez does not need to teach downconverting digital signals even he also mentions this embodiment in column 12, lines 29-33 and claims 17 and 21. Instead as clearly indicated in the rejection on page 6, the teaching about downconverting RF signals is being relied upon.

In addition, the Patent Owner alleges that in Gomez mixer performs up-conversion but there is no teaching about down-conversion. The Examiner disagrees with this assessment because as explained in the rejection on page 6, the Examiner

relied upon RF (analog) signal downconversion, thus before signal is converted to its digital form the downconversion would take place. Accordingly, Pugel discusses analog signal processing and so does Gomez.

Argument #8: Then in the last argument on page 17, the Patent Owner alleges that "*Third, Gomez actually teaches that there are disadvantages with using analog components such as mixers, and one of the stated goals of Gomez is to minimize the number of such analog components that are used*".

***Examiner's Response**:* The Examiner did not find the above argument persuasive because Gomez explicitly teaches downconverting RF signal in column 4, lines 4-19, thus even though he would suggest that digital signal processing may be more beneficial to analog, he certainly confirms that downconverting analog signal was well known in the art at the time the invention was made and could be reliably performed.

Conclusion

Claims 1 and 11 are rejected under 35 U.S.C. 103(a).

THIS ACTION IS MADE FINAL.

A shortened statutory period for response to this action is set to expire 2 months from the mailing date of this action.

Extensions of time under 37 CFR 1.136(a) do not apply in reexamination proceedings. The provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Further, in 35 U.S.C. 305 and in 37 CFR

1.550(a), it is required that reexamination proceedings "will be conducted with special dispatch within the Office."

Extensions of time in reexamination proceedings are provided for in 37 CFR 1.550(c). A request for extension of time must be filed on or before the day on which a response to this action is due, and it must be accompanied by the petition fee set forth in 37 CFR 1.17(g). The mere filing of a request will not effect any extension of time. An extension of time will be granted only for sufficient cause, and for a reasonable time specified.

The filing of a timely first response to this final rejection will be construed as including a request to extend the shortened statutory period for an additional month, which will be granted even if previous extensions have been granted. In no event however, will the statutory period for response expire later than SIX MONTHS from the mailing date of the final action. See MPEP § 2265.

NOTICE RE PATENT OWNER'S CORRESPONDENCE ADDRESS

Effective May 16, 2007, 37 CFR 1.33(c) has been revised to provide that: The Patent owner's correspondence address for all communications in an ex parte reexamination is designated as the correspondence address of the patent.

Revisions and Technical Corrections Affecting Requirements for Ex Parte Reexamination, 72 FR 18892 (April, 16, 2007) (Final Rule)

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of

this revision to 37 CFR 1.33(c), automatically changed to that of the patent file as of the effective date.

This change is effective for any reexamination proceeding which is pending before the Office as of May 16, 2007, including the present reexamination proceeding, and to any reexamination proceeding which is filed after that date.

Parties are to take this change into account when filing papers, and direct communications accordingly.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of Change of Correspondence Address in the reexamination proceeding and/or the patent (depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone Numbers for reexamination inquiries:

Reexamination	(571) 272-7703
Central Reexam Unit (CRU)	(571) 272-7705
Reexamination Facisimile Transmission No.	(571) 273-9900

Extensions of Time

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and

not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extension of time in reexamination proceedings are provided for in 37 CFR 1.550(c). After the filing of a request for reexamination by a third party requester, any document filed by either the patent owner of the third party requester must be served on the other party (or parties where two or more third-party-requester proceedings are merged) in the reexamination proceeding in the manner provided in 37 CFR 1.248. See 37 CFR 1.550(f).

Litigation Reminder

The patent owner is reminded of the continued responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP § 2207, 2282 and 2286.

Correspondence

All correspondence relating to this *ex parte* reexamination proceeding should be directed:

Patent Center: Please use Patent Center (https://www.uspto.gov/patents/apply/patent-center) to file and manage your applications and requests.

By Mail to: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Patent Center

The USPTO is retiring EFS-Web and Private Pair, effective 15 November 2023. Please use Patent Center (https://www.uspto.gov/patents/apply/patent-center) to file and manage your applications and requests. Visit the EFS-Web and Private PAIR Retirement (https://www.uspto.gov/patents/efs-web-and-private-pair-be-retired) and Patent Center Information pages for more information.

Patent Center has 100% of the functionality of EFS-Web and Private PAIR, and is available to all users for electronic filing and management of patent applications. Attend a transition to Patent Center Training session (https://www.uspto.gov/about-us/events/patent-center) to learn more about filing and managing patent applications.

Any inquiry concerning this communication should be directed to the Central Reexamination Unit at telephone number 571-272-7705.

/ANGELA M LIE/
Primary Examiner, Art Unit 3992

Conferees:

/LUKE S WASSUM/
Primary Examiner, Art Unit 3992
/MICHAEL FUELLING/
Supervisory Patent Examiner, Art Unit 3992

Office Action in Ex Parte Reexamination	**Control No.** 90/019,255	**Patent Under Reexamination** 9210362	
	Examiner ANGELA M LIE	**Art Unit** 3992	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a. ☑ Responsive to the communication(s) filed on 18 June 2024.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

b. ☑ This action is made FINAL.

c. ☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☑ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☑ Claims 1 and 11 are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims _____ are patentable and/or confirmed.
4. ☑ Claims 1 and 11 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a) ☐ approved (7b) ☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the certified copies have
   1 ☐ been received.
   2 ☐ not been received.
   3 ☐ been filed in Application No. _____.
   4 ☐ been filed in reexamination Control No. _____.
   5 ☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

Reexamination	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/019,255	9210362
	Certificate Date	Certificate Number

Requester Correspondence Address: ☐ **Patent Owner** ☑ **Third Party**

Haynes and Boone, LLP
2801 N. Harwood St.
Suite 2300
Dallas TX 75201

LITIGATION REVIEW ☑	A.M.L (examiner initials)	14 March 2024 (date)
Case Name		Director Initials
IPR2024-00434		
IPR2024-00433		
IPR2024-00432		
2:23cv1049 Entropic Communications Llc v. Cox Communications, Inc		
2:22cv125 Entropic Communications Llc v. Charter Communications Inc.		

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	**NUMBER**

/ANGELA M LIE/ Primary Examiner, Art Unit 3992	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.M.L/

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	90019255
	Filing Date	2023-09-20
	First Named Inventor	Madhukar Reddy
	Art Unit	3992
	Examiner Name	LIE, ANGELA M
	Attorney Docket Number	189005.TR003

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	9210326	B2	2015-12-08	AKIRA MIYATA	
	2	5535240	A	1996-07-09	RONALD R. CARNEY et al.	
	3	6906498	B2	2005-06-14	GEORG BREUCH et al.	
	4	6992855	B2	2006-01-31	RICHARD M. EHRLICH	
	5	7265792	B2	2007-09-04	PIERRE FAVRAT et al.	
	6	7522901	B2	2009-04-21	LEONARD DAUPHINEE	
	7	7496158	B2	2009-02-24	GERALD L. FUDGE et al.	
	8	7421259	B2	2008-09-02	RAMON A. GOMEZ et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.M.L/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Art Unit	3992
	Examiner Name	LIE, ANGELA M
	Attorney Docket Number	189005.TR003

	9	7373125	B2	2008-05-13	NIHAL GODAMBE et al.	
	10	5280636	A	1994-01-18	EDWIN A. KELLEY et al.	
	11	7685217	B2	2010-03-23	HENRIK T. JENSEN et al.	
	12	7167694	B2	2007-01-23	RAMIN KHOINI-POORFARD et al.	
	13	8577319	B2	2013-11-05	CURTIS LING et al.	
	14	7362178	B2	2008-04-22	RAYMOND MONTEMAYOR et al.	
	15	9059672	B2	2015-06-16	CURTIS LING et al.	
	16	7599673	B2	2009-10-06	ADRIAN MAXIM et al.	
	17	8300681	B2	2012-10-30	BRANISLAV PETROVIC et al.	
	18	6334051	B1	2001-12-25	HIROSHI TSURUMI et al.	
	19	8374569	B2	2013-02-12	KISHORE SEENDRIPU et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.M.L/

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	Attorney Docket Number	189005.TR003

	20	8374568	B2	2013-02-12	KISHORE SEENDRIPU et al.	
	21	8909187	B2	2014-12-09	KISHORE SEENDRIPU et al.	
	22	8285240	B2	2012-10-09	KISHORE SEENDRIPU et al.	
	23	7027520	B2	2006-04-11	MICHAEL ANTHONY PUGEL	
	24	8526898	B2	2013-09-03	MADHUKAR REDDY et al.	
	25	8902369	B2	2014-12-02	MICHAEL ANTHONY PUGEL	
	26	8374570	B2	2013-02-12	KISHORE SEENDRIPU et al.	
	27	8666350	B2	2014-03-04	ARI VAUHKONEN	
	28	6704372	B2	2004-03-09	WEIMIN ZHANG et al.	
	29	7394871	B2	2008-07-01	WEIMIN ZHANG et al.	
	30	7095454	B2	2006-08-22	MATTHEW GLENN WAIGHT et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.M.L/

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	Attorney Docket Number	189005.TR003

	31	7237214	B1	2007-06-26	AWARTIKA PANDEY et al.	
	32	7783958	B1	2010-08-24	DONALD BRIAN EIDSON et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20070111661	A1	2007-05-17	KEITH BARGROFF et al.	
	2	20100061432	A1	2010-03-11	OREN BEN-HAMO et al.	
	3	20070081617	A1	2007-04-12	GERALD FUDGE	
	4	20030228855	A1	2003-12-11	WILLIAM HERZ et al.	
	5	20070042742	A1	2007-02-22	BONKEE KIM et al.	
	6	20080186409	A1	2008-08-07	HYUN-KOO KANG et al.	
	7	20050190777	A1	2005-09-01	KENDAL HESS et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.M.L/

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	8	20070091212	A1	2007-04-26	JEONG-HO LEE et al.	
	9	20070098089	A1	2007-05-03	JUNSONG LI et al.	
	10	20080261638	A1	2008-10-23	SAMI R. WAHAB et al.	
	11	20090290659	A1	2009-11-26	BRANISLAV PETROVIC et al.	
	12	20080225175	A1	2008-09-18	VYACHESLAV SHYSHKIN et al.	
	13	20040001688	A1	2004-01-01	RICHARD SHEN	
	14	20060083335	A1	2006-04-20	KISHORE SEENDRIPU et al.	
	15	20050040909	A1	2005-02-24	MATTHEW WAIGHT et al.	
	16	20080100753	A1	2008-05-01	FUCHENG WANG et al.	
	17	20060233147	A1	2006-10-19	PETERD.KARABINIS	
	18	20060256216	A1	2006-11-16	KISHI TAKAHIKO et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.M.L/

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	Examiner Name	LIE, ANGELA M
	Attorney Docket Number	189005.TR003

	19	20060029170	A1	2006-02-09	HENRIK T. JENSEN et al.			

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2006119489	WO	A2	2006-11-09	DAVID LOWELL MCNEELY		☒
	2	2006119490	WO	A2	2006-11-09	DAVID LOWELL MCNEELY		☒
	3	2087623	EP	A2	2009-08-12	RF MAGIC INC		☒
	4	0696854	EP	A1	1996-02-14	WERNER BOIE		☐
	5	2007145637	WO	A1	2007-12-21	MICHAEL ANTHONY PUGEL		☐
	6	2006118722	WO	A1	2006-11-09	DAVID EMERY VIRAG et al.		☐

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.M.L/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Madhukar Reddy
	Art Unit	3992
	Examiner Name	LIE, ANGELA M
	Attorney Docket Number	189005.TR003

	1	JEFFREY A. WELDON, et al. "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter With Harmonic-Rejection Mixers," IEEE Journal of Solid-Slate Circuits, December 2001, pages: 2003-2015, Vol. 36, No. 12, Seattle, WA, USA.	☐
	2	FRANCESCO GATTA, et al. "An embedded 65nm CMOS low-IF 48 MHz to 1 GHz dual tuner for DOCSIS 3.0," 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, Feb. 12, 2009,pages: 122-123, San Francisco, CA, USA.	☐
	3	System Art - Broadcom BCM 3380 Broadcom Jun. 10, 2008	☐
	4	Silicon-based RF front-ends for ultra wideband radios UWB textbook Jan. 2008	☐
	5	System Art - Motorola SURFboard cable modem SB6120 Motorola / Arris 2007	☐
	6	MIRABBASI and K. MARTIN, “Classical and Modern Receiver Architectures,” IEEE Communications Magazine, vol. 38, no. 11, pp. 132-139, November 2000	☐
	7	JAN M RABAEY, “Digital Integrated Circuits: A Design Perspective” Pearson, 2nd ed. 2002	☐
	8	J. CROLS and M. S. J. STEYAERT, “Low-IF topologies for high-performance analog front ends of fully integrated receivers,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998	☐
	9	A. P. CHANDRAKASAN, “Ultra low power digital signal processing,” Proceedings of 9th International Conference on VLSI Design, Bangalore, India, 1996, pp. 352-357	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/ANGELA M LIE/	Date Considered	07/31/2024

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
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	Filing Date	2023-09-20
	First Named Inventor	Madhukar Reddy
	Art Unit	3992
	Examiner Name	LIE, ANGELA M
	Attorney Docket Number	189005.TR003

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2023-09-20
	First Named Inventor	Madhukar Reddy
	Art Unit	3992
	Examiner Name	LIE, ANGELA M
	Attorney Docket Number	189005.TR003

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Hao Tan/	Date (YYYY-MM-DD)	2024-06-18
Name/Print	Hao Tan	Registration Number	73,711

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/019,255	09/20/2023	9210362	189005.TR003	5785

153979 7590 09/27/2024

Arch & Lake LLP
203 North LaSalle Street, Suite 2100
Chicago, IL 60601

EXAMINER	
LIE, ANGELA M	

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
09/27/2024	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

Haynes and Boone, LLP
2801 N. Harwood St.
Suite 2300
Dallas TX 75201

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/019,255* .

PATENT UNDER REEXAMINATION *9210362* .

ART UNIT *3992* .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

PTOL-465 (Rev.07-04)

Ex Parte Reexamination Interview Summary	Control No.	Patent Under Reexamination	
	90/019,255	9210362	
	Examiner	Art Unit	AIA (FITF) Status
	ANGELA M LIE	3992	No

All participants (USPTO personnel, patent owner, patent owner's representative):

(1) ANGELA LIE (PE), Luke Wassum (PE)	(3) Frank Koperda (Expert), Zhangyuan Ji (80046)
(2) Alexander Kosowski (SPE)	(4) Hao Tan (73711), Christopher Fahy

Date of Interview: 23 September 2024

Type: a) ☐ Telephonic b) ☑ Video Conference
c) ☐ Personal (copy given to: 1) ☐ patent owner 2) ☐ patent owners representative)

Exhibit shown or demonstration conducted: d) ☐ Yes e) ☑ No.
If Yes, brief description: _____

Agreement with respect to the claims f) ☐ was reached. g) ☐ was not reached. h) ☑ N/A.
Any other agreement(s) are set forth below under "Description of the general nature of what was agreed to..."

Claim(s) discussed: 1 .

Identification of prior art discussed: Pugel and Gomez .

Description of the general nature of what was agreed to if an agreement was reached, or any other comments:
See Continuation Sheet .

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims patentable, if available, must be attached. Also, where no copy of the amendments that would render the claims patentable is available, a summary thereof must be attached.)

A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION MUST INCLUDE PATENT OWNER'S STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. (See MPEP § 2281). IF A RESPONSE TO THE LAST OFFICE ACTION HAS ALREADY BEEN FILED, THEN PATENT OWNER IS GIVEN **ONE MONTH** FROM THIS INTERVIEW DATE TO PROVIDE THE MANDATORY STATEMENT OF THE SUBSTANCE OF THE INTERVIEW
(37 CFR 1.560(b)). THE REQUIREMENT FOR PATENT OWNERS STATEMENT CAN NOT BE WAIVED.
EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).

/ANGELA M LIE/ Primary Examiner, Art Unit 3992	/LUKE S WASSUM/ Primary Examiner, Art Unit 3992	/A.J.K/ Supervisory Patent Examiner, Art Unit 3992

cc: Requester (if third party requester)

Continuation of Description of the general nature of what was agreed to if an agreement was reached, or any other comments: Ms. Ji has disccused Gomez as a secondary prior art. She has contended that Gomez operates at different frequency ranges than Pugel. Furthermore it has also been argued that claim 1 recites multiple channels going into the mixer for downconversion and multiple channels being outputted while Gomez allegedly teaches multiple channels inputted for downconversion and only a single channel being outputted, therefore Ms. Ji submitted that Gomez's mixer would not read on the mixer disclosed in claim 1. The Examiner has stated that once the formal response is submitted, the rejections will be reconsidered in view of the remarks and Koperda Declaration.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 90/019,255	Filing Date 09/20/2023	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	09/30/2024	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/RHONDA BELL/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

I. INTRODUCTION

1. My name is Frank Koperda, and I am over 21 years old and otherwise competent to make this Declaration. I make this Declaration based on facts and matters within my own knowledge and on information provided to me by others, and, if called as a witness, I could and would competently testify to the matters set forth herein.

2. I have been retained as a technical expert witness in this matter by Counsel for the Patent Owner, Entropic Communications, LLC ("Entropic") to provide my independent opinions on certain issues relating to Ex Parte Reexamination No. 90/019,255 for U.S. Patent No. 9,210,362 ("the '362 Patent"), in which Claims 1 and 11 currently stand rejected. My compensation in this matter is not based on the substance of my opinions or on the outcome of this matter. Nor do I hold any financial interest in Entropic.

II. QUALIFICATIONS

3. I have earned a Master's of Science Degree in Computer Engineering from Case Western Reserve University and have been involved in designing, building, and programming electronic systems since 1971. I have participated in the standards development process including several relating to data/video delivery over the Cable TV systems. I have several patents relating to the monitoring and control of information sent in such systems.

4. I worked for IBM over a number of years and was their representative to national and international standards groups. I participated in the IEEE standards development of the 802.11 Wireless LAN standard which includes multiple types of physical layers, including several RF bands and a variety of modulation techniques.

5. I started the IEEE committee 802.14 relating to data/video over the cable TV systems. Later, I was chief architect for data communications at Scientific Atlanta developing the

cable modems and headend systems that monitor and control content delivery. Later, this effort transitioned to CableLabs where I also participated in that standards evolution (DOCSIS).

6. I have extensive knowledge in RF communications, having an FCC First Class Commercial Radio telephone license. I have worked in commercial TV & radio stations monitoring and repairing transmitters and other equipment. I also hold an FCC Technicians Class Amateur Radio license. I am very familiar with many modulation techniques, channel issues, interference, down converting, and RF mixers (transmit and receive).

7. Appendix 1 contains my detailed CV.

III. MATERIALS CONSIDERED

8. In forming my opinions, I have reviewed the '362 Patent, the August 7, 2024 Final Rejection, and the prior art references cited therein, including:

a. WO 2006/119490 to David Lowell McNeely ("McNeely")

b. WO 2007/145637 to Michael Anthony Pugel ("Pugel")

c. U.S. Patent No. 8,224,274 to Ramon Gomez et al. ("Gomez")

IV. LEGAL FRAMEWORK

9. I am a technical expert, and I do not offer any legal opinions. However, I have been informed about certain legal principles regarding patentability and related matters under United States patent law, which I have applied in performing my analysis and arriving at my technical opinions in this matter.

a. Obviousness

10. I understand that a patent claim is obvious if the subject matter of the claim would have been obvious to one of ordinary skill in the art in light of the teachings of the prior art. Obviousness often involves combining more than one prior art reference. I understand that the following factors must be evaluated to determine whether a claim is obvious:

a. the scope and content of the prior art;

b. the difference or differences, if any, between each claim and the prior art;

c. the level of ordinary skill in the art at the time the invention was made; and

d. additional secondary considerations, if any, that indicate that the invention was obvious or not obvious.

11. I understand that it would be improper to base an obviousness determination on a "hindsight" analysis, *i.e.*, to use the teachings of the patent as a roadmap to combine prior art references or otherwise to find a claim obvious. Instead, the analysis must be guided by the prior art references and the then-existing knowledge, skill, and creativity of a POSITA at the time of the invention.

12. I understand that, to support the conclusion that the claimed invention is directed to obvious subject matter, the references must either expressly or impliedly suggest the claimed invention. I understand that rejections based on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. I understand that if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims obviousness. I understand that if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.

b. Analogous Art

13. I understand that, for a reference to be considered as part of an obviousness determination, the reference must be analogous art to the claimed invention. To be analogous, a reference must either be 1) from the same field of endeavor as the patent or 2) reasonably pertinent

to the particular problem which the patent inventor sought to address. I understand that these are two separate tests, and a reference need not fulfill both tests to qualify as analogous art.

14. When determining whether the "relevant field of endeavor" test is met, I understand that one should consider explanations of the invention's subject matter in the patent application, including the embodiments, function, and structure of the claimed invention. When determining whether a prior art reference is in the same field of endeavor, the primary focus is on what the reference discloses. The examiner must also consider the disclosure of each reference in view of the reality of the circumstances. These circumstances are to be weighed from the vantage point of the common sense likely to be exerted by one of ordinary skill in the art in assessing the scope of the endeavor.

15. As for the "reasonably pertinent" test, I understand that one should consider the problem faced by the inventor as reflected, either explicitly or implicitly, in the specification. For a reference to be "reasonably pertinent" to the problem, it must logically have commended itself to an inventor's attention in considering his problem." A reference outside of the field of endeavor is reasonably pertinent if a person of ordinary skill would have consulted it and applied its teachings when faced with the problem that the inventor was trying to solve. I understand the question of whether a reference is reasonably pertinent often turns on how the problem to be solved is perceived. If the problem to be solved is viewed in a narrow or constrained way, and such a view is not consistent with the specification, the scope of available prior art may be inappropriately limited. It may be necessary for the examiner to explain why an inventor seeking to solve the identified problem would have looked to the reference in an attempt to find a solution to the problem, *i.e.*, factual reasons why the prior art is pertinent to the identified problem.

16. For example, I understand that a reference directed to a gel used in the ***extraction of crude oil*** was not analogous art to a similar gel used in the ***storage of refined oil***. In this regard, that each was directed to oil, or oil refining was found to be insufficient to establish the reference was analogous. In another example, I understand that a reference directed to memory circuits in which modules of varying sizes could be added or replaced was not analogous art to compact modular memories with a fixed size. In this regard, that each was directed towards memory modules was not enough to establish that a variable sized reference was analogous to compact fixed modules.

c. Motivation to Combine

17. I understand that for a claim to be obvious, it must be that a POSITA would have been motivated to combine or modify the prior art to achieve the claimed invention and would have had a reasonable expectation of successfully combining or modifying the prior art. I understand that the suggestion to modify or combine relevant prior art references may come from either:

a. a teaching or suggestion in the prior art references;

b. the common sense of a POSITA;

c. any need or problem known to a POSITA and addressed by the claimed invention, including, but not limited to, the problem addressed by the patent; or

d. design incentives and other market forces.

18. I further understand that obviousness should not be evaluated using the benefit of hindsight or what is known today.

19. I further understand that it is improper to combine references where the references teach away from their combination. I understand that a reference may be said to teach away when a POSITA, upon reading the reference, would be discouraged from following the path set out in

the patent, or would be led in a direction divergent from the path that was taken by the patent applicant. In general, a reference teaches away if it suggests that the line of development flowing from the reference's disclosure is unlikely to produce result sought by the patentee. I understand that references teach away, for example, if (1) the combination would produce a seemingly inoperative device, or (2) the references leave the impression that the resulting product would not have the property or properties sought by the patentee. However, I understand that a reference does not teach away if it merely expresses a general preference for an alternative invention, without criticizing, discrediting, or otherwise discouraging investigation into the claimed invention. Further, a POSITA will often appreciate that different courses of action often have simultaneous advantages and disadvantages, and I understand the existence of such does not necessarily obviate a motivation to combine.

V. OPINIONS

a. Level of Ordinary Skill

20. In my opinion, a POSITA with respect to the '362 Patent would be an engineer with at least a bachelor's degree in electrical engineering (or equivalent), with at least two years of experience developing cable TV communication systems and solutions. This is the perspective from which I have analyzed the '362 Patent for my opinions.

21. By this standard, I believe I was a person with at least ordinary skill in the art around the time of the earliest priority date of the '362 Patent.

b. Overview of the '362 Patent

22. The '362 Patent relates to a "Wideband Tuner Architecture" for use in "[a] wideband receiver system." '362 Patent, Abstract. In particular, the patent "relates to wideband receiver systems that are capable of receiving multiple desired television channels that extend over

multiple non-contiguous portions of the broad frequency spectrum and grouping them into a contiguous, or substantially-contiguous, frequency spectrum." *Id.* at 1:18–23.

23. In television systems, a *receiver* is a device located within the customer's home that receives analog signals comprising one or more television channels. The receiver tunes and demodulates (*i.e.*, extracts) the desired channels from the signal and outputs those channels as a digital datastream to a television set or DVR. *See e.g. id.* at 1:24–25 ("Receivers used to down-convert and selectively filter TV channels are referred to as tuners"); *see also* Abstract.

24. The '362 Patent describes how the RF input signal to the receiver "may include the VHF and UHF television channels in a terrestrial television broadcasting system or the CATV channels in cable networks." *Id.* at 1:52–55.

25. An important aspect of the '362 Patent is that it claims to select a plurality of desired television channels from an input stream and output said selected plurality of television channels as a digital data stream. *See id.* at Claim 1, element c.

26. The '362 Patent was filed February 5, 2015, but claims priority to a provisional application filed on April 17, 2009. I have assumed April 17, 2009 as the relevant date for evaluating the state of the art and the level of ordinary skill.

c. Overview of the Prior Art References

i. Pugel

27. "Pugel" relates to a receiver device for use in a cable television environment. *See* Pugel, Title ("Multichannel Digital Cable Tuner"). In one embodiment, a multichannel receiver circuit includes a plurality of amplifier-filter circuits, a plurality of analog-to-digital converters, a digital tuner, and a plurality of demodulator circuits. *See id* at [0023]. Pugel discloses that the plurality of amplifier-filter circuits segregates the analog input signal into a plurality of separate analog signals of differing frequency ranges, or "bands." *Id.* at [0024]. For example, an

arrangement of three amplifier-filter circuits might be used, wherein the three circuits are configured to process frequencies from 5–300 MHz, 300–600 MHz, and 600–900 MHz respectively. *See id.* at [0028]. Each separate analog signal band is then converted from analog to digital form by an analog-to-digital converter (ADC). *See id.* at [0024].

28. Pugel then discloses that the converted digital signals are coupled to digital tuner 130, which demultiplexes the converted digital signals to generate a plurality of digital channel signals. *See id.* at [0027]. Pugel notes in particular that "[t]he digital tuner 130 may include a channel selector 315 to permit selection of one or more particular digital channels desired to be recovered." *Id.* at [0038]. Each digital channel signal is then coupled to a separate demodulator, which performs demodulation and forward-error-correction (FEC) operations appropriate for the content of that digital channel. *Id.* at [0027].

ii. Gomez

29. "Gomez" relates to a scalable architecture for a satellite channel switch, or frequency translation module (FTM). *See* Gomez, Title. More specifically, Gomez "relates to processing one or more input channels to a frequency translation module through a scalable switch architecture." *See id.* at 1:17–20.

30. An FTM is a device that is used in satellite television systems and which is typically located at or near a customer's satellite outdoor unit (ODU). This is depicted in Figure 1 of WO 2006/119490 ("McNeely"), which the Examiner previously cited as prior art.

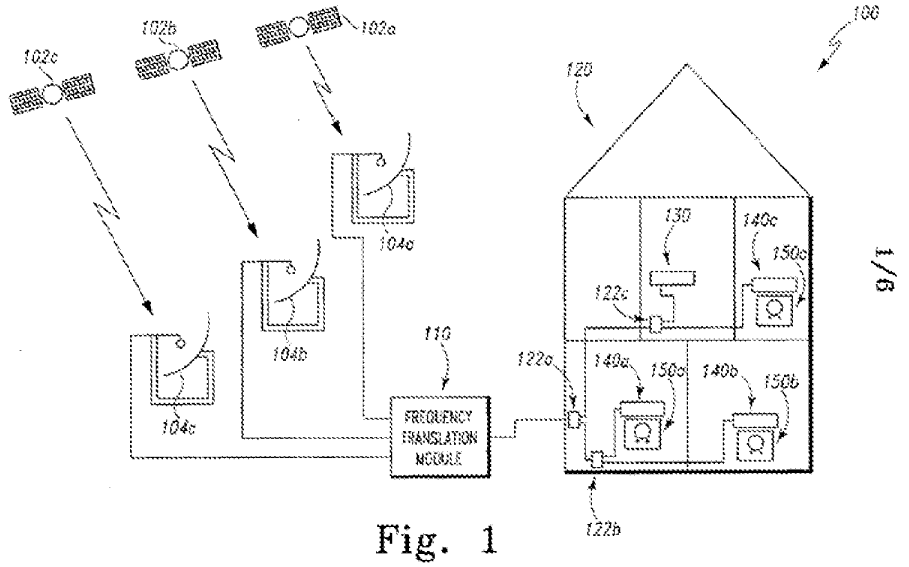


Fig. 1

31. The reason for using an FTM is that a typical subscriber household receives satellite broadcasts from multiple sources. The household might receive signals from multiple satellites in different orbital locations. *See* Gomez, 1:29–32. Moreover, each individual satellite may have multiple transponders, each of which transmits a signal with its own frequency band, direction of signal, and/or polarization. *See id.* at 1:32–35. An FTM "enables a user to selectively switch the signals received from each satellite antenna and deliver these signals to an IRD [integrated receiver decoder] located within a household." *See* Gomez, 1:38–41. This means that the signal which ultimately arrives at the IRD has a greatly reduced bandwidth. *See id.* at 8:58–9:2 (describing how the FTM produces a "reduced bandwidth signal containing channels of interest" and outputs it as an analog signal that the IRD can decode and separate into viewer channels); *see also* McNeely 7:11–21 (characterizing the FTM as performing a "preselection of certain physical channels" by extracting certain ranges of frequencies from the satellite signals).

32. Gomez's system is designed to provide at most a single TV channel from each of its antennas to be delivered into the IRD. Referring to Figure 3, one antenna (101) is coupled to a tuner (201) for that antenna, which outputs the single TV channel of interest.

> Mixer 303 receives the output of lowpass filter 302 and also receives a LO signal from PLL 306. Mixer 303 up-converts the output of lowpass filter 302 to generate a RF signal containing the channel of interest. Typically, the frequency of PLL 306 is tuned to a frequency within a frequency bandwidth that may be decoded by the IRD.
>
> Gomez, 4:34–39.

33. Gomez contains additional references to at most a single TV channel of interest being obtained from each antenna. *See id.* at 4:47–57 (referring to Figure 4 spectrum); 4:12–15 (PLL tuned to select the desired channel); 8:50–57 (each band has a single channel of interest); and 9:21–25 (D/A containing one channel of interest).

34. Accordingly, Gomez is directed to channel switching in a satellite FTM. In particular, Gomez states there is need for "a method or apparatus for implementing a scalable switch architecture for a FTM that minimizes circuit area and power consumption." *Id.* at 1:55–57. Accordingly, Gomez discloses that "digital frequency converters and filters, which are compact in modern integrated circuit technology and consume less power than their analog counterparts, may be used to implement a scalable FTM architecture." *Id.* at 1:61–65.

d. Gomez is Not Analogous Art

35. In my opinion and as I further explain below, a POSITA would not consider Gomez to be analogous art to the '362 Patent.

i. Field of Endeavor

36. As I have described above, the '362 Patent is directed to a receiver device for use in cable television systems. The patent states that it "relates to wideband receiver systems that are capable of receiving multiple desired television channels that extend over multiple non-contiguous

portions of the broad frequency spectrum and grouping them into a contiguous, or substantially-contiguous, frequency spectrum." *See* '362 Patent, 1:18–23; *see also* '362 Patent, Title. The patent also describes how the input RF signal to the receiver "may include the VHF and UHF television channels in a terrestrial television broadcasting system or the CATV channels in cable networks," indicating use in cable television systems. *Id.* at 1:52–55.

37. In contrast, Gomez's field of endeavor is channel switching in a *satellite* television system. In my opinion, a POSITA would not consider satellite systems to be part of the same field of endeavor as cable systems. Although both are forms of RF communication, there are important differences between the problems and solutions that arise in both fields, as well as in the ways persons skilled in the art seek to optimize these systems. A few of these operational and distinguishing differences are:

- Signal orientation;
- Ionizing radiation;
- IC / circuit board packaging;
- Power / cooling;
- Component costs;
- Signal strength / signal to noise ratio; and
- Frequency slots containing the TV channels.

38. **Signal strength / signal to noise ratio.** Satellite signals are subject to signal fade and high signal loss, as well as environmental factors such as rain, all of which contribute to a lower signal amplitude arriving at the satellite antenna. *See* Appendix 2, Intelsat Presentation, slides 36–37 (showing expected signal degradation due to rain, *e.g.*, for a signal directed toward Brazil). As such, the signal-to-noise ratio (SNR) is much lower, and design techniques are needed

for increasing the signal strength. One distinguishing point between satellite and CATV signals is that satellite accomplishes this by keeping the processing bands as narrow as possible.

39. A POSITA wanting to use Gomez's system would be aware of this problem with low signal amplitude and would further be cognizant of the International Telecommunications Union (ITU) technical recommendation, "*Propagation data and prediction methods required for the design of Earth-Space Telecommunications Systems*" (ITU-R P.618-8). *See* Appendix 3. As taught therein, a POSITA would understand the issue of signal fading from weather[1] and would design the system to use directional transponder antennas optimized to have the receive signal increased, as well as different antennas for each of the frequency bands.

40. The above issue of variable signal strength and reduced SNR is something not present in a CATV/HFC system. In contrast, a cable system like that of the '362 Patent can directly process a several hundred MHz baseband signal with a high SNR.

41. **Radiation.** It is well understood by a POSITA that the selection of integrated circuit (IC) technology for space-based satellites that are subject to high levels of radiation is different than CATV/HFC[2] integrated circuit technology. ICs for terrestrial-based applications are often fabricated using denser, cheaper, lower power technology and are packaged in circuit carriers that do not need to be shock and vibration resistant.

42. Addressing this serious issue, NASA has provided the following information for ICs destined for space applications such as satellites. On the topic of just a single event effect (SEE) of an ionizing particle causing complete failure of the circuit, the guidance states:

[1] The signal degradation a POSITA would expect due to rain in both sending and receiving a signal intended for a system in Brazil is 50 dB (see Appendix 2, slides 36-37).
[2] HFC refers to the hybrid fiber-coaxial network used to deliver cable television to the subscriber's home.

> SEEs can also cause errors that permanently damage the transistor. ASICs are sensitive to single-event latchups, snapbacks, and burnouts (although burnouts have not yet been observed in space). Latchups occur when a p-n-p-n or n-p-n-p CMOS transistor is traversed by a high-LET particle. If enough charge is injected into the base of the parasitic bipolars, the normally high- impedance state can become low, thereby turning the cell on permanently. Similarly, a snapback permanently turns a cell on, but without the p-n-p-n structure. For a snapback, charge collection in the p-well surrounding n-channel transistors produces a drain avalanche current and the source-to-drain voltage sustains this current. A single-event burnout (SEB) can occur when a heavy ion traverses a high voltage junction, creating a low resistance path between the gate and the substrate. This burns the cell and renders it inoperative.
>
> Appendix 4, *Space Radiation Effects on Integrated Circuits*.

43. **Frequency slots containing the TV channels.** Satellites use transponders with limited frequency range. One reason for this is the ability to reuse the same carrier frequency multiple times, *i.e.* by having different geographic areas covered by different transponders. Another reason is that by using a reduced frequency range, the SNR can be increased. A third reason is that by international treaty, other countries are also entitled to use satellites for their own domestic purposes so no one satellite (or country) is allowed to hog the entire range. Geosynchronous orbital slots and their assigned frequencies are a limited resource that countries must share.

44. With this limitation on transponder frequency range, satellites that relay a large number of TV channels must use multiple transponders. For example, the ARSAT-1 satellite transmits Ku band signals using twelve 36 MHz transponders, eight 54 MHz transponders and four 72 MHz transponders.

45. Segmenting these frequencies in small chunks in various places in the Ku band is not a restriction for CATV/HFC. There is no need for frequency segmentation in this environment. There is also no carrier frequency that needs to be down-converted because the cable RF signal is

already at baseband. In satellites, such is not the case. For example, the Ku band operates at 14 GHz and must be down-converted before any significant processing can be done.

46. The FCC is responsible for allocating spectrum for the U.S. They assign various wireless services to specific frequency ranges. *See* Appendix 5, FCC Allocation Chart. Because wireless spectrum is such a scarce and valuable resource, most TV relay frequencies have the same attribute of narrow frequency ranges such as airborne relays, terrestrial fixed station, or maritime applications. Having a dedicated isolated transmission medium such as fiber and/or coaxial cable avoids the issue of having to segment slots of small frequency ranges.

47. The chart below summarizes the technological differences between satellite and CATV/HFC systems that I have described above.

Technology	Satellite	CATV/HFC
Signal Orientation	Signal can be polarized, *e.g.*, horizontal, vertical, circular, linear[3]	Signal polarization does not exist for signals transported over HFC
Radiation	ICs must use radiation hardened technology, which is normally more expensive	CATV will often use common technology such as CMOS which is normally cheaper, denser, and consumes less power than other technologies
IC / Circuit Board Packaging	Must be designed with vibration & shock considerations in mind, further increasing expense	Uses standard ICs and circuit board technology
Power / Cooling	Satellite technology is solar powered and very expensive. Cooling of components is also difficult and expensive	Power and cooling are not significant design considerations.
Component Costs	More important to optimize factors such as power consumption, cooling, and radiation-hardening rather than component cost	Component costs are more important than power & cooling, and there is virtually no concern about ionizing radiation
Signal Strength / SNR	Satellite signals are usually weak compared to cable-delivered signals. They are also subject to environmental factors such as rain, sunspots, and troposphere changes. Therefore, frequency ranges must be kept narrow, and more costly low-noise circuits must be used	The signal from the CATV headend is usually very strong, very stable, and has extremely high SNR, allowing for very high data rate (*e.g.*, QAM 256 with 8 bits/Hz vs. QPSK with 1.5 bits/Hz)
Frequency Slots Containing the TV Channels	Satellite transponders are governed by FCC rules that assign	A CATV signal is not segmented and operates at baseband, reducing

[3] *See* Appendix 2, Intelsat Presentation, slides 9–19.

	transponder frequency slots within the allocated carrier frequency band (*e.g.*, C – 6 GHz, Ku – 14 GHz, Ka – 27 GHz). In this environment, "wideband" is relatively small compared to CATV.	circuit complexity. The entire 806 MHz is available for processing.

48. Because of these fundamental differences between Gomez's satellite system and the '362 Patent's CATV/HFC system, a POSITA would not consider them related to the same field of endeavor. Rather, a POSITA would distinguish between satellite and cable systems because of the different problems that emerge and the different ways that these technologies are optimized.

ii. Reasonably Pertinent to the Problem Addressed by the '362 Patent

49. Gomez is also not reasonably pertinent to the problem addressed by the '362 Patent. As I explained above, the '362 Patent is directed to an improved architecture for a wideband cable receiver. The specific problem sought to be addressed by the '362 Patent is one that arises in the cable environment, where the wide bandwidth of the incoming RF signal necessitates higher performance and complex digital processing circuitry. *See* '362 Patent, 2:20–23. This means that a *wideband* cable receiver must include analog-to-digital converters and other circuitry capable of processing hundreds of megahertz of bandwidth, while also—as I discussed above—remaining cost-effective through the use of non-radiation hardened technologies such as CMOS and standard IC packaging. Circuitry of this kind is absent from satellite systems.

50. Gomez is directed to satellite systems that do not include wideband analog-to-digital converters capable of processing hundreds of megahertz of consecutive bandwidth concurrently to extract hundreds of TV channels in parallel. A POSITA would understand that satellite communications are divided between various bands (*e.g.*, C band, Ku band, Ka band). Their antennas likely have different polarization for the same frequency and have antennas directed at to various geographic locations. *See* Gomez, 5:24–27 (describing two separate bands of 950–1450 MHz and 1650–2150). Moreover, a POSITA would understand that the satellite signals in

each band are further divided among multiple transponders, each of which carries a limited number of TV channels in its 36–72 MHz bandwidth. This contrasts with the '362 Patent, where the input is a single RF signal having a continuous bandwidth of over 800 MHz. *See* '362 Patent, 2:14–23.

51. To support the aggregating of multiple transponders, Gomez teaches that a device like an FTM is used to "selectively switch" between the signals received from each transponder. *See* Gomez, 1:38–41. A POSITA would understand this to mean that Gomez avoids the use of wideband analog-to-digital conversion techniques like those employed by the '362 Patent and instead uses many mixers, A/D converters, and filters to process the signals from the multiple transponders.[4] Gomez's solution of switching between multiple bands and switching between multiple transponders is not something a POSITA would contemplate implementing into a cable receiver.

52. As another matter, Gomez's earth-based FTM is designed at most to select a single channel of interest from the multiple input TV channels of a transponder, as mentioned in my summary of Gomez above. This is a far easier design task than selecting hundreds of channels of interest as disclosed with the '362 Patent. Assuming a standard TV channel is 6 MHz, the one desired channel can be processed with a simply designed A/D converter, D/A converter, and up-converter. Dealing with hundreds of these channels concurrently requires much wider bandwidth circuitry and ensuring the signals are flat across the entire RF range (55 MHz → 860 MHz).

53. Because Gomez is not reasonably pertinent to the problem of improving efficiency of a cable receiver, is not related to the '362 Patent's field of cable receivers, and does not provide

[4] Figures 5 and 6 of Gomez depict an analog signal converter (block 501) which includes two signal converters (blocks 610 and 611). A POSITA would understand that the actual circuitry represented by these blocks is more complicated and necessarily includes many more mixers, A/D converters, and filters than are shown.

multiple desired TV channels from a single frequency range, it is my opinion that a POSITA would not consider Gomez analogous art.

e. A POSITA Would Not be Motivated to Combine Gomez and Pugel as Suggested by the Examiner

54. I understand the Examiner has alleged that Pugel discloses downconverting, but not necessarily by a mixer module. *See* OA, p. 4. I further understand the Examiner has alleged it would be obvious to modify Pugel to "utilize Gomez's teaching about employing a mixer to perform down-conversion in order to efficiently process[] inputted signals." *Id.* at 5. In my opinion, a POSITA would not be motivated to modify Pugel as the Examiner has suggested.

55. I first note that Gomez and Pugel are from different fields of endeavor. Like the '362 Patent, Pugel is directed to "a single digital receiver circuit suitable for use with conventional ***cable*** delivery systems." Pugel, Abstract (emphasis added). For the same reasons I discussed above, a POSITA would not look to modify Pugel's *cable* receiver in view of Gomez's teachings about channel switching in a *satellite* FTM.

56. The second problem with the Examiner's suggestion has to do with the fact that Pugel—like the '362 Patent—relates to a *wideband* cable receiver. Specifically, Pugel discloses that the analog input signal is segregated into three bands of 5–300 MHz, 300–600 MHz, and 600–900 MHz. *See id.* at [0028]. Each of these bands is digitized in its entirety by an analog-to-digital converter (*id.* at [0024]) and then downconverted. *See id.* at Claim 18. Thus, Pugel's downconverters are configured to downconvert a bandwidth of at least 300 MHz.

57. The third problem is that Gomez's system is for outputting a single desired TV channel in a frequency range. A POSITA would therefore not incorporate Gomez's teachings into a system for providing multiple desired output TV channels concurrently in a cable/HFC frequency range.

58. Moreover, the mixer of Gomez and the mixer of '362 are functionally quite different and a POSITA in designing them could not use them interchangeably because of technical differences. Some of these differences are explained below.

59. Gomez's mixer inputs a transponder's signal that contains only a few TV channels in its 36–72 MHz allotted bandwidth. The mixer of Gomez then outputs only a single TV channel from that transponder. Gomez does have an alternate embodiment that can provide multiple, concurrent TV channels but it requires additional mixers. If another channel is desired, it cannot be on the same transponder but could be on other transponders. Gomez uses these multiple mixers to provide multiple channels which then requires a combiner(s) to aggregate the desired channels.

60. A mixer requires a very controlled signal amplitude input to work effectively; too high and the mixer distorts, too low and the output has a poor Signal-to-Noise Ratio. The mixer usually provides a feedback signal to the RF pre-processing so that it can optimizes the mixer output signal. Gomez's control signal needs to monitor that one selected output TV channel and base the feedback RF Automatic Gain Control to the RF pre-processing to get the optimal result. It does not need to consider non-selected channels.

61. Conversely, the '362 Patent uses a single mixer to provide multiple desired TV channels. The '362 Patent's mixer monitors all the channels in the output frequency band, selected and non-selected channels. The optimal result that is needed to control the RF Automatic Gain Control might be best on a non-selected TV channel to keep the mixer from overloading and distorting the selected TV channels.

62. A POSITA knows it is much more difficult to design a mixer that spans hundreds of MHz vs one that is designed for a single TV channel. An example of this complexity involves obtaining consistent amplitude of the signal across the output (flatness) and not altering the tilt

(Phase shift). A design of a single channel mixer cannot be used for the design of multi-channel system such as in these two operational environments.

63. The complexity differences obtaining the desired output signal (the in-band signal) in these two operational environments is also present in dealing with the issues of handling the out-of-band signals that inherently occur in a mixer. Technically, a mixer mixes the frequency of the carrier signal (F_C) with the frequency of an appropriate oscillator (F_O) to produce two signals. One signal is the addition of the two frequencies and the other is the difference of these frequencies. In most cases, only one of these signals is needed and the other must be filtered out.

64. Gomez's mixer has the very easy task of designing a fixed filter since the one TV channel can be selected from a range of frequencies in the transponder by simply changing the oscillator frequency F_O. This is often done using a voltage-controlled oscillator with the voltage controlled by its intelligent control system.

65. Because of the very wide range of the output band in the '362 Patent, the sum and difference signals are most likely both in the output band so different techniques must be used to filter out only the desired information. The harmonics of these sum and difference signals also offer significant design challenges to keep them from interfering in the desired frequency range.

66. In my opinion, the different requirements placed upon the mixer in pre-processing, post-processing, and functionality would make a POSITA not look to the mixers of Gomez in the manner the office action suggests, and such a POSITA would not have used such a mixer in the proposed combination to render obvious the claimed subject matter of the '362 Patent. Moreover, attempting to create the '362 Patent's mixer using a Gomez mixer would lead to a non-functional system for at least the reasons above.

67. A POSITA would understand that Gomez's FTM switches between satellite transponders with separate, relatively narrow frequency ranges. Accordingly, a POSITA would recognize that Gomez relies on multiple mixers, A/D converters, and filters arranged to process the signals from each transponder.

68. Because of this difference, a POSITA would appreciate that Gomez's analog mixers are not suitable for use in Pugel's wideband cable receiver. Gomez's mixers are not compatible with and would not work in the Pugel system and would not have led a POSITA to the system of the '362 Patent.

69. Gomez's circuitry simply lacks the complexity needed to process the wide bandwidths and multiple channels that are present in a cable system. Therefore, a POSITA would not be motivated to look to Gomez in order to modify the system of Pugel.

VI. CONCLUSION

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: 9/24/2024

By: Signed by: Frank Koperda 60DD1E329EE54EE...

Frank Koperda

Appendix 1

Detailed Curriculum Vitae of Frank Koperda

Expertise

- Data Communications Protocols (TCP/IP, Wi-Fi, DOCSIS, ADSL, PON)
- Hardware Design (ICs, circuits, RF, Systems)
- Standards Development (IEEE, ETSI, ITU)
- Networking hardware (Switches, Routers, Telco, CableTV)
- Software (14 Programming Languages, System Design, Code Analysis)
- Big Data (Natural Language Processing-NLP, machine learning, untagged data)
- Intellectual Property (patenting useful technology, patent litigation, patent office IPRs/PGRs)

Professional Summary

My technical expertise is in computer systems and data communications. The breadth of this expertise includes hardware design, software development, communications protocols, and "big data". As identified below, I have depth in each of these areas and this unique combination allows valuable insight into creating cutting edge products, helping companies solve difficult problems, and help in patent litigation issues.

Development experience includes hardware design of integrated circuits, circuit boards, and complex systems. I program in a number of computer languages and have applied this to operating systems, device control, data networking, and natural language processing. During my career, there are over 60 patents/applications in which I am a named inventor.

Current research and development is related to "big data" processing systems that enable the computer to automatically learn all technical areas using untagged data and natural language. This work involves sophisticated algorithms that automatically identify important information, can find related material, and can provide automatic grouping of related documents given examples of document in various such classifications.

Consulting services also include various aspects relating to Intellectual Property. I assist companies in identifying core technologies that should be protected, performing patent searches, testifying in Federal District courts for patent infringement cases, and providing opinions before the US Patent office relating to IPRs and PGRs.

Practice Areas

- Communications: ADSL, VoIP, Cable modems, Telephony, Wireless (e.g. Wi-Fi, IEEE 802.11, cell phone), Fiber Protocols
- Engineering: VLSI, digital, analog, RF, system, and card design
- Software: Communications, DSP, embedded systems, operating systems, compilers, NLP algorithms, proficiency in many languages (e.g. C#, C++, JAVA)
- Standards/Forums: CableLabs, ADSL Forum, FSAN, IEEE 802.11, ANSI X3T9, T1A1, WINForum
- Expert Witness: Patent analysis, claim charts, tutorials (including Markman hearings), trial testimony, IPRs, PGRs, and identification of technology in commercial products

Data Communications Experience

- Wireless data communications including LANs and working with FCC to get the PCS spectrum
- ADSL Deployment in Digital Loop Carrier Systems
- Fiber communications including passive optical networks (PONs) such as APON, GPON, EPON, G.983, G.984, G.987, and the Fibre Channel Standard
- Developed products, systems and protocols to support data and telephony over the CableTV plant (e.g. DOCSIS, PacketCable, CableHome)
- Communication Protocols VoIP, SIP, TCP/IP, ATM, Frame Relay, X.25, Fibre Channel, FDDI, HIPPI, LANs
- Standards Participation in IEEE 802.11 (Wireless), IEEE 802.14 (Cable modem), ANSI X3T9.3 (Fibre Channel), FSAN (fiber system definition by 10 Telcos), ADSL Forum, UAWG

Software Experience

- System design: function partitioning, code sizing, testing, problem determination
- Systems programming: operating system design, device drivers, compilers, communications
- Device control: disk controllers, DSP, printers, data acquisition, speech recognition

Hardware Experience

- System design: function partitioning, fault tolerance, cooling, power systems, safety, servicing
- Product design: 2 Gb/s communications router / switch, workstations, printers
- Digital: VLSI design and simulation, card design and manufacture
- Analog: Transducers, interfaces, preamplifiers, power amplifiers
- RF design (holder of First Class Radiotelephone and Technician Class Amateur licenses)

Employment History

From: 1999 **NextGen Datacom, Inc.**
To: Present
Position: *Owner*
Working with a variety of customers on creating new datacom products, helping investors evaluate opportunities, and patent protection for products. The product development has included, Home Networking (CableHome), Wireless (IEEE 802.11), Voice over IP (VoIP) transport products, ADSL, and big data.

From: 2010 **DocuNOWledge, LLC**
To: 2014
Position: *CTO / Co-owner*
The company provided the marketing and licensing of the document search/classification. This patented technology developed by NextGen Datacom implemented "big data" searching of USPTO Utility patents, patent applications, European patents, and publicly

available Defense Department documents (DTIC). Experiments were conducted showing the algorithms worked effectively on documents written in other human languages (e.g. French, German, Spanish).

From: 1998 **Hayes Microcomputer Products**
To: 1999
Position: *Director of Research and Systems Engineering*
Responsible for defining future products, determining the key technologies required for the future and establishing relationships with other companies. This group was also responsible for determining standards participation, reviewing Intellectual Property issues and ensuring common, interoperable features across all product lines including ADSL, Remote Access servers, and Home LANs.

From: 1996 **BellSouth Telecommunications**
To: 1998
Position: *Distinguished Member of Technical Staff -Exploratory Development*
I helped develop the Passive Optical Network (PON) fiber delivery systems within FSAN (15 international telcos), a hybrid fiber-wireless system, and network computing. Part of the job involved understanding how the technologies are likely to evolve, new business opportunities enabled by the technologies and which ones will become cost effective for this environment.

From: 1994 **Scientific-Atlanta Inc.**
To: 1996
Position: *Chief Architect for Data Communications*
Lead System Architect for Data over CATV. Worked with customers to develop product and system requirements. Developed new data protocols, did performance analysis, scheduling, cost estimating, staffing, and the IEEE 802.14 standards. Was awarded several US patents for the data-over-cable architecture.

From: 1977 **IBM**
To: 1994
Position:
- (1990-1994) *Communications Architecture*:
  Modified Fibre Channel Standard (ANSI X3T9.3) to allow multimedia packets using Q.2931
  Modified MPEG-2 DSMCC protocol to allow more flexibility
  Designed wireless protocols and worked with IEEE, created industry association, lobbied FCC
  Writing LAN Access Agent for BBNS (ATM network)
- (1989-1990) *Communications Concentrator*:

Hardware project lead of 2 Gb/s fast packet switch
Switch had SONET, T1, T3, HiPPI, RVX, LAN, FDDI, X.25 links
Received patents for design to multicast packets through network

- (1986-1989) *3471 / 3476 Terminal*:
  VLSI design of integrated micro, CRT ctlr, keyboard cntrl, 1.5 mb/s com link
  Programming to recognize brain waves for control of CRT cursor
  Programming to recognize facial muscle movement for control of PC
- (1984-1986) *3472/Infowindow*: (first IBM multimedia terminal)
  Design of PC card to attach to phone line, record & playback speech, speech recognition
  Programming of speech recognition (parameter extraction, word boundary, template matching)
  Application programming
- (1983-1984) *Integrated Telephone/Terminal*:
  Project lead and programming of SNA type 2 terminal emulation
  Communications programming of SDLC and BISYNC
  Application programming
- (1982-1983) *PBX Advanced Call Processing*: (first IBM PBX)
  Software design of advanced call processing using Series/1 attached to PBX
  Project lead and programming of custom operating system for PC attaching to PBX
- (1980-1982) *4975 Printer*: (first IBM desktop printers)
  Card design of microprocessor based printer including power drivers for printhead and motors
  Programming of motor control, printhead control and BISYNC communications using 8085
  Design of new technique for determining printhead position using magnetic delays
- (1979-1980) *System/23*: (first IBM desktop computer)
  Hardware design and programming of floppy disk subsystem
  Standardization within IBM of diskette information formats
  Concept and design of first IBM PC (68000 based)
- (1977-1979) *Series/1*: (first IBM minicomputer)
  Hardware design and programming of I/O card for hard disk drive
  Hardware design and programming for magnetic bubble and CCD storage
  Operating System programming

Education

Year	College/University	Degree
1976	Case-Western Reserve University, Cleveland, OH	MS, Computer Engineering
1974	State University of New York, Plattsburgh, NY	BA, Physics & BA, Chemistry

Patents / Patent Filings

Patent Number	Date Issued	Title
U.S. 8,838,614	September 2014	Method And System For Document Classification Or Search Using Discrete Words
U.S. 8,316,030	November 2012	Method And System For Document Classification Or Search Using Discrete Words
PCT/US2011/050037	August 2011	Method And System For Document Classification Or Search Using Discrete Words
U.S. 6,983,327	July 2006	System and Method for providing Statistics for Flexible Billing in a Cable Environment
U.S. 7,028,088	April 2006	System and Method for providing Statistics for Flexible Billing in a Cable Environment
US Patent filing	July 2004	Enhanced Apparatus for an Electronic Mascot Sound Simulator
Taiwan Patent TW589838	June 2004	Method And System For Simplifying Wiring In A Modular Communications Gateway
Taiwan Patent TW573411	January 2004	Method and Systems for A Modular Residential Gateway
World Patent WO 02085086	October 2002	Method and Systems for A Modular Residential Gateway
China Patent CN 1427613	July 2003	Method And System For Simplifying Wiring In A Modular Communications Gateway
Australia Patent 2002326800	March 2003	Method And System For Simplifying Wiring In A Modular Communications Gateway
World Patent WO 03021797	March 2003	Method And System For Simplifying Wiring In A Modular Communications Gateway
US Patent filing 20030021080	January 2003	Method And System For Simplifying Wiring In A Modular Communications Gateway
Germany DE69331310T	August 2002	Function Distribution in a Packet Switched Network
U.S. 6,467,091	October 2002	Constant Bit Rate Transport in a Contention based Medium Access Control
US Patent filing 20020065935	May 2002	Method and Systems for A Modular Residential Gateway
Austria AT210907T	December 2001	Function Distribution in a Packet Switched Network
U.S.6,230,203	May 2001	Method for providing Statistics for Flexible Billing in a Cable Environment

Patent Number	Date Issued	Title
US Patent filing	December 2000	Method for Providing Proper Addressing in the Presence of a Network Address Translator (NAT) When Using Security Protocols
US Patent filing 09/689,071	October 2000	An Independent Central Office Connected To Customers Via Packet Switched Transport Systems
US Patent filing 09/552,055	April 2000	An Independent Central Office Connected To The Public Switched Telephone Network Via Alternative MAN Transport Systems
Germany DE69325957T	March 2000	Methods and Apparatus for Routing Packets in Packet Transmission Networks
US Provisional Application	February 2000	Transmission of Modem Signals over a Universal Digital Loop Carrier System
US Patent filing 60/177,972	January 2000	Method to Provide Virtual Firewall Functionality from a Remote Service Provider
Spain 2136118T	November 1999	Methods and Apparatus for Routing Packets in Packet Transmission Networks
U.S.5,966,163	October 1999	Providing Constant Bit Rate Upstream Data Transport In A Two Way Cable System By Scheduling Preemptive Grants For Upstream Data Slots Using Selected Fields Of A Plurality Of Grant Fields
Austria 183349T	August 1999	Methods and Apparatus for Routing Packets in Packet Transmission Networks
US Provisional Application	May 1999	Digitizing the Transmission of a 56 kbit/s Modem Signals over a Universal Digital Loop Carrier System
US Provisional Application	June 1999	Method and Apparatus for Transmission of Digital Voice Band Modem Signals over a Universal Digital Loop Carrier System
Great Britain Patent GB2321373	July 1998	Constant Bit Rate Transport in a Contention based Medium Access Control
U.S. 5,790,806	August 1998	Cable Data Network Architecture
World Patent WO9737493	October 1997	Cable Data Network Architecture
Australia Patent 2219597	October 1997	Cable Data Network Architecture
World Patent WO9716895	May 1997	Constant Bit Rate Transport in a Contention based Medium Access Control
Australia Patent AU7464296	May 1997	Constant Bit Rate Transport in a Contention based Medium Access Control

Patent Number	Date Issued	Title
Japan JPH6216942 / JP2959659	1997	Function Distribution in a Packet Switched Network
Korea 9614986	1996	Methods and Apparatus for Routing Packets in Packet Transmission Networks
US. Provisional Application	October 1995	Priority Preempt Mechanism in a Mini-Slot Control Contention Based Medium Access Control
European Patent EP0598671	May 1995	Function Distribution in a Packet Switched Network
Canada CA2100539	May 1994	Function Distribution in a Packet Switched Network
Spain ES2168093T	May 1994	Function Distribution in a Packet Switched Network
Canada CN2094405	May 1994	Methods and Apparatus for Routing Packets in Packet Transmission Networks
China CN1032109	July 1994	Function Distribution in a Packet Switched Network
U.S. 5,309,433	May 1994	Methods and Apparatus for Routing Packets in Packet Transmission Networks
China CN1081056	January 1994	Methods and Apparatus for Routing Packets in Packet Transmission Networks
European Patent EP 0579567	January 1994	Methods and Apparatus for Routing Packets in Packet Transmission Networks
Australia AU3838993	December 1993	Methods and Apparatus for Routing Packets in Packet Transmission Networks
Japan JPH0662053 / JP2739023	1992	Methods and Apparatus for Routing Packets in Packet Transmission Networks
US Patent filing 19920978609	November 1992	Function Distribution in a Packet Switched Network
Germany DE3072189D	March 1991	Serial Storage Interface Apparatus for Coupling a Serial Storage Mechanism to a Data Processor Input/Output Bus
European Patent EP 0031031	July 1981	Serial Storage Interface Apparatus for Coupling a Serial Storage Mechanism to a Data Processor Input/Output Bus
Canada CA1163724	March 1984	Serial Storage Interface Apparatus for Coupling a Serial Storage Mechanism to a Data Processor Input/Output Bus

Patent Number	Date Issued	Title
U.S. 4,344,132	August 1982	Serial Storage Interface Apparatus for Coupling a Serial Storage Mechanism to a Data Processor Input/Output Bus
Japan JPS56087154	1981	Serial Storage Interface Apparatus for Coupling a Serial Storage Mechanism to a Data Processor Input/Output Bus
US Patent filing 60/159,032	October 1999	Method and Apparatus to Bypass a Local Exchange Carrier using an Independent Central Office having LAN Technology for providing Data and Telephony Services
US Patent filing 60/159,052	October 1999	Method and Apparatus to Bypass a Local Exchange Carrier Using Packet Transfer Technologies to Connect a Customer to the Public Switched Telephone Network
US Patent filing 60/159,061	October 1999	Method and Apparatus to Bypass a Local Exchange Carrier Using an Independent Central Office Having Wireless Transport to the Residence.
US Patent filing 60/159,591	October 1999	Method and Apparatus to Bypass a Local Exchange Carrier using an Independent Central Office having Customer Provisioned Services
US Patent filing 60/159,525	October 1999	An Independent Central Office which provides Local and Long Distance Calling Services to Existing Residential and Commercial Developments
US Patent filing 60/159,591	October 1999	Method and Apparatus for Installing and Monitoring Residential Water Utility Services
US Patent filing 60/159,593	October 1999	Method and Apparatus for Installing and Monitoring Residential Natural Gas Utility Services
US Provisional Application	October 1999	Method and Apparatus for Installing and Monitoring Residential Electricity Utility Services
US Provisional Application	October 1999	Method and Apparatus for installing and monitoring Residential Utility Services

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F.R. Koperda
Cable Modem: Old Protocols for a new Paradigm
National Cable Television Association Technical Papers, May 1996

F. Farhan, F.R. Koperda.
Challenges with Transmission of Data over CATV Networks
National Cable Television Association Technical Papers, May 1995

A.L. Bond, D.W. Davenport, F.R. Koperda.
Mechanism for Non-Disruptive Dynamic Testing of a Communications Network
IBM Technical Disclosure Bulletin, Vol 34 No 7A, pages 239-240 December 1991

F.R. Koperda, D.K. Popken
Automatic Compensation of Skin Conductance in Electromyographic Sensing
IBM Technical Disclosure Bulletin, Vol 34 No 4B, pages 124-126 September 1991

F.R. Koperda, ***Extraction of the Electric Fields of the Brain in a Noisy Environment***,
IBM Technical Disclosure Bulletin, V32: No 7. 1989.

R.A. Schulz, F.R. Koperda, ***Position Determination Using Pulse Delays***
IBM Technical Disclosure Bulletin, V27:2385, 1984.

F.R. Koperda, ***Ultrasonic Position Locator,***
IBM Technical Disclosure Bulletin, V27:1670, 1984.

F.R. Koperda
Voice Recognition
The McGraw-Hill Computer Handbook, pp 30.1 - 30.24, McGraw-Hill 1983.

F.R. Koperda
Position Detection in Printers
IBM Technical Disclosure Bulletin, V25:4673, 1983.

F.R. Koperda
Voice Recognition
Microprocessor Applications Handbook, pp 14.1, McGraw-Hill 1982.

J.D. Dixon, R.F. Farrel, F.R. Koperda, G.U. Merckel
Parity Mechanism for Detecting both Address and Data Errors
IBM Technical Disclosure Bulletin, V24:794, 1981.

F.R. Koperda
Bubble Memory Resynchronization Mechanism
IBM Technical Disclosure Bulletin, V22:450, 1979.

F.R. Koperda, F.I. Parke
Interactive Design of Visual Aids
Proceedings 1977 Annual Conference, Association for Computing Machinery, pp 434, 1977

Appendix 2

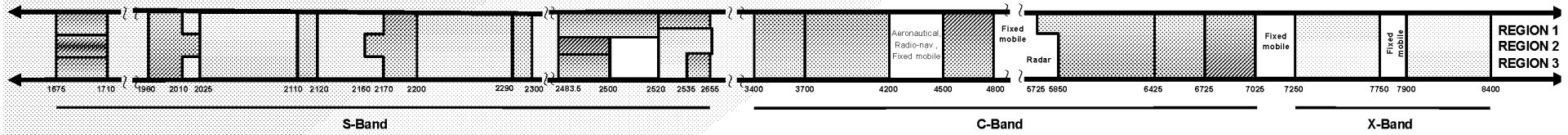
INTELSAT

satellite communications

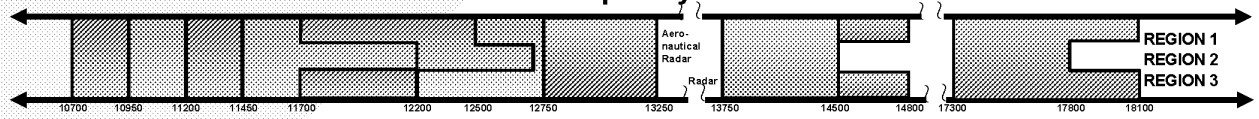
INTELSAT
ITU Satellite Frequency
Allocations

Satellite Frequency Allocations

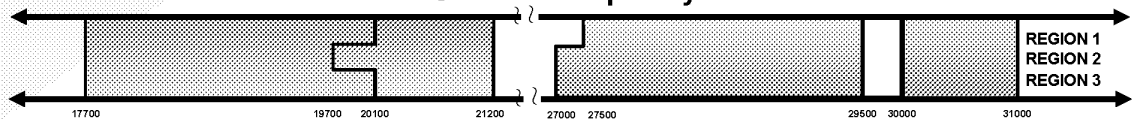
S-Band, C-Band and X-Band Satellite Frequency Allocations in MHz



Ku-Band Satellite Frequency Allocations in MHz



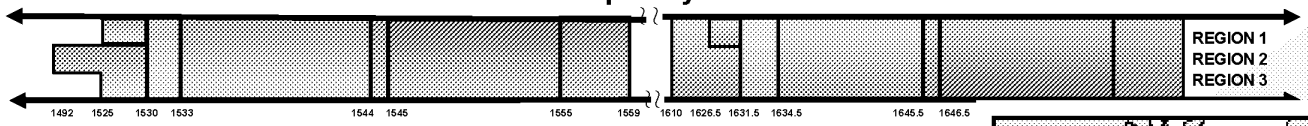
Ka-Band Satellite Frequency Allocations in MHz



Legend

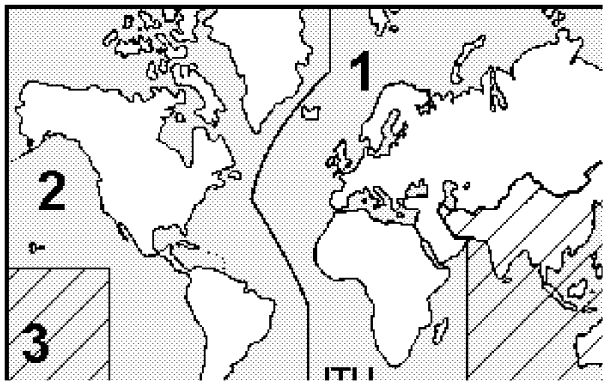
FSS Down	Extended FSS Down	FSS Allotment Plan Down	Government FSS Down	Space Operation/Earth Exploration/Space Research Down (Co-Primary)	Space Research Down
FSS Up	Extended FSS Up	FSS Allotment Plan Up	Government FSS Up	Space Operation/Earth Exploration/Space Research Up (Co-Primary)	Space Research Up
MSS Down	Meteorological Down	FSS/MSS Up (Co-Primary)	MSS/Radiodetermination Up (Co-Primary)	MSS/Government FSS Down (Co-Primary)	BSS Plan Down
MSS Up	Meteorological Down/ MSS Up (Co-Primary)	FSS/BSS Up (Co-Primary)		MSS/Government FSS Up (Co-Primary)	BSS Plan Up

L-Band Satellite Frequency Allocations in MHz



Legend

MSS Down	Maritime/Land Mobile Down (Co-Primary)	Emergency/Distress Down
MSS Up	Maritime/Land Mobile Up (Co-Primary)	Emergency/Distress Up
Maritime Mobile Down	Land Mobile Down	Aeronautical Mobile Down
Maritime Mobile Up	Land Mobile Up	Aeronautical Mobile Up



BSS = Broadcast Satellite Service FSS = Fixed Satellite Service MSS = Mobile Satellite Service

Frequency allocations

- C-Band
  - Transmit 5.925 - 6.425 GHz (U.S.)
    5.625 - 6.425 GHz (I.T.U.)
  - Receive 3.700 - 4.200 GHz (U.S.)
    3.400 - 4.200 GHz (I.T.U.)
- Ku-Band
  - Transmit 14.00 - 14.50 GHz (U.S.)
    13.75 - 14.50 GHz (I.T.U.)
  - Receive 11.70 - 12.20 GHz (U.S.)
    11.20 - 11.70 GHz (ITU)
- Ka-Band
  - Transmit 27.5 - 30.0 GHz
  - Receive 17.7 - 20.0 GHz

C-Band

- **Advantages**
  - Wide footprint coverage
  - Minor effects from rain
  - Lower cost for earth station antenna
- **Disadvantages**
  - Requires larger antennas
  - Requires larger RF power amplifier
  - Effected by terrestrial interference (TI)
  - Difficult to obtain transmit license
    - Frequency clearance

Ku-Band

- **Advantages**
  - Smaller antennas
  - Smaller RF power amplifiers
- **Disadvantages**
  - Greater effect from rain
  - Smaller footprint (beam) coverage

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Ka-Band

- **Advantages**
  - Smaller antennas
  - Smaller RF power amplifier

- **Disadvantages**
  - Greater effect from rain
  - Smaller footprint (beam) coverage
  - High equipment cost

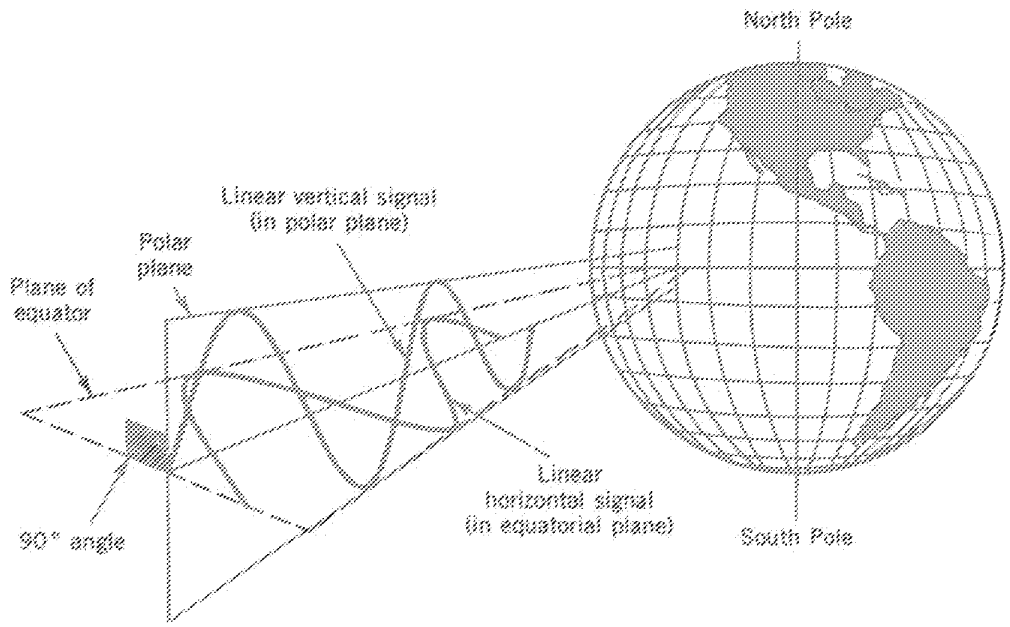
INTELSAT
Polarization

Polarization

- **Provides increased satellite capacity (Allows frequency reuse)**
- The directional aspects of the electrical field of a radio signal
- **Linear** *(90° Out of Phase)*
  - Horizontal (H)
  - Vertical (V)
  - All Ku-Band satellites are Linear
- **Circular** *(180° Out of Phase)*
  - Right Hand Circular (RHCP)
  - Left Hand Circular (LHCP)

Linear Polarization

- Linear Polarization
  - The electrical field is wholly in one plane containing the direction of propagation
- Horizontal
  - Field lies in a plane parallel to the earth's surface.
- Vertical
  - Field lies in a plane perpendicular to the earth's surface.

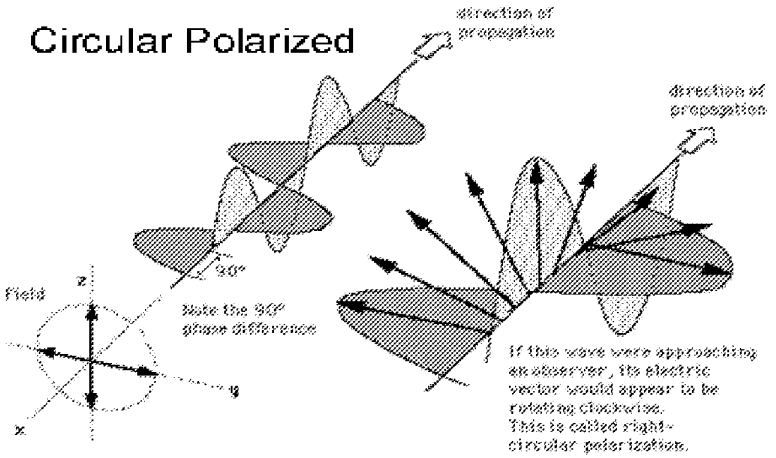


Notes:

1. In some satellites horizontal and vertical planes plane may be rotated with respect to earth's equator...

Circular Polarization

- Circular Polarization
  - The electrical field radiates energy in both the horizontal and vertical planes and all planes in between
- Right Hand Circular Polarization (RHCP)
  - the electric field is rotating clockwise as seen by an observer towards whom the wave is moving
- Left Hand Circular Polarization (LHCP)
  - the electric field is rotating counterclockwise as seen by an observer towards whom the wave is moving



Linear Polarization

- **Advantage**
  - Lower Cost Antenna System
    - Feed Assembly (OMT)
  - Better Cross-Pol Isolation

- **Disadvantage**
  - Polarization Adjustment Required
  - Polarization changes depending on Latitude and Longitude
  - Greater chance of problems due to cross-pol interference
  - Faraday rotation in the ionosphere

Circular Polarization

- **Advantage**
  - No polarization adjustment required
    - Fixed by Ortho-Mode-Transducer (OMT)
  - Less chance of cross-Pol interference

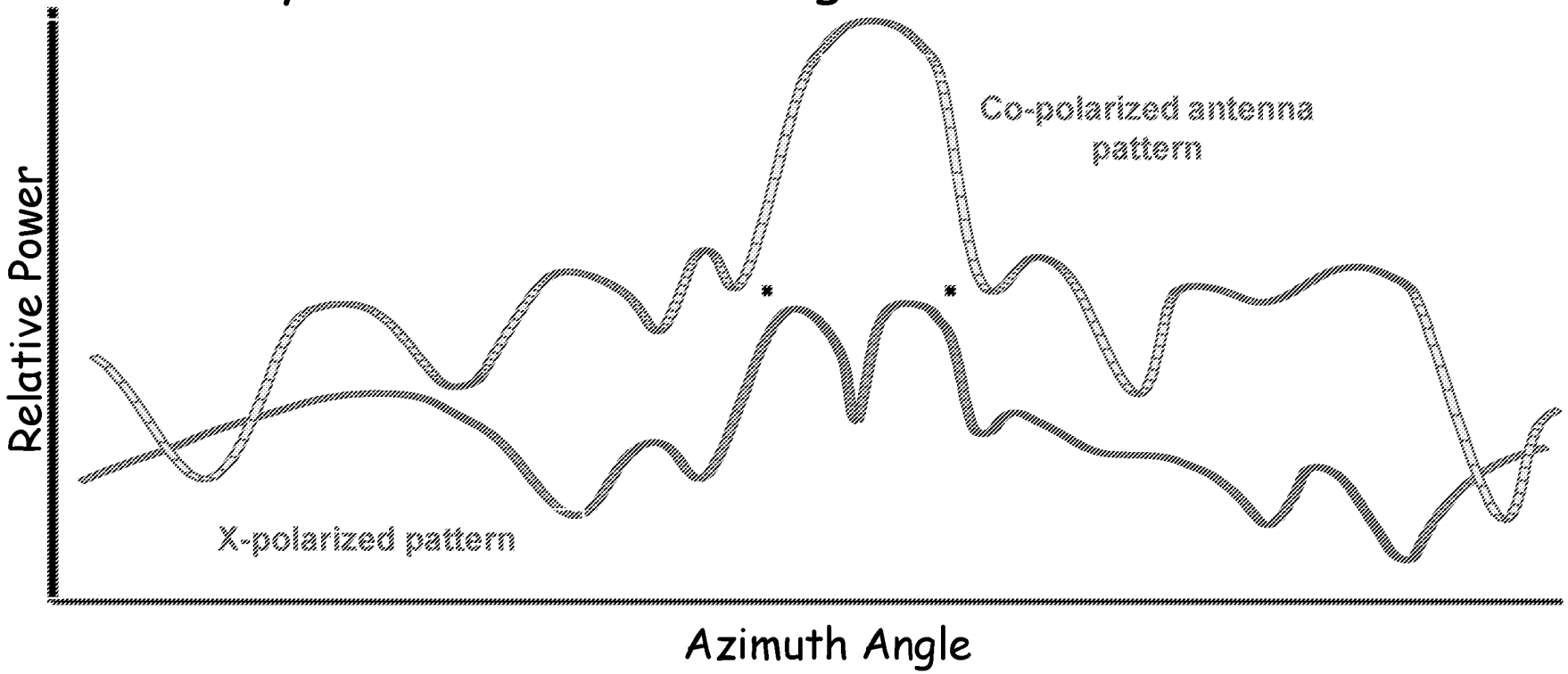
- **Disadvantage**
  - Higher cost antenna systems
    - Feed Assembly (OMT)
  - Slightly lower cross-Pol isolation

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Cross Polarization Isolation

Antenna Polarization

- Co-Polarization
  - Polarity of the desired signal
- Cross-Polarization
  - Polarity of the unwanted signal

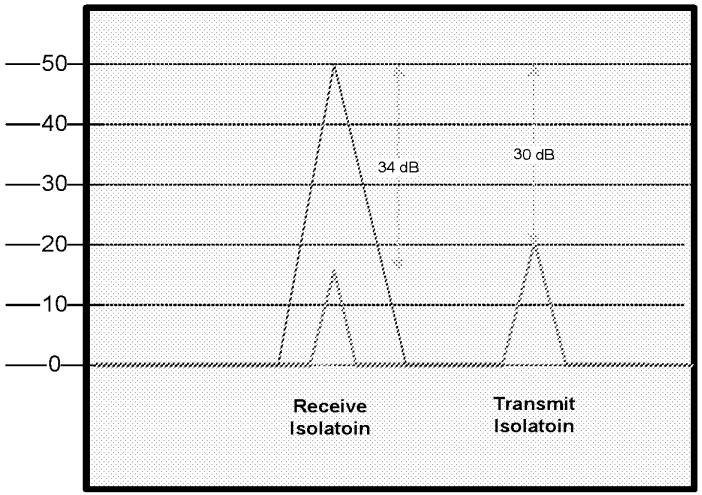


Antenna Cross Polarization

In addition to the *Main Carrier(V)* a *Cross-Pol Component (H)* is also transmitted from the Uplink Antenna

Both the *Main Carrier (V)* and the *Cross-Pol Component (H)* are received by the satellite

Both the *Main Carrier (H)* and the *Cross-Pol Component (V)* are transmitted from the satellite and received at the downlink Antenna.

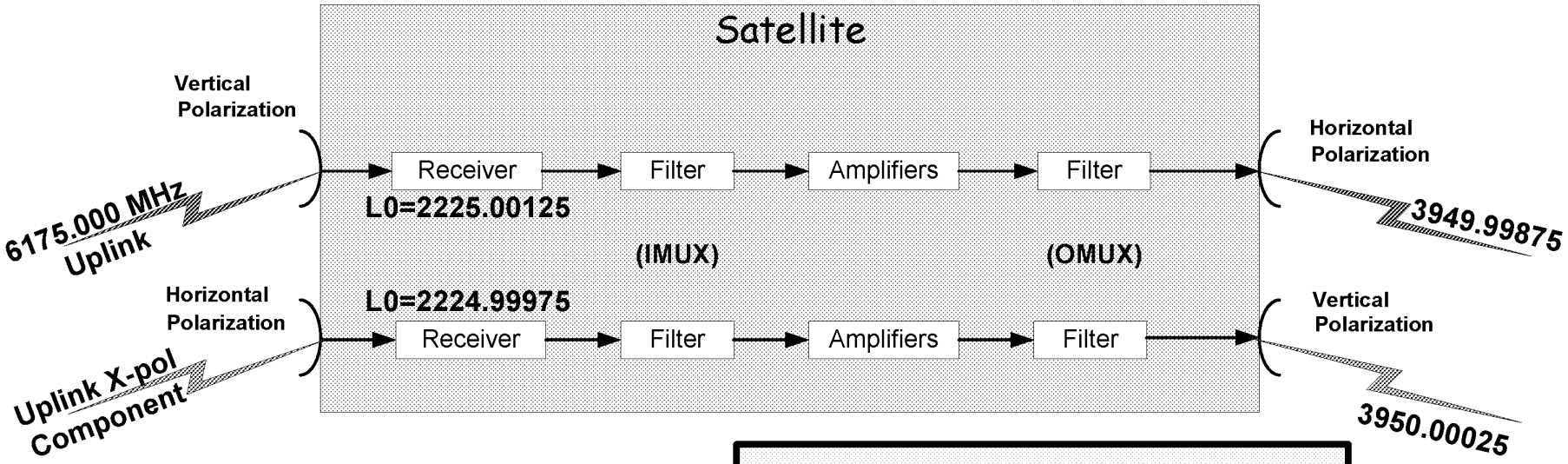


At the downlink station a second *Cross-Pol Component* is introduced.
Receive Antenna Isolation.

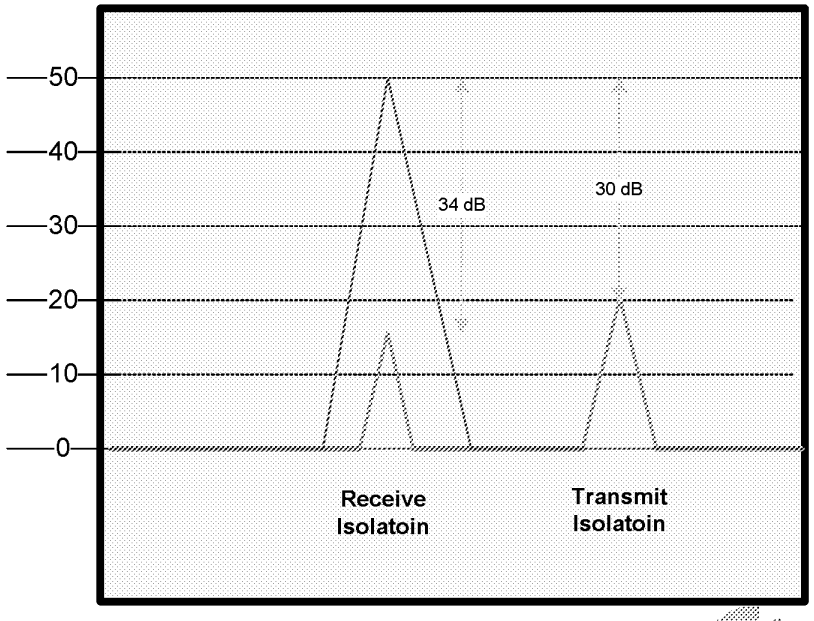
The Cross-Pol component that is at the same frequency as the main carrier is receive isolation

The Cross-Pol component that is offset from the main carrier is the transmit antenna isolation

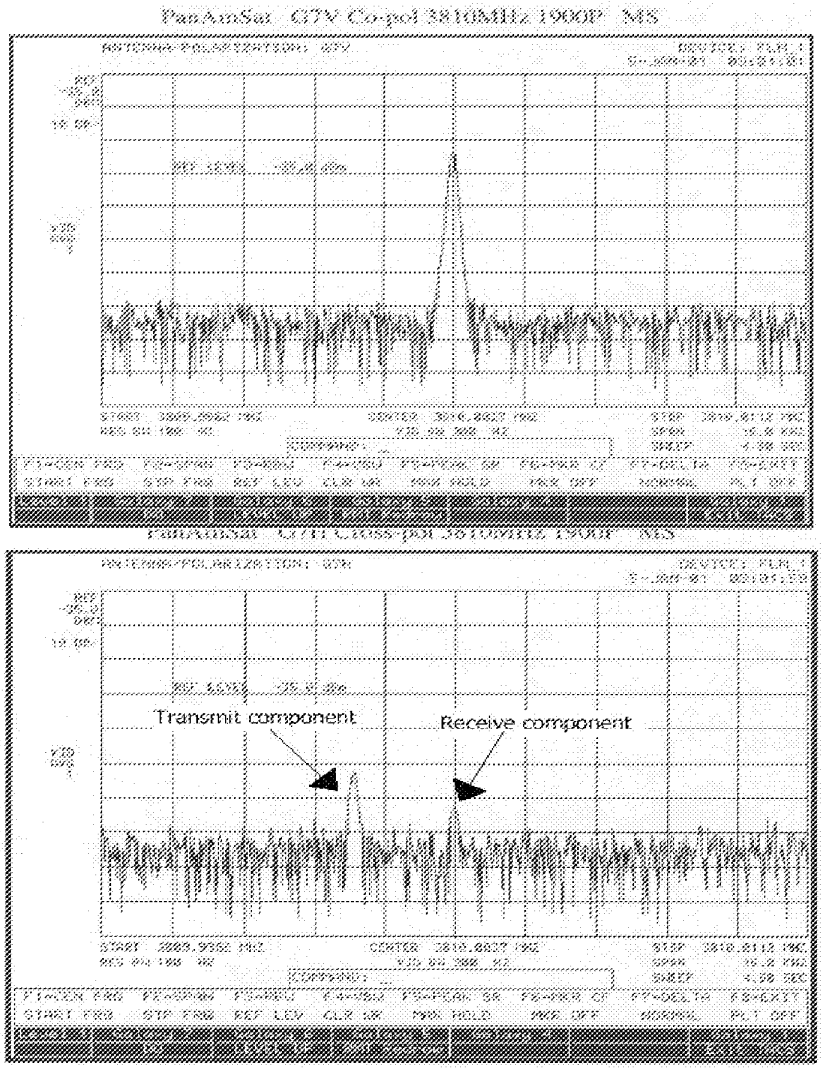
Antenna Cross Polarization



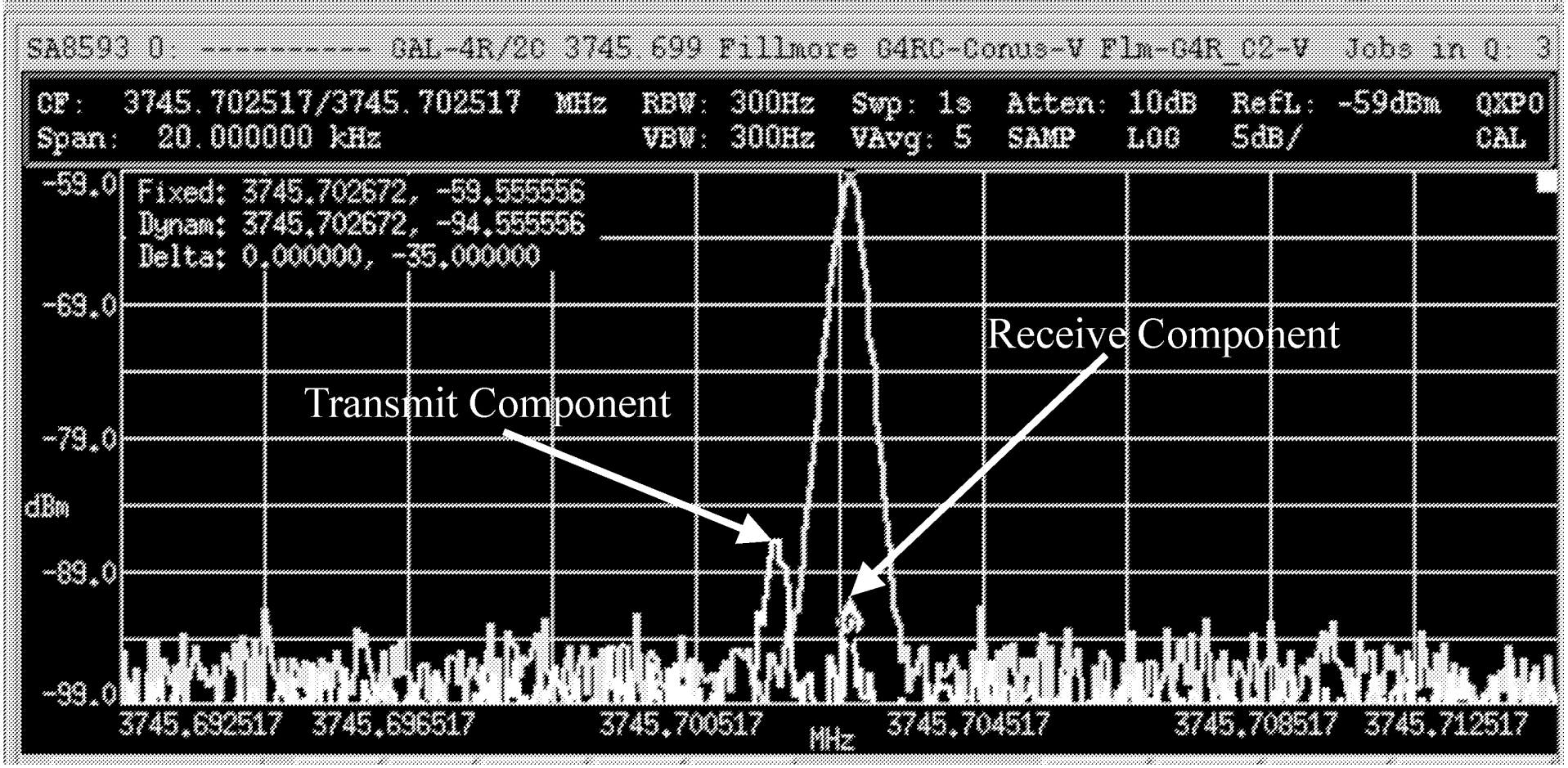
The satellite LO frequencies are not at the exact same frequency



Antenna Cross Polarization



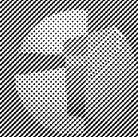
Antenna Cross Polarization



- Transmit Isolation ≈ 27.5 dB
- Receive Isolation ≈ 35.0 dB

IFL Uplink Link Budgets

CONFIDENTIAL INTELSAT PROPRIETARY



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IFL Downlink Link Budget

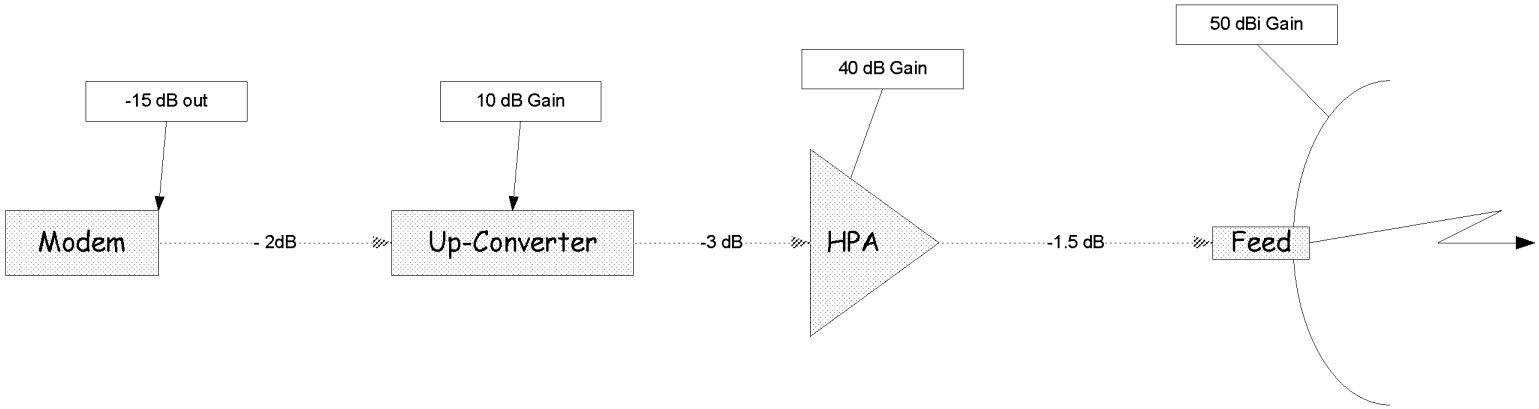
- Basic Link Budget
  - Illustrative purposes only

Mod output =	-15			dBm
IFL	-6.5	dB	-21.5	dBm
U/C gain =	10	dB	-11.5	dBm
HPA gain =	40	dB	28.5	dBm
TX antenna gain	50	dBi	78.5	dBm
Uplink space loss =	-199.4	dB	-120.9	dBm
Sat RX ant gain =	41	dBi	-79.9	dBm
Sat receiver gain =	60	dB	-19.9	dBm
Sat Losses =	-5.9	dB	-25.8	dBm
Sat amplifier gain	40	dB	14.2	dBm
Sat TX ant gain =	38	dBi	52.2	dBm
Downlink space loss=	-195.8	dB	-143.6	dBm
RX antenna gain =	47	dBi	-96.6	dBm
LNA gain =	60	dB	-36.6	dBm
IFL losses =	-14	dB	-50.6	dBm
D/C gain =	10	dB	-40.6	dBm
Demod Input =	-40.6			dBm

$C/N_u = EIRP_e + G/T_s - Lpu + K - 10log(BW)$		
Earth Station EIRP =	48.5	dBW
Sat G/T =	8.2	dB/K
Uplink loss =	199.4	dB
Boltzman =	228.6	dB
Bandwidth =	1265000	Hz
Uplink C/N =	**24.88**	dB

$C/N_d = EIRP_s + G/T_e - Lp_d - 10log(K) - 10log(BW)$		
Sat EIRP =	22.2	dBW
Earth Station G/T =	20.9	dBK
Path Loss =	195.8	dB
Carrier Bandwidth =	1265000	Hz
Boltzmans Constant =	228.6	
Downlink C/N =	14.9	dB

IFL Uplink Link Budget



EIRP = Modem out – IF cable loss + U/C gain – RF cable loss + HPA gain – W/G loss + Antenna gain

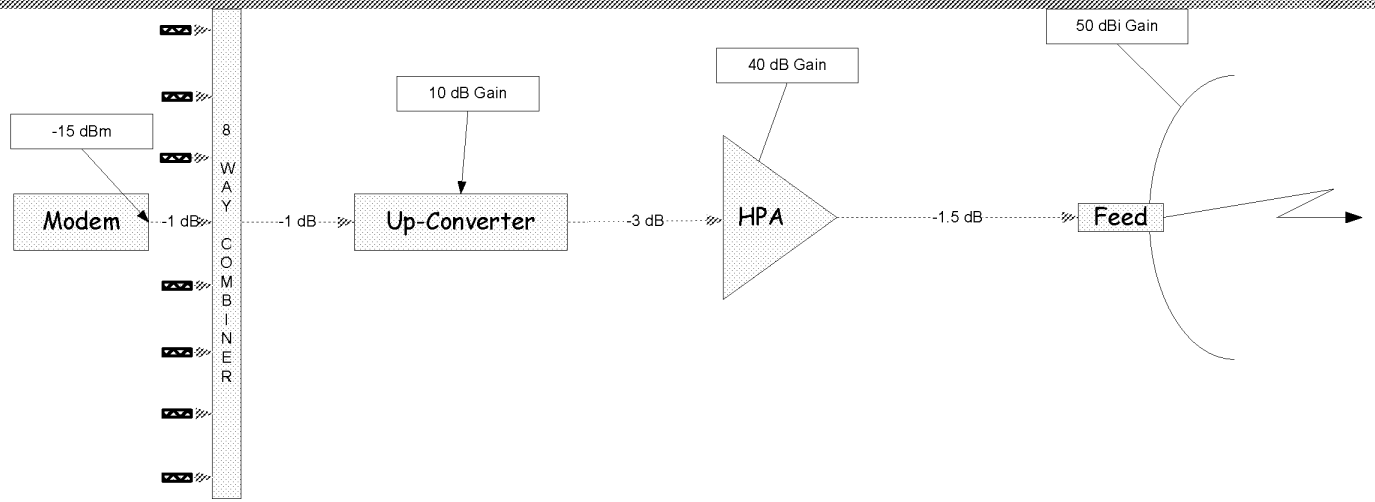
EIRP = -15 dBm –2 dB + 10 dB – 3 dB + 40 dB – 1.5dB + 50 dBi

EIRP = 78.5 dBm

EIRP = 48.5 dBW

	Gain/Loss	Unit
Modem Output =	-15.00	dBm
IF Cable Loss =	-2.00	dB
U/C Gain =	10.00	dB
RF Cable Loss =	-3.00	dB
HPA Gain =	40.00	dB
W/G Loss =	-1.50	dB
Antenna Gain =	50.00	dB
EIRP =	78.50	dBm
	48.50	**dBW**

IFL Uplink Link Budget



EIRP = Modem out – combiner loss– IF cable loss + U/C gain – RF cable loss + HPA gain – W/G loss + Antenna gain

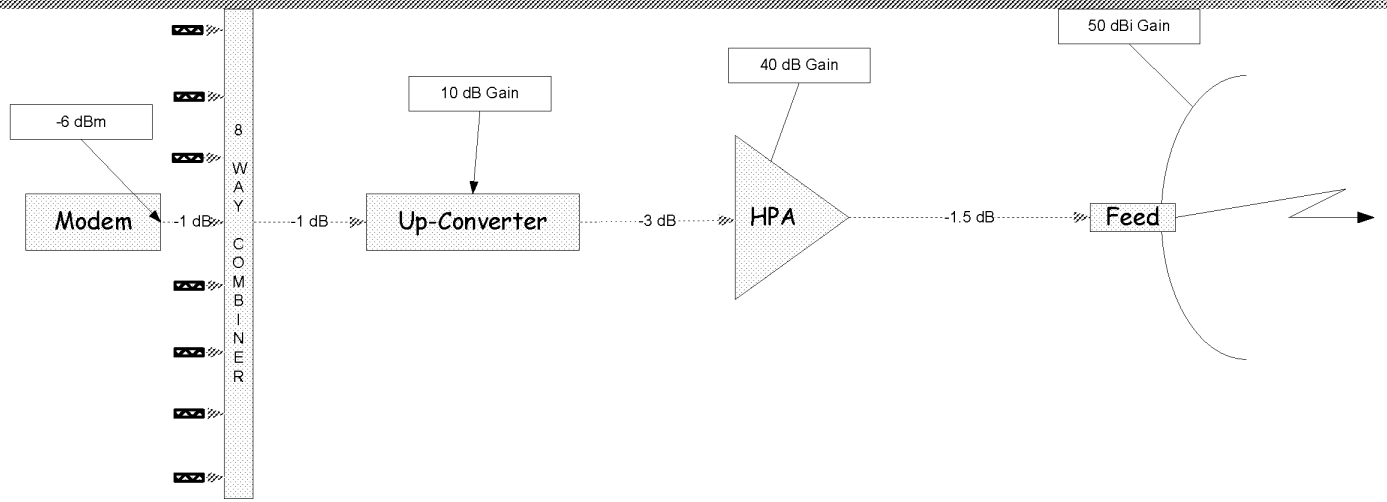
EIRP = -15 dBm – 9 - 2 dB + 10 dB – 3 dB + 40 dB – 1.5dB + 50 dBi

EIRP = 69.5 dBm

EIRP = 39.5 dBW

	Gain/Loss	Unit
Modem Output =	-15.00	dBm
Combiner Loss =	-9.00	dB
IF Cable Loss =	-2.00	dB
U/C Gain =	10.00	dB
RF Cable Loss =	-3.00	dB
HPA Gain =	40.00	dB
W/G Loss =	-1.50	dB
Antenna Gain =	50.00	dB
EIRP =	69.50	dBm
	39.50	**dBW**

IFL Uplink Link Budget



EIRP = Modem out – combiner loss– IF cable loss + U/C gain – RF cable loss + HPA gain – W/G loss + Antenna gain

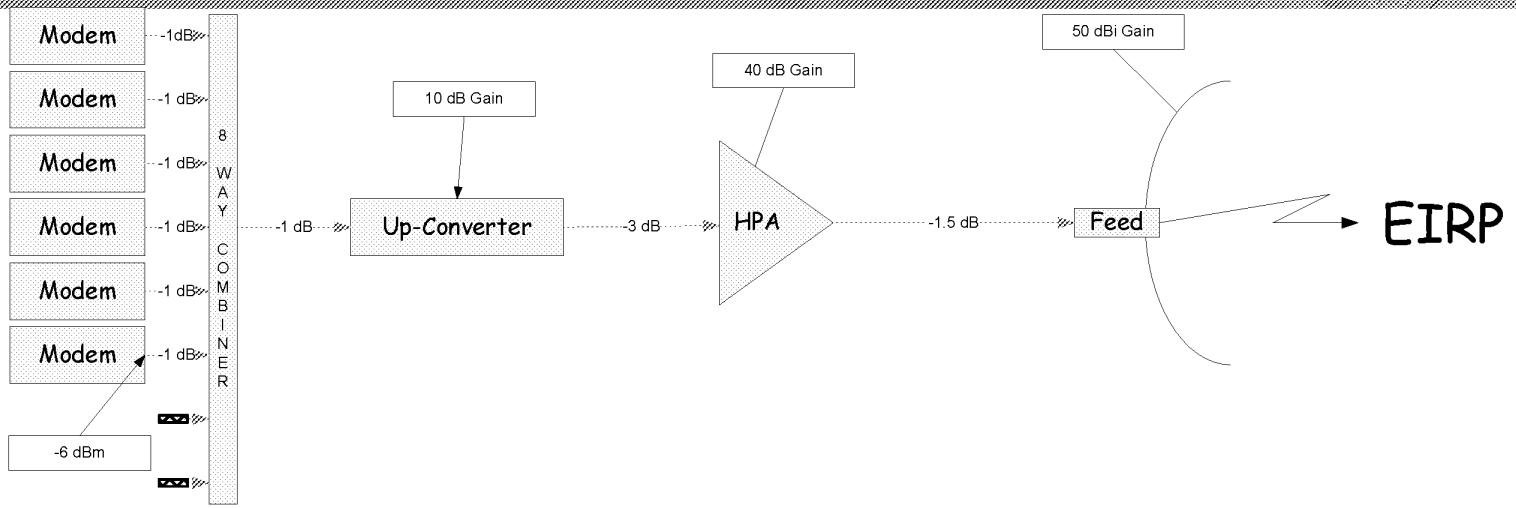
EIRP = -6 dBm – 9 - 2 dB + 10 dB – 3 dB + 40 dB – 1.5dB + 50 dBi

EIRP = 78.5 dBm

EIRP = 48.5 dBW

	Gain/Loss	Unit
Modem Output =	-6.00	dBm
Combiner Loss =	-9.00	dB
IF Cable Loss =	-2.00	dB
U/C Gain =	10.00	dB
RF Cable Loss =	-3.00	dB
HPA Gain =	40.00	dB
W/G Loss =	-1.50	dB
Antenna Gain =	50.00	dB
EIRP =	78.50	dBm
	48.50	**dBW**

IFL Uplink Link Budget



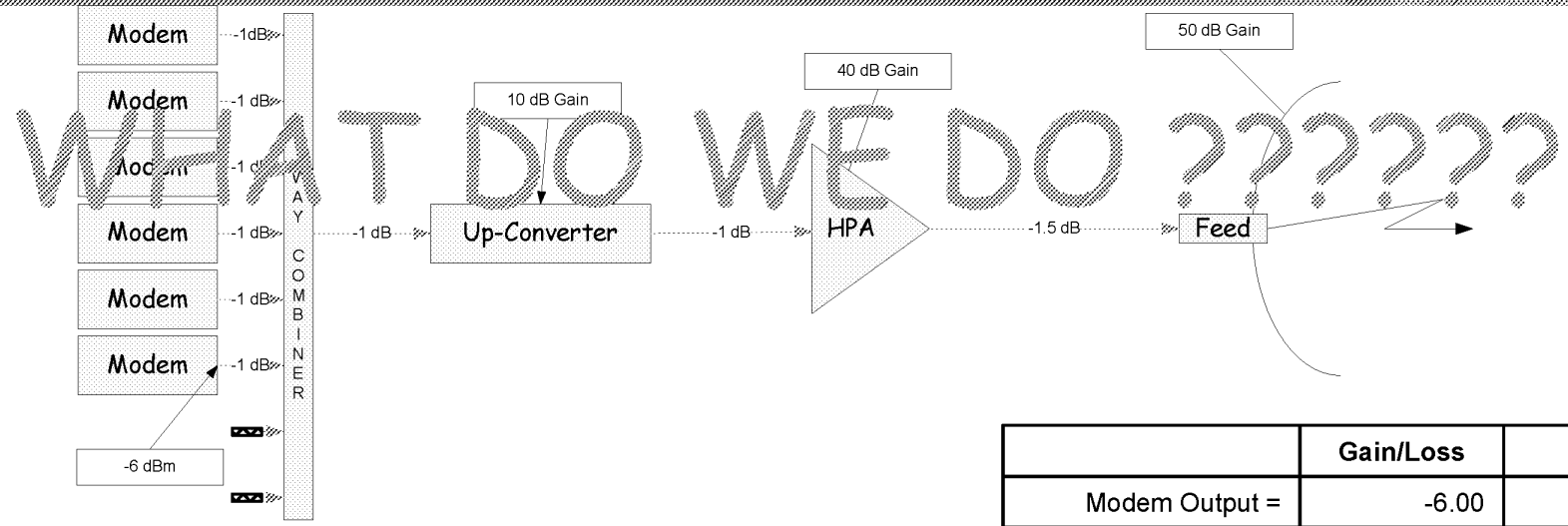
EIRP = Modem out – combiner loss – IF cable loss + U/C gain – RF cable loss + HPA gain – W/G loss + antenna gain

Does each carrier has an EIRP of 48.5 dBW? **YES**

What is the total EIRP?

48.5 dBW? **NO**
53.5 dBW? **NO**
54.5 dBW? **NO**
291 dBW? **NO**

IFL Uplink Link Budget



- Convert Modem output from dBm to dBW
- dBm – 30 = dBW
- Convert dBW to Watts
- $10^{(dBW/10)}$ = Watts
- Watts X Number of modems
- Convert total Watts to dBW
- 10*log (Watts)

	Gain/Loss	Unit
Modem Output =	-6.00	dBm
Convert dBm to dBW	-36.00	dBW
Convert dBW to Watt	0.000251	Watts
Total Modem Power =	.001507132	Watts
Convert Watt to dBW	-28.22	dBW
Combiner Loss =	-9.00	dB
IF Cable Loss =	-2.00	dB
U/C Gain =	10.00	dB
RF Cable Loss =	-3.00	dB
HPA Gain =	40.00	dB
W/G Loss =	-1.50	dB
Antenna Gain =	50.00	dBi
	56.28	**dBW**

EIRP

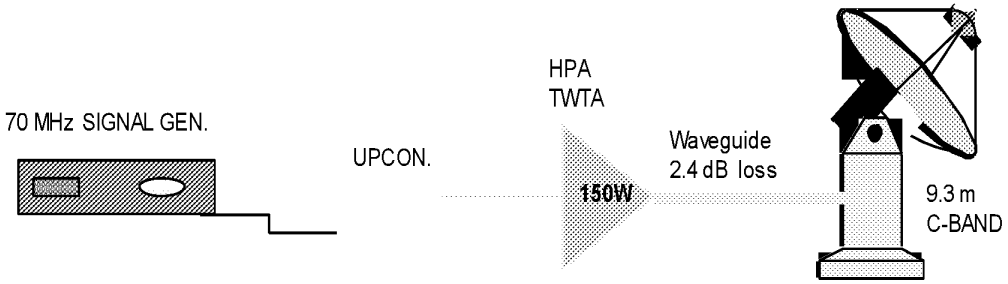
EFFECTIVE ISOTROPIC RADIATED POWER (dBW)

IT IS THE GROUND STATION OUTPUT POWER FOR A GIVEN ANTENNA GAIN TIMES THE INPUT POWER IN WATTS.

- **EIRP = GAIN (dBi) X POWER (watts)**

  OR

- **EIRP = ANT Gain (dBi) +Power (dBw) - line Loss (dBm)**



TEL Downlink Link Budgets

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IFL Downlink Link Budget

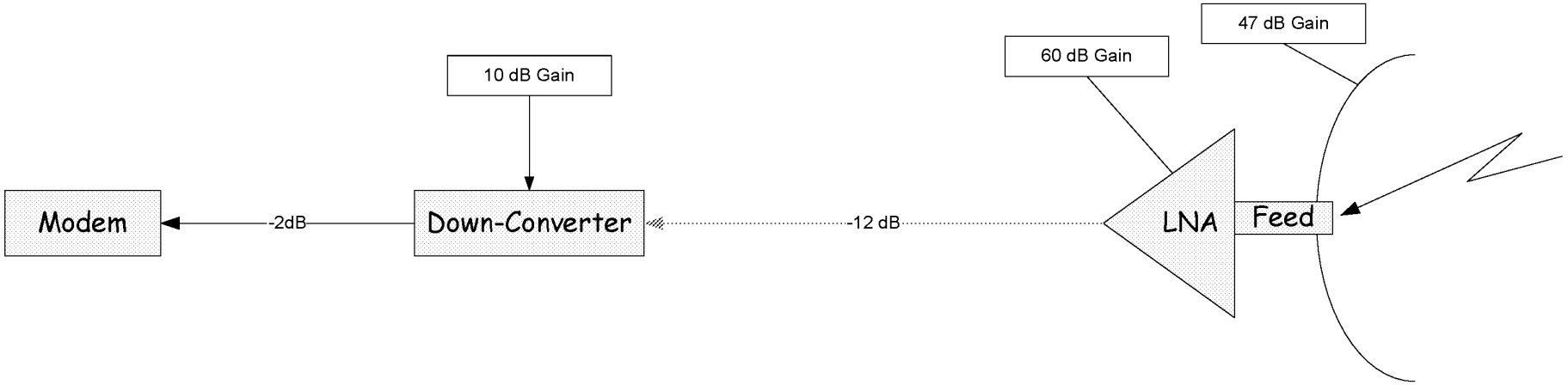
- Actual total receive signal level the antenna receives from the satellite is all carriers from the satellite on the receiving polarity and downlink beams visible at the receive station
- There is virtually no control over the receive signal level
- Example:
  - Receiving 12 transponders with downlink EIRP of 40dBW per
  - Receiving 4 transponders with downlink EIRP of 40dBW per

Transponder EIRP	40			dBW
Downlink space loss=	-195.8	dB	-155.8	dBm
RX antenna gain =	47	dBi	-108.8	dBW
	Per transponder		1.31826E-11	W
Total LNA input power	**12** transponders		1.58191E-10	W
			-98.00818754	dBW
			-68.00818754	dBm

Transponder EIRP	40			dBW
Downlink space loss=	-195.8	dB	-155.8	dBm
RX antenna gain =	47	dBi	-108.8	dBW
	Per transponder		1.31826E-11	W
Total LNA input power	**4** transponders		5.27303E-11	W
			-102.7794001	dBW
			-72.77940009	dBm

- LNA input level does not exceed typical maximum of -60 dBm

IFL Downlink Link Budget



Demodulator input = Sat EIRP – Space Loss + Ant gain + LNA gain – IF cable loss + D/C gain

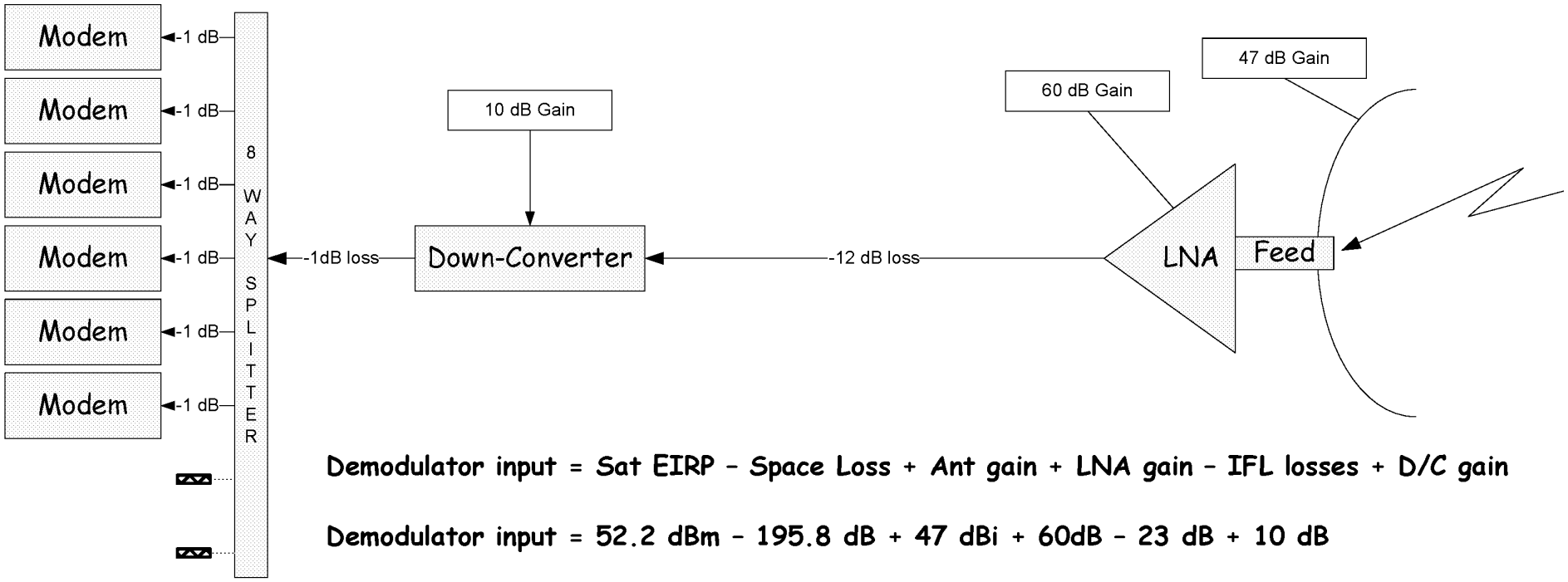
Demodulator input = 52.2 dBm – 195.8 dB + 47 dBi + 60dB – 14 dB + 10 dB

Demodulator input = -40.6 dBm

Sat EIRP =	22.2	dBW
Earth Station G/T =	20.9	dBK
Path Loss =	195.8	dB
Carrier Bandwidth =	1265000	Hz
Boltzmans Constant =	228.6	
C/N =	14.9	dB

Sat EIRP	22.2	dBW
	52.2	dBm
Space loss (195.8 dB)	-143.6	dB
ant gain (47 dBi)	-96.6	dBi
LNA gain (60 =dB)	-36.6	dB
IFL losses (14 dB)	-50.6	dB
D/C gain (10 dB)	-40.6	dBm

IFL Downlink Link Budget



Demodulator input = Sat EIRP – Space Loss + Ant gain + LNA gain – IFL losses + D/C gain

Demodulator input = 52.2 dBm – 195.8 dB + 47 dBi + 60dB – 23 dB + 10 dB

Demodulator input = -49.6 dBm

Sat EIRP =	22.2	dBW
Earth Station G/T =	20.9	dBK
Path Loss =	195.8	dB
Carrier Bandwidth =	1265000	Hz
Boltzmans Constant =	228.6	
C/N =	14.9	dB

Sat EIRP	22.2	dBW
	52.2	dBm
Space loss (195.8 dB)	-143.6	dB
ant gain (47 dBi)	-96.6	dBi
LNA gain (60 =dB)	-36.6	dB
IFL losses (23 dB)	-59.6	dB
D/C gain (10 dB)	-49.6	dBm

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Satellite Link Budget

Link Budgets

- This will provide an overview of the information that is required to perform a link budget and their impact on the Communication link

- Link Budget tool
  - Has much of the information we'll cover in the database
    - Make's your job much easier
  - Will be covered later in the training

Link Budget Information

- Site latitude
- Site longitude
- Altitude
- Frequency
- Polarization
- Availability
- Rain-climatic zone
- Antenna aperture
- Antenna efficiency (or gain)
- Coupling Loss
- Antenna mispointing loss
- LNB noise temperature
- Antenna ground noise temperature
- Adjacent channel interference C/ACI
- Adjacent satellite Interference C/ASI
- Cross polarization interference C/XPI
- HPA intermodulation interference C/I
- Satellite longitude
- Satellite receive G/T
- Satellite saturation flux density SFD
- Satellite gain setting
- Satellite EIRP (saturation)
- Transponder bandwidth
- Transponder input back-off (IBO)
- Transponder output back-off (OBO)
- Transponder intermodulation interference C/IM
- Required Overall Eb/No
- Information rate
- Overhead (% information rate)
- Modulation
- Forward error correction (FEC) code rate
- Roll off factor
- System margin
- Modulation
- Bit Error Rate (BER)

Link Availability

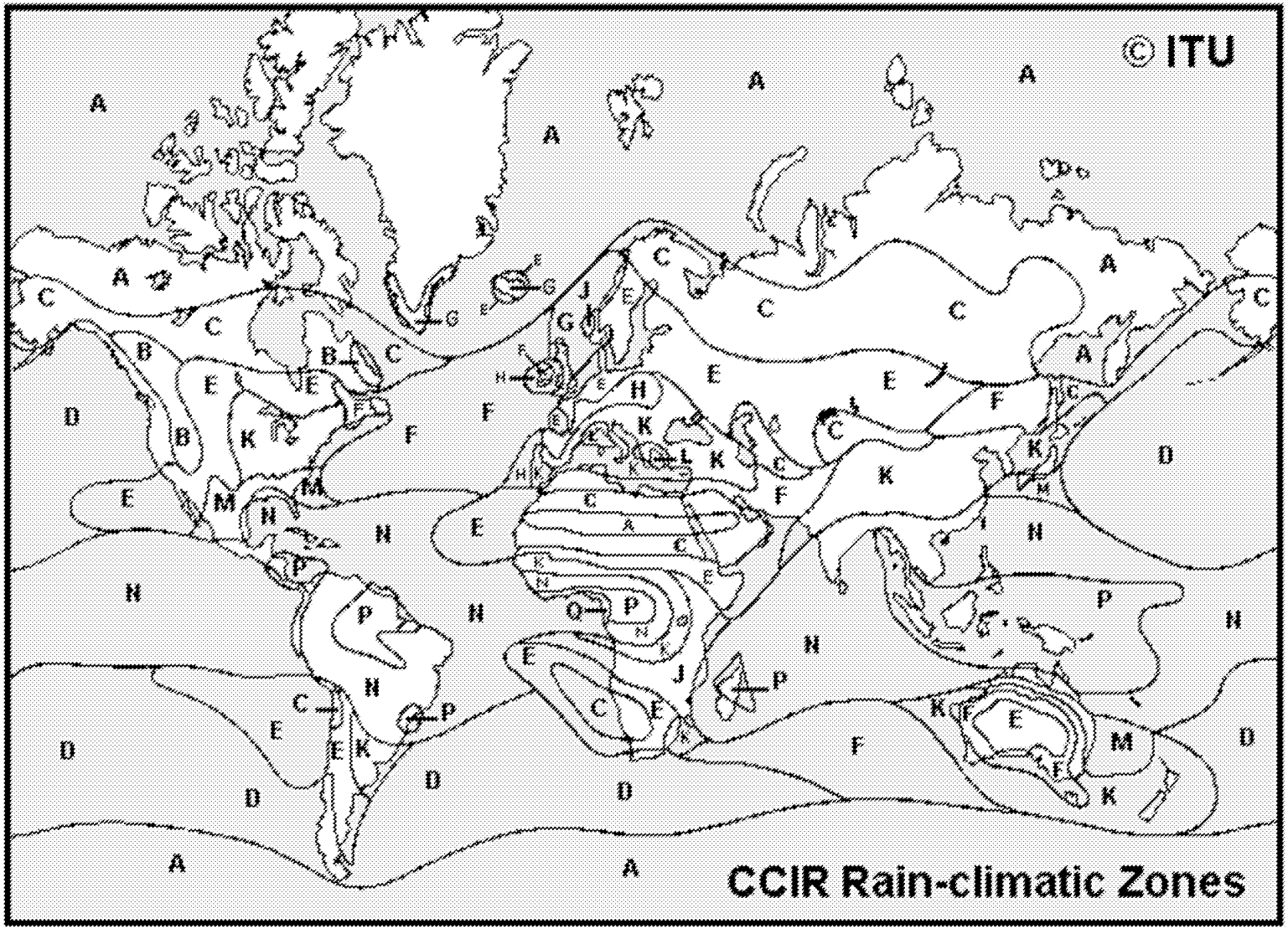
- Uplink in %
- Downlink in %
- End to End Link = $100-[(100-A_u)+(100-A_d)]$
  - Example: 99.75 % uplink, 99.75 % downlink

    = 100 - [(100-99.75)+(100-99.75)]

    = 100- (.25)+(.25)

  End to End Link = **99.50 %**
- Uplink and Downlink rain attenuation must also be added
  - Minor impact on C-Band
  - Major impact on Ku-Band
- Caution:
  - Do not use a large difference in uplink and downlink availability to meet End to End availability requirements

Rain-Climatic Zones



Rain-Climatic Zones

14 GHz Rain Attenuation vs. Availability for ITU rain Zones

	14 GHz Rain Attenuation by Zone													
AV(av.yr.)	A	B	C	D	E	F	G	H	J	K	L	M	N	P
99.999	4.15	6.56	8.42	10.93	12.83	16.62	17.88	19.13	20.98	25.23	35.24	36.75	49.19	50.47
99.995	2.49	3.93	5.04	6.55	7.69	9.96	10.71	11.46	12.58	15.12	21.12	22.02	29.48	30.25
99.990	1.94	3.06	3.93	5.10	5.99	7.76	8.34	8.92	9.79	11.77	16.44	17.15	22.96	23.55
99.950	1.01	1.60	2.05	2.66	3.12	4.05	4.35	4.66	5.11	6.14	8.58	8.95	11.98	12.29
99.900	0.74	1.17	1.50	1.95	2.29	2.97	3.19	3.42	3.75	4.51	6.30	6.56	8.79	9.02
99.700	0.44	0.69	0.89	1.15	1.35	1.75	1.88	2.02	2.21	2.66	3.71	3.87	5.18	5.32
99.500	0.34	0.53	0.68	0.89	1.04	1.35	1.45	1.55	1.70	2.05	2.86	2.98	3.99	4.10
99.000	0.23	0.37	0.47	0.61	0.72	0.93	1.00	1.07	1.18	1.42	1.98	2.06	2.76	2.83
98.000	0.16	0.25	0.32	0.42	0.49	0.63	0.68	0.73	0.80	0.96	1.34	1.40	1.87	1.92
97.000	0.13	0.20	0.25	0.33	0.39	0.50	0.54	0.58	0.63	0.76	1.06	1.11	1.48	1.52
96.000	0.11	0.17	0.21	0.28	0.33	0.42	0.45	0.49	0.53	0.64	0.89	0.93	1.25	1.28
95.000	0.09	0.15	0.19	0.24	0.28	0.37	0.40	0.42	0.47	0.56	0.78	0.82	1.09	1.12

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Rain-Climatic Zones

12 GHz Rain Attenuation vs. Availability for ITU rain Zones

	12 GHz Rain Attenuation by Zone													
AV(av.yr.)	A	B	C	D	E	F	G	H	J	K	L	M	N	P
99.999	2.86	4.61	5.98	7.85	9.28	12.17	13.13	14.09	15.53	18.84	26.77	27.99	38.22	39.32
99.995	1.71	2.76	3.58	4.71	5.56	7.29	7.87	8.45	9.31	11.29	16.05	16.77	22.91	23.57
99.990	1.33	2.15	2.79	3.66	4.33	5.68	6.13	6.58	7.25	8.79	12.49	13.06	17.84	18.35
99.950	0.70	1.12	1.46	1.91	2.26	2.96	3.20	3.43	3.78	4.59	6.52	6.82	9.31	9.58
99.900	0.51	0.82	1.07	1.40	1.66	2.17	2.35	2.52	2.77	3.37	4.78	5.00	6.83	7.02
99.700	0.30	0.49	0.63	0.83	0.98	1.28	1.38	1.48	1.64	1.99	2.82	2.95	4.03	4.14
99.500	0.23	0.37	0.49	0.64	0.75	0.99	1.07	1.14	1.26	1.53	2.17	2.27	3.10	3.19
99.000	0.16	0.26	0.34	0.44	0.52	0.68	0.74	0.79	0.87	1.06	1.50	1.57	2.14	2.21
98.000	0.11	0.18	0.23	0.30	0.35	0.46	0.50	0.54	0.59	0.72	1.02	1.07	1.46	1.50
97.000	0.09	0.14	0.18	0.24	0.28	0.37	0.40	0.42	0.47	0.57	0.81	0.84	1.15	1.18
96.000	0.07	0.12	0.15	0.20	0.24	0.31	0.33	0.36	0.39	0.48	0.68	0.71	0.97	1.00
95.000	0.06	0.10	0.13	0.17	0.21	0.27	0.29	0.31	0.34	0.42	0.59	0.62	0.85	0.87

Rain-Climatic Zones

6 GHz Rain Attenuation vs. Availability for ITU rain Zones

	6 GHz Rain Attenuation by Zone													
AV(av.yr.)	A	B	C	D	E	F	G	H	J	K	L	M	N	P
99.999	0.31	0.51	0.67	0.89	1.06	1.42	1.54	1.66	1.84	2.25	3.28	3.44	4.84	5.00
99.995	0.18	0.30	0.40	0.53	0.64	0.85	0.92	0.99	1.10	1.35	1.97	2.06	2.90	2.99
99.990	0.14	0.24	0.31	0.42	0.50	0.66	0.72	0.77	0.86	1.05	1.53	1.61	2.26	2.33
99.950	0.07	0.12	0.16	0.22	0.26	0.34	0.37	0.40	0.45	0.55	0.80	0.84	1.18	1.22
99.900	0.05	0.09	0.12	0.16	0.19	0.25	0.27	0.30	0.33	0.40	0.59	0.62	0.86	0.89
99.700	0.03	0.05	0.07	0.09	0.11	0.15	0.16	0.17	0.19	0.24	0.35	0.36	0.51	0.53
99.500	0.02	0.04	0.05	0.07	0.09	0.11	0.12	0.13	0.15	0.18	0.27	0.28	0.39	0.41
99.000	0.02	0.03	0.04	0.05	0.06	0.08	0.09	0.09	0.10	0.13	0.18	0.19	0.27	0.28
98.000	0.01	0.02	0.03	0.03	0.04	0.05	0.06	0.06	0.07	0.09	0.13	0.13	0.18	0.19
97.000	0.01	0.02	0.02	0.03	0.03	0.04	0.05	0.05	0.06	0.07	0.10	0.10	0.15	0.15
96.000	0.01	0.01	0.02	0.02	0.03	0.04	0.04	0.04	0.05	0.06	0.08	0.09	0.12	0.13
95.000	0.01	0.01	0.01	0.02	0.02	0.03	0.03	0.04	0.04	0.05	0.07	0.08	0.11	0.11

Rain-Climatic Zones

4 GHz Rain Attenuation vs. Availability for ITU rain Zones

	4 GHz Rain Attenuation by Zone													
AV(av.yr.)	A	B	C	D	E	F	G	H	J	K	L	M	N	P
99.999	0.08	0.12	0.15	0.19	0.22	0.29	0.31	0.33	0.36	0.42	0.57	0.60	0.77	0.79
99.995	0.05	0.07	0.09	0.12	0.13	0.17	0.18	0.20	0.21	0.25	0.34	0.36	0.46	0.47
99.990	0.04	0.06	0.07	0.09	0.10	0.13	0.14	0.15	0.17	0.20	0.27	0.28	0.36	0.37
99.950	0.02	0.03	0.04	0.05	0.05	0.07	0.07	0.08	0.09	0.10	0.14	0.15	0.19	0.19
99.900	0.01	0.02	0.03	0.03	0.04	0.05	0.05	0.06	0.06	0.08	0.10	0.11	0.14	0.14
99.700	0.01	0.01	0.02	0.02	0.02	0.03	0.03	0.03	0.04	0.04	0.06	0.06	0.08	0.08
99.500	0.01	0.01	0.01	0.02	0.02	0.02	0.02	0.03	0.03	0.03	0.05	0.05	0.06	0.06
99.000	0.00	0.01	0.01	0.01	0.01	0.02	0.02	0.02	0.02	0.02	0.03	0.03	0.04	0.04
98.000	0.00	0.00	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.02	0.02	0.02	0.03	0.03
97.000	0.00	0.00	0.00	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.02	0.02	0.02	0.02
96.000	0.00	0.00	0.00	0.00	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.02	0.02	0.02
95.000	0.00	0.00	0.00	0.00	0.00	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.02	0.02

Coupling Loss

- **Uplink**
  - The total loss between HPA output and the antenna
    - Waveguide components
    - OMT
    - Feed
    - Filter truncation
- **Downlink**
  - The total loss between antenna and LNA/LNB input
    - Feed
    - OMT
    - Waveguide components

Antenna Mispointing Loss

- Allows for the pointing loss between the ground station antenna and the satellite antenna
  - It is unlikely that the antenna will be targeted exactly due to initial installation errors
  - Antenna stability due to wind
  - Station keeping accuracy of the satellite
- A typical allowance for mispointing is 0.5 dB
  - A large antenna without tracking may require more due to the narrow beamwidth

LNA / LNB Noise Temperature

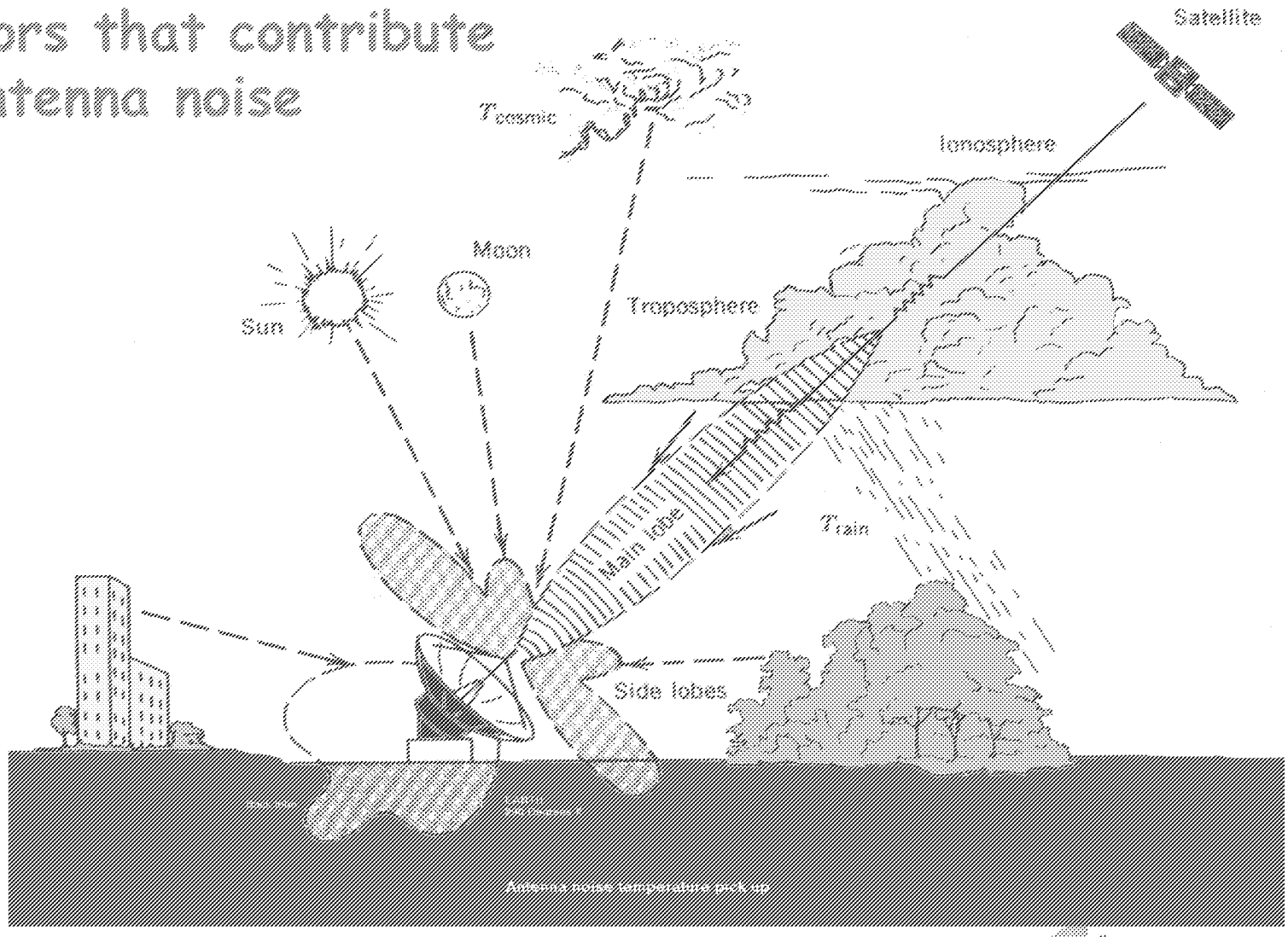
- C-Band are normally quoted as Noise Temperature in °Kelvin
- Ku-Band are normally quoted as Noise Figure in dB
  - Noise Figure to Noise Temperature
    - Noise temperature (T) = 290 * (10^(Noise Figure/10)-1)

  Example: Noise Figure = 1.0 dB
  Noise Temp = 290 * (10^(1.0/10)-1 = 75°K

  - The higher the frequency the more difficult and expensive it is to achieve low noise figures
- The LNA/LNB is one of the most critical components of an antenna system receive system
  - Major factor in determining the systems figure of merit (G/T)
  - Frequency stability of LNB critical depending on type of service
  - Low data rate carriers

Antenna Noise Temperature

- Factors that contribute to antenna noise



Antenna Noise Temperature

- The total noise temperature of the antenna , ($T_{ant} = T_{sky} + T_{gnd}$) depends mainly on the following factors:
  - Sky Noise (T_{sky})
    - The sky noise consists of two main components, atmospheric and the background radiation (2.7K)
    - The upper atmosphere is an absorbing medium
    - Sky noise increases with elevation due to the increasing path through the atmosphere
  - Ground Noise (T_{gnd})
    - The dominant contribution to antenna noise is ground noise pick up through side lobes
    - Noise temperature increases as the elevation angle decreases since lower elevation settings, will pick up more ground noise due to side lobes intercepting the ground
    - A deep dish picks up less ground noise at lower elevations than do shallow ones
- Since antenna noise temperature has so many variable factors, an estimate is perhaps the best we can hope for

Antenna Noise Temperature

- Typical 3.6m antenna - Offset

Elevation angle (deg)	Noise temp (C band)	Noise temp (Ku band) (K)
10	24	31
20	16	23
30	15	21
40	14	20

- Typical 6m antenna

Elevation angle (deg)	Noise temp (C band)	Noise temp (Ku band)
10	39	55
20	30	40
40	23	37

Antenna Noise Temperature

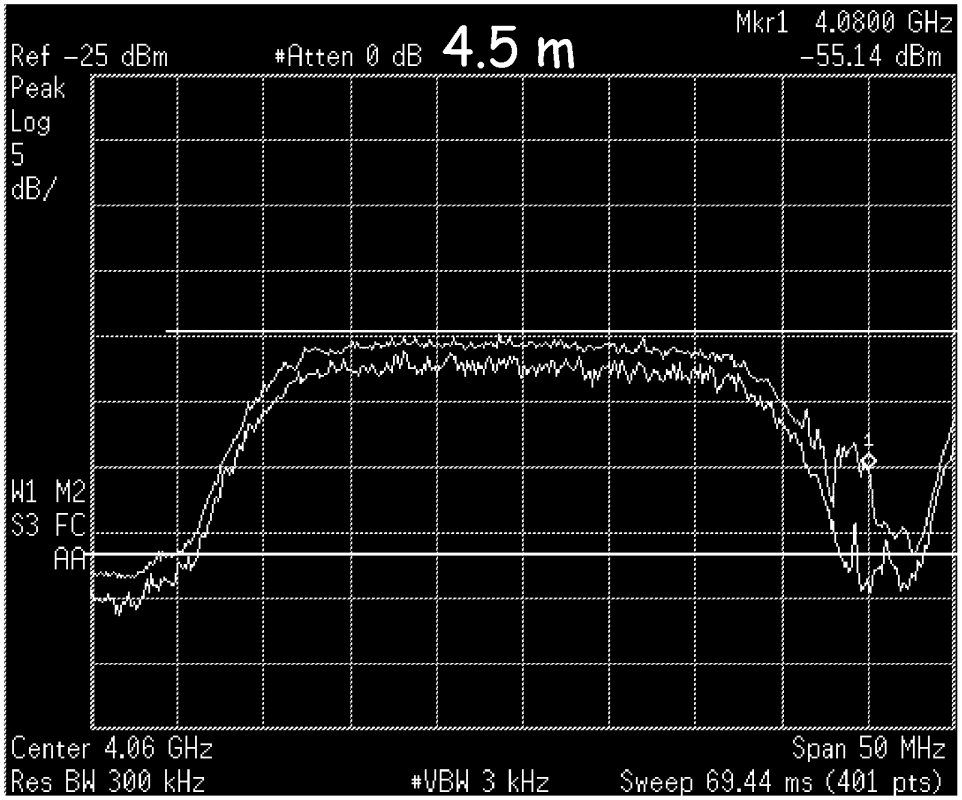
- Typical 10m C-Band antenna

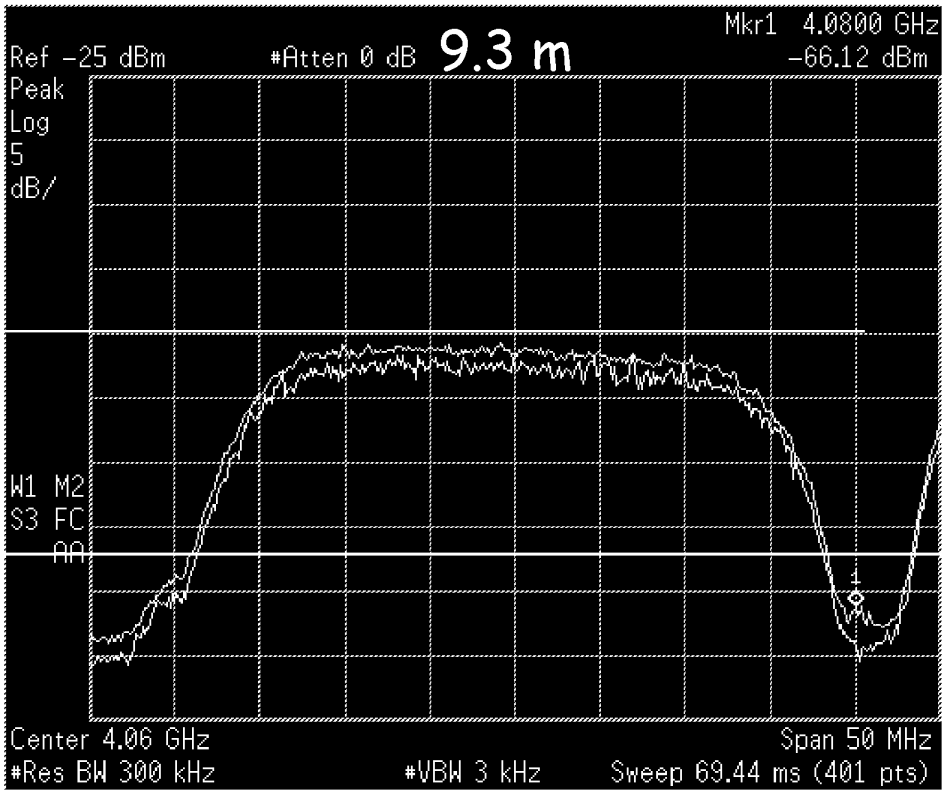
Elevation angle (deg)		Antenna noise temperature
5	-	46
10	-	35
15	-	29
20	-	24
30	-	17
40	-	14

- To the above you need to add extra according to the complexity of the feed:
  - 2 port rx only, add 4.5
  - 2 port rx and tx, add 4.5
  - 3 port 2 rx and 1 tx, add 4.5
  - 4 port 2 rx and 2 tx, add 9.9

Antenna G/T

- Spec An plots showing G/T difference
- 4.5m
  - C+N/N ≈ 17.5 dB
  - NF ≈ -65 dBm
- 9.3M
  - C+N/N ≈ 22.5 dB
  - NF ≈ -70 dBm



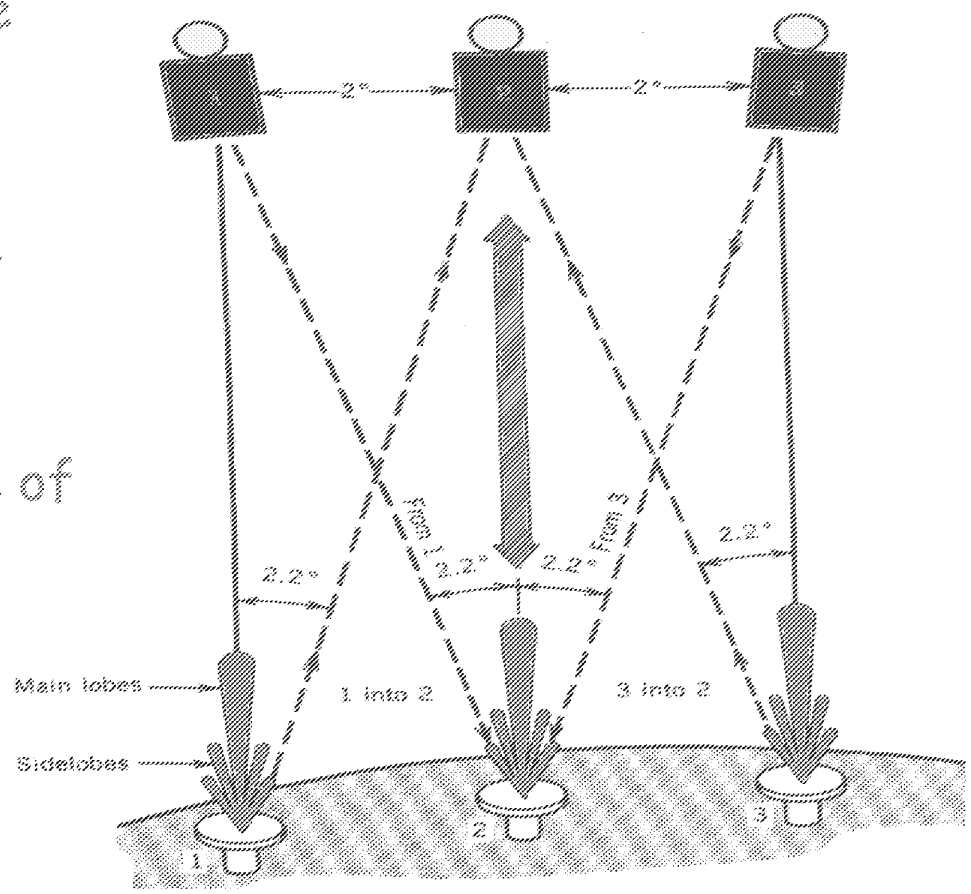


Adjacent Channel Interference C/ACI

- Unwanted electrical interference from signals that are immediately adjacent in frequency to the desired signal
  - Due to imperfections in the transmission channel and/or equipment
- This parameter specifies the expected interference level with respect to the wanted carrier
- Typical values, irrespective of whether the uplink or downlink co-channel C/ASI is of interest, are in the range 24 to 30 dB

Adjacent Satellite Interference (C/ASI)

- The level of ASI is a function of several parameters:
  - Orbital separation between the desired and the interfering satellites
  - Antenna side lobe performance of the interfering uplink earth station
  - Antenna side lobe performance of the receiving earth station
  - Spectral Power density of the carriers
  - Typically in the range of 18 to 30 dB



Cross Polarization Interference C/XPI

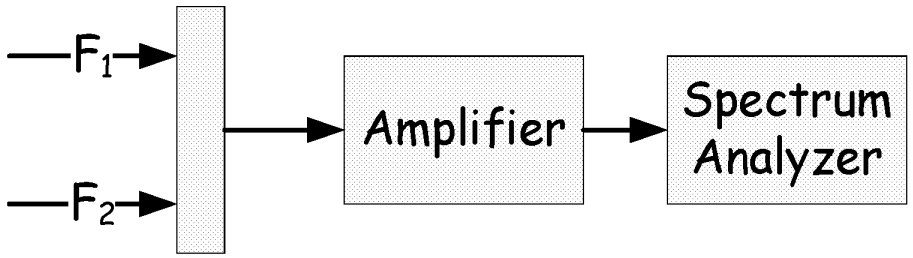
- A value for the carrier to cross polarization interference noise ratio C/XPI in dB
- Specifies the expected interference level with respect to the wanted carrier
- Typical values, irrespective of whether the uplink or downlink C/XPI is of interest, are in the range 24 to 34 dB

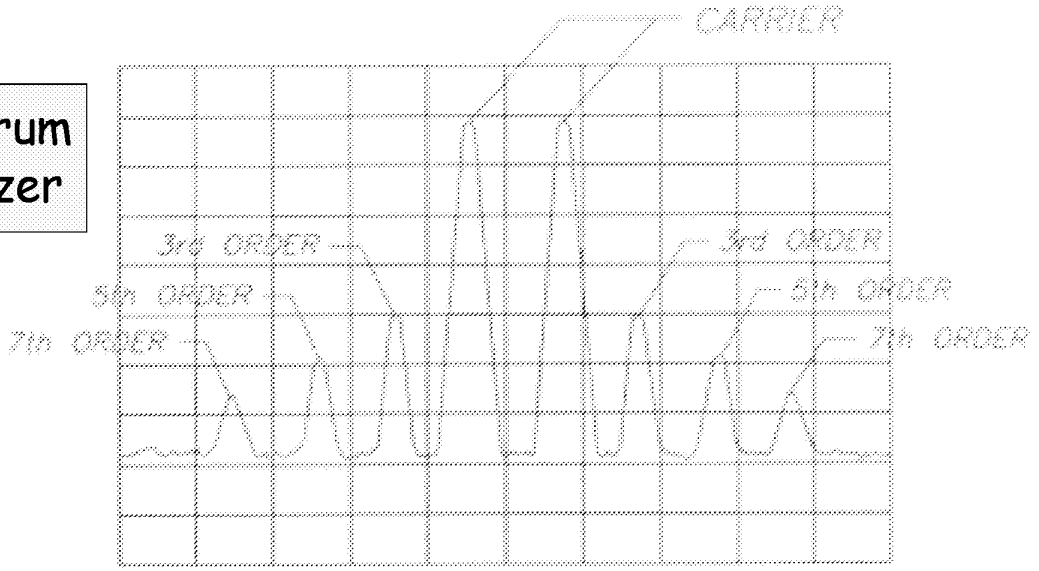
Total Cross-Pol Isolation Total XPI =-20log[$10^{(Sxp/20)}$+$10^{(Exp/20)}$]		
Satellite X-Pol =	40	db
Antenna X-Pol =	35	dB
Total X-Pol Isolation =	31.1	dB

Cross Polarization Interference C/XPI

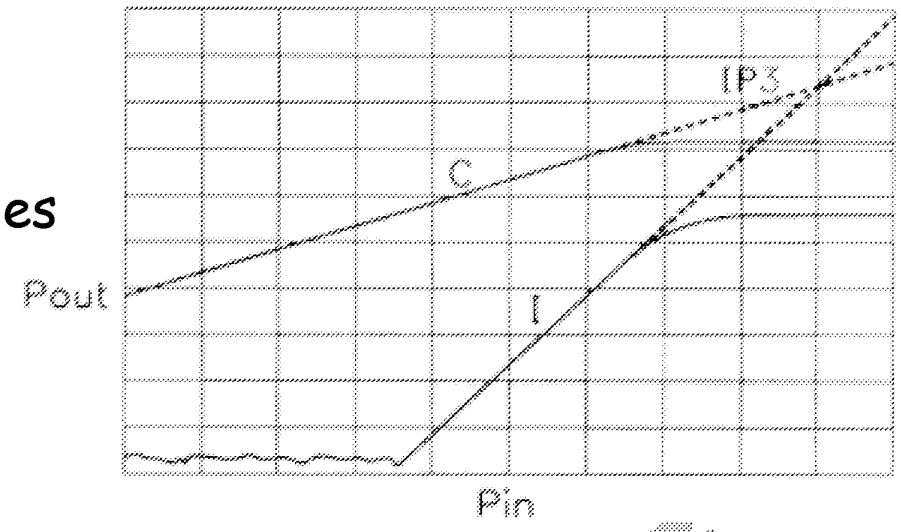
- Frequency re-use by dual polarization doubles the available frequency spectrum at each orbital location using orthogonal signals (V-H)
- Since orthogonal polarization is not perfect in actual implementation
  - There is some coupling between the orthogonal signals generated by the transmitting antenna and at the receiving antenna
    - These couplings can create signal degradation
  - In addition, the transmitted wave and the orientation of the receiving antenna polarizer also affect the polarization angle and, hence, introduce degradation to the receiving antenna polarization performance
  - The rotation of the antenna polarizer angle with respect to the satellite downlink wave's tilt angle effects the receiving antenna polarization isolation performance.

HPA Intermodulation (C/IM)





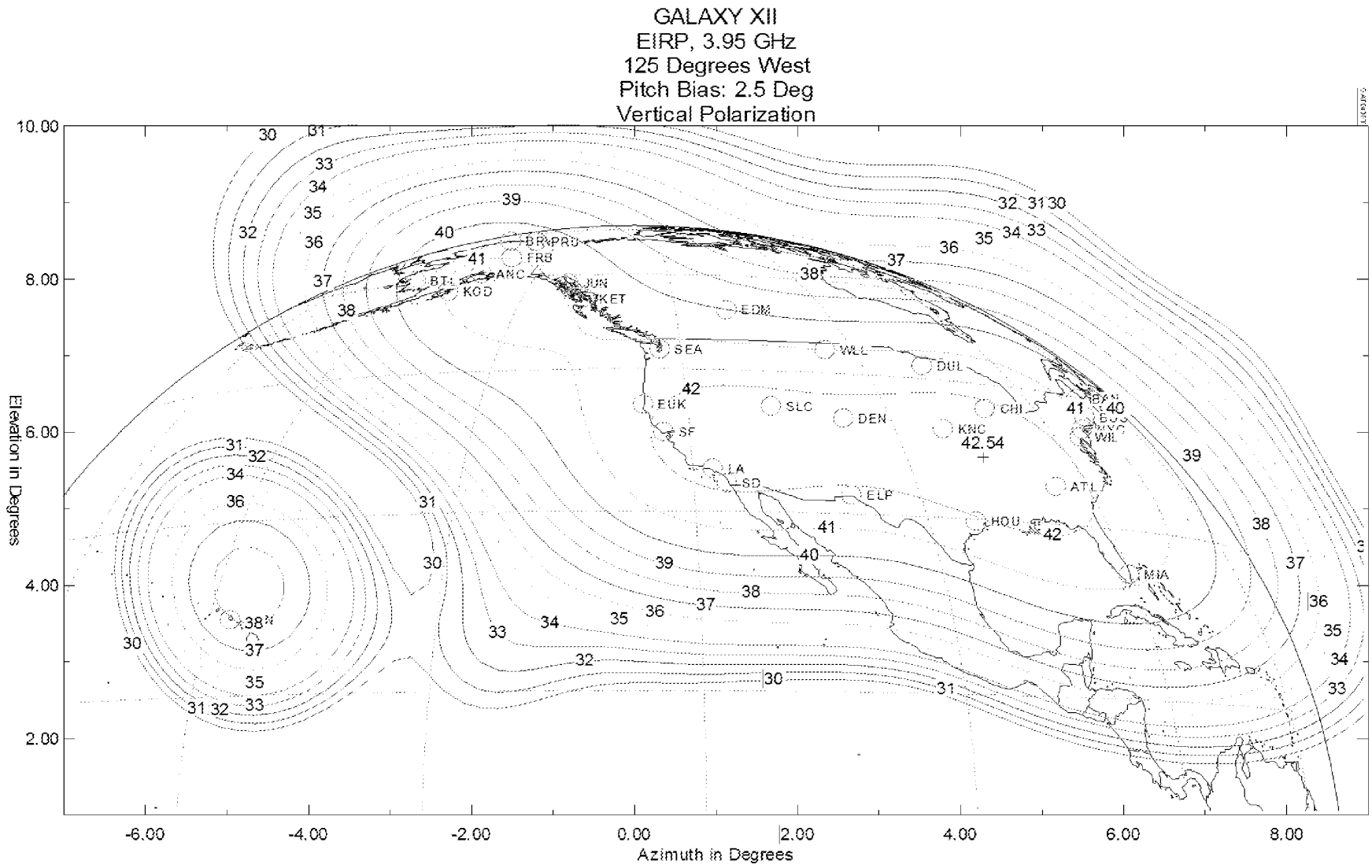
As P_{in} is increased, the intermodulation signal will increase with power three times as fast as the carrier signal.



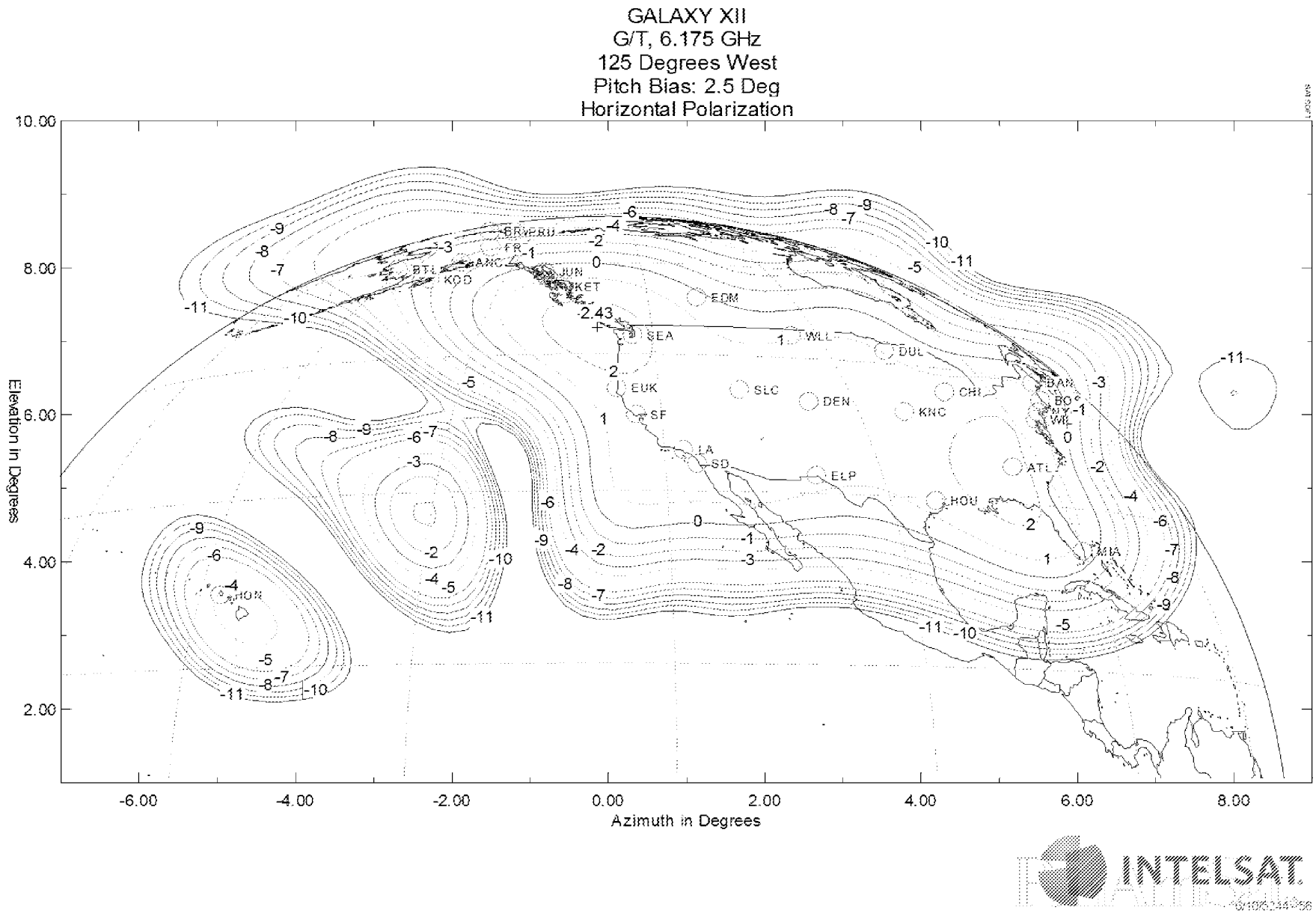
Satellite Information

- Satellite Longitude
  - Orbital position
- Satellite receive G/T
  - Value to the specific location of the uplink earth station
  - Obtained from satellite operators or G/T contour maps
- Satellite saturation flux density SFD
  - The power needed to saturate the satellite's transponder
- Satellite gain setting
  - Most satellites have a gain step attenuator, which affects all carriers in the transponder
  - May, or may not, be include in the SFD specification
- Satellite EIRP (saturation)
  - Transponder's effective isotropic radiated power (EIRP) at saturation in the specific direction of the receive earth receive station Value to the specific location of the uplink earth station
  - Obtained from satellite operators or G/T contour maps

Example of EIRP Contour



Example of G/T Contour



Satellite Information

- Transponder bandwidth
  - Satellites full transponder bandwidth
- Transponder input back-off (IBO)
  - Input back off, or operating point, relative to saturation to reduce intermodulation interference
- Transponder output back-off (OBO)
  - Related, in a non linear fashion, to the input back-off
- Transponder intermodulation interference C/IM
  - Specifies the carrier-to-intermodulation noise ratio in dB
  - Depends on such factors as center frequency and the exact number, type and positions of other carriers sharing the transponder
  - Increasing the input back-off also reduces the effect of this interference.
  - There is little C/IM effect if only one carrier is present in the transponder

Carrier Information

- Required Overall Eb/No for desired BER
  - Depends on
    - Modulation Type
    - FEC Rate
    - Coding

BER PERFORMANCE (E_b/N_o, dB)

Viterbi

BER	1/2	3/4	7/8
10^{-3}	3.8	4.9	6.1
10^{-4}	4.6	5.7	6.9
10^{-5}	5.3	6.4	7.6
10^{-6}	6.0	7.2	8.3
10^{-7}	6.6	7.9	8.9
10^{-8}	7.2	8.5	9.6

Viterbi & Reed-Solomon

BER	1/2	3/4	7/8
10^{-6}	4.1	5.6	6.7
10^{-7}	4.2	5.8	6.9
10^{-8}	4.4	6.0	7.1
10^{-10}	5.0	6.3	7.5

56 kbps, Sequential

BER	1/2	3/4	7/8
10^{-3}		4.6	5.5
10^{-4}	4.1	5.1	6.1
10^{-5}	4.5	5.5	6.6
10^{-6}	5.0	5.9	7.3
10^{-7}	5.4	6.4	7.8
10^{-8}	5.8	6.8	8.4

1544 kbps Sequential

BER	1/2	3/4	7/8
10^{-3}	4.8	5.2	6.0
10^{-4}	5.2	5.7	6.4
10^{-5}	5.6	6.1	6.9
10^{-6}	5.9	6.5	7.4
10^{-7}	6.3	7.0	7.9
10^{-8}	6.7	7.4	8.4

1544 kbps, Sequential & RS

BER	1/2	3/4	7/8
10^{-6}	4.1	5.6	6.7
10^{-7}	4.2	5.8	6.9
10^{-8}	4.4	6.0	7.1
10^{-10}	5.0	6.3	7.5

8PSK with/without RS

BER	2/3 w/o RS	2/3 with RS
10^{-6}	8.7	6.1
10^{-7}	9.5	6.4
10^{-8}	10.2	6.6
10^{-9}	11	6.9
10^{-10}	11.8	7.2

Viterbi, OQPSK

BER	1/2	3/4	7/8
10^{-3}	4.1	5.2	6.4
10^{-4}	4.9	6.0	7.2
10^{-5}	5.6	6.7	7.9
10^{-6}	6.3	7.5	8.6
10^{-7}	6.9	8.2	9.2
10^{-8}	7.5	8.8	9.9

Turbo Product Codec

	QPSK	BPSK		8PSK
BER	3/4	21/44	5/16	3/4
10^{-6}	3.9	2.8	-	7.0
10^{-7}	4.1	3.1	-	7.3
10^{-8}	4.3	3.3	-	7.6
10^{-9}	4.8	3.7	4.0	8.0

Carrier Information

- **Information rate**
  - User information rate of the data in Mbps
- **Overhead (% information rate)**
  - Amount of "overhead" added to the information data rate to account for miscellaneous signaling requirements
    - i.e. Reed Solomon
- **Modulation**
  - Type of modulation
    - BPSK, QPSK, 8PSK, 16QAM, etc.
- **Forward error correction (FEC) code rate**
  - Code rate used with forward error correction
    - 0.5, 0.667, 0.75, .875, etc.

Carrier Information

- Roll off factor
  - The occupied bandwidth of a carrier is normally taken to be 1.1 times the symbol rate, thus the roll off factor is 1.1
- System margin
  - Accounts for uncertainty in the various input parameters and to allow for difficult to quantify non-linear effects such as AM-PM conversion and perhaps terrestrial interference
- Bit error rate (BER)
  - The BER of the link
  - 10-7 was typical of legacy systems
  - 10-9 is desirable for IP links

INTELSAT

Controllable parameters

Link Budget Parameters

- The majority of link budget parameters are out of your control
- Those that you may control
  - Antenna size
    - Transmit
    - Receive
      - Existing or new
  - LNA / LNB
    - Noise Temperature
  - Carrier
    - Modulation type
    - FEC rate
    - Coding

Link Budget Parameters

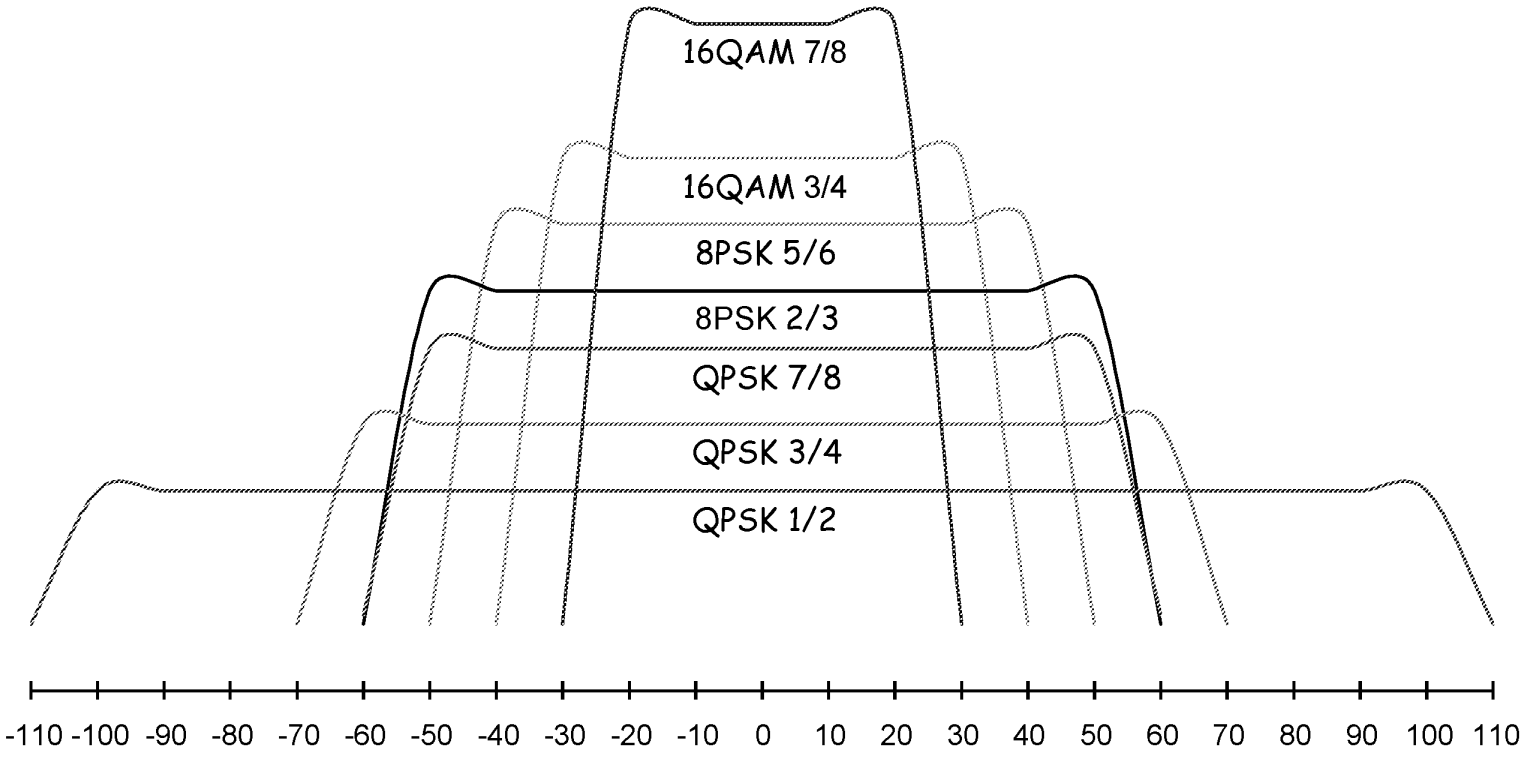
- Antenna
  - Typically as small as possible
    - Cost
    - Zoning requirements
    - Aesthetics
- LNA / LNB
  - Noise Temperature
    - Major impact on system G/T
  - Frequency stability
    - Critical for low data rates

Link Budget Parameters

- Carrier – (modulation, FEC, coding)
  - Satellite bandwidth required
    - Balanced power and bandwidth operation
      - i.e. 10% transponder power, 10% transponder bandwidth
- HPA power requirement
  - Ensure proper backoff to prevent intermodulation and spectral regrowth
  - Antenna requirements
    - Larger transmit, less HPA power required
    - Larger receive, less satellite power required

Effect of Modulation & FEC

Bandwidth For Various Modulation & Coding Types



Symbol Rate and OBW Calculations

Bandwidth Calculation		
Symbol Rate = Information Rate/(Modulation * FEC Rate)		
Information Rate =	1544	kbps
Modulation Type =	2	1 = BPSK, 2 = QPSK, 3 = 8PSK, 4 = 16QAM
FEC Rate =	0.75	.5, .75, .875, etc
Symbol Rate =	1029.3	kHz
Occupied Bandwidth =	1132.3	kHz

Bandwidth Calculation with Reed Solomon		
Symbol Rate = Information Rate/(Modulation * FEC Rate * Coding)		
Information Rate =	1544	kbps
Modulation Type =	2	1 = BPSK, 2 = QPSK, 3 = 8PSK, 4 = 16QAM
FEC Rate =	0.75	.5, .75, .875, etc
Inner =	188	
Outer =	204	
Reed Solomon	0.92	Overhead
Symbol Rate =	1116.9	kHz
Occupied Bandwidth =	1229	kHz

Satellite Carrier Spacing

- Occupied Bandwidth *(OBW)*
  - Bandwidth the carrier actually occupies
    - Typically 1.1 - 1.2 x Symbol Rate
- Allocated bandwidth *(ABW)*
  - Satellite bandwidth allocated for the carrier
    - Equal Symbol Rate *(SR)* carriers
      - (SR) x 1.4 = Carrier Space Traditional
      - (SR) x 1.2 = Carrier Space Practical
    - Different Symbol Rate carriers
      - (SR1 + SR2) x 0.7 = Carrier Space Traditional
      - (SR1 + SR2) x 0.6 = Carrier Space Practical

Eb/No and C/N

- Convert C/N to Eb/No

Eb/No = C/N + (10*log(OBW/DR)		
Bandwidth =	750.9	kHz
bps =	1024	kbps
C/N =	10.65	dB
Eb/No =	**9.30**	dB

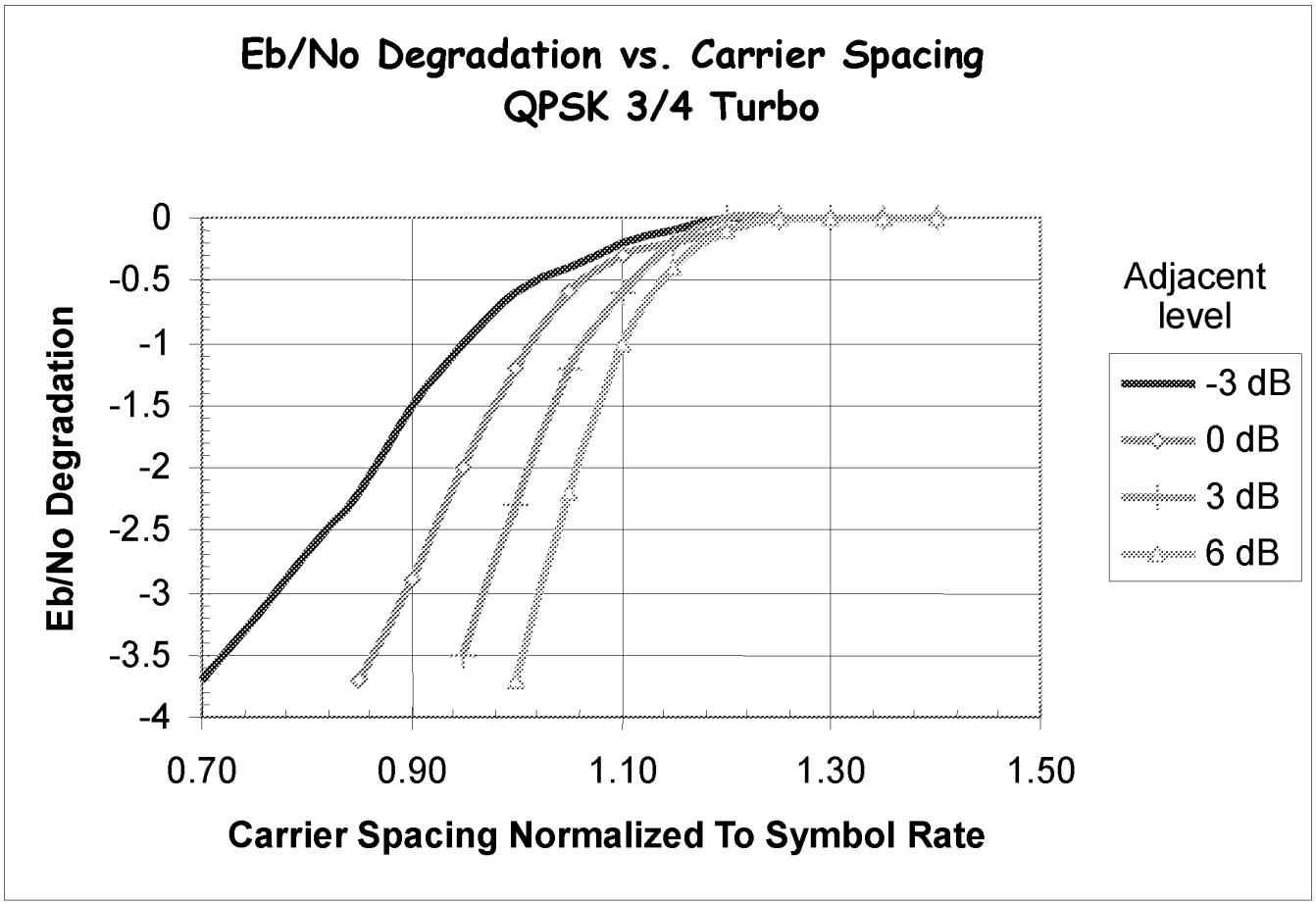
- Convert Eb/No to C/N

C/N = Eb/No - 10*log(OBW/DR)		
OBW =	750.9	kHz
DR =	1024	kbps
Eb/No =	9.3	dB
C/N =	**10.6**	dB

Performance as effected by Channel Spacing

Degradation created by 2 adjacent carriers QPSK

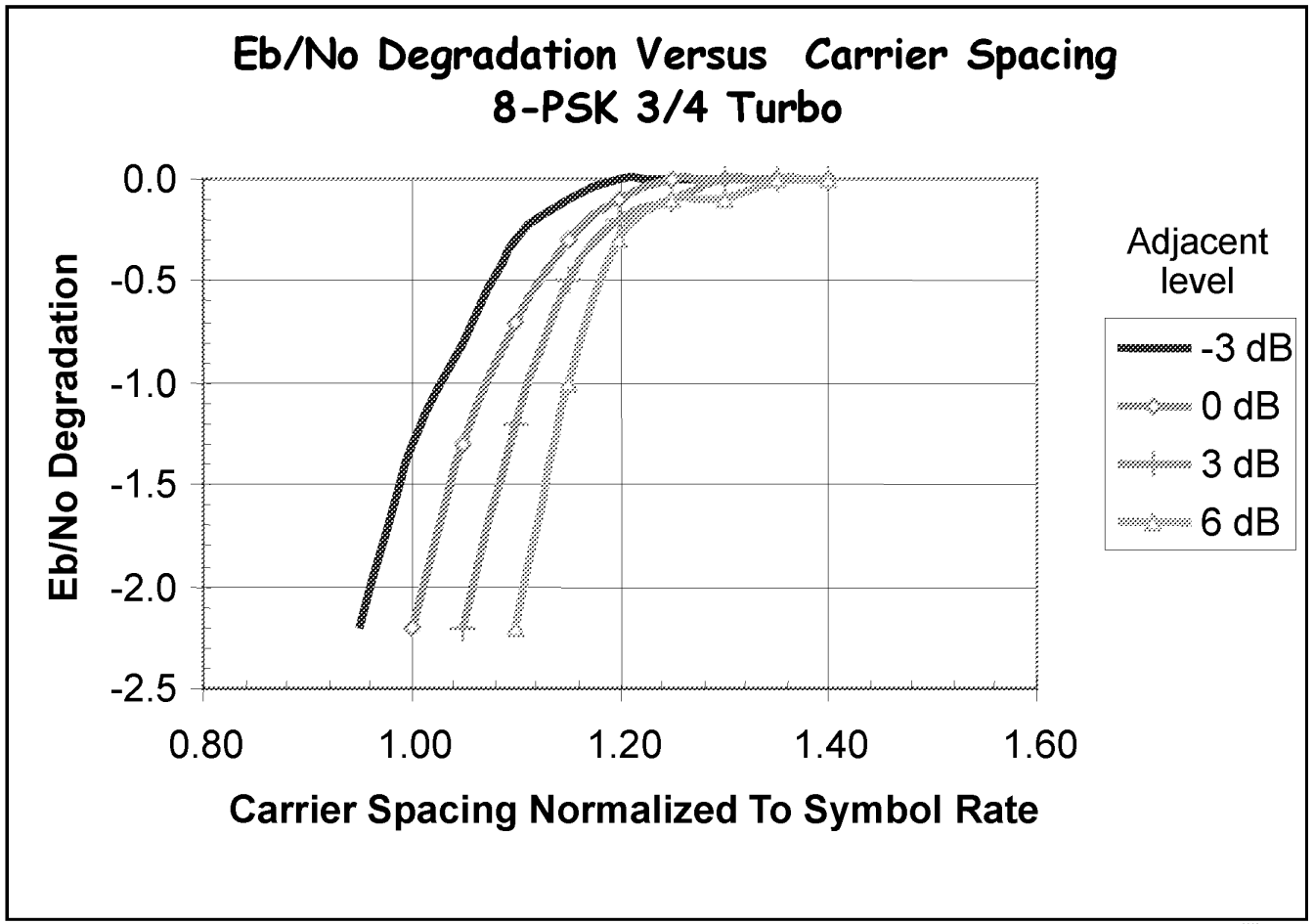
Zero degradation line = BER performance 10^{-8}



Performance as effected by Channel Spacing

Degradation created by 2 adjacent carriers 8PSK

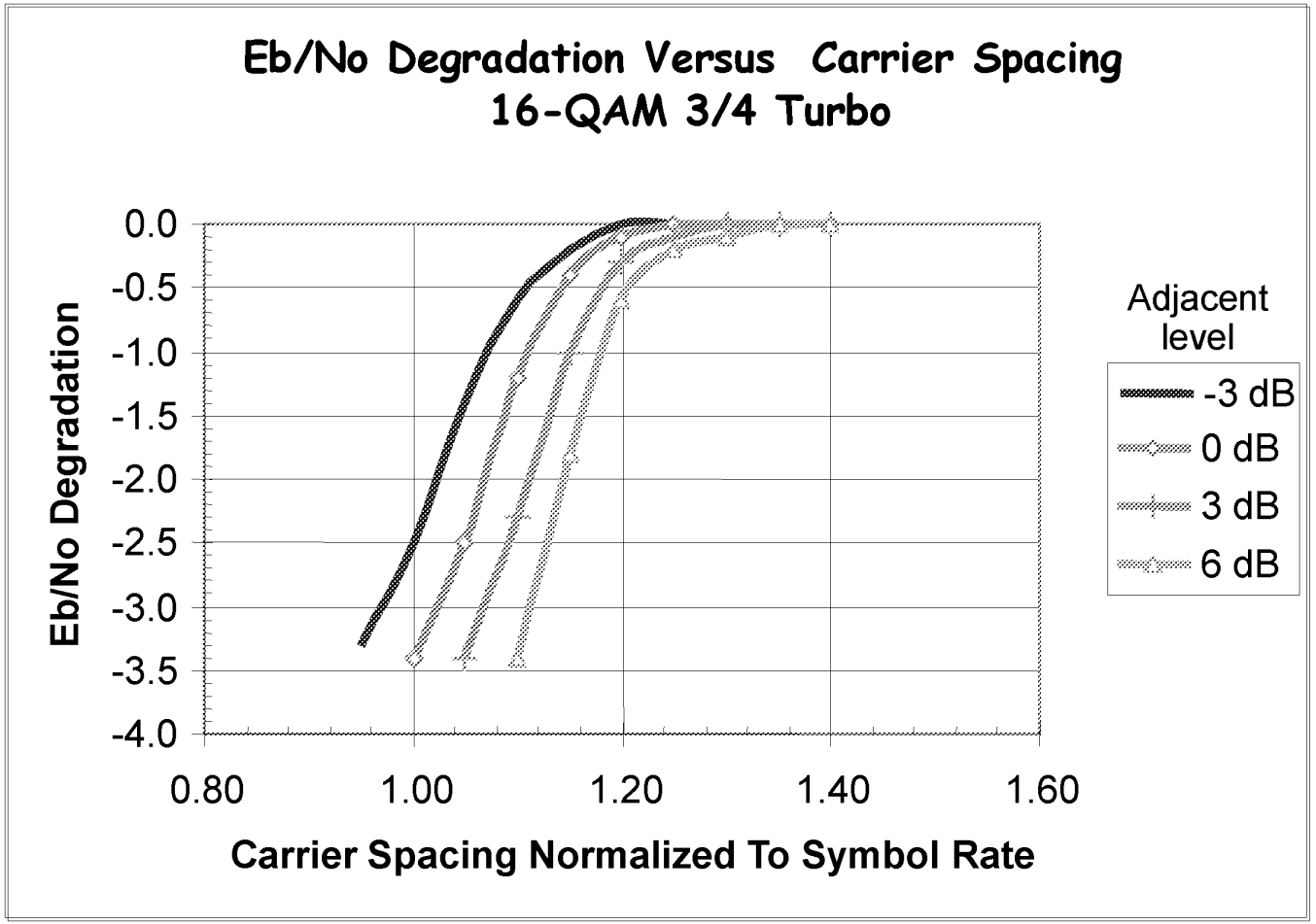
Zero degradation line = BER performance 10^{-8}



Performance as effected by Channel Spacing

Degradation created by 2 adjacent carriers 16QAM

Zero degradation line = BER performance 10^{-8}

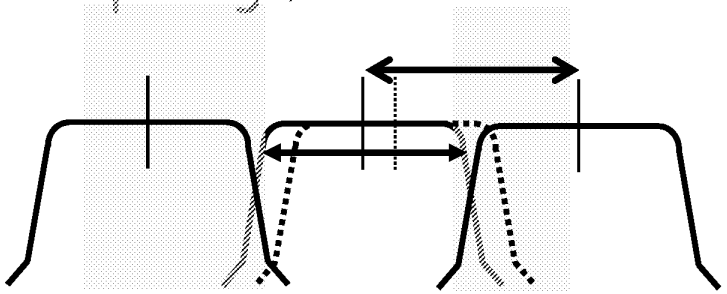


Carrier Spacing at Low Data Rates

- Low Data Rate carriers
  - Must take into consideration frequency drift possibilities for all uplink carrier equipment
  - Use worse case frequency drift based on the equipment specs

Example:	Symbol Rate	= 19.200 kbps
	1.2 channel spacing	= 23.040 kHz
	Mod Freq Stability	= 0.255 kHz
	U/C Freq Stability	= 3.055 kHz
	Spacing with drift	= 22.510 kHz

  - Carriers could be impacted by ACI
    - Use 1.3 or 1.4 spacing for low data rate carriers



Coding

- Reed Solomon
  - Advantages
    - 2 dB better Eb/No performance over Viterbi
    - Excellent when combined with 8PSK TCM
  - Disadvantages
    - Increased Latency
    - ≈ 10% bandwidth for overhead
    - Hard decision decoder

Coding

- Turbo Product Codec
  - Advantages
    - Best BER performance at given power level
    - Typical 1.8 dB improvement over Reed Solomon
    - Less latency then Reed Solomon
    - Soft Decision Decoder
    - Fade Tolerant
  - Disadvantages
    - Compatibility between vendors

Link Budget

- Where to start
  - TX antenna gain (Size and efficiency)
  - RX antenna gain (Size and efficiency)
  - LNA noise temperature
  - Modulation Type
  - FEC Rate
  - Coding
  - Required Eb/No for desired availability
  - Uplink rain margin
  - Downlink rain margin
- Run calculation

Link Budget Results

- Verify bandwidth % vs. power % of transponder
  - Bandwidth greater than power
    - Smaller receive antenna
    - Higher order modulation
    - Higher FEC rate
  - Power greater than bandwidth
    - Larger receive antenna
    - Lower order modulation
    - Lower FEC rate
  - Change Eb/No requirements
- Repeat calculations

BER Performance

BER PERFORMANCE (E_b/N_o, dB)

Viterbi

BER	1/2	3/4	7/8
10^{-3}	3.8	4.9	6.1
10^{-4}	4.6	5.7	6.9
10^{-5}	5.3	6.4	7.6
10^{-6}	6.0	7.2	8.3
10^{-7}	6.6	7.9	8.9
10^{-8}	7.2	8.5	9.6

Viterbi & Reed-Solomon

BER	1/2	3/4	7/8
10^{-6}	4.1	5.6	6.7
10^{-7}	4.2	5.8	6.9
10^{-8}	4.4	6.0	7.1
10^{-10}	5.0	6.3	7.5

56 kbps, Sequential

BER	1/2	3/4	7/8
10^{-3}		4.6	5.5
10^{-4}	4.1	5.1	6.1
10^{-5}	4.5	5.5	6.6
10^{-6}	5.0	5.9	7.3
10^{-7}	5.4	6.4	7.8
10^{-8}	5.8	6.8	8.4

1544 kbps Sequential

BER	1/2	3/4	7/8
10^{-3}	4.8	5.2	6.0
10^{-4}	5.2	5.7	6.4
10^{-5}	5.6	6.1	6.9
10^{-6}	5.9	6.5	7.4
10^{-7}	6.3	7.0	7.9
10^{-8}	6.7	7.4	8.4

1544 kbps, Sequential & RS

BER	1/2	3/4	7/8
10^{-6}	4.1	5.6	6.7
10^{-7}	4.2	5.8	6.9
10^{-8}	4.4	6.0	7.1
10^{-10}	5.0	6.3	7.5

8PSK with/without RS

BER	2/3 w/o RS	2/3 with RS
10^{-6}	8.7	6.1
10^{-7}	9.5	6.4
10^{-8}	10.2	6.6
10^{-9}	11	6.9
10^{-10}	11.8	7.2

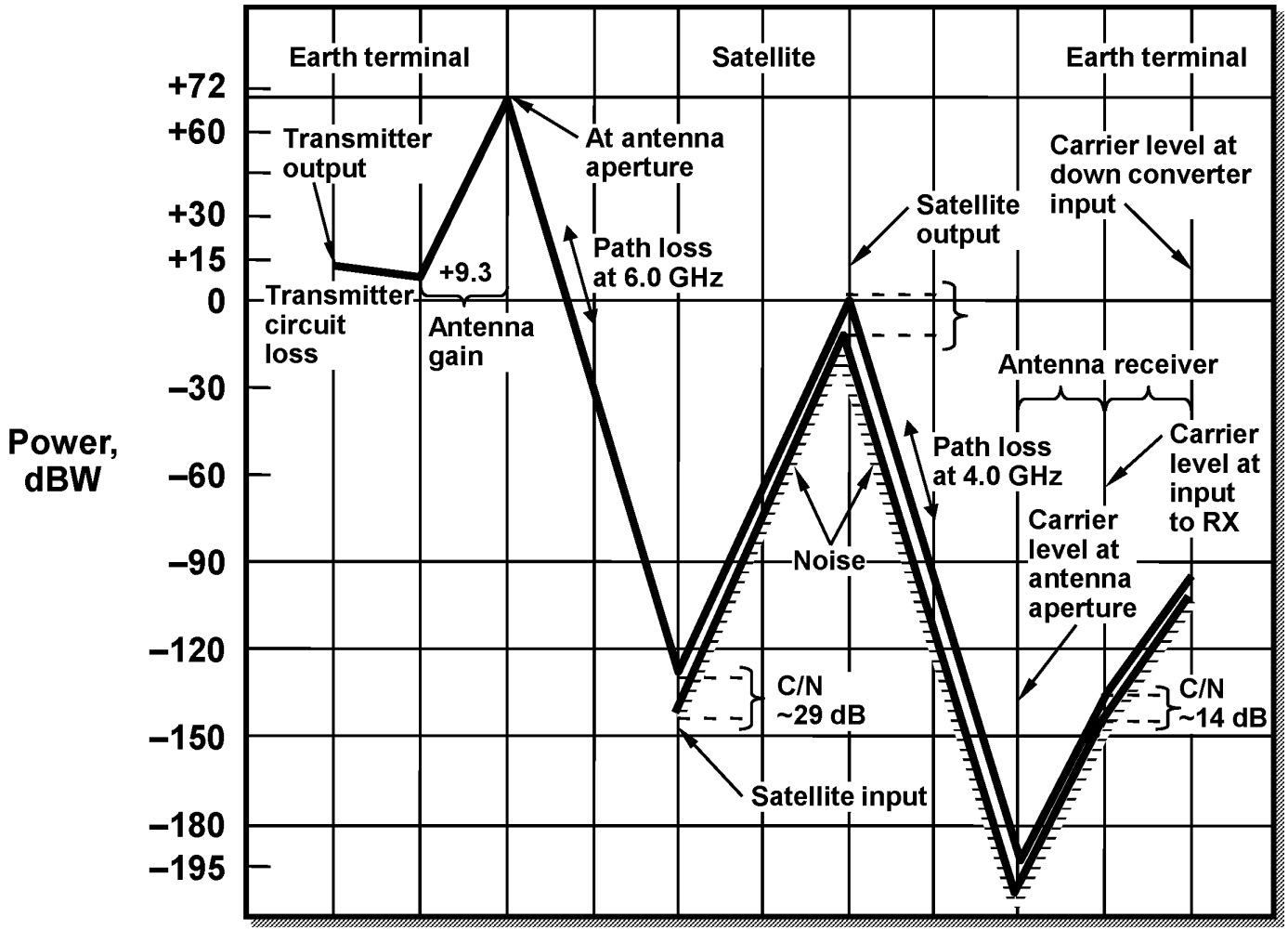
Viterbi, OQPSK

BER	1/2	3/4	7/8
10^{-3}	4.1	5.2	6.4
10^{-4}	4.9	6.0	7.2
10^{-5}	5.6	6.7	7.9
10^{-6}	6.3	7.5	8.6
10^{-7}	6.9	8.2	9.2
10^{-8}	7.5	8.8	9.9

Turbo Product Codec

	QPSK	BPSK		8PSK
BER	3/4	21/44	5/16	3/4
10^{-6}	3.9	2.8	-	7.0
10^{-7}	4.1	3.1	-	7.3
10^{-8}	4.3	3.3	-	7.6
10^{-9}	4.8	3.7	4.0	8.0

Link Budget Representation (C/N)



Gain, losses, and noise over the up and downlinks of a communication satellite system

INTELSAT

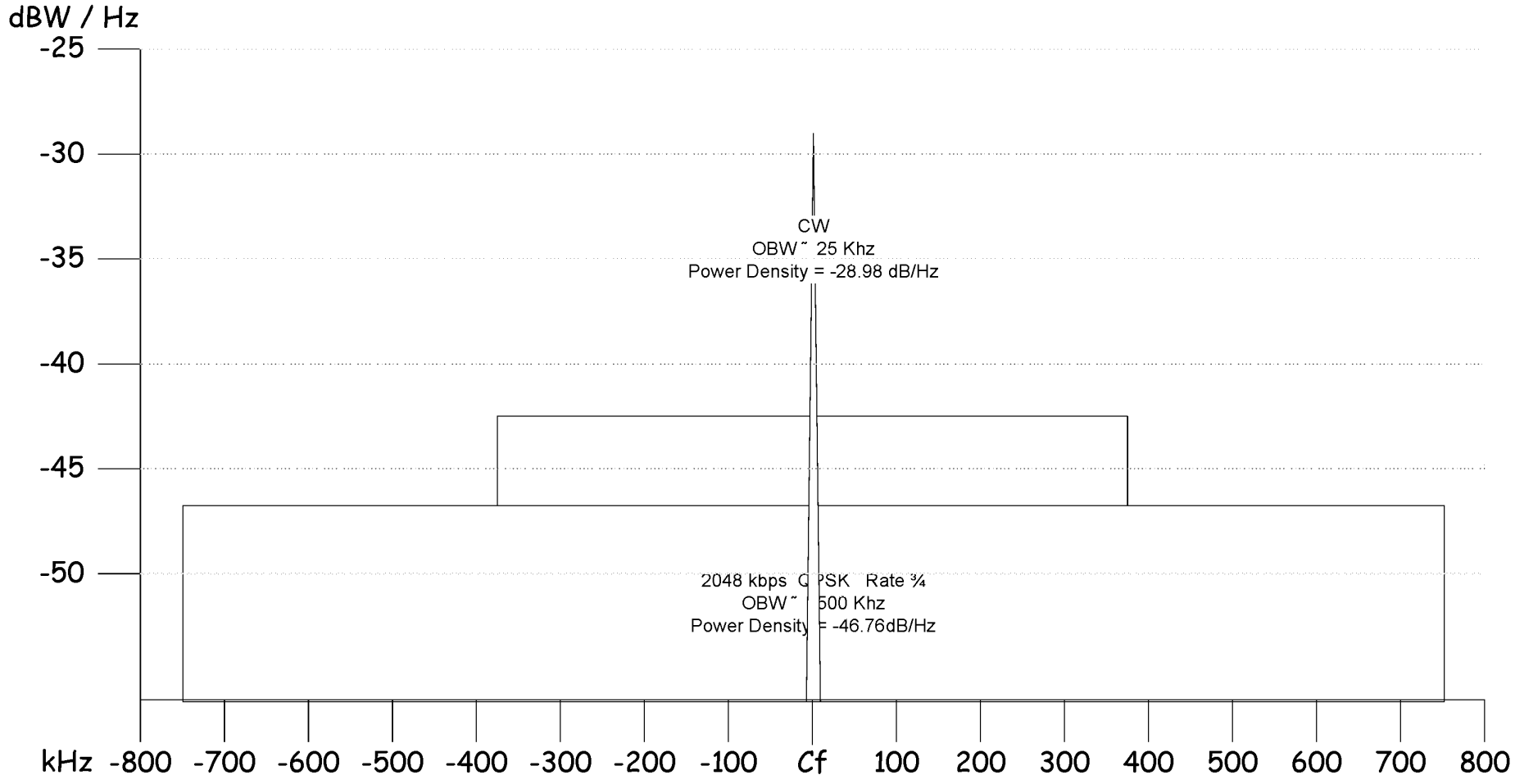
Spectral Power Density

Spectral Power Density

- What is Spectral power density?
  - The amount of power in dBW over a specified frequency span (dBW/Hz, dBW/4kHz, dBW/40kHz)
- Intelsat typical C-Band limits for antenna > 3.8 meter:
  Minus (-) 43 dBW / Hz
- Intelsat typical Ku-Band limits for antenna > 1.9 meter:
  Minus (-) 42 dBW / Hz
- Smaller antenna may be used but there are power density restrictions
- Why do we have restrictions?
  - Prevent uplink interference to adjacent satellites
- Actual power density allowable coordinated on a satellite by satellite basis

Spectral Power Density

- Increase of OBW results in a decrease in dBW/Hz



Spectral Power Density

- Power Density may be given in:
  - dB/Hz for both C and Ku-Band
  - dBW/4 kHz for C-Band
  - dBW/40 kHz for Ku-band

Power Density				
Feed Flange Power	10.52	dBW		
	11.27	Watts	11.27	Watts
Occupied Bandwidth	750.90	kHz	750.90	kHz
	0.000015	Watts / Hz	0.000015	Watts Hz
Power Density	-48.24	dBW / Hz	-48.24	dBW / Hz
	-12.22	dBW / 4 kHz	-12.22	dBW / 4 kHz
	-2.22	dBW / 40 kHz	-2.22	dBW / 40 kHz

Spectral Power Density

- Example
  - 64 kbps, QPSK, Rate $\frac{3}{4}$ with 40 Watts transmit power
  - 1024 kbps, QPSK, Rate $\frac{3}{4}$ with 40 Watts transmit power
  - 64 kbps = -31.32 dBW / Hz

40.00	Watts	
54.20	kHz	Calculated Occupied Bandwidth
0.000738	Watts / Hz	OBW_{Hz} / Watts
-31.32	dBW / Hz	10*log (Watts/Hz)

  - 1024 kbps = - 43.36 dBW / Hz

40.00	Watts
867.00	kHz
0.000046	Watts / Hz
-43.36	dBW / Hz

C-Band Power Density Restrictions

	C-band				
Antenna Size (m)	Mid-band Gain (dBi) 60%	Antenna Pattern Restriction (dB)	Antenna Off-point Restriction (.5 dB)	Total Restriction	Density Limits dBW/Hz
1.20	35.58	8.35	3.63	11.98	-54.98
1.30	36.28	7.65	3.51	11.16	-54.49
1.40	36.92	7.48	3.44	10.92	-53.92
1.50	37.52	6.90	3.30	10.15	-53.15
1.60	38.08	6.10	3.20	9.30	-52.30
1.70	38.61	5.72	3.05	8.27	-51.27
1.80	39.11	4.23	2.88	7.11	-50.11
1.90	39.58	3.13	2.76	5.89	-48.89
2.00	40.02	1.92	2.64	4.56	-47.56
2.10	40.45	0.67	2.45	3.06	-46.06
2.20	40.85	0.00	2.33	2.33	-45.33
2.30	41.24	0.00	1.94	1.94	-44.94
2.40	41.61	0.00	1.46	1.46	-44.46
2.60	42.30	0.00	1.32	1.32	-44.32
2.80	42.94	0.00	0.88	0.88	-43.88
3.00	43.54	0.00	0.76	0.76	-43.76
3.50	44.88	0.00	0.78	0.78	-43.78
3.70	45.36	0.00	0.46	0.46	-43.46
3.80	45.60	0.00	0.16	0.16	-43.16

Ku-Band Power Density Restrictions

	Ku-band				
Antenna Size (m)	Mid-band Gain (dBi) 60%	Antenna Pattern Restriction (dB)	Antenna Off-point Restriction (.5 dB)	Total Restriction	Density Limits dBW / Hz
0.60	36.83	7.57	3.42	10.99	-52.99
0.65	37.52	6.88	3.28	10.16	-52.15
0.70	38.17	6.97	3.22	9.19	-51.19
0.75	38.77	4.83	3.20	8.03	-50.03
0.80	39.33	3.74	2.93	6.67	-48.67
0.85	39.85	2.93	2.82	5.75	-47.75
0.90	40.35	0.92	2.72	3.64	-45.64
0.95	40.82	0.60	2.60	3.20	-45.20
1.00	41.26	0.00	2.42	2.42	-44.42
1.10	42.09	0.00	2.25	2.25	-44.25
1.20	42.85	0.00	1.98	1.98	-43.98
1.30	43.54	0.00	1.68	1.68	-43.68
1.40	44.19	0.00	1.50	1.50	-43.50
1.50	44.79	0.00	1.20	1.20	-43.20
1.60	45.35	0.00	1.00	1.00	-43.00
1.70	45.87	0.00	0.75	0.75	-42.75
1.80	46.37	0.00	0.47	0.47	-42.47
1.90	46.84	0.00	0.28	0.28	-42.28
2.00	47.28	0.00	0.00	0.00	-42.00

Appendix 3

RECOMMENDATION ITU-R P.618-8

Propagation data and prediction methods required for the design of Earth-space telecommunication systems

(Question ITU-R 206/3)

(1986-1990-1992-1994-1995-1997-1999-2001-2003)

The ITU Radiocommunication Assembly,

considering

a) that for the proper planning of Earth-space systems it is necessary to have appropriate propagation data and prediction techniques;

b) that methods have been developed that allow the prediction of the most important propagation parameters needed in planning Earth-space systems;

c) that as far as possible, these methods have been tested against available data and have been shown to yield an accuracy that is both compatible with the natural variability of propagation phenomena and adequate for most present applications in system planning,

recommends

1 that the methods for predicting the propagation parameters set out in Annex 1 be adopted for planning Earth-space radiocommunication systems, in the respective ranges of validity indicated in Annex 1.

NOTE 1 – Supplementary information related to the planning of broadcasting-satellite systems as well as maritime, land, and aeronautical mobile-satellite systems, may be found in Recommendations ITU-R P.679, ITU-R P.680, ITU-R P.681 and ITU-R P.682, respectively.

Annex 1

1 Introduction

In the design of Earth-space links for communication systems, several effects must be considered. Effects of the non-ionized atmosphere need to be considered at all frequencies, but become critical above about 1 GHz and for low elevation angles. These effects include:

a) absorption in atmospheric gases; absorption, scattering and depolarization by hydrometeors (water and ice droplets in precipitation, clouds, etc.); and emission noise from absorbing media; all of which are especially important at frequencies above about 10 GHz;

b) loss of signal due to beam-divergence of the earth-station antenna, due to the normal refraction in the atmosphere;

c) a decrease in effective antenna gain, due to phase decorrelation across the antenna aperture, caused by irregularities in the refractive-index structure;

d) relatively slow fading due to beam-bending caused by large-scale changes in refractive index; more rapid fading (scintillation) and variations in angle of arrival, due to small-scale variations in refractive index;

e) possible limitations in bandwidth due to multiple scattering or multipath effects, especially in high-capacity digital systems;

f) attenuation by the local environment of the ground terminal (buildings, trees, etc.);

g) short-term variations of the ratio of attenuations at the up- and down-link frequencies, which may affect the accuracy of adaptive fade countermeasures;

h) for non-geostationary satellite (non-GSO) systems, the effect of varying elevation angle to the satellite.

Ionospheric effects (see Recommendation ITU-R P.531) may be important, particularly at frequencies below 1 GHz. For convenience these have been quantified for frequencies of 0.1; 0.25; 0.5; 1; 3 and 10 GHz in Table 1 for a high value of total electron content (TEC). The effects include:

j) Faraday rotation: a linearly polarized wave propagating through the ionosphere undergoes a progressive rotation of the plane of polarization;

k) dispersion, which results in a differential time delay across the bandwidth of the transmitted signal;

l) excess time delay;

m) ionospheric scintillation: inhomogeneities of electron density in the ionosphere cause refractive focusing or defocusing of radio waves and lead to amplitude fluctuations termed scintillations. Ionospheric scintillation is maximum near the geomagnetic equator and smallest in the mid-latitude regions. The auroral zones are also regions of large scintillation. Strong scintillation is Rayleigh distributed in amplitude; weaker scintillation is nearly log-normal. These fluctuations decrease with increasing frequency and depend upon path geometry, location, season, solar activity and local time. Table 2 tabulates fade depth data for VHF and UHF in mid-latitudes, based on data in Recommendation ITU-R P.531.

Accompanying the amplitude fluctuation is also a phase fluctuation. The spectral density of the phase fluctuation is proportional to $1/f^3$, where f is the Fourier frequency of the fluctuation. This spectral characteristic is similar to that arising from flicker of frequency in oscillators and can cause significant degradation to the performance of receiver hardware.

This Annex deals only with the effects of the troposphere on the wanted signal in relation to system planning. Interference aspects are treated in separate Recommendations:

– interference between earth stations and terrestrial stations (Recommendation ITU-R P.452);

– interference from and to space stations (Recommendation ITU-R P.619);

– bidirectional coordination of earth stations (Recommendation ITU-R P.1412).

An apparent exception is path depolarization which, although of concern only from the standpoint of interference (e.g. between orthogonally-polarized signal transmissions), is directly related to the propagation impairments of the co-polarized direct signal.

The information is arranged according to the link parameters to be considered in actual system planning, rather than according to the physical phenomena causing the different effects. As far as possible, simple prediction methods covering practical applications are provided, along with indications of their range of validity. These relatively simple methods yield satisfactory results in most practical applications, despite the large variability (from year to year and from location to location) of propagation conditions.

As far as possible, the prediction methods in this Annex have been tested against measured data from the data banks of Radiocommunication Study Group 3 (see Recommendation ITU-R P.311).

2 Propagation loss

The propagation loss on an Earth-space path, relative to the free-space loss, is the sum of different contributions as follows:

– attenuation by atmospheric gases;

– attenuation by rain, other precipitation and clouds;

– focusing and defocusing;

– decrease in antenna gain due to wave-front incoherence;

– scintillation and multipath effects;

– attenuation by sand and dust storms.

TABLE 1

Estimated* ionospheric effects for elevation angles of about 30° one-way traversal**
(derived from Recommendation ITU-R P.531)

Effect	Frequency dependence	0.1 GHz	0.25 GHz	0.5 GHz	1 GHz	3 GHz	10 GHz
Faraday rotation	$1/f^2$	30 rotations	4.8 rotations	1.2 rotations	108°	12°	1.1°
Propagation delay	$1/f^2$	25 μs	4 μs	1 μs	0.25 μs	0.028 μs	0.0025 μs
Refraction	$1/f^2$	< 1°	< 0.16°	< 2.4′	< 0.6′	< 4.2″	< 0.36″
Variation in the direction of arrival (r.m.s.)	$1/f^2$	20′	3.2′	48″	12″	1.32″	0.12″
Absorption (auroral and/or polar cap)	$\approx 1/f^2$	5 dB	0.8 dB	0.2 dB	0.05 dB	6×10^{-3} dB	5×10^{-4} dB
Absorption (mid-latitude)	$1/f^2$	< 1 dB	< 0.16 dB	< 0.04 dB	< 0.01 dB	< 0.001 dB	$< 1 \times 10^{-4}$ dB
Dispersion	$1/f^3$	0.4 ps/Hz	0.026 ps/Hz	0.0032 ps/Hz	0.0004 ps/Hz	1.5×10^{-5} ps/Hz	4×10^{-7} ps/Hz
Scintillation(1)	See Rec. ITU-R P.531	See Rec. ITU-R P.531	See Rec. ITU-R P.531	See Rec. ITU-R P.531	> 20 dB peak-to-peak	≈ 10 dB peak-to-peak	≈ 4 dB peak-to-peak

* This estimate is based on a TEC of 10^{18} electrons/m^2, which is a high value of TEC encountered at low latitudes in daytime with high solar activity

** Ionospheric effects above 10 GHz are negligible.

(1) Values observed near the geomagnetic equator during the early night-time hours (local time) at equinox under conditions of high sunspot number.

TABLE 2

Distribution of mid-latitude fade depths due to ionospheric scintillation (dB)

Percentage of time (%)	Frequency (GHz)			
	0.1	**0.2**	**0.5**	**1**
1	5.9	1.5	0.2	0.1
0.5	9.3	2.3	0.4	0.1
0.2	16.6	4.2	0.7	0.2
0.1	25	6.2	1	0.3

Each of these contributions has its own characteristics as a function of frequency, geographic location and elevation angle. As a rule, at elevation angles above 10°, only gaseous attenuation, rain and cloud attenuation and possibly scintillation will be significant, depending on propagation conditions. For non-GSO systems, the variation in elevation angle should be included in the calculations, as described in § 8.

(In certain climatic zones, snow and ice accumulations on the surfaces of antenna reflectors and feeds can produce prolonged periods with severe attenuation, which might dominate even the annual cumulative distribution of attenuation.)

2.1 Attenuation due to atmospheric gases

Attenuation by atmospheric gases which is entirely caused by absorption depends mainly on frequency, elevation angle, altitude above sea level and water vapour density (absolute humidity). At frequencies below 10 GHz, it may normally be neglected. Its importance increases with frequency above 10 GHz, especially for low elevation angles. Annex 1 of Recommendation ITU-R P.676 gives a complete method for calculating gaseous attenuation, while Annex 2 of the same Recommendation gives an approximate method for frequencies up to 350 GHz.

At a given frequency the oxygen contribution to atmospheric absorption is relatively constant. However, both water vapour density and its vertical profile are quite variable. Typically, the maximum gaseous attenuation occurs during the season of maximum rainfall (see Recommendation ITU-R P.836).

2.2 Attenuation by precipitation and clouds

2.2.1 Prediction of attenuation statistics for an average year

The general method to predict attenuation due to precipitation and clouds along a slant propagation path is presented in § 2.2.1.1.

If reliable long-term statistical attenuation data are available that were measured at an elevation angle and a frequency (or frequencies) different from those for which a prediction is needed, it is often preferable to scale these data to the elevation angle and frequency in question rather than using the general method. The recommended frequency-scaling method is found in § 2.2.1.2.

Site diversity effects may be estimated with the method of § 2.2.4.

2.2.1.1 Calculation of long-term rain attenuation statistics from point rainfall rate

The following procedure provides estimates of the long-term statistics of the slant-path rain attenuation at a given location for frequencies up to 55 GHz. The following parameters are required:

$R_{0.01}$: point rainfall rate for the location for 0.01% of an average year (mm/h)

h_s: height above mean sea level of the earth station (km)

θ: elevation angle (degrees)

φ: latitude of the earth station (degrees)

f: frequency (GHz)

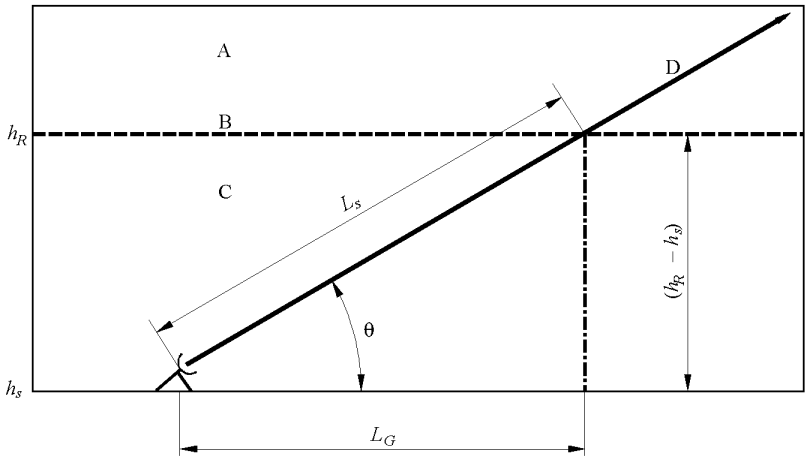
R_e: effective radius of the Earth (8 500 km).

If local data for the earth station height above mean sea level is not available, an estimate can be obtained from the maps of topographic altitude given in Recommendation ITU-R P.1511.

The geometry is illustrated in Fig. 1.

FIGURE 1

Schematic presentation of an Earth-space path giving the parameters to be input into the attenuation prediction process



A: frozen precipitation
B: rain height
C: liquid precipitation
D: Earth-space path

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Step 1: Determine the rain height, h_R, as given in Recommendation ITU-R P.839.

Step 2: For $\theta \geq 5°$ compute the slant-path length, L_s, below the rain height from:

$$L_s = \frac{(h_R - h_s)}{\sin\theta} \quad \text{km} \tag{1}$$

For $\theta < 5°$, the following formula is used:

$$L_s = \frac{2(h_R - h_s)}{\left(\sin^2\theta + \frac{2(h_R - h_s)}{R_e}\right)^{1/2} + \sin\theta} \quad \text{km} \tag{2}$$

If $h_R - h_s$ is less than or equal to zero, the predicted rain attenuation for any time percentage is zero and the following steps are not required.

Step 3: Calculate the horizontal projection, L_G, of the slant-path length from:

$$L_G = L_s \cos\theta \quad \text{km} \tag{3}$$

Step 4: Obtain the rainfall rate, $R_{0.01}$, exceeded for 0.01% of an average year (with an integration time of 1 min). If this long-term statistic cannot be obtained from local data sources, an estimate can be obtained from the maps of rainfall rate given in Recommendation ITU-R P.837. If $R_{0.01}$ is equal to zero, the predicted rain attenuation is zero for any time percentage and the following steps are not required.

Step 5: Obtain the specific attenuation, γ_R, using the frequency-dependent coefficients given in Recommendation ITU-R P.838 and the rainfall rate, $R_{0.01}$, determined from Step 4, by using:

$$\gamma_R = k\,(R_{0.01})^{\alpha} \quad \text{dB/km} \tag{4}$$

Step 6: Calculate the horizontal reduction factor, $r_{0.01}$, for 0.01% of the time:

$$r_{0.01} = \frac{1}{1 + 0.78\sqrt{\frac{L_G\,\gamma_R}{f}} - 0.38\left(1 - e^{-2L_G}\right)} \tag{5}$$

Step 7: Calculate the vertical adjustment factor, $v_{0.01}$, for 0.01% of the time:

$$\zeta = \tan^{-1}\left(\frac{h_R - h_s}{L_G\,r_{0.01}}\right) \quad \text{degrees}$$

For $\zeta > \theta$,

$$L_R = \frac{L_G\,r_{0.01}}{\cos\theta} \quad \text{km}$$

Else,

$$L_R = \frac{(h_R - h_s)}{\sin\theta} \quad \text{km}$$

If $|\varphi| < 36°$,

$$\chi = 36 - |\varphi| \quad \text{degrees}$$

Else,

$$\chi = 0 \quad \text{degrees}$$

$$v_{0.01} = \frac{1}{1 + \sqrt{\sin\theta}\left(31\left(1 - e^{-(\theta/(1+\chi))}\right)\frac{\sqrt{L_R\,\gamma_R}}{f^2} - 0.45\right)}$$

Step 8: The effective path length is:

$$L_E = L_R\,v_{0.01} \quad \text{km} \tag{6}$$

Step 9: The predicted attenuation exceeded for 0.01% of an average year is obtained from:

$$A_{0.01} = \gamma_R L_E \quad \text{dB} \tag{7}$$

Step 10: The estimated attenuation to be exceeded for other percentages of an average year, in the range 0.001% to 5%, is determined from the attenuation to be exceeded for 0.01% for an average year:

If $p \geq 1\%$ or $|\varphi| \geq 36°$: $\beta = 0$

If $p < 1\%$ and $|\varphi| < 36°$ and $\theta \geq 25°$: $\beta = -0.005(|\varphi| - 36)$

Otherwise: $\beta = -0.005(|\varphi| - 36) + 1.8 - 4.25 \sin\theta$

$$A_p = A_{0.01}\left(\frac{p}{0.01}\right)^{-(0.655 + 0.033 \ln(p) - 0.045 \ln(A_{0.01}) - \beta(1-p)\sin\theta)} \quad \text{dB} \tag{8}$$

This method provides an estimate of the long-term statistics of attenuation due to rain. When comparing measured statistics with the prediction, allowance should be given for the rather large year-to-year variability in rainfall rate statistics (see Recommendation ITU-R P.678).

2.2.1.2 Long-term frequency and polarization scaling of rain attenuation statistics

The method of § 2.2.1.1 may be used to investigate the dependence of attenuation statistics on elevation angle, polarization and frequency, and is therefore a useful general tool for scaling of attenuation according to these parameters.

If reliable attenuation data measured at one frequency are available, the following empirical formula giving an attenuation ratio directly as a function of frequency and attenuation may be applied for frequency scaling on the same path in the frequency range 7 to 55 GHz:

$$A_2 = A_1 (\varphi_2 / \varphi_1)^{1 - H(\varphi_1, \varphi_2, A_1)} \tag{9}$$

where:

$$\varphi(f) = \frac{f^2}{1 + 10^{-4} f^2} \tag{10a}$$

$$H(\varphi_1, \varphi_2, A_1) = 1.12 \times 10^{-3} (\varphi_2 / \varphi_1)^{0.5} (\varphi_1 A_1)^{0.55} \tag{10b}$$

A_1 and A_2 are the equiprobable values of the excess rain attenuation at frequencies f_1 and f_2 (GHz), respectively.

Frequency scaling from reliable attenuation data is preferred, when applicable, rather than the prediction methods starting from rain data.

When polarization scaling is required, it is more appropriate to use directly the parameters k and α as given in Recommendation ITU-R P.838. These parameters also provide a radiometeorological basis for frequency scaling.

2.2.2 Seasonal variations – worst month

System planning often requires the attenuation value exceeded for a time percentage, p_w, of the worst month. The following procedure is used to estimate the attenuation exceeded for a specified percentage of the worst month.

Step 1: Obtain the annual time percentage, p, corresponding to the desired worst-month time percentage, p_w, by using the equation specified in Recommendation ITU-R P.841 and by applying any adjustments to p as prescribed therein.

Step 2: For the path in question obtain the attenuation, A (dB), exceeded for the resulting annual time percentage, p, from the method of § 2.2.1.1, or from measured or frequency-scaled attenuation statistics. This value of A is the estimated attenuation for p_w per cent of the worst month.

Curves giving the variation of worst-month values from their mean are provided in Recommendation ITU-R P.678.

2.2.3 Variability in space and time of statistics

Precipitation attenuation distributions measured on the same path at the same frequency and polarization may show marked year-to-year variations. In the range 0.001% to 0.1% of the year, the attenuation values at a fixed probability level are observed to vary by more than 20% r.m.s. When the models for attenuation prediction or scaling in § 2.2.1 are used to scale observations at a location to estimate for another path at the same location, the variations increase to more than 25% r.m.s.

2.2.4 Site diversity

Intense rain cells that cause large attenuation values on an Earth-space link often have horizontal dimensions of no more than a few kilometres. Diversity systems able to re-route traffic to alternate earth stations, or with access to a satellite with extra on-board resources available for temporary allocation, can improve the system reliability considerably.

Two concepts exist for characterizing diversity performance: the diversity improvement factor is defined as the ratio of the single-site time percentage and the diversity time percentage, at the same attenuation level. Diversity gain is the difference (dB) between the single-site and diversity attenuation values for the same time percentage. Both parameters are important, depending on the system design approach, and prediction procedures for both are given below.

The procedures have been tested at frequencies between 10 and 30 GHz, which is the recommended frequency range of applicability. The diversity prediction procedures are only recommended for time percentages less than 0.1%. At time percentages above 0.1%, the rainfall rate is generally small and the corresponding site diversity improvement is not significant.

2.2.4.1 Diversity improvement factor

The diversity improvement factor, I, is given by:

$$I = \frac{p_1}{p_2} = \frac{1}{(1+\beta^2)}\left(1+\frac{100\,\beta^2}{p_1}\right) \approx 1+\frac{100\,\beta^2}{p_1} \qquad (11)$$

where p_1 and p_2 are the respective single-site and diversity time percentages, and β is a parameter depending on link characteristics. The approximation on the right-hand side of equation (11) is acceptable since β^2 is generally small.

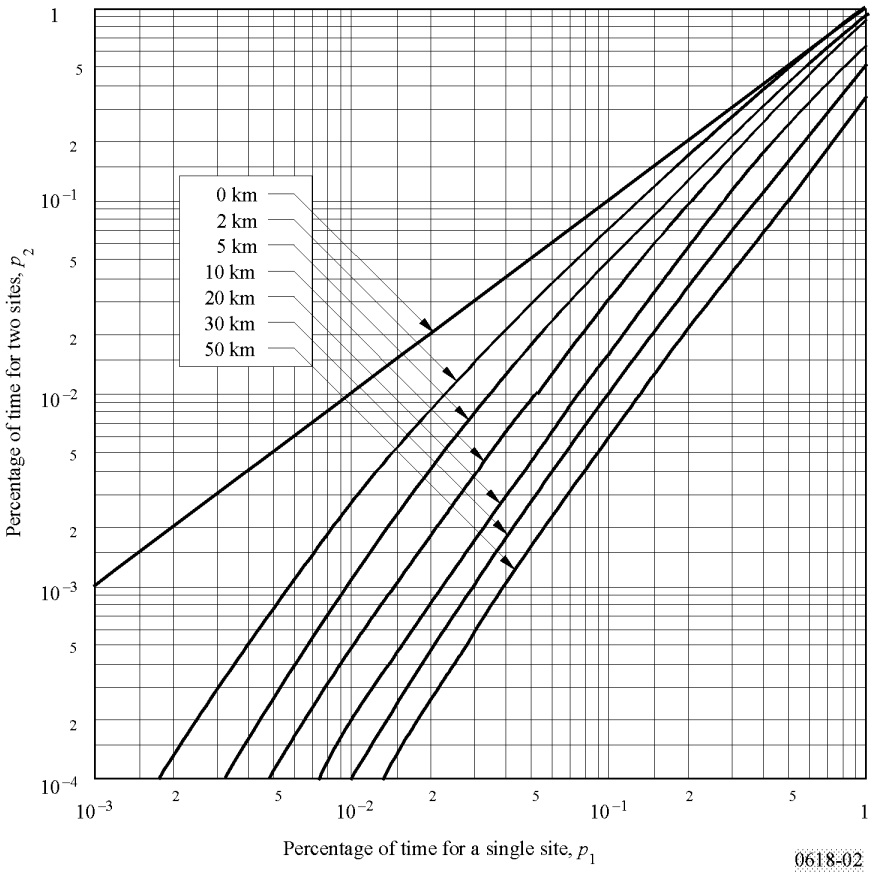
From a large number of measurements carried out in the 10-20 GHz band, and mainly between 11 GHz and 13.6 GHz, it has been found that the value of β^2 depends basically on the distance, d, between the stations, and only slightly on the angle of elevation and the frequency. It is found that β^2 can be expressed by the following empirical relationship:

$$\beta^2 = 10^{-4} d^{1.33} \tag{12}$$

Figure 2 shows p_2 versus p_1 on the basis of equations (11) and (12).

FIGURE 2

Relationship between percentages of time with and without diversity for the same attenuation (Earth-satellite paths)



2.2.4.2 Diversity gain

The diversity gain, G (dB), between pairs of sites is calculated with the empirical expression given below. Parameters required for the calculation of diversity gain are:

d: separation (km) between the two sites

A: path rain attenuation (dB) for a single site

f: frequency (GHz)

θ: path elevation angle (degrees)

ψ: angle (degrees) made by the azimuth of the propagation path with respect to the baseline between sites, chosen such that $\psi \leq 90°$.

Step 1: Calculate the gain contributed by the spatial separation from:

$$G_d = a\left(1 - e^{-bd}\right) \tag{13}$$

where:

$$a = 0.78\,A - 1.94\left(1 - e^{-0.11A}\right)$$

$$b = 0.59\left(1 - e^{-0.1A}\right)$$

Step 2: Calculate the frequency-dependent gain from:

$$G_f = e^{-0.025f} \tag{14}$$

Step 3: Calculate the gain term dependent on elevation angle from:

$$G_\theta = 1 + 0.006\,\theta \tag{15}$$

Step 4: Calculate the baseline-dependent term from the expression:

$$G_\psi = 1 + 0.002\,\psi \tag{16}$$

Step 5: Compute the net diversity gain as the product:

$$G = G_d \cdot G_f \cdot G_\theta \cdot G_\psi \quad \text{dB} \tag{17}$$

When the above method was tested against the Radiocommunication Study Group 3 site diversity data bank, the arithmetic mean and standard deviation were found to be 0.14 dB and 0.96 dB, respectively, with an r.m.s. error of 0.97 dB.

2.2.5 Characteristics of precipitation events

2.2.5.1 Durations of individual fades

The durations of rain fades that exceed a specified attenuation level are approximately log-normally distributed. Median durations are of the order of several minutes. No significant dependence of these distributions on fade depth is evident in most measurements for fades of less than 20 dB, implying that the larger total time percentage of fades observed at lower fade levels or at higher frequencies is composed of a larger number of individual fades having more or less the same distribution of durations. Significant departures from log-normal seem to occur for fade durations of less than about half a minute. Fade durations at a specified fade level tend to increase with decreasing elevation angle.

For the planning of integrated services digital network (ISDN) connections via satellite, data are needed on the contribution of attenuation events shorter than 10 s to the total fading time. This information is especially relevant for the attenuation level corresponding to the outage threshold, where events longer than 10 s contribute to system unavailable time, while shorter events affect system performance during available time (see Recommendation ITU-R S.579). Existing data

indicate that in the majority of cases, the exceedance time during available time is 2% to 10% of the net exceedance time. However, at low elevation angles where the short period signal fluctuations due to tropospheric scintillation become statistically significant, there are some cases for which the exceedance time during available time is far larger than in the case at higher elevation Earth-space paths.

2.2.5.2 Rates of change of attenuation (fading rate)

There is broad agreement that the distributions of positive and negative fade rates are log-normally distributed and very similar to each other. The dependence of fade rate on fade depth has not been established.

2.2.5.3 Correlation of instantaneous values of attenuation at different frequencies

Data on the instantaneous ratio of rain attenuation values at different frequencies are of interest for a variety of adaptive fade techniques. The frequency-scaling ratio has been found to be log-normally distributed, and is influenced by rain type and rain temperature. Data reveal that the short-term variations in the attenuation ratio can be significant, and are expected to increase with decreasing path elevation angle.

2.3 Clear-air effects

Other than atmospheric absorption, clear-air effects in the absence of precipitation are unlikely to produce serious fading in space telecommunication systems operating at frequencies below about 10 GHz and at elevation angles above 10°. At low elevation angles ($\leq 10°$) and at frequencies above about 10 GHz, however, tropospheric scintillations can on occasion cause serious degradations in performance. At very low elevation angles ($\leq 4°$ on inland paths, and $\leq 5°$ on overwater or coastal paths), fading due to multipath propagation effects can be particularly severe. At some locations, ionospheric scintillation may be important at frequencies below about 6 GHz (see Recommendation ITU-R P.531).

2.3.1 Decrease in antenna gain due to wave-front incoherence

Incoherence of the wave-front of a wave incident on a receiving antenna is caused by small-scale irregularities in the refractive index structure of the atmosphere. Apart from the rapid signal fluctuations discussed in § 2.4, they cause an antenna-to-medium coupling loss that can be described as a decrease of the antenna gain.

This effect increases both with increasing frequency and decreasing elevation angle, and is a function of antenna diameter. Although not explicitly accounted for in the refraction models presented below, this effect is negligible in comparison.

2.3.2 Beam spreading loss

The regular decrease of refractive index with height causes ray-bending and hence a defocusing effect at low angles of elevation (Recommendation ITU-R P.834). The magnitude of the defocusing loss of the antenna beam is independent of frequency, over the range of 1-100 GHz.

The loss A_{bs} due to beam spreading in regular refractive conditions can be ignored at elevation angles above about 3° at latitudes less than 53° and above about 6° at higher latitudes.

At all latitudes, the beam spreading loss in the average year at elevation angles less than 5° is estimated from:

$$A_{bs} = 2.27 - 1.16 \log (1 + \theta_0) \quad \text{dB} \quad \text{for } A_{bs} > 0 \tag{18}$$

where θ_0 is the apparent elevation angle (mrad) taking into account the effects of refraction. The beam spreading loss in the average worst month at latitudes less than 53° is also estimated from equation (18).

At latitudes greater than 60°, the beam spreading loss at elevation angles less than 6° in the average worst month is estimated from:

$$A_{bs} = 13 - 6.4 \log (1 + \theta_0) \quad \text{dB} \quad \text{for } A_{bs} > 0 \tag{19}$$

At latitudes ψ between 53° and 60°, the median beam spreading loss can be estimated by a linear interpolation between the values obtained from equation (18) (designated A_{bs} (< 53°)) and equation (19) (designated A_{bs} (> 60°)) as follows:

$$A_{bs} = A_{bs} \ (> 60°) - \frac{60}{7} \Delta A_{bs} + \frac{1}{7} \Delta A_{bs} \ \psi \quad \text{dB} \tag{20}$$

where $\Delta A_{bs} = A_{bs} \ (> 60°) - A_{bs} \ (< 53°)$.

2.4 Scintillation and multipath fading

The magnitude of tropospheric scintillations depends on the magnitude and structure of the refractive index variations, increasing with frequency and with the path length through the medium, and decreasing as the antenna beamwidth decreases because of aperture averaging. Monthly-averaged r.m.s. fluctuations are well-correlated with the wet term of the radio refractivity, N_{wet}, which depends on the water vapour content of the atmosphere. N_{wet} may be estimated for periods of a month or longer from meteorological data obtained at the surface.

At very small percentages of time, or conversely large fade depths (greater than about 10 dB), the fading at very low elevation angles (≤4°, and ≤5° for links over water or in coastal areas) is observed to be more severe than that predicted due to scintillation. The fading is also observed to have a character similar to multipath fading on terrestrial links. Like the distribution on terrestrial links, the distribution for very-low-angle satellite links also appears correlated with refractivity gradient statistics. The overall fading distribution shows a gradual transition from a scintillation distribution at large exceedance percentages to a multipath fading distribution (with a slope of 10 dB/decade) at small percentages. The methods in § 2.4.2 and 2.4.3, for the deep fading and shallow fading portions of the overall distribution, respectively, use the refractivity gradient statistic p_L for describing climatic variations in the distribution.

For overwater and coastal paths with elevation angles in the 4° to 5° range, the methods of § 2.4.2 and 2.4.3 should be applied as well as the method of § 2.4.1, and the one giving the largest fade depths then employed in estimates of path fading statistics.

The net fade distribution due to tropospheric refractive effects, $A_{ref}(p)$, is the combination of the beam spreading, scintillation, and multipath-fading effects described above. Tropospheric and ionospheric scintillation distributions may be combined by summing the respective time percentages that specified fade levels are exceeded.

2.4.1 Calculation of monthly and long-term statistics of amplitude scintillations at elevation angles greater than 4°

A general technique for predicting the cumulative distribution of tropospheric scintillation at elevation angles greater than 4° is given below. It is based on monthly or longer averages of temperature t (°C) and relative humidity H, and reflects the specific climatic conditions of the site. As the averages of t and H vary with season, distributions of scintillation fade depth exhibit seasonal variations, which may also be predicted by using seasonal averages of t and H in the method. Values of t and H may be obtained from weather information for the site(s) in question.

The procedure has been tested at frequencies between 7 and 14 GHz, but is recommended for applications up to at least 20 GHz.

Parameters required for the method include:

t: average surface ambient temperature (°C) at the site for a period of one month or longer

H: average surface relative humidity (%) at the site for a period of one month or longer

(NOTE 1 – If no experimental data are available for t and H, the maps of N_{wet} in Recommendation ITU-R P.453 may be used.)

f: frequency (GHz), where 4 GHz $\leq f \leq$ 20 GHz

θ: path elevation angle, where $\theta \geq 4°$

D: physical diameter (m) of the earth-station antenna

η: antenna efficiency; if unknown, $\eta = 0.5$ is a conservative estimate.

Step 1: For the value of t, calculate the saturation water vapour pressure, e_s, (hPa), as specified in Recommendation ITU-R P.453.

Step 2: Compute the wet term of the radio refractivity, N_{wet}, corresponding to e_s, t and H as given in Recommendation ITU-R P.453. (Steps 1 and 2 are not needed if N_{wet} is obtained directly from Recommendation ITU-R P.453.)

Step 3: Calculate the standard deviation of the signal amplitude, σ_{ref}, used as reference:

$$\sigma_{ref} = 3.6 \times 10^{-3} + 10^{-4} \times N_{wet} \quad \text{dB} \tag{21}$$

Step 4: Calculate the effective path length L according to:

$$L = \frac{2h_L}{\sqrt{\sin^2 \theta + 2.35 \times 10^{-4}} + \sin\theta} \quad \text{m} \tag{22}$$

where h_L is the height of the turbulent layer; the value to be used is h_L = 1 000 m.

Step 5: Estimate the effective antenna diameter, D_{eff}, from the geometrical diameter, D, and the antenna efficiency η:

$$D_{eff} = \sqrt{\eta}\, D \qquad \text{m} \tag{23}$$

Step 6: Calculate the antenna averaging factor from:

$$g(x) = \sqrt{3.86\,(x^2+1)^{11/12} \cdot \sin\left[\frac{11}{6}\arctan\frac{1}{x}\right] - 7.08\,x^{5/6}} \tag{24}$$

with:

$$x = 1.22\, D_{eff}^2\,(f/L)$$

where f is the carrier frequency (GHz).

If the argument of the square root is negative (i.e. when $x \geq 7.0$), the predicted scintillation fade depth for any time percentage is zero and the following steps are not required.

Step 7: Calculate the standard deviation of the signal for the considered period and propagation path:

$$\sigma = \sigma_{ref}\; f^{7/12}\; \frac{g(x)}{(\sin\theta)^{1.2}} \tag{25}$$

Step 8: Calculate the time percentage factor, $a(p)$, for the time percentage, p, of concern in the range $0.01 < p \leq 50$:

$$a(p) = -0.061\,(\log_{10} p)^3 + 0.072\,(\log_{10} p)^2 - 1.71\log_{10} p + 3.0 \tag{26}$$

Step 9: Calculate the scintillation fade depth for the time percentage p by:

$$A_s(p) = a(p) \cdot \sigma \qquad \text{dB} \tag{27}$$

2.4.2 Calculation of the deep fading part of the scintillation/multipath fading distribution of elevation angles less than 5°

This method estimates the large fade depth range (typically fades larger than about 25 dB) of the combined beam spreading, scintillation and multipath fading distribution of A_{ref} in the average worst month and average year (predictions for the average year being derived from those for the average worst month). The method also serves as a basis for the interpolation procedure given in § 2.4.3 for predicting the shallow fading range of the distribution. The step-by-step procedure is as follows:

Step 1: Obtain the apparent boresight elevation angle θ_0 (mrad) (taking account of the effects of refraction) for the path location in question (see Recommendation ITU-R P.834).

Step 2: For the path location in question, obtain the geoclimatic factor, K_w, applicable for the average worst month from:

$$K_w = 10^{0.1\left(C_0 + C_{Lat}\right)}\, p_L^{1.5} \tag{28}$$

The variable p_L is the percentage of time that the refractivity gradient in the lowest 100 m of the atmosphere is less than –100 N units/km in that month having the highest value of p_L from the four seasonally representative months of February, May, August and November for which maps are given in Figs. 8 to 11 of Recommendation ITU-R P.453.

As an exception, only the maps for May and August should be used for latitudes greater than 60° N or 60° S.

The values of the coefficient C_0 in equation (28) and the conditions for their applicability are summarized in Table 3. The coefficient C_{Lat} of latitude ψ (in °N or °S) is given by:

$$C_{Lat} = 0 \qquad \text{for} \qquad 53° \text{ S} \geq \psi \leq 53° \text{ N} \tag{29}$$

$$C_{Lat} = -53 + \psi \qquad \text{for} \quad 53° \text{ N or S} < \psi < 60° \text{ N or S} \tag{30}$$

$$C_{Lat} = 7 \qquad \text{for} \qquad \psi \geq 60° \text{ N or S} \tag{31}$$

TABLE 3

Values of the coefficient C_0 in equation (28) for various types of propagation path

Type of path	C_0
Propagation paths[1] entirely over land for which the earth-station antenna is less than 700 m above mean sea level[2]	76
Propagation paths for which the earth-station antenna is higher than 700 m above mean sea level	70
Propagation paths entirely or partially over water or coastal areas beside such bodies of water (see[1] for definition of propagation path, coastal areas, and definition of r)	$76 + 6r$

(1) The propagation path is the lowest portion of the Earth-space path over which the relevant tropospheric fading mechanisms are believed to occur. The approximate length of the propagation path is given by:

$$d_{eff} = 14\,000(1 + \theta_0)^{-1.3} \qquad \text{km} \qquad d_{eff} \leq 300 \text{ km} \tag{32}$$

where θ_0 is the boresight elevation angle (mrad).

The propagation path is considered to be crossing a coastal area if a section of the path profile (i.e. the profile of terrain altitudes over a distance along the path equal to that given by equation (32)) is less than 100 m above mean sea level (or the mean level of large inland bodies of water) or within 50 km of the coastline, and if there is no height of land above 100 m altitude between the propagation path and the coast.

The variable r in the expression for C_0 is the fraction of the propagation path that crosses a body of water or adjacent coastal areas.

(2) Propagation paths passing over a small lake or river are classed as being entirely over land. Although such bodies of water could be included in the calculation of r, this yields negligible increases in the value of the coefficient C_0 from the overland non-coastal values.

Step 3: Calculate the percentage of time that fade depth A_{ref} (dB) is exceeded in the average worst month from the power-law expression:

$$p = K_w \, f^{0.9} (1 + \theta_0)^{-5.5} \times 10^{-A_{ref}/10} \qquad \% \tag{33}$$

Alternatively, calculate the fade depth, A_{ref}, exceeded for p% of the time at frequency, f, in the average worst month from:

$$A_{ref} = G_w + 92 + 9 \log f - 55 \log (1 + \theta_0) - 10 \log p \quad \text{dB} \tag{34}$$

where G_w is the logarithmic geoclimatic factor for the average worst month given by:

$$G_w = 10 \log K_w - 92 \quad \text{dB} \tag{35}$$

Step 4: Calculate the percentage of time that fade depth A_{ref} (dB) is exceeded in the average year from equation (33), with K_w replaced by K_a, where:

$$K_a = K_w \times 10^{-0.1 \Delta G} \tag{36}$$

with:

$$\Delta G = -1.8 - 5.6 \log \left(1.1 \pm |\cos 2\psi|^{0.7} \right) + 4.5 \log (1 + \theta_0) \quad \text{dB} \tag{37}$$

The positive sign in equation (37) is employed for latitude $\psi \leq 45$ (°N or °S) and the negative sign for $\psi > 45°$. Alternatively, calculate the fade depth A_{ref} exceeded for p% of the time at frequency f in the average year from equation (34), with G_w replaced by $G_a = G_w - \Delta G$.

Equations (33) and (34) are valid for A_{ref} greater than about 25 dB. They were developed from data in the frequency range 6-38 GHz and elevation angles in the range of 1° to 4°. They are expected to be valid at least in the frequency range 1-45 GHz and elevation angles in the range of 0.5° to 5°.

2.4.3 Calculation of the shallow fading part of the scintillation/multipath fading distribution at elevation angles less than 5°

Step 1: Estimate the fade depth $A_{ref}(63\%)$ exceeded for 63% of the average worst month or average year (denoted A_{63}) as desired, as follows: at latitudes greater than 60° in the average worst month, use:

$$A_{63} = 9.4 - 4.5 \log (1 + \theta_0) \quad \text{dB} \quad \text{for } A_{bs} > 0 \tag{38}$$

where θ_0 is again the apparent elevation angle (mrad). At latitudes less than 53°, use the expression in equation (18). At latitudes between 53° and 60°, carry out a linear interpolation as in equation (20). For average-year calculations, use equation (18) for all latitudes.

Step 2: For average-worst-month predictions, calculate the percentage of time p_t that fade depth of $A_t = 25$ dB is exceeded in the multipath tail of the distribution using equation (33). For average year predictions, replace K_w in equation (33) by K_a in equation (36) for this calculation.

Step 3: Calculate the new percentage of time p from:

$$p = 10^{-0.1 A_{63} + \log p_t} \quad \% \tag{39}$$

Step 4: Calculate the value of the parameter q' corresponding to the fade depth A_t and percentage of time p from:

$$q' = -\frac{20}{A_t}\log_{10}\left[-\ln\left(\frac{100-p}{100}\right)\right] \tag{40}$$

Step 5: Calculate the values of the shape factor q_t from:

$$q_t = (q'-2)/\left[\left(1+0.3\times10^{-A_t/20}\right)\times10^{-0.016\,A_t}\right] - s_0\left(10^{-A_t/20} + A_t/800\right) \tag{41}$$

where:

$$s_0 = -1.6 - 3.2\log f + 4.2\log(1+\theta_0) \tag{42}$$

with:

f: frequency (GHz)

θ_0: apparent elevation angle (mrad).

Step 6: If $q_t < 0$, repeat Steps 2 to 5 for $A_t = 35$ dB to obtain the definitive value of q_t.

Step 7: For $A_{63} < A_{ref}(p) < 25 + A_{63}$ dB or $A_{63} < A_{ref}(p) < 35 + A_{63}$ dB, depending on the value required for A_t, calculate the percentage of time p that A_{ref} is exceeded using the following:

$$p = 100\left[1-\exp\left(-10^{-q(A_{ref}-A_{63})/20}\right)\right] \quad \% \tag{43}$$

where q is also a function of A_{ref} and is given by:

$$q = 2 + 10^{-0.016(A_{ref}-A_{63})}\left[1+0.3\times10^{-(A_{ref}-A_{63})/20}\right]\cdot\left[q_t + s_0\left(10^{-(A_{ref}-A_{63})/20} + (A_{ref}-A_{63})/800\right)\right] \tag{44}$$

Here the value of the parameter q_t is that obtained in Step 5 or 6, as appropriate.

For $A_{ref} \geq 25 + A_{63}$ dB or $A_{ref} \geq 35 + A_{63}$ dB, depending on the value required for A_t, calculate the percentage of time p that A_{ref} is exceeded from equation (33).

Step 8: For $A_{ref}(p) < A_{ref}(63\%)$, and for the enhancement range of the distribution, the enhancement relative to $A_{ref}(63\%)$ is expressed as:

$$E_{ref}(p_e) = A_{ref}(63\%) - A_{ref}(p) \quad \text{dB} \tag{45}$$

This enhancement, exceeded for percentages p_e of the time (not exceeded for $p = 100 - p_e\%$ of the time), can be approximated using the method of § 2.3.3 of Recommendation ITU-R P.530:

– In applying this method for the average worst month, the calculation of the fade depth $A_{0.01}$ exceeded for 0.01% of the average worst month should be obtained using equation (34) in place of the equations for terrestrial links.

– In applying the method for the average year, equation (34) should be employed with G_w replaced by G_a as obtained in Step 4 following equation (34).

It should be noted that this method can underpredict the relative enhancement by up to 78% at $p_e = 10\%$ and 47% at $p_e = 1\%$. Reasonable accuracy is achieved for the small percentages $p_e < 0.1\%$ of greatest interest.

The method in Steps 1 to 7 is valid for values of q_t greater than –1.5, which covers virtually all the combined ranges of K, f and θ_0 most likely to arise under operational circumstances. For values of q_t less than –1.5, the method is not recommended. The method implicitly includes the beam-spreading loss discussed in § 2.3.2.

2.5 Estimation of total attenuation due to multiple sources of simultaneously occurring atmospheric attenuation

For systems operating at frequencies above about 18 GHz, and especially those operating with low elevation angles and/or margins, the effect of multiple sources of simultaneously occurring atmospheric attenuation must be considered.

Total attenuation (dB) represents the combined effect of rain, gas, clouds and scintillation and requires one or more of the following input parameters:

$A_R(p)$: attenuation due to rain for a fixed probability (dB), as estimated by A_p in equation (8)

$A_C(p)$: attenuation due to clouds for a fixed probability (dB), as estimated by Recommendation ITU-R P.840

$A_G(p)$: gaseous attenuation due to water vapour and oxygen for a fixed probability (dB), as estimated by Recommendation ITU-R P.676

$A_S(p)$: attenuation due to tropospheric scintillation for a fixed probability (dB), as estimated by equation (27)

where p is the probability of the attenuation being exceeded in the range 50% to 0.001%.

Gaseous attenuation as a function of percentage of time can be calculated using § 2.2 of Annex 2 of Recommendation ITU-R P.676 if local meteorological data at the required time percentage are available. In the absence of local data at the required time percentage, the mean gaseous attenuation should be calculated and used in equation (46).

A general method for calculating total attenuation for a given probability, $A_T(p)$, is given by:

$$A_T(p) = A_G(p) + \sqrt{(A_R(p) + A_C(p))^2 + A_S^2(p)} \quad (46)$$

where:

$$A_C(p) = A_C(1\%) \qquad \text{for } p < 1.0\% \quad (47)$$

$$A_G(p) = A_G(1\%) \qquad \text{for } p < 1.0\% \quad (48)$$

Equations (47) and (48) take account of the fact that a large part of the cloud attenuation and gaseous attenuation is already included in the rain attenuation prediction for time percentages below 1%.

When the complete prediction method above was tested using the procedure set out in Annex 1 to Recommendation ITU-R P.311, the results were found to be in good agreement with available measurement data for all latitudes and in the probability range 0.001% to 1%, with an overall r.m.s. error of about 35%, when used with the contour rain maps in Recommendation ITU-R P.837. When

tested against multi-year Earth-space data, the overall r.m.s. error was found to be about 25%. Due to the dominance of different effects at different probabilities as well as the inconsistent availability of test data at different probability levels, some variation of r.m.s. error occurs across the distribution of probabilities.

2.6 Attenuation by sand and dust storms

Very little is known about the effects of sand and dust storms on radio signals on slant-paths. Available data indicate that at frequencies below 30 GHz, high particle concentrations and/or high moisture contents are required to produce significant propagation effects.

3 Noise temperature

As attenuation increases, so does emission noise. For earth stations with low-noise front-ends, this increase of noise temperature may have a greater impact on the resulting signal-to-noise ratio than the attenuation itself.

The atmospheric contribution to antenna noise in a ground station may be estimated with the equation:

$$T_s = T_m \left(1 - 10^{-A/10}\right) \tag{49}$$

where:

T_s: sky-noise temperature (K) as seen by the antenna

A: path attenuation (dB)

T_m: effective temperature (K) of the medium.

The effective temperature is dependent on the contribution of scattering to attenuation and on the physical extent of clouds and rain cells on the vertical variation of the physical temperature of the scatterers and, to a lesser extent, on the antenna beamwidth. By comparing radiometric observations and simultaneous beacon attenuation measurements, the effective temperature of the medium has been determined to lie in the range 260-280 K for rain and clouds along the path at frequencies between 10 and 30 GHz.

When the attenuation is known, the following effective temperatures of the mediums may be used to obtain an upper limit to sky-noise temperature at frequencies below 60 GHz:

$T_m = 280$ K for clouds

$T_m = 260$ K for rain

The noise environments of stations on the surface of the Earth and in space are treated in detail in Recommendation ITU-R P.372.

For satellite telecommunication systems using the geostationary orbit, earth stations will find that the Sun and, to a lesser extent, the Moon, are significant noise sources at all frequencies and that the galactic background is a possibly significant consideration at frequencies below about 2 GHz (see Recommendation ITU-R P.372). In addition, contributions to the sky background noise temperature may be given by Cygnus A and X, Cassiopeia A, Taurus and the Crab nebula.

To determine the system noise temperature of earth stations from the brightness temperatures discussed above, the equations of Recommendation ITU-R P.372 may be used.

4 Cross-polarization effects

Frequency reuse by means of orthogonal polarizations is often used to increase the capacity of space telecommunication systems. This technique is restricted, however, by depolarization on atmospheric propagation paths. Various depolarization mechanisms, especially hydrometeor effects, are important in the troposphere.

Faraday rotation of the plane of polarization by the ionosphere is discussed in Recommendation ITU-R P.531. As much as 1° of rotation may be encountered at 10 GHz, and greater rotations at lower frequencies. As seen from the earth station, the planes of polarization rotate in the same direction on the up- and down-links. It is therefore not possible to compensate for Faraday rotation by rotating the feed system of the antenna, if the same antenna is used both for transmitting and receiving.

4.1 Calculation of long-term statistics of hydrometeor-induced cross-polarization

To calculate long-term statistics of depolarization from rain attenuation statistics the following parameters are needed:

A_p: rain attenuation (dB) exceeded for the required percentage of time, p, for the path in question, commonly called co-polar attenuation (CPA)

τ: tilt angle of the linearly polarized electric field vector with respect to the horizontal (for circular polarization use $\tau = 45°$)

f: frequency (GHz)

θ: path elevation angle (degrees).

The method described below to calculate cross-polarization discrimination (XPD) statistics from rain attenuation statistics for the same path is valid for $8 \leq f \leq 35$ GHz and $\theta \leq 60°$. The procedure for scaling to frequencies down to 4 GHz is given in § 4.3 (and see Step 8 below).

Step 1: Calculate the frequency-dependent term:

$$C_f = 30 \log f \qquad \text{for } 8 \leq f \leq 35 \text{ GHz} \tag{50}$$

Step 2: Calculate the rain attenuation dependent term:

$$C_A = V(f) \log A_p \tag{51}$$

where:

$$V(f) = 12.8 f^{0.19} \qquad \text{for } 8 \leq f \leq 20 \text{ GHz}$$

$$V(f) = 22.6 \qquad \text{for } 20 < f \leq 35 \text{ GHz}$$

Step 3: Calculate the polarization improvement factor:

$$C_\tau = -10 \log [1 - 0.484 (1 + \cos 4\tau)] \tag{52}$$

The improvement factor $C_\tau = 0$ for $\tau = 45°$ and reaches a maximum value of 15 dB for $\tau = 0°$ or 90°.

Step 4: Calculate the elevation angle-dependent term:

$$C_\theta = -40 \log (\cos \theta) \qquad \text{for } \theta \le 60° \tag{53}$$

Step 5: Calculate the canting angle dependent term:

$$C_\sigma = 0.0052\, \sigma^2 \tag{54}$$

σ is the effective standard deviation of the raindrop canting angle distribution, expressed in degrees; σ takes the value 0°, 5°, 10° and 15° for 1%, 0.1%, 0.01% and 0.001% of the time, respectively.

Step 6: Calculate rain XPD not exceeded for p% of the time:

$$XPD_{rain} = C_f - C_A + C_\tau + C_\theta + C_\sigma \qquad \text{dB} \tag{55}$$

Step 7: Calculate the ice crystal dependent term:

$$C_{ice} = XPD_{rain} \times (0.3 + 0.1 \log p)/2 \qquad \text{dB} \tag{56}$$

Step 8: Calculate the XPD not exceeded for p% of the time, including the effects of ice:

$$XPD_p = XPD_{rain} - C_{ice} \qquad \text{dB} \tag{57}$$

In this prediction method in the frequency band 4 to 6 GHz where path attenuation is low, A_p statistics are not very useful for predicting XPD statistics. For frequencies below 8 GHz, the frequency-scaling formula of § 4.3 can be used to scale cross-polarization statistics calculated for 8 GHz down to the 6 to 4 GHz band.

4.2 Joint statistics of XPD and attenuation

The conditional probability distribution of XPD for a given value of attenuation, A_p, can be modelled by assuming that the cross-polar to co-polar voltage ratio, $r = 10^{-XPD/20}$, is normally distributed. Parameters of the distribution are the mean value, r_m, which is very close to $10^{-XPD_{rain}/20}$, with XPD_{rain} given by equation (55), and the standard deviation, σ_r, which assumes the almost-constant value of 0.038 for 3 dB $\le A_p \le$ 8 dB.

4.3 Long-term frequency and polarization scaling of statistics of hydrometeor-induced cross-polarization

Long-term XPD statistics obtained at one frequency and polarization tilt angle can be scaled to another frequency and polarization tilt angle using the semi-empirical formula:

$$XPD_2 = XPD_1 - 20 \log \left[\frac{f_2 \sqrt{1 - 0.484\,(1 + \cos 4\,\tau_2)}}{f_1 \sqrt{1 - 0.484\,(1 + \cos 4\,\tau_1)}} \right] \qquad \text{for } 4 \le f_1, f_2 \le 30 \text{ GHz} \tag{58}$$

where XPD_1 and XPD_2 are the XPD values not exceeded for the same percentage of time at frequencies f_1 and f_2 and polarization tilt angles, τ_1 and τ_2, respectively.

Equation (58) is based on the same theoretical formulation as the prediction method of § 4.1, and can be used to scale XPD data that include the effects of both rain and ice depolarization, since it has been observed that both phenomena have approximately the same frequency dependence at frequencies less than about 30 GHz.

4.4 Data relevant to cross-polarization cancellation

Experiments have shown that a strong correlation exists between rain depolarization at 6 and 4 GHz on Earth-space paths, both on the long term and on an event basis, and uplink depolarization compensation utilizing concurrent down-link depolarization measurements appears feasible. Only differential phase effects were apparent, even for severe rain events, and single-parameter compensation (i.e. for differential phase) appears sufficient at 6 and 4 GHz.

Measurements at 6 and 4 GHz have also shown that 99% of the XPD variations are slower than ±4 dB/s, or equivalently, less than ±1.5°/s in the mean path differential phase shift. Therefore, the time constant of a depolarization compensation system at these frequencies need only be about 1 s.

5 Propagation delays

Radiometeorologically-based methods for estimating the average propagation delay or range error, and the corresponding variations, for Earth-space paths through the troposphere are available in Recommendation ITU-R P.834. The delay variance is required for satellite ranging and synchronization in digital satellite communication systems. At frequencies above 10 GHz, the ionospheric time delay (see Recommendation ITU-R P.531) is generally smaller than that for the troposphere, but may have to be considered in special cases.

Range determination to centimetre accuracy requires careful consideration of the various contributions to excess range delay. The water vapour component amounts to 10 cm for a zenith path and a reference atmosphere with surface water vapour concentration of 7.5 g/m^3 and 2 km scale height (see Recommendation ITU-R P.676). This contribution is the largest source of uncertainty, even though the dry atmosphere adds 2.3 m of the zenithal excess range delay.

For current satellite telecommunication applications, additional propagation delays contributed by precipitation are sufficiently small to be ignored.

6 Bandwidth limitations

In the vicinity of the absorption lines of atmospheric gases, anomalous dispersion produces small changes in the refractive index. However, these refractive index changes are small in the bands allocated to Earth-space communications, and will not restrict the bandwidth of systems.

Multiple scattering in rain can limit the bandwidth of incoherent transmission systems due to variation in time delays of the multiple-scattered signals; however, the attenuation itself under such circumstances will present a far more serious problem. A study of the problem of bandwidth limitations imposed by the frequency dependence of attenuation and phase shift due to rain on coherent transmission systems showed that such bandwidth limitations are in excess of 3.5 GHz for all situations likely to be encountered. These are greater than any bandwidth allocated for Earth-space communications below 40 GHz, and the rain attenuation will therefore be far more important than its frequency dependence.

7 Angle of arrival

Elevation-angle errors due to refraction are discussed in Recommendation ITU-R P.834. The total angular refraction (the increase in apparent elevation) is about 0.65°, 0.35° and 0.25°, for elevation angles of 1°, 3° and 5°, respectively, for a tropical maritime atmosphere. For a polar continental climate the corresponding values are 0.44°, 0.25° and 0.17°. Other climates will have values between these two extremes. The day-to-day variation in apparent elevation is of the order of 0.1° (r.m.s.) at 1° elevation, but the variation decreases rapidly with increasing elevation angle.

Short-term angle-of-arrival fluctuations are discussed in Recommendation ITU-R P.834. Short-term variations, due to changes in the refractivity-height variation, may be of the order of 0.02° (r.m.s.) at 1° elevation, again decreasing rapidly with increasing elevation angle. In practice, it is difficult to distinguish between the effect of the short-term changes in the refractivity-height distribution and the effect of random irregularities superimposed on that distribution. A statistical analysis of the short-term angle-of-arrival fluctuation at 19.5 GHz and at an elevation angle of 48° suggests that both in elevation and azimuth directions, standard deviations of angle-of-arrival fluctuations are about 0.002° at the cumulative time percentage of 1%. The seasonal variation of angle-of-arrival fluctuations suggests that the fluctuations increase in summer and decrease in winter. The diurnal variation suggests that they increase in the daytime and decrease both in the early morning and the evening.

8 Calculation of long-term statistics for non-GSO paths

The prediction methods described above were derived for applications where the elevation angle remains constant. For non-GSO systems, where the elevation angle is varying, the link availability for a single satellite can be calculated in the following way:

a) calculate the minimum and maximum elevation angles at which the system will be expected to operate;

b) divide the operational range of angles into small increments (e.g. 5° wide);

c) calculate the percentage of time that the satellite is visible as a function of elevation angle in each increment;

d) for a given propagation impairment level, find the time percentage that the level is exceeded for each elevation angle increment;

e) for each elevation angle increment, multiply the results of c) and d) and divide by 100, giving the time percentage that the impairment level is exceeded at this elevation angle;

f) sum the time percentage values obtained in e) to arrive at the total system time percentage that the impairment level is exceeded.

In the case of multi-visibility satellite constellations employing satellite path diversity (i.e. switching to the least impaired path), an approximate calculation can be made assuming that the spacecraft with the highest elevation angle is being used.

Appendix 4

Appendix Three: Space Radiation Effects on Integrated Circuits

Objective:

To describe the radiation environment in space, the physics of radiation interactions with solids, radiation effects on semiconductor devices, and strategies for with standing the space radiation environment.

Semiconductor devices are sensitive to many types of radiation found in the natural space radiation environment. For this reason, ICs intended for use in this environment often require special design and fabrication. Parts so designed are called radiation-hardened, or rad-hard. Although many design strategies can reduce a part's susceptibility to radiation damage, the primary determinants of that susceptibility depend upon the fabrication process. Using special processes and design methodologies, certain vendors can produce ICs that meet severe radiation environmental stresses. Rad-hard standard parts have specifications that indicate radiation exposure limits beyond which they function less efficiently or not at all. When designing ASICs, control over their design provides the opportunity for additional radiation-tolerant design approaches. Military standards such as MIL-M-38510, MIL-I-38535, and MIL-STD- 883 provide a common language for radiation concepts as well as radiation test standards.

Finding Radiation Information in This Guide

This guide provides three sections with information about how radiation affects ASICs. For information on how radiation relates to ASIC qualification, see the management section. For information on design issues regarding radiation tolerance, see Chapter 4 of the design section. Finally, for background information about the physics of radiation and how it applies to ICs in general, continue reading this appendix.

This appendix gives a brief overview of the radiation environment in space, the physics of radiation interactions with solids, radiation effects on semiconductor devices, and strategies for withstanding the space radiation environment.

The Radiation Environment in Space

In space, high-energy particles (in the MeV range) can penetrate devices and cause temporary upsets and permanent damage. Particle sources in space are the cosmic-ray background, solar flare events, and trapped particles in planetary magnetic fields. Interactions with spacecraft components cause secondary particle emissions as well. Finally, components on the spacecraft itself, such as radioactive heaters, radioisotope thermo-elastic generators, and nuclear reactors, can emit particles.

Cosmic rays originate in the outer regions of the galaxy and provide our solar system with a constant onslaught of particles from all directions. Of these particles, 85 percent are protons, 14 percent are alpha particles, and 1 percent are heavy ions. The flux 1 AU from the Earth is about 4/cm-s, with energies from almost 0 to over 10 GeV. Hydrogen, helium, carbon and oxygen ions are the bulk of the heavy ions, peaking at energies around 1 GeV, while ions with atomic numbers above 26 are rarely observed.

Solar flares represent a potential source of radiation damage. These bursts of high-energy charged particles originate from certain regions on the sun. Of these particles, over 90 percent are protons, and the rest are alpha particles, heavy ions, and electrons. These large, sudden fluxes occur sporadically, at about three times per year. The heaviest doses occur 10 to 12 years apart, according to the solar flare cycle. In a typical burst, the flux peak occurs between 2 and 24 hours after its origin and decays over a period of a few days. Heavy ion fluxes from solar flares are usually far below the galactic background, but they can be up to four orders of

magnitude above the background during some flares.

Planetary magnetic fields tend to trap electrons and protons from cosmic and solar sources and, in the case of our planet, man-made sources. The strongest known radiation of this type exists in Jupiter's radiation belts. To illustrate planetary magnetic fields, we offer a description of the Earth's magnetic field.

The solar wind causes the Earth's magnetic trapping region facing the sun to be hemispherical, with a radius 10 to 12 times that of Earth, and the trapping region extends cylindrically for hundreds of Earth radii in the direction away from the sun. Van Allen belts result when the Earth catches electrons and protons gyrating around magnetic field lines. Physicists classify trapped electrons into inner and outer zones, divided at a distance of about 2.5 Earth radii from the Earth's surface. The flux of electrons in the outer zone is about 10 times that of the inner zone, with outer zone electron energies of about 7 MeV and inner zone energies of less than 5 MeV. Proton energies vary approximately inversely with altitude and can have energies over 400 MeV close to the Earth. A region in the Atlantic Ocean near Brazil contains magnetic field lines that are depressed relatively low into the Earth's atmosphere. This region, called the South Atlantic Anomaly (SAA), contains the highest concentration of radiation for low- Earth orbits. It is especially rich in proton energies and flux due to the protons' inverse relation with altitude.

The Physics of Radiation Interactions with Solids

Radiation interactions with solids are classified into three groups: photon, charged particle, and neutron interactions. Photons (X-rays and gamma rays) interact with atoms through the photoelectric effect, Compton scattering, and pair production, and in each case they generate energetic free electrons that cause secondary charged particle interactions. Those charged particles, as well as charged particles from other sources, interact through Rutherford (Coulombic) interaction or, if heavy enough, nuclear interactions. Neutrons, which interact through nuclear interactions, are not a problem in space but rather in nuclear explosions and from nuclear reactors.

Rutherford scattering liberates (ionizes) or excites atomic electrons, while nuclear interactions displace atoms in crystal lattices or transmute atoms from one element to another. These two mechanisms change the state of a solid. Two effects of these mechanisms concern the solid state electronics industry: ionization and atomic displacement.

Ionization occurs when an atom loses an excited valence electron to the conduction band. A charged particle ionizes a valence electron by liberating that electron and creating lattice vibrations that may ionize further atoms. The electron absence created by this process is called a hole. If an electric field is present, some electrons and holes immediately recombine with other atoms or become "trapped" in lattice defect sites. Physicists refer to this phenomenon as "initial recombination." While ionization produces electron absences, atomic displacement produces lattice defects.

Atomic displacement occurs when heavy particles interact with atomic nuclei, removing them from their lattice sites to new (interstitial) sites. This upsets the periodicity of the lattice, thus creating lattice defects.

Radiation Effects on Semiconductor Devices

In space, radiation effects on semiconductor devices are classified into two major types: total ionizing dose (TID) and single-event effects (SEE). TID is the accumulated effect of ionizing radiation over the lifetime of a space mission, and SEEs are transient or permanent effects due to single particles. A third type, displacement damage, is less important.

TOTAL IONIZING DOSE

Ionizing radiation primarily effects the oxide layer of MOS structures, silicon dioxide (SiO_2). The oxide is a crystal lattice vulnerable to the build-up of injected ions. Engineers measure TID in terms of radiation absorbed dose or rad (1 rad = 100 ergs per gram of material).

Ionizing radiation produces electron-hole pairs in SiO_2 which allow holes to cause further damage. These pairs form at the rate of 7.6×10^{12} pairs/rad(SiO_2)- cm^3. After initial recombination the gate immediately collects the mobile electrons leaving holes to transport to an interface, both via the electric field across the transistor. Holes travel to the Si-SiO_2 interface if the field is positive. In modern devices this occurs in microseconds, but it can take seconds to hours in thicker oxides with low fields.

These positively-charged holes can cause a catastrophic negative shift in the threshold voltage of the device. A fraction (a fifth or more for unhardened devices) of the holes are trapped at the Si- SiO_2 interface. If this voltage shift is great enough in the right direction, a device which is normally "off" threshold can turn "on" (or vice-versa) with 0 volts applied to it. Also, the positive charge can invert p-type isolation regions, causing leakage currents between adjacent transistors. These traps remain until they are annealed (detrapped) over a period of hours to years via effects such as electron tunneling.

Radiation also induces permanent interface traps that can shift threshold voltages. These interface traps can also hinder carrier mobility, which slows device speeds. These traps are energy levels within the Si bandgap near the Si-SiO_2 interface. Their tendency to form, as with trapped holes, depends upon the fabrication process of the device. These extra energy levels form both immediately and over a period of up to a day, causing a net negative charge for n-channel metallic oxide semiconductor field effect transistors (MOSFETs) and a net positive charge for p-channel MOSFETs. Combined with the positive charge due to hole trapping, interface traps offset the hole trapping charge for n-channel devices, and the two effects add for p-channel devices.

A phenomenon known as the rebound effect significantly increases the threshold voltage. Trapped hole charge build-ups tend to dominate over interface trap charge build- ups initially, but trapped holes anneal over time as the interface traps remain. For n-channel devices, this implies a net positive charge that initially reduces the threshold voltage. But as the net positive charge lessens due to annealing of the trapped holes, the smaller effect of negative charge from the interface traps begins to dominate, thus causing "rebound." If there are few interface traps, rebound may favorably readjust the threshold voltages. Using this mechanism rebound may naturally cure devices that previously failed due to trapped hole buildup. However, if there are many interface traps, rebound may also cause the device to fail by shifting the threshold voltage from too low to too high. For p- channel devices, the threshold shifts described here move in opposite directions.

TID depends not only upon total trapped charge, but upon the rate of incoming particles as well. The interplay between hole trapping, hole annealing and interface trap buildup causes this complex dependency.

SINGLE-EVENT EFFECTS

Integrated circuits are susceptible to transient upsets (soft errors) and permanent damage (hard errors) when single high-energy particles impinge on a transistor. A single charged particle can traverse through a transistor's reverse-biased p-n junction and create an ionizing path along its line of trajectory. This causes excess charge along that path, the amount of which is called the Linear Energy Transfer (LET). The electric field across the junction is distorted along the ionizing path (this is called funneling), which increases the electric field's ability to attract the charge to one of the nodes. Eventually, the nodes collect the leftover charge through diffusion.

Soft Errors

Transient errors called single-event upsets (SEUs), which are the most common manifestations of SEEs. An SEU is an ion-induced change in the logical state of a transistor. This will happen if the LET exceeds the critical charge (Q_{CRIT}) required to change the logical state of the transistor. SEUs are temporary since they merely cause a logical error--they do not damage the chip. Once any affected registers are reset, the chip will resume correct operation. But that error has the potential to propagate and effect critical functions, causing any number of permanent problems on board the spacecraft.

Hard-Errors

SEEs can also cause errors that permanently damage the transistor. ASICs are sensitive to single-event latchups, snapbacks, and burnouts (although burnouts have not yet been observed in space). Latchups occur when a p-n-p-n or n-p-n-p CMOS transistor is traversed by a high-LET particle. If enough charge is injected into the base of the parasitic bipolars, the normally high- impedance state can become low, thereby turning the cell on permanently. Similarly, a snapback permanently turns a cell on, but without the p-n-p-n structure. For a snapback, charge collection in the p-well surrounding n-channel transistors produces a drain avalanche current and the source-to-drain voltage sustains this current. A single-event burnout (SEB) can occur when a heavy ion traverses a high voltage junction, creating a low resistance path between the gate and the substrate. This burns the cell and renders it inoperative.

DISPLACEMENT DAMAGE

Although rarely a concern for ASICs, high-energy protons--and to some extent heavy ions--can displace atoms in a crystal lattice, creating energy levels in the forbidden band gap. This can reduce the minority carrier lifetimes and thereby reduce gain by introducing new recombination centers. Typically this only concerns solar cells and wide-base bipolar transistors.

Strategies for Withstanding the Radiation Environment

Everyone involved in designing a spacecraft and its mission should be aware of ASIC radiation-tolerance issues. These designers can minimize the effects of radiation by using carefully planned trajectories, shields, rad-hard parts, and fault tolerant design methods.

Currently available tools for mission designers determine flight paths that minimize radiation exposure. These tools can ensure that a spacecraft spends the least possible amount of time in planetary radiation belts.

Radiation shielding is an integral part of any spacecraft design. Low-energy particles are trivial to shield, whereas high-energy particles become much more difficult. The best shields have low atomic number, such as carbon and aluminum. Designers often sculpt shields to work in conjunction with the spacecraft's inherent shielding, thereby minimizing mass. Engineers design many IC packages with shielding as well. Shielding can significantly reduce TID, but it can rarely affect SEEs since particles energetic enough to cause SEEs typically require shields several inches thick to be adequately attenuated. Unfortunately, shielding may also enhance TID and SEEs by slowing fast particles into energy ranges of SEE or TID sensitivity.

Given that flight path considerations and shielding cannot completely shelter electronics from radiation, designers must use rad-hard and fault tolerant subsystems as the final recourse.

Vendors and designers produce rad-hard ASICs by hardening the fabrication process and the design. Hardening the process deals mainly with hardening the oxide layer, since it is the most sensitive to radiation. Hardening the circuit design requires conservative practices such as widening design margins for stability, gain, and noise. Fan-out, slew rate, propagation delays, and other circuit parameters must account for worst-case radiation effects.

Fault tolerance includes built-in self tests, redundancy, and other methods. Built-in self tests constantly check faults so that the system can implement backup procedures immediately. Since SEUs are not permanent, designers often use redundancy techniques to incorporate repetition. By verifying that successive independent repetitions produce the same result, a system can ignore SEU- affected operations. Also, three or more redundant parts may "vote" on the correct operation, avoiding the need for repetition. For more information on "Design for Radiation Tolerance," see Section Three: Chapter 4.

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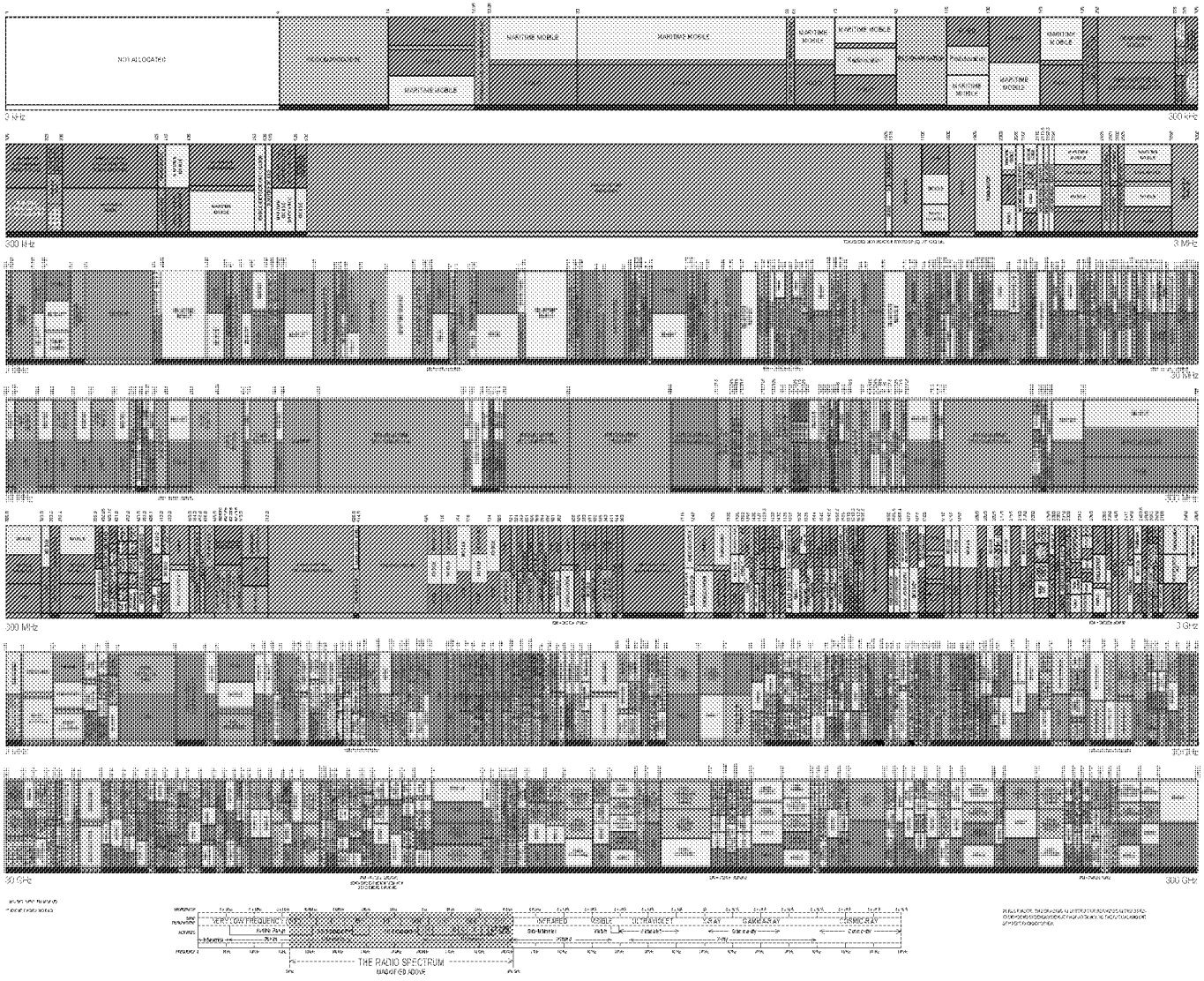
Now you may jump to:

- the next appendix: Appendix 4: "Failure Analysis"
- the Table of Contents
- the Index
- the Acronym list
- the Glossary

Appendix 5

UNITED STATES FREQUENCY ALLOCATIONS

THE RADIO SPECTRUM



RADIO SERVICES COLOR LEGEND

- AERONAUTICAL MOBILE
- AERONAUTICAL MOBILE SATELLITE
- AERONAUTICAL RADIONAVIGATION
- AMATEUR
- AMATEUR SATELLITE
- BROADCASTING
- BROADCASTING SATELLITE
- EARTH EXPLORATION SATELLITE
- FIXED
- FIXED SATELLITE
- INTER-SATELLITE
- LAND MOBILE
- LAND MOBILE SATELLITE
- MARITIME MOBILE
- MARITIME MOBILE SATELLITE
- MARITIME RADIONAVIGATION
- METEOROLOGICAL AIDS
- METEOROLOGICAL SATELLITE
- MOBILE
- MOBILE SATELLITE
- RADIO ASTRONOMY
- RADIODETERMINATION SATELLITE
- RADIOLOCATION
- RADIOLOCATION SATELLITE
- RADIONAVIGATION
- RADIONAVIGATION SATELLITE
- SPACE OPERATION
- SPACE RESEARCH
- STANDARD FREQUENCY AND TIME SIGNAL
- STANDARD FREQUENCY AND TIME SIGNAL SATELLITE

ACTIVITY CODE

- GOVERNMENT EXCLUSIVE
- NON-GOVERNMENT EXCLUSIVE
- GOVERNMENT/NON-GOVERNMENT SHARED

ALLOCATION USAGE DESIGNATION

SERVICE	EXAMPLE	DESCRIPTION
Primary	FIXED	Capital Letters
Secondary	Mobile	1st Capital with lower case letters

U.S. DEPARTMENT OF COMMERCE
National Telecommunications and Information Administration
Office of Spectrum Management
October 2003

CERTIFICATE OF ELECTRONIC SUBMISSION
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Owner: Entropic Communications, LLC

Inventors: Madhukar Reddy et al.

App. No.: 90/019,255

Filed: 09/20/2023

Conf. No. 5785

Examiner: LIE, ANGELA M

Art Unit: 3992

Title: WIDEBAND TUNER ARCHITECTURE

Docket No.: 189005.TR003

RESPONSE TO FINAL OFFICE ACTION

Mail Stop *Ex Parte Reexam*
Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner,

In response to the Final Office Action dated August 7, 2024, please consider the following remarks.

A **Listing of Claims** begins on page 2 of this paper.

Applicant's **Remarks** begin on page 6 of this paper.

LISTING OF CLAIMS

No claim is amended. The listing of all claims of the Patent is provided for reference only. Only two claims, Claims 1 and 11, are rejected in the OA:

1. A wideband receiver system comprising:

a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

digital circuitry configured to:

select said plurality of desired television channels from said digitized plurality of frequencies; and

output said selected plurality of television channels to a demodulator as a digital datastream.

2. The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface.

3. The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface.

4. The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.

5. The wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises:

a first ADC configured to generate a digital in-phase signal; and

a second ADC configured to generate a digital quadrature signal.

6. The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.

7. The wideband receiver system of claim 6, wherein:

prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and

after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.

8. The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.

9. The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter.

10. The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels.

11. A method comprising:

in a wideband receiver system:

downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;

digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and

outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.

12. The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface.

13. The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface.

14. The method of claim 11, comprising:

generating, by a first mixer of said mixer module, an in-phase signal; and

generating, by a second mixer of said mixer module, a quadrature signal.

15. The method of claim 11, comprising:

generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and

generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.

16. The method of claim 15, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry.

17. The method of claim 16, wherein:

prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and

after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum.

18. The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.

19. The method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter.

20. The method of claim 11, comprising decimating, by said digital circuitry, one or more of said selected plurality of desired television channels prior to said outputting of said selected plurality of television channels.

REMARKS

Claims 1 and 11 are subject to reexamination. No new matter has been added. Patent Owner respectfully requests reconsideration of the claims in view of the following remarks.

Response to Rejection under 35 U.S.C. § 103

Claims 1 and 11 are rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Pugel in view of Gomez.

I. Gomez is not analogous art.

The OA fails to demonstrate that Gomez is analogous art. "A reference qualifies as prior art for an obviousness determination . . . only when it is analogous to the claimed invention." *In re Klein*, 647 F.3d 1343, 1348 (Fed. Cir. 2011). An obviousness ground that relies upon non-analogous art fails. *Id.* at 1352. To be analogous, a reference must either be (1) from the same field of endeavor as the patent-at-issue or (2) reasonably pertinent to the particular problem with which the inventor of the challenged patent is involved. *In re Clay*, 966 F.2d 656, 658–59 (Fed. Cir. 1992). The OA fails to demonstrate that Gomez is analogous under either prong.

a. Gomez and the '362 Patent are from two different fields of endeavor

The Federal Circuit has explained that "substantial evidence must support the PTO's factual assessment of the field of endeavor." *In re Bigio*, 381 F.3d 1320, 1326 (2004) (citing *In re Gartside*, 203 F.3d 1305, 1315 (Fed. Cir. 2000)). "In other words, the PTO must show adequate support for its findings on the scope of the field of endeavor in the application's written description and claims, including the structure and function of the invention." *Id.* The Federal Circuit has also cautioned that "it is necessary to consider 'the reality of the circumstances'—in other words, common

sense—in deciding in which fields a person of ordinary skill would reasonably be expected to look for a solution to the problem facing the inventor." *Id.* (citing *In re Oetiker*, 977 F.2d 1443, 1447 (Fed. Cir. 1992)).

A finding that Gomez is directed to the same field of endeavor as the '362 Patent is inconsistent with Federal Circuit precedent, which has held that even art with substantial similarities and in the same technological area as the patent-at-issue may not be in the same field when, as here, the patent office over-simplifies the field of endeavor. The Examiner's suggested field of "receiving and processing signals and tuners" is simply too broad to adequately explain the field of Gomez.

The OA alleges that "Pugel and Gomez are considered analogous arts because they belong to the same field of endeavor covering receiving and processing signals and tuners." OA at 11. However, the OA does not cite any support, let alone "substantial evidence," for such a broad field of endeavor.

As set forth in the accompanying declaration of Frank Koperda—an expert in this area who provides helpful testimony about the scope and content of the prior art through the eyes of a POSITA—Gomez's field of endeavor is channel switching in a *satellite* television system. *See* Koperda Decl. ¶ 37; *see also* ¶¶ 3–7, 21. Specifically, Gomez is directed to a channel switch device, also called a "frequency translation module" or "FTM." *See id.* at ¶¶ 29, 34; *see also* Gomez, Title ("Scalable Architecture for Satellite Channel Switch"); 1:16–20 ("The present invention generally relates to the field of channel switches in a multi-channel communication system. More specifically, the present invention relates to processing one or more input channels to a frequency translation module through a scalable switch architecture."); Claim 1 ("A frequency translation module . . .").

As Mr. Koperda explains, an FTM is a device that is used in *satellite* television systems. *See* Koperda Decl. ¶ 30. A typical arrangement is depicted in Figure 1 of WO 2006/119490 ("McNeely"), which the Examiner previously cited as prior art.

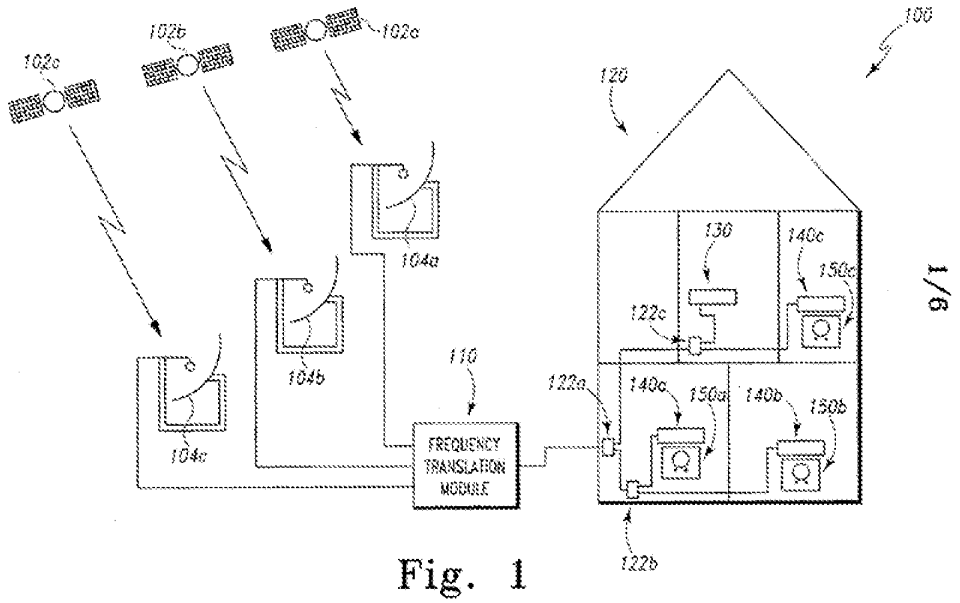


Fig. 1

The FTM is used to address a problem that arises in satellite television, but not in cable television. That is that a single household might receive signals from multiple satellites in different orbital locations. *See* Koperda Decl. ¶ 31. Moreover, each individual satellite transmits signals using multiple transponders, each of which transmits a signal with its own frequency band, direction of signal, and/or polarization. *Id.* The FTM addresses this problem by "enabl[ing] a user to selectively switch the signals received from each satellite antenna and deliver these signals to an IRD [integrated receiver decoder] located within a household." Gomez, 1:38–41.

Conversely, the '362 Patent's field of endeavor is wideband receiver devices for use in a *cable* television system. *See* Koperda Decl. ¶¶ 22–26, 36; *see also* '362 Patent, 1:52–55 ("The RF input signal may include the VHF and UHF television channels in a terrestrial television

broadcasting system or the CATV channels in cable networks"). The '362 Patent's title and abstract further confirm it is directed to wideband receivers. *See generally Airbus S.A.S. v. Firepass Corp.*, 941 F.3d 1374, 1380–81 (Fed. Cir. 2019) (affirming Board's finding of field of endeavor based on "the title of the [] patent and the preamble of a . . . claim"); *In re Wood*, 599 F.2d 1032, 1036 (CCPA 1979) (determining field of endeavor based on "Background of Invention"); *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1237–38 (Fed. Cir. 2010) (similar).

As Mr. Koperda explains, there are significant differences between cable and satellite television systems, such that a POSITA would consider them different fields of endeavor. *See* Koperda Decl. ¶¶ 37, 48. Each has unique problems and design considerations that require POSITA's to take different approaches to optimizing solutions. *See id.* For example, satellite signals are subject to higher distortion than signals transmitted over cable. *See id.* at ¶¶ 38–40. However, it is possible to reuse the same carrier frequency in a satellite system, *e.g.* by having multiple transponders transmit the same frequency toward different geographic areas or with different signal polarization. *See id.* at ¶¶ 43, 47. This is not possible in a cable environment, where the entire RF signal (with bandwidth of several hundred MHz) is transmitted concurrently over hybrid fiber coaxial (HFC) cable. *See id.* at ¶¶ 40, 45. But this also requires satellites that relay many TV channels to use multiple transponders. *See id.* at ¶ 44.

As another example, space-based satellite systems must be designed to survive in space, which requires shock- and radiation-hardening and presents unique challenges relating to power and cooling. *See id.* at ¶¶ 41–42, 47. There is also a scarcity of wireless spectrum, which in the U.S. is assigned by the FCC in accordance with international treaties. *See id.* at ¶¶ 43, 46. Because these are non-factors in the cable environment, it frees up cable engineers to optimize other factors such as component cost. *See id.* at ¶ 47.

Clay, the leading analogous art decision, is instructive as to the impropriety of the rejection's treatment of Gomez as analogous art. *Clay*, 966 F.2d at 658. In *Clay*, a finding of analogous art was "clearly erroneous" where the patent-at-issue and the allegedly analogous art (Syndansk) were two patents owned by the same company (Marathon Oil), and the patent-at-issue concerned a gel for use in the petroleum industry while Syndansk concerned a "similar" gel for use in the petroleum industry. *Id.* at 657–60. As to the field-of-endeavor test, the Court found that the Board clearly erred in finding Syndansk was analogous because the patent-at-issue's "field of endeavor is the *storage* of refined liquid hydrocarbons" whereas "[t]he field of endeavor of Syndansk's invention . . . is the *extraction* of crude petroleum." *Id.* at 659. Thus, the "storage" and "extraction" of oil are two separate fields.

Similarly, semiconductor "memory" is also too broad a field. As the Federal Circuit found:

> The Allen-Bradley art is not in the same field of endeavor as the claimed subject matter merely because it relates to memories. It involves memory circuits in which modules of varying sizes may be added or replaced; in contrast, the subject patents teach compact modular memories.

Wang Labs., Inc. v. Toshiba Corp., 993 F.2d 858, 864–65 (Fed. Cir. 1993).

Here too, the Examiner's suggested field of "receiving and processing signals and tuners" is too broad. Although Gomez and the '362 Patent both involve RF communication, there are fundamental differences between Gomez's *satellite* systems and the *cable* systems involved in the '362 Patent. *See e.g.* '362 Patent, 1:52–55. These are considered separate fields by those skilled in the art because of the challenges and design consideration unique to each field, and the Examiner has presented no evidence to the contrary.

Accordingly, Gomez is not from the same field of endeavor as the '362 Patent.

b. Gomez is not reasonably pertinent to the problem addressed by the '362 Patent

The OA does not address whether Gomez is reasonably pertinent to the problem addressed by the '362 Patent, and therefore that cannot be the basis to conclude Gomez is analogous art. Regardless, the two are directed to fundamentally different problems and Gomez does not propose solutions that would be relevant to the problems addressed by the '362 Patent.

The '362 Patent is directed to an improved architecture for a wideband *cable* receiver. In that environment, the input RF signal has a continuous bandwidth of over 800 MHz, delivered over HFC. *See* '362 Patent, 2:14–23. This means that a "wideband" receiver must include circuitry capable of processing hundreds of megahertz of bandwidth concurrently. *See* Koperda Decl. ¶ 49. This kind of circuitry is not used in Gomez or in satellite systems generally. *See id.*

As noted above, satellite systems use multiple transponders to transmit signals. A POSITA would understand that each of these transponders has a typical bandwidth of 36–72 MHz. *See id.* at ¶ 50. Gomez teaches that an FTM is used to "selectively switch" between the signals from each transponder. *See id.* at ¶ 51; *see also* Gomez, 1:38–41. A POSITA would understand this to mean that Gomez uses a system of many mixers, A/D converters, and filters to process the signals from the multiple transponders, thereby avoiding the use of wideband analog-to-digital conversion techniques required for the '362 Patent. *See* Koperda Decl. ¶ 51. A POSITA would further recognize that switching between multiple transponders is a technique with no application to cable systems. *See id.* at ¶¶ 45, 51. Lastly, a POSITA would recognize that Gomez's system outputs only a single channel of interest. *See id.* at ¶¶ 32–33, 52, 57; *see also* Gomez, 4:34–39, 4:47–57; 4:12–15; 8:50–57; 9:21–25. This is far less complex than selecting many channels as disclosed in the '362 Patent.

A POSITA would therefore not view Gomez as related to the problem sought to be solved by the '362 Patent—improving the efficiency of a wideband cable receiver. *See* Koperda Decl. ¶

53. The fact that Gomez and the '362 Patent may have some technological overlap is immaterial as even technologically similar references may not be reasonably pertinent. *Clay* found it was "clearly erroneous" to consider Syndansk as reasonably pertinent because a POSITA "would not reasonably have expected to solve the problem of dead volume in tanks for storing refined petroleum by considering a reference dealing with plugging underground formation anomalies." *Clay*, 966 F.2d at 660; *see also Wang*, 993 F.2d at 864 (prior art memory modules not reasonably pertinent to patented memory modules); *Polygroup Ltd. v. Willis Elec. Co., Ltd.*, IPR2016-01610, Paper 187, 31, 35–40 (Feb. 26, 2018) (rejecting argument that "structurally and functionally similar" electrical connectors in reference and patent made reference reasonably pertinent). Regardless of the presence of certain overlapping words, the field of Gomez and the problem/solution of Gomez are not at all related to the problems and solution of the '362 Patent.

Thus, the OA fails to demonstrate that Gomez is analogous art to the '362 Patent.

II. The OA fails to demonstrate a motivation to combine Pugel and Gomez.

The OA alleges that Pugel discloses downconverting, but acknowledges that Pugel "does not explicitly disclose that the downconverting is performed by a mixer module of the wideband receiver system." OA, p. 4. The OA then alleges it would have been obvious to combine the teachings of Pugel and Gomez "and utilize Gomez's teaching about employing a mixer to perform down-conversion in order to efficiently process[] inputted signals." *Id.* at 5. However, the OA does not articulate any reason why a POSITA would be motivated to modify Pugel in this way.

It is well-settled that obviousness is not established merely because the "elements of the claimed invention were independently known in the prior art." *Metalcraft of Mayville, Inc. v. Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017). "The obviousness inquiry does not merely ask whether a skilled artisan ***could*** combine the references, but instead asks whether 'they ***would*** have been

motivated to do so.'" *Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1359 (Fed. Cir. 2020) (quoting *InTouch Techs., Inc. v. VGO Commc'ns, Inc.*, 751 F.3d 1327, 1352 (Fed. Cir. 2014)) (emphasis added). Or as the Federal Circuit has more recently explained, "it does not suffice to simply be known. A reason for combining ***must exist***." *Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 888 (Fed. Cir. 2024) (emphasis added). There is no reason to make the proposed combination, short of reliance on the '362 Patent's disclosures itself as a roadmap.

As an initial matter, a POSITA would not look to modify Pugel in view of Gomez because the two are directed to different fields of endeavor. *See* Koperda Decl. ¶ 55. Like the '362 Patent, Pugel is directed to *cable* systems which a POSITA would not look to combine with Gomez's *satellite* teachings. *See id.* at ¶¶ 27–28, 55. There is no basis to conclude that a POSITA would have combined the teachings from such disparate references "in the normal course of research and development." *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011).

Moreover, Pugel relates to a *wideband* cable receiver, where each downconverter is configured to downconvert a bandwidth of at least 300 MHz. *See* Koperda Decl. ¶ 56; *see also* Pugel, ¶¶ [0024], [0028], Claim 18 (the analog input signal is separated into three bands of 5–300 MHz, 300–600 MHz, and 600–900 MHz; then each of these bands is digitized and down-converted). As noted above, Gomez's FTM switches between satellite transponders with frequency ranges from 36–72 MHz. As such, a POSITA would understand that Gomez's analog mixers are designed to downconvert signals with much narrower bandwidths than those in Pugel. *See* Koperda Decl. ¶ 58-69. The mixers of Gomez are, as discussed during the interview, fundamentally different than would be applicable to the system of Pugel. *Id.* Moreover, the mixers of Gomez would not lead a POSITA to the subject matter of the claims of the '362 Patent, capable of

"downconvert[ing] a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels."

This means there are at least two problems with the Examiner's proposed modification to Pugel. First, Pugel already performs downconverting, and the Examiner cites no teaching or indication that would motivate a POSITA to modify Pugel's downconverting techniques. But second, even if a POSITA were to consider Pugel and Gomez together, the POSITA would recognize that Gomez's analog mixers are not suitable for use in Pugel's wideband cable receiver because they lack the complexity needed to process the wide bandwidths demanded by Pugel's cable receiver. *See* Koperda Decl. ¶¶ 58-69.

The OA does not address these issues. It states only that "it would be obvious to one of ordinary skill in the art to change the order of the operations ***if needed***," but this only begs the question. *Why would such a change be needed?* The OA does not provide an answer. This is exactly the kind of hindsight bias that the Federal Circuit has cautioned must be avoided. *See Virtek*, 97 F.4th at 886 ("It does not suffice to meet the motivation to combine requirement to recognize that two alternative arrangements . . . were both known in the art"); *see also Ruiz v. A.B. Chance Co.*, 357 F.3d 1270, 1275 (Fed. Cir. 2004) ("This form of hindsight reasoning, using the invention as a roadmap to find its prior art components, would discount the value of combining various existing features or principles in a new way to achieve a new result - often the very definition of invention").

The fact that Pugel already includes downconverting techniques that are appropriate for that system is something both the Federal Circuit and the PTAB have found to weigh against a finding of obviousness. For example, in *NTP, Inc.*, the patent-at-issue related to a system for sending an email from a personal computer to a mobile device using an intermediary RF receiver. *See In re NTP, Inc.*, 654 F.3d 1279, 1285 (Fed. Cir. 2011). Initially, the claims were rejected over

the applicant's admitted prior art in view of "Harrison," which taught the use of an RF network to deliver data. *See id.* at 1297–98. However, the Federal Circuit held that the Board had improperly relied on hindsight. *See id.* at 1299. In particular, the Federal Circuit noted that the Board's position was "weakened by the fact that the [applicant's admitted prior art] already discloses an RF network that connects portable computers to the system. Thus, adding an RF network [from Harrison] . . . would render the RF network connecting the portable PCs in figure 1 superfluous." *Id.* Similarly, in this case, adding Gomez's downconverting to the system of Pugel would be superfluous.

In another example, the PTAB denied institution of *inter partes* review against a patent relating to a radio communication system in which a subscriber station maintains a transmit power difference or "power headroom" while transmitting messages. *Apple Inc. v. Cellular Comm'ns Equipment, LLC*, IPR2015-00576, Paper 7, 2–3 (June 12, 2015). The petitioner relied on combining "Hall," which related to estimating a communication mode quality in a wireless communications system (*id.* at 6), with "Reed," which relates to establishing headroom for a mobile station operating in a wireless communications system. *Id.* at 11. For the motivation to combine, Petitioner argued that replacing Hall's scheme with Reed's would ensure a minimum power margin is maintained and avoid excessive or inadequate headroom. *See id.* at 11–12. However, the Federal Circuit disagreed because the petition "fails to provide a specific explanation why Hall did not already accomplish that by itself." *Id.* at 12. Similarly, in this case, Pugel already accomplishes efficient downconverting, so there is no motivation to incorporate Gomez's incompatible method of downconverting. *See* Koperda Decl. ¶¶ 58-69.

In yet another example involving a patent directed to managing and load balancing in an IP network, petitioner sought to combine a "lookup table" from one reference (Veerina) with a "routing table" from another reference (Ota). *See F5 Networks, Inc. v. Radware, Ltd.*, IPR2017-

00124, Paper 48, 63 (Apr. 23, 2018). As the PTAB noted, however, Ota used the information in its routing table to select a route. *See id.* at 65. Veerina's lookup table already included a selected route (which had been selected by other means). *See id.* Thus, adding information from Ota's routing table to Veerina's lookup table would "serve no purpose." *Id.* Similarly, in this case, adding Gomez's mixer module to Pugel would serve no purpose because Pugel already teaches how to accomplish downconverting.

As noted at the onset, "[t]he obviousness inquiry does not merely ask whether a skilled artisan *could* combine the references, but instead asks whether they would have been *motivated* to do so." *Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1359 (Fed. Cir. 2020) (quotes omitted) (emphasis added).

In this case, a POSITA would not look to modify Pugel's wideband cable receiver based on Gomez's teachings about satellite television systems. And even if a POSITA were to consider the two references together, there is no basis to modify Pugel's downconverting techniques in view of Gomez's mixers, which operate in a fundamentally different realm. Therefore, the OA has not shown the obviousness of its proposed combination, and Patent Owner respectfully requests withdrawal of the rejection.

Conclusion

Thus, withdrawal of the rejections under 35 U.S.C. 103 are respectfully requested. These remarks are believed to address all of the rejections in the instant Office Action. Applicant respectfully requests that the rejections be withdrawn and that a Notice of Allowance be granted. The Examiner is respectfully requested to contact the undersigned in the event that a telephone interview would expedite consideration of the application. Should any fee be required in this response, please charge the fee due to Deposit Account 60-2239.

Respectfully submitted,

Date: September 30, 2024

/ Hao Tan/

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Owner: Entropic Communications, LLC
Inventors: Madhukar Reddy et al.
App. No.: 90/019,255
Filed: September 20, 2023
Conf. No.: 5785
Examiner: LIE, ANGELA M
Art Unit: 3992
Title: WIDEBAND TUNER ARCHITECTURE
Docket No.: 189005.TR003

SUMMARY OF TELEPHONE INTERVIEW

Patent Owner thanks the Examiners for their time and attention in this matter. During the interview conducted on September 23, 2024 at 10:30 am (Eastern), representatives of Patent Owner and technical expert (Frank Koperda) participated in the interview with Examiners and discussed the rejection of claims 1 and 11 under pre-AIA 35 U.S.C. 103(a) as allegedly being unpatentable over Pugel (WO 2007/145637) in view of Gomez (US 8,224,274).

In the interview, Patent Owner presented arguments that Gomez is not analogous art and the final office action fails to demonstrate a motivation to combine Pugel and Gomez. It was agreed that Patent Owner could submit a Declaration by Frank Koperda with the response to the final office action. No agreement was reached regarding the patentability of the claims.

Respectfully submitted,

Date: September 30, 2024

/ Hao Tan/

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Document Description: Transmittal Letter

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TRANSMITTAL FORM

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Total Number of Pages in This Submission

Application Number	90/019,255
Filing Date	09/20/2023
First Named Inventor	Madhukar Reddy
Art Unit	3992
Examiner Name	ANGELA M LIE
Attorney Docket Number	189005.TR003

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☑ Amendment/Reply
  - ☑ After Final
  - ☑ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
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- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):
  1. Applicant summary of interview with Examiner

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Arch & Lake LLP		
Signature	/Hao Tan/		
Printed name	Hao Tan		
Date	2024-09-30	Reg. No.	73,711

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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
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Title of Invention

WIDEBAND TUNER ARCHITECTURE

Application Information

APPLICATION TYPE	Utility / ex parte reexam	PATENT #	9210362
CONFIRMATION #	5785	FILED BY	Xuanjie Wang
PATENT CENTER #	67376209	FILING DATE	09/20/2023
CUSTOMER #	153979	FIRST NAMED INVENTOR	- 9210362
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Hao Tan

Documents

TOTAL DOCUMENTS: 6

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
189005.TR003_Applicant summary of interview with examiner.pdf		2	Applicant summary of interview with examiner	124 KB
362 Reexam Response to FR319871832.7.pdf		17	-	281 KB
362 Reexam Response to FR319871832.7-A.NE.pdf	(1-1)	1	Response After Final Action	131 KB
362 Reexam Response to FR319871832.7-CLM.pdf	(2-5)	4	Claims	78 KB
362 Reexam Response to FR319871832.7-REM.pdf	(6-17)	12	Applicant Arguments/Remarks Made in an Amendment	229 KB
Complete_with_Docusign_Koperda_Decl.pdf		149	Affidavit-traversing rejections or objections rule 132	5059 KB

189005.TR003 Transmittal.pdf	2	Transmittal Letter	289 KB

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DOCUMENT	MESSAGE DIGEST(SHA-512)
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362 Reexam Response to FR319871832.7-A.NE.pdf	3FA11581BE071BA24B43184CD1B6DDE74EF8DB8AD174D5BE037ED6F2F9390CFF64AEB199F10B9DF0C4BAC81445C77C0E63F2E2C96BF226AA23861798618D7339
362 Reexam Response to FR319871832.7-CLM.pdf	C637559B32B3EFED587A9D3E27ED606D443CDEBE2DEB8B7D618811376191BA58E0F91878B9C235781B8CDFEFADC9D49FBFE4FE3CFC3432BB2F59A1D355173D38
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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
90/019,255	**10/01/2024 04:03:29 PM Z ET**	**189005.TR003**

Title of Invention

WIDEBAND TUNER ARCHITECTURE

Application Information

APPLICATION TYPE	Utility / ex parte reexam	PATENT #	9210362
CONFIRMATION #	5785	FILED BY	ZHANGYUAN JI
PATENT CENTER #	67398872	FILING DATE	09/20/2023
CUSTOMER #	153979	FIRST NAMED INVENTOR	- 9210362
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Certificate of Service 2024-10-1.pdf	1	Reexam Certificate of Service	121 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
Certificate of Service 2024-10-1.pdf	69D16952121B9DEDDC2E5548845D23DF9D471B22176CEF0811EA89296D5F4D0C90DFE4CD9261B94B988EE44516ED67635C8524967CFFABCDE5EAF2124FC74148

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Owner: Entropic Communications, LLC.
Inventors: Madhukar Reddy et al.
App. No.: 90/019,255
Filed: September 20, 2023
Conf. No.: 5785
Examiner: LIE, ANGELA M
Art Unit: 3992
Title: WIDEBAND TUNER ARCHITECTURE
Docket No.: 189005.TR003

CERTIFICATE OF SERVICE

Mail Stop *Ex Parte Reexam*
Central Reexamination Unit
Commissioner for Patents
P O Box 1450
Alexandria, VA 22313-1450

Dear Commissioner,

I hereby certify that I served a copy of the Response to the Final Office Action of August 7, 2024 in the *ex parte* reexamination requestor in accordance with MPEP § 2266, 37 C.F.R. § 1.550 and 35 C.F.R. 1.248 via first class mail on Oct. 1, 2024. The name and address of the party served is:

Raghav Bajaj
Haynes and Boone, LLP
2323 Victory Avenue, Suite 700
Dallas, Texas 75219

Respectfully submitted,

Date: October 1, 2024 / Hao Tan/
Hao Tan, Reg. No. 73,711