

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00189
U.S. Patent No. 11,145,666 B2
Issue Date: Oct. 12, 2021

Title: STAIRCASE STRUCTURE FOR MEMORY DEVICE

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,145,666
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,145,666 B2 to Lu et al. (the “’666 patent”)
1002	File History of U.S. Patent No. 11,145,666 B2 to Lu et al.
1003	Declaration of Dr. Jack C. Lee
1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
1005	U.S. Patent No. 10,229,929 to Kim et al. (“Kim”)
1006	U.S. Patent Publication No. 2018/0026046 A1 to Nam et al. (“Nam”)
1007	U.S. Patent Publication No. 2014/0191389 A1 to Lee et al. (“Lee”)
1008	U.S. Patent No. 10,297,543 to Park et al. (“Park”)
1009	U.S. Patent No. 9,589,978 to Yip
1010	Aritome, “NAND Flash Memory Technologies” (2016)
1011	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1012	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1013	Excerpts from the File History of PCT/CN2018/098962
1014	File History of U.S. Patent No. 10,680,003 (Appl. 16/126,956)
1015	U.S. Patent Publication No. 2015/255385 to Lee
1016	U.S. Patent No. 9,373,540 to Hyun
1017	U.S. Pub. 2011/0031630 A1 to Hashimoto
1018	U.S. Patent No. 9,343,452 to Yun et al.

Exhibit	Description
1019	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1020	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1021	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.'s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1022	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:24-cv-04223-RFL which has been consolidated with Case No. 3:23-cv-05792-RFL

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 17:	
[17.PRE]	A memory device, comprising::
[17.A]	a substrate, wherein the substrate comprises a top surface
[17.B]	a memory string disposed over the substrate; and
[17.C]	a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:
[17.C.1]	a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer,
[17.C.2]	wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.
Claim 19:	
[19]	The memory device of claim 17, wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack.
Claim 20:	
[20]	The memory device of claim 17, wherein the conductive layer comprises a first conductive material, and wherein the curved side surface comprises a second conductive material.

I. Introduction

Petitioner Micron Technology, Inc. requests IPR of claims 17, 19, and 20 of U.S. Patent 11,145,666 (Ex. 1001, the “’666 patent”), assigned to Yangtze Memory Technologies Co., Ltd. (“Patent Owner”).

The ’666 patent relates to 3D NAND memory devices. Typical prior art 3D NAND memory devices include vertically oriented strings of memory cells. These memory cell strings pass through alternating layers of conductive and insulating material stacked on a substrate. The stacked conductive/insulating layers of these typical 3D NAND memory devices were routinely formed with a step or staircase structure outside of the area where the memory cells are located. This staircase structure allows for electrical interconnection with each of the conductive layers.

The ’666 patent discusses and claims a staircase structure with landing pads—referred to as a “second portion” of a “conductive layer” in the claims—on each step. Claim 17, which is the only independent claim addressed by this petition, requires that the landing pad have a “curved” “side surface” that is in “contact” with the “side surface” of the adjacent insulating layer in the stacked staircase structure. While not discussed in the specification, an example of a landing pad with a “curved” side surface appears to be shown in Figure 8 of the ’666 patent (the “curve”—which is difficult to see—is located at the interface between the orange landing pad and the blue insulation):

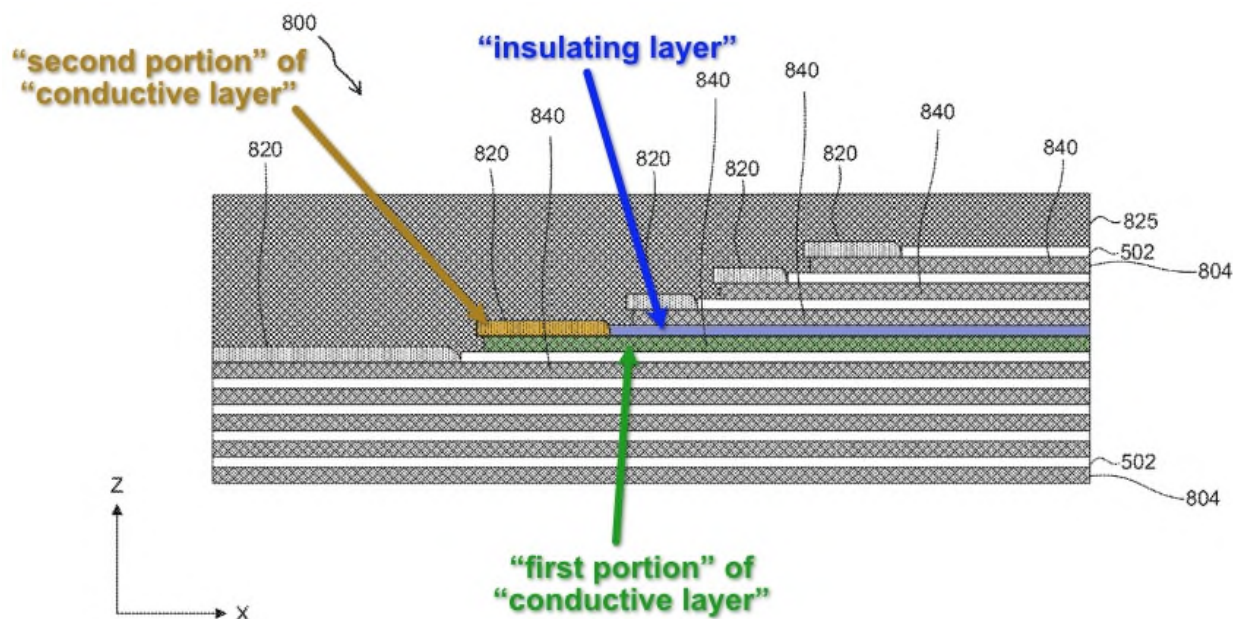


FIG. 8

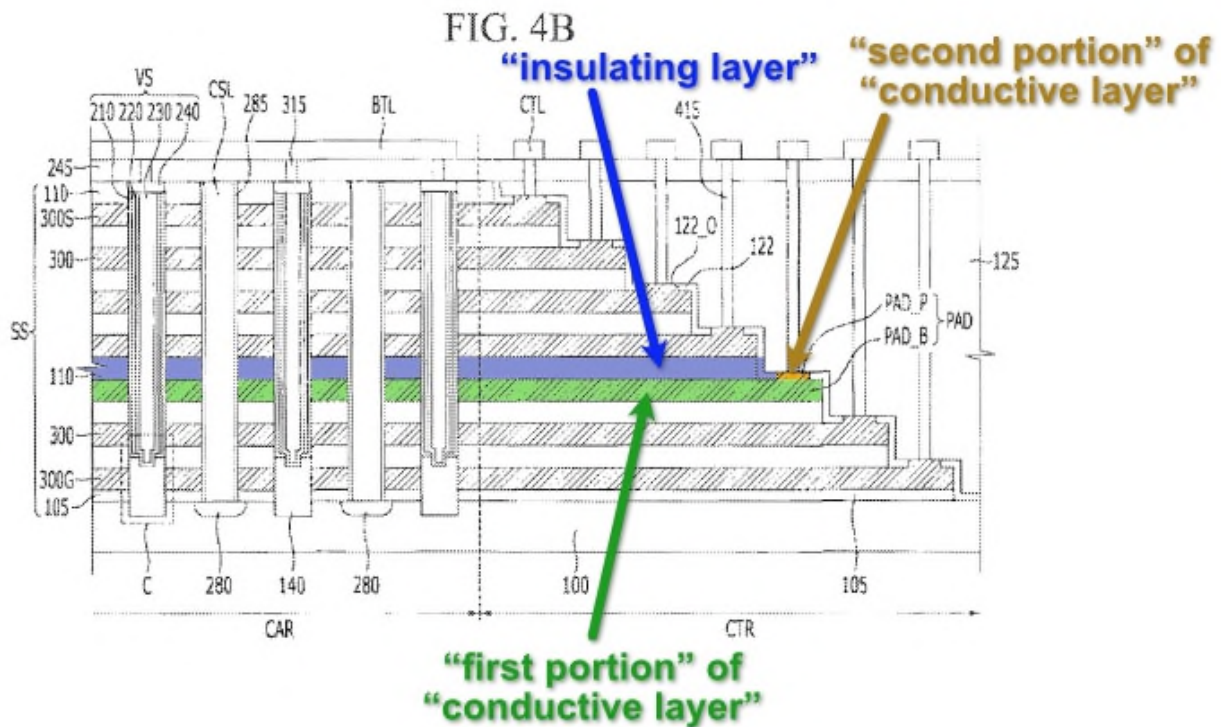
Ex. 1001, Fig. 8 (annotated).

The prior art makes clear, however, that there was nothing patentable about this structure. This Petition focuses on the following exemplary references: U.S. Patent No. 10,229,929 to Kim et al. (Ex. 1005, “Kim”), U.S. Pub. 2018/0026046 A1 to Nam et al. (Ex. 1006, “Nam”), U.S. Pub. 2014/0191389 A1 to Lee et al. (Ex. 1007, “Lee”), and U.S. Patent No. 10,297,543 to Park et al. (Ex. 1008, “Park”). As discussed below, these references render the claims obvious.

Patent claims can be rendered obvious by a single prior art reference that teaches every claim limitation. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1372-73 (Fed. Cir. 2019). This is what both Kim and Nam do here: a POSITA would have understood that these references’ memory devices include the very type of

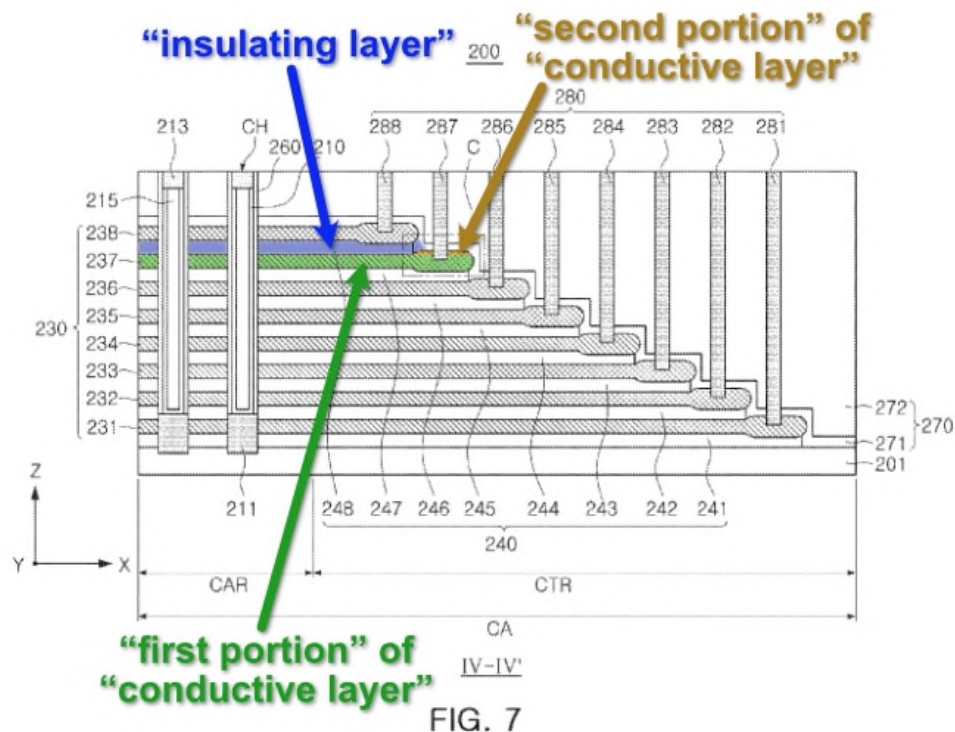
landing pad with a “curved” side surface in “contact” with insulation that the ’666 patent’s claims require.

Kim—just like the ’666 patent—teaches a 3D memory device with vertically oriented strings of memory cells. It also includes a stacked step/staircase structure outside of the area where the memory strings are located. The stack is formed from alternating conductive and insulating layers. Further, in Kim, each of the conductive layers in this stepped stack includes a contact or landing pad (PAD_P) to facilitate electrical connection. Figure 4B below provides an example:



Kim, Fig. 4B (annotated). While the PAD_P is shown as generally rectangular in the figure, Kim explains that it can instead be formed with a “curved surface,” just as the ’666 patent requires. *Id.*, 8:29-34.

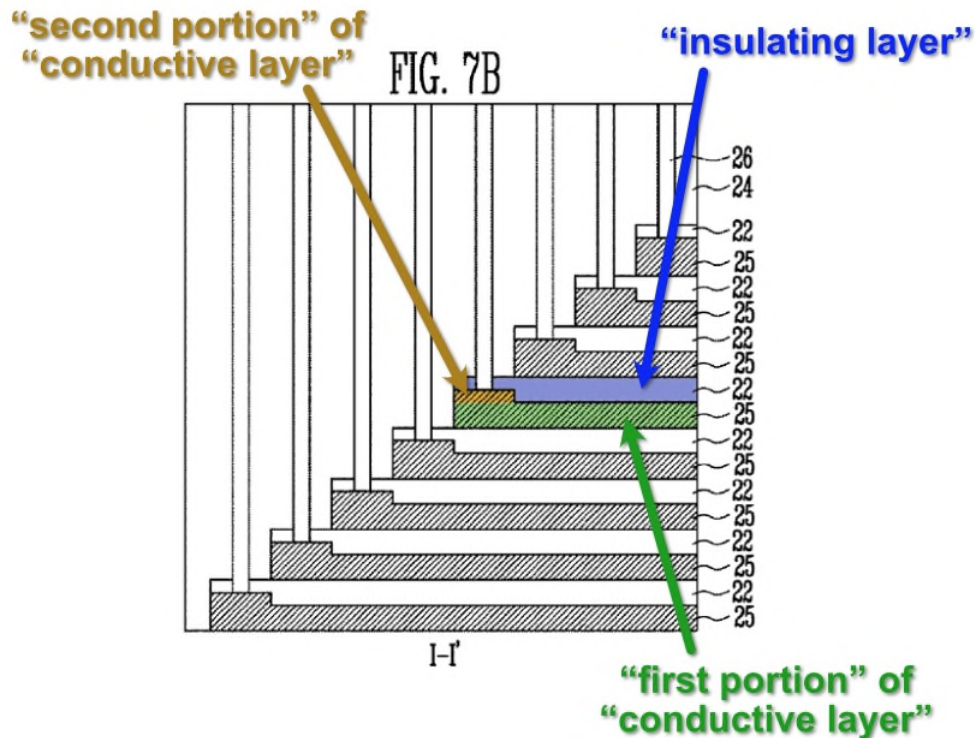
Nam also teaches a 3D memory device with vertically oriented strings of memory cells. Like both Kim and the '666 patent, Nam's device includes a stepped contact structure outside of the area where the memory strings are located. The stack is formed from alternating conductive and insulating layers. Further, Nam teaches that each of the conductive layers in the stack includes a thicker contact pad at its end. Contact pad thickness is increased to prevent the contact from passing through the pad and creating a short. This thicker contact pad is formed via ion injection and has a convex shape. This results in the same type of "curved" side surface required by the claims here:



Nam, Fig. 7 (annotated).

The claims are also rendered obvious by the combination of Lee and Park.

Lee provides yet another example of a 3D memory device with vertically oriented strings of memory cells. Lee's device includes a stacked structure—formed with a stepped pattern—that includes alternately arranged insulating layers and conductive layers. An insulating layer is on top of each step. The insulating layer also surrounds what Lee calls a “pad portion PAD” at the end of each conductive layer. The pad has an increased height relative to the rest of the layer to avoid issues when connecting a contact to the conductive layer. One of Lee's insulating layers, conductive layers, and pads is annotated below. As shown, a side of the insulating layer is in “contact” with the pad as the '666 patent's claims require:



Lee, Fig. 7B (annotated).

While Lee depicts its pads with straight sides, a POSITA would have

considered it obvious to make the sides “curved” in view of Park. Lee explains that it is important to ensure that there is sufficient distance between the pad and adjacent conductive layers to avoid electrical breakdown. Park—like Lee—teaches a 3D memory device employing a staircase structure with contact pads. Moreover, it explains that the distance between the pads and adjacent conductive layers can be increased—and the risk of breakdown minimized—by rounding the sides of the contact pads.

II. Mandatory Notices

A. Real Party-in-Interest

Petitioner Micron Technology, Inc., and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

B. Related Matters

On July 12, 2024, YMTC asserted the ’666 patent and U.S. Patent Nos. 10,672,711, 10,879,164, 10,879,254, 10,886,291, 11,101,276, 11,450,604, 11,482,532, 11,568,941, 11,581,322, and 12,010,838 against Micron in district court (the “YMTC2 case”). On August 21, 2024, the YMTC2 case was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co-Pending Litigation”). U.S. Patent Nos. 10,658,378, 10,861,872, 10,868,031, 10,937,806, 10,950,623, 11,468,957, 11,501,822, and

11,600,342 were asserted by Patent Owner in the first-filed case, leading to a total of 19 patents-at-issue in the now consolidate Co-Pending Litigation.

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each of the 19 asserted patents in the Co-Pending Litigations:

Patent	PTAB Proceeding	Wave
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	
10,672,711	IPR2025-00117	Wave 3 Petitions
10,879,164	IPR2025-00118	
10,879,254	IPR2025-00034	
10,879,254	IPR2025-00119	

Patent	PTAB Proceeding	Wave
10,886,291	IPR2025-TBD	
11,101,276	IPR2025-00228	
11,450,604	IPR2025-00035	
11,482,532	IPR2025-TBD	
11,568,941	IPR2025-00190	
11,581,322	IPR2025-00191	
12,010,838	IPR2025-00229	

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a).

C. Counsel, Service, and Fee Information

Petitioner designates the following counsel:

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Petitioner consents to service by electronic mail at the following addresses: P52PTABDocket@orrick.com, PTABDocketJJL2@orrick.com, PTABDocketJ3B3@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner attaches a Power of Attorney.

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

III. Requirements for IPR

A. Grounds for Standing

Petitioner certifies that the '666 patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Petitioner was served with a

complaint alleging infringement of the '666 patent on July 12, 2024. This petition is being filed within 1 year of that date.

B. Identification of Challenge and Statement of Precise Relief Requested

Petitioner requests IPR of claims 17, 19, and 20. This petition discusses claim construction, explains why the claims are unpatentable, provides details regarding where the various claim limitations are found in the prior art, and is supported by the accompanying Declaration of Dr. Jack C. Lee (Ex. 1003), a leading expert in the 3D memory field.

The application underlying the '666 patent—U.S. App. 16/885,858—was filed May 28, 2020. The patent facially identifies itself as a continuation of a September 10, 2018 U.S. application and an August 6, 2018 PCT filing. Ex. 1001, Cover. The patent also makes a priority claim back to an August 28, 2017 foreign filing. *See id.* For purposes of this Petition only, it is assumed that the '666 patent is entitled to the benefit of this August 28, 2017 date.

Petitioner relies on Kim (Ex. 1005), Nam (Ex. 1006), Lee (Ex. 1007), and Park (Ex. 1008). Kim, Nam, Lee, and Park are all prior art to the '666 patent. *See* §VIII.

Petitioner challenges claims 17, 19, and 20 on the following grounds:

Ground 1: Claims 17, 19, and 20 are obvious over Kim;

Ground 2: Claims 17, 19, and 20 are obvious over Nam; and

Ground 3: Claims 17, 19, and 20 are obvious over Lee and Park.

IV. Institution Should Be Granted

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There Are No Grounds for a § 314 Discretionary Denial in this Case

There is a pending district court action involving the '666 patent. The PTAB has explained that it “will not ... discretionarily deny institution in view of parallel district court litigation where a petition presents compelling evidence of unpatentability.” 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it presents a compelling case here: the claims of the '666 patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (PTAB Mar. 20, 2020) (precedential). In particular: the district court may stay the case, any potential trial will occur years from now, little district court work has occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24, 7 (PTAB June 16, 2020) (informative); *Fintiv*, 6-9, 12 (similar).

2. Proximity of the Court’s Trial Date

On September 18, 2024, the district court entered a scheduling order which set a trial date of June 15, 2026. *See* Ex. 1019. If IPR is instituted, it should be completed before this date. *See also* Ex. 1020 (indicating an average of 48.9 months to trial). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and Court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings and consolidation, little substantive progress has been made. *See* §II.B. Virtually no progress has been on the Wave 3 patents (which includes the ’666 patent). The parties have not completed the exchange of contentions for the Wave 3 patents (from the YMTC2 case) and have not taken any depositions in the entire Co-Pending Litigation. Fact discovery is in its infancy. No claim construction positions have been exchanged for the Wave 3 patents, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no

summary judgment motions have been filed. This weighs in favor of institution. See *Sand Revolution*, 10-11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv*, 11. Here, on July 12, 2024, PO asserted eleven Wave 3 patents against Petitioner—asserting 149 claims for the Wave 3 patents. Ex. 1021. Petitioner proceeded with diligence, starting the filing of eleven petitions approximately three months after being served with the YMTC2 complaint. Ex. 1022. This also weighs strongly in favor of institution.

4. Issue Overlap

Should the Board institute, Micron stipulates that it will not advance in District Court any ground asserted in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution*, 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not

previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under § 325(d) Would Be Inappropriate

Kim and Nam were not cited by Patent Owner or considered by the Examiner during prosecution of the '666 patent. *See generally* Ex. 1002. While Lee and Park are identified by the '666 patent, neither was not assessed by the Examiner or used to reject the claims during prosecution. *See infra* §V.D. Indeed, as explained in Section V.D below, the Examiner allowed claims 17, 19, and 20 without any rejection over the prior art at all. While certain prior art references were used to reject other claims in applications to which the '666 patent claims priority, none of these claims requires the same type of “curved” “side surface” in “contact” with insulation as claim 17. Moreover, none of this prior art appears to teach landing pads with “curved” side surfaces as Kim, Nam, and Park do. And none teaches insulating layers with the same physical extent as those in Lee. Thus, the issues and prior art references raised by this Petition are unique and were not previously considered by the Office. It also constituted error for the Examiner to allow claims 17, 19, and 20 without substantive analysis or rejection.

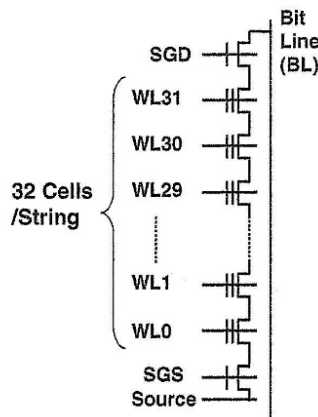
V. The '666 Patent

A. Technological Background

The '666 patent and the prior art discussed in this petition relate to 3D memory. One type of memory that is often implemented as 3D memory is “flash memory.” “Flash memory” is a form of “non-volatile memory.” Ex. 1009, 1:24-26.

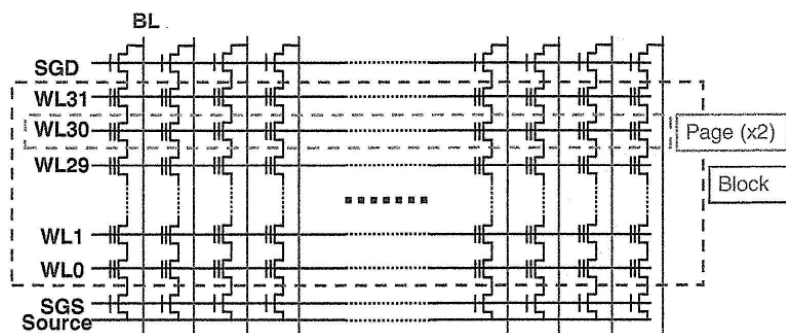
“Non-volatile memory ... can retain its data values ... without the application of power.” *Id.*, 1:26-28. NAND flash stores data in a “cell” formed from a transistor. Ex. 1010, 38-39; Ex. 1011, 109; *see also* Ex. 1003, ¶¶ 40-46.

NAND cells are arranged in “strings” with multiple cells “connected in series.” Ex. 1010, 38. The cells are surrounded by “select transistors (SGD, SGS).” *Id.* The “SGD connects” at the string’s drain side “to isolate it from the bit line (BL),” and the “SGS connects” at the string’s source side “to isolate it from a source line (SL).” *Id.* Word lines connect to each memory cell’s control gate. *Id.*, 38-39. One such string is shown below:

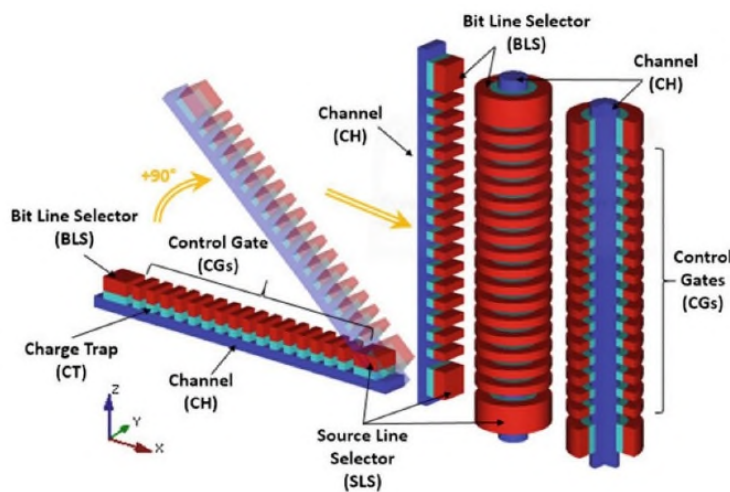


Id., 39.

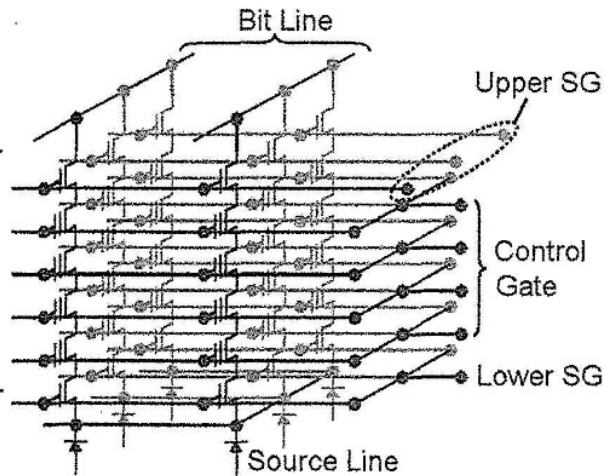
Early NAND devices were formed as two-dimensional arrays of cells on a substrate surface. *Id.*, 38.



Id., 40. “[T]o further scale down the memory cell size,” 3D NAND was developed in 2006. *Id.*, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1012, 3.

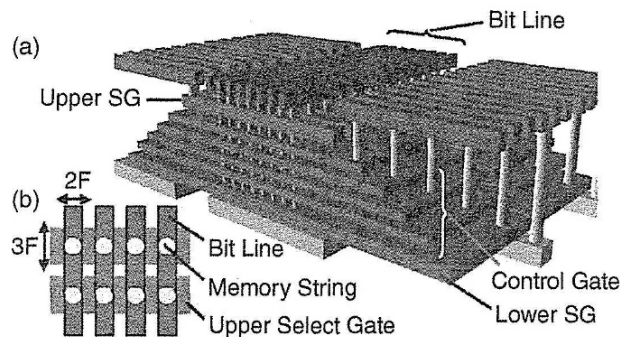


Ex. 1011, 122. Multiple such vertical channels are then repeated in a three-dimensional array:



Ex. 1010, 296; *see also* Ex. 1003, ¶¶ 47-55.

3D NAND includes “multi-stacked layers of gate (plate)” material alternated with “dielectric” in a “[s]tack.” Ex. 1010, 294. A “through-hole” channel “filled by memory film ... and channel poly-Si” passes through the layers to form the string of vertically arranged memory cells. *Id.*, 295. “Each” layer of “electrode plate acts as a control gate.” *Id.* “[T]he control gates ... are connected” to the memory’s “metal layers at [a] stair-like gate structure” with contact points located outside the memory array. *Id.*, 295, 297.



Id., 296; *see also* Ex. 1003, ¶¶ 56-61 .

B. Overview

The '666 patent relates generally to “a staircase structure for a memory device (e.g., 3D memory device).” Ex. 1001, 1:37-39. The patent notes that this structure somehow results in “yield and manufacturing cost improvements.” *Id.*, 1:39-41. But it never explains why that is the case.

The patent goes on to reference “3D memory devices” that include “vertically oriented strings of memory cell transistors.” *Id.*, 5:6-11. The “3D memory device[’s]” “staircase structures[]” is “disposed adjacent to” these “memory strings for word line, fan-out....” *Id.*, 5:31-33. “FIG. 8 illustrates a cross-sectional view of a staircase structure 800 with a dielectric layer 825 disposed thereon.” *Id.*, 9:35-37. The structure includes alternating “insulating layer[s] 502” and “wordline layer[s] 804.” *Id.*, 9:48-50. The layers are located over a “substrate.” *Id.*, 6:1-2. Each wordline layer includes a “landing pad 820 and conductive layer 840” and is intended to “control a portion of a memory string in the stacked storage region of a memory device.” *Id.*, 9:57-61. The “landing pad 820 contacts a portion of a side of insulating layer 502.” *Id.*, 9:61-65. The “landing pad 820” can be “made of the same or different conductive material as conductive layer 840.” *Id.*, 10:3-5.

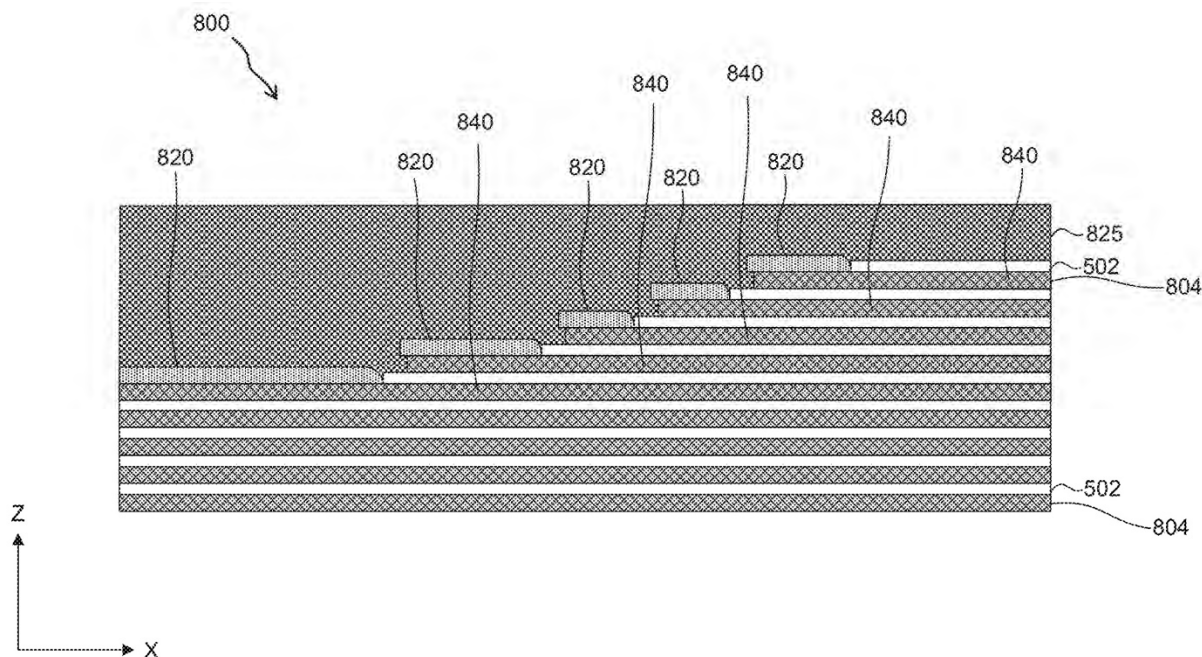


FIG. 8

Id., Fig. 8.

C. Claims

This Petition challenges claims 17, 19, and 20 of the '666 patent. Consistent with the specification, claim 17—the sole independent claim addressed by this Petition—references a “memory device” with a “substrate,” “memory string,” “staircase structure,” and alternating “insulating” and “conductive” layers. The “conductive layer[s]” include both a “first portion” (like layer 840 in Figure 8) and “second portion” (like landing pad 820 in the same figure). The claim also requires that the “second portion of the conductive layer” have a “**curved** side surface” that is “**in contact** with a side surface of the insulating layer.” While Figure 8 of the '666

patent may depict a “conductive layer” formed this way—landing pad 820 in the figure appears to be drawn slanted and/or curved in area where it contacts adjacent insulation layer 502—neither feature is discussed in the specification. The specification does not elaborate on what qualifies as a “curved side surface,” or what it means for “side surface[s]” to be “in contact.” The specification also attributes no importance or significance to either feature.

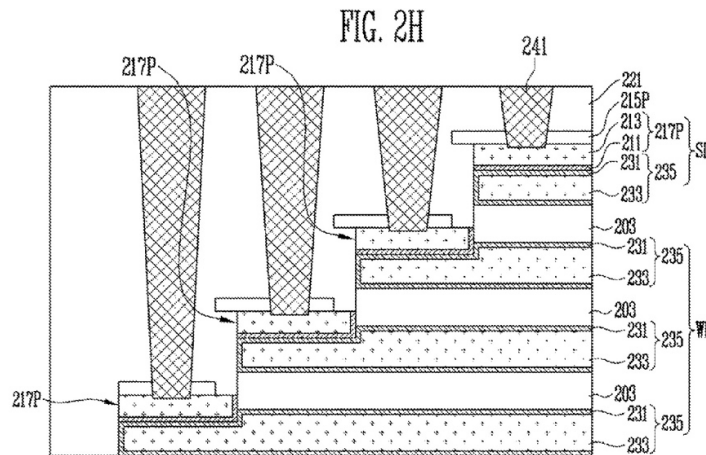
D. Prosecution History

The ’666 patent was filed May 28, 2020 as U.S. App. 16/885,858 (the “’858 App.”) and identifies itself as a continuation of a PCT application (PCT/CN2018/098962) and U.S. App. 16/126,956 (the “’956 App.”). *See* Ex. 1001, Cover. Neither the PCT nor the ’956 App. included a claim requiring a “curved side surface” like claim 17 does here. *See* Ex. 1013, 21-24; Ex. 1014, 36-39.

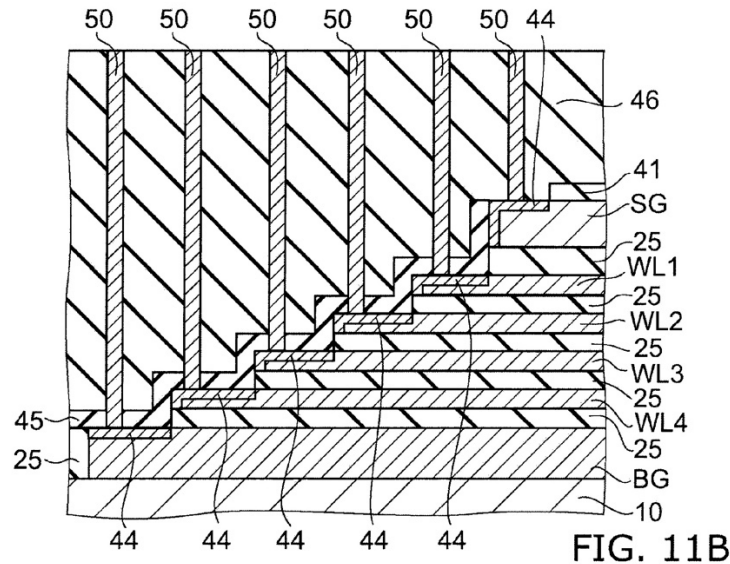
During pendency of the PCT application, a written opinion issued comparing U.S. Pub. 2015/255385 to Lee (“Lee 385,” Ex. 1015) to the claims. *See* Ex. 1014, 177. While Lee—one of the references at issue in this Petition—and Lee 385 have the same set of inventors, these references’ respective disclosures are substantively different. Lee 385 does teach a memory device with a staircase structure formed from alternating conductive and insulating layers. *See* Ex. 1015, ¶¶ [0003], [0009]. Lee 385’s device also includes a “pad part” on each of its conductive layers. *Id.*, ¶ [0010]. This pad can be structured in different ways. *See, e.g., id.*, Figs. 1A-1D.

But none of Lee 385's pads appear to include the "curved side surface" that claim 17 of the '666 patent requires. Moreover, in Lee 385, the insulation layers between the conductive layers are structured differently than those in the Lee reference discussed in this Petition. *Compare* Lee, Fig. 7A with Lee 385, Fig. 2F.

Prior art was also discussed during the prosecution of the '956 App. This art included U.S. Patent No. 9,373,540 to Hyun ("Hyun," Ex. 1016) and U.S. Pub. 2011/0031630 A1 to Hashimoto ("Hashimoto," Ex. 1017). *See* Ex. 1014, 202-208. The discussion of Hyun focused on Figure 2H, which is reproduced below:



Ex. 1016, Fig. 2H. Per the Examiner, this figure shows a "staircase structure" with alternating insulating (203) and conductive (235) layers. *See* Ex. 1014, 204. There are "landing pads" (217P) on each conductive layer. *Id.* Each landing pad is also covered by a protective layer of insulation 215P. *See* Ex. 1016, 6:66-7:14. The discussion of Hashimoto focused on Figure 11B shown below:



Ex. 1017, Fig. 11B. The Examiner explained that this figure also shows a device with a “staircase structure” with alternating conductive (WL) and insulating (25) layers. *See* Ex. 1014, 206. Each conductive layer includes a “landing pad” (44). *Id.* Like the prior art discussed during the PCT, Hyun and Hashimoto do not appear to illustrate landing pads with the type of “curved side surface” that claim 17 of the ’666 patent requires.

The application underlying the ’666 patent was filed next. Independent claim 17 was part of the application at the time of filing. *See* Ex. 1002, 31-34. The application also included two other independent claims: 1 and 9. *See id.* Neither of these required a “curved side surface” like claim 17. Claim 1 was rejected for nonstatutory double patenting over the patent that issued from the ’956 App. *Id.*, 103-109. Independent claims 9 and 17 were allowed without rejection. *See id.* In response to this rejection, the applicant amended claim 1 to require that the “top

surface” of the “landing pad” be “above” the “top surface” of an adjacent insulating layer (i.e., the landing pad must be thicker than the insulating layer). *See id.*, 128. This led to allowance of all the pending claims. *See id.*, 138-142. The Examiner did not issue a statement explaining why the allowed claims differed from the prior art. *See generally id.*

Unlike all the prior art of record discussed above, Kim, Nam, and the combination of Lee and Park teach landing or contact pads formed on each conductive layer of a memory device’s staircase structure with “curved” side surfaces that are in “contact” with an insulation layer. *See infra* §VIII.

VI. Claim Construction

The Board applies the same *Phillips* claim construction standard used by district courts. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). For purposes of this petition, Petitioner submits that the terms of the ’666 patent’s claims do not require further construction and can be afforded their plain and ordinary meaning. *See* Ex. 1003, ¶¶ 94-97.

The ’666 patent’s specification includes a section discussing the meaning of certain terms used in claims 17, 19, and 20. For instance, the specification explains that the terms “on,” “above,” and “over” “should be interpreted in the broadest manner such that ‘on’ not only means ‘directly on’ something, but also includes the meaning of ‘on’ something with an intermediate feature or a layer therebetween.”

Ex. 1001, 4:1-9. The terms “beneath,” “below,” “lower,” “above,” and “upper” are also simply meant to refer to the “relationship” between two elements regardless of how they are “oriented.” *Id.*, 4:10-20. Next, according to the patent, the “term ‘substrate’ refers to a material onto which subsequent material layers are added.” *Id.*, 4:21-35. Examples include “silicon,” “glass,” or a range of other materials. *Id.* The patent also explains that “the term ‘layer’ refers to a material portion including a region with a thickness.” *Id.*, 4:36-45. A “layer can be a region of homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure.” *Id.*, 4:43-45. “[A] layer can be located between any set of horizontal planes” and can even “include multiple layers.” *Id.*, 4:45-52. A POSITA would have recognized that none of this operates to limit the ’666 patent’s claims. See Ex. 1003, ¶¶ 159-165. Instead, it simply serves to confirm that the patent intends the claims to be interpreted broadly. See *id.* Additional details regarding how a POSITA would have interpreted the ’666 patent’s claims are provided in the sections below.

VII. Level of Ordinary Skill in the Art

A POSITA in the field of the ’666 patent would have had a bachelor’s degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) 3D memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced

degree may substitute for professional experience). *See* Ex. 1003, ¶¶ 34-37. This POSITA would also have been aware of and generally knowledgeable about 3D memory's structure, its component parts, and how it operates. *Id.*

VIII. Prior Art Overview

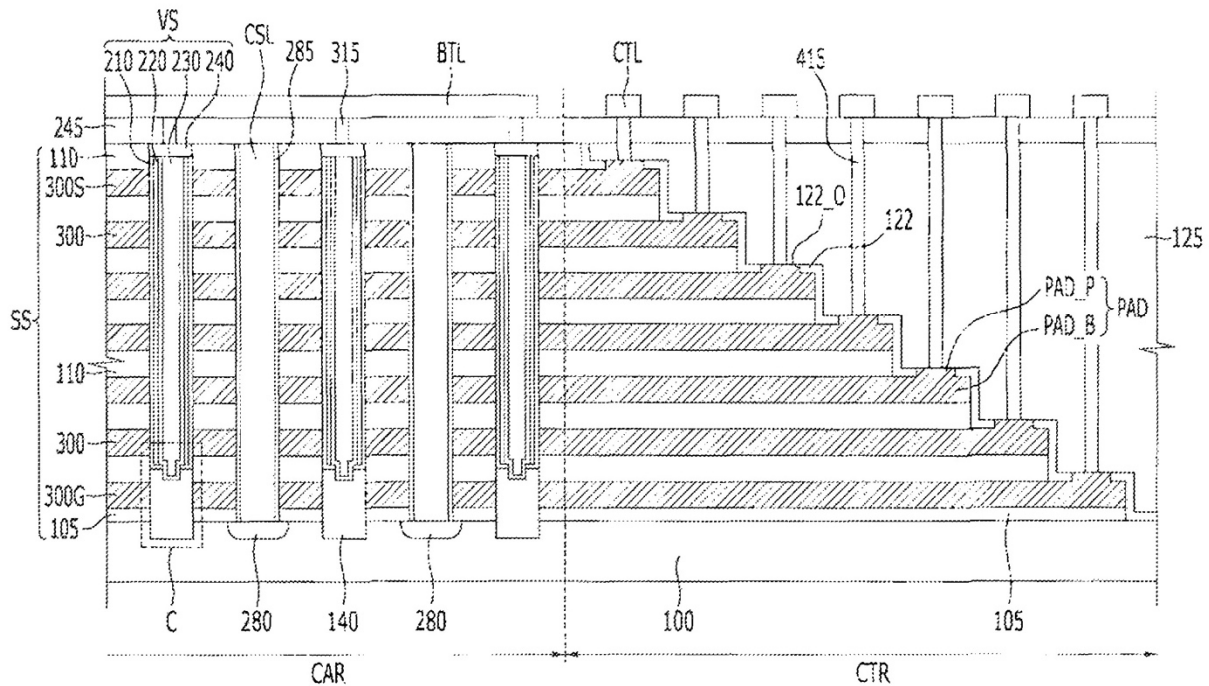
A. Kim

Kim was filed in the U.S. on July 18, 2017. Kim, Cover. It is prior art under AIA § 102(a)(2).

Kim relates to “semiconductor memory devices having enhanced reliability.” Kim, 1:38-39. The device can be implemented as a “3D semiconductor memory device[]” with “memory cells ... arrayed in 3D.” *Id.*, 1:26-30. The device includes a “cell array region” and a “contact region.” *Id.*, 1:41-46. The “cell array region” includes “memory cell[s]” arranged in vertically oriented memory “cell strings.” *Id.*, 4:26-28; *see also* Fig. 3. The “contact region” includes a “stacking structure” with a “stepwise structure.” *Id.*, 1:40-47.

Figure 4B—reproduced below—provides an example of one such “contact region”:

FIG. 4B



Id., Fig. 4B. A step-shaped “stacking structure SS” is formed from a “plurality” of alternating “insulating layers 110 and ... gate electrodes 300” located over a “substrate 100.” *Id.*, 5:53-55; Fig. 4B. The “gate electrodes” are formed from conductive material. *Id.*, 6:31-35. The insulating layer 110 can be integrated with an “auxiliary insulating layer 122.” *Id.*, 9:29-38. Each gate electrode 300 includes a “pad unit PAD” formed from “a base pad PAD_B and a protrusion pad PAD_P....” *Id.*, 7:58-62. The pad units PAD “electrically and physically connect” the gate electrodes 300 to an upper “connection line CTL.” *Id.*, 9:64-67. As shown in Figure 4B, “protrusion pad PAD_P” is located “inside” and is touching the sides of “opening 122_O” in Kim’s insulation layer 122. *Id.*, 9:21-23. While PAD_P is shown with a rectangular shape in the figure, Kim explains that it can “[also] have a

shape including a curved surface based on a virtual rectangular parallel[] shape, a cylindrical shape, or any shape.” *Id.*, 8:29-34.

B. Nam

Nam was filed in the U.S. on December 12, 2016. Nam, Cover. It is prior art under AIA § 102(a)(2).

Nam relates to “memory device[s]” such as a “NAND flash device” with arrays of memory cells. Nam, ¶¶ [0002], [0025], [0032], Figs. 1-2. The memory cells are arranged in vertically oriented “cell strings” located over a substrate. *Id.*, ¶¶ [0025]-[0026], [0033]; Figs. 2-3. The device includes both a “cell array region CAR” including the memory strings and a “contact region CTR” allowing for electrical connection to other circuitry. *Id.*, ¶¶ [0043], [0062]. The contact region has a “stepped shape.” *Id.*, ¶ [0043].

Nam’s device also includes a “stack of alternating first interlayer insulating layers and gate electrode layers on a substrate.” *Id.*, ¶ [0005]. Each gate electrode ends with a contact “pad region” that is thicker than the rest of the gate electrode to which it is attached. *Id.*, ¶ [0045]. Nam explains that thinner gate electrodes mean that “integration” can be “improved” via an “increased” “number of stacked gate electrode layers.” *Id.*, ¶¶ [0044], [0108]. Thicker contacts improve manufacturability and prevent “short circuits.” *Id.*, ¶¶ [0044]-[0045].

Nam’s contact pads can have a variety of shapes. In one example, the pads have a “convex” or “bull nose” shape. *Id.*, ¶ [0066]. This is shown in Figure 7:

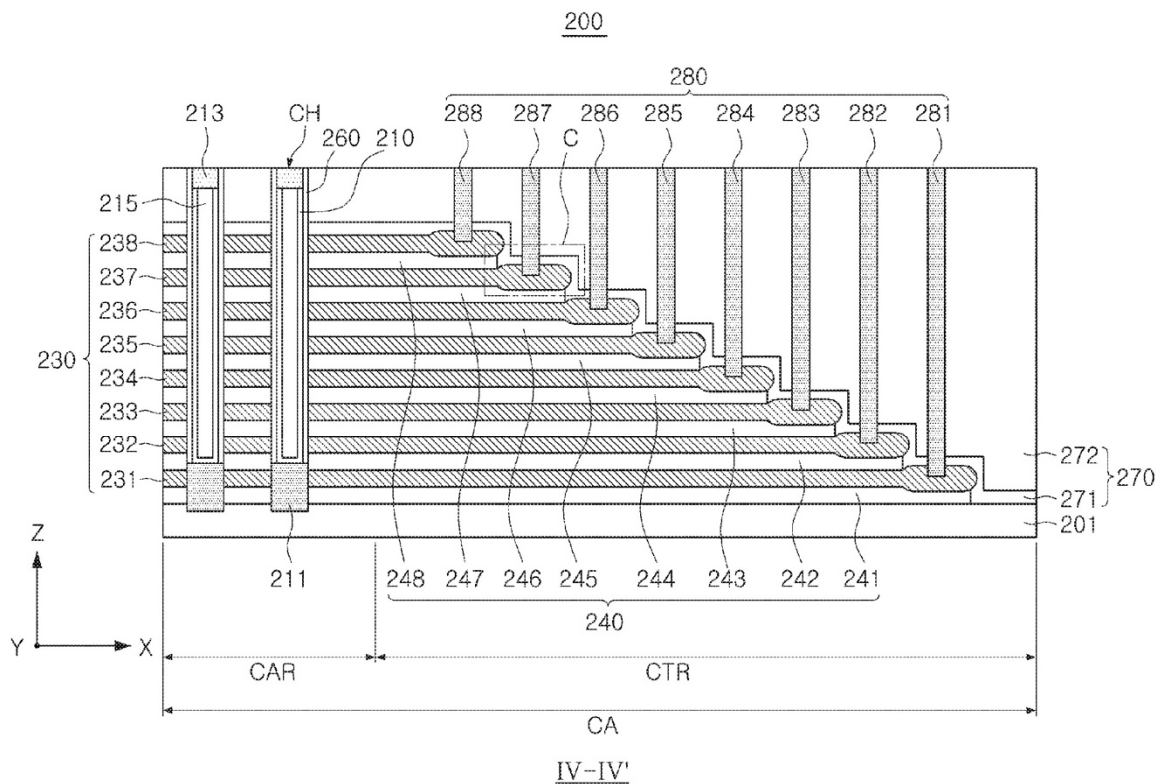
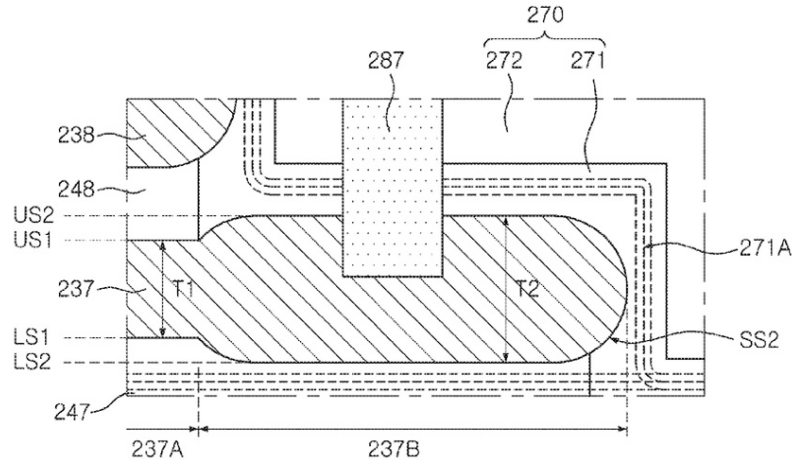


FIG. 7

Id., Fig. 7. Figure 8A shows the contact pad in greater detail:



C
FIG. 8A

Id., Fig. 8A.

C. Lee

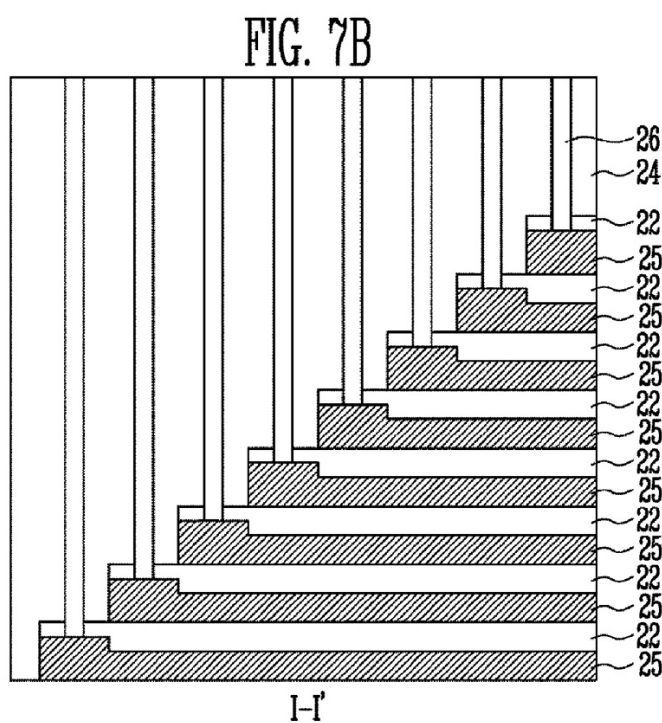
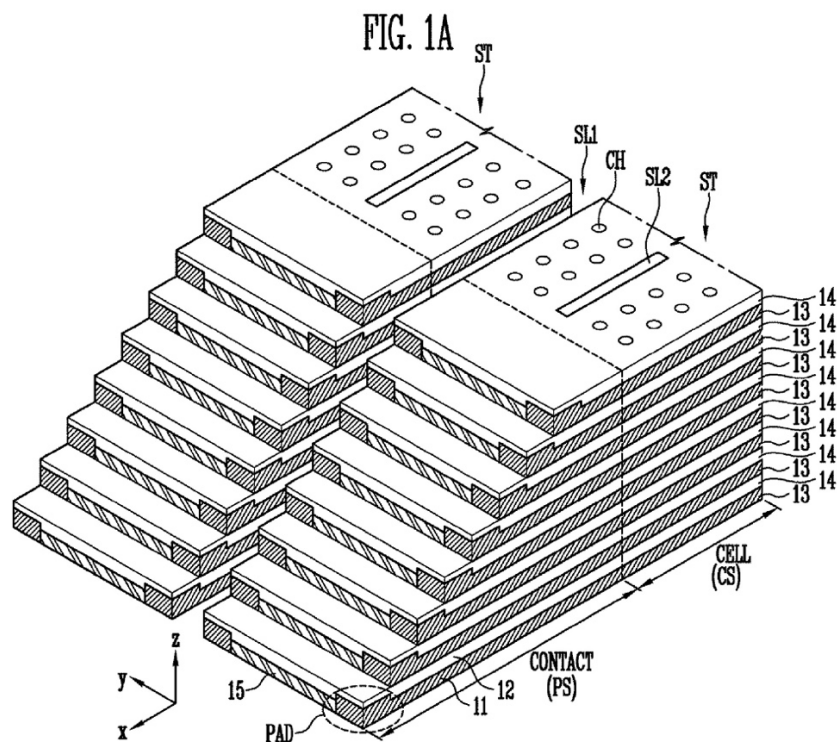
Lee was filed in the U.S. on March 18, 2013 and published on July 10, 2014.

Lee, Cover. It is prior art under AIA §§ 102(a)(1) and 102(a)(2).

Lee relates to “semiconductor device[s]” such as “three-dimensional (3D) non-volatile memory devices.” Lee, ¶¶ [0005], [0008]-[0009]. Per Lee, this type of device is intended to “increase[] ... integration” of a memory by including more memory cells in a smaller space. *Id.*, ¶ [0005]. This type of memory includes “interlayer insulating layers and word lines stacked alternately with each other” over a substrate. *Id.*, ¶ [0006]. “[C]hannel layers” pass through the stack to form “[m]emory cells.” *Id.* The stack is “patterned stepwise” to allow for connection or contact with each layer. *Id.*, ¶ [0009].

According to Lee, existing three-dimensional memories encountered difficulties when “form[ing] pad portions on word lines stacked on top of one another....” *Id.*, ¶ [0007]. In these devices, “a punch phenomenon may occur in which a contact plug passes through a pad portion, or the contact plug and the pad portion are not coupled to each other since a pad portion is not exposed along a bottom surface of a contact hole.” *Id.*

Lee then goes on to discuss a “semiconductor device” that, like known three-dimensional memories, includes a “stacked structure ST” with alternately arranged “insulating layers” and “conductive layers.” *Id.*, ¶¶ [0020]-[0021]. The “stacked structure ST” is “patterned stepwise” with an “insulating layer ... located on [the] top surface of each step.” *Id.*, ¶ [0021]. To address the problems with prior art memories, however, Lee includes “pad portions PAD” at the end of each of conductive layers in a “contact region CONTACT” of its stepped “stacked structure ST.” *Id.*, ¶¶ [0022]-[0023]. “The pad portions PAD” have a “greater thickness than unexposed portions of the ... conductive layer[s].” *Id.*, ¶ [0023]. Use of a thicker pad prevents the various contact problems experienced by prior art devices. *See id.*, ¶ [0043]. Lee’s pads are shown in both Figures 1A (a three-dimensional view) and 7B (a cross-sectional view):



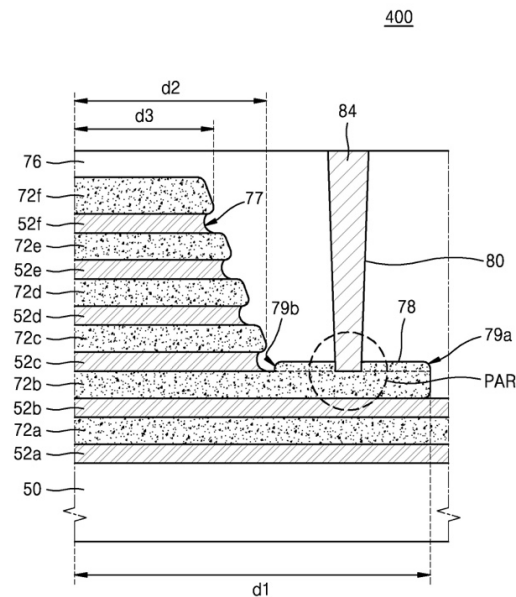
Id., Figs. 1A, 7B.

D. Park

Park was filed in the U.S. on June 13, 2017 and issued on May 21, 2019. Park, Cover. It is prior art under AIA § 102(a)(2).

Park relates to a “vertical semiconductor device” with an array of “stacked” “memory cells.” Park, 1:14-16. The device includes a stepped “connection region” with alternating conductive gate electrodes and insulating layers. *Id.*, 6:7-12. Raised “[p]ad region[s] PAR” are located on the ends of gate electrodes. *Id.*, 6:7-12, 6:36-47, 7:4-16. Rather than having straight sides, an “end 79b” of each of these “raised pad portion 78” may be “rounded” to “prevent a short circuit” between the pad and an “adjacent ... conductive layer pattern 72c.” *Id.*, 11:35-41. This is shown below:

FIG. 7



Id., Fig. 7.

IX. The '666 Patent's Claims Are Obvious

A. *Ground 1: Claims 17, 19, and 20 Are Obvious Over Kim*

Kim, when considered in view of the knowledge of a POSITA, renders claims 17, 19, and 20 obvious.

1. Claim 17

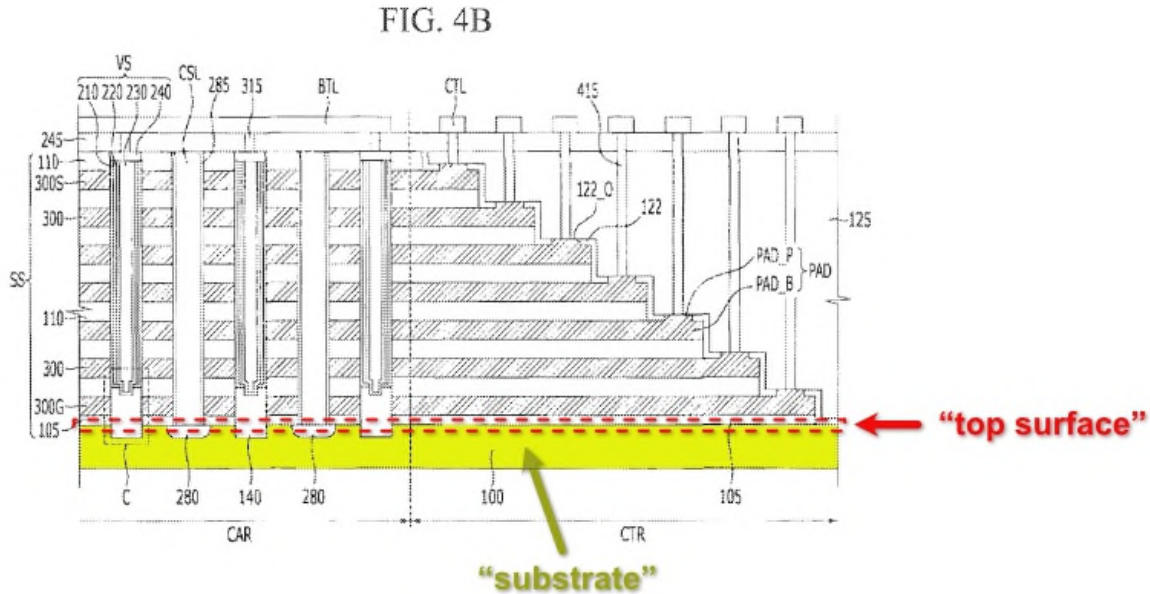
[17.Pre] “A memory device, comprising:”

To the extent this preamble language is limiting, it is taught by Kim. In particular, Kim explains that it relates to “semiconductor memory devices” with “enhanced reliability.” Kim, 1:38-39; *see also id.*, Abstract; 1:15-17; 3:43-44; Fig. 1. This device can be implemented as a “3D semiconductor memory device[]” with “memory cells ... arrayed in 3D” for purposes of improving “integration.” *Id.*, 1:26-30; *see also id.*, Figs. 3, 4A, 4B, 5-9; Ex. 1003, ¶¶ 136-140.

[17.A] “a substrate, wherein the substrate comprises a top surface;”

Kim teaches a “**substrate**” with a “**top surface.**” More specifically, Kim explains that its “semiconductor memory device” includes a “substrate 100.” Kim, 5:33-39. This “substrate 100 may include a semiconductor material and may be, for example, a silicon substrate, a germanium substrate, a silicon-germanium substrate, or a silicon-on-insulator (SOI substrate).” *Id.*, 5:40-44. Further, the “substrate” includes an “upper surface” on which “a plurality of gate electrodes” are “stacked.” *Id.*, 2:3-10; *see also id.*, 5:45-52 (similarly referencing the “uppermost surface of the substrate 100”); 6:7-9, 6:37-38, 13:35-38 (same). Kim’s substrate—along with the

substrate's top or upper surface—are annotated in Figure 4B below:

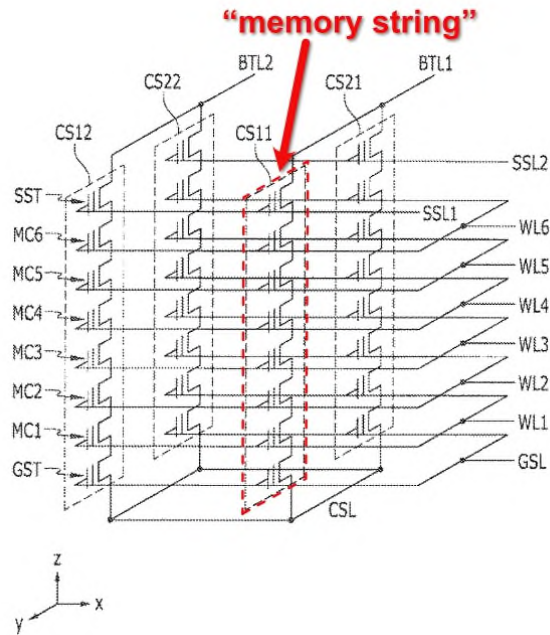


Id., Fig. 4B (annotated); see also Ex. 1003, ¶¶ 141-144.

[17.B] “a memory string disposed over the substrate; and”

This is also taught by Kim. Here, Kim explains that its “semiconductor memory device” includes a “cell array region” on the substrate. Kim, 1:41-46. This “memory cell array may include a plurality of cell strings....” *Id.*, 4:26-28. Because Kim teaches “memory cells which are arrayed in 3D[,]” the “cell strings” have a “vertical structure” and thus “extend[] in a vertical direction (z direction) to a plane of a substrate.” *Id.*, 1:28-30; 4:28-31. One such memory cell string—labeled CS11—is annotated in Figure 3 below:

FIG. 3

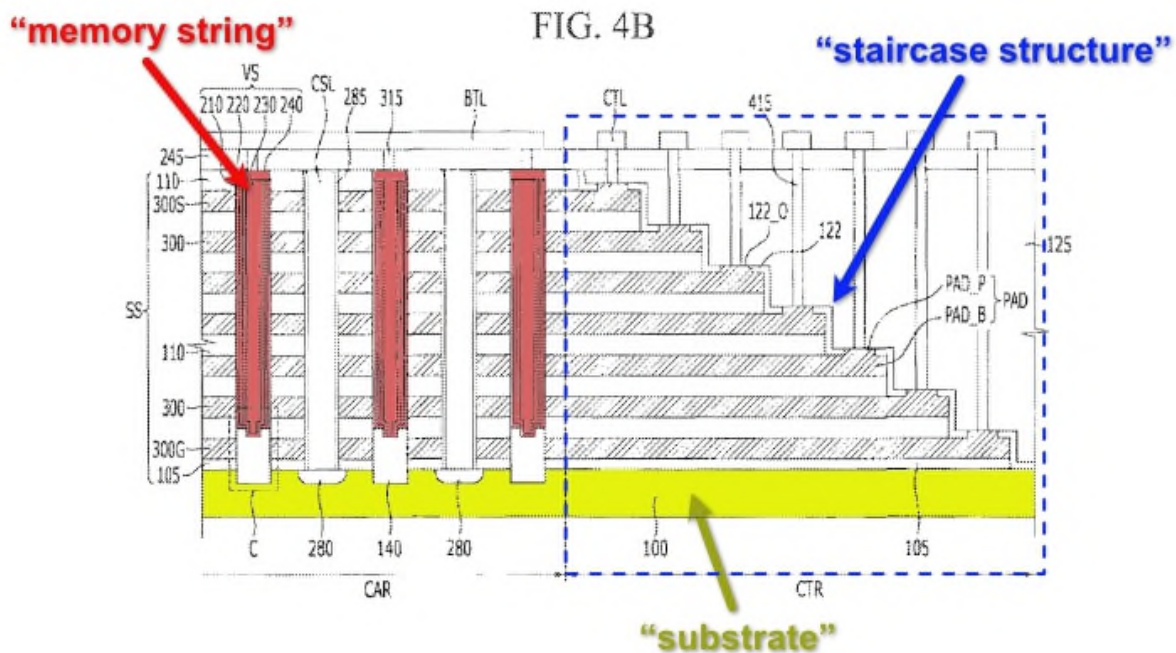


Id., Fig. 3 (annotated); *see also id.*, Fig. 4B (showing a vertical stacking structure “VS” that is located over Kim’s substrate 100 and forms a vertically oriented string of memory cells); Ex. 1003, ¶¶ 145-149.

[17.C] “a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises;”

This is also taught by Kim. According to Kim, its “semiconductor memory device[]” includes “stepwise structures.” Kim, 1:15-17. More particularly, the “semiconductor memory device” includes both a “cell array region” and an adjacent “contact region.” *Id.*, 1:40-47. The “contact region” includes a “stacking structure” with a “stepwise structure.” *Id.* Figure 4B provides an example. As shown, Kim’s device includes a “cell array region (CAR)” that includes “vertical pattern

structure[s] VS” forming strings of memory cells. *Id.*, 5:33-39. A “contact region CTR” with a stepped structure is “positioned on the periphery of the cell array region CAR.” *Id.*; *see also* 3:52-62 (similarly explaining that Kim’s “memory device” includes a “cell array region (CAR)” with “a plurality of memory cells” and an adjacent “contact region CTR”); 6:42-46 (the “vertical pattern structures VS” are “surrounded by the” step-shaped “stacking structure SS on an xy-direction plane”). Both Kim’s “*staircase structure*” (stepped contact region CTR) and example “*adjacent*” “*memory string[s]*” (vertical structures VS) are annotated below:



Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 150-156.

[17.C.1] “a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer,”

Claim 17 next requires a “*plurality of layer stacks*” where each “*layer stack*”

includes an ***“insulating”*** and ***“conductive” “layer.”*** The ***“insulating layer”*** must be ***“disposed over”*** a ***“first portion of a conductive layer.”***

Besides requiring that each “layer stack” include insulation over a conductive layer, nothing further is required by this limitation. For instance, the insulation and conductive material do not need to be coextensive. Indeed, the claim itself provides that insulation is only required to be “over” a “portion” of the underlying conductive layer. This is also what the ’666 patent’s figures show. *See, e.g.* Ex. 1001, Fig. 8 (showing each insulation layer 502 covering only a portion of the underlying conductive layer 804). Nor do the layers need to cooperate in any particular way to form a step in the claimed staircase structure. The claim simply requires that that “staircase structure” include a “plurality of layer stacks.” The layers must be part of the staircase. But no particular layer—insulation or conductive material—is required to form the top of the steps in the staircase. The claim also does not require that the entirety of the “staircase structure” from top to bottom be formed from insulation over conductive material. Instead, there simply must be a “plurality of layer stacks” (*i.e.*, more than one), where each such layer stack includes insulation over conductive material.

It would also be wrong to limit the claimed “layer stack” to a structure like that shown in Fig. 2A. This figure depicts a preliminary stage of manufacture before the formation of landing pads and other structure. Claim 17 covers the finished

structure shown in Figure 8, not the preliminary structure in Fig. 2A. Indeed, numerous required claim limitations are missing from Fig. 2A. Among other things, this figure's structure lacks both "conductive layer[s]" (the layers in the figure are sacrificial, not conductive) and the claimed "second portion" with a "curved side surface" (there are no landing pads at all, let alone pads with a curved side surface). Nor does the specification of the '666 patent include a definition of the term "layer stack" that would cause it to require co-extensive conductive and insulating layers or exclude what Kim discloses. The term "layer stack" is used in several places throughout the '666 patent. For instance, the patent notes that a "layer stack" or "staircase layer" 'exposes ... a portion of a top surface of a layer stack.' Ex. 1001, 5:59-67. This is not definitional. Moreover, nothing about this imposes a requirement that there be insulating material fully covering the top of every "layer stack." Again, this cannot be required because it is not what the '666 patent discloses. In Figure 8, each insulating layer covers only a portion of the underlying conductive layer that it pairs with to form a "layer stack." *See id.*, Fig. 8.

Next, the '666 patent also uses the term "layer" broadly. According to the patent, a "layer" does not need to be only a single, defined layer of homogenous material. Instead, a "layer can include **multiple** layers" and can be "**inhomogenous**." Ex. 1001, 4:36-56 (emphasis added). The patent also explains that a "layer" can simply be material "located between any set of horizontal planes...." *Id.*, 4:45-48.

Kim teaches what this limitation requires. Kim's memory device includes a step-shaped "stacking structure SS" formed from a "plurality" of alternating "insulating layers 110 and ... gate electrodes 300" located "on the substrate 100." Kim, 5:53-55; *see also id.*, 1:41-46 (the "stacking structure" includes "a plurality of insulating layers and a plurality of gate electrodes alternately stacked on the substrate. The stacking structure may" have "a stepwise structure....").

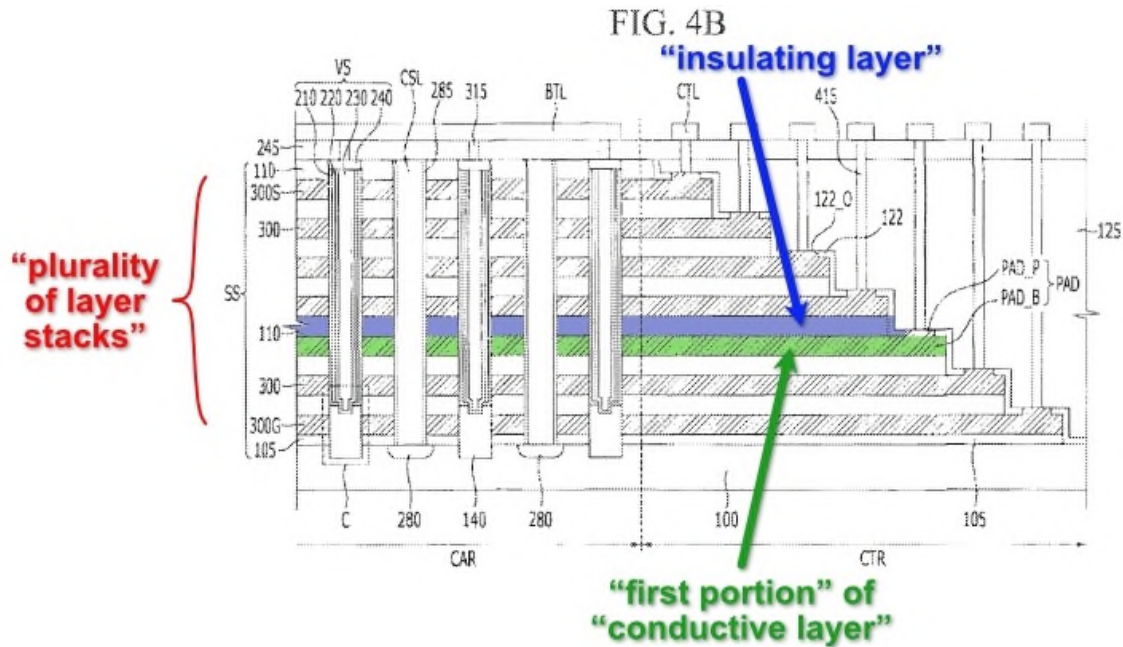
According to Kim, "[t]he plurality of insulating layers 110 may be, for example, silicon oxide layers." *Id.*, 6:35-36. Kim also explains that its device includes an "auxiliary insulating layer 122." *Id.*, 9:12-13. "The auxiliary insulating layer 122 may include the same or similar material as the insulating layer 110" such that "a boundary between the auxiliary insulating layer 122 and the insulating layer 110 may not be distinguished and the auxiliary insulating layer 122 and the insulating layer 110 may form one structure." *Id.*, 9:29-38. Moreover, right after patterning the staircase, Kim forms the auxiliary layer 122, such that portions of the conformal insulating layer becomes "one structure" with the insulating layers 122 to extend the insulating layers in the horizontal direction. *Id.*, 12:34-37. The "gate electrodes 300" can be formed from conductive material such as, among other things, "metal (for example, tungsten, copper, and aluminum)..." *Id.*, 6:31-35.

A POSITA would have understood that Kim's insulating layer 110 and the adjacent portion of auxiliary insulation layer 122 together constitute the claimed

“insulating layer” in a **“layer stack.”** See Ex. 1003, ¶¶ 157-172. Layers 110 are located between and serve to separate the gate electrodes 300 making up Kim’s stack. Kim, 5:53-55; Fig. 4B. Further, layer 122 also forms an integral part of this same stack. Layer 122 is not simply a conformal or protecting layer of oxide applied over complete conductive layers with contact pads. Instead, this layer is applied **before** Kim’s contact pads are formed. See *id.*, 12:34-37; Fig. 11. Moreover, the layer is used to form the contact pads: the pads are formed within a shaped opening etched in this insulating layer 122. See *id.*, 12:61-13:11, 13:51-14:17; Figs. 13, 16, 17. The layer 122 remains behind in Kim’s final device. See, e.g., *id.*, Fig. 17. Put another way, unlike other layers in Kim like “buried insulating layer 125” (see *id.*, 9:56-63), layer 122 does more than simply cover and protect the staircase’s conductive layers. It is used to define and is thus part of Kim’s stacked staircase structure. See Ex. 1003, ¶¶ 173-181. Because of this, and because these layers are formed from the same material such that they “form one structure” as Kim explains, a POSITA would have understood that they together form an **“insulating layer.”** *Id.* Again, the ’666 patent plainly embraces insulating layers—like that taught by Kim—formed from multiple components. See Ex. 1001, 4:36-56 (explaining that a “layer” can be “inhomogeneous” and formed from “multiple” layers). Moreover, consistent with the ’666 patent’s explanation that a “layer” can be the material “located between any set of horizontal planes” (*id.*, 4:45-48), in Kim insulating layer 110 and the

adjacent portion of auxiliary insulating layer 122 are located between the planes formed by the bottom of one gate electrode 300 and the top of another gate electrode 300. *See, e.g.*, Kim, Fig. 4B.

An example **“layer stack”** including an **“insulating layer”** (the combination of Kim’s insulating layer 110 and auxiliary insulating layer 122) and **“conductive layer”** (the gate electrode 300) are annotated in Figure 4B below. As shown, the **“insulating layer”** is **“disposed over a first portion”** of the depicted **“conductive layer.”** This same insulation-over-conductive-material structure is repeated throughout Kim’s device. Thus, Kim includes a **“plurality of layer stacks”** (there are multiple pairs of insulation on top of conductive material in Kim’s stacking structure SS). Moreover, although claim 17 does not require that the entirety of the **“staircase structure”** be formed from layers of insulation on top of conductive material, this is taught by Kim. In each layer of Kim’s stacking structure from the top to the bottom, an insulating layer 110 (and auxiliary insulating layer 122) is located over a gate electrode 300:

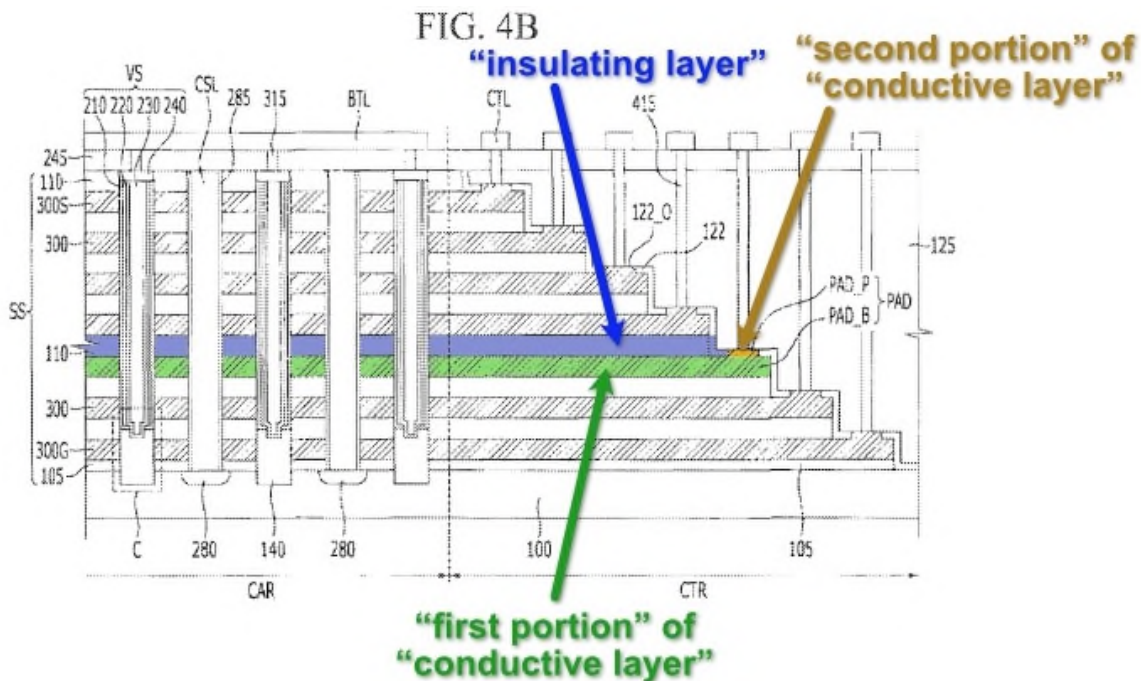


Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 182-185.

[17.C.2] “wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.”

Kim, in view of the knowledge of a POSITA, renders this limitation obvious. Again, Kim’s “stacking structure SS” includes alternating “insulating layers 110 and ... gate electrodes 300[.]” Kim, 5:53-55. Per Kim, “[a]n end of” each “gate electrode 300” is “exposed through the stepwise structure” and includes a “pad unit PAD” formed from “a base pad PAD_B and a protrusion pad PAD_P...” *Id.*, 7:58-62. “The base pad PAD_B may be a part of the gate electrode 300 in the contact region CTR.” *Id.*, 7:63-64. “The protrusion pad PAD_P may contact the ... uppermost surface of the base pad PAD_B.” *Id.*, 8:3-10; *see also id.*, 7:61-62 (noting that the “protrusion pad PAD_P contact[s] a surface of the base pad PAD_B”); 10:23-25 (similarly referencing location of “the protrusion pad PAD_P” on a

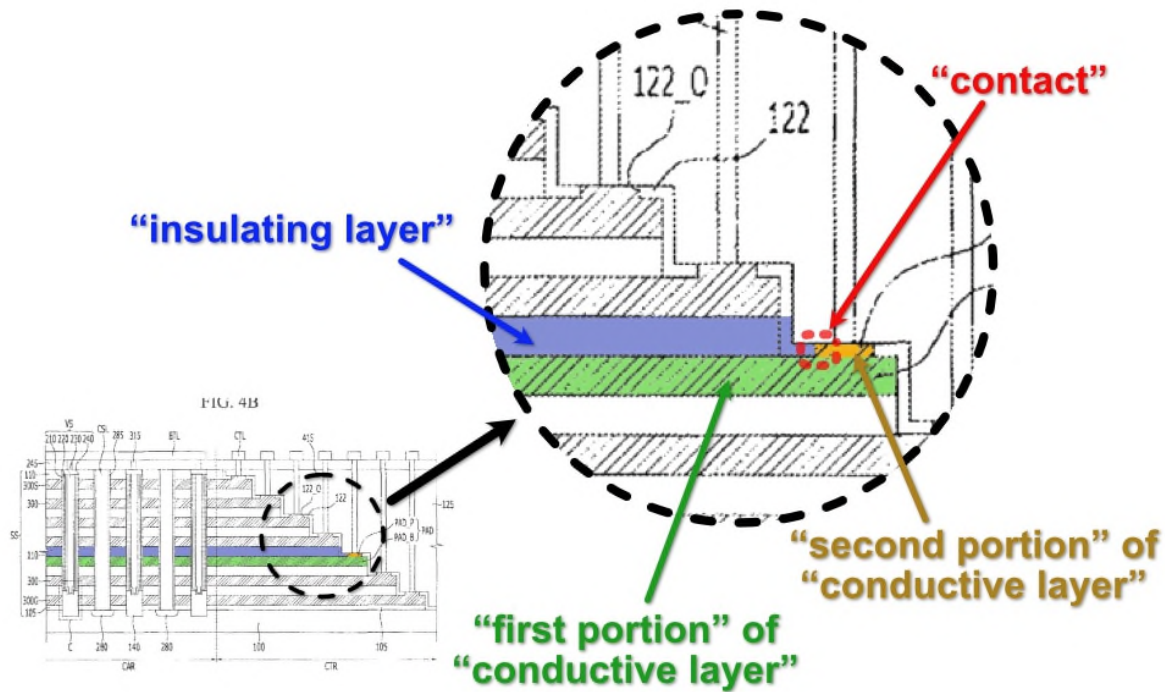
“surface of the base pad PAD_B”). The pad units PAD “electrically and physically connect” the gate electrodes 300 to a “connection line CTL” via a “word line contact plug 415.” *Id.*, 9:64-67. The “gate electrode 300” and the attached “base pad PAD_B and ... protrusion PAD_P” may be formed from the same “common material composition” such as a “metal.” *Id.*, 6:31-35, 14:12-17. This is shown in the below annotated version of Figure 4B. Kim’s device includes both a “**conductive layer**” with both a “**first portion**” (gate electrode 300 and attached base pad PAD_B) and “**second portion**” (protrusion pad PAD_P):



Id., Fig. 4B (annotated); see also Ex. 1003, ¶¶ 186-193.

Next, the components of Kim’s device are also in “**contact**” as this limitation requires. As explained, Kim’s stacking structure includes “insulating layers 110” and “auxiliary insulating layers 122” made from the same material such that they

“form one structure.” Kim, 9:29-38; *see also id.*, 12:34-37, Fig. 11 (insulating layers 110 and auxiliary insulating layer 122 formed sequentially before contact pads). Together, layers 110 and 122 correspond to the claimed **“insulating layer.”** *See* Ex. 1003, ¶¶ 194-196. Kim also explains that “auxiliary insulating layer 122” has an “opening 122_O and the protrusion pad PAD_P” is located “inside” this “opening 122_O.” *Id.*, 9:21-23; *see also id.*, 13:51-14:17, Figs. 16-17 (opening 122_O filled with conductive material to form PAD_P during gate electrode forming process). Because Kim’s protrusion pad PAD_P is located within and fills the opening 122_O in its auxiliary insulation layer 122, there is **“contact”** between a **“side surface”** of Kim’s **“second portion”** (the protrusion pad PAD_P) and a **“side surface of the insulating layer”** (the side walls of opening 122_O in auxiliary insulating layer 122):

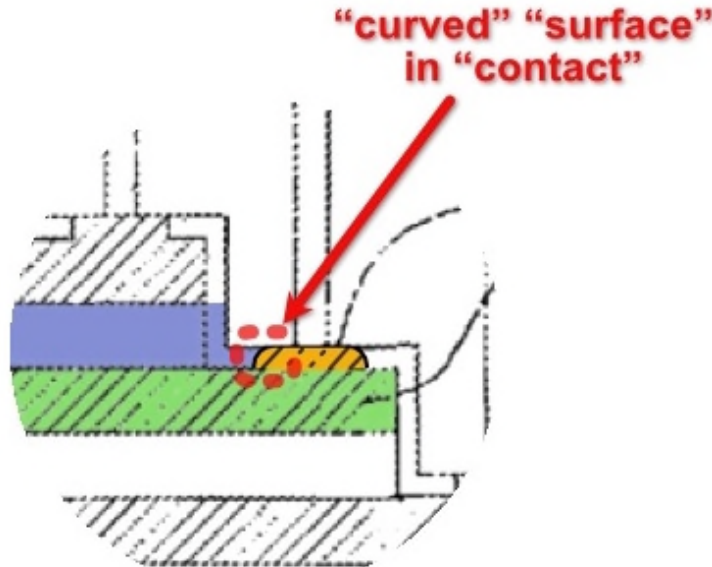


Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 197-199.

Finally, Kim also teaches that the “*side surface*” of its “*second portion of the conductive layer*” that is in “*contact*” with its “*insulating layer*” is (or at the very least obviously can be) “*curved*.” Kim explains that while its figures show “[e]mbodiments ... in which the protrusion pad PAD_P has a rectangular parallel[] shape[,]” “the protrusion pad PAD_P is not limited thereto and ... may have a shape including a curved surface based on a virtual rectangular parallel[] shape, a cylindrical shape, or any shape.” Kim, 8:29-34. A POSITA would have understood that this teaches a variety of different protrusion pad PAD_P shapes, many of which have the type of “*curved*” side surface claim 17 requires.

For example, a POSITA would have understood that when Kim references a

“curved surface based on a virtual rectangular parallel[] shape,” PAD_P would obviously be shaped in the manner shown in the demonstrative below:

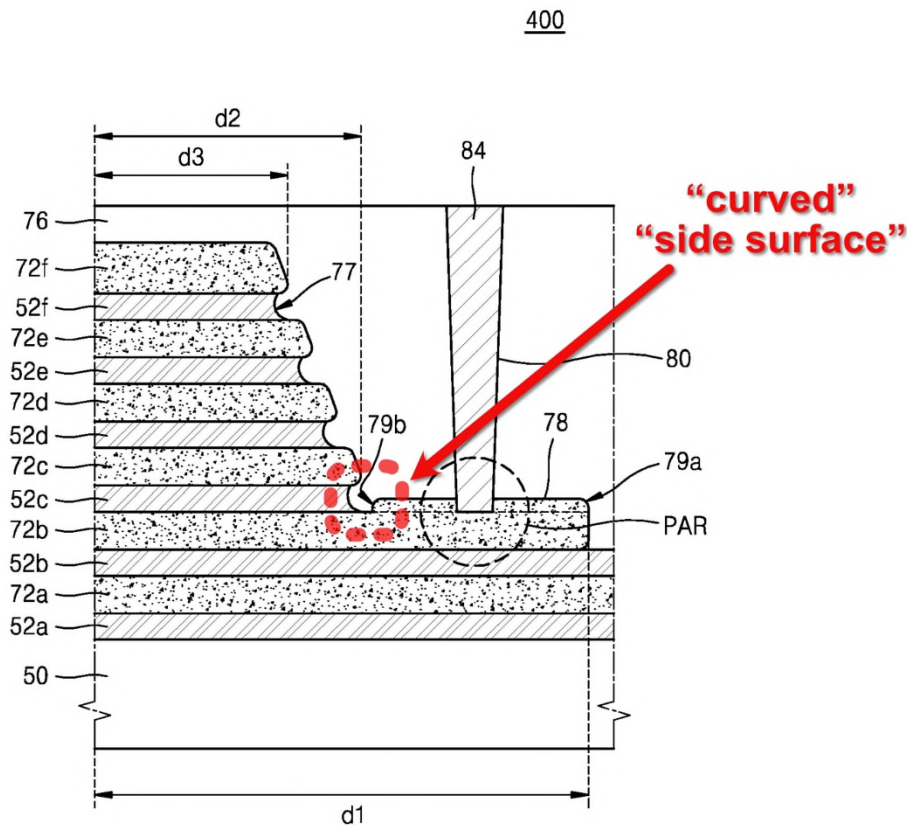


Ex. 1003, ¶¶ 200-203 (annotated, modified). As can be seen, just as Kim teaches, the pad continues to have a generally rectangular shape. And it continues to be located in the opening in auxiliary insulation layer 122. But now, the pad’s sides are “curved” in the area where they contact auxiliary insulation layer 122. Kim, 8:29-34; *see also* Ex. 1003, ¶ 203.

Contact pads with this type of “curved” side surfaces were well-known in the art at the time the ’666 patent was filed. For example, a reference to Park (Ex. 1008) teaches a “vertical semiconductor device” with an array of “stacked” “memory cells.” Park, 1:14-16. Park’s device—like Kim’s—includes a stepped “connection region” with “pad region[s] PAR” located on the end of gate electrodes. *Id.*, 6:7-12, 6:36-47. Each “pad region PAR” includes a “raised pad portion 28.” *Id.*, 7:4-16.

Park goes on to explain that the “end 79b” of the “raised pad portion 78” may be “rounded” to “prevent a short circuit” between the pad and an “adjacent ... conductive layer pattern 72c.” *Id.*, 11:35-41. This is shown in Figure 7 from Park below:

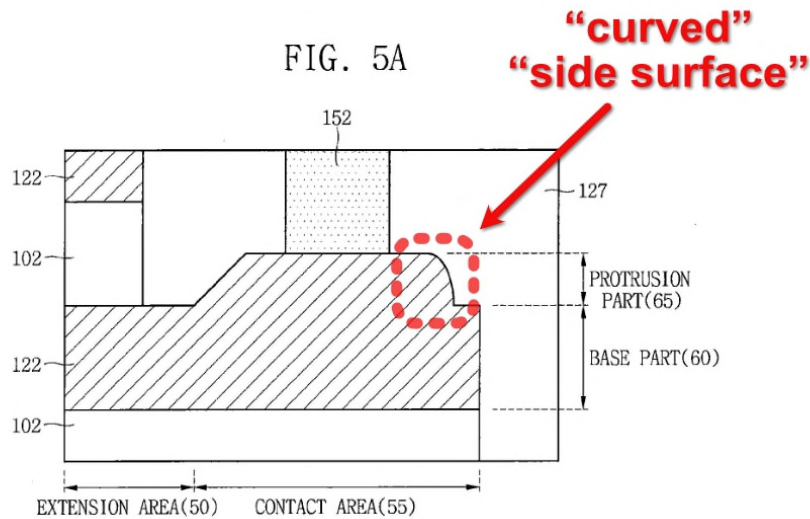
FIG. 7



Id., Fig. 7 (annotated).

Another reference to Yun (Ex. 1018) also relates to a “semiconductor device[] having three-dimensionally arranged memory cells...” Ex. 1018, 1:33-35. The device has a “stepped” or “cascade structure.” *Id.*, 9:22-25. The steps hold “contact

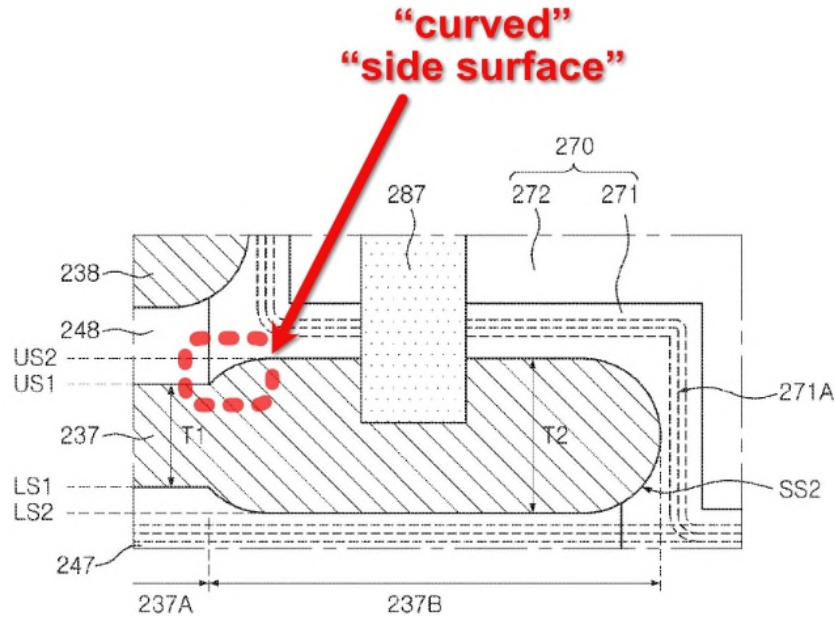
area[s] 55” that are “co-planar with” the device’s “gate electrodes” and have both a “base part 60 and a protrusion part 65.” *Id.*, 8:15-28. Per Yun, the “protrusion part 65” may have either “inclined” or “rounded” “side surface[s].” *Id.*, 8:33-40. An example of this is shown below (with the “rounded” surface shown on the right side of the contact pad):



Id., Fig. 5A (annotated).

A reference to Nam (Ex. 1006) provides yet another example. Nam—like Kim, Park, and Yun—teaches a “semiconductor device” formed from memory cell strings arranged in a three-dimensional array. See Nam, ¶¶ [0005], [0025], [0033]; Fig. 2. Gate electrodes connecting to the memory cells may “have a stepped shape having step structures.” *Id.*, ¶ [0043]. Layers of insulation are located between the gate electrodes. *Id.*, ¶ [0043]. Each gate electrode includes a “pad region” at its end where “the gate electrode ... is connected to a contact 187.” *Id.*, ¶ [0057]. And,

among other shapes, as shown below this “pad region” can have a “bull nose” or “convex” shape. *Id.*, ¶ [0066].



C
FIG. 8A

Id., Fig. 8A (annotated); *see also* Ex. 1003, ¶¶ 204-218.

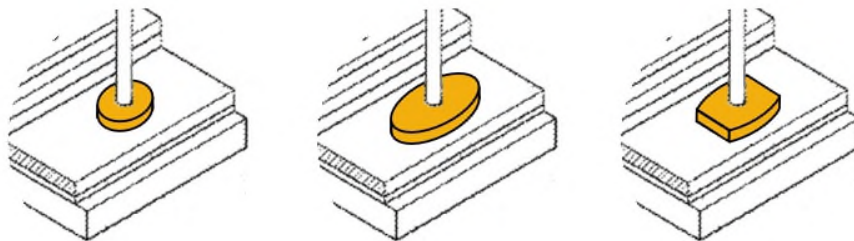
A POSITA would have been motivated to employ a contact pad with curved side surfaces when implementing Kim. To begin, Kim itself already contemplates that its pad can have a “curved surface.” Kim, 8:29-34. This type of pad was also well known in the art. *See, e.g.*, Park, Fig. 7; Yun, Fig. 5A; Nam, Fig. 8A. Thus, contact pads with curved side surfaces would have been among the available design choices a POSITA would have considered for use. *See* Ex. 1003, ¶¶ 219-222. Additionally, a POSITA would have recognized that using a “curved” side surface with Kim’s pads would have improved Kim by increasing the minimum distance

between the pad and adjacent conductive layers, thereby reducing the risk of short circuit. *See* Park, 11:35-41. This would have further motivated use of such a pad with Kim. *See* Ex. 1003, ¶¶ 223-225.

A POSITA would also have had every reason to believe that a curved pad could be successfully used with Kim. Again, this is one of the shapes that Kim already contemplates and deems acceptable. *See* Kim, 8:29-34. And it had also been successfully used in other semiconductor memory devices with stepped structures. *See, e.g.*, Park, Fig. 8; Yun, Fig. 5A. Moreover, Kim explains that the opening in auxiliary insulation layer 122 that will eventually contain its protrusion pad PAD_P obtains its shape via an “ion injection process.” Kim, 13:1-11. More particularly, Kim explains that ion injection is used to form an appropriately shaped “doped region 122_I” in auxiliary insulating layer 122. *See id.* This doped region is then etched away to form “opening 122_O” “simultaneously with the process of removing the sacrificial layer 120” which forms “gaps 260.” *Id.*, 13:55-14:8. Then both the gaps 260 and openings 122_O are filled with conductive material to form the gate electrodes and pads. *See id.*, 14:9-17; *see also* Figs. 12-16. A POSITA would have recognized that this process could be readily adapted to form a curved opening that surrounds a curved contact pad. *See, e.g.*, Park, 7:17-29 (referencing the use of “ion implantation” and “oxidation” to form a “raised pad portion” with “rounded” sides); Nam, ¶¶ [0066], [0098]-[0107]; Figs. 30-39 (discussing and

depicting the use of “an ion implantation process” to form a “convex” contact pad). Ion implantation would be employed to form a “doped region 122_I” with a rounded as opposed to rectangular shape resulting in a contact pad with rounded sides once the gate and pad formation process is completed. See Ex. 1003, ¶¶ 226-238.

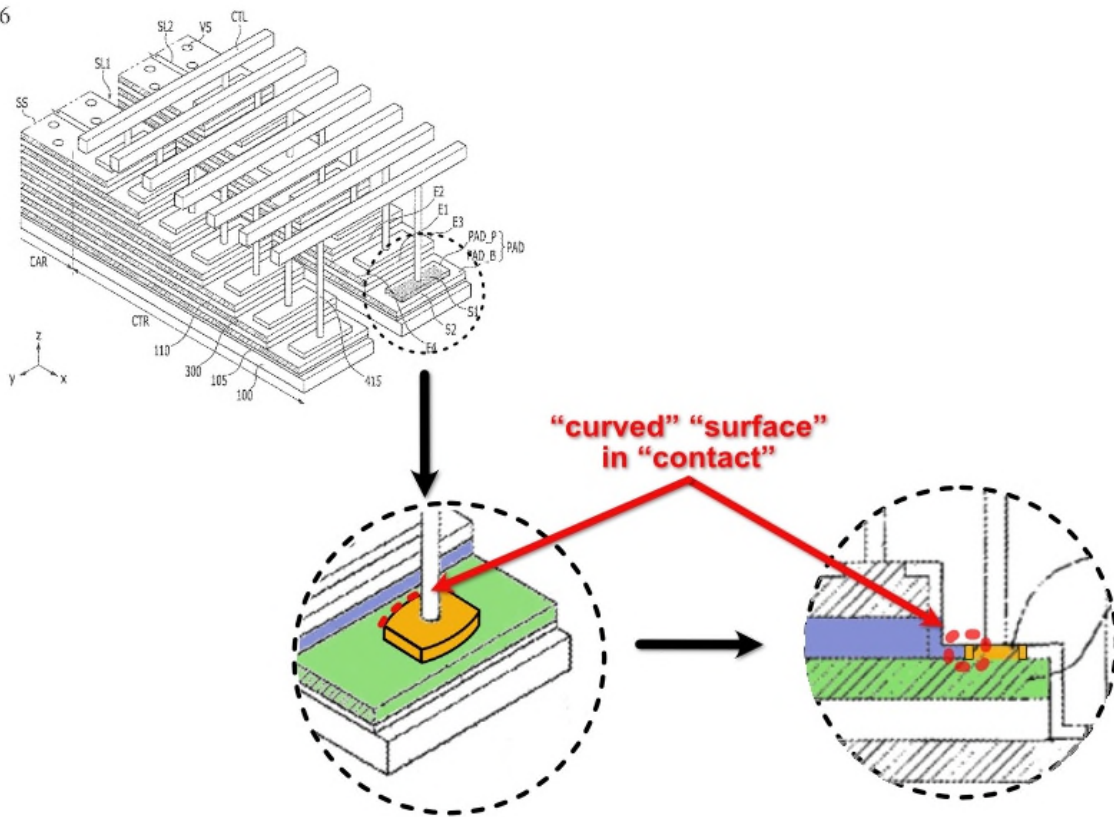
Next, a POSITA would have understood that Kim’s “cylindrical[ly]”-shaped protrusion pads PAD_P also include the type of “**curved**” surface that claim 17 requires. A POSITA would have understood that a “cylindrical” contact pad can be implemented as, for instance, a right cylinder, an elliptical cylinder, or even a generally rectangular pad with two sides that follow a cylindrical pattern. . This latter shape is another way a POSITA would obviously have followed Kim’s instruction to form a pad with a “curved surface based on a virtual rectangular parallel[] shape....” See Ex. 1003, ¶¶ 239-240; Kim, 8:29-34. Examples of how a POSITA would have understood these pads to be shaped are shown below:



Ex. 1003, ¶ 241. Employing any of these “cylindrical” contact pads also results in the claimed “**conductive layer**” “**second portion**” having a “**curved**” “**side surface**” that is in “**contact**” with the side surface of Kim’s **insulating layer.**” This is shown

in the demonstrative below generated using Figure 6 of Kim. The rectangular protrusion pad PAD_P in that figure has been replaced with a pad with curved sides that follow a cylindrical shape. While auxiliary insulation layer 122 is not shown in the three-dimensional view of Figure 6, a side view has been added to the demonstrative below to show how the pad, even though now shaped with curved sides following the general shape of a cylinder, will continue to be located within the opening through and will contact the side of auxiliary insulation layer 122:

FIG. 6



Ex. 1003, ¶¶ 242-244. A POSITA also would have been motivated to employ this shape and would have expected to succeed when doing so. Kim itself identifies “cylindrical”-shaped contact pads as acceptable and contemplates their use. A

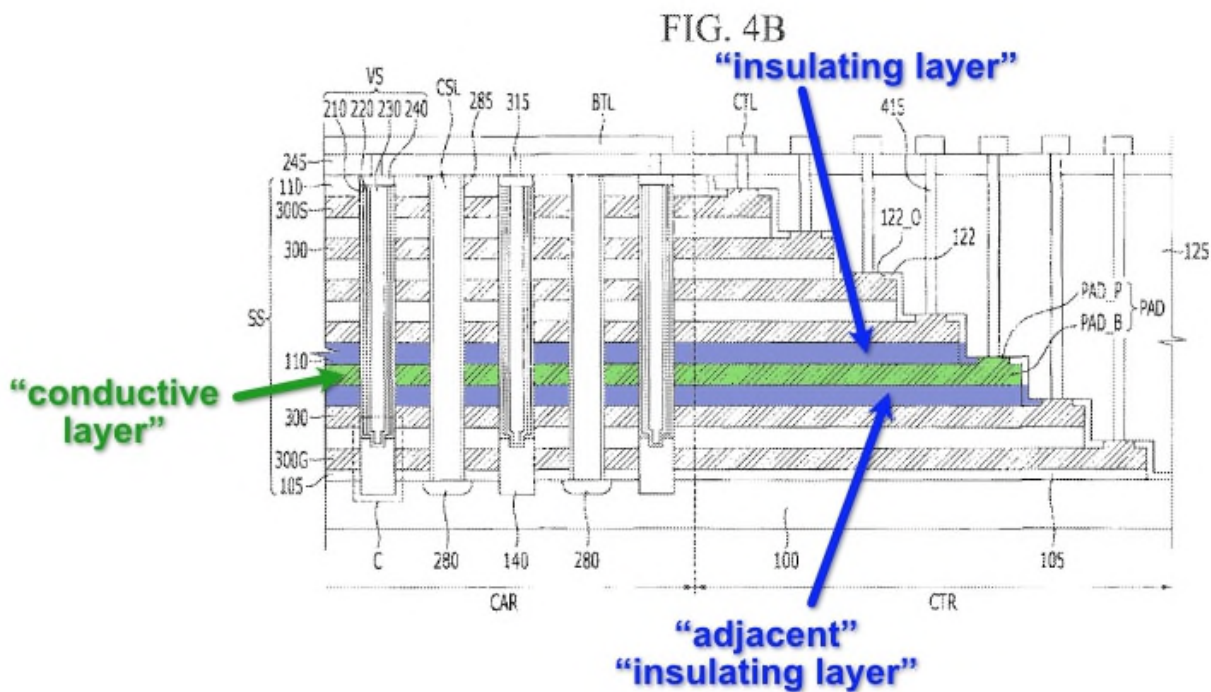
POSITA would consider this to be nothing more than a minor variation in design from the rectangular pads shown in Kim's figures. *Id.*, ¶¶ 245-247. And this type of pad could be made following the same process Kim employs to make its rectangular pad (just with differently shaped mask patterns to account for the curves of the cylinder). *See id.*, ¶ 248.

2. Claim 19

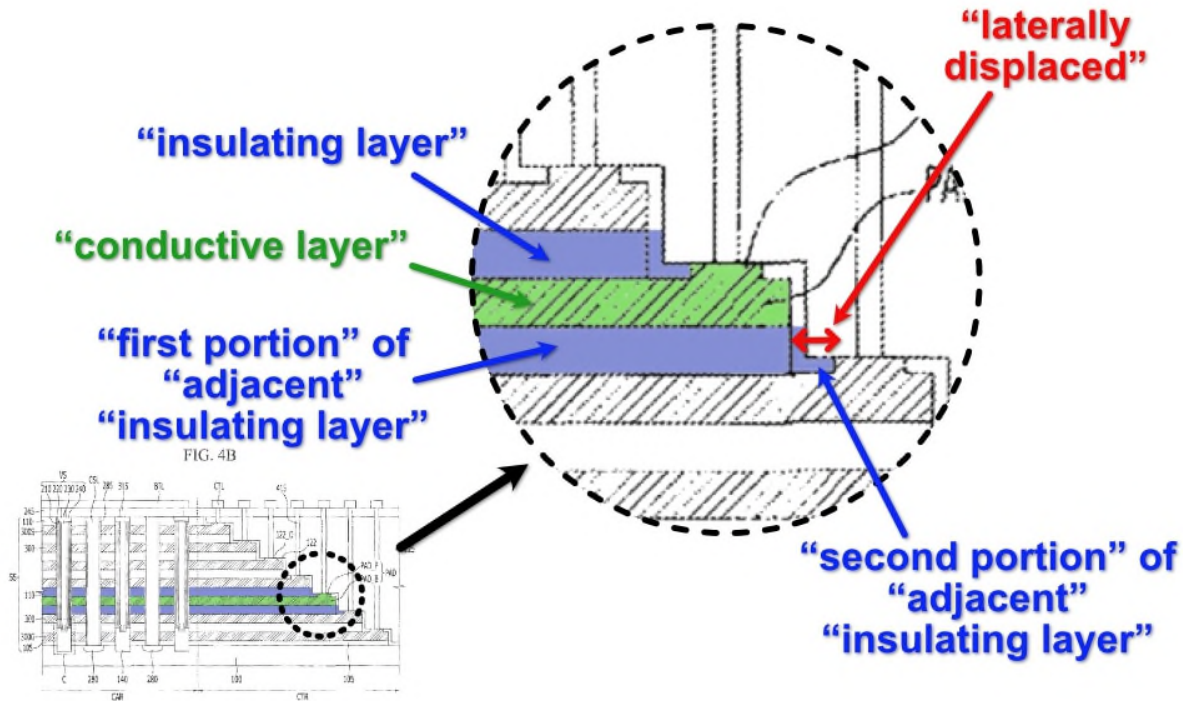
Claim 19 depends on claim 17 and further requires:

[19] “wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack”

This is taught by Kim. According to Kim, its “stacking structure SS” includes a “plurality” of alternating “insulating layers 110 and ... gate electrodes 300.” Kim, 5:53-55; *see also id.*, 1:41-46 (the “stacking structure” includes “insulating layers” and “gate electrodes” that are “alternatively stacked.”) Because it includes alternating conductive and insulating layers, each of Kim's “***conductive layer[s]***” (the gate electrode 300) is located over “***a first portion of the insulating layer of an adjacent layer stack***” (the insulating layer 110 immediately below the gate electrode):



Id., Fig. 4B (annotated); see also Ex. 1003, ¶¶ 250-252 . Further, each insulating layer 110 can be integrated with an “auxiliary insulating layer 122” such that layers 110 and 122 form “one structure.” Kim, 9:12-13, 9:29-38. As shown below, this causes a **“second portion of the insulating layer of the adjacent layer stack”** (the portion of auxiliary insulating layer 122 adjacent to layer 110) to be **“laterally displaced from the conductive layer”**:



Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 253-254.

3. Claim 20

Claim 20 depends on claim 17 and further requires that:

[20] “wherein the conductive layer comprises a first conductive material, and wherein the curved side surface comprises a second conductive material.”

This is also taught by Kim. According to Kim, its “gate electrode 300”—the claimed **“conductive layer”**—and the attached “base pad PAD_B and ... protrusion PAD_P”—which includes the claimed **“curved side surface”**—may be formed from the same “common material composition” such as a “metal.” Kim, 6:31-35, 14:12-17. While this claim does reference a “first conductive material” and “second conductive material,” these materials need not be different. *See, e.g.*, Ex. 1001, 1:55-59 (“The second material layer is made of a first conductive material. The plurality

of landing pads are made of a second conductive material. The first conductive material can be the same or different from the second material.”); *see also* Ex. 1003, ¶¶ 256-258.

B. Ground 2: Claims 17, 19, and 20 Are Obvious Over Nam

Nam, when considered in view of the knowledge of a POSITA, renders claims 17, 19, and 20 obvious.

1. Claim 17

[17.Pre] “A memory device, comprising:”

To the extent this preamble language is limiting, it is taught by Nam. In particular, Nam explains that it relates to a “memory device.” Nam, ¶ [0002]; *see also id.*, ¶ [0025]; Fig. 1. This memory device can be a “NAND flash device” with memory cells arranged in a three-dimensional array. *Id.*, ¶ [0032]; Fig. 2; *see also* Ex. 1003, ¶¶ 261-263.

[17.A] “a substrate, wherein the substrate comprises a top surface;”

Nam teaches a “**substrate**” with a “**top surface.**” More specifically, Nam explains that its “memory device” includes a “substrate 101” with an “upper surface.” Nam, ¶ [0038]; *see also id.*, ¶ [0005] (similarly explaining that Nam’s “semiconductor device includes ... a substrate”). The “upper surface of the substrate 101 may correspond to an X-Y plane” as shown in Nam’s figures. *Id.*, ¶ [0039]; *see also, e.g.*, Fig. 3. In Figure 7, reproduced below, this “substrate” is labeled as item 201. *Id.*, ¶ [0062].

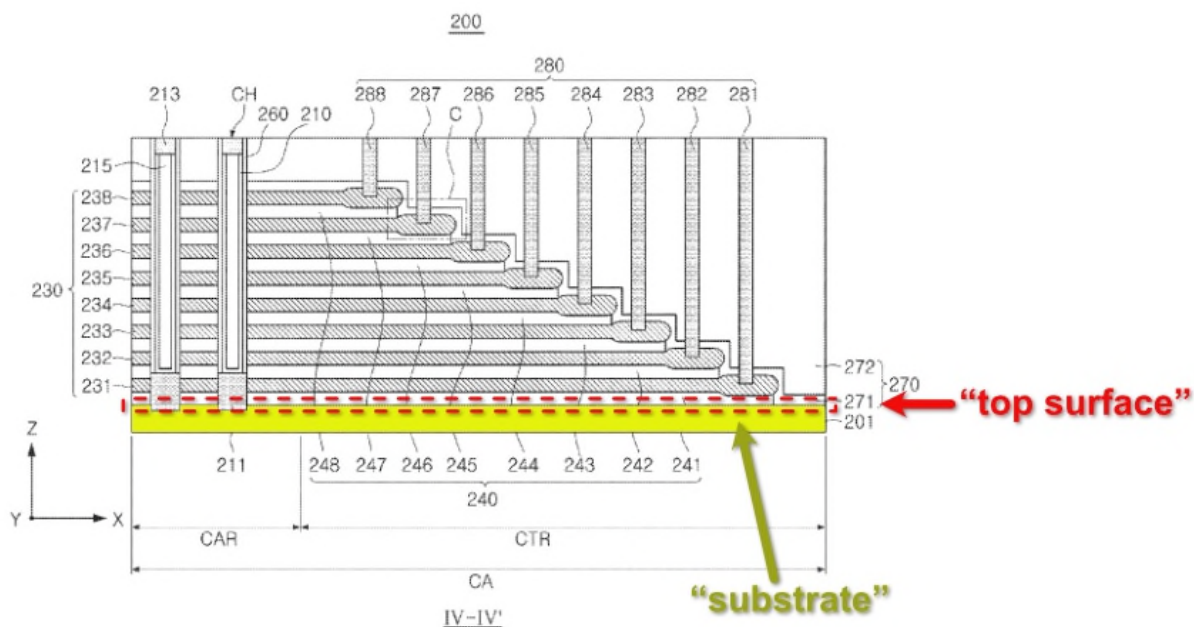
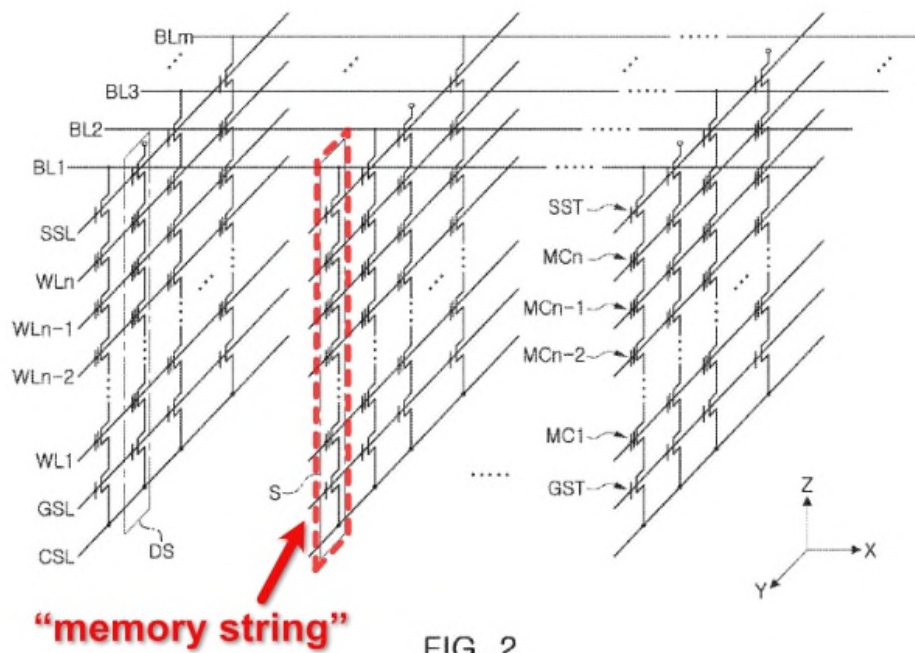


FIG. 7

Id., Fig. 7 (annotated); see also Ex. 1003, ¶¶ 264-267.

[17.B] “a memory string disposed over the substrate; and”

Nam includes “**memory strings**” that are “**disposed over**” its “**substrate.**” According to Nam, its “memory device” includes a “memory cell array” with “a plurality of memory cells arranged in a plurality of rows and a plurality of columns.” Nam, ¶¶ [0025]-[0026]. The “memory cell array may include a plurality of memory cell strings S[,]” each of which includes “memory cells MC1 to MCn connected to one another in series....” *Id.*, ¶ [0033]. One such memory string is annotated in Figure 2 below:

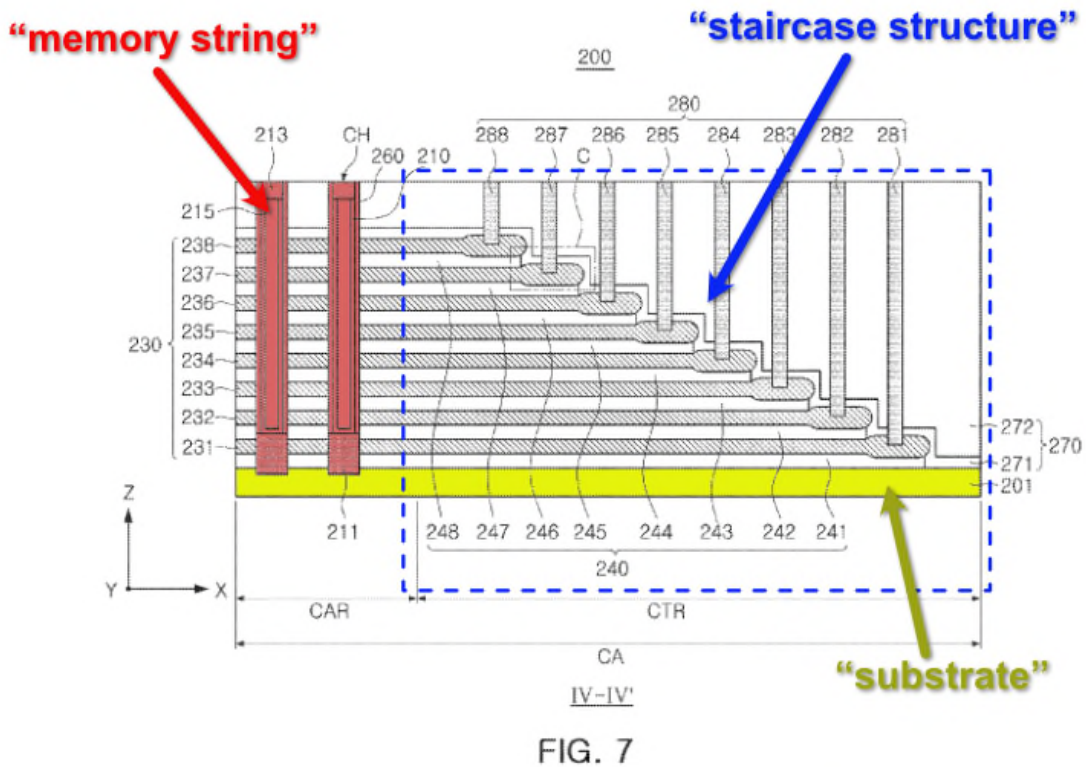


Id., Fig. 2 (annotated). A “channel structure[] CH” forming the memory strings is located over the “upper surface of [the] substrate....” *Id.*, ¶ [0038]; Ex. 1003, ¶¶ 268-272.

[17.C] “a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises;”

This is also taught by Nam. Nam explains that its “memory device” includes both a “cell array region CAR” and a “contact region CTR.” Nam, ¶¶ [0043], [0062]. The “channel structures CH” forming Nam’s memory strings are located in the “cell array region.” *Id.*, ¶ [0062]. “[C]ontact region CTR” includes a “plurality of contacts 281 to 288 (contacts 280)” that connect to “gate electrode layers 231 to 238.” *Id.*, ¶ [0063]. The gate electrodes “have step structures” or a “stepped shape having step structures” where they are “connected to the contacts 180.” *Id.*, ¶ [0043].

This stepped “contact region CTR” corresponds to the claimed **“staircase structure”**:



Id., Fig. 7 (annotated); see also Ex. 1003, ¶¶ 273-278.

[17.C.1] “a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer,”

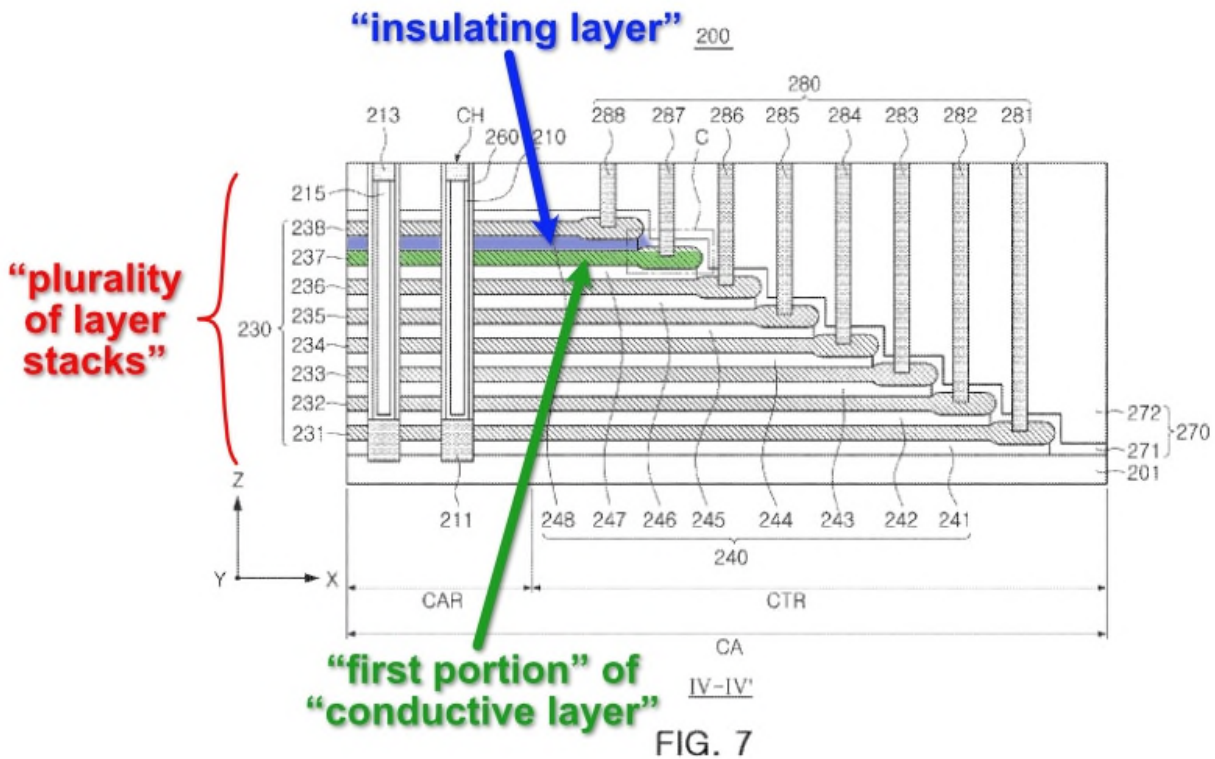
Nam teaches the claimed **“plurality of layer stacks”** with alternating **“insulating”** and **“conductive” “layer[s].”** In particular, Nam explains that its device “includes a stack of alternating first interlayer insulating layers and gate electrode layers on a substrate.” Nam, ¶ [0005]. For example, in the “memory device 200” of Figure 7, “[a] plurality of gate electrode layers 231 to 238 (gate electrode layers 230)” are alternately arranged such that they “form[] a pair with one

of a plurality of insulating layers 241 to 248 (240) adjacent thereto in a stack direction (Z-axis direction)....” *Id.*, ¶ [0063]. The “insulating layers” may be formed from “silicon oxide.” *Id.*, ¶ [0081]. The gate electrode layers are formed with a “conductive material” such as “metal.” *Id.*, ¶ [0094]. Nam also explains that “[a] first interlayer insulating layer 271”—made from the same “silicon oxide” material as insulating layers 240—is formed adjacent to insulating layers 240 and surrounds the ends of its gate electrodes. *Id.*, ¶ [0098]. A “doped region 271A” is located near the boundary of and separates layer 271 from a separate TEOS “second interlayer insulating layer 272.” *Id.*, ¶ [0100]; *see also id.*, Figs. 7, 8A.

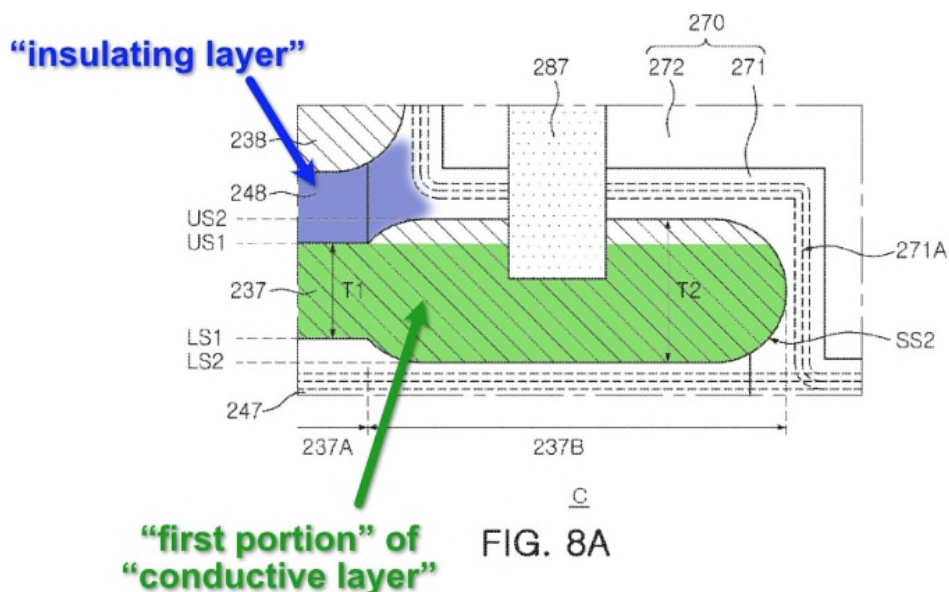
A POSITA would have considered both Nam’s insulating layer 240 and the adjacent insulating layer 271 to be the claimed “**insulating layer.**” Again, layers 240 are located between the gate electrode layers 230. *See id.*, Fig. 7. Further, layer 271 is applied before Nam’s staircase structure is complete. *See, e.g., id.*, ¶ [0098]; Fig. 31. The pads at the end of Nam’s gate electrode layers are then formed within openings etched in the layer 271. *See id.*, ¶¶ [0099]-[0106]; Figs. 32-34, 36, 39. The layer 271 remains behind in Nam’s final product. *See id.*, Fig. 7. Because layer 271 is not only formed from the same material as layer 240, but is used to define the shape of Nam’s pads, a POSITA would have understood it to be part of Nam’s “**insulating layer.**” Ex. 1003, ¶¶ 279-289. Layer 271 is distinguishable from other insulating layers in Nam that are not similarly part of Nam’s layer stack, such as

“second interlayer insulating layer 272.” Nam, ¶ [0100]; Fig. 7; *see also* Ex. 1003, ¶¶ 279-290.

An example “**insulating layer**” (insulating layer 248 and the adjacent portion of layer 271) and “**conductive layer**” (the gate electrode 237) are annotated below. As shown, both layers are part of a “**plurality of layer stacks**” (the combination of layers 230 and 240). And the “**insulating layer**” is “**disposed over a first portion**” of the depicted “**conductive layer.**” Moreover, each of the “**layer stacks**” in Nam’s device includes insulation (layers 240 and 271) over conductive material (layer 230):



Nam, Fig. 7 (annotated). The layers are also shown in Figure 8A, which “is an enlarged view of region C of FIG. 7.” *Id.*, ¶ [0065].



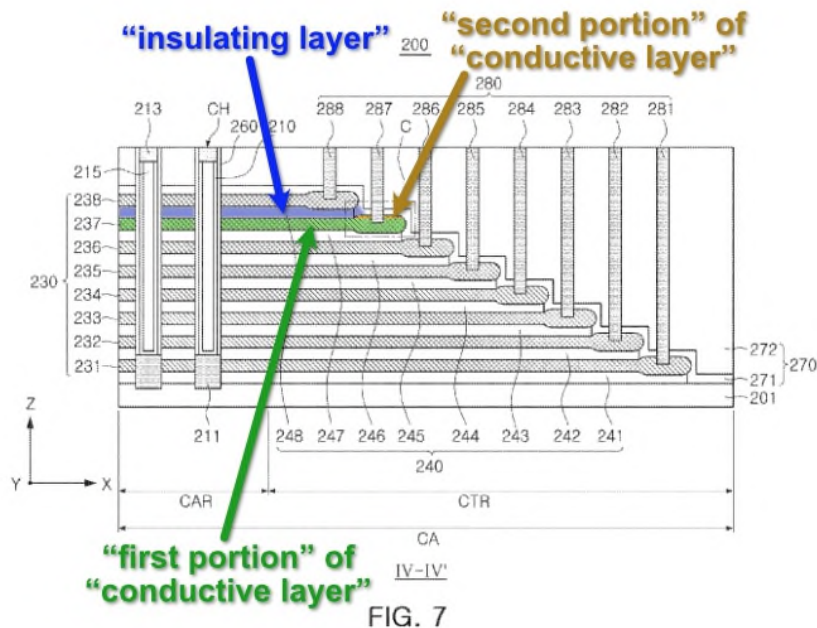
Id., Fig. 8A (annotated); *see also* Ex. 1003, ¶¶ 291-295.

[17.C.2] “wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.”

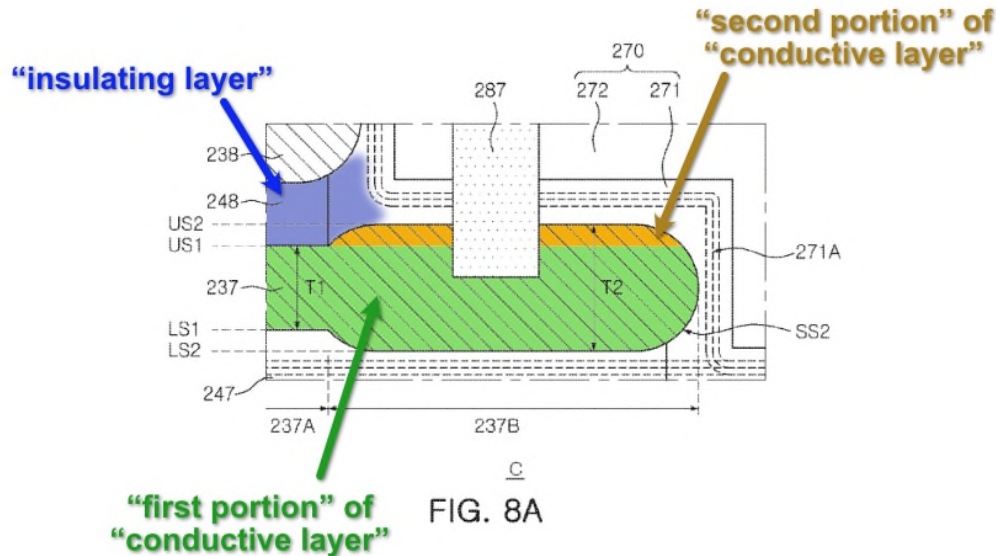
Nam renders this claim limitation obvious. Nam explains that its “gate electrode layers” include both a “first portion and a second portion.” Nam, ¶ [0005]. The “second portion forms an end portion” of the “gate electrode layer.” *Id.* This end portion serves as Nam’s contact “pad region.” *Id.*, ¶ [0045]. The pad has an “increased” “thickness” compared to the rest of the “gate electrode layer[.]” *Id.* Nam explains that making the gate electrode thin with a thick contact pad at its end serves two purposes. Employing thin gate electrodes “increase[s] a capacity of the memory device....” *Id.*, ¶ [0044]. Device “integration” can be “improved” via an “increased” “number of stacked gate electrode layers.” *Id.*, ¶ [0108]; *see also id.*, ¶ [0096]. But thinner gate electrodes create an issue: “a portion of the contacts 180”

that interconnect the gate electrodes to other portions of the memory “may penetrate through the gate electrode layer” and reach adjacent layers resulting in “the occurrence of defects such as short circuits.” *Id.*, ¶ [0044]. Making the contact pads on the ends of the electrodes thicker, according to Nam, “mitigate[s]” this problem by ensuring that the contact remains within the correct layer. *Id.*, ¶ [0045].

Because Nam’s “**conductive layer**” (its gate electrode) employs a thicker end, this layer has both a “**first portion**” and “**second portion**” as claim 17 requires. This is shown by, for instance, the below annotated version of Figure 7. Nam’s “**first portion**” is the thinner portion of its gate electrode and the bottom portion of its contact pad (one such electrode 237 is annotated below). Nam’s “**second portion**” is the upper, thicker portion located at the end of this same electrode:



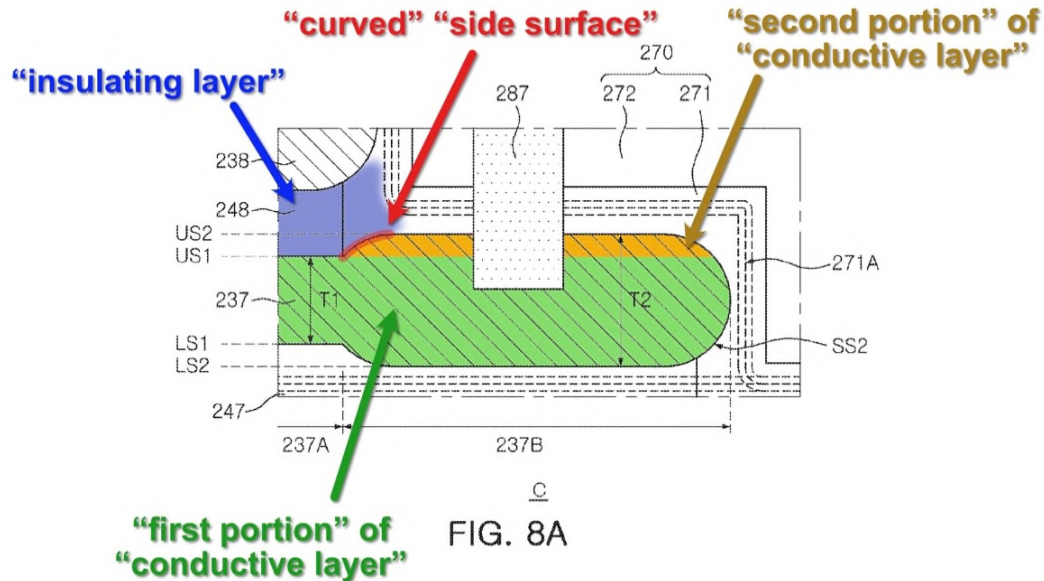
Id., Fig. 7 (annotated). This same structure is shown in more detail in Figure 8A:



Id., Fig. 8A (annotated). The gate electrode includes a “first region 237A” and a “second region 237B.” *Id.*, ¶ [0065]. The “second region 237B” is “provided as a pad region” that has a “thickness T2” that is “greater than a thickness T1 of the first region 237A.” *Id.* Because this pad region has an increased thickness, its “upper surface US2” is “disposed ... higher than an upper surface US1 of the first region of portion 237A.” *Id.* Again, the thicker portion of the pad between surfaces US1 and US2 and extending out of the top of the rest of the gate electrode is the “**second portion**” of Nam’s “**conductive layer.**” See Ex. 1003, ¶¶ 296-309.

According to Nam, its contact pad can also have a variety of shapes. For instance, the pad can be formed with a “concave shape” that is “recessed inwardly.” Nam, ¶ [0059]; Fig. 6. Alternatively, the pad can have a “convex” or “bull nose” shape. *Id.*, ¶ [0066]; Fig. 8A. The pad can also be formed either with a shaped bottom, or a “lower surface” that is “coplanar” with the rest of the gate electrode.

Id., ¶ [0072]; Fig. 10. As shown below, when formed with a “convex” shape, Nam’s contact pad includes the “*curved*” “*side surface*” claim 17 requires:



Id., Fig. 8A (annotated); *see also* Ex. 1003, ¶¶ 310-314.

In addition to identifying possible shapes, Nam details the process used to form its gate electrodes and contact pads. To begin, an alternating stack of sacrificial layers 220 and insulating layers 240 are formed. Nam, ¶ [0098]; Figs. 30, 31. Then, steps are formed in these layers. *Id.* The steps are then covered with “first interlayer insulating layer 271.” *Id.* Next, a multi-step “ion implantation process” is performed to create a “damaged region” “DA1” surrounding the ends of the sacrificial layers 220. *Id.*, ¶ [0099]. This “damaged region” is more susceptible to etching, is located at the “interface” between the sacrificial layer and the “interlayer insulating layers,” and has the shape of the intended contact pad. *Id.*, ¶¶ [0066], [0090], [0103]. An example of the damaged region locations is shown below:

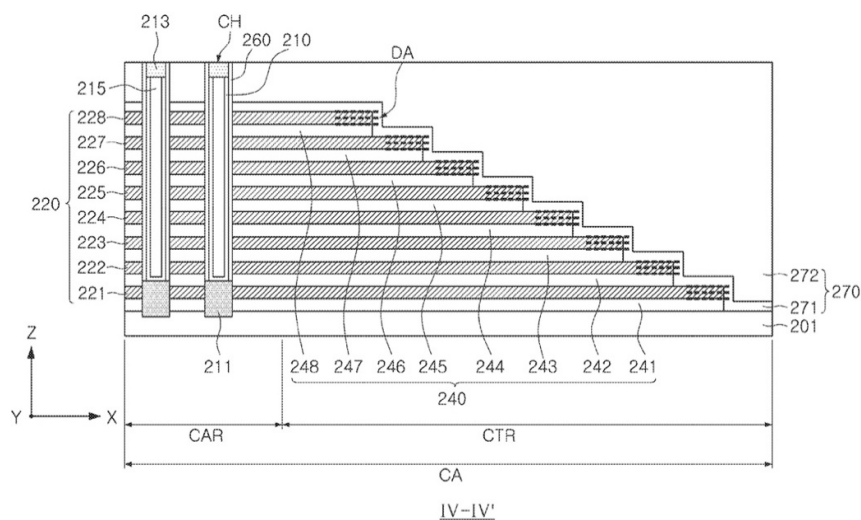


FIG. 34

Id., Fig. 34. After implantation is complete, a separate “second interlayer insulating layer 272” of “TEOS oxide film” is formed on top of the existing staircase structure.

Id., ¶ [0100]. Then, both the sacrificial layers and the damaged regions are etched to form “opening regions OP” in the shape of the gate electrodes and contact pads.

Id., ¶ [0104]. These openings are surrounded by insulating layers 240 and 271:

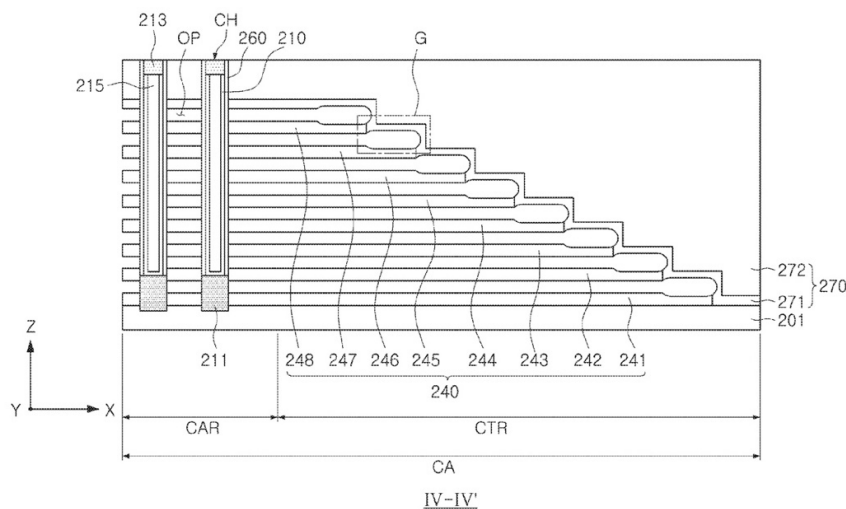
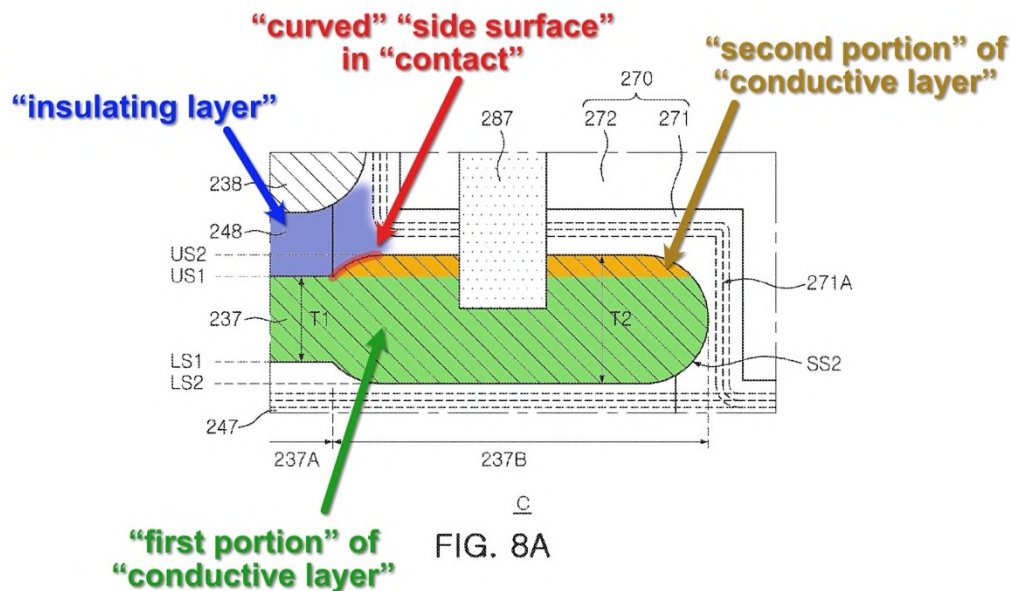


FIG. 36

Id., Fig. 36; see also *id.*, Fig. 37 (showing one of the contact pad openings in more

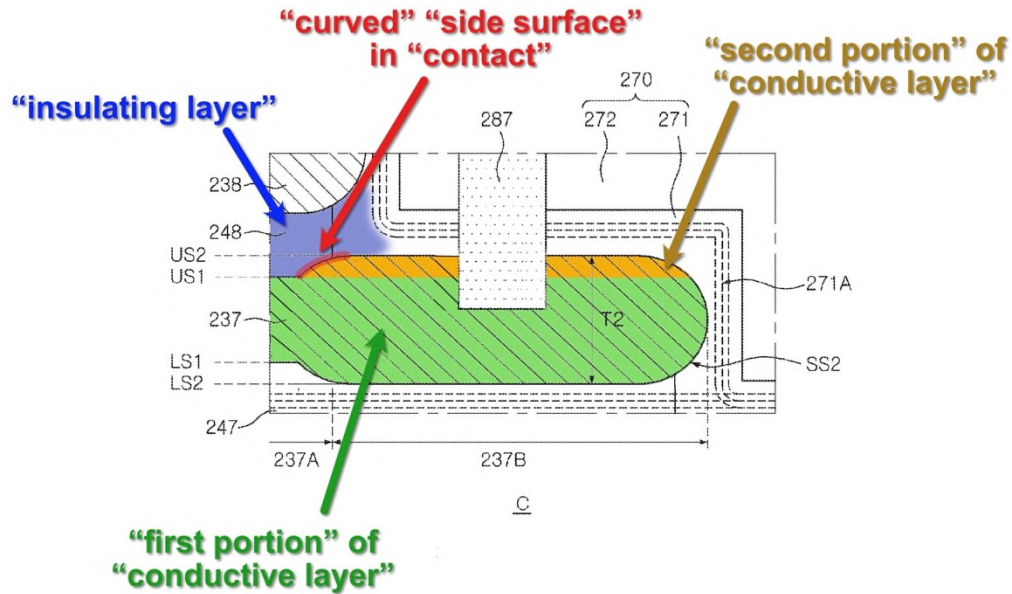
detail.) Finally, the openings are filled with conductive material to form the gate electrodes and pads. *Id.*, ¶ [0107]. Nam explains that during this process, some of the “implanted material” is “diffused to the inside of the first interlayer insulating layer 271 and then remains.” *Id.*, ¶ [0105]. This creates a “doped region 271A ... along an interface surface between the first interlayer insulating layer 271 and the second interlayer insulating layer 272.” *Id.*; *see also* Ex. 1003, ¶¶ 315-325.

Because Nam’s contact pad is formed within and at the “interface” of its insulating layer 271, a POSITA would have understood that the **“curved” “side surface”** of Nam’s **“second portion”** (the top part of its contact pad) is in **“contact”** with the **“side surface”** of its **“insulating layer”** (the portion of insulating layer 271 adjacent to the contact pad) as this limitation requires. This is shown in Figure 8A below:



Nam, Fig. 8A (annotated); *see also* Ex. 1003, ¶ 326.

Patent Owner may argue that only Nam's insulating layer 248—and not its layer 271—corresponds to the claimed “**insulating layer.**” Again, as explained, Nam layer 271 is formed along with the alternating stack of insulating and conductive layers and is used to form Nam's contact pads. Thus, both layer 248 and layer 271 together form Nam's “**insulating layer.**” And Nam's contact pad does contact insulation layer 271. *Id.*, ¶¶ 327-329. Regardless, a POSITA would have understood that because Nam forms its contact pad via ion implantation, a range of structures will result. *See id.*, ¶¶ 330-334. In other words, while Figure 8A depicts the intended or representative pad structure, ion implantation will result in both somewhat larger and somewhat smaller pads. *See id.* Because of this, in some layers, a POSITA would have understood that the pad will extend beyond the bounds shown in Figure 8A into layer 248 by some amount. This will in turn result in a longer interface of contact between the curved surface of the pad and layer 248. The demonstrative below—created using Nam Figure 8A but with the pad shown having expanded size due to increased amounts of ion implantation—shows this additional contact interface:



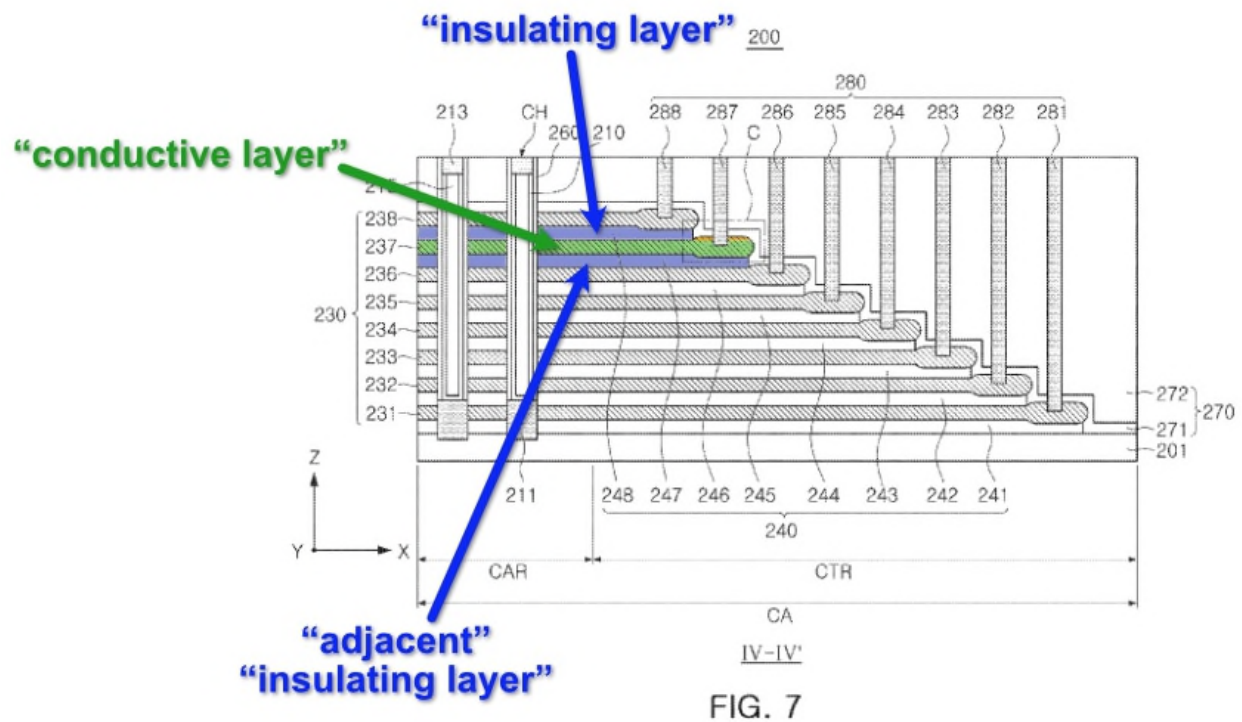
Id., ¶ 335. Moreover, a POSITA would have understood that the amount of contact between Nam's pad and insulating layer 248 could be readily adjusted by tailoring the ion implantation process. Nam includes examples where both (1) the corner of its contact pad (see Nam, Figs. 8A, 8B) and (2) the entire side surface of its contact pad (see *id.*, Figs. 6, 10) contact insulating layer 248. A POSITA would have considered these pad designs to simply be examples on a continuum of possible pad shapes within the scope of Nam's disclosure. See Ex. 1003, ¶¶ 336-339. A POSITA would thus have considered—and would have been able given Nam's teachings—to adjust both the shape of Nam's contact pad and achieve different amounts of contact between its various insulating layers. See *id.*

2. Claim 19

Claim 19 depends on claim 17 and further requires:

[19] “wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack”

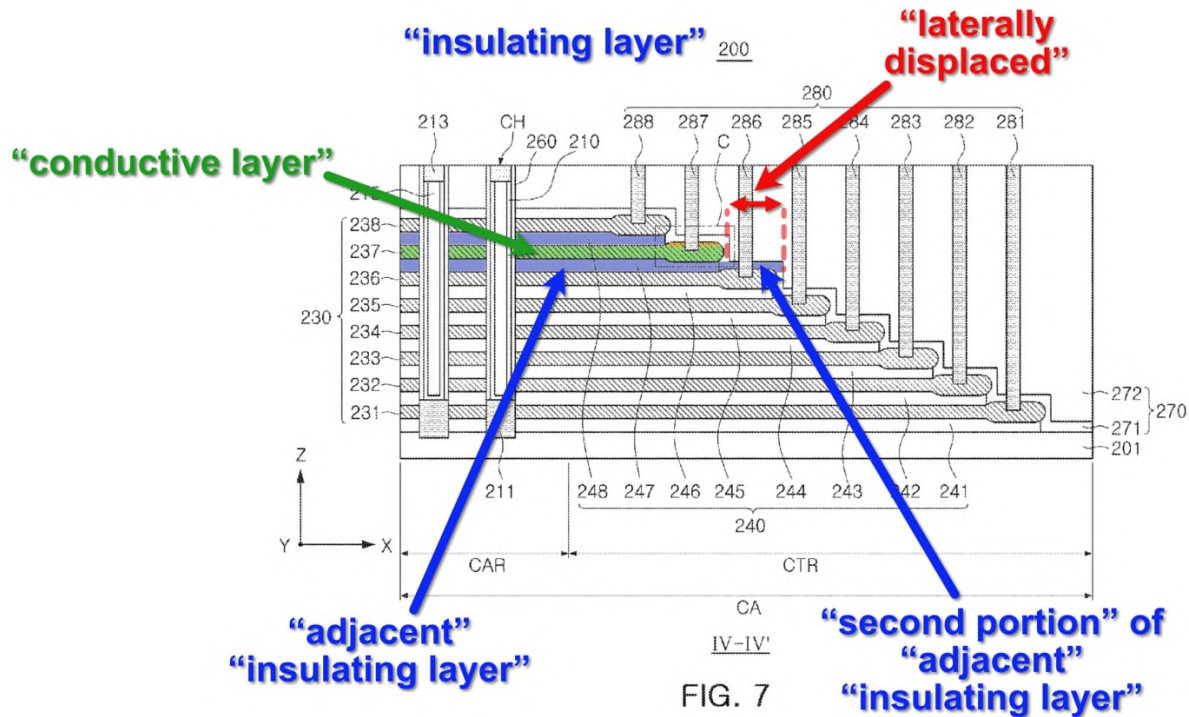
This is taught by Nam. Nam’s device is formed from alternating conductive and insulating layers. See Nam, ¶¶ [0005], [0062]-[0063]. Because of this, as shown in Figure 7, each of Nam’s “conductive layer[s]” (such as layer 237) is located over “a first portion of the insulating layer of an adjacent layer stack” (such as layer 247):



Id., Fig. 7 (annotated); see also Ex. 1003, ¶¶ 341-343.

Further, each of Nam’s contact pads is formed within interlayer insulating layer 271. Nam, ¶¶ [0067], [0098]-[0105]. The layer 271 follows the “steps” of

Nam's device. See *id.*, ¶ [0098]; see also *id.*, Fig. 7. This causes a **“second portion of the insulating layer of the adjacent layer stack”** (insulating layer 271 below the contact pad) to be **“laterally displaced from the conductive layer”** (the lower layer 271 extends beyond the end of Nam's conductive layer 237):



Id., Fig. 7 (annotated); see also Ex. 1003, ¶¶ 344-345.

3. Claim 20

Claim 20 depends on claim 17 and further requires that:

[20] “wherein the conductive layer comprises a first conductive material, and wherein the curved side surface comprises a second conductive material.”

This is also taught by Nam. According to Nam, its **“conductive layer”**—including the **“second portion”** with a **“curved side surface”**—may be formed from the same “metal” material. Nam, ¶ [0107]; see also *id.*, ¶ [0094]. Again, per the

'666 patent, while this claim does reference a “first conductive material” and “second conductive material,” these materials need not be different and may be the “same.” *See, e.g.*, Ex. 1001, 1:55-59; Ex. 1003, ¶¶ 347-349.

C. Ground 3: Claims 17, 19, and 20 Are Obvious Over Lee and Park

Lee, when modified following Park’s teachings, also renders claims 17, 19, and 20 obvious.

1. Claim 17

[17.Pre] “A memory device, comprising:”

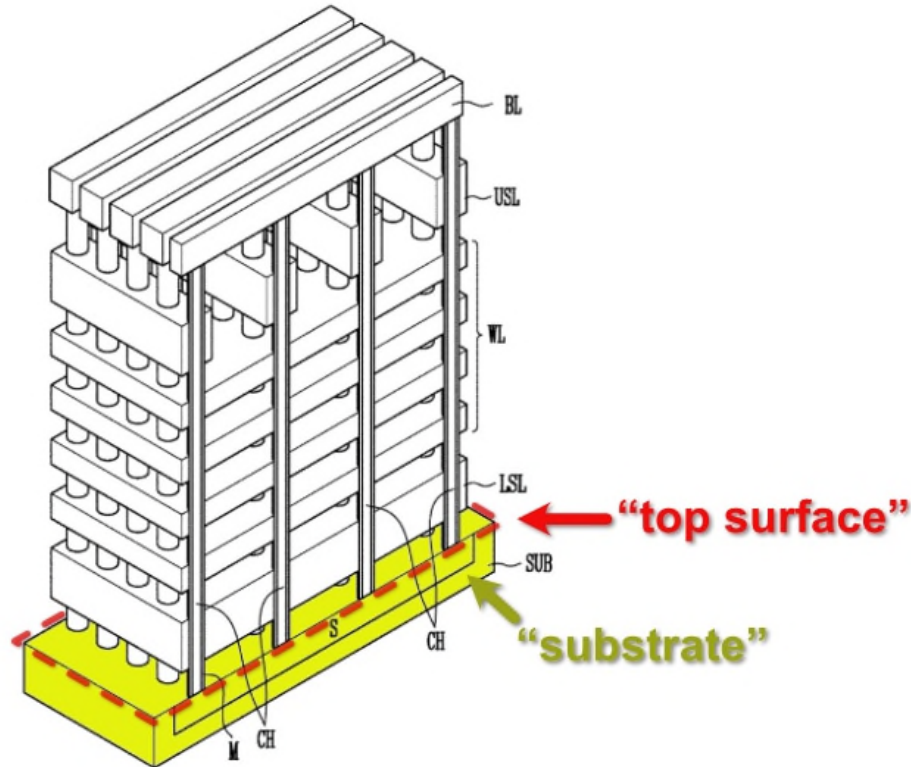
To the extent this preamble language is limiting, it is taught by Lee. Per Lee, it relates to “semiconductor device[s]” such as “three-dimensional (3D) non-volatile memory devices.” Lee, ¶¶ [0005], [0008]-[0009]. This device can be part of a system including a “non-volatile memory device 120 and a memory controller 110.” *Id.*, ¶¶ [0085]-[0090]; Fig. 13; *see also* Ex. 1003, ¶¶ 352-355.

[17.A] “a substrate, wherein the substrate comprises a top surface;”

Lee teaches a “**substrate**” with a “**top surface.**” More specifically, Lee’s “semiconductor device” includes “a substrate” that includes a “cell region and a contact region.” Lee, ¶ [0009]; *see also id.*, ¶¶ [0010] (noting that there are a “plurality of stacked structures” on the “substrate”); [0020] (the semiconductor device includes a “substrate”). An example of one such “substrate SUB” is shown in Figure 12B of Lee below. *Id.*, ¶ [0068]. As can be seen, the substrate includes an upper or top surface over which components of the memory are located. *Id.*; *see*

also id., ¶¶ [0062]-[0063] (similarly discussing a “substrate SUB”).

FIG. 12B

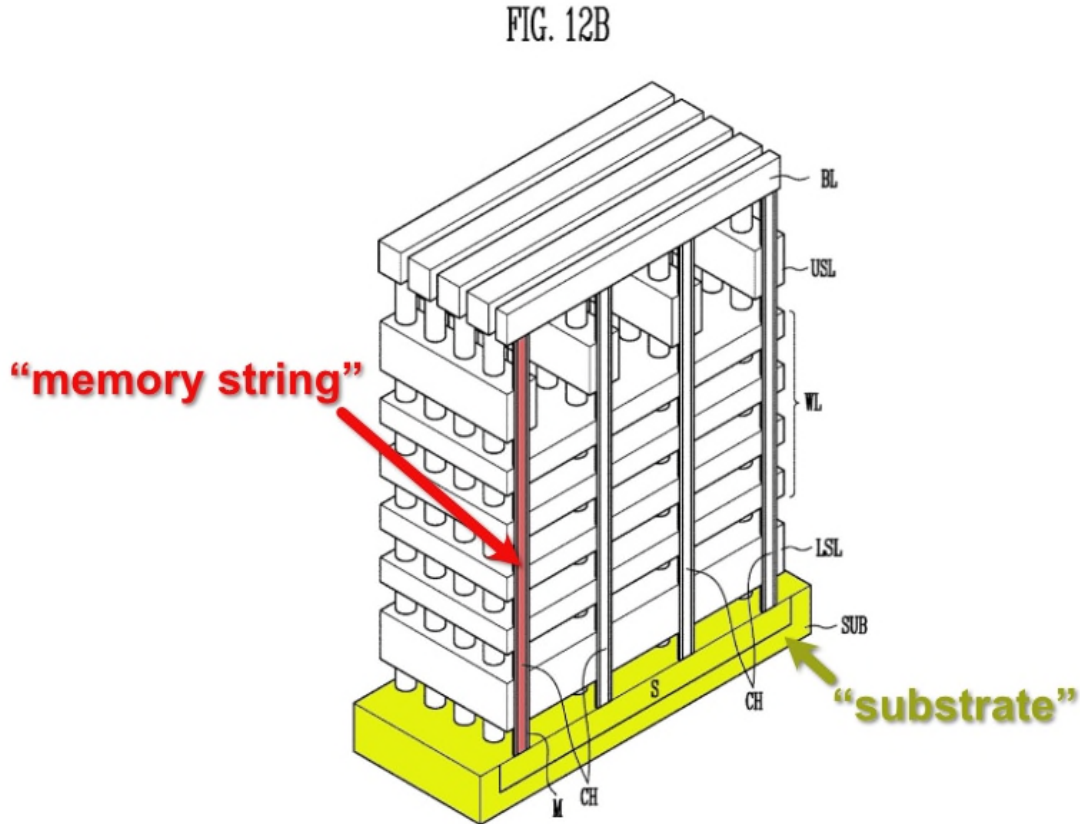


Id., Fig. 12B (annotated); *see also* Ex. 1003, ¶¶ 356-359.

[17.B] “a memory string disposed over the substrate; and”

This is also taught by Lee. According to Lee, its device includes a “plurality of memory cells” that are “coupled in series with each other” to form a “single string.” Lee, ¶ [0071]. Lee’s device includes multiple such “string[s]” “arranged in a vertical manner.” *Id.* The strings include a central “channel layer CH” with individual “memory cell[s]” formed at the “intersection between the channel layer CH” and a “word line WL.” *Id.* The “channel layers CH” are located above and

“protrude from the substrate SUB.” *Id.*, ¶ [0069]. One such “**memory string**” is annotated in Figure 12B below:

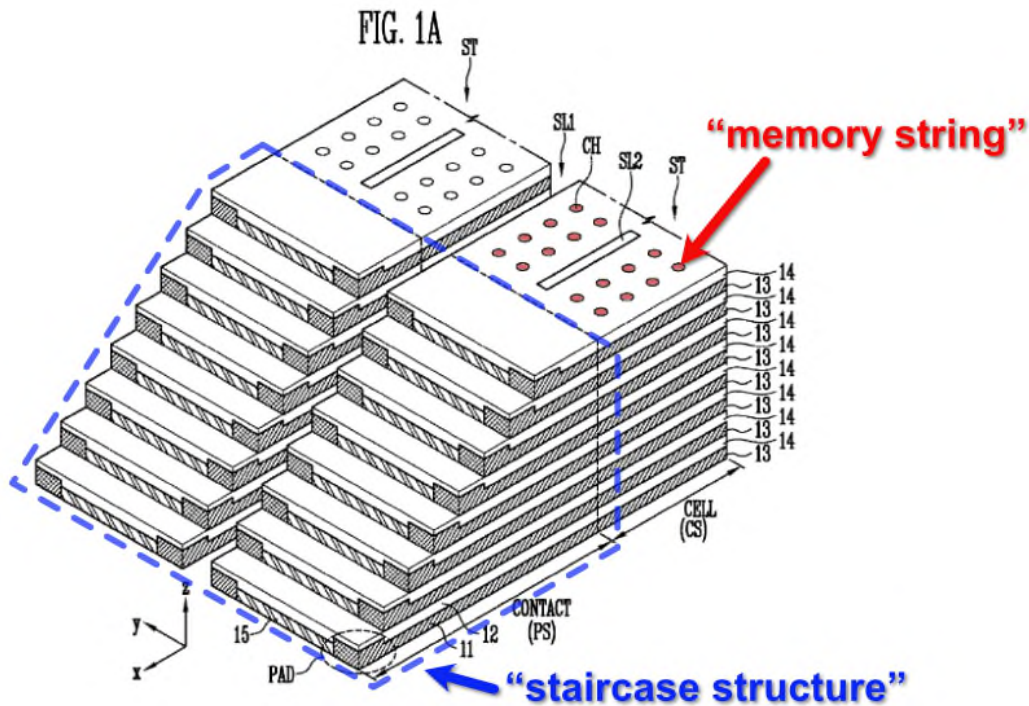


Id., Fig. 12B (annotated); Ex. 1003, ¶¶ 360-364.

[17.C] “a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises;”

This is also taught by Lee. According to Lee, its device includes both a “contact region CONTACT” and a “cell region CELL.” Lee, ¶ [0020]. The “cell region” includes the “channel layers CH” along which Lee’s memory cells (and the strings containing those cells) are formed. *Id.*, ¶ [0026]. A “stacked structure ST” formed from “conductive layers 11 and 13 and insulating layers 12 and 14” is located

in both the CONTACT and CELL regions. *Id.*, ¶ [0020]. Lee explains that “[a]n end of the stacked structure ST may be patterned stepwise.” *Id.*, ¶ [0021]; *see also id.*, ¶¶ [0009] (similarly noting that “an end of the pad structure is patterned stepwise.” Lee’s “**staircase structure**” (the stepped portion of the CONTACT region) and example “**memory string[s]**” (located along channel layers CH) are annotated in Figure 1A below:



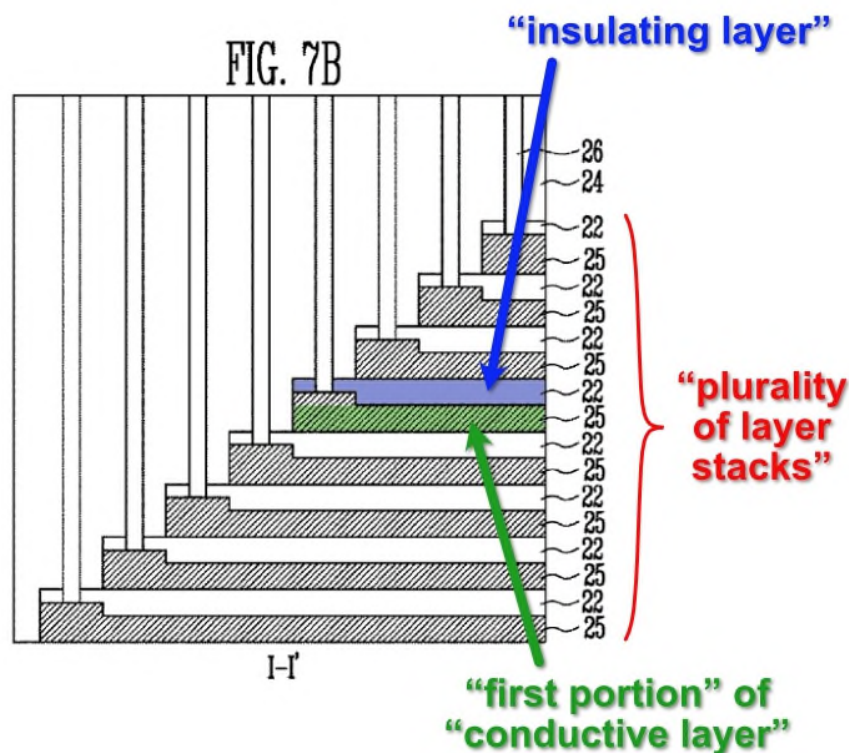
Id., Fig. 1A (annotated); *see also* Ex. 1003, ¶¶ 365-370.

[17.C.1] “a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer,”

Lee teaches the claimed “**plurality of layer stacks**” with alternating “**insulating**” and “**conductive**” “**layer[s]**.” According to Lee, its device includes a “stacked structure ST” that is “patterned stepwise.” Lee, ¶ [0021]. The “stacked

structure ST” is formed from “conductive layers ... and insulating layers ... that are formed alternately with each other on the substrate.” *Id.*, ¶ [0020]. “Each step of the stacked structure” includes “at least one conductive layer ... and at least one insulating layer....” *Id.*, ¶ [0021]. The “insulating layer” is “located on” the “top surface of each step.” *Id.*; *see also id.*, ¶ [0010] (similarly referencing a “stacked structure[] including a plurality of conductive layers and a plurality of insulating layers formed alternately with each other”).

Figure 7B below provides an example. In this figure, layers 22 are “interlayer insulating layers.” *Id.*, ¶ [0046]. Layers 25 are “conductive layers.” *Id.*, ¶ [0041]. As shown, in each “**layer stack**” (the combination of an insulating layer 22 and conductive layer 25 forming a step), the “**insulating layer**” (layer 22) is “**disposed over a first portion of a conductive layer**” (the annotated portion of conductive layer 25):

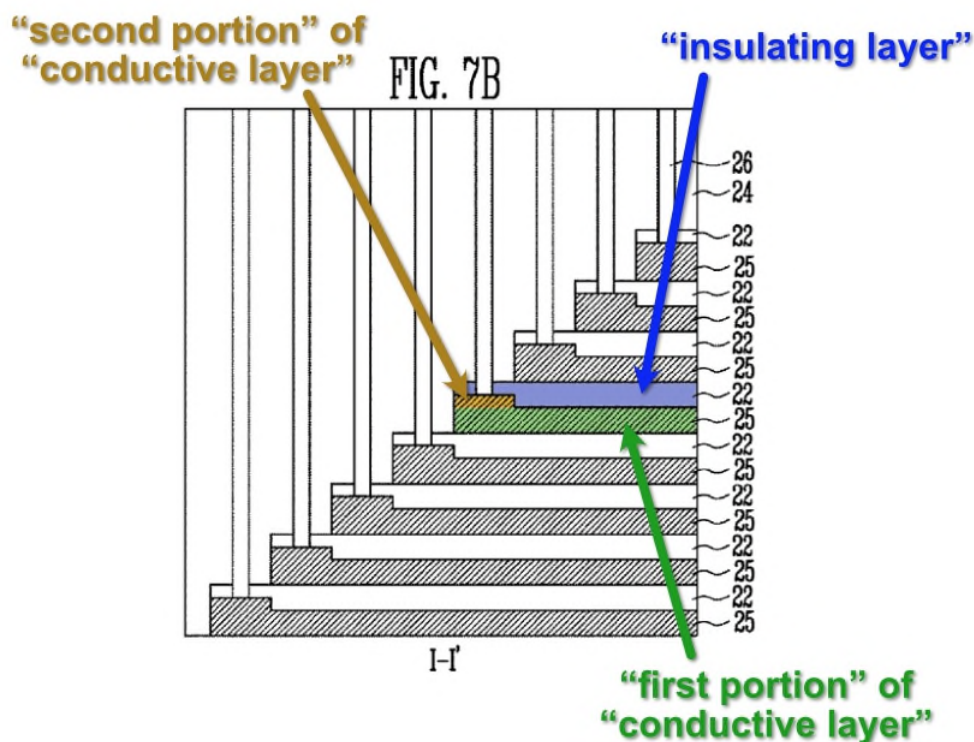


Id., Fig. 7B (annotated); *see also id.*, Figs. 1A, 6B (similarly showing insulating layers alternating with conductive layers); Ex. 1003, ¶¶ 371-376.

[17.C.2] “wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.”

Lee, when modified following Park’s teachings, renders this limitation obvious. Lee’s device already includes a “**conductive layer**” with both a “**first portion**” and “**second portion.**” According to Lee, each of the “conductive layers” in its stepped stack may include a “pad portion[] PAD” at its end that has “a greater thickness” than other portions of “the ... conductive layer.” Lee, ¶ [0023]; *see also id.*, ¶ [0009] (noting that the “semiconductor device” includes “pad portions” that “have a greater thickness than unexposed portions of the plurality of first conductive

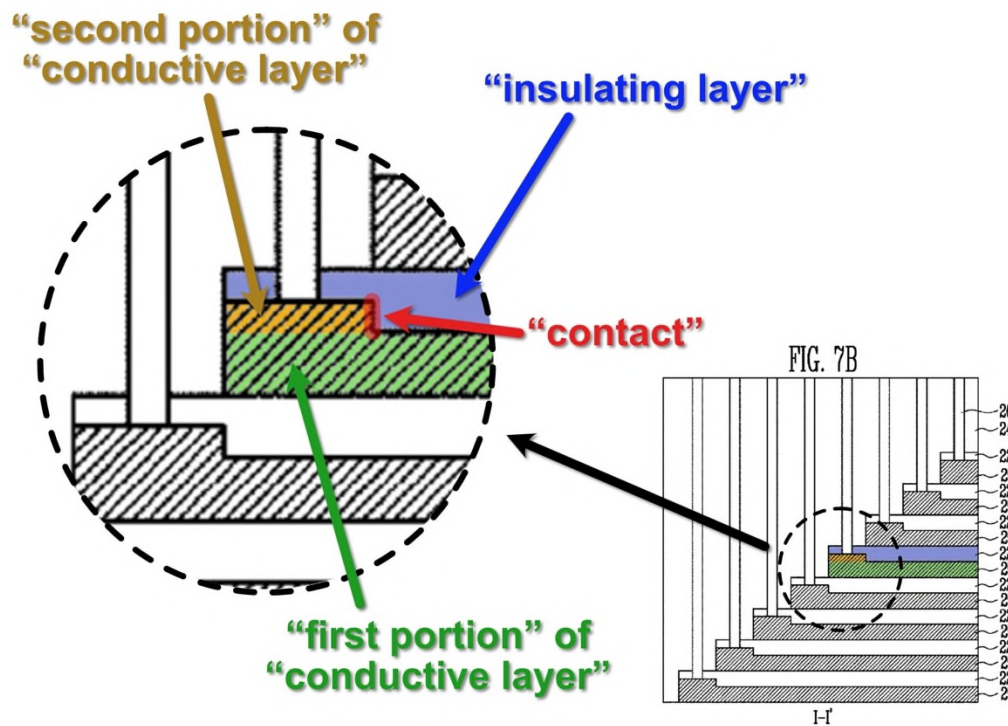
layers”); ¶ [0027] (similar). According to Lee, because the pad is located only on the end of each conductive layer in its stack, “the thickness of the pad portion PAD may be selectively increased without increasing the height of stacked structure ST.” *Id.*, ¶ [0027]. The “pad portions PAD” allow “contact plugs 26” to be “coupled” to each of Lee’s conductive layers. *Id.*, ¶ [0042]. The increased height of the pads is intended to avoid a “punch phenomenon ... due to over-etching of upper pad portions PAD” or a “not-open phenomenon” resulting from “lower pad portions PAD” which “may not be exposed along bottom surfaces of the contact holes.” *Id.*, ¶ [0043]. This pad portion PAD on the end of each of Lee’s conductive layer is the claimed “**second portion**” of a “**conductive layer**”:



Id., Fig. 7B (annotated); see also *id.*, Fig. 1A (similarly showing device with

alternating insulating and conductive layers and pad portion PAD); Ex. 1003, ¶¶ 377-383.

Next, just as this claim requires, the “*side surface*” of the “*second portion*” of Lee’s “*conductive layer*” (Lee’s pad portion PAD) is in “*contact*” with “*a side surface of the insulating layer*” (insulating layer 22 in Figure 7B). This is shown in the below annotated version of Figure 7B:

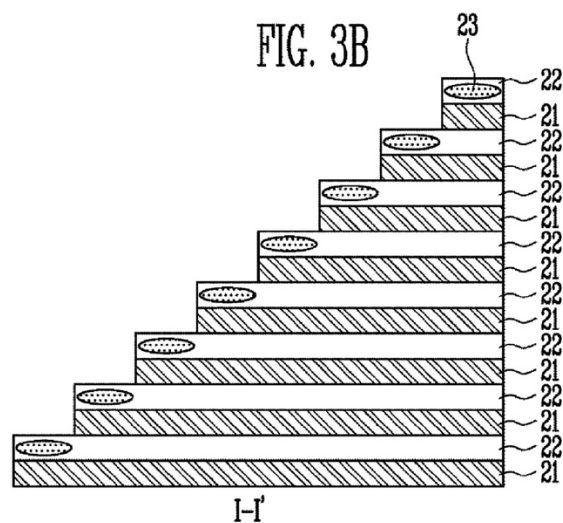


Lee, Fig. 7B (annotated); see also Ex. 1003, ¶ 384.

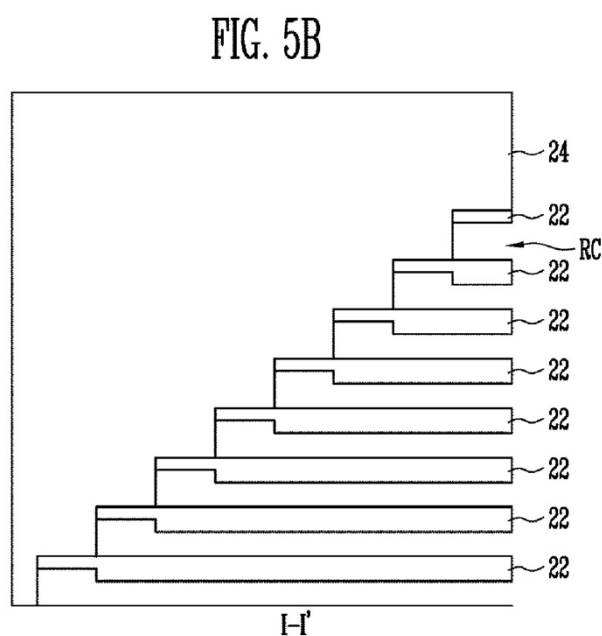
While the “*side surface*” of Lee’s insulating layer 22 that is in contact with the pad portion PAD is not at the extreme end of the insulating layer, there is nothing about claim 17 that requires this to be the case. The claim provides only that there be contact with “*a side surface of the insulating layer.*” There is no requirement that

this side surface be at any particular location along the length of the insulation layer. Consistent with this, the '666 patent explains that a “layer” can “include multiple layers” or sub-layers. Ex. 1001, 4:36-37, 4:52-53. Lee’s pad portion PAD is in contact with the side of the lower portion—or sub-layer—of insulating layer 22. See Ex. 1003, ¶¶ 385-387.

The process Lee employs to form its pad portion PAD confirms that there is contact between the PAD and the adjacent insulating layer. Lee begins by forming “a plurality of first material layers 21 and a plurality of second material layers 22 ... alternatively with each other.” Lee, ¶ [0029]. The “layers 21,” which will eventually be replaced by Lee’s “conductive layers,” are “formed of materials having a high etch selectivity with respect to second material layers 22.” *Id.*, ¶ [0030]. The “second material layers 22” are “an insulating layer such as an oxide layer.” *Id.* Lee then employs an “ion implantation process” to “implant[]” “impurity regions 23” into the insulating layers 22. *Id.*, ¶ [0034]. These impurity regions will eventually form the thicker portions of Lee’s pad portions PAD. See *id.*, ¶¶ [0038]-0041]. This is shown in Figure 3B below:



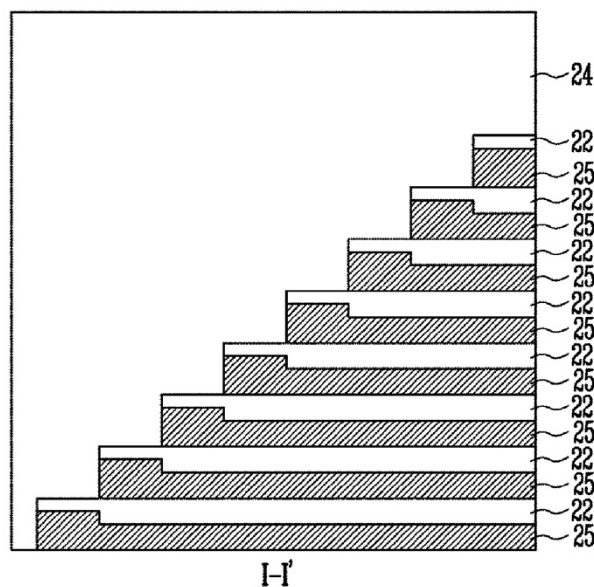
Id., Fig. 3B. Then, Lee etches layers 21 using an isotropic etch step. *Id.*, ¶ [0038]. Then, it performs a second wet etch step to remove the impurity regions 23 to form “recessed regions RC” between the remaining portions of the insulating layers 22. *Id.* This is shown in Figure 5B:



Id., Fig. 5B. Then, the openings are filled with “conductive layers 25” forming “pad

portions PAD exposed at the end of stacked structure ST.” *Id.*, ¶ [0041].

FIG. 6B

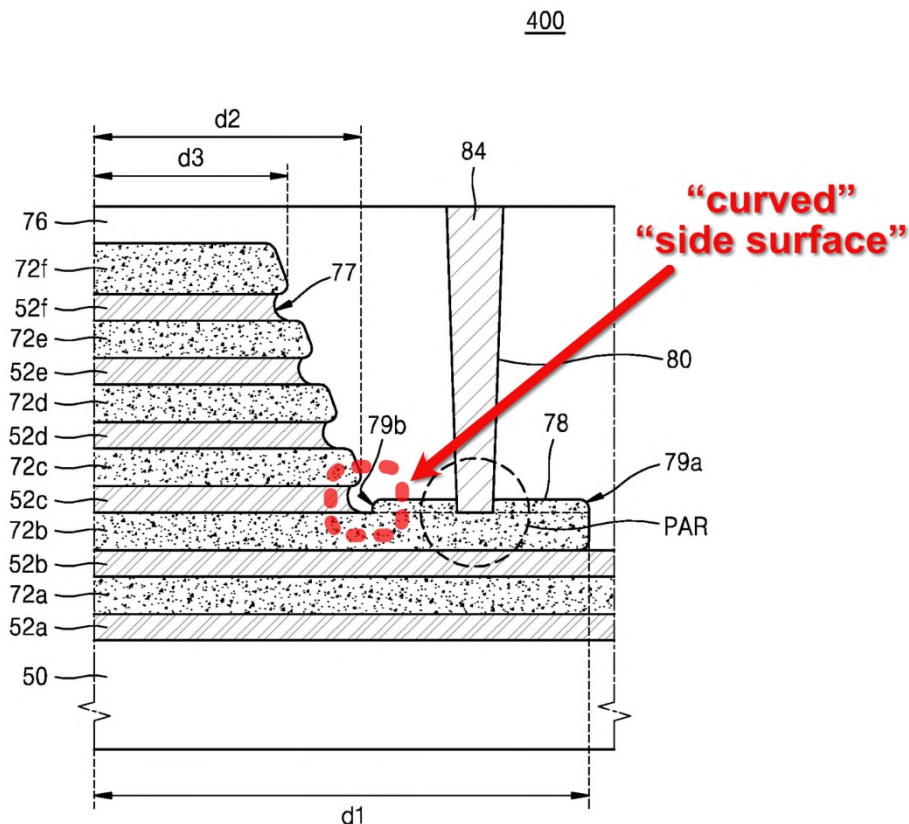


Id., Fig. 6B. Because Lee's pad portions PAD are formed within an opening in its insulating layers 22, a POSITA would have understood that the sides of the pad portions PAD contact the sides of the insulating layers. See Ex. 1003, ¶¶ 388-399.

Lee depicts its pad portions PAD as having straight sides in its figures. Regardless, a POSITA would have considered it obvious to make the ***“side surface”*** of Lee’s ***“second portion of the conductive layer” “curved”*** in view of Park’s teachings. Again, Park teaches a three-dimensional memory device that includes a stepped “connection region” with “pad region[s] PAR” located on the end of gate electrodes. Park, 6:7-12, 6:36-47. Further, each of Park’s electrodes terminates with a “pad region PAR” that includes a “raised pad portion 28.” *Id.*, 7:4-16. Per Park, the “end 79b” of this “raised pad portion 78” may be “rounded” to “prevent a short

circuit” between the pad and an “adjacent ... conductive layer pattern 72c.” *Id.*, 11:35-41. Park achieves its rounded contact pad by “ion implanting impurities” in “into” an “insulating layer” and performing an “oxidation process” to create an “additional sacrificial layer” “having a higher etching rate” than the surrounding insulation. *Id.*, 12:16-23, 39-47. The sacrificial material is then removed and replaced with conductive material to form insulation-surrounded electrodes and curved pads. *Id.*, 12:48-56. This is shown in Figure 7 from Park:

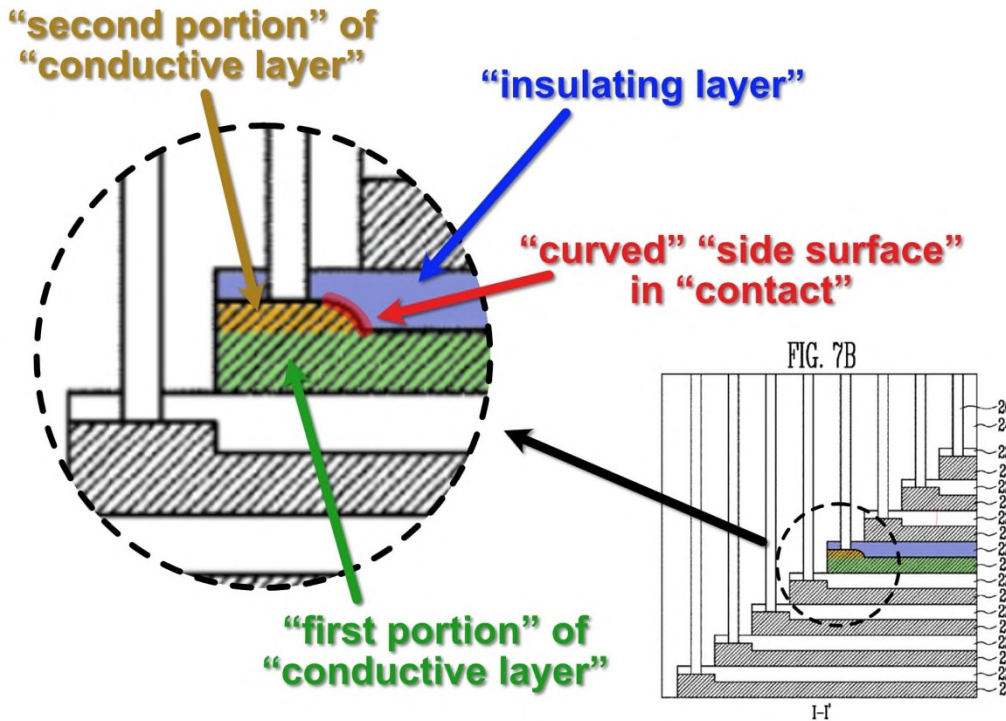
FIG. 7



Id., Fig. 7 (annotated). Similarly processes were also used by other prior art to form contact pads with rounded sides surrounded by insulation. *See, e.g.*, Nam, ¶¶ [0097]-

[0105]; Figs. 30-37; *see also* Ex. 1003, ¶¶ 400-409.

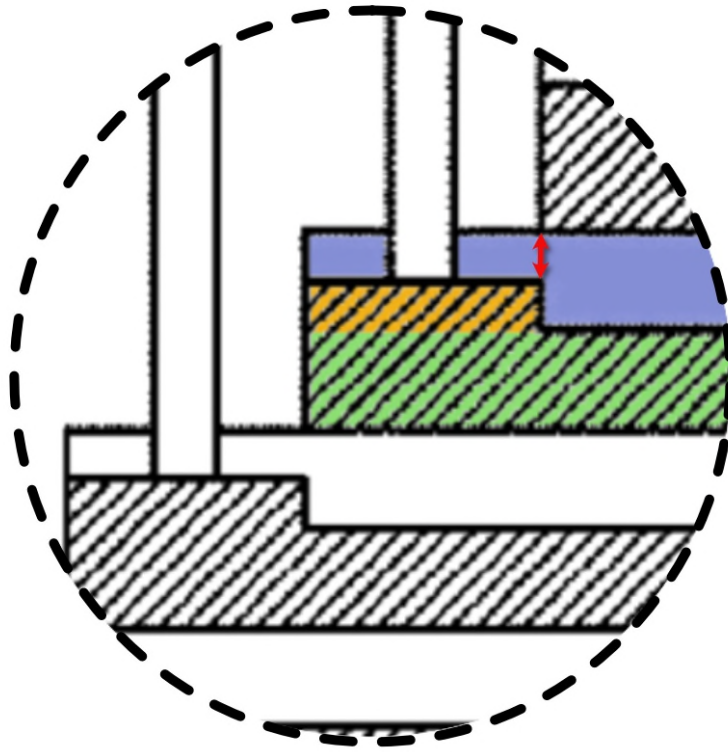
Applying Park’s teachings to Lee—and making at least the end of Lee’s pad portion PAD facing its conductive layers rounded—results in what this limitation requires. Now, the “**second portion**” of Lee’s “**conductive layer**” (pad portion PAD) includes a “**curved**” “**side surface**” that is in “**contact**” with a “**side surface**” of its “**insulating layer**.” This is shown in the below demonstrative figure created by modifying Figure 7B of Lee:



Lee, Fig. 7B (modified and annotated); Ex. 1003, ¶¶ 410-415.

A POSITA would have been motivated to make the end of Lee’s pad portion PAD facing its conductive layers rounded. Again, Park explains that rounding the contact pad helps “prevent a short circuit” between the pad and an “adjacent”

conductive layer. Park, 11:35-41. A POSITA would have recognized that due to their straight sides, each of Lee's pad portions PAD is physically proximate to the adjacent conductive layer immediately above the pad:



Lee, Fig. 7B (excerpted and annotated); see also Ex. 1003, ¶¶ 416-418. A POSITA would have recognized that this creates a risk of short circuit in the event variances in the manufacturing process cause either the pad or the adjacent conductive layer to extend further than intended. See *id.*, ¶ 419. A POSITA would have recognized that applying Park's teachings and rounding the side of Lee's pad portion PAD would have improved Lee—and limited the risk of short circuit—by increasing the minimum distance between the pad and the immediately adjacent conductive layer.

See id., ¶ 420. Similarly, Lee itself notes that if the PAD and conductive layer are too close, there is a risk that the “breakdown voltage” between these layers may be “deteriorated.” Lee, ¶ [0049]. This can be avoided by ensuring that there is “sufficient distance ... between the stacked conductive layers (pad portions).” *Id.* A POSITA would have understood that applying Park’s teachings and rounding Lee’s pad portions PAD furthers this goal: the distance between conductive layers would be increased avoiding deterioration of the breakdown voltage. *See* Ex. 1003, ¶¶ 421-423.

Contact pads with rounded, curved side surfaces were also a known, routinely used alternative for memory devices with staircase structures at the time the ’666 patent was filed. *See, e.g.*, Kim, 8:29-34 (noting that contact pads can have a “curved surface”); Park, 11:35-41 (contact pad can be “rounded”); Yun, 8:33-40 (contact pad can have “rounded” “side surface”; Nam, ¶ [0066] (contact pad can have “bull nose” or “convex” shape). Given the prevalence of contact pads with this type of shape in the prior art, a POSITA would have considered the use of rounded/curved pads with Lee to be nothing more than a routine, obvious design choice. *See* Ex. 1003, ¶¶ 424-425.

A POSITA would also have had every reason to believe that a curved pad could be successfully used with Lee. Again, numerous prior art references identified this type of pad as acceptable for three-dimensional memory devices with staircase

structures. *See, e.g.*, Kim, 8:23-34; Park, Fig. 8; Yun, Fig. 5A; Nam, Fig. 8A. Moreover, Lee explains that the shape of its pad portion PAD is controlled via an “ion implantation process.” Lee, ¶¶ [0034], [0038]-[0041]. As explained in Ground 1, a POSITA would have recognized that this type of process could be readily adapted to form a curved contact pad. *See, e.g.*, Park, 7:17-29 (“ion implantation” and “oxidation” employed to form pad with “rounded” sides); Nam, ¶¶ [0066], [0098]-[0107]; Figs. 30-39 (discussing use of “an ion implantation process” at length to form “convex” contact pad); *see also* Ex. 1003, ¶¶ 426-429. For example, POSITA would have recognized that Park’s process could be readily applied to Park to round Park’s contact pads. Lee’s ion implantation and etching steps would be performed in the same manner as Lee already teaches. *See id.*, Ex. 1003, ¶¶ 411-413. Then, once the openings shown in Figure 5B of Lee are formed, oxidant would be introduced into the opening for a controlled period of time to produce a rounded opening (and later, a rounded contact pad). *See id.*

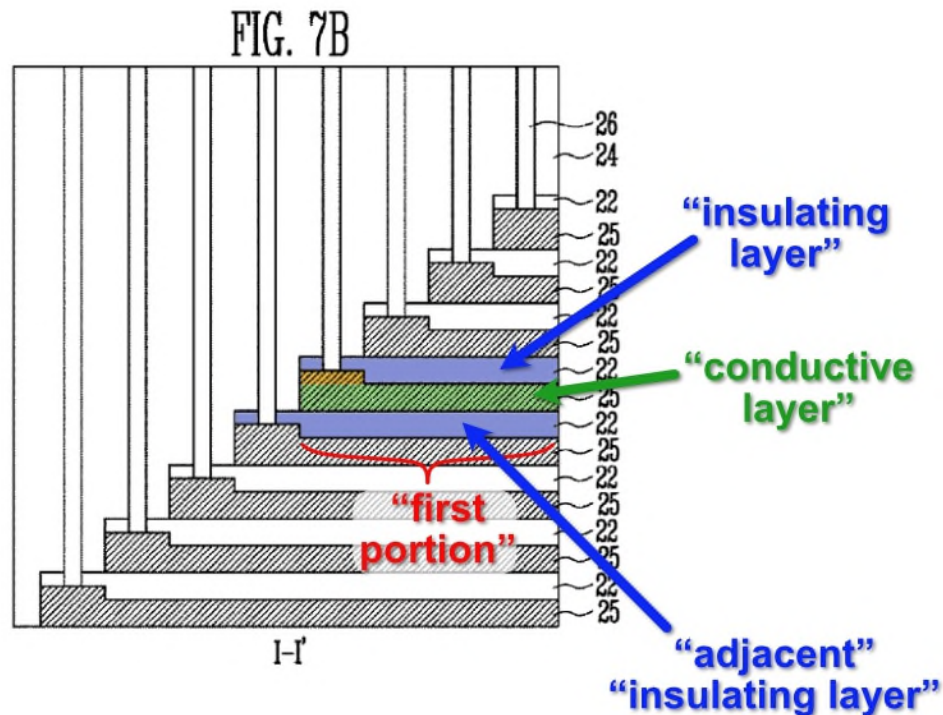
2. Claim 19

Claim 19 depends on claim 17 and further requires:

[19] “wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack”

This is taught by Lee. Again, Lee’s device includes a “stacked structure ST”

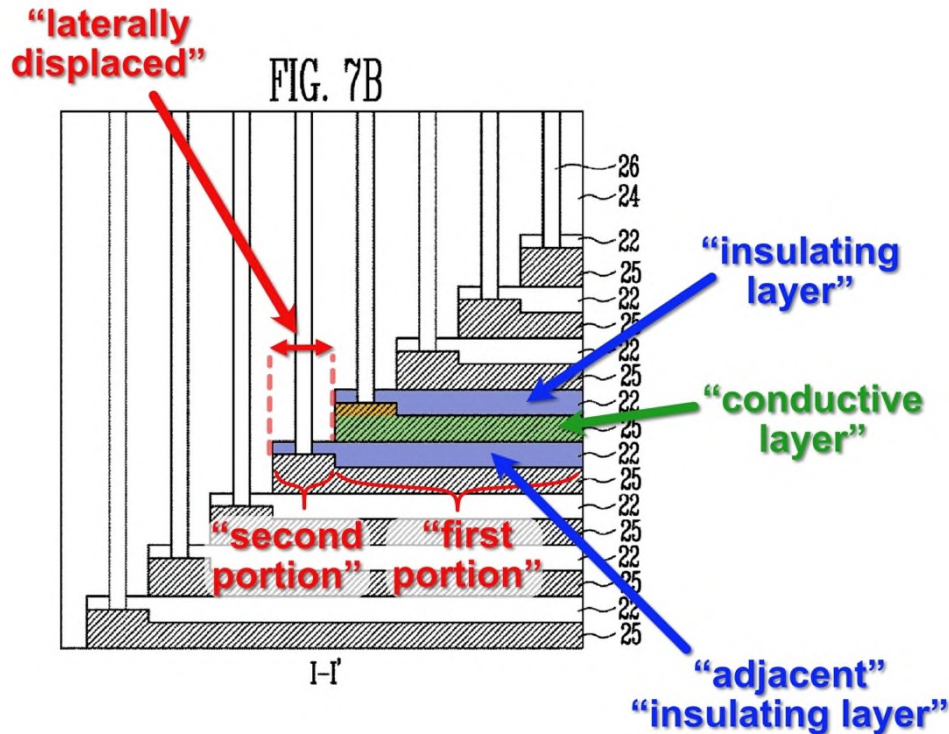
formed from alternating “conductive layers” and “insulating layers.” Lee, ¶¶ [0020]-[0021]; *see also id.*, ¶¶ [0010], [0041], [0046]; Figs. 1A, 7A. Because of this, each of Lee’s “**conductive layer[s]**” (conductive layer 25 in Fig. 7B) is located over “**a first portion of the insulating layer of an adjacent layer stack**” (the portion of insulating layer 22 in Fig. 7B immediately below the conductive layer):



Id., Fig. 7B (annotated); *see also* Ex. 1003, ¶¶ 431-433.

Next, in Lee, “[e]ach step of the stacked structure ST that is patterned stepwise” includes “one conductive layer” and “one insulating layer.” Lee, ¶ [0021]. In Figure 7B, “the insulating layer” is “located on a top surface of each step.” *Id.* As shown below, this results in “**second portion of the insulating layer of the adjacent layer stack**” (the portion of a lower insulating layer 22 that extends out

beyond an upper adjacent conductive layer 25 for purposes of forming a step) being ***“laterally displaced from the conductive layer”***:



Id., Fig. 7B (annotated); see also Ex. 1003, ¶¶ 434-436.

3. Claim 20

Claim 20 depends on claim 17 and further requires that:

[20] “wherein the conductive layer comprises a first conductive material, and wherein the curved side surface comprises a second conductive material.”

This is also taught by Lee. Per Lee, both its conductive layer 25 and the pad portion PAD on the end of that layer are formed from “conductive” material. Lee, ¶¶ [0040]-[0041]; see also *id.*, ¶ [0021] (noting that “conductive layers” are employed). Again, while this claim does reference a “first conductive material” and

“second conductive material,” the ’666 patent explains that these materials need not be different. *See, e.g.*, Ex. 1001, 1:55-59; Ex. 1003, ¶¶ 438-440.

D. Secondary Considerations

There is no evidence in the ’666 patent’s prosecution history of any pertinent secondary considerations of nonobviousness.

X. Conclusion

For the foregoing reasons, Petitioner respectfully requests institution of IPR and cancellation of claims 17, 19, and 20.

Respectfully submitted,

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Dated: 11/25/2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,942 words.

Dated: 11/25/2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on November 25, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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Copies of this Petition and accompanying documents and exhibits were also served via electronic mail on Patent Owner's counsel of record for related PTAB proceedings and in the related district court litigation – ROPES & GRAY LLP and LATHAW & WATKINS LLP:

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