UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00189
U.S. Patent No. 11,145,666 B2
Issue Date: Oct. 12, 2021

Title: STAIRCASE STRUCTURE FOR MEMORY DEVICE

DECLARATION OF DR. JACK C. LEE IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,145,666

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1. Claim 17 42

[17.Pre] "A memory device, comprising:" *42*

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[17.A] "a substrate, wherein the substrate comprises a top surface;" *43*

[17.B] "a memory string disposed over the substrate; and" ... *44*

[17.C] "a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises;" *46*

[17.C.1] "a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer," *47*

[17.C.2] "wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer." *53*

2. Claim 19 73

[19] "wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack" *73*

3. Claim 20 75

[20] "wherein the conductive layer comprises a first conductive material, and wherein the curved side surface comprises a second conductive material." *75*

C. *Ground 2*: Claims 17, 19, and 20 Are Obvious Over Nam 76

1. Claim 17 76

[17.Pre] "A memory device, comprising:" *76*

[17.A] "a substrate, wherein the substrate comprises a top surface;" *77*

[17.B] "a memory string disposed over the substrate; and" ... *78*

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[17.C] "a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises;" 79

[17.C.1] "a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer," 81

[17.C.2] "wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer." 85

2. Claim 19 96

[19] "wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack" 96

3. Claim 20 98

[20] "wherein the conductive layer comprises a first conductive material, and wherein the curved side surface comprises a second conductive material." 98

D. *Ground 3*: Claims 17, 19, and 20 Are Obvious Over Lee and Park ...98

1. Claim 17 99

[17.Pre] "A memory device, comprising:" 99

[17.A] "a substrate, wherein the substrate comprises a top surface;" 99

[17.B] "a memory string disposed over the substrate; and" .100

[17.C] "a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises;" 102

[17.C.1] "a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer," 103

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[17.C.2] "wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer." *105*

2. Claim 19 120

[19] "wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack" *120*

3. Claim 20 122

[20] "wherein the conductive layer comprises a first conductive material, and wherein the curved side surface comprises a second conductive material." *122*

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I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. ("Micron") as an independent expert consultant in this proceeding before the United States Patent and Trademark Office ("PTO"). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in the claims of U.S. Patent No. 11,145,666, which I refer to herein as the '666 patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of $680 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My *curriculum vitae* ("CV") is attached hereto as Ex. 1004 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and three-dimensional memory technology.

6. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University

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of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley ("UC Berkeley").

7. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

8. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers ("IEEE") International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

9. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin ("UT Austin"). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. This includes classes relating to, among other things, 3D memory technology. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professorship in Engineering in the Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

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10. My current research and teaching interests include semiconductor devices, semiconductor memory applications (including non-volatile memory), fabrication processes, silicon-on-insulator technologies, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, high-K gate dielectrics and electrode, and alternative channel materials. I routinely encounter and address topics relating to NAND flash memory, and more specifically 3D NAND flash memory, in my research. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

11. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 books and book chapters on semiconductor technologies. Many of these relate to the structure and operation of memory devices, including non-volatile memory such as NAND flash memory and 3D NAND flash memory. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., inventor recognition and best paper awards.

12. In 2002, I became an IEEE fellow for my "contributions to the understanding and development of ultra-thin dielectrics and their application to

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silicon devices." I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

13. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

III. ASSIGNMENT AND MATERIALS CONSIDERED

14. I have been asked to provide analysis and explain the subject matter of the '666 patent, including the state of the art when the application underlying the '666 patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '666 patent including how that art relates to the challenged Claims of the '666 patent and to provide my opinions regarding whether that art invalidates the claimed subject matter.

15. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the claims of the '666 patent. Therefore, the fact that I do not address a particular point should

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not be understood to indicate an agreement on my part that any Claim complies with the requirements of any other applicable rule.

16. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the ’666 patent.

17. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the ’666 patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

Exhibit	Description
1005	U.S. Patent No. 10,229,929 to Kim et al. (“Kim”)
1006	U.S. Patent Publication No. 2018/0026046 A1 to Nam et al. (“Nam”)
1007	U.S. Patent Publication No. 2014/0191389 A1 to Lee et al. (“Lee”)
1008	U.S. Patent No. 10,297,543 to Park et al. (“Park”)
1009	U.S. Patent No. 9,589,978 to Yip
1010	Aritome, “NAND Flash Memory Technologies” (2016)
1011	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1012	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1013	Excerpts from the File History of PCT/CN2018/098962

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Exhibit	Description
1014	File History of U.S. Patent No. 10,680,003 (Appl. 16/126,956)
1015	U.S. Patent Publication No. 2015/255385 to Lee
1016	U.S. Patent No. 9,373,540 to Hyun
1017	U.S. Pub. 2011/0031630 A1 to Hashimoto
1018	U.S. Patent No. 9,343,452 to Yun et al.

IV. UNDERSTANDING OF THE LAW

18. I am not an attorney, but have been instructed in and applied the law as described in this section.

19. I understand that the first step in comparing an asserted Claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the claims of the alleged invention in Section V below.

20. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

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21. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

22. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

23. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

24. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that

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it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

25. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

26. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a Claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

27. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one

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field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

28. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

29. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

30. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

31. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a "nexus," between any such secondary indicia and the claimed invention.

32. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

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33. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

34. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

35. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

36. In my opinion, a POSITA in the field of the '666 patent would have had a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) 3D memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may substitute for professional experience).

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37. In my opinion, this POSITA would also have been aware of and generally knowledgeable about 3D memory's structure, its component parts, and how it operates.

38. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile 3D NAND flash memory—I was a person of more than the ordinary level of skill in the art as of August 2017. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed by taking into account the perspective of an ordinarily skilled artisan.

VI. TECHNOLOGICAL BACKGROUND

39. Before addressing the '666 patent in detail, some background on the technology of the '666 patent should be considered.

40. The '666 patent and the prior art discussed in this petition relate generally to three-dimensional (or "3D") memory. One type of memory that is currently implemented as 3D memory is flash.

41. "Flash memory" is a form of "non-volatile memory." Ex. 1009, 1:24-26. "Non-volatile memory is memory that can retain its data values for some extended period without the application of power." *Id.*, 1:26-28. Two common types of flash memory array architectures are the NAND and NOR architectures. NAND offers a higher integration density and occupies a larger market than NOR flash.

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42. NAND flash was first developed in 1987. *See* Ex. 1010, 22.

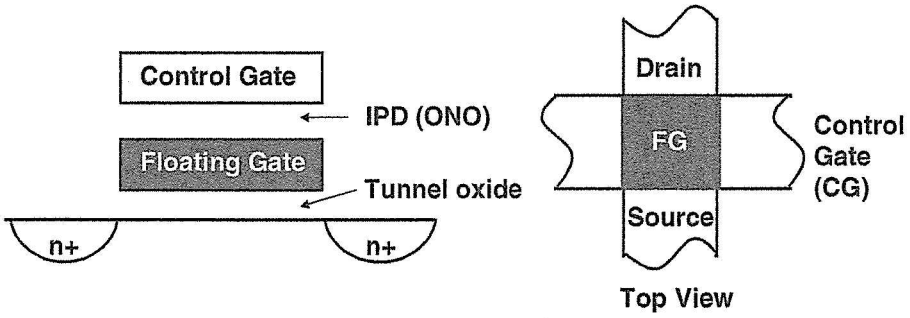
43. NAND flash stores data in a memory "cell" formed from a single transistor that is the logical equivalent of a NOT AND circuit. Ex. 1010, 38-39.

44. In one known type of NAND flash, the memory cell is formed from a "Nch MOS transistor with [a] poly-silicon floating gate (FG)." Ex. 1010, 38-39. The FG is electrically isolated by the surrounding insulating layer, hence the name, "floating" gate and electrons placed on the floating gate are trapped. In other words, "charge is stored in [the] FG" and the "potential of [the] FG is controlled by [a] control gate (CG) voltage with capacitive coupling between [the] CG and FG." *Id.* When negative-charge electrons are stored in the FG, these trapped charges push electrons away from the surface of the substrate (the channel) due to coulombic force. The CG would have to be applied a higher voltage to attract electrons back to the channel in order to turn on the transistor. This means that a negative-charged FG causes an increase in the threshold voltage (e.g., to V_{T0}), in comparison to the threshold voltage of an uncharged FG (V_{T1}). Therefore, by sensing the transistor current by applying a voltage (V_{READ}) on the CG where $V_{T1} < V_{READ} < V_{T0}$, one can determine whether the FG is charged (i.e., the cell is of bit "0") or uncharged (bit "1"). This is essentially the *reading* operation of a NAND flash cell. To *program* (or *write*) a NAND flash memory cell, a high voltage (V_{pgm}) is applied to the CG while keeping substrate/source/drain at 0V. "Electrons are injected to the floating

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gate (FG)" by "a tunneling mechanism through the tunnel oxide" *Id*., 44. The threshold voltage of the memory cell would increase from V_{T1} to V_{T0}. "An erase operation is performed by applying high-voltage (V_{era}) to substrate…while keeping CG at 0V" *Id*. Electrons in the FG are ejected to the substrate through the tunnel oxide.

45. The below figure provides an example of a flash memory cell:

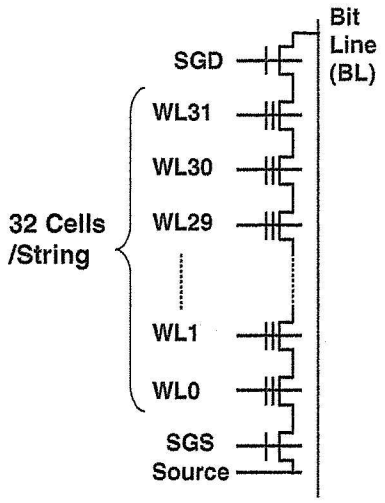


Ex. 1010, 39.

46. Other NAND flash employ a transistor with a "charge trap" layer. *See* Ex. 1011, 109. In this type of transistor, charge is stored in "non-conducting dielectric layer"—like silicon nitride—instead of a floating gate. *See id*.

47. NAND flash memory cells are arranged in so-called "strings" with multiple cells "connected in series." Ex. 1010, 38. The source of one cell is connected to the drain of the next one. Depending on the technology, typically a string consists of 32 to 128 NAND cells. An example of one such string is shown below:

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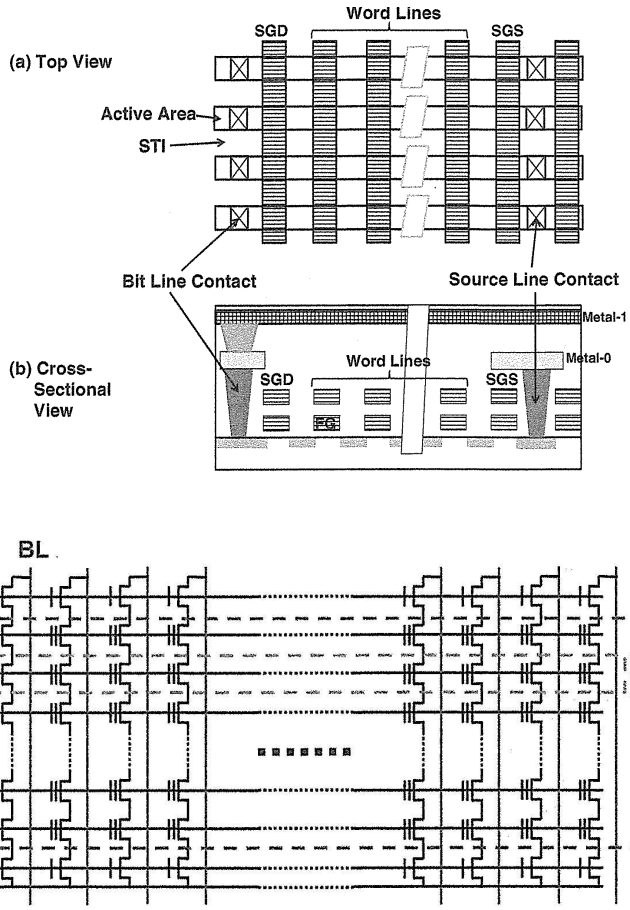
Ex. 1010, 39.

48. Early NAND flash devices were formed as two-dimensional arrays on a substrate surface.

49. Here, the "memory array is formed by straight active area lines … and straight gate lines" located on a substrate surface. Ex. 1010, 38. Memory cells are located at the "intersection[s]" of the lines. *Id.*

50. An example of a two-dimensional NAND flash memory array is shown below. Figures (a) and (b) illustrate the top view and the cross-sectional view of the memory array, respectively. The third figure shows the circuit schematic drawing of the memory array.

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Ex. 1010, 40.

51. As also shown, the cells are grouped into "page[s]" extending along the word lines and "block[s]" which include all the pages along the bit lines, excluding the SGD and the SGS select transistors Ex. 1010, 40. "[R]ead and program operations are performed per page" while "the erase operation is performed per block." Ex. 1010, 39. For example, to *read* a selected group of cells, e.g., all the memory cells on the page along WL30 in the circuit schematic above, the voltage on the CG (WL30) is pulled up to V_{READ} while all other word lines (unselected cells) are pulled up above V_{T0}. This way all "[the] unselected cells act as pass transistors."

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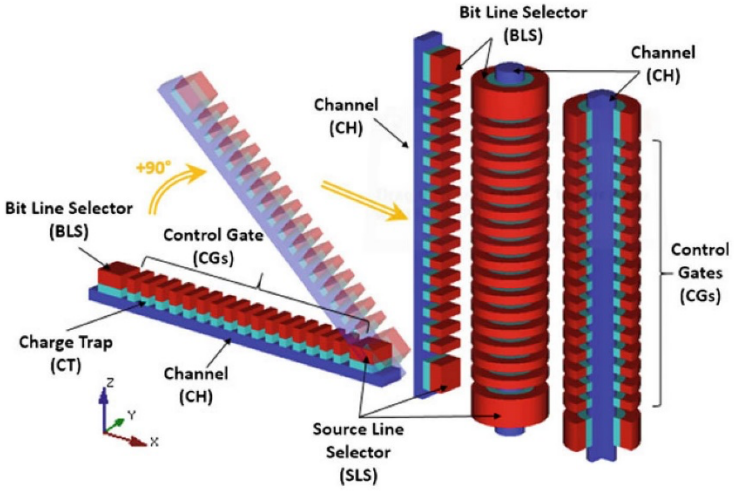
Id., 45. A string is selected by a bit line and the drain-end select gate transistor (SGD). The string of memory cells along a bit line would conduct if the selected cell is programmed to bit "1", i.e. uncharged FG. The *program* operation of the NAND flash is similar to the read operation, except a higher voltage (V_{pgm}) is used on the selected page. The *erase* operation is performed in the entire block consisting of multiple pages. "The word[]lines of the selected blocks are grounded" (*id*., 47) while high erase voltage (V_{era}) is applied to the p-well (i.e., the "substrate" in the memory cell area). This causes extraction of electrons from the FG into the p-well via tunneling mechanism. All the memory cells in the block are then set to bit "1." Since the block size is the minimum granularity of erase operation, reducing the block size could reduce the system burden of the data management and thereby improve system performance.

52. To boost data storage densities and reduce cost per gigabit, the art developed so-called "three-dimensional (3D) NAND flash cells" starting in about 2006. Ex. 1010, 292.

53. In 3D NAND, rather than arranging memory cells in a two-dimensional array, 3D NAND arranges cells in a three-dimensional array that is built up in layers. "Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1012, 3.

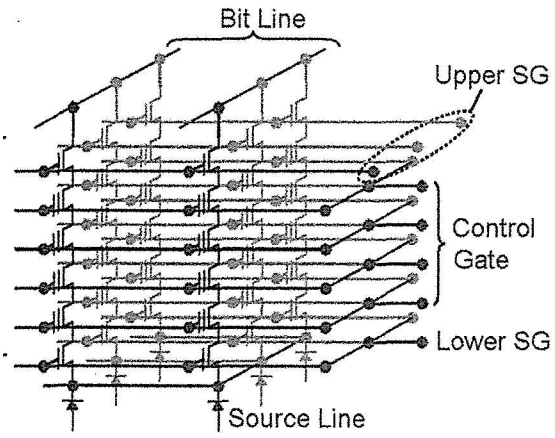
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54. The following image provides an example:



Ex. 1011, 122.

55. Multiple of such vertical channels are then repeated in a three-dimensional array:



Ex. 1010, 296.

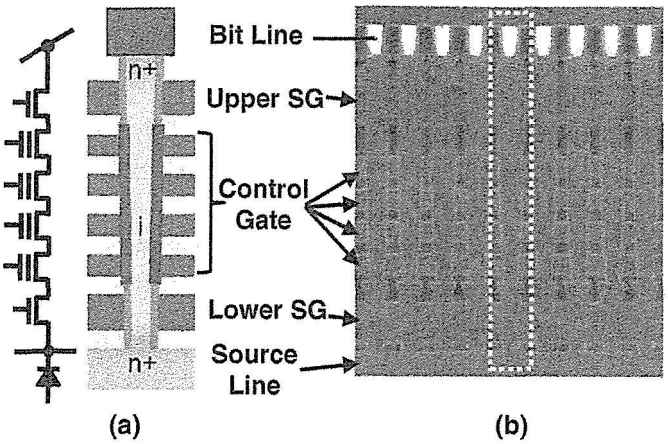
56. 3D NAND includes "multi-stacked layers of gate (plate)" material alternated with "dielectric" "deposited" in a "[s]tack." Ex. 1010, 294. The flash memory device offers the industry's highest layer count and the highest areal density

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(bits per unit area). A "through-hole is fabricated through" the layers and is "filled by memory film … and channel poly-Si" to form a string of vertically arranged memory cells. *Id.*, 294-95. "Each" layer of "electrode plate acts as a control gate except the lowest plate," which "function[s] as the lower select gate (lower SG)", i.e., SGS, the source-end select gate transistor. *Id.*, 295.

57. "A single bit" of memory cell "is located" at "the intersection of a control gate plate" and the memory film/poly-Si channel. Ex. 1010, 295.

58. An example 3D NAND vertical memory cell string is shown below:



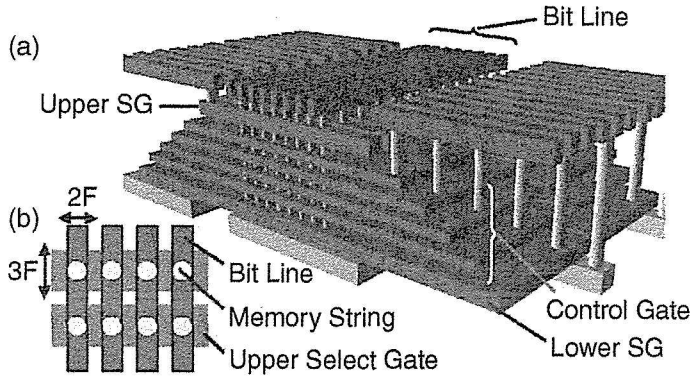
Ex. 1010, 296.

59. For purposes of programming the cells in a memory string, the "string is selected by a bit line and an upper select gate (upper SG)." Ex. 1010, 295.

60. "[T]he control gates and upper/lower SG are connected" to the memory's conductive "layers at [a] stair-like gate structure" located outside the memory array. Ex. 1010, 295, 297. The stair-like (terrace) structure is created to

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expose and allow connection to each conductive layer via vertical word line contacts. The conductive layers are insulated from each other by insulating materials, also known as "dielectrics." The dielectric layers serve the purposes of preventing interference of electrical signals from one conductive layer to other layers and providing structural support so that the conductive structures do not collapse. An example of this is shown below:



Ex. 1010, 296.

61. "Production of 3D NAND flash memory … started in August 2013." Ex. 1010, 393.

VII. THE '666 PATENT

A. Effective Filing Date

62. I understand that the application leading to the '666 patent was filed on May 28, 2020.

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63. Based on my review of the ’666 patent, I note that it identifies itself as a continuation of another U.S. application filed September 10, 2018 and a PCT application filed August 6, 2018. It also identifies an August 28, 2017 foreign filing.

64. For purposes of this declaration, I have been instructed to use August 28, 2017 as the effective filing date of the ’666 patent. My opinions in this declaration were formed from the perspective of a POSITA as of August 28, 2017, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

B. Overview

65. The ’666 patent relates generally to “a staircase structure for a memory device (e.g., 3D memory device).” Ex. 1001, 1:37-39.

66. The patent notes that this structure somehow results in “yield and manufacturing cost improvements.” Ex. 1001, 1:39-41. But it never explains why that is the case.

67. The patent goes on to reference “3D memory devices” that include “vertically oriented strings of memory cell transistors.” Ex. 1001, 5:6-11.

68. The “3D memory device[’s]” “staircase structures[]” is “disposed adjacent to” these “memory strings for word line, fan-out….” Ex. 1001, 5:31-33.

69. “FIG. 8 illustrates a cross-sectional view of a staircase structure 800 with a dielectric layer 825 disposed thereon.” Ex. 1001, 9:35-37.

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70. The structure includes alternating "insulating layer[s] 502" and "wordline layer[s] 804." Ex. 1001, 9:48-50.

71. The layers are located over a "substrate." Ex. 1001, 6:1-2.

72. Each wordline layer includes a "landing pad 820 and conductive layer 840" and is intended to "control a portion of a memory string in the stacked storage region of a memory device." Ex. 1001, 9:57-61.

73. The "landing pad 820 contacts a portion of a side of insulating layer 502." Ex. 1001, 9:61-65.

74. The "landing pad 820" can be "made of the same or different conductive material as conductive layer 840." Ex. 1001, 10:3-5.

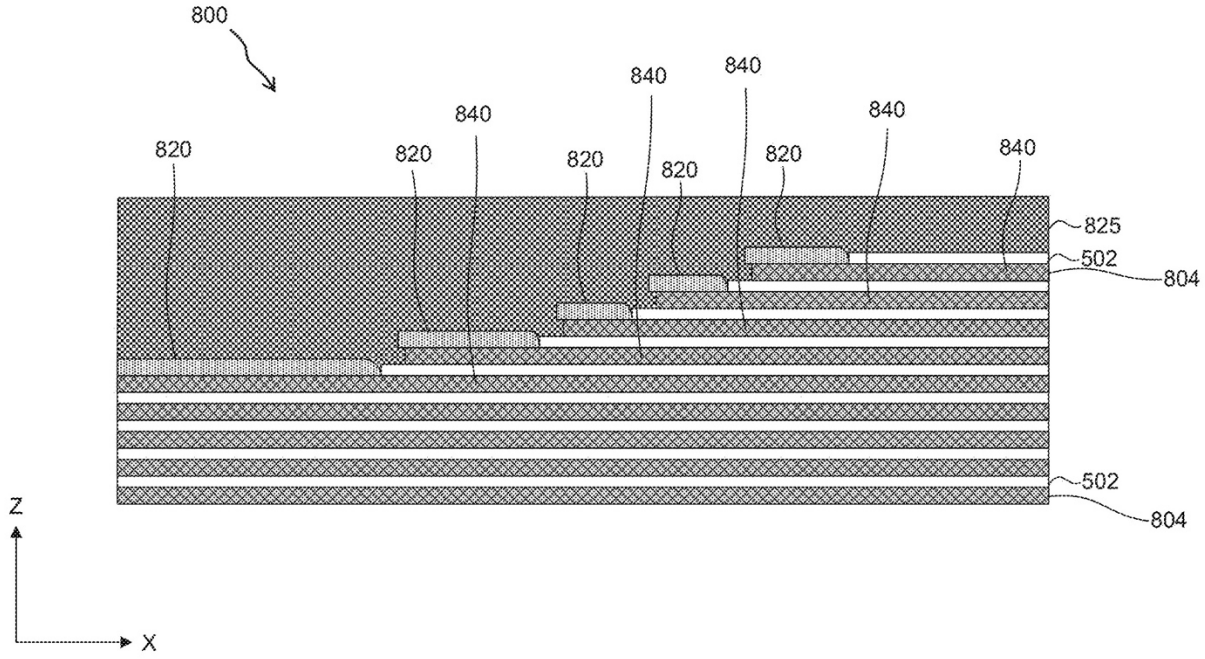


FIG. 8

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Ex. 1001, Fig. 8

C. Prosecution History

75. As noted above, I have reviewed the '666 patent's prosecution history.

76. The '666 patent was filed May 28, 2020 as U.S. App. 16/885,858 (the "'858 App.") and identifies itself as a continuation of both a 2018 PCT application (PCT/CN2018/098962) and U.S. App. 16/126,956 (the "'956 App."). *See* Ex. 1001, Cover.

77. Neither the PCT nor the '956 App. included a claim requiring a "curved side surface" like issued independent Claim 17 does here. *See* Ex. 1013, 21-24; Ex. 1014, 36-39.

78. During pendency of the PCT application, a written opinion issued comparing U.S. Pub. 2015/255385 to Lee ("Lee 385," Ex. 1015) to the claims. *See* Ex. 1014, 177.

79. While Lee—one of the references at issue in this Petition—and Lee 385 have the same set of inventors, these references' respective disclosures are substantively different.

80. Lee 385 does teach a memory device with a staircase structure formed from alternating conductive and insulating layers. *See* Ex. 1015, ¶¶ [0003], [0009].

81. Lee 385's device also includes a "pad part" on each of its conductive layers. Ex. 1015, ¶ [0010]. This pad can be structured in different ways. *See, e.g.,*

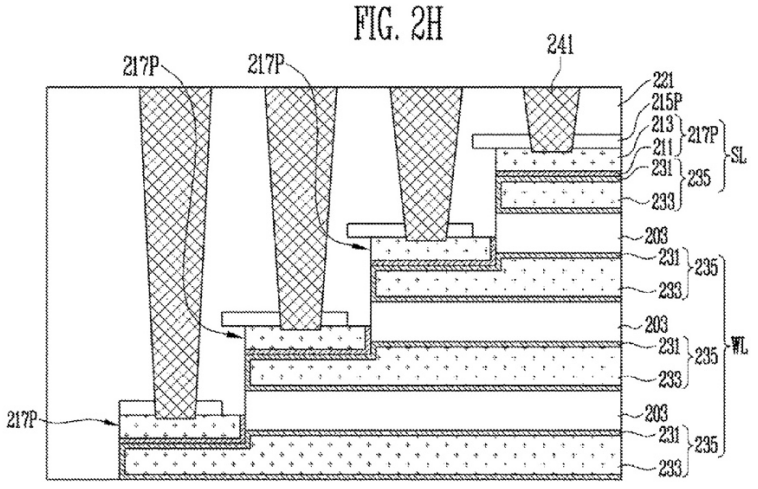
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id., Figs. 1A-1D. But none of Lee 385's pads appear to include the "curved side surface" that Claim 17 of the '666 patent requires.

82. Moreover, in Lee 385, the insulation layers between the conductive layers are structured differently than those in the Lee reference discussed in this Petition. *Compare* Lee, Fig. 7A with Lee 385, Fig. 2F.

83. Prior art was also discussed during the prosecution of the '956 App. This art included U.S. Patent No. 9,373,540 to Hyun ("Hyun," Ex. 1016) and U.S. Pub. 2011/0031630 A1 to Hashimoto ("Hashimoto," Ex. 1017). *See* Ex. 1014, 202-208.

84. The discussion of Hyun focused on Figure 2H, which is reproduced below:



Ex. 1016, Fig. 2H.

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85. The Examiner explained that this figure shows a "staircase structure" formed from alternating insulating (203) and conductive (235) layers. *See* Ex. 1014, 204. The device also includes "landing pads" (217P) on each conductive layer. *Id.* As shown and further discussed in Hyun, each landing pad is also covered by a protective layer of insulation 215P. *See* Ex. 1016, 6:66-7:14.

86. The discussion of Hashimoto focused on Figure 11B shown below:

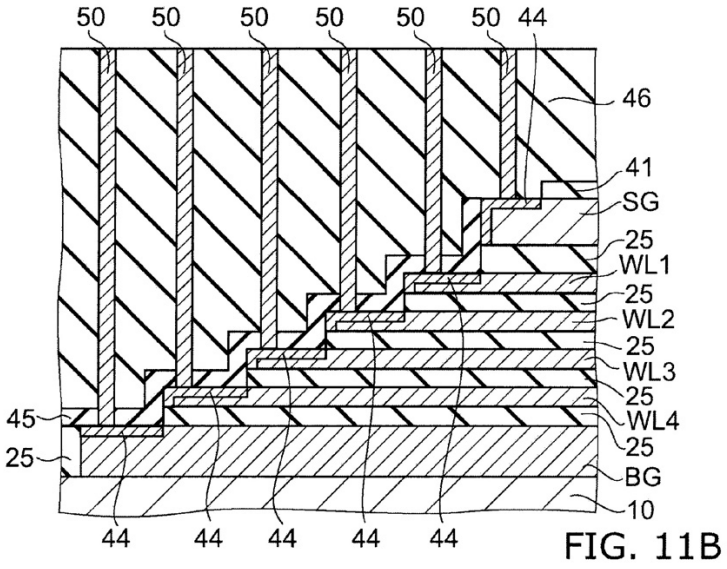


FIG. 11B

Ex. 1017, Fig. 11B.

87. The Examiner explained that this figure also shows a device with a "staircase structure" with alternating conductive (WL) and insulating (25) layers. *See* Ex. 1014, 206. Each conductive layer includes a "landing pad" (44). *Id.* Like the prior art discussed during the PCT, Hyun and Hashimoto do not appear to illustrate landing pads with the type of "curved side surface" that Claim 17 of the '666 patent requires.

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88. The application underlying the ’666 patent was filed next. Independent Claim 17 was part of the application at the time of filing. *See* Ex. 1002, 31-34.

89. The application also included two other independent Claims: 1 and 9. *See* Ex. 1002, 31-34. Neither of these claims required the same “curved side surface” that issued Claim 17 requires.

90. Claim 1 was rejected for nonstatutory double patenting over the patent that issued from the ’956 App. Ex. 1002, 103-109. Independent Claims 9 and 17 were allowed without rejection. *See id.*

91. In response to this rejection, the applicant amended Claim 1 to require that the “top surface” of the “landing pad” be “above” the “top surface” of an adjacent insulating layer (i.e., the landing pad must be thicker than the insulating layer). *See* Ex. 1002, 128.

92. This led to allowance of all the pending claims. *See* Ex. 1002, 138-142. The Examiner did not issue a statement explaining why the allowed claims differed from the prior art. *See generally id.*

D. Claims

93. For reference, Claims 17, 19, and 20 of the ’666 patent are reproduced below:

17. A memory device, comprising:

a substrate, wherein the substrate comprises a top surface;

a memory string disposed over the substrate; and

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a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:

a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.

19. The memory device of Claim **17**, wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack.

20. The memory device of Claim **17**, wherein the conductive layer comprises a first conductive material, and wherein the curved side surface comprises a second conductive material.

VIII. CLAIM CONSTRUCTION

94. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

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95. I have been informed that the words of a claim are generally given their plain and ordinary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the "intrinsic evidence" or "intrinsic record").

96. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the "extrinsic evidence" or the "extrinsic record"), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

97. In my opinion, the terms of the '666 patent's claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration. I have provided further discussion of how a POSITA would have understood the '666 patent's claim terms in the sections below.

IX. UNPATENTABILITY ANALYSIS

98. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the '666 patent, a POSITA would have considered Claims 17, 19, and 20 of the '666 patent to be unpatentable as obvious over the prior art discussed in this declaration.

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A. Overview of the Prior Art

99. The following paragraphs provide an overview of the main prior art references I discuss throughout this declaration.

1. Kim

100. Kim (Ex. 1005) indicates on its face that it was filed in the U.S. on July 18, 2017. *See* Kim, Cover. In view of this date filing, which is before the '666 patent's own August 2017 effective filing date, I understand that Kim is prior art under 35 U.S.C. § 102(a)(2).

101. Kim relates to "semiconductor memory devices having enhanced reliability." Kim, 1:38-39.

102. The device can be implemented as a "3D semiconductor memory device[]" with "memory cells … arrayed in 3D." Kim, 1:26-30.

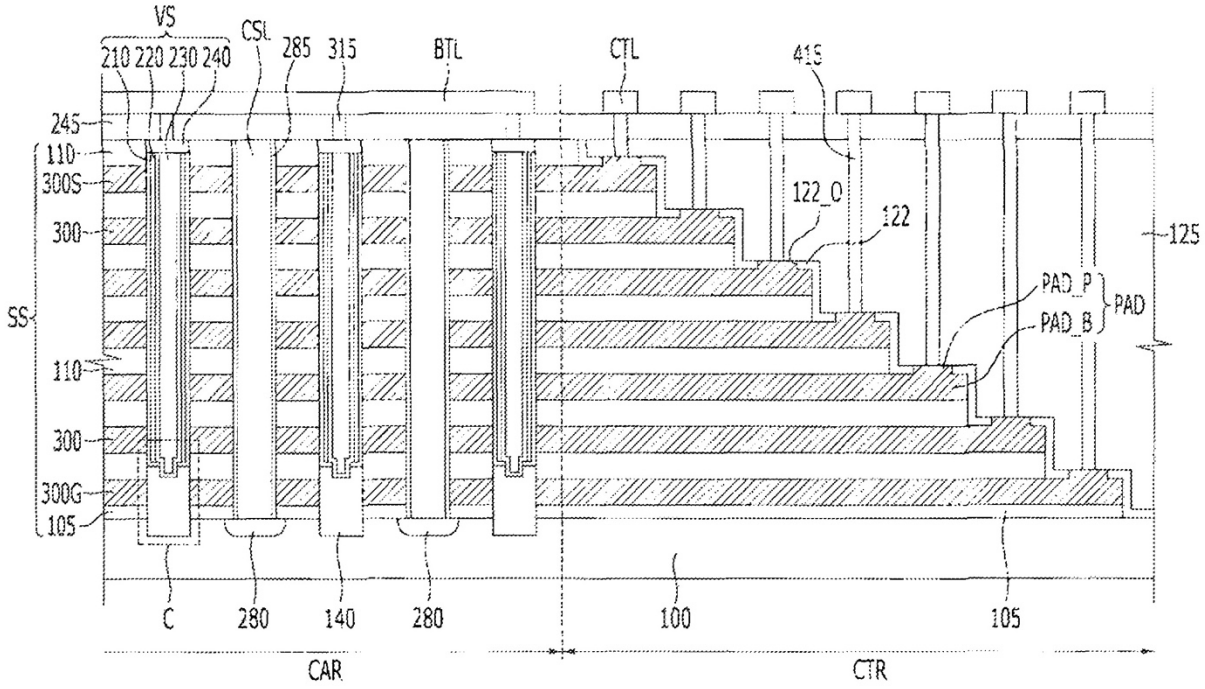
103. According to Kim, the device includes a "cell array region" and a "contact region." Kim, 1:41-45.

104. The "cell array region" includes "memory cell[s]" arranged in vertically oriented memory "cell strings." Kim, 4:26-28; *see also* Fig. 3 (showing Kim's 3D array of memory cells with multiple example cell strings "CS"). The "contact region" includes a "stacking structure" with a "stepwise structure." *Id*., 1:40-47.

105. Figure 4B—reproduced below—provides an example of one such "contact region":

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FIG. 4B



Kim, Fig. 4B.

106. As shown, a step-shaped "stacking structure SS" is formed from a "plurality" of alternating "insulating layers 110 and … gate electrodes 300" located over a "substrate 100." Kim, 5:53-55; Fig. 4B.

107. The "gate electrodes" are formed from conductive material. Kim, 6:31-35.

108. The insulating layer 110 can be integrated with an "auxiliary insulating layer 122." Kim, 9:29-38.

109. Each gate electrode 300 includes a "pad unit PAD" formed from "a base pad PAD_B and a protrusion pad PAD_P…." Kim, 7:58-62. The pad units PAD

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"electrically and physically connect" the gate electrodes 300 to an upper "connection line CTL." *Id.*, 9:64-66.

110. As shown in Figure 4B, "protrusion pad PAD_P" is located "inside" and is touching the sides of "opening 122_O" in Kim's insulation layer 122. Kim, 9:21-23.

111. While PAD_P is shown with a rectangular shape in the figure, Kim explains that it can "[also] have a shape including a curved surface based on a virtual rectangular parallel[] shape, a cylindrical shape, or any shape." Kim, 8:29-34.

2. Nam

112. Nam (Ex. 1006) indicates on its face that it was filed in the U.S. on December 12, 2016. *See* Nam, Cover. This predates the '666 patent's own August 2017 filing. In view of this, I understand that Nam is prior art under 35 U.S.C. § 102(a)(2).

113. Nam relates to "memory device[s]" such as a "NAND flash device" with arrays of memory cells. Nam, ¶¶ [0002]. [0025], [0032], Figs. 1-2. The memory cells are arranged in vertically oriented "cell strings" located over a substrate. *Id.*, ¶¶ [0025]-[0026], [0033]; Figs. 2-3. The device includes both a "cell array region CAR" including the memory strings and a "contact region CTR" allowing for electrical connection to other circuitry. *Id.*, ¶¶ [0043], [0062]. The contact region has a "stepped shape." *Id.*, ¶ [0043].

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114. Nam's device also includes a "stack of alternating first interlayer insulating layers and gate electrode layers on a substrate." Nam, ¶ [0005]. Each gate electrode ends with a contact "pad region" that is thicker than the rest of the gate electrode to which it is attached. *Id.*, ¶ [0045]. Nam explains that thinner gate electrodes mean that "integration" can be "improved" via an "increased" "number of stacked gate electrode layers." *Id.*, ¶¶ [0044], [0108]. Thicker contacts improve manufacturability and prevent "short circuits." *Id.*, ¶¶ [0044]-[0045].

115. Per Nam, its contact pads can have a variety of shapes. In one example, the pads have a "convex or bull nose shape." Nam, ¶ [0066]. This is shown in Figure 7:

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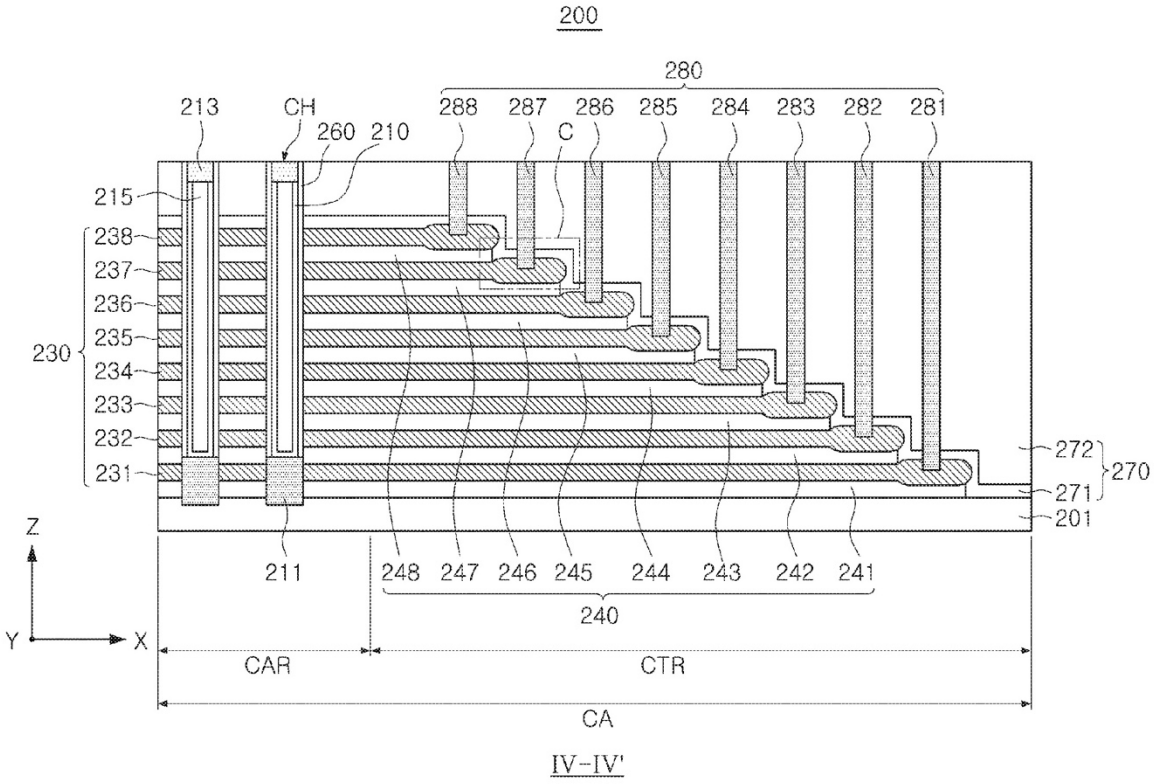


FIG. 7

Nam, Fig. 7.

116. Figure 8A shows the contact pad in greater detail:

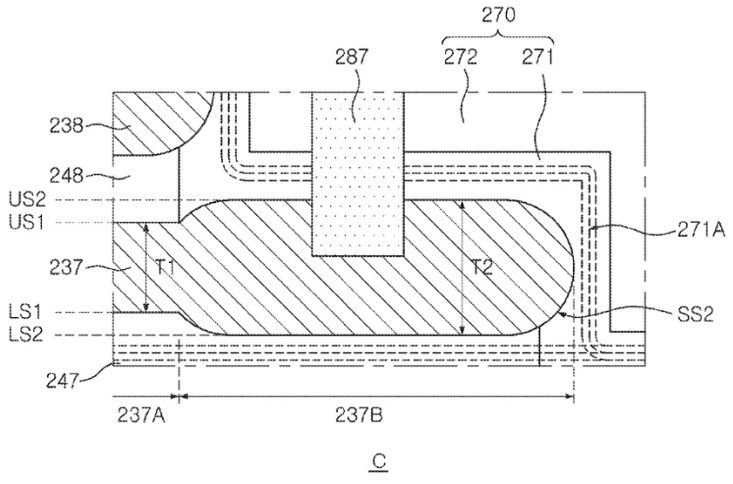


FIG. 8A

Nam, Fig. 8A.

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3. Lee

117. Lee (Ex. 1007) indicates on its face that was filed in the U.S. on March 18, 2013 and published on July 10, 2014. Lee, Cover. In view of these dates of filing and publication, both of which pre-date the '666 patent's own August 2017 filing, I understand that Lee is prior art under AIA §§ 102(a)(1) and 102(a)(2).

118. Lee relates to "semiconductor device[s]" such as "three-dimensional (3D) non-volatile memory devices." Lee, ¶¶ [0005], [0008]-[0009].

119. Per Lee, this type of device is intended to "increase[] … integration" of a memory by including more memory cells in a smaller space. Lee, ¶ [0005].

120. Lee goes on to explain that this type of memory includes "interlayer insulating layers and word lines stacked alternately with each other" over a substrate. Lee, ¶ [0006].

121. "[C]hannel layers" pass through the stack to form "[m]emory cells." Lee, ¶ [0006]. The stack is "patterned stepwise" to allow for connection or contact with each layer. *Id.*, ¶ [0009].

122. According to Lee, existing three-dimensional memories encountered difficulties when "form[ing] pad portions on word lines stacked on top of one another…." Lee, ¶ [0007]. In these devices, "a punch phenomenon may occur in which a contact plug passes through a pad portion, or the contact plug and the pad

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portion are not coupled to each other since a pad portion is not exposed along a bottom surface of a contact hole." *Id.*

123. Lee then goes on to discuss a "semiconductor device" that, like known three-dimensional memories, includes a "stacked structure ST" with alternately arranged "insulating layers" and "conductive layers." Lee, ¶¶ [0020]-[0021].

124. The "stacked structure ST" is "patterned stepwise" with an "insulating layer … located on [the] top surface of each step." Lee, ¶ [0021].

125. To address the problems with prior art memories, however, Lee includes "pad portions PAD" at the end of each of conductive layers in a "contact region CONTACT" of its stepped "stacked structure ST." Lee, ¶¶ [0022]-[0023].

126. "The pad portions PAD" have a "greater thickness than unexposed portions of the … conductive layer[s]." Lee, ¶ [0023]. Use of a thicker pad prevents the various contact problems experienced by prior art devices. *See id.*, ¶ [0043].

127. Lee's pads are shown in both Figures 1A (a three-dimensional view) and 7B (a cross-sectional view):

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FIG. 1A

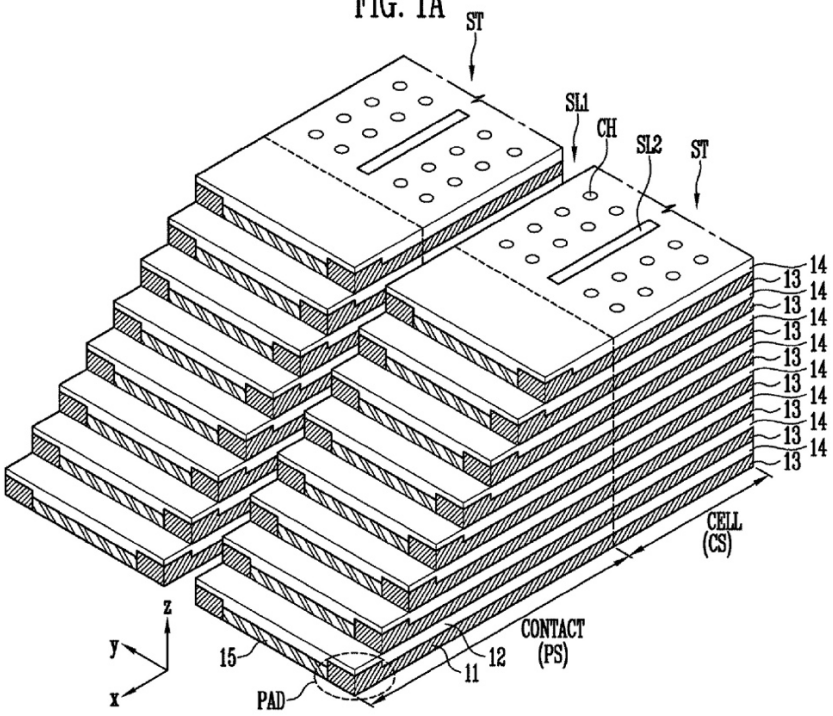
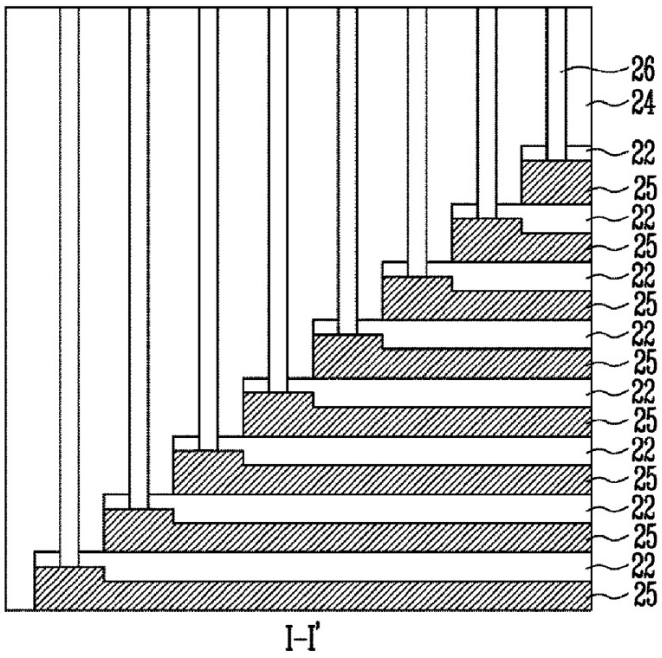


FIG. 7B



Lee, Figs. 1A, 7B.

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4. Park

128. Park (Ex. 1008) indicates on its face that it was filed in the U.S. on June 13, 2017. Park, Cover. As this date of filing pre-dates the '666 patent's own August 2017 filing, I understand that Park is prior art under AIA § 102(a)(2).

129. Park relates to a "vertical semiconductor device" with an array of "stacked" "memory cells." Park, 1:14-16.

130. The device includes a stepped "connection region" with alternating conductive gate electrodes and insulating layers. Park, 6:7-12.

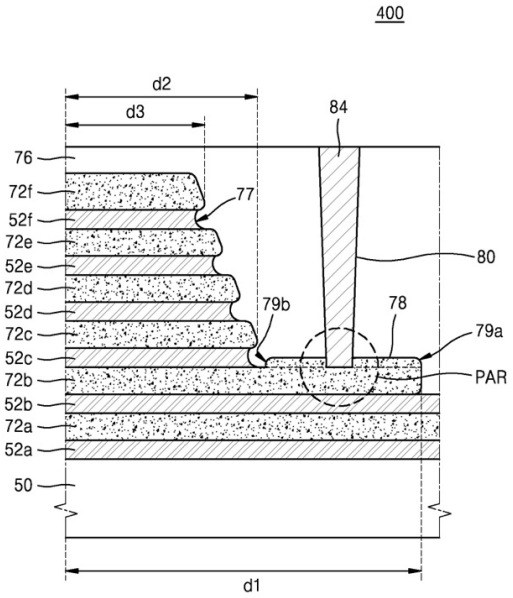
131. Raised "[p]ad region[s] PAR" are located on the ends of gate electrodes. Park, 6:7-12, 6:36-47, 7:4-16.

132. Park also explains that rather than having straight sides, an "end 79b" of each of these "raised pad portion 78" may be "rounded" to "prevent a short circuit" between the pad and an "adjacent … conductive layer pattern 72c." Park, 11:35-41.

133. This is shown in Figure 7 from Park below:

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FIG. 7



Park, Fig. 7.

B. *Ground 1*: Claims 17, 19, and 20 Are Obvious Over Kim

134. In my opinion, a POSITA would have considered Kim to be within the scope of the prior art and highly relevant to the patentability of the '666 patent's claims.

135. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Kim renders Claims 17, 19, and 20 of the '666 patent obvious.

1. Claim 17

[17.Pre] "A memory device, comprising:"

136. To the extent this preamble language is limiting, in my opinion it is taught by Kim.

137. Kim relates to "a semiconductor memory device." Kim, Abstract.

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138. Indeed, Kim repeatedly explains that "[e]mbodiments of the inventive concepts relate to semiconductor memory devices…." Kim, 1:15-17; *see also id.*, 1:38-39 ("[T]he inventive concepts … provide semiconductor memory devices having enhanced reliability."); 3:43-44 ("FIG. 1 is a block diagram illustrating a schematic configuration of a plan view [of] a semiconductor memory device…."); Fig. 1.

139. Moreover, Kim explains that it relates not just to memory, but to three-dimensional memory. In particular, Kim's device can be a "3D semiconductor memory device[]" with "memory cells … arrayed in 3D" for purposes of improving "integration." Kim, 1:26-30; *see also id.*, Figs. 3, 4A, 4B, 5-9.

140. The "integration" of a memory device refers to the number of memory cells arranged in a particular space. By forming its memory three-dimensionally, Kim is able to locate more memory cells within a given device footprint.

[17.A] "a substrate, wherein the substrate comprises a top surface;"

141. In my opinion, Kim teaches a ***"substrate"*** with a ***"top surface."***

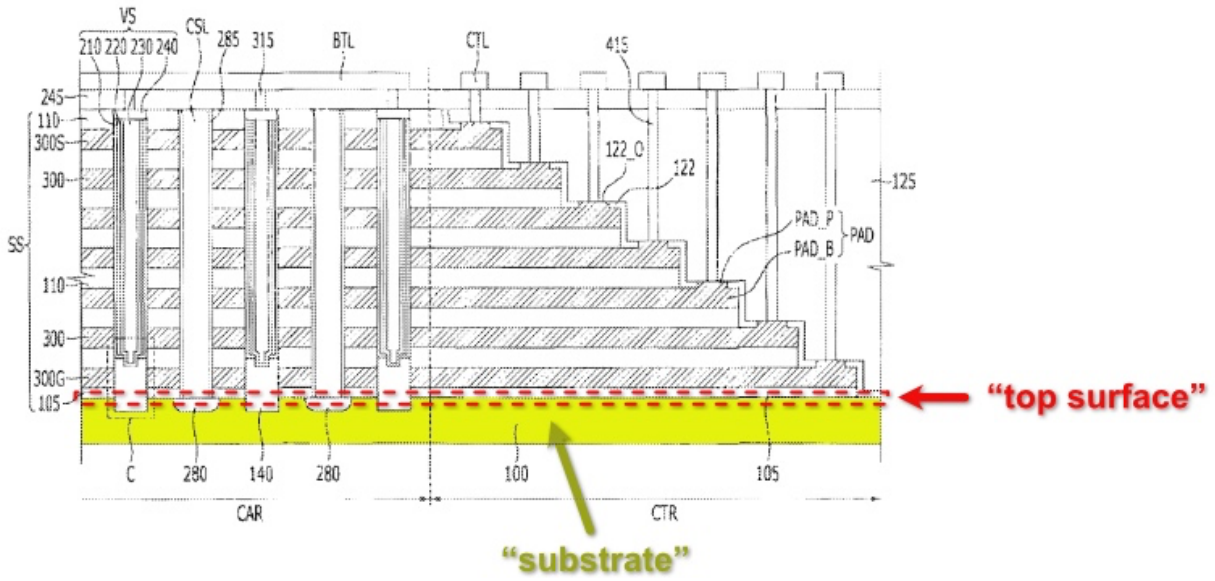
142. Kim's "semiconductor memory device" includes a "substrate 100." Kim, 5:33-39. This "substrate 100 may include a semiconductor material and may be, for example, a silicon substrate, a germanium substrate, a silicon-germanium substrate, or a silicon-on-insulator (SOI substrate)." *Id.*, 5:40-45.

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143. Further, as in most substrates, Kim's "substrate" includes an "upper surface" on which "a plurality of gate electrodes" are "stacked." Kim, 2:3-10; *see also id.*, 5:45-52 (similarly referencing the "uppermost surface of the substrate 100"); 6:7-9, 6:37-38, 13:35-38 (also referencing the upper surface of substrate 100).

144. Figure 4B of Kim is reproduced below. The substrate 100 is highlighted yellow, while the top surface of this substrate is indicated by red dashed circling. As can be seen, the rest of Kim's memory device is located above the top surface of the substrate:

FIG. 4B



Kim, Fig. 4B (annotated).

[17.B] "a memory string disposed over the substrate; and"

145. In my opinion, what this limitation requires is also taught by Kim.

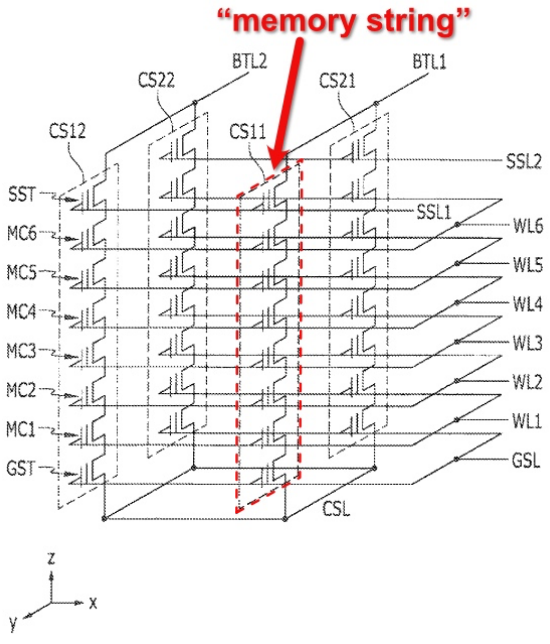
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146. According to Kim, its "semiconductor memory device" includes a "cell array region" on the substrate. Kim, 1:41-45. This "memory cell array may include a plurality of cell strings…." *Id.*, 4:26-28.

147. Again, in Kim, the "memory cells … are arrayed in 3D." Because of this, the "cell strings" have a "vertical structure" and thus "extend[] in a vertical direction (z direction) to a plane of a substrate." Kim, 1:28-30; 4:28-31.

148. Figure 3 of Kim is reproduced below. This figure provides a basic circuit diagram of Kim's memory cell array. One such memory cell string (the cell string labeled CS11) is annotated with red dashed circling:

FIG. 3



Kim, Fig. 3 (annotated).

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149. Kim's memory strings are also shown in other figures. For instance, Figure 4B depicts a vertical stacking structure "VS" that is located over Kim's substrate 100 and forms a vertically oriented string of memory cells. *See* Kim, Fig. 4B. Kim's memory cell string is located along this vertical stacking structure.

[17.C] "a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises;"

150. Kim, in my opinion, also teaches what this limitation requires.

151. According to Kim, the "semiconductor memory device" includes both a "cell array region" and an adjacent "contact region." Kim, 1:40-47.

152. The "contact region" includes a "stacking structure" with a "stepwise structure." Kim, 1:40-47. The "stepwise structures" facilitate connection to its conductive layers. *Id.*, 1:15-17.

153. Figure 4B, which is reproduced below, provides an example of this stepped contact structure.

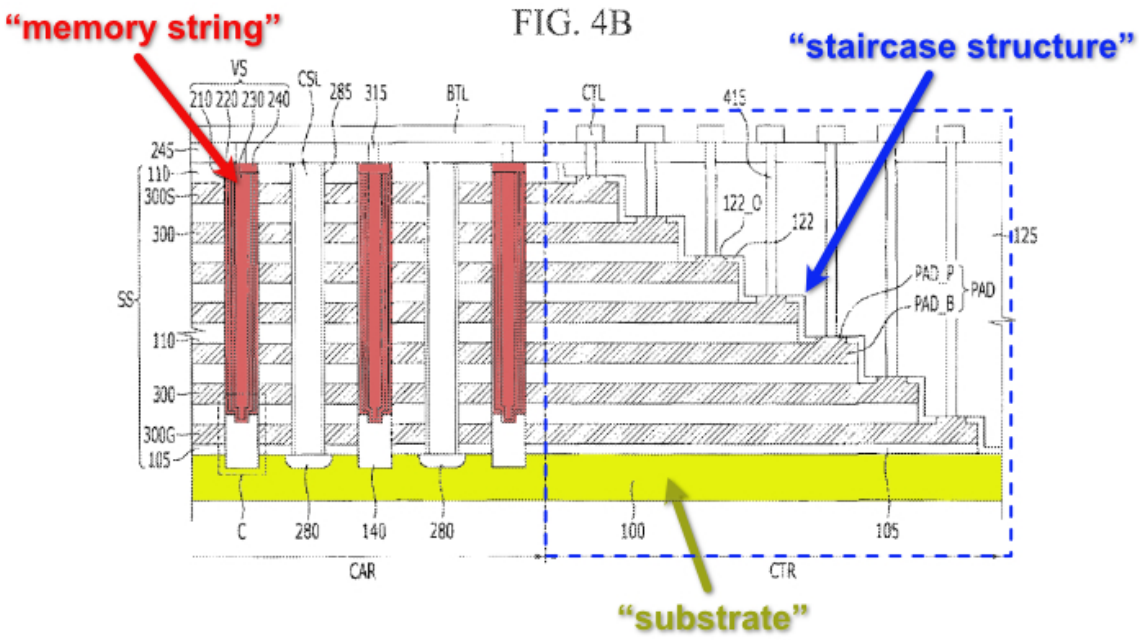
154. As shown in the figure, Kim's device includes a "cell array region (CAR)" that includes "vertical pattern structure[s] VS" forming strings of memory cells. Kim, 5:33-39.

155. A "contact region CTR" with a stepped structure is "positioned on the periphery of the cell array region CAR." Kim, 5:33-39; *see also id.* 3:52-62 (similarly explaining that Kim's "memory device" includes a "cell array region (CAR)" with "a plurality of memory cells" and an adjacent "contact region CTR");

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6:42-46 (the "vertical pattern structures VS" are "surrounded by the" step-shaped "stacking structure SS on an xy-direction plane").

156. Both Kim's ***"staircase structure"*** (stepped contact region CTR, outlined with blue dashes) and example ***"adjacent" "memory string[s]"*** (vertical structures VS, annotated red) are shown below:



Kim, Fig. 4B (annotated).

[17.C.1] "a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer,"

157. Claim 17 next requires a ***"plurality of layer stacks."*** Each ***"layer stack"*** in this plurality must include an ***"insulating"*** and ***"conductive" "layer."*** The ***"insulating layer"*** must be ***"disposed over"*** a ***"first portion of a conductive layer."***

158. In my opinion, this is taught by Kim.

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159. Before discussing Kim's teachings, I will briefly summarize how the '666 patent intends the terms "layer stack" and "layer" to mean.

160. Claim 17 itself specifies what makes up the claimed "layer stack." In particular, "each" such stack must include insulation over a conductive layer.

161. This, however, is all a POSITA would have understood this limitation to require. Among other things, there is no requirement that the insulation and conductive material making up the "layer stack" be coextensive. Showing this, Claim 17 itself provides that insulation is only required to be "over" a "portion" of the underlying conductive layer. This is also what the '666 patent's figures show. *See, e.g.* Ex. 1001, Fig. 8 (showing each insulation layer 502 covering only a portion of the underlying conductive layer 804).

162. Next, the claim does not require that the insulation and conductive layers form steps in any particular way. Claim 17 requires only that that "staircase structure" include a "plurality of layer stacks." No particular layer is required to form the top of the steps in the staircase so long as there is a stepped structure.

163. The claim also does not require that the entirety of the "staircase structure" from top to bottom be formed from insulation over conductive material. Instead, there simply must be a "plurality of layer stacks" (i.e., more than one), where each such layer includes insulation over conductive material.

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164. The ’666 patent also includes a paragraph discussing what it intends the term “layer” to mean. *See* Ex. 1001, 4:36-56.

165. In this paragraph, the patent explains that, a “layer” does not need to be only a single, defined layer of homogenous material. Instead, a “layer can include ***multiple*** layers” and can be “***inhomogenous***.” Ex. 1001, 4:36-56 (emphasis added). The patent also explains that a “layer” can simply be material “located between any set of horizontal planes….” *Id.*, 4:45-47.

166. Moving back to Kim, Kim explains that its memory device includes a step-shaped “stacking structure SS” formed from a “plurality” of alternating “insulating layers 110 and … gate electrodes 300” located “on the substrate 100.” Kim, 5:53-55. Likewise, Kim notes that the “stacking structure” includes “a plurality of insulating layers and a plurality of gate electrodes alternately stacked on the substrate. The stacking structure may” have “a stepwise structure….” *Id.*, 1:41-46.

167. The “gate electrodes 300” can be formed from conductive material such as, among other things, “metal (for example, tungsten, copper, and aluminum)….” Kim, 6:31-35.

168. “The plurality of insulating layers 110 may be, for example, silicon oxide layers.” Kim, 6:35-36.

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169. Kim's device includes an "auxiliary insulating layer 122." Kim, 9:12-13.

170. "The auxiliary insulating layer 122 may include the same or similar material as the insulating layer 110" such that "a boundary between the auxiliary insulating layer 122 and the insulating layer 110 may not be distinguished and the auxiliary insulating layer 122 and the insulating layer 110 may form one structure." Kim, 9:29-38.

171. Kim forms the auxiliary layer 122 immediately after forming its staircase such that this layer such becomes "one structure" with the insulating layers 122 to extend the insulating layers in the horizonal direction. Kim, 12:34-37.

172. In my opinion, a POSITA would have understood that Kim's insulating layer 110 and the adjacent portion of auxiliary insulation layer 122 together constitute the claimed ***"insulating layer"*** in a ***"layer stack."***

173. To begin, in Kim, layers 110 are located between and serve to separate the gate electrodes 300 making up Kim's stack. Kim, 5:53-55; Fig. 4B.

174. A POSITA would have recognized that layer 122 also forms an integral part of this same stack. It is not simply a conformal or protecting layer of oxide applied over complete conductive layers with contact pads.

175. Rather than being a protective layer, layer 122 is applied ***before*** Kim's contact pads are formed. In particular, after "the plurality of insulating layers 110"

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are "patterned in the stepwise structure in the contact region CTR," then the auxiliary insulating layer 122: is "formed thereon." *See* Kim, 12:34-37; Fig. 11.

176. Then, the layer 122 is used to form the contact pads. An "ion injection process" is used to form a "doped region 122_I" in the layer. Kim, 12:61-13:11. This doped region will eventually correspond to the contact pads. Another "buried insulating layer 125" is applied over the staircase structure. *Id.*, 13:15-20. Then, sacrificial layers and the doped region are etched away to form openings, including an "opening 122_O" that will correspond to the pads. *Id.*, 13:51-14:17. The openings are then filled with conductive material. *Id.*, Figs. 13, 16, 17. The layer 122 remains behind in Kim's final device. *See, e.g., id.*, Fig. 17.

177. Put another way, Kim's layer 122 does more than simply cover and protect the staircase's conductive layers. Instead, it is used during the formation of Kim's contact pads, is part of what defines the pads' structure, and is thus part of Kim's stacked staircase structure.

178. Because the layer 122, along with layer 110, is used to define Kim's stacked structure, and because layers 110 and 122 are formed from the same material such that they "form one structure" as Kim itself states, in my opinion a POSITA would have understood that they together form an ***"insulating layer."***

179. While I recognize that Kim labels the layers 110 and 122 with separate item numbers, as I have explained the '666 patent states that the term "layer" is

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meant to embrace insulating layers formed from multiple components. *See* Ex. 1001, 4:36-56 (explaining that a "layer" can be "inhomogeneous" and formed from "multiple" layers).

180. Moreover, the '666 patent also explains that a "layer" can be the material "located between any set of horizontal planes." *Id.*, 4:45-48.

181. This is what Kim teaches: insulating layer 110 and the adjacent portion of auxiliary insulating layer 122 are located between the planes formed by the bottom of one gate electrode 300 and the top of another, adjacent gate electrode 300. *See, e.g.,* Kim, Fig. 4B.

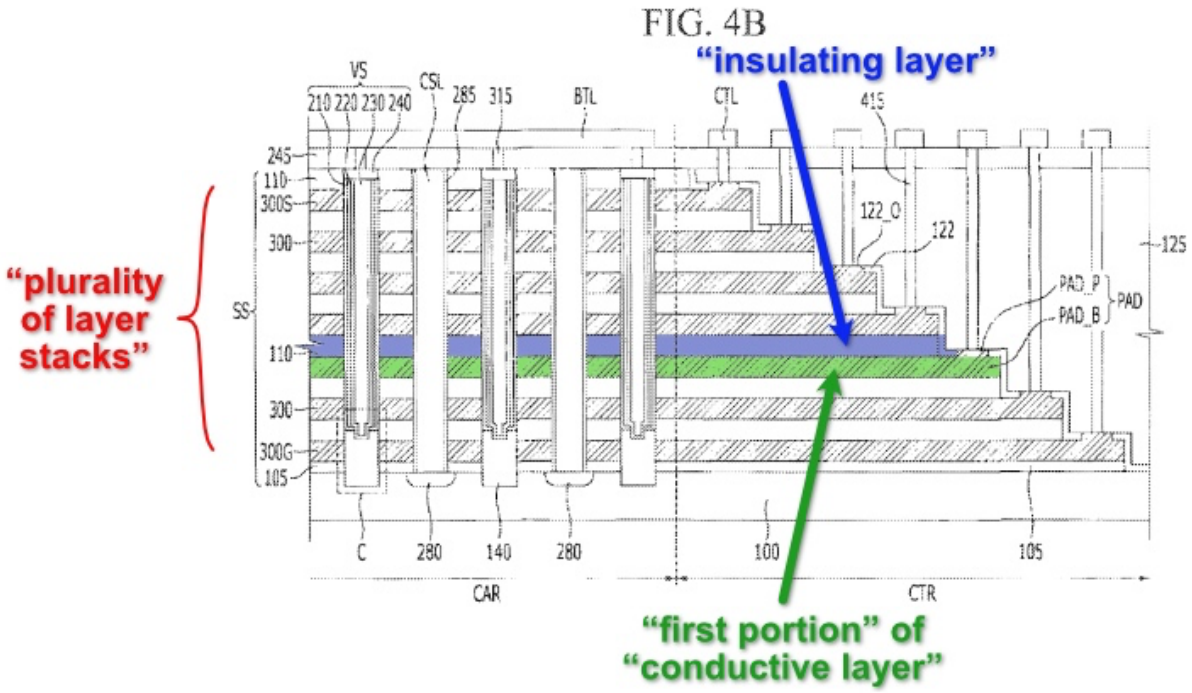
182. An example ***"layer stack"*** including an ***"insulating layer"*** (the combination of Kim's insulating layer 110 and auxiliary insulating layer 122) and ***"conductive layer"*** (the gate electrode 300) are shown in the below annotated version of Figure 4B.

183. Both layers are part of a ***"plurality of layer stacks"*** (Kim's stacking structure SS).

184. Further, as shown, the ***"insulating layer"*** is ***"disposed over a first portion"*** of the depicted ***"conductive layer."***

185. This is repeated throughout Kim's device. In each layer of its stacking structure from the top to the bottom, an insulating layer 110 (and auxiliary insulating layer 122) is located over a gate electrode 300:

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Kim, Fig. 4B (annotated).

[17.C.2] "wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer."

186. In my opinion, Kim, in view of the knowledge of a POSITA, renders this limitation obvious.

187. As I have explained, Kim's "stacking structure SS" includes alternating "insulating layers 110 and … gate electrodes 300[.]" Kim, 5:53-55.

188. "An end of" each "gate electrode 300" is "exposed through the stepwise structure" and includes a "pad unit PAD" formed from "a base pad PAD_B and a protrusion pad PAD_P…." Kim, 7:58-62.

189. "The base pad PAD_B may be a part of the gate electrode 300 in the contact region CTR." Kim, 7:63-64. "The protrusion pad PAD_P may contact

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the … uppermost surface of the base pad PAD_B." *Id.*, 8:3-10; *see also id.*, 7:61-62 (noting that the "protrusion pad PAD_P contact[s] a surface of the base pad PAD_B"); 10:23-25 (similarly referencing location of "the protrusion pad PAD_P" on a "surface of the base pad PAD_B").

190. The pad units PAD "electrically and physically connect" the gate electrodes 300 to a "connection line CTL" via a "word line contact plug 415." Kim, 9:64-67.

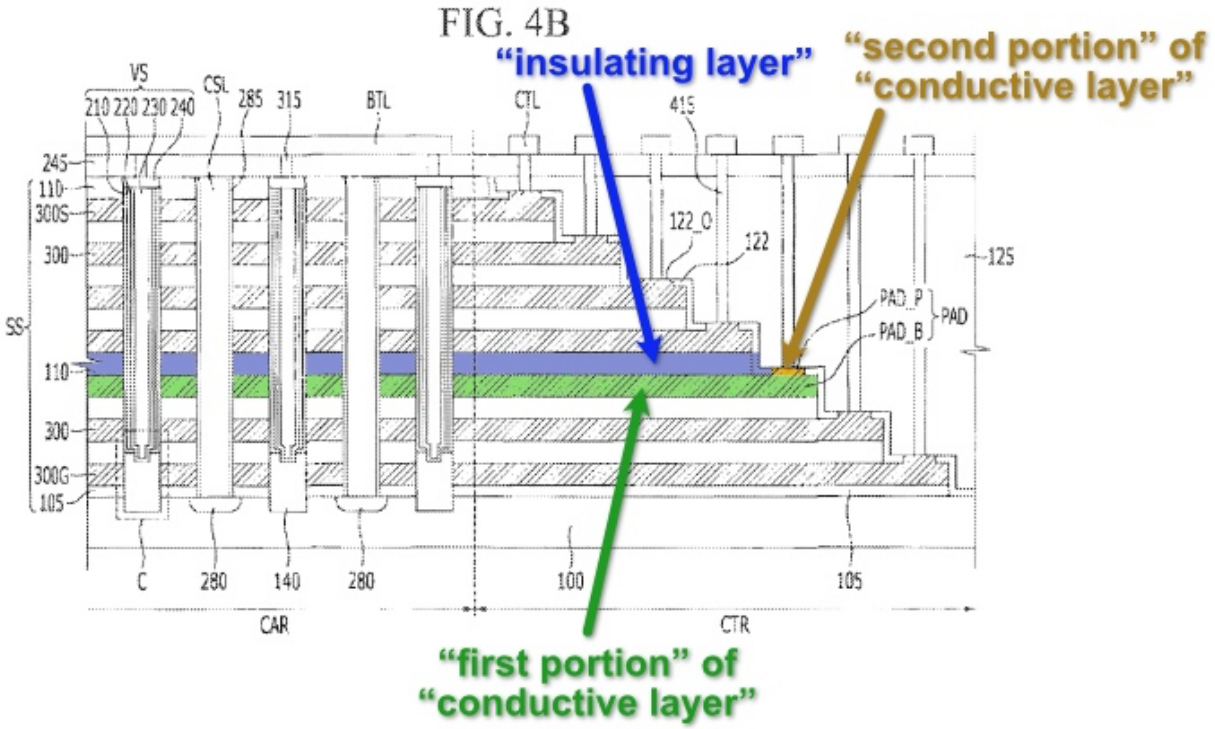
191. The "gate electrode 300" and the attached "base pad PAD_B and … protrusion PAD_P" may be formed from the same "common material composition" such as a "metal." Kim, 6:31-35, 14:12-17.

192. Put another way, each PAD on the end of Kim's gate electrodes is made from metal and allows for electrical interconnection between the gate electrode and an associated word line (or connection line CTL) via a contact plug that contacts the protrusion pad PAD_P.

193. This structure is shown in Figure 4B from Kim below. As shown by the annotations Kim's device includes both a ***"conductive layer"*** (one such layer is annotated green) with both a ***"first portion"*** (gate electrode 300 and attached base pad PAD_B, again green) and ***"second portion"*** (protrusion pad PAD_P, annotated in orange and brown). The overlying insulation layer 110 that—along with the

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annotated conductive layer—makes up one of Kim's staircase layers has again been annotated blue:



Kim, Fig. 4B (annotated).

194. Next, in my opinion, the components of Kim's device are also in ***"contact"*** as this limitation requires.

195. As I have explained, Kim's stacking structure includes "insulating layers 110" and "auxiliary insulating layers 122" made from the same material such that they "form one structure." Kim, 9:29-38. Further, in Kim, the insulation layers 110 and auxiliary insulation layers 122 are formed sequentially before the protrusion pads. *See, e.g., id.*, 12:34-37; Fig. 11. Then, the layer 122 is used to shape the pads. *See id.*, 12:61-13:11.

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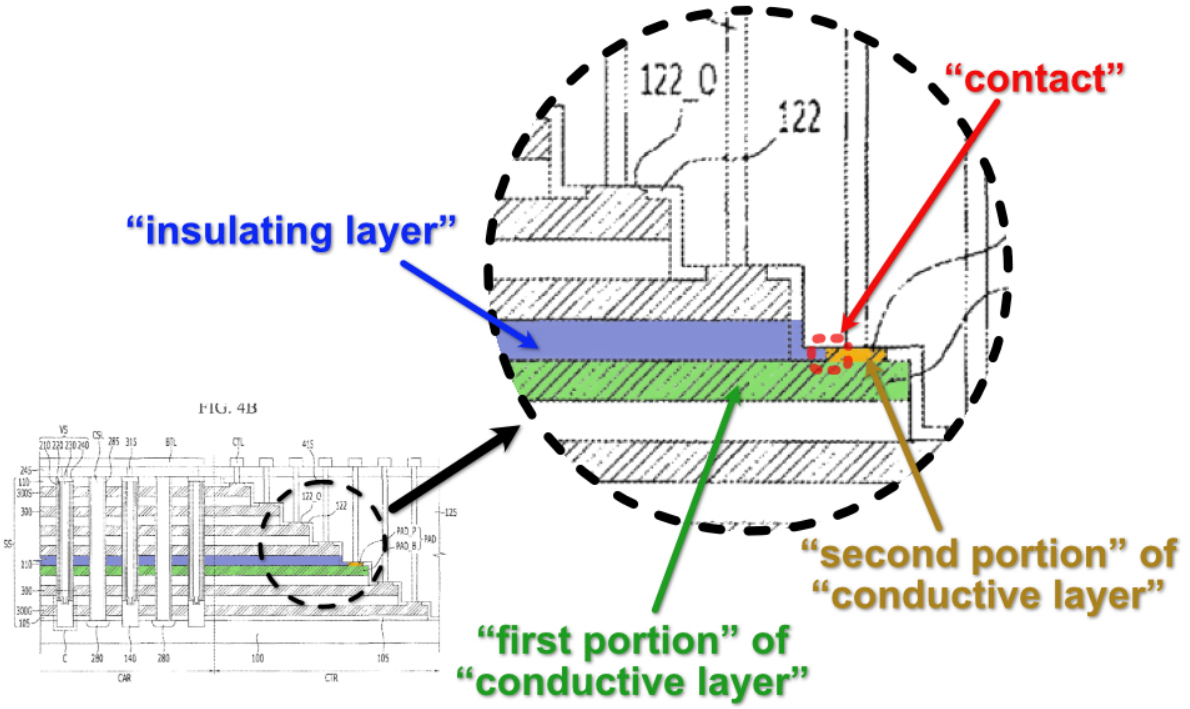
196. In my opinion, and as I explained in greater detail above when discussing limitation [17.C.1], layers 110 and 122 together correspond to the claimed ***"insulating layer."***

197. Kim also explains that "auxiliary insulating layer 122" has an "opening 122_O and the protrusion pad PAD_P" is located "inside" this "opening 122_O." Kim, 9:21-23.

198. This opening 122_O is filled with conductive material to form PAD_P during gate electrode forming process. Kim, 13:51-14:17, Figs. 16-17.

199. Figure 4B is reproduced below. The portion of this figure showing one of Kim's protrusion pads PAD_P is expanded to right. As shown, because Kim's protrusion pad PAD_P is located within and fills the opening 122_O in its auxiliary insulation layer 122, there is ***"contact"*** between a ***"side surface"*** of Kim's ***"second portion"*** (the protrusion pad PAD_P, annotated orange and brown) and a ***"side surface of the insulating layer"*** (the side walls of opening 122_O in auxiliary insulating layer 122, annotated blue):

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Kim, Fig. 4B (annotated).

200. Finally, in my opinion, Kim also teaches that the ***"side surface"*** of its ***"second portion of the conductive layer"*** that is in ***"contact"*** with its ***"insulating layer"*** is (or at the very least obviously can be) ***"curved."***

201. Kim explains that while its figures show "[e]mbodiments … in which the protrusion pad PAD_P has a rectangular parallel[] shape[,]" "the protrusion pad PAD_P is not limited thereto and … may have a shape including a curved surface based on a virtual rectangular parallel[] shape, a cylindrical shape, or any shape." Kim, 8:29-34. A POSITA would have recognized that this includes configurations where the sides of the protrusion pads are curved, particularly to optimize electrical

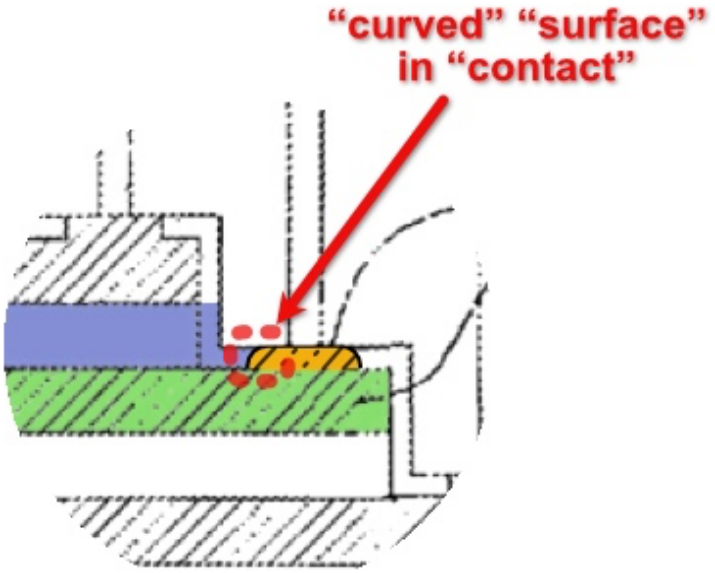
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connectivity and mitigate stress at material interfaces. Such curved configurations are routine in the fabrication of three-dimensional memory devices, as further supported by references like Park, Yun, and Nam.

202. In my opinion, a POSITA would have understood that this teaches a variety of different protrusion pad PAD_P shapes, many of which have the type of ***"curved"*** side surface Claim 17 requires. This includes, for instance, pads with curved sides when viewed in cross-section or pads with curved sides when viewed above.

203. More particularly, a POSITA would have understood that when Kim references a "curved surface based on a virtual rectangular parallel[] shape," PAD_P would obviously be shaped in the manner shown in the demonstrative below. This demonstrative was created using an expanded version of Figure 4B. The rectangular pad shown by that figure has been replaced with a pad with curved sides following Kim's teachings:

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As shown in the demonstrative, the pad continues to have a generally rectangular shape. It also continues to sit on top of Kim's gate electrode layer. Moreover, it continues to be located in the opening in auxiliary insulation layer 122. But now, the pad's sides are "curved" in the area where they contact auxiliary insulation layer 122. *See* Kim, 8:29-34 (explaining that the protrusion pad can have a "curved" surface).

204. In my opinion, not only does Kim itself explain that its pad can have a "curved surface," but contact pads with this type of "curved" side surfaces were well-known in the art at the time the '666 patent was filed. Example references showing this include (1) Park (Ex. 1008), (2) Yun (Ex. 1018), and (e) Nam (Ex. 1006). Each of these will be discussed in greater detail below.

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205. Park (Ex. 1008) teaches a "vertical semiconductor device" with an array of "stacked" "memory cells." Park, 1:14-16.

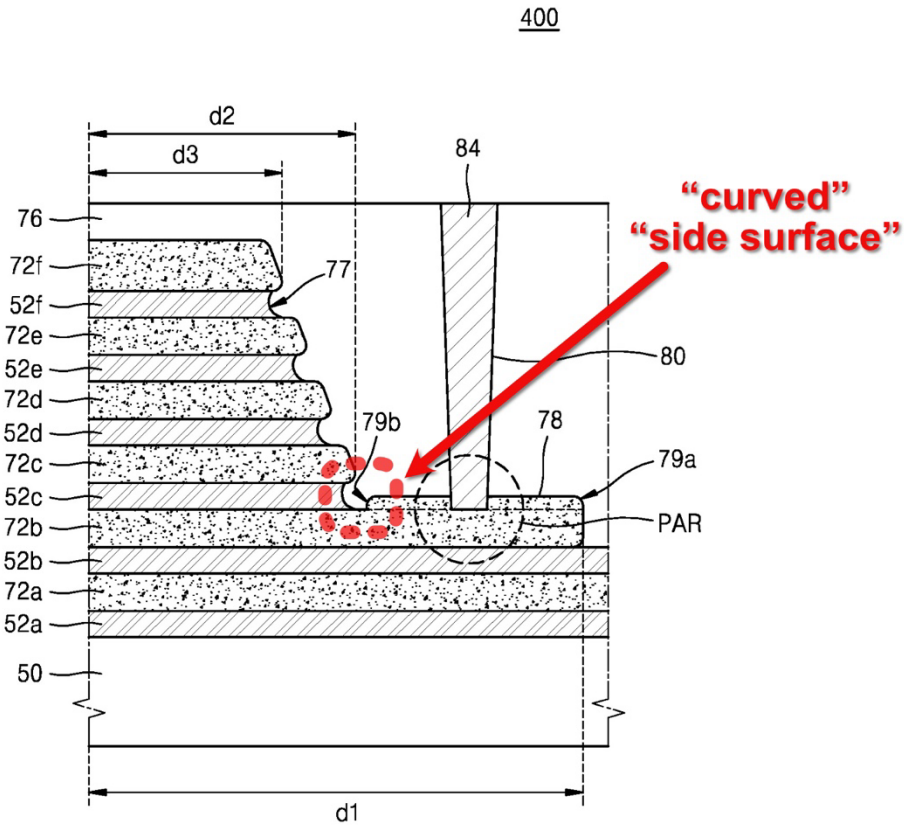
206. Park's device—like Kim's and most references teaching three-dimensional memory—includes a stepped "connection region" with "pad region[s] PAR" located on the end of gate electrodes. Park, 6:7-12, 6:36-47.

207. Each "pad region PAR" includes a "raised pad portion 28." Park, 7:4-16.

208. Per Park, the "end 79b" of the "raised pad portion 78" may be "rounded" to "prevent a short circuit" between the pad and an "adjacent … conductive layer pattern 72c." Park, 11:35-41. An example pad with a rounded end is shown in Figure 7 from Park, which is reproduced below:

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FIG. 7



Id., Fig. 7 (annotated).

209. Yun (Ex. 1018) also relates to a "semiconductor device[] having three-dimensionally arranged memory cells…" Ex. 1018, 1:33-35.

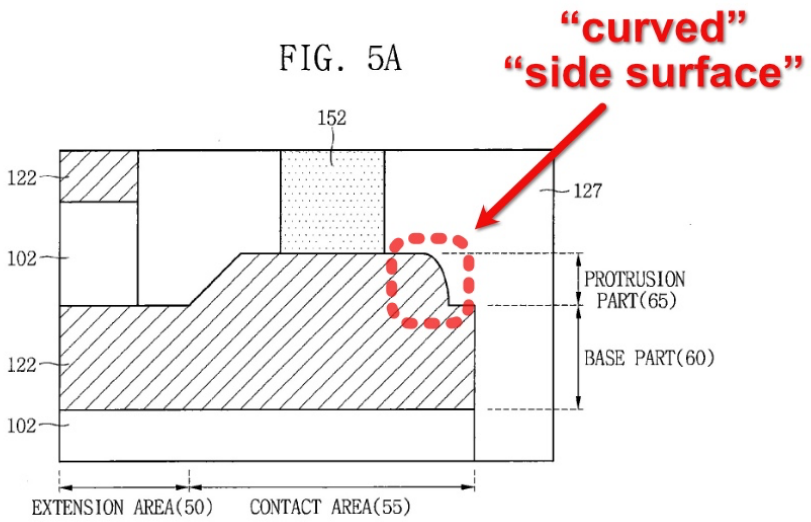
210. Yun explains that the device, once again like most three-dimensional memory devices, has a "stepped" or "cascade structure." Ex. 1018, 9:22-25.

211. The steps hold "contact area[s] 55" that are "co-planar with" the device's "gate electrodes" and have both a "base part 60 and a protrusion part 65." Ex. 1018, 8:15-28.

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212. Per Yun, the "protrusion part 65" may have either "inclined" or "rounded" "side surface[s]." Ex. 1018, 8:33-40.

213. An example of this is shown in Figure 5A of Yun which is reproduced below. The "rounded" surface is shown on the right side of the contact pad:



Ex. 1018, Fig. 5A (annotated).

214. Nam (Ex. 1006) provides another example.

215. Nam—like the Kim, Park, and Yun references I have discussed above—teaches a "semiconductor device" formed from memory cell strings arranged in a three-dimensional array. *See* Nam, ¶¶ [0005], [0025], [0033]; Fig. 2.

216. Gate electrodes connecting to the memory cells may "have a stepped shape having step structures." Nam, ¶ [0043]. Layers of insulation are located between the gate electrodes. *Id.*, ¶ [0043].

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217. Nam explains that each gate electrode includes a "pad region" at its end where "the gate electrode … is connected to a contact 187." Nam, ¶ [0057].

218. As shown below in Figure 8A from Nam, the "pad region" at the end of each gate electrode can have a "bull nose" or "convex" shape. Nam, ¶ [0066].

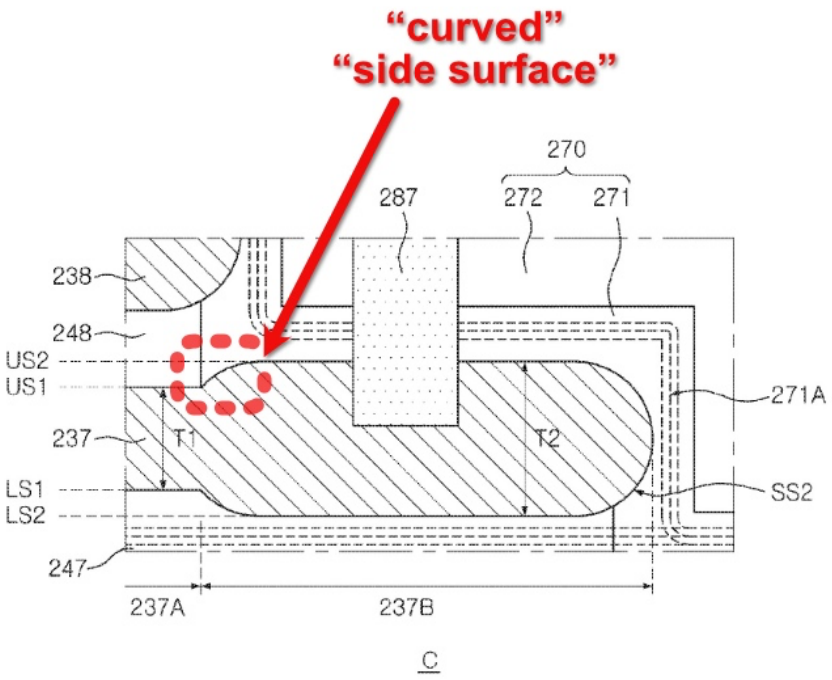


FIG. 8A

Id., Fig. 8A (annotated).

219. In my opinion, a POSITA would have been motivated to employ a contact pad with curved side surfaces when implementing Kim.

220. As I have explained, Kim itself already contemplates that its pad can have a "curved surface." Kim, 8:29-34.

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221. Moreover, this type of pad was also well known in the art as shown, not only by Kim, but also by Park, Yun, and Nam. *See, e.g.,* Park, Fig. 7; Yun, Fig. 5A; Nam, Fig. 8A.

222. Because Kim itself identifies contact pads with curved surfaces as acceptable for use with its device, and because contact pads with this shape were well-known in the art, contact pads with curved side surfaces would have been among the available design choices a POSITA would have considered for use when implementing Kim. Employing this shape would have been considered a highly obvious and routine design choice.

223. Additionally, a POSITA would have recognized that using a "curved" side surface with Kim's pads would have improved Kim by increasing the minimum distance between the pad and adjacent conductive layers, thereby reducing the risk of short circuit.

224. Again, Park explains that "rounded" pad side surfaces helps "prevent a short circuit" between the pad and an "adjacent … conductive layer pattern." Park, 11:35-41. A POSITA would have recognized that forming Kim's pads with straight (or square) sides would have increased the possibility of short circuit with adjacent conductive layers. While also problem for equally sized pads like those shown in Figure 4B, this would have been particularly the case when Kim's pads are made with larger widths causing the pad to occupy a larger percentage of the exposed

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portion of each step in its staircase structure. *See, e.g.,* Kim, 11:57-67 (explaining that certain pads can have a "larger … width"); Fig. 9 (showing larger protrusion pad portions near the top of Kim's stacking structure).

225. In my opinion, the decreased risk of short circuit resulting from the use of rounded pads would have provided a strong motivation to use such a pad with Kim.

226. A POSITA would also have had every reason to believe that a curved pad could be successfully used with Kim.

227. Again, as I have explained, this is one of the shapes that Kim already contemplates and deems acceptable. *See* Kim, 8:29-34.

228. Further, as I have also explained, contact pads with curved side surfaces had also been successfully used in other semiconductor memory devices with stepped structures. *See, e.g.,* Park, Fig. 8; Yun (Ex. 1018), Fig. 5A.

229. Given both the fact that Kim identifies curved pads as acceptable and others similarly taught that pads of this shape can (and had) been used with three-dimensional memory devices, a POSITA would have had every reason to believe that Kim's device would also be able to successfully employ pads of this shape. Furthermore, a POSITA would have found Park's approach for forming such a pad to be highly applicable because it does not introduce new steps but instead optimizes

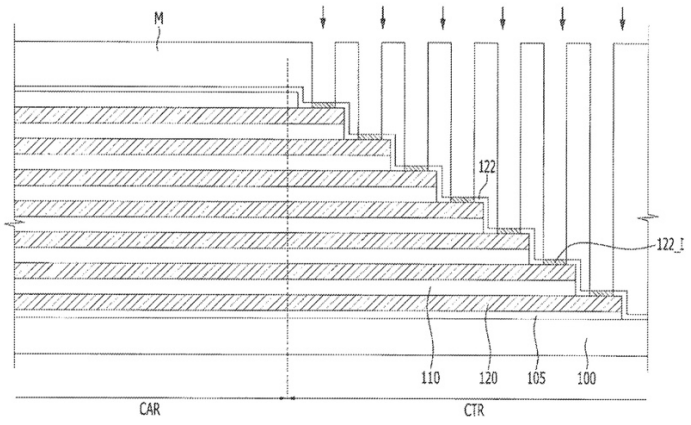
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an existing manufacturing process to achieve improved reliability and performance in Kim's three-dimensional memory devices.

230. Moreover, Kim explains that the opening in auxiliary insulation layer 122 that will eventually contain its protrusion pad PAD_P obtains its shape via an "ion injection process." Kim, 13:1-11.

231. More particularly, in Kim, ion injection is used to form an appropriately shaped "doped region 122_I" in auxiliary insulating layer 122. *See* Kim, 13:1-11. This is shown in Figure 12 below:

FIG. 12

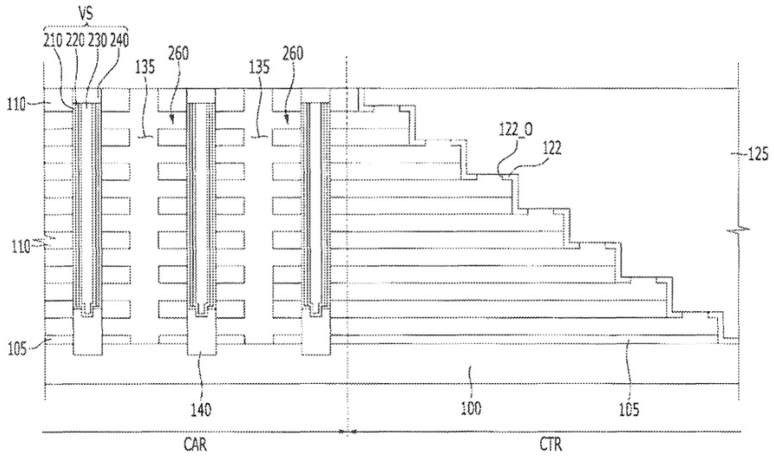


Kim, Fig. 12.

232. This doped region is then etched away to form "opening 122_O" "simultaneously with the process of removing the sacrificial layer 120" which forms "gaps 260." Kim, 13:55-14:8. The formed openings are shown in Figure 16 of Kim:

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FIG. 16



Id., Fig. 16.

233. Then both the gaps 260 and openings 122_O are filled with conductive material to form the gate electrodes and pads. *See id.*, 14:9-17; *see also* Figs. 12-16.

234. In my opinion, a POSITA would have recognized that this process could be readily adapted to form a curved opening that surrounds a curved contact pad. In particular, the ion implantation step shown in Figure 12 of Kim would simply be tailored to form a "doped region 122_I" with curved rather than straight sides. The rest of the process would proceed in the same way, resulting on contact pads located within an opening 122_O in insulation layer 122 with curved sides.

235. Showing this, numerous prior art references similarly employ ion implantation to form contact pads with rounded or curved sides using a process that is analogous to that in Kim.

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236. For example, Park details how "oxidation" and "ion implantation" is used form a "raised pad portion" with "rounded" sides. *See, e.g.,* Park, 7:17-29. In particular, "an additional sacrificial layer 44" with the desired rounded shape is formed by both an "oxidation process" and "ion implanting impurities 42 into" an "additional insulating layer 40." *Id.*, 8:33-49. Implanting the impurities creases a region "having a higher etching rate than" the surrounding "additional insulating layer 40" allowing this region to be removed and later replaced with a properly shaped conductive contact pad. *Id.*, 8:49-51, 9:3-11; Figs. 6D-6F.

237. Nam similarly discusses and depicts the use of "an ion implantation process" to form a "convex" contact pad. Nam, ¶¶ [0066], [0098]-[0107]; Figs. 30-39. In Nam, an "ion implantation process" is employed to form an appropriately shaped "damage region DA1" within insulating layers 272 surrounding sacrificial layers 220. *Id.*, ¶¶ [0099]-[0100]. The shape of the eventual contact pad can be controlled via the use of multiple ion-injection steps targeting different areas. *See, e.g., id.*, ¶¶ [0060], [0066], [0073]; Figs. 22, 32-34. The damaged regions have a "relatively rapid etching rate" resulting in the formation of an opening in the surrounding insulation corresponding to the contact pad. *Id.*, ¶¶ [0103]-[0104]. This opening is then replaced with conductive material. *Id.*, ¶¶ [0106]-[0107].

238. Again, a POSITA would have understood that ion implantation would similarly be employed to form a "doped region 122_I" in Kim's auxiliary insulation

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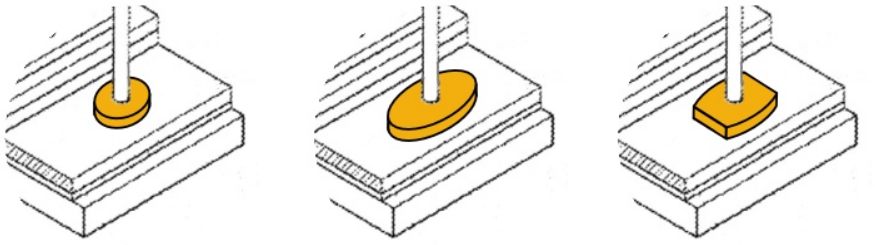
layer 122 with a rounded as opposed to rectangular shape. When this region is then etched to form an opening 122_O and replaced with conductive material as Kim teaches, a contact pad with rounded sides (that continue to be surrounded by and in contact with insulation) results. Alternatively, an opening with straight sides formed by etching could be subjected to a further oxidation step like that taught by Park to achieve the desired rounding. The amount of rounding would be controlled by adjusting the time of application of the oxidant to the opening (the oxidant will remove exposed corners first, producing the desired rounding before it meaningfully impacts the other surfaces within the opening).

239. Next, in my opinion, a POSITA would have understood that Kim's "cylindrical[ly]"-shaped protrusion pads PAD_P also include the type of ***"curved"*** surface that Claim 17 requires.

240. A POSITA would have understood that a "cylindrical" contact pad can be implemented as, for instance, a right cylinder, an elliptical cylinder, or even a generally rectangular pad with two sides that follow a cylindrical pattern. While all these types of pad shapes include "curved" side surfaces, a POSITA would have understood that a generally rectangular pad with two flat sides and two sides following a cylindrical pattern is yet another way a POSITA would have considered implementing Kim's teaching that its pad can have a "curved surface based on a virtual rectangular parallel[] shape…." Kim, 8:29-34.

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241. Examples of how a POSITA would have understood these pads to be shaped are shown in the demonstrative images below. Note that Kim does not include any figures showing "cylindrical" contact pads. Nonetheless, it does reference this type of pad. The below examples of what a POSITA would have understood Kim to mean when it references a "cylindrical" pad were generated using the three-dimensional view of Figure 6 as a starting point. Figure 6 shows rectangular pads. The rectangular pads in that figure have been replaced with (1) a right cylinder (left-most demonstrative), (2) elliptical cylinder (central figure), and (3) rectangular pad with two straight sides and two sides following an elliptical cylindrical shape:



242. In my opinion, employing any of these "cylindrical" contact pads also results in the claimed ***"conductive layer" "second portion"*** having a ***"curved" "side surface"*** that is in ***"contact"*** with the side surface of Kim's ***insulating layer."***

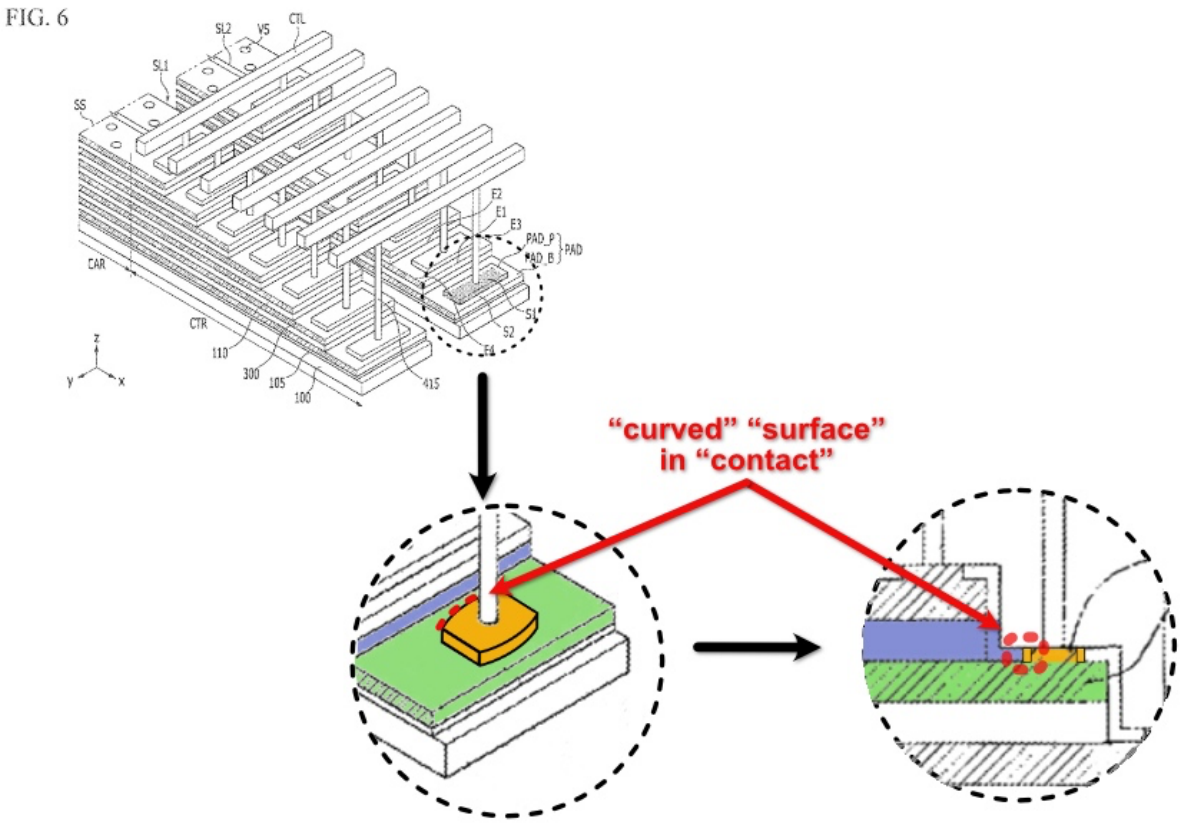
243. This is shown in the demonstrative below generated using Figure 6 of Kim. Again, in Figure 6, the contact pads are shown to be rectangular. In the demonstrative below, there is an expanded view—the bottom left of the

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demonstrative—of one such rectangular pad replaced with a pad that has two straight surfaces and two curved sides that follow a cylindrical shape (design option (3) discussed above). The bottom right of the demonstrative is meant to show a cross-sectional view. Because the pad has a generally cylindrical shape, the "curved" sides will only appear "curved" when viewed from above. When viewed in cross-section, the sides appear straight.

244. While auxiliary insulation layer 122 is not shown in the three-dimensional view of Figure 6, a side view has been added to the demonstrative below to show how the pad, even though now shaped with curved sides following the general shape of a cylinder, will continue to be formed and located within the opening through and will contact the side of auxiliary insulation layer 122. Because the cylindrical pad is formed within the opening in insulation layer 122, its sides contact that insulation layer:

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245. In my opinion, a POSITA also would have been motivated to employ this shape and would have expected to succeed when doing so.

246. As I have explained, Kim itself identifies "cylindrical"-shaped contact pads as acceptable and contemplates their use.

247. Because of this, a POSITA would have considered use of cylindrical pads to be nothing more than a minor variation in design from the rectangular pads shown in Kim's figures. Use of this shape pad—as opposed to any of the others taught by Kim—would have been a simple, straightforward design choice.

248. Further, a POSITA would have recognized that a cylindrical pad could be made following the same process and same steps Kim employs to make its

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rectangular pad (just with differently shaped mask patterns during the ion implantation process shown in Figure 12 to produce a cylindrical rather than rectangular pad). Thus, a POSITA would have every reason to believe that a cylindrical contact pad would be successfully employed with Kim's device.

2. Claim 19

249. Claim 19 depends on Claim 17 and further requires:

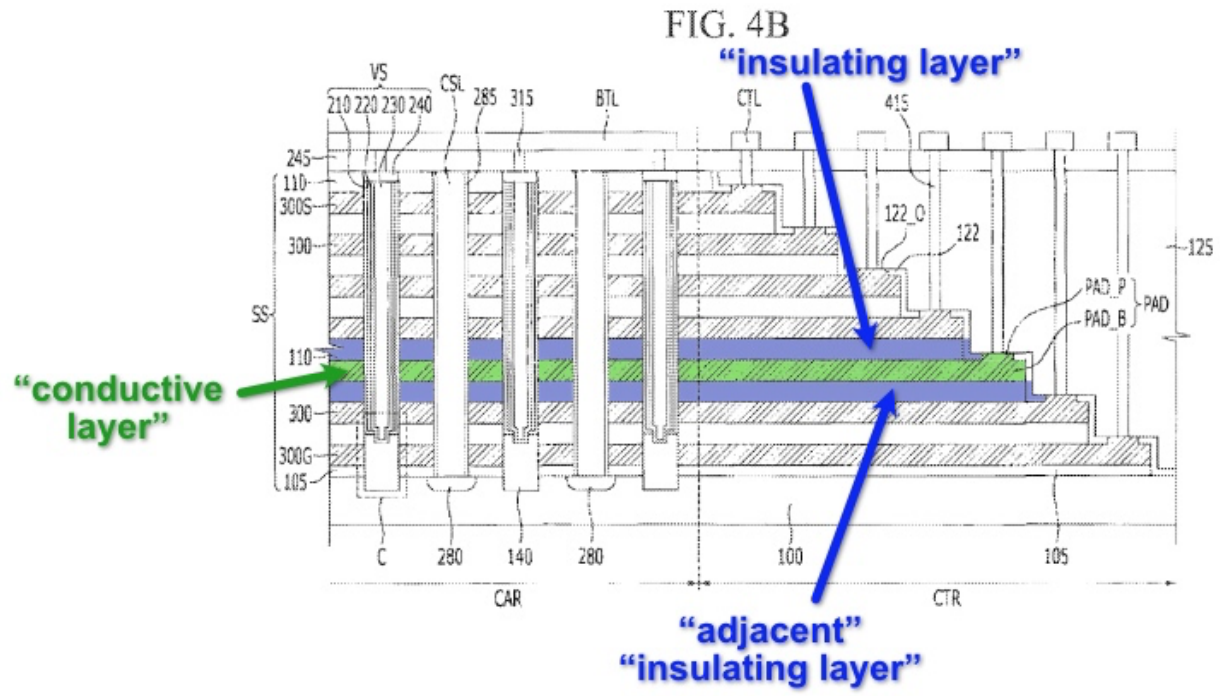
[19] "wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack"

250. In my opinion, this is taught by Kim.

251. Kim's "stacking structure SS" includes a "plurality" of alternating "insulating layers 110 and … gate electrodes 300." Kim, 5:53-55; *see also id.*, 1:41-46 (the "stacking structure" includes "insulating layers" and "gate electrodes" that are "alternatively stacked.")

252. Figure 4B of Kim is reproduced below. As shown, because Kim's stacking structure includes alternating conductive and insulating layers, each of Kim's ***"conductive layer[s]"*** (the gate electrode 300, annotated green) is located both above an insulating layer (insulating layer 110 above the electrode, annotated blue) and over ***"a first portion of the insulating layer of an adjacent layer stack"*** (another insulating layer 110 immediately below the gate electrode, also annotated blue):

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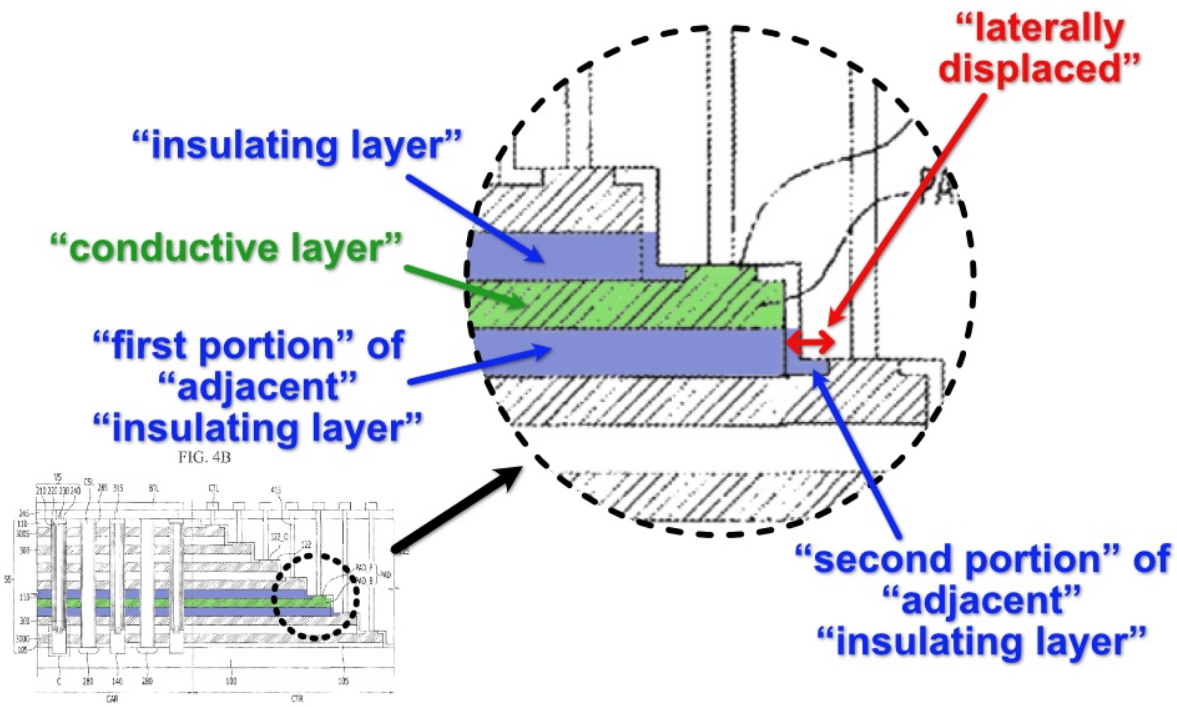


Kim, Fig. 4B (annotated).

253. Further, in Kim, each insulating layer 110 can be integrated with an "auxiliary insulating layer 122" such that layers 110 and 122 form "one structure." Kim, 9:12-13, 9:29-38.

254. Figure 4B is again reproduced below. This time, however, the area around one contact pad has been expanded to the right. As shown below, a ***"second portion of the insulating layer of the adjacent layer stack"*** (the portion of auxiliary insulating layer 122 adjacent to layer 110) is ***"laterally displaced from the conductive layer."*** This is because the insulating layer below the green annotated conductive layer extends out to make contact with the side surface of the protrusion pad of the conductive layer below:

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Kim, Fig. 4B (annotated).

3. Claim 20

255. Claim 20 depends on Claim 17 and further requires that:

[20] "wherein the conductive layer comprises a first conductive material, and wherein the curved side surface comprises a second conductive material."

256. This, in my opinion, is also taught by Kim.

257. Kim explains that its "gate electrode 300"—again this is the claimed ***"conductive layer"***—and the attached "base pad PAD_B and … protrusion PAD_P"—this is the portion of Kim's conductive layer including the claimed ***"curved side surface"***—may be formed from the same "common material composition" such as a "metal." Kim, 6:31-35, 14:12-17. Thus, Kim's ***"conductive***

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layer" and ***"curved side surface"*** are made from ***"a first conductive material"*** (metal) and ***"a second conductive material"*** (also metal).

258. While this claim does reference a "first conductive material" and "second conductive material," per the '666 patent, these materials can be the same and do not need to be different. *See, e.g.,* Ex. 1001, 1:55-59 ("The second material layer is made of a first conductive material. The plurality of landing pads are made of a second conductive material. The first conductive material can be the same or different from the second material.")

C. *Ground 2*: Claims 17, 19, and 20 Are Obvious Over Nam

259. In my opinion, a POSITA would have considered Nam to be within the scope of the prior art and highly relevant to the patentability of the '666 patent's claims.

260. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Nam renders Claims 17, 19, and 20 of the '666 patent obvious.

1. Claim 17

[17.Pre] "A memory device, comprising:"

261. To the extent this preamble language is limiting, in my opinion it is taught by Nam.

262. Nam relates to a "memory device." Nam, ¶ [0002]. Per Nam, its "FIG. 1" shows a "memory device 1" with various components. *Id.*, ¶ [0025]; Fig. 1.

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263. Nam's memory device can be a "NAND flash device" with memory cells arranged in a three-dimensional array. *Id.*, ¶ [0032]; Fig. 2.

[17.A] "a substrate, wherein the substrate comprises a top surface;"

264. In my opinion, Nam teaches a ***"substrate"*** with a ***"top surface."***

265. Nam's "memory device" includes a "substrate 101" with an "upper surface." Nam, ¶ [0038]; *see also id.*, ¶ [0005] (similarly explaining that Nam's "semiconductor device includes … a substrate").

266. According to Nam, the "upper surface of the substrate 101 may correspond to an X-Y plane." Nam, ¶ [0039]; *see also, e.g.,* Fig. 3.

267. Figure 7 from Nam is reproduced below. Nam's ***"substrate"*** is labeled as item 201 and is annotated in yellow. Nam, ¶ [0062]. The ***"top surface"*** of this substrate is shown with red dashed outlining. As shown, the rest of Nam's device is located on top of the substrate's top surface:

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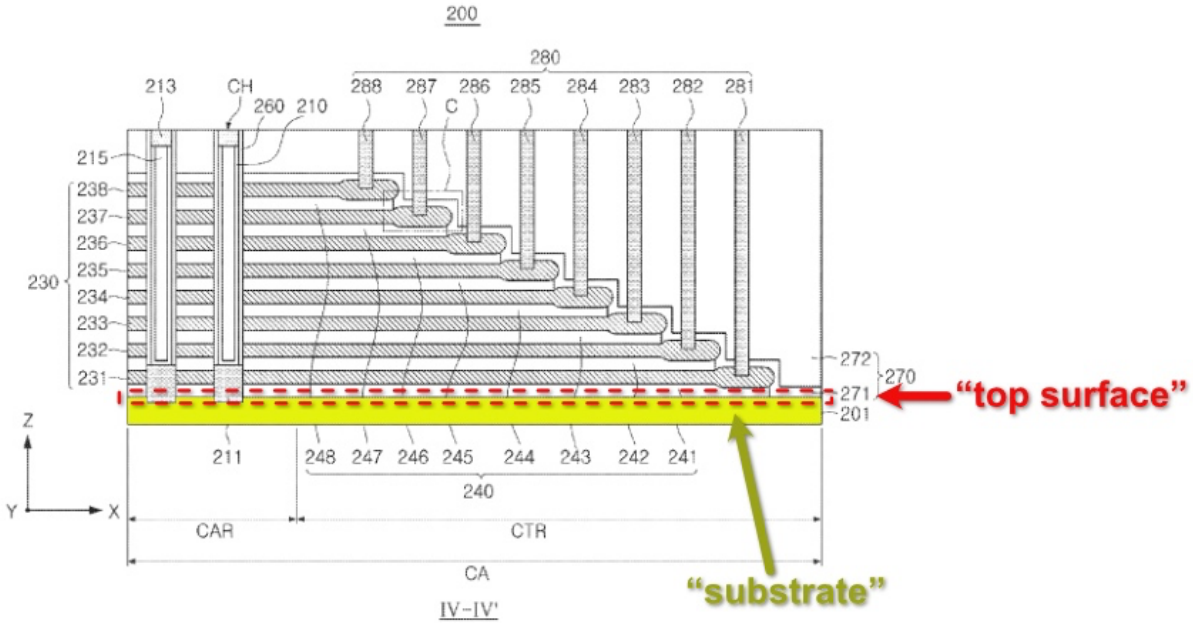


FIG. 7

Id., Fig. 7 (annotated).

[17.B] "a memory string disposed over the substrate; and"

268. In my opinion, Nam includes ***"memory strings"*** that are ***"disposed over"*** its ***"substrate."***

269. Nam's "memory device" includes a "memory cell array" with "a plurality of memory cells arranged in a plurality of rows and a plurality of columns." Nam, ¶¶ [0025]-[0026].

270. The "memory cell array may include a plurality of memory cell strings S[,]" each of which includes a "number of memory cells MC1 to MCn connected to one another in series…." Nam, ¶ [0033].

271. Figure 2, which is reproduced below, provides a basic circuit diagram of Nam's memory cells. As shown, the cells are arranged in a three dimensional

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array along vertical strings. One such memory string S is annotated with red-dashed outlining in Figure 2 below:

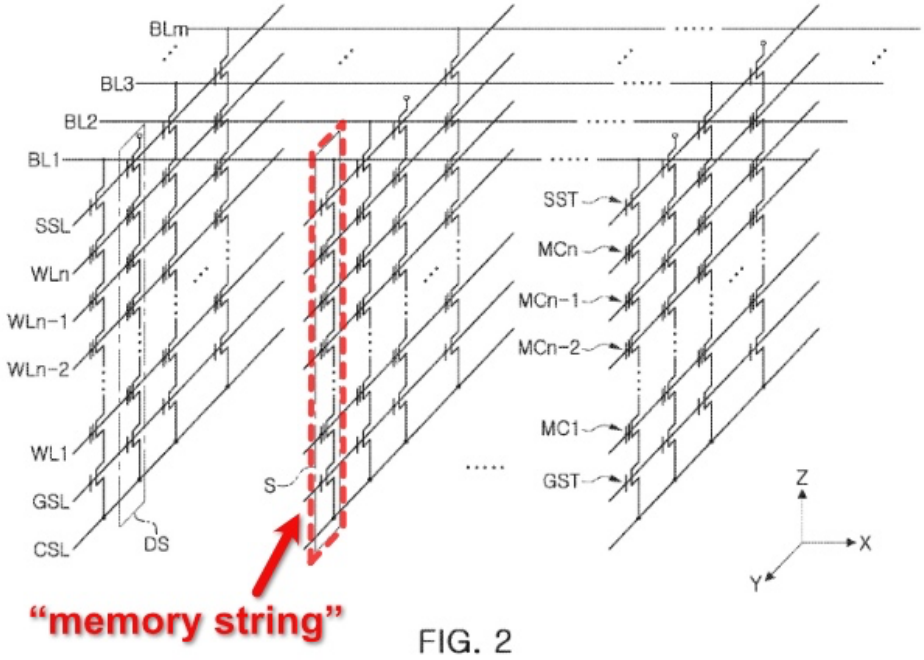


FIG. 2

Nam, Fig. 2 (annotated).

272. Nam also explains that its memory strings are formed along "channel structure[] CH." Nam, ¶ [0038]. According to Nam, this channel structure is located over the "upper surface of [the] substrate…." *Id.*

[17.C] "a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises;"

273. This, in my opinion, is also taught by Nam.

274. Nam's "memory device" includes both a "cell array region CAR" and a "contact region CTR." Nam, ¶¶ [0043], [0062].

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275. The "channel structures CH" forming Nam's memory strings are located in the "cell array region." Nam, ¶ [0062].

276. "[C]ontact region CTR" includes a "plurality of contacts 281 to 288 (contacts 280)" that connect to "gate electrode layers 231 to 238." Nam, ¶ [0063].

277. The gate electrodes "have step structures" or a "stepped shape having step structures" where they are "connected to the contacts 180." Nam, ¶ [0043].

278. Figure 7 of Nam is reproduced below. Two channel regions CH which are in the cell array region CAR and form Nam's ***"memory strings"*** are annotated red. The stepped "contact region CTR," annotated blue, corresponds to the claimed ***"staircase structure"***:

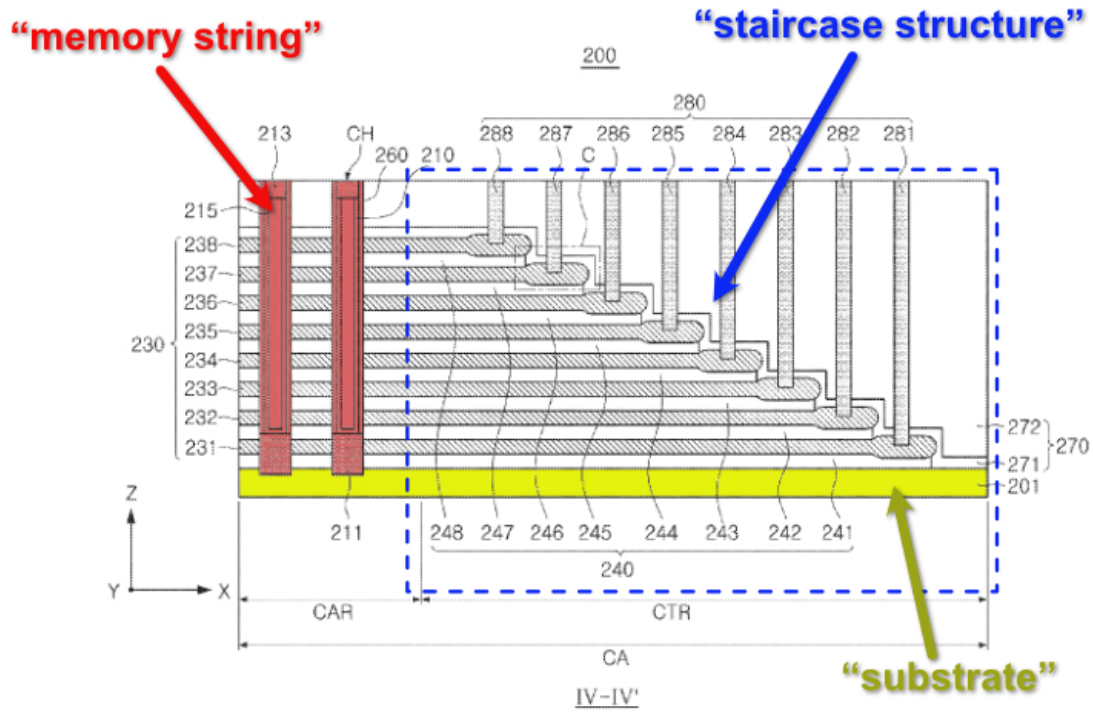


FIG. 7

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Nam, Fig. 7 (annotated).

[17.C.1] "a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer,"

279. In my opinion, Nam teaches the claimed ***"plurality of layer stacks"*** with alternating ***"insulating"*** and ***"conductive" "layer[s]."***

280. Nam explains that its device "includes a stack of alternating first interlayer insulating layers and gate electrode layers on a substrate." Nam, ¶ [0005].

281. For example, in the "memory device 200" of Figure 7, "[a] plurality of gate electrode layers 231 to 238 (gate electrode layers 230)" are alternately arranged such that they "form[] a pair with one of a plurality of insulating layers 241 to 248 (240) adjacent thereto in a stack direction (Z-axis direction)…." Nam, ¶ [0063].

282. The gate electrode layers are formed with a "conductive material" such as "metal." Nam, ¶ [0094].

283. The "insulating layers" may be formed from "silicon oxide." Nam, ¶ [0081].

284. Nam also explains that "[a] first interlayer insulating layer 271" is formed adjacent to insulating layers 240 and surrounds the ends of its gate electrodes. Nam, ¶ [0098]. This layer 271 is made from the same "silicon oxide" material as insulating layers 240. *Id.*

285. A "doped region 271A" is located within layer 271 near the boundary between this layer and a separate "second interlayer insulating layer 272." Nam, ¶

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[0100]; *see also id.*, Figs. 7, 8A. Layer 272 is formed from a different material: TEOS. *Id.*

286. In my opinion, a POSITA would have considered both Nam's insulating layer 240 and the adjacent insulating layer 271 to be the claimed ***"insulating layer."***

287. Again, layers 240 are located between and separate the gate electrode layers 230 forming Nam's stacked staircase. *See* Nam, Fig. 7.

288. A POSITA would also consider layer 271 to be part of the stacked, staircase structure. This layer is applied before Nam's staircase structure is complete. *See, e.g.*, Nam, ¶ [0098]; Fig. 31. Further, layer 271 is used to form the pads at the end of Nam's gate electrode layers: the pads are formed within openings that are defined by ion injection into and then etching of this layer 271. *See id.*, ¶¶ [0099]-[0106]; Figs. 32-34, 36, 39. The layer 271 remains behind in Nam's final product. *See id.*, Fig. 7.

289. Because layer 271 is not only formed from the same material as layer 240, but is used to define the shape of Nam's pads, in my opinion a POSITA would have understood this layer to be part of Nam's ***"insulating layer***" along with insulating layer 240.

290. Moreover, a POSITA would have recognized that insulating layer 271 is distinguishable from other insulating layers—like the field "second interlayer

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insulating layer 272" that is applied over the staircase structure and around the contacts—in Nam. *See* Nam, ¶ [0100]; Fig. 7. Layer 271 is part of the layered staircase structure as it is used to form Nam's contact pads. Layer 272, however, is not part of the staircase structure and is instead just applied as a protective layer over that structure. *See, e.g., id.*, Fig. 7.

291. An annotated version of Figure 7 is reproduced below. In this figure, an example ***"insulating layer"*** (insulating layer 248 and the adjacent portion of layer 271, both annotated blue) and ***"conductive layer"*** (the gate electrode 237, annotated green) are shown.

292. Both layers are part of a ***"plurality of layer stacks"*** (the combination of layers 230 and 240).

293. And the ***"insulating layer"*** is ***"disposed over a first portion"*** of the depicted ***"conductive layer."***

294. Moreover, each of the ***"layer stacks"*** in Nam's device includes insulation (layers 240 and 271) over conductive material (layer 230). And in each layer making up Nam's staircase, there is insulation (either 271 alone, or 271 and 240) over that layer's conductive material (230):

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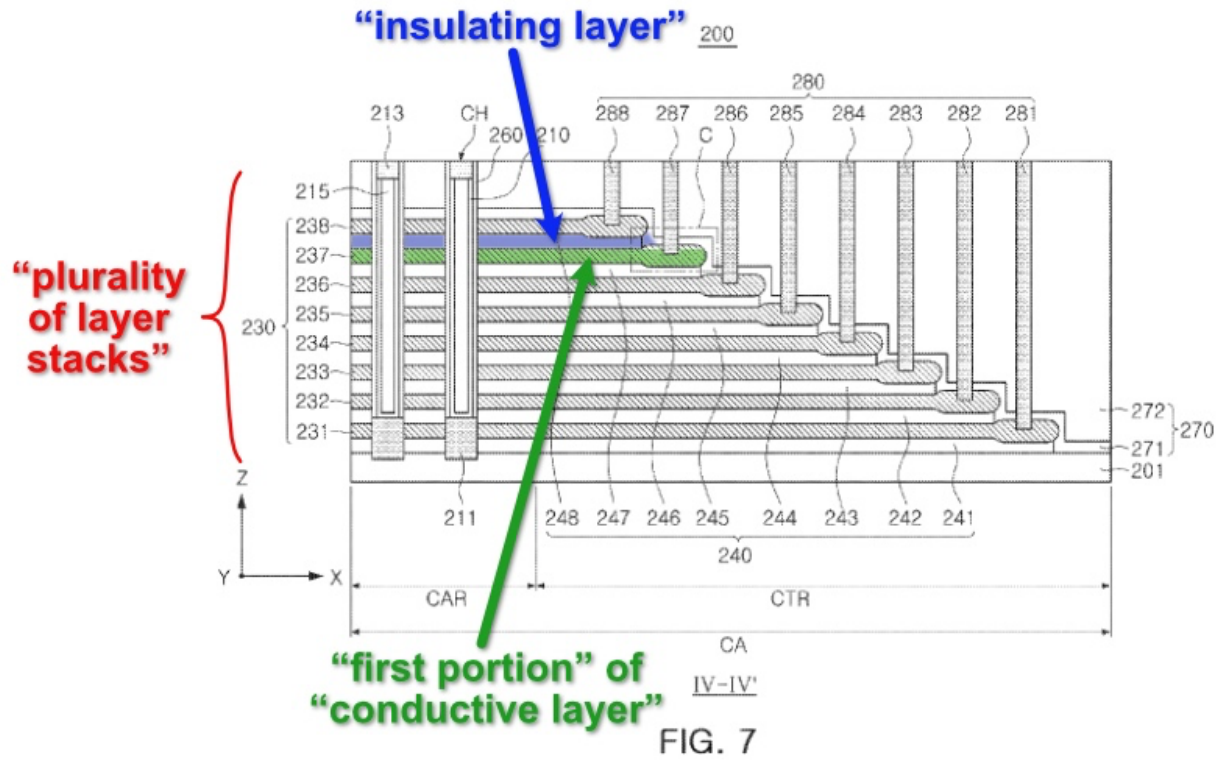


FIG. 7

Nam, Fig. 7 (annotated).

295. These same layers are also shown in Figure 8A, which "is an enlarged view of region C of FIG. 7." Nam, ¶ [0065].

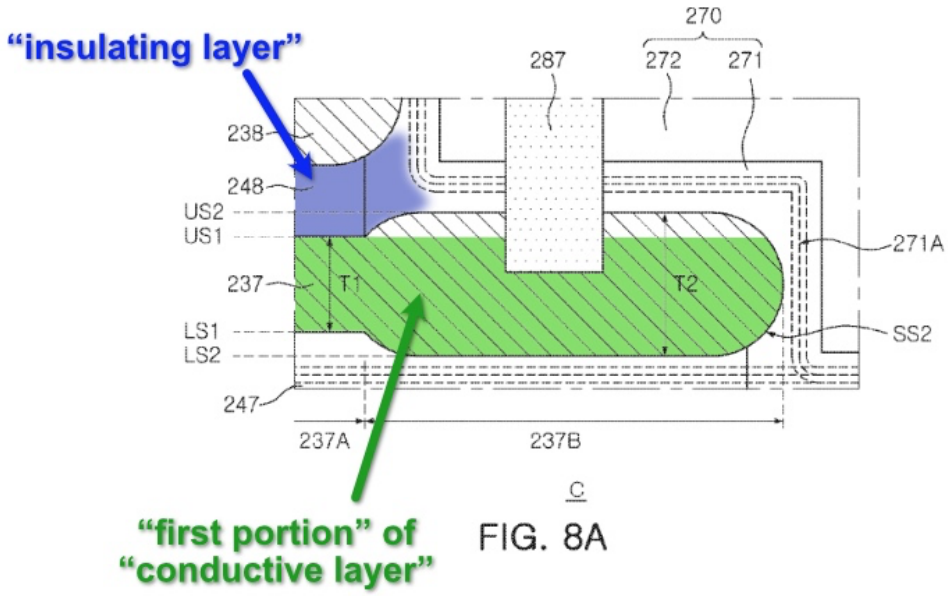


FIG. 8A

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Id., Fig. 8A (annotated).

[17.C.2] "wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer."

296. In my opinion, Nam renders this claim limitation obvious.

297. Nam's "gate electrode layers" include both a "first portion and a second portion." Nam, ¶ [0005].

298. The "second portion forms an end portion" of the "gate electrode layer." Nam, ¶ [0005]. This end portion serves as Nam's contact "pad region." *Id.*, ¶ [0045].

299. According to Nam, the pad has an "increased" "thickness" compared to the rest of the "gate electrode layer[]." Nam, ¶ [0045].

300. Per Nam, making the gate electrode thin with a thick contact pad at its end serves competing goals.

301. By employing thin gate electrodes "increase[s] a capacity of the memory device…." Nam, ¶ [0044]. Device "integration" can be "improved" via an "increased" "number of stacked gate electrode layers." *Id.*, ¶ [0108]; *see also id.*, ¶ [0096]. In other words, thinner gate electrodes allow more gate electrodes (and more memory cell layers) to be located over a substrate surface without excessively increasing the device's height.

302. But Nam explains that thinner gate electrodes create an issue: "a portion of the contacts" (280 in Figure 7) that interconnect the gate electrodes to other

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portions of the memory "may penetrate through the gate electrode layer" and reach adjacent layers resulting in "the occurrence of defects such as short circuits." Nam, ¶¶ [0044], [0064]. According to Nam, making the contact pads on the ends of the electrodes thicker, the problem of potential short circuits "may be mitigated or solved, and the integration and reliability of the memory device 200 may be improved." *Id.*, ¶ [0064]. A contact is less likely to either (1) not fully contact or (2) punch through a thicker pad region.

303. Because Nam's ***"conductive layer"*** (its gate electrode) employs a thicker end, this layer has both a ***"first portion"*** and ***"second portion"*** as Claim 17 requires.

304. Figure 7 of Nam, which is reproduced below, shows this. Nam's ***"first portion"*** is the thinner portion of its gate electrode and the bottom portion of its contact pad (one such electrode 237 is annotated in green below). Nam's "***second portion"*** is the upper, thicker portion located at the end of this same electrode (which is annotated in orange / brown below):

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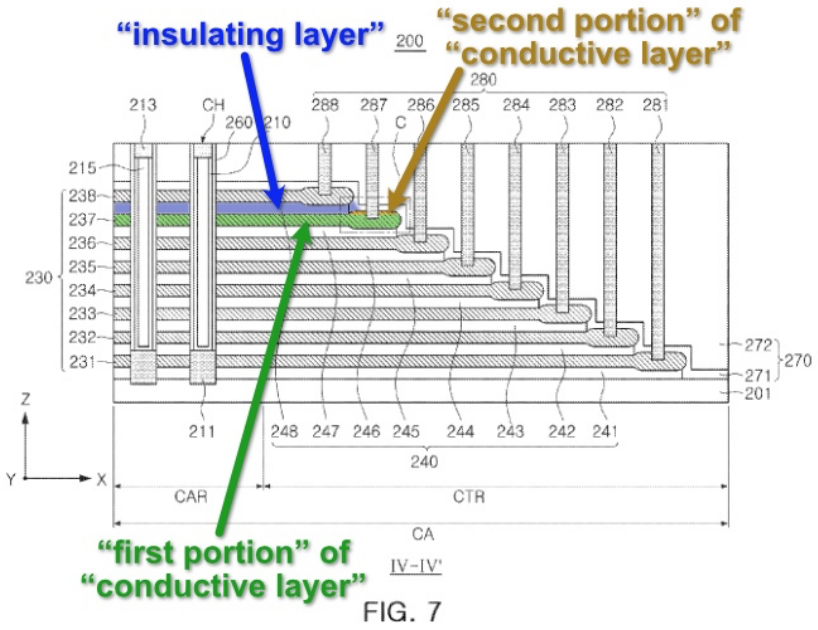


FIG. 7

Nam, Fig. 7 (annotated).

305. This same structure is shown in more detail in Figure 8A. The components discussed above have been annotated using the same colors:

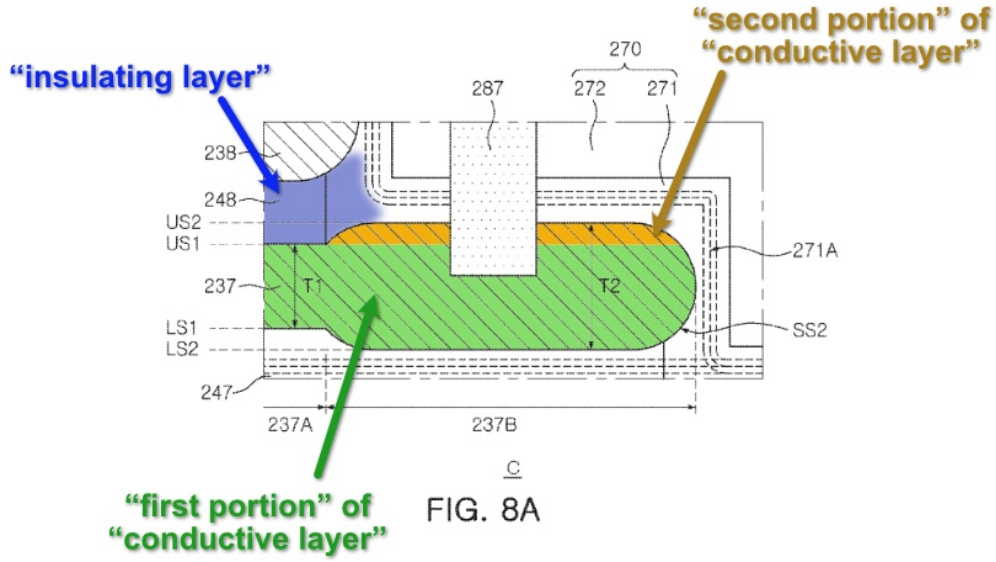


FIG. 8A

Nam, Fig. 8A (annotated).

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306. As shown in Figure 8A, Nam's gate electrode 237 includes a "first region 237A" and "a second region 237B." Nam, ¶ [0065].

307. The "second region 237B" is "provided as a pad region" that has a "thickness T2" that is "greater than a thickness T1 of the first region 237A." Nam, ¶ [0065].

308. Because this pad region has an increased thickness compared to the rest of the gate electrode, its "upper surface US2" is "disposed … higher than an upper surface US1 of the first region of portion 237A." Nam, ¶ [0065].

309. Once again, in my opinion, the thicker portion of the pad between surfaces US1 and US2 and extending out of the top of the rest of the gate electrode is the claimed ***"second portion"*** of Nam's ***"conductive layer."***

310. Nam also explains that its contact pad can also have a variety of shapes.

311. For instance, the pad can be formed with a "concave shape" that is "recessed inwardly." Nam, ¶ [0059]; Fig. 6.

312. Alternatively, the pad can have a "convex" or "bull nose" shape. Nam, ¶ [0066]; Fig. 8A. This feature reduces stress concentration and minimizes the likelihood of short circuits or electrical failures. A POSITA would recognize this as a design optimization routinely applied in stacked memory devices to enhance reliability and compatibility with manufacturing processes.

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313. The pad can also be formed either with a shaped bottom, or a "lower surface" that is "coplanar" with the rest of the gate electrode. Nam, ¶ [0072]; Fig. 10.

314. Figure 8A employs a "convex" shaped pad. As shown, because it employs a "convex" shape, Nam's contact pad includes the "***curved" "side surface"*** Claim 17 requires. For reference, the pad's curved side surface is annotated with red outlining:

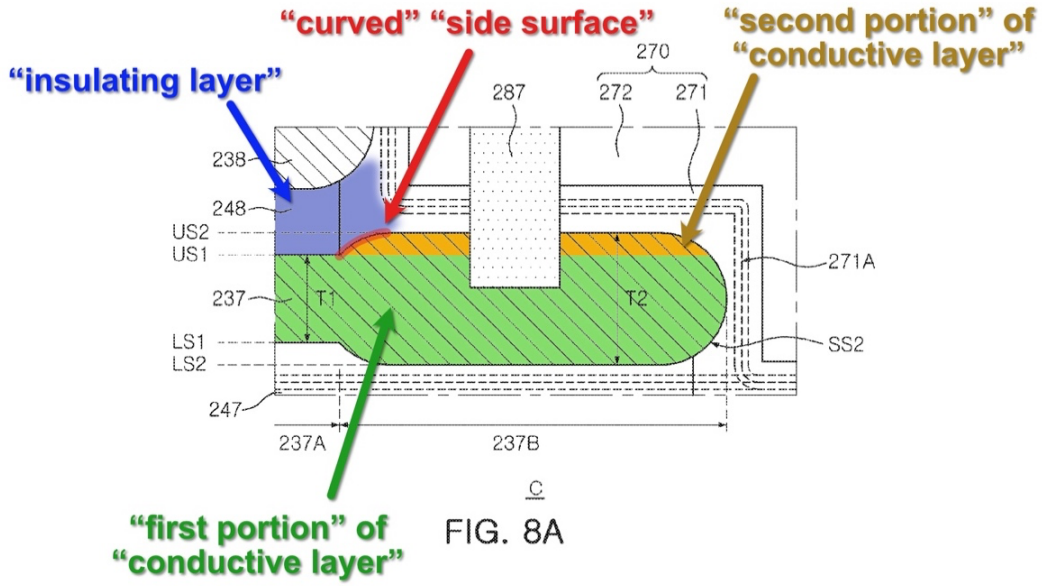


FIG. 8A

Nam, Fig. 8A (annotated).

315. In addition to identifying possible shapes, Nam also discusses the process used to form its gate electrodes and contact pads in detail.

316. To begin this process, Nam forms an alternating stack of sacrificial layers 220 and insulating layers 240. Nam, ¶ [0098]; Figs. 30, 31.

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317. Then, steps are formed in these layers. Nam, ¶ [0098] The steps are then covered with "first interlayer insulating layer 271." *Id.*

318. Next, a multi-step "ion implantation process" is performed to create a "damaged region" "DA1" surrounding the ends of the sacrificial layers 220. Nam, ¶ [0099].

319. This "damaged region" is more susceptible to etching, is located at the "interface" between the sacrificial layer and the "interlayer insulating layers," and has the shape of the intended contact pad. Nam, ¶¶ [0066], [0090], [0103].

320. Figure 34, which is reproduced below, is meant to show the general locations of ion implantation. Per Nam, the implanted impurities can be diffused into the surrounding insulating layer 271 via the application of heat. *See* Nam, ¶ [0090], [0105].

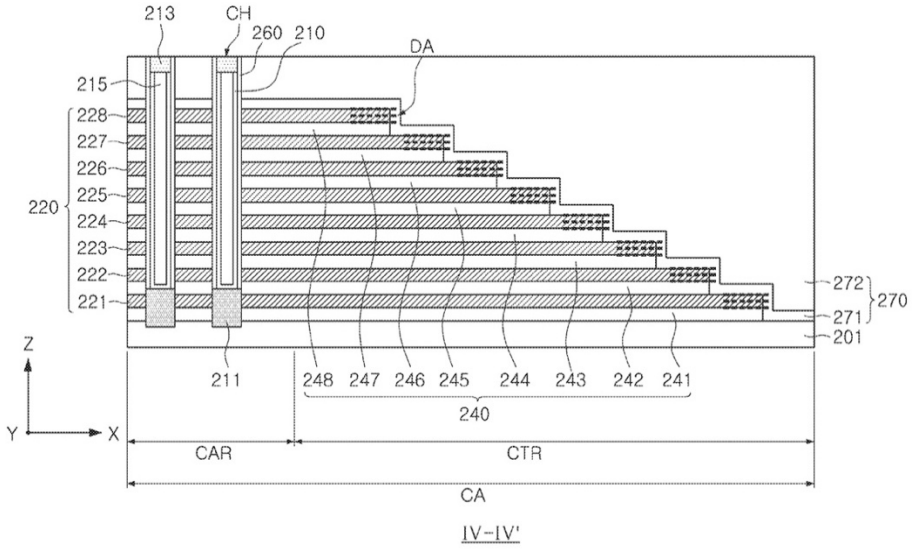


FIG. 34

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Id., Fig. 34.

321. After implantation is complete, a separate "second interlayer insulating layer 272" of "TEOS oxide film" is formed on top of the existing staircase structure. Nam, ¶ [0100].

322. Then, both the sacrificial layers and the damaged regions are etched to form "opening regions OP" in the shape of the gate electrodes and contact pads. Nam, ¶ [0104].

323. As shown in Figure 36 below, these openings are surrounded by both insulating layers 240 and 271:

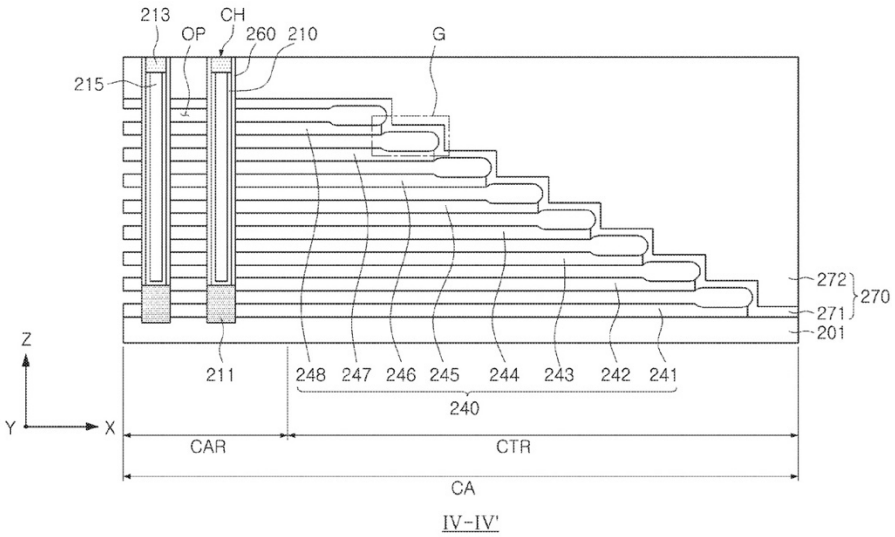


FIG. 36

Nam, Fig. 36. Figure 37 shows the area G in Figure 36, and the contact pad opening within that area, in more detail. *See id.*, Fig. 37.

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324. Finally, the openings are filled with conductive material to form the gate electrodes and pads. Nam, ¶ [0107].

325. Nam explains that during this process, some of the "implanted material" is "diffused to the inside of the first interlayer insulating layer 271 and then remains." Nam, ¶ [0105]. This creates a "doped region 271A … along an interface surface between the first interlayer insulating layer 271 and the second interlayer insulating layer 272." *Id.*

326. Figure 8A is once again reproduced below. In my opinion, because Nam's contact pad is formed within and at the "interface" of its insulating layer 271, a POSITA would have understood that the ***"curved" "side surface"*** of Nam's ***"second portion"*** (the top part of its contact pad, annotated orange below) is in ***"contact"*** with the ***"side surface"*** of its ***"insulating layer"*** (the portion of insulating layer 271 adjacent to the contact pad, annotated blue below) as this limitation requires.

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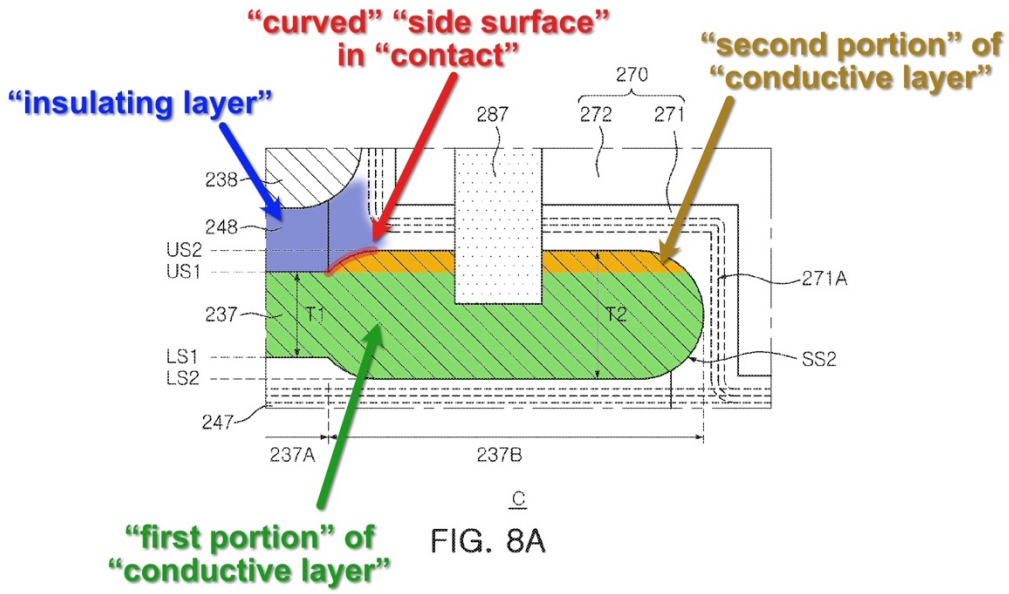


FIG. 8A

Nam, Fig. 8A (annotated).

327. I have been asked to consider whether only Nam's insulating layer 248—and not its layer 271—corresponds to the claimed ***"insulating layer."***

328. This is not how, in my opinion, a POSITA would have interpreted Nam.

329. As I have explained, Nam layer 271 is formed along with the alternating stack of insulating and conductive layers and is used to form Nam's contact pads. Thus, in my opinion, a POSITA would have understood that *both* layer 248 and layer 271 together form Nam's ***"insulating layer."*** And Nam's contact pad does contact insulation layer 271.

330. Regardless, in my opinion even if contact with layer 248 is required for some reason, in my opinion, Nam would still render the final limitation of Claim 17 obvious.

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331. A POSITA would have understood that because Nam forms its contact pad via ion implantation, a range of structures will result.

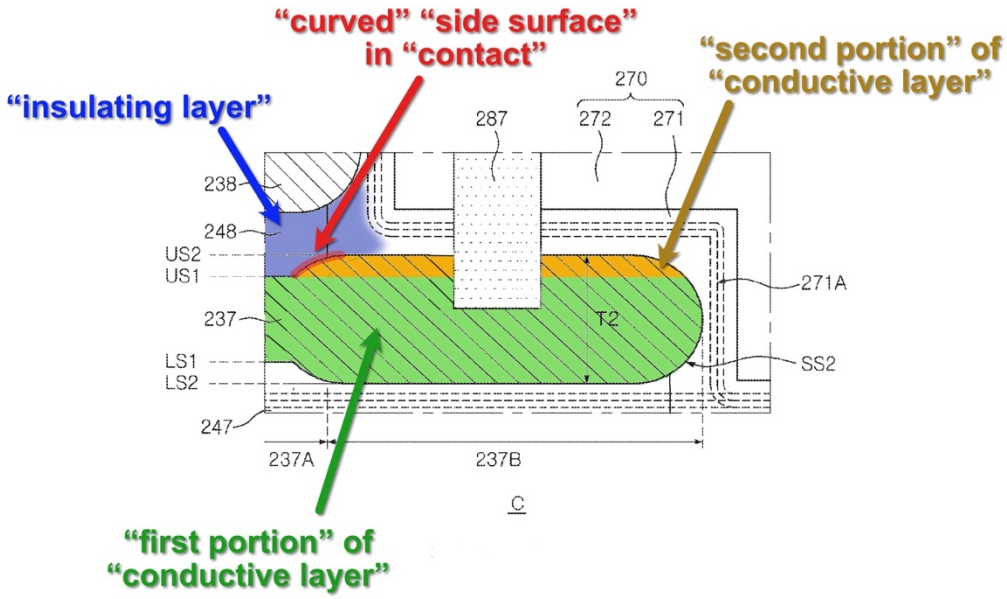
332. In other words, while Figure 8A depicts the intended or representative pad structure, ion implantation will result in both somewhat larger and somewhat smaller pads.

333. Because of this, in some layers, a POSITA would have understood that the pad will extend beyond the bounds shown in Figure 8A into layer 248 by some amount.

334. When the pad extends beyond the bounds of layer 248, there will be a longer interface of contact between the curved surface of the pad and layer 248.

335. An example of this is shown in the below demonstrative. This demonstrative was created using Figure 8A as the starting point. However, the pad has been shown with increased size resulting from an increased area of ion implantation. As shown, this causes the pad to expand into insulating layer 248 resulting in an increase in the contact interface between the pad side surface and that layer 248 (which has been annotated in red):

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336. In my opinion, a POSITA would also have understood that the amount of contact between Nam's pad and insulating layer 248 could be readily adjusted by tailoring the ion implantation process.

337. Nam includes examples where both (1) the corner of its contact pad (*see* Nam, Figs. 8A, 8B) and (2) the entire side surface of its contact pad (*see id.*, Figs. 6, 10) contact insulating layer 248.

338. A POSITA would have considered these pad designs to simply be examples on a continuum of possible pad shapes within the scope of Nam's disclosure.

339. In my opinion, a POSITA would thus have considered and been able given Nam's teachings to adjust both the shape of Nam's contact pad and achieve different amounts of contact between its various insulating layers.

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2. Claim 19

340. Claim 19 depends on Claim 17 and further requires:

[19] "wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack"

341. This, in my opinion, is taught by Nam.

342. Nam's device is formed from alternating conductive and insulating layers. *See* Nam, ¶¶ [0005], [0062]-[0063].

343. Figure 7 of Nam is reproduced below. As shown, each of Nam's ***"conductive layer[s]"*** (such as layer 237, annotated green) is located over ***"a first portion of the insulating layer of an adjacent layer stack"*** (such as layer 247, annotated blue):

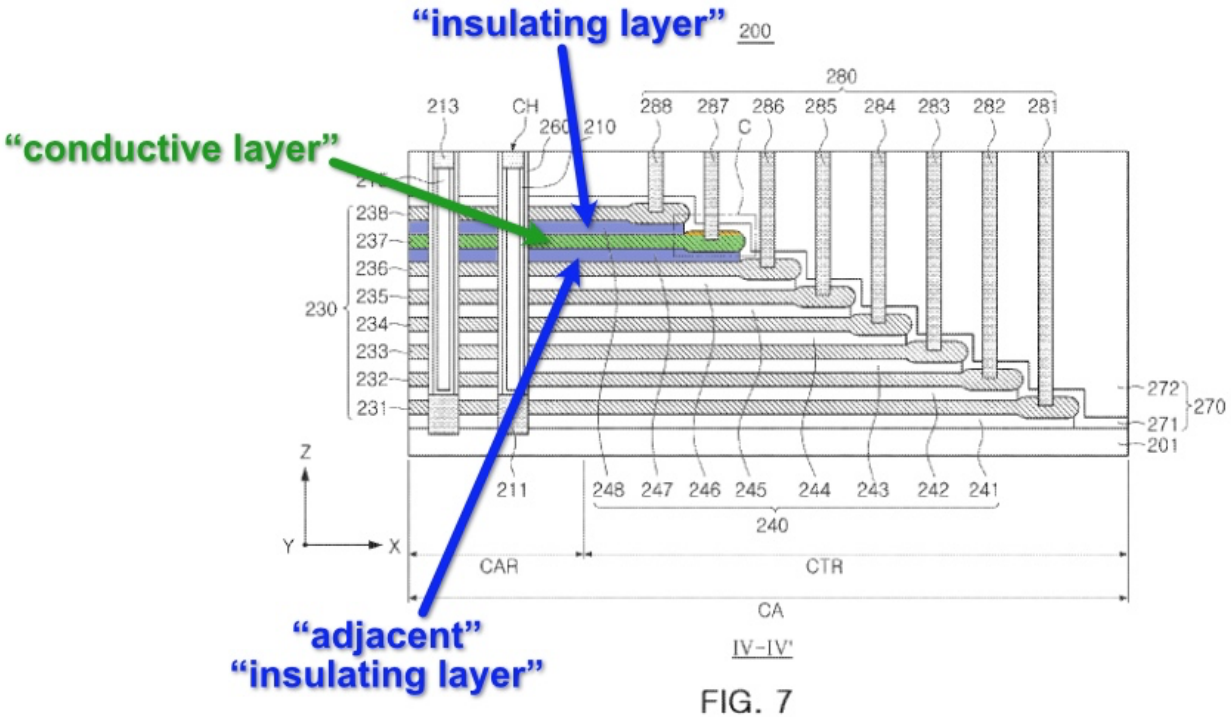


FIG. 7

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Nam, Fig. 7 (annotated).

344. Nam also explains that in the example contact pad shown in Figure 8A, the pad has a "lateral surface SS2 protruding outwardly therefrom in the first direction (X-axis direction)." Nam, ¶ [0066]. Moreover, each of Nam's contact pads are formed within interlayer insulating layer 271. *Id.*, ¶¶ [0067], [0098]-[0105]. The layer 271 follows the "step structure" of Nam's device. *See id.*, ¶ [0098]; *see also id.*, Fig. 7

345. As shown below, this causes a ***"second portion of the insulating layer of the adjacent layer stack"*** (insulating layer 271 below the extending contact pad) to be ***"laterally displaced from the conductive layer"*** (the lower layer 271 extends beyond the end of Nam's conductive layer 237 and the associated contact pad):

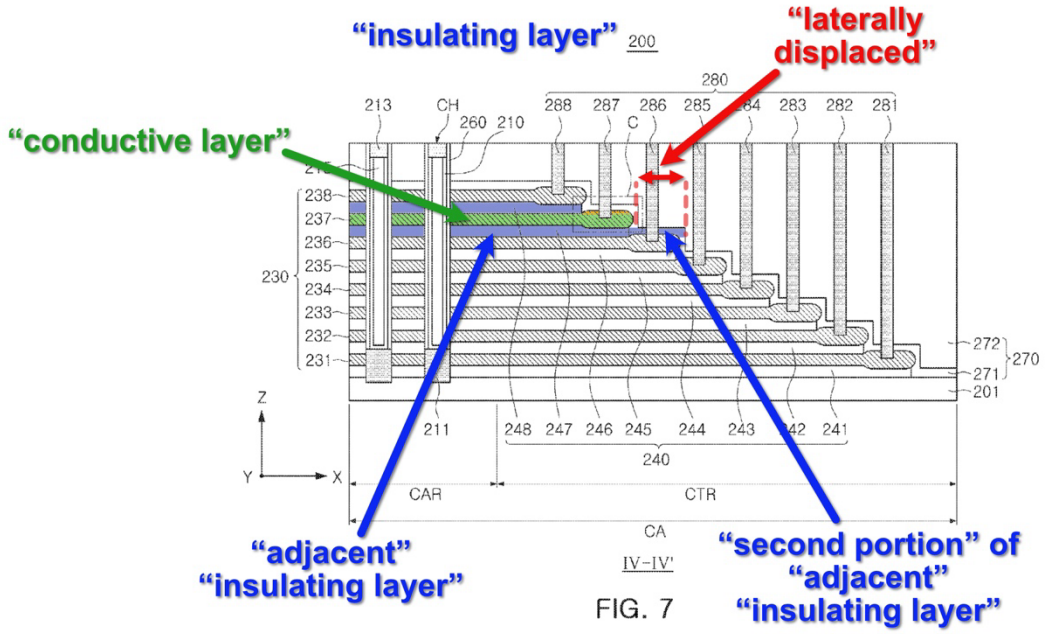


FIG. 7

Nam, Fig. 7 (annotated).

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3. Claim 20

346. Claim 20 depends on Claim 17 and further requires that:

[20] "wherein the conductive layer comprises a first conductive material, and wherein the curved side surface comprises a second conductive material."

347. This, in my opinion, is also taught by Nam.

348. Nam explains that its entire ***"conductive layer"*** 237—this includes both portion 237A and including the ***"second portion"*** 237B with the ***"curved side surface"*** —may be formed from the same "metal" material. Nam, ¶ [0107]; *see also id.*, ¶ [0094].

349. Again, as I note above, in the '666 patent the "first conductive material" and "second conductive material" need not be different and may be the "same." *See, e.g.,* Ex. 1001, 1:55-59.

D. *Ground 3*: Claims 17, 19, and 20 Are Obvious Over Lee and Park

350. In my opinion, a POSITA would have considered both Lee and Park to be within the scope of the prior art and highly relevant to the patentability of the '666 patent's claims.

351. In my opinion, when Lee is modified in view of Park and the knowledge of a POSITA, Claims 17, 19, and 20 of the '666 patent are rendered obvious.

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1. Claim 17

[17.Pre] "A memory device, comprising:"

352. To the extent this preamble language is limiting, in my opinion it is taught by Lee.

353. Lee explains that relates to "semiconductor device[s]" such as "three-dimensional (3D) non-volatile memory devices." Lee, ¶¶ [0005], [0008]-[0009].

354. Figure 13 of Lee depicts "the configuration of a memory system according to an embodiment of the… invention." Lee, ¶ [0017].

355. In this example figure, Lee's "memory system 100" can include " non-volatile memory device 120 and a memory controller 110." Lee, ¶¶ [0085]-[0090]; Fig. 13.

[17.A] "a substrate, wherein the substrate comprises a top surface;"

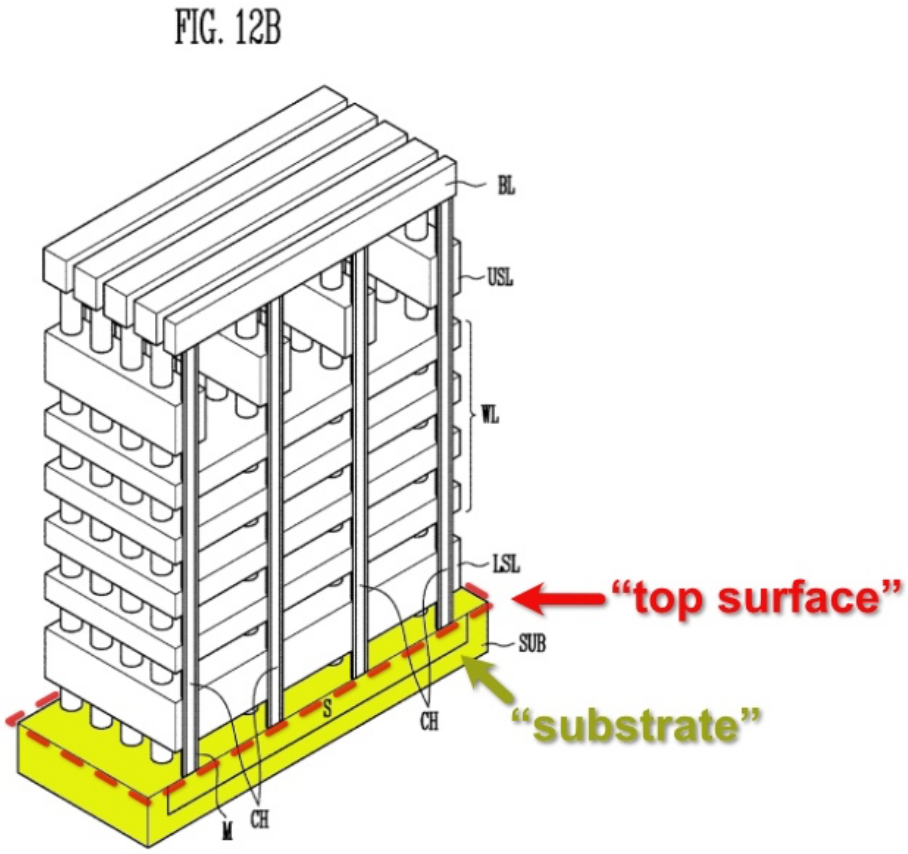
356. In my opinion, Lee teaches a ***"substrate"*** with a ***"top surface."***

357. Lee explains that its "semiconductor device" includes "a substrate" that includes a "cell region and a contact region." Lee, ¶ [0009]; *see also id.*, ¶¶ [0010] (noting that there are a "plurality of stacked structures" on the "substrate"); [0020] (the semiconductor device includes a "substrate").

358. Figure 12B of Lee, which is reproduced below, includes an example of a device with a "substrate SUB." Lee, ¶ [0068].

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359. As shown in this figure, the substrate includes an upper or top surface over which components of the memory are located. Lee, ¶ [0068]; *see also id.*, ¶¶ [0062]-[0063] (similarly discussing a "substrate SUB").



Id., Fig. 12B (annotated).

[17.B] "a memory string disposed over the substrate; and"

360. This, in my opinion, is also taught by Lee.

361. Lee's device includes a "plurality of memory cells" that are "coupled in series with each other" to form a "single string." Lee, ¶ [0071].

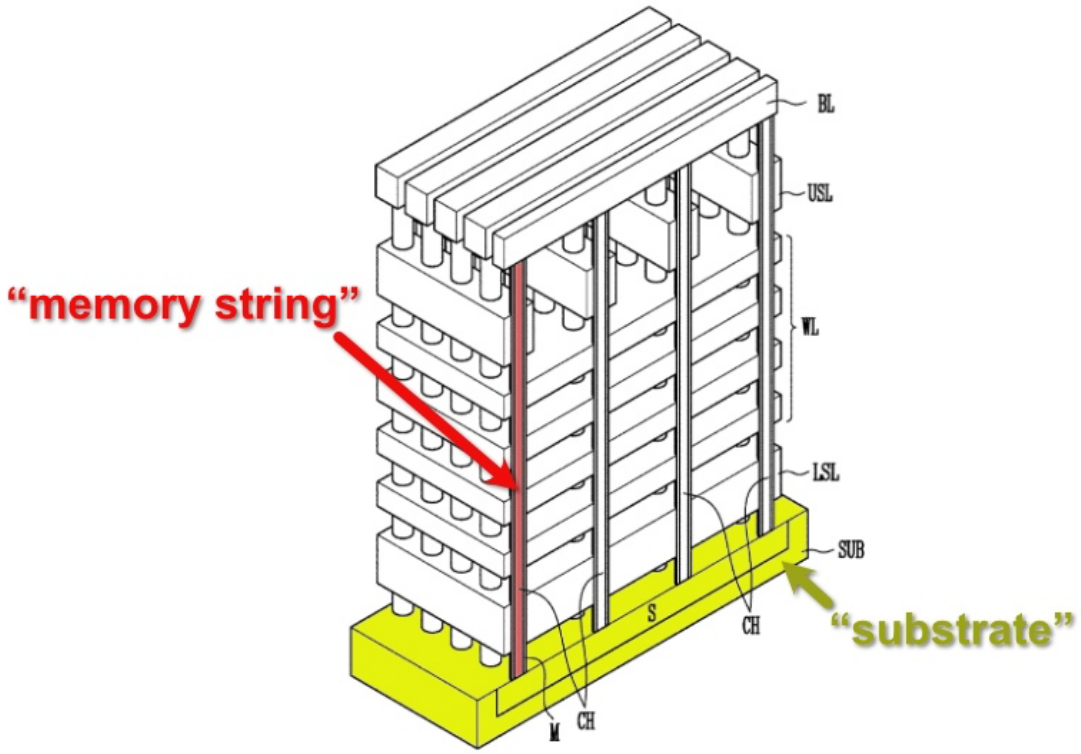
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362. According to Lee, there are many such "string[s]" "arranged in a vertical manner" in its device. Lee, ¶ [0071].

363. Lee also explains that each of these memory strings include a central "channel layer CH" with individual "memory cell[s]" formed at the "intersection between the channel layer CH" and a "word line WL." Lee, ¶ [0071]. The "channel layers CH" are located above and "protrude from the substrate SUB." *Id.*, ¶ [0069].

364. One such "***memory string"*** is annotated in red in Figure 12B below. As shown, the string is located over the surface of the substrate SUB, which is shown in yellow:

FIG. 12B



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Lee, Fig. 12B (annotated).

[17.C] "a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises;"

365. This, in my opinion, is also taught by Lee.

366. Lee explains that its device includes both a "contact region CONTACT" and a "cell region CELL." Lee, ¶ [0020].

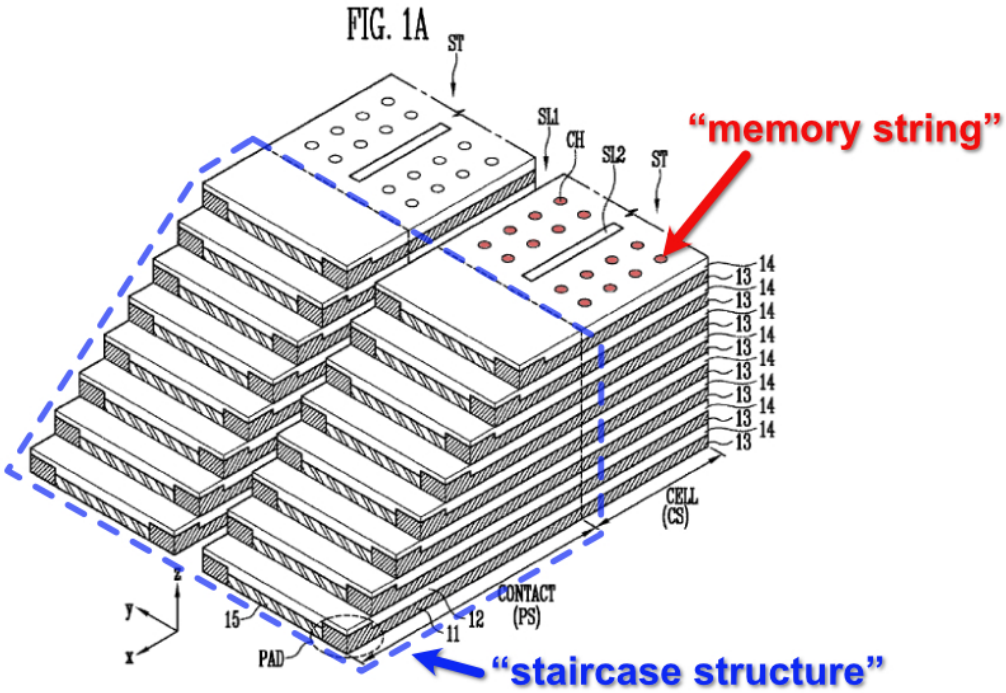
367. The "cell region" includes the "channel layers CH" along which Lee's memory cells (and the strings containing those cells) are formed. Lee, ¶ [0026].

368. A "stacked structure ST" formed from "conductive layers 11 and 13 and insulating layers 12 and 14" is located in both the CONTACT and CELL regions. Lee, ¶ [0020].

369. Lee explains that "[a]n end of the stacked structure ST may be patterned stepwise." Lee, ¶ [0021]. Likewise, per Lee, "an end of the pad structure is patterned stepwise." *Id.*, ¶¶ [0009].

370. Figure 1A of Lee is reproduced below. In this Figure, Lee's ***"staircase structure"*** (the stepped portion of the CONTACT region, outlined in blue) and example ***"memory string[s]"*** (located along channel layers CH, annotated in red) are both emphasized:

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Lee, Fig. 1A (annotated).

[17.C.1] "a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer,"

371. In my opinion, Lee teaches the claimed ***"plurality of layer stacks"*** with alternating ***"insulating"*** and ***"conductive" "layer[s]."***

372. Lee's device includes a "stacked structure ST" that is "patterned stepwise." Lee, ¶ [0021].

373. The "stacked structure ST" is formed from "conductive layers … and insulating layers … that are formed alternately with each other on the substrate." Lee, ¶ [0020]. "Each step of the stacked structure" includes "at least one conductive layer … and at least one insulating layer…." *Id.*, ¶ [0021]. The "insulating layer" is "located on" the "top surface of each step." *Id.* Similarly, Lee explains that in its

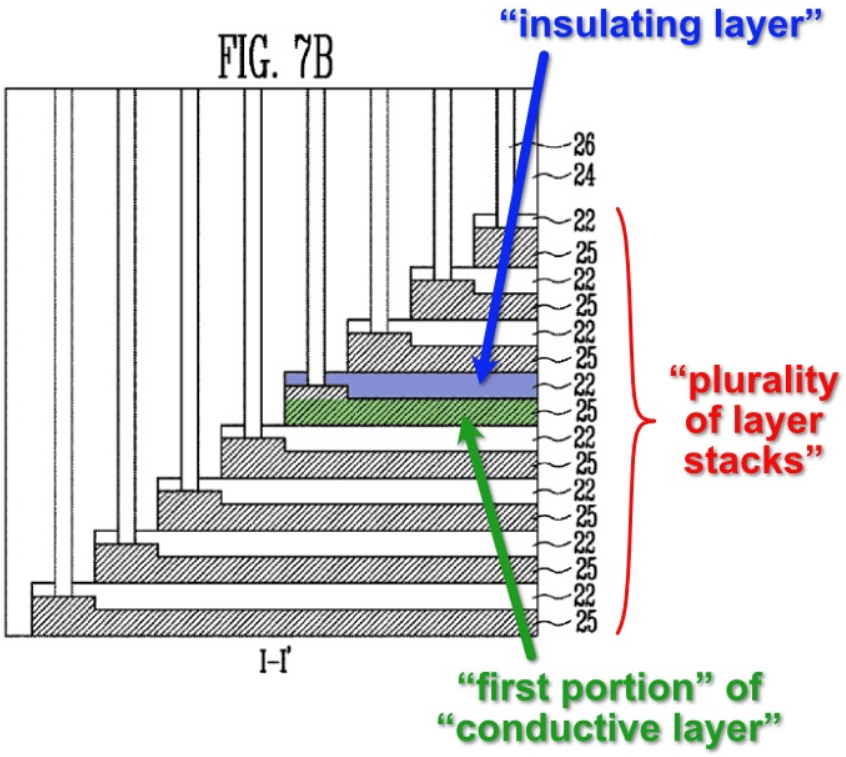
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"stacked structure[,]" "a plurality of conductive layers and a plurality of insulating layers" are "formed alternately with each other." *Id.*, ¶ [0010].

374. Figure 7B, which is reproduced below, provides an example.

375. In this figure, layers 22 are "interlayer insulating layers." Lee, ¶ [0046]. Layers 25 are "conductive layers." *Id.*, ¶ [0041].

376. As shown, in each ***"layer stack"*** (the combination of an insulating layer 22 and conductive layer 25 that together form a step), the ***"insulating layer"*** (layer 22, annotated blue) is ***"disposed over a first portion of a conductive layer"*** (the green annotated portion of conductive layer 25):



Lee, Fig. 7B (annotated). Figures 1A and 6B similarly show devices with alternating conductive and insulating layers. *See id.*, Figs. 1A, 6B.

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[17.C.2] "wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer."

377. In my opinion, Lee, when modified following Park's teachings, renders this limitation obvious. Lee highlights the importance of maintaining sufficient spacing between conductive layers to prevent breakdown voltages. Park's teachings on rounded pad designs directly address this issue by increasing the distance between adjacent conductive layers. A POSITA would recognize that rounding Lee's pad portions would align with Lee's stated goals and provide a straightforward design modification with predictable success.

378. To begin, Lee's device already includes a ***"conductive layer"*** with both a ***"first portion"*** and ***"second portion."***

379. According to Lee, each of the "conductive layers" in its stepped stack may include a "pad portion[] PAD" at its end that has "a greater thickness" than other portions of "the … conductive layer." Lee, ¶ [0023]; *see also id.*, ¶ [0009] (Lee's "semiconductor device" includes "pad portions" that "have a greater thickness than unexposed portions of the plurality of first conductive layers"); ¶ [0027] (similar).

380. Lee explains that because the pad is only on the end of each conductive layer in its stack, "the thickness of the pad portion PAD may be selectively increased without increasing the height of stacked structure ST." Lee, ¶ [0027]. In other

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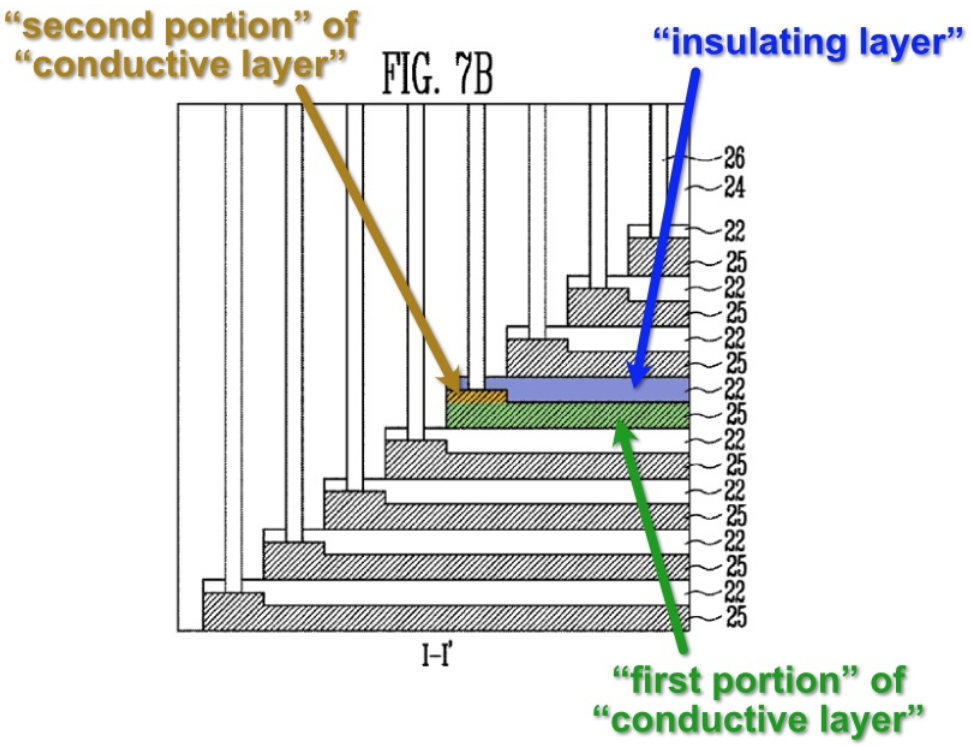
words, the stack's height does not increase, but the thickness of each pad does increase.

381. The "pad portions PAD" allow "contact plugs 26" to be "coupled" to each of Lee's conductive layers. Lee, ¶ [0042].

382. According to Lee, the increased height of the pads is intended to avoid a "punch phenomenon … due to over-etching of upper pad portions PAD" or a "not-open phenomenon" resulting from "lower pad portions PAD" which "may not be exposed along bottom surfaces of the contact holes." Lee, ¶ [0043].

383. Figure 7B from Lee is reproduced below. In this figure, the pad portion PAD on the end of each of Lee's conductive layer is the claimed ***"second portion"*** of a ***"conductive layer."*** One such ***"second portion"*** is annotated brown/orange. The underlying ***"conductive layer"*** is annotated blue:

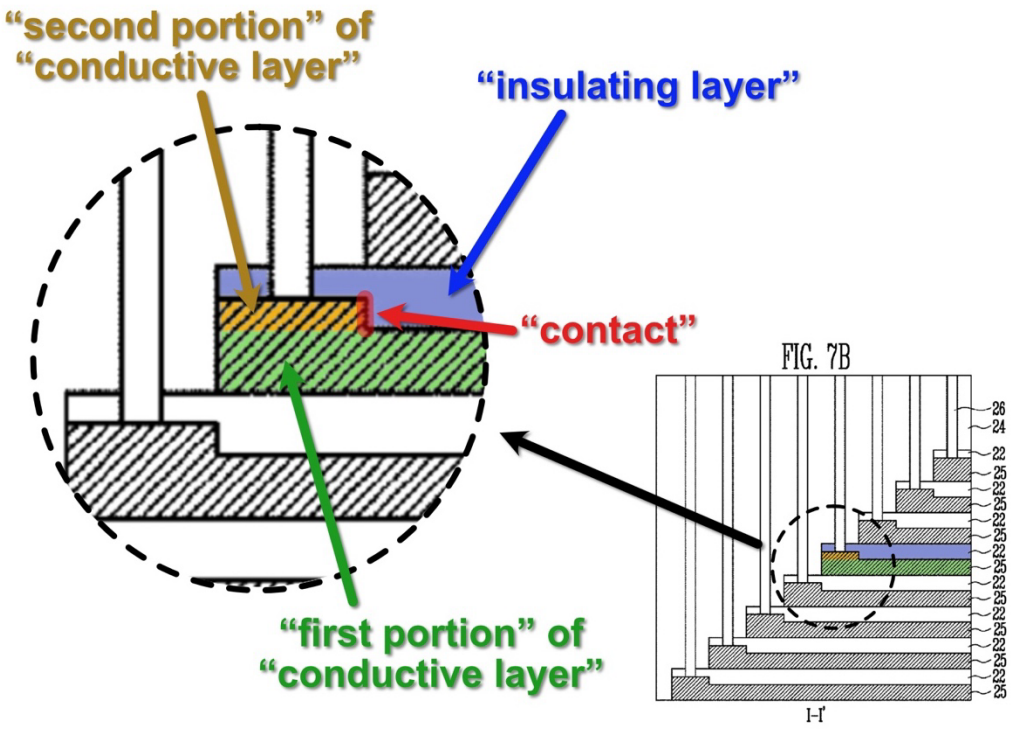
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Lee, Fig. 7A (annotated). Figure 1A similarly showing device with alternating insulating and conductive layers and pad portion PAD. *See id.*, Fig. 1A.

384. Another annotated version of Figure 7B is reproduced below. The portion of the figure showing one example pad is expanded to the left of the figure. As shown, and as this claim requires, the ***"side surface"*** of the ***"second portion"*** of Lee's ***"conductive layer"*** (Lee's pad portion PAD, annotated orange / brown) is in ***"contact"*** with ***"a side surface of the insulating layer"*** (insulating layer 22 in Figure 7B, annotated blue). The area of contact is annotated in red:

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Lee, Fig. 7B (annotated).

385. The ***"side surface"*** of Lee's insulating layer 22 that is in contact with the pad portion PAD is not at the extreme end of the insulating layer. In my opinion, however, there is nothing about Claim 17 that requires this to be the case.

386. Claim 17 requires only that there be contact with "***a*** side surface of the insulating layer." There is no requirement in the claim that this side surface be at any particular location along the length of the insulation layer.

387. Confirming this, the '666 patent explains that a "layer" can "include multiple layers" or sub-layers. Ex. 1001, 4:36-37, 4:52-53. This is all that Lee teaches: its insulating layer effectively includes two portions or layers, a lower portion or layer that contacts the side of the contact pad and an upper portion of layer

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that extends over the contact pad. Put another way, Lee's pad portion PAD is in contact with the side of the lower portion—or lower or sub-layer—of insulating layer 22.

388. A POSITA also would have understood that the process Lee employs to form its pad portion PAD confirms that there is contact between the PAD and the adjacent insulating layer.

389. Lee begins by forming "a plurality of first material layers 21 and a plurality of second material layers 22 … alternatively with each other." Lee, ¶ [0029].

390. The "layers 21," which will eventually be replaced by Lee's "conductive layers," are "formed of materials having a high etch selectivity with respect to second material layers 22." Lee, ¶ [0030].

391. The "second material layers 22" are "an insulating layer such as an oxide layer." Lee, ¶ [0030].

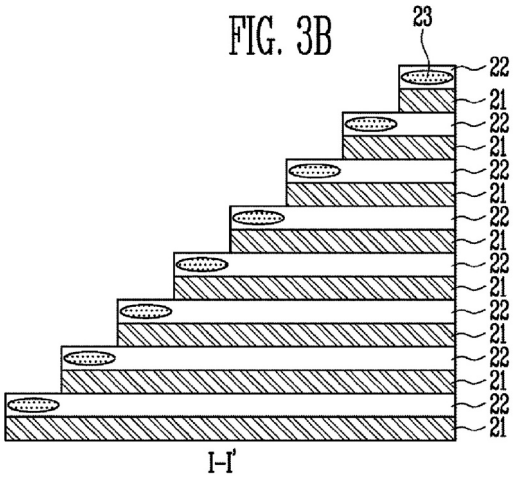
392. Lee then employs an "ion implantation process" to "implant[]" "impurity regions 23" into the insulating layers 22. Lee, ¶ [0034].

393. These impurity regions will eventually form the thicker portions of Lee's pad portions PAD. *See* Lee, ¶¶ [0038]-0041].

394. Figure 3B below generally shows how (and generally where) the impurity regions are created in insulating layers 22:

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FIG. 3B



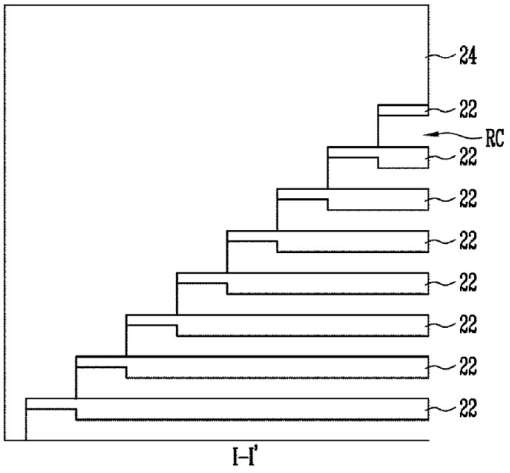
Lee, Fig. 3B.

395. Then, Lee etches layers 21 using an isotropic etch step. Lee, ¶ [0038].

396. Then, it performs a second wet etch step to remove the impurity regions 23 to form "recessed regions RC" between the remaining portions of the insulating layers 22. Lee, ¶ [0038].

397. The formation of these openings or recessed regions RC are shown in Figure 5B.

FIG. 5B

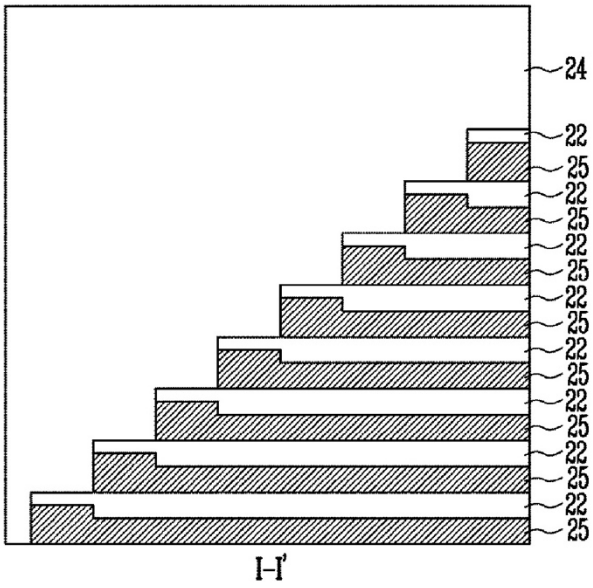


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Lee, Fig. 5B.

398. Then, Lee explains that the openings formed via etching are filled with "conductive layers 25" to create the "pad portions PAD exposed at the end of stacked structure ST." Lee, ¶ [0041].

FIG. 6B



Id., Fig. 6B.

399. Because Lee's pad portions PAD are formed within an opening in its insulating layers 22, a POSITA would have understood that the sides of the pad portions PAD contact the sides of the insulating layers.

400. Lee does depict its pad portions PAD as having straight sides in its figures.

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401. Regardless, in my opinion, a POSITA would have considered it obvious to make the ***"side surface"*** of Lee's ***"second portion of the conductive layer" "curved"*** in view of Park's teachings.

402. Again, as I have explained above, including in Ground 1, Park teaches a three-dimensional memory device that includes a stepped "connection region" with "pad region[s] PAR" located on the end of gate electrodes. Park, 6:7-12, 6:36-47.

403. Each of Park's electrodes terminates with a "pad region PAR" that includes a "raised pad portion 28." Park, 7:4-16.

404. Park also explains that the "end 79b" of this "raised pad portion 78" may be "rounded" to "prevent a short circuit" between the pad and an "adjacent … conductive layer pattern 72c." Park, 11:35-41.

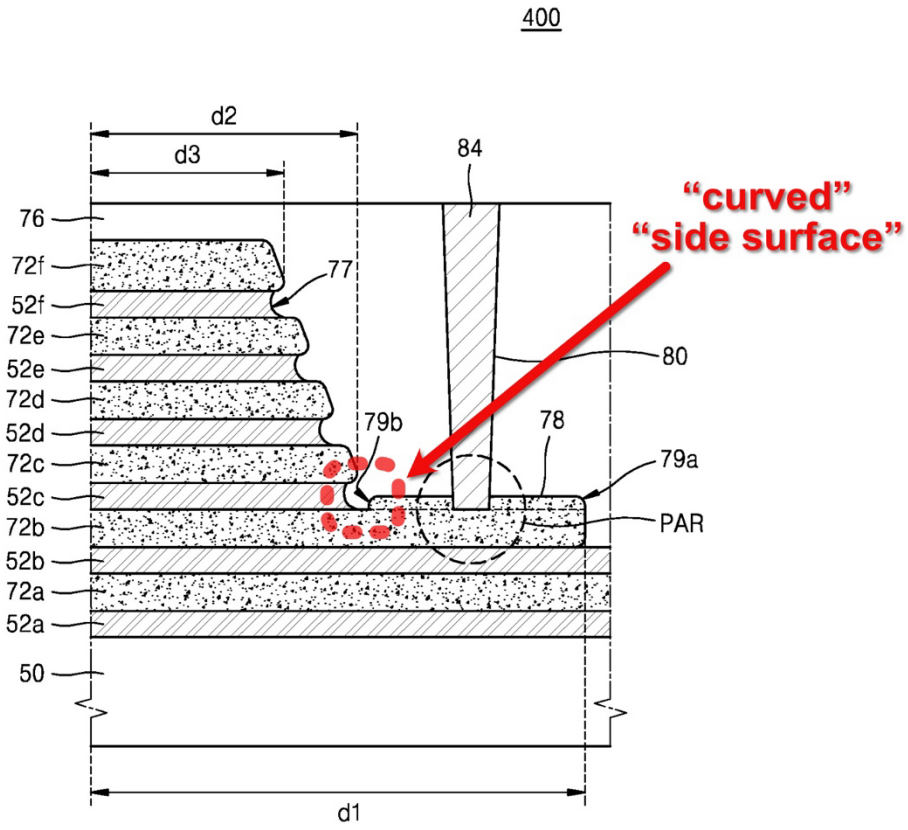
405. Park explains that it achieves its rounded contact pad by "ion implanting impurities" "into" an "insulating layer" and performing an "oxidation" step to create a "additional sacrificial layer" "having a higher etching rate" than the surrounding insulation. Park, 12:16-23, 39-47.

406. The sacrificial material is then removed and replaced with conductive material to form insulation surrounded electrodes and curved pads. Park, 12:48-56.

407. Figure 7 from Park below shows the eventual result of this process: a pad 78 with a curved surface 79b facing towards Park's stack of alternating conductive and insulating layers:

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FIG. 7



Park, Fig. 7 (annotated).

408. Similar processes—the implantation of impurities into a layer of insulation to form an etchable region corresponding to a desired contact pad shape—was also used by other prior art to form contact pads with rounded sides surrounded by insulation.

409. For example, Nam discusses the use of multiple ion implantation steps to form a contact pad with a bullnose or a convex shape with rounded sides similar to those taught in Park. *See, e.g.,* Nam, ¶¶ [0097]-[0105]; Figs. 30-37.

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410. Applying Park's teachings to Lee—and making at least the end of Lee's pad portion PAD facing its conductive layers rounded—results in what this limitation requires.

411. Again, a pad with a rounded side would have been achieved by tailoring the ion implantation steps (or ion implantation and oxidation steps like that taught by Park) to produce this particular shape. In particular, a POSITA would have understood that to achieve a contact pad with a curved side, the process shown in Figures 3B, 4B, and 5B of Lee could still be followed: ion implantation would be performed on the insulating layers, and then etching steps would be performed to remove the intervening sacrificial layers followed by the region where ion implantation occurred. This would then result in the same-shaped openings shown in Figure 5B of Lee. Then, to achieve a rounded rather than straight sided contact pad, oxidant would be introduced into the openings.

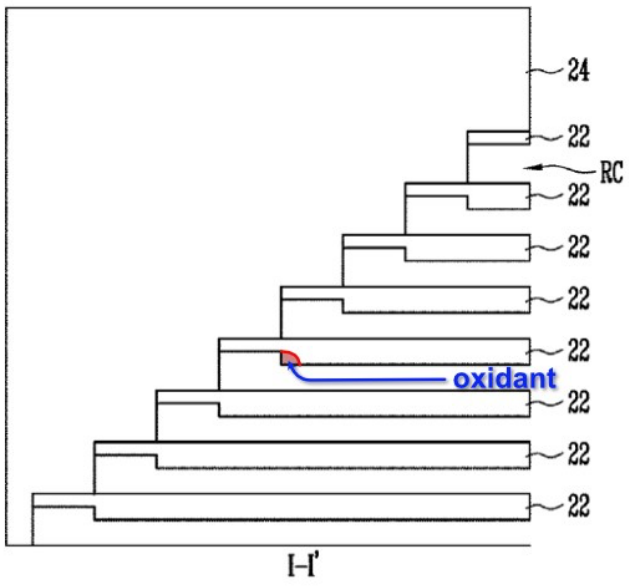
412. A POSITA would have recognized that oxidation rates differ at exposed corners and planar surfaces due to variations in oxidant flux and material redistribution, leading to rounded corners. The exterior corner (red below) would be rounded via oxidation first and most aggressively. The oxidant's actions on the interior corners would be somewhat slower, while the action on the planar surfaces would be even slower. A convex (or exterior) corner like that highlighted below rounds off during oxidation because the sharp geometry increases the flux of

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oxidizing species and the strain energy at the tip, leading to a faster reaction rate compared to flat surfaces. As oxidation progresses, the oxide material redistributes, smoothing the sharp corner into a rounded shape. Concave (or interior) corner will also round off, albeit more slowly. The sharp geometry of the corner reduces localized stress concentrations, prompting material diffusion and redistribution to lower the strain energy. Due to the difference in geometry and mechanism of action, this produces a more gradual smoothing than experienced at a convex (or exterior) corner. Neither of these effects apply to planar surfaces.

413. The amount of rounding would be readily controllable—and confined to the depicted exterior corner with only limited impact on the interior corners and planar surfaces—by adjusting the amount of time the oxidant is permitted to remain within the opening:

FIG. 5B

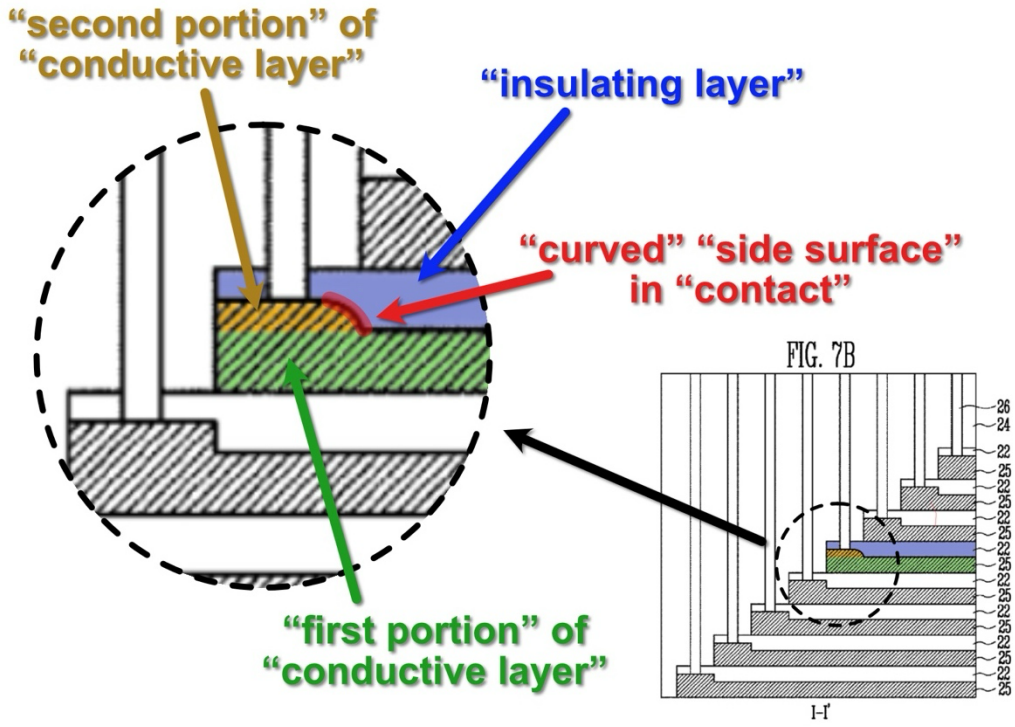


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Lee, Fig. 5B. Then, when this now rounded opening is filled with conductive material, a contact pad with a rounded side results.

414. Application of this to Lee is shown in the below demonstrative. This demonstrative was created using Figure 7B from Lee, just with the pad with rectangular or square sides replaced with a rounded side.

415. Because the contact pad is curved or rounded, now the ***"second portion"*** of Lee's ***"conductive layer"*** (pad portion PAD, which is annotated orange)) includes a ***"curved" "side surface"*** (annotated in red) that is in ***"contact"*** with a ***"side surface"*** of its ***"insulating layer"*** (which is annotated blue):



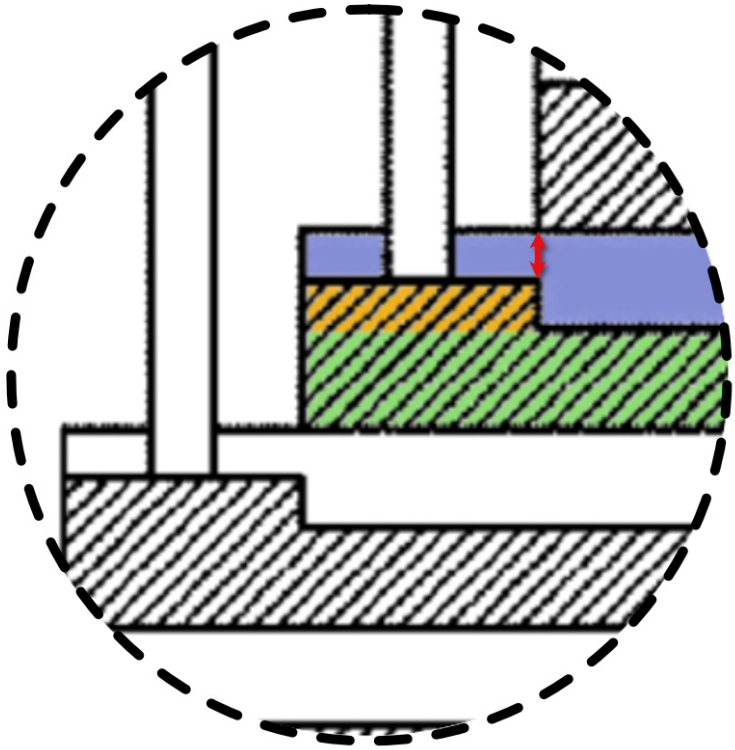
Lee, Fig. 7B (modified and annotated).

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416. In my opinion, a POSITA would have been motivated to make the end of Lee's pad portion PAD facing its conductive layers rounded.

417. Again, Park explains that rounding the contact pad helps "prevent a short circuit" between the pad and an "adjacent" conductive layer. Park, 11:35-41.

418. In my opinion, a POSITA would have recognized that due to their straight sides, each of Lee's pad portions PAD is physically proximate to the adjacent conductive layer immediately above the pad. This is shown below. As depicted, the orange contact pad is located relatively close to the conductive layer immediately above it:



Lee, Fig. 7B (excerpted and annotated).

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419. In my opinion, a POSITA would have recognized that this creates a risk of short circuit in the event variances in the manufacturing process cause either the pad or the adjacent conductive layer to extend further than intended such that unwanted electrical connection or bridging over the intervening dielectric occurs.

420. In my opinion, a POSITA would have recognized that applying Park's teachings and rounding the side of Lee's pad portion PAD would have improved Lee—and limited the risk of short circuit or other adverse electrical effects—by increasing the minimum distance between the pad and the immediately adjacent conductive layer.

421. Similarly, and consistent with Park's teachings that short circuits should be avoided, Lee itself notes that if the PAD and conductive layer are too close, there is a risk that the "breakdown voltage" between these layers may be "deteriorated." Lee, ¶ [0049].

422. According to Lee, this can be avoided by ensuring that there is "sufficient distance … between the stacked conductive layers (pad portions)." Lee, ¶ [0049].

423. In my opinion, a POSITA would have understood that applying Park's teachings and rounding Lee's pad portions PAD furthers this goal: when the pads are rounded, the distance between conductive layers would be increased avoiding deterioration of the breakdown voltage.

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424. A POSITA further would have recognized that contact pads with rounded, curved side surfaces were also a known, routinely used alternative for memory devices with staircase structures at the time the '666 patent was filed. *See, e.g.*, Kim, 8:29-34 (noting that contact pads can have a "curved surface"); Park, 11:35-41 (contact pad can be "rounded"); Yun, 8:33-40 (contact pad can have "rounded" "side surface"; Nam, ¶ [0066] (contact pad can have "bull nose" or "convex" shape).

425. In my opinion, given the prevalence of contact pads with this type of shape in the prior art, a POSITA would have considered the use of rounded/curved pads with Lee to be nothing more than a routine, obvious design choice.

426. A POSITA would also have had every reason to believe that a curved pad could be successfully used with Lee.

427. Again, numerous prior art references identified this type of pad as acceptable for three-dimensional memory devices with staircase structures. *See, e.g.,* Kim, 8:23-34; Park, Fig. 8; Yun, Fig. 5A; Nam, Fig. 8A.

428. Moreover, Lee explains that the shape of its pad portion PAD is controlled via an "ion implantation process." Lee, ¶¶ [0034], [0038]-[0041].

429. As explained in Ground 1, a POSITA would have recognized that this type of process could be readily adapted to form a curved contact pad. *See, e.g.,* Park, 7:17-29 ("ion implantation" employed to form pad with "rounded" sides);

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Nam, ¶¶ [0066], [0098]-[0107]; Figs. 30-39 (discussing use of "an ion implantation process" at length to form "convex" contact pad).

2. Claim 19

430. Claim 19 depends on Claim 17 and further requires:

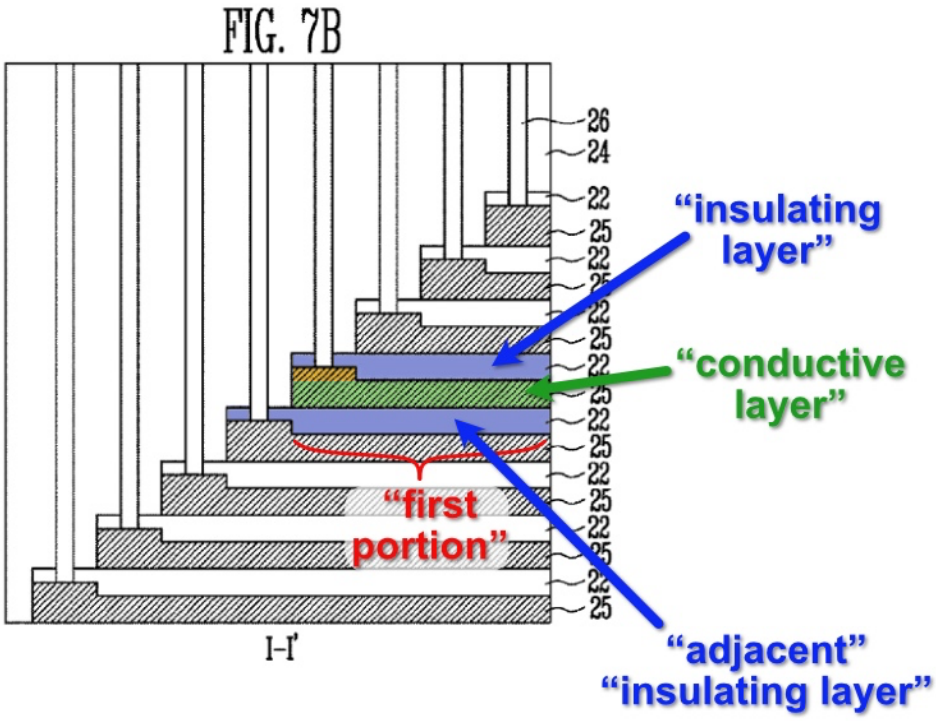
[19] "wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack"

431. This, in my opinion, is taught by Lee.

432. As I have explained, Lee's device includes a "stacked structure ST" formed from alternating "conductive layers" and "insulating layers." Lee, ¶¶ [0020]-[0021]; *see also id.*, ¶¶ [0010], [0041], [0046]; Figs. 1A, 7A.

433. Figure 7B of Lee is again reproduced below. As shown, because there are alternating conductive and insulating layers, each of Lee's ***"conductive layer[s]"*** (conductive layer 25 in Fig. 7B, annotated green) is located over ***"a first portion of the insulating layer of an adjacent layer stack"*** (the portion of insulating layer 22 in Fig. 7B immediately below the conductive layer, annotated blue):

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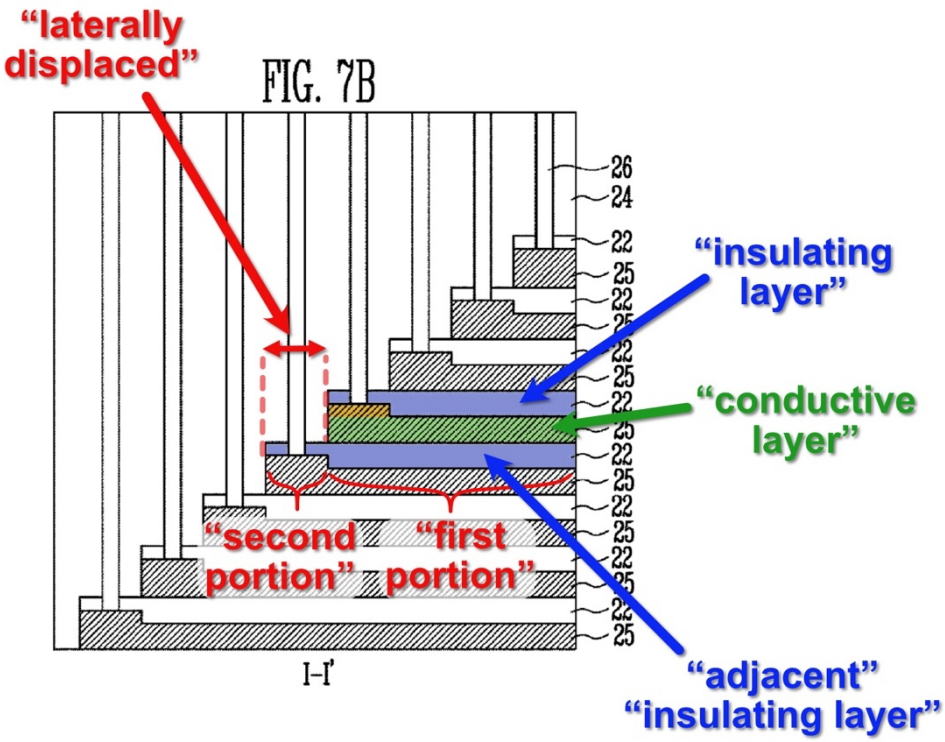
Lee, Fig. 7B (annotated).

434. Next, in Lee, "[e]ach step of the stacked structure ST that is patterned stepwise" includes "one conductive layer" and "one insulating layer." Lee, ¶ [0021].

435. In Figure 7B, again annotated below, "the insulating layer" is "located on a top surface of each step." *Id.*

436. This results in ***"second portion of the insulating layer of the adjacent layer stack"*** (the portion of a lower insulating layer 22, annotated blue, that extends out beyond an upper adjacent conductive layer 25, annotated green, for purposes of forming a step) being ***"laterally displaced from the conductive layer"***:

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Lee, Fig. 7B (annotated).

3. Claim 20

437. Claim 20 depends on Claim 17 and further requires that:

[20] "wherein the conductive layer comprises a first conductive material, and wherein the curved side surface comprises a second conductive material."

438. This, in my opinion, is also taught by Lee.

439. In Lee, conductive layer 25 and the pad portion PAD on the end of that layer are formed from "conductive" material. Lee, ¶¶ [0040]-[0041]; *see also id.*, ¶ [0021] (noting that "conductive layers" are employed).

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440. Again, as I have explained, while this claim does reference a "first conductive material" and "second conductive material," the '666 patent explains that these materials need not be different. *See, e.g.,* Ex. 1001, 1:55-59.

E. Secondary Considerations of Non-Obviousness

441. Based on my review of the '666 patent's prosecution history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's claims.

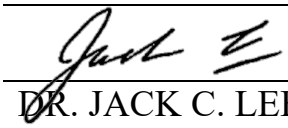
442. I am not separately aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like. Instead, as discussed above, it is my opinion that the subject matter embraced by the '666 patent's claims was known in and obvious over the prior art. Moreover, it is also my opinion the teachings of the prior art would have been expected to successfully function as or be usable with working 3D memory devices.

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I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: November 22, 2024

Location: Austin TX

Signature: 

DR. JACK C. LEE

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