

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00189
Patent 11,145,666

**DECLARATION OF KONSTANTINOS GIAPIS
IN SUPPORT OF
PATENT OWNER'S PRELIMINARY RESPONSE**

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I. Introduction and Qualifications

1. I have been retained by Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) to provide my opinions concerning the validity of claim 19 of the U.S. Patent. No. 11,145,666 (Ex. 1001).

2. I am a professor of chemical engineering at the California Institute of Technology (“Caltech”). I have held a professional position at Caltech since 1993.

3. My primary research relates to the processing of semiconductors, dielectrics, and metals, as performed in the fabrication of semiconductor devices, including microprocessors and digital memories. In particular, my work has focused upon experimental and computational studies of various aspects of depositing and patterning of layers of electronic materials to fabricate sub-micron features such as transistor gates, vias, and interconnect channels found in VLSI circuits and digital storage. My research group has contributed to the understanding of the evolution of such features (profiles) in single-crystalline silicon, poly-silicon, metal, and dielectric layers subjected to plasma processing (etching, deposition, ion implantation). Since the start of my graduate career in 1985, I have accumulated over 40 years of experience on most aspects of processing of semiconductor materials and devices.

4. In my professorial duties at Caltech, I have developed and taught new undergraduate and graduate level courses on semiconductor device physics, processing, and fabrication. These innovative courses combined solid state physics and electronic materials processing technologies with the more traditional chemical engineering subjects of transport phenomena and chemical thermodynamics. The courses have prepared several generations of students for successful careers in the semiconductor industry.

5. During my research career, I have authored or co-authored 100 peer-reviewed papers, 12 refereed conference proceedings, and two book chapters. Most of my publications relate to basic aspects of semiconductor processing and, in particular, the interaction dynamics of plasma ions with patterned and unpatterned surfaces of materials used in semiconductor manufacturing. My papers on charging damage during plasma-processing of VLSI devices are highly cited. The latter work includes studies of charging effects and surface breakdown during directional (plasma) deposition of interlevel dielectrics on patterned metal interconnects. My laboratory has also extensively used and studied plasma-deposited silicon oxide layers from silane and TEOS precursors.

6. Additional information regarding my education, technical experience and publications, including a list of 14 U.S. patents I have co-

invented, is included in my *Curriculum Vitae*, which I understand is attached at Exhibit 2006.

II. Summary of Materials Reviewed and Considered

7. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor fabrication, I reviewed the following documents, and other documents cited herein:

Ex.	Description
1001	United States Patent No. 11,145,666 (“the ’666 patent”)
1002	File History for ’666 patent (“’666 FH”)
1003	Declaration of Dr. Jack C. Lee
1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
1005	U.S. Patent No. 10,229,929 to Kim et al. (“Kim”)
1006	U.S. Patent Publication No. 2018/0026046 A1 to Nam et al. (“Nam”)
1007	U.S. Patent Publication No. 2014/0191389 A1 to Lee et al. (“Lee”)
1008	U.S. Patent No. 10,297,543 to Park et al. (“Park”)
1010	Aritome, “NAND Flash Memory Technologies” (2016)
1011	Michelsoni et al, “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1013	Excerpts from the File History of PCT/CN2018/098962
1014	File History of U.S. Patent No. 10,680,003 (Appl. 16/126,956)
1018	U.S. Patent No. 9,343,452 to Yun et al.

8. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the '666 patent at the time of the alleged invention, which I have been asked to assume is August 28, 2017.

III. Understanding of Legal Standards

9. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

10. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

A. Claim construction

11. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of

filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim construction presumes that different words in a claim have different meanings, unless there is evidence to the contrary.

12. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the United States Patent and Trademark Office ("USPTO"). I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. Obviousness

13. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While

such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

14. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA) is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

15. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the

pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

16. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). Thus, in considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, an assertion that a person of ordinary skill could combine the references, rather than that they would have been motivated to do so, is an impermissible form of hindsight. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

17. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a skilled artisan would be motivated

to make a combination includes whether he/she would select particular references in order to combine their elements.

18. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

19. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient reasoning. But, common sense can only be used to supply a limitation missing from the prior art where the technology is unusually simple and straightforward.

20. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not

to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be taken into account in determining obviousness.

IV. Person of Ordinary Skill in the Art

21. Dr. Lee defines a person of ordinary skill in the art (“POSITA”) as a person having “a bachelor’s degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) 3D memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may substitute for professional experience).” Ex. 1003 ¶ 36. Dr. Lee further notes that “this POSITA would also have been aware of an generally knowledgeable about 3D memory’s structure, its component parts, and how it operates.” Ex. 1003 ¶ 37.

22. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art. In view of my educational background and work experience, I surpass Dr. Lee’s definition of a POSITA,

and did so before August 28, 2017. Regardless of the precise definition of a POSITA, none of the Grounds in the Petition show that the challenged claims are obvious. I reserve the right to opine as to an alternative level of a POSITA in other proceedings or if the Board institutes review in this proceeding.

V. Overview of 3D NAND Memories

23. 3D NAND memory is an assembly of discrete memory cells in three dimensions, developed to increase digital memory density. While the process has matured over the years, it is not a simple or straightforward technology.

24. 3D NAND memory devices include “a stack of word lines horizontally arranged over a substrate, with vertical semiconductor channels that intersect the word lines.” ’666 patent at 1:29-32. “The intersection of a word line and a vertical semiconductor channel forms a memory cell.” ’666 patent at 1:32-33. Memory cells can be written or read by applying a voltage to the “word lines,” which are made of an electrically conductive material and run horizontally across the memory array. *E.g.*, ’666 patent at 5:24-30; Nam (Ex. 1006) at [0030]-[0031], Fig 2. For example, the figure below, from Exhibit 1011, shows vertically stacked memory cells on the left hand side, each controlled by a Control Gate (CG) accessible electrically by means of word lines. Ex. 1011 at

134; *see also* Ex. 1010 at 62, Fig. 3.4 (equating “Control Gate” with “Word Line”).¹

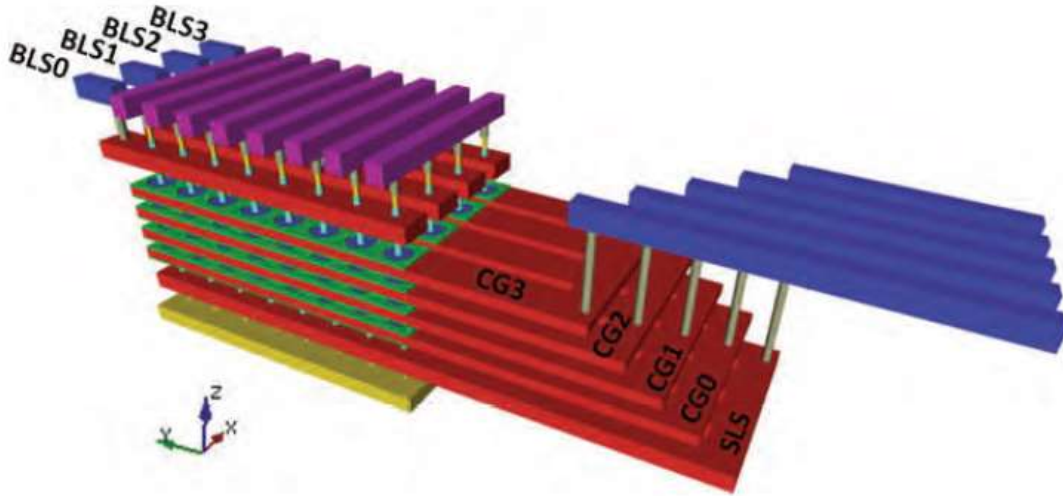


Fig. 5.20 C-FG NAND Flash array with fan-out

25. The word lines (CG0, CG1, CG2, and CG3) themselves need to be accessed externally to the memory device in order to control the memory. To enable such access, word lines can be “fanned out” in an area adjacent to the memory array ending in conductive portions similar to stair steps arranged in a staircase pattern, as shown above. Ex. 1011, 134; ’666 patent at 5:31-40. That way, the word lines can then be separately accessed through vertical metal columns (tan) connecting the conductive steps electrically to external conductive

¹ Unless otherwise noted my citations are to page numbers in captions added by the parties.

lines (blue). Ex. 1011, 134. The metal columns are formed by first drilling channels, called “vias”, in the interlevel dielectric material covering the steps, then filling the vias with metal.

26. A potential problem with the staircase structure is the possibility of a device malfunction by way of a short-circuit “as the demand for higher storage capacity continues to increase [and] the number of vertical levels of the staircase structures also increases.” *E.g.*, ’666 patent at 5:33-36. “As a result, when applying a BEOL process to form interconnects on the staircase structures, an upper portion of the staircase structures is exposed to the BEOL process for a longer period of time than a lower portion of the staircase structures. This differential in BEOL exposure time increases the process variation of the final 3D memory device, thus introducing challenges in balancing manufacturing yield and process complexity/cost.” ’666 patent at 5:36-43.

27. For example, when upper stair steps are exposed to a BEOL (Back End Of Line) process longer during the formation of the interconnects (vertical metal columns), there is a possibility of breaking through the stair step material and forming an interconnect that extends to one or more word lines lying underneath, thereby risking electrically shorting the word lines. One way to prevent this is to increase the thickness of each stair step, which however brings the step closer to the upper word line creating the potential for electrical

breakdown (i.e., a short-circuit), even in the presence of insulating material between the word lines.

28. The semiconductor process must account for this problem to ensure short-circuits do not occur. The process and structure disclosed in the '666 patent provides one way to address this problem.

VI. Overview of the '666 Patent

29. The '666 patent discloses a process for making “a staircase structure for a memory device” and claims specific structures. '666 patent at 1:35-39, 6:1-13:8, Figs. 1-9. The structure formed by the process “provide[s] numerous benefits including, but not limited to, yield and manufacturing cost improvements.” '666 patent at 1:39-41. A specific structure disclosed and claimed includes a “staircase structure [that] includes a plurality of layer stacks, where each layer stack includes a first material layer disposed over a first portion of a second material layer.” '666 patent at 1:42-46, Fig. 8. The second material layer is made of conductive material or materials to form word lines, and the first material layer is made of insulating or dielectric material. '666 patent at 1:53-62, Fig. 8. As described above, contacts must be formed to the word lines. The second material layer in the '666 patent's structure may have two portions, such as a landing pad area where the contacts are made, as well as the rest of the second material layer that goes into the structure toward the memory cells. '666

patent at 1:46-50, 9:37-56, Fig. 8. A portion of the second material layer has a curved side surface that is in contact with a side surface of the first material layer (i.e., the insulating dielectric layer). '666 patent at Fig. 8. The second material layer is also disposed over a first portion of the first material layer of an adjacent layer of the staircase structure while a second portion of the first material layer of the adjacent layer is laterally displaced from the second material layer. '666 patent at 1:62-64, Fig. 8.

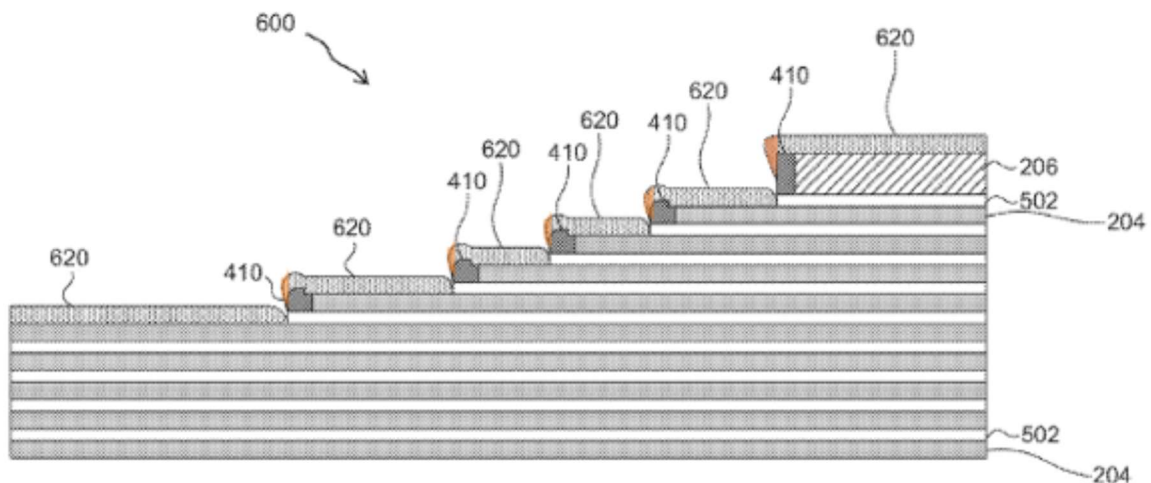
30. The process of forming the structure is described throughout the specification using the accompanying figures. To form the structure, the process begins with an alternating layer stack formed over a substrate. '666 patent at 6:1-63, 10:56-11:23, Fig. 1. At this stage, the alternating layer stack includes a plurality of layers, with each layer having an insulating layer over a sacrificial layer. '666 patent at 6:1-63, 10:56-11:23, Fig. 1. The alternating layer stack is formed into a staircase structure by repeating an etch-trim process using a mask stack. '666 patent at 6:64-7:62, 11:24-12:3, Figs. 2A-2B. After stairs have been formed, spacers are formed at a side of each layer of the staircase by conformally depositing a material on the staircase structure and then removing a portion of that material. '666 patent at 7:63-8:28, 12:4-23, Figs. 3-4. The exposed portion of the insulating layer of each step is then removed to expose a top portion of sacrificial layer underneath. '666 patent 8:29-40, 12:24-31, Fig. 5. A dielectric

material is then deposited onto the staircase structure so that the ensuing “layer 620 has poor step coverage on staircase structure 500.” ’666 patent at 8:51-52.

A POSITA would have understood what the ’666 patent meant by “poor step coverage.” *See, e.g.*, Ex. 2008 (Plummer) at 509-510. The term describes the non-conformal profile obtained on patterned surfaces when the flux of depositing species arriving at the patterned surface has both a directional and an isotropic component. Ex. 2008 (Plummer) at 544, 552, 577; *see also* Yun (Ex. 1018) at 9:41-65. Under such deposition conditions, a stair step shadows the step below it thus limiting the flux of depositing species arriving there from the gas phase.

This is particularly acute for the sidewall of all the steps. As a result, the vertical sidewall surfaces of the steps accumulate less material than the horizontal flat surfaces. Depending on the balance of fluxes (directional vs. isotropic), the sidewalls may be covered by a non-uniform or even discontinuous layer of dielectric material, with excess thickness at the upper portion of the sidewalls, thus creating an overhang. The ’666 patent shows that clearly in Figure 6, where I highlighted the overhang in orange color. ’666 patent at 8:41-9:7, 12:32-44, Fig. 6. Note that before the deposition of dielectric layer 620, the steps leading up to Figure 6 consist of a composite of materials 410 and 204 stacked on top of layer 502. In short, this approach relies on employing a (gas-phase) vapor deposition technique with both directional and isotropic flux components, where

the two flux components must be carefully balanced (optimized). Ex. 2008 (Plummer) at 552. The '666 patent contemplates multiple embodiments of the profile shape and continuity of the dielectric layer 620 to be deposited, all resulting in a dielectric layer with a curved surface at the bottom corner of each step. '666 patent at 8:41-9:7. To obtain such profiles, a POSITA must select and optimize specific deposition techniques capable of supplying both directional and isotropic fluxes of depositing species to the staircase structure, such as plasma-enhanced CVD and directional sputter deposition (PVD). Ex. 2008 (Plummer) at 547-554, 590-600.

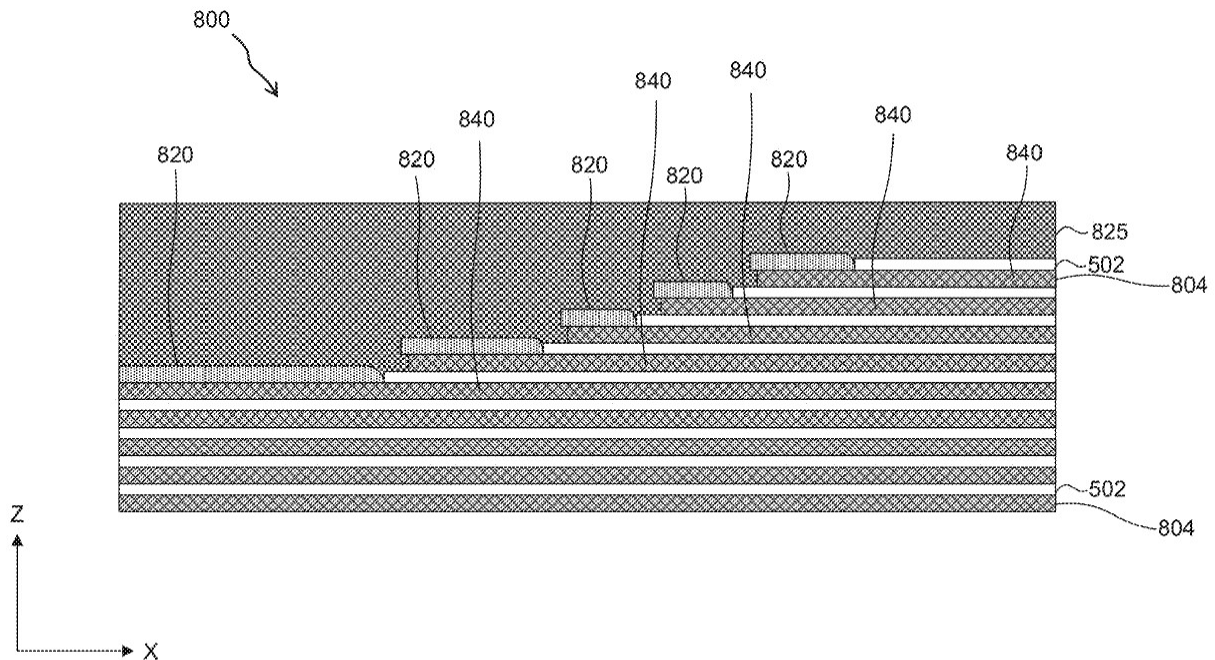


'666 patent at Fig. 6 (annotated).

31. The overhang reduces (shadows) further the delivery of additional depositing species to the bottom corner of each step from the space above the structure. As the overhang grows out, progressively less-and-less material is

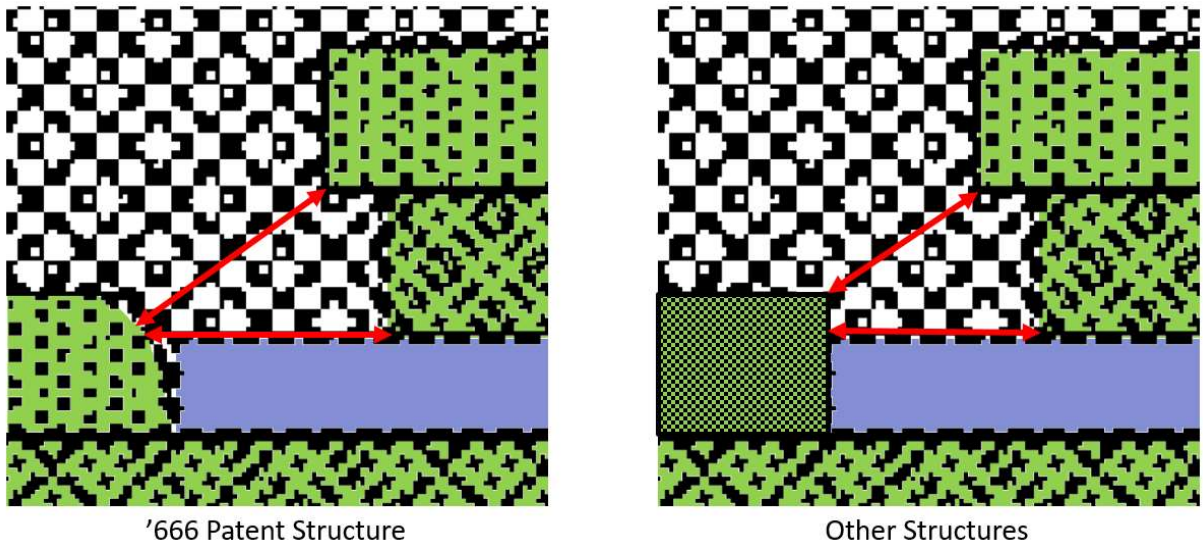
deposited directly below it, resulting in a layer (620) with a surface that curves into the corner by the step sidewall, precisely where layer 620 meets the insulating layer 502 of the respective layer stack. '666 patent at 8:41-9:7, 12:32-44, Fig. 6. In the next processing step, the spacers 410 and a portion of the dielectric layer 620 are removed to form landing pads 720 such that landing pads 720 remain in contact with the sacrificial layer 204. '666 patent at 9:8-34, 12:45-57, Fig. 7. Then, an insulating dielectric layer is formed over the entire structure and word lines are formed in the staircase structure by removing the sacrificial layer and the remaining dielectric layer 620/landing pads 720 to form recesses and then filling the recesses with one or more conducting material layers. '666 patent at 9:35-10:43, 12:58-13:8, Fig. 8.

32. At the end of this process, a structure is formed as depicted in Figure 8 below, in accordance with claim 19. Layers 804, 820, and 840 are all made of electrically conductive material and form the word lines. The word lines are thicker in the area of 820 where the landing pads are. As described above, this is where contacts will be formed to the word lines in a subsequent process that is not part of the '666 patent's disclosure.

**FIG. 8**

33. Figure 8 notes that it is depicting the x-z plane of the staircase structure. The y-axis is into and coming out of the page. To avoid confusion, I note that the axes in Figure 8 are different from the axes in the figure from page 134 of Ex. 1011, discussed earlier in my declaration. In the '666 patent, the x-axis runs along the steps toward the memory cells, where as in the figure from page 134 of Ex. 1011 shown earlier, the x-axis runs along the steps, but perpendicular to the direction from the end of the steps toward the memory cells. Of particular note, Figure 8 of the '666 patent shows that conductive material layers each have a curved side surface in the x-z plane, which is in contact with the side surface of each respective insulating layer 502. As can be seen, the

curvature in the x-z plane provides further separation between consecutive conductive material layers as compared to a structure where there was no curvature. This is depicted below, by zooming into one step. The colors used in these figures match those in the Petition and Dr. Lee's declaration, with insulating material colored blue and conductive material colored green. On the left is shown a zoom-in portion from Figure 8 of the '666 patent, while on the right I have edited the figure such that 820 has no curvature. The arrows in both Figures mark the physical separation of the landing pad from the upper word line. The corresponding distances are shorter in the picture on the right, which indicates a heightened risk of electrical shorting between the word lines in the absence of curvature. Thus, the curved side surface of the landing pad 820 illustrates an additional benefit of the '666 patent. This additional margin leads to yield and manufacturing cost improvements because of fewer short-circuit defects. *See* '666 patent at 1:34-41. The Petition argues this as well. *See* Pet. 32, 46-47, 49-50, 84-86; Ex. 1003 ¶¶ 132-133, 223-225, 417-418.



34. Additionally, in the area of landing pads 820, the combination of the conductive material(s) produces a thicker layer. This thicker portion helps prevent punch-through during the fabrication of the pad contacts thus avoiding short-circuits to word lines underneath the pads. *See* '666 patent at 5:14-43. The Petition makes this same point with respect to prior art. *See* Pet. 27; Ex. 1003 ¶ 114.

VII. Ground 1: A POSITA Would Not Have Found Claim 19 Obvious Based on Kim

A. Overview of Kim (Ex. 1005)

35. Kim describes 3D semiconductor memory devices with a “stepwise” “stacking structure” in the contact region. Kim at 1:13-35, 1:40-53, Fig. 4B. “Ones of the plurality of gate electrodes, may include a respective pad unit that comprises a step of the stepwise structure. At least one of the pad units may include a base pad and a protrusion pad on the base pad.” Kim at 1:47-50. The

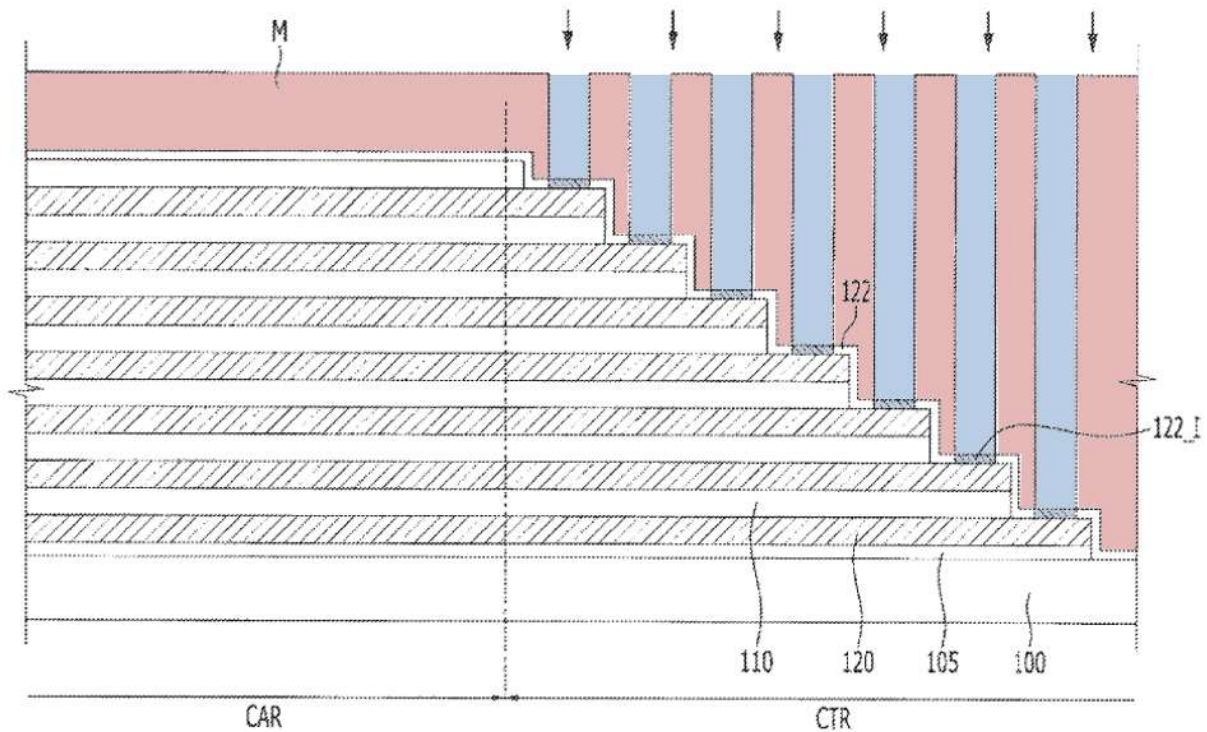
pad units are where contacts plugs are formed for electrical connection to word lines in upper layers. Kim at 9:64-10:4, Fig. 4B. Kim describes the process by which its complete stepwise stacking structure is formed, including the pad units. Steps described include the formation of the memory cells, but I omit those details here to focus on the contact region.

36. A set of alternating layers of insulating layers 110 and sacrificial layers 120 are formed on a lower insulating layer 105. Kim at 12:20-25, Fig. 10. The stepwise structure is formed by using a mask pattern to etch some material, then the mask pattern itself is etched so that more of the alternating layer structure is exposed and etched further. This process is repeated until the stepwise structure is formed. Kim at 12:43-56, Fig. 11. An auxiliary insulating layer 122 is then formed over the stepwise structure conformally covering the top and side surfaces of the stepwise structure. Kim at 9:12-20, 12:57-60, Fig. 11.

37. A photosensitive resin pattern M is then formed on the structure over the auxiliary insulating layer 122. Kim at 12:61-67, Fig. 12. The photosensitive resin pattern M is formed so that predetermined regions of auxiliary insulating layer 122 are exposed. Kim at 12:61-67, Fig. 12. The predetermined regions are referred to as region 122_I, and are for forming the protrusion pad. Kim at 12:61-67, Fig. 12. To better show this, in the figure below, I have colored in light blue the openings made in photosensitive resin pattern M, extending all the

way down to and including the corresponding exposed regions 122_I. The portion in pink is the solid photosensitive resin pattern M that remains in place during this step. Once the openings are made, predetermined ions are injected from above, as indicated by the arrows. The ions can travel freely only in the openings made in the photosensitive resin pattern M and are thus able to reach the exposed regions 122_I of the auxiliary insulating layer only at these locations. Through this process, the regions 122_I become “doped region[s]” and therefore have a different etching ratio as compared to the rest of the auxiliary insulating layer 122 that was not exposed through the mask pattern but remained covered by the solid portion of the mask pattern (pink below) and thus it was not injected with ions. Kim at 12:61-13:11 (“The doped region 122_I may have a different etching ratio from another region of the auxiliary insulating layer 122 which overlaps with the photosensitive resin pattern M.”), Fig. 12. A POSITA would understand this from these disclosures in Kim.

FIG. 12



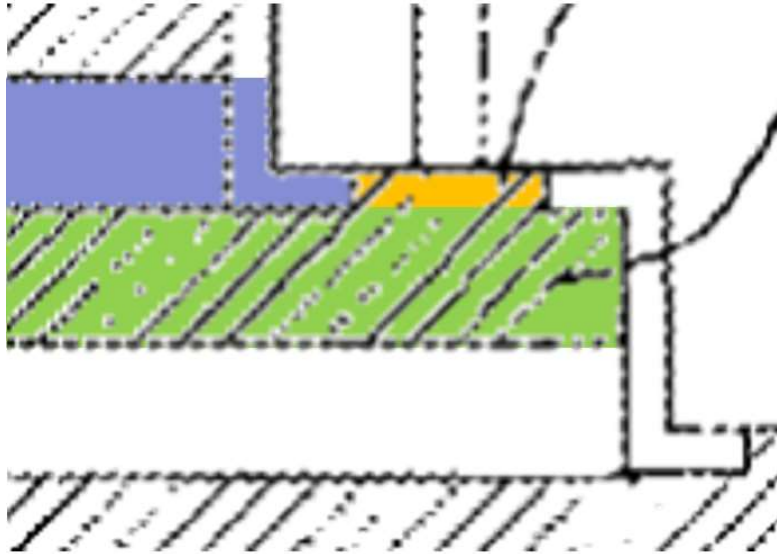
38. After the ion injection, remaining material of the mask pattern (pink above) is removed and an insulating layer 125 is placed over the stepwise structure. Kim at 13:12-20, Fig. 13. Thereafter, the sacrificial layers 120 can be removed. As a POSITA would understand from Kim, because the regions 122_I have the different etching ratio compared to the rest of auxiliary insulating layer 122, the regions 122_I can be removed either along with the sacrificial layers 120 or separately, such that there is an opening in the auxiliary insulating layer 122 only at those implanted locations termed openings 122_O in Kim. Kim at 13:51-67, Fig. 16. Furthermore, a POSITA would understand that the entirety of each exposed region 122_I would be removed during that etching process because the

ion injection process alters the etching ratio everywhere within each exposed region 122_I. This is what Kim depicts and Kim never says otherwise and a POSITA would not expect otherwise. *E.g.*, Kim at 13:55-60, Fig. 4B, Figs. 16-18. The rest of the auxiliary insulating layer 122 (i.e., the portion not exposed through the mask pattern) is not etched in this process and remains in place.

39. The area where the sacrificial layers 120 were and the openings 122_O, which Kim refers to as “gaps 260,” are then filled with conductive material to form gate electrodes 300. Kim at 13:55-67, 14:6-7. Kim refers to the portion defined by the openings 122_O and subsequently filled by conductive material as the “protrusion pad PAD_P.” The longer portion below that, which is not covered by insulating layer 120, is referred to as the “base pad PAD_B.” Kim at 9:21-28, 14:6-17, Fig. 6, Fig. 17. In this way, Kim’s pad unit PAD combines base pad PAD_B with protrusion pad PAD_P, thus increasing the thickness of the PAD in the vertical z-direction, which helps prevent damage to the PAD during the manufacturing process. Kim at 9:39-45, 11:48-52. As Kim explains, this may occur when forming the word line contact plugs 415, which can result in the contact punching through the pad region causing a short-circuit between different steps. Kim at 9:39-45, 11:48-52, Fig. 18. Furthermore, by using the mask pattern to form the PAD_P in precise locations, Kim can ensure that “the protrusion pad PAD_P [is] inside from the edge of a surface of the base

pad PAD_B to prevent the short-circuit between the pad units PAD positioned at different rows.” Kim at 9:46-49, Fig. 4B, Fig. 18; *see also* Kim at 8:1-22, 8:35-59, 10:19-48, Fig. 5, Fig. 6. Kim further notes that short-circuits are “effectively prevented” because the auxiliary insulating layer 122 remains in place. Kim at 9:50-55, Fig. 4B, Fig. 18.

40. The below figure is a zoomed in and annotated version of Kim’s Figure 4B. The colored annotations match those used in the Petition. Pet. 43-45. While Kim’s Figure 4B does not provide axes, it is clear from the axes provided on Kim’s Figures 4A, 5, 6, and 7, in the stepwise region, which Kim also calls the contact region or CTR, that the below figure zooms in on, a POSITA would readily understand it to be the x-z plane. Kim at 5:22-39, Fig. 4A, Figs. 5-7. This matches the plane of Figure 8 of the ’666 patent. As can be seen, in the x-z plane, there is no curvature depicted—it is a straight vertical surface. This is precisely what a POSITA would expect in light of the process described in Kim, which I have detailed above. The vertical (z-direction), straight contact between the annotated blue and orange occurs because the entirety of the regions 122_I are removed and the openings 122_O filled with conductive material.



41. Kim notes that what is illustrated is “the protrusion pad PAD_P has a rectangular parallele [sic] shape.” Kim at 8:29-31. Kim explains that “[t]he protrusion pad PAD_P may have an island shape with respect to the one surface of the base pad PAD_B.” Kim at 8:23-26. This is shown in Kim’s Figure 6, where “the protrusion pad PAD_P ... [is] positioned inside from four edges E1, E2, E3, and E4 of the surface of the base pad PAD_B.” Kim at 10:19-48, Fig. 6. Regardless of whether PAD_P is an island or not, Kim’s Figure 4B would look the same because the cut is taken where contact plug 415 contacts PAD_P. Kim at 9:64-10:4, Fig. 4B, Figs. 5-6. A POSITA would understand from Kim’s disclosure that the difference in forming PAD_P as in Figure 5 versus forming PAD_P as in Figure 6 would be a change to the shape of the openings in the photosensitive resin pattern M. I illustrate this using a cropped version of Kim’s Figure 4A, below. Employing the same colors as in Paragraph 37 above where I

illustrated this in the x-z plane using Kim's Figure 4B, the solid part of photosensitive resin pattern M is shown in pink while the openings are shown in light blue. Figure 4A and the colored figures below are in the x-y plane, looking from above, down onto the stepwise structure. On the left, the openings extend the full width of the steps in the y-direction and would result in PAD_Ps that extend the full width of the steps in the y-direction, as in Kim's Figure 5. On the right, the openings are shorter in the y-direction and would result in PAD_Ps that are islands on stair steps (PAD_B) as in Kim's Figure 6. I have included Figures 5 and 6 below the annotated figures, but note that Figures 5 and 6 each show two sets of steps, whereas I have only depicted one set of steps in the colored drawings as indicated by the dotted lines annotated on Figures 5 and 6.

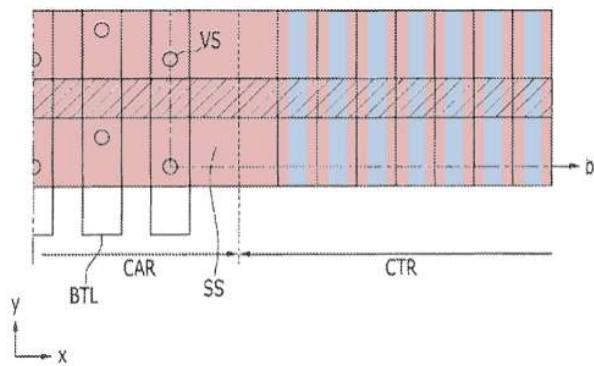


FIG. 5

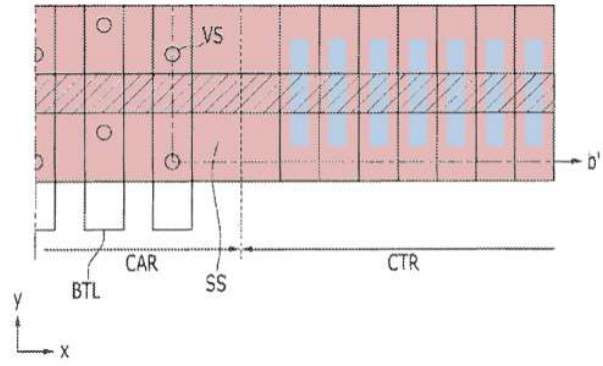
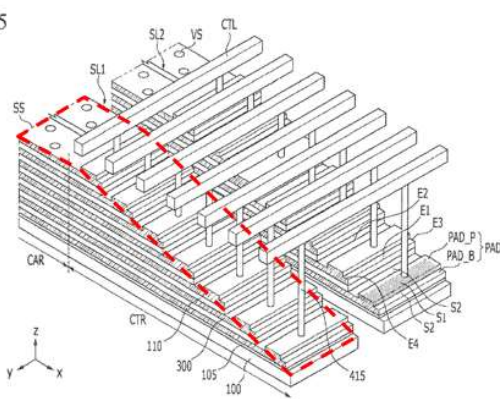
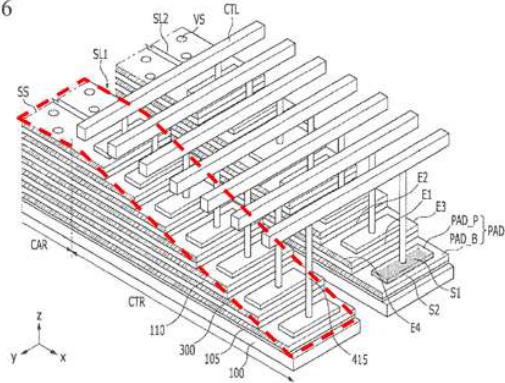
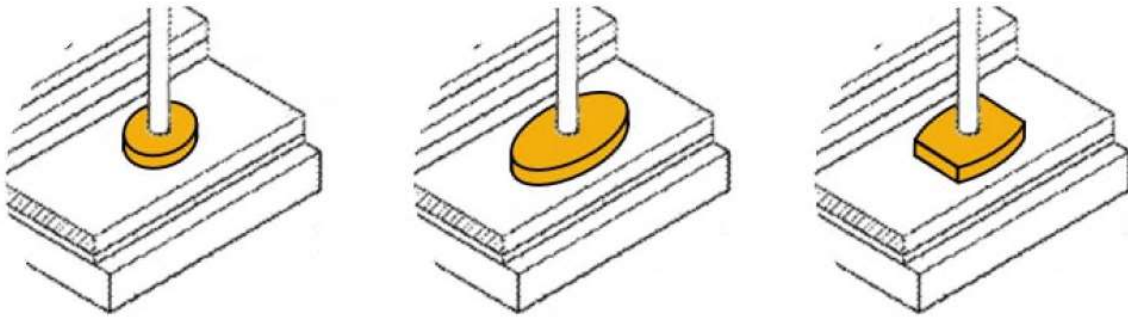


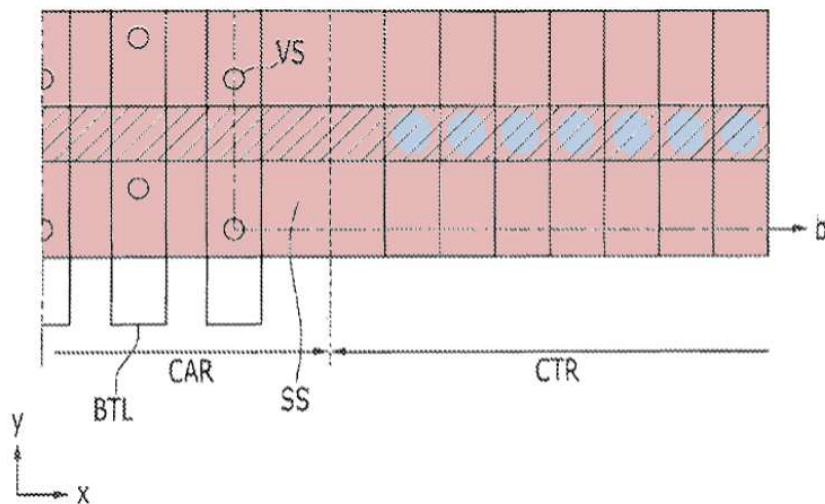
FIG. 6



42. Kim also explains that, “in some embodiments,” PAD_P “may have a shape including a curved surface based on a virtual rectangular parallelepiped shape, a cylindrical shape, or any shape.” Kim at 8:32-34. The Petition and Dr. Lee provide the below figures as depicting such shaped PAD_Ps. Pet. 51; Ex. 1003 ¶¶ 239-241. But neither explains whether or why a POSITA would want to use any of these shaped PAD_Ps.

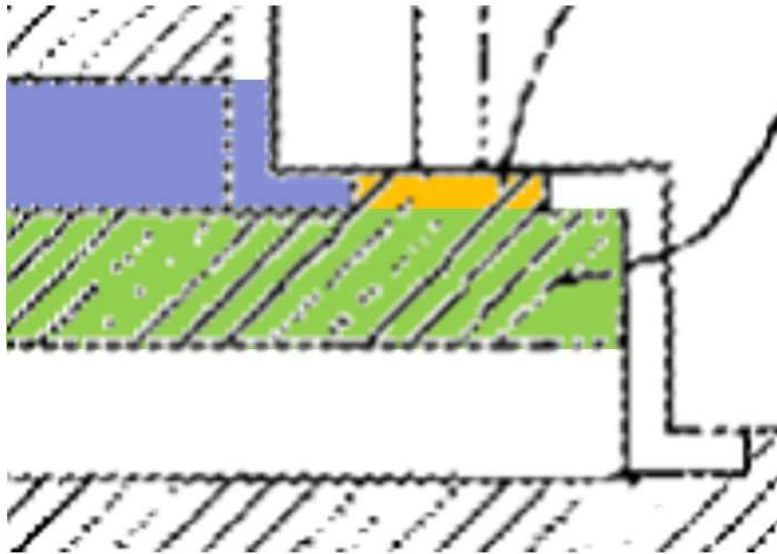


43. Assuming the above shapes would be used by a POSITA, the PAD_P would be formed by changing the photosensitive resin pattern M such that openings were not rectangular, but instead had the shapes above. *See Ex. 1003 ¶ 248.* As I did above in Paragraph 41, I depict this again with the solid part of photosensitive resin pattern M is shown in pink while the openings are shown in light blue, to form the smaller circular pad on the left in the Petition's figures.



44. Regardless of the shape of the openings formed in the photosensitive resin pattern M, the resulting structure will look the same in the x-z plane of Kim's Figure 4B, which I again depict below (same as in the discussion of

Paragraph 40). The only difference would be the width of the orange portion in the x-direction (left to right in the figure below). There will always be vertical (z-direction), straight contact between the annotated blue and orange because the entirety of the regions 122_I are removed and the openings 122_O filled with conductive material.



45. While Kim refers to PAD_P “including a curved surface,” Kim at 8:29-34, a POSITA would understand that there is no curvature in the x-z plane, because in cross-sectional view it will always look as it does above, i.e., with straight vertical sidewalls. In one explanation, the Petition and Dr. Lee appear to treat the curved areas of the cylindrical PAD_Ps in top view, depicted above in connection with my Paragraph 42, as the “curved side surface” in the ’666 patent. If that is what Kim refers to, then there will not be a curvature in the x-z plane to

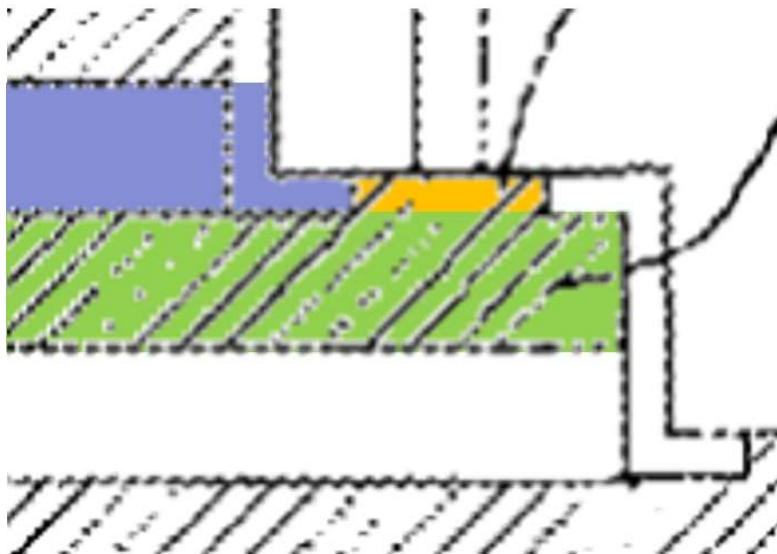
the contact between the annotated blue and orange in the above figure. This does not satisfy the claimed “curved side surface.”

B. Kim, Alone or in Combination, Does Not Disclose “curved side surface in contact with a side surface of the insulating layer”

46. In my opinion, Kim does not teach nor render obvious claim 19.

Specifically, a POSITA would not arrive at a structure “wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer,” as recited in claim 19, based on Kim.

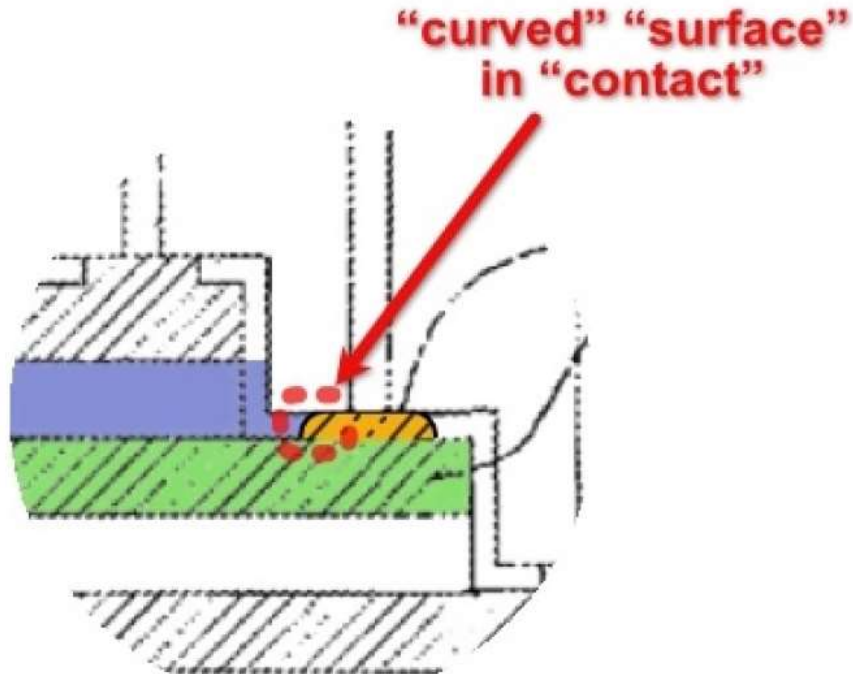
47. As explained above, Kim does not show a “curved side surface in contact with a side surface of the insulating layer” in its figures. Instead, there will always be vertical straight contact between the annotated blue and orange regions because the entirety of the regions 122_I are removed and the openings 122_O are filled with conductive material, as depicted again below. Dr. Lee depicts this the same as I do. Ex. 1003 ¶ 199.



48. But then Dr. Lee asserts that “Kim also teaches that the ‘side surface’ of its ‘second portion of the conductive layer’ that is in ‘contact’ with its ‘insulating layer’ is (or at the very least obviously can be) ‘curved.’” Ex. 1003 ¶ 200. I disagree.

49. Dr. Lee points to the discussion of the shape of Kim’s PAD_P, which I thoroughly discussed above, as something a POSITA would recognize as including “configurations where the sides of the protrusion pads are curved, particularly to optimize electrical connectivity and mitigate stress at material interfaces.” Ex. 1003 ¶ 201. He also asserts that “[s]uch curved configurations are routine in the fabrication of three-dimensional memory devices, as further supported by references like Park, Yun, and Nam.” Ex. 1003 ¶ 201. He then asserts that “a POSITA would have understood that this teaches a variety of different protrusion pad PAD_P shapes, many of which have the type of ‘curved’ side surface Claim 17 requires. This includes, for instance, pads with curved sides when viewed in cross-section or pads with curved sides when viewed above.” Ex. 1003 ¶ 202. Finally, he asserts that “a POSITA would have understood that when Kim references a ‘curved surface based on a virtual rectangular parallel[] shape,’ PAD_P would obviously be shaped in the manner shown in the demonstrative below,” which he says would be formed “following Kim’s teachings.” Ex. 1003 ¶ 203. I have reproduced Dr. Lee’s demonstrative

below, showing a curvature in the x-z plane, which he also refers to as “when viewed in cross-section.”



50. Dr. Lee is wrong that the above shaped PAD_P could result from following Kim’s process. For the reasons I have already explained, there will always be vertical (z-direction), straight contact between the annotated blue and orange regions in the x-z plane (or as Dr. Lee says, “when viewed in cross-section”) because the entirety of the regions 122_I are removed leaving behind openings 122_O with straight vertical sidewalls. These openings 122_O are filled subsequently with conductive material retaining the straight vertical sidewall shape. Dr. Lee provides no explanation at all for how sidewall curvature in the z-direction could be formed following Kim’s process. And for all the

reasons I have already provided, it could not be formed as Dr. Lee depicts.

Furthermore, this is not the “curved surface” that Kim refers to, as noted above in Paragraph 45.

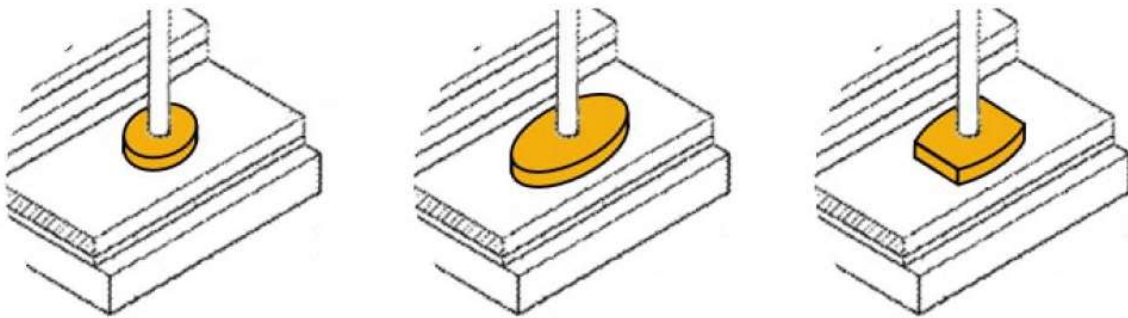
51. With nothing in Kim showing the made-up shape that Dr. Lee draws, Dr. Lee asserts that “a POSITA would have been motivated to employ a contact pad with curved side surfaces when implementing Kim.” Ex. 1003 ¶ 219. Dr. Lee provides three purported reasons why. Ex. 1003 ¶¶ 220-221, 223. In brief, Dr. Lee asserts (1) Kim already contemplates a curved side surface; (2) this type of pad was well known in the art; and (3) doing so would reduce the risk of short-circuit in Kim. I disagree with all three assertions. I address (1) below in this section, (2) in Section VII.C.2, and (3) in Section VII.C.1.

52. Dr. Lee asserts that “Kim itself already contemplates that its pad can have a “curved surface.” Ex. 1003 ¶ 220; *see also* Ex. 1003 ¶ 204. But as I explained in Paragraphs 46-51, a POSITA would not understand Kim to be referring to a curved surface in the x-z plane as in the claimed structure.

53. Dr. Lee states that “a POSITA would have understood that Kim’s ‘cylindrical[ly]’-shaped protrusion pads PAD_P also include the type of ‘curved’ surface that Claim 17 requires.” Ex. 1003 ¶ 239. I disagree.

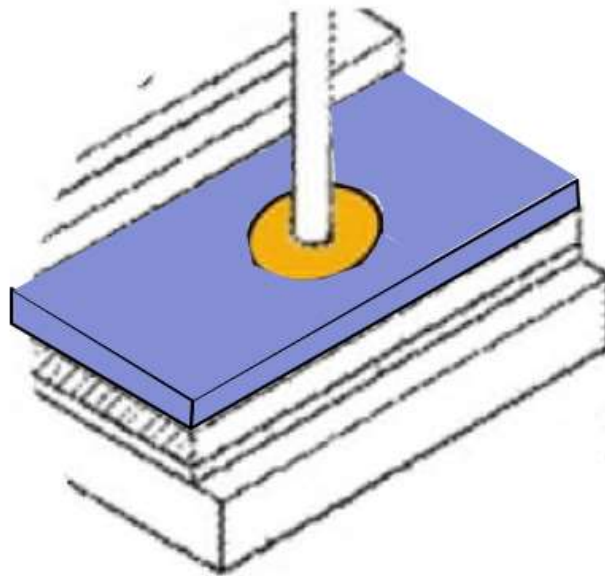
54. As described above, Dr. Lee relies on the below figure as showing the “cylindrical” contact pads that he asserts could be used. Ex. 1003 ¶¶ 241-

242. What Dr. Lee fails to depict is what happens to the auxiliary insulating layer 122 when a PAD_P like the ones below is formed.



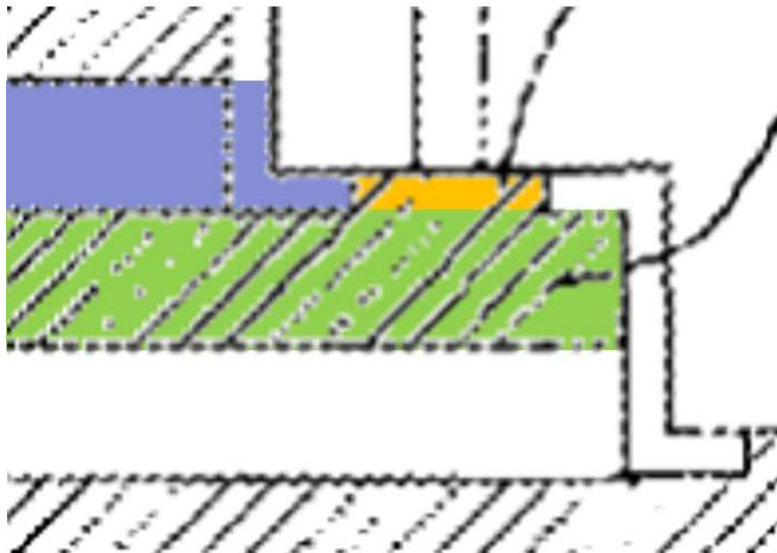
55. Using the PAD_P on the left in the above figures as an example, and focusing just in the area of one of Kim's PADs, the auxiliary insulating layer 122 would entirely surround the PAD_P as shown below. I have used the blue color to show this because the Petition relies on auxiliary insulating layer 122 as part of the claimed "insulating layer" and depicts it in the same blue. Pet. 43-45. Kim explicitly describes this when discussing Figure 6, which the above figures are based on (Ex. 1003 ¶ 241). Kim explains that PAD_B has "the first region S1 contacting the protrusion pad PAD_P," meaning the portion of PAD_B underneath PAD_P, and has "the second region S2 other than the first region S1," meaning everywhere on the step surface not covered by PAD_P. Kim at 10:30-32, Fig. 6. Kim then explains that "[t]he auxiliary insulating layer 122 may contact the second region S2 of the surface of the base pad PAD_B" Kim at

10:49-51. A POSITA would understand this description to look as below. The same is generally true for each of the PAD_P shapes depicted above.



56. As can be seen, when using a PAD_P shaped as Dr. Lee proposes, there is no contact between the PAD_P (what the Petition relies on as the “second portion of the conductive layer” in claim 19) and “a side surface of the insulating layer” as required by claim 19. Instead, PAD_P contacts the purported insulating layer at an internal or inner surface of it because it is completely surrounded by the insulating material. Rather than depicting this view, Dr. Lee only shows the side view. Ex. 1003 ¶ 244. I note however that in the demonstrative Dr. Lee provides between paragraphs 244 and 245 of his declaration, the PAD_P in the far right image showing the side view has an unexplained shape. It is unclear to me what the small rectangles on either side are meant to be. Further, when I

zoom in, there appears to be a curvature shown in the x-z plane, but it is unclear if this is intentional or not as it is unexplained. As I explained above in Paragraph 44, regardless of the shape of the openings formed in the photosensitive resin pattern M, the resulting structure will look the same in the x-z plane of Kim's Figure 4B, which I again depict below. The only difference would be the width of the orange portion in the x-direction (left to right in the figure below). There will always be vertical (z-direction), straight contact between the annotated blue and orange regions because the entirety of the injected regions 122_I are removed and the openings 122_O are filled with conductive material. This does not satisfy the claimed "curved side surface."



57. While Dr. Lee states that "a POSITA also would have been motivated to employ this shape [the one shown above his paragraph 245] and would have expected to succeed when doing so," Ex. 1003 ¶ 245, he provides no

explanation for why a POSITA would use these shapes. The shape of PAD_P in Kim is a function of Kim's photosensitive resin pattern M and would be selected depending on margins associated with landing contacts and contact shape. The shape of PAD_P will not further improve the short-circuit problem beyond what Kim's offset from the edges of PAD_B already does, which I explain in the next section.

C. Kim, Alone or in Combination, Does Not Teach nor Render Obvious a “curved side surface in contact with a side surface of the insulating layer”

1. A POSITA Would Not Have Been Motivated to Modify Kim to Reduce the Risk of Short-Circuit

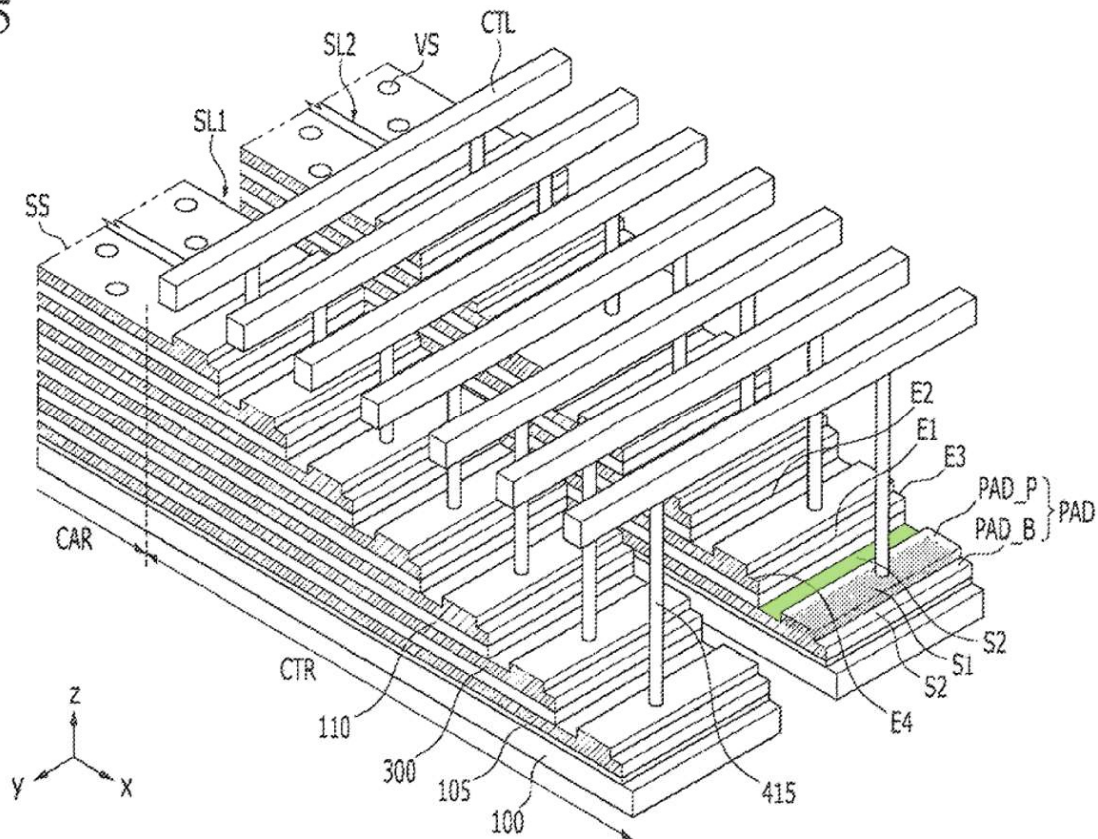
58. Dr. Lee asserts that “a POSITA would have recognized that using a ‘curved’ side surface with Kim’s pads would have improved Kim by increasing the minimum distance between the pad and adjacent conductive layers, thereby reducing the risk of short circuit.” Ex. 1003 ¶ 223. This is the only reason given for why a POSITA would change Kim’s process. But a POSITA would not have been motivated to change Kim’s process to reduce the risk of short-circuit because Kim already accounts for the risk of short-circuit in multiple but different ways. Thus, Dr. Lee and the Petition provide no reasons at all for why a POSITA would modify Kim’s process to have the claimed “curved side surface.”

59. In my opinion, a POSITA would not be motivated to modify Kim “by increasing the minimum distance between the pad and adjacent conductive

layers, thereby reducing the risk of short circuit.” Ex. 1003 ¶ 223. This is because Kim already has numerous features that address and solve this very same short-circuit problem.

60. I explained Kim’s process above. As part of its process, Kim explains that the protrusion pad PAD_P is formed “inside from the edge of a surface of the base pad PAD_B to prevent the short-circuit between the pad units PAD positioned as different rows.” Kim at 9:46-49, Figs. 5-9. What would be apparent to a POSITA from this process, and what is depicted in Kim, is that Kim’s process ensures that the PAD_P is set off from the adjacent conducting layer in the step direction (x-direction in the figure below) to avoid a short-circuit. The set off has been highlighted in green in the figure below. As I explained above, this set off is created because Kim uses photosensitive mask pattern M to precisely control the location of the PAD_Ps. By providing the green offset, Kim’s process already increases the minimum distance between the pad and adjacent conductive layers to prevent a short-circuit. Kim’s process further deals with this by ensuring that pad unit’s of adjacent conductive layers do not overlap. Kim at 7:63-67.

FIG. 5

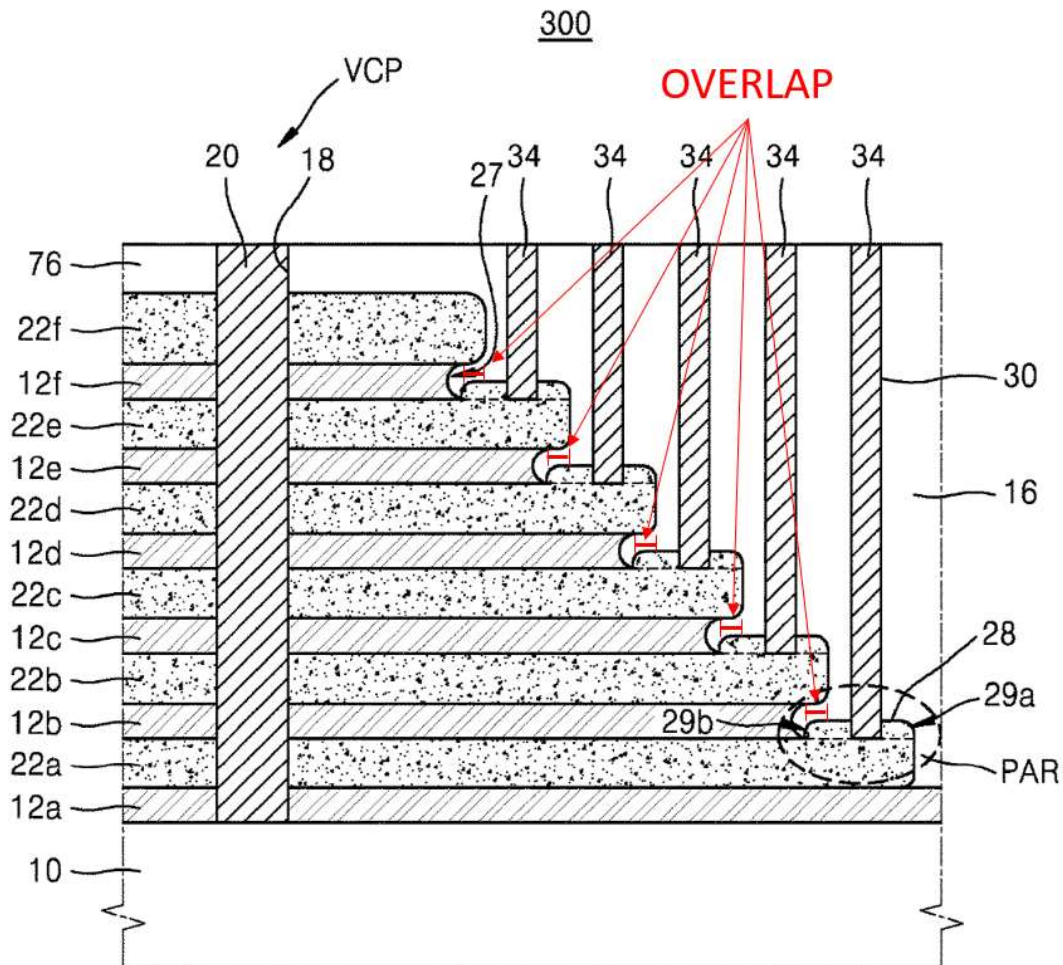


61. A POSITA would know that this offset could be precisely controlled for these types of devices. Kim itself makes this clear by describing that the PAD_Ps could be made narrower, showing the accuracy of the mask. Kim at 11:57-12:11, Fig. 9. I note that Dr. Lee points to this same disclosure as an explanation for why a POSITA would want to round the sides of the PAD_P. Ex. 1003 ¶ 224. But Kim merely says that differing widths may be used. Kim never suggests that a width so large as to erase the green offset such that short-circuits are again a problem should be used and a POSITA would not read Kim in such a way.

62. Dr. Lee only points to Park as teaching that rounded pad side surfaces help prevent short-circuits. Ex. 1003 ¶ 224. But Park and Kim are fundamentally different in this regard such that a POSITA would not look at Park as teaching something useful in Kim's process.

63. With respect to Park, Dr. Lee mixes his discussion and explanation of the reference. Park describes an embodiment in connection with Park Figure 5, and a different embodiment in connection with Park Figure 7. In describing Park, Dr. Lee includes discussion regarding both embodiments. *See* Ex. 1003 ¶¶ 129-133, 205-208, 224, 236. Dr. Lee never includes Park Figure 5 despite citing discussion about it. He instead applies that discussion to Park Figure 7 without explanation. This matters because, according to Park, the Figure 7 embodiment “do[es] not have a stepped form.” Park at 9:50-59. Kim, on the other hand, does have a stepped form. Dr. Lee provides no explanation for why a POSITA would look to a reference without a stepped form and be motivated to apply it to Kim, which does have a stepped form. Below is Park's Figure 5 embodiment, which has a stepped form, which I have annotated to note the overlap between Park's pad regions (PAR). This overlap creates a higher risk of short-circuit in Park's pad regions and is part of the reason why Park uses a process with rounded pad regions. *See, e.g.*, Park at 7:17-22.

FIG. 5



64. As explained above, Kim does not have this overlap because it uses the photosensitive resin pattern M to precisely control the location of its PAD_P to avoid overlap and to avoid this short-circuit problem. *See, e.g.*, Kim at 7:63-67 (“The pad unit PAD and the adjacent pad unit PAD may not overlap with each other.”). Park, by contrast, does not use a mask pattern to control the location of its pad regions.

65. As noted above, Park itself explains that the Figure 7 embodiment is similar to the Figure 5 embodiment with the exception that the stacked layers “do not have a stepped form but are inclined.” Park at 9:53-58. As shown in Figure 7, the lack of steps means a lack of pad regions for connection of individual word lines. In other words, in Figure 7, aside from the single contact 84 shown, the other conductive layers 72c-72f are not used as word lines. A POSITA would not find Park’s Figure 7 embodiment suitable for 3D memories like those in Kim or the ’666 patent. For example, as the ’666 patent explains, “[a]s the demand for higher storage capacity continues to increase, the number of vertical levels of the staircase structures also increases.” ’666 patent at 5:31-36. In other words, to increase the density of 3D memories, more stairs are desirable. Park’s Figure 7 embodiment does not have this feature. Furthermore, like Park’s Figure 5 embodiment, Park’s Figure 7 embodiment also does not use a mask pattern to control the location of its one pad region. Because Kim’s process forms its PAD regions in a completely different way, a POSITA would understand that (a) Kim does not need rounded sides for the reasons Park explains and (b) Park’s pad regions could not be swapped into Kim’s structure without completely changing Kim’s process, which would eliminate numerous stated benefits in Kim,

including this short-circuit problem that Kim solves through its process. Dr. Lee did not provide any reason or motivation for a POSITA to do so.²

66. Another way that Kim addresses short-circuits is that Kim retains “auxiliary insulating layer 122 positioned between the adjacent protrusion pads PAD_P positioned at different rows.” Kim at 9:50-55, Fig. 4B. As Kim explains, because of this, “the short-circuit between the pad units PAD may be effectively prevented.” Kim at 9:50-55, Fig. 4B. As I explained above, this is a result of Kim’s process using photosensitive resin pattern M with the green offset I depicted above. Because only the specific regions 122_I in Kim are subjected to the ion injection process, the other portions that remained covered by the solid (pink) part of the photosensitive resin pattern M are unaffected and remain in place and provide insulation between the PADs in Kim.

67. Should short-circuits between PAD regions still be a concern to a POSITA, Kim provides a third way to prevent short-circuits. As Kim explains, if due to the PAD_P a minimum distance rule would be violated, the “z-direction

² The same is true of Park’s Figure 8 embodiment, which Dr. Lee and the Petition occasionally cite as well. Like Park Figure 7, Park Figure 8 also does not have a stepped structure and has only a single contact to a single pad. Park at 11:6-13, Fig. 8.

thickness of the insulating layer 110 may be larger than the minimum distance in the z-direction between two adjacent pad units PAD to effectively prevent a short-circuit between the two adjacent pad units PAD.” Kim at 8:66-9:11. What this means is, if a POSITA is making Kim’s device and has a short-circuit problem, Kim instructs the POSITA to slightly thicken the insulating layers as a further measure to avoid short-circuits.

68. In my opinion, because Kim already provides its process three different ways to avoid short-circuits between adjacent PAD regions, a POSITA would not be motivated to change Kim in order to solve a problem Kim already solved. A POSITA especially would not do so based on Park, which is the only reference Dr. Lee cites for his opinion, because Park’s structures (Figure 5 and Figure 7) are formed by a different process that has a more problematic structure for short-circuits and does not provide ways to avoid the short-circuit like Kim already does.

2. A POSITA Would Not Have Modified Kim In View Of Park, Yun, Or Nam

69. As explained in the previous section, a POSITA would not be motivated to modify Kim to avoid short-circuits. Dr. Lee’s only other explanation is that “this type of pad was also well known in the art as shown, not only by Kim, but also by Park, Yun, and Nam.” Ex. 1003 ¶ 221; *see also* Ex. 1003 ¶ 204. But this is wrong too. First, as I explain further below, Yun does not

teach a pad region with curved side surface that could contact the insulating layer of the layer stack. Thus, a POSITA modifying Kim according to Yun's teaching would not arrive at the claimed structure. Second, given that Dr. Lee and the Petition put forward only two references that purportedly show a curved pad region in the correct location, this does not prove that such structures were well known to a POSITA. For example, neither Dr. Lee nor the Petition point to textbooks showing such a structure that may suggest that a POSITA would have been well aware of such structures. Third, semiconductor processes are not so simple that a POSITA simply sees a particularly shaped structure and substitutes it into a structure made by a different process. The pad regions of each of Park, Yun, and Nam are formed through processes significantly different from Kim's. I address these differences below for each reference.

70. As to all three references, Dr. Lee only says that “[a] POSITA would have recognized that this process could be readily adapted to form a curved opening that surrounds a curved contact pad.” Ex. 1003 ¶ 234. His explanation is that “the ion implantation step shown in Figure 12 of Kim would simply be tailored to form a ‘doped region 122_I’ with curved rather than straight sides. The rest of the process would proceed in the same way, resulting on contact pads located within an opening 122_O in insulation layer 122 with curved sides.” Ex. 1003 ¶ 234. Notably, Dr. Lee never explains how the ion implantation step could

be tailored in this way. Indeed, it could not for the reasons I explained in connection with describing Kim's process. Specifically, Kim creates openings in the photosensitive resin pattern M so that the entire region 122_I is doped and subsequently removed. Rounded corners cannot be formed in this process. And because the pad regions of each of Park, Yun, and Nam are formed through processes significantly different from Kim's, a POSITA would not modify Kim's process absent very compelling reason, which Dr. Lee and the Petition fail to give.

Park

71. Part of the reason why a POSITA would not be motivated to modify Kim to improve short-circuits in the way suggested by Park is because the processes in Kim and Park are very different. Dr. Lee does not address this.

72. Dr. Lee notes that Park also uses ion implantation, Ex. 1003 ¶¶ 235-236, but the ion implantation in Park is not what creates the rounded sides. And so Park does not teach a POSITA a way to tailor the implantation step of Kim as Dr. Lee states. Ex. 1003 ¶ 234.

73. Instead, as Dr. Lee admits, Park uses oxidation and ion implantation to arrive at rounded sides. The rounded shape is a result of the oxidation and not the ion implantation. As Park explains, "[a]s shown in FIG. 6C, an additional insulating layer 40 is formed by oxidizing surfaces and side surfaces of the

stepped sacrificial layer patterns 14a through 14f that are externally exposed.

The additional insulating layer 40 may be formed by thermally oxidizing the surfaces and the side surfaces of the sacrificial layer patterns 14a through 14f. ...

One end of the additional insulating layer 40 may be rounded by an oxidation process.” Park at 8:28-38, Fig. 6C. As can be seen in Park Figure 6C the rounded shape already appears before any ion injection occurs, which happens in a subsequent step. Park at 8:43-51, Fig. 6D.

74. Dr. Lee does not explain how a POSITA would add this oxidation step to Kim's process to create rounded sides, let alone why a POSITA would do so. In my opinion, a POSITA would not be able to substitute Park's additional insulating layer 40, formed through thermal oxidation, into Kim's process and would not be motivated to do so. In Park, the additional insulating layer 40 is grown through thermal oxidation on sacrificial layer 14a-14f. Because of the intervening insulating layers 12b-12f, the additional insulating layer 40 is discontinuous, grown only on the tops and sides of the sacrificial layers. Park at 8:28-38; Fig. 6A-6C. The discontinuity is necessary in Park because the entirety of the additional insulating layer 40 becomes conductive after subsequent processing steps. Park at 8:43-9:21, Fig. 6F. By contrast, Kim forms a continuous auxiliary insulating layer 122 over its entire stepped structure. Kim at 12:58-60, Fig. 11. This continuous structure is one of the key features in Kim.

As Kim explains, “the short-circuit between the pad units PAD may be effectively prevented through the auxiliary insulating layer 122 positioned between the adjacent protrusion pads PAD_P positioned at different rows. The semiconductor memory device according to same [sic] embodiments of the inventive concepts may have enhanced reliability.” Kim at 9:50-55. To achieve a rounded side as Dr. Lee suggests, a POSITA would have to change Kim’s process at least by not forming the auxiliary insulating layer 122 and not using the photosensitive resin pattern M to precisely locate its PAD_P, two key features of Kim’s process. Moreover, this would eliminate Kim’s stated enhanced reliability and other advantages described above. Removing those steps would effectively abandon Kim’s process, as they are key parts of the process, and use Park’s process from the start. There is no reason for a POSITA to modify Kim in this way, and Dr. Lee does not provide any explanation.

Yun

75. Dr. Lee provides no explanation at all for why a POSITA would look to Yun to modify Kim. While Dr. Lee states “numerous prior art references similarly employ ion implantation to form contact pads with rounded or curved sides,” he does not cite Yun as one of them. Ex. 1003 ¶ 235. Yun does not mention ion implantation. Dr. Lee’s only purported basis is that that curved structures were well known, Ex. 1003 ¶¶ 221-222, 228, but as noted above Yun

does not even disclose a curved surface that would lead to claim 19's structure, and Dr. Lee has not demonstrated that such structures were so well known that a POSITA would be able to simply modify Kim's process to use them. In my opinion, a POSITA would not have been motivated to modify Kim's process to try and use pad structures from Yun.

76. Furthermore, in every embodiment of Yun, the side of pads 120 that are closest to the interlayer insulating layers 102 are not rounded or curved. As Yun explains, the "inner side surface of the protrusion part 65 may have a flat surface," while only the "outer side surface," away from the interlayer insulating layers 102 "may be rounded." Yun at 8:31-40, Fig. 3, Figs. 5A-5F. Furthermore, in every embodiment of Yun, the inner side surface of the pads 120 does not contact the interlayer insulating layer 102. A POSITA would therefore understand that the portion of Yun's pads that Dr. Lee says Kim could simply be tailored to use would not have "a curved side surface in contact with a side surface of the insulating layer," as recited in claim 19.

77. While Dr. Lee has pointed to no motivation to do so, a POSITA looking to use Yun's pad structures in Kim's process would recognize the differences in those processes and that significant changes would be needed to Kim. Yun's pad structures are formed thicker on the stepped area to provide "a process margin for forming contact plugs 150 having different vertical heights."

Yun at 7:27-33. Kim already includes PAD_P for this very reason. Kim at 11:48-50. Thus, a POSITA would have no reason to use Yun's pad structures in place of Kim's. Furthermore, Yun does not use a mask pattern to create its pad structures, and therefore cannot precisely control their location and provide margin against short-circuits in the same way that Kim already does. In my opinion, a POSITA would not be motivated to make such changes to Kim, which would negate some of Kim's advantages, as I have discussed above, without any benefit.

Nam

78. Dr. Lee provides no explanation at all for why a POSITA would look to Nam to modify Kim. While Dr. Lee notes that Nam also uses ion implantation, Ex. 1003 ¶¶ 235, 237, the ion implantation in Nam is very different from that in Kim, as is the rest of Nam's pad formation. And so Nam does not teach a POSITA a way to tailor the implantation step of Kim as Dr. Lee states. Ex. 1003 ¶ 234.

79. Nam purports to form a convex, or bull nose shaped, pad regions by injecting impurities into a sacrificial layer to create a damaged region, and then enlarging the damaged regions through heat. Nam at [0099]-[0100], Fig. 32, Fig. 33, Fig. 34, Fig. 36. Thus, in Nam, ion injection is performed such that impurities are implanted toward the center of the sacrificial layer in the area

where the pads are formed. Nam at [0099], Fig. 33. The curvature in Nam supposedly results from the application of heat when forming another layer causing diffusion of the impurities and an increase in the volume of the damaged regions. Nam does this because it wants to increase the size of the pad regions to avoid the problem of the contact punching through the pad causing a short-circuit between gate electrode layers. Nam at [0044]-[0045], [0065], [0107]-[0108], Fig. 7, Figs. 8A-8B, Fig. 37, Fig. 39. But as can be seen by comparing Nam's Figures 34, 36, and 37, the increase in the pad size has the effect of pushing the pads closer together. Decreasing that distance could lead to a short-circuit defect between gate electrode layers. I also note that the Petition appears to argue that a POSITA would have understood that Nam's process of forming its pad regions is not very precise, because the Petition states that "a range of structures will result" "in both somewhat larger and somewhat smaller pads," such extending "beyond the bounds shown in Figure 8A into layer 248 by some amount." Pet. 68-69. If this is true, then there is even more potential for a short-circuit defect between gate electrodes to occur because the enlarged pads would be brought even closer to pads in other layers. I further note that Nam does not provide any description or way to mitigate a potential short-circuit defect between gate electrode layers.

80. Nam's process described in the last paragraph is different from Kim's process. Rather than performing ion injection on the sacrificial region in

hopes of enlarging it, Kim performs ion injection through the photosensitive resin pattern M into the auxiliary insulating layer 122 that was formed on top of the sacrificial layer. As I explained above, this precisely controls the location of Kim's PAD_P. A POSITA would see Kim's existing process as more controllable and less likely to lead to defect than a process like Nam's which even the Petition explains can result in a range of structures if followed. Moreover, as I already explained, Kim's PAD_P already solves the very problem of punch through in forming contacts that Nam tries to solve with its enlarged pad regions. Kim at 7:58-8:28, 11:48-56. In my opinion, a POSITA would not be motivated to make such changes to Kim, which would negate some of Kim's advantages, as I have discussed above, without any benefit.

81. Thus, in my opinion, a POSITA would not modify Kim for any of the reasons suggested in the Petition and by Dr. Lee. As Kim does not show the claimed "curved side surface" on its own, nor render it obvious, a POSITA would not have found claim 19 obvious with respect to Ground 1.

VIII. Ground 2: A POSITA Would Not Have Found Claim 19 Obvious Based on Nam

82. The embodiment of Nam primarily relied on in the Petition forms at "step structure" alternating sacrificial layers 220 (sacrificial layers 221 to 228) and insulating layers 240 (insulating layers 241 to 248). Nam at [0098]; *see also* Nam at [0097] (explaining that figures 30 to 39 describe the method of

manufacturing for the structures in figures 7 and 8). After the step structure is formed, “first interlayer insulating layer 271” is formed over the top and side surfaces of the structure. Nam at [0098], Fig. 31. I note that Dr. Lee and the Petition also refer to this “interlayer” insulating layer as “adjacent insulating layer 271,” though Nam itself never describes it this way. Pet. 60; Ex. 1003 ¶ 286. Below I have annotated Nam’s Figure 7 and Figure 8 with Nam’s insulating layers 240 in blue, and first interlayer insulating layer 271 in yellow.

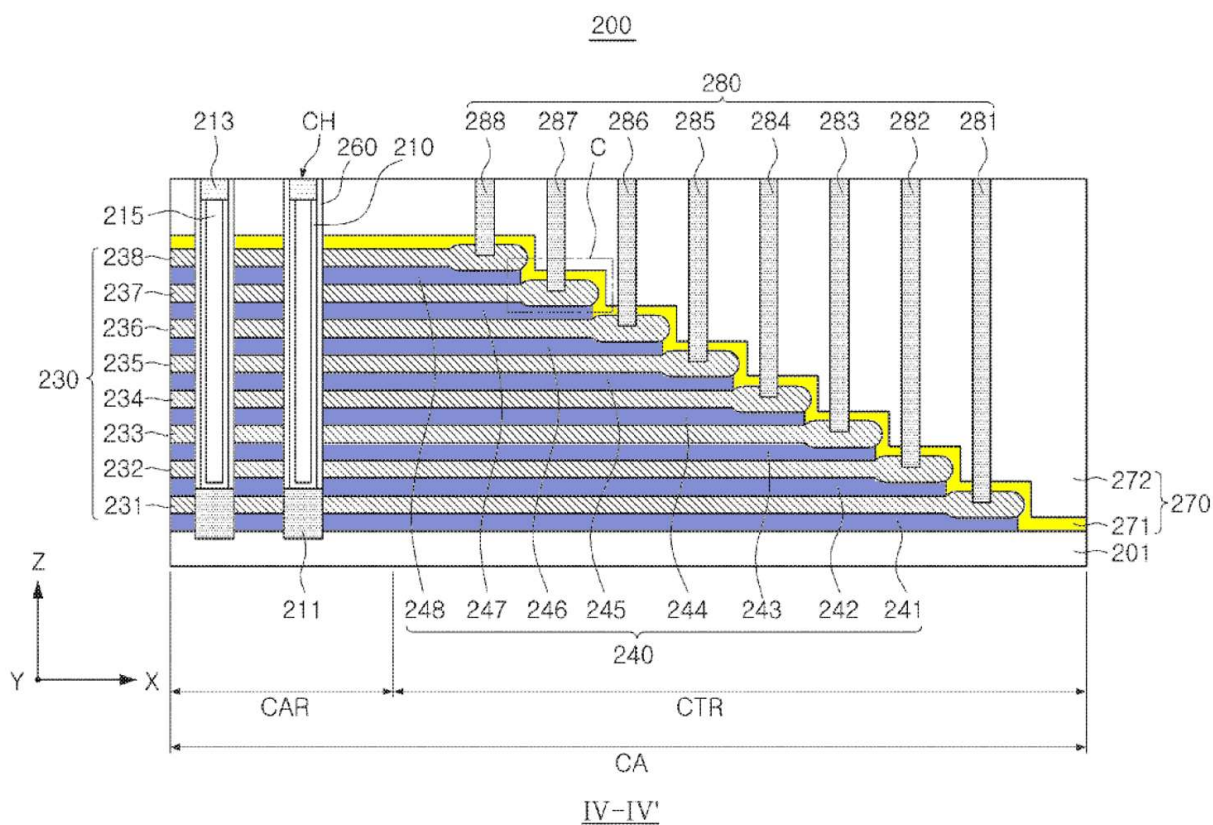


FIG. 7

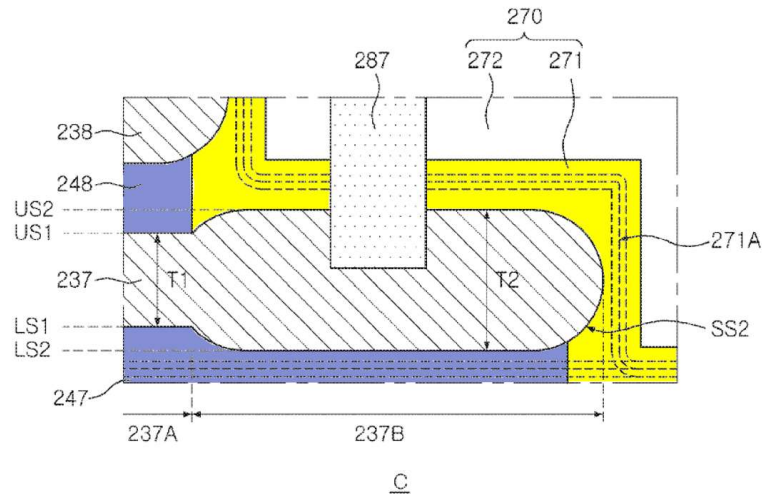
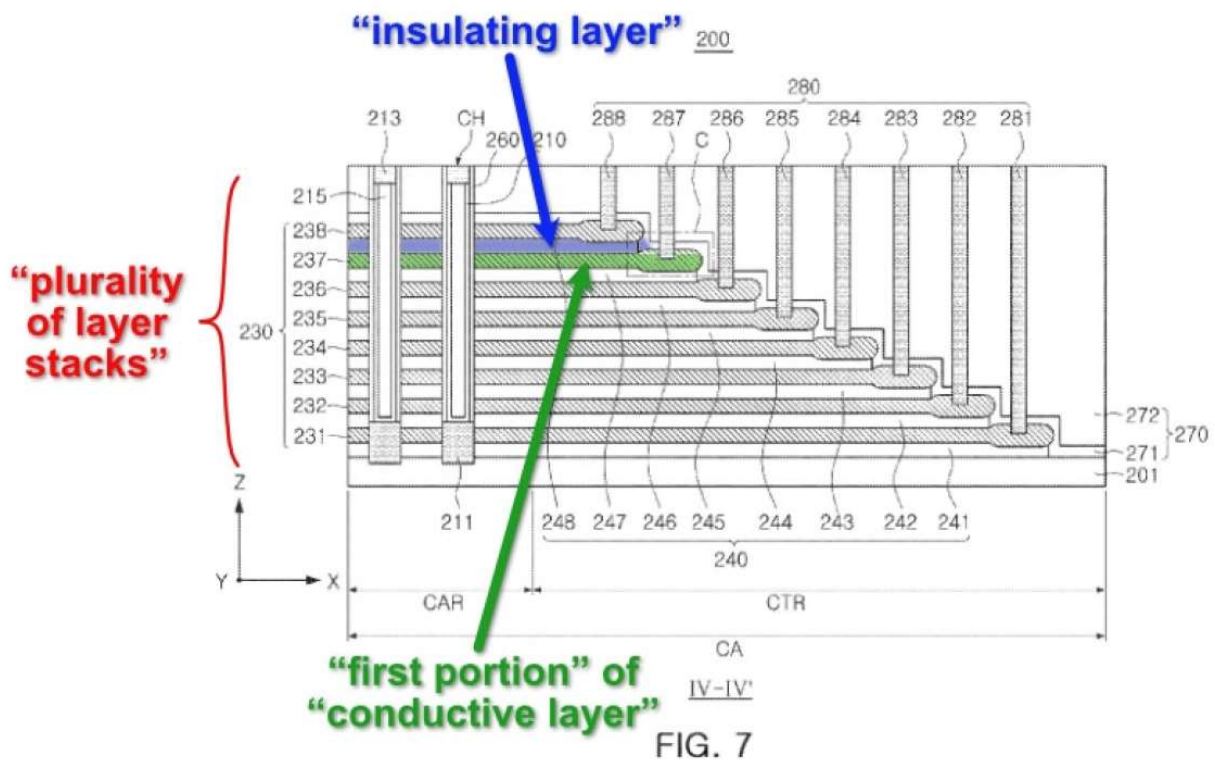
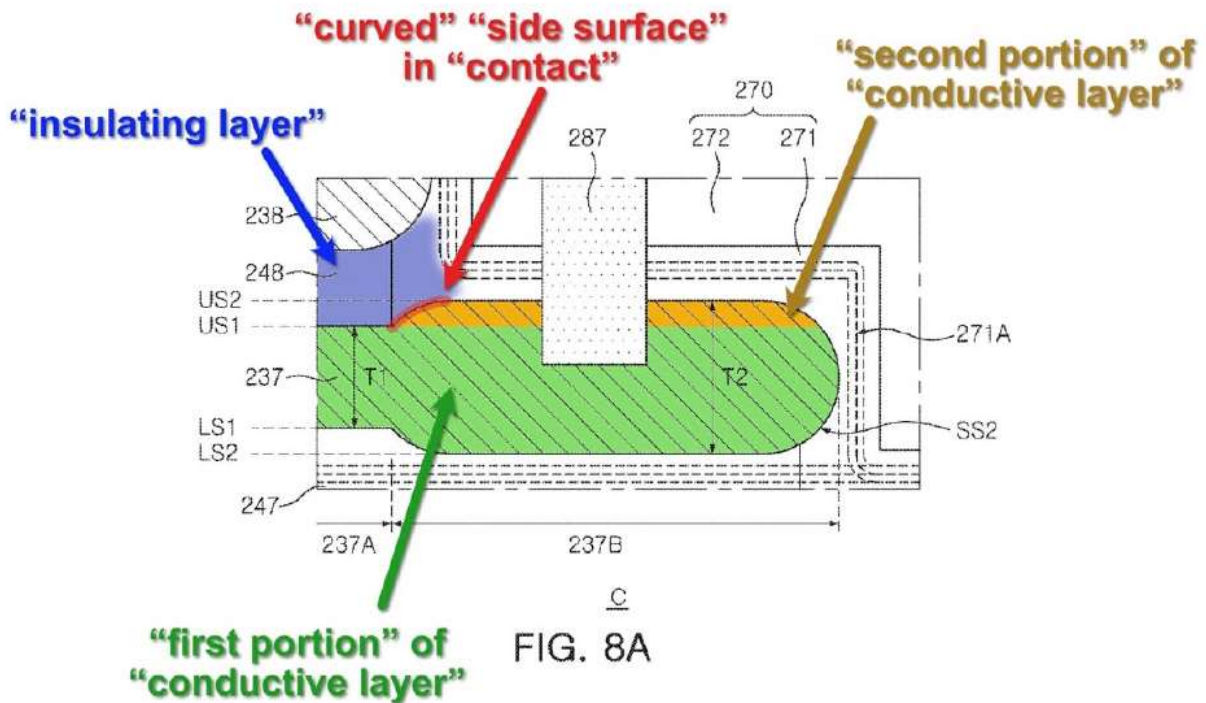


FIG. 8A

83. By contrast, Dr. Lee and the Petition annotate the same two figures as shown below, which come from Petition pages 61 and 67 and paragraphs 294 and 305 of Dr. Lee's declaration.

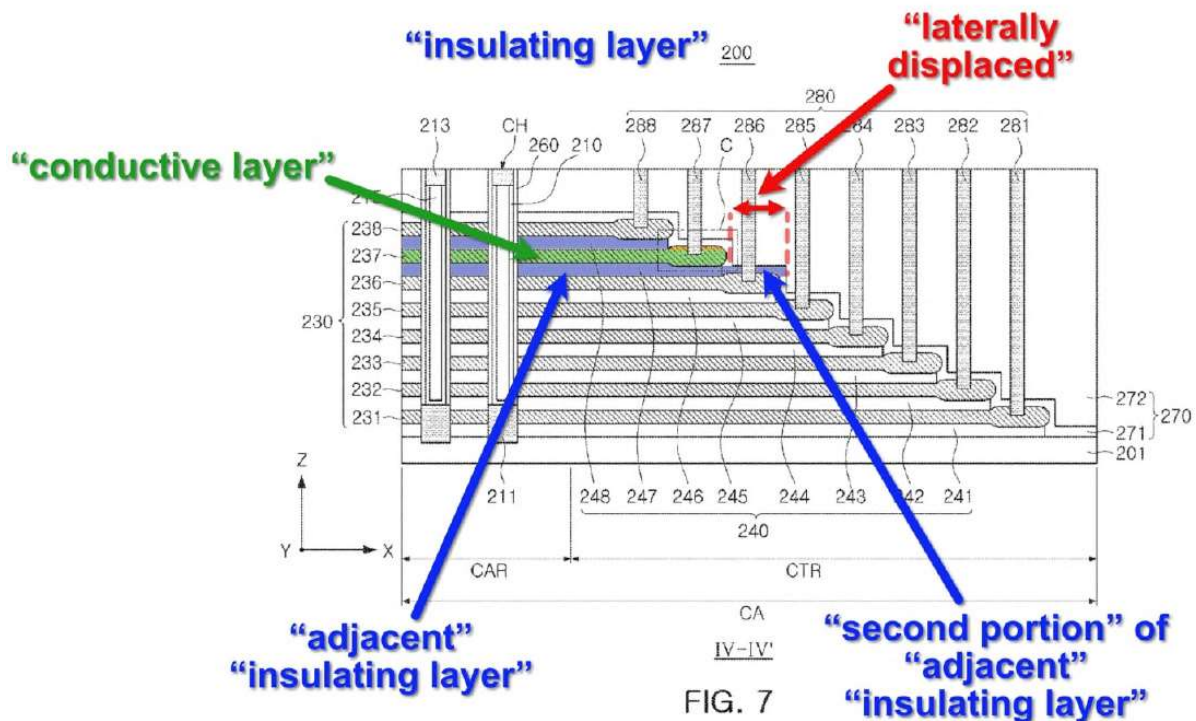




84. As can be seen in the Petition's annotations, the blue of the purported "insulating layer" is depicted as bleeding from Nam's insulating layer 248 into Nam's first interlayer insulating layer 271. The bleeding then arbitrarily stops, apparently to try and show that Nam has the claimed "curved side surface in contact with a side surface of the insulating layer." While Dr. Lee states that "a POSITA would have considered both Nam's insulating layer 240 and the adjacent insulating layer 271 to be the claimed 'insulating layer,'" Ex. 1003 ¶¶ 286-295, he does not explain why a POSITA would arbitrarily consider only part of the adjacent insulating layer 271 to be part of the claimed insulating layer. In my opinion, in the context of Nam, a POSITA would either consider them separate, or consider them all together. But a POSITA arbitrarily considering

only a portion is, in my opinion, a hindsight reconstruction of claim 19 and unsupported.

85. Further supporting that the Petition and Dr. Lee are engaging in hindsight is how they change their view in connection with the claim 19. Claim 19 recites, “wherein **the conductive layer** of a layer stack of the plurality of layer stacks **is disposed over a first portion of the insulating layer of an adjacent layer stack** of the plurality of layer stacks, wherein **a second portion of the insulating layer** of the adjacent layer stack **is laterally displaced from the conductive layer** of the layer stack.” ’666 patent at cl. 19 (emphasis added). At page 71 of the Petition and paragraph 345 of Dr. Lee’s declaration, the below figure is used to purportedly illustrate this part of claim 19 in Nam.



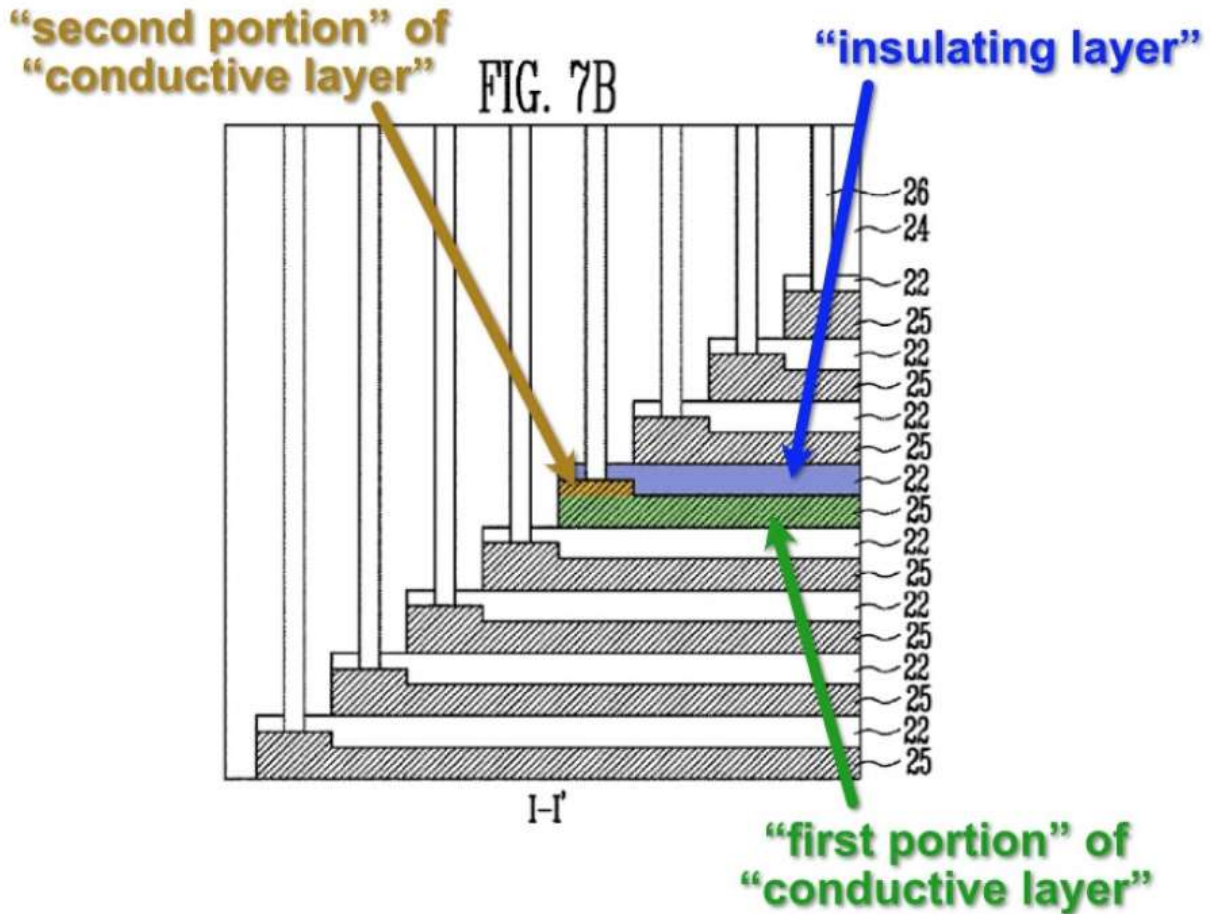
86. As can be seen, now the Petition and Dr. Lee rely on the entirety of Nam's first interlayer insulating layer 271 at the step for the "the insulating layer of an adjacent layer stack" of claim 19. This arbitrary and unexplained switch is inconsistent with how a POSITA would understand Nam's structure. A POSITA would treat each row of Nam's stepped structure the same. When doing so, the structure of claim 19 is not shown by Nam, nor rendered obvious by Nam. The Petition's and Dr. Lee's inconsistent approach, in my opinion, evidences the hindsight in their positions. Thus, Nam does not teach or render obvious claim 19.

IX. Ground 3: A POSITA Would Not Have Found Claim 19 Obvious Based on Lee in View of Park

87. The Petition and Dr. Lee assert that a POSITA would combine Lee with Park to arrive at claim 19. I note that the Petition simply provides the purported result of this combination on Page 84, but does not describe how a POSITA would combine Lee with Park to get there. The Petition cites to Dr. Lee's declaration to provide the missing details. In my opinion, Dr. Lee has made two critical errors in his analysis, which show that combining Lee with Park as the Petition proposes would not lead a POSITA to claim 19's structure, and in fact, would be impossible as proposed.

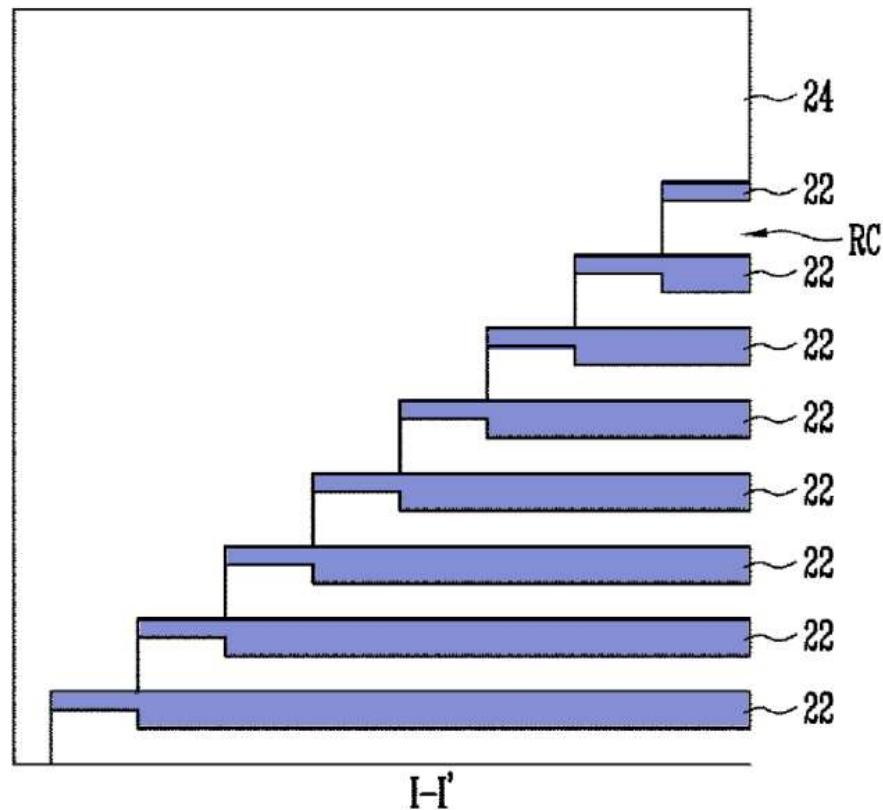
88. The Petition uses the below figure to identify structures in Lee. As the Petition recognizes, where Lee's pad portions PAD contact insulating layer

22, there are “straight sides.” Pet. 79, 82. The Petition and Dr. Lee rely on Park’s process to get to a purported curved side surface.



89. Dr. Lee explains that insulating layer 22 is an “oxide layer.” Ex. 1003 ¶ 391 (quoting Lee at [0030]). Dr. Lee then states that, in the combination, “the process shown in Figures 3B, 4B, and 5B of Lee could still be followed,” resulting “in the same-shaped openings shown in Figure 5B of Lee.” Ex. 1003 ¶ 411. Below I have reproduced Figure 5B of Lee, with the insulating layers 22 filled in with blue. Thus, according to Dr. Lee, the blue below is solid oxide after following the process in Lee through Figure 5B.

FIG. 5B

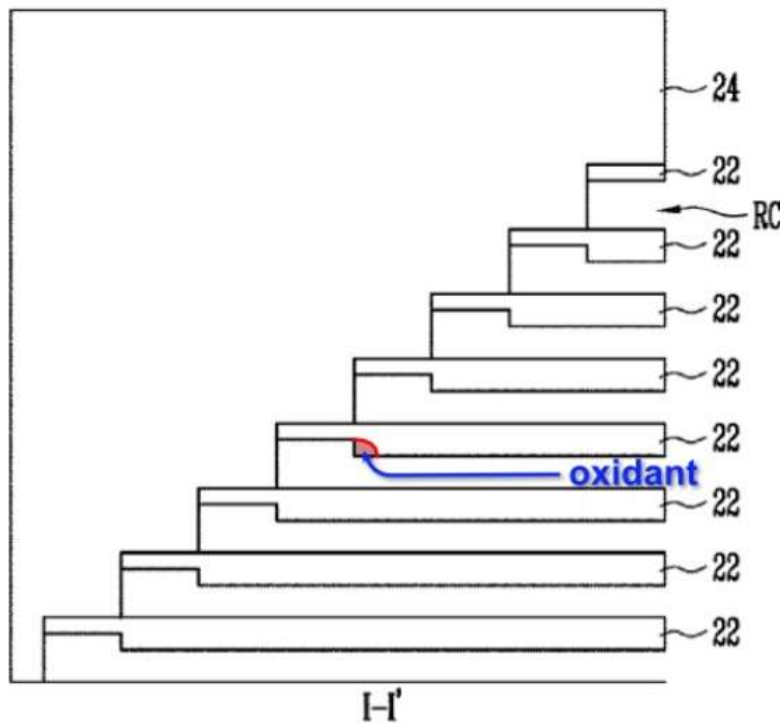


90. To get to curved sides, supposedly following Park's teachings, Dr. Lee says, "to achieve a rounded rather than straight sided contact pad, oxidant would be introduced into the openings." Ex. 1003 ¶ 411. In the above figure, the white portions are the "openings" and the blue portions are oxide insulating layers. By contrast, the oxidation in Park is performed on the "sacrificial layer patterns." Park at 12:6-23. In Park, the sacrificial layers are made of "silicon nitride" or "polysilicon." Park at 11:67-12:2. In Park's process then, an oxygen gas would be used to oxidize the silicon nitride or polysilicon.

91. Introducing such an oxidant into the openings of Lee's structure above will not promote further oxidation to the existing oxide layers 22. Nor would it change the shape of the existing oxide layers 22. It is not possible to further oxidize a solid oxide material with oxygen gas as in Park. That is why Park's thermal oxidation process is performed on silicon nitride or polysilicon, which are not oxides to begin with but they can be oxidized to form silicon dioxide. *See, e.g.,* Ex. 2008 (Plummer) at 345-350. A POSITA would understand this and not expect the combination of Lee and Park to achieve any change in shape or any rounding in Lee's Figure 5B. Thus, in my opinion, a POSITA would not have an expectation of success following the Petition and Dr. Lee's proposed combination.

92. There are further problems with Dr. Lee's combination. Using the figure below, Dr. Lee says "[t]he exterior corner (red below) would be rounded via oxidation first and most aggressively." Ex. 1003 ¶ 412. But where Dr. Lee has drawn this supposed "exterior corner" is inside the solid insulating layer 22.

FIG. 5B



93. To go from the above figure to Dr. Lee's figure under paragraph 415 of his declaration suggests that he is somehow removing insulating layer 22, but Dr. Lee never mentions any removal. The oxidation process in Park that he is combining with Lee is a growing of an oxide layer. This can be seen in comparing Park's Figure 9A with Park's Figure 9B, the latter of which depicts "additional insulating layer 66 [] formed by oxidizing surfaces and side surfaces of the sacrificial layer patterns 62b through 62f that are externally exposed." Park at 12:6-9. As can be seen, layer 66 has been formed on top of the exposed surfaces, it did not eat into and remove any of the sacrificial layers. In my opinion, a POSITA would not expect success in trying to form rounding inside a

solid oxide structure by introducing an oxidant. While the oxidant may diffuse through the oxide, it cannot react further with a fully formed oxide. *See, e.g.,* Ex. 2008 (Plummer) at 312-321.

94. Thus, in my opinion, a POSITA would not combine Lee with Park in the manner proposed by the Petition and Dr. Lee, as a POSITA would have no expectation of success in arriving at a curved side surface.

CONCLUSION

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed on March 12, 2025, in Pasadena, CA.

A handwritten signature in dark ink, appearing to read 'Konstantinos Giapis', written over a horizontal line.

Konstantinos Giapis