

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00189
Patent 11,145,666 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 17, 19, and 20 of U.S. Patent No. 11,145,666 B2 (“the ’666 patent,” Ex. 1001). Paper 1 (“Pet.”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 9 (“Prelim. Resp.”). In the Preliminary Response, Patent Owner indicates that it filed a Statutory Disclaimer pursuant to 35 U.S.C. § 253 and 37 C.F.R. § 1.321(a), disclaiming claims 17 and 20 of the ’666 patent, and, accordingly, claim 19 (“the challenged claim”) is the only claim at issue. Prelim. Resp. 4 (citing Ex. 2005).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314; *see also* 37 C.F.R. § 42.4. For the reasons discussed below, we determine that Petitioner establishes a reasonable likelihood of prevailing with respect to the unpatentability of claim 19. We also determine that the arguments and evidence of record do not support discretionary denial of the Petition under 35 U.S.C. § 314. Accordingly, we institute an *inter partes* review of claim 19 of the ’666 patent.

A. Patent Owner’s Disclaimer of Claims 17 and 20

As indicated above, Patent Owner filed a statutory disclaimer of claims 17 and 20 of the ’666 patent. *See* Ex. 2005. In view of Patent Owner’s statutory disclaimer, we treat claims 17 and 20 as having never been part of the ’666 patent. *See Vectra Fitness, Inc. v. TNWK Corp.*, 162 F.3d 1379, 1383 (Fed. Cir. 1998) (“This court has interpreted the term ‘considered as part of the original patent’ in [35 U.S.C.] § 253 to mean that

the patent is treated as though the disclaimed claims never existed.”). Because *inter partes* review cannot be instituted based on disclaimed claims, we do not consider claims 17 and 20 to be within the scope of this proceeding. 37 C.F.R. § 42.107(e) (“No *inter partes* review will be instituted based on disclaimed claims.”); *General Elec. Co. v. United Techs. Corp.*, IPR2017-00491, Paper 9 (PTAB July 6, 2017) (precedential) (denying institution in view of a statutory disclaimer of all the challenged claims). Thus, we confine our analysis in this Decision to claim 19, the challenged claim that has not been disclaimed.

B. Real Parties in Interest

Petitioner identifies “Micron Technology, Inc., and its subsidiaries, including Micron Consumer Products Group LLC” as the real parties in interest. Pet. 6. Patent Owner identifies itself as the real party in interest. Paper 4 (Mandatory Notice), 1.

C. Related Matters

The parties indicate that the ’666 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.) (“the parallel proceeding”). Pet. 6; Paper 4, 1.

D. The ’666 Patent

The ’666 patent, titled “Staircase Structure for Memory Device,” is “directed to a staircase structure for a memory device (e.g., 3D memory device)” that “provide[s] numerous benefits including, but not limiting to, yield and manufacturing cost improvements.” Ex. 1001, code (54), 1:37–41. Figure 8 of the ’666 patent is reproduced below.

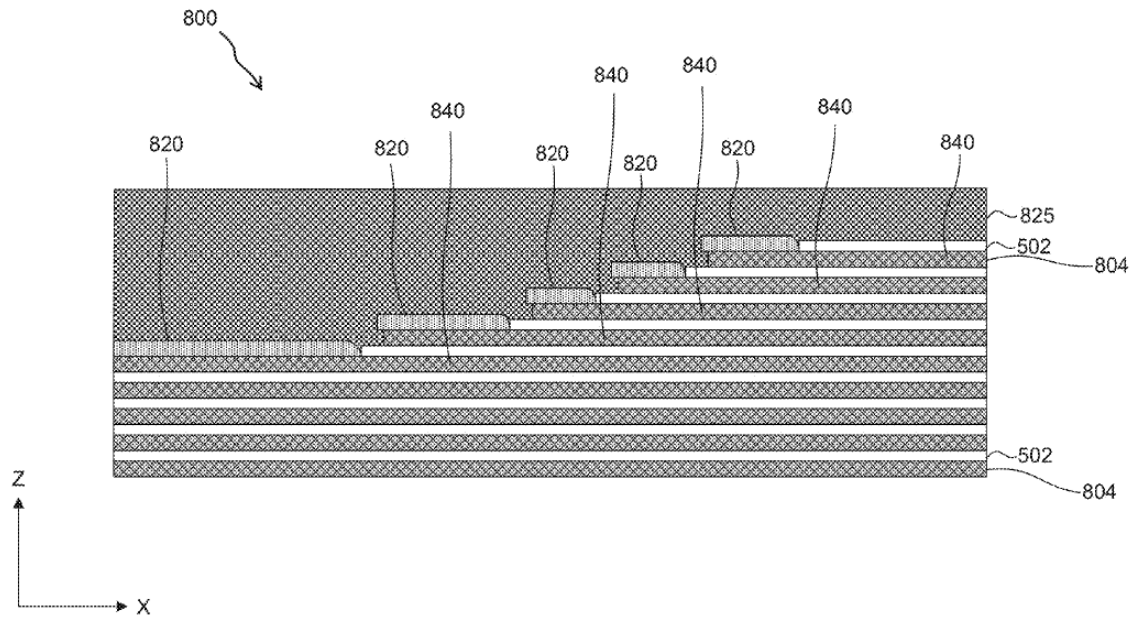


Figure 8 is a cross-sectional view of a staircase structure with a dielectric layer disposed thereon as described in the '666 patent. *Id.* at 3:25–27. Staircase structure 800 includes dielectric layer 825, wordline layers 804, insulating layers 502, landing pads 820, and conductive layers 840. *Id.* at 9:48–61.

The '666 patent explains that each wordline layer 804 of a staircase (“SC”) layer is disposed over a portion of insulating layer 502 of another vertically adjacent SC layer. Ex. 1001, 9:48–50. Landing pad 820 is thicker than insulating layer 502 and is insulated from another landing pad 820 disposed on another vertically adjacent SC layer. *Id.* at 9:53–56. Each wordline layer 804, including landing pad 820 and conductive layer 840 can control a portion of a memory string in the stacked storage region of a memory device. *Id.* at 9:57–61. The '666 patent further explains that each wordline layer 804 is a wordline of the memory device, where conductive layer 840 contacts a portion of a memory string of a memory device, and landing pad 820 contacts a portion of a side of insulating layer 502. *Id.*

at 9:61–65. In some embodiments, landing pad 820 is thicker than conductive layer 840 of wordline layer 804. *Id.* at 9:65–10:1.

E. Challenged Claim

Petitioner challenges claim 19 of the '666 patent. Claim 19 is reproduced below, along with claim 17 from which claim 19 depends.

17. A memory device, comprising:
- a substrate, wherein the substrate comprises a top surface;
 - a memory string disposed over the substrate; and
 - a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:
 - a plurality of layer stacks, each layer stack comprising an insulated layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.

Ex. 1001, 15:11–16:2.

19. The memory device of claim 17, wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack.

Id. at 16:8–14.

F. Asserted Grounds

Petitioner asserts that claim 19 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
19	103 ¹	Kim ²
19	103	Nam ³
19	103	Lee, ⁴ Park ⁵

Pet. 10–11. Petitioner relies on the Declaration of Dr. Jack C. Lee (“Lee Declaration,” Ex. 1003) in support of its Petition. Patent Owner relies on the Declaration of Konstantinos Giapis (Ex. 2007) in support of its Preliminary Response.

II. ANALYSIS

A. Discretionary Denial under 35 U.S.C. § 314(a)

Under 35 U.S.C. § 314(a) we have discretion to deny institution of an *inter partes* review. *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016). Petitioner argues against discretionary denial under 35 U.S.C. § 314(a). Pet. 11–14. Patent Owner argues that we should exercise our discretion under 35 U.S.C. § 314(a) and not institute trial. Prelim. Resp. 31–38. For the reasons set forth below, we do not exercise our discretion to deny institution in view of the parallel district court proceeding.

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the ’666 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (60)), we refer to the AIA version of Sections 102 and 103.

² US 10,229,929 B2, issued March 12, 2019 (“Kim,” Ex. 1005).

³ US 2018/0026046 A1, published Jan. 25, 2018 (“Nam,” Ex. 1006).

⁴ US 2014/0191389 A1, published July 10, 2014 (“Lee,” Ex. 1007).

⁵ US 10,297,543 B2, issued May 21, 2019 (“Park,” Ex. 1008).

Institution of an *inter partes* review is discretionary. *See* 35 U.S.C. § 314(a) (authorizing institution of an *inter partes* review under particular circumstances, but not requiring institution under any circumstances); *Cuozzo*, 136 S. Ct. at 2140 (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”); *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) (“[Section] 314(a) invests the Director with discretion on the question whether to institute review” (emphasis omitted)); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”).

We consider several factors when determining whether to deny institution under § 314(a) based on a parallel district court proceeding, specifically

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board’s exercise of discretion, including the merits.

Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”).

1. *Factor 1 – Whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted*

Under the first *Fintiv* factor, we consider “whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted.” *Fintiv* at 6.

In the Preliminary Response, Patent Owner represents that the parallel proceeding was temporarily stayed pending consideration of Petitioner’s motion for a stay in light of the filed *inter partes* review proceedings. Prelim. Resp. 32 (citing Ex. 2001; Ex. 2003). Subsequently, Patent Owner notified the Board that the parallel proceeding “was stayed pending resolution of related IPR proceedings.” Paper 10, 1; *see also* Ex. 3001 (district court order granting motion to stay case). Accordingly, we determine that *Fintiv* factor 1 weighs strongly against exercising our authority to deny institution. *See Snap, Inc. v. SRK Technology, Inc.*, IPR2020-00820, Paper 15 at 9 (PTAB Oct. 21, 2020) (precedential) (“The granting of a stay pending *inter partes* review has weighed strongly against exercising discretion to deny institution under *NHK*.”).

2. *Factor 2 – The proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision*

Under the second *Fintiv* factor, we consider the “proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision.” *Fintiv* at 6.

Patent Owner asserts that trial in the parallel proceeding is scheduled for June 15, 2026, which “is three days after the statutory deadline for a Final Written Decision in this case (June 12, 2026).” Prelim. Resp. 33. Patent Owner asserts “[a] Final Written Decision here would issue after

expert discovery, after dispositive motions, and after the pretrial conference.” *Id.* at 34 (citing Ex. 1019, 2). Patent Owner contends that “[t]his factor therefore favors denial of institution, or is at worst neutral.” *Id.* (citing *Fintiv*, IPR2020-00019, Paper 11 at 9). Petitioner argues that, if instituted, this proceeding “should be completed” before the June 15, 2026 trial date, and “[t]his weighs strongly in favor of institution.” Pet. 12 (citing Ex. 1019; Ex. 1020).

Because the parallel proceeding is stayed pending the resolution of the related IPR proceedings, any trial that occurs will happen well after the projected statutory deadline for a final written decision in this case. *See* Ex. 3001, 3 (“The parties shall file a joint status report every six months, and shall notify the Court within 30 days of the completion of *all* IPR proceedings.” (emphasis added)). Accordingly, factor 2 weighs against exercising our authority to deny institution.

3. *Factor 3 – Investment in the parallel proceeding by the court and the parties*

Under the third *Fintiv* factor, we consider the “investment in the parallel proceeding by the court and the parties.” *Fintiv* at 6.

Patent Owner argues that the parties have expended “substantial resources into the Parallel Proceeding,” including propounding and responding to numerous interrogatories and requests for production, and Patent Owner “has narrowed its claims of infringement to 70 asserted claims, which has required extensive analysis of infringement, validity, and damages issues.” Prelim. Resp. 34–35 (citing Ex. 2002, 12). Patent Owner argues that, “[b]ecause the parties and the Court will expend significant effort in the parallel litigation *before institution*, this factor favors discretionary denial of institution.” *Id.* at 35.

Petitioner contends that “[v]irtually no progress has been [made] on the Wave 3 patents (which includes the ’666 patent),” and “[t]he parties have not completed the exchange of contentions for the Wave 3 patents . . . and have not taken any depositions in the [parallel proceeding].” Pet. 12. Petitioner also argues that it “proceeded with diligence, starting the filing of eleven petitions [for the Wave 3 patents] three months after being served with” the complaint. *Id.* at 13 (citing Ex. 1022).

Although we recognize that the parties have invested some resources, much work remains to be done in the parallel proceeding. The parallel proceeding appears to be in an early stage, there is no evidence that the district court has issued any substantive orders related to the ’666 patent or the prior art set forth in the Petition, and the parallel proceeding was stayed as of March 14, 2025. *See* Ex. 3001, 1 (staying the parallel proceeding and noting that “the litigation is in an early stage” and “[c]laim construction briefs have not yet been filed”). Thus, we determine that *Fintiv* factor 3 weighs slightly against exercising our authority to deny institution.

4. *Factor 4 – Overlap between issues raised in the petition and in the parallel proceeding*

Under the fourth *Fintiv* factor, we consider the “overlap between issues raised in the petition and in the parallel proceeding.” *Fintiv* at 6.

Petitioner states that, “[s]hould the Board institute, [Petitioner] stipulates that it will not advance in District Court any ground asserted in this Petition,” which “eliminates any potential overlap in issues between the proceedings here and in District Court.” Pet. 13. Patent Owner asserts that Petitioner served invalidity contentions in the parallel proceeding “identifying the same art from its Petition, and explicitly incorporating its IPR petition by reference.” Prelim. Resp. 36. Patent Owner also asserts that

although Petitioner offers a stipulation in the Petition, “no such stipulation has been made in the district court.” *Id.* (citing Pet. 13). In any event, Patent Owner argues, “[s]uch a narrow stipulation runs the risk of significant overlap both in consideration of the same evidence and arguments framed as ‘different grounds’ than the Petition.” *Id.*

Here, any potential overlap in issues is mitigated by the district court’s stay of the parallel proceeding pending resolution of the related IPR proceedings. *See* Ex. 3001, 2 (“The overlapping subject matter of these claims means that staying the case pending IPR will likely simplify infringement, validity, and claim construction issues in this case.”). Accordingly, we determine that *Fintiv* factor 4 weighs slightly against exercising our authority to deny institution.

5. *Factor 5 – Whether the petitioner and the defendant in the parallel proceeding are the same party*

Under the fifth *Fintiv* factor, we consider “whether the petitioner and the defendant in the parallel proceeding are the same party.” *Fintiv* at 6. In consideration of the fact that the parallel District Court proceeding is stayed, and that Petitioner’s stipulation reduces potential overlap between the invalidity contentions and the Petition challenges, we regard the consideration of the fifth *Fintiv* factor as neutral or, at most, weighing slightly in favor of exercising discretion to deny institution.

6. *Factor 6 – Other circumstances that impact the Board’s exercise of discretion, including the merits*

Under the sixth *Fintiv* factor, we consider “other circumstances that impact the Board’s exercise of discretion, including the merits.” *Fintiv* at 6. Petitioner contends this factor weighs against discretionary denial because the Petition “has significant substantive merit.” Pet. 13.

The parties disagree on the strength of the merits of the Petition. Pet. 13; Prelim. Resp. 38. As detailed below, we determine that the Petitioner meets its burden for institution for the challenged claim. *See* §§ II.D–II.E, *infra*. As noted, Petitioner’s case is not undermined by any facts or arguments on the current record. *Id.* Thus, on this record, factor 6 weighs against exercising our authority to deny institution.

7. *Conclusion – Fintiv*

Absent a compelling reason to the contrary, we take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review” when evaluating the *Fintiv* factors. *Fintiv* at 6. Having evaluated all of the factors on this record, we determine that the circumstances presented do not support exercising our discretion under § 314(a) to deny institution of this *inter partes* review.

B. *Level of Ordinary Skill in the Art*

Petitioner contends that a person of ordinary skill in the art (“POSITA”) “would have had a bachelor’s degree in electrical engineering or a similar discipline, along with 2–3 years of professional experience working with (e.g., researching, designing, or teaching) 3D memory devices, or an equivalent level of skill, knowledge and experience (e.g., an advanced degree may substitute for professional experience).” Pet. 24–25 (citing Ex. 1003 ¶¶ 34–37). Petitioner further contends that the “POSITA would also have been aware of and generally knowledgeable about 3D memory’s structure, its component parts, and how it operates.” *Id.* at 25 (citing Ex. 1003 ¶¶ 34–37). Patent Owner “takes no position on the level of ordinary skill in the art” as this stage of the proceeding. Prelim. Resp. 6.

Petitioner’s undisputed proposed definition appears to be consistent with the cited prior art and the disclosure of the ’666 patent, and we adopt it

for purposes of this Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown” (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

C. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

Based on the record before us, we determine that no claim term requires express construction for purposes of this Decision.

D. Asserted Obviousness over Kim

Petitioner contends that claim 19 would have been obvious over Kim. Pet. 33–55.

1. Overview of Kim

Kim is directed to “semiconductor memory devices having enhanced reliability.” Ex. 1005, 1:38–39. Kim teaches that the semiconductor memory device includes a substrate with a cell array region, a contact region, and stacking structure including a plurality of insulating layers and a plurality of gate electrodes alternately stacked on the substrate. *Id.* at 1:41–

46. “The stacking structure may include a stepwise structure in the contact region.” *Id.* at 1:46–47. Kim teaches that ones of the plurality of gate electrodes “may include a respective pad unit that comprises a step of the stepwise structure,” and “[a]t least one of the pad units may include a base pad and a protrusion pad on the base pad.” *Id.* at 1:47–50. Kim further teaches that “[t]he protrusion pad may be between and spaced apart from two edges of a surface of the base pad that are perpendicular to an extension direction of the respective gate electrode.” *Id.* at 1:51–53.

Figure 4B is reproduced below.

FIG. 4B

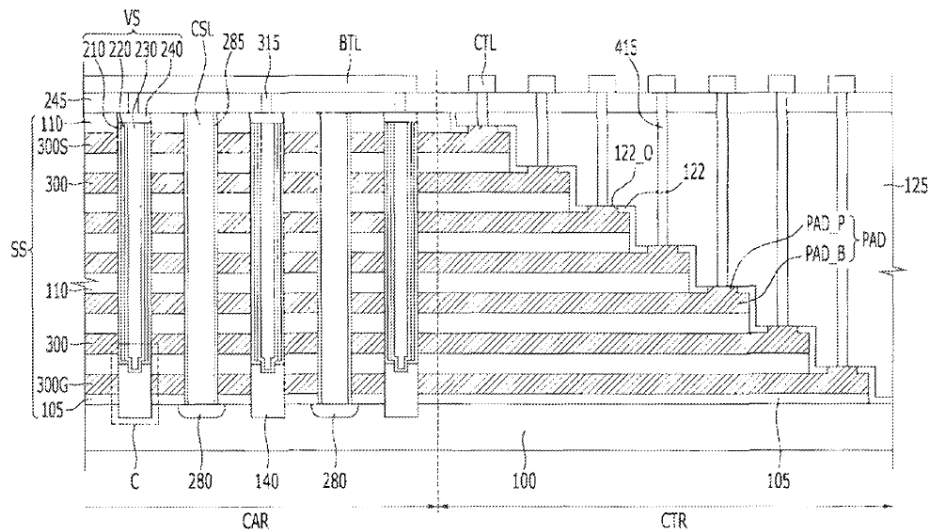


Figure 4B is a cross-sectional view of a partial region of a semiconductor device described in Kim. Ex. 1005, 2:41–42. Substrate 100 includes cell array region CAR, contact region CTR positioned on the periphery of cell array region CAR, and a plurality of common source regions 280. *Id.* at 5:33–37, 5:45–46. Vertical pattern structure VS, stacking structure SS, and bit line BTL may also be on substrate 100. *Id.* at 5:37–39. Stacking structure SS includes a plurality of insulating layers 110 and a plurality of gate electrodes 300 that are alternately stacked. *Id.* at 5:53–55. Common

source line CSL is between adjacent stacking structures SS and penetrates a plurality of gate electrodes 300 and a plurality of insulating layers 110 in a vertical direction that is perpendicular to the uppermost surface of substrate 100. *Id.* at 5:63–67. Trench spacer 285 between common source line CSL and gate electrode 300 electrically insulates common source line CSL and the gate electrode 300 adjacent in the y direction. *Id.* at 6:1–6.

The plurality of gate electrodes 300 and plurality of insulating layers 110 extending from the cell array region CAR into the contact region CTR have a stepwise structure. Ex. 1005, 7:47–52. Pad unit PAD is at an end of gate electrode 300 exposed through the stepwise structure. *Id.* at 7:58–59. Pad units PAD include base pad PAD_B and protrusion pad PAD_P contacting a surface of base pad PAD_B. *Id.* at 7:60–62. Base pad PAD_B may be part of gate electrode 300 in contact region CTR, and “may be exposed by an adjacent pad unit PAD that is stacked on the pad unit PAD.” *Id.* at 7:63–66. “The pad unit PAD and the adjacent pad unit PAD may not overlap with each other.” *Id.* at 7:66–67. Protrusion pad PAD_P may contact the uppermost surface of base pad PAD_B that is exposed by the adjacent base pad PAD_B. *Id.* at 8:3–10.

2. Claim 19

Claim 19 depends from, and includes all of the limitations of, claim 17. Ex. 1001, 16:8–14. Petitioner contends that Kim teaches or discloses all of the limitations of claim 17. Pet. 33–53. For example, Petitioner contends that Kim teaches “a substrate, wherein the substrate comprises a top surface” (substrate 100 with an upper surface on which a plurality of gate electrodes are stacked), “a memory string disposed over the substrate” (memory cell array includes a plurality of cell strings extending in a vertical direction to a plane of the substrate), and “a staircase structure

disposed adjacent to the memory string” (contact region CTR with a stepped structure positioned on the periphery of cell array region CAR). *Id.* at 33–36 (emphases omitted); Ex. 1003 ¶¶ 141–156.

With respect to the “a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer” limitation of claim 17, Petitioner contends that “Kim’s memory device includes a step-shaped ‘stacking structure SS’ formed from a ‘plurality’ of alternating ‘insulating layers 110 and . . . gate electrodes 300’ located ‘on the substrate 100.’” Pet. 36, 39 (citing Ex. 1005, 6:35–36) (alterations in original). Petitioner contends that “Kim also explains that its device includes an ‘auxiliary insulating layer 122’ that “‘may include the same or similar material as the insulating layer 110’ such that ‘a boundary between the auxiliary insulating layer 122 and the insulating layer 110 may not be distinguished and the auxiliary insulating layer 122 and the insulating layer 110 may form one structure.’” *Id.* (citing Ex. 1005, 9:12–13, 9:29–38). According to Petitioner, “[a] POSITA would have understood that Kim’s insulating layer 110 and the adjacent portion of auxiliary insulation layer 122 together constitute the claimed ‘insulating layer’ in a ‘layer stack.’” *Id.* at 39–40 (citing Ex. 1003 ¶¶ 157–172) (emphases omitted). Petitioner identifies gate electrodes 300, which “can be formed from conductive material,” as the claimed “conductive layer.” *Id.* at 39; *see also id.* at 41 (“An example ‘layer stack’ including an ‘insulating layer’ (the combination of Kim’s insulating layer 110 and auxiliary insulating layer 122) and ‘conductive layer’ (the gate electrode 300) are annotated in Figure 4B below.” (emphases omitted)).

With respect to the “wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the

insulating layer” limitation of claim 17, Petitioner first contends that “Kim’s device includes both a ‘conductive layer’ with a ‘first portion’ (gate electrode 300 and attached base pad PAD_B) and a ‘second portion’ (protrusion pad PAD_P).” Pet. 42–43 (citing Ex. 1005, Fig. 4B; Ex. 1003 ¶¶ 186–193) (emphases omitted). Petitioner then contends that, because protrusion pad PAD_P is located inside opening 122_O in auxiliary insulating layer 122, “there is ‘contact’ between a ‘side surface’ of Kim’s ‘second portion’ (the protrusion pad PAD_P) and a ‘side surface of the insulating layer’ (the side walls of opening 122_O in auxiliary insulating layer 122).” *Id.* at 44–45 (citing Ex. 1005, 9:21–23, Fig. 4B; Ex. 1003 ¶¶ 197–199) (emphases omitted).

Finally, Petitioner asserts Kim explains that protrusion pad PAD_P “may have a shape including a curved surface based on a virtual rectangular parallell[] shape, a cylindrical shape, or any shape,” and contends that “[a] POSITA would have understood that this teaches a variety of different protrusion pad PAD_P shapes, many of which have the type of ‘*curved*’ side surface claim 17 requires.” Pet. 45 (citing Ex. 1005, 8:29–34). Petitioner also contends that “[t]his type of pad was also well known in the art.” *Id.* at 49 (citing Ex. 1008, Fig. 7; Ex. 1018, Fig. 5A; Ex. 1006, Fig. 8A). Therefore, Petitioner contends, “contact pads with curved side surfaces would have been among the available design choices a POSITA would have considered for use,” and “a POSITA would have recognized that using a ‘curved’ side surface with Kim’s pads would have improved Kim by increasing the minimum distance between the pad and adjacent conductive layers, thereby reducing the risk of short circuit.” *Id.* at 49–50 (citing Ex. 1003 ¶¶ 219–222; Ex. 1008, 11:35–41).

Patent Owner responds that Kim does not disclose a “curved side surface in contact with a side surface of the insulating layer” because Kim’s etching process results only in straight side surfaces and Petitioner does not explain how Kim’s process can form the claimed “curved side surface.” Prelim. Resp. 7–12. Patent Owner also argues that a POSITA would not have been motivated to modify Kim’s semiconductor device to reduce the risk of short circuit, or that a POSITA would have had a reasonable expectation of success in modifying Kim as Petitioner proposes. *Id.* at 12–21.

Based on the record before us, we are persuaded that Kim’s teachings and Dr. Lee’s explanations adequately establish that Kim discloses “a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer” as recited in claim 17. In particular, Kim states:

Embodiments of the inventive concepts in which the protrusion pad PAD_P has a rectangular parallel[] shape is illustrated, but the protrusion pad PAD_P is not limited thereto and, in some embodiments, may have a shape *including a curved surface* based on a virtual rectangular parallel[] shape, a cylindrical shape, or *any shape*.

Ex. 1005, 8:29–34 (emphases added). Dr. Lee testifies that “[a] POSITA would have recognized that this includes configurations where the sides of the protrusion pads are curved, particularly to optimize electrical connectivity and mitigate stress at material interfaces.” Ex. 1003 ¶ 201. Dr. Lee further testifies that a POSITA would have understood Kim’s disclosure “teaches a variety of different protrusion pad PAD_P shapes” including “pads with curved sides when viewed in cross-section or pads with curved sides when viewed from above.” *Id.* ¶ 202; *see also id.* ¶ 203

(Dr. Lee explaining that a “curved surface based on a virtual parallel[] shape” would have “a generally rectangular shape” wherein “the pad’s sides are ‘curved’ in the area where they contact auxiliary insulating layer 122”), ¶ 240 (Dr. Lee explaining that “a POSITA would have understood that a generally rectangular pad with two flat sides and two sides following a cylindrical pattern is yet another way a POSITA would have considered implementing Kim’s teaching that its pad can have a ‘curved surface based on a virtual rectangular parallel[] shape”).

Having determined that Petitioner adequately establishes that Kim discloses the recited “a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer,” we do not reach the parties’ allegations regarding a motivation to modify Kim with a reasonable expectation of success. Pet. 46–53; Prelim. Resp. 12–21. This does not constitute, however, a determination regarding the persuasiveness of the arguments in this regard. The parties will have the opportunity to further develop these facts and arguments during trial, and the Board will evaluate the fully-developed record at the close of evidence.

At this stage of the proceeding, Patent Owner does not address Petitioner’s specific contentions with respect to the other limitations of claim 19. *See* Prelim. Resp. We reviewed Petitioner’s contentions for all of the elements of claim 19, including the elements of claim 17 from which claim 19 depends, and are persuaded, on this record, that Petitioner’s discussion of the particular structures Kim and the explanations in the Lee Declaration establish a reasonable likelihood that Kim teaches all of the limitations of claim 19. *See* Pet. 33–55.

E. Asserted Obviousness over Nam

Petitioner contends that claim 19 would have been obvious over Nam. Pet. 56–71.

1. Overview of Nam

Nam is directed to a semiconductor device that includes a stack of alternating first interlayer insulating layers and gate electrodes on a substrate. Ex. 1006 ¶ 5. Figure 7 is reproduced below.

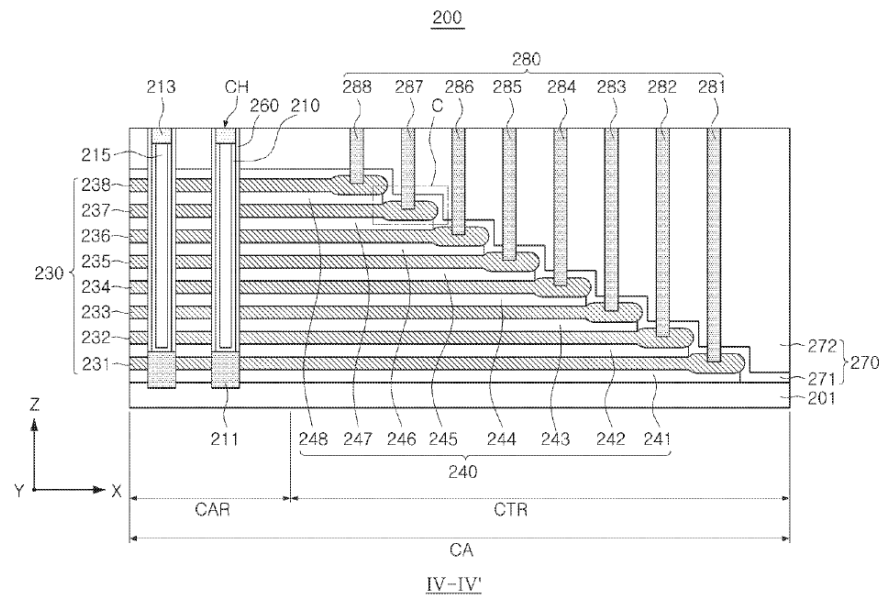
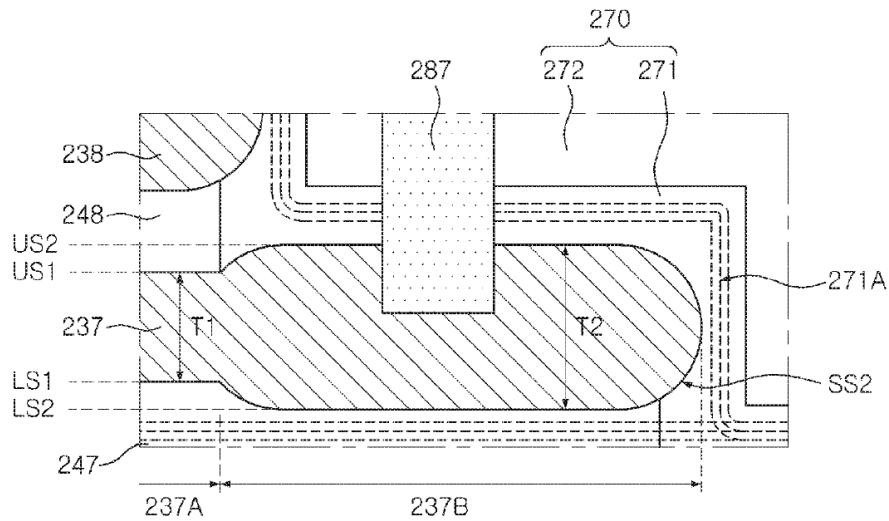


FIG. 7

Figure 7 is a schematic view of a memory device according to an embodiment described in Nam. *Id.* ¶ 15. Memory device 200 includes cell array region CAR and contact region CTR in cell region CR. *Id.* ¶ 62. A plurality of cell channel structures CH are disposed in cell array region CAR. *Id.* Cell channel structure CH includes epitaxial layer 211 connected to substrate 201, channel layer 210, bit line pad 213, embedded insulating layer 215, and gate insulating layer 260. *Id.* A plurality of gate electrode layers 231 to 238 (collectively, gate electrode layers 230) are connected to a plurality of contacts 281 to 288 (collectively, contacts 280) in contact region

CTR. *Id.* ¶ 63. Gate electrodes 230 extend in a first direction (X-axis direction), while forming a pair with one of a plurality of insulating layers 241 to 248 (collectively, insulating layers 240) adjacent thereto in a stack direction (Z-axis direction), respectively, to form a plurality of pad regions. *Id.* Each of gate electrode layers 230 have a relatively greater thickness in the pad region. *Id.* ¶ 64.

Figure 8A is reproduced below.



C
FIG. 8A

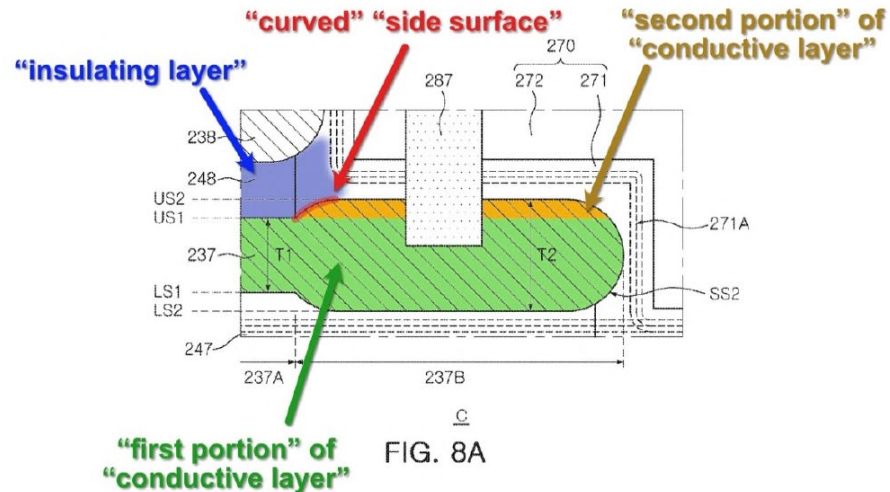
Figure 8A is an enlarged view of region C of Figure 7. Ex. 1006 ¶ 16. Gate electrode layer 237 includes first region 237A and second region 237B. *Id.* ¶ 65. Second region 237B is provided as a pad region with thickness T2 that is greater than thickness T1 of first region 237A. *Id.* Upper surface US2 of second region 237B is disposed to be higher than upper surface US1 of first region 237A, and lower surface LS2 of second region 237B is disposed to be lower than lower surface LS1 of first region 237A. *Id.* Lateral surface SS2 of second region 237B protrudes outwardly therefrom in the first direction

(X-axis direction). *Id.* ¶ 66. Lateral surface SS2 may be convex or have a bull nose shape. *Id.*

2. *Claim 19*

Claim 19 depends from, and includes all of the limitations of, claim 17. Ex. 1001, 16:8–14. Petitioner contends that Nam teaches or discloses all of the limitations of claim 17. Pet. 56–69. For example, with respect to the “a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer” limitation of claim 17, Petitioner contends that “Nam explains that its device ‘includes a stack of alternating first interlayer insulating layers and gate electrode layers on a substrate’” such as that shown in Nam’s Figure 7, where gate electrode layers 230 (formed from a conductive material such as metal) are alternately arranged to form a pair with one of insulating layers 240 (formed of silicon oxide) adjacent thereto in the Z-axis direction. Pet. 59–60 (citing Ex. 1006 ¶¶ 5, 63, 81, 94). Petitioner contends that first interlayer insulating layer 271 (also made from silicon oxide) is formed adjacent to insulating layers 240 and surrounds the ends of gate electrode layers 230. *Id.* at 60 (citing Ex. 1006 ¶ 98). Petitioner contends that “[a] POSITA would have considered both Nam’s insulating layer 240 and the adjacent insulating layer 271 to be the claimed ‘insulating layer’” because it “is not only formed from the same material as layer 240, but is used to define the shape of Nam’s pads.” *Id.* (citing Ex. 1003 ¶¶ 279–289) (emphases omitted).

Petitioner relies on an annotated version of Nam’s Figure 8A, reproduced below, to illustrate its contentions regarding the “wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer” limitation of claim 17.



Annotated Figure 8A is an enlarged view of region C of Figure 7, with Petitioner’s added blue shading to insulating layer 248 and part of interlayer insulating layer 271 labeled “insulating layer,” orange shading to the portion of second region 237B between upper surface US1 of first region 237A and upper surface US2 of second region 237B of gate electrode layer 237 labeled “‘second portion’ of ‘conductive layer,’” green shading to the remainder of gate electrode layer 237 labeled “‘first portion’ of ‘conductive layer,’” and a red line tracing the curve of the pad where the orange shading meets the blue shading labeled “‘curved’ ‘side surface.’” Pet. 64–65; Ex. 1006 ¶ 16.

Petitioner contends:

Because Nam’s contact pad is formed within and at the “interface” of its insulating layer 271, a POSITA would have understood that the “curved” “side surface” of Nam’s “second portion” (the top part of its contact pad) is in “contact” with the “side surface” of its “insulating layer” (the portion of insulating layer 271 adjacent to the contact pad) as this limitation requires.

Pet. 67 (emphases omitted).

Patent Owner responds that “Petitioner attempts to create a ‘side surface’ where Nam does not show one.” Prelim. Resp. 22. Pointing to Petitioner’s annotated version of Nam’s Figure 8A, Patent Owner argues that

“Petitioner identifies only an arbitrary section of the interlayer insulating layer 271 as part of the Petition’s identified ‘insulating layer,’” and “[n]either Petitioner nor Petitioner’s expert explain[s] why the blue ‘insulating layer’ depicted above purportedly stops where it does, or why a POSITA would draw the same conclusion.” *Id.* at 22–24 (citing Pet. 61, 67; Ex. 2007 ¶¶ 83–84). According to Patent Owner, “[t]his conclusory identification without evidentiary support cannot demonstrate a ‘side surface of the insulating layer’ that is in contact with the ‘curved side surface’ of a conductive layer.” *Id.* at 24.

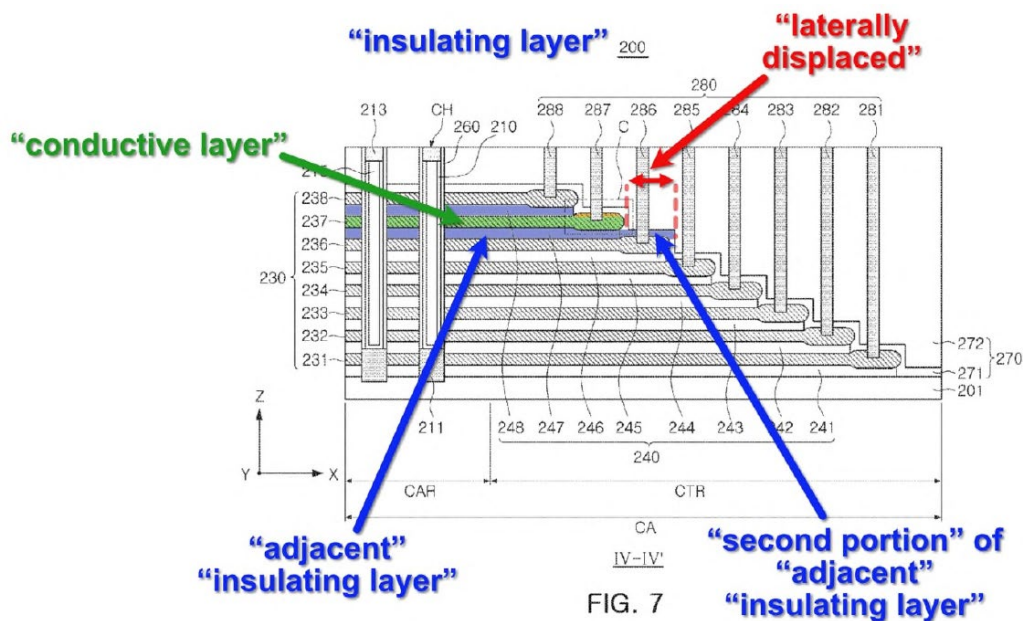
Based on the current record, we are persuaded that Petitioner sufficiently establishes that Nam teaches “a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer” as recited in claim 17. Petitioner identifies “insulating layer 240 *and* the adjacent insulating layer 271” as the recited “insulating layer.” Pet. 60 (emphasis added). Dr. Lee explains that interlayer insulating layer 271 “is formed along with the alternating stack of insulating and conductive layers and is used to form Nam’s contact pads,” and that “Nam’s contact pad does contact insulation layer 271.” Ex. 1003 ¶ 329. Dr. Lee also explains that only a portion of insulating layer 248 and interlayer insulating layer 271 is shaded blue in annotated Figure 8A of Nam to indicate the “side surface” of the “insulating layer” that is in “contact” with the “‘curved’ ‘side surface’” of the “‘second portion’ of ‘conductive layer.’” *Id.* ¶ 326. Petitioner, therefore, does not contend that Nam’s insulating layer extends only as far as the blue shading in annotated Figures 7 and 8A as Patent Owner asserts, but instead uses the blue shading to identify that part of the insulating layer Petitioner contends is in contact with the curved side surface of Nam’s pad region. The disclosures in Nam and Dr. Lee’s

testimony are sufficient to support Petitioner’s contention that Nam teaches the “a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer” limitation of claim 17.

Claim 19 further recites

wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack.

Ex. 1001, 16:8–14. Petitioner provides an annotated version of Nam’s Figure 7, reproduced below, to illustrate its contentions with respect to claim 19.



Annotated Figure 7 shows a schematic view of a memory device described in Nam, with Petitioner’s addition of blue shading and arrows identifying the “insulating layer,” “adjacent insulating layer,” and “second portion of adjacent insulating layer,” green shading and arrow identifying “conductive layer,” and a red dotted-line square described as “laterally

displaced.” Pet. 71 (citing Ex. 1006 Fig. 7; Ex. 1003 ¶¶ 344–345); Ex. 1006 ¶ 15. Petitioner contends that annotated Figure 7 shows “each of Nam’s ‘conductive layer[s]’ (such as layer 237) is located over ‘a first portion of the insulating layer of an adjacent layer stack’ (such as layer 247).” Pet. 70 (emphases omitted). Petitioner further contends that “each of Nam’s contact pads is formed within interlayer insulating layer 271” that “follows the ‘steps’ of Nam’s device,” which “causes a ‘second portion of the insulating layer of the adjacent layer stack’ (insulating layer 271 below the contact pad) to be ‘laterally displaced from the conductive layer’ (the lower layer 271 extends beyond the end of Nam’s conductive layer 237).” *Id.* at 70–71 (citing Ex. 1006 ¶¶ 67, 98–105, Fig. 7).

Patent Owner responds that Petitioner identifies “only insulating layer 248 as ‘the insulating layer’” but “identifies layer 247 and the entirety of layer 271 at that step as ‘the insulating layer of the adjacent layer stack,’” which Patent Owner argues is inconsistent and arbitrary. Prelim. Resp. 24–25. As explained above, however, Petitioner identifies the recited “insulating layer” as including Nam’s insulating layers 240 and interlayer insulating layer 271. *See, e.g.*, Pet. 60. Consistent with that identification, Petitioner further identifies “a first portion of the insulating layer of an adjacent stack” as recited in claim 19 as insulating layer 247, and “a second portion of the insulating layer of the adjacent layer stack” as recited in claim 19 as interlayer insulating layer 271 below the extending contact pad. *Id.* at 70–71; Ex. 1003 ¶¶ 342–345.

At this stage of the proceeding, Patent Owner does not address Petitioner’s specific contentions with respect to the other limitations of claim 19. *See* Prelim. Resp. We reviewed Petitioner’s contentions for all of the elements of claim 19, including the elements of claim 17 from which

claim 19 depends, and are persuaded, on this record, that Petitioner's discussion of the particular structures in Nam and the explanations in the Lee Declaration establish a reasonable likelihood that Nam teaches all of the limitations of claim 19.

F. Asserted Obviousness over Lee and Park

Petitioner contends that claim 19 would have been obvious over the combined teachings of Lee and Park. Pet. 72–89.

1. Overview of Lee

Lee relates “to a semiconductor device capable of easily forming a pad portion and a method of manufacturing the same.” Ex. 1007 ¶ 8. Lee's Figure 1A is reproduced below.

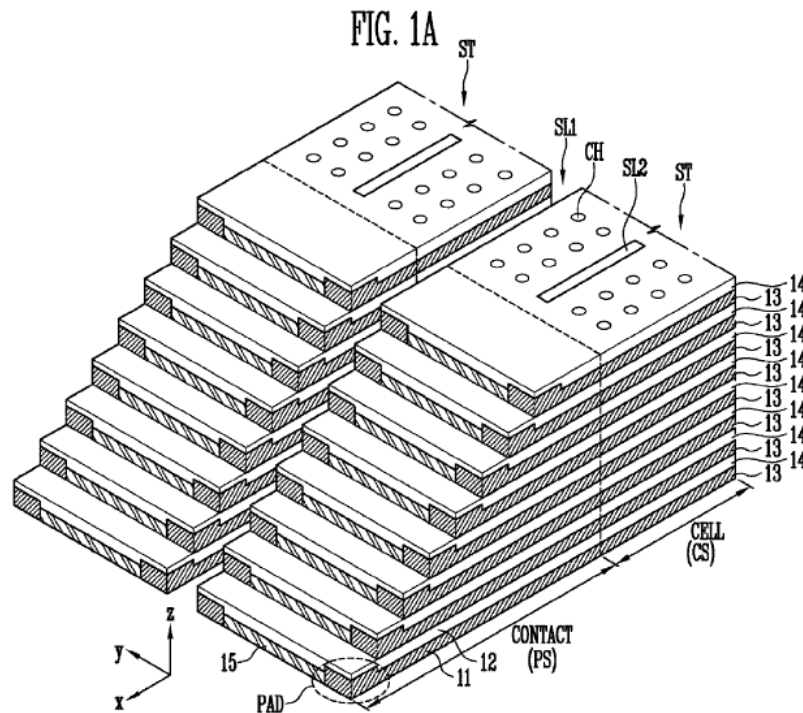


Figure 1A is a perspective view of the structure of a semiconductor device described in Lee. *Id.* ¶ 11. The semiconductor device includes cell region CELL and contact region CONTACT defined in a substrate (not shown). *Id.* ¶ 20. Stacked structures ST include conductive layers 11, 13 and insulating

layers 12, 14 that are formed alternately with each other on the substrate. *Id.* First slit SL1 separates neighboring stacked structures ST from each other. *Id.* An end of stacked structures ST is patterned stepwise, with each step including at least one conductive layer 11 or 13 and at least one insulating layer 12 or 14. *Id.* ¶ 21. Stacked structure ST also includes pad structure PS located in contact region CONTACT, and cell structure CS located in cell region CELL. *Id.* ¶ 22. Pad structure PS includes first conductive layers 11 and first insulating layers 12 that are alternately formed in contact region CONTACT, with an end of pad structure PS being patterned stepwise. *Id.* ¶ 23. Pad portions PAD are defined as portions of first conductive layers 11 that are exposed along the stepped end of pad structures PS. *Id.* Pad structures PS further include sacrificial layers 15 that are coupled to first conductive layers 11. Ex. 1007 ¶ 24. Lee teaches that, for example, first conductive layers 11 are stacked on side walls along the z-axis of pad structure PS exposed through first slit SL1, i.e., in the side regions thereof. *Id.* Sacrificial layers 15 are stacked along the z-axis in a central region of pad structure PS. *Id.* Lee further teaches that pad portion PAD may have a greater thickness than other unexposed portions of first conductive layer 11, and may have a greater thickness than second conductive layer 13 and sacrificial layer 15, such that “the thickness of the pad portion PAD may be selectively increased without increasing the height of the stacked structure ST.” *Id.* ¶ 27.

Cell structure CS includes second conductive layers 13 and second insulating layers 14 formed alternately with each other in cell region CELL. Ex. 1007 ¶ 25. First conductive layers 11 and second conductive layers 13 that are formed on the same level are coupled to each other, and first insulating layers 12 and second conductive layers 14 that are formed on the

same level are coupled to each other. *Id.* The semiconductor device further includes channel layers CH that penetrate cell structure CS and at least one second slit SL2 that penetrates cell structure CS. *Id.* ¶ 26.

2. Overview of Park

Park relates to a vertical semiconductor device in which memory cells are stacked in a direction perpendicular to a surface of a substrate. Ex. 1008, 1:12–16. Park teaches that the vertical semiconductor device is “capable of easily forming a connection wiring with a contact plug on each of [the] vertically stacked conductive layer patterns.” *Id.* at 1:26–29.

Figure 5 is reproduced below.

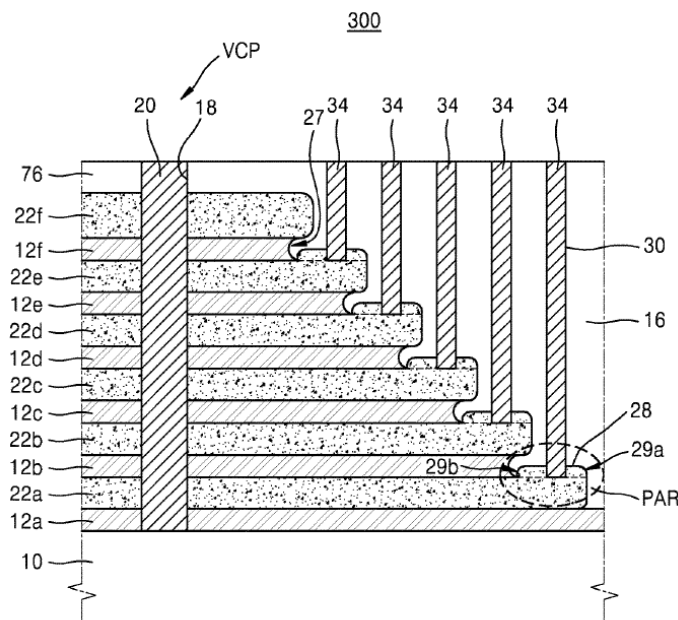


Figure 5 is a partial cross-sectional view of a connection region of a vertical semiconductor device described in Park. Ex. 1007, 2:11–13. Vertical semiconductor device 300 includes a stepped conductive structure in which interlayer insulating layer patterns 12a–12f and conductive layer patterns 22a–22f are repeatedly stacked on substrate 10 in a vertical direction. *Id.* at 6:7–11. Each of interlayer insulating layer patterns 12a–12f

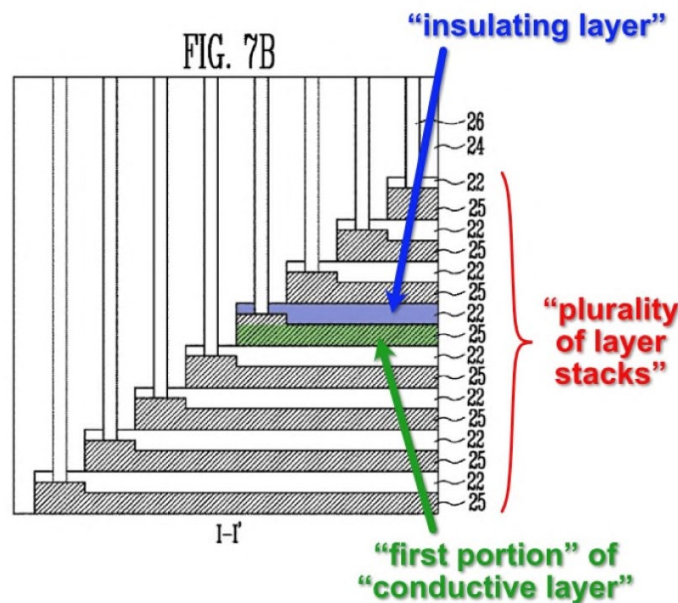
include recessed portion 27 recessed from a side wall of each of conductive layer patterns 22a–22f when recessed portion 27 is formed. *Id.* at 6:22–25. Park teaches that “[i]t may be advantageous to prevent a short circuit between the conductive layer patterns 22a through 22f when the recessed portion 27 is formed.” *Id.* at 6:25–28.

Vertical structure VCP including channel layer 20 is formed in hole 18 through interlayer insulating layer patterns 12a–12f and conductive layer patterns 22a–22f. Ex. 1008, 6:29–34. Each of conductive layer patterns 22a–22f has a pad region PAR in which a contact is formed on at least one edge. *Id.* at 6:43–45. Pad region PAR includes raised pad portion 28 protruding from a surface of each of conductive layer patterns 22a–22f. *Id.* at 7:4–6. Raised pad portion 28 extends in a horizontal direction of one side of each of interlayer insulating layer patterns 12b–12f. *Id.* at 7:6–8. End 29a of raised pad portion 28 extends farther than interlayer insulating layer patterns 12b–12e formed at a lower portion. *Id.* at 7:8–11. Raised pad portion 28 may partially overlap conductive layer patterns 22b–22f formed at an upper portion due to recessed portion 27, and may occupy the entire portion exposed by conductive layer patterns 22b–22f formed at an upper portion. *Id.* at 7:11–16.

Ends 29a and 29b of raised pad portion 28 are rounded. Ex. 1008, 7:17–18. Park teaches that “raised pad portion 28 may prevent a short circuit between the adjacent conductive layer patterns 22a through 22f when the other end 29b is rounded adjacent to the adjacent conductive layer patterns 22a through 22f.” *Id.* at 7:18–22.

3. *Claim 19*

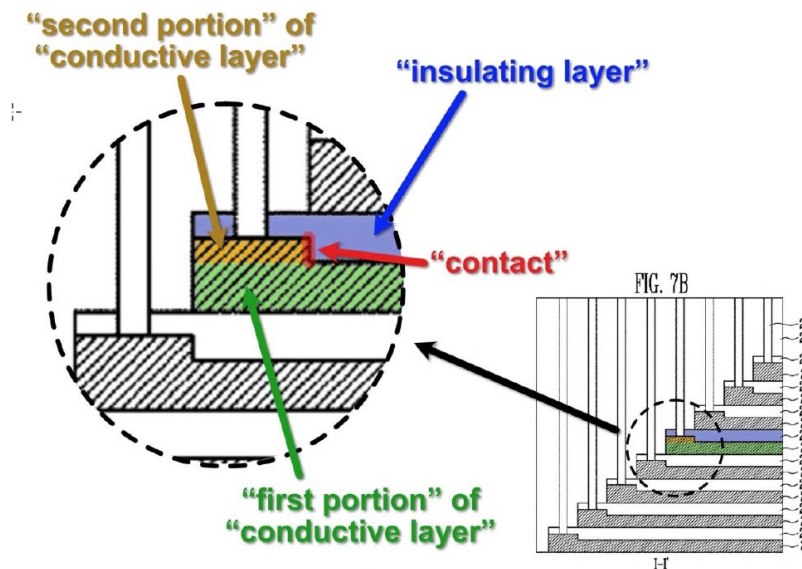
Claim 19 depends from, and includes all of the limitations of, claim 17. Ex. 1001, 16:8–14. Petitioner contends that Lee teaches most of the limitations of claim 17. Pet. 72–87. For example, Petitioner relies on the following annotated version of Lee Figure 7B to illustrate its contentions with respect to the “a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer” limitation of claim 17:



Annotated Figure 7B is a cross-sectional view of a portion of a semiconductor device during one step of the manufacturing process described in Lee, with Petitioner’s added annotations identifying second material layers 22 and conductive layers 25 as “plurality of stack layers,” adding blue shading to insulating layer 22 labeled “insulating layer,” and adding green shading to a portion of conductive layer 25 labeled “‘first portion’ of ‘conductive layer.’” Pet. 77 (citing Ex. 1008, Fig. 7B); Ex. 1008 ¶ 13. Petitioner contends that the combination of insulating layer 22 and conductive layer 25 forming a step is the claimed “plurality of layer stacks,”

and insulating layer 22 over the green portion of conductive layer 25 is the claimed “insulating layer disposed over a first portion of a conductive layer.” Pet. 76; Ex. 1003 ¶¶ 371–376.

Petitioner contends that Lee modified with Park’s teachings renders the “a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer” limitation of claim 17 obvious. Pet. 77. Petitioner identifies “pad portion PAD on the end of each of Lee’s conductive layer[s]” as “the claimed ‘second portion’ of a ‘conductive layer.’” *Id.* at 78 (citing Ex. 1007, Fig. 7B) (emphases omitted). Petitioner refers to the annotated version of Lee’s Figure 7B reproduced below to illustrate its other contentions with respect to this limitation.



Annotated Figure 7B is a cross-sectional view of a portion of a semiconductor device during one step of the manufacturing process described in Lee, with Petitioner’s addition of a dotted circle around a portion of the stepped end pointing enlarged view of the circled area. Pet. 79. Petitioner also added blue shading to insulating layer 22 labeled

“insulating layer,” green shading to a portion of conductive layer 25 labeled “‘first portion’ of ‘conductive layer,’” orange shading to pad portion PAD of conductive layer 25 labeled “‘second portion’ of ‘conductive layer,’” and a red line where pad portion PAD meets insulating layer 22 labeled “contact.” *Id.*; Ex. 1003 ¶ 384. Relying on this illustration, Petitioner contends that “the ‘side surface’ of the ‘second portion’ of Lee’s ‘conductive layer’ (Lee’s pad portion PAD) is in ‘contact’ with ‘a side surface of the insulating layer’ (insulating layer 22 in Figure 7B).” Pet. 79 (emphases omitted).

Petitioner further contends that “a POSITA would have considered it obvious to make the ‘side surface’ of Lee’s ‘second portion of the conductive layer’ ‘curved’ in view of Park’s teachings.” Pet. 82 (emphases omitted). Petitioner asserts that “each of Park’s electrodes terminates with a ‘pad region PAR’ that includes a ‘raised pad portion 28,’” and that, “[p]er Park, the ‘end 79b’ of this ‘raised pad portion 78’ may be ‘rounded’ to ‘prevent a short circuit’ between the pad and an ‘adjacent . . . conductive layer pattern 72c.’” *Id.* at 82–83 (citing Ex. 1008, 7:4–16, 11:35–41). Petitioner contends that a POSITA would have recognized that “each of Lee’s pad portions PAD is physically proximate to the adjacent conductive layer immediately above the pad,” which “creates a risk of short circuit in the event variances in the manufacturing process cause either the pad or the adjacent conductive layer to extend further than intended.” *Id.* at 85 (citing Ex. 1007, Fig. 7B; Ex. 1003 ¶¶ 416–419). Petitioner further contends that “[a] POSITA would have recognized that applying Park’s teachings and rounding the side of Lee’s pad portion PAD would have improved Lee—and limited the risk of short circuit—by increasing the minimum distance between the pad and the immediately adjacent conductive layer.” *Id.* at 85–86 (citing Ex. 1003 ¶ 420).

Patent Owner responds that it is “technically infeasible” to use Park’s process of using an oxidant gas to form a curved surface in Lee’s oxide-based insulating layer 22. Prelim. Resp. 28 (citing Ex. 2007 ¶¶ 90–91). In particular, Patent Owner argues that “introducing an oxidant to an oxide layer [would] not lead to oxide growth” or “to the rounding depicted inside already-existing solid oxide material.” *Id.* at 30 (citing Ex. 2007 ¶¶ 93–94). Therefore, according to Patent Owner, “a POSITA would have had no expectation of success in combining the methods” described in Lee and Park “as proposed.” *Id.* at 30–31.

On this record, we are persuaded that Petitioner, with supporting testimony from Dr. Lee, provides adequate reasons why a POSITA would have been motivated to round the side surface of Lee’s pad portion PAD as taught by Park. *See* Pet. 84–86 (and evidence cited therein). Petitioner also sufficiently establishes that a POSITA would have had a reasonable expectation of success in modifying Lee’s pad portion PAD to have a curved side surface as taught by Park because “numerous prior art references identified this type of pad as acceptable for three-dimensional memory devices with staircase structures,” “Lee explains that the shape of its pad portion PAD is controlled via an ‘ion implantation process,’” and “a POSITA would have recognized that this type of process could be readily adapted to form a curved contact pad.” Pet. 86–87; Ex. 1003 ¶¶ 426–429.

We acknowledge that Patent Owner disagrees, but find that Patent Owner’s disagreement raises issues of fact that are best resolved on a full trial record. Accordingly, we find that Petitioner sufficiently shows that a POSITA would have reason to combine the disclosures set forth in Lee and Park with a reasonable expectation of success of arriving at the claimed subject matter. *See* Pet. 84–87.

At this stage of the proceeding, Patent Owner does not address Petitioner's specific contentions with respect to the limitations of claim 19. *See* Prelim. Resp. We reviewed Petitioner's contentions for all of the elements of claim 19, including the elements of claim 17 from which claim 19 depends, and are persuaded, on this record, that Petitioner's discussion of the particular structures in Lee and Park and the explanations in the Lee Declaration establish a reasonable likelihood that Lee and Park teach all of the limitations of claim 19. *See* Pet. 72–89.

III. CONCLUSION

Based on the arguments in the Petition and the Preliminary Response, and the evidence of record, we determine that Petitioner establishes a reasonable likelihood that it will prevail on its challenge to claim 19 of the '666 patent. We also determine that the arguments and evidence of record do not support discretionary denial of the Petition under 35 U.S.C. § 314(a). Accordingly, we institute an *inter partes* review of claim 19 on all the challenged grounds.

The factual findings set forth in this Decision are preliminary and provided for the sole purpose of deciding whether to institute a review. Any final findings will be based on the full trial record, including any information presented in a timely filed response to the Petition. *See Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (noting that “there is a significant difference between a petitioner's burden to establish a ‘reasonable likelihood of success’ at institution, and actually proving invalidity by a preponderance of the evidence at trial”) (quoting 35 U.S.C. § 314(a); comparing *id.*, with § 316(e)).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review is instituted with respect to all the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

IPR2025-00189
Patent 11,145,666 B2

For PETITIONER:

K. Patrick Herman
Jeremy Jason Lang
ORRICK, HERRINGTON & SUTCLIFFE LLP
p52ptabdocket@orrick.com
ptabdocketjjl2@orrick.com

For PATENT OWNER:

Inge A. Osman
Brenda L. Danek
Steven W. Peters
Amit Makker
LATHAM & WATKINS LLP
inge.osman@lw.com
brenda.danek@lw.com
steven.peters@cgsh.com
amit.makker@lw.com