

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case No. IPR2025-00189
U.S. Patent No. 11,145,666

REPLY DECLARATION OF DR. JACK C. LEE

I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron” or “Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to reply to certain of the positions set forth in Patent Owner’s Response (Paper 25) and opinions in a September 2, 2025 declaration of Konstantinos Giapis submitted by Patent Owner in an *inter partes* review proceeding relating to U.S. Patent No. 11,145,666, which I refer to herein as the ’666 patent.

3. I am being compensated at my current standard consulting rate, plus reimbursement for any reasonable expenses. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

4. The prior declaration I submitted in connection with this proceeding, which I understand has been designated as Ex. 1003, sets forth among other topics my educational background and professional experience (Ex. 1003, ¶¶ 5-13 and associated Exhibit 1004), my understanding of the law (*id.*, ¶¶ 18-33), an overview

of pertinent technical background (*id.*, ¶¶ 39-61), an overview of the '666 patent and its prosecution history (*id.*, ¶¶ 62-93), the knowledge and characteristics of a person having ordinary skill in the art (*id.*, ¶¶ 34-38), and certain claim construction opinions (*id.*, ¶¶ 94-97).

5. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, my work with those of ordinary skill at the time of the alleged invention, and my general experience in the field of art.

6. I have also reviewed and considered the materials listed in my prior declaration (*id.*, ¶ 17), the Board's Institution Decision (Paper 19), Patent Owner's Response (Paper 25), the transcript of my deposition in this proceeding (Ex. 2010), the Giapis Declaration (Ex. 2023), and the following materials to the extent relevant to my opinions:

Exhibit	Description
1024	Excerpt from the <u>Merriam Webster Dictionary</u> (1998)
1025	Falcony, <u>Characterization of Excess Si in Nonstoichiometric SiO₂ Films by Optical and Surface Analysis Techniques</u> , J. Electrochem. So., Vol 144, No. 1, 379-383 (Jan 1997)
1026	Bedjaoui et al., <u>Si nanocrystal-containing SiO_x (x<2) produced by thermal annealing of PECVD realized thin films</u> , Materials Science and Engineering B 124-125, 508-512 (2005)
1028	Transcript of the November 12, 2025 Deposition of Konstantinos Giapis
1029	U.S. Patent No. 9,728,547 to Ohsaki et al.

2008	James D. Plummer et al., SILICON VLSI TECHNOLOGY: FUNDAMENTALS, PRACTICE AND MODELING (Prentice Hall Elecs. & VLSI Series) (Charles Sodini ed. 2000) (excerpts)
2009	U.S. Patent Application Publication No. 2018/0301460 A1 (“Yoo”)
2020	3D FLASH MEMORIES (Roni Micheloni ed. 2016) (“Micheloni”) (excerpt)
2021	Counterpoint Tech. Mkt. Rsch., Scaling to 1,000-Layer 3D NAND in the AI Era (July 2024), https://filecache.mediaroom.com/mr5mr_lamresearch/182770/Counterpoint_Research_Paper_Scaling_to_1000-Layer_3D_NAND_in_the_AI_Era.pdf (“Counterpoint”)
2022	Steven S. Zumdahl et al., CHEMISTRY: AN ATOMS FIRST APPROACH (3d ed. 2021) (excerpt)

II. RESPONSE TO CERTAIN OF PATENT OWNER’S ARGUMENTS

7. The paragraphs below respond to certain of the arguments and assertions made by Patent Owner and Dr. Giapis in this proceeding. In these paragraphs, I address only a fraction of the opinions and assertions Dr. Giapis set forth in his declaration. The fact that I do not respond to any particular opinion expressed by Dr. Giapis should not be considered to indicate agreement with that opinion

A. Construction of “Side Surface”

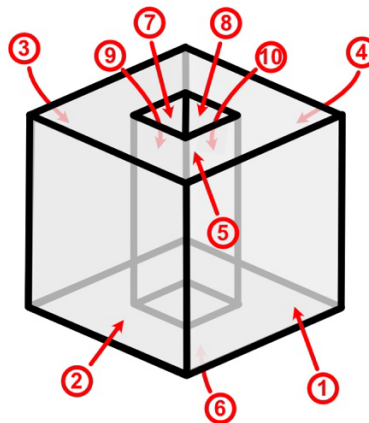
8. Dr. Giapis includes a lengthy discussion of meaning of the term “side surface” in the ’666 patent claim limitation requiring “wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.” *See* Ex. 2023, ¶¶ 40-61.

9. As I explained in my opening declaration, the '666 patent's claim terms do not require further construction and can instead be afforded their plain and ordinary meaning. *See* Ex. 1003, ¶ 97.

10. This includes the term “side surface.” The term is readily understandable, and would be understood to refer to any of the bounding surfaces of a three-dimensional structure.

11. I repeatedly explained this to Patent Owner's counsel during my prior deposition, noting that “three-dimensional structure[s]”—like the '666 patent's conductive and insulating layers—include “many sides.” Ex. 1017, 71:3-72:14, 79:18-80:16, 101:17-102:10. Every one of these many sides is a “side surface.” This includes the top, bottom, front, back, lateral sides, any interior sides, and so on.

12. For instance, the example three-dimensional shape shown below has a total of 10 side surfaces (the top, bottom, four lateral surfaces, and the four surfaces bounding the hole through the shape's middle):



13. This, in my opinion, is entirely consistent with the plain and ordinary meaning of the term “side surface.” A POSITA would have understood a “side” (and relatedly a “side surface”) when referring to a three-dimensional object to refer to any “outer surface of [the] object.” Ex. 1024 at 483.

14. Dr. Giapis does not apply the plain and ordinary meaning of “side surface” in his declaration. Instead, he reads a number of narrowing limitations into the term that depart significantly from that plain and ordinary meaning.

15. According to Dr. Giapis, a “side surface” must be “vertical.” *See, e.g.*, Ex. 2023, ¶ 41. The “curved side surface” must also be curved “along” the “z-axis.” *Id.*, ¶ 40. Further, the “side surface” of the claimed “insulating layer” must be at the very end of the insulating layer, and not what Dr. Giapis calls an “internal or inner surface.” *Id.*, ¶ 84. A POSITA, however, would recognize that internal or inner sidewalls exposed by etching, selective removal, or partial deposition are still “side surfaces” of a three-dimensional structure and are routinely treated as such in semiconductor processing (for example, in STI trenches, dual-damascene vias, and other embedded structures).

16. Not only does Dr. Giapis’s understanding of “side surface” depart from the plain and ordinary meaning of the term, but it finds no support in claims, specification, or prosecution history.

17. In particular, claim 17 (on which claim 19 depends) requires only a landing pad (referred to as a “second portion of the conductive layer”) with “a curved side surface” that contacts a “side surface” of the “insulating layer.” ’666 patent, claim 17. The claim does not use the words “vertical” or “z-axis.” The claim also does not mention (or exclude) “internal” or “inner” insulating layer surfaces.

18. Dr. Giapis notes in his declaration that claim 17 also references “a top surface” of the claimed “substrate.” *See* Ex. 2023, ¶ 42. This, however, does not redefine or change the meaning of the term “side surface.” The applicant plainly could have claimed a “side surface” that is oriented in a particular way relative to the “top surface” (i.e., the claim could have specified that the “side surface” is “perpendicular” to the “top surface” of the substrate). But the applicant did not do so. Thus, “side surface” must continue to have its plain and ordinary meaning.

19. Dr. Giapis also references the limitations in claim 1 and 2 specifying that the “landing pad” of those claims includes a “bottom surface,” “a top surface,” a “first side surface,” and a “second side surface.” This, in my opinion, also does not redefine or change the meaning of the term. *Id.*, ¶ 43. Instead, it once again merely shows that the applicant knew how to craft a claim that excludes the top and bottom surfaces of a layer from the scope of the term “side surface” (this is accomplished by specifying that the layer has a “top,” “bottom,” and “side” in the same claim). The applicant chose not to do so in claim 17, referencing only a “side

surface.” It follows that the term “side surface” must include not only the lateral surfaces, but also the top and bottom surfaces of a layer.

20. The specification of the ’666 patent also does not require any of the narrowing limitations Dr. Giapis seeks to impose. According to Dr. Giapis “the ’666 patent refers to a ‘side’ surface (without the modifier ‘top’ or ‘bottom’) 53 times, each time referring to a vertical surface.” *Id.*, ¶ 44. Dr. Giapis quotes certain of these references to the term “side” in his declaration. *Id.*, ¶¶ 45-55. In each and every case, however, the specification merely references “a side.” In other words, the referenced “side” is simply one of the many sides of the layer being discussed in the ’666 patent. And a POSITA would also recognize that even though the figures depict vertically oriented surfaces, those drawings are merely illustrative examples, and a POSITA would not import an orientation requirement (e.g., “vertical”) into the claim term “side surface” based solely on the way a figure is drawn.

21. The patent does not redefine the term “side” to be just a vertical surface (or just a surface curved in the z-axis direction). Instead, it simply notes (correctly) that the vertically oriented surfaces of the layers making up its staircase structure are the layers’ “sides.” The top and bottom are also “sides.” In fact, the ’666 patent says this explicitly, noting that its “layer[s]” include both a “top side” and “bottom side.” ’666 patent, 4:36-40 (emphasis added). The specification also explains that the “phraseology and terminology” it uses “is for the purpose of description and not

of limitation...” *Id.*, 13:19-24 (emphasis added). This further confirms that the ’666 patent did not intend to redefine the term “side surface” in the narrow way discussed throughout Dr. Giapis’s declaration.

22. Next, the ’666 patent defines both the term “horizontal” (“nominally parallel to a lateral surface of a substrate”) and “vertical” (“nominally perpendicular to the lateral surface of a substrate”). ’666 patent, 5:3-13. Terms like these plainly could have been included in claim 19. For instance, if the applicant wanted to limit “side surface” to just a vertical surface, the claim could have included the word “vertical” or the phrase “nominally perpendicular” in reference to the substrate’s top surface. The fact that this type of language is missing—despite the fact that the applicant went to the trouble to include it in the specification—would strongly indicate to a POSITA that the claims are not limited in the way Dr. Giapis argues.

23. Dr. Giapis also takes the position that “[t]he methods of manufacturing taught by the ’666 patent form a curved side surface that is a ‘vertical surface curved along a direction (e.g., the z-axis) perpendicular to the top surface of the structure.” Ex. 2023, ¶ 56. Per Dr. Giapis, “there is no process described in the ’666 patent for curving the surfaces of the landing pads in connection with the insulating layers in the x-y plane.” *Id.*, ¶ 57.

24. In my opinion, there are numerous problems with this opinion.

25. First, the '666 patent includes no views of its memory device in the x-y plane. Thus, it is not possible to state—as Dr. Giapis does—that the patent lacks a “curved side surface” in this plane. The patent does not say one way or the other.

26. Second, it is not true that the “methods of manufacturing” set forth in the '666 patent produce only a surface that is curved along the z-axis. Dr. Giapis references the '666 patent's figures (which he believes show a “curved side surface”) and the specification's discussion of “poor step coverage” to conclude that a POSITA would have “select[ed] and optimize[d] specific gas-phase deposition techniques capable of supplying both directional and isotropic fluxes of depositing molecules to the staircase structure, such as plasma-enhanced CVD and directional sputter deposition (PVD) among others.” Ex. 2023, ¶ 32. By “carefully balance[ing]” these “two flux components,” a “surface curvature in the vertical direction” is supposedly produced. *Id.* In any event, claim 19 is directed to the resulting apparatus, not to any particular manufacturing recipe, and a POSITA would understand that the claimed “curved side surface” limitation describes the structure of the conductive layer, not a specific way of depositing or etching films to achieve that structure.

27. The '666 patent says none of this. It does not use the word “curved.” It does not discuss “flux components.” It does not mention “directional” or “isotropic fluxes.”

28. Further, the patent does not even limit itself to techniques “such as plasma-enhanced CVD and directional sputter deposition (PVD).” Instead, it states that its layers can be formed using other techniques, such as “low pressure CVD (LPCVD)” and “atomic layer deposition (ALD)” along with “any suitable deposition techniques or combinations thereof.” ‘666 patent, 9:2-7; *see also id.*, 2:39-45.

29. Deposition techniques like LPCVD and ALD—by themselves—will not produce a vertically curved landing pad side surface like that shown in the ‘666 patent’s figures. These techniques can, however, produce landing pads that are curved in the x-y plane (using an appropriate shaped mask during deposition). Moreover, “poor step coverage” is a descriptive term for non-conformal thickness distribution and does not impose any particular direction of curvature. A POSITA would understand that non-conformal deposition can produce curvature in different directions depending on feature geometry, shadowing, and mask shape, rather than only in the z-direction.

30. This is reflected in Plummer textbook (Ex. 2008) that Dr. Giapis cites. In particular, Plummer explains that “CVD has historically been used in the integrated circuit industry mainly for silicon and dielectric deposition, primarily due to its good quality films and good step coverage[.]” Ex. 2008, 511. And LPCVD deposition processes in particular are designed such that “equal fluxes of reactant gases ... reach every location in order to achieve uniform depositions.” *Id.*, 525.

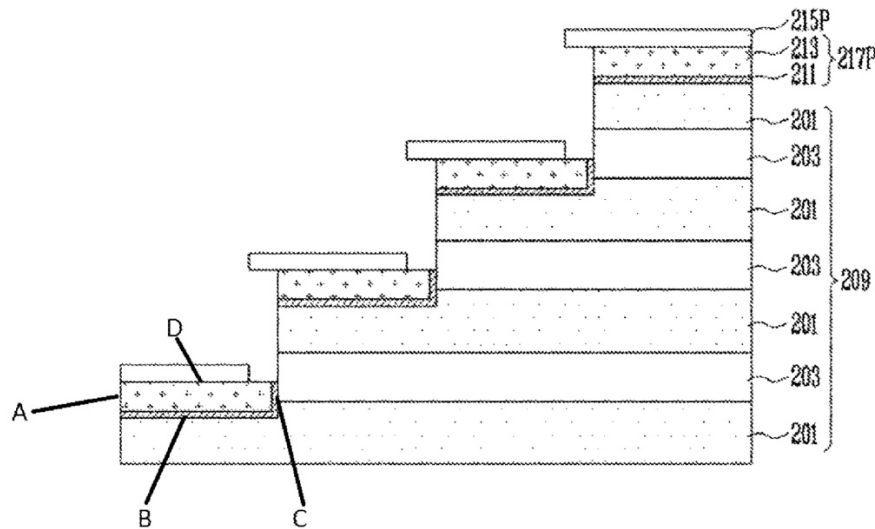
Thus, use of a LPCVD process will produce good step coverage (and no curve in the z-axis direction), not poor step coverage. ALD similarly produces conformal step coverage and also will not produce a curve in the z-axis direction. Both methods, however, can produce a curve in the y-axis direction. This, in my view, further confirms that the claims cannot be properly limited to just “curved side surfaces” that curve in the z-axis direction. Instead, the claims also embrace surfaces that curve in other directions, including the y-axis direction.

31. Dr. Giapis also states that he “reviewed the prosecution history and saw nothing that would change my opinions.” He appears to have missed that there is a discussion of the meaning of the term “side.”

32. During prosecution of one of the '666 patent's parent applications (U.S. App. 16/126,956, which led to U.S. Patent No. 10,680,003), the applicant was pursuing claims directed to a “semiconductor structure” with a “landing pad” having a “first side surface and a second side surface.” Ex. 1014, pp. 241-242.

33. The examiner rejected the claims in view of the following prior art memory staircase structure:

FIG. 2E



Id., p. 270.

34. In discussing the structure shown in this figure, the examiner explained that the memory staircase includes a “landing pad” with “4 side surfaces: A, B, C, and D.” *Id.*, p. 269. “Sides B and D” (the top and bottom) corresponded to the claimed “side surface[s].” *Id.*

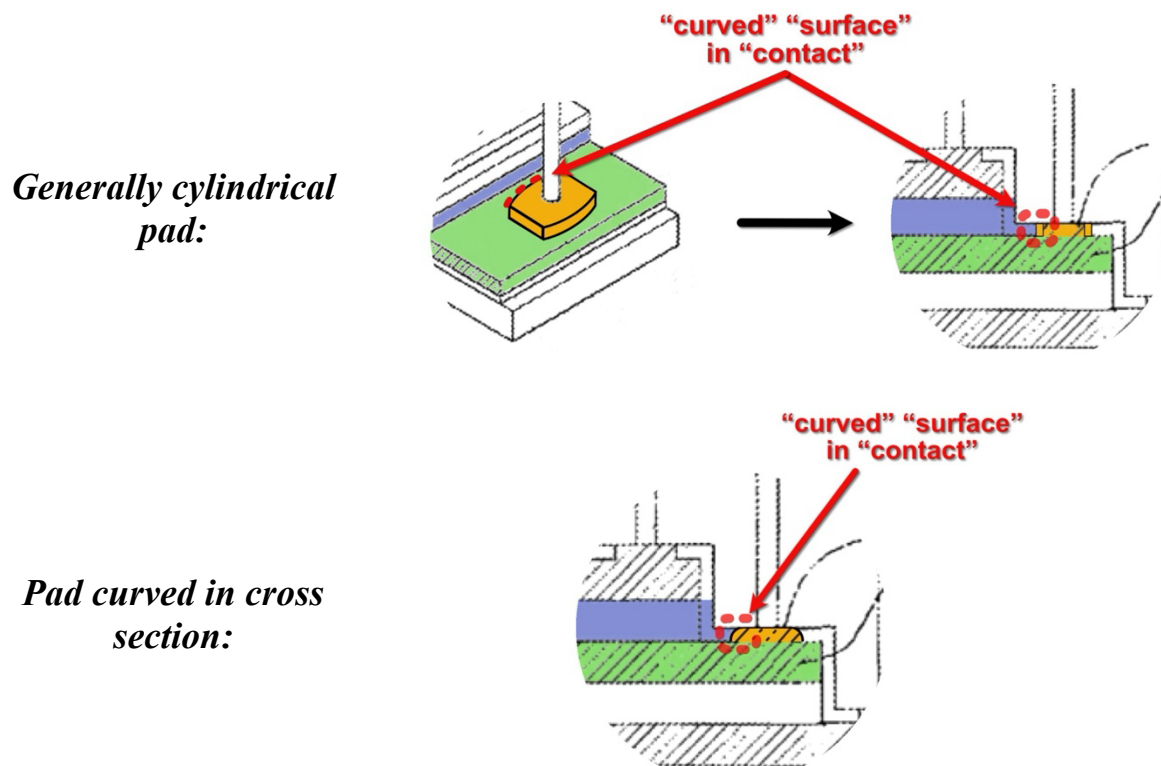
35. The applicant did not dispute the Examiner’s characterization of the landing pad’s top and bottom as “side surfaces.” *See id.*, pp. 282-290. Instead, it amended the claims to require that the claimed “side surface[s]” be surfaces that are “substantially perpendicular to the top surface” of the substrate. *Id.*, pp. 284-285 (emphasis added).

36. No such limitation is present in the ’666 patent claims: while the claims could have specified that each “side surface” is “substantially perpendicular” to the

substrate's top surface, they do not. This, in my opinion, further confirms that it would be improper to construe "side surface" in a way that departs from its plain and ordinary meaning.

B. Ground 1: Obviousness Over Kim

37. In my original declaration, I explained that Kim (Ex. 1005) discloses two types of landing pads with "curved" surfaces: (1) generally cylindrical pads that are curved when viewed from above and (2) pads that are curved when viewed in cross section. Examples of these are shown in the demonstrative figures below:



38. As I explained in my declaration, both types of pad satisfy claim 19. See Ex. 1003, ¶¶ 202-248.

39. Dr. Giapis argues that the first type of pad (the generally cylindrical pad) does not fall within the scope of the claims because (1) it is curved in the x-y plane and not the x-z plane and (2) the contact between the curved surface and Kim's insulation layer 122 occurs at what Dr. Giapis calls an "internal" or "inner" surface.

40. Neither argument distinguishes Kim. As I explain above in Section II.A (discussing claim construction), the "curved side surface" can be curved in any plane, including the x-y plane. And the "side surface" of the claimed "insulating layer" that contacts the "curved side surface" of the landing pad can be any side surface, including internal or inner side surfaces.

41. According to Dr. Giapis, the second type of pad I mentioned in my declaration—one curved when viewed from the side — "cannot be formed" using the manufacturing process that Kim expressly discloses. Ex. 2023, ¶ 100. Dr. Giapis does not dispute that this type of pad includes a "curved side surface" as claimed.

42. As I noted in my original declaration, pads that are curved when viewed from the side are disclosed in numerous prior art references, including Park (Ex. 1008), Nam (Ex. 1006), and Yun (Ex. 1018). For example, Park teaches rounding through an additional oxidation step, Nam teaches rounding through post-implantation heat-induced spreading, and Yun teaches similar curved pad geometries. *See* Ex. 1003, ¶¶ 204-211.

43. Not only do these references provide examples of memories that employ landing pads with curved side surfaces when viewed in cross-section, but they explain how such a pad can be manufactured. Each of these references teaches a practical, well-established technique for producing rounded or curved pads.

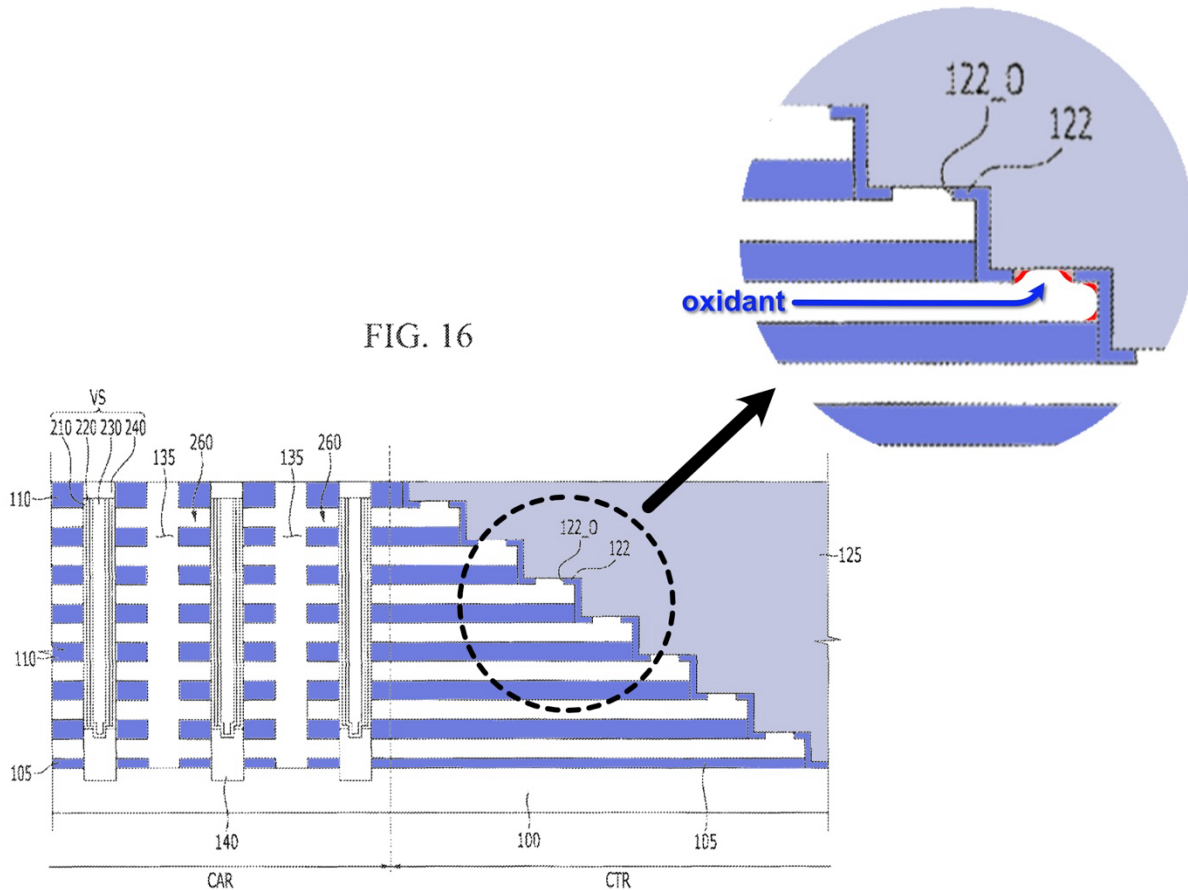
44. As I previously noted, a POSITA would have recognized that these pad manufacturing methods are readily applicable to Kim. *See id.*, ¶¶ 226-238.

45. For example, Park teaches that a rounded pad can be achieved by performing an additional “oxidation” step during the pad formation process. *See* Park, 7:17-29, 8:33-49.

46. A POSITA would have understood that Kim is readily modifiable to produce rounded landing pads (with curved side surfaces) following this same approach, because Park’s oxidation-induced rounding process is additive, occurs preferentially at exposed corners, and can be incorporated into Kim’s sequence without altering Kim’s overall architecture or fabrication objectives.

47. In particular, after Kim’s sacrificial layers are removed (along with the area 122_I where ion implantation occurred), an oxidant would be introduced into the space between the remaining oxide layers (shown in blue below). This oxidant would further oxidize excess silicon present in the oxide layer resulting in the formation of additional silicon oxide (shown in red below).

48. Further oxidation would occur and silicon oxide would form preferentially in the corners and exposed edges of the oxide layers:

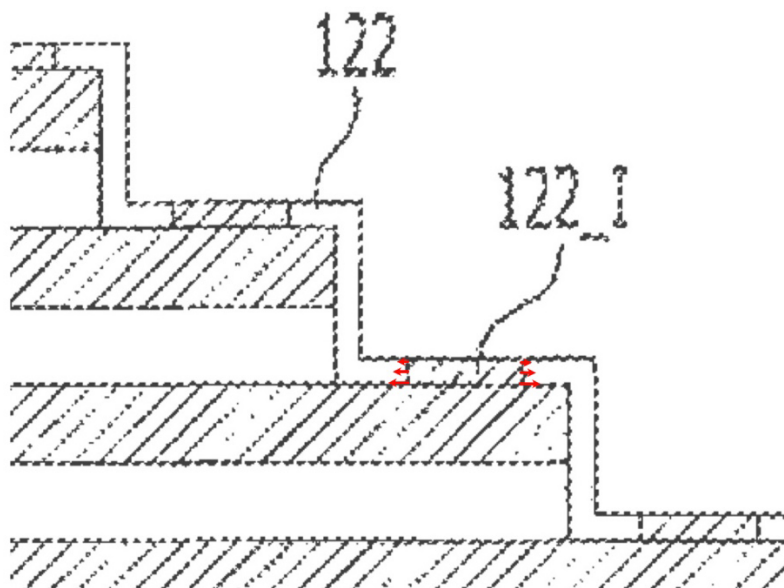


49. As I discuss below in connection with the Lee reference, a POSITA would have recognized (and considered it obvious) to achieve rounding by further oxidizing an existing oxide layer like that taught by Kim. Dr. Giapis's opinion to the contrary is incorrect and unsupported.

50. Alternatively, a POSITA would have considered it obvious to employ Nam's process to obtain landing pads with curved side surfaces in Kim.

51. As I explained in my opening declaration, Kim already shapes its contact pad by performing ion implantation on the areas 122_I of its insulating layer 122. *See* Ex. 1003, ¶¶ 230-234. To achieve a rounded contact pad, all that is required is a minor adaptation or tailoring of this ion implantation step via an additional heating step. As Nam explains, application of heat after ion implantation causes the damaged region to spread, resulting in curved contact pad. *See* Nam, ¶ [0060] (after ion implantation, “[t]he impurity doped” in the target areas, including the “interlayer insulating layers[,]” “may be spread due to heat applied thereto in a subsequent process”).

52. An example of this is shown below. Application of heat will cause the impurities implanted in Kim’s insulating layer 122 in area 122_I to spread, resulting in a damaged region with a rounded shape (and curved side surfaces). The spread is indicated with small red arrows. This in turn will produce a rounded landing pad like that depicted in Nam:



Kim, Fig. 13 (excerpted and annotated).

53. Dr. Giapis argues that the processes used by references like Park and Nam are “fundamentally different” from that in Kim. Ex. 2023, ¶ 92. This is not the case.

54. Kim, Park, and Nam all teach 3D memory structures. *See* Kim, Fig. 3, 1:28-30; Park, Fig. 1, 1:12-22; Nam, Fig. 2, ¶ [0003]. They all also reference various types of curved landing pads. Kim, 8:29-34; Park, 8:37-42; Nam, ¶¶ [0066], [0077]. And they all employ ion implantation during the formation of these pads. *See* Kim, 13:1-11; Park, 7:17-29; Nam, ¶¶ [0066], [0098]-[0107].

55. Park and Nam are thus not “fundamentally different” from Kim. Instead, all that is required to generate a rounded landing pad using Kim’s existing process is (1) an extra oxidation step (when Park’s rounding approach is employed)

or (2) an extra heating step (when Nam’s rounding approach is employed). This is simple, straightforward design work that is well within the capabilities of a POSITA. A POSITA also would have fully expected either approach to succeed when applied to Kim (as both approaches were demonstrated to successfully produce rounded landing pads in both Park and Nam). In practice, semiconductor engineers routinely adapt individual process steps — such as oxidation steps that promote rounding, or post-implant anneals that promote diffusion — from one flow to another, and a POSITA would not view differences in overall device layout as a reason to ignore well-understood rounding techniques taught in Park and Nam.

56. In sum, Dr. Giapis’s opinion appears to require the bodily grafting of Park and Nam into Kim, as opposed to the straightforward and obvious adaptation of Kim that a POSITA would have performed following the teachings of the prior art.

57. Dr. Giapis also takes the position that use of Nam’s pad rounding method “would negate some of Kim’s advantages.” Ex. 2023, ¶ 110. According to Dr. Giapis, increasing the pad size via a heating step would bring them closer to adjoining conductive structure and be contrary to Kim’s purported instruction to “precisely control[] the location” of its landing pads. *Id.* I disagree with both points.

58. Kim explains both that its pads can have different widths (Kim, 11:57-12:7) and different shapes (*id.*, 8:29-34). A POSITA would have understood that a

rounded contact pad that is slightly wider than a square or rectangular pad is one of the shapes Kim contemplates for use. Moreover, a rounded pad would have provided two clear benefits: (1) the bottom of the pad would be wider, thus producing a more extensive thicker area for purposes of preventing contact punch-through during manufacture while (2) the top of the pad would be narrower, which would increase the distance between the pads and adjacent conductive structures.

59. Next, Kim does not use the word “precise,” or state anywhere that its pad formation process is intended to produce “precisely” shaped pads. Again, as I note immediately above, Kim is open to various different pad shapes and sizes (including pad shapes that vary from step-to-step).

60. Dr. Giapis also takes the position that a POSITA would not have been motivated to employ a rounded pad with Kim because “Kim already has numerous features that address and solve” the “short-circuit problem.” Ex. 2023, ¶ 88. This is also wrong.

61. To address the potential short circuit problem between conductive structures in its memory, Kim adjusts the size, shape, and positioning of its pads. *See* Kim, 9:46-49 (noting that Kim’s pad can be sized and located “inside from the edge surface” of the base pad “to prevent ... short-circuit”). It also adds thickened layers of insulation around the pad. *See id.*, 9:50-55 (“auxiliary insulating layer 122”

is “positioned between ... adjacent protrusion pads”), 9:7-11 (insulation “thickness” is increased to “prevent[] ... short circuit”).

62. A POSITA would have recognized that rounded landing pad (with curved side surfaces) operates to increase the distance between the landing pad and adjacent conductive structure.

63. A rounded landing also—because it is further away—increases the thickness of insulation surrounding the landing pad.

64. In other words, a POSITA would have recognized that a rounded landing pad not only furthers Kim’s goal to avoid short circuits, but does so in a way that is both consistent with Kim and amounts to nothing more than an extension of the short-circuit preventing approaches Kim already employs. This is why a POSITA would have been motivated to employ a rounded pad with Kim: it assists in solving a problem Kim identifies (potential short circuits) and does so in a way Kim itself identifies as a potential solution (increasing distance and insulation between conductive structures). Even if Dr. Giapis’s narrow view were adopted and the “curved side surface” had to be curved only in the z-direction (which I do not agree with), claim 19 would still be obvious. Park’s oxidation and Nam’s annealing both create vertical curvature at exposed corners, and a POSITA would expect the same result when applied to Kim’s pads. Thus, even under Patent Owner’s

construction, the prior art still yields a pad with a curved side surface in contact with the insulating layer, as claim 19 requires.

C. Ground 2: Obviousness Over Nam

65. My original declaration also explained why Nam renders the '666 patent's claims obvious. *See* Ex. 1003, ¶¶ 259-349.

66. In response, Dr. Giapis argues that I presented “changing theories” regarding what constitutes the claimed “insulating layer” in Nam when annotating Nam's figures. *E.g.*, Ex. 2023, ¶ 117.

67. This appears to misunderstand the purpose of the figures in my first declaration. Each annotated figure addresses a different claim limitation (and thus highlighted the portion of the “insulating layer” pertinent to that claim limitation).

68. One figure shows why Nam includes an “insulating layer” that is “disposed over a first portion of a conductive layer” and part of a “layer stack.” *See* Ex. 1003, ¶ 294. Here, alternating layers of insulation and conductive materials forming Nam's stack are highlighted. *Id.*

69. Another figure shows why Nam's “insulating layer” includes a “side surface” in “contact” with the “curved side surface” of a conductive landing pad. *Id.*, ¶¶ 315, 326. Because of this, the portion of the insulating layer contacting Nam's pad is highlighted. *Id.*

70. Yet another figure shows why Nam includes an “adjacent” “insulating layer” in its stack. *Id.*, ¶ 343. As a result, the adjacent layer is highlighted. *Id.*

71. And another figure addresses the limitation requiring an adjacent layer of insulation including a “second portion” that is “laterally displaced” from the “conductive layer.” *Id.*, ¶ 345.

72. There is nothing inconsistent about this: in all cases the “insulating layer” is both Nam’s layer 248 (which is one of Nam’s layers 240) and the adjacent portion of layer 271. I have simply highlighted different portions of this same structure in different figures for emphasis purposes.

73. I also note that I explained in words what constitutes the “insulating layer” in Nam: it is “insulating layer 248 and the adjacent portion of layer 271.” *Id.*, ¶ 291.

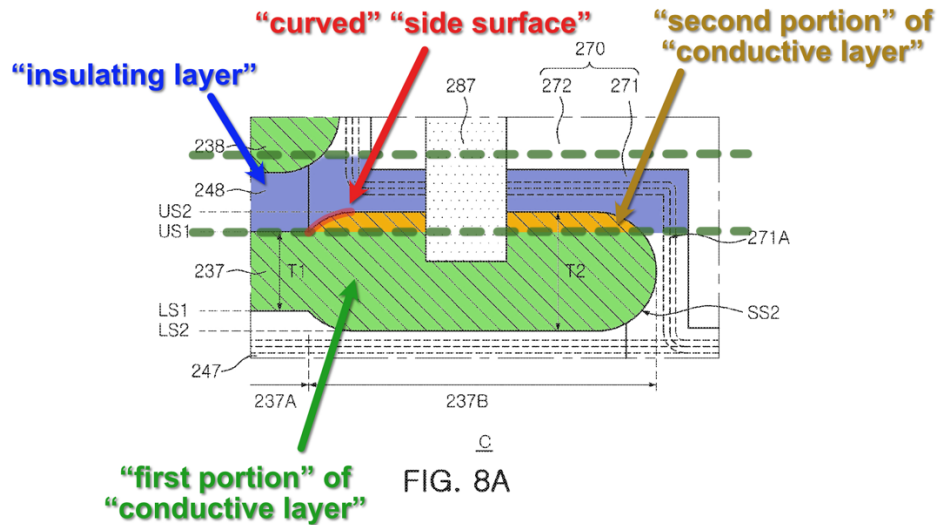
74. According to Dr. Giapis, this “insulating layer” identification is improper because it is “arbitrary.” Ex. 2023, ¶ 114.

75. There is nothing “arbitrary” about my identification. As I have already explained, layer 248 and 271 together constitute the claimed “insulating layer” because they (1) are located between the planes formed by adjacent “gate electrode layers 230,” (2) cooperate on a layer-by-layer basis to define Nam’s landing pads, and (3) are both formed from the same insulating material making them a continuous

structure. Ex. 1003, ¶¶ 287-290. So, Nam itself provides a basis for identifying both layer 248 and 271 as together forming an “insulating layer.”

76. Moreover, my identification of an “insulating layer” simply follows the ’666 patent’s instruction regarding what constitutes a “layer.” Per the patent, a “layer” may be “homogenous” or “inhomogeneous,” can include “multiple layers,” and can be the material located “between any set of horizontal planes.” ’666 patent, 4:36-45. A POSITA applying that definition would consistently treat Nam’s insulating material between two such planes as a single “layer,” rather than alternately including or excluding portions of layer 271 depending on which characterization is more favorable to a particular non-obviousness argument, as Dr. Giapis does.

77. The blue highlighted “insulating layer” in Nam is such a “layer.” As shown, layer 248 and the adjacent portion of layer 271 (both annotated blue) form a continuous structure and are located between the planes (indicated by dark green dashed lines) formed by the bottom surface conductive layer 238 (annotated lighter green) and top surface of conductive layer 237 (also annotated lighter green):



78. The rest of Dr. Giapis’s arguments regarding Nam rely on his erroneous construction of the term “side surface.” Dr. Giapis misreads the claims as I have already explained above. *See* above Section II.A.

D. Ground 3: Obviousness Over Lee and Park

79. The final section of my original declaration explained why the claims would have been obvious over the combination of Lee and Park. *See* Ex. 1003, ¶¶ 350-440.

80. Here, Dr. Giapis argues that a POSITA would have been unable “to achieve any change in shape or any rounding in Lee’s” landing pads because “[i]t is not possible to further oxidize a solid oxide material with oxygen gas as in Park.” Ex. 2023, ¶ 133. Dr. Giapis goes on to assert that Lee’s “silicon dioxide” layer includes “no ... extra silicon” that can be oxidized. *Id.*, ¶¶ 134-141.

81. To begin, Lee explains that its insulation layers are formed from “oxide” (*see* Lee, ¶ [0030]), not “solid” “silicon dioxide” as Dr. Giapis appears to assume.

82. Next, a silicon oxide layer can (and often does) include extra silicon such that it is able to be further oxidized when exposed to an oxidant.

83. For example, when the '666 patent was filed, silicon oxide films with non-stoichiometric amounts of oxygen (*i.e.*, SiO_x , where $0 < x < 2$) were both known and in routine use.

84. This is discussed in numerous references. For example, the Plummer text cited by Dr. Giapis explains that CVD “deposited films of silicon dioxide” used in “microelectronic structures” as “dielectric layers to electrically separate conductive regions” “can be nonstoichiometric.” Ex. 2008, 563-64.

85. Another article notes that CVD—a deposition method routinely used when forming insulating layers in memory devices—can be employed to form “stoichiometric SiO_2 to an oxide with about 14 a/o of Si in excess” *See, e.g.*, Ex. 1025, 379.

86. Yet another reference explains that “substoichiometric SiO_x ($0 < x < 2$) thin films” can also be formed using other methods, such as PECVD. Ex. 1026, 508.

87. Indeed, the prior art even specifically discloses the use of non-stoichiometric silicon oxides as insulating layers in 3D memory. U.S. Patent No.

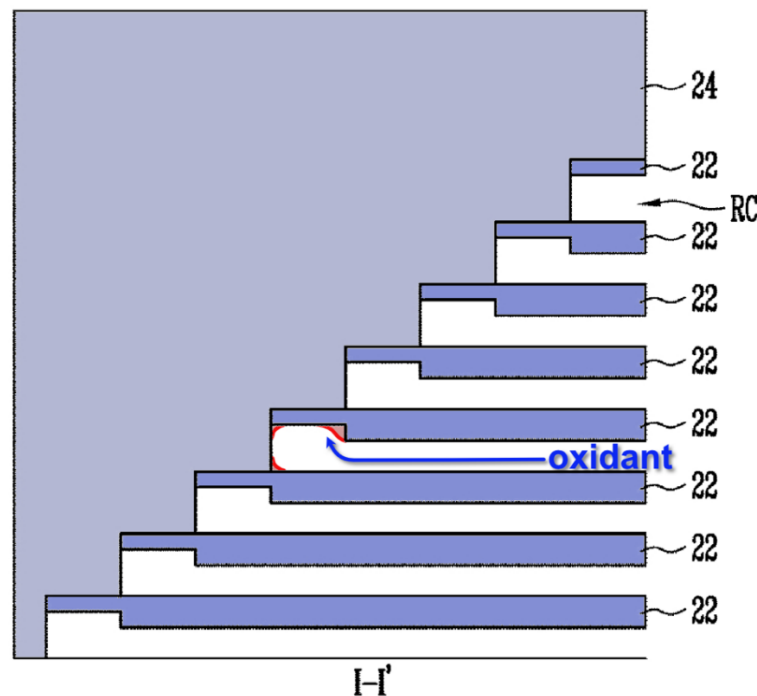
9,728,547 to Osaki et al. (Ex. 1029) provides an example. Osaki explains that it “relates generally to the field of three-dimensional memory devices.” *Id.*, 1:9-10. Like all such devices, Osaki’s memory includes alternating “insulating layers 32” and “gate dielectric layer[s] 12” arranged in a stack on a substrate. *Id.*, 7:25-29. Osaki explains that “each insulating layer 32 can be an insulating material layer” formed from, for instance, “silicon oxide...” *Id.*, 8:4-16. Per Osaki, the term “silicon oxide” includes “silicon dioxide as well as non-stoichiometric silicon oxides having more or less than two oxygen atoms for each silicon atom[.]” *Id.*, 6:45-51.

88. This type of nonstoichiometric silicon oxide film will include more than one atom of silicon for every two atoms of oxygen. Because of this, the film includes excess silicon and will be further oxidized when it is exposed to an oxidant. I explained how this type of further oxidation occurs during my prior deposition. Ex. 2010, 261:20-266:1. In such a film, the excess silicon atoms act as readily available reaction sites, so when oxygen is introduced, these silicon atoms can oxidize to form additional Si–O bonds, leading to further oxide growth.

89. As I noted in my original declaration—and during deposition—when a silicon oxide layer is further oxidized, additional silicon oxide forms preferentially in the areas of exposed, exterior corners. *See* Ex. 1003, ¶¶ 412-413; Ex. 2010, 267:7-268:22. This includes the corners within the spaces between Lee’s existing oxide layers 22 as illustrated in Fig. 5B below (with the original corners indicated in blue).

By “exterior corner,” I did not mean above Lee’s staircase structure. This was a reference to corners that are exposed within the spaces previously occupied by Lee’s sacrificial layers. Further oxide growth—and rounding—will occur in the regions shown in red in Fig. 5B, with the largest amount of oxidation occurring in the rightmost area (as there are two adjacent corners there). This is an additive process. Additional silicon oxide will form on top of the original silicon oxide. The process will continue either until all excess silicon is consumed, or the oxidant is removed. Because the nonstoichiometric film contains silicon atoms that are not fully bonded to oxygen, these under-coordinated silicon atoms preferentially react first, with oxide growth initiating and accelerating at the exposed corner sites.

FIG. 5B



90. I have also reviewed Dr. Giapis's deposition testimony regarding "nonstoichiometric" silicon oxides. His testimony is inaccurate, fails to account for chemical realities, is not consistent with how a POSITA would understand the term "nonstoichiometric," and is contradicted by the very textbook on which he relies in an effort to show how a POSITA would have understood the '666 patent (along with other published articles that make the same point).

91. According to Dr. Giapis, there is "no such thing" as nonstoichiometric silicon oxide. He testified that other atoms—such as hydrogen—would always be incorporated into the silicon oxide film changing it into a "different" material. He also testified that such a material would be "defective" and unusable. Ex. 1028, 91:14-100:13.

92. First, nonstoichiometric silicon oxide does in fact exist. It is referenced not only in the Plummer text (Ex. 2008) on which Dr. Giapis himself relies, but also in other published articles (*See* Exs. 1025, 1026). Nonstoichiometric silicon oxides are also identified as usable as memory dielectric layers. *E.g.*, Ex. 2008, 563-64.

93. Next, nonstoichiometric silicon oxide does not necessarily incorporate other atoms (like hydrogen) in order to exist. Dr. Giapis is instead describing a different type of material: a compound in which some of the oxygen atoms in an ideal SiO_2 network are replaced by another atom (e.g., hydrogen) so that all local bonding configurations continue to satisfy the so-called "octet rule" (i.e., each atom

attains a full valence shell). Such a material would not be “nonstoichiometric” silicon oxide, but rather a different, stoichiometric compound (for example, a silicon oxy-hydride). By contrast, as used in the semiconductor processing literature, “nonstoichiometric” silicon oxide (SiO_x with $0 < x < 2$) refers to an oxide network in which there is excess silicon (oxygen deficiency) relative to the ideal SiO_2 ratio, resulting in silicon–silicon bonds and oxygen vacancies within the silicon–oxygen lattice, not substitution of oxygen with another element.

94. Nonstoichiometric silicon oxide is a material that includes more than one atom of silicon per two atoms of oxygen. *See, e.g.,* Ex. 1025, 379; Ex. 1026, 508. As Plummer explains, oxidant species can diffuse through SiO_2 at elevated temperatures and oxidation proceeds preferentially at corners and stress-concentrated regions (Ex. 2008, 329-359), so a POSITA would understand that oxygen can continue to react in oxygen-deficient regions or at exposed geometric discontinuities in a nonstoichiometric oxide film, resulting in additional oxide growth and local rounding even when an SiO_2 film is already present.

95. It results from the presence of extra silicon atoms (creating oxygen vacancies) within the silicon-oxygen crystalline lattice.

96. An example of this is shown in the Plummer text below. Note the extra silicon atom that is not surrounded by oxygen atoms. A nonstoichiometric silicon oxide will have many instances of such silicon atoms within its crystalline lattice

(some present via silicon-silicon bonds, and some present via a silicon-oxygen bond but missing a second such bond to oxygen):

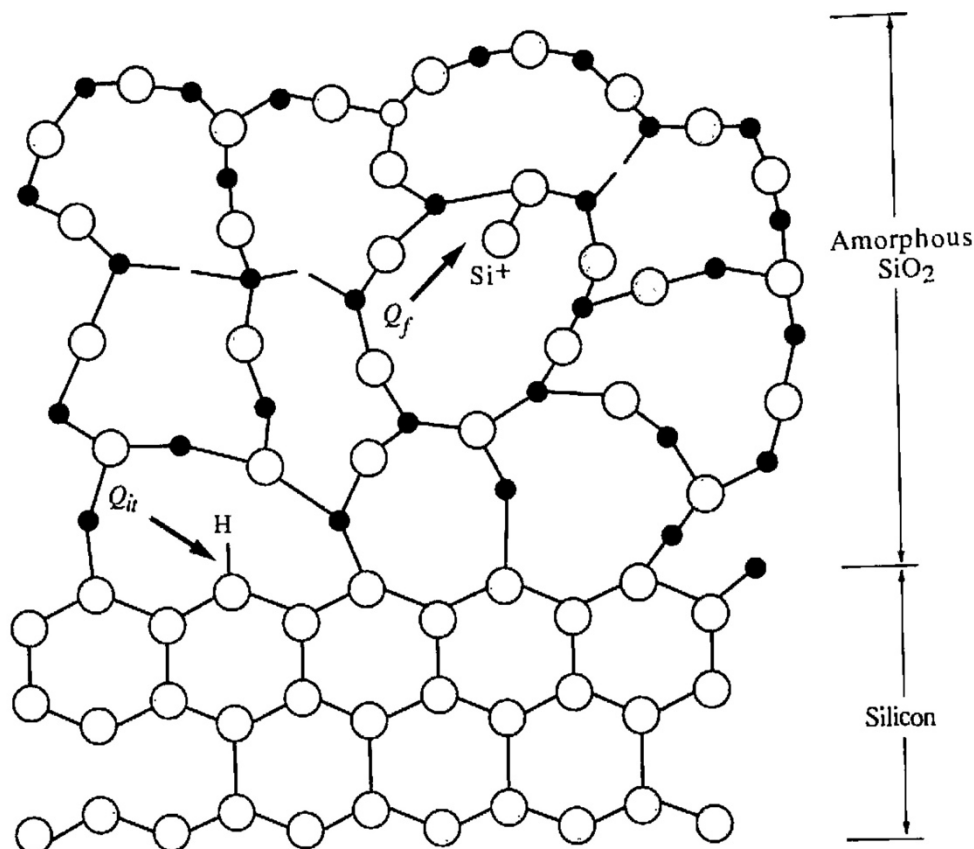


Figure 6-39 Conceptual atomic level picture of the Si/SiO₂ interface showing possible structural origins of Q_f and Q_{it} . Q_f corresponds to the excess Si^+ atom; Q_{it} is shown as an incompletely bonded Si atom near the interface, passivated in this example with an H bond. The larger circles correspond to Si atoms; the smaller circles to O atoms.

Ex. 2008, 354.

97. A non-stoichiometric silicon oxide film (particularly one where x in SiO_x is closer to 1 than 2) will include many such extra silicon atoms.

98. Not only is such a material known and readily achievable, but a POSITA would have immediately recognized that it would have been desirable to

further oxidize the non-stoichiometric film to reduce the amount of extra silicon. This would not only produce a rounded landing pad but would allow the material's uniformity to improve.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: Nov. 25, 2025
Location: Austin, TX
Signature: 
Dr. Jack C. Lee