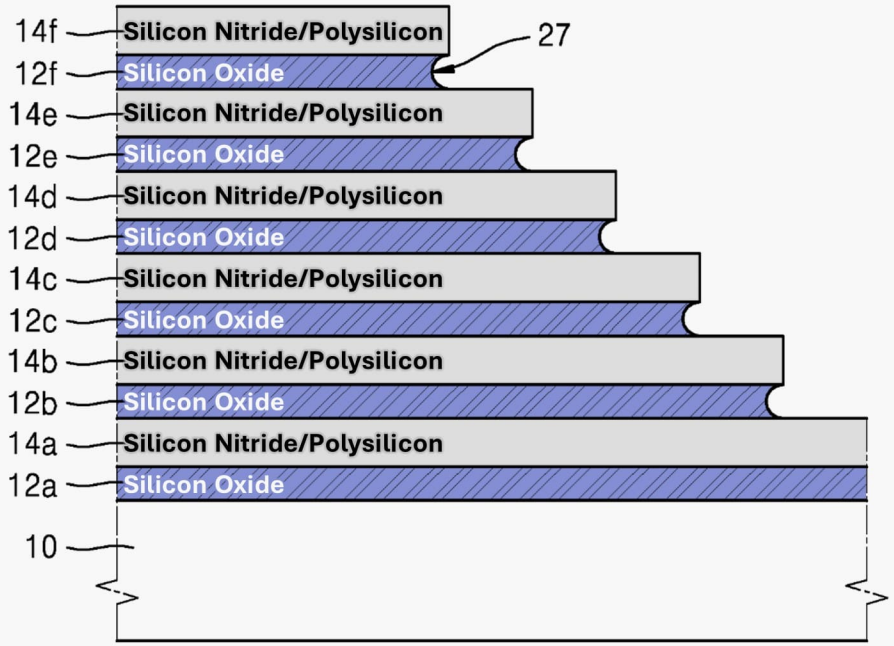
Park's Process Cannot Be Combined With Kim

FIG. 6B



Ex. 1008 (Park), Fig. 6B

Park

As shown in FIG. **6**C, an additional insulating layer **40** is formed by oxidizing surfaces and side surfaces of the stepped sacrificial layer patterns **14***a* through **14***f* that are externally exposed. The additional insulating layer **40** may be formed by thermally oxidizing the surfaces and the side surfaces of the sacrificial layer patterns **14***a* through **14***f*. The additional insulating layer **40** may be formed on the surfaces and side surfaces of the sacrificial layer patterns **14***a* through **14***f* not covered by the interlayer insulating layer patterns **12***b* through **12***f*. One end of the additional insulating layer **40** may be rounded by an oxidation process. When one end

Ex. 1008 (Park), 8:28-38

Dr. Lee Deposition

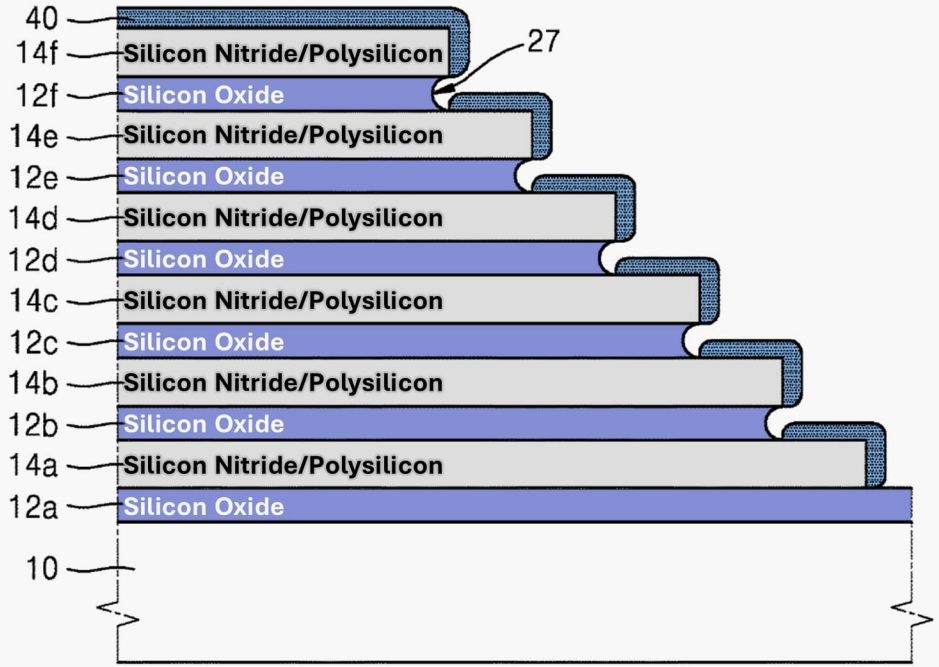
Q. Okay. Can you point to me where the oxidant is added in Park Figure 7 to form the rounded pads?

A. Well, it's due to the oxidation step as shown in Figure 6C. Figure 6C is -- the additional insulating layer 40 is formed by oxidizing the surface and the side surface of the step sacrificial layer patterns 14a through 14f that are externally exposed.

Ex. 2024 (Jack C. Lee, Ph. D.), 136:14-22

Park's Process Cannot Be Combined With Kim

FIG. 6C



Ex. 1008 (Park), Fig. 6C

Park

As shown in FIG. **6**C, an additional insulating layer **40** is formed by oxidizing surfaces and side surfaces of the stepped sacrificial layer patterns **14***a* through **14***f* that are externally exposed. The additional insulating layer **40** may be formed by thermally oxidizing the surfaces and the side surfaces of the sacrificial layer patterns **14***a* through **14***f*. The additional insulating layer **40** may be formed on the surfaces and side surfaces of the sacrificial layer patterns **14***a* through **14***f* not covered by the interlayer insulating layer patterns **12***b* through **12***f*. One end of the additional insulating layer **40** may be rounded by an oxidation process. When one end

Ex. 1008 (Park), 8:28-38

Dr. Lee Deposition

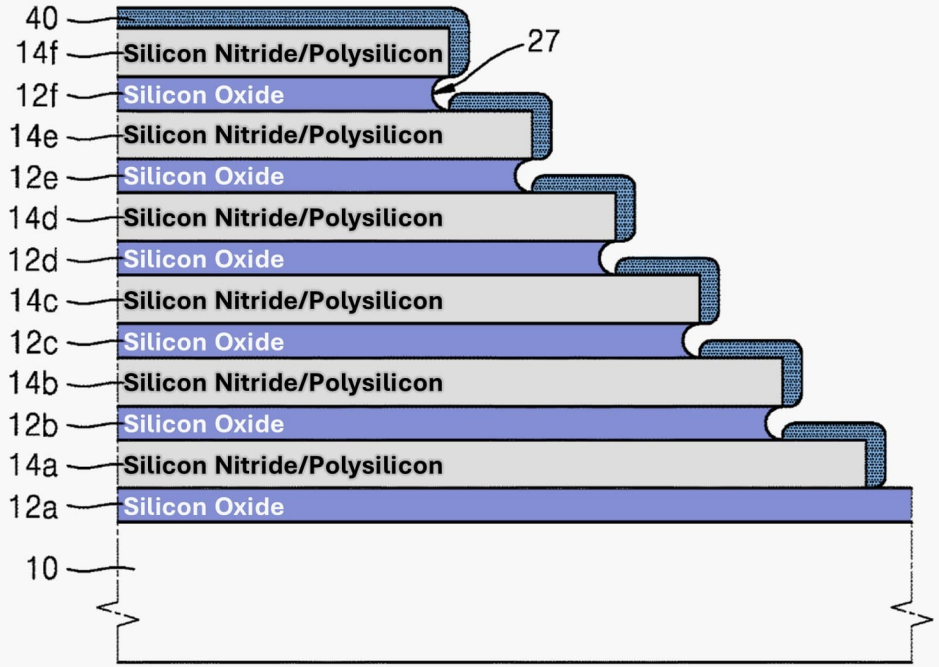
Q. Okay. Can you point to me where the oxidant is added in Park Figure 7 to form the rounded pads?

A. Well, it's due to the oxidation step as shown in Figure 6C. Figure 6C is -- the additional insulating layer 40 is formed by oxidizing the surface and the side surface of the step sacrificial layer patterns 14a through 14f that are externally exposed.

Ex. 2024 (Jack C. Lee, Ph. D.), 136:14-22

Park's Process Cannot Be Combined With Kim

FIG. 6C



Ex. 1008 (Park), Fig. 6C

Park

The interlayer insulating layer patterns **12***a* through **12***f* may be formed of a silicon oxide layer. The sacrificial layer patterns **14***a* through **14***f* may be formed of a material having an etching selectivity with respect to the interlayer insulating layer patterns **12***a* through **12***f*. The sacrificial layer patterns **14***a* through **14***f* may be formed of a material such as a silicon nitride layer or a polysilicon layer. The interlayer insulating layer patterns **12***a* through **12***f* and the sacrificial layer patterns **14***a* through **14***f* may be formed by a deposition process such as chemical vapor deposition (CVD) or atomic layer deposition (ALD).

Ex. 1008 (Park), 8:1-11

Dr. Lee Deposition

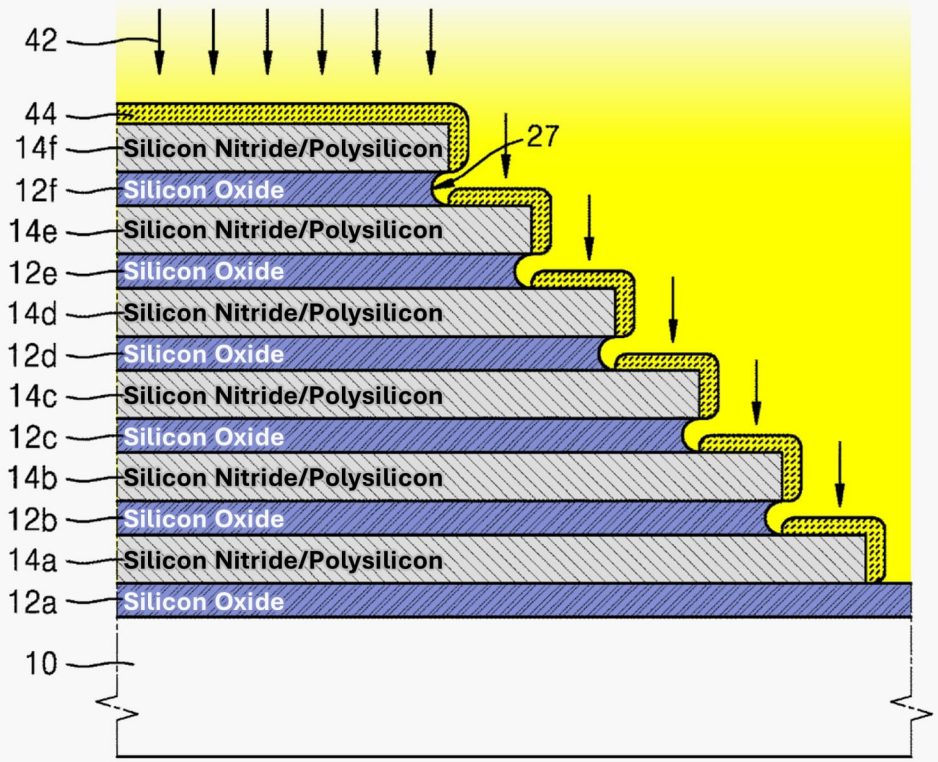
Q. Okay. Can you point to me where the oxidant is added in Park Figure 7 to form the rounded pads?

A. Well, it's due to the oxidation step as shown in Figure 6C. Figure 6C is -- the additional insulating layer 40 is formed by oxidizing the surface and the side surface of the step sacrificial layer patterns 14a through 14f that are externally exposed.

Ex. 2024 (Jack C. Lee, Ph. D.), 136:14-22

Park's Process Cannot Be Combined With Kim

FIG. 6D



Ex. 1008 (Park), Fig. 6D

Park

As shown in FIG. **6**C, an additional insulating layer **40** is formed by oxidizing surfaces and side surfaces of the stepped sacrificial layer patterns **14***a* through **14***f* that are externally exposed. The additional insulating layer **40** may be formed by thermally oxidizing the surfaces and the side surfaces of the sacrificial layer patterns **14***a* through **14***f*. The additional insulating layer **40** may be formed on the surfaces and side surfaces of the sacrificial layer patterns **14***a* through **14***f* not covered by the interlayer insulating layer patterns **12***b* through **12***f*. One end of the additional insulating layer **40** may be rounded by an oxidation process. When one end

Ex. 1008 (Park), 8:28-38

Dr. Lee Deposition

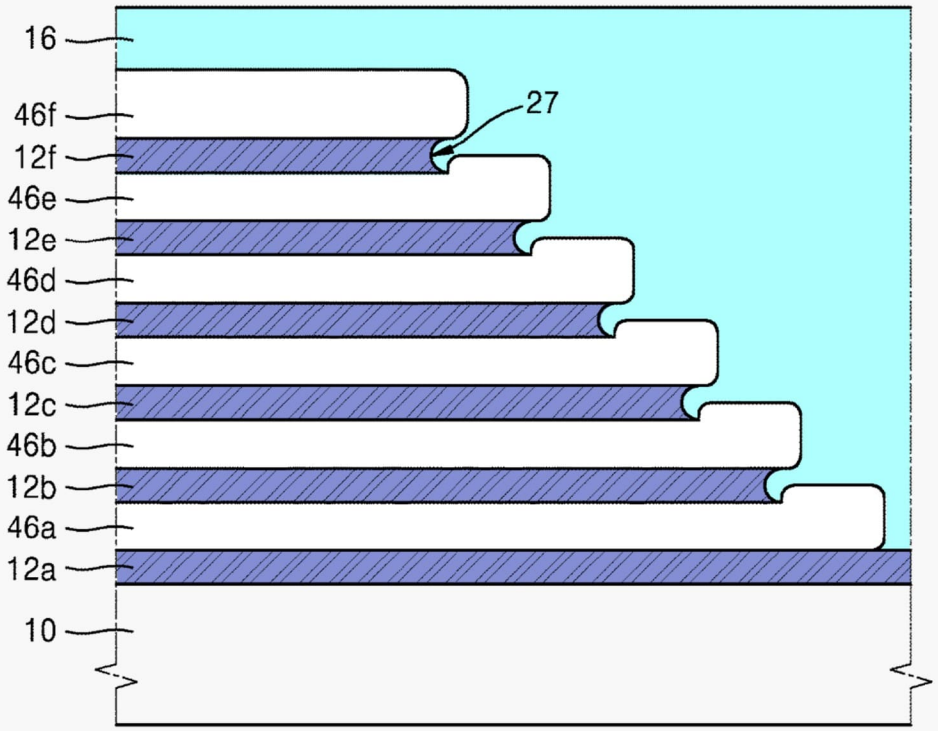
Q. Okay. Can you point to me where the oxidant is added in Park Figure 7 to form the rounded pads?

A. Well, it's due to the oxidation step as shown in Figure 6C. Figure 6C is -- the additional insulating layer 40 is formed by oxidizing the surface and the side surface of the step sacrificial layer patterns 14a through 14f that are externally exposed.

Ex. 2024 (Jack C. Lee, Ph. D.), 136:14-22

Park's Process Cannot Be Combined With Kim

FIG. 6E



Ex. 1008 (Park), Fig. 6E

Park

As shown in FIG. **6**C, an additional insulating layer **40** is formed by oxidizing surfaces and side surfaces of the stepped sacrificial layer patterns **14***a* through **14***f* that are externally exposed. The additional insulating layer **40** may be formed by thermally oxidizing the surfaces and the side surfaces of the sacrificial layer patterns **14***a* through **14***f*. The additional insulating layer **40** may be formed on the surfaces and side surfaces of the sacrificial layer patterns **14***a* through **14***f* not covered by the interlayer insulating layer patterns **12***b* through **12***f*. One end of the additional insulating layer **40** may be rounded by an oxidation process. When one end

Ex. 1008 (Park), 8:28-38

Dr. Lee Deposition

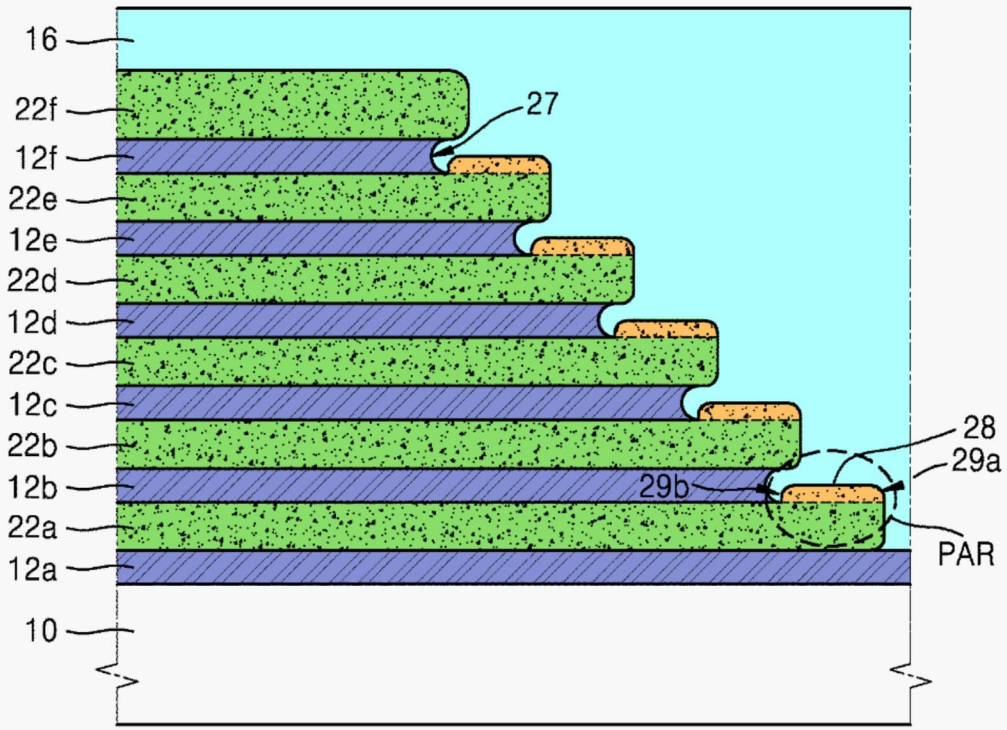
Q. Okay. Can you point to me where the oxidant is added in Park Figure 7 to form the rounded pads?

A. Well, it's due to the oxidation step as shown in Figure 6C. Figure 6C is -- the additional insulating layer 40 is formed by oxidizing the surface and the side surface of the step sacrificial layer patterns 14a through 14f that are externally exposed.

Ex. 2024 (Jack C. Lee, Ph. D.), 136:14-22

Park's Process Cannot Be Combined With Kim

FIG. 6F



Ex. 1008 (Park), Fig. 6F

Park

As shown in FIG. **6**C, an additional insulating layer **40** is formed by oxidizing surfaces and side surfaces of the stepped sacrificial layer patterns **14***a* through **14***f* that are externally exposed. The additional insulating layer **40** may be formed by thermally oxidizing the surfaces and the side surfaces of the sacrificial layer patterns **14***a* through **14***f*. The additional insulating layer **40** may be formed on the surfaces and side surfaces of the sacrificial layer patterns **14***a* through **14***f* not covered by the interlayer insulating layer patterns **12***b* through **12***f*. One end of the additional insulating layer **40** may be rounded by an oxidation process. When one end

Ex. 1008 (Park), 8:28-38

Dr. Lee Deposition

Q. Okay. Can you point to me where the oxidant is added in Park Figure 7 to form the rounded pads?

A. Well, it's due to the oxidation step as shown in Figure 6C. Figure 6C is -- the additional insulating layer 40 is formed by oxidizing the surface and the side surface of the step sacrificial layer patterns 14a through 14f that are externally exposed.

Ex. 2024 (Jack C. Lee, Ph. D.), 136:14-22

Park's Process Cannot Be Combined With Kim

Dr. Lee Reply Declaration

48. Further oxidation would occur and silicon oxide would form preferentially in the corners and exposed edges of the oxide layers:

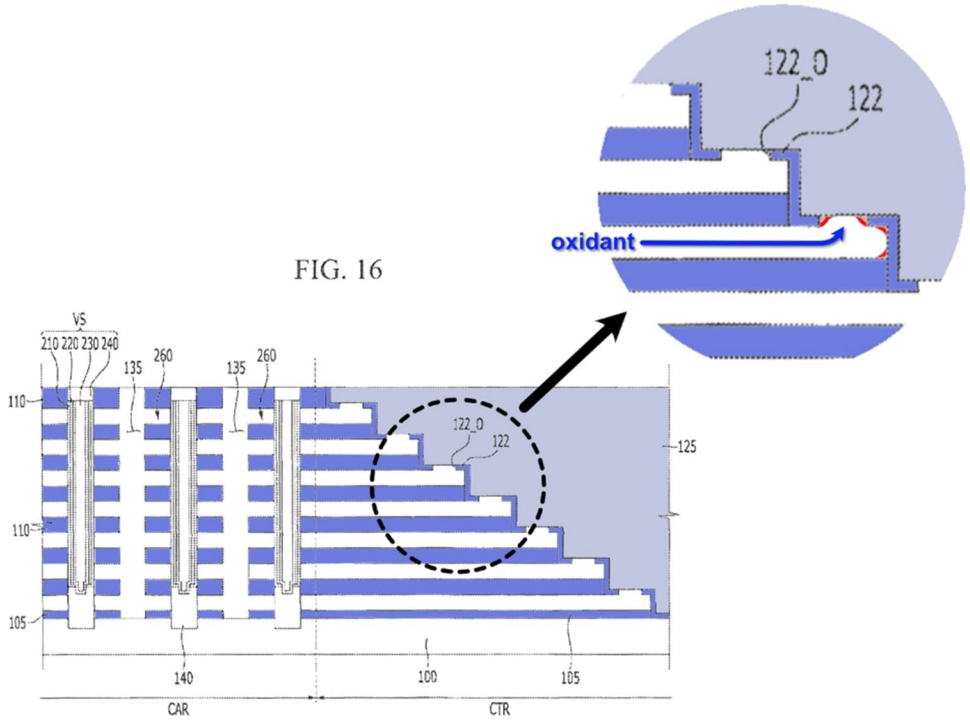


FIG. 16

Ex. 1027 (Dr. Lee Rpl. Decl.) ¶ 48

Dr. Lee Deposition

Q. The silicon oxide in Kim is not formed by oxidizing silicon in another step?

A. No, because at that point the steps involve both the layer 110, which is silicon oxide, and layer 120, which is silicon nitride. So it can't really oxidize nitride that easily.
So layer 122 is deposited.

Ex. 2024 (Jack C. Lee, Ph. D.), 120:14-20

Q. If oxidation in Lee occurred on the edge of the staircase, would layer 22 be oxidized?

A. Well, it depends on the state of layer 22, but layer 22 is deposited as an oxide. So -- a silicon dioxide. So at least the purpose of the -- of the process is that that layer is not subject to any subsequent oxidations.

Q. So layers 22 is not subject to any subsequent oxidation, correct?

A. You're right. It's not -- in general, even if it is exposed to even -- it might oxidize slightly but not very much. At least it's not designed to oxidize.

Ex. 2024 (Jack C. Lee, Ph. D.), 185:17-186:9

New Theory Is A Stretch

Deposited films of silicon dioxide

microelectronic structures

dielectric layers to electrically separate conducting regions

Dr. Lee Reply Declaration

84. This is discussed in numerous references. For example, the Plummer text cited by Dr. Giapis explains that CVD "deposited films of silicon dioxide" used in "microelectronic structures" as "dielectric layers to electrically separate conductive regions" "can be nonstoichiometric." Ex. 2008, 563-64.

Ex. 1027 (Dr. Lee Rpl. Decl.) ¶ 84

can be nonstoichiometric

Ex. 2008

9.3.4 Silicon Dioxide Deposition

Deposited films of silicon dioxide are utilized throughout silicon microelectronic structures as described in the CMOS process flow in Chapter 2 (see, for example, Figures 2–29 and 2–38). They are used for dielectric layers to electrically separate conducting regions as well as for masks against implantation and diffusion. The requirements for the films will be discussed in more detail in Chapter 11, but obtaining films of good quality in terms of density, purity, and thermal stability, as well as good step coverage and filling properties are of major concern.

Most oxide films today are deposited at relatively low temperatures, from 200°C to 500°C using CVD techniques. Sputtered oxide films have worse coverage and more particulates (mostly due to flaking off of the metal chamber walls) than CVD oxides. Atmospheric systems have been used for many years, but today LPCVD and PECVD systems have become more commonly used.

Silane and oxygen are common source gases for CVD silicon dioxide deposition, following the net reaction

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \quad (9.32)$$

Oxidants other than O_2 are sometimes used, such as N_2O, NO, and CO_2. When nonplasma, silane-based deposition of SiO_2 is done at temperatures less than 500°C, it is commonly referred to as Low-Temperature Oxide, or "LTO," deposition.

Other sources of silicon are also used. One such source is tetraethooxysilane—$Si(OC_2H_5)_4$—or "TEOS." It can form silicon dioxide by decomposing via the reaction

$$Si(OC_2H_5)_4 \rightarrow SiO_2 + \text{byproducts} \quad (9.33)$$

(O_2 is often added as an extra oxidizer to reduce the carbon content in the film.) This deposition occurs at higher temperatures, in the 650–800°C range, but because of the low sticking coefficient of TEOS compared to silane, more conformal films are produced. The deposition temperature can be lowered to below 400°C by either utilizing plasma enhanced deposition, or by including ozone, O_3, in the chamber:

$$Si(OC_2H_5)_4 + O_3 \rightarrow SiO_2 + \text{byproducts} \quad (9.34)$$

Because at low pressures (<150 torr) the deposition using TEOS and O_3 is limited by O_3 and gives worse film properties, a so-called Sub-Atmospheric CVD (SACVD) system has been developed for doped premetal films and undoped intermetal films [9.22, 9.23]. The deposition pressure in this system is at higher pressures (200–400 torr) and the deposition temperature is 300–550°C. Oxide films with good gap fill and reflow ability can be obtained with this system.

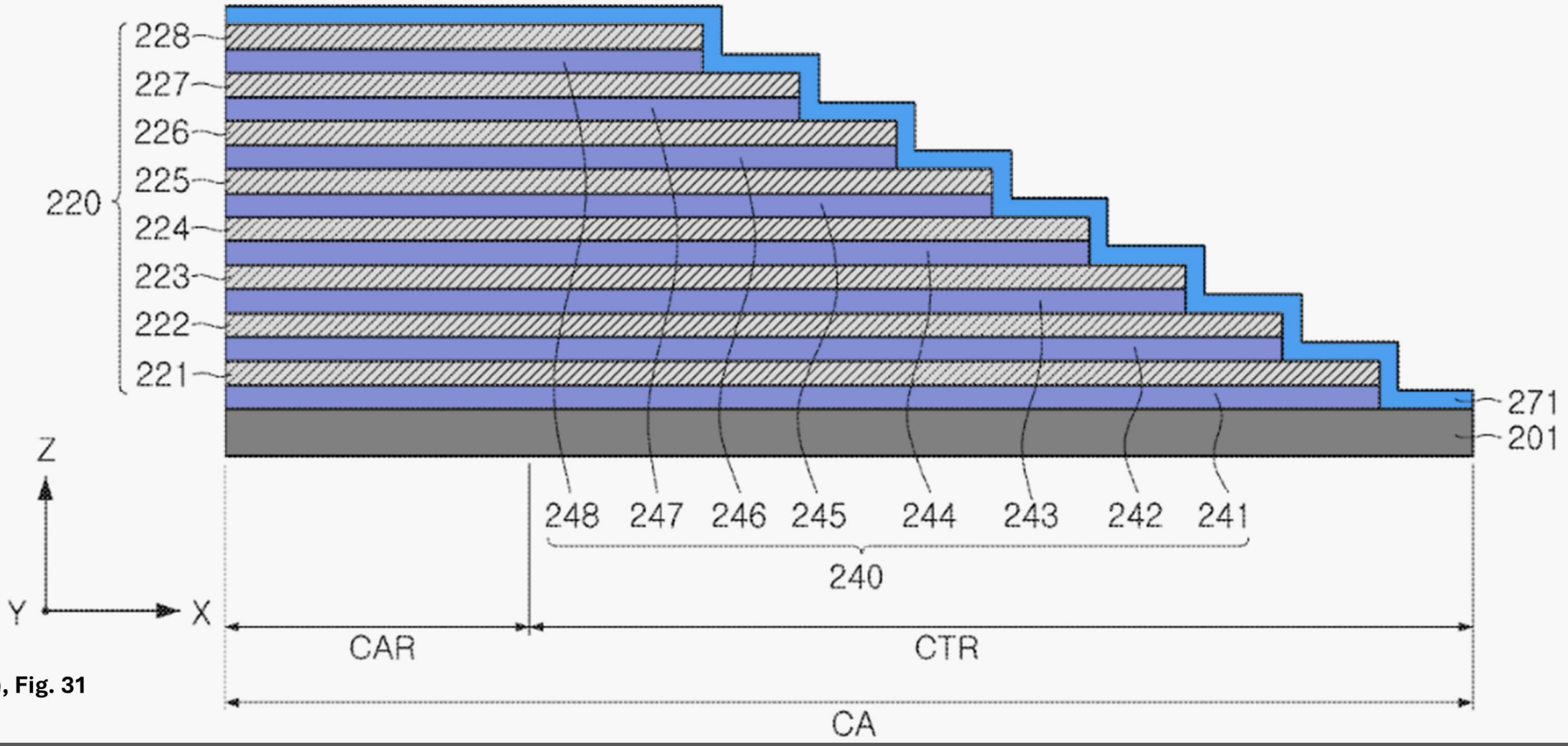
The major drawbacks to using TEOS are that it is a more difficult source to use (it is an organometallic liquid), the relatively high levels of carbon in the deposited film (from the TEOS itself), and the more porous films that are sometimes formed. But TEOS is still commonly used due to the conformality of the films it produces.

Silicon dioxide films deposited using LPCVD or APCVD at low temperatures (less than 500°C) can be nonstoichiometric and are often porous. They can also exhibit in-

Ex. 2008, 563-64

Nam's Process Cannot Be Combined With Kim

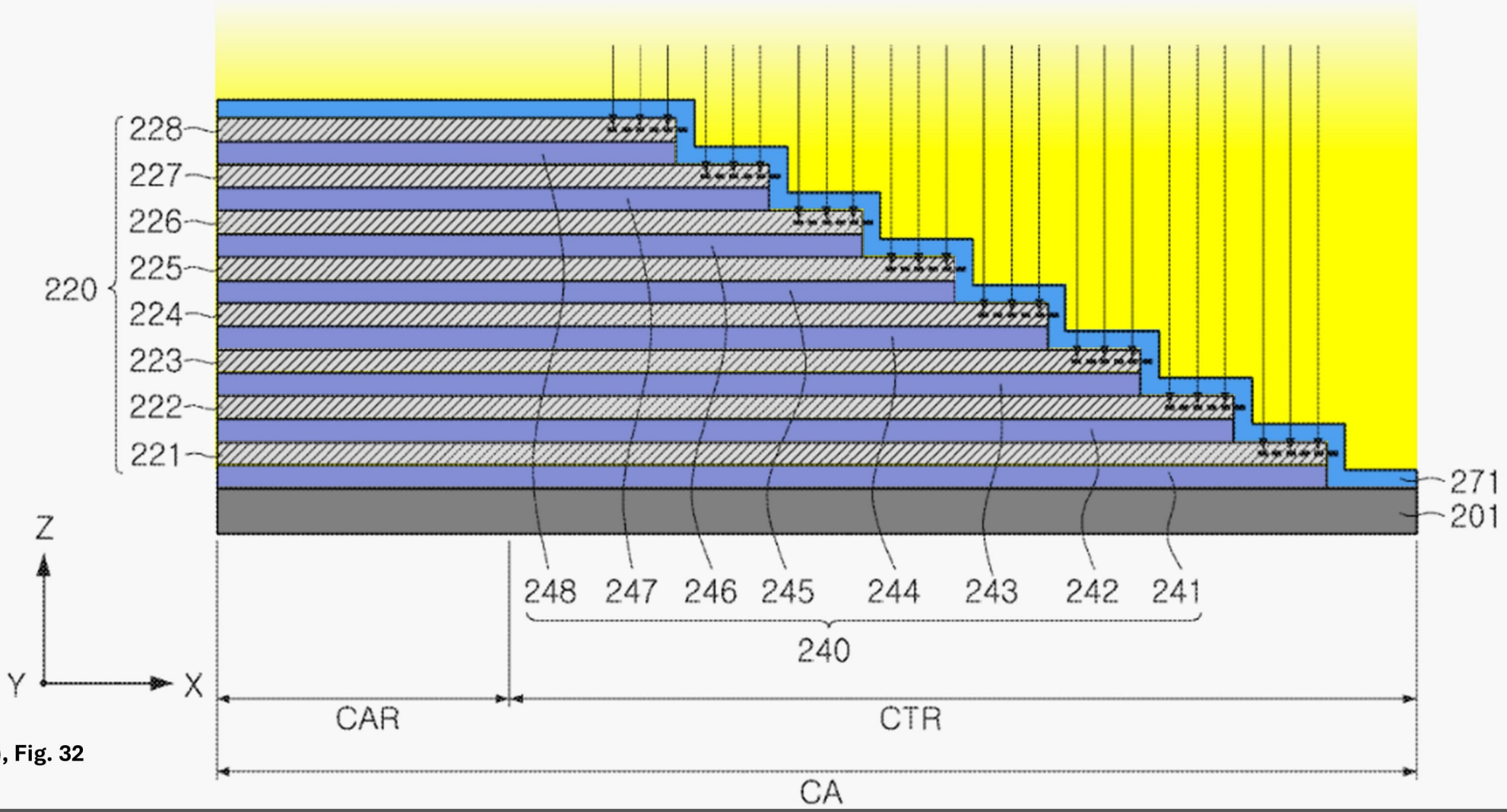
FIG. 31



Ex. 1006 (Nam), Fig. 31

Nam's Process Cannot Be Combined With Kim

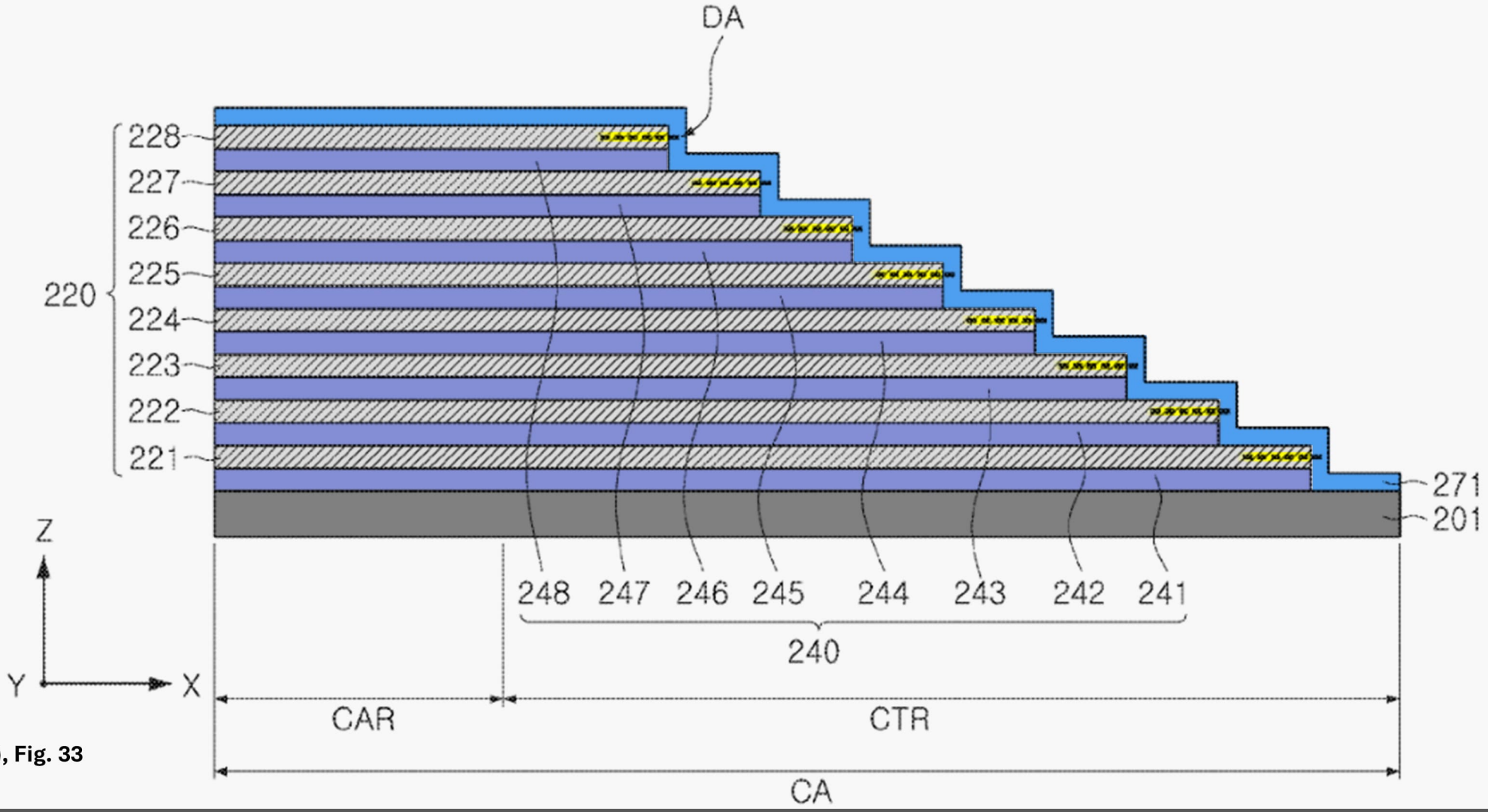
FIG. 32



Ex. 1006 (Nam), Fig. 32

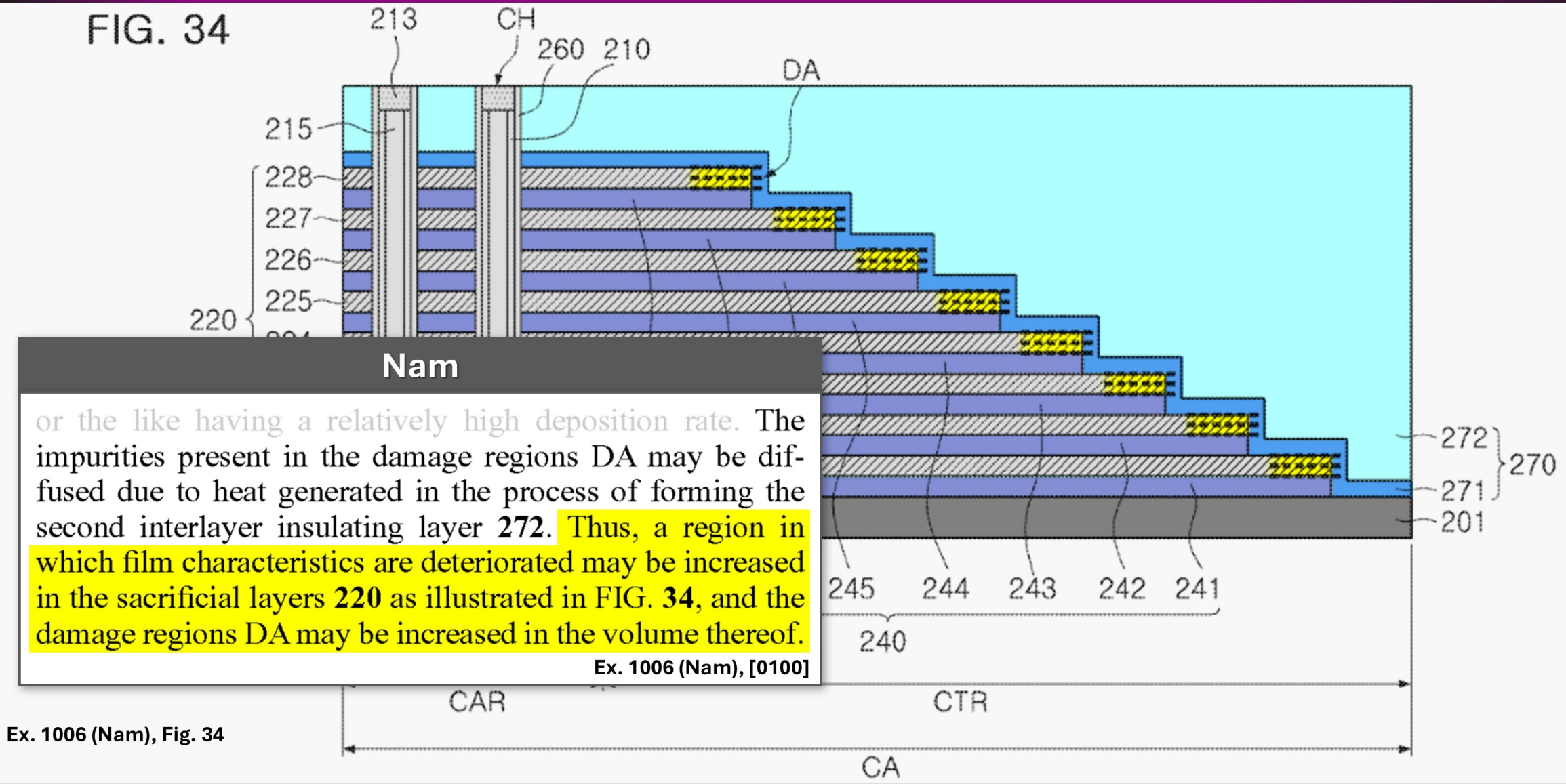
Nam's Process Cannot Be Combined With Kim

FIG. 33



Ex. 1006 (Nam), Fig. 33

Nam's Process Cannot Be Combined With Kim



Nam

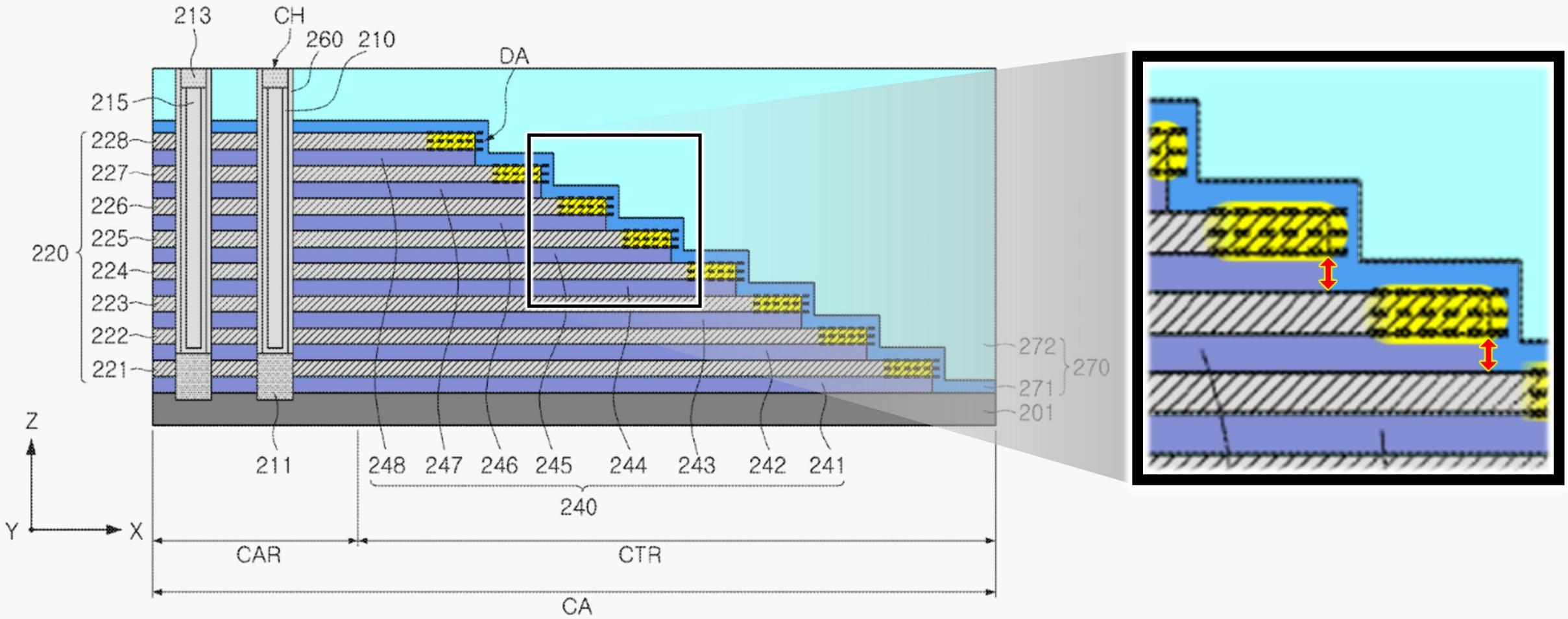
or the like having a relatively high deposition rate. The impurities present in the damage regions DA may be diffused due to heat generated in the process of forming the second interlayer insulating layer **272**. Thus, a region in which film characteristics are deteriorated may be increased in the sacrificial layers **220** as illustrated in FIG. **34**, and the damage regions DA may be increased in the volume thereof.

Ex. 1006 (Nam), [0100]

Ex. 1006 (Nam), Fig. 34

Nam's Process Cannot Be Combined With Kim

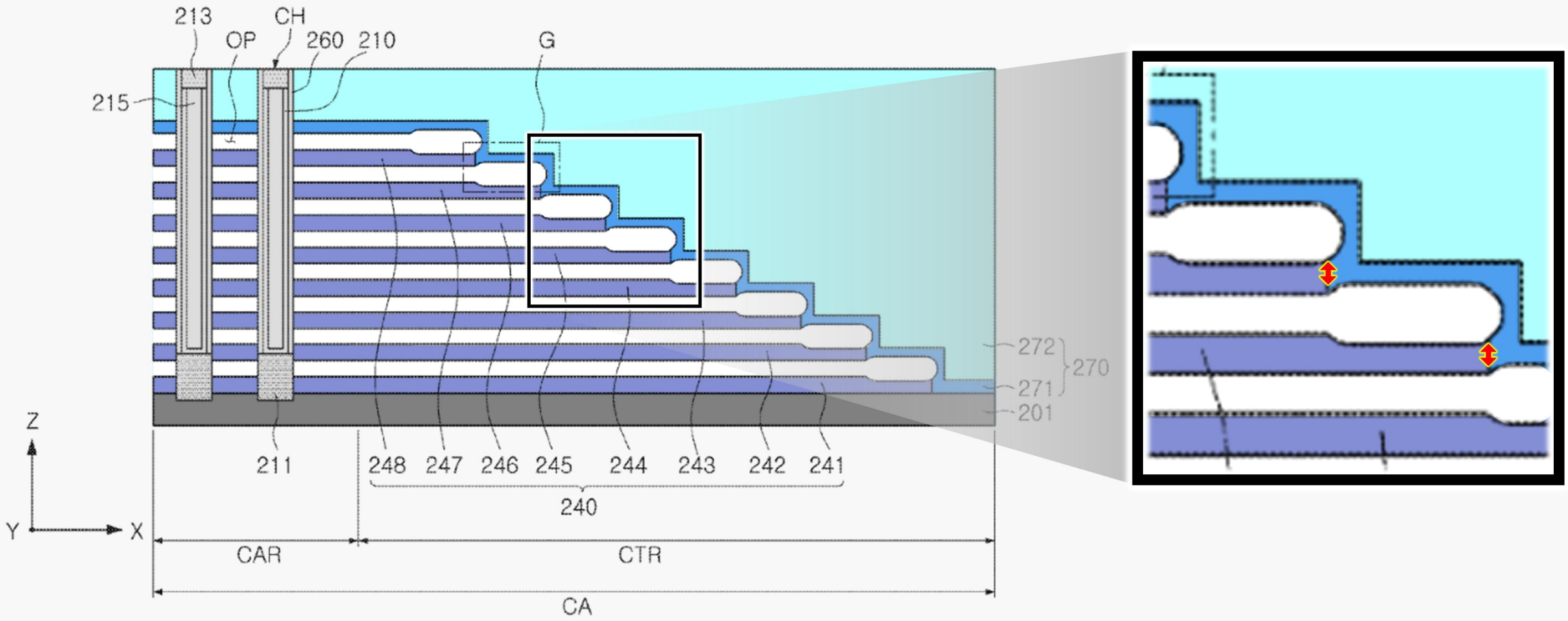
FIG. 34



Ex. 1006 (Nam), Fig. 34

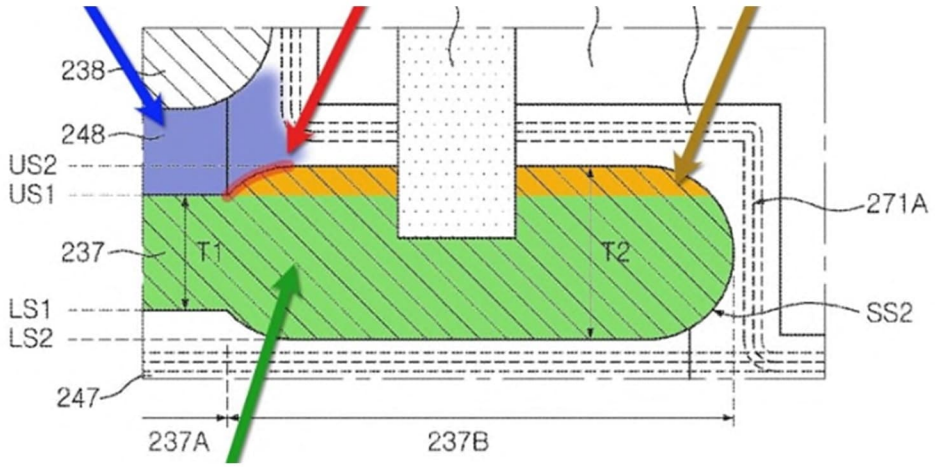
Nam's Process Cannot Be Combined With Kim

FIG. 36

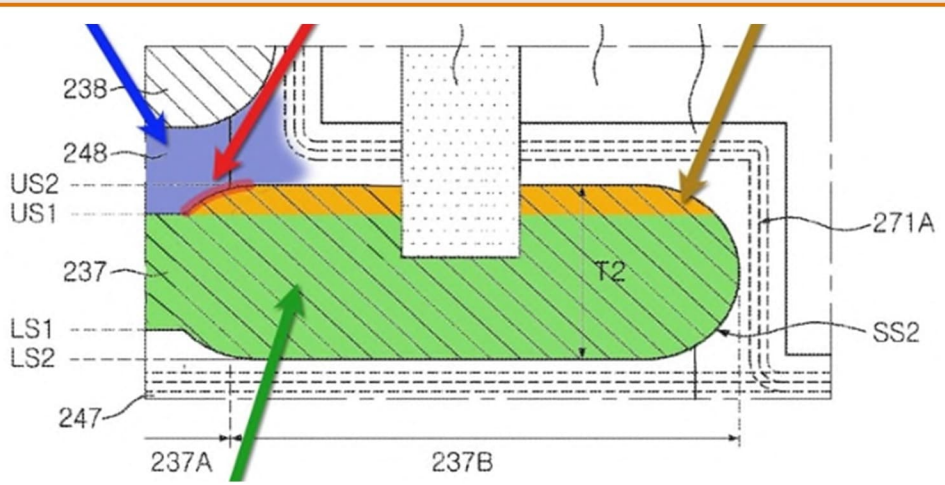


Ex. 1006 (Nam), Fig. 36

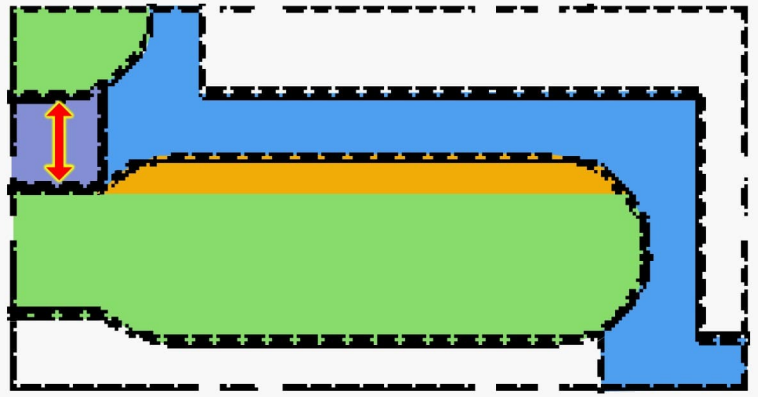
Nam's Process Cannot Be Combined With Kim



Pet. 67



Pet. 69



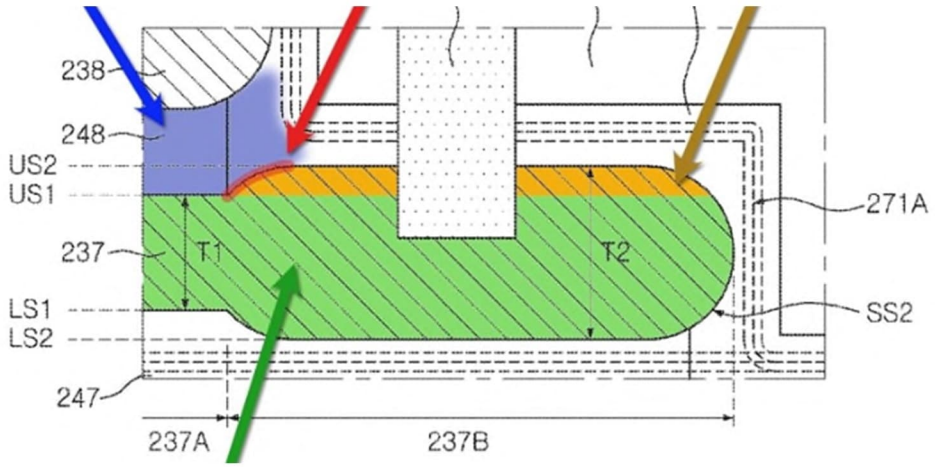
Ex. 1006 (Nam), Fig. 36

Petition

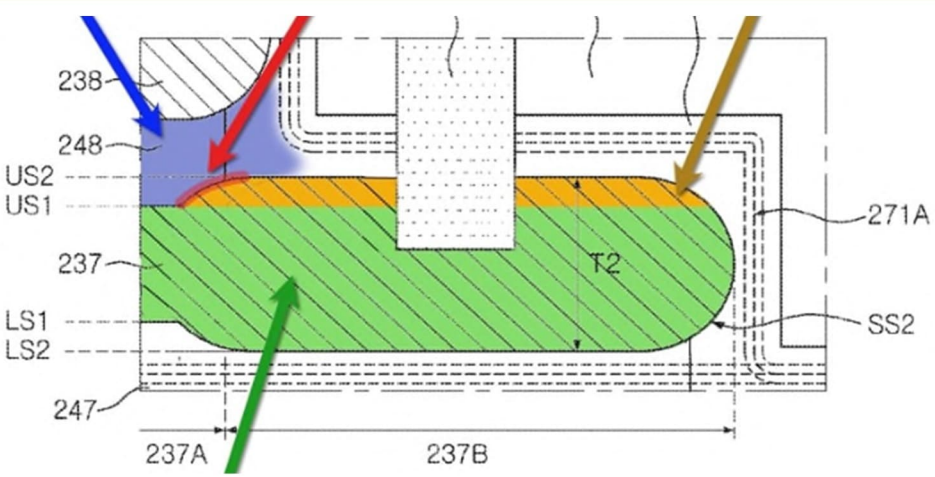
contact insulation layer 271. *Id.*, ¶¶ 327-329. Regardless, a POSITA would have understood that because Nam forms its contact pad via ion implantation, a range of structures will result. *See id.*, ¶¶ 330-334. In other words, while Figure 8A depicts the intended or representative pad structure, ion implantation will result in both somewhat larger and somewhat smaller pads. *See id.* Because of this, in some layers, a POSITA would have understood that the pad will extend beyond the bounds shown in Figure 8A into layer 248 by some amount. This will in turn result in a

Pet. 68-69

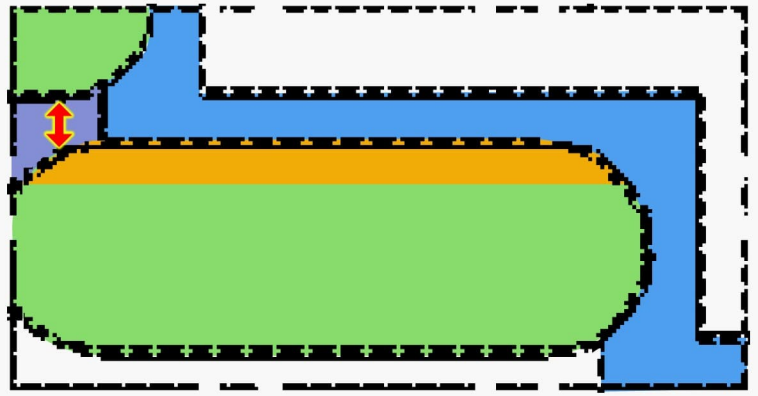
Nam's Process Cannot Be Combined With Kim



Pet. 67



Pet. 69



Ex. 1006 (Nam), Fig. 36 (modified)

Petition

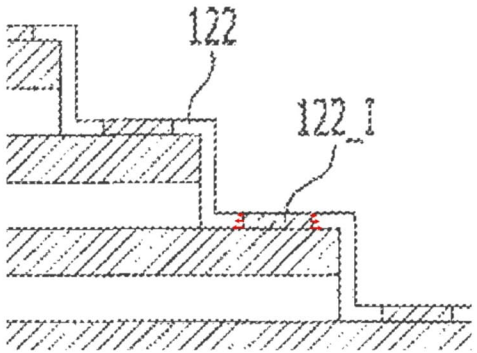
contact insulation layer 271. *Id.*, ¶¶ 327-329. Regardless, a POSITA would have understood that because Nam forms its contact pad via ion implantation, a range of structures will result. *See id.*, ¶¶ 330-334. In other words, while Figure 8A depicts the intended or representative pad structure, ion implantation will result in both somewhat larger and somewhat smaller pads. *See id.* Because of this, in some layers, a POSITA would have understood that the pad will extend beyond the bounds shown in Figure 8A into layer 248 by some amount. This will in turn result in a

Pet. 68-69

Nam's Process Cannot Be Combined With Kim

Dr. Lee Reply Declaration

52. An example of this is shown below. Application of heat will cause the impurities implanted in Kim's insulating layer 122 in area 122_I to spread, resulting in a damaged region with a rounded shape (and curved side surfaces). The spread is indicated with small red arrows. This in turn will produce a rounded landing pad like that depicted in Nam:



Ex. 1027 (Dr. Lee Rpl. Decl.) ¶ 52

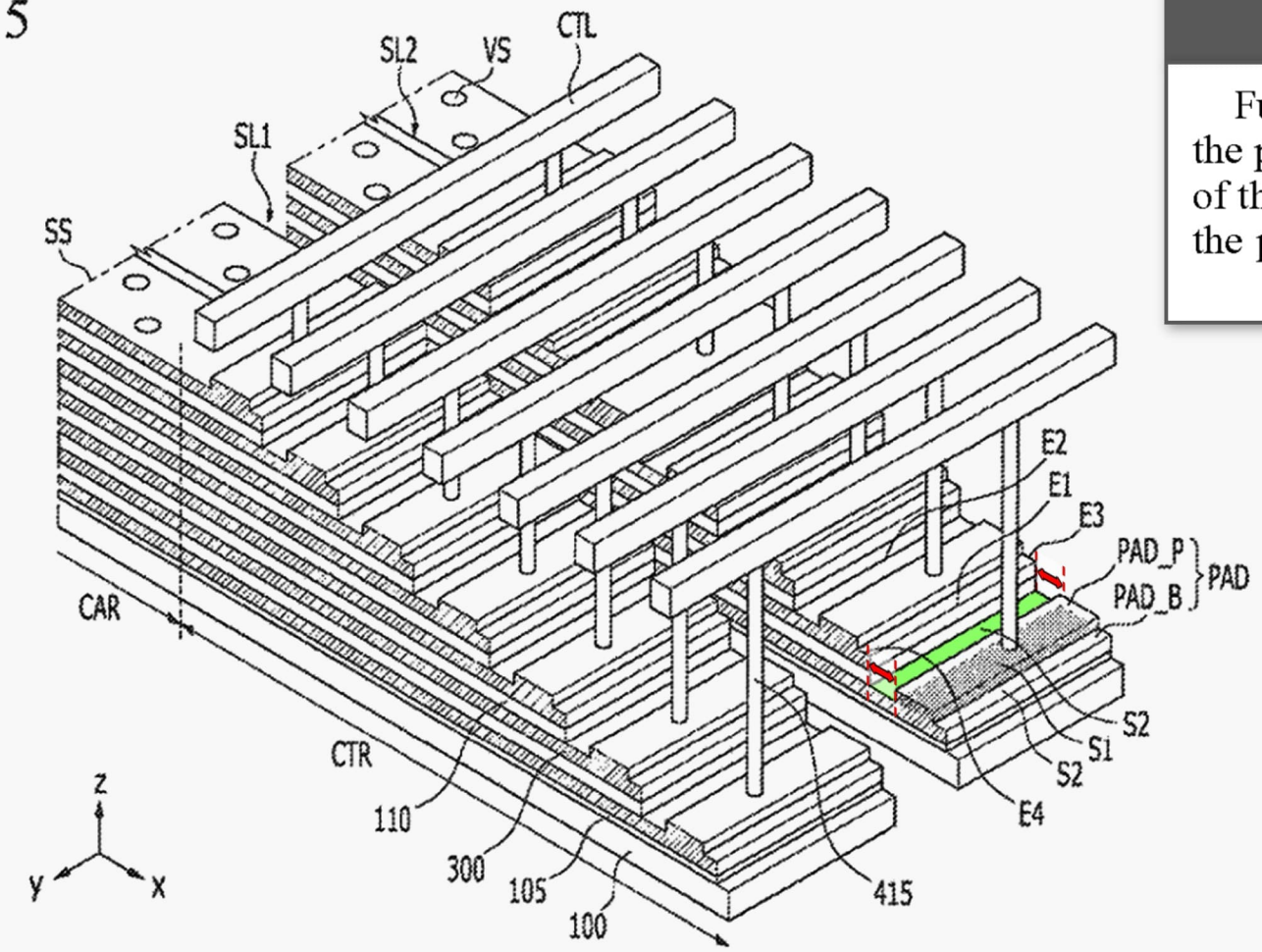
Petition

contact insulation layer 271. *Id.*, ¶¶ 327-329. Regardless, a POSITA would have understood that because Nam forms its contact pad via ion implantation, a range of structures will result. *See id.*, ¶¶ 330-334. In other words, while Figure 8A depicts the intended or representative pad structure, ion implantation will result in both somewhat larger and somewhat smaller pads. *See id.* Because of this, in some layers, a POSITA would have understood that the pad will extend beyond the bounds shown in Figure 8A into layer 248 by some amount. This will in turn result in a

Pet. 68-69

Petitioner Provides No Motivation To Modify Kim

FIG. 5

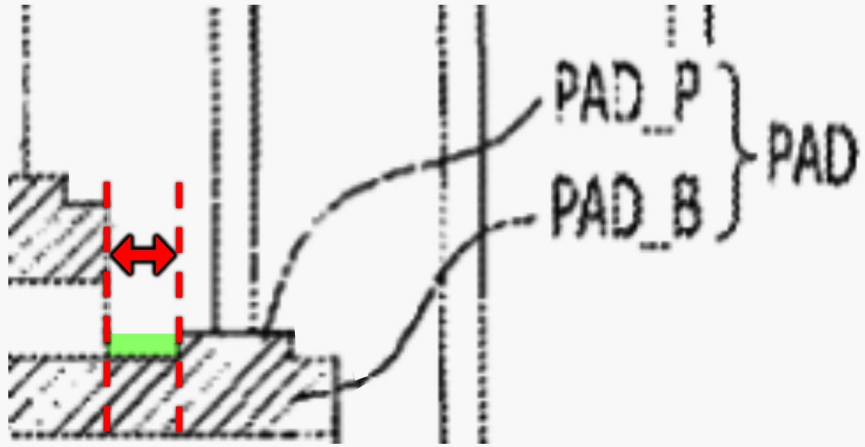


Ex. 1005 (Kim), Fig. 5

Kim

Further, the semiconductor memory device may include the protrusion pad PAD_P inside from the edge of a surface of the base pad PAD_B to prevent the short-circuit between the pad units PAD positioned at different rows.

Ex. 1005 (Kim), 9:46-49

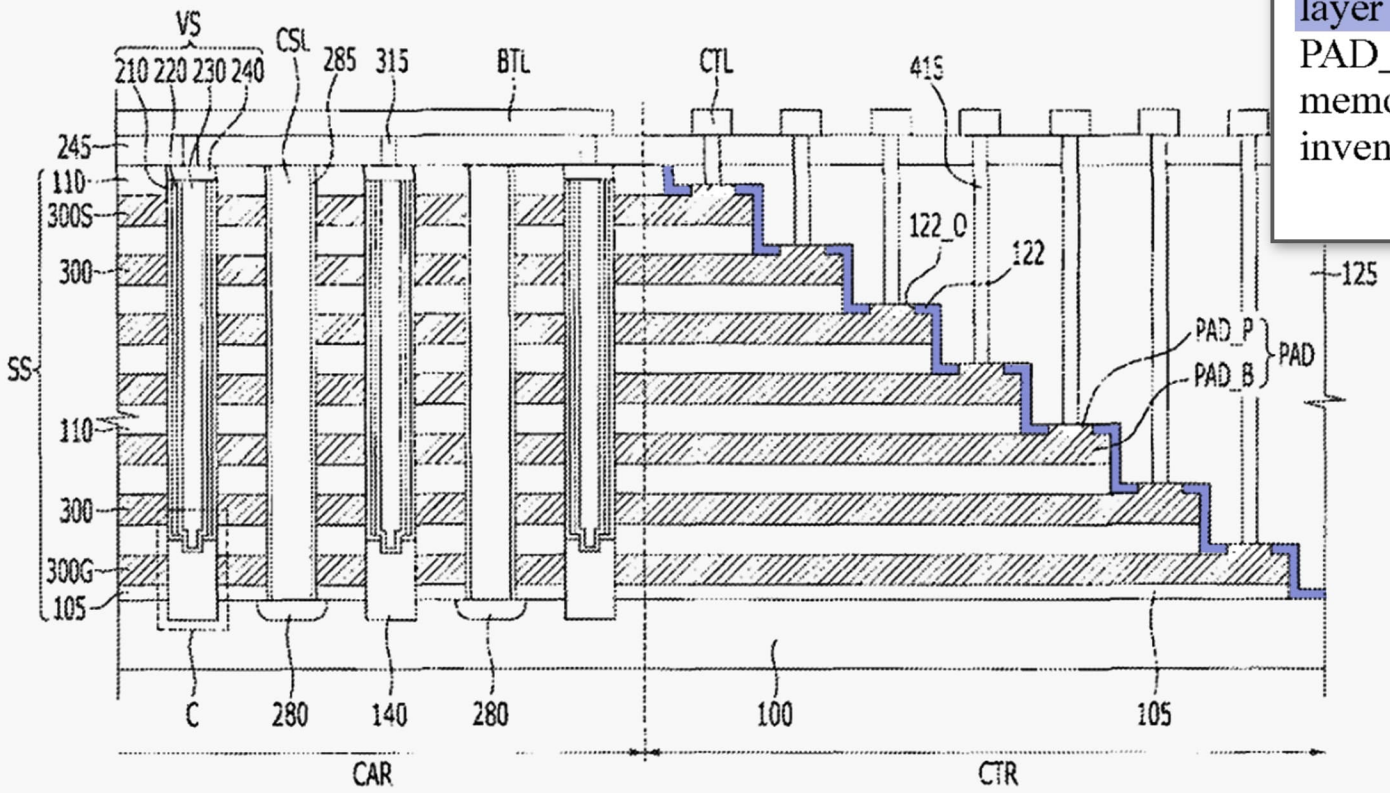


Ex. 1005 (Kim), Fig. 4B (modified)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Petitioner Provides No Motivation To Modify Kim

FIG. 4B



Ex. 1005 (Kim), Fig. 4B

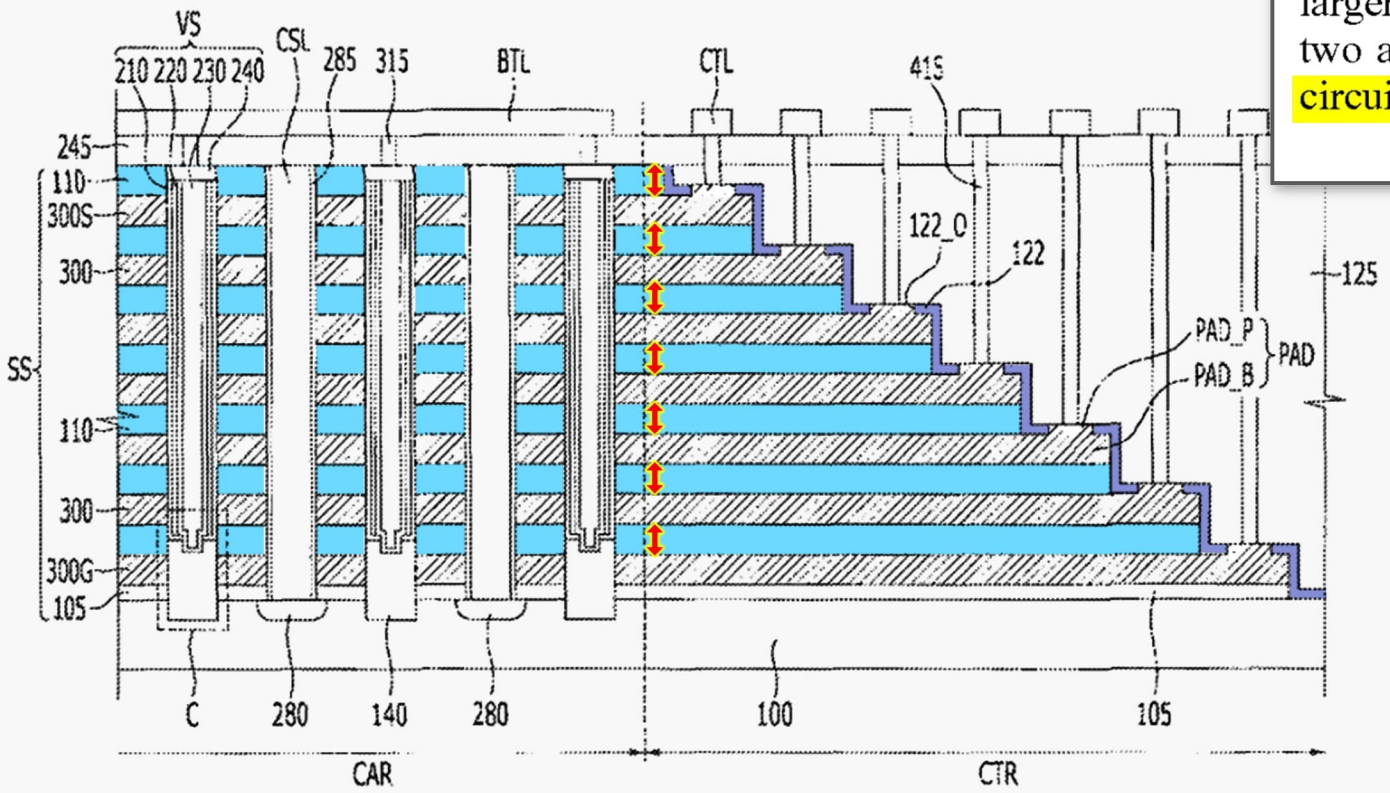
Kim

Further, the short-circuit between the pad units PAD may be effectively prevented through the auxiliary insulating layer **122** positioned between the adjacent protrusion pads PAD_P positioned at different rows. The semiconductor memory device according to same embodiments of the inventive concepts may have enhanced reliability.

Ex. 1005 (Kim), 9:50-55

Petitioner Provides No Motivation To Modify Kim

FIG. 4B



Ex. 1005 (Kim), Fig. 4B

Kim

positioned at the n+1-th row based on the substrate 100. A z-direction thickness of the insulating layer **110** may be larger than the minimum distance in the z-direction between two adjacent pad units PAD to effectively prevent a short-circuit between the two adjacent pad units PAD.

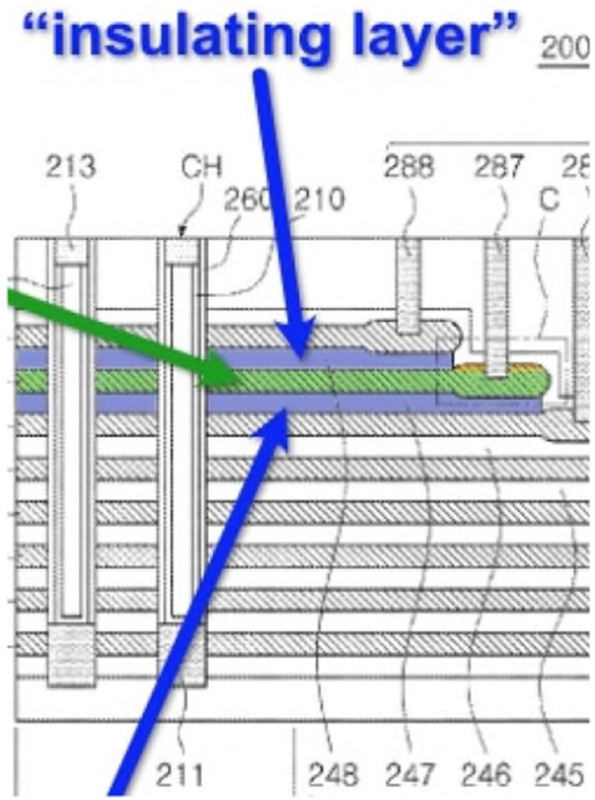
Ex. 1005 (Kim), 9:7-11

Agenda

- '666 Patent and Claim 19
- Claim Construction
- Ground 1 (Kim) Fails
- **Ground 2 (Nam) Fails**
- Ground 3 (Lee+Park) Fails

Petitioner Failed To Clearly Specify Ground 2

"insulating layer" as layer 248



Pet. 70 (Fig. 7, concentrated)

"insulating layer" as layers 248 and 271

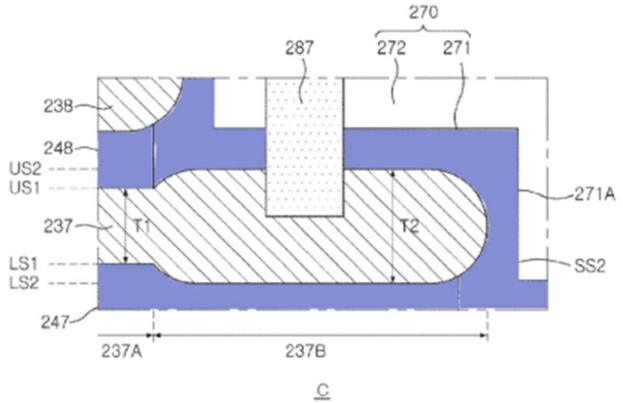


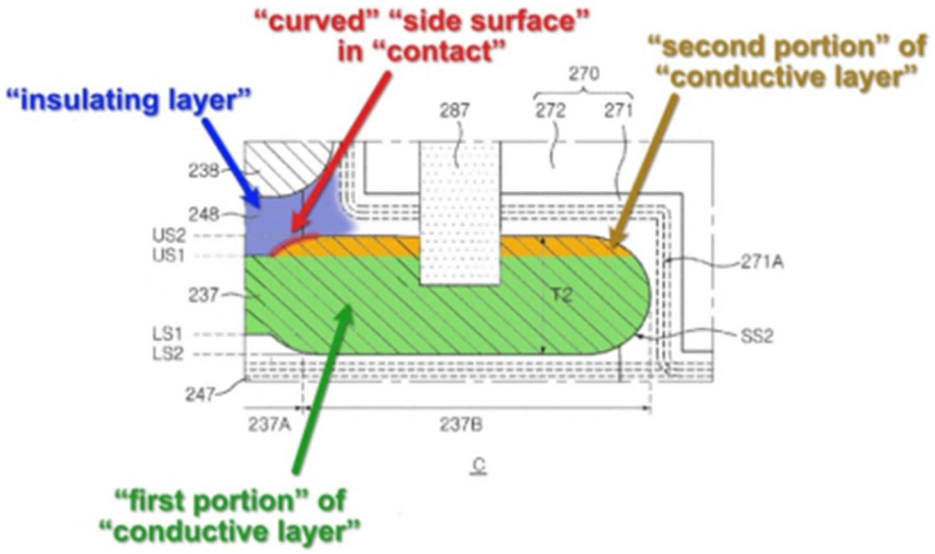
FIG. 8A

Ex.2014 (Lee Dep. Ex. 4); Pet. 60 ("A POSITA would have considered both Nam's insulating layer 240 and the adjacent insulating layer 271 to be the claimed 'insulating layer.'")

POR 3

Petitioner Failed To Clearly Specify Ground 2

"insulating layer" as layer 248 & portion of layer 271



Pet. 65

"insulating layer" as layer 248 & different portion of layer 271

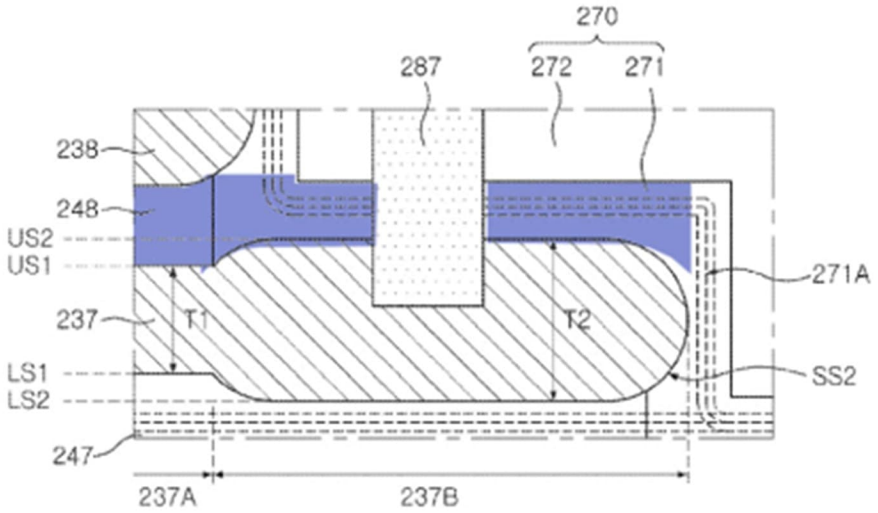


FIG. 8A

Ex.2018 (Lee Dep. Ex. 8)

POR 3

Ground 2 Fails To Show Curved Side Surface In Contact With Side Surface Of Insulating Layer

Petitioner's Reply

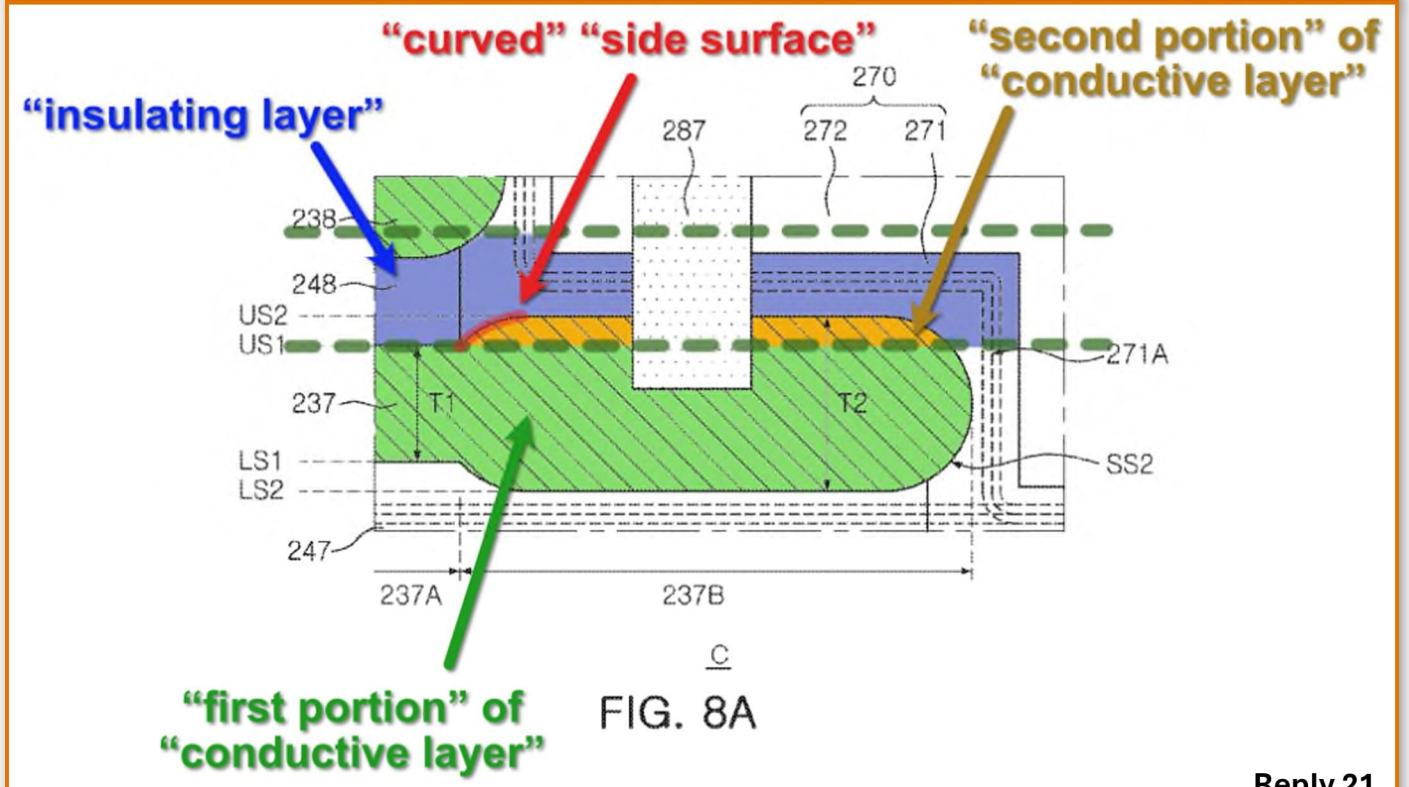
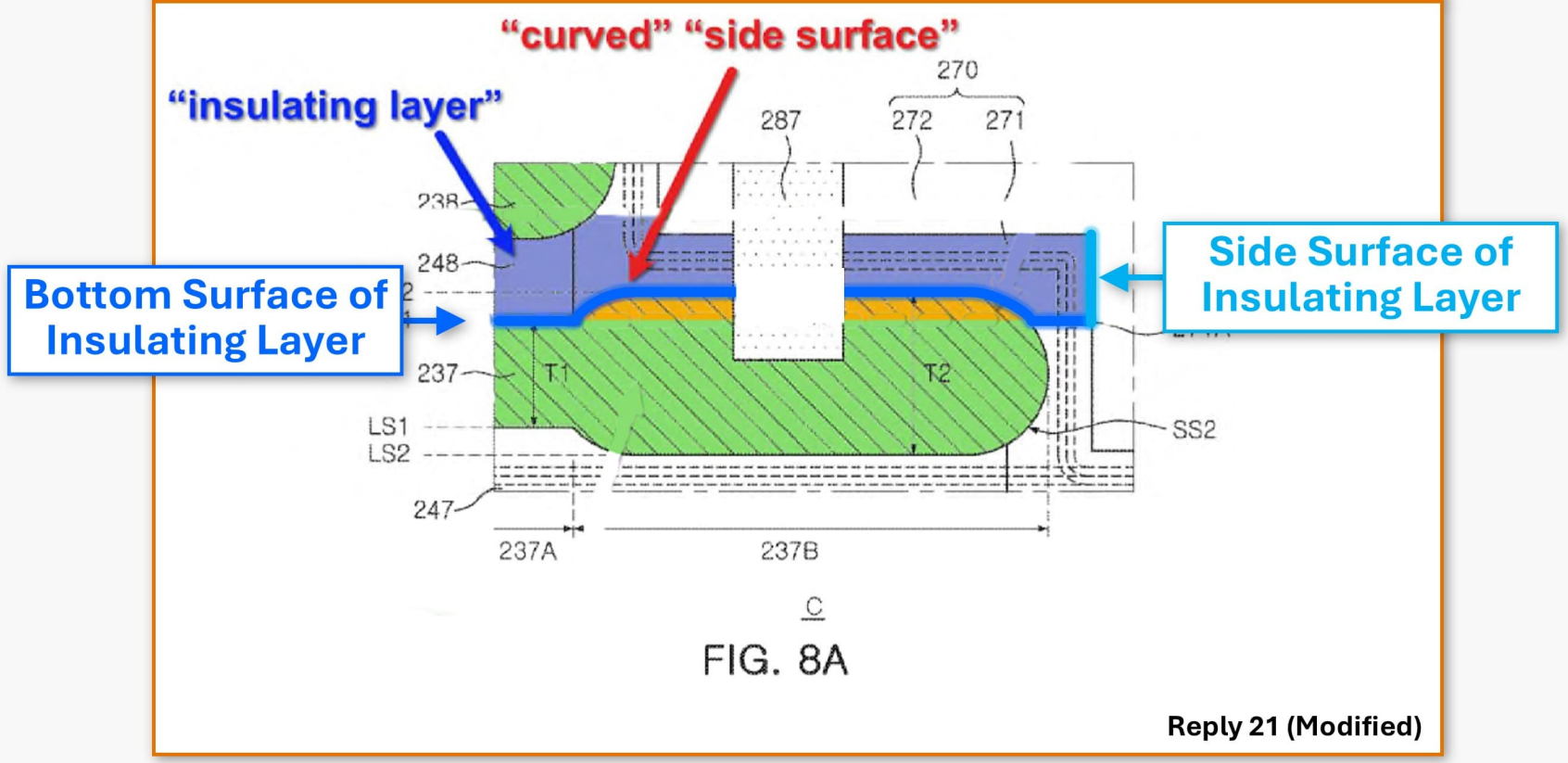


FIG. 8A

Reply 21

Ground 2 Fails To Show Curved Side Surface In Contact With Side Surface Of Insulating Layer

Petitioner's Reply



Reply 21 (Modified)

Ground 2 Fails To Show Insulating Layer Over Only A First Portion Of Conductive Layer

Lee Deposition Ex. 9

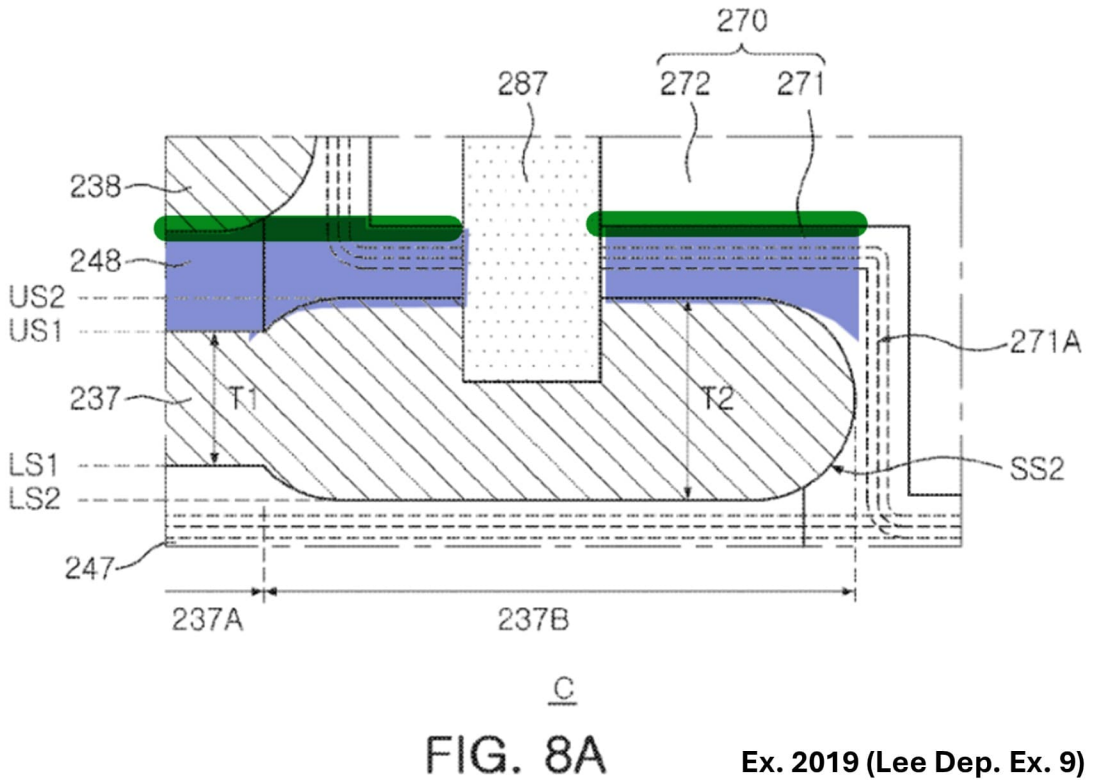


FIG. 8A

Ex. 2019 (Lee Dep. Ex. 9)

Dr. Lee Deposition

Q. In this Lee Exhibit 9, can you identify the bottom surface of the insulating layer?

A. And what do you mean by the "bottom surface"? The blue regions shows the bottom follow the contour of the contact pad. Is that what you mean?

Q. Sure.

A. Well, if that's what you mean, then the bottom of the layer is following the contour of the blue region. Your question is very confusing.

Ex. 2010 (Jack C. Lee, Ph. D.), 275:5-17

Ground 2 Fails To Show Insulating Layer Over Only A First Portion Of Conductive Layer

Petitioner's Reply

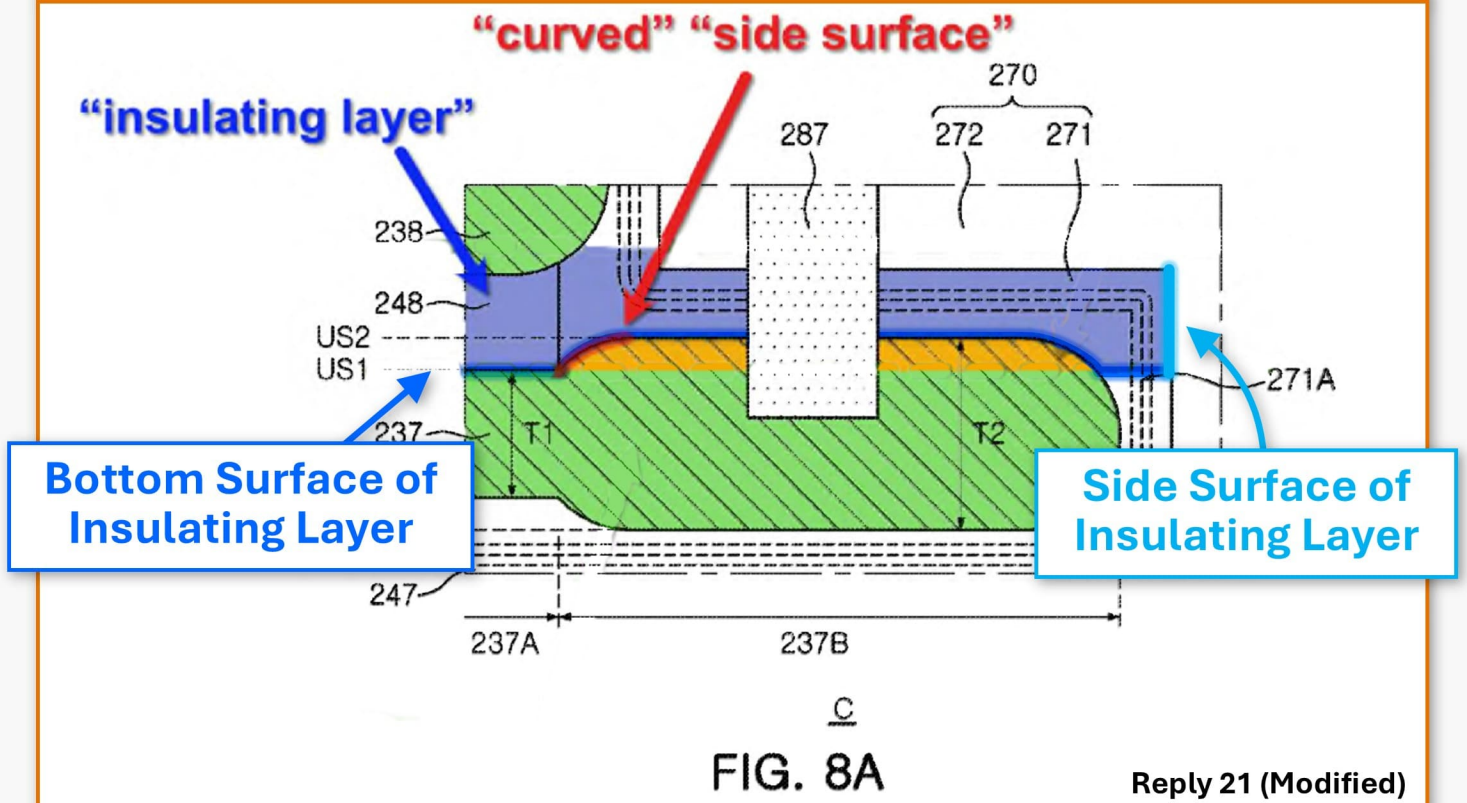


FIG. 8A

Reply 21 (Modified)

17. A memory device, comprising:

a substrate, wherein the substrate comprises a top surface;

a memory string disposed over the substrate; and

a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:

a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.

Ex. 1001 ('666 Patent), Claim 17

19. The memory device of claim **17**, wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack.

Ex. 1001 ('666 Patent), Claim 19

Agenda

- '666 Patent and Claim 19
- Claim Construction
- Ground 1 (Kim) Fails
- Ground 2 (Nam) Fails
- **Ground 3 (Lee+Park) Fails**

Ground 3 Fails For Four Reasons

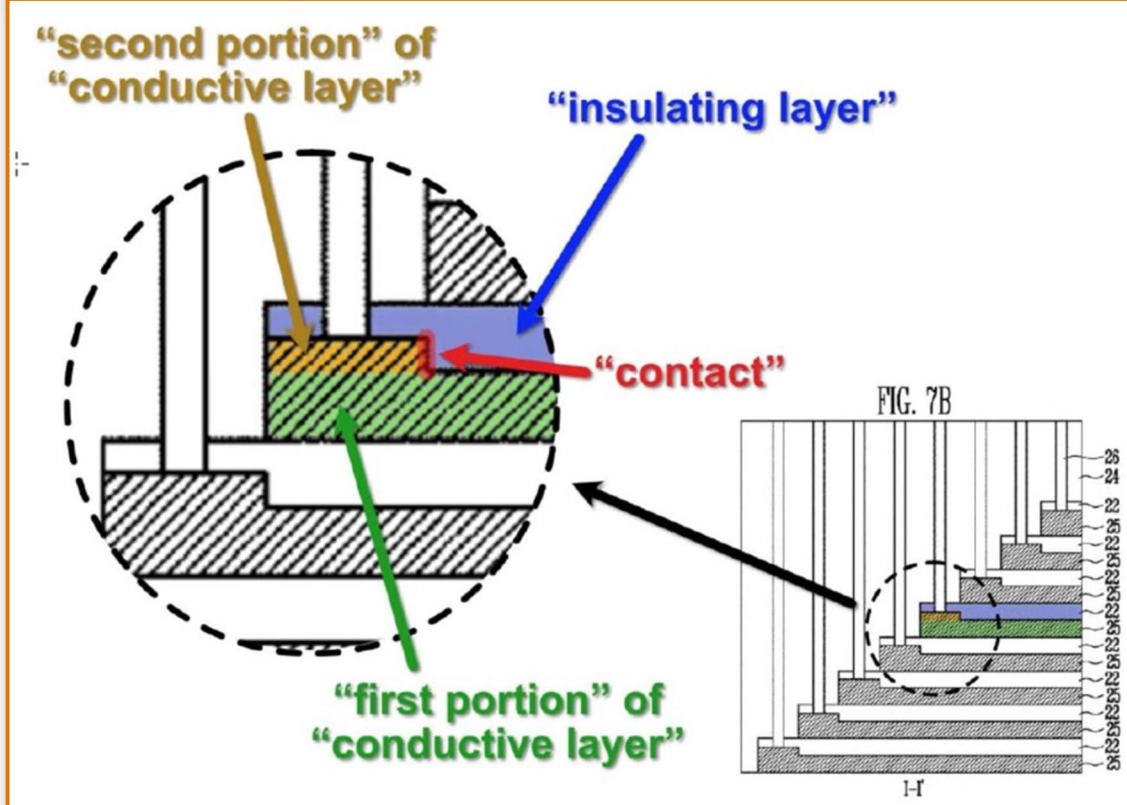
1. Lee cannot be oxidized to form a "curved side surface"
2. A POSITA would not be motivated to oxidize Lee layer 22 because oxidation would increase risk of electrical failure
3. A POSITA would not be motivated to add a "curved side surface" to Lee because it is redundant of Lee's protections
4. Lee lacks an "insulating layer disposed over a first portion of a conductive layer"

Ground 3 Fails For Four Reasons

1. **Lee cannot be oxidized to form a "curved side surface"**
2. A POSITA would not be motivated to oxidize Lee layer 22 because oxidation would increase risk of electrical failure
3. A POSITA would not be motivated to add a "curved side surface" to Lee because it is redundant of Lee's protections
4. Lee lacks an "insulating layer disposed over a first portion of a conductive layer"

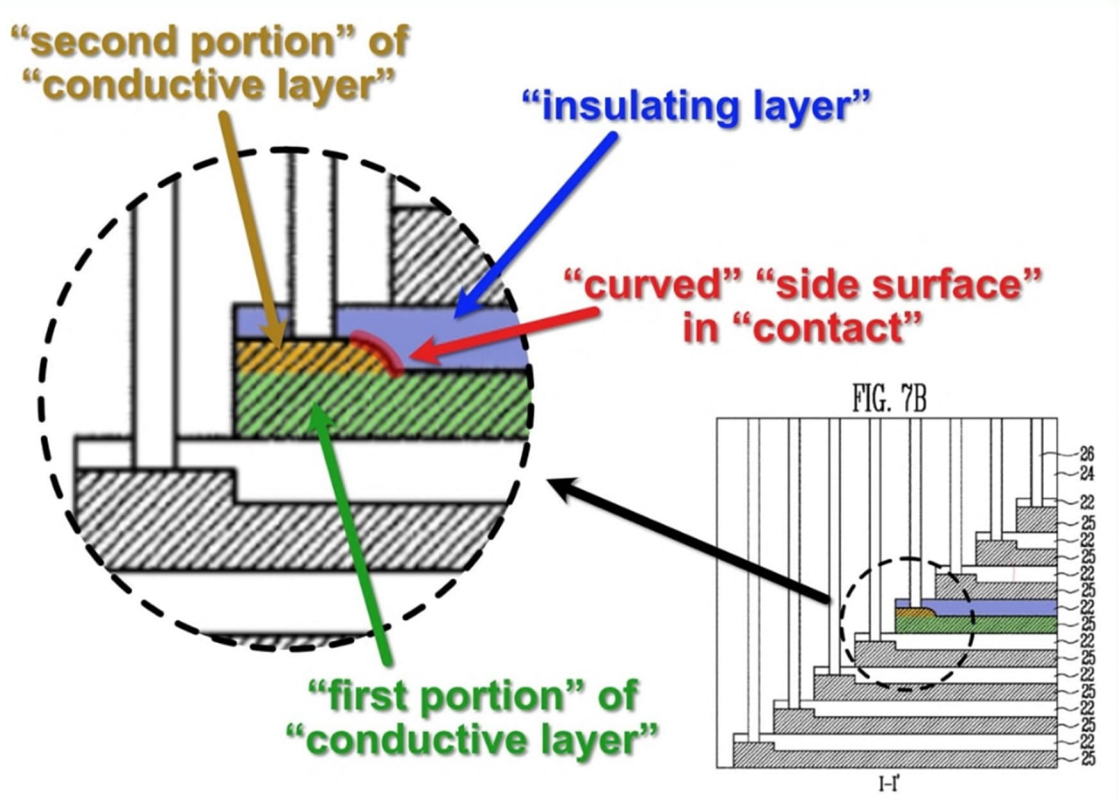
Lee Does Not Teach A "curved side surface"

Actual Figure From Lee



POR 61

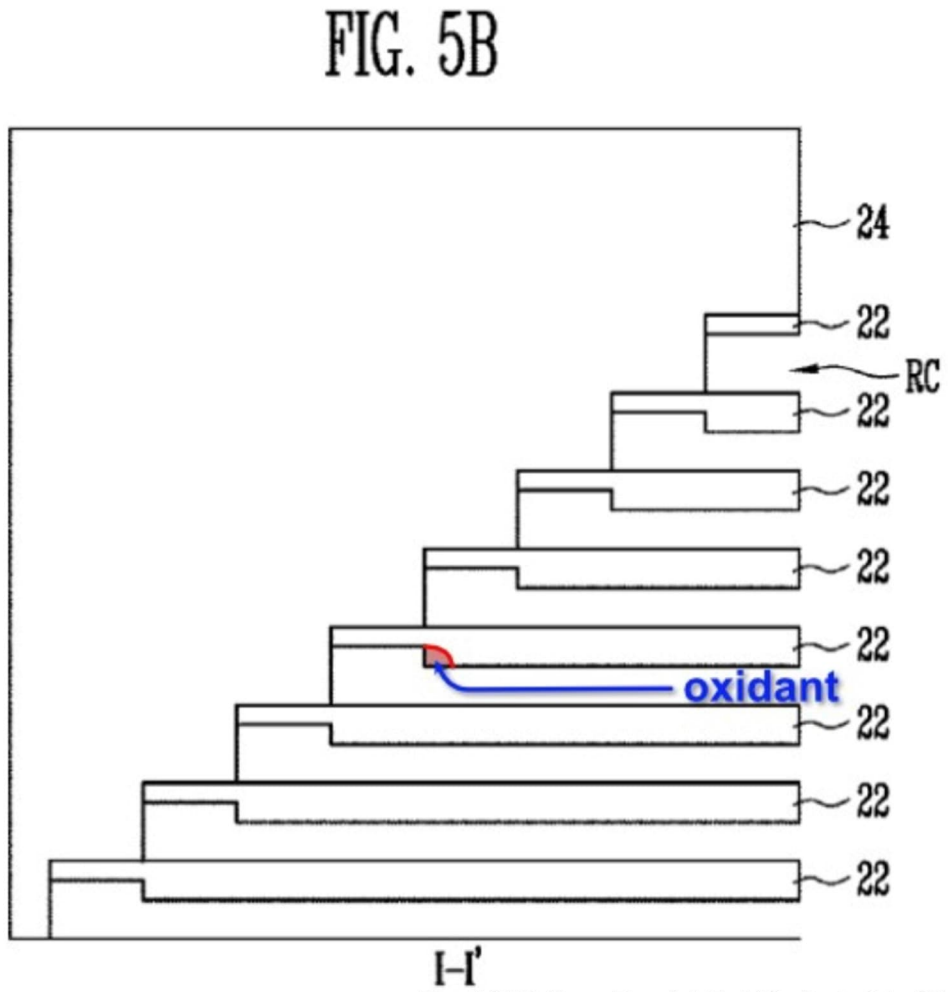
Petitioner's Modified Figure



Pet. 84

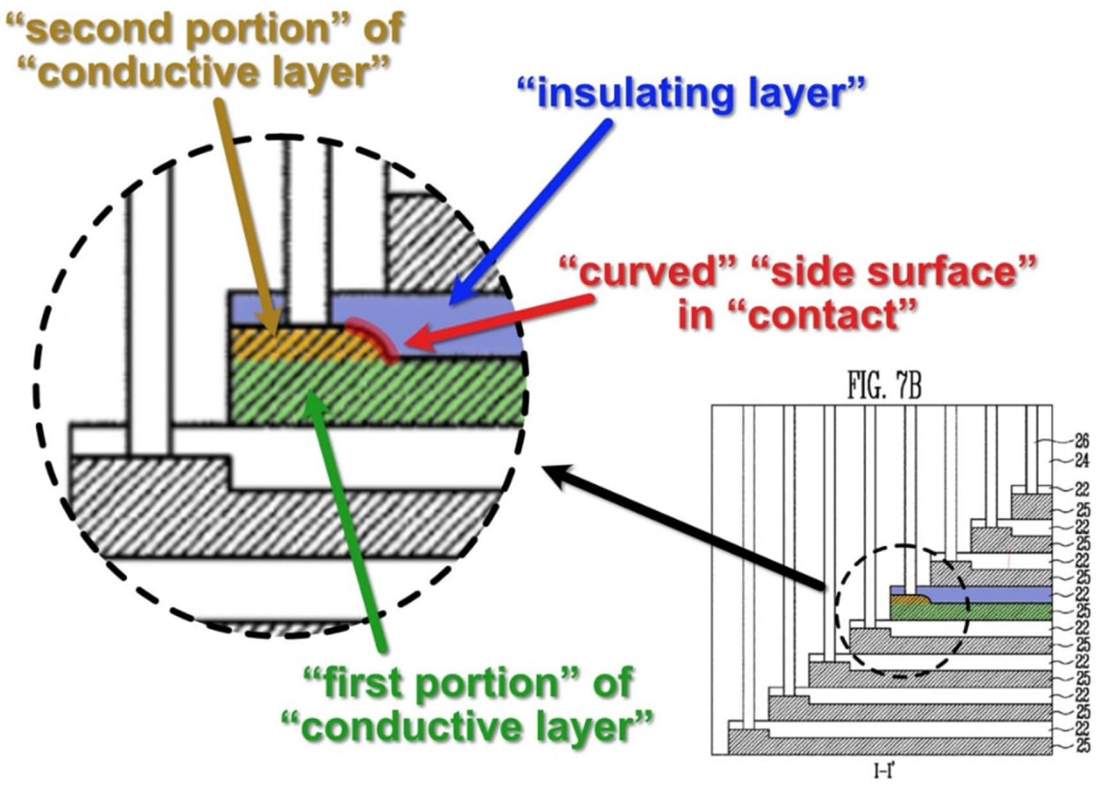
Petitioner's Modification Of Lee Is Technically Unfeasible

Dr. Lee Declaration



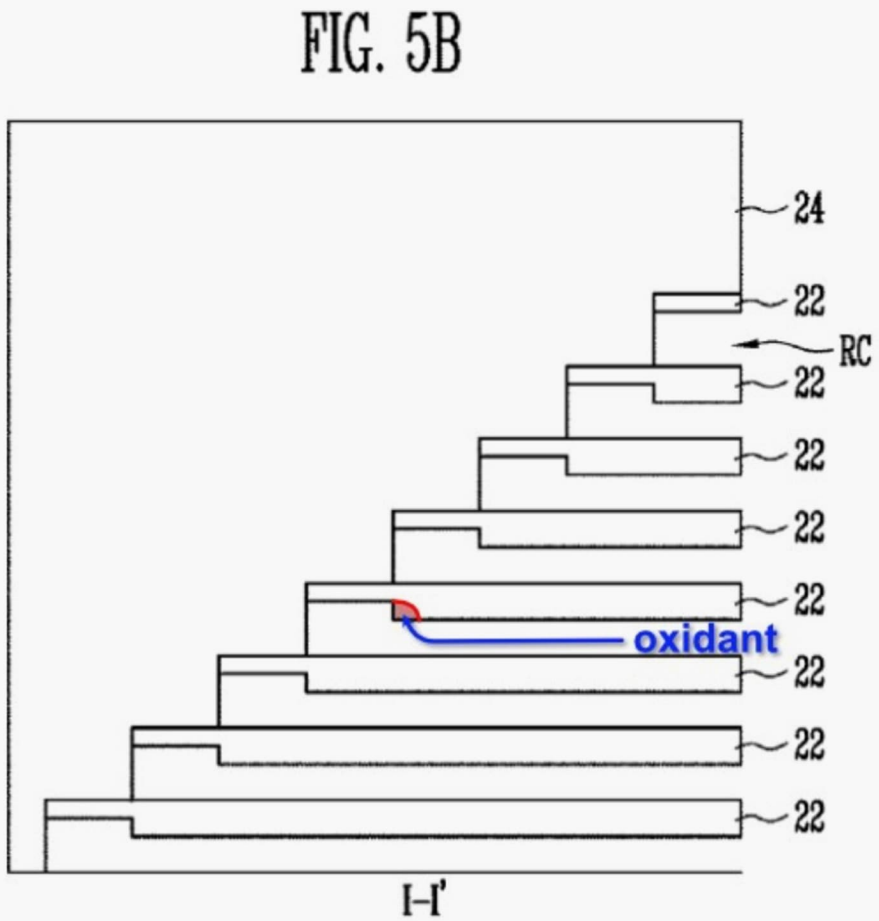
Ex. 1003 (Lee Decl.) ¶ 413; Pet. 84, 89

Petitioner's Modified Figure



Pet. 84

Lee's Layer 22 Does Not Oxidize



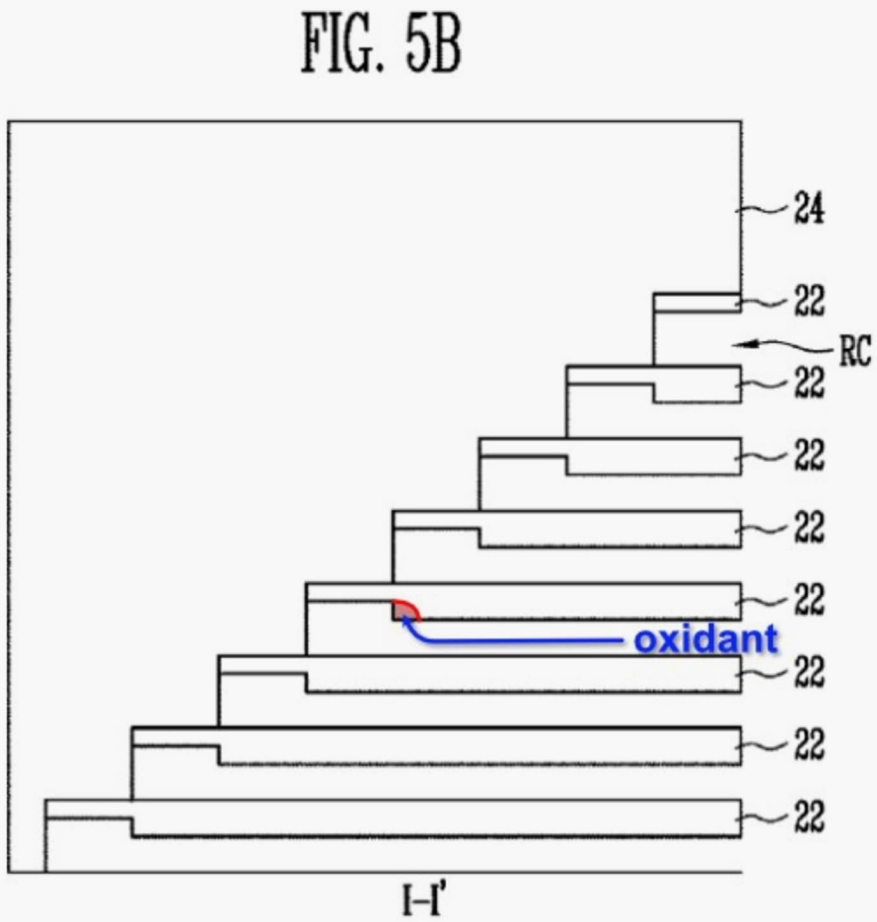
Ex. 1003 (Lee Decl.) ¶ 413; Pet. 84, 89

Lee

[0030] The first material layers **21** may be formed of materials having a high etch selectivity with respect to the second material layers **22**. For example, the first material layers **21** may include a conductive layer such as a polysilicon layer, and the second material layers **22** may include an insulating layer such as an oxide layer. In another example, the first material layers **21** may include a sacrificial layer such as a nitride layer, and the second material layers **22** may include an insulating layer such as an oxide layer.

Ex. 1007 (Lee) [0030]

Dr. Lee Admits "Lee does not oxidize layer 22"



Ex. 1003 (Lee Decl.) ¶ 413; Pet. 84, 89

Dr. Lee Deposition

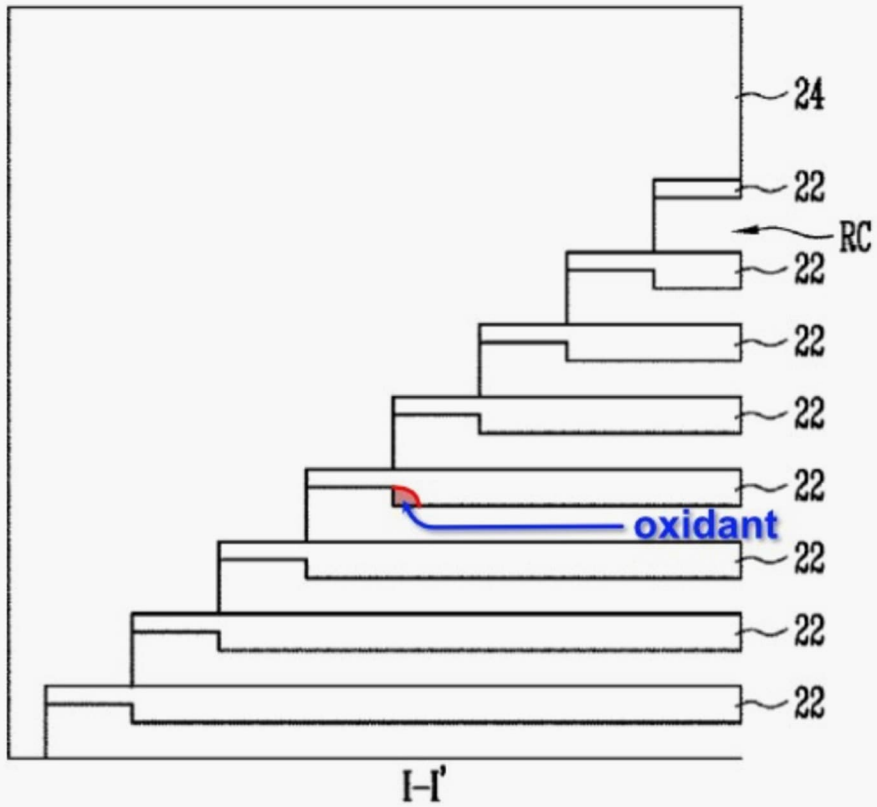
Q. So Lee never describes oxidizing layer 22, correct?

A. Sorry, it's getting late and -- I believe you're correct. Lee does not oxidize layer 22.

Ex. 2024 (Jack C. Lee, Ph. D.), 185:13-16

Dr. Lee Admits Lee's Layer 22 Is "not designed to oxidize"

FIG. 5B



Ex. 1003 (Lee Decl.) ¶ 413; Pet. 84, 89

Dr. Lee Deposition

Q. So layers 22 is not subject to any subsequent oxidation, correct?

A. You're right. It's not -- in general, even if it is exposed to even -- it might oxidize slightly but not very much. At least it's not designed to oxidize.

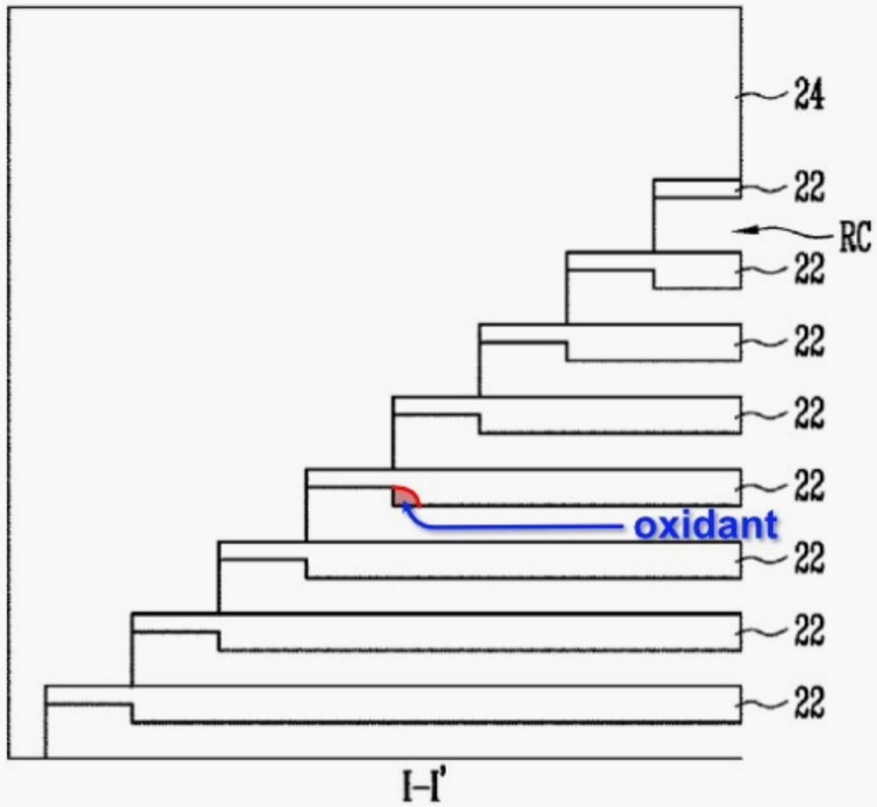
Q. If layer 22 were able to be oxidized at the end of the staircase, these pads would be shortened. Is that fair to say?

A. Again, it's not designed to be oxidized.

Ex. 2024 (Jack C. Lee, Ph. D.),186:3-14

Lee's Layer 22 Does Not Oxidize

FIG. 5B



Ex. 1003 (Lee Decl.) ¶ 413; Pet. 84, 89

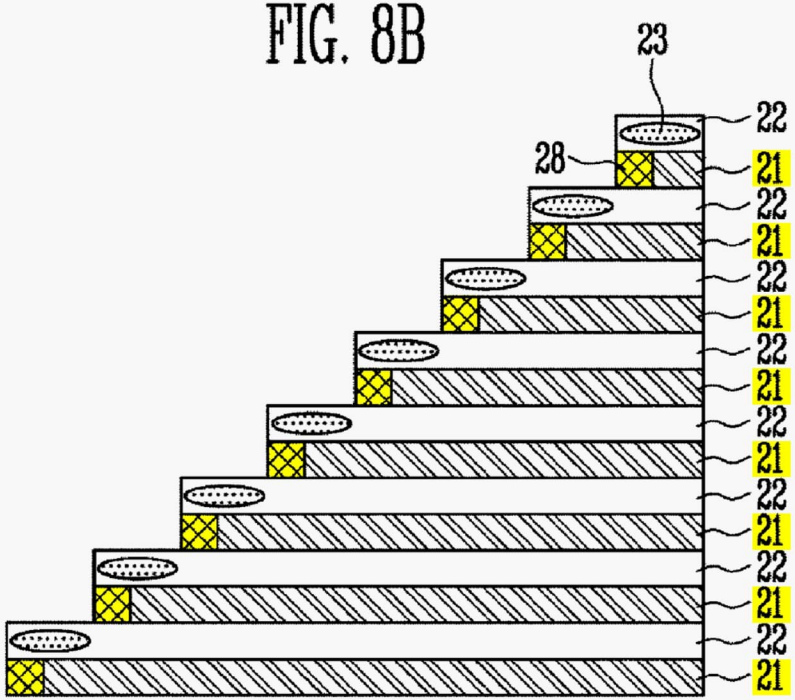
Professor Giapis Declaration

133. In contrast to Park, introducing such an oxidant into the openings of Lee's structure above will not promote further oxidation to the existing oxide layers 22. Any sacrificial layer 21 has already been removed in the relevant region that Dr. Lee annotates in Lee Figure 5B, so nothing remains to be oxidized. *See* Ex. 1007 (Lee) at [0036]. Nor would introducing an oxidant change the shape of the existing oxide layers 22. It is not possible to further oxidize a solid oxide material with oxygen gas as in Park. That is why Park's

Ex. 2023 ¶ 133

Lee Oxidizes Layer 21, Not Layer 22

FIG. 8B



Ex. 1007 (Lee), Fig. 8B

Lee

[0030] The first material layers **21** may be formed of materials having a high etch selectivity with respect to the second material layers **22**. For example, the first material layers **21** may include a conductive layer such as a polysilicon layer, and the second material layers **22** may include an insulating layer such as an oxide layer. In another example, the first material layers **21** may include a sacrificial layer such as a nitride layer, and the second material layers **22** may include an insulating layer such as an oxide layer.

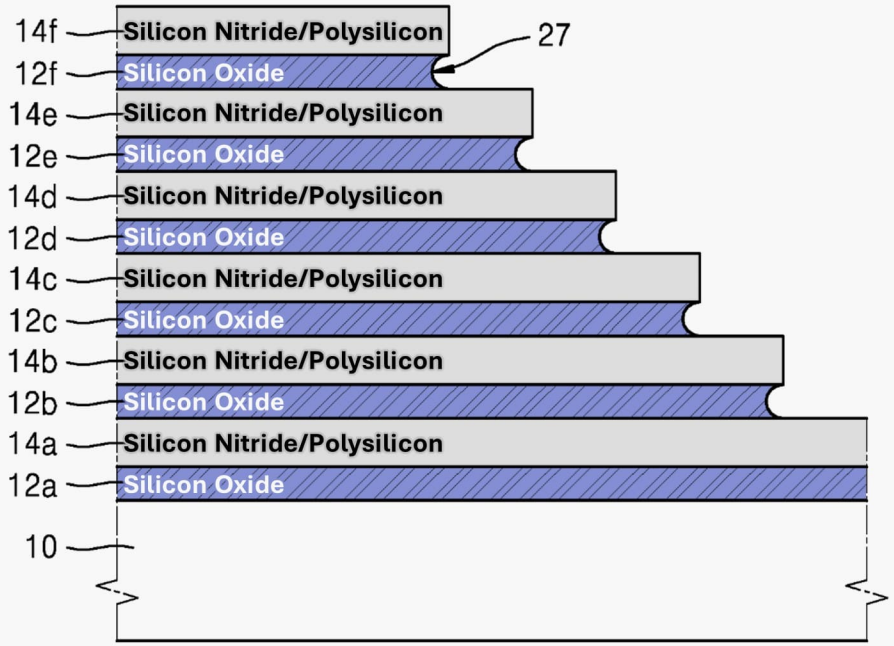
Ex. 1007 (Lee), [0030]

[0048] As illustrated in FIG. **8**A, before an impurity implantation process is performed, a barrier layer **27** may be formed on the entire surface of the intermediate resultant structure that is patterned stepwise. Alternatively, as illustrated in FIG. **8**B, before an impurity implantation process is performed, side walls of the first material layers **21** exposed at respective steps may be oxidized to thereby form a plurality of barrier layers **28**.

Ex. 1007 (Lee), [0048]

Park Does Not Oxidize Oxide Layers

FIG. 6B



Ex. 1008 (Park), Fig. 6B (annotated)

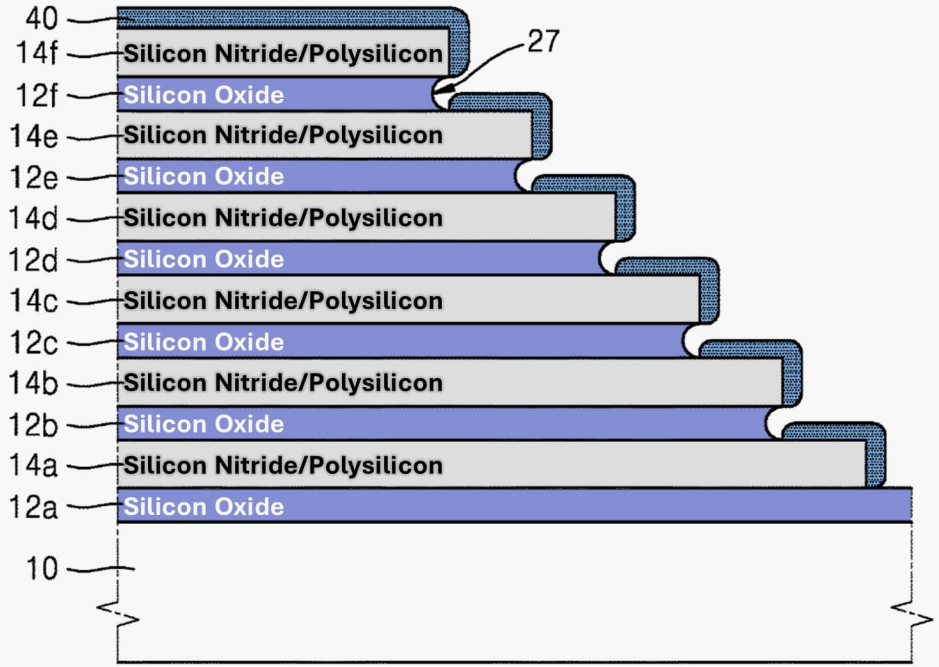
Park

The interlayer insulating layer patterns **12***a* through **12***f* may be formed of a silicon oxide layer. The sacrificial layer patterns **14***a* through **14***f* may be formed of a material having an etching selectivity with respect to the interlayer insulating layer patterns **12***a* through **12***f*. The sacrificial layer patterns **14***a* through **14***f* may be formed of a material such as a silicon nitride layer or a polysilicon layer. The interlayer

Ex. 1008 (Park), 8:1-7

Park Does Not Oxidize Oxide Layers

FIG. 6C



Ex. 1008 (Park), Fig. 6C (annotated)

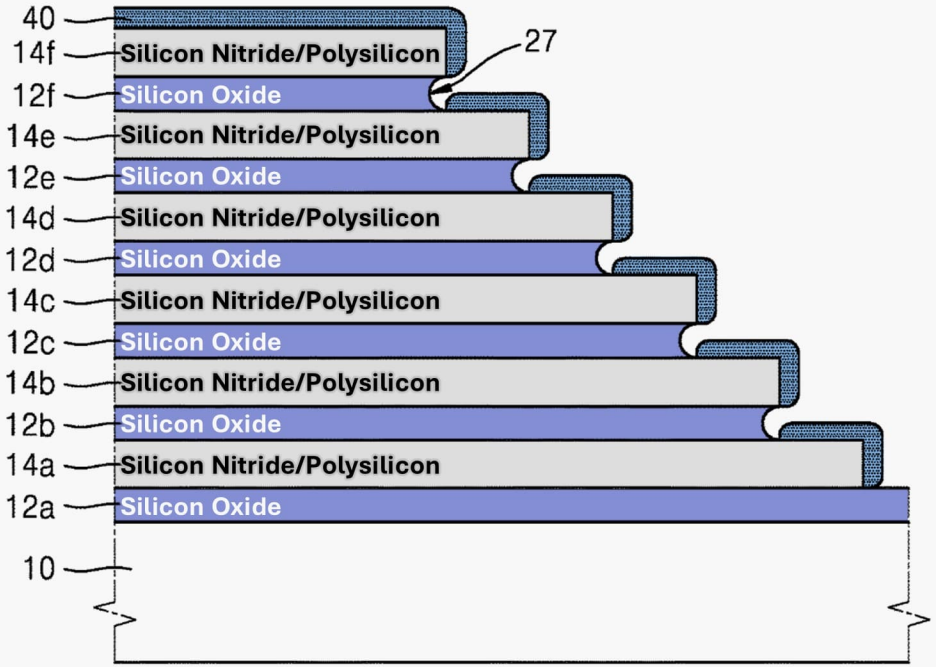
Park

As shown in FIG. **6**C, an additional insulating layer **40** is formed by oxidizing surfaces and side surfaces of the stepped sacrificial layer patterns **14***a* through **14***f* that are externally exposed. The additional insulating layer **40** may

Ex. 1008 (Park), 8:28-31

Park Does Not Oxidize Oxide Layers

FIG. 6C



Ex. 1008 (Park), Fig. 6C (annotated)

Dr. Lee Deposition

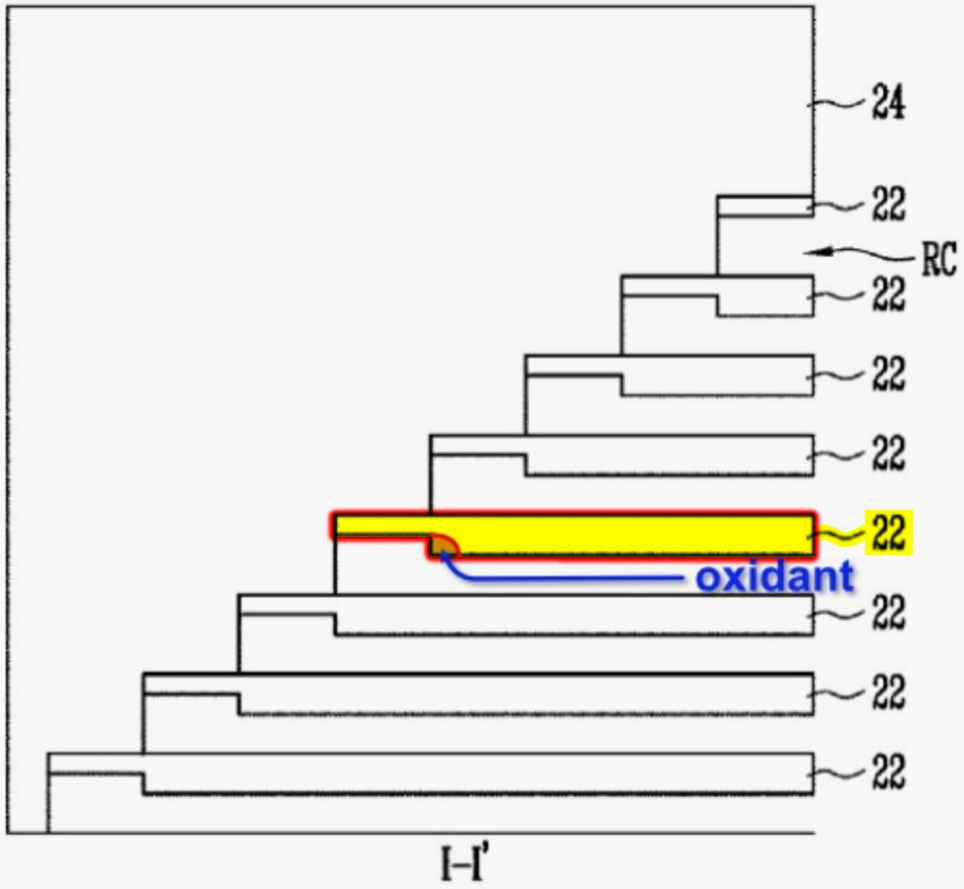
Q. Okay. Can you point to me where the oxidant is added in Park Figure 7 to form the rounded pads?

A. Well, it's due to the oxidation step as shown in Figure 6C. Figure 6C is -- the additional insulating layer 40 is formed by oxidizing the surface and the side surface of the step sacrificial layer patterns 14a through 14f that are externally exposed.

Ex. 2024 (Jack C. Lee, Ph. D.),136:14-22

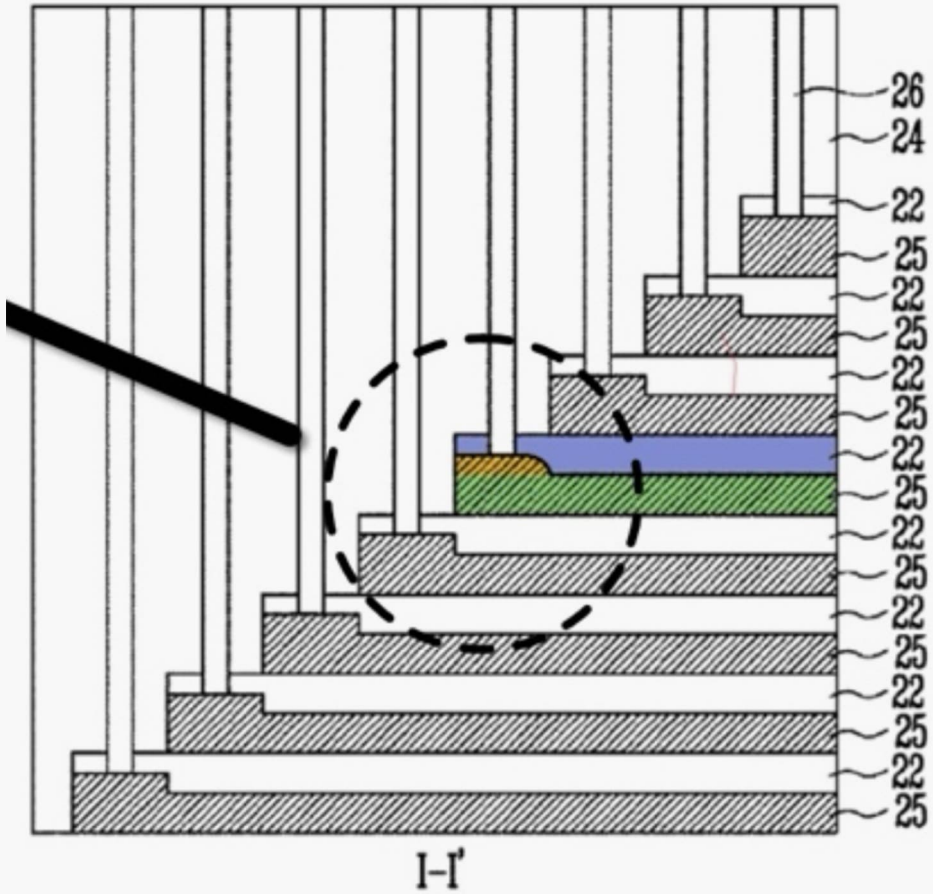
Petitioner's Change Removes Parts Of Layer 22

FIG. 5B



Ex. 1003 (Lee Decl.) ¶ 413; Pet. 84, 89

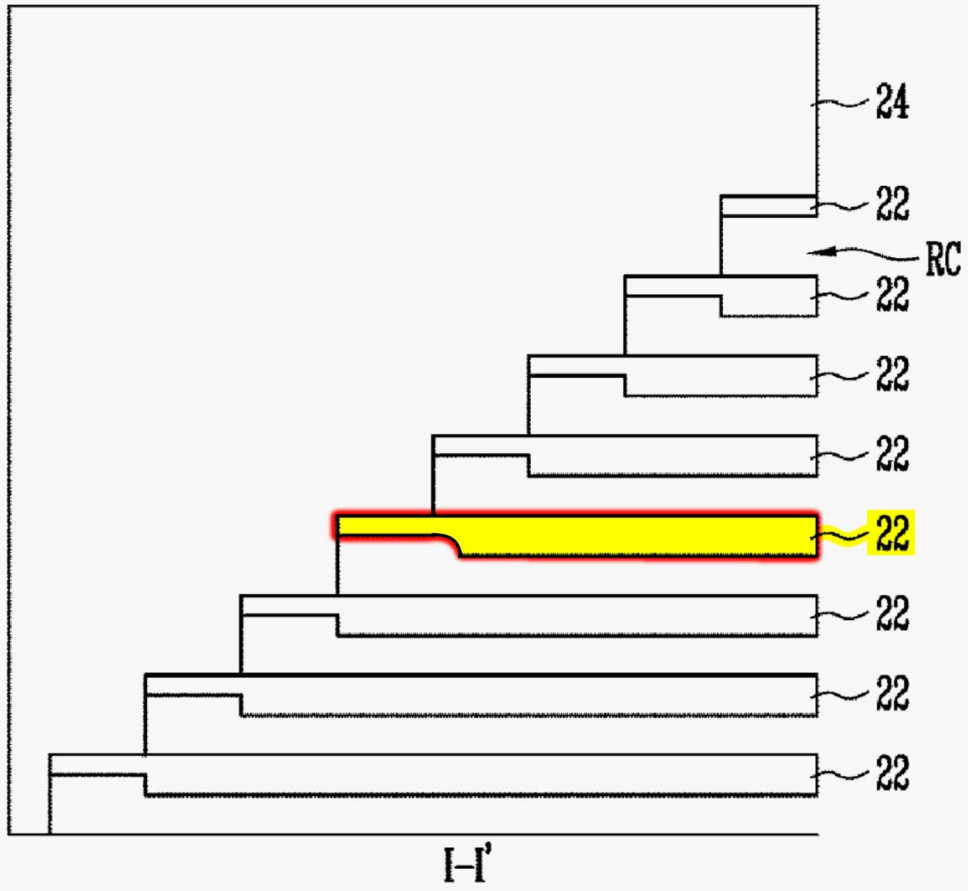
FIG. 7B



Ex. 1003 (Lee Decl.) ¶ 415

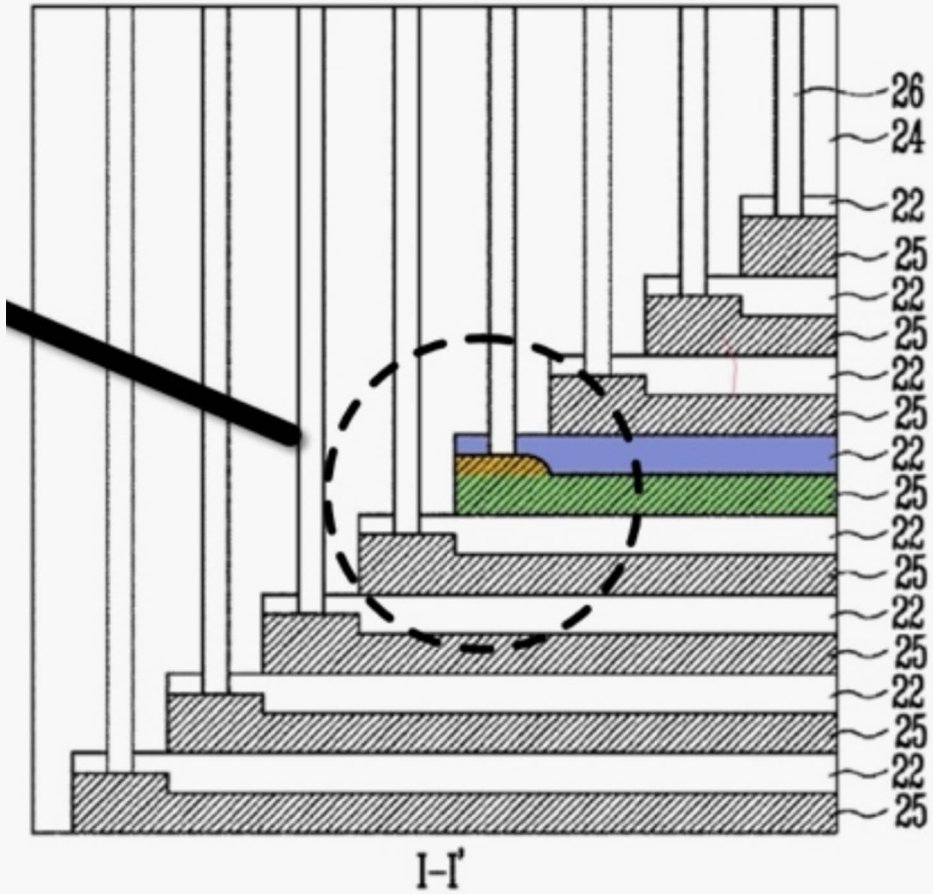
Petitioner's Change Removes Parts Of Layer 22

FIG. 5B



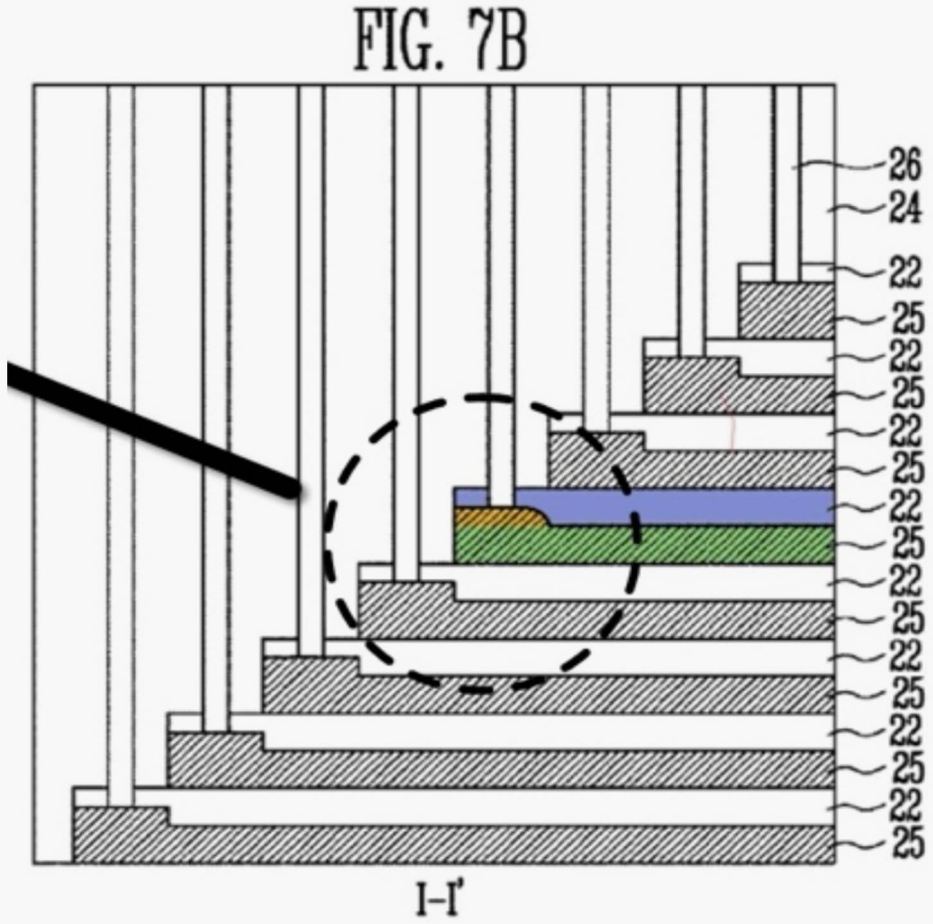
Ex. 1007 (Lee), Fig. 5B (modified)

FIG. 7B



Ex. 1003 (Lee Decl.) ¶ 415

Oxidation Processes Grow The Layer, Not Remove It



Ex. 1003 (Lee Decl.) ¶ 415

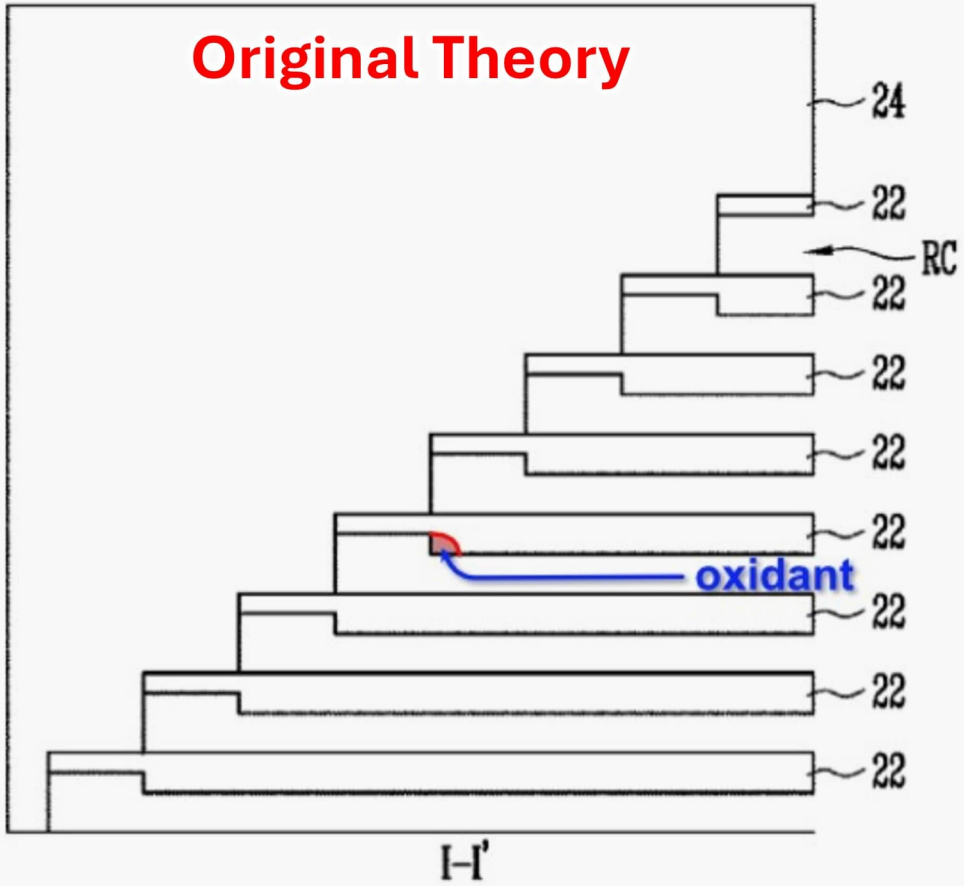
Professor Giapis Declaration

136. To go from the above figure to Dr. Lee's figure under paragraph 415 of his declaration suggests that he is somehow removing part of insulating layer 22, but Dr. Lee never mentions any removal. By contrast, the oxidation process in Park that he is combining with Lee is a growing of an oxide layer. This can be

Ex. 2023 ¶ 136

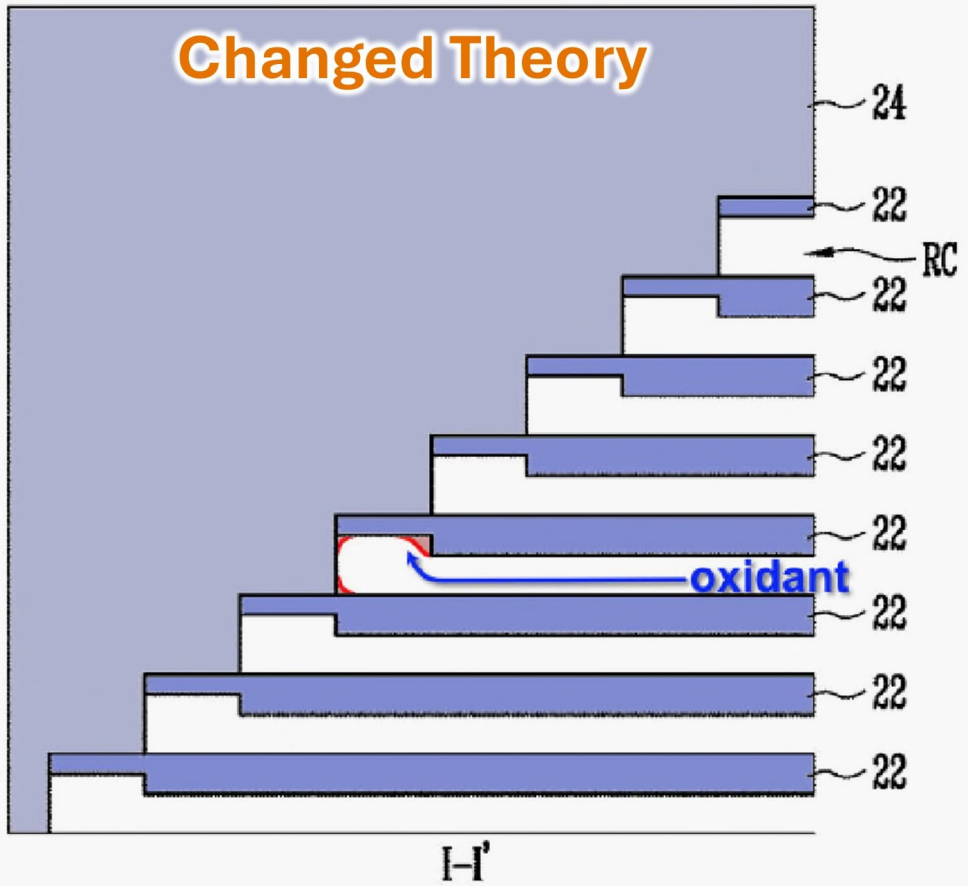
Petitioner Changes Its Theory In Reply

FIG. 5B



Ex. 1003 (Lee Decl.) ¶ 413; Pet. 84, 89

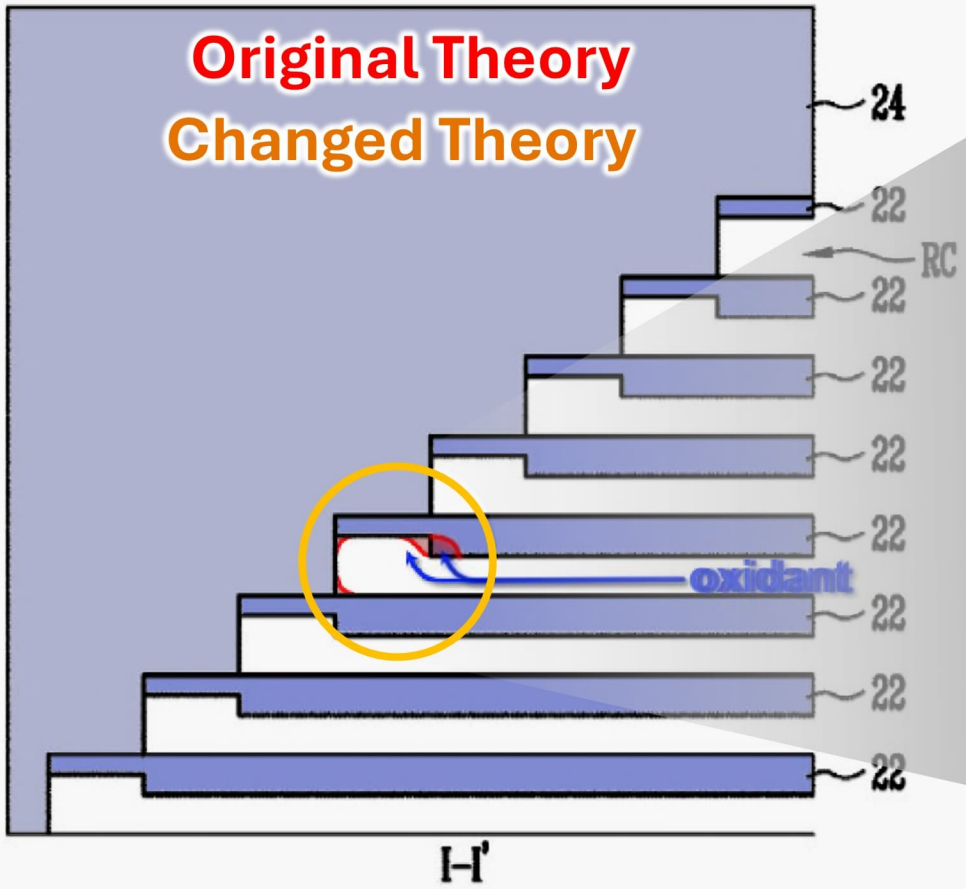
FIG. 5B

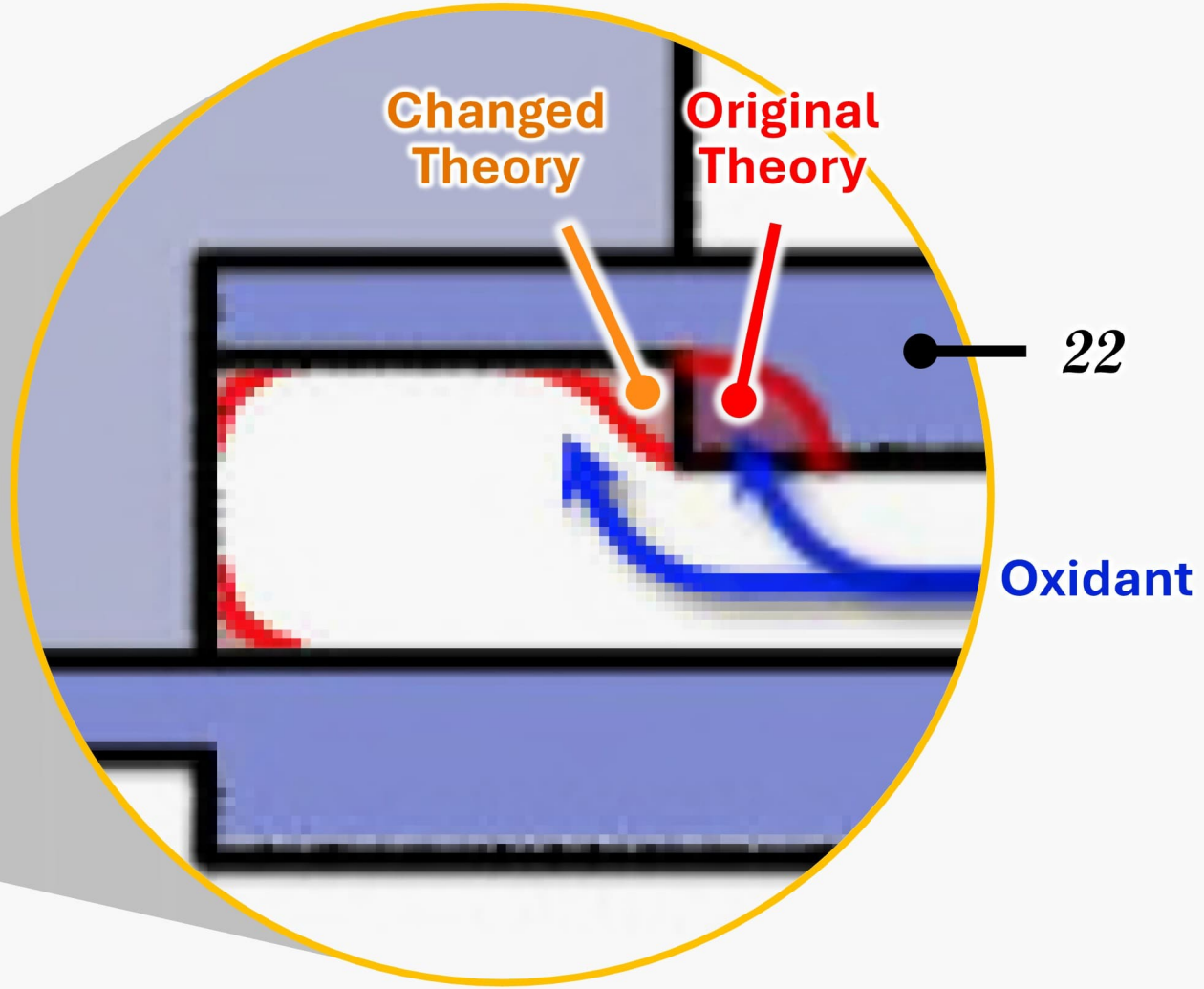


Reply 25

Petitioner Changes Its Theory In Reply

FIG. 5B

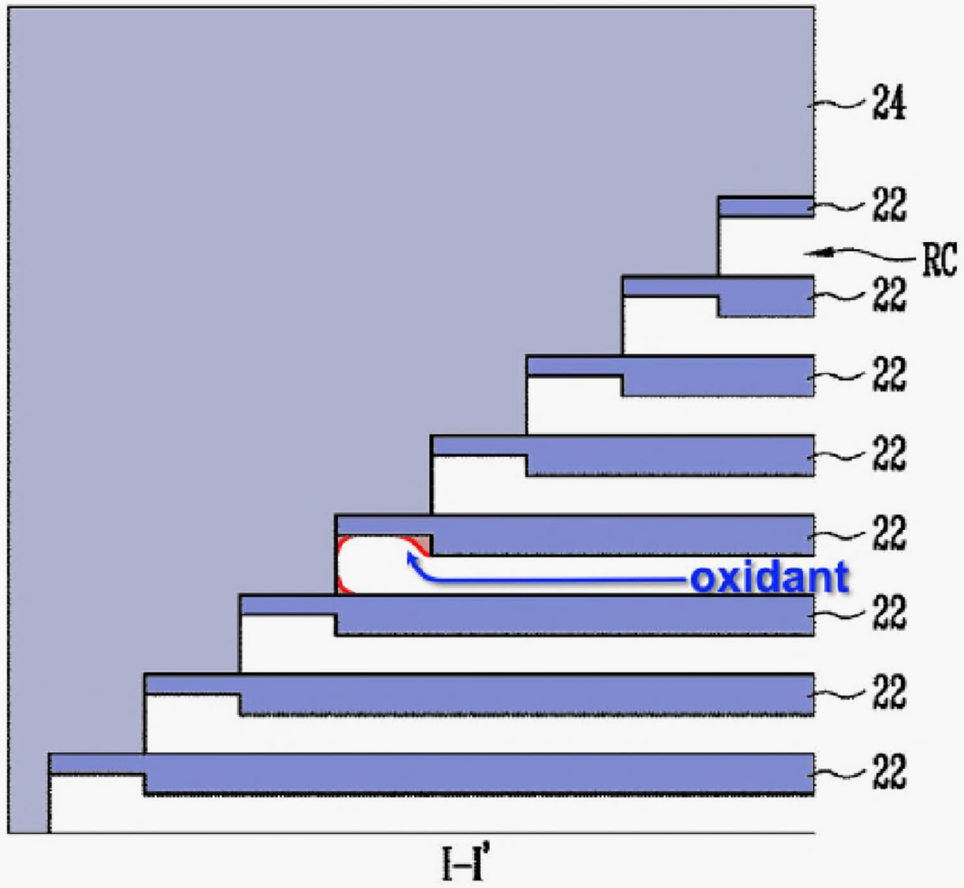




Ex. 1003 (Lee Decl.) ¶ 413; Pet. 84, 89 ; Reply 25 (stacked)

Petitioner's New Theory Argues Layer 22 Is Nonstoichiometric Oxide

FIG. 5B



Reply 25

Petitioner's Reply

Lee, however, explains that its insulation layers are formed from "oxide" (Lee, ¶ [0030]), not necessarily completely pure "silicon dioxide" as Patent Owner appears to assume. When the '666 patent was filed, silicon oxide films with non-memory). Because it contains excess silicon, this type of non-stoichiometric oxide layer ***is*** further oxidized when it is exposed to an oxidant. Ex. 1027, ¶¶ 79-88, 90-98; Ex. 2010, 261:20-266:1.

* * *

Reply 24

Petitioner's New Theory Is Improper

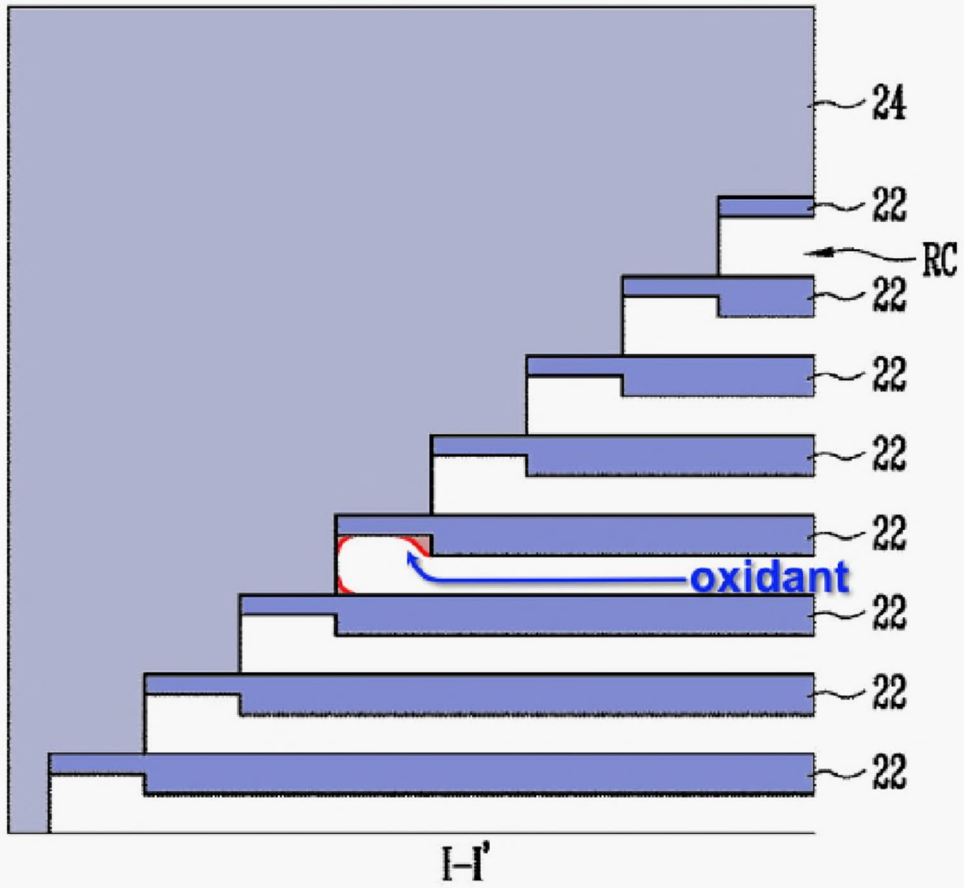
Intelligent Bio-Systems v. Illumina Cambridge

"Unlike district court litigation—where parties have greater freedom to revise and develop their arguments over time and in response to newly discovered material—the expedited nature of IPRs bring with it an obligation for petitioners to make their case in their petition to institute. While the Board's requirements are strict ones, they are requirements of which petitioners are aware when they seek to institute an IPR."

Intelligent Bio-Systems, Inc. v. Illumina Cambridge, Ltd., 821 F.3d 1359, 1369 (Fed. Cir. 2016)

Lee Layer 22 Is Deposited As "silicon dioxide"

FIG. 5B



Reply 25

Dr. Lee Deposition

Q. If oxidation in Lee occurred on the edge of the staircase, would layer 22 be oxidized?

A. Well, it depends on the state of layer 22, but layer 22 is deposited as an oxide. So -- a silicon dioxide. So at least the purpose of the -- of the process is that that layer is not subject to any subsequent oxidations.

Ex. 2024 (Jack C. Lee, Ph. D.), 185:17-186:2 (objections omitted)

Nonstoichiometric Silicon Oxide Not Used In 3D NAND

Professor Giapis Deposition

Q. A silicon oxide film that includes less than two atoms of oxygen per atom of silicon would be considered nonstoichiometric. True?

A. …So guess what, if you use this type of an oxide in a 3D NAND structure, you're done. The structure will never work because it will not be able to withstand the electric fields that are forming during operation. It will conduct and it will corrupt all your information.

…But it will never be on a -- on a NAND structure. It's just incompatible. It's an unstable oxide.

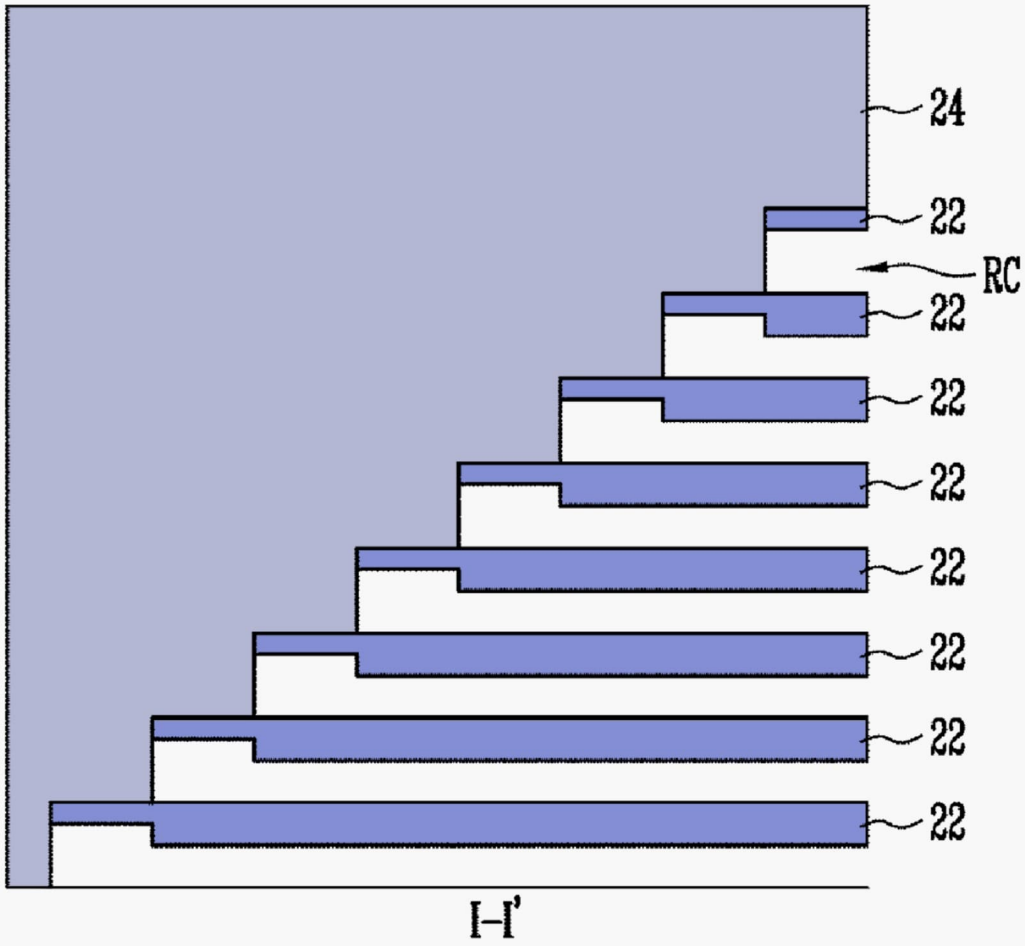
Ex. 1028 (Prof. Konstantinos Giapis), 91:22-95:1

Ground 3 Fails For Four Reasons

1. Lee cannot be oxidized to form a "curved side surface"
2. **A POSITA would not be motivated to oxidize Lee layer 22 because oxidation would increase risk of electrical failure**
3. A POSITA would not be motivated to add a "curved side surface" to Lee because it is redundant of Lee's protections
4. Lee lacks an "insulating layer disposed over a first portion of a conductive layer"

Petitioner Theory Increases Risk Of Short Circuits

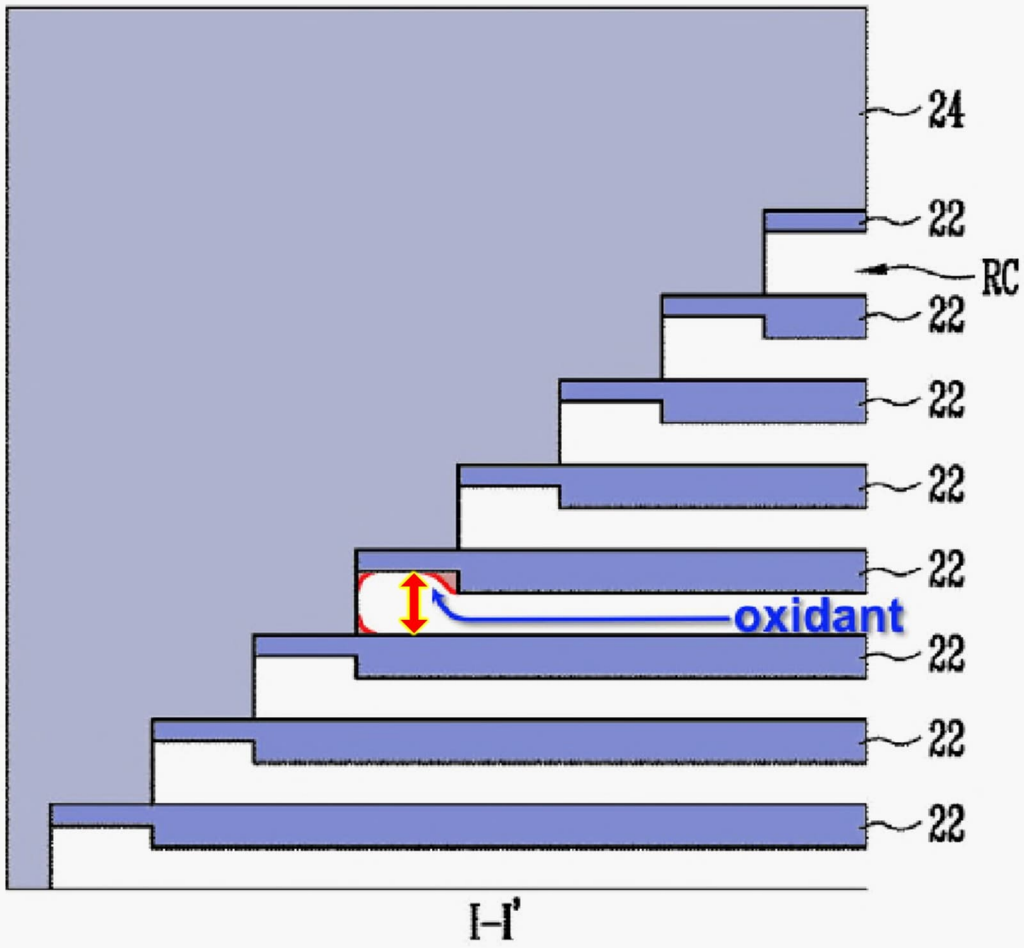
FIG. 5B



Ex. 1007 (Lee), Fig. 5B

Petitioner Theory Increases Risk Of Short Circuits

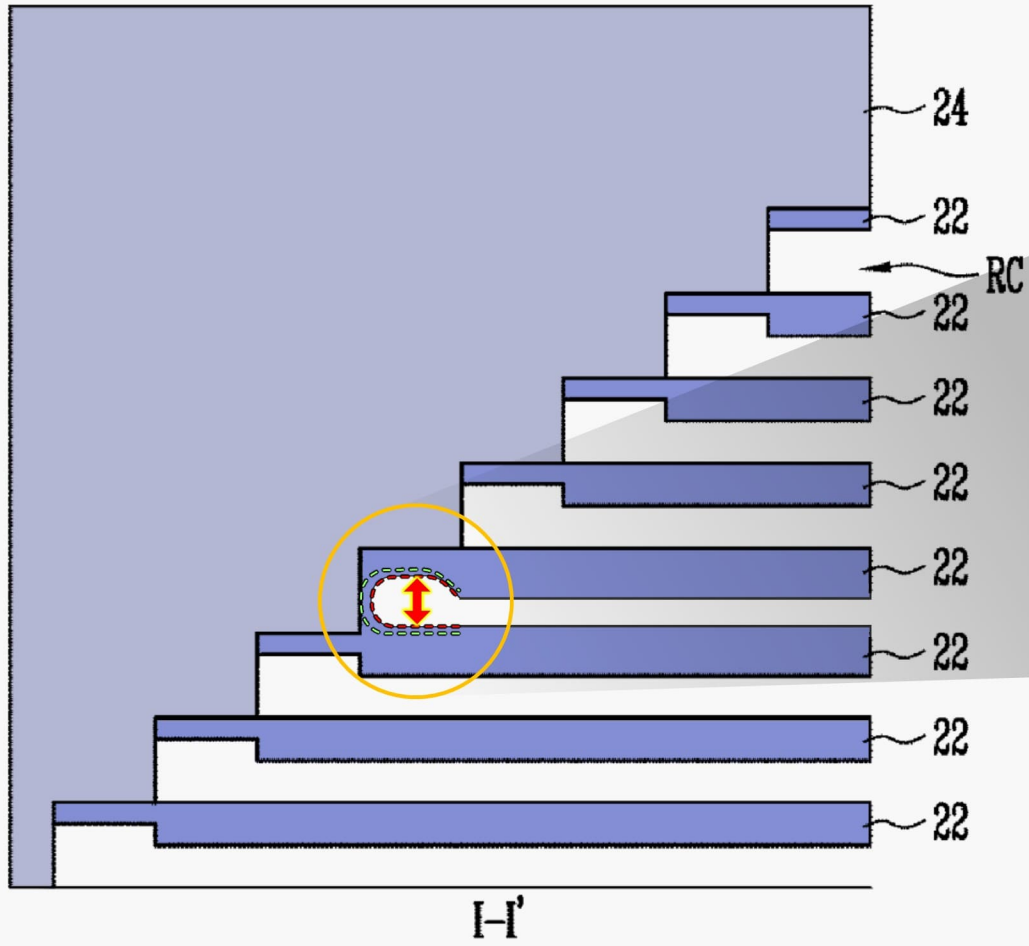
FIG. 5B



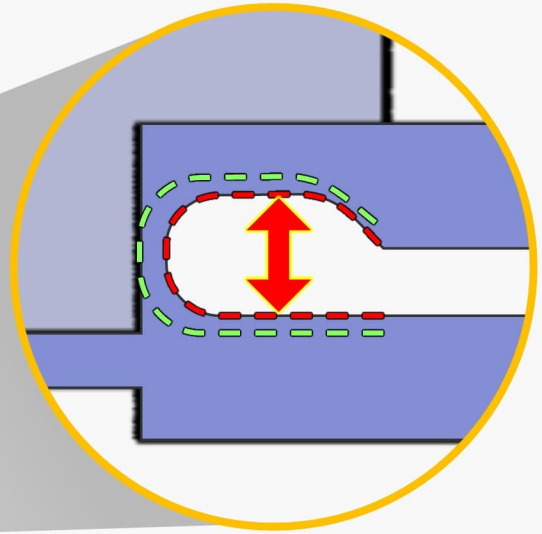
Reply 25

Petitioner Theory Increases Risk Of Short Circuits

FIG. 5B



Thinner Pad Increases Risk of Short Circuits Due To Punchthrough



Ex. 1007 (Lee), Fig. 5B (modified)

Dr. Lee Admits Thinner Pads Increase Risk Of Short Circuit

Dr. Lee Deposition

Q. Does increasing the thickness of the pad help prevent damage to the pad during the manufacturing process?

A. Yes. Of course.

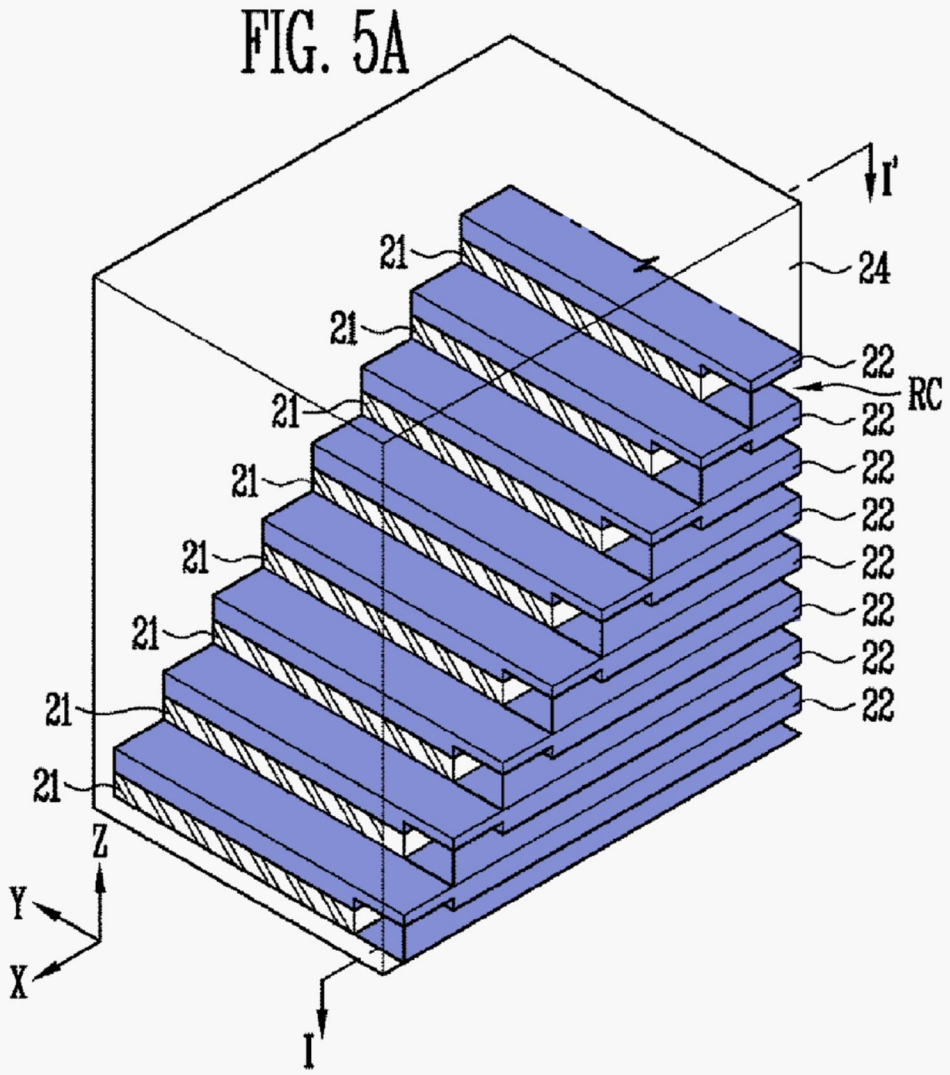
Q. Okay.

A. Because those pads are eventually used to form the conductive veer, meaning the vertical conduit. And if the pad is thin, that it can -- you know, first you do an oxide etch of the field oxide, and then you deposit the -- the content material, conductive material.

Those process, if the contact pad is thin, can easily damage the contact region and such that the -- you would have a potential shorting issues.

Ex. 2010 (Jack C. Lee, Ph. D.), 168:17-169:10

Petitioner's Theory Increases Risk Of Electrical Failure



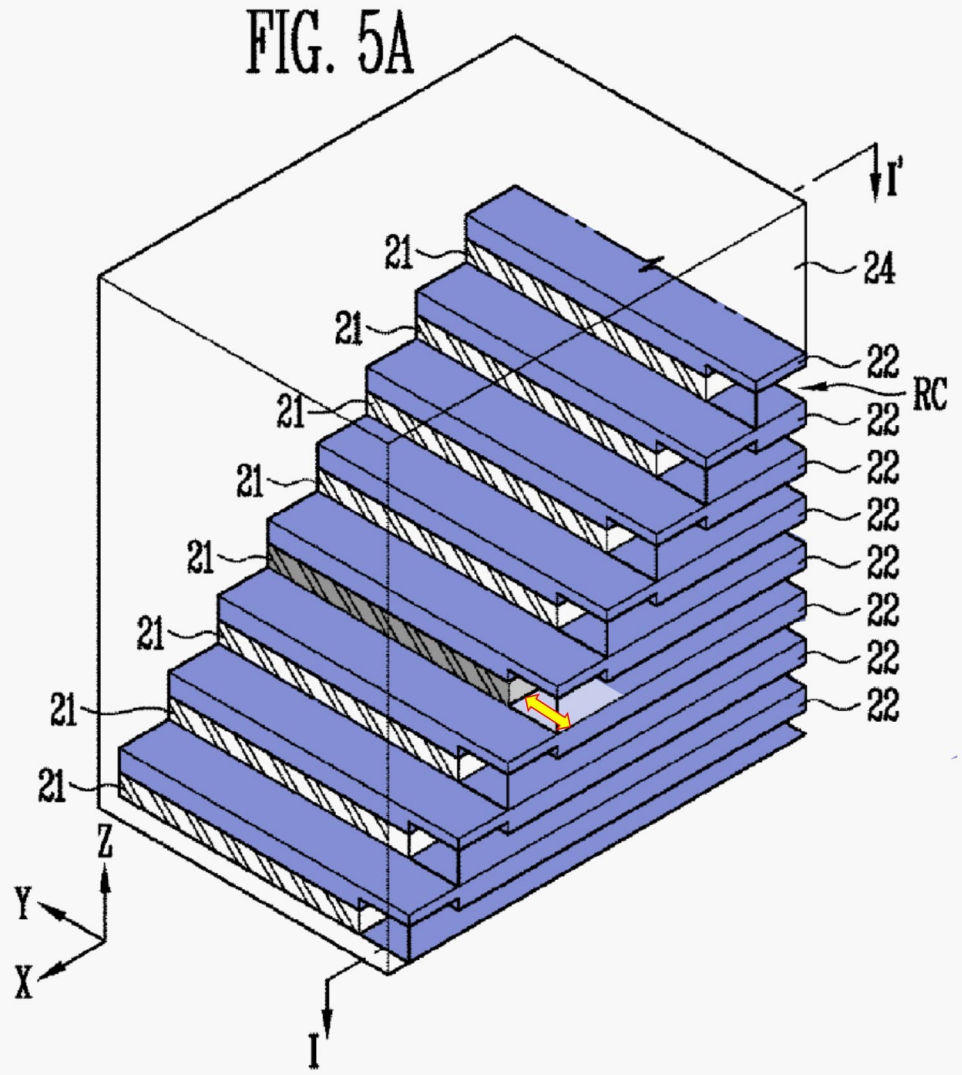
Ex. 1007 (Lee), Fig. 5A

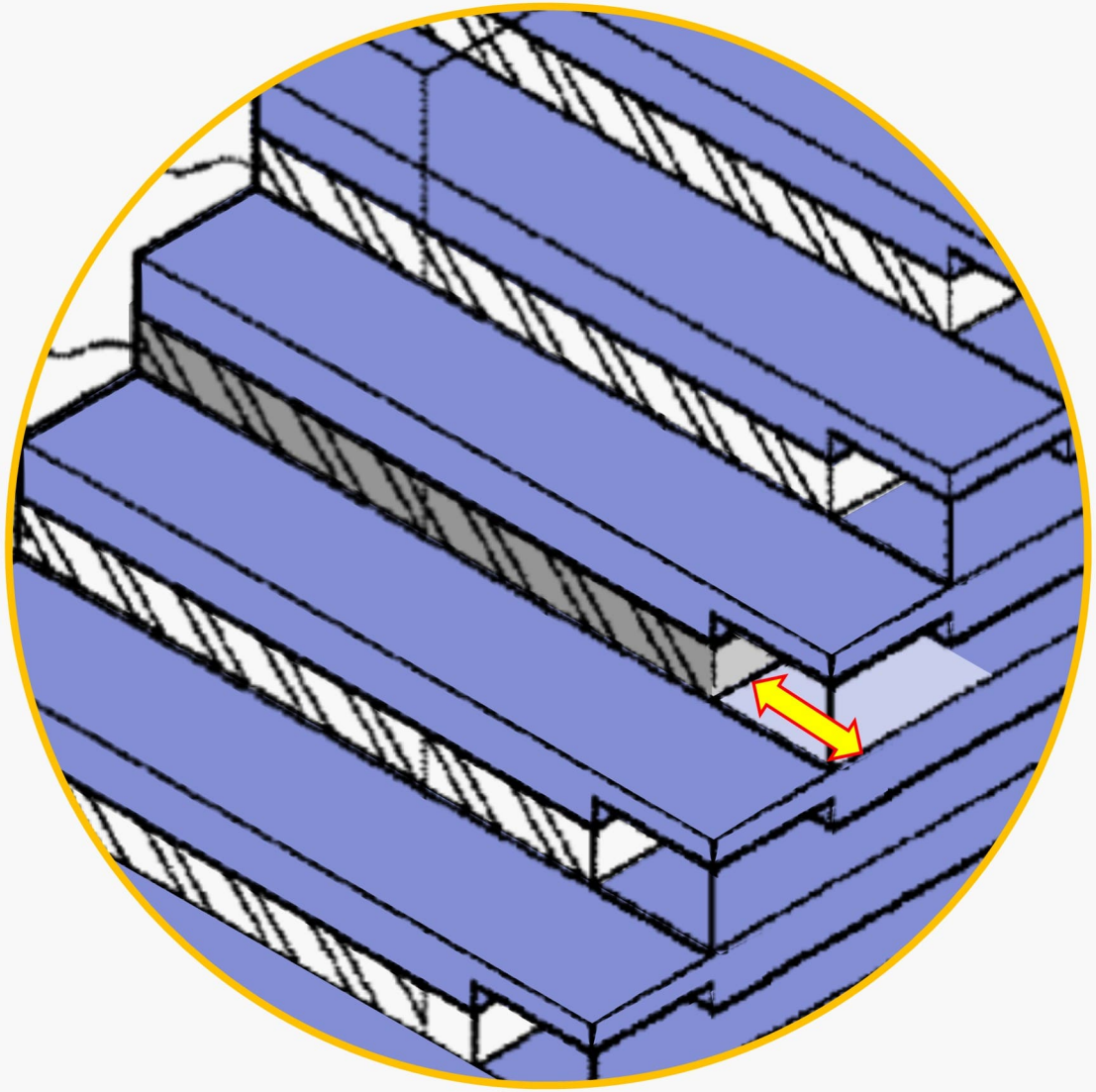
Lee

[0030] The first material layers **21** may be formed of materials having a high etch selectivity with respect to the second material layers **22**. For example, the first material layers **21** may include a conductive layer such as a polysilicon layer, and the second material layers **22** may include an insulating layer such as an oxide layer. In another example, the first material layers **21** may include a sacrificial layer such as a nitride layer, and the second material layers **22** may include an insulating layer such as an oxide layer.

Ex. 1007 (Lee) [0030]

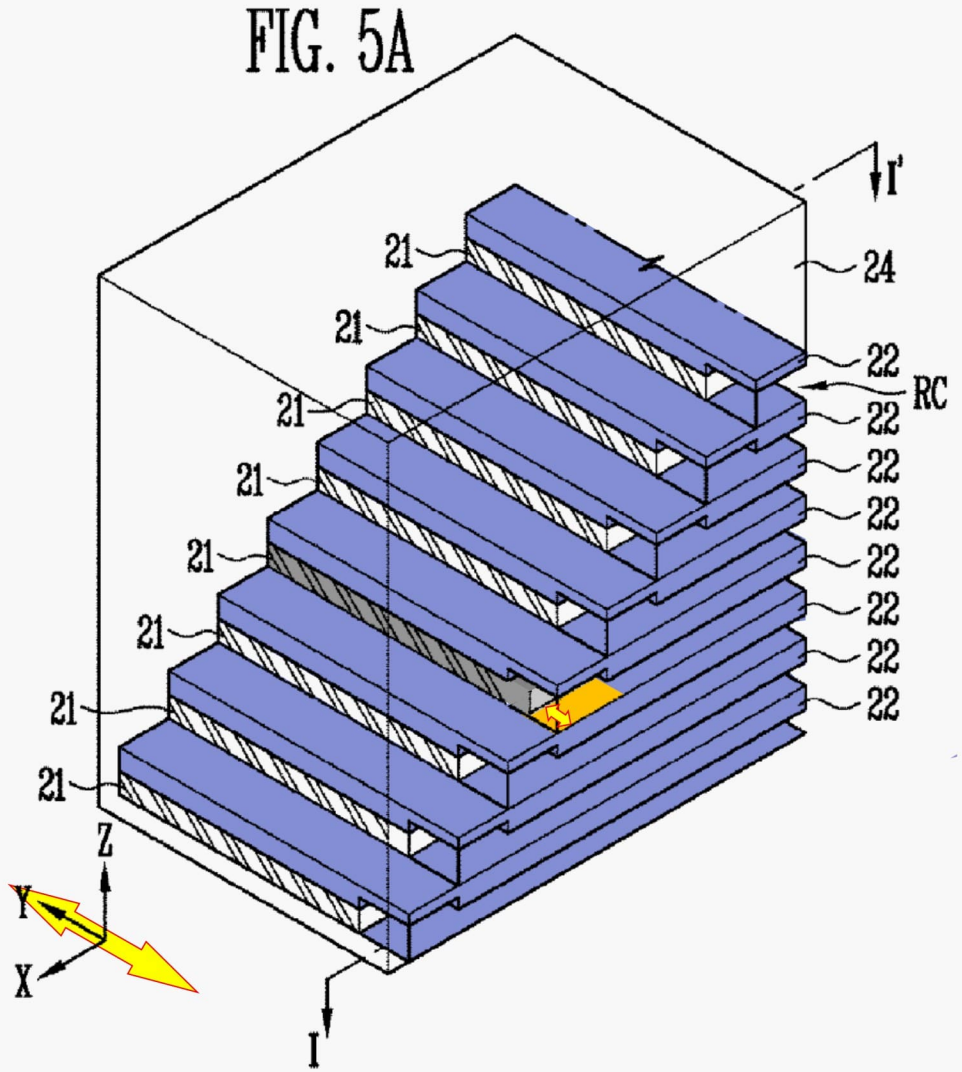
Petitioner's Theory Increases Risk Of Electrical Failure

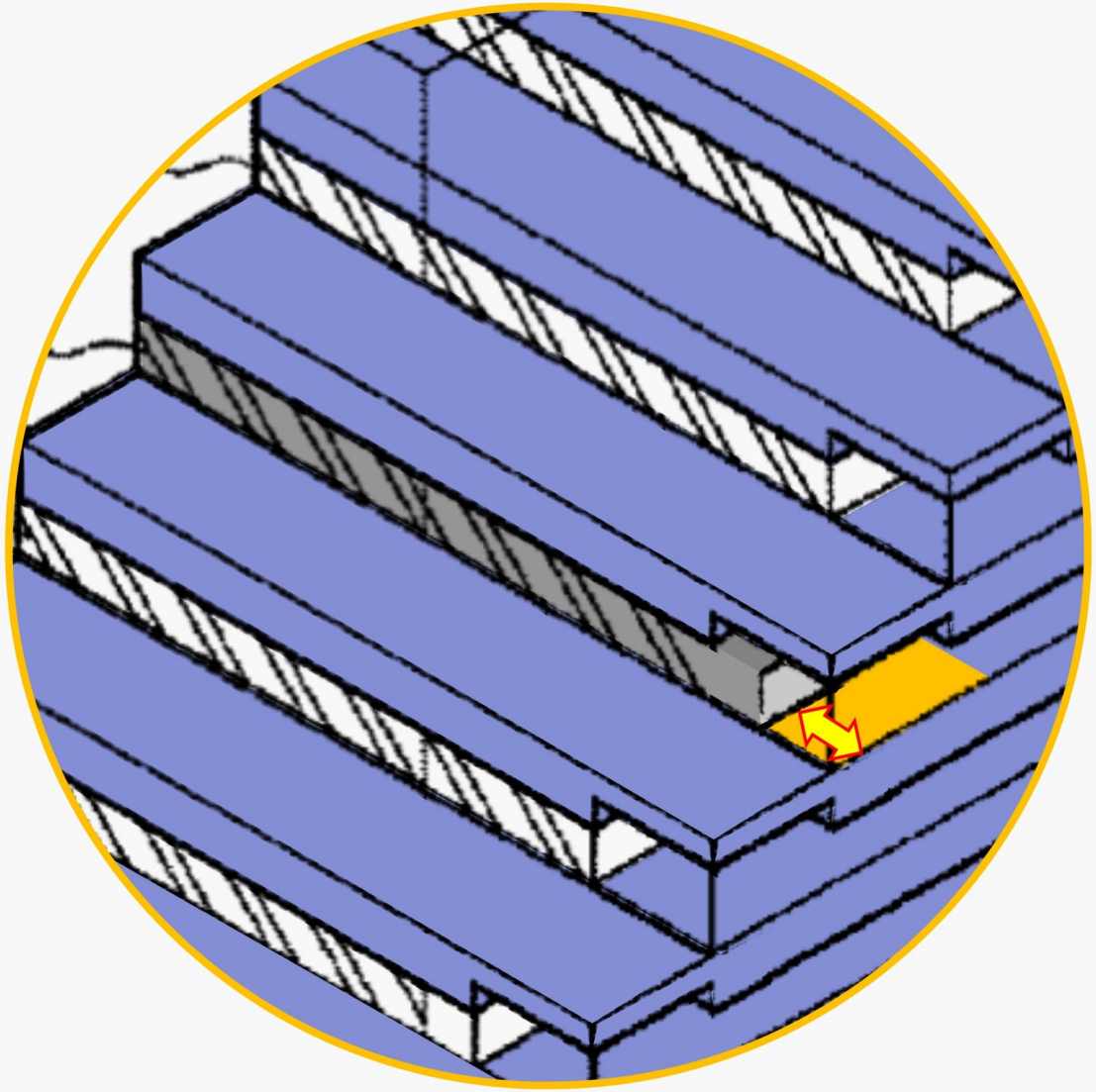




Ex. 1007 (Lee), Fig. 5A

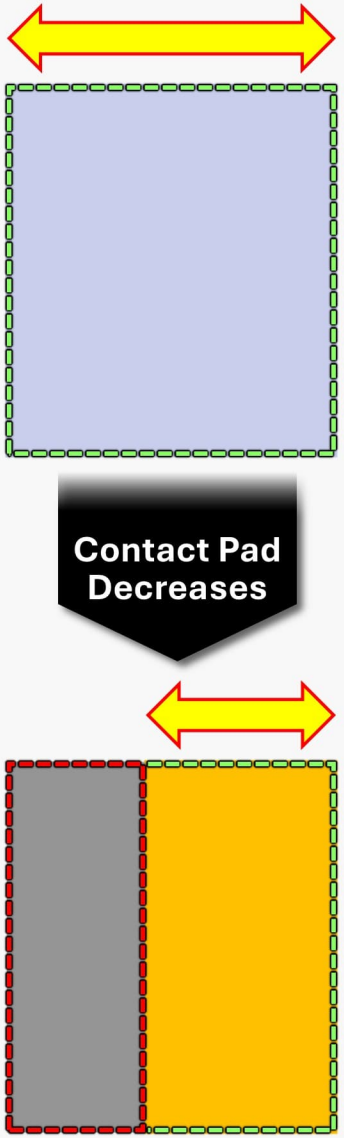
Petitioner's Theory Increases Risk Of Electrical Failure

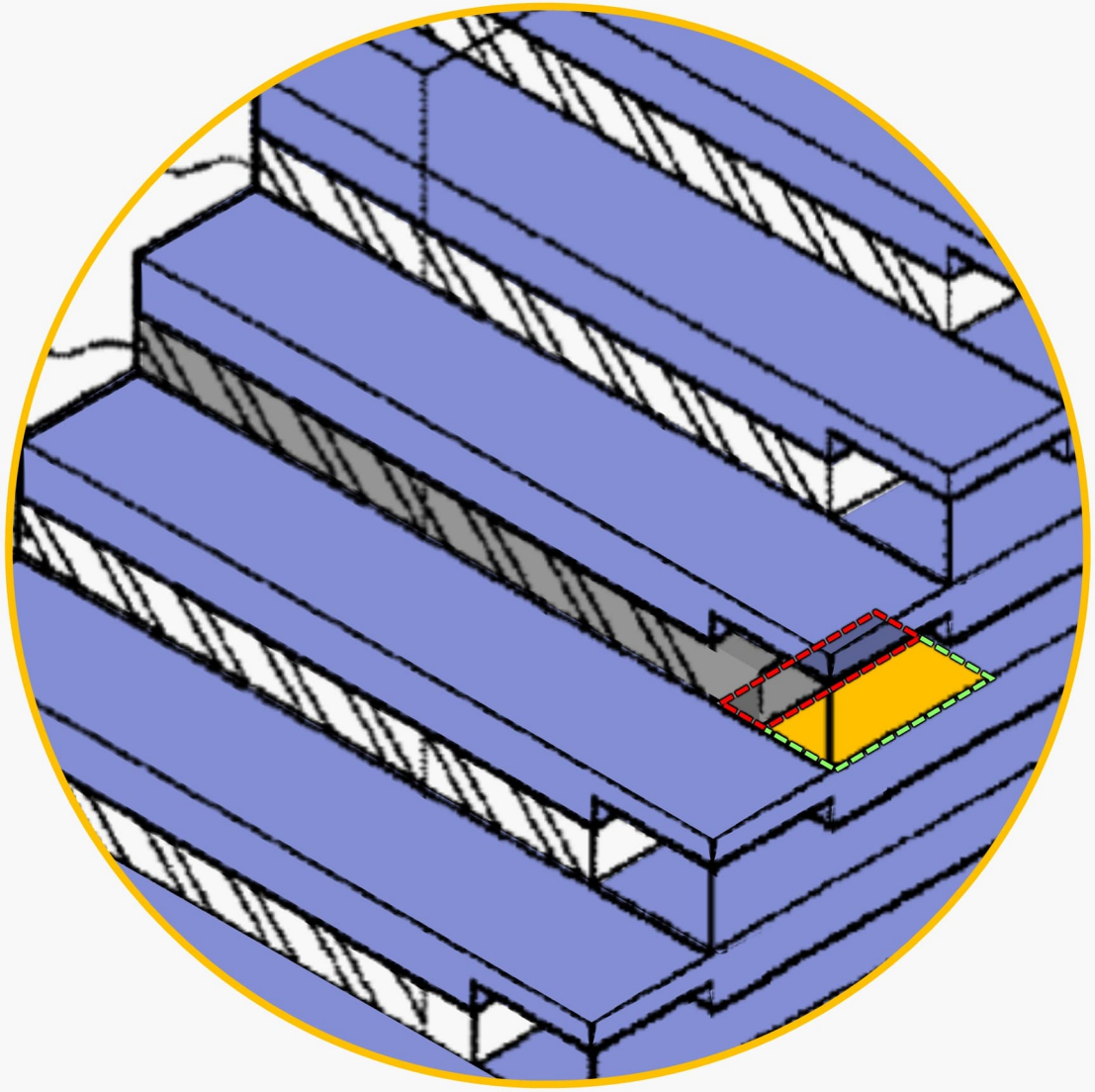




Ex. 1007 (Lee), Fig. 5A

Petitioner's Theory Increases Risk Of Electrical Failure



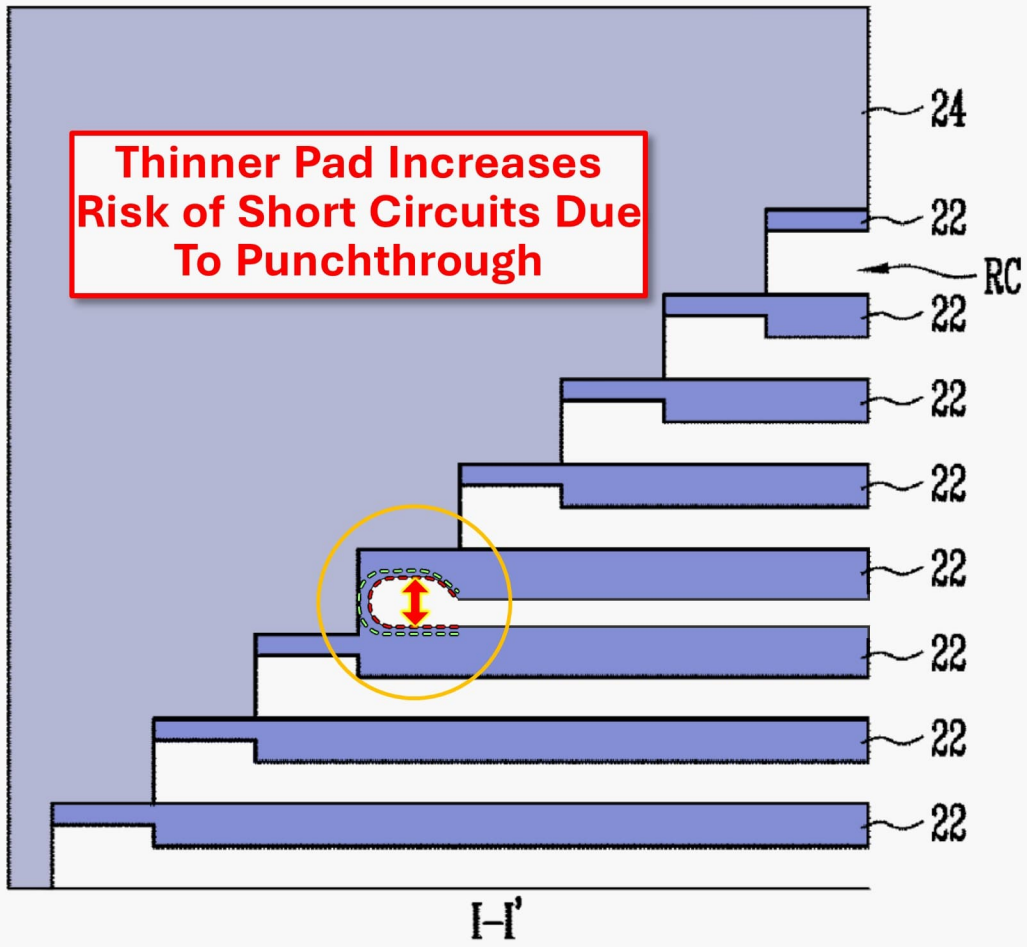


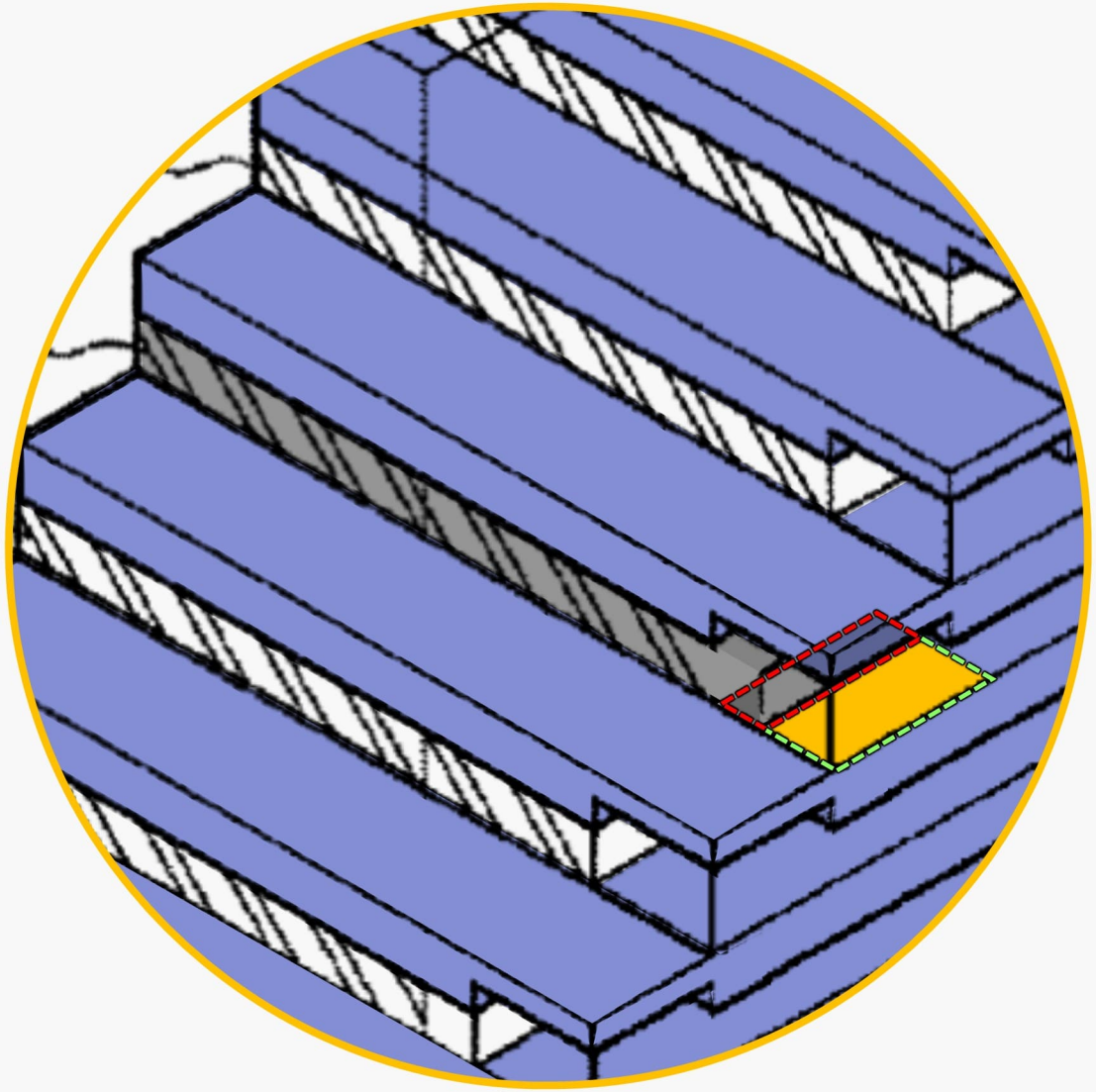
POSR 26-27 (citing Lee Fig. 5A)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Oxidizing Lee Would Increase, Not Decrease, Risk Of Electrical Failure

FIG. 5B





Oxidizing Lee Contradicts Lee's Purpose Of Reducing Short Circuits

Plas-Pak Indus. v. Sulzer Mixpac AG

"However, combinations that change the 'basic principles under which the [prior art] was designed to operate,' or that render the prior art "inoperable for its intended purpose," may fail to support a conclusion of obviousness.

Plas-Pak Indus. v. Sulzer Mixpac AG, 600 F. App'x 755, 758 (Fed. Cir. 2015) (internal citations omitted)

Ground 3 Fails For Four Reasons

1. Lee cannot be oxidized to form a "curved side surface"
2. A POSITA would not be motivated to oxidize Lee layer 22 because oxidation would increase risk of electrical failure
3. **A POSITA would not be motivated to add a "curved side surface" to Lee because it is redundant of Lee's protections**
4. Lee lacks an "insulating layer disposed over a first portion of a conductive layer"

Rounding Corners Is Redundant Of Lee's Electrical Failure Protections

Lee

the X direction during an etch process. Conventionally, the distance between the stacked conductive layers (pad portions) may decrease, and therefore a breakdown voltage of the conductive layers **25** may be deteriorated. However, according to an embodiment of the present invention, since an etch margin is ensured by the barrier layers **27** and **28**, a sufficient distance may be ensured between the stacked conductive layers (pad portions) to prevent any deterioration.

Ex. 1007 (Lee), [0049]

No Motivation To Add Redundant Features

Kinetic Concepts, Inc. v. Smith & Nephew, Inc.

"In addition, both of these references independently accomplish similar functions, namely, draining fluids. Because each device independently operates effectively, a person having ordinary skill in the art, who was merely seeking to create a better device to drain fluids from a wound, would have no reason to combine the features of both devices into a single device."

Kinetic Concepts, Inc. v. Smith & Nephew, Inc., 688 F.3d 1342, 1369 (Fed. Cir. 2012)

Ground 3 Fails For Four Reasons

1. Lee cannot be oxidized to form a "curved side surface"
2. A POSITA would not be motivated to oxidize Lee layer 22 because oxidation would increase risk of electrical failure
3. A POSITA would not be motivated to add a "curved side surface" to Lee because it is redundant of Lee's protections
4. **Lee lacks an "insulating layer disposed over a first portion of a conductive layer"**

Ground 3 Fails To Show Insulating Layer Over Only A First Portion Of Conductive Layer

17. A memory device, comprising:

a substrate, wherein the substrate comprises a top surface;

a memory string disposed over the substrate; and

a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:

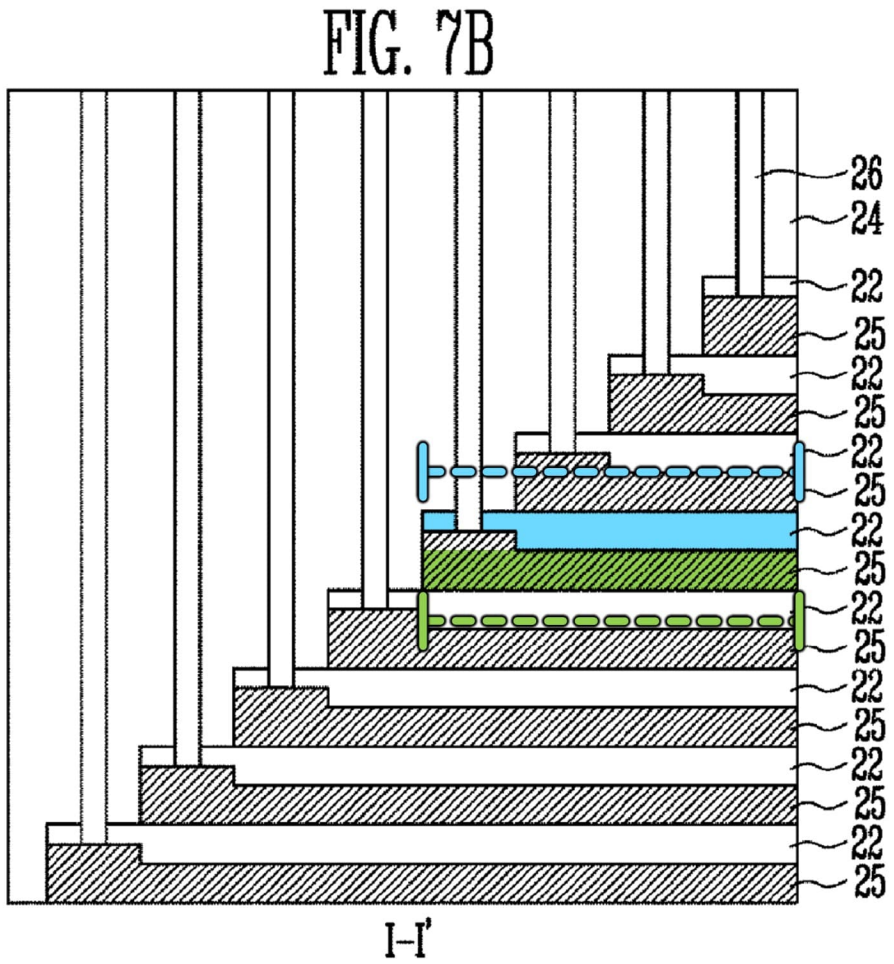
a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.

Ex. 1001 ('666 Patent), Claim 17

19. The memory device of claim **17**, wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack.

Ex. 1001 ('666 Patent), Claim 19

Petition



Reading Out "portion" Is Highly Disfavored

Intel Corp. v. Qualcomm Inc.

"It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous."

Intel Corp. v. Qualcomm Inc., 21 F.4th 801, 810 (Fed. Cir. 2021) (internal citations omitted)

Ground 3 Fails For Four Reasons

1. Lee cannot be oxidized to form a "curved side surface"
2. A POSITA would not be motivated to oxidize Lee layer 22 because oxidation would increase risk of electrical failure
3. A POSITA would not be motivated to add a "curved side surface" to Lee because it is redundant of Lee's protections
4. Lee lacks an "insulating layer disposed over a first portion of a conductive layer"