

MICRON TECHNOLOGY, INC.
Petitioner
v.
YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.
Patent Owner

Case No. IPR2025-00189
U.S. Patent No. 11,145,666

Micron's Hearing Demonstratives

March 12, 2026

Overview of the '666 Patent

Embodiments of the present disclosure are directed to a staircase structure for a memory device (e.g., 3D memory device). The disclosed embodiments provide numerous benefits including, but not limiting to, yield and manufacturing cost improvements.

*Ex. 1001 ('666 Patent), 1:37-41;
See also Paper 1 (Petition), 18.*

Claim 19 of the '666 Patent

17. A memory device, comprising:

a substrate, wherein the substrate comprises a top surface;

a memory string disposed over the substrate; and

a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:

a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.

19. The memory device of claim 17, wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack.

Ex. 1001 ('666 Patent), Claims 17, 19

The '666 Patent's Example Staircase Structure

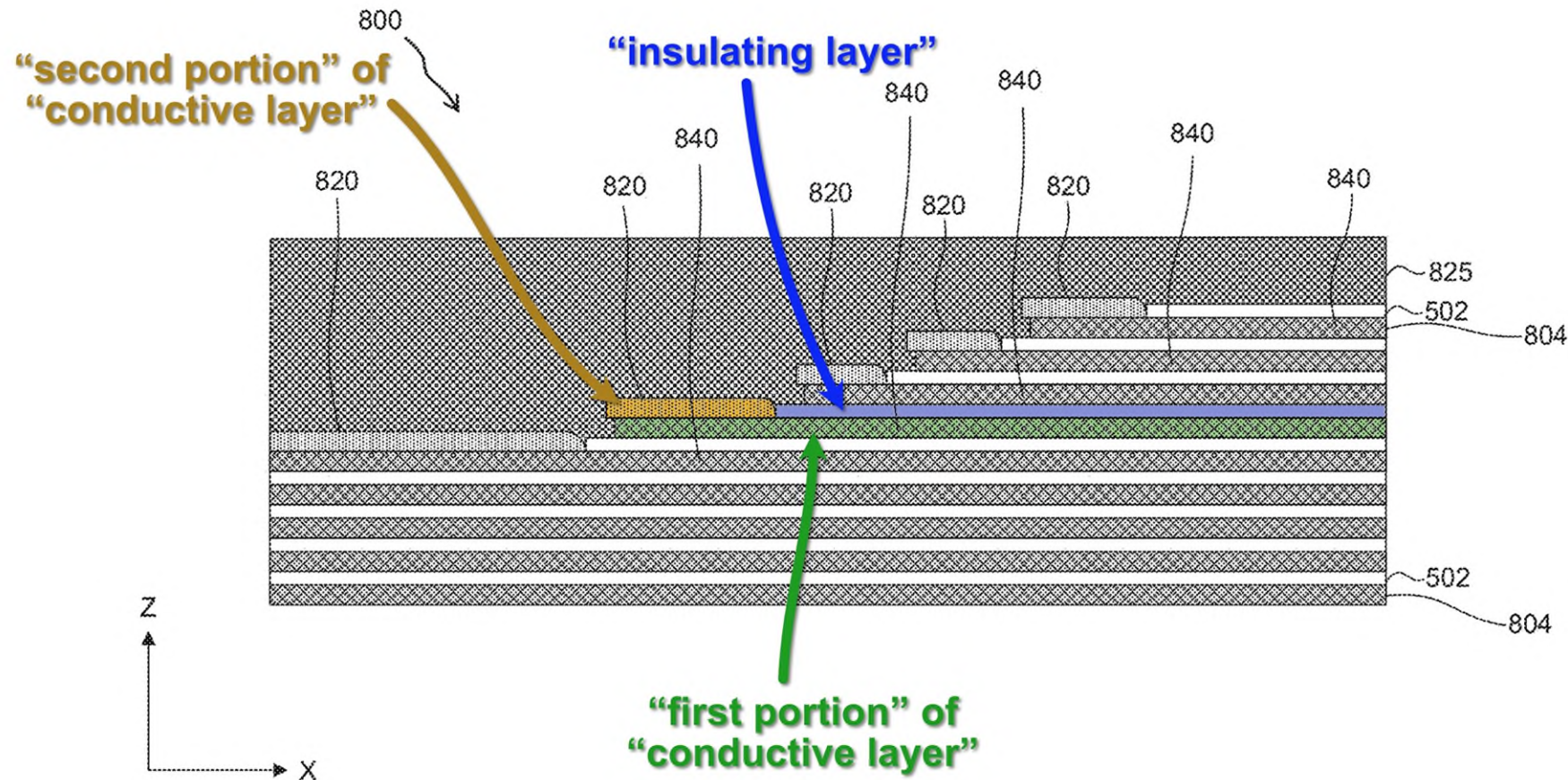


FIG. 8

*Ex. 1001 ('666 Patent), Fig. 8;
see also Paper 1 (Petition), 19.*

THE PETITION'S GROUNDS

Instituted Grounds

Ground	Prior Art	Original Claims at Issue
1	Kim	Claims 17, 19, 20 obvious
2	Nam	Claims 17, 19, 20 obvious
3	Lee + Park	Claims 17, 19, 20 obvious

Paper 1 (Petition), 10-11.

Overview of Kim

Embodiments of the inventive concepts may provide semiconductor memory devices having enhanced reliability.

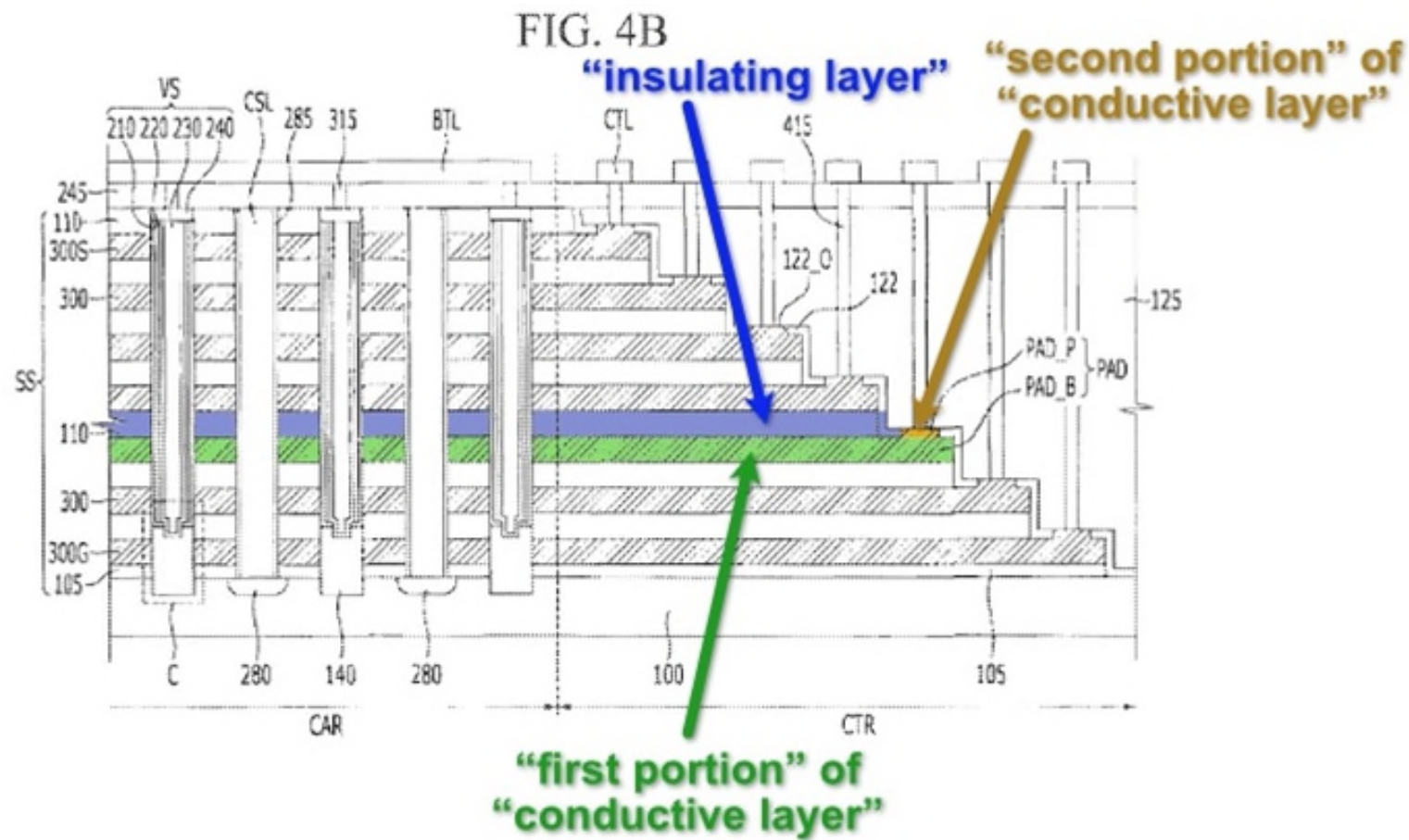
According to some embodiments of the inventive concepts, semiconductor memory devices are provided. A semiconductor memory device may include a substrate including a cell array region and a contact region and a stacking structure including a plurality of insulating layers and a plurality of gate electrodes alternately stacked on the substrate. The stacking structure may include a stepwise structure in the contact region. Ones of the plurality of gate

An end of the gate electrode 300 exposed through the stepwise structure may be a pad unit PAD. One or more of the plurality of pad units PAD may include a base pad PAD_B and a protrusion pad PAD_P contacting a surface of the base pad PAD_B.

Embodiments of the inventive concepts in which the protrusion pad PAD_P has a rectangular parallele shape is illustrated, but the protrusion pad PAD_P is not limited thereto and, in some embodiments, may have a shape including a curved surface based on a virtual rectangular parallele shape, a cylindrical shape, or any shape.

*Ex. 1005 (Kim), 1:38-47, 7:58-62, 8:29-34;
see also Paper 1 (Petition), 25-27.*

Overview of Kim



Ex. 1005 (Kim), Fig. 4B;
see also Paper 1 (Petition), 26, 43.

Overview of Nam

[0002] The inventive concepts relate to a memory device.

of a gate structure. However, in a case in which the thickness of each of the gate electrode layers is reduced, at least a portion of the contacts 180 may penetrate through the gate electrode layer to be connected to other gate electrode layers, which may cause the occurrence of defects such as short circuits.

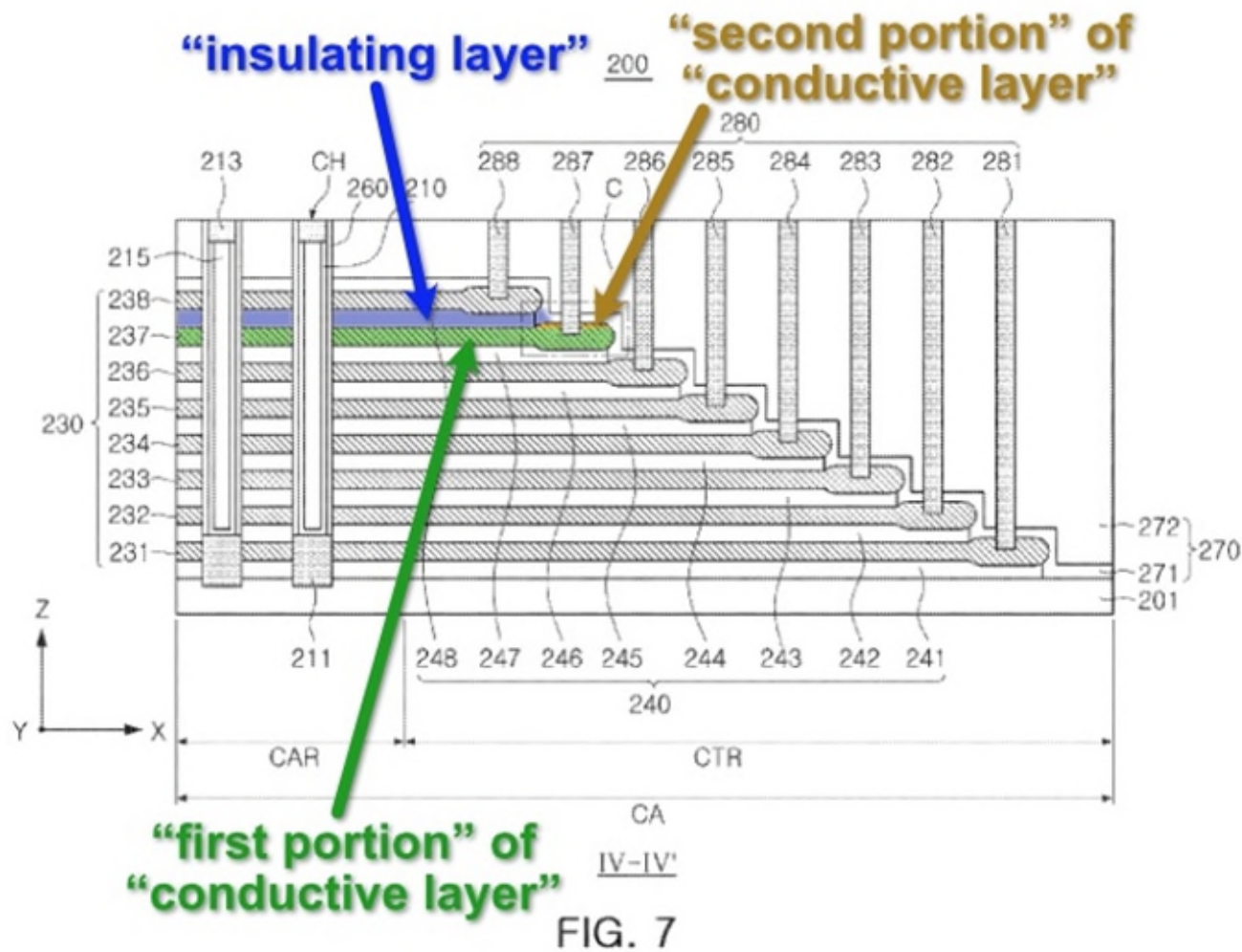
[0045] In an example embodiment of the inventive concepts, as a thickness of each of the gate electrode layers may be increased only in a pad region in which the contacts 180 are connected to the gate electrode layers, the problem described as above may be mitigated or solved. A descrip-

[0005] In one embodiment, the semiconductor device includes a stack of alternating first interlayer insulating layers and gate electrode layers on a substrate. At least one of the gate electrode layers has a first portion and a second portion. The second portion forms an end portion of the at least one gate electrode layer, and a bottom surface of the second portion is at a lower level than a bottom surface of the first portion. A contact plug extends from the second portion.

[0066] In the example embodiment illustrated in FIG. 8A, the second region 237B may have a lateral surface SS2 protruding outwardly therefrom in the first direction (X-axis direction). For example, the lateral surfaces SS2 may be convex or have a bull nose shape. As interfaces at middle

*Ex. 1006 (Nam), ¶¶ [0002], [0005], [0044]-[0045], [0066];
see also Paper 1 (Petition), 19-20.*

Overview of Nam



Ex. 1006 (Nam), Fig. 7;
see also Paper 1 (Petition), 28-29, 63.

Overview of Lee

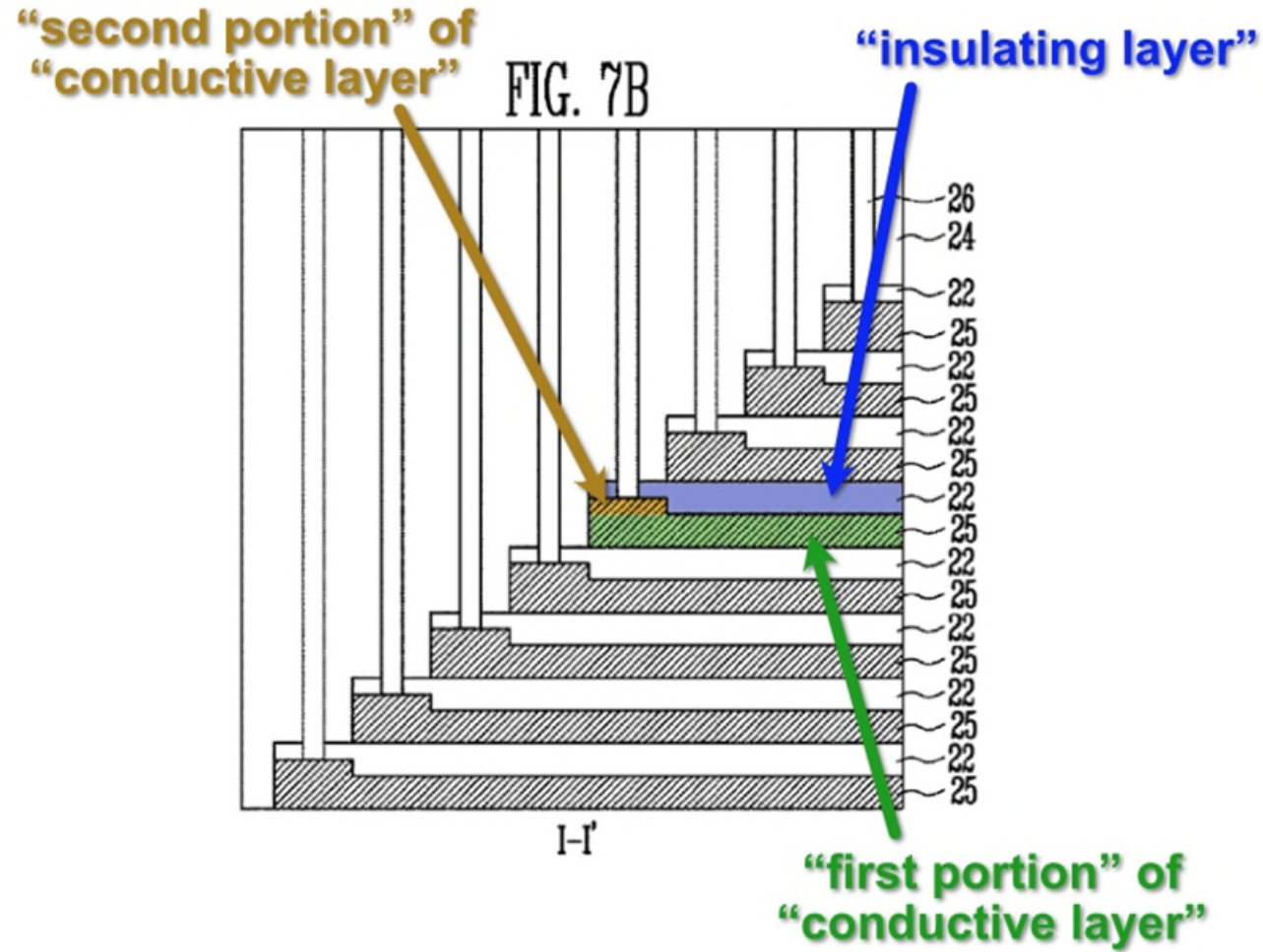
[0005] A non-volatile memory retains data stored therein even when not powered. Two-dimensional memory devices in which memory cells are fabricated in a single layer over a silicon substrate have reached physical limits and may no longer have increased degrees of integration. Accordingly, three-dimensional (3D) non-volatile memory devices in which memory cells are stacked in a vertical direction over a silicon substrate have been proposed.

[0021] An end of the stacked structure ST may be patterned stepwise. Each step of the stacked structure ST that is patterned stepwise may include at least one conductive layer 11 or 13 and at least one insulating layer 12 or 14. As illustrated in FIG. 1A, the insulating layer 12 or 14 may be located on a top surface of each step. Alternatively, as illustrated in FIG. 1B, the conductive layer 11 or 13 may be located on the top surface of each step.

[0023] The pad structure PS may include first conductive layers 11 and first insulating layers 12 that are alternately formed in the contact region CONTACT of the substrate. An end of the pad structure PS may be patterned stepwise. Portions of the first conductive layers 11 that are exposed along the stepped end of the pad structure PS may be defined as pad portions PAD. The pad portions PAD may have a greater thickness than unexposed portions of the first conductive layer 11.

*Ex. 1007 (Lee), ¶¶ [0005], [0021], [0023];
see also Paper 1 (Petition), 29-30.*

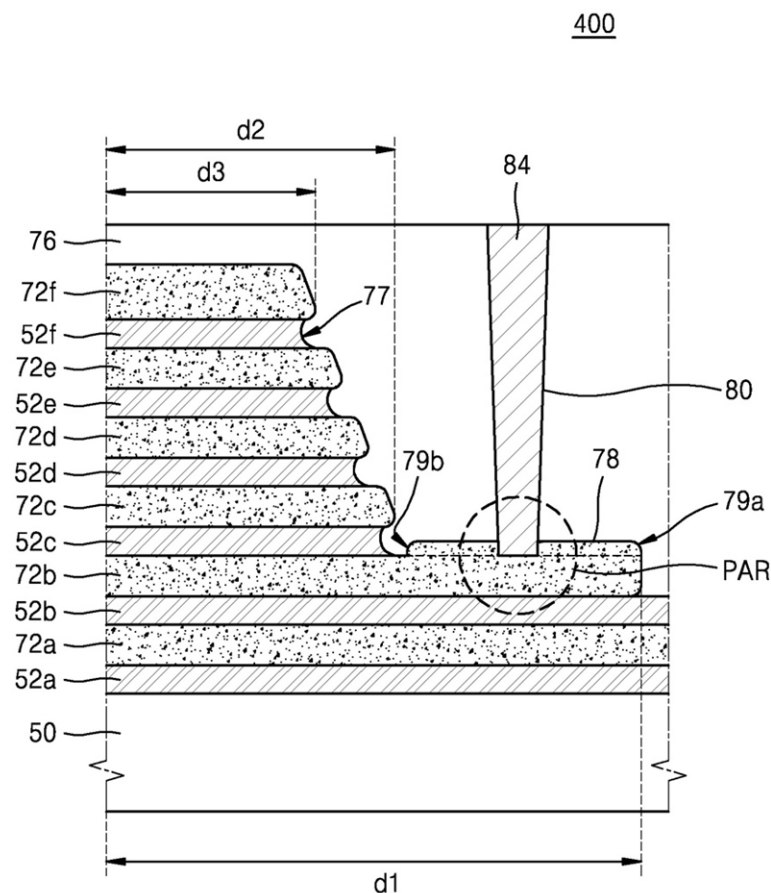
Overview of Lee



*Ex. 1007 (Lee), Fig. 7B;
see also Paper 1 (Petition), 31, 78.*

Overview of Park

FIG. 7



The inventive concept relates to a semiconductor device, and more particularly, to a vertical semiconductor device.

A vertical semiconductor device, in which memory cells are stacked in a direction perpendicular to a surface of a substrate, may include a connection wiring that is formed by

portion. The pad region PAR may include a raised pad portion 78 protruding from a surface of the conductive layer pattern 72b. The raised pad portion 78 may prevent a short circuit between the raised pad portion 78 and the conductive layer pattern 72c because the other end 79b of the raised pad portion 78 is rounded adjacent to the conductive layer pattern 72c.

*Ex. 1008 (Park), 1:14-16, 11:35-41, Fig. 7;
see also Paper 1 (Petition), 32.*

THE PARTIES' REMAINING DISPUTES

Overview of Remaining Disputes

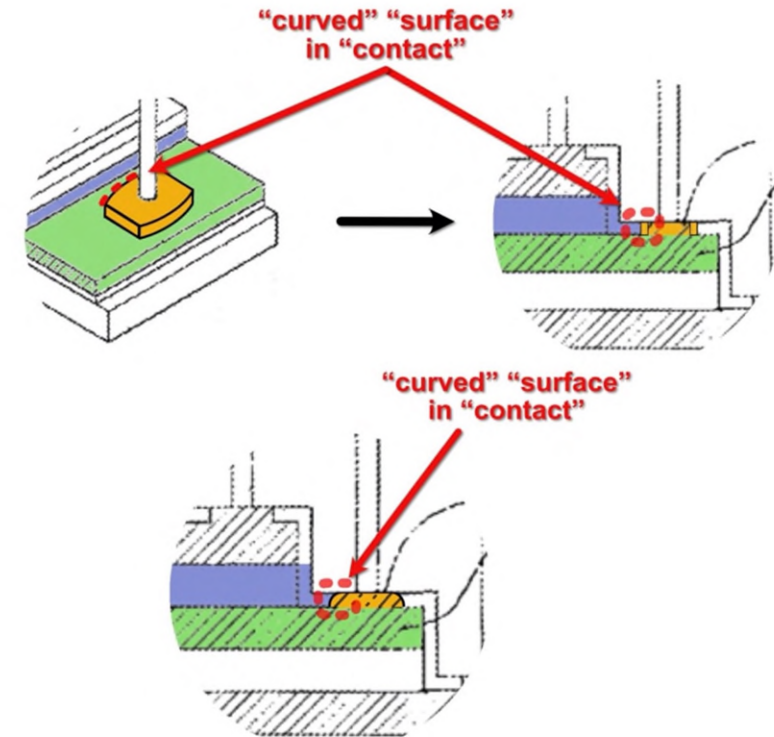
- **Do Kim's generally cylindrical landing pads include a "curved side surface"?**
- **Even if Patent Owner's narrow claim construction is accepted, is claim 19 still unpatentable because Kim also renders obvious landing pads that are "curved" when viewed from the side?**
- **Is the "curved side surface" of Nam's landing pad "in contact with a side surface of the insulating layer"?**
- **Would it have been obvious to apply Park's landing pad with a "curved side surface" to Lee?**

**KIM’S CYLINDRICAL LANDING PADS INCLUDE A “CURVED
SIDE SURFACE”**

A POSITA Would Have Understood Kim to Teach Two Different Types of “Curved” Landing Pads

Embodiments of the inventive concepts in which the protrusion pad PAD_P has a rectangular parallele shape is illustrated, but the protrusion pad PAD_P is not limited thereto and, in some embodiments, may have a shape including a curved surface based on a virtual rectangular parallele shape, a cylindrical shape, or any shape.

Generally cylindrical pad:



Pad curved in cross section:

*Ex. 1005 (Kim), 1:38-47, 8:29-34;
see also Paper 1 (Petition), 45-53.*

Patent Owner's Argument Regarding Kim's Cylindrical Landing Pads Is Premised Exclusively on an Erroneous Claim Construction

Patent Owner's Position:

To distinguish Kim, Patent Owner argues that a landing pad's "curved side surface" must be curved in the "vertical" "z-axis" direction to fall within the claim scope. It also argues that the "side surface" of the insulating layer contacted by this "curved side surface" must be the insulating layer's end, and not an "inner" or "internal" surface.

E.g., Paper 25 (Response), 1, 35, 38-39.

Patent Owner Is Incorrect:

- The claim includes **none** of the limitations read in by Patent Owner: it broadly embraces a variety of "curved side surface[s]."
- The claims also **do not exclude** "inner" surfaces from the scope of "side surface."
- The specification repeatedly explains that it is **not limited** to the depicted embodiment.
- The language used in the specification confirms that the applicant could have—but **chose not to**—limit the claims in the way Patent Owner now proposes.

Paper 29 (Reply), 3-10.

The Claims Require Only a Landing Pad with “a Curved Side Surface” in “Contact” with “a Side Surface” of the “Insulating Layer”

17. A memory device, comprising:
a substrate, wherein the substrate comprises a top surface;
a memory string disposed over the substrate; and
a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:
a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.

*Ex. 1001 ('666 Patent), Claim 17;
see also Paper 29 (Reply), 3-5.*

The Claims Require Only a Landing Pad with “a Curved Side Surface” in “Contact” with “a Side Surface” of the “Insulating Layer”

“The words of a claim are generally given their ordinary and customary meaning...”

*Johnson Worldwide Assocs., Inc. v. Zebco Corp.,
175 F.3d 985, 989 (Fed. Cir. 1999)*

“[M]odifiers will not be added to broad terms standing alone[.]”

*Thorner v. Sony Comput. Entm’t Am., LLC,
669 F.3d 1362, 1365 (Fed. Cir. 2012)*

see also Paper 29 (Reply), 3

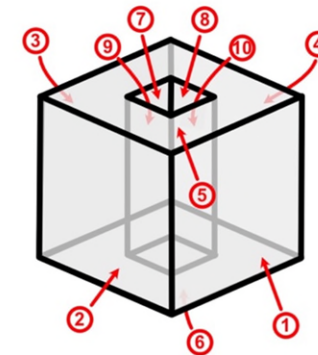
Patent Owner Does Not Dispute that “Side Surface” Has a Straightforward Plain and Ordinary Meaning

9. As I explained in my opening declaration, the '666 patent's claim terms do not require further construction and can instead be afforded their plain and ordinary meaning. *See* Ex. 1003, ¶ 97.

10. This includes the term “side surface.” The term is readily understandable, and would be understood to refer to any of the bounding surfaces of a three-dimensional structure.

11. I repeatedly explained this to Patent Owner's counsel during my prior deposition, noting that “three-dimensional structure[s]”—like the '666 patent's conductive and insulating layers—include “many sides.” Ex. 1017, 71:3-72:14, 79:18-80:16, 101:17-102:10. Every one of these many sides is a “side surface.” This includes the top, bottom, front, back, lateral sides, any interior sides, and so on.

12. For instance, the example three-dimensional shape shown below has a total of 10 side surfaces (the top, bottom, four lateral surfaces, and the four surfaces bounding the hole through the shape's middle):



*Ex. 1027 (Lee Reply), ¶¶ 9-12
see also Paper 29 (Reply), 4*

The '666 Patent's Specification Repeatedly Explains that the Claims Are Not to be Limited to Just the Depicted Embodiment

The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the disclosure and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the disclosure and guidance.

Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

The Summary and Abstract sections can set forth one or more but not all exemplary embodiments of the present disclosure and thus are not intended to limit the present disclosure and the appended claims.

The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

*Ex. 1001 ('666 Patent), 13:10-40;
see also Paper 29 (Reply), 8.*

The Specification Characterizes Both the Top and Bottom of a Layer as “Side[s]” and Defines the term “Layer” Broadly

As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer has a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate. A layer can extend over the entirety of an underlying or overlying structure, or can have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or

*Ex. 1001 ('666 Patent), 4:36-53;
see also Paper 29 (Reply), 7*

The Specification Uses the Narrowing Language Patent Owner Improperly Attempts to Read Into the CLaims

A patent's claims are not limited where “the specification ... suggests that the patentees knew how to” use narrowing language but instead “chose a different term that implies a broader scope[.]”

Acumed LLC v. Stryker Corp., 483 F.3d 800, 807 (Fed. Cir. 2007)

direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

formation of structures over it). A vertical direction can refer to a direction (e.g., the z-axis) perpendicular to the top surface of the structure.

*Ex. 1001 ('666 Patent), 5:11-13, 5:56-58;
see also Paper 29 (Reply), 6*

**KIM ALSO RENDERS OBVIOUS LANDING PADS THAT ARE
“CURVED” WHEN VIEWED FROM THE SIDE:
THE CLAIMS ARE UNPATENTABLE EVEN IF PATENT
OWNER’S CONSTRUCTION IS ACCPETED**

Patent Owner's Arguments Regarding Kim's Other "Curved" Landing Pads Are Inconsistent with the Teachings of the Prior Art

Patent Owner's Position:

Patent Owner argues that Kim cannot employ a landing pad that is "curved" when viewed from the side. It also argues that a POSITA would not have been motivated to employ such a pad.

Paper 25 (Response), 30, 39.

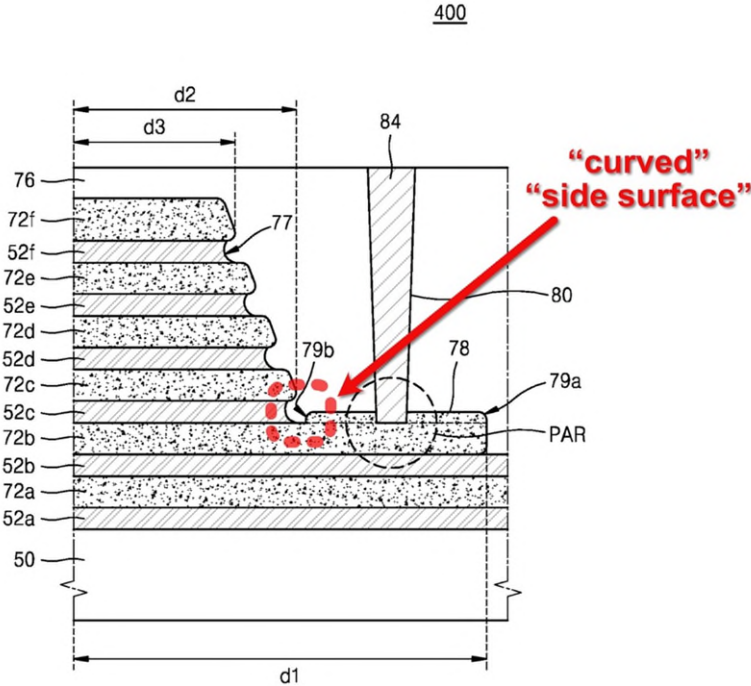
Patent Owner Is Incorrect:

- The prior art includes numerous examples of "curved" landing pads, showing that this type of pad was **both known and readily achievable**.
- Both Park's and Nam's methods are **directly applicable** to Kim and would have successfully produced a "curved" landing pad
- A POSITA would have recognized that a "curved" landing pad **further**s Kim's goals.

Paper 29 (Reply), 13-19.

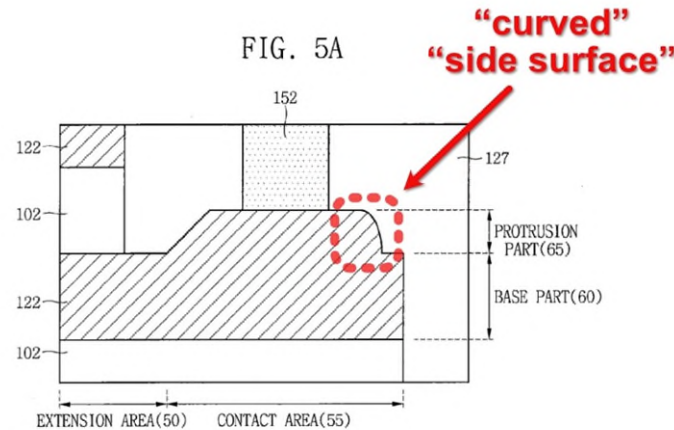
“Curved” Landing Pads Were Known, Considered Suitable For Use, and Were Routinely Employed in 3D Memory Staircases

FIG. 7



Ex. 1008 (Park), Fig. 7.

FIG. 5A



Ex. 1018 (Yun), Fig. 5A.

“curved”
“side surface”

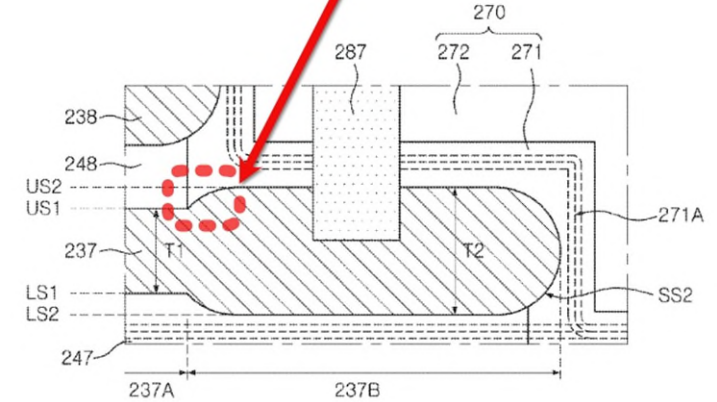


FIG. 8A

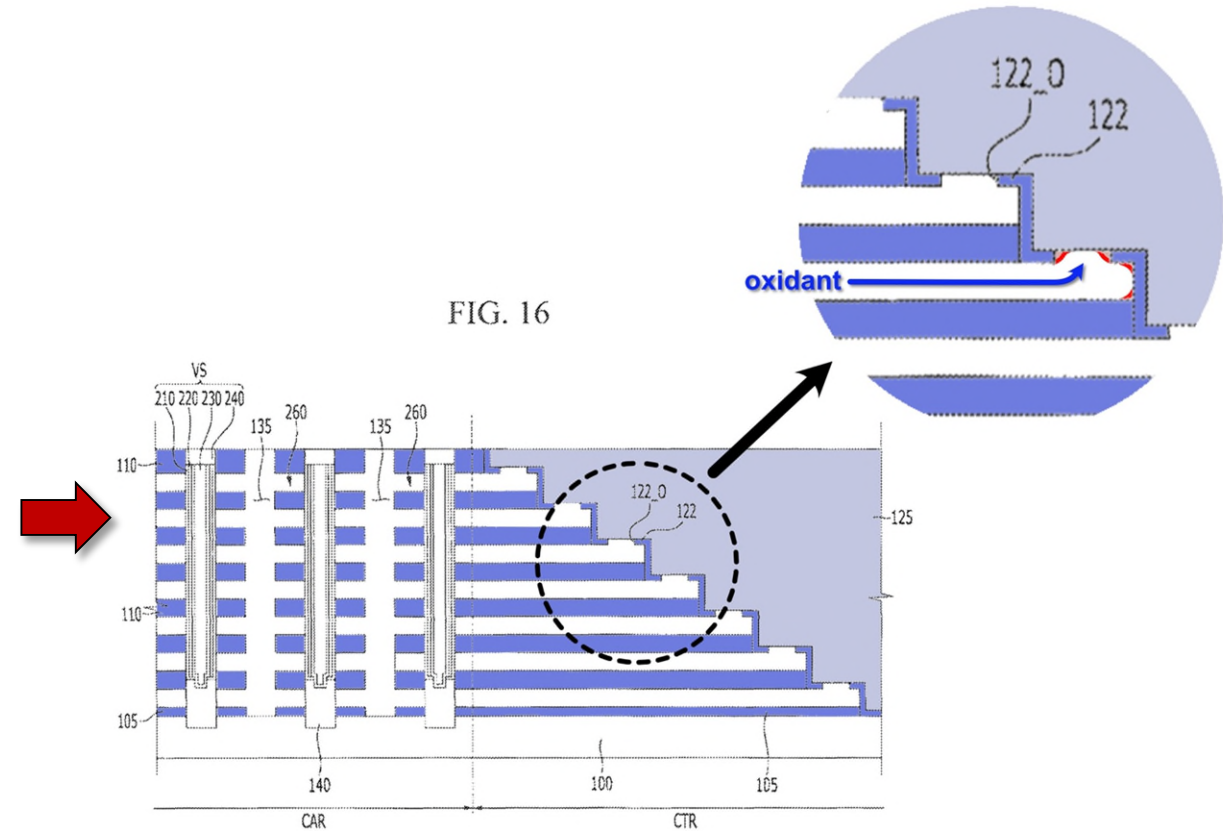
Ex. 1006 (Nam), Fig. 8A.

see also Paper 1 (Petition), 46-49.

A POSITA Would Have Recognized that Park's Two Step Oxide Forming Process Would Also Produce a Rounded Landing Pad in Kim

externally exposed. The additional insulating layer 40 may be formed by thermally oxidizing the surfaces and the side surfaces of the sacrificial layer patterns 14a through 14f. The additional insulating layer 40 may be formed on the surfaces and side surfaces of the sacrificial layer patterns 14a through 14f not covered by the interlayer insulating layer patterns 12b through 12f. One end of the additional insulating layer 40 may be rounded by an oxidation process. When one end of the additional insulating layer 40 is rounded, one end of each of conductive layer patterns in a subsequent process may be rounded to prevent a short circuit between the conductive layer patterns.

Ex. 1008 (Park), 8:31-42.



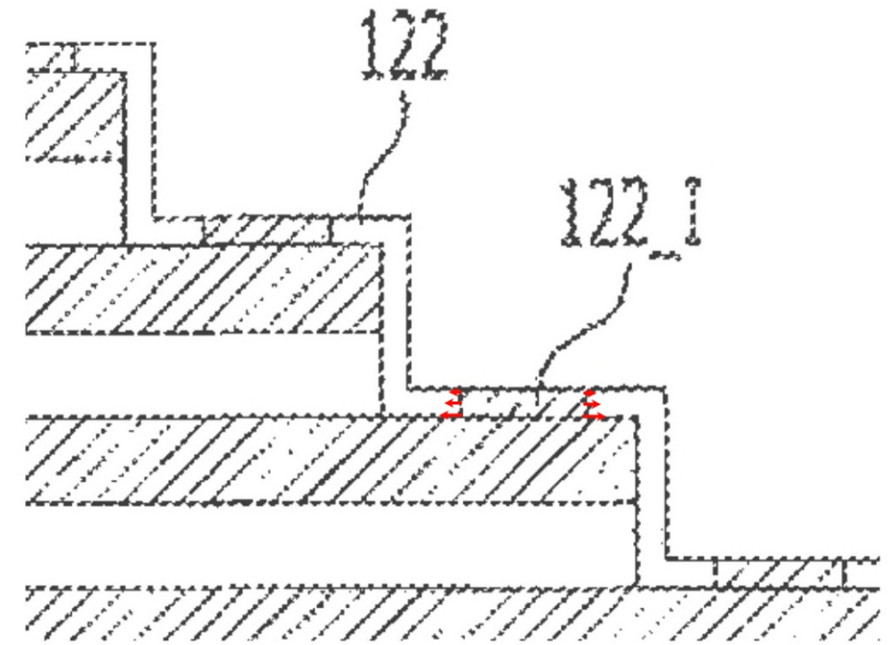
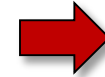
Ex. 1005 (Kim), Fig. 16; Ex. 1027 (Lee Reply), ¶¶ 46-48.

*see also Paper 29 (Reply), 15;
Paper 1 (Petition), 50-51.*

A POSITA Would Have Recognized that Nam's Heating Step Would Also Produce a Rounded Pad in Kim

[0060] In order to form the second region 137B having a thickness greater than that of the first region 137A, upper and lower surfaces of sacrificial layers and respective inter-layer insulating layers may be doped with an impurity in the manufacturing process. The impurity doped on the upper and lower surfaces of the sacrificial layers and respective interlayer insulating layers may be spread due to heat applied thereto in a subsequent process. Thus, a doped region 171A in which the impurity partially remains may be formed inside of a first interlayer insulating layers 171 as illustrated in FIG. 6. The doped region 171A may be located on upper surfaces, lower surfaces, and/or lateral surfaces of the gate electrode layers 130.

Ex. 1006 (Nam), ¶ [0060].



Ex. 1005 (Kim), Fig. 13; Ex. 1027 (Lee Reply), ¶¶ 50-52.

*see also Paper 29 (Reply), 15;
Paper 1 (Petition), 50-51.*

A Landing Pad With a “Curved Side Surface” Furthers Kim’s Goals Using the Same Methods Kim Already Employs

62. A POSITA would have recognized that rounded landing pad (with curved side surfaces) operates to increase the distance between the landing pad and adjacent conductive structure.

63. A rounded landing also—because it is further away—increases the thickness of insulation surrounding the landing pad.

64. In other words, a POSITA would have recognized that a rounded landing pad not only furthers Kim’s goal to avoid short circuits, but does so in a way that is both consistent with Kim and amounts to nothing more than an extension of the short-circuit preventing approaches Kim already employs. This is why a POSITA would have been motivated to employ a rounded pad with Kim: it assists in solving a problem Kim identifies (potential short circuits) and does so in a way Kim itself identifies as a potential solution (increasing distance and insulation between conductive structures). Even if Dr. Giapis’s narrow view were adopted and

Ex. 1027 (Lee Reply), ¶¶ 62-64.

positioned at the $n+1$ -th row based on the substrate 100. A z-direction thickness of the insulating layer 110 may be larger than the minimum distance in the z-direction between two adjacent pad units PAD to effectively prevent a short-circuit between the two adjacent pad units PAD.

Further, the semiconductor memory device may include the protrusion pad PAD_P inside from the edge of a surface of the base pad PAD_B to prevent the short-circuit between the pad units PAD positioned at different rows.

Ex. 1005 (Kim), 9:7-11, 9:46-49.

*see also Paper 29 (Reply), 17;
Paper 1 (Petition), 49-50.*

THE “SIDE SURFACE” OF NAM’S LANDING PAD CONTACTS “A SIDE SURFACE” OF ITS “INSULATING LAYER”

Patent Owner Both Misinterprets the Petition and Misconstrues the Claims

Patent Owner's Position:

The Petition purportedly “arbitrarily” identifies Nam’s “insulating layer.” Nam’s “insulating layer” is not “in contact with a side surface of the insulating layer.” There is only contact with the layer’s bottom.

Paper 25 (Response), 49-57.

Patent Owner Is Incorrect:

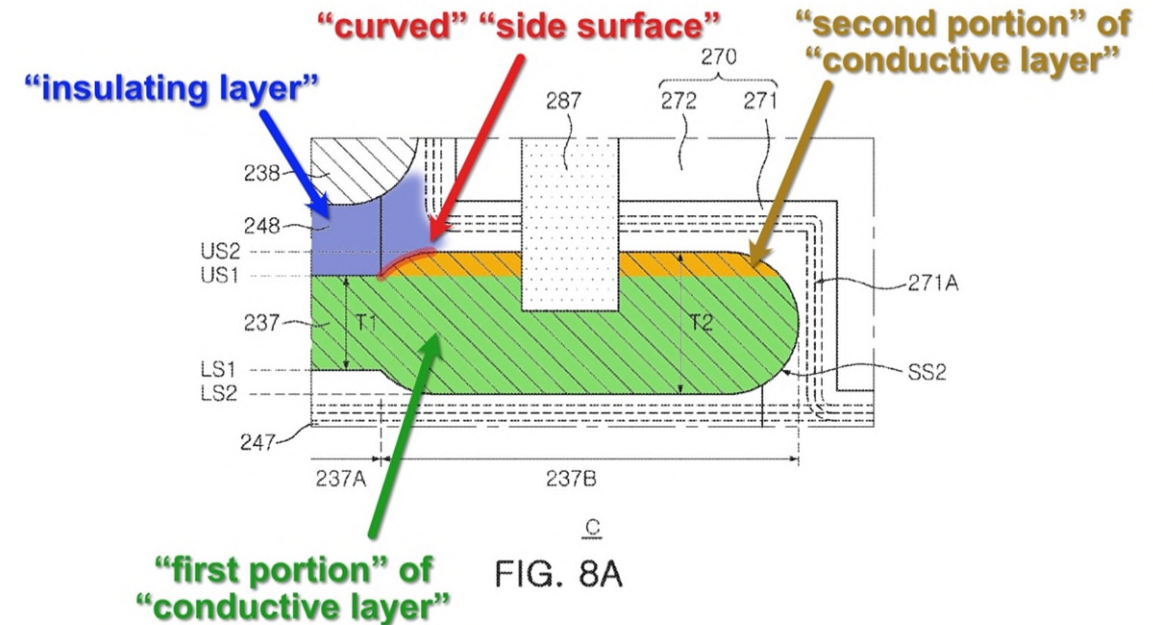
- The Petition **repeatedly identified** both Nam’s insulating layer 240 and the adjacent portion of layer 271 as the claimed “insulating layer”
- The Petition’s discussion of Nam’s “insulating layer” applied **the '666 patent's own** definition of the term
- The “curved side surface” of Nam’s landing pad **does** contact “a side surface” (and not just the “bottom”) of the “insulating layer”

Paper 29 (Reply), 19-22.

The Petition Repeatedly Identified Both Layer 240 and the Adjacent Portion of Layer 271 as the Claimed “Insulating Layer”

A POSITA would have considered both Nam's insulating layer 240 and the adjacent insulating layer 271 to be the claimed **"insulating layer."** Again, layers 240 are located between the gate electrode layers 230. *See id.*, Fig. 7. Further, layer 271 is applied before Nam's staircase structure is complete. *See, e.g., id.*, ¶ [0098]; Fig. 31. The pads at the end of Nam's gate electrode layers are then formed within openings etched in the layer 271. *See id.*, ¶¶ [0099]-[0106]; Figs. 32-34, 36, 39. The layer 271 remains behind in Nam's final product. *See id.*, Fig. 7. Because layer 271 is not only formed from the same material as layer 240, but is used to define the shape of Nam's pads, a POSITA would have understood it to be part of Nam's **"insulating layer."** Ex. 1003, ¶¶ 279-289. Layer 271 is distinguishable from other

An example “*insulating layer*” (insulating layer 248 and the adjacent portion of layer 271) and “*conductive layer*” (the gate electrode 237) are annotated below.

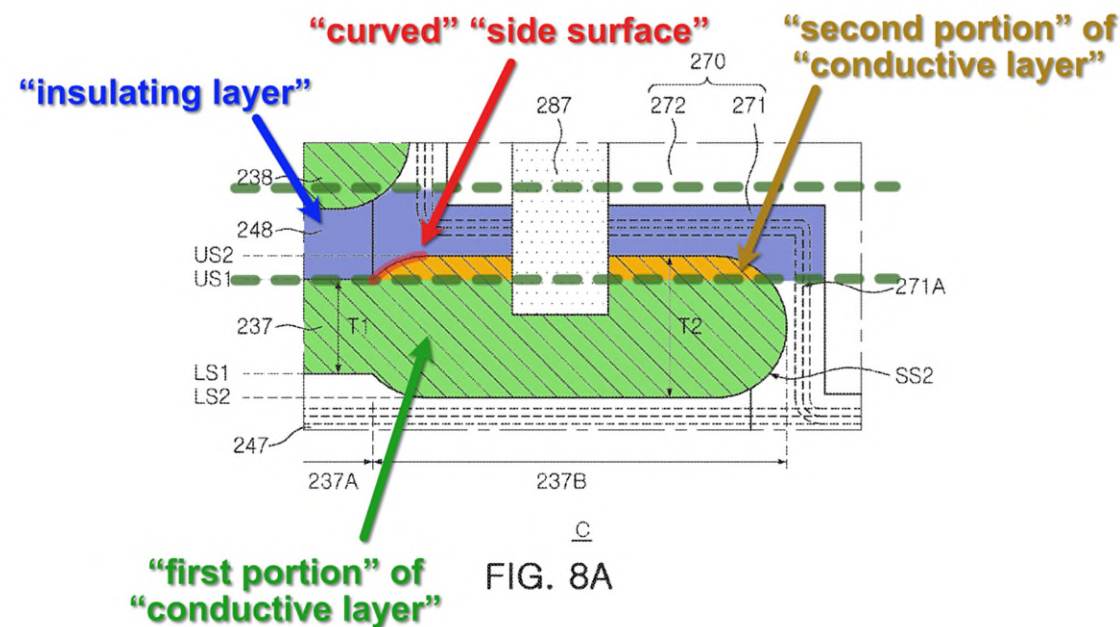


Paper 1 (Petition), 60-62, 65.

The Petition Simply Applied the '666 Patent's Own Definition of the Term "Layer" When Identifying Nam's "Insulating Layer"

As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer has a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate. A layer can extend over the entirety of an underlying or overlying structure, or can have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or

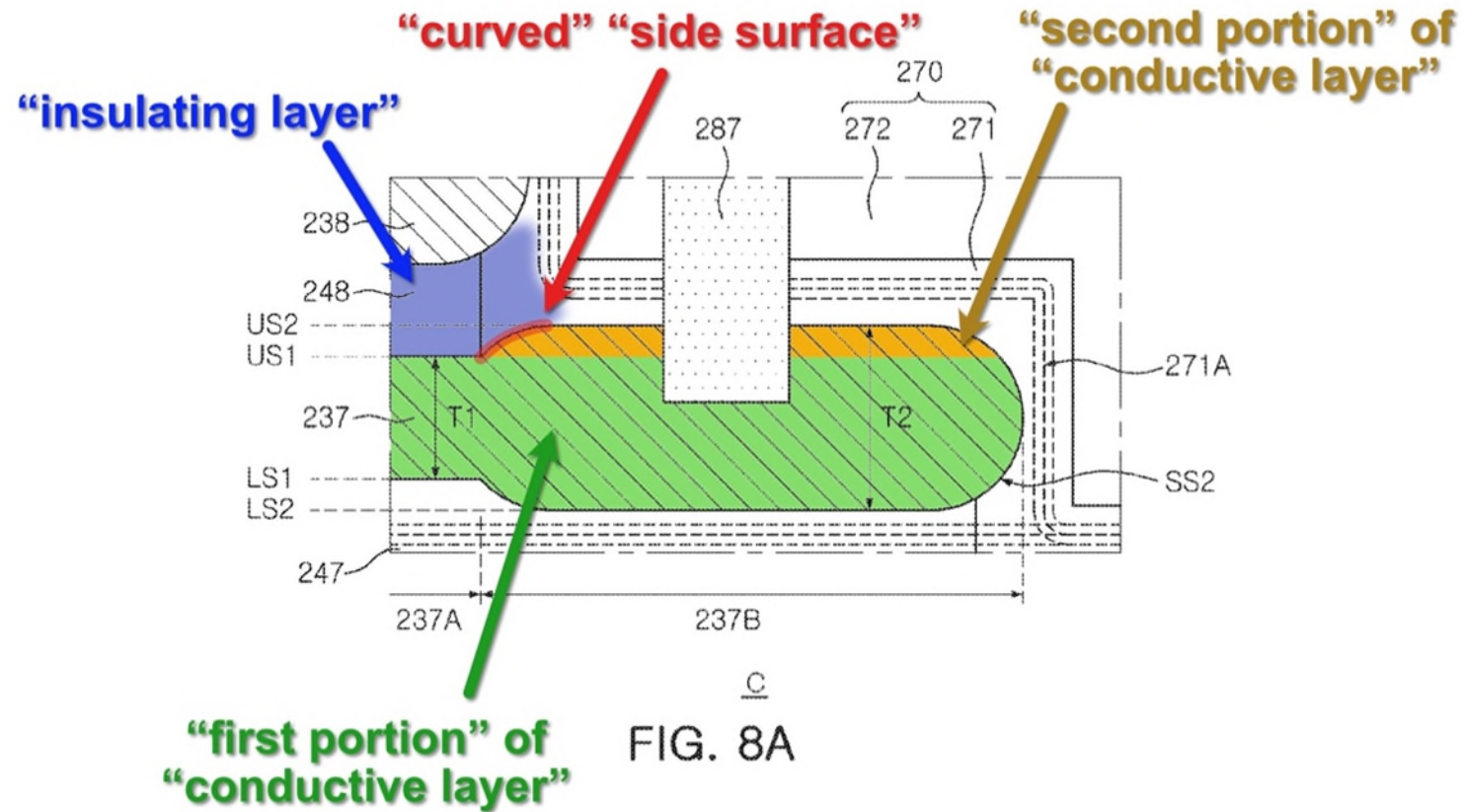
Ex. 1001 ('666 Patent), 4:36-53.



Ex. 1006 (Nam), Fig. 8A;

*see also Paper 29 (Reply), 20-21;
Paper 1 (Petition), 60-62.*

The “Curved Side Surface” of Nam’s Landing Pad Has Dimension in the Z-Axis Direction and Thus Vertical and Contacts “a Side Surface” of the “Insulating Layer” Even Under Patent Owner’s Narrow Construction



Ex. 1006 (Nam), Fig. 8A;
Paper 1 (Petition), 64-65.

**A POSITA WOULD HAVE CONSIDERED IT OBVIOUS TO
EMPLOY A “CURVED” LANDING PAD WITH LEE**

Patent Owner's Arguments Regarding Lee and Park Ignore Both the Petition and the Teachings of the Prior Art

Patent Owner's Position:

Patent Owner argues that the Petition “does not establish” why a POSITA would have been motivated to use a “curved” landing pad like that in Park with Lee. It also argues that it is “techn[ologically] infeasible” to do so.

Paper 25 (Response), 62.

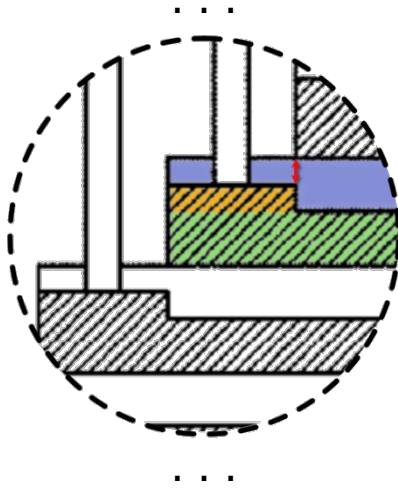
Patent Owner Is Incorrect:

- The Petition **did** explain why a POSITA would have used a landing pad with a “curved side surface” when implementing Lee: not only was this well-known, but doing so would reduce the risk of short circuit.
- A POSITA would have recognized that—just as Park discloses—Lee’s oxide layers **are further oxidizable** to produce rounded landing pads.

Paper 29 (Reply), 22-25.

A POSITA Would Have Recognized that Rounded Landing Pads Would Have Furthered Lee's Goal of Avoiding Short Circuits

418. In my opinion, a POSITA would have recognized that due to their straight sides, each of Lee's pad portions PAD is physically proximate to the adjacent conductive layer immediately above the pad. This is shown below. As



420. In my opinion, a POSITA would have recognized that applying Park's teachings and rounding the side of Lee's pad portion PAD would have improved Lee—and limited the risk of short circuit or other adverse electrical effects—by increasing the minimum distance between the pad and the immediately adjacent conductive layer.

Ex. 1003 (Lee Opening Decl.), ¶¶ 418-420.

the X direction during an etch process. Conventionally, the distance between the stacked conductive layers (pad portions) may decrease, and therefore a breakdown voltage of the conductive layers **25** may be deteriorated. However, according to an embodiment of the present invention, since an etch margin is ensured by the barrier layers **27** and **28**, a sufficient distance may be ensured between the stacked conductive layers (pad portions) to prevent any deterioration.

Ex. 1007 (Lee), ¶ [0049]

see also Paper 29 (Reply), 23; Paper 1 (Petition), 85-86.

Lee's Insulating Layers Can Employ Any Oxide (And Not Necessarily "Solid" "Silicon Dioxide" as Patent Owner Assumes)

[0030] The first material layers **21** may be formed of materials having a high etch selectivity with respect to the second material layers **22**. For example, the first material layers **21** may include a conductive layer such as a polysilicon layer, and the second material layers **22** may include an insulating layer such as an oxide layer. In another example, the first material layers **21** may include a sacrificial layer such as a nitride layer, and the second material layers **22** may include an insulating layer such as an oxide layer.

*Ex. 1007 (Lee), ¶ [0030];
see also Paper 29 (Reply), 24; Paper 1 (Petition), 80.*

Park Itself Teaches that Pad Rounding Can Be Achieved by Performing an “Oxidation Process” on an Existing Oxide Layer

externally exposed. The additional insulating layer 40 may be formed by thermally oxidizing the surfaces and the side surfaces of the sacrificial layer patterns 14a through 14f. The additional insulating layer 40 may be formed on the surfaces and side surfaces of the sacrificial layer patterns 14a through 14f not covered by the interlayer insulating layer patterns 12b through 12f. One end of the additional insulating layer 40 may be rounded by an oxidation process. When one end of the additional insulating layer 40 is rounded, one end of each of conductive layer patterns in a subsequent process may be rounded to prevent a short circuit between the conductive layer patterns.

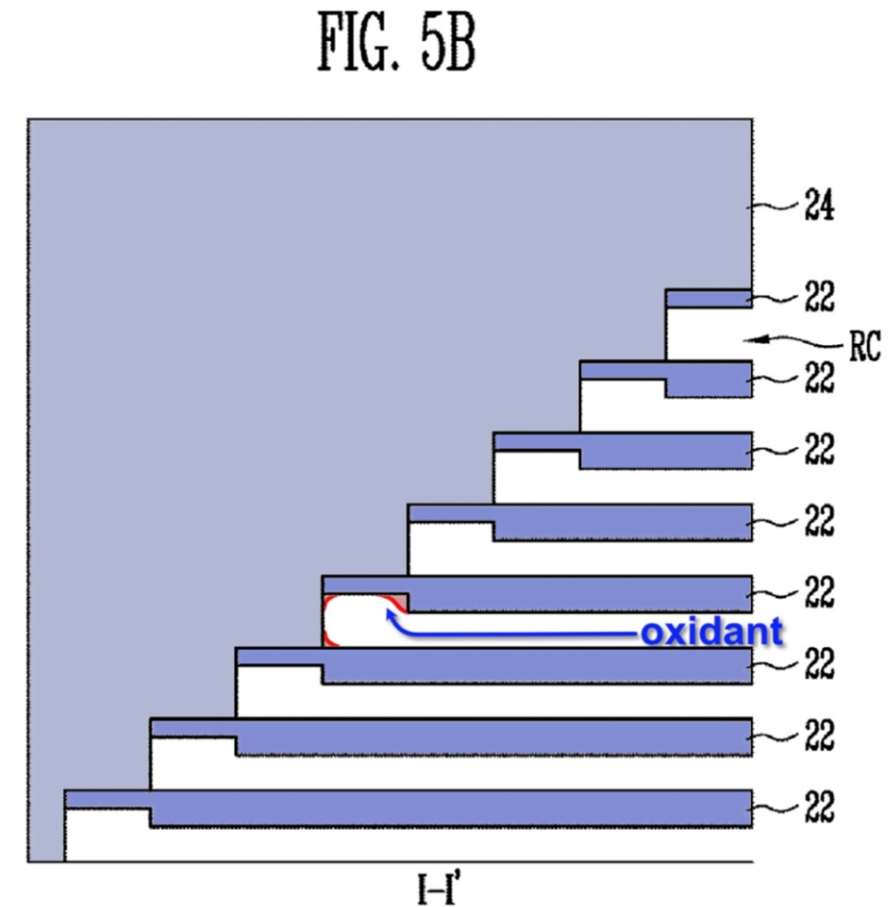
Ex. 1008 (Park), 8:31-42;

see also Paper 29 (Reply), 25

Paper 1 (Petition), 87.

There Is No Dispute That a Non-Stoichiometric Silicon Oxide Is Further Oxidizable (Which Will Result in Landing Pad Rounding)

89. As I noted in my original declaration—and during deposition—when a silicon oxide layer is further oxidized, additional silicon oxide forms preferentially in the areas of exposed, exterior corners. See Ex. 1003, ¶¶ 412-413; Ex. 2010, 267:7-268:22. This includes the corners within the spaces between Lee’s existing oxide layers 22 as illustrated in Fig. 5B below (with the original corners indicated in blue). By “exterior corner,” I did not mean above Lee’s staircase structure. This was a reference to corners that are exposed within the spaces previously occupied by Lee’s sacrificial layers. Further oxide growth—and rounding—will occur in the regions shown in red in Fig. 5B, with the largest amount of oxidation occurring in the rightmost area (as there are two adjacent corners there). This is an additive process. Additional silicon oxide will form on top of the original silicon oxide. The process will continue either until all excess silicon is consumed, or the oxidant is removed. Because the nonstoichiometric film contains silicon atoms that are not fully bonded to oxygen, these under-coordinated silicon atoms preferentially react first, with oxide growth initiating and accelerating at the exposed corner sites.



Ex. 1027 (Lee Reply Decl.), ¶ [0030];
see also Paper 29 (Reply), 23-25; Paper 1 (Petition), 86-87.

The Prior Art Includes Numerous Examples of the Use of Oxidizable Non-Stoichiometric Silicon Oxides in Microelectronics Devices

9.3.4 Silicon Dioxide Deposition

Deposited films of silicon dioxide are utilized throughout silicon microelectronic structures as described in the CMOS process flow in Chapter 2 (see, for example, Figures 2–29 and 2–38). They are used for dielectric layers to electrically separate conducting regions as well as for masks against implantation and diffusion. The requirements for

. . .

Silicon dioxide films deposited using LPCVD or APCVD at low temperatures (less than 500°C) can be nonstoichiometric and are often porous. They can also exhibit inadequate step coverage or filling. The films that are deposited before aluminum is on

Ex. 2008 (Plummer Text), 563-64;

see also Paper 29 (Reply), 24.

The Prior Art Includes Numerous Examples of the Use of Oxidizable Non-Stoichiometric Silicon Oxides in Microelectronics Devices

Recently, considerable research effort was directed to study the silicon-rich silicon oxide films in view of their important role in device manufacturing technology such as memory devices

Ex. 1026 (Bedjaoui Article), 379

The present disclosure relates generally to the field of three-dimensional memory devices and specifically to three-

be optionally formed. Each of the first and second dielectric liners (161, 162) can comprise a silicon oxide layer, a silicon nitride layer, and/or a dielectric metal oxide layer. As used herein, silicon oxide includes silicon dioxide as well as non-stoichiometric silicon oxides having more or less than two oxygen atoms for each silicon atoms. Silicon dioxide is

Ex. 1029 (Oshaki Patent), 1:9-10, 6:45-51;

see also Paper 29 (Reply), 24.

