

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: August 7, 2026

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00189
Patent 11,145,666

PATENT OWNER'S NOTICE OF APPEAL

Notice is hereby given, pursuant to 37 C.F.R. § 90.2(a), that Patent Owner Yangtze Memory Technologies Company, Ltd. ("Patent Owner") appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered by the Patent Trial and Appeal Board (the "Board") on June 9, 2026 (Paper 41) (the "Final Written Decision," a copy of which is attached hereto as Exhibit A).

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal may include, without limitation:

- Whether the Board erred in determining that Petitioner has shown by a preponderance of the evidence that the challenged claim (claim 19) of U.S. Patent No. 11,145,666 is unpatentable as obvious, along with all reasons, findings, opinions, and orders leading thereto or underlying that decision.

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a), this Notice is being filed with the Director of the USPTO, and a copy of this Notice is being concurrently filed with the Board. In addition, a copy of the Notice of Appeal, along with the required docketing fee, is being filed with the Clerk of Court for the United States Court of Appeals for the Federal Circuit.

Respectfully submitted,

Dated: August 7, 2026

By: / Amit Makker /

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CERTIFICATE OF SERVICE

I hereby certify that, pursuant to 37 C.F.R. § 90.2(a)(1)(ii), on this 7th day of August, 2026, I electronically filed the foregoing **PATENT OWNER'S NOTICE OF APPEAL** with the Patent Trial and Appeal Board via P-TACTS, in accordance with 37 C.F.R. § 42.6(b)(1).

I also hereby certify that, pursuant to 37 CFR 90.2(a)(1)(i), on this 7th day of August, 2026, a true and correct copy of the foregoing **PATENT OWNER'S NOTICE OF APPEAL** is being filed with the Director of the United States Patent and Trademark Office by electronic mail to efileSO@uspto.gov.

I also hereby certify that, pursuant to Federal Circuit Rule 52(a)(2), on the 7th day of August, 2026, a true and correct copy of the foregoing **PATENT OWNER'S NOTICE OF APPEAL** and the filing fee, were filed with the Clerk's Office of the U.S. Court of Appeals for the Federal Circuit via CM/ECF.

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 7th day of August 2026, a true and correct copy of the foregoing **PATENT OWNER'S NOTICE OF APPEAL** was served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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EXHIBIT A

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00189
Patent 11,145,666 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We have jurisdiction to conduct this *inter partes* review under 35 U.S.C. § 6, and issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Micron Technology, Inc. (“Petitioner”) shows by a preponderance of the evidence that claim 19 (the “challenged claim”) of U.S. Patent No. 11,145,666 B2 (“the ’666 patent,” Ex. 1001) is unpatentable.

A. Procedural Background

Petitioner filed a Petition to institute an *inter partes* review of claims 17, 19, and 20 of the ’666 patent. Paper 1 (“Pet.”). Yangtze Memory Technologies Company (“Patent Owner”) filed a Preliminary Response. Paper 9. In the Preliminary Response, Patent Owner indicated that it filed a Statutory Disclaimer pursuant to 35 U.S.C. § 253 and 37 C.F.R. § 1.321(a), disclaiming claims 17 and 20 of the ’666 patent, and, accordingly, claim 19 (“the challenged claim”) is the only claim at issue. *Id.* at 4 (citing Ex. 2005).

Pursuant to 35 U.S.C. § 314(a), we instituted an *inter partes* review of claim 19 on the grounds advanced in the Petition on June 10, 2025. Paper 19 (“Dec.”). Patent Owner filed a Patent Owner Response (“PO Resp.,” Paper 25), Petitioner filed a Reply (“Pet. Reply,” Paper 29), and Patent Owner filed a Sur-reply (“PO Sur-reply,” Paper 32).

We held an oral hearing on March 12, 2026, and a transcript is included in the record. Paper 40.

B. Patent Owner’s Disclaimer of Claims 17 and 20

As indicated above, Patent Owner filed a statutory disclaimer of claims 17 and 20 of the ’666 patent. *See* Ex. 2005. In view of Patent Owner’s statutory disclaimer, we treat claims 17 and 20 as having never been part of the ’666 patent. *See Vectra Fitness, Inc. v. TNWK Corp.*,

162 F.3d 1379, 1383 (Fed. Cir. 1998) (“This court has interpreted the term ‘considered as part of the original patent’ in [35 U.S.C.] § 253 to mean that the patent is treated as though the disclaimed claims never existed.”). Because *inter partes* review cannot be instituted based on disclaimed claims, we do not consider claims 17 and 20 to be within the scope of this proceeding. 37 C.F.R. § 42.107(e) (“No *inter partes* review will be instituted based on disclaimed claims.”); *General Elec. Co. v. United Techs. Corp.*, IPR2017-00491, Paper 9 (PTAB July 6, 2017) (precedential) (denying institution in view of a statutory disclaimer of all the challenged claims). Thus, we confine our analysis in this Decision to claim 19, the challenged claim that has not been disclaimed.

C. Real Parties in Interest

Petitioner identifies “Micron Technology, Inc., and its subsidiaries, including Micron Consumer Products Group LLC” as the real parties in interest. Pet. 6. Patent Owner identifies itself as the real party in interest. Paper 4 (Mandatory Notice), 1.

D. Related Matters

The parties indicate that the ’666 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.) (“the parallel proceeding”). Pet. 6; Paper 4, 1.

E. The ’666 Patent

The ’666 patent, titled “Staircase Structure for Memory Device,” is “directed to a staircase structure for a memory device (e.g., 3D memory device)” that “provide[s] numerous benefits including, but not limiting to, yield and manufacturing cost improvements.” Ex. 1001, code (54), 1:37–41. Figure 8 of the ’666 patent is reproduced below.

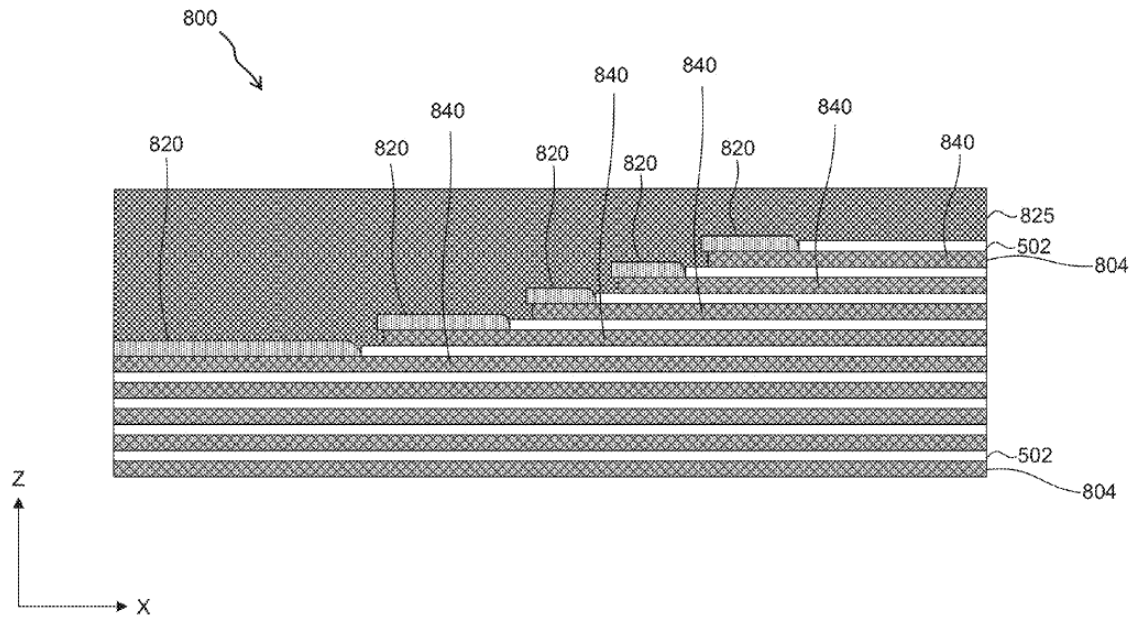


Figure 8 is a cross-sectional view of a staircase structure with a dielectric layer disposed thereon as described in the '666 patent. *Id.* at 3:25–27. Staircase structure 800 includes dielectric layer 825, wordline layers 804, insulating layers 502, landing pads 820, and conductive layers 840. *Id.* at 9:48–61.

The '666 patent explains that each wordline layer 804 of a staircase (“SC”) layer is disposed over a portion of insulating layer 502 of another vertically adjacent SC layer. Ex. 1001, 9:48–50. Landing pad 820 is thicker than insulating layer 502 and is insulated from another landing pad 820 disposed on another vertically adjacent SC layer. *Id.* at 9:53–56. Each wordline layer 804, including landing pad 820 and conductive layer 840 can control a portion of a memory string in the stacked storage region of a memory device. *Id.* at 9:57–61. The '666 patent further explains that each wordline layer 804 is a wordline of the memory device, where conductive layer 840 contacts a portion of a memory string of a memory device, and landing pad 820 contacts a portion of a side of insulating layer 502. *Id.*

at 9:61–65. In some embodiments, landing pad 820 is thicker than conductive layer 840 of wordline layer 804. *Id.* at 9:65–10:1.

F. Illustrative Claim

Petitioner challenges claim 19 of the '666 patent. Claim 19 is reproduced below, along with claim 17 from which claim 19 depends.

17. A memory device, comprising:
- a substrate, wherein the substrate comprises a top surface;
 - a memory string disposed over the substrate; and
 - a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:
 - a plurality of layer stacks, each layer stack comprising an insulated layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.

Ex. 1001, 15:11–16:2.

19. The memory device of claim 17, wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack.

Id. at 16:8–14.

G. Asserted Grounds

Petitioner asserts that claim 19 is unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
19	103 ¹	Kim ²
19	103	Nam ³
19	103	Lee, ⁴ Park ⁵

Pet. 10–11. Petitioner relies on the Declaration of Dr. Jack C. Lee (Ex. 1003) and the Reply Declaration of Dr. Jack C. Lee (Ex. 1027) in support of its contentions. Patent Owner relies on the Declaration of Konstantinos Giapis (Ex. 2023) in support of its contentions.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) “would have had a bachelor’s degree in electrical engineering or a similar discipline, along with 2–3 years of professional experience working with (e.g., researching, designing, or teaching) 3D memory devices, or an equivalent level of skill, knowledge and experience (e.g., an advanced degree may substitute for professional experience).” Pet. 24–25 (citing Ex. 1003 ¶¶ 34–37). Petitioner further contends that the “POSITA would also have been aware of and generally knowledgeable about 3D memory’s structure, its component parts, and how it operates.” *Id.* at 25 (citing Ex. 1003 ¶¶ 34–37).

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the ’666 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (60)), we refer to the AIA version of Sections 102 and 103.

² US 10,229,929 B2, issued March 12, 2019 (“Kim,” Ex. 1005).

³ US 2018/0026046 A1, published Jan. 25, 2018 (“Nam,” Ex. 1006).

⁴ US 2014/0191389 A1, published July 10, 2014 (“Lee,” Ex. 1007).

⁵ US 10,297,543 B2, issued May 21, 2019 (“Park,” Ex. 1008).

Patent Owner responds that it “does not dispute Petitioner’s proposed level of a” POSITA “for purposes of this IPR.” PO Resp. 8 (citing Pet. 24–25).

In the Institution Decision, we adopted the assessment offered by Petitioner. Dec. 12–13. Because Petitioner’s definition of the level of skill in the art is consistent with the ’666 patent and the asserted prior art, we maintain Petitioner’s definition for purposes of this Final Written Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir 2001).

B. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

Based on our review of the complete trial record and the arguments raised by the parties, we determine that it is necessary to address the claim term “curved side surface.”

1. “curved side surface”

Claim 17 recites, *inter alia*, “a second portion of the conductive layer comprises a curved side surface.” Ex. 1001, 15:18–16:1. Patent Owner proposes that “curved side surface” be construed as a “vertical surface curved along a direction (e.g., the z-axis) perpendicular to the top surface of

the structure.” PO Resp. 8. Patent Owner argues that the “claim language contrasts vertical ‘side surface[s]’ with horizontal ‘top surface[s]’/‘bottom surface[s].’” *Id.* at 9; *see also id.* at 9–10 (asserting that claim 1 recites “a bottom surface” and “a top surface opposite the bottom surface,” and claim 2 recites “a first side surface and a second side surface”). Patent Owner’s declarant, Dr. Giapis, testifies that “claim 17 claims ‘*a curved side surface* in contact with *a side surface* of the insulating layer,’ using the term ‘side surface’ to describe what a POSITA would have understood to be a vertical surface.” Ex. 2023 ¶ 42. Dr. Giapis further testifies:

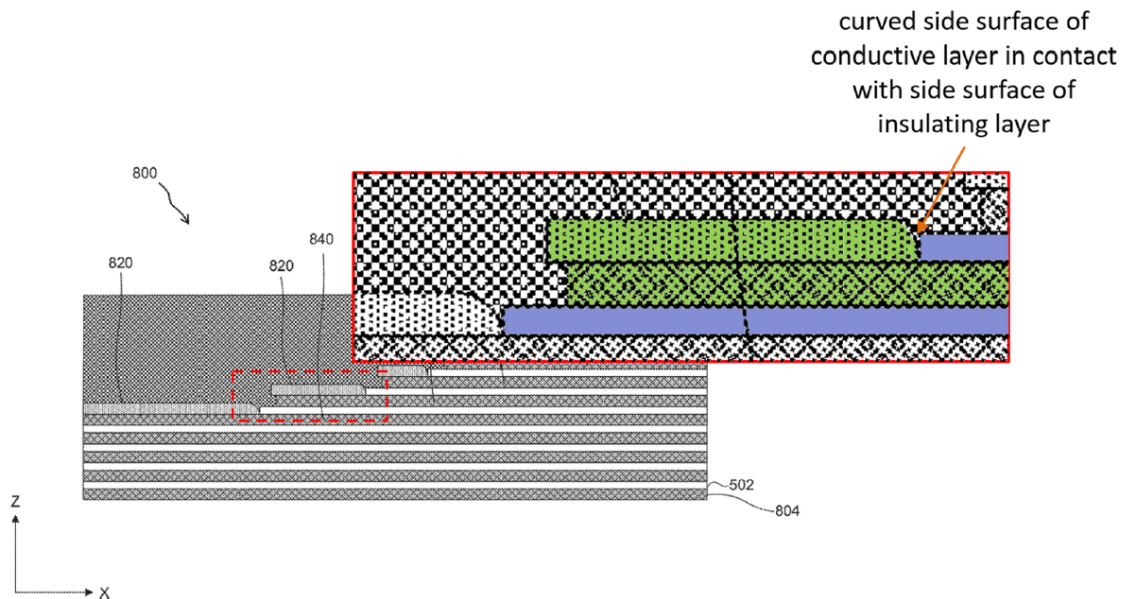
Claim 1 states “each landing pad comprises: **a bottom surface**; and **a top surface** opposite to **the bottom surface**,” surfaces a POSITA would understand to be horizontal surfaces. Claim 2 depends from claim 1 and states that each of the landing pads “comprises **a first side surface** and **a second side surface**.” As such, the claims themselves show that the landing pad has a “top” and “bottom” “surface,” which are horizontal surfaces, and a first and second “side surface,” which are vertical. As claims 17 and 19 use similar language, a POSITA would interpret the use of the similar terms the same across the claims.

Id. ¶ 43.

Patent Owner argues that the Specification confirms its proposed construction. PO Resp. 10–24. Patent Owner notes that claim 19 recites “a staircase structure,” and the Specification explains that a staircase structure includes “at least two horizontal surfaces (e.g., along an x-y plane) and at least two vertical surfaces (e.g., along a z-axis)” where “[a] horizontal direction can refer to a direction (e.g., the x-axis or the y-axis) parallel with a top surface of the substrate” and “[a] vertical direction can refer to a direction (e.g., the z-axis) perpendicular to the top surface of the structure.” *Id.* at 10–11 (citing Ex. 1001, 5:44–58). Patent Owner asserts that the Specification consistently refers to a horizontal surface as a top or bottom

surface and consistently refers to a vertical surface as a side or side surface. *Id.* at 11 (citing Ex. 1001, 5:52–58, 5:63–65, 7:1–7, 7:63–8:2, 8:11–20, 8:36–39, 8:41–60, 11:55–59, 12:16–20, 12:32–39, 12:58–61, 7:5–7, 7:63–8:2, 8:11–27, 8:39–40, 8:41–60, 9:61–65, 11:52–57, 12:4–5, 12:13–15, 12:33–39, 12:50–51, cls. 1–3, 5, 6, 8–11, 13, 15, 17–18, 20; Ex. 2023 ¶¶ 44–55).

Patent Owner also argues that “the only embodiment of the ‘curved side surface’ of the ‘conductive layer’ . . . is shown to be curved only along the vertical direction.” PO Resp. 17. Patent Owner provides an annotated and concentrated version of Figure 8, reproduced below, to illustrate its arguments.



Id. at 18. Figure 8 is a cross-sectional view of a staircase structure with a dielectric layer disposed thereon according to some embodiments of the ’666 patent, with Patent Owner’s identification of the location of the curved side surface. *Id.*; Ex. 1001, 3:25–28. Patent Owner argues that, “consistent with claim 19, the ’666 patent describes that ‘landingpad 820 contacts a portion of a **side** of insulating layer 502,’ as identified above in the figure.” PO

Resp. 18 (citing Ex. 1001, 9:61–65; Ex. 2023 ¶¶ 53–54). Patent Owner argues that, “as the ‘only embodiment’ of a ‘curved side surface,’ it is ‘highly indicative of the scope of the claims.’” *Id.* (quoting *Medicines Co. v. Mylan, Inc.*, 853 F.3d 1296, 1309 (Fed. Cir. 2017)). Patent Owner further argues that “a curved side surface that is a ‘vertical surface curved along a direction (e.g., the z-axis) perpendicular to the top surface of the structure’ is the only kind of curved side surface that can be formed from the only process disclosed in the ’666 patent.” *Id.* at 19 (citing Ex. 2023 ¶¶ 56–58).

Patent Owner further argues that “[t]he stated purpose of the ’666 patent’s invention is to provide ‘a staircase structure for a memory device’ that ‘provide[s] numerous benefits including, but not limiting to, yield and manufacturing cost improvements.” PO Resp. 22 (citing Ex. 1001, 1:37–41). According to Patent Owner, “[a] POSITA would have understood that one of these yield and manufacturing cost improvements is to have a ‘curved side surface,’ which limits the risk of short-circuits while also making it easy to manufacture.” *Id.* (citing Ex. 2023 ¶¶ 36–37, 59).

Petitioner responds that “[c]laim 19 (and claim 17 on which it depends) does not use the words ‘vertical’ or ‘z-axis’” and “does not mention (or exclude) ‘internal’ or ‘inner’ insulating layer surfaces.” Pet. Reply 3 (citing Ex. 1001, cl. 17). Petitioner contends that “a ‘side’ of a three-dimensional object is any ‘outer surface of [the] object,” and that claim 19 uses “side” “to refer to any of the various surfaces making up the claimed ‘second portion of the conductive layer’ (or landing pad) and ‘insulating layer.’” *Id.* at 3–4 (citing Ex. 1024, 483). In that regard, Petitioner contends that the recited “side” can be a vertical or horizontal surface, a surface that includes both vertical and horizontal components, the top, bottom, left, right, front, or back of a “layer,” an internal side that

bounds a hole through the layer, or at the end of a layer. *Id.* at 4. Petitioner further contends that, even if the claims did require the “curved side surface” to be vertical, “it most certainly does not require a curve ‘along . . . the z-axis.’” *Id.* at 5. According to Petitioner, as “long as there is surface curvature, the claim is satisfied.” *Id.*

Petitioner further contends that “the word ‘curved’ does not appear anywhere in the ’666 patent’s specification,” and “[t]he specification does not attribute any importance to this claimed feature, or state that the claimed ‘curved side surface’ must curve in any specific way.” Pet. Reply 5. Petitioner points to the Specification’s definitions of “horizontal” and “vertical,” and contends that such terms “could have been included in claim 19 to further characterize the claimed ‘curved side surface’ or ‘side surface of the insulating layer.’” *Id.* Petitioner contends that the absence of such descriptors in claim 19 “impl[ies] that the applicant intended the claims to more broadly embrace horizontal, vertical, and other differently oriented surfaces.” *Id.* (citing *Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 807 (Fed. Cir. 2007); Ex. 1028, 51:24–52:7). Petitioner further contends that “the specification explicitly characterizes both the ‘top’ and ‘bottom’ of a ‘layer’ (which are horizontal, not vertical) as ‘sides.’” *Id.* at 7 (citing Ex. 1001, 4:36–40); *see also* Ex. 1001, 4:48–57 (explaining that “a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure” and “can extend horizontally, vertically, or along a tapered surface”).

In the Sur-reply, Patent Owner argues that “reading ‘side’ to mean any surface improperly renders ‘side’ meaningless such that it ‘would be erased from the claims’—an outcome the Federal Circuit highly disfavors.” PO Sur-reply 4 (citing *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 809–810

(Fed. Cir. 2021); *SSI Techs., LLC v. Dongguan Zhengyang Elec. Mech. Ltd.*, 59 F.4th 1328, 1335 (Fed. Cir. 20223)). Patent Owner also argues that, because claims 1 and 2 “recite a ‘top surface’ and a ‘bottom surface’ as distinct from a ‘side surface,’” “the same is true for claim 19’s” side surface. *Id.* at 4–5.

Having reviewed the claim language, the Specification, and the evidence from the complete record now before us, we determine that the claim term “curved side surface” encompasses any outer surface of the structure with curvature. *See Hamilton Beach Brands, Inc. v. F’real Foods, LLC*, 908 F.3d 1328, 1338–1339 (Fed. Cir. 2018) (finding that it is acceptable for the Board to adopt its own claim construction where the parties “had notice of the contested claim construction and an opportunity to be heard”). We do not adopt Patent Owner’s position that “curved side surface” requires the side surface to be curved along a direction perpendicular to the top surface of the structure (e.g., the z-axis).

Claim 17 recites “the staircase structure comprises . . . a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer.” Ex. 1001, 15:14–16:2. “Side surface” is not defined in the Specification. The Specification does, however, define “layer” as having “a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate” that “can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of a continuous structure.” *Id.* at 4:37–40, 4:45–48. The Specification describes the “substrate” as including a top surface and a bottom surface, and explains that “[t]he top

surface of the substrate is where a semiconductor device is formed at a top side of the substrate” and “[t]he bottom surface is opposite to the top surface and therefore a bottom side.” *Id.*

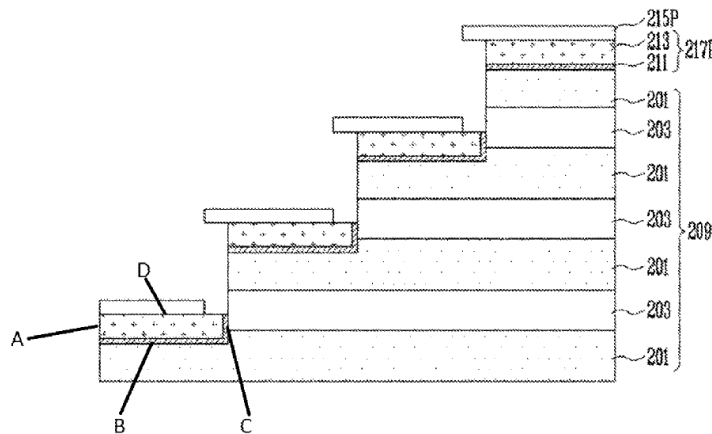
Taken together, these disclosures indicate that the top and bottom of the structure are “sides,” and that when the ’666 patent refers to the “top surface” and the “bottom surface,” it is referring to the horizontally-oriented top and bottom sides of the structure.

The claims also distinguish between the top, bottom, and side surfaces of a structure. For example, claim 1 recites that “each landing pad comprises: a bottom surface; and a top surface opposite to the bottom surface, wherein the top surface is above another top surface of the first material layer of the respective layer stack.” Ex. 1001, 13:55–60. Claim 2 depends from claim 1 and further recites that each landing pad “comprises a first side surface and a second side surface, wherein the first side surface is in contact with the first material layer of the respective layer stack, and wherein the second side surface is laterally displaced from a third side surface of the second portion of the second material layer of the respective layer stack.” *Id.* at 13:62–67. The “first side surface” and “second side surface” recited in claim 2 are different parts of the structure than the “top surface” and “bottom surface” recited in claim 1. Because the top and bottom surfaces recited in claim 1 are the horizontal surfaces (top and bottom sides) of the landing pad, the “first side surface” and “second side surface” are two distinct surfaces of the landing pad, the relative location of which is provided by other claim limitations (the first side surface “is in contact with the first material layer of the respective layer stack,” and the second side surface “is laterally displaced from a third side surface of the second portion of the second material layer of the respective layer stack.”).

Likewise, claim 17 refers to a “top surface” of a substrate, a “side surface” of a second portion of the conductive layer, and a “side surface” of the insulating layer. When read in context of the Specification and the claim as a whole, the “top surface” is the top (horizontal) side of the substrate, and the “side surfaces” of the conductive layer and insulating layer are other surfaces (i.e., not the top side) of the conductive and insulating layers.

This understanding is also consistent with the '666 patent's prosecution history. The '666 patent is a continuation of U.S. Patent No. 10,680,003 (“the '003 patent”). Ex. 1001, code (63). During prosecution of the '003 patent, the Examiner rejected pending claim 1 directed to a semiconductor structure with a landing pad comprising “a first side surface and a second side surface, wherein the second side surface is vertically below and laterally displaced from the first side surface” over art (Hyun) that disclosed a landing pad with 4 side surfaces. Ex. 1014, 240, 269. The rejection was based on Hyun's Figure 2E, reproduced below.

FIG. 2E



Id. at 270. Referring to Figure 2E, the Examiner explained:

An example landing pad has 4 side surfaces: A, B, C, and D. Side surfaces B and D can be viewed as first and second side

surfaces, wherein side B is vertically below (and thus laterally displaced) from side D. (In addition, sides A and C of Hyun would also be side surfaces, side A would also be laterally displaced from side C, and sides A and C would be adjacent one another—though not in an above/below relationship as B and D are).

Id. at 269. The Examiner also rejected pending claim 18, which recited “the second portion of the conductive layer comprises a first side surface and a second side surface, wherein the second side surface is vertically below and laterally displaced from the first side surface,” for the same reasons. *Id.* at 241, 271.

The Applicant responded, “[w]ithout acquiescing to the propriety of the rejections,” by amending claim 1 “to include the feature of ‘wherein each landing pad comprises a bottom surface substantially coplanar with another bottom surface of the first material layer of the respective layer stack’ as recited in claim 21.” Ex. 1014, 287. The Applicant also amended claim 18 “to recite ‘wherein the first side surface and the second side surface are substantially perpendicular to the top surface.’” *Id.* at 288. The Applicant explained:

Referring to annotated Fig. 2E of Hyun (see Final Office Action, p. 4), the Office concedes that “sides A and C . . . would not in an above/below relationship B and D are.” (see Final Office Action, p. 3). Thus, Hyun does not disclose or suggest the above-noted distinguishing feature “wherein the first side surface and the second side surface are substantially perpendicular to the top surface,” as recited in claim 18.

Id. The claims as amended were subsequently allowed. *Id.* at 299.

The addition of “top surface” and “bottom surface” to claims 1 and 18 of the ’033 patent demonstrates that “side surface” the Applicant distinguishes the claimed “side surface” from the top and bottom surfaces,

which, per the Specification shared with the '666 patent, are defined as the top and bottom sides. This is further confirmed by claim 18's requirement that the first and second side surfaces be "substantially perpendicular to the top surface."

Petitioner asserts that the Applicant "did not dispute the Examiner's characterization of the landing pad's top and bottom as 'side surfaces,'" instead choosing to amend the claims to add the "substantially perpendicular to the top surface" limitation to claim 18. Pet. Reply 10 (citing Ex. 1014, 284–285). Petitioner argues that, because "[n]o such limitation is present in the '666 patent claims," the '666 patent "claims embrace all possible 'side surfaces' of a 'layer,' including the top and bottom." *Id.* We agree, for the reasons set forth above. The claims of the '666 patent, like the claims of the '033 patent, set forth the relative location of the sides through other limitations. In the '033 patent, the phrases "top surface," "bottom surface," and "the first side surface and the second side surface are substantially perpendicular to the top surface" distinguish the different sides of the structure; in the '666 patent, "top surface" and "curved side surface in contact with a side surface of the insulating layer" provide the details needed to identify which side of the structure is being referred to in the claims.

We do not find, however, that the recited "curved side surface" must be curved in a vertical direction (e.g., along the z-axis). Patent Owner argues that Figure 8 is the only embodiment of a "curved side surface" provided in the Specification, and, "as the 'only embodiment' of a 'curved side surface,' it is 'highly indicative of the scope of the claims.'" PO Resp. 18 (citing *Medicines Co. v. Mylan, Inc.*, 853 F.3d 1296, 1309 (Fed. Cir. 2017)). That a patent describes only a single embodiment, however, does not require that the claims be construed as limited to that embodiment.

Liebel-Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 906 (Fed. Cir. 2004). A patent will only be read restrictively when “the patentee has demonstrated a clear intention to limit the claim scope using ‘words or expressions of manifest exclusion or restriction.’” *Id.* (quoting *Teleflex, Inc. v. Ficoso N. Am. Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002)). The Specification here does not describe a “curved side surface” in connection with Figure 8 or otherwise, let alone demonstrate an intention to limit the scope of “curved side surface” to a side surface curved in a particular direction. The Specification does describe that the second portion of the conductive layer is in contact with a side surface of the insulating layer “in some embodiments,” and that the “second portion of the conductive material layer is thicker than the first portion of the conductive material layer.” Ex. 1001, 2:46–57. Moreover, without a view of the staircase structure in the x-y plane, we cannot state that the curved surface shown in Figure 8 is only curved in the vertical direction as Patent Owner contends. *See* Ex. 1027 ¶ 25 (Dr. Lee testifying that “the ’666 patent includes no views of its memory device in the x-y plane. Thus, it is not possible to state—as Dr. Giapis does—that the patent lacks a ‘curved side surface’ in this plane. The patent does not say one way or another.”). We are not convinced that the Specification suggests that the recited “curved side surface” must be curved in the vertical direction. *See Promptu Sys. Corp. v. Comcast Corp.*, 92 F.4th 1372, 1379 (Fed. Cir. 2024) (“[F]eatures recited in the specification merely as aspects of embodiments, and not expressly or even implicitly identifying requirements of the invention, do not narrow a claim term that is otherwise broader in its ordinary meaning.”).

Patent Owner also argues that “the specification discloses a process flow that yields a side surface curved only along the x-axis.” PO Sur-reply 7

(citing Ex. 2023 ¶¶ 32–36). In that regard, the Specification states that “[t]he operations of method 900 can be used to form memory device structures illustrated in FIGS. 1–8,” and that the operations “are not exhaustive” and “other operations can be performed as well before, after, or between any of the illustrated operations.” Ex. 1001, 10:46–50. Further, Dr. Lee testifies:

[T]he patent does not even limit itself to techniques “such as plasma-enhanced CVD and directional sputter deposition (PVD).” Instead, it states that its layers can be formed using other techniques, such as “low pressure CVD (LPCVD)” and “atomic layer deposition (ALD)” along with “any suitable deposition techniques or combinations thereof.” ‘666 patent, 9:2–7; *see also id.*, 2:39–45.

Deposition techniques like LPCVD and ALD—by themselves—will not produce a vertically curved landing pad side surface like that shown in the ‘666 patent’s figures. These techniques can, however, produce landing pads that are curved in the x-y plane (using an appropriately shaped mask during deposition). Moreover, “poor step coverage” is a descriptive term for non-conformal thickness distribution and does not impose any particular direction of curvature. A POSITA would understand that non-conformal deposition can produce curvature in different directions depending on feature geometry, shadowing, and mask shape, rather than only in the z-direction.

Ex. 1027 ¶¶ 28–29. We are not convinced that the process described in the ‘666 patent, which does not describe making a curved side surface and, in any event, is not within the scope of the claims, requires that the curved side surface be curved in the vertical direction.

For these reasons, we determine that “curved side surface” encompasses any outer surface of the structure with curvature, which construction expressly does not require that the surface be curved in any specific direction.

C. Ground 1: Asserted Obviousness over Kim

Petitioner contends that claim 19 would have been obvious over Kim. Pet. 33–55.

1. Overview of Kim

Kim is directed to “semiconductor memory devices having enhanced reliability.” Ex. 1005, 1:38–39. Kim teaches that the semiconductor memory device includes a substrate with a cell array region, a contact region, and stacking structure including a plurality of insulating layers and a plurality of gate electrodes alternately stacked on the substrate. *Id.* at 1:41–46. “The stacking structure may include a stepwise structure in the contact region.” *Id.* at 1:46–47. Kim teaches that one of the plurality of gate electrodes “may include a respective pad unit that comprises a step of the stepwise structure,” and “[a]t least one of the pad units may include a base pad and a protrusion pad on the base pad.” *Id.* at 1:47–50. Kim further teaches that “[t]he protrusion pad may be between and spaced apart from two edges of a surface of the base pad that are perpendicular to an extension direction of the respective gate electrode.” *Id.* at 1:51–53.

CTR have a stepwise structure. Ex. 1005, 7:47–52. Pad unit PAD is at an end of gate electrode 300 exposed through the stepwise structure. *Id.* at 7:58–59. Pad units PAD include base pad PAD_B and protrusion pad PAD_P contacting a surface of base pad PAD_B. *Id.* at 7:60–62. Base pad PAD_B may be part of gate electrode 300 in contact region CTR, and “may be exposed by an adjacent pad unit PAD that is stacked on the pad unit PAD.” *Id.* at 7:63–66. “The pad unit PAD and the adjacent pad unit PAD may not overlap with each other.” *Id.* at 7:66–67. Protrusion pad PAD_P may contact the uppermost surface of base pad PAD_B that is exposed by the adjacent base pad PAD_B. *Id.* at 8:3–10.

2. Claim 19

Claim 19 depends from, and includes all of the limitations of, claim 17. Ex. 1001, 16:8–14. Petitioner contends that Kim teaches or discloses all of the limitations of claim 17. Pet. 33–53. For example, Petitioner contends that Kim teaches “a substrate, wherein the substrate comprises a top surface” (substrate 100 with an upper surface on which a plurality of gate electrodes are stacked), “a memory string disposed over the substrate” (memory cell array includes a plurality of cell strings extending in a vertical direction to a plane of the substrate), and “a staircase structure disposed adjacent to the memory string” (contact region CTR with a stepped structure positioned on the periphery of cell array region CAR). *Id.* at 33–36 (emphases omitted); Ex. 1003 ¶¶ 141–156.

With respect to the “a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer” limitation of claim 17, Petitioner contends that “Kim’s memory device includes a step-shaped ‘stacking structure SS’ formed from a ‘plurality’ of alternating ‘insulating layers 110 and . . . gate electrodes 300’

located ‘on the substrate 100.’” Pet. 36, 39 (citing Ex. 1005, 6:35–36) (alterations in original). Petitioner contends that “Kim also explains that its device includes an ‘auxiliary insulating layer 122’” that “‘may include the same or similar material as the insulating layer 110’ such that ‘a boundary between the auxiliary insulating layer 122 and the insulating layer 110 may not be distinguished and the auxiliary insulating layer 122 and the insulating layer 110 may form one structure.’” *Id.* (citing Ex. 1005, 9:12–13, 9:29–38). According to Petitioner, “[a] POSITA would have understood that Kim’s insulating layer 110 and the adjacent portion of auxiliary insulation layer 122 together constitute the claimed ‘insulating layer’ in a ‘layer stack.’” *Id.* at 39–40 (citing Ex. 1003 ¶¶ 157–172) (emphases omitted). Petitioner identifies gate electrodes 300, which “can be formed from conductive material,” as the claimed “conductive layer.” *Id.* at 39; *see also id.* at 41 (“An example ‘layer stack’ including an ‘insulating layer’ (the combination of Kim’s insulating layer 110 and auxiliary insulating layer 122) and ‘conductive layer’ (the gate electrode 300) are annotated in Figure 4B below.” (emphases omitted)).

With respect to the “wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer” limitation of claim 17, Petitioner first contends that “Kim’s device includes both a ‘conductive layer’ with a ‘first portion’ (gate electrode 300 and attached base pad PAD_B) and a ‘second portion’ (protrusion pad PAD_P).” Pet. 42–43 (citing Ex. 1005, Fig. 4B; Ex. 1003 ¶¶ 186–193) (emphases omitted). Petitioner then contends that, because protrusion pad PAD_P is located inside opening 122_O in auxiliary insulating layer 122, “there is ‘contact’ between a ‘side surface’ of Kim’s ‘second portion’ (the protrusion pad PAD_P) and a ‘side surface of the

insulating layer’ (the side walls of opening 122_O in auxiliary insulating layer 122).” *Id.* at 44–45 (citing Ex. 1005, 9:21–23, Fig. 4B; Ex. 1003 ¶¶ 197–199) (emphases omitted).

Finally, Petitioner asserts Kim explains that protrusion pad PAD_P “may have a shape including a curved surface based on a virtual rectangular parallell[] shape, a cylindrical shape, or any shape,” and contends that “[a] POSITA would have understood that this teaches a variety of different protrusion pad PAD_P shapes, many of which have the type of ‘*curved*’ side surface claim 17 requires.” Pet. 45 (citing Ex. 1005, 8:29–34). Petitioner contends that the claim “is open to any type of ‘curved side surface’ and that Kim’s cylindrical pad “has a ‘curved side surface’ (the surface following the shape of a cylinder when viewed from above).” Pet. Reply 11–12.

Patent Owner responds that “Kim does not teach the claimed ‘curved side surface in contact with a side surface of the insulating layer’ because it does not teach a ‘vertical surface curved along the vertical direction.’” PO Resp. 29. Patent Owner argues that “a POSITA would have understood that none of Kim’s disclosures involve a vertical surface curved along a direction (Kim’s z-axis) perpendicular to the top surface of the structure.” *Id.* at 30 (citing Ex. 2023 ¶¶ 66–73). Patent Owner also argues that “Kim’s manufacturing process cannot produce a vertical surface curved along the vertical direction” because “Kim uses ‘a photosensitive resin pattern M’ that precisely defines ‘the region 122_I for forming the protrusion pad’ (i.e., conductive layer)” and “the Petition says nothing about how Kim’s process will form a vertical surface curved along the vertical direction.” *Id.* (citing Ex. 1005, 12:61–67), 33. Patent Owner also argues that “[r]egardless of whether a ‘right cylinder, an elliptical cylinder, or even a generally rectangular cylinder with two sides that follow a cylindrical pattern’ is

formed, as argued, none of these shapes curve vertically, and thus they do not form the claimed ‘curved side surface.’” *Id.* at 35 (citing Pet. 51–53; Ex. 2023 ¶¶ 81–86).

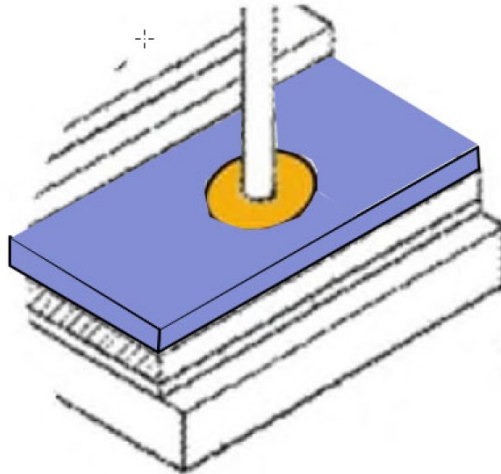
Patent Owner’s arguments that Kim does not disclose the claimed “curved side surface” are premised on its proposed claim construction which, as set forth above, we decline to adopt. Instead, we determined that “curved side surface” as used in the challenged claim encompasses any outer surface of the structure with curvature, which does not need to be curved in any specific direction. *See* § II.B.1, *supra*. Kim states:

Embodiments of the inventive concepts in which the protrusion pad PAD_P has a rectangular parallel[] shape is illustrated, but the protrusion pad PAD_P is not limited thereto and, in some embodiments, may have a shape *including a curved surface* based on a virtual rectangular parallel[] shape, a cylindrical shape, or *any shape*.

Ex. 1005, 8:29–34 (emphases added). Dr. Lee testifies that “[a] POSITA would have recognized that this includes configurations where the sides of the protrusion pads are curved, particularly to optimize electrical connectivity and mitigate stress at material interfaces.” Ex. 1003 ¶ 201. Dr. Lee further testifies that a POSITA would have understood Kim’s disclosure “teaches a variety of different protrusion pad PAD_P shapes” including “pads with curved sides when viewed in cross-section or pads with curved sides when viewed from above.” *Id.* ¶ 202. Accordingly, we determine that Kim discloses a cylindrically-shaped PAD_P that has a “curved side surface” as required by the challenged claim.

Patent Owner further argues that “if PAD_P is shaped as a ‘cylindrical’ contact pads, as discussed in the Petition, then there will be no contact between the PAD_P . . . and ‘a side surface of the insulating layer’

as required by claim 19.” PO Resp. 37. Patent Owner argues that, when PAD_P is cylindrically shaped, “a POSITA would have understood the auxiliary insulating layer 122 (blue) would entirely surround the PAD_P (orange), as shown below,” using a cylindrically-shaped PAD_P as an example.



Id. (citing Ex. 2023 ¶¶ 82–86; Ex. 1005, 10:30–32, 10:49–51, Fig. 6). According to Patent Owner, “PAD_P (orange) contacts the purported insulating layer (blue) at an internal or inner surface, not a side surface, because it is completely surrounded by the insulating material.” *Id.* at 39 (citing Ex. 2023 ¶¶ 82–84).

We disagree. Claim 19 only requires contact with “a side surface of the insulating layer.” As we discuss above, the term “side surface” itself, as it is used in the ’666 patent, encompasses any outer surface of the structure. *See* § II.B.1, *supra*. What Patent Owner refers to as “an internal or inner surface” is an outer surface of the insulating layer. If cylindrical PAD_P were removed from the insulating layer depicted above, outer surfaces of the insulating layer bordering the area previously occupied by PAD_P would be visible. There is nothing in claim 19 that indicates that “a side surface of the

insulating layer” requires that the side surface be on the end of the insulating layer.

We note that Patent Owner argues that Dr. Lee “admits that ‘Kim does not expressly or inherently disclose the curved side surface.’” PO Resp. 28–29 (citing Ex. 2010, 130:8–133:3). Patent Owner argues that this undermines Petitioner’s obviousness theory. PO Sur-reply 12 (citing *AIA Eng’g Ltd. v. Magotteaux Int’l S/A*, 657 F.3d 1264, 1278 (Fed. Cir. 2011)). In *AIA Engineering*, which Patent Owner cites for the proposition that arguments “where the proponent’s expert’s admissions undermined the position” should be rejected, AIA proposed a claim construction that required a material that AIA’s expert admitted was physically impossible to produce. *AIA Eng’g*, 657 F.3d at 1278. The Court, however, did not reject AIA’s construction based on its expert testimony, instead determining that the specification provided “a special meaning” of the disputed claim term that governed the construction and also avoided the inoperable claim construction. *Id.* Here, Dr. Lee’s testimony, elicited on cross-examination, is not sufficient to overcome Kim’s disclosure of “a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer” as required by the challenged claim.

Patent Owner does not address Petitioner’s specific contentions with respect to the other limitations of claim 19. *See* PO Resp. 27–49. We reviewed Petitioner’s contentions for all of the elements of claim 19, including the elements of claim 17 from which claim 19 depends, and are persuaded, on this record, that Petitioner’s discussion of the particular structures Kim and the explanations in the Lee Declarations establish by a

preponderance of the evidence that claim 19 would have been obvious over the teachings of Kim. *See* Pet. 33–55.⁶

D. Ground 2: Asserted Obviousness over Nam

Petitioner contends that claim 19 would have been obvious over Nam.
Pet. 56–71.

1. Overview of Nam

Nam is directed to a semiconductor device that includes a stack of alternating first interlayer insulating layers and gate electrodes on a substrate. Ex. 1006 ¶ 5. Figure 7 is reproduced below.

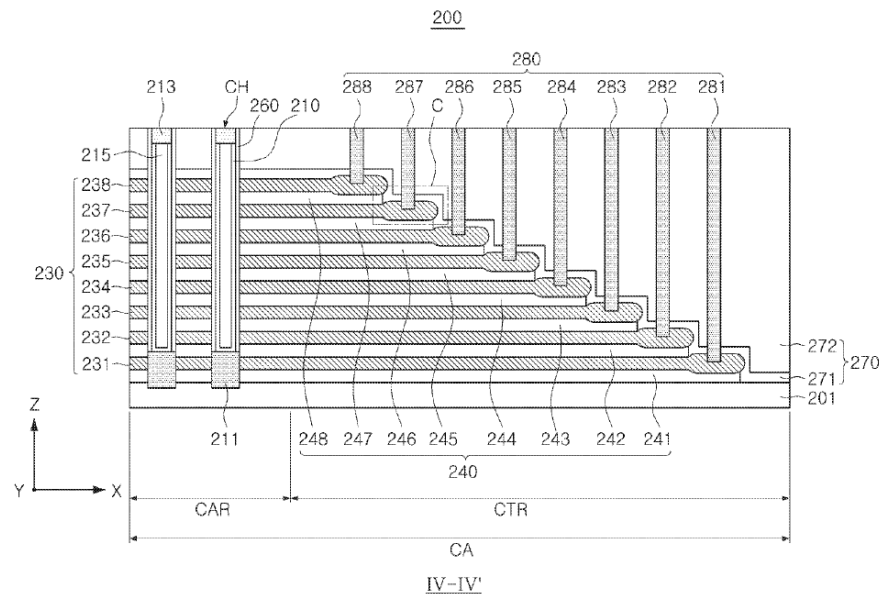


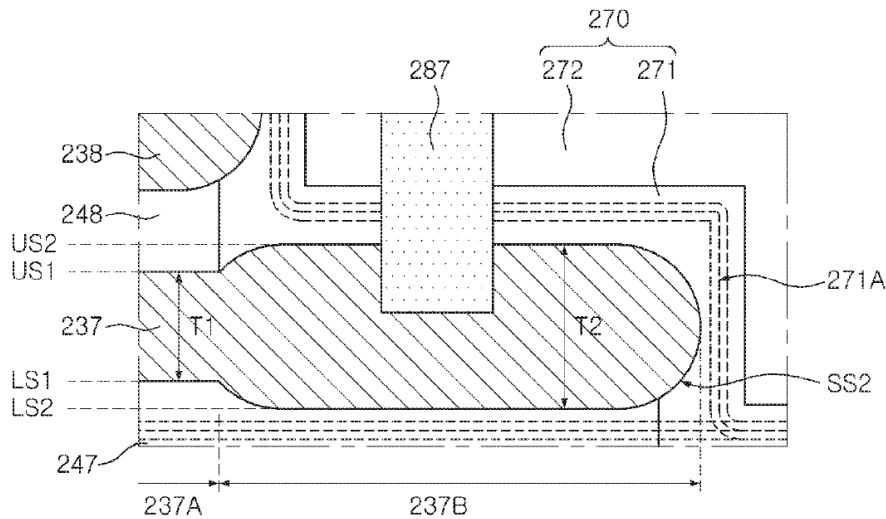
FIG. 7

Figure 7 is a schematic view of a memory device according to an embodiment described in Nam. *Id.* ¶ 15. Memory device 200 includes cell array region CAR and contact region CTR in cell region CR. *Id.* ¶ 62. A plurality of cell channel structures CH are disposed in cell array region CAR. *Id.* Cell channel structure CH includes epitaxial layer 211 connected

⁶ We do not reach the parties' allegations regarding a motivation to modify Kim with a reasonable expectation of success. Pet. 46–53; PO Resp. 39–49/

to substrate 201, channel layer 210, bit line pad 213, embedded insulating layer 215, and gate insulating layer 260. *Id.* A plurality of gate electrode layers 231 to 238 (collectively, gate electrode layers 230) are connected to a plurality of contacts 281 to 288 (collectively, contacts 280) in contact region CTR. *Id.* ¶ 63. Gate electrodes 230 extend in a first direction (X-axis direction), while forming a pair with one of a plurality of insulating layers 241 to 248 (collectively, insulating layers 240) adjacent thereto in a stack direction (Z-axis direction), respectively, to form a plurality of pad regions. *Id.* Each of gate electrode layers 230 have a relatively greater thickness in the pad region. *Id.* ¶ 64.

Figure 8A is reproduced below.



C
FIG. 8A

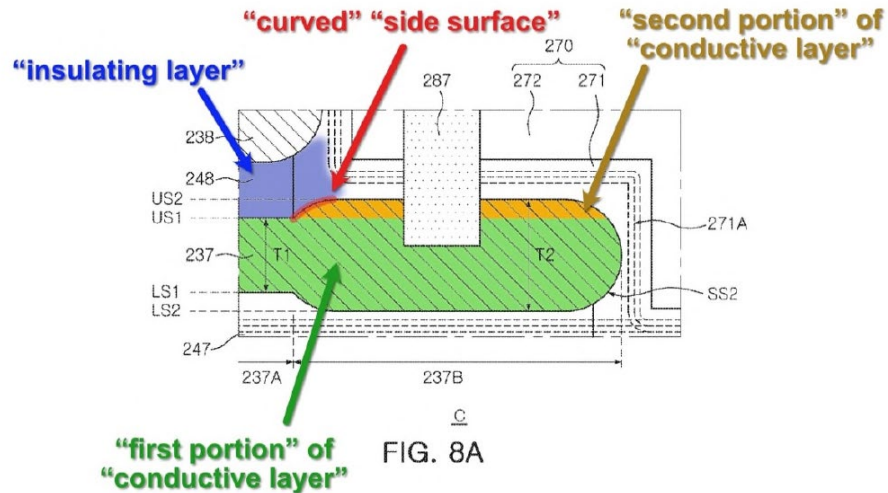
Figure 8A is an enlarged view of region C of Figure 7. Ex. 1006 ¶ 16. Gate electrode layer 237 includes first region 237A and second region 237B. *Id.* ¶ 65. Second region 237B is provided as a pad region with thickness T2 that is greater than thickness T1 of first region 237A. *Id.* Upper surface US2 of second region 237B is disposed to be higher than upper surface US1 of first

region 237A, and lower surface LS2 of second region 237B is disposed to be lower than lower surface LS1 of first region 237A. *Id.* Lateral surface SS2 of second region 237B protrudes outwardly therefrom in the first direction (X-axis direction). *Id.* ¶ 66. Lateral surface SS2 may be convex or have a bull nose shape. *Id.*

2. Claim 19

Claim 19 depends from, and includes all of the limitations of, claim 17. Ex. 1001, 16:8–14. Petitioner contends that Nam teaches or discloses all of the limitations of claim 17. Pet. 56–69. For example, with respect to the “a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer” limitation of claim 17, Petitioner contends that “Nam explains that its device ‘includes a stack of alternating first interlayer insulating layers and gate electrode layers on a substrate’” such as that shown in Nam’s Figure 7, where gate electrode layers 230 (formed from a conductive material such as metal) are alternately arranged to form a pair with one of insulating layers 240 (formed of silicon oxide) adjacent thereto in the Z-axis direction. Pet. 59–60 (citing Ex. 1006 ¶¶ 5, 63, 81, 94). Petitioner contends that first interlayer insulating layer 271 (also made from silicon oxide) is formed adjacent to insulating layers 240 and surrounds the ends of gate electrode layers 230. *Id.* at 60 (citing Ex. 1006 ¶ 98). Petitioner contends that “[a] POSITA would have considered both Nam’s insulating layer 240 and the adjacent insulating layer 271 to be the claimed ‘insulating layer’” because it “is not only formed from the same material as layer 240, but is used to define the shape of Nam’s pads.” *Id.* (citing Ex. 1003 ¶¶ 279–289) (emphases omitted).

Petitioner relies on an annotated version of Nam's Figure 8A, reproduced below, to illustrate its contentions regarding the "wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer" limitation of claim 17.



Annotated Figure 8A is an enlarged view of region C of Figure 7, with Petitioner's added blue shading to insulating layer 248 and part of interlayer insulating layer 271 labeled "insulating layer," orange shading to the portion of second region 237B between upper surface US1 of first region 237A and upper surface US2 of second region 237B of gate electrode layer 237 labeled "second portion' of 'conductive layer,'" green shading to the remainder of gate electrode layer 237 labeled "first portion' of 'conductive layer,'" and a red line tracing the curve of the pad where the orange shading meets the blue shading labeled "curved' 'side surface.'" Pet. 64–65; Ex. 1006 ¶ 16.

Petitioner contends:

Because Nam's contact pad is formed within and at the "interface" of its insulating layer 271, a POSITA would have understood that the "curved" "side surface" of Nam's "second portion" (the top part of its contact pad) is in "contact" with the "side surface" of its "insulating layer" (the portion of insulating layer 271 adjacent to the contact pad) as this limitation requires.

Pet. 67 (emphases omitted).

Patent Owner responds that “[t]he only purported ‘curved side surface’ Petitioner identifies in Nam is never ‘in contact with a side surface of the insulating layer,’ as required by claim 19.” PO Resp. 57. Instead, Patent Owner argues, “it contacts the bottom surface of what Petitioner identifies as the insulating layer.” *Id.* at 57–58 (citing Ex. 2023 ¶¶ 121–124). In that regard, Patent Owner argues that “[i]n Nam, the surface of any purported ‘insulating layer’ that includes some portion of layer 271 that is in contact with the purported ‘curved side surface’ is not nominally perpendicular to the lateral surface of a substrate, and thus is not a vertical surface.” *Id.* at 58. According to Patent Owner, “each purported ‘insulating layer’ in Nam that Petitioner identified as including some portion of layer 271 is a bottom or horizontal surface because it is nominally parallel to a lateral surface of a substrate.” *Id.* at 58–59.

We disagree with Patent Owner. As set forth above, we determine that “side surface” encompasses any outer surface of the structure. *See* II.B.A, *supra*. Petitioner’s annotated version of Nam’s Figure 8A illustrates that the curved surface portion of insulating layer 271 is adjacent to the contact pad (Petitioner’s identified “second portion of the conductive layer”) and is in contact with the “curved side surface” of the “second portion of the conductive layer.” *See* Pet. 67; Ex. 1006, Fig. 8A; Ex. 1003 ¶ 326. Accordingly, Petitioner shows that Nam discloses a curved side surface “in contact with a side surface of the insulating layer” as required by claim 19. Our conclusion is the same if the insulating layer comprises both Nam’s layer 248 (one of Nam’s layer 240) and the adjacent portion of layer 271. *See* Pet. Reply 20–21; Ex. 1027 ¶ 72.

We reviewed Petitioner’s contentions for all of the elements of claim 19, including the elements of claim 17 from which claim 19 depends, and Patent Owner’s arguments in response, and are persuaded, on this record, that Petitioner’s discussion of the particular structures Nam and the explanations in the Lee Declarations establish by a preponderance of the evidence that claim 19 would have been obvious over the teachings of Nam. *See* Pet. 56–71.

E. Asserted Obviousness over Lee and Park

Petitioner contends that claim 19 would have been obvious over the combined teachings of Lee and Park. Pet. 72–89.

1. Overview of Lee

Lee relates “to a semiconductor device capable of easily forming a pad portion and a method of manufacturing the same.” Ex. 1007 ¶ 8. Lee’s Figure 1A is reproduced below.

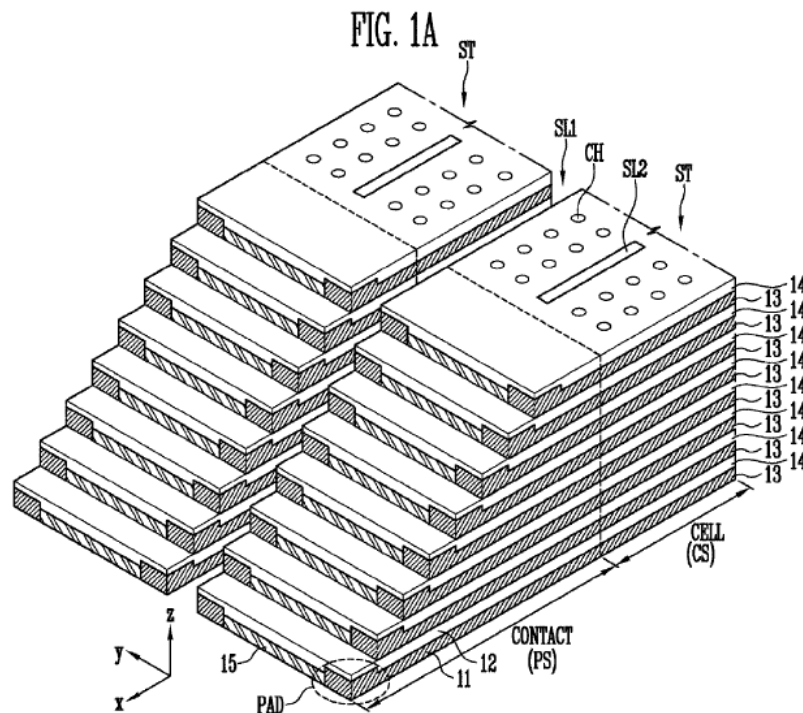


Figure 1A is a perspective view of the structure of a semiconductor device described in Lee. *Id.* ¶ 11. The semiconductor device includes cell region CELL and contact region CONTACT defined in a substrate (not shown). *Id.* ¶ 20. Stacked structures ST include conductive layers 11, 13 and insulating layers 12, 14 that are formed alternately with each other on the substrate. *Id.* First slit SL1 separates neighboring stacked structures ST from each other. *Id.* An end of stacked structures ST is patterned stepwise, with each step including at least one conductive layer 11 or 13 and at least one insulating layer 12 or 14. *Id.* ¶ 21. Stacked structure ST also includes pad structure PS located in contact region CONTACT, and cell structure CS located in cell region CELL. *Id.* ¶ 22. Pad structure PS includes first conductive layers 11 and first insulating layers 12 that are alternately formed in contact region CONTACT, with an end of pad structure PS being patterned stepwise. *Id.* ¶ 23. Pad portions PAD are defined as portions of first conductive layers 11 that are exposed along the stepped end of pad structures PS. *Id.* Pad structures PS further include sacrificial layers 15 that are coupled to first conductive layers 11. Ex. 1007 ¶ 24. Lee teaches that, for example, first conductive layers 11 are stacked on side walls along the z-axis of pad structure PS exposed through first slit SL1, i.e., in the side regions thereof. *Id.* Sacrificial layers 15 are stacked along the z-axis in a central region of pad structure PS. *Id.* Lee further teaches that pad portion PAD may have a greater thickness than other unexposed portions of first conductive layer 11, and may have a greater thickness than second conductive layer 13 and sacrificial layer 15, such that “the thickness of the pad portion PAD may be selectively increased without increasing the height of the stacked structure ST.” *Id.* ¶ 27.

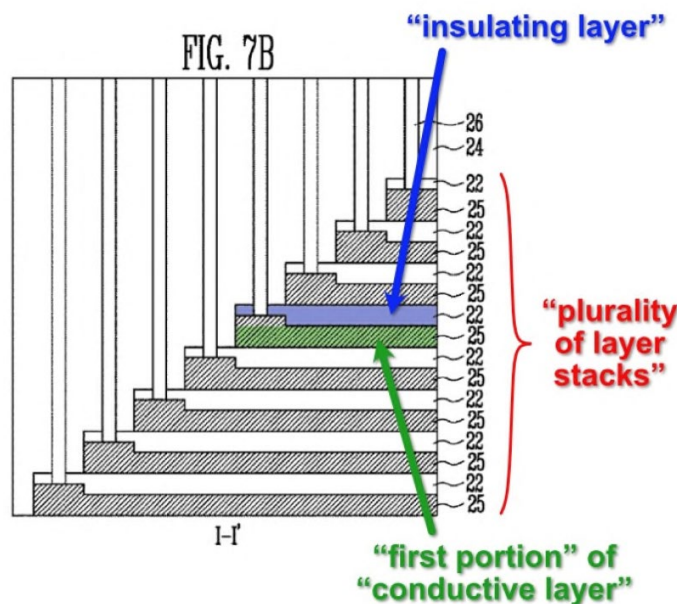
Figure 5 is a partial cross-sectional view of a connection region of a vertical semiconductor device described in Park. Ex. 1007, 2:11–13. Vertical semiconductor device 300 includes a stepped conductive structure in which interlayer insulating layer patterns 12a–12f and conductive layer patterns 22a–22f are repeatedly stacked on substrate 10 in a vertical direction. *Id.* at 6:7–11. Each of interlayer insulating layer patterns 12a–12f include recessed portion 27 recessed from a side wall of each of conductive layer patterns 22a–22f when recessed portion 27 is formed. *Id.* at 6:22–25. Park teaches that “[i]t may be advantageous to prevent a short circuit between the conductive layer patterns 22a through 22f when the recessed portion 27 is formed.” *Id.* at 6:25–28.

Vertical structure VCP including channel layer 20 is formed in hole 18 through interlayer insulating layer patterns 12a–12f and conductive layer patterns 22a–22f. Ex. 1008, 6:29–34. Each of conductive layer patterns 22a–22f has a pad region PAR in which a contact is formed on at least one edge. *Id.* at 6:43–45. Pad region PAR includes raised pad portion 28 protruding from a surface of each of conductive layer patterns 22a–22f. *Id.* at 7:4–6. Raised pad portion 28 extends in a horizontal direction of one side of each of interlayer insulating layer patterns 12b–12f. *Id.* at 7:6–8. End 29a of raised pad portion 28 extends farther than interlayer insulating layer patterns 12b–12e formed at a lower portion. *Id.* at 7:8–11. Raised pad portion 28 may partially overlap conductive layer patterns 22b–22f formed at an upper portion due to recessed portion 27 and may occupy the entire portion exposed by conductive layer patterns 22b–22f formed at an upper portion. *Id.* at 7:11–16.

Ends 29a and 29b of raised pad portion 28 are rounded. Ex. 1008, 7:17–18. Park teaches that “raised pad portion 28 may prevent a short circuit between the adjacent conductive layer patterns 22a through 22f when the other end 29b is rounded adjacent to the adjacent conductive layer patterns 22a through 22f.” *Id.* at 7:18–22.

3. Claim 19

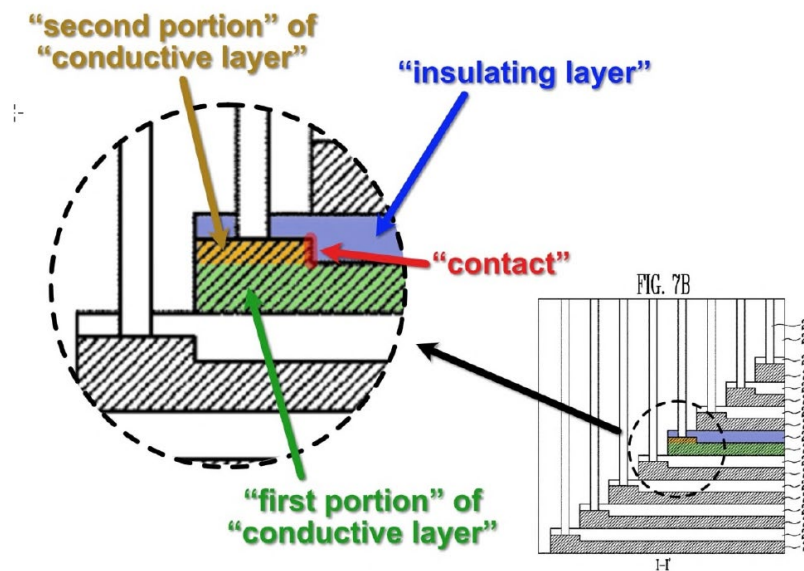
Claim 19 depends from, and includes all of the limitations of, claim 17. Ex. 1001, 16:8–14. Petitioner contends that Lee teaches most of the limitations of claim 17. Pet. 72–87. For example, Petitioner relies on the following annotated version of Lee Figure 7B to illustrate its contentions with respect to the “a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer” limitation of claim 17:



Annotated Figure 7B is a cross-sectional view of a portion of a semiconductor device during one step of the manufacturing process described in Lee, with Petitioner’s added annotations identifying second material layers 22 and conductive layers 25 as “plurality of stack layers,”

adding blue shading to insulating layer 22 labeled “insulating layer,” and adding green shading to a portion of conductive layer 25 labeled “‘first portion’ of ‘conductive layer.’” Pet. 77 (citing Ex. 1008, Fig. 7B); Ex. 1008 ¶ 13. Petitioner contends that the combination of insulating layer 22 and conductive layer 25 forming a step is the claimed “plurality of layer stacks,” and insulating layer 22 over the green portion of conductive layer 25 is the claimed “insulating layer disposed over a first portion of a conductive layer.” Pet. 76; Ex. 1003 ¶¶ 371–376.

Petitioner contends that Lee modified with Park’s teachings renders the “a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer” limitation of claim 17 obvious. Pet. 77. Petitioner identifies “pad portion PAD on the end of each of Lee’s conductive layer[s]” as “the claimed ‘second portion’ of a ‘conductive layer.’” *Id.* at 78 (citing Ex. 1007, Fig. 7B) (emphases omitted). Petitioner refers to the annotated version of Lee’s Figure 7B reproduced below to illustrate its other contentions with respect to this limitation.



Annotated Figure 7B is a cross-sectional view of a portion of a semiconductor device during one step of the manufacturing process described in Lee, with Petitioner's addition of a dotted circle around a portion of the stepped end pointing enlarged view of the circled area.

Pet. 79. Petitioner also added blue shading to insulating layer 22 labeled "insulating layer," green shading to a portion of conductive layer 25 labeled "'first portion' of 'conductive layer,'" orange shading to pad portion PAD of conductive layer 25 labeled "'second portion' of 'conductive layer,'" and a red line where pad portion PAD meets insulating layer 22 labeled "contact." *Id.*; Ex. 1003 ¶ 384. Relying on this illustration, Petitioner contends that "the 'side surface' of the 'second portion' of Lee's 'conductive layer' (Lee's pad portion PAD) is in 'contact' with 'a side surface of the insulating layer' (insulating layer 22 in Figure 7B)." Pet. 79 (emphases omitted).

Petitioner further contends that "a POSITA would have considered it obvious to make the 'side surface' of Lee's 'second portion of the conductive layer' 'curved' in view of Park's teachings." Pet. 82 (emphases omitted). Petitioner asserts that "each of Park's electrodes terminates with a 'pad region PAR' that includes a 'raised pad portion 28,'" and that, "[p]er Park, the 'end 79b' of this 'raised pad portion 78' may be 'rounded' to 'prevent a short circuit' between the pad and an 'adjacent . . . conductive layer pattern 72c.'" *Id.* at 82–83 (citing Ex. 1008, 7:4–16, 11:35–41).

Petitioner contends that a POSITA would have recognized that "each of Lee's pad portions PAD is physically proximate to the adjacent conductive layer immediately above the pad," which "creates a risk of short circuit in the event variances in the manufacturing process cause either the pad or the adjacent conductive layer to extend further than intended." *Id.* at 85 (citing Ex. 1007, Fig. 7B; Ex. 1003 ¶¶ 416–419). Petitioner further contends that

“[a] POSITA would have recognized that applying Park’s teachings and rounding the side of Lee’s pad portion PAD would have improved Lee—and limited the risk of short circuit—by increasing the minimum distance between the pad and the immediately adjacent conductive layer.” *Id.* at 85–86 (citing Ex. 1003 ¶ 420).

Patent Owner responds that Petitioner does not establish why a POSITA would have been motivated to modify Lee’s pad portions PAD with Park’s teachings to attain a “curved side surface” of the PAD. PO Resp. 61–67. Patent Owner argues that “Petitioner’s only identified motivation for ‘mak[ing] the end of Lee’s PAD facing its conductive layers rounded’ is to ‘limit the risk of short circuit,’” but “Lee already provides a method to achieve this without rounding the pads, by ensuring ‘sufficient distance . . . between the stacked conductive layers (pad portions) to prevent any deterioration.” *Id.* at 67 (citing Ex. 1007 ¶ 49). According to Patent Owner, “a POSITA would not be motivated to use Park’s teaching to round the pads in Lee to reduce short-circuit risk, as Lee already addresses that risk by other means.” *Id.*

We agree with Petitioner that a POSITA would have been motivated by Park’s teachings to round the end of Lee’s PAD that faces the conductive layers. Lee teaches:

The distance between conductive layers (pad portions) may decrease, and therefore a breakdown voltage of the conductive layers 25 may be deteriorated. However, according to an embodiment of the present invention, since an etch margin is ensured by the barrier layers 27 and 28, a sufficient distance may be ensured between the stacked conductive layers (pad portions) to prevent any deterioration.

Ex. 1007 ¶ 49.

Similarly, Park teaches:

The one end 29a and another end 29b of the raised pad portion 28 are rounded. The raised pad portion 28 may present a short circuit between the adjacent conductive layer patterns 22a through 22f when the other end 29b is rounded adjacent to the adjacent conductive layer patterns 22a through 22f.

Ex. 1008, 7:17–22.

Dr. Lee testifies that “a POSITA would have understood that applying Park’s teachings and rounding Lee’s pad portions PAD furthers” Lee’s goal of avoiding the risk that the breakdown voltage between the conductive layers may deteriorate when the PAD and the conductive layer are too close together. Ex. 1003 ¶¶ 421–423. And Dr. Lee explains that “when the pads are rounded, the distance between conductive layers would be increased avoiding the deterioration of the breakdown voltage.” *Id.* ¶ 423. We are persuaded that Dr. Lee sufficiently explains why a POSITA would have been motivated to round Lee’s pad portions PAD, in addition to the means Lee teaches to avoid deterioration of the breakdown voltage.

We are not persuaded, however, that Petitioner establishes that a POSITA would have had a reasonable expectation of success in modifying Lee in this way. Petitioner argues that “numerous prior art references identified this type of [curved] pad as acceptable for three-dimensional memory devices with staircase structures,” “Lee explains that the shape of its pad portion PAD is controlled via an ‘ion implantation process,’” and “a POSITA would have recognized that this type of process could be readily adapted to form a curved contact pad.” Pet. 86–87; Ex. 1003 ¶¶ 411–413, 426–429. Patent Owner, with supporting testimony from Dr. Giapis, argues Petitioner’s proposed modification of Lee

requires a POSITA to (1) start with an oxide-based insulating layer 22 as shown in Figure 5B of Lee, (2) introduce an oxidant gas into the adjacent openings, and (3) oxidize a surface that is already oxide-based to form a curved surface. A POSITA would not have been motivated to make these changes to Lee, as they are technically infeasible.

PO Resp. 63 (citing Ex. 2023 ¶¶ 128–142).

Dr. Giapis explains that in Park’s process, “an oxygen gas would be used to oxidize the silicon nitride or polysilicon,” but “introducing such an oxidant into the openings of Lee’s structure above will not promote further oxidation to the existing oxide layers 22” because “[a]ny sacrificial layer 21 had already been removed in the relevant region . . . so nothing remains to be oxidized.” Ex. 2023 ¶¶ 131–133. Dr. Giapis testifies:

It is not possible to further oxidize a solid oxide material with oxygen gas as in Park. That is why Park’s thermal oxidation process is performed on silicon nitride or polysilicon, which are not oxides to begin with but they can be oxidized to form silicon dioxide. *See, e.g.*, Ex. 2008 (Plummer) at 345–350. A POSITA would understand this and not expect the combination of Lee and Park to achieve any change in shape or any rounding in Lee’s Figure 5B.

Id. ¶ 133.

Dr. Lee responds that “a silicon oxide layer can (and often does) include extra silicon such that it is able to be further oxidized when exposed to an oxidant,” and that “silicon oxide films with non-stoichiometric amounts of oxygen (*i.e.*, SiO_x , where $0 < x < 2$) were both known and in routine use.” Ex. 1027 ¶ 81. Dr. Lee identifies references that indicate that non-stoichiometric and sub-stoichiometric SiO_2 can be formed using known deposition methods, and asserts that the prior art “discloses the use of non-stoichiometric silicon oxides as insulating layers in 3D memory,” and testifies that “a POSITA would have immediately recognized that it would

have been desirable to further oxidize the non-stoichiometric film to reduce the amount of extra silicon,” which would “not only produce a rounded landingpad but would allow the material’s uniformity to improve.” *Id.* ¶ 98. Dr. Lee, however, does not sufficiently establish that a POSITA would have known or expected that Lee’s silicon oxide film contained non-stoichiometric amounts of oxygen. *Id.* ¶¶ 82–88. That a POSITA would have recognized the desirability of further oxidizing a non-stoichiometric film alone is not sufficient to establish that a POSITA would have had a reasonable expectation of success in oxidizing Lee’s film as described in Park.

It is Petitioner’s burden to establish facts supporting its challenge that claim 19 would have been obvious over the combined teachings of Lee and Park by a preponderance of the evidence. 35 U.S.C. § 316(e). After considering Petitioner’s and Patent Owner’s positions, as well as their supporting evidence, we are not persuaded that Petitioner demonstrate that a POSITA would have been motivated to modify Lee with Park as proposed with a reasonable expectation of success. Accordingly, we determine that Petitioner does not demonstrate by a preponderance of the evidence that claim 19 would have been obvious over the combination of Lee and Park.

III. CONCLUSION⁷

After reviewing the parties’ arguments and weighing the evidence offered by both parties, we determine that Petitioner establishes by a

⁷ Should Patent Owner wish to pursue amendment of the challenged claim in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application

preponderance of the evidence that claim 19 of the '666 patent is unpatentable.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
19	103	Kim	19	
19	103	Nam	19	
19	103	Lee, Park		19
Overall Outcome			19	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner establishes by a preponderance of the evidence that claim 19 of the '666 patent is unpatentable; and

FUTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

IPR2025-00189
Patent 11,145,666 B2

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