

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case No. IPR2025-00190
U.S. Patent No. 11,568,941
Issue Date: January 31, 2023

Title: MEMORY INCLUDING A PLURALITY OF PORTIONS AND USED
FOR REDUCING PROGRAM DISTURBANCE AND PROGRAM METHOD
THEREOF

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,568,941
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

TABLE OF CONTENTS

	Page
I. INTRODUCTION	1
II. REQUIREMENTS FOR INTER PARTES REVIEW	3
A. Grounds for Standing (37 C.F.R. §42.104(a))	3
B. Notice of Lead and Backup Counsel and Service Information (37 C.F.R. §§42.8(b)(3-4), 41.10(a))	3
C. Notice of Real Parties-in-Interest (37 C.F.R. §42.8(b)(1))	4
D. Notice of Related Matters (37 C.F.R. §42.8(b)(2))	5
E. Fee for Inter Partes Review	6
F. Proof of Service	7
III. IDENTIFICATION OF GROUNDS AND CLAIMS BEING CHALLENGED (§42.104(b))	7
IV. INSTITUTION SHOULD BE GRANTED	7
A. There are No Grounds for §314 Discretionary Denial	8
1. Possibility of a Stay	8
2. Proximity of the Court’s Trial Date	8
3. Investment in the Parallel Proceeding	9
4. Issue Overlap	10
5. Party Overlap	10
6. Other Circumstances	10
B. Denial Under §325(d) Would Be Inappropriate	10
V. TECHNOLOGY BACKGROUND	11
VI. THE ’941 PATENT AND ITS PROSECUTION HISTORY	15
A. ’941 Patent Summary	15
B. ’941 Patent File History	22
VII. CLAIM CONSTRUCTION	22
VIII. LEVEL OF ORDINARY SKILL IN THE ART	22
IX. PRIOR ART DESCRIPTION	23

A.	U.S. Pub. 2008/0279008 (Ex. 1005, “Dong”).....	23
B.	U.S. Pub. 2018/0012667 (Ex. 1012, “Costa”).....	25
C.	U.S. Pub. 2019/0214405 (Ex. 1018, “Shirai”).....	27
X.	FOUNDATIONS 1 and 2 (DONG).....	28
A.	Claim 5	29
1.	[5.PRE] “A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first wordline to a kth wordline from bottom to top, the second portion formed above the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top, the program method comprising:”	34
2.	[5.A] “applying a first voltage to the [sic] to the first wordline to an (x–2)th wordline when an xth wordline is used to perform a program operation;”	38
3.	[5.B] “applying a second voltage to an (x–1)th wordline; and”	39
4.	[5.C] “applying a third voltage to an (x+1)th wordline;”	40
5.	[5.D] “wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.”	42
B.	Claim 6: “The program method of claim 5, further comprising:”	44
1.	[6.A] “applying a fourth voltage to an (x+2)th wordline to the mth wordline; and”	44
2.	[6.B] “wherein $x < (m-1)$.”	45
C.	Claim 7	46
1.	[7.PRE] “The program method of claim 5, wherein the memory further comprises a third portion formed above the second portion, the third portion comprises an (m+1)th wordline to an nth wordline from bottom to top, and the program method further comprises:”	46
2.	[7.A] “applying a fourth voltage to the (x+2)th wordline to the nth wordline;”	47
3.	[7.B] “wherein $m < n$, and $x < (n-1)$.”	49

D.	Claim 1:	50
1.	[1.PRE] “A memory comprising:”	51
2.	[1.A] “a first portion comprising an (m+1)th wordline to an nth wordline from bottom to top; and”	52
3.	[1.B] “a second portion formed below the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top; and”	53
4.	[1.C] “a controller configured to apply [various voltages]”	55
5.	[1.D] “a first voltage to an (x+2)th wordline to the nth wordline,”	55
6.	[1.E] “a second voltage to an (x+1)th wordline,”	57
7.	[1.F] “a third voltage to an (x−1)th wordline,”	58
8.	[1.G] “a fourth voltage to the (m+1)th wordline to an (x−2)th wordline, and”	60
9.	[1.H] “a fifth voltage to the (k+1)th wordline to the mth wordline when an xth wordline is used to perform a program operation;”	63
10.	[1.I] “wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.”	64
E.	Claim 3	66
1.	[3.A] “a third portion formed above the first portion and comprising a plurality of wordlines”	66
2.	[3.B] “wherein the controller is further configured to apply the first voltage to the plurality of wordlines when the xth wordline is used to perform the program operation.”	67
F.	Claim 11	68
1.	[11.PRE]	68
2.	[11.A] “applying a first voltage to an (x+2)th wordline to the nth wordline when an xth wordline is used to perform a program operation;”	69

3.	[11.B] “applying a second voltage to an (x+1)th wordline;”	69
4.	[11.C] “applying a third voltage to an (x-1)th wordline;”	69
5.	[11.D] “applying a fourth voltage to the (m+1)th wordline to an (x-2)th wordline; and”	69
6.	[11.E] “applying a fifth voltage to the (k+1)th wordline to the mth wordline;”	69
7.	[11.F] “wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.”	70
G.	Claim 13	70
1.	[13.PRE] “The program method of claim 11, wherein the memory further comprises a third portion formed above the first portion, the third portion comprises a plurality of wordlines, and the program method further comprises:”	70
2.	[13.A] “applying the first voltage to the plurality of wordlines of the third portion.”	70
XI.	GROUND 3 (DONG COMBINED WITH COSTA)	70
A.	Motivation to Combine Dong and Costa	70
B.	Claim 8: “The program method of claim 7, wherein: [A] the first voltage has a first level if the xth wordline is in the first portion; [B] the first voltage has a second level if the xth wordline is in the second portion; [C] the first voltage has a third level if the xth wordline is in the third portion; and [D] the first level is lower than the second level, and the second level is lower than the third level.”	74
C.	Claim 9: “The method of claim 5, wherein: [A] the first voltage has a first level if the xth wordline is in the first portion; [B] the first voltage has a second level if the xth wordline is in the second portion; and [C] the first level is lower than the second level.”	77
XII.	GROUND 4 (DONG COMBINED WITH SHIRAI)	77
A.	Motivation to Combine Dong and Shirai	77

B.	Claim 4: “The memory of claim 1, further comprising: an upper dummy wordline formed below the first portion; a lower dummy wordline formed above the second portion; and a joint oxide layer formed between the upper dummy wordline and the lower dummy wordline; wherein the memory has a two-deck structure.”	80
C.	Claim 10: “The program method of claim 5, wherein the memory further comprises: a lower dummy wordline formed above the first portion; an upper dummy wordline formed below the second portion; a joint oxide layer formed between the lower dummy wordline and the upper dummy wordline; wherein the memory has a two-deck structure.”	83
D.	Claim 14: “[PRE] The program method of claim 11, wherein the memory further comprises: [A] an upper dummy wordline formed below the first portion; [B] a lower dummy wordline formed above the second portion; and [C] a joint oxide layer formed between the upper dummy wordline and the lower dummy wordline; [D] wherein the memory has a two-deck structure.”	84
XIII.	SECONDARY CONSIDERATIONS	85
XIV.	CONCLUSION.....	85

LISTING OF EXHIBITS

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 11,568,941 to Song et al. (the “’941 Patent”)
1002	File History for U.S. Patent No. 11,568,941
1003	File History for U.S. Patent No. 11,195,590
1004	Declaration of David Kuan-Yu Liu, Ph.D. (“Liu”)
1005	U.S. Patent Publication No. 2008/0279008 (“Dong”)
1006	U.S. Patent Publication No. 2008/0159003 (“Dong II”)
1007	U.S. Patent Publication No. 2006/0250850 (“Lee”)
1008	U.S. Patent Publication No. 2018/0190498 (“Lee II”)
1009	Aritome, “NAND Flash Memory Technologies” (2016)
1010	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1012	U.S. Patent Publication No. 2018/0012667 (“Costa”)
1013	U.S. Patent Publication No. 2019/0102104 (“Righetti”)
1014	U.S. Patent Publication No. 2012/0003800 (“Lee III”)
1015	U.S. Patent No. 6,859,397 (“Lutze”)
1016	U.S. Patent No. 10,269,570 (“Lee IV”)
1017	U.S. Patent Publication No. 2012/0163096 (“Futatsuyama”)
1018	U.S. Patent Publication No. 2019/0214405 (“Shirai”)
1019	U.S. Patent No. 10,438,671 (“Chen”)

EXHBIT NO.	DESCRIPTION
1020	U.S. Patent No. 9,589,978 (“Yip”)
1021	<i>Curriculum Vitae</i> of David Kuan-Yu Liu, Ph.D.
1022	Yeh et al., “Z-Interference and Z-Disturbance in Vertical Gate-Type 3-D NAND,” IEEE Transactions on Electron Devices, Vol. 63, No. 3, March 2016, pp. 1047-1053
1023	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1024	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1025	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.’s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1026	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:24-cv-04223-RFL which has been consolidated with Case No. 3:23-cv-05792-RFL

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 1:	
[1.PRE]	A memory comprising:
[1.A]	a first portion comprising an (m+1)th wordline to an nth wordline from bottom to top; and
[1.B]	a second portion formed below the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top; and
[1.C]	a controller configured to apply
[1.D]	a first voltage to an (x+2)th wordline to the nth wordline,
[1.E]	a second voltage to an (x+1)th wordline,
[1.F]	a third voltage to an (x−1)th wordline,
[1.G]	a fourth voltage to the (m+1)th wordline to an (x−2)th wordline, and
[1.H]	a fifth voltage to the (k+1)th wordline to the mth wordline when an xth wordline is used to perform a program operation;
[1.I]	wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.
Claim 3:	
[3.PRE]	The memory of claim 1, further comprising
[3.A]	a third portion formed above the first portion and comprising a plurality of wordlines
[3.B]	wherein the controller is further configured to apply the first voltage to the plurality of wordlines when the xth wordline is used to perform the program operation.

Ref. #	Listing of Challenged Claims
Claim 4:	
[4]	The memory of claim 1, further comprising:
[4.A]	an upper dummy wordline formed below the first portion;
[4.B]	a lower dummy wordline formed above the second portion; and
[4.C]	a joint oxide layer formed between the upper dummy wordline and the lower dummy wordline;
[4.D]	wherein the memory has a two-deck structure.
Claim 5:	
[5.PRE]	A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first wordline to a kth wordline from bottom to top, the second portion formed above the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top, the program method comprising:
[5.A]	applying a first voltage to the to the first wordline to an (x-2)th wordline when an xth wordline is used to perform a program operation;
[5.B]	applying a second voltage to an (x-1)th wordline; and
[5.C]	applying a third voltage to an (x+1)th wordline;
[5.D]	wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.
Claim 6:	
[6.PRE]	The program method of claim 5, further comprising:
[6.A]	applying a fourth voltage to an (x+2)th wordline to the mth wordline; and
[6.B]	wherein $x < (m-1)$.

Ref. #	Listing of Challenged Claims
Claim 7:	
[7.PRE]	The program method of claim 5, wherein the memory further comprises a third portion formed above the second portion, the third portion comprises an (m+1)th wordline to an nth wordline from bottom to top, and the program method further comprises:
[7.A]	applying a fourth voltage to the (x+2)th wordline to the nth wordline;
[7.B]	wherein $m < n$, and $x < (n-1)$.
Claim 8:	
[8.PRE]	The program method of claim 7, wherein:
[8.A]	the first voltage has a first level if the xth wordline is in the first portion;
[8.B]	the first voltage has a second level if the xth wordline is in the second portion;
[8.C]	the first voltage has a third level if the xth wordline is in the third portion; and
[8.D]	the first level is lower than the second level, and the second level is lower than the third level.
Claim 9:	
[9.PRE]	The method of claim 5, wherein:
[9.A]	the first voltage has a first level if the xth wordline is in the first portion;
[9.B]	the first voltage has a second level if the xth wordline is in the second portion; and
[9.C]	the first level is lower than the second level.

Ref. #	Listing of Challenged Claims
Claim 10:	
[10.PRE]	The program method of claim 5, wherein the memory further comprises:
[10.A]	a lower dummy wordline formed above the first portion;
[10.B]	an upper dummy wordline formed below the second portion;
[10.C]	a joint oxide layer formed between the lower dummy wordline and the upper dummy wordline;
[10.D]	wherein the memory has a two-deck structure.
Claim 11:	
[11.PRE]	A program method of a memory, the memory comprising a first portion and a second portion formed below the first portion, the first portion comprising an (m+1)th wordline to an nth wordline from bottom to top, the second portion comprising a (k+1)th wordline to an mth wordline from bottom to top, the program method comprising:
[11.A]	applying a first voltage to an (x+2)th wordline to the nth wordline when an xth wordline is used to perform a program operation;
[11.B]	applying a second voltage to an (x+1)th wordline;
[11.C]	applying a third voltage to an (x-1)th wordline;
[11.D]	applying a fourth voltage to the (m+1)th wordline to an (x-2)th wordline; and
[11.E]	applying a fifth voltage to the (k+1)th wordline to the mth wordline;
[11.F]	wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

Ref. #	Listing of Challenged Claims
Claim 13:	
[13.PRE]	The program method of claim 11, wherein the memory further comprises a third portion formed above the first portion, the third portion comprises a plurality of wordlines, and the program method further comprises:
[13.A]	applying the first voltage to the plurality of wordlines of the third portion.
Claim 14:	
[14.PRE]	The program method of claim 11, wherein the memory further comprises:
[14.A]	an upper dummy wordline formed below the first portion;
[14.B]	a lower dummy wordline formed above the second portion; and
[14.C]	a joint oxide layer formed between the upper dummy wordline and the lower dummy wordline;
[14.C]	wherein the memory has a two-deck structure.

I. INTRODUCTION

Petitioner Micron Technology, Inc. (“Micron” or “Petitioner”) respectfully requests *Inter Partes* Review (“IPR”) of claims 1, 3-11, and 13-14 (the “Challenged Claims”) of U.S. Pat. 11,568,941 (the “’941 Patent”) assigned to Yangtze Memory Technologies Co., Ltd. (“YMTC,” “Patent Owner,” or “PO”). There is more than a reasonable likelihood Petitioner will prevail on at least one claim.

The ’941 Patent relates to programming memory cells in NAND flash memory devices. Ex. 1001, Title, 1:19-22, 3:4-8. Three-dimensional (“3D”) NAND flash memory cells are typically arranged in vertical memory strings where each cell is programmed (*i.e.*, written) by a different wordline.¹ *Id.*, 3:4-8. The ’941 Patent asserts that a solution for reducing “program disturbance” (*e.g.*, introducing errors on adjacent cells during programming) is needed. *Id.*, 1:39-41. It then presents (and claims) applying various combinations of voltages (*viz.*, “first voltage,” “second voltage,” “third voltage,” etc.) to specified wordlines during programming. *See, e.g., id.*, Figs. 1-13, 1:45-54. But the ’941 Patent never explains how its programming techniques mitigate program disturb, nor do the claims require any such effect. *See generally* Ex. 1001.

¹ For consistency, Petitioner uses the spelling “wordline,” instead of “word line” throughout.

By the earliest possible priority date in 2020, the claimed programming voltages and wordline groupings had already been disclosed more than a decade earlier in U.S. Pub. 2008/0279008 (Ex. 1005, “Dong”). Dong was not before the Examiner during prosecution, nor were the other prior art references relied on herein. *See generally* Exs. 1002 and 1003.

Ground 1 (anticipation) and 2 (obviousness): Dong anticipates and/or renders obvious claims 1, 3, 5-7, 11, and 13. Dong discloses programming techniques for memory “string[s]” in “NAND flash memory device[s]” (Dong, [0010]), and specifically concerns “reduc[ing] program disturb” during programming (*id.*, [0012]). To achieve this, Dong discloses applying specified voltages—*e.g.*, isolation voltages (V_{ISO}), pass voltages ($V_{\text{PASS-LOW}}$, $V_{\text{PASS-MEDIUM}}$, and $V_{\text{PASS-HIGH}}$), etc.—to particular wordlines during programming. *See, e.g.*, Dong, [0056]-[0060]. Dong Figs. 5a and 5g disclose the same combination of voltages and wordlines recited in claims 1, 3, 5-7, 11, and 13 and thus render those claims unpatentable. §X.

Ground 3: Dong combined with U.S. Pub. 2018/0012667 (Ex. 1012, “Costa”) renders claims 8-9 obvious. Dependent claims 8-9 require that the “first voltage” level increases as programming proceeds up the memory string. Dong is silent on this point, but Costa discloses the same concept and explains that doing so maintains uniform channel resistance and reduced program disturb during the verify phase of

programming, which is complementary to Dong. Costa, [0029]-[0030]. Thus, Dong combined with Costa renders claims 8-9 obvious. §XI.

Ground 4: Dong combined with U.S. Pub. 2019/0214405 (Ex. 1018, “Shirai”) renders dependent claims 4, 10, and 14 obvious. These claims require the memory to have “a two-deck structure.” Dong is silent on this point, but Shirai discloses the same claimed two-deck structure. See Shirai, Fig. 2. Using multiple decks in 3D NAND was common-place by 2020 due to its well-known benefit of increasing memory density by using longer memory strings. Applying this well-known technique to Dong renders claims 4, 10, and 14 obvious. §XII.

Petitioner requests the Board institute trial and find the Challenged Claims unpatentable.

II. REQUIREMENTS FOR INTER PARTES REVIEW

A. Grounds for Standing (37 C.F.R. §42.104(a))

Petitioner certifies the '941 Patent is available for IPR and no law bars Petitioner from requesting IPR of the Challenged Claims on the grounds herein.

B. Notice of Lead and Backup Counsel and Service Information (37 C.F.R. §§42.8(b)(3-4), 41.10(a))

Pursuant to 37 C.F.R. §§42.8(b)(3-4) and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

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PTABDocketJJL2@orrick.com, T61PTABDocket@orrick.com,
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37 C.F.R. §42.10(b), Petitioner attaches a Power of Attorney.

C. Notice of Real Parties-in-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Micron Technology, Inc., and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest. No other parties exercised or could have exercised control over this Petition. No other parties funded or directed this Petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

D. Notice of Related Matters (37 C.F.R. §42.8(b)(2))

According to USPTO records, the '941 Patent is currently assigned to Yangtze Memory Technologies Co., Ltd. On July 12, 2024, YMTC asserted the '941 Patent and U.S. Pat. Nos. 10,672,711, 11,450,604, 10,879,254, 10,886,291, 11,101,276, 11,145,666, 11,482,532, 10,879,164, 11,581,322, and 12,010,838 against Micron (the "YMTC2 case"). On August 21, 2024, the litigation was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) ("Co-Pending Litigation").

In addition to this Petition, Petitioner is filing (or has filed) IPR petitions for each asserted patent in the Co-Pending Litigation:

Patent	PTAB Proceeding	Wave
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	

Petition for *Inter Partes* Review of U.S. Pat. 11,568,941

Patent	PTAB Proceeding	Wave
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	
10,672,711	IPR2025-00117	Wave 3 Petitions
10,879,164	IPR2025-00118	
10,879,254	IPR2025-00034	
10,879,254	IPR2025-00119	
10,886,291	IPR2025-TBD	
11,101,276	IPR2025-00228	
11,145,666	IPR2025-00189	
11,450,604	IPR2025-00035	
11,482,532	IPR2025-TBD	
11,581,322	IPR2025-00191	
12,010,838	IPR2025-00229	

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a).

E. Fee for Inter Partes Review

The USPTO is authorized to charge the fee specified by 37 C.F.R. §42.15(a), and any other required fees, to Deposit Account No. 15-0665.

F. Proof of Service

Petitioner has attached proof of service of this Petition on the Patent Owner at the correspondence addresses of record for the '941 Patent.

III. IDENTIFICATION OF GROUNDS AND CLAIMS BEING CHALLENGED (§42.104(B))

This Petition assumes the earliest possible priority date (PCT filing date) of February 10, 2020 (the “Priority Date”).

Petitioner relies on three references: (1) Dong (Ex. 1005); (2) Costa (Ex. 1012); and (3) Shirai (Ex. 1018). All are prior art. *See* §IX.

Petitioner asserts the following grounds:

Ground 1: Dong anticipates claims 1, 3, 5-7, 11, and 13 under §102.

Ground 2: Dong renders obvious claims 1, 3, 5-7, 11, and 13 under §103.

Ground 3: Dong in combination with Costa renders obvious claims 8-9 under §103.

Ground 4: Dong in combination with Shirai renders obvious claims 4, 10, and 14 under §103.

The Declaration of Dr. David Liu (Ex. 1004, “Liu”) supports these grounds.

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR are met. The Board should institute IPR.

A. There are No Grounds for §314 Discretionary Denial

There is a pending district court action involving the '941 Patent. Petitioner submits it “presents compelling evidence of unpatentability” and the Board should not discretionarily deny institution. 6/21/22 Interim Procedure, 2, 4-5. Petitioner also notes the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively favor institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (PTAB Mar. 20, 2020) (precedential).

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24, 7 (PTAB June 16, 2020) (informative); *Fintiv*, 6-9, 12 (similar).

2. Proximity of the Court’s Trial Date

On September 18, 2024, the district court entered a scheduling order which set trial for June 15, 2026. *See* Ex. 1023. As a result, if IPR proceedings are instituted, they should be completed before the scheduled trial date. *See also* Ex. 1024 (statistics indicating average 48.9 months to reach trial in district). This strongly favors institution.

3. Investment in the Parallel Proceeding

Regarding the Co-Pending Litigation, to date, the parties and the district court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings and consolidation, little substantive progress has been made. *See* §II.D. Virtually no progress has been made on the Wave 3 patents (which includes the '941 Patent). The parties only recently completed the exchange of contentions for the Wave 3 patents (from the YMTC2 case) and have not taken any depositions in the entire Co-Pending Litigation. Fact discovery is in its infancy. No claim construction positions have been exchanged for the Wave 3 patents, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This favors institution. *See Sand Revolution*, 10-11.

The Board has explained institution is appropriate where “petitioner filed the petition expeditiously....” *Fintiv*, 11. Here, on July 12, 2024, PO asserted eleven Wave 3 patents against Petitioner, and later asserted 149 claims across those patents. Ex. 1025. Petitioner proceeded with diligence, starting the filing of eleven petitions approximately three months after being served with the YMTC2 complaint. Ex. 1026. This also strongly favors institution.

4. Issue Overlap

Should the Board institute, Micron stipulates it will not advance in District Court any ground asserted in this Petition. Micron submits this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found such stipulations favor institution. *Sand Revolution*, 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding.

6. Other Circumstances

Here, Petitioner submits its Petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also favors institution.

B. Denial Under §325(d) Would Be Inappropriate

The two-part *Advanced Bionics* framework weighs against §325(d) denial. As in *Advanced Bionics* Part I, none of the references in Petitioner's grounds (*viz.*, Dong, Costa, or Shirai) was before the Examiner during prosecution. *See generally* Exs. 1002 and 1003. Thus, there is no basis for a §325(d) discretionary denial and there is no need to consider Part II of the *Advanced Bionics* framework.

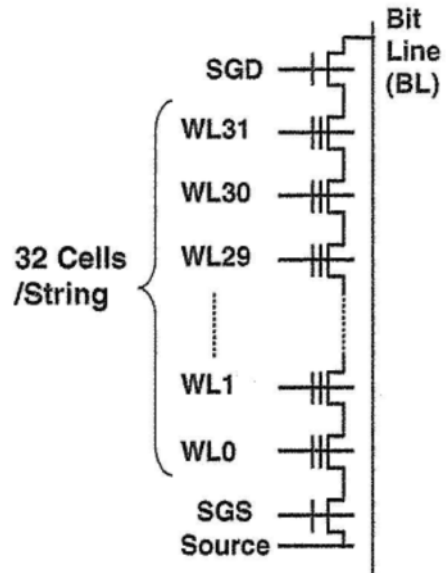
Regardless, at Part II, even if any disclosure similar to Dong, Costa, or Shirai was before the Examiner, the Examiner erred by failing to reject the claims considering such references. The record here is silent as to what, if any, substantive consideration the Examiner gave any references other than U.S. Pat. 10,269,570 (Ex.

1016, “Lee IV”) and U.S. Pub. 2012/0163096 (Ex. 1017, “Futatsuyama”). Ex. 1002, 381. Even as to Lee IV and Futatsuyama, the Examiner’s entire analysis spanned one paragraph. *Id.* Accordingly, the record is not well-developed, which favors institution. *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8, 22-23 (factor (c)) (PTAB Dec. 15, 2017).

V. TECHNOLOGY BACKGROUND

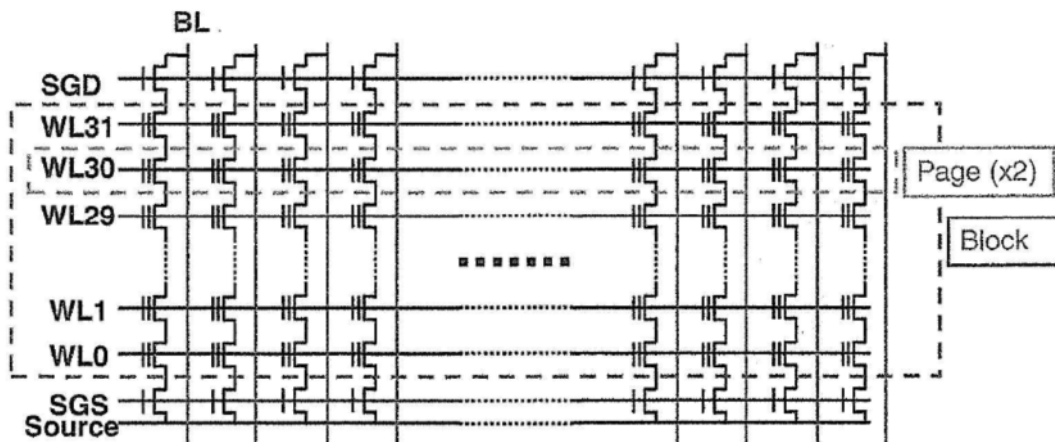
The ’941 Patent and prior art relate to programming NAND flash memory cells. NAND flash memory devices have existed for decades. “Flash memory” is a form of “non-volatile memory.” Ex. 1020 (“Yip”), 1:24-26. “Non-volatile memory ... can retain its data values ... without the application of power.” *Id.*, 1:26-28. NAND flash stores data in a “cell” formed from a transistor. Ex. 1009, 38-39; Ex. 1010, 109; Liu, ¶¶ 43-62.

NAND cells are arranged in “string[s]” with multiple cells “connected in series.” Ex. 1009, 38. The cells within each string are bracketed by “select transistors (SGD, SGS).” *Id.* The “SGD connects” at the string’s drain-side “to isolate it from a bit line (BL),” and the “SGS connects” at the string’s source-side “to isolate it from a source line (SL).” *Id.* Wordlines (“WL”) connect to each memory cell. *Id.*, 38-39.



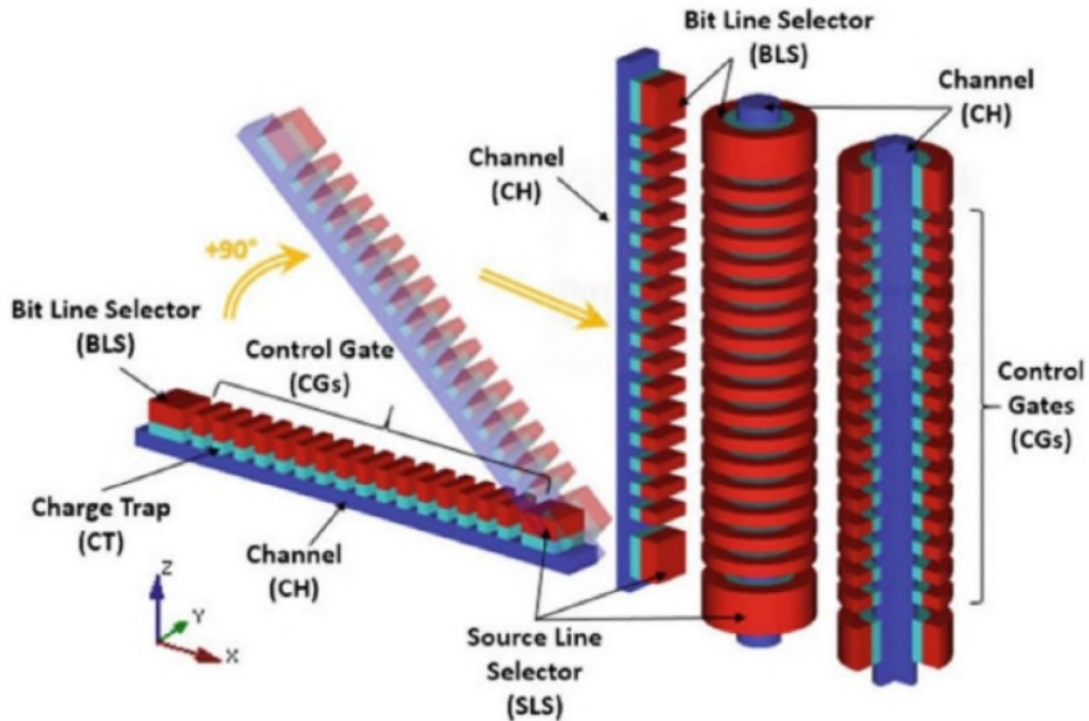
Id., 39.

NAND flash memory devices were originally formed as two-dimensional memory arrays. Ex. 1009, 58.

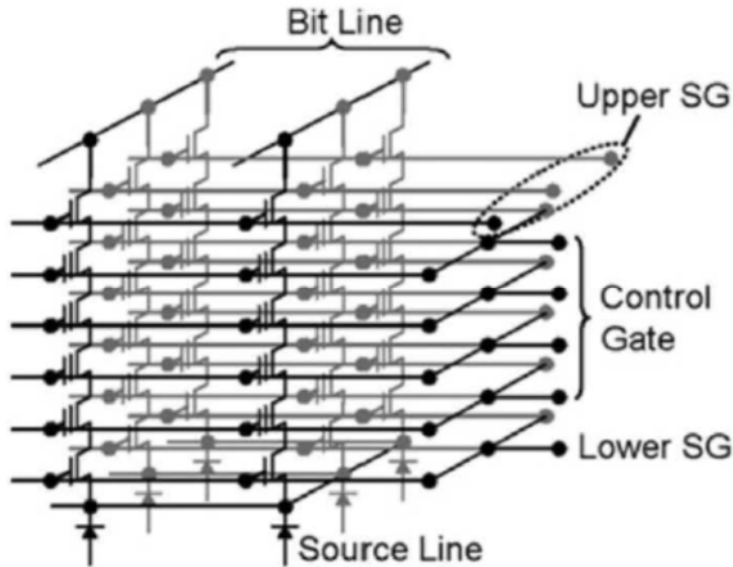


Id., 40. “[T]o further scale down the memory cell size,” “three-dimensional (3D) NAND flash cells” were developed. *Id.*, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block”

and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1011, 3.



Ex. 1010, 122. Multiple such vertical channels are then repeated in a three-dimensional array:



Ex. 1009, 296. Thus, there are many similarities between 2D and 3D NAND flash memory devices, including the techniques and algorithms used to program memory cells. See Liu, ¶¶ 49-56.

One important aspect of NAND flash memory is “programming,” which refers to “saving” or “writing” data to a memory cell. Liu, ¶ 54. To program a particular NAND memory cell in a memory string, a “high-voltage V_{pgm} ” is applied to the wordline connected to the cell—known as the “selected” wordline—while “keeping” the string’s bit line at “0V.” Ex. 1009, 44. This causes electron movement into the cell and sets the cell’s threshold voltage to a value within a specific range. *Id.*, 45. Because the selected wordline also is connected to cells in other strings, an “inhibit” voltage is applied to these strings’ bit lines to prevent undesired programming. *Id.*, 46. A lower “ V_{pass} ” voltage is also applied to all unselected wordlines. *Id.*, 44-46; Liu, ¶ 57-59.

Due to the close proximity of memory cells—and the application of these various different voltages—NAND is subject to a “phenomenon” known as “[p]rogram disturb.” Ex. 1009, 52. “Program disturb” involves “the threshold voltage ... of unselected cell[s]” undesirably “increas[ing] during program operation.” *Id.*, 52-53. This is problematic, as cells not selected for programming modification may nonetheless enter a different/unintended programmed state. *Id.* “Program disturb” can occur both in the NAND string that includes the programmed cell and in adjacent strings. *Id.* It was known that applied voltages can be tailored to either avoid or minimize program disturb. *Id.* For instance, increasing the V_{pass} voltage applied to unselected wordlines increases the so-called “boosting” voltage in adjacent NAND strings—a voltage that is induced in part by wordline voltage—thereby reducing program disturb in those strings. *Id.* But this also has the effect of increasing program disturb in the string that includes the programmed cell. *Id.* A lower V_{pass} has the opposite effect, reducing program disturb in the programmed cell’s string, but increasing it in adjacent strings. *Id.*; see also *Liu*, ¶¶ 59-62.

VI. THE ’941 PATENT AND ITS PROSECUTION HISTORY

A. ’941 Patent Summary

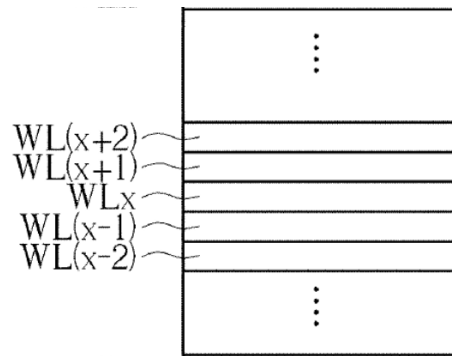
The ’941 Patent is titled “Memory Including a Plurality of Portions and Used for Reducing Program Disturbance and Program Method Thereof.” The ’941 specification identifies purported problems with “[p]rogram disturbance” that “lead

to a higher failure rate of programming a memory” as the number of memory cells in a string increases. Ex. 1001, 1:34-38; *see also id.* (discussing “pass voltage disturbance”); Liu, ¶¶ 65-74.

To mitigate these alleged problems, the ’941 Patent proposes applying various voltages to specified wordlines (which correspond to memory string cells) during programming. *See generally* Ex. 1001. None of the voltages is quantified. *Id.* And only in particular instances are relative voltage levels specified. *See, e.g., id.*, 1:66-67 (“The fifth voltage is lower than the fourth voltage.”). While the ’941 Patent asserts that “program disturbance and pass voltage disturbance may be reduced according to simulations and experiments,” it never presents nor discusses any such “simulations” or “experiments.” *Id.*, 6:39-43. Indeed, the ’941 Patent provides no explanation of how its programming techniques allegedly reduce program disturb. *See generally* Ex. 1001.

Before discussing programming voltages, it is helpful to understand how the ’941 Patent identifies wordlines. In the nomenclature of the ’941 Patent, the index “x” identifies the memory cell being programmed, and “WLx” refers to the corresponding wordline. *Id.*, Abstract, 3:9-11. Other wordlines are identified by their relative location to memory cell “x.” For example, WL(x+1) and WL(x-1) are the wordlines immediately above and below WLx, respectively. *See id.*, Figs. 1-5,

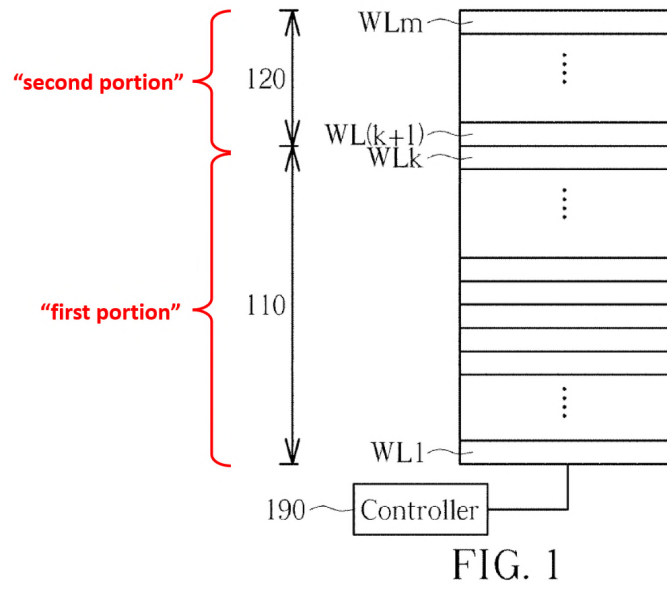
and 7-11. So, too, with the next adjacent wordlines denoted as $WL(x+2)$ and $WL(x-2)$, as shown in the Fig. 1 excerpt below. *Id.*



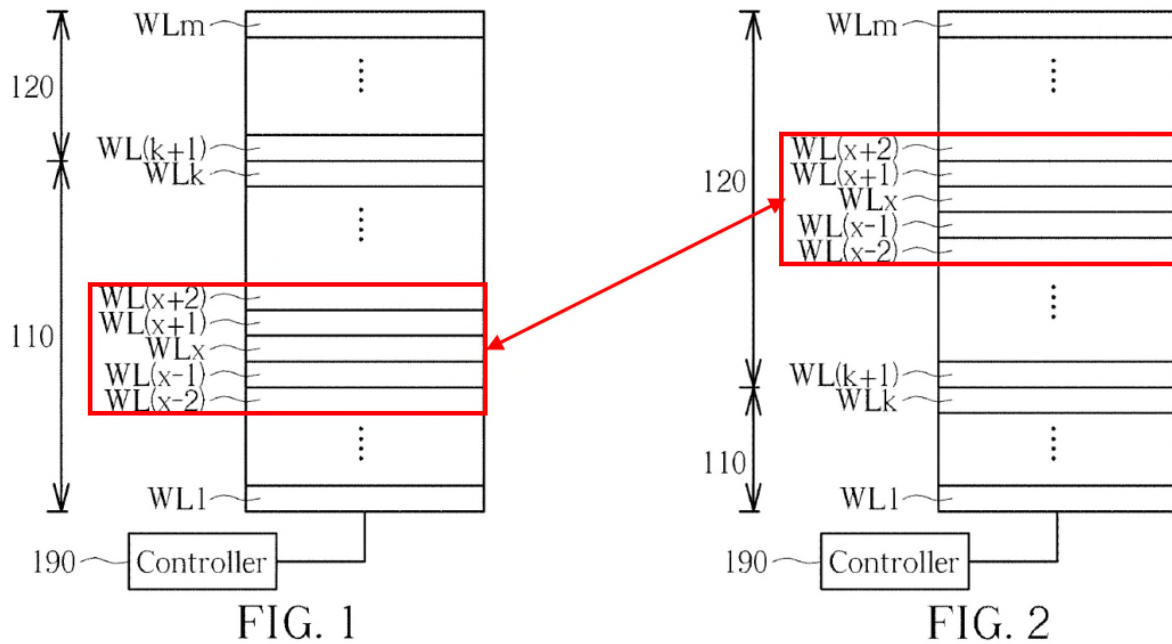
Id., Fig. 1 (excerpted).

The '941 patent uses another scheme to identify so-called “portions” of a memory string (and corresponding wordlines). A “portion” is always illustrated as a contiguous group of memory cells (and corresponding wordlines). *See id.*, Figs. 1-11. For purposes of identifying what “portion” a wordline belongs to, the '941 Patent uses the indices “k” and “m” (and in some embodiments “n”).² *Id.* For example, in the excerpted and annotated version of Fig. 1 below, the “first portion 110” “include[s] a first wordline WL_1 to a k th wordline” and “second portion 120” includes “wordline $WL(k+1)$ to an m th wordline WL_m .” *Id.*, 2:63-3:3.

² As before, an increment of “+1” identifies a wordline by its relative location to (viz., immediately above) “k,” “m,” etc. *See* Ex. 1001, Figs. 1-11.



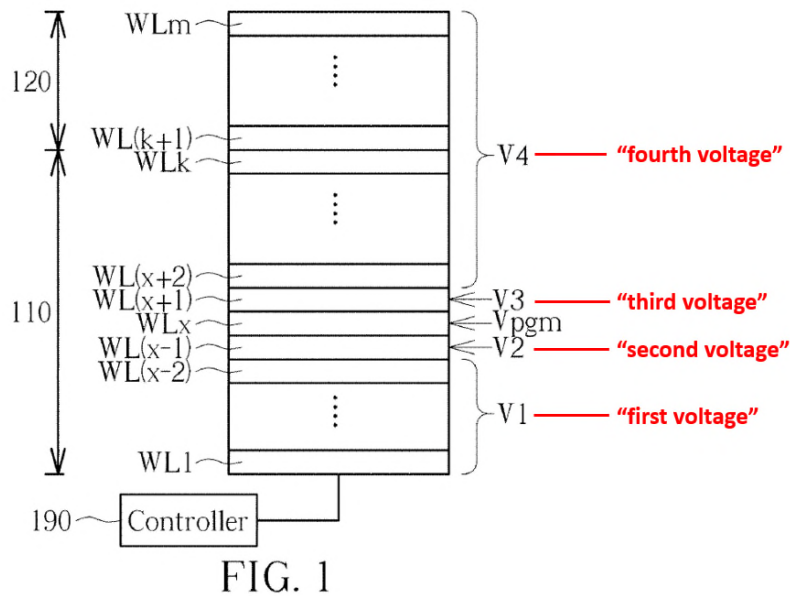
Id., Fig. 1 (excerpted and annotated). The '941 Patent combines these two numbering schemes to identify the portion in which a cell is being programmed. This can be seen, for example, by comparing Figs. 1 and 2 below where Fig. 2 is the same as Fig. 1 except "the xth wordline WLx is located in the second portion 120." *Id.*, 3:26-28.



Id., Figs. 1 and 2 (excerpted and annotated).

Returning now to programming voltages, the '941 Patent states that the voltage " V_{pgm} " is applied to the wordline for the cell being programmed. *Id.*, 3:9-11 ("When an xth wordline WL_x is used to perform[] a program operation, the controller 190 may apply a program voltage V_{pgm} to the xth wordline WL_x "); Figs. 1-5 and 7-11. All other wordline voltages are simply referred to as "first voltage V_1 ," "second voltage V_2 ," "third voltage V_3 ," etc. *See, e.g., id.*, 3:11-16. The '941 Patent does not specify any actual values (or ranges) for these voltages. And, with only limited exceptions, the '941 Patent is silent regarding the relationships (*e.g.*, whether the values can be the same, overlap, are mutually exclusive, etc.) between V_1 , V_2 , V_3 , etc.

Depending on the embodiment, the named voltages apply to one or more specified wordlines. *See id.*, Figs. 1-5 and 7-11. For example, as shown in Fig. 1 below, “first voltage V1” is applied from WL1 to WL(x-2), “second voltage V2” is applied to WL(x-1), Vpgm is applied to WLx, V3 is applies to WL(x+1), and V4 is applied from WL(x+2) to WLm. *Id.*, 3:11-21. The same is true for Fig. 2. *See id.*, 3:28-30, Fig. 2.



Id., Fig. 1 (annotated).

One other example—Fig. 8—is given here to show that the assignment of voltage labels V1, V2, V3,³ etc. is flexible. Unlike Fig. 1, in Fig. 8 the second voltage is above the cell being programmed and the third voltage is below the cell being programmed. *Id.*, 4:37-61, Fig. 8.

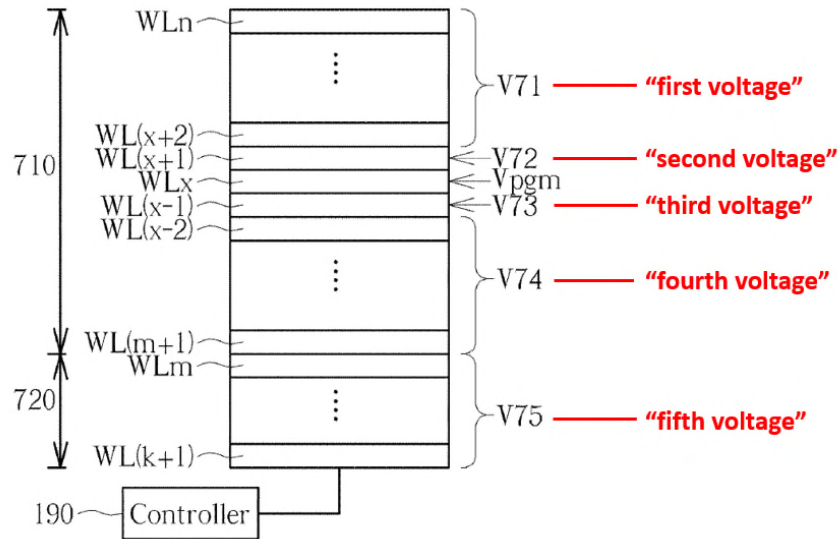


FIG. 8

Id., Fig. 8 (annotated). As noted previously, only in particular instances are relative voltage levels specified. Fig. 8 is one such example where the fifth voltage is less than the fourth voltage. *Id.*, 4:60-61.

³ Note that Figs. 7-11 use a slightly different naming convention for the voltages, calling them V71 (first voltage), V72 (second voltage), V73 (third voltage), etc.

Ex. 1001, 4:37-61. In other words, the prefix “7” is included in the voltage names.

B. '941 Patent File History

The '941 Patent file history is short as all Challenged Claims resulted from a first action allowance. Ex. 1002, 378-382. The stated reasons for allowance simply recited the majority of the claim language for each independent claim without identifying any particular novelty. *Id.*, 379-380.

The '941 Patent is a divisional of U.S. Pat. 11,195,590 (the "'590 Patent"). Ex. 1001, Cover. The file history for the parent '590 Patent is likewise short, as all its claims resulted from a first action allowance as well. Ex., 1003, 388-389, 417, and 424-425.

VII. CLAIM CONSTRUCTION

For purposes of this Petition, Petitioner submits the '941 Patent's claims do not require further construction and should receive their plain and ordinary meaning.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '941 patent would have had a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) NAND memory devices (including issues relating to the operation, *e.g.*, programming, of said devices), or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). Liu, ¶¶ 40-42. This POSITA would have been aware of and generally knowledgeable about NAND

memory's structure and fabrication, its component parts, how it operates, and how it is controlled. *Id.*, ¶ 41.

IX. PRIOR ART DESCRIPTION

A. U.S. Pub. 2008/0279008 (Ex. 1005, “Dong”)

Dong is titled “Non-volatile Storage with Boosting Using Channel Isolation Switching” and published November 13, 2008 (more than a decade before the '941 Priority Date), making it prior art under 35 U.S.C. §§102(a)(1) and (a)(2). Dong, Cover; *see generally* Liu, ¶¶ 81-86.

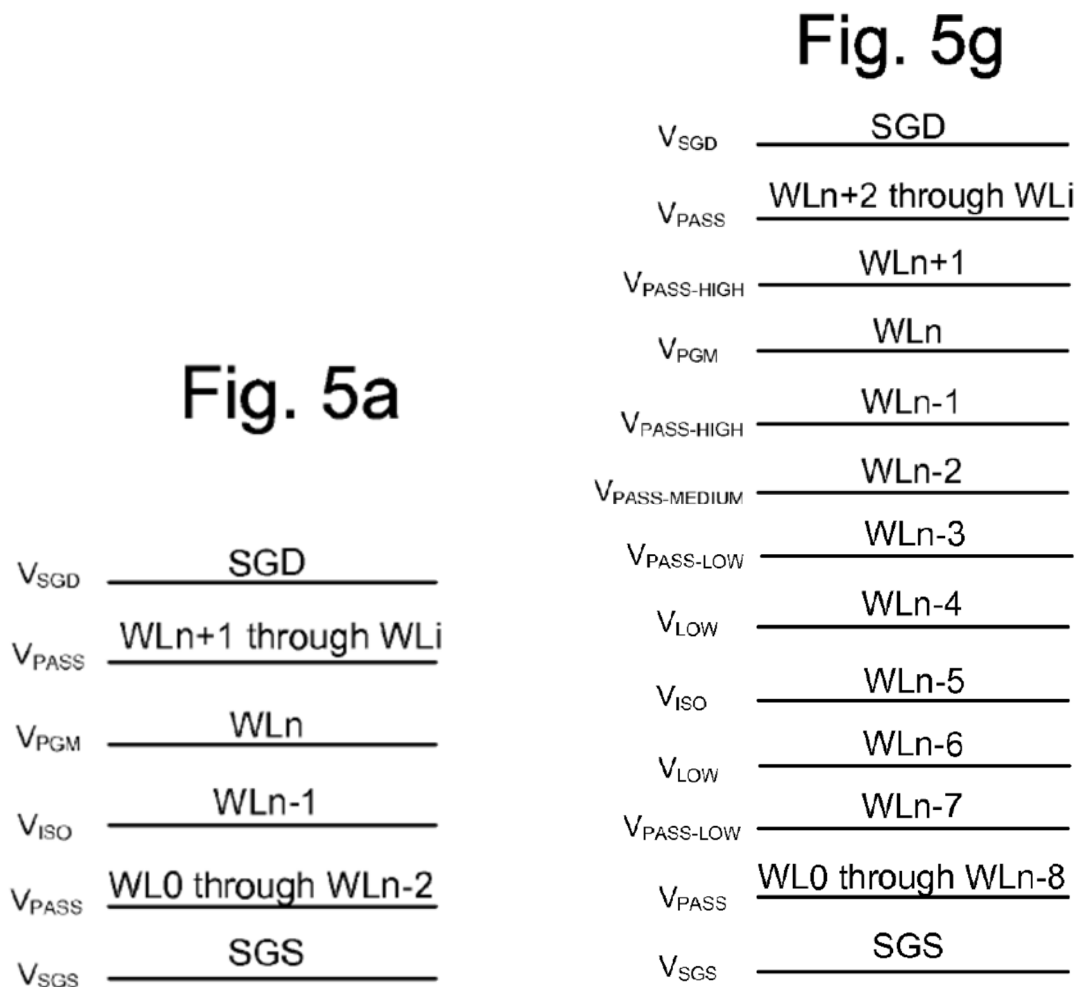
Dong relates to programming techniques for NAND flash memory strings to reduce program disturb. Dong, Abstract. Dong discloses that its programming techniques are applicable to both two-dimensional and three-dimensional memory arrays. Dong, [0095].

Dong explains that “[t]ypically, a program voltage V_{PGM} [is] applied to the control gate during a program operation ... as a series of pulses that increase in magnitude over time.” Dong, [0009]. “However, one issue which continues to be problematic is program disturb,” which “can occur at inhibited NAND strings during programming of other NAND strings, and sometimes at the programmed NAND string itself.” *Id.*, [0011]. “Program disturb occurs when the threshold voltage of an unselected non-volatile storage element is shifted due to programming of other non-volatile storage elements. Program disturb can occur on previously programmed

storage elements as well as erased storage elements that have not yet been programmed.” *Id.*

To combat problems associated with program disturb, Dong discloses a variety of programming algorithms and techniques that apply various program voltages (V_{PGM}), isolation voltages (V_{ISO}), pass voltages (V_{PASS}), etc. to the wordlines that control the memory strings. *See generally, e.g., id.*, Figs. 4-9. Some pass voltages used include $V_{\text{PASS-LOW}}$, $V_{\text{PASS-MEDIUM}}$, and $V_{\text{PASS-HIGH}}$. Dong, [0056]-[0060]; [0057] (“[M]ultiple V_{PASS} voltages can be used at the same time. ... Further, multiple V_{PASS} voltages can be used at both the drain and source sides.”).

Most relevant here are the embodiments of Figs. 5a (described at [0049]-[0051]) and 5g (described at [0058]-[0059]), reproduced below. Generally speaking, “FIGS. 5 a-h depict different examples of ... boosting modes [which] have been developed to combat program disturb. During programming of storage elements on a selected wordline, the boosting modes can be implemented by applying a set of voltages to unselected wordlines which are in communication with storage elements which are not currently being programmed. The storage elements which are being programmed are associated with selected NAND strings while other storage elements are associated with unselected NAND strings.” *Id.*, [0047].



Dong, Figs. 5a and 5g.

B. U.S. Pub. 2018/0012667 (Ex. 1012, “Costa”)

Costa is titled “Wordline Dependent Pass Voltages in Non-volatile Memory” and published January 11, 2018, making it prior art under 35 U.S.C. §§102(a)(1) and 102(a)(2). Costa, Cover; *see generally* Liu, ¶¶ 87-91.

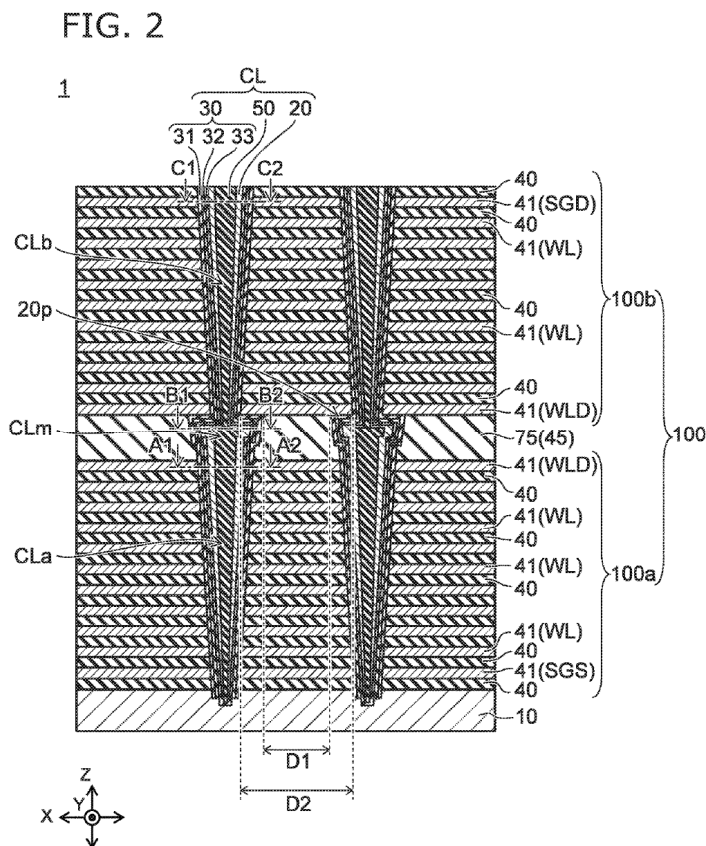
Costa discloses techniques for programming and reading NAND memory strings. Costa, Abstract. Costa’s techniques are applicable to both 2D and 3D

NAND memories. Costa, [0038], [0048], [0169]. Costa explains that as a memory string is programmed from the source end toward the drain, “channel resistance increases as each memory cell is programmed.” *Id.*, [0029]. Costa calls this undesirable phenomenon “back-pattern effect,” and explains that “later programmed memory cells may be programmed to higher levels which can cause a widening of the final threshold voltage distributions and potential read errors.” *Id.*, [0101].

To combat this, Costa discloses that “[a]s programming progresses ..., the pass voltage for at least a subset of the unselected memory cells that have already been subjected to programming may be increased.” Costa, Abstract; *see also id.*, [0028]-[0030], [0033] (describing use of “variable pass voltage”), [0104], Figs. 8-10, [0111] (“the second pass voltage $V_{read}+100$ is higher than the first read pass voltage V_{read} by 100 mV”). The reason for this is “to compensate for the increase in channel resistance from programming. In this manner, overprogramming the later programmed memory cells may be avoided.” *Id.*, [0104]. Costa provides a detailed explanation and specific examples in connection with Figs. 8-10. *See id.*, [0096], [0100]-[0134] (esp. [0110]-[0111] and [0114]-[0116]). Costa explains that “[t]his technique may reduce the effects of an increased channel resistance that occurs as more memory cells are programmed.” *Id.*, Abstract.

C. U.S. Pub. 2019/0214405 (Ex. 1018, “Shirai”)

Shirai published July 11, 2019 and is prior art under 35 U.S.C. §§102(a)(1) and 102(a)(2). Shirai, Cover. Shirai discloses a 3D NAND memory device comprised of multiple memory decks, which Shirai calls “stacked portions.” See, *e.g.*, Shirai, [0003]; Figs. 2 and 7-15; see generally Liu, ¶¶ 92-95. Fig. 2 “includes a first stacked portion 100a, a connection portion 45, and a second stacked portion 100b.” Shirai, [0030].



Id., Fig. 2. The connection portion 45 may be “made of the same material (for example, a silicon oxide) as the insulator 40.” *Id.*, [0045]; see also *id.*, [0031] (“The connection portion 45 includes a high dielectric layer 75,” which may comprise “a

hafnium oxide, a zirconium oxide, and an aluminum oxide.”). As shown above, although the memory cells are located in different decks, they are coupled in series to the same memory string. *Id.*, [0033]-[0042]; Liu, ¶ 95.

Shirai explains that memory decks 100a and 100b “may include the electrode layer 41 functioning as a dummy wordline WLD.” Shirai, [0032]. In lower deck 100a, “electrode layer 41 closest to the connection portion 45 functions as a dummy wordline WLD,” and in upper deck 100b, “electrode layer 41 closest to the connection portion 45 functions as a dummy wordline WLD.” *Id.*

X. GROUNDS 1 AND 2 (DONG)

Dong anticipates (Ground 1) and renders obvious (Ground 2) claims 1, 3, 5-7, 11, and 13. These claims can be broken into two groups as follows:

Group One: independent claim 5 and its dependent claims 6-7.

Group Two: independent claims 1 and 11, and their respective dependent claim 3 and 13.

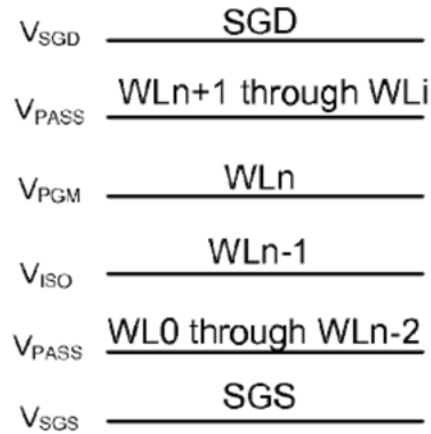
Different embodiments in Dong map to each group. In particular, Dong Fig. 5a maps to **Group One**. And Dong Fig. 5g maps to **Group Two**. The analysis below begins with independent claim 5 because it is broader than claim 1. *See generally* Liu, ¶¶ 98-102.

A. Claim 5

It is helpful at the outset to observe that claim 5 reads on '941 Patent Fig. 1 (among others). Liu, ¶ 103.

Dong anticipates and/or renders obvious claim 5. Liu, ¶¶ 104-136. The Dong embodiment that maps to claim 5 is Fig. 5a. Some preliminary comments about Dong Fig. 5a are provided here to facilitate the claim analysis that follows. Dong teaches that SGS is “the source-side select gate control line” and SGD is “the drain-side select gate control line.” Dong, [0048]. As reflected in Fig. 5a, the wordlines connected to memory cells that store data begin with the letters “WL” (for WordLine) and do not include SGS or SGD. Liu, ¶¶ 104-105. Most wordlines are identified by their relative location to wordline “n,” which is used for programming. Dong, [0049] (“a program voltage, V_{PGM} ... is applied to the selected wordline WL_n ”).

Fig. 5a



Dong, Fig. 5a. While the bottom/lowest wordline is identified as “WL0,” the top/uppermost wordline “WLi” is not assigned a number, and a POSITA would understand the index “i” is used to reflect that the specific number of wordlines (and the corresponding memory cells) is left open ended. Liu, ¶¶ 106-107. This is confirmed by U.S. Pat. 6,859,397 (Ex. 1015, “Lutze”), which Dong incorporates by reference. Dong, [0010]; Lutze, 2:11-18 (“[S]ome NAND strings will include eight memory cells, 16 memory cells, 32 memory cells, etc. The discussion herein is not limited to any particular number of memory cells in a NAND string.”). *See, e.g., Arbutus Biopharma Corp. v. Modernatx, Inc.*, 65 F.4th 656, 662-63 (Fed. Cir. 2023) (quoting *Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000)) (incorporated material is “effectively part of the host document as if [it] were explicitly contained therein.”).

At a minimum, it would have been obvious to a POSITA to utilize a 32-cell memory string given that (1) Dong Fig. 5 is not limited to any particular memory string length; (2) Dong expressly references Lutze which explicitly discloses 32-cell memory strings; and (3) Dong expressly discloses embodiments with 32 cell memory strings (Dong, [0090], [0108]). Liu, ¶¶ 108-111. Moreover, 32-cell (and larger) memory strings were well-known to POSITAs by the Priority Date and would have been obvious to use. Liu, ¶¶ 109-110; Ex. 1006 (“Dong II”), [0010], Fig. 1 (showing 32 wordlines); Costa [0093] (128 cell NAND string); Shirai, [0019] (“Any number of electrode layers 41 may be stacked.”); Ex. 1013 (“Righetti”), Fig. 6 (showing 74 wordlines); Futatsuyama, [0050] (memory string may have “8, 16, 32, 33, 34, 64, 66, 68 or 88” cells).

For illustrative purposes and to provide a concrete example, a 32-cell NAND string will be used. Liu, ¶¶ 111, 114-115; Dong, [0090], [0108] (disclosing memory strings with “16, 32, 64 or another number” of cells). As disclosed by Dong Fig. 10 (*e.g.*, step 1065 and 1075), programming continues sequentially until all memory cells in a string are programmed. Dong, Fig. 10 (steps 1065 and 1075), [0089]. When the fourth wordline is being programmed (which is WL3 because Dong Fig. 5a begins at WL0), the wordlines have the assignments shown below in annotated Fig. 5a. Liu, ¶ 114.

Fig. 5a

V_{SGD}	SGD
V_{PASS}	WL7 (WL_n+4) to WL31 (WL_i)
V_{PASS}	WL6 (WL_n+3)
V_{PASS}	WL5 (WL_n+2)
V_{PASS}	WL4 (WL_n+1)
V_{PGM}	WL3 (WL_n)
V_{ISO}	WL2 (WL_n-1)
V_{PASS}	WL1 (WL_n-2)
V_{PASS}	WL0 (WL_n-3)
V_{SGS}	SGS

Dong, Fig. 5a (annotated).

The further annotated version of Fig. 5a below with colors and labels added provides a holistic view of how Dong Fig. 5a maps to claim 5.

1. [5.PRE] “A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first wordline to a k th wordline from bottom to top, the second portion formed above the first portion and comprising a $(k+1)$ th wordline to an m th wordline from bottom to top, the program method comprising:”

To the extent the preamble is limiting, Dong discloses it. Liu, ¶¶ 116-127.

Dong discloses a *memory*.⁴ Dong, Fig. 12 (“memory device 1296,” “memory die 1298,” and “memory array 1100”); [0095] (“Memory device 1296 may include one or more memory die 1298. Memory die 1298 includes a two-dimensional array of storage elements 1100, control circuitry 1210, and read/write circuits 1265. In some embodiments, the array of storage elements can be three dimensional.”).

Substantially the entirety of Dong concerns *program method[s]* for a memory. See, e.g., *id.*, [0009]-[0010], [0048] (“A set of voltages which is applied to the control lines is also depicted. Programming can proceed in a programming sequence one wordline at a time”).

The claimed *first* and *second portion[s]* of the *memory* are defined by the claim itself: *the first portion compris[es] a first wordline to a k th wordline from bottom to top*; and *the second portion formed above the first portion and comprising a $(k+1)$ th wordline to an m th wordline from bottom to top*. Before

⁴ Claim language is set off using *red italics*.

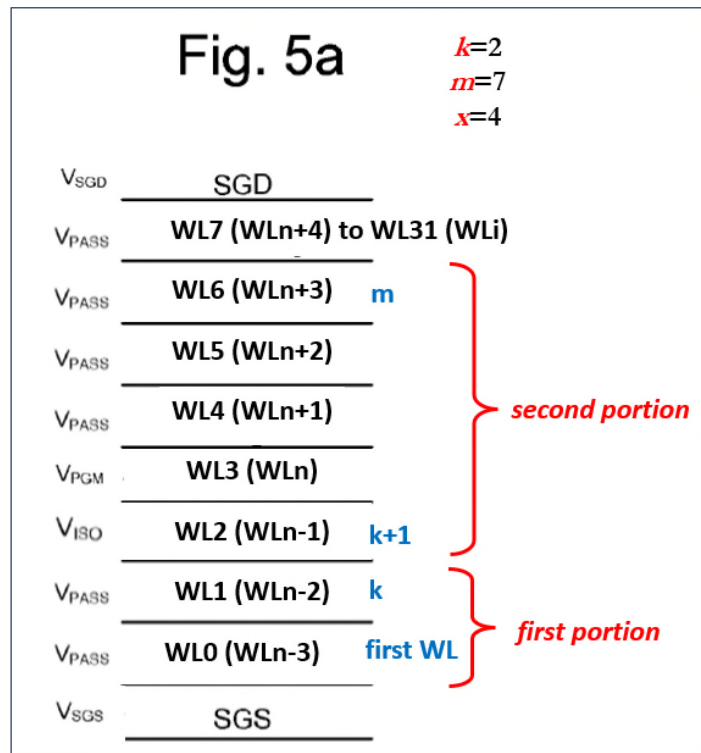
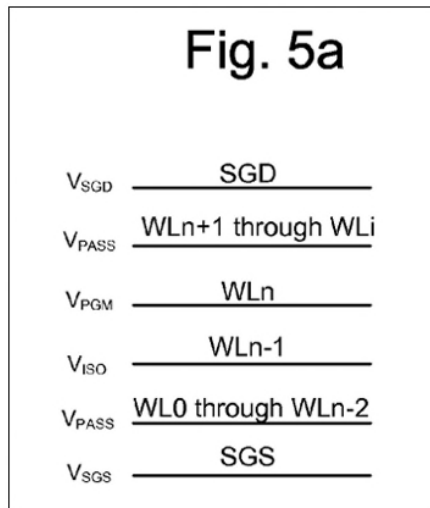
identifying the *first* and *second portion[s]* in Dong, it is helpful to discuss two points of nomenclature in the claim: (1) *bottom to top*; and (2) the variables *k* and *m*.

The '941 patent does not define the phrase *bottom to top*, but it was (and is) common in NAND flash memory devices to refer to the source end of a memory string as the “bottom,” and the drain end as the “top.” Liu, ¶¶ 112-113, 120. That common usage will be applied here. Regardless, to the extent *bottom to top* is interpreted to require vertical strings in a 3D NAND memory, Dong discloses its “array of storage elements can be three dimensional” and shows Fig. 5a in a vertical orientation which satisfies the claim. Dong, [0095]; Liu, ¶ 120.

Turning now to the terms *k* and *m*, the claim uses these terms as indices or variables for referencing a wordline location corresponding to a memory string cell. Liu, ¶¶ 121-123. Neither the term *k* nor *m* is a term of art. Liu, ¶ 121. There is nothing special about the claim’s selection of those variables, and other variables (*e.g.*, “a”, “b,” “g,” “r,” etc.) could have been selected instead without changing the meaning or substance of the claim. *Id.* A POSITA would understand the *(k+1)th wordline* refers to the wordline immediately above the wordline *k*, *i.e.*, closer to the drain. *Id.*, ¶ 122. Likewise, “k-1” would refer to the wordline immediately below the wordline *k*. *Id.* This is how the indexing scheme is described in the '941 patent. See, *e.g.*, Ex. 1001, Fig. 1. The same convention applies for identifying wordlines that are two wordlines away from a reference wordline (*e.g.*, the “k+2” wordline

would be two wordlines above, closer to the drain, than wordline **k**). *Id.* Likewise, the same indexing scheme applies when other variables (such as “x”) are used to identify the reference wordline. Liu, ¶ 122; Ex. 1001, Fig. 1. The only concrete parameters the claim places on **k** and **m** are that **k and m are positive integers, $1 < k < m$** . These conditions (and others) are discussed further for element [5.D] where the claim recites them. This discussion regarding variable applies generally anywhere other variables (such as **n** and **x**) are used in the Challenged Claims. Liu, ¶ 122.

Dong’s wordlines WL0 through WLn-2 (viz., WL1) in Fig. 5a below correspond to the claimed **first portion**. Liu, ¶¶ 124-126. And Dong’s wordlines WLn-1 (viz., WL2) through WLn+3 (WL6) in Fig. 5a correspond to the claimed **second portion**. Liu, ¶ 127. Similar to the ’941 patent’s use of the variable **x**, Dong uses the variable “n” to indicate relative wordline locations. Dong, [0049]; Fig. 5a (showing wordline “WLn-1” as one wordline below “WLn”). Unannotated and annotated versions of Fig. 5a are shown below to illustrate how “WL0 through WLn-2” and “WLn+1 through WLi” were expanded.



Dong, Fig. 5a (unannotated at left, annotated at right).

The **first portion** must include **a first wordline to a kth wordline from bottom to top**. Dong satisfies this. Liu, ¶¶ 124-126. Dong teaches that SGS is “the source-side select gate control line” and SGD is “the drain-side select gate control line.” Dong, [0048]. As reflected in Fig. 5a, the wordlines connected to memory cells that actually store data begin with the letter “WL” (for Wordline) and do not include SGS or SGD. Liu, ¶¶ 104-105. Thus, Dong’s wordline WL0 corresponds to the claimed **first wordline from bottom to top**. Liu, ¶¶ 107, 124. And Dong’s wordline WLn-2 (viz., WL1) corresponds to the claimed **kth wordline**. Liu, ¶ 124.

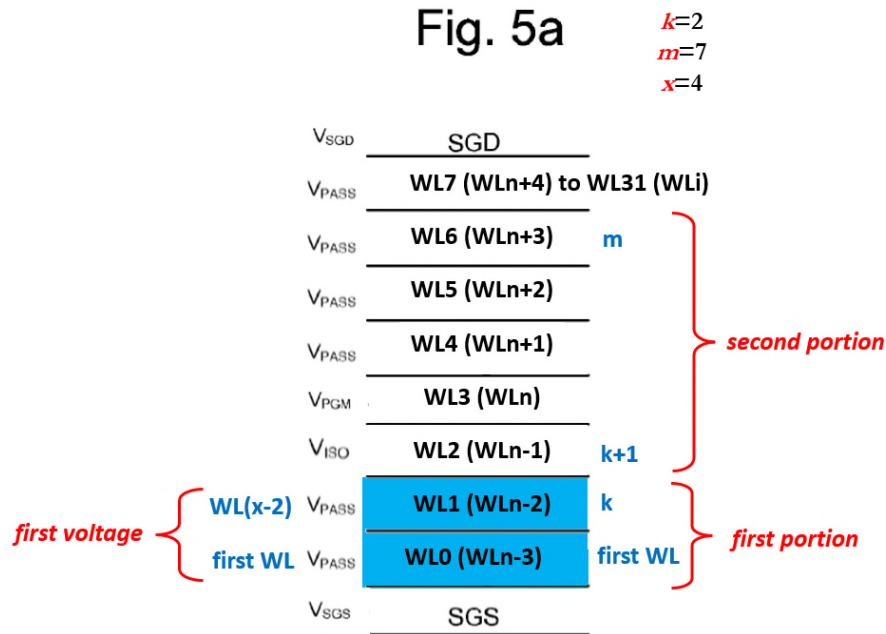
The **second portion** must be **formed above the first portion** and include **a (k+1)th wordline to an mth wordline from bottom to top**. Dong satisfies this. Liu, ¶ 127. Dong's wordline WLn-1 (viz., WL2) corresponds to the claimed **(k+1)th wordline**. *Id.* And Dong's wordline WLn+3 (viz., WL6) corresponds to the claimed **mth wordline** (which means **m=7** in the example being used). *Id.* Additionally, as is apparent from Fig. 5a, Dong's **second portion** (from WL2 to WL6) is **formed above the first portion** (WL0 to WLn-2). *Id.* Thus, Dong satisfies the preamble of claim 5.

2. [5.A] “applying a first voltage to the [sic] to the first wordline to an (x-2)th wordline when an xth wordline is used to perform a program operation;”

Dong satisfies element [5.A]. Liu, ¶¶ 128-130. To begin, the claim uses the variable **x** to identify the wordline being **used to perform a program operation**. The claimed **xth** wordline corresponds to the selected wordline WLn in Dong Fig. 5. Dong, [0049] (“a program voltage, V_{PGM}, which is applied to the selected wordline WLn”); *see also id.*, [0048] (“the selected wordline is WLn”).

When the **xth** wordline is used for programming, a **first voltage** is applied **to the first wordline to an (x-2)th wordline**. Dong satisfies this. Liu, ¶ 129. In Dong, because WLn is used for programming, a **first voltage** must be applied to the wordlines from WL0 (the **first wordline**) to WLn-2 (viz., WL1, the **(x-2)th wordline**). Dong does just this as shown in Fig. 5a below, by applying V_{PASS} to WL0

(the **first wordline**) through WL1 (viz., WLn-2, the **(x-2)th wordline**). Dong, Fig. 5a; Liu, ¶¶ 129-130.

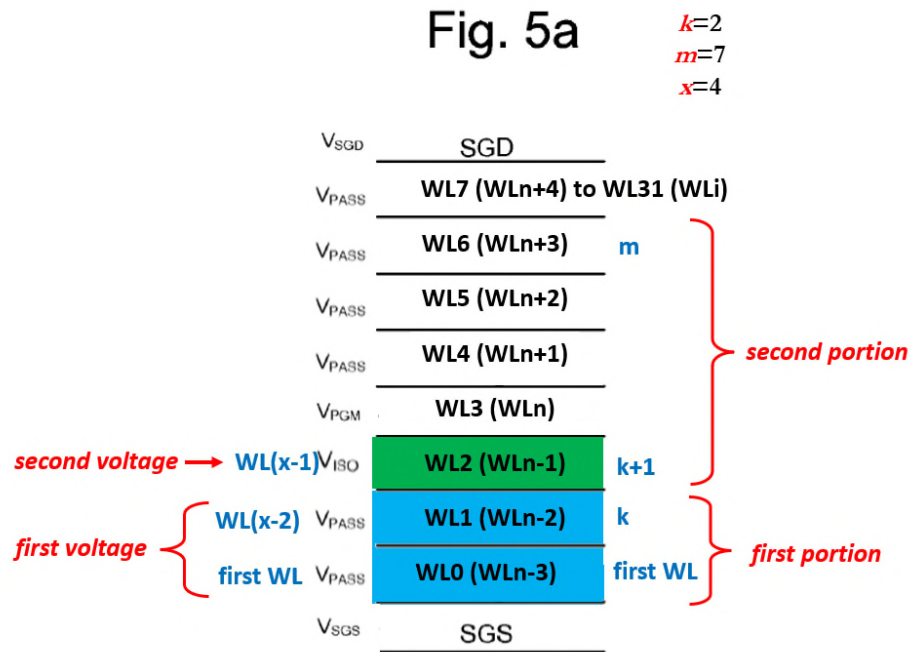


Dong, Fig. 5a (annotated). Dong explains that “a pass voltage, V_{PASS} , ... is applied to each of the unselected wordlines, WL0 through WLn-2.” Dong, [0049]. Neither the claim nor the ’941 patent specification require any particular voltage (or voltage range) for the claimed **first voltage**. See generally Ex. 1001. All that is required is that the same voltage (whatever voltage it is) be applied to the specified wordlines. Liu, ¶ 130. Thus, because, V_{pass} is applied to the requisite wordlines, Dong satisfies element [5.A].

3. [5.B] “applying a second voltage to an (x-1)th wordline; and”

Dong satisfies element [5.B]. Liu, ¶ 131. Dong discloses **applying a second voltage** [V_{ISO}] **to an (x-1)th wordline** [WLn-1], as shown below in Fig. 5a. Dong,

Fig. 5a, [0049] (“[A]n isolation voltage V_{ISO} ... is applied to $WLn-1$, the wordline which is adjacent to the selected wordline on the source side ... A low isolation voltage V_{ISO} , in a typical range of 0-4 V, is applied to the wordline which is adjacent to the selected wordline on the source side, in the example of FIG. 5 a.”). As previously explained, the ***(x-1)th wordline*** is the wordline immediately below the wordline being used for programming (*i.e.*, the wordline below ***x***). Thus, in Dong, the ***(x-1)th wordline*** is $WLn-1$ (*viz.*, $WL2$). Liu, ¶ 131.



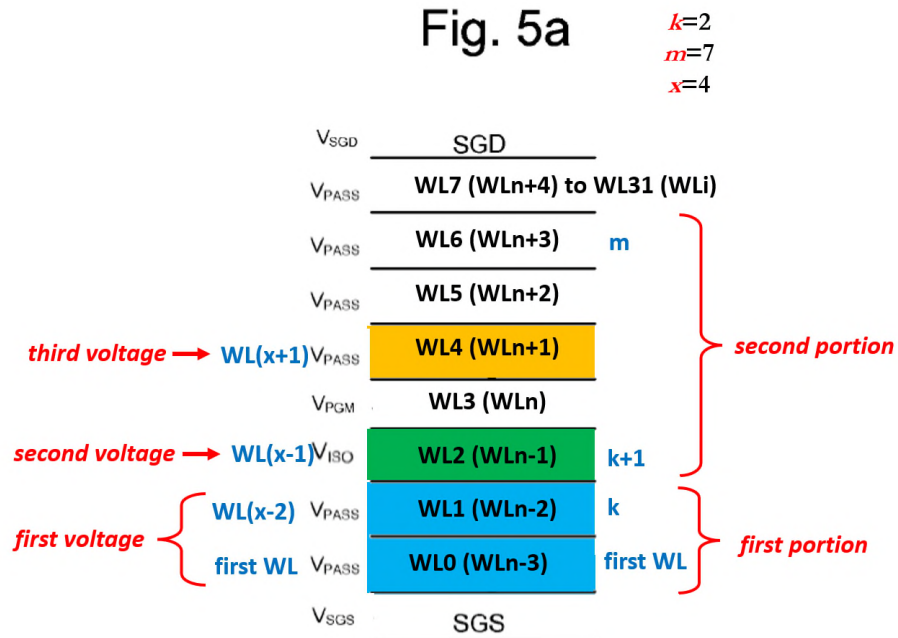
Dong, Fig. 5a (annotated). Thus, Dong satisfies element [5.B].

4. [5.C] “applying a third voltage to an (x+1)th wordline;”

Dong satisfies element [5.C]. Liu, ¶¶ 132-133. Dong discloses ***applying a third voltage*** [V_{PASS}] ***to an (x+1)th wordline*** [$WLn+1$], as shown below in Fig. 5a.

Dong, Fig. 5a, [0049] (“a pass voltage, V_{PASS} , ... is applied to each of the unselected

wordlines,” including “WL_{n+1}”); Liu, ¶ 132. As previously explained, the **(x+1)th wordline** is the wordline immediately above the wordline being used for programming (*i.e.*, the wordline above **x**). Thus, in Dong, the **(x+1)th wordline** is WL_{n+1} (WL4). Liu, ¶ 132.



Dong, Fig. 5a (annotated). Neither claim 5 nor the ’941 Patent specification requires that the claimed **third voltage** be different than the **first voltage**. See generally Ex. 1001; Liu, ¶ 133; *Affymetrix, Inc. v. Hyseq, Inc.*, 132 F. Supp. 2d 1212, 1228-29 (N.D. Cal. 2001). Indeed, the ’941 specification suggests otherwise. Ex. 1001, 6:43-46 (“by using a same voltage source to apply a voltage to wordlines of a same portion or wordlines of different portions, less voltage sources may be required”). And when the ’941 patent claims require different relative voltages, they expressly say so. For example, claim 1 states that **the fifth voltage is lower than the fourth voltage**. By

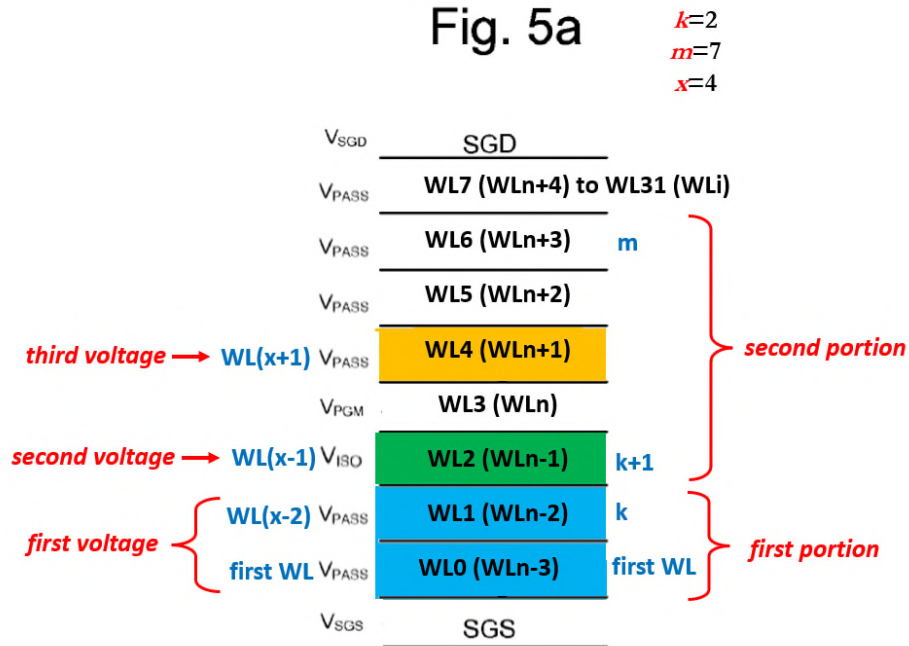
contrast, claim 5 says no such thing. *See U.S. Ethernet Innovations, LLC v. Acer, Inc.*, 646 F. App'x 929, 935 (Fed. Cir. 2016). Thus, it is irrelevant whether the same voltage (*e.g.*, V_{PASS}) is applied to the wordlines receiving the **first voltage** and **third voltage**, and Dong satisfies element [5.C].

5. [5.D] “wherein x , k and m are positive integers, $1 < k < m$ and $3 \leq x$.”

Dong satisfies element [5.D]. Liu, ¶¶ 134-136. The index “ n ” used in Dong to identify wordlines is always an integer.⁵ *See generally* Dong; Liu, ¶ 134. In the same way that the '941 patent never provides an actual number for the wordline **x** being programmed (or the variables **k** and **m**), Dong likewise simply refers to the wordline being used for programming as “WL n ,” and references other wordline locations relative thereto. Accordingly, Dong satisfies element [5.D] in the same way as the '941 patent. Liu, ¶ 134.

Nevertheless, we continue to apply the same concrete example provided above where the memory cell connected to WL3 (*viz.*, WL n) is being programmed.

⁵ *See* <https://dictionary.cambridge.org/us/dictionary/english/integer> (defining integer as “a whole number and not a fraction”).



Dong, Fig. 5a (annotated).

When WL3 is being programmed, then $x=4$ in Dong (because Dong's first wordline is WL0⁶ instead of WL1). Liu, ¶ 135. Because Dong's index "n" correlates to the claimed variable x , the claimed condition is satisfied that $3 \leq x$ (i.e., $3 \leq 4$ because $x=4$). Liu, ¶ 136. Further, the claimed variable k can be taken as 2, which satisfies the condition that $1 < k$. *Id.* Taking k as 2, the claimed *first portion* comprises a *first wordline* [WL0] *to a kth wordline from bottom to top* [WL1 is the second wordline from the bottom]. *Id.* Taking m as 7, then the claimed *second*

⁶ Engineers frequently number a series of items beginning with "0" instead of "1."

Liu, ¶135.

portion comprises a *(k+1)th wordline* [WL2] *to an mth wordline from bottom to top* [WL6 is the seventh wordline from the bottom]. *Id.* Because *k* is 2 and *m* is 7, the claimed condition that *k < m* is satisfied (*i.e.*, 2 is less than 7). *Id.* Accordingly, all conditions are satisfied and Dong discloses element [5.D]. Liu, ¶¶ 134-136.

B. Claim 6: “The program method of claim 5, further comprising:”

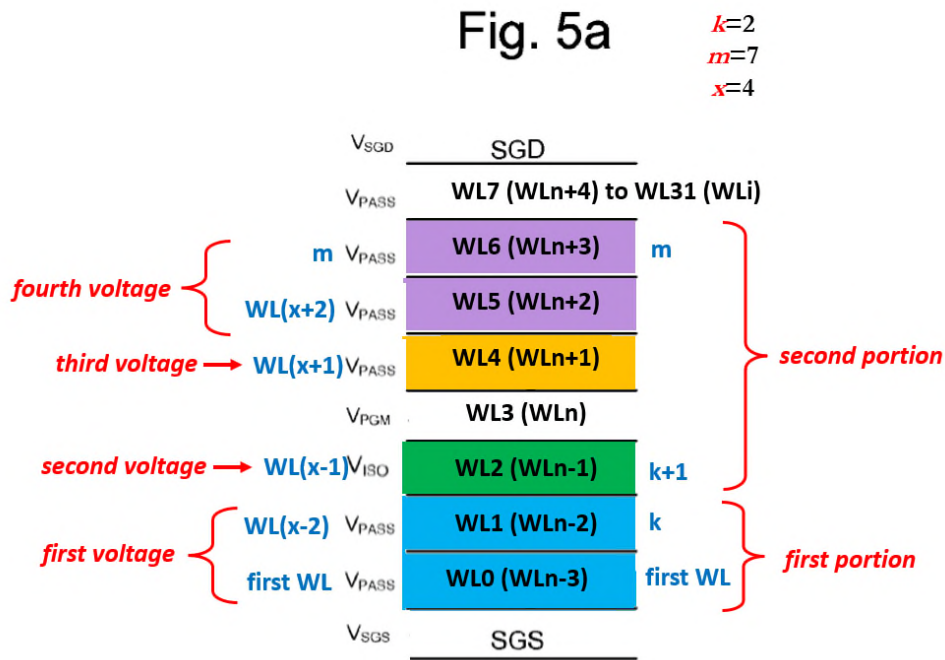
Dong satisfies both elements of claim 6. Liu, ¶ 137.

1. [6.A] “applying a fourth voltage to an (x+2)th wordline to the mth wordline; and”

Dong satisfies element [6.A]. Liu, ¶¶ 138-140. The claimed *fourth voltage* in Dong is V_{PASS} (as applied, *e.g.*, to WL5 and WL6). *Id.*, ¶ 138. As previously discussed, there is no requirement that the *fourth voltage* be a different voltage than the *first, second, or third voltages*. Rather, the only requirement imposed by the *fourth voltage* is that the same voltage be applied to the specified wordlines (*i.e.*, *to an (x+2)th wordline to the mth wordline*). Recall that element [5.A] specifies the *xth wordline is used to perform a program operation*. In Dong’s vernacular, “n” is the wordline used for programming. Dong, [0049] (“a program voltage, V_{PGM} ... is applied to the selected wordline WLn ”).

Thus, the claimed *(x+2)th* wordline corresponds to $WLn+2$ (*viz.*, WL5) in Dong because WLn (*viz.*, WL3) is used for programming. Liu, ¶¶ 139-140. And, as explained for [5.PRE], *m*=7. In Dong Fig. 5a, “a pass voltage, V_{PASS} , ... is applied to each of the unselected wordlines, $WL0$ through $WLn-2$ and $WLn+1$ through

WLi.” Dong, [0049]. Thus, $WLn+2$ (viz., WL5) through $WLn+3$ (viz., WL6) necessarily receive the V_{PASS} voltage. Accordingly, as shown below, **a fourth voltage** [V_{PASS} shown in purple] is applied **to an $(x+2)$ th wordline** [WL5] **to the m th wordline** [WL6]. Thus, Dong satisfies element [6.A]. Liu, ¶¶ 138-140.



Dong, Fig. 5a (annotated).

2. [6.B] “wherein $x < (m-1)$.”

Dong satisfies element [6.B]. Liu, ¶¶ 141-142. Because Dong’s bottom/first wordline is WL0, the wordline used for programming (WLn) is WL3, as shown in Fig. 5a above. This means the index x is 4 (i.e., the fourth wordline is used for programming). Liu, ¶ 141. Recall that the claim defines the **second portion** as extending to the **m th wordline from bottom to top**. As noted for [5.PRE], $m=7$. And

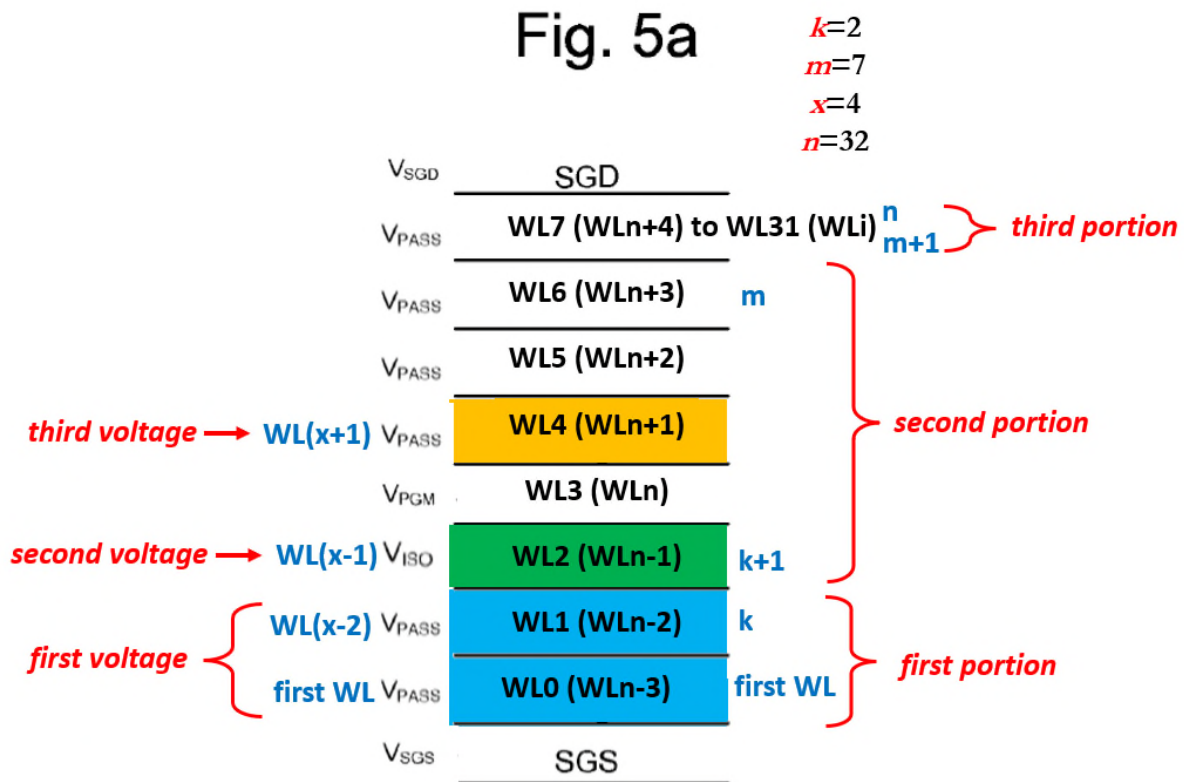
it follows that $m-1$ is 6. Now, it is a simple matter of substitution to plug in the values for x (which is 4) and $m-1$ (which is 6) to evaluate the claimed inequality (*i.e.*, $x < (m-1)$). Liu, ¶ 142. Doing the substitution results in $4 < 6$, which satisfies the inequality. *Id.* Thus, Dong satisfies element [6.B].

C. Claim 7

Dong satisfies claim 7. Liu, ¶ 143.

1. [7.PRE] “The program method of claim 5, wherein the memory further comprises a third portion formed above the second portion, the third portion comprises an $(m+1)$ th wordline to an n th wordline from bottom to top, and the program method further comprises:”

To the extent the preamble is limiting, Dong discloses it. Liu, ¶¶ 144-145. Continuing with the Fig. 5a example of 32 wordlines where the fourth wordline is used for programming, an exemplary *third portion* is shown below (*e.g.*, WL7-WL31). As can be seen, it is located *above the second portion*. Liu, ¶ 145.

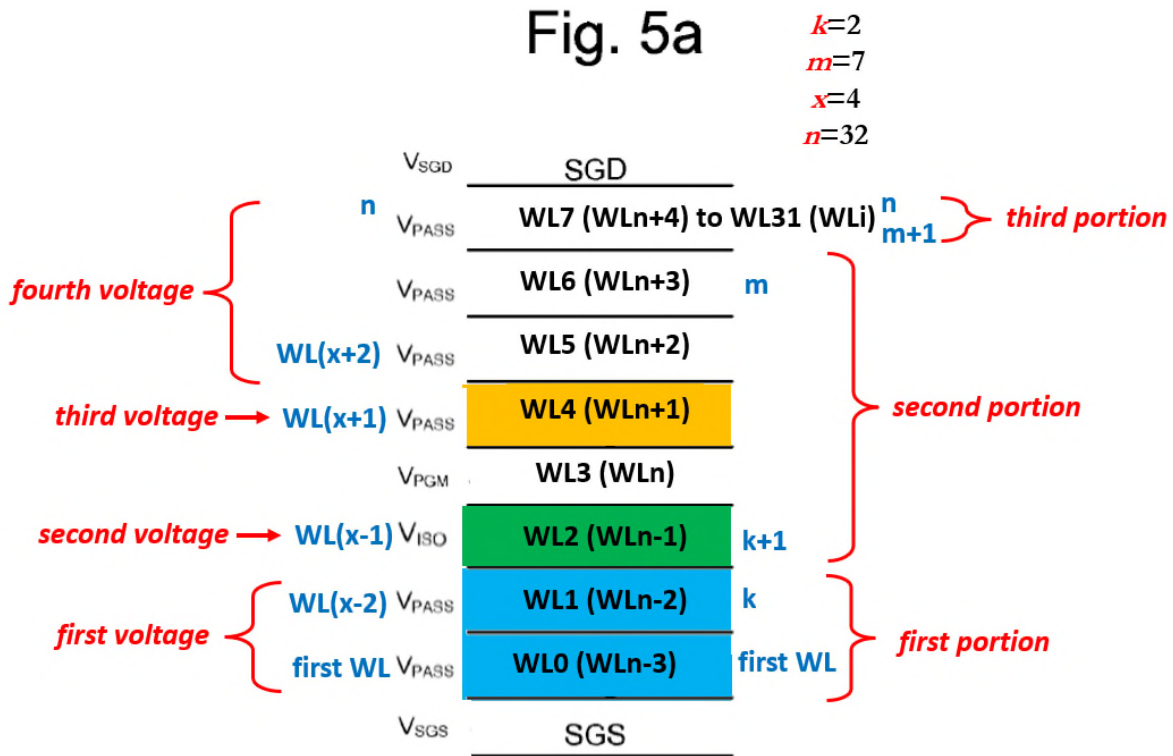


Dong, Fig. 5a (annotated). Recall that in the example being used, $m=7$. The claimed variable n (which differs from Dong’s variable “n” which indicates the cell being programmed), can also be taken as $n=32$. In this case, Dong’s **third portion** comprises an $(m+1)$ th wordline [WL7] to an n th wordline [WL31] from bottom to top. Liu, ¶ 145. Thus, Dong satisfies [7.PRE].

2. [7.A] “applying a fourth voltage to the $(x+2)$ th wordline to the n th wordline;”

Dong satisfies element [7.A]. Liu, ¶¶ 146-148. The claimed **fourth voltage** in Dong is V_{PASS} (as applied, *e.g.*, to WL5 through WL31). *Id.*, ¶ 146. As previously discussed, there is no requirement that the **fourth voltage** be a different voltage than

the *first, second, or third voltages*. Rather, the only requirement imposed by the *fourth voltage* is that the same voltage be applied to the specified wordlines (i.e., *to an (x+2)th wordline to the nth wordline*). Recall that element [5.A] specifies that the *xth wordline is used to perform a program operation*. In Dong's vernacular, "n" is the wordline used for programming. Dong, [0049]. Thus, the claimed *(x+2)th* wordline corresponds to $WLn+2$ (viz., WL5) in Dong. Liu, ¶ 147. Assigning the claimed *nth wordline* as 32 means that Dong's wordline WLi (viz., WL31) is the *nth wordline*. *Id.* Accordingly, WL5 to WL31 in Dong must receive the same *fourth voltage*. Dong Fig. 5a discloses that " $WLn+1$ through WLi " (which is the uppermost wordline) receives V_{PASS} , which would include the additional wordlines near the drain end of the memory string. Dong, Fig. 5a, [0049] ("a pass voltage, V_{PASS} , ... is applied to each of the unselected wordlines, WL0 through $WLn-2$ and $WLn+1$ through WLi ").



Dong, Fig. 5a (annotated).

Thus, WL_{n+2} (viz., WL5) through WL_i (viz., WL31) receive the V_{PASS} voltage. Accordingly, **a fourth voltage** [V_{PASS}] is applied **to an (x+2)th wordline** [WL5] **to the mth wordline** [WL31], as shown above. Liu, ¶¶ 146-148.

3. [7.B] “wherein $m < n$, and $x < (n-1)$.”

Dong satisfies element [7.B]. Liu, ¶ 149. In the Dong Fig. 5a example being used, the fourth wordline is used for programming. Thus, $x=4$. And, as previously described, $m=7$ (see [5.PRE]) and $n=32$ (see [7.PRE]). Thus, $n-1=31$. Substituting in these values, simple math confirms that $m < n$ (viz., $7 < 31$) in Dong Fig. 5a, and $x < (n-1)$ (viz., $4 < 31$). Liu, ¶ 149. Accordingly, Dong satisfies element [7.B].

D. Claim 1:

It is helpful at the outset to observe that claim 1 reads on '941 Patent Fig. 8 (among others). Liu, ¶ 150.

Dong anticipates and/or renders obvious claim 1. Liu, ¶¶ 151-185. The embodiment in Dong that maps to claim 1 is Fig. 5g. The same preliminary comments about Dong Fig. 5a (provided in §X.A for claim 5) apply here. For illustrative purposes and to provide a concrete example, a 32-cell NAND string is used for Fig. 5g where WL12 is the wordline used for programming. Liu, ¶¶ 152-153; Dong, [0090], [0108] (“Although four storage elements are shown to be included in each NAND string, more or less than four can be used (e.g., 16, 32, 64 or another number).”); Luzte, 2:11-18. In this example, the wordlines have the assigned voltages and identifiers shown below. *Id.*

Fig. 5g		
V_{SGD}	SGD	
V_{PASS}	WL _{n+2} through WL _i	WL14 to WL31
$V_{PASS-HIGH}$	WL _{n+1}	WL13
V_{PGM}	WL _n	WL12
$V_{PASS-HIGH}$	WL _{n-1}	WL11
$V_{PASS-MEDIUM}$	WL _{n-2}	WL10
$V_{PASS-LOW}$	WL _{n-3}	WL9
V_{LOW}	WL _{n-4}	WL8
V_{ISO}	WL _{n-5}	WL7
V_{LOW}	WL _{n-6}	WL6
$V_{PASS-LOW}$	WL _{n-7}	WL5
V_{PASS}	WL0 through WL _{n-8}	WL0 to WL4
V_{SGS}	SGS	

Dong, Fig. 5g (annotated).

The further annotated version of Fig. 5g below with colors and additional labels added provides a holistic view of how Dong Fig. 5g maps to claim 1.



Dong, Fig. 5g (annotated). Each element is discussed in detail in the following sections. For reference, the relevant variable and wordline assignments used are aggregated below. It bears noting that these mappings are merely exemplary and other mappings also satisfy the claim. Liu, ¶ 154.

$k = 9$	$WL(n) = WL19$	$WL(x+2) = WL(n+2) = WL14$
$m = 10$	$WL(m+1) = WL10$	$WL(x+1) = WL(n+1) = WL13$
$x = 13$	$WL(m) = WL9$	$WL(x) = WL(n) = WL12$
$n = 20$	$WL(k+1) = WL9$	$WL(x-1) = WL(n-1) = WL11$
		$WL(x-2) = WL(n-2) = WL10$

1. [1.PRE] “A memory comprising:”

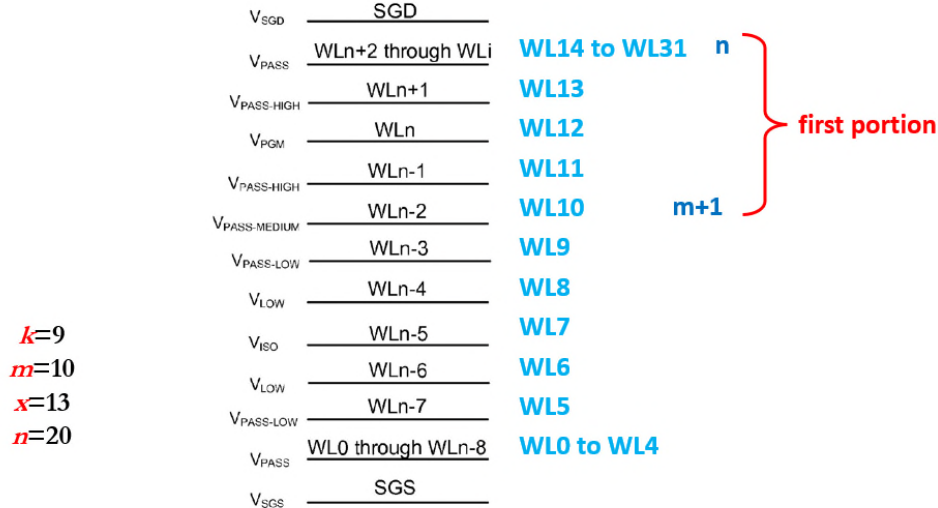
To the extent the preamble is limiting, Dong discloses it for the same reasons as [5.PRE]. Liu, ¶ 155.

2. [1.A] “a first portion comprising an (m+1)th wordline to an nth wordline from bottom to top; and”

Dong satisfies element [1.A]. Liu, ¶¶ 156-157. The term *first portion* is not a term of art. *Id.*, ¶ 156. But the claimed *first portion* of the *memory* is defined by the claim itself as *an (m+1)th wordline to an nth wordline from bottom to top*. The same discussion in §X.A.1 ([5.PRE]) is applicable here regarding (1) the meaning of *bottom to top*; and (2) usage of variables (*e.g.*, *m*, *n*, *k*, and *x*).

The only concrete parameters the claim places on the variables are that *x*, *k* and *m* are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, as recited in [1.I]. These conditions are discussed further at element [1.I], where the claim recites them. As it relates to *m* and *n* as recited in [1.A], *m* can be taken as 10, and *n* can be taken as 20 to provide a specific example. Liu, ¶ 157. Thus, the *(m+1)th wordline* in Dong is WL10 (*viz.*, WL_{n-2}), which is the eleventh wordline from the bottom because Dong’s first wordline is WL0 instead of WL1, and the *nth wordline from bottom to top* maps to WL19. *Id.* The resulting *first portion* (*viz.* WL10 to WL19) is shown below.

Fig. 5g

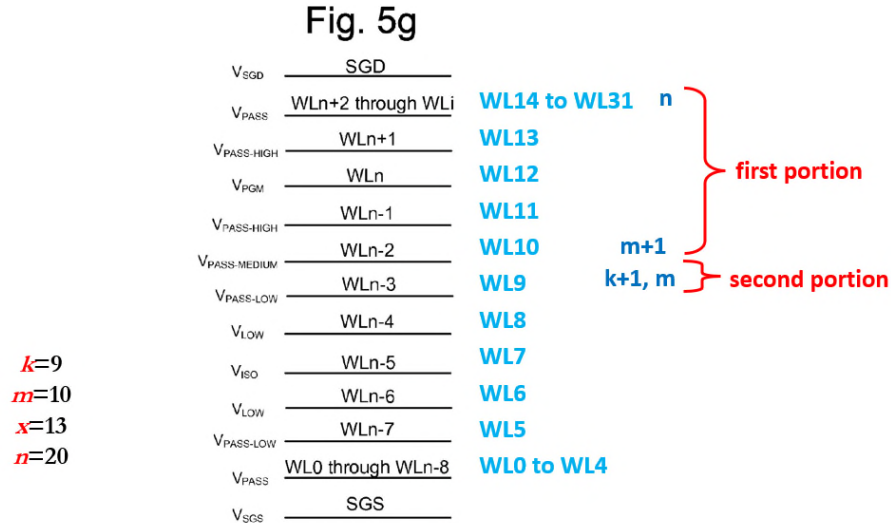


Dong, Fig. 5g (annotated).

3. [1.B] “a second portion formed below the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top; and”

Dong satisfies element [1.B]. Liu, ¶¶ 158-164. The term **second portion** is not a term of art. *Id.*, ¶ 158. But the claimed **second portion** is defined by the claim itself as **a (k+1)th wordline to an mth wordline from bottom to top**.

As in [1.A], **m** is taken as 10 (which corresponds to WL9) and **n** is taken as 20 (which corresponds to WL19). Liu, ¶ 159. And **k** can be taken as 9. *Id.* Thus, the **(k+1)th wordline** in Dong is WL9 (*viz.*, WLn-3), which is the tenth wordline from the bottom because Dong’s first wordline is WL0 instead of WL1. *Id.* The resulting **second portion** (*viz.* from WL9 to WL9) is shown below.



Dong, Fig. 5g (annotated).

To the extent PO argues the **second portion** must comprise multiple wordlines, it is wrong for at least three reasons. **First**, the claim places no upper or lower size limit on the **second portion**, and even a single wordline is sufficient as long as the conditions in [1.I] are satisfied. Liu, ¶¶ 160-163. And the Dong example below satisfies those conditions. In particular, both m and k are integers, and the condition $0 \leq k < m$ is met because $0 \leq 9 < 10$. *Id.*, ¶ 161. The wordline used for programming (x) is taken as 13, which corresponds to WL12 (viz., WLn). Thus, the condition $(m+2) < x < (n-1)$ is met because $12 < 13 < 19$. *Id.* **Second**, where the patentee intended for a **portion** to comprise multiple wordlines, it said so. For example, element [3.A] recites **a third portion formed above the first portion and comprising a plurality of wordlines**. No such language is present in element [1.B]. **Third**, a POSITA's knowledge confirms that a portion may be a single wordline.

Liu, ¶ 163. For example, in connection with memory string programming, Costa discloses that “[a]ny number of zones may be used, including a zone for each wordline.” Costa, [0116]; *see also id.*, [0132], [0162] (“each wordline may be its own zone”).

Element [1.B] also requires that the claimed **second portion** is **formed below the first portion**. Dong satisfies this. Dong’s **second portion** (viz., WL9) is below the **first portion**, which spans WL10 to WL20 as explained for element [1.A]. Liu, ¶ 164. Thus, Dong satisfies element [1.B].

4. [1.C] “a controller configured to apply [various voltages]”

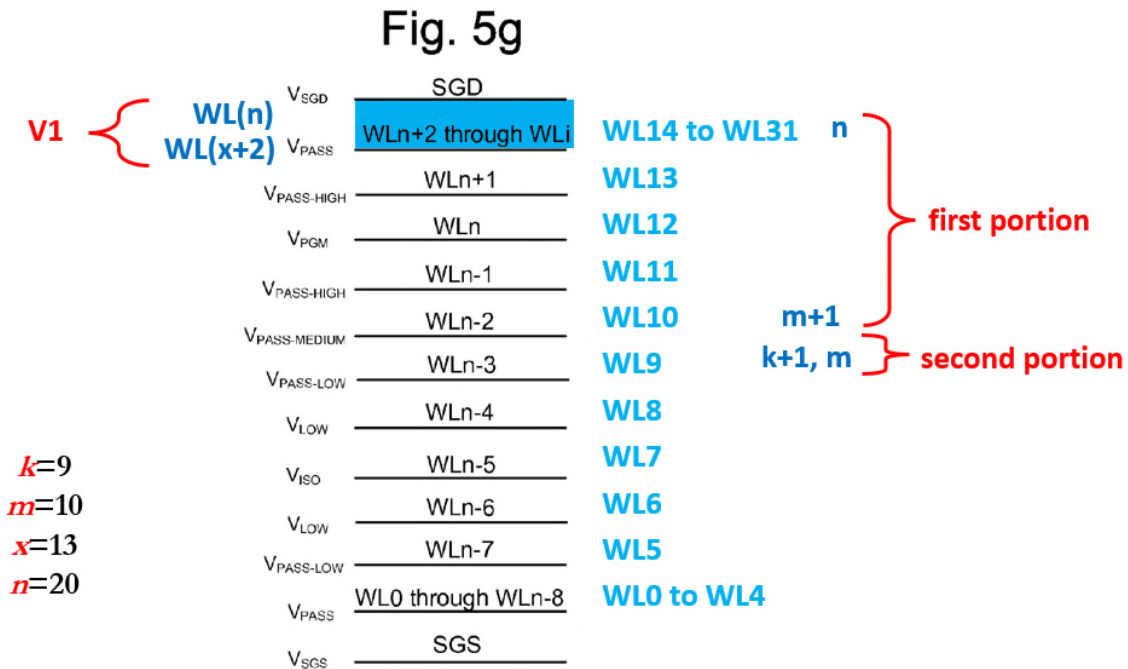
Dong satisfies element [1.C]. Liu, ¶ 165. Component 1250 and/or control circuitry 1250 in Dong Fig. 12 is the claimed **controller**. Dong, Fig. 12, [0095]-[0098] (describing controller operation), [0128] (“a ‘program’ command is issued by the controller”). Dong expressly teaches that “some [] components of FIG. 12 can be combined,” including “control circuitry 1210 ... and control 1250.” *Id.*, [0097].

5. [1.D] “a first voltage to an (x+2)th wordline to the nth wordline,”

Dong satisfies element [5.A]. Liu, ¶¶ 166-170. To begin, the claim uses the variable **x** to identify the wordline **used to perform a program operation**. See element [1.H] (**an xth wordline is used to perform a program operation**). The claimed **xth** wordline corresponds to WLn in Dong. Dong, [0049] (“a program

voltage, V_{PGM} , which is applied to the selected wordline WL_n "); *see also id.*, [0048] ("the selected wordline is WL_n ").

When the x th wordline is used for programming, a **first voltage** is applied **to an $(x+2)$ th wordline to the n th wordline**. Dong satisfies this. In Dong, because WL_n (viz., WL_{12}) is used for programming, a **first voltage** must be applied to the wordlines from WL_{n+2} (viz., WL_{14} , the **$(x+2)$ th wordline**) to WL_{19} (the **n th wordline**). Liu, ¶¶ 167-168. Dong does just this as shown in Fig. 5g below, by applying V_{PASS} to WL_{14} (the **$(x+2)$ th wordline**) through WL_{19} (the **n th wordline**). *Id.*, ¶ 168; Dong, Fig. 5g.

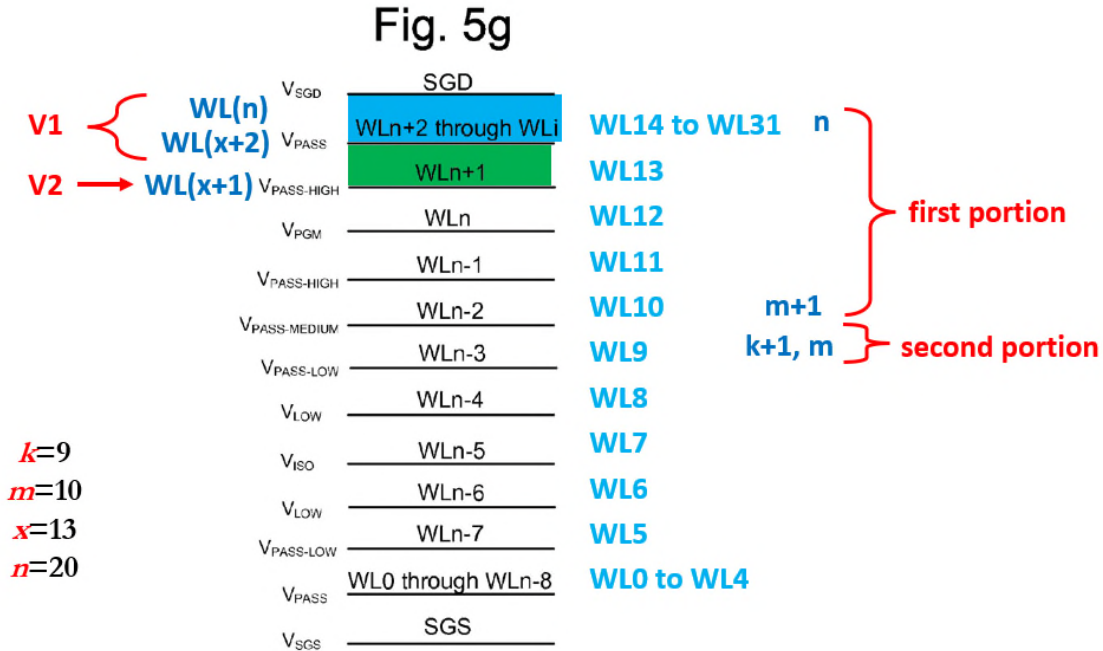


Dong, Fig. 5a (annotated). The claimed **first voltage** corresponds to V_{PASS} in Dong Fig. 5g (applied from WL_{14} to WL_{19}). Liu, ¶ 168. Describing the programming of

Fig. 5f, Dong explains that “ V_{PASS} is applied to a second group of storage elements associated with $\text{WLn}+1$ through WLi .” Dong, [0058]. Dong then explains that Fig. 5g is the same as 5f, except that “($\text{WLn}+1$) adjacent to the selected wordline (WLn) receives $V_{\text{PASS-HIGH}}$ instead of V_{PASS} .” *Id.*, [0059]. Thus, Dong’s description of Fig. 5f applies to Fig. 5g in relevant part here. Neither the claim nor the ’941 patent specification requires any particular voltage (or voltage range) for the claimed **first voltage**. See generally Ex. 1001. All that is required is that the same voltage (whatever voltage it is) be applied to the specified wordlines. Liu, ¶ 170. Thus, because V_{PASS} is applied to the requisite wordlines, Dong satisfies element [5.D].

6. [1.E] “a second voltage to an (x+1)th wordline,”

Dong satisfies element [1.E]. Liu, ¶ 171. Dong discloses applying **a second voltage** [$V_{\text{PASS-HIGH}}$] **to an (x+1)th wordline** [$\text{WLn}+1$, which maps to WL13], as shown below in Fig. 5g. Dong, Fig. 5a, [0059] (“the drain-side wordline ($\text{WLn}+1$) adjacent to the selected wordline (WLn) receives $V_{\text{PASS-HIGH}}$ ”); Liu, ¶ 171. As previously explained, the **(x+1)th wordline** is the wordline immediately above the wordline being used for programming (*i.e.*, the wordline above **x**). Thus, in Dong, the **(x+1)th wordline** is $\text{WLn}+1$ (*viz.*, WL13) and Dong satisfies element [1.D]. Liu, ¶ 171.



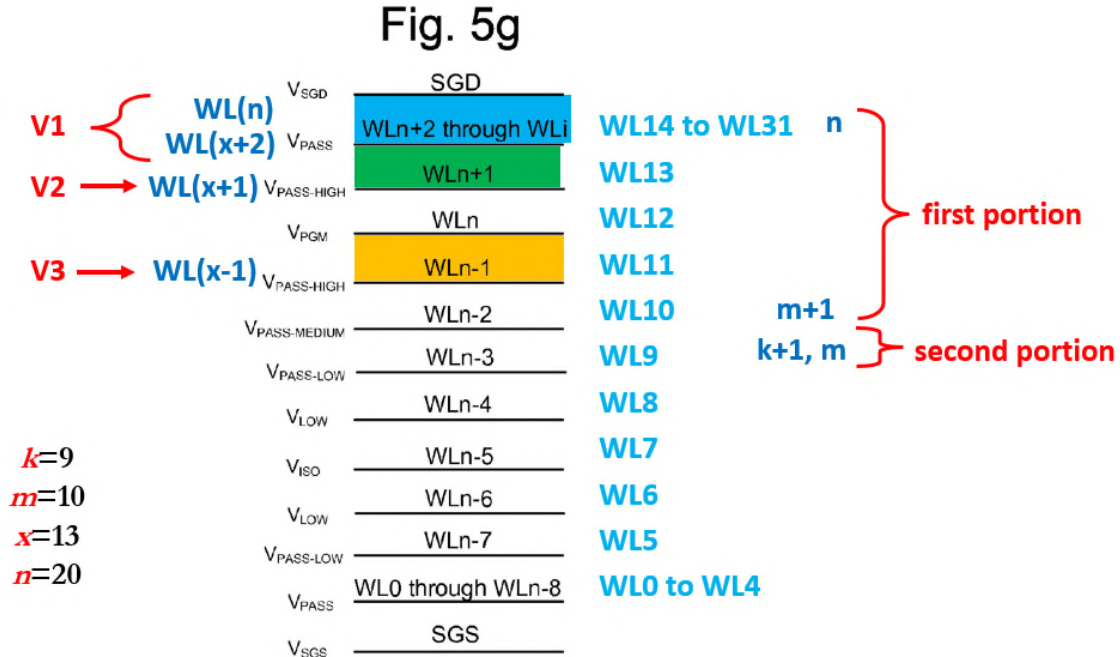
Dong, Fig. 5g (annotated).

7. [1.F] “a third voltage to an (x-1)th wordline,”

Dong satisfies element [1.F]. Liu, ¶¶ 172-173. Dong discloses applying **a third voltage** [V_{PASS-HIGH}] **to an (x-1)th wordline** [WL_{n-1}, which maps to WL11], as shown below in Fig. 5g. Dong, Fig. 5g, [0058] (“the source-side wordline (WL_{n-1}) adjacent to the selected wordline (WL_n) receives V_{PASS-HIGH}”)⁷; Liu, ¶¶ 172-173. As previously explained, the **(x-1)th wordline** is the wordline immediately below the wordline being used for programming (*i.e.*, the wordline

⁷ Even though this statement describes Fig. 5f, it applies equally to Fig. 5g. See Dong, [0058]-[0059] (describing Fig. 5f and only noting differences in Fig. 5g).

below x). Thus, in Dong, the $(x-1)$ *th wordline* is $WLn-1$ (WL11), and Dong satisfies element [1.F].



Dong, Fig. 5g (annotated).

Neither claim 1 nor the specification of the '941 patent requires that the claimed *third voltage* be different than the *first voltage*. See generally Ex. 1001; Liu, ¶ 173. To the contrary, when the '941 patent claims required different relative voltages, they expressly said so. For example, element [1.I] states that *the fifth voltage is lower than the fourth voltage*. By contrast, element [1.F] says no such thing. Thus, it is irrelevant whether the same voltage (viz., $V_{PASS-HIGH}$) is applied to the wordlines receiving the *first voltage* and *third voltage*, and Dong satisfies element [1.F].

8. [1.G] “a fourth voltage to the (m+1)th wordline to an (x-2)th wordline, and”

Dong satisfies element [1.G]. Liu, ¶¶ 174-176. Dong discloses applying **a fourth voltage** [$V_{\text{PASS-MEDIUM}}$] **to the (m+1)th wordline** [WL10 because $m=10$] **to an (x-2)th wordline** [WLn-2, which maps to WL10], as shown below in Fig. 5g. Dong, Fig. 5g, [0058] (“the next wordline (WLn-2) receives $V_{\text{PASS-MEDIUM}}$ ”)⁸; Liu, ¶¶ 174-176. As previously discussed for element [1.A], m is taken as 10, which makes $m+1$ =WL10 (because Dong’s first wordline is WL0). And, in the Dong mapping below, the wordline used for programming is WLn, which corresponds to WL12. Dong, [0049]; Liu, ¶ 174. Thus, the **(x-2)th wordline** in Dong is WLn-2 (*i.e.*, two wordlines beneath the wordline being used for programming), which maps to WL10. Liu, ¶ 174. Accordingly, the specified wordline(s) to which the claimed **fourth voltage** must be applied is just WL10. *Id.*, ¶¶ 174-175. As shown below, the **fourth voltage** in Dong is $V_{\text{PASS-MEDIUM}}$ which is applied to WL10, in satisfaction of element [1.G].

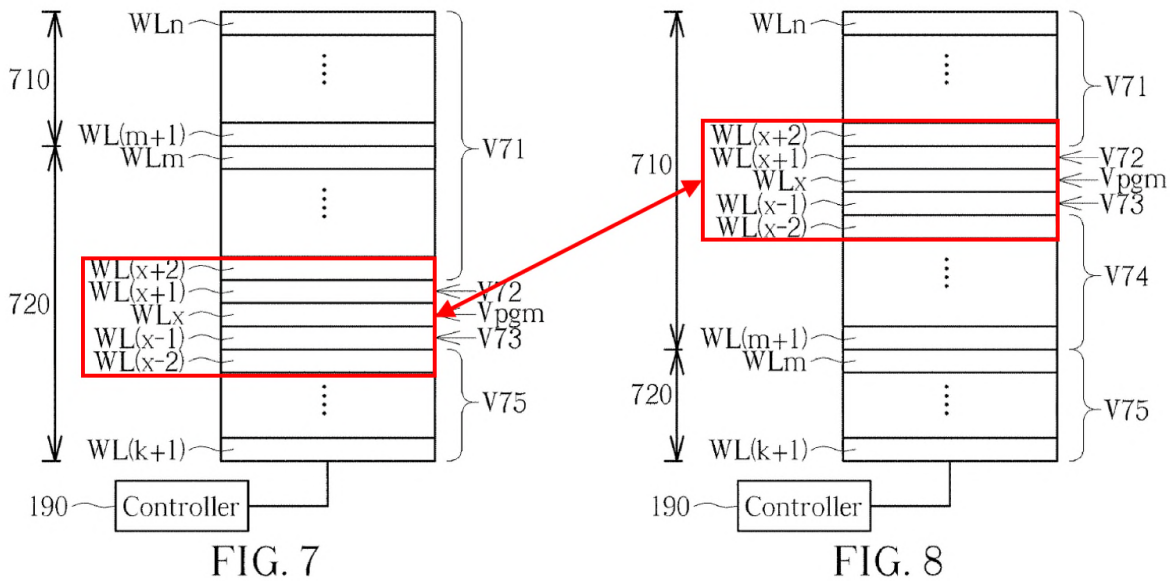
⁸ Even though this statement is describing Fig. 5f, it applies equally to Fig. 5g. See Dong, [0058]-[0059] (describing Fig. 5f and only noting differences in Fig. 5g).

Fig. 5g



Dong, Fig. 5g (annotated).

To the extent PO argues the **fourth voltage** must be applied to multiple wordlines, it is incorrect for the reasons discussed in element [1.B] regarding the **second portion**. Additionally, the '941 specification confirms as much. Figs. 7 and 8 in the '941 specification show programming at two different memory cell locations.



Ex. 1001, Figs. 7-8 (annotated). A POSITA would understand that memory string programming typically advances one cell at a time (but multiple strings may be programmed simultaneously). Liu, ¶ 176. Thus, as programming progressed from Fig. 7 to Fig. 8, WLx advanced up the memory string one wordline at a time—from second portion 720 where WLx (and its adjacent wordlines) are all beneath WL(m+1) to first portion 710 where WLx (and its adjacent wordlines) are all above WL(m+1)—which necessarily includes the scenario where the *(m+1)th wordline* is the same as the *(x-2)th wordline* (i.e., forming a range that spans a single wordline). Liu, ¶ 176.

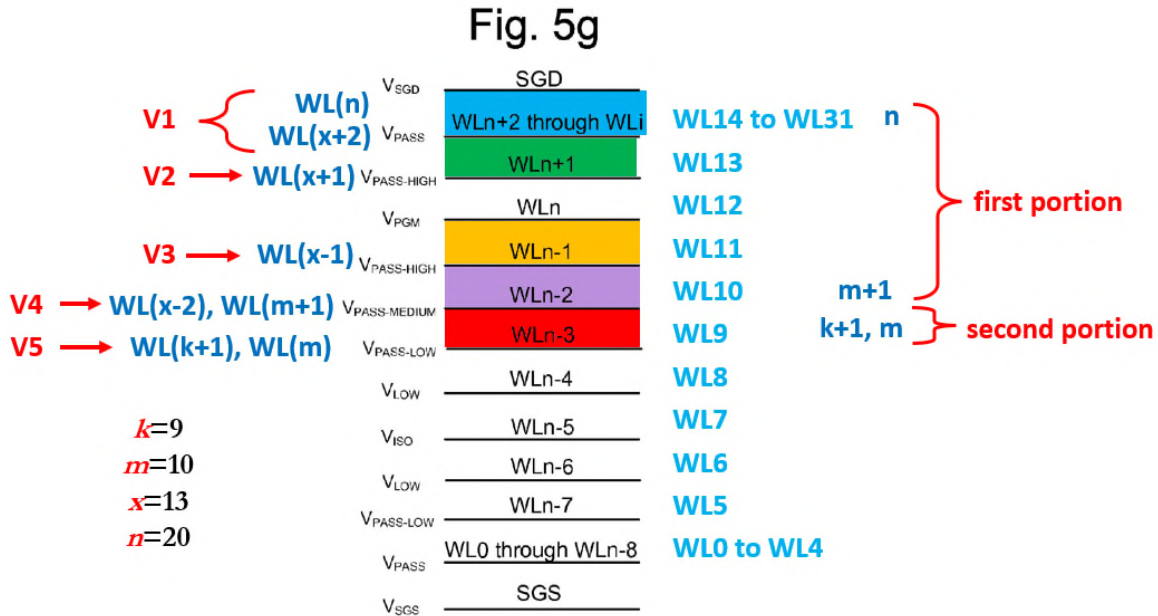
9. [1.H] “a fifth voltage to the (k+1)th wordline to the mth wordline when an xth wordline is used to perform a program operation;”

Dong satisfies element [1.H]. Liu, ¶¶ 177-179. As noted elsewhere, the claimed **xth wordline [] used to perform a program operation** corresponds to WLn in Dong Fig. 5g, which is the wordline used for programming. Dong, Fig. 5g, [0049] (“a program voltage, V_{PGM} , which is applied to the selected wordline WLn”).

The claimed **fifth voltage** in Dong is $V_{\text{PASS-LOW}}$. Dong, Fig. 5g, [0058] (“the next wordline (WLn-3) receives $V_{\text{PASS-LOW}}$ ”)⁹; Liu, ¶ 177. As discussed for element [1.B], **k** is taken as 9. Thus, the **(k+1)th wordline** in Dong is WL9 (viz., WLn-3), which is the tenth wordline from the bottom because Dong’s first wordline is WL0 instead of WL1. Liu, ¶ 178. And, as discussed for element [1.A], **m** is taken as 10, which also corresponds to WL9 in Dong Fig. 5g. *Id.* Accordingly, the specified wordline(s) to which the claimed **fifth voltage** must be applied is just WL9. *Id.* There is no requirement in the claim that the **fifth voltage** must be applied to multiple wordlines. *Id.*

⁹ Even though this statement is describing Fig. 5f, it applies equally to Fig. 5g. See Dong, [0058]-[0059] (describing Fig. 5f and only noting differences in Fig. 5g).

Accordingly, Dong discloses applying **a fifth voltage** [$V_{\text{PASS-LOW}}$] **to the (k+1)th wordline** [WL9] **to the mth wordline** [WL9], as shown below in Fig. 5g, in satisfaction of element [1.H].



Dong, Fig. 5g (annotated).

10. [1.I] “wherein x , k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.”

Dong satisfies element [1.I]. Liu, ¶¶ 180-185. With respect to the requirement that **the fifth voltage is lower than the fourth voltage**, recall element [1.G] mapped the claimed **fourth voltage** to $V_{\text{PASS-MEDIUM}}$ in Dong. And the element [1.H] mapped the claimed **fifth voltage** to $V_{\text{PASS-LOW}}$ in Dong. Dong explains that “multiple V_{PASS} voltages can be used at the same time,” and that “multiple V_{PASS} voltages can be used at both the drain and source sides.” Dong, [0057]. And Dong expressly

discloses that “multiple wordlines ... are biased to different V_{PASS} values, e.g., $V_{\text{PASS-LOW}}$, $V_{\text{PASS-MEDIUM}}$ and $V_{\text{PASS-HIGH}}$. In one implementation, $V_{\text{PGM}} > V_{\text{PASS-HIGH}} > V_{\text{PASS-MEDIUM}} > V_{\text{PASS-LOW}} > V_{\text{LOW}} > V_{\text{ISO}}$.” *Id.* (emphasis added). Thus, Dong’s *fifth voltage* ($V_{\text{PASS-LOW}}$) is less than Dong’s *fourth voltage* ($V_{\text{PASS-MEDIUM}}$). Liu, ¶ 181.

As discussed above in the previous claim elements, the variables *x*, *k*, and *m* in Dong are all integers. See [1.A] (providing example where *m*=10 and *n*=20); [1.B] (providing example where); see generally Dong; Liu, ¶ 182.

All that remains to confirm is that the example of Dong Fig. 5g satisfies the two inequalities in element [1.I]. In the same way that the ’941 patent never provides an actual number for the wordline *x* being programmed (or the variables *k*, *m*, and *n*), Dong likewise simply refers to the wordline being used for programming as “WL_n,” and references the locations of other wordlines relative thereto. Accordingly, Dong satisfies element [1.I] in the same way as the ’941 patent. Liu, ¶ 183. Nevertheless, we continue to apply the same concrete example provided above where the memory string cell connected to WL12 (*viz.*, WL_n) in Dong Fig. 5g is being programmed.

The first inequality requires that $0 \leq k < m$. As noted above, in the Dong example *m*=10. As discussed for element [1.B], *k*=9 in the Dong Fig. 5g example being used. Plugging these values into the inequality produces the following result: $0 \leq 9 < 10$, which satisfies the claimed inequality that $0 \leq k < m$. Liu, ¶ 184.

The next claimed inequality requires that $(m+2) < x < (n-1)$. Because $m=10$, $x=13$, and $n=20$ in the Dong Fig. 5g example being used, $m+2=12$ and $n-1=19$. Liu, ¶ 185. Plugging these values into the inequality produces the following result: $12 \leq 13 < 19$, which satisfies the claimed inequality that $(m+2) < x < (n-1)$. *Id.* Accordingly, both inequalities are satisfied and Dong discloses element [1.I].

E. Claim 3

Dong satisfies claim 3. Liu, ¶ 186. The preamble of claim 3 recites “The memory of claim 1, further comprising” and is met for the same reasons as claim 1. *Id.*

1. [3.A] “a third portion formed above the first portion and comprising a plurality of wordlines”

Dong satisfies element [3.A]. Liu, ¶¶ 187-189. The term **third portion** is not a term of art, and must simply **compris[e] a plurality of wordlines** that are located **above the first portion**. *Id.*, ¶ 187. Unlike the claimed **first** and **second portions**, the claim does not use any specific variables or ranges to define the **third portion**. *Id.*, ¶ 188. As discussed in connection with element [1.A], the claimed **first portion** in Dong mapped to wordlines WL10 to WL19. Thus, Dong’s **third portion** must be above WL19. Liu, ¶ 189. In the Dong Fig. 5g example being used, the memory strings have 32 bits as explained in §X.D, corresponding to wordlines WL0 to WL31. Thus, the **third portion** can be taken as WL20 to WL21, which are both **above** the **first portion**. *Id.*

2. [3.B] “wherein the controller is further configured to apply the first voltage to the plurality of wordlines when the xth wordline is used to perform the program operation.”

Dong satisfies element [3.B]. Liu, ¶¶ 190-192. The part of this limitation requiring a *controller configured to apply the first voltage ... when the xth wordline is used to perform the program operation* has already been addressed in connection with elements [1.C] and [1.H]. All that remains is that the *first voltage* be applied to the *plurality of wordlines* recited in element [3.A]. The *plurality of wordlines* in the Dong example being used is WL20 to WL21. See [3.A]. And as was explained for element [1.D], the claimed *first voltage* in Dong Fig. 5g is V_{PASS} . Describing the programming of Fig. 5f (which in relevant part is applicable to Fig. 5g),¹⁰ Dong teaches that “ V_{PASS} is applied to a second group of storage elements associated with $WLn+1$ through WLi .” Dong, [0058]. Dong’s *plurality of wordlines* in Fig. 5g (viz., WL20 to WL21) fall within the range of $WLn+1$ (viz., WL14) through WLi (viz., WL31). Liu, ¶ 192. Accordingly, because, V_{PASS} is applied to the requisite wordlines, Dong satisfies element [3.B].

¹⁰ In particular, Dong explains that Fig. 5g only “differs from that of FIG. 5f in that the drain-side wordline ($WLn+1$) adjacent to the selected wordline (WLn) receives $V_{\text{PASS-HIGH}}$ instead of V_{PASS} .” *Id.*, [0059].

F. Claim 11

Claim 11 is a method claim whereas claim 1 is an apparatus claim, but claim 11 is substantially similar to claim 1 and is met by Dong for the same reasons. Liu, ¶ 193.

1. [11.PRE]

If the preamble of claim 11 is limiting, Dong satisfies it for the same reasons as [1.PRE], [1.A], and [1.B]. Liu, ¶¶ 194-195. While claim 11 is a method claim, the preamble does not contain any method steps and merely recites the same structural limitations (viz., a **first portion** and **second portion**) recited in elements [1.A] (**first portion**) and [1.B] (**second portion**). *Id.* A color-coded comparison mapping [11.PRE] to the same limitation in claim 1 is shown in the table below.

Claim 11	Claim 1
[11.PRE] A program method of a memory, the memory comprising a first portion and a second portion formed below the first portion, the first portion comprising an (m+1)th wordline to an nth wordline from bottom to top, the second portion comprising a (k+1)th wordline to an mth wordline from bottom to top , the program method comprising:	[1.PRE] A memory comprising: [1.A] a first portion comprising an (m+1)th wordline to an nth wordline from bottom to top; and [1.B] a second portion formed below the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top; and

2. **[11.A] “applying a first voltage to an (x+2)th wordline to the nth wordline when an xth wordline is used to perform a program operation;”**

The limitation **when an xth wordline is used to perform a program operation** is present in element [1.H] and is met for the same reasons. Liu, ¶ 196. The balance of element [11.A] is substantively the same as element [1.D] and is met for the same reasons. *Id.*

3. **[11.B] “applying a second voltage to an (x+1)th wordline;”**

Element [11.B] is substantively the same as element [1.E] and is met for the same reasons. Liu, ¶ 197.

4. **[11.C] “applying a third voltage to an (x–1)th wordline;”**

Element [11.C] is substantively the same as element [1.F] and is met for the same reasons. Liu, ¶ 198.

5. **[11.D] “applying a fourth voltage to the (m+1)th wordline to an (x–2)th wordline; and”**

Element [11.D] is substantively the same as element [1.G] and is met for the same reasons. Liu, ¶ 199.

6. **[11.E] “applying a fifth voltage to the (k+1)th wordline to the mth wordline;”**

Element [1.H] contains substantively the same limitation as element [11.E] and [11.E] is met for the same reasons. Liu, ¶ 200.

7. **[11.F] “wherein x , k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.”**

Element [11.F] is identical to element [1.I] and is met for the same reasons.

Liu, ¶ 201.

G. Claim 13

Dong satisfies claim 13 for substantially the same reasons as claim 3. Liu, ¶ 202.

1. **[13.PRE] “The program method of claim 11, wherein the memory further comprises a third portion formed above the first portion, the third portion comprises a plurality of wordlines, and the program method further comprises:”**

If the preamble of claim 3 is limiting, Dong satisfies it for the same reasons as [3.A]. Liu, ¶ 203.

2. **[13.A] “applying the first voltage to the plurality of wordlines of the third portion.”**

Element [3.B] includes the same requirement as element [13.A], and [13.A] is met by Dong for the same reasons. Liu, ¶ 204.

XI. GROUND 3 (DONG COMBINED WITH COSTA)

Dong combined with Coast renders obvious claims 8-9. Liu, ¶ 205.

A. Motivation to Combine Dong and Costa

A POSITA would have been motivated to combine Costa’s teachings with Dong to improve memory reliability. Liu, ¶¶ 206-213. Dong and Costa both address NAND flash memory programming (see Dong, [0011]; Costa, [0014],

[0041]), and both are specifically concerned with reliability issues related to program operations (Dong, Abstract; Costa, Abstract).

NAND flash programming is an iterative process involving application of a programming pulse followed by program verification pulses. Dong, Figs. 19 (flow chart) and 20 (showing program and verification pulses); Costa, Fig. 6 (showing program and verification pulses). A POSITA knew that a “disturb free” memory programming operation would require both aspects of the operation (*viz.*, application of the program pulse(s) and verification pulses) to be disturb free. Liu, ¶ 208. A POSITA would have recognized that both phenomena should be addressed to improve the reliability of flash devices during the iterative programming operation. Thus, a POSITA would have considered using Dong’s techniques with other techniques for a more comprehensive improvement of memory reliability. Liu, ¶¶ 208-209.

Dong and Costa focus on two different (but complementary) phenomena that impact memory device reliability during programming. Dong’s teachings focus on mitigating the effects of program disturb resulting from the application of the actual programming pulse. Dong, Figs. 4, 19-20, [0042]-[0043] (“Program disturb occurs when the threshold voltage of an unselected non-volatile storage element is shifted due to programming of other non-volatile storage elements”). Costa, in contrast, focuses on addressing program disturb impacts arising from the verification phase

of programming. Costa, [0029]-[0030] (discussing channel resistance impact on programming verification).

Dong's programming techniques reduce unintended program disturb on memory cells due to high electric field in the channel region during application of the program pulse(s). Dong, [0015]. A POSITA considering reliability issues relating to program disturb in Dong would have been motivated to consider references like Costa that address other programming concerns, such as increased channel resistance as more memory cells in a string are programmed. Liu, ¶¶ 211-212.

As Costa teaches (and a POSITA would have known), “[t]he channel resistance increases as each memory cell is programmed, leading to the highest resistance and lowest channel conductance when programming the later programmed memory cells.” Costa, [0029]; *see also id.*, [0101]; Liu, ¶ 210. The increased channel resistance may cause “later programmed memory cells ... to be programmed to higher levels than intended.” Costa, [0029]. Costa combats this adverse impact on memory cell threshold voltages by applying “a variable pass voltage” dependent on the location of the cell being programming in the memory string. Costa, Abstract, [0029], [0101]-[0104]. Dong is silent regarding how V_{PASS} (and other programming voltage values) change as the cell being programmed advances from the source end of a memory string to the drain end, thus lending itself

to Costa's "variable pass voltage" technique, especially as the number cells in a memory string grows. Liu, ¶ 210. What's more, Dong acknowledges that program disturb can occur on previously programmed memory cells as well as erased cells. Dong [0011]. In other words, Dong describes a program disturb issue that occurs as programming advances along a memory string. Liu, ¶ 212. That would have motivated a POSITA to investigate and apply techniques (like Costa's) to address program disturb/errors that occur as function of the location of a cell being programmed within a memory string (*e.g.*, closer to the source end or drain end). Liu, ¶ 211.

A POSITA would have had a reasonable expectation of success in combining Dong and Costa because their respective programming teachings are mutually compatible. Liu, ¶ 213. Combining both teachings would address memory cell errors introduced during both phases of the program operation (*viz.*, the programming pulse and verification pulse). *Id.* Moreover, a POSITA would have reasonably expected success because both references disclose similar control circuitry, memory arrays, read-operation processes, etc. *Id.* No new/additional hardware is necessary to combine Dong and Costa. *Id.* To the contrary, implementing Costa's teachings would require only minimal software changes to Dong's controller, which was well within the knowledge and skill of a POSITA as

it involved nothing more than the routine application of known techniques. *Id.*; See *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

- B. Claim 8: “The program method of claim 7, wherein: [A] the first voltage has a first level if the xth wordline is in the first portion; [B] the first voltage has a second level if the xth wordline is in the second portion; [C] the first voltage has a third level if the xth wordline is in the third portion; and [D] the first level is lower than the second level, and the second level is lower than the third level.”**

Dong in view of Costa renders claim 8 obvious. Liu, ¶¶ 214-220. The reasons for combining Dong and Costa are discussed in §XI.A. And Dong satisfies the underlying elements of claims 5 and 7 as discussed in §X.A (claim 5) and §X.C (claim 7).

Although verbose, all claim 8 requires is that the voltage level of the *first voltage* (which is applied from the *first wordline to an (x-2)th wordline*) increases as the wordline used for programming (i.e., the *xth wordline*) moves up the memory string from the *first portion*, to the *second portion*, to the *third portion*. Liu, ¶ 214. The location of the *xth wordline* relative to the three claimed *portions* can be seen in ’941 patent Figs. 3 (*xth wordline* in *first portion*), 4 (*xth wordline* in *second portion*), and 5 (*xth wordline* in *third portion*). Dong is silent regarding what (if anything) happens to the V_{PASS} voltage depending on which cell is being programmed. However, Costa specifically discloses that V_{PASS} increases (for the wordlines below the cell being programmed) as programming proceeds up the memory string. See §IX.C (summarizing Costa).

Costa discloses that wordlines (and their corresponding memory cells) are “partitioned into ranges or zones.” Costa, [0032]; *see also* [0114]-[0116]. Costa’s zones/range correspond to the claimed **portions** in the ’941 patent. Liu, ¶ 216. Costa discloses that the pass voltage applied to “the earlier programmed memory cells” (Costa, [0031])—*i.e.*, the cells beneath the cell being programmed— “varie[s] based on the zone of the selected memory cell” and that “[g]enerally, a lower pass voltage is applied to these memory cells when the selected wordline is in a lower zone corresponding to earlier programmed memory cells closer to a first select line (*id.*, [0032]). “[T]he pass voltage for the memory cells is higher when programming memory cells in higher zones after programming for lower zone memory cells completes. A higher pass voltage is used for the memory cells as more wordlines of the group undergo programming.” Costa, [0032]; *id.*, Abstract (similar), [0030], [0033] (describing “variable pass voltage”), [0104], Figs. 8-10, [0111] (“the second pass voltage $V_{read}+100$ is higher than the first read pass voltage V_{read} by 100 mV”), [0028] (“the pass voltage that is applied is dependent upon the position of the selected memory cell.”), [0104] (similar).

Costa provides “a simple example,” where “a NAND string [is divided] into two equal-sized zones.” Costa, [0115]. “When verifying a selected wordline in the first zone (e.g., WL3), a lower read pass voltage (e.g., $V_{read}-100$ [mV]) is applied to a subset of unselected wordlines on the already programmed (source) side of the

selected wordline. When verifying a selected wordline in the second zone (e.g., WL124), a higher read pass voltage (e.g., V_{read}) is applied to the subset of unselected wordlines on the source side of the selected wordline.” *Id.*; *see also id.*, [0114]. But Costa expressly discloses that “the size of the zones may not be equal ... [and] more than two zones may be used. Any number of zones may be used, including a zone for each wordline. When verifying a selected wordline in a zone, the read pass voltage applied to the subset of unselected memory cells is higher than the read pass voltage that was applied when verifying a selected wordline in any of the previously programmed zones.” *Id.*, [0116].

Applying Costa’s teachings of “wordline dependent pass voltages” (which is the title of Costa) to Dong satisfies claim 8. Liu, ¶ 220. In particular, claim 7 discusses the three **portions** in Dong Fig. 5a. Taking each claimed **portion** in Dong as one of Costa’s “zones,” the claimed **V1** voltage (viz., Dong’s V_{PASS} voltage) applied to the previously programmed cells in a memory string will increase as the cell being programmed moves from the **first portion** (first zone) to the **second portion** (second zone), and from the **second portion** (second zone) to the **third portion** (third zone). *Id.* This satisfies the claimed condition that **the first [voltage] level** in the first portion **is lower than the second level**, and the **second [voltage] level** in the second portion **is lower than the third [voltage] level** in the third portion.

- C. Claim 9: “The method of claim 5, wherein: [A] the first voltage has a first level if the xth wordline is in the first portion; [B] the first voltage has a second level if the xth wordline is in the second portion; and [C] the first level is lower than the second level.”**

Claim 9 is broader than claim 8 and is thus met for the same reasons as claim 8. Liu, ¶ 221. In particular, claim 9 requires the same underlying concept as claim 8 vis-à-vis the relative level of the *first voltage*, but only applies it to the circumstance when the *xth wordline* is in the *first* and *second portions*. *Id.*

XII. GROUND 4 (DONG COMBINED WITH SHIRAI)

The combination of Dong and Shirai renders obvious claims 4, 10, and 14. Liu, ¶ 222.

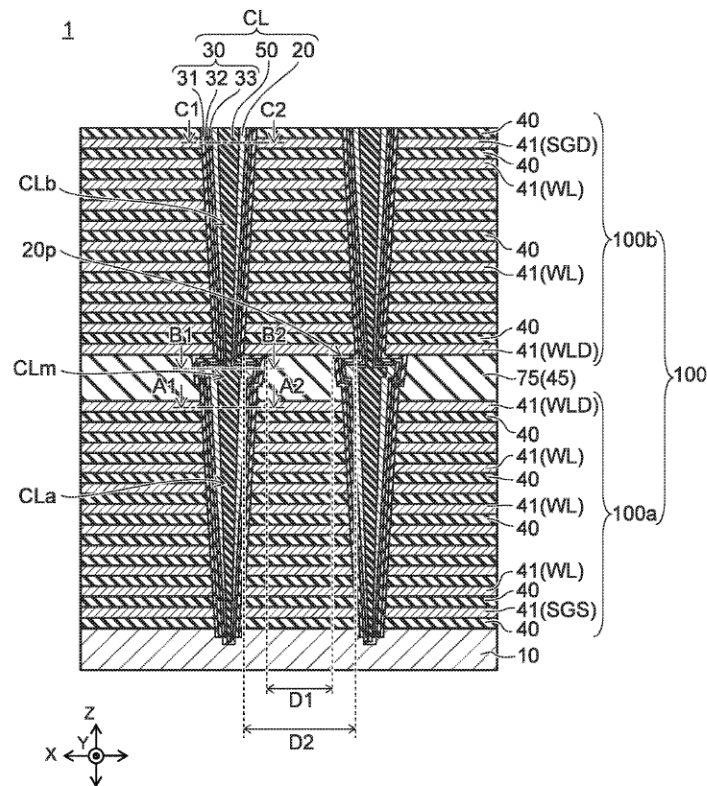
A. Motivation to Combine Dong and Shirai

A POSITA would have been motivated to combine Shirai’s teaching of a multiple deck memory structure with Dong for manufacturing purposes to improve yield. Liu, ¶¶ 223-228. Dong discloses its “array of storage elements can be three dimensional.” Dong, [0095]. Dong teaches its memory strings are “not limited to any particular number of memory cells,” and it was well-known that 3D NAND strings often exceed 100 cells by the Priority Date. Lutze, 2:11-18; see §X.A (discussing long memory strings); Liu, ¶ 224. The reason for this was the relentless demand for increased memory capacity at lower cost per bit, which was largely achieved by longer 3D NAND memory strings. Ex. 1009, 292-295; Liu, ¶¶ 223, 49-52.

As was well-known to POSITAs and explained by Shirai, when “manufacturing [3D NAND memory devices], holes are formed in a stacked body including multiple conductive layers. As the number of stacked layers in the stacked body increases, it becomes difficult to collectively form the holes.” Shirai, [0003]; This is because maintaining an anisotropic etch profile is increasingly difficult as the number of layers (*viz.*, memory cells and wordlines) increases. *Id.*, [0042] (“As the number of stacked layers in the stacked body 100 increases, it becomes difficult to form the holes.”); Ex. 1019 (“Chen”), 4:10-32 (“Due to a desire to increase the height of the stack to allow for more layers and more memory cells in each NAND string, ... [t]he memory hole is etched separately in each tier so that a low aspect ratio can be achieved.”); Liu, ¶¶ 223-227.

Thus, Shirai teaches a multi-deck memory structure in which memory holes are etched separately in each deck and connected to form longer memory strings. Shirai, Figs. 2 and 7-15, [0042], [0003] (“A method has been proposed in which holes can be easily formed even in a stacked body having a large number of stacked layers by repeating formation of the holes and formation of the stacked body (stacked portion).”). The etching profile of the memory holes (wider at the top and narrower at the bottom of each deck) is apparent from Shirai Fig. 2.

FIG. 2



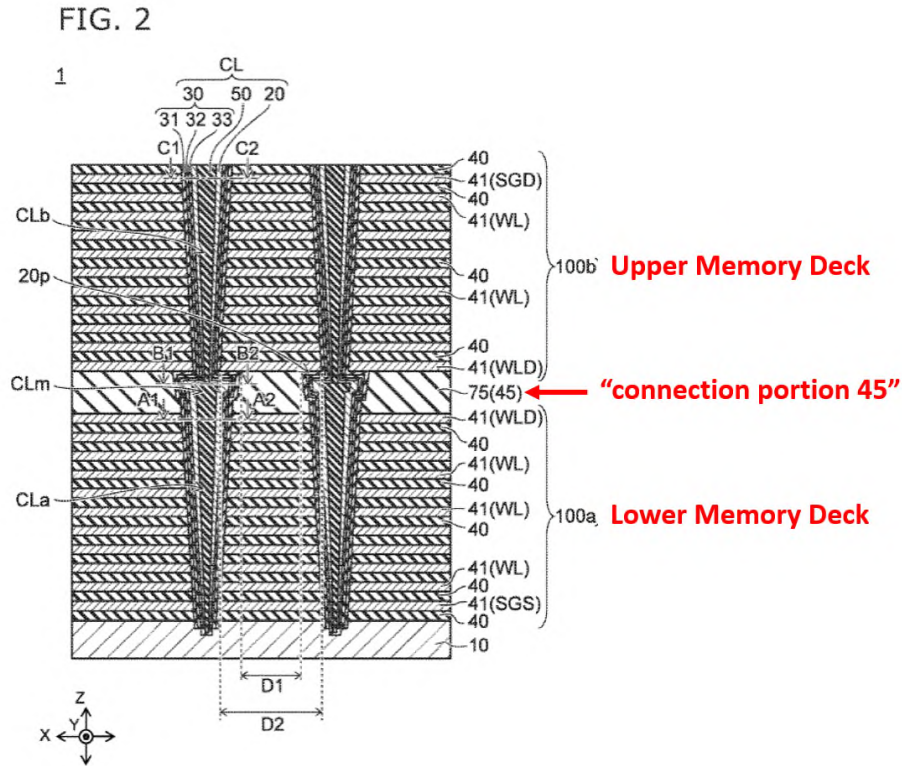
Shirai, Fig. 2. As a POSITA would recognize, trying to form a memory hole using a single etch through the entire structure would result in memory strings that did not extend through all layers and/or were too wide at top (which would limit the number of memory strings in a given area and reduce memory density). Liu, ¶ 227. Such memory strings would be inoperable and/or have significant yield, reliability, and density issues. *Id.* Thus, a POSITA would have been motivated to use a multi-deck structure and manufacturing process (like Shirai's) with Dong. Liu, ¶¶ 223-227.

Dong is not limited to memory stacks of a particular height or manufacturing process. *See generally* Dong. A POSITA would have had a reasonable expectation of success applying Shirai's two-deck architecture to Dong because the

manufacturing process for doing so was taught by Shirai (including the use of dummy wordlines near the boundary of the two decks) and manufacturing/using multiple decks was common practice by the Priority Date. Shirai, Figs. 5-15; Ex. 1014 (“Lee III”), Figs. 28, 33, [0005], [0074]; Righetti, [0002], [0017], Fig. 1; Chen, Figs. 6 and 16, 4:10-32 (“The memory hole is etched separately in each tier so that a low aspect ratio can be achieved.”), 14:64-15:25; Liu, ¶ 228.

B. Claim 4: “The memory of claim 1, further comprising: an upper dummy wordline formed below the first portion; a lower dummy wordline formed above the second portion; and a joint oxide layer formed between the upper dummy wordline and the lower dummy wordline; wherein the memory has a two-deck structure.”

Applying Shirai’s teaching of a two-deck memory structure to Dong (as described above) renders claim 4 obvious. Liu, ¶¶ 229-232. Shirai discloses a 3D NAND memory device comprising multiple memory decks, which Shirai calls “stacked portions.” See, e.g., Shirai, [0030] (Fig. 2 “includes a first stacked portion 100a, a connection portion 45, and a second stacked portion 100b.”); Figs. 2 and 7-15. Thus, Shirai discloses a *two-deck structure*, as shown below in Fig. 2. Liu, ¶ 229.



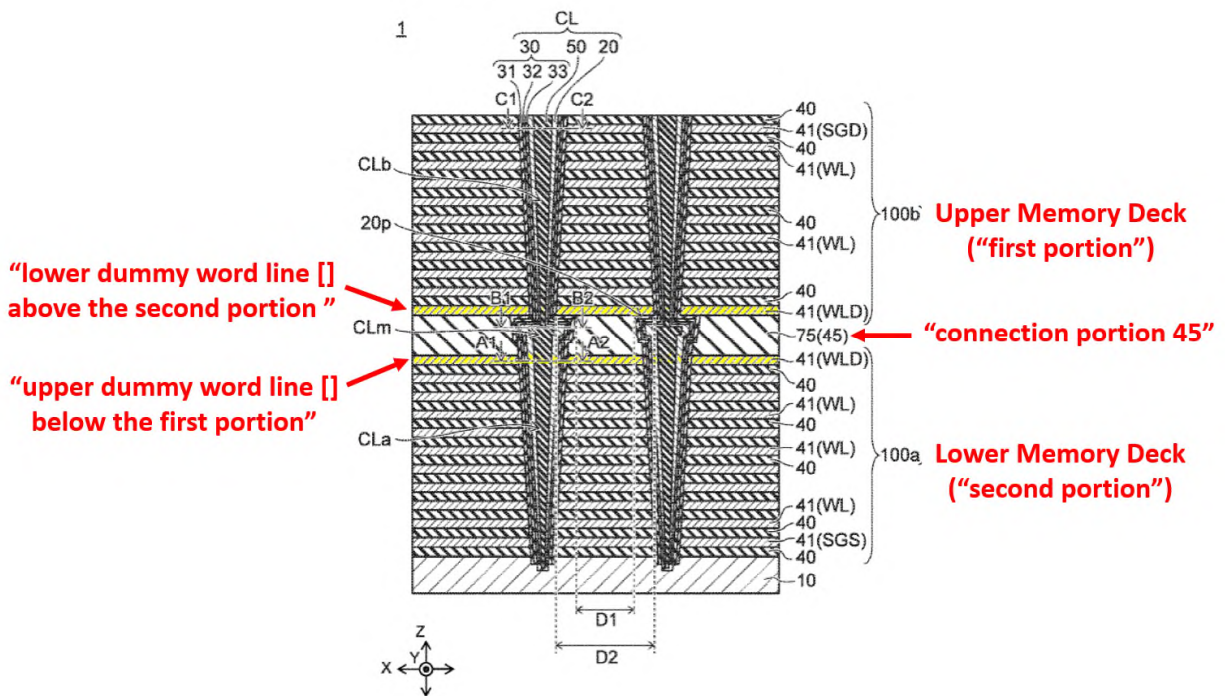
Shirai, Fig. 2 (annotated).

After forming the lower deck 100a, a “connection portion 45 is provided on the first stacked portion 100a. The second stacked portion 100b is provided on the connection portion 45.” *Id.*, [0030]. Shirai discloses that connecting portion 45 may be “silicon oxide.” *Id.*, [0045]; *see also id.*, [0014] (“The connection portion includes an insulating layer between the high dielectric layer and the second stacked portion.”); [0031] (disclosing various oxides for connecting portion 45). Thus, Shirai discloses a **joint oxide layer** [connecting portion 45]. Liu, ¶ 230. The presence and location of the claimed **dummy wordlines** is discussed next.

Shirai further discloses that in lower deck 100a, “the electrode layer 41 closest to the connection portion 45 functions as a dummy wordline WLD,” and in upper deck 100b, “the electrode layer 41 closest to the connection portion 45 functions as a dummy wordline WLD.” *Id.*, [0032]. Thus, Shirai discloses the claimed **dummy wordlines**. Liu, ¶¶ 231-232. As shown above, connection portion 45 is **formed between the [dummy wordlines]**.

Claim 4 further requires that the **upper dummy wordline [is] formed below the first portion** and the **lower dummy wordline [is] formed above the second portion**. Shirai discloses this. *Id.* The dummy wordline locations relative to stack portions 100a and 100b (viz., the **[memory] decks**) can be seen in Shirai Fig. 2 below. Recall that in base claim 1, the **second portion [is] formed below the first portion**. See element [1.B]. Dong’s first portion corresponds to Shirai’s upper deck 100b, and Dong’s second portion corresponds to Shirai’s bottom deck 100a. Liu, ¶ 232. Thus, Shirai’s dummy wordline 41 in 100a is an **upper dummy wordline[s] formed below the first portion** [e.g., below upper deck 100b]. *Id.* And dummy wordline 41 in 100b is a **lower dummy wordline formed above the second portion** [e.g., above lower deck 100a]. *Id.*

FIG. 2



Shirai, Fig. 2 (showing dummy wordlines in yellow).

C. Claim 10: “The program method of claim 5, wherein the memory further comprises: a lower dummy wordline formed above the first portion; an upper dummy wordline formed below the second portion; a joint oxide layer formed between the lower dummy wordline and the upper dummy wordline; wherein the memory has a two-deck structure.”

Claim 10 is substantively the same as claim 4 and is met for the same reasons.

Liu, ¶¶ 233-234. Sub-elements [4.C] and [4.D] are identical to [10.C] and [10.D], respectively. While not worded identically, sub-elements [4.A] and [4.B] are substantively identical to [10.B] and [4.B], respectively. *Id.*

Sub elements [4.A] and [10B] both require *an upper dummy wordline*. But [4.A] says the *upper dummy wordline* is *formed below the first portion*,” whereas

[10B] says it is *formed below the second portion*. Sub elements [4.B] and [10A] both require *a lower dummy wordline*. But [4.B] says the *lower dummy wordline* is *formed above the second portion*,” whereas [10.A] says it is *formed above the first portion*. The reason these are substantively the same is because of claim 1 (on which claim 4 depends) and claim 5 (on which claim 10 depends) define the *first* and *second* portions. Liu, ¶ 234. In claim 1, *a second portion [is] formed below the first portion*. See element [1.B]. In claim 5, *the second portion [is] formed above the first portion*. See element 5[PRE].

Claim 4	Claim 10
[4.A] an upper dummy wordline formed below the first portion;	[10.A] a lower dummy wordline formed above the first portion;
[4.B] a lower dummy wordline formed above the second portion; and	[10.B] an upper dummy wordline formed below the second portion;

- D. Claim 14: “[PRE] The program method of claim 11, wherein the memory further comprises: [A] an upper dummy wordline formed below the first portion; [B] a lower dummy wordline formed above the second portion; and [C] a joint oxide layer formed between the upper dummy wordline and the lower dummy wordline; [D] wherein the memory has a two-deck structure.”**

Claim 14 is identical to claim 4 and is met for the same reasons. Liu, ¶ 235.

XIII. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See generally* Exs. 1002 and 1003. Even if such considerations existed, none would overcome this Petition's strong *prima facie* showing of obviousness.

XIV. CONCLUSION

Petitioner respectfully requests the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

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Dated: 11/26/2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,991 words.

Dated: 11/26/2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on November 26, 2024 via international courier upon the following counsel of record for Patent Owner:

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