

Z-Interference and Z-Disturbance in Vertical Gate-Type 3-D NAND

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Abstract—In vertical gate (VG)-type 3-D NAND, reducing either channel polycrystalline silicon (PL) or intersilicon dioxide (OX), or both, allows packing more cells in a fixed volume. However, when programming cells in such an array, the neighbor top/bottom cells suffer significant threshold voltage (V_t) shift due to two unique mechanisms. The first mechanism is the fringing field of the programmed charges (Z-interference), whereas the second one is the degraded inhibited potential affected by the programmed PL channel, which is grounded (Z-disturbance). Z-interference happens before Z-disturbance, so it is more critical to the memory window. Optimizing PL/OX thickness or engineering the PL sidewall profile can balance the constraint of Z-interference and the demand of higher memory density. They are important guidelines when designing VG-type 3-D NAND memory.

Index Terms—Vertical gate (VG)-type 3-D NAND flash, Z-disturbance, Z-interference.

I. INTRODUCTION

BY STACKING multiple layers and punchthrough etching, 3-D NAND is believed to be capable of outpacing 1Z-nm 2-D NAND in density [1] and in cost.

There are two types of 3-D NAND depending on their channel arrangement. Vertical channel type [2]–[5] has the cell current flowing vertically, and the gate signals are horizontally shared. Vertical gate (VG) type [6]–[9] has the cell current flowing horizontally, and the gate signals are vertically shared.

The cell number in a VG-type 3-D NAND string is independent of the memory layers, so it is commonly believed that the VG-type 3-D NAND will not suffer cell current degradation after increasing more layers into an array.

This eases the sensing circuit design.

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2-layer array architecture of VG-type 3D NAND

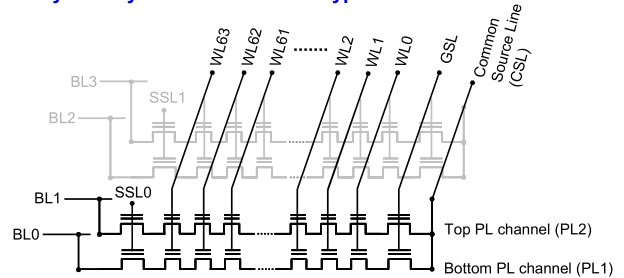


Fig. 1. Array architecture of two-layer VG-type 3-D NAND memory [10]. Charges are stored in the BE-SONOS film stack [11]. Each NAND string is selected by a combination of BL, SSL, and GSL. Bottom and top PL channels are routed to even and odd BLs.

Scaling down the z -direction pitch (i.e., PL thickness or OX thickness, or both) is a way to obtain an even higher 3-D NAND density when the aspect ratio of the punchthrough etching process is limited. However, Z-interference in the vertical direction [10] has been found worse after reducing the OX thickness. If the programming voltage is too high, Z-disturbance happens and further degrades the V_t window. Both Z-interference and Z-disturbance degrade the memory window of VG-type 3-D array, and a detailed study is needed to understand the underlying mechanisms.

This paper is organized as follows. Section II discusses the physics of inhibited top/bottom cells during programming and the impact to the memory window. Section III examines the Z-interference in eight-layer VG-type 3-D arrays with various PL/OX thickness designs. In Section IV, rounding PL sidewall profile is proposed to suppress the Z-interference and to improve the memory window. The concept is verified by simulation. Finally, the conclusion is drawn in Section V.

II. PROGRAMMING CHARACTERISTICS OF A VG-TYPE 3-D NAND

To study the programming characteristics of VG-type 3-D NAND, a simplified two-layer array is fabricated. Fig. 1 shows the array architecture [7], [9]. The memory cells are double-gated devices equipped with Bandgap-Engineered Silicon/Oxide/Nitride/Oxide/Silicon (BE-SONOS) films as their charge storage layer [11]. The channel PLs located in different layers are routed to different metal bitlines (BLs) through an MiLC design [9].

Z-pitch of VG-type 3-D NAND is the thickness sum of one PL and one OX. The minimum requirement of the

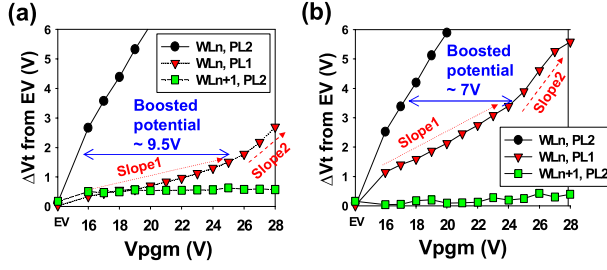


Fig. 2. Program behavior from two-layer arrays with different OX thicknesses. (a) PL/OX = 18/30 nm. (b) PL/OX = 18/12 nm. Both (a) and (b) suggest that the inhibited cell, which is below the programmed cell in the vertical direction, has a two-step V_t shift. The x-axis stands for the programming voltage (V_{pgm}) of selected WL, whereas the y-axis is the corresponding V_t shift from the erase verification state. The V_t shift increases when the OX thickness is reduced.

PL thickness is to guarantee a sufficient string current for read speed [10], [12]. The requirement of OX thickness is to provide enough PL-to-PL isolation and to reduce the cell-to-cell coupling [9], [13], [14]. Each NAND string can be decoded by a combination of metal BLs, island-gate string select lines (SSLs), and ground select lines (GSLs).

Identical to conventional 2-D NAND, the program inhibition of VG-type 3-D NAND is achieved by the self-boosting scheme. After turning OFF both SSLs and GSLs of deselected strings in either selected or deselected layers, the channel potential of inhibited cells is boosted, so the inhibited cells will not be programmed. The tunneling dielectric E -field of an inhibited cell in a selected wordline (WL) can be expressed as $(V_{pgm} - V_{boosted-channel})/EOT_{BE-SONOS}$. Here, V_{pgm} is the programming voltage, $V_{boosted-channel}$ is the boosted-channel potential of the inhibited cells, and $EOT_{BE-SONOS}$ is the effective oxide thickness of the BE-SONOS charge storage dielectric.

Fig. 2 shows the incremental step pulse programming (ISPP) and program inhibition behaviors from the two-layer cells with PL/OX = 18/30 nm or PL/OX = 18/12 nm. When programming a top WL_n cell, both V_t of the bottom WL_n cell and V_t of the top WL_{n+1} cell shift. The V_t shift of the top WL_{n+1} cell is minor and independent to the Z-pitch. On the contrary, V_t of the bottom WL_n cell is larger and strongly affected by the choice of Z-pitch, especially in the case of PL/OX = 18/12 nm.

The inhibited bottom WL_n cell (red lines) in both Fig. 2(a) and (b) shows two different slopes of V_t shift when increasing V_{pgm} from 16 to 28 V. Each slope is governed by its unique mechanism, which will be further discussed in the following paragraphs.

A. Z-Interference

Regarding the first slope, such as the cell-to-cell interference in 2-D NAND, the V_t shift is primarily affected by the amount of the stored charges and the distance between the programmed cell and the inhibited cell. When a top cell is programmed, the injected electrons change the electrostatic potential of the bottom inhibited channel. This phenomenon is clearly shown in Fig. 3(a).

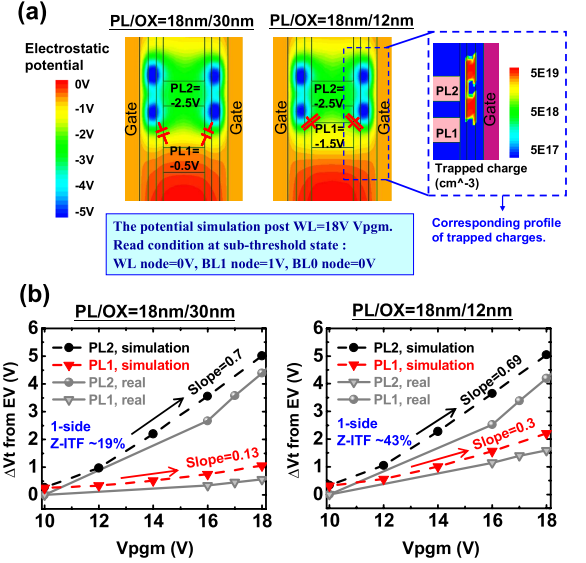


Fig. 3. (a) One-side Z-ITF simulation corresponding to different OX thicknesses at low programming voltage (18 V). The charges in the top layer cell extend along the z-direction and increase V_t of the bottom layer, especially when decreasing OX thickness. The V_t shifts of the programmed/inhibited cells with (b) PL/OX = 18/30 nm and PL/OX = 18/12 nm.

Already shown in Fig. 2, the $V_{boosted-channel}$ values of the inhibited cells are 9.5 and 7 V when shrinking the OX thickness from 30 to 12 nm. The corresponding $V_{pgm} - V_{boosted-channel}$ is not high enough to cause F-N tunneling in the inhibited cells when $V_{pgm} < 24$ V. Thus, the first slope of the inhibited cell is purely a consequence of the fringing field penetration from charges in the programmed cell. In other words, there is no real charge injection into the storage layer of inhibited cells (i.e., the nitride film of BE-SONOS), and the V_t shift, here, is only due to the charge coupling effect along the vertical direction. This V_t shift is called Z-interference, and it increases after scaling the OX thickness. It should be noted that the higher E -field at PL channel corners in Fig. 3(a) leads to more charge injection away from the corners (as shown in the zoomed-in plot) and thus worsens the Z-interference after programming.

Fig. 3(b) shows that, when scaling the OX thickness from 30 to 12 nm, the slope of the V_t shift in the inhibited cell increases from 0.13 to 0.3. To quantify the Z-interference, we introduce a parameter, Z-interference factor (Z-ITF), which is defined as the ratio of the V_t shift of an inhibited cell to the V_t shift of a programmed cell in the vertical direction ($V_{pgm} \leq 24$ V). Z-ITF is formulated as

$$\begin{aligned} \text{Z-ITF} &= \frac{\Delta V_t (\text{inhibited cell, WL}_n)}{\Delta V_t (\text{programmed cell, WL}_n)} \\ &= \frac{\text{ISSP_slope} (\text{inhibited cell, WL}_n)}{\text{ISSP_slope} (\text{programmed cell, WL}_n)}. \end{aligned} \quad (1)$$

Simulation shows that the two-layer devices [Fig. 3(b)] with 30-nm OX can have Z-ITF = 19% to the bottom cell when programming its top neighbor. However, Z-ITF becomes 43% when the OX is scaled to 12 nm, which results in a serious memory window loss. To maintain enough memory window

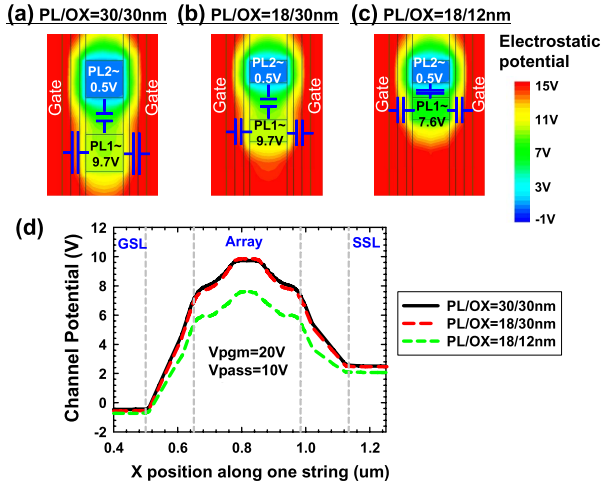


Fig. 4. (a)–(c) Boosted potential of the inhibited NAND string associated with different PL/OX thicknesses. The selected WL is applied with 20 V, and the pass gate voltage of other WLs (V_{pass}) is 10 V. (d) Boosted-channel potential decreases when shrinking OX thickness is from 30 to 12 nm, whereas no obvious impact on the boosted-channel potential is seen when shrinking PL thickness is from 30 to 18 nm.

for multilevel cell (MLC) operation, the Z-ITF should be suppressed and the scaling of OX thickness should be limited. Z-ITF posts a fundamental limit to the path of increasing VG-type 3-D NAND.

B. Z-Disturbance

As for the second slope of V_t shift in the inhibited cell, the mechanism stems from the channel coupling effect during programming operation. Soft programming causes the V_t shift in this regime, and it is called Z-disturbance. In VG-type 3-D array architecture, $V_{\text{boosted-channel}}$ of the inhibited cell is determined by the capacitive coupling from WLs with V_{pgm} and the adjacent channels as well. $V_{\text{boosted-channel}}$ of the inhibited cell is reduced when its top and bottom channels are biased at 0 V for programming. When that happens, the inhibited cell is more vulnerable to soft programming. Such a phenomenon is a unique feature of VG-type 3-D NAND, because multiple PL channels are stacked vertically [10], [13].

The channel coupling effect during programming is verified by Technology Computer-Aided Design (TCAD) and shown in Fig. 4. The channel of the inhibited cell (PL1) is floating, so the PL1 potential is determined by the surrounding conductors, including gates (WLs) and the neighbor channel (PL2). The electrostatic potential of the inhibited channel (the bottom layer) is lowered due to the presence of the programmed channel (the top layer), which is 0.5 V in this case. If the self-boosted-channel potential is degraded too much, electron injection from the deselected channel into the nitride layer happens. Simulation clearly suggests that the coupling effect has strong OX thickness dependence, as shown in Fig. 4(c) and (d).

PL1 potential is degraded from 9.7 to 7.6 V when the OX is shrunk from 30 to 12 nm. On the contrary, Z-disturbance is not sensitive to PL thickness.

The VG-type 3-D NAND intrinsically possesses better gate controllability compared with 2-D NAND and can offer

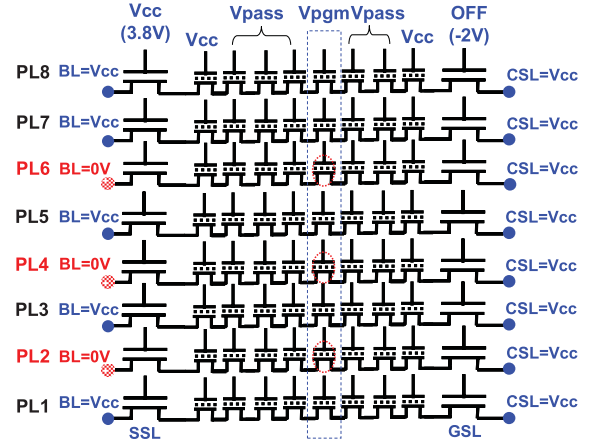


Fig. 5. Schematic of an eight-layer VG-type 3-D array and the programming biasing voltages. Selected layers are PL2, PL4, and PL6. Cells in PL3 and PL5 suffer two-side Z-interference, whereas cells in PL1 and PL7 suffer one-side Z-interference.

superior $V_{\text{boosted-channel}}$ (i.e., >9 V with OX = 30 nm) due to the double-gated feature. Nevertheless, the channel potential of inhibited cells is coupled to the neighbor channels and can be degraded by the neighbor channels when they are grounded for programming. This is particularly worsened after scaling OX thickness. Therefore, the second side effect of scaling OX is the worse Z-disturbance.

Recent studies [15] have shown that the Z-disturbance can be mitigated by modifying the programming algorithm. The new algorithm divides programmed data into different groups to avoid some data patterns, which results in Z-disturbance. Because Z-interference happens before Z-disturbance and Z-disturbance can be solved by programming algorithm, only Z-interference is critical to the memory window design of VG-type 3-D NAND.

III. Z-INTERFERENCE ON VG-TYPE NAND ARRAYS HAVING MORE THAN TWO LAYERS

A. One-Side Z-Interference and Two-Side Z-Interference

For a VG-type 3-D NAND array with more than three layers, Z-interference for the cells in the middle layer becomes larger (i.e., when cells both above and beneath an inhibited one are programmed at the same time, the inhibited cell suffers two-side Z-interference). To quantify the magnitude of one-side Z-interference and two-side Z-interference, we test an eight-layer VG-type 3-D NAND array. This eight-layer array is composed of 64 WLs in each string with BL pitch = 86 nm and WL pitch = 86 nm. Hence, the effective feature size corresponding to 2-D NAND array is ~ 15 nm. The array architecture and the corresponding operation for programming are shown in Fig. 5.

The Z-pitch is composed of a 30-nm PL and a 30-nm OX. Cells at the second layer (PL2), fourth layer (PL4), and sixth layer (PL6) are programmed simultaneously. This is done by forcing BLs to the selected layers to be 0 V, whereas the other BLs to the deselected layers are biased at $V_{\text{cc}} = 3.8$ V for inhibiting. Similar to 2-D NAND, the selected GSL is turned OFF (-2 V) to boost the channels of the inhibited strings.

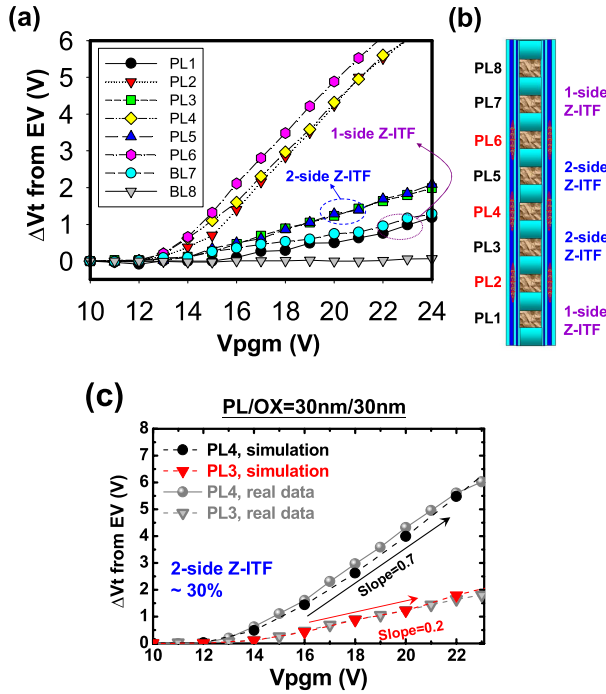


Fig. 6. (a) ISPP and program inhibition behaviors of an eight-layer array with PL/OX = 30/30 nm. The one-side Z-ITF is 15%, whereas the two-side Z-ITF is 30%. (b) Illustration of one-side of a two-side Z-ITF of an eight-layer device. (c) Two-side Z-ITF comparison between simulation and experimental data.

As shown in Fig. 6(a), the V_t shift of the topmost layer, namely, PL8 in this eight-layer array, almost keeps constant with respect to V_{pgm} , because no charge is stored in its neighbor bottom cell in PL7. As to the cells in PL7 and PL1, they suffer the one-side Z-ITF, which is $\sim 15\%$ of the programming window. Cells on PL3 and PL5 suffer the two-side Z-ITF, which is $\sim 30\%$. Experimental data confirm that the two-side Z-ITF is $2\times$ of the one-side Z-ITF. Z-ITF positively shifts V_t of erase state cells, leading to a wider V_t distribution of the erase state, and equivalently reduces the available memory window.

B. PL and OX Thicknesses Effect on Two-Side Z-ITF

Fig. 7(a) shows the simulation data together with the experimental data of two-side Z-ITF with respect to different PL or OX thicknesses. When increasing OX thickness for a given PL thickness, the two-side Z-ITF decreases remarkably because the stored electrons in the top and bottom neighbor cells have less influence on the inhibited cell. As shown in Fig. 7(b), the channel potential of an inhibited cell is coupled both by the sidewall gates and by the stored electrons in the top/bottom cells during read operation. Using a thicker PL can slightly reduce two-side Z-ITF because the portion of unaffected channel increases.

Thus, the two-side ITF can be reduced by increasing either PL or OX thickness, whereas OX plays a more critical role than PL. Fig. 8 shows that the two-side Z-ITF can be suppressed from 18% to less than 5% by increasing the OX thickness from 45 to 75 nm.

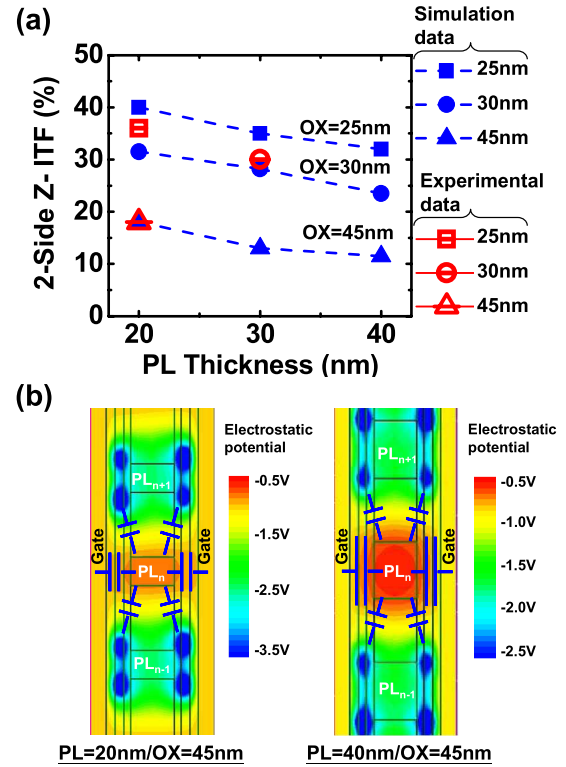


Fig. 7. (a) Simulation and experimental data of two-side Z-ITF with respect to various PL/OX thicknesses. In general, thicker OX leads to smaller Z-ITF because the stored charges of adjacent layers have less influence on the inhibited cells. (b) Channel potential of inhibited cell is coupled both by sidewall gate and by stored electrons in the top/bottom neighbor cells during read operation. Using thicker PL can slightly reduce the Z-ITF.

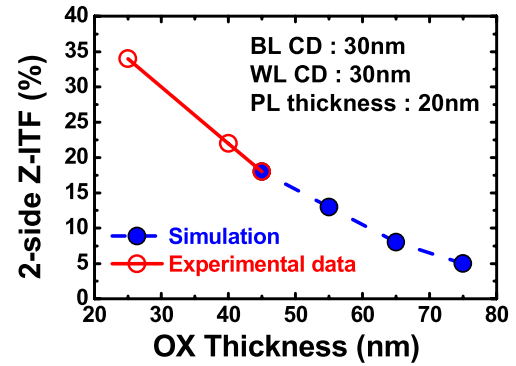


Fig. 8. Two-side Z-ITF as a function of OX thickness when the PL thickness is 20 nm. The two-side ITF is predicted to be reduced from 18% to less than 5% when OX thickness is increased from 45 to 75 nm.

Although increasing the Z-pitch reduces the Z-interference and leaves a larger window for MLC operation, the total array stack height and aspect ratio increase.

Those are not good in terms of the process integration and the memory design density. To conclude this session using the results of Figs. 7 and 8, a Z-pitch composed of PL/OX = 20/45 nm is a good compromise achieving acceptable device performance and reasonable stack height for process integration. The PL thickness is kept at 20 nm for maintaining sufficient read current above 100 nA [10].

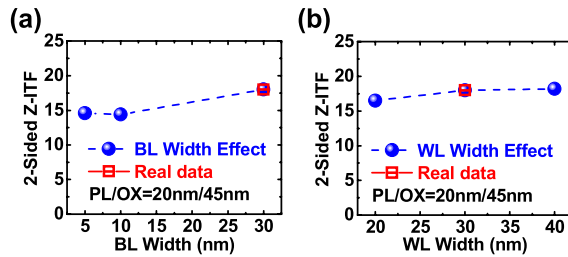


Fig. 9. Simulation of two-side Z-ITF with different BL or WL CDs. (a) Narrower BL CD slightly improved two-side Z-ITF. (b) Two-side Z-ITF is insensitive to the WL CD because the gate coupling ratio is similar to different WL dimensions.

On the contrary, the minimal OX thickness should be 45 nm to suppress the two-side Z-ITF below 20%. Therefore, the total stack height of the eight-layer array with the designed PL/OX thicknesses would be ~ 520 nm, which is similar to that of [9].

C. Effect of BL and WL Critical Dimensions on Two-Side Z-ITF

The effect of the BL critical dimension (CD) and the WL CD on Z-interference is also examined by simulation (Fig. 9). Narrower BL CD is expected to yield a smaller two-side Z-ITF, which could be attributed to the ultrathin body of thin-film transistor device and better depletion of channel body under the same gate bias. However, only little improvement is found (3%, from 18% to 15%) even when the BL CD is shrunk from 30 nm to less than 10 nm [Fig. 9(a)]. As to the WL CD effect, there is no apparent change of two-side Z-ITF, as shown in Fig. 9(b), after WL CD is shortened from 40 to 20 nm. This is because the gate coupling ratio is similar when adjusting the WL dimension. When altering the CD size, both the pitches of BL and WL are fixed at 86 nm (the sum of one line and one space). Changing the BL pitch would not change the value of Z-ITF at all, because the sidewall gate has shielding effect that blocks the influence of the programmed charges in the adjacent BL. For the effect decreasing the WL width, the total parasitic capacitance will be decreased, so Z-ITF is expected to be slightly lowered. However, the side effect of too narrow WL width (e.g., < 20 nm) lies in the creation of a high aspect ratio topology (e.g., > 30) in WL etching step. Because the Z-ITF is insensitive to either the BL or the WL CD size according to Fig. 9, both BL and WL CD are fixed at 30 nm as the baseline to meet the process capability previously demonstrated [9], [13].

IV. CHANNEL PL SIDEWALL PROFILE ENGINEERING FOR REDUCING Z-INTERFERENCE

TCAD simulation in Fig. 10(a) indicates that the root cause of Z-interference is the trapped electrons, which is too close to the adjacent channels and without being shielded.

A noticeable amount of trapped electrons that extend outside the channel is a consequence of higher E -field due to the corners of PL channel [16]. The extension of the trapped

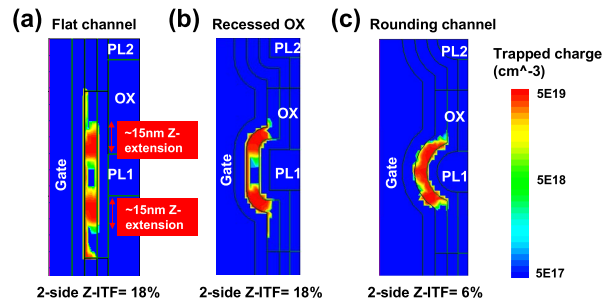


Fig. 10. Simulation of two-side Z-ITF with different channel shapes. (a) Flat channel shows a 15-nm Z-extension because a considerable number of electrons tunnel and spread around the channel corner region. (b) Recessed OX structure shows no improvement due to the similarly sharp corner of PL channel. (c) Recessed OX with rounding PL channel can reduce the two-side Z-ITF from 18% to 6%, owing to less extension of storage charges.

electrons, named as Z-extension, can be 15 nm away from the PL channel corner.

Another way to reduce Z-ITF is to shield the programmed charges by modifying the channel PL sidewall profile. Different channel sidewall shapes are checked. Here, we use a Z-pitch of 20-nm PL and 45-nm OX in TCAD simulation to evaluate the two-side Z-ITF. The OX is pulled back laterally [Fig. 10(b)] and even further rounded [Fig. 10(c)] to create a recessed profile before BE-SONOS and gate material deposition. By recessing the OX, the PL channels are wrapped by the gate to a certain extent. The flat channel device in Fig. 10(a) shows ~ 15 -nm Z-extension and 18% two-side Z-ITF, because there are a considerable number of electrons injected into the storage layer, which is too close to the neighbor channel [10]. The device in Fig. 10(b) has a surrounding gate structure, but the sharp corners of the PL channel create high corner E -field, which still results in appreciable amount of tunneling electrons and no improvement of two-side Z-ITF. In Fig. 10(c), the sidewalls of PL channel are rounded, and the two-side Z-ITF is reduced from 18% to 6%. Unlike the channel with sharp corners, the trapped charges are well confined along the surrounding gate without obvious Z-extension. Moreover, the surrounding gate shields the trapped charges. Our simulation data confirm that the rounded PL channel is a promising way to solve the unique Z-interference issue in VG-type 3-D NAND array.

Fig. 11 compares the memory window with various two-side Z-ITF values. In the V_t distribution simulation, 16 Mb from an eight-layer array, checkerboard programming scheme, 64 WLs, and 16 SSLs are assumed. The ISPP slope of each cell is assumed to be 0.8. The V_t sigma values of dumb programming distribution and random telegraph noise are 400 and 60 mV, respectively. As shown in Fig. 11(a), the shift of erase state high bound can be reduced by more than 1 V after decreasing the two-side Z-ITF from 18% to 6%. On the contrary, when the Z-interference increases, the erase state V_t distribution becomes wider. Once the two-side Z-ITF reaches 18%, a non-Gaussian distribution is observed. Layer-by-layer analysis in Fig. 11(b) shows that such a non-Gaussian behavior is due to the different amounts of the Z-interference in different layers. Cells in the topmost and

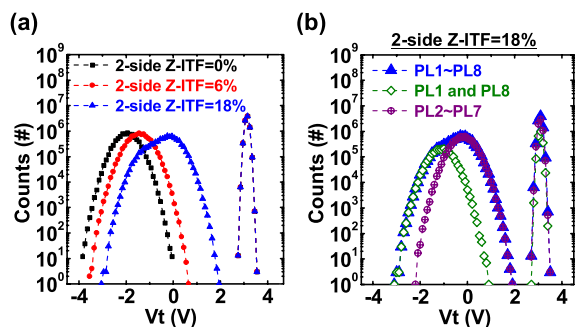


Fig. 11. Memory window simulation with various Z-ITF values. (a) There will be more than 1 V improvement in memory window when the two-side Z-ITF is reduced from 18% to 6%. (b) Non-Gaussian erase state distribution is caused by the inhibited cells in the topmost and the bottommost layers.

bottommost layers are only subjected to one-side Z-ITF, and cells in the other layers suffer two-side Z-ITF. In other words, larger Z-interference not only shifts the erase state distribution peak but also widens the erase state distribution. Engineering channel PL sidewall profile and optimizing Z-pitch are must to reduce the Z-ITF magnitude and ensure a sufficient single-level cell and MLC memory windows.

V. CONCLUSION

VG-type 3-D NAND flash memory with various Z-pitch designs (PL/OX stack thicknesses) is extensively studied in this paper. The memory window is significantly affected by Z-interference, which is a unique behavior in VG-type array. Using a thicker OX improves the Z-interference but makes WL etching process more challenging. The best combination of the PL and OX thicknesses is determined to be 20 and 45 nm, respectively. Simulation results suggest that the two-side Z-ITF can be further reduced to 6% by using rounded PL sidewalls, because of the shielding effect of surrounding gate and less Z-extension of programmed electrons. With such device designs, the memory window of VG-type 3-D NAND can be improved to meet the requirements of high-density applications.

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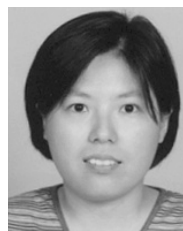
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