JARED BOBROW (STATE BAR NO. 133712)
jbobrow@orrick.com
JASON LANG (STATE BAR NO. 255642)
jlang@orrick.com
DIANA M. RUTOWSKI (STATE BAR NO. 233878)
drutowski@orrick.com
ORRICK, HERRINGTON & SUTCLIFFE LLP
1000 Marsh Road
Menlo Park, CA 94025-1015
Telephone: +1 650 614 7400
Facsimile: +1 650 614 7401

Attorneys for Defendant and Counter-claim Plaintiff Micron Technology, Inc., and Defendant Micron Consumer Products Group LLC

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD., Plaintiff, v. MICRON TECHNOLOGY, INC., et al., Defendants.	Case No. 3:23-cv-05792-RFL **DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND DOCUMENT PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS RE YMTC II ASSERTED PATENTS (PATENT LOCAL RULES 3-3 AND 3-4)** Honorable Rita F. Lin
MICRON TECHNOLOGY, INC., Counterclaim Plaintiff, v. YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD., and YANGTZE MEMORY TECHNOLOGIES, INC., Counterclaim Defendants.	[redacted]

YMTC
Exhibit 2001
Micron v. YMTC
IPR2025-00190

Ex. 2001-001

Pursuant to Patent Local Rules 3-3 and 3-4, Defendant Micron Technology, Inc. ("MTI") and Defendant Micron Consumer Products Group LLC (MCPG) (collectively "Micron" or "Defendants") hereby submit to Plaintiff Yangtze Memory Technologies Company, Ltd. ("YMTC" or "Plaintiff") these Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions relating to the YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4) ("Invalidity Contentions").

I. INTRODUCTION

These Invalidity Contentions are based on Defendants' current knowledge of the 11 patents asserted by YMTC in this case, namely 11 patents YMTC first asserted against Micron in another complaint filed and later consolidated with this case (U.S. Patent Nos. 10,879,254 ("'254 Patent"), 11,581,322 ("'322 Patent"), 10,886,291 ("'291 Patent"), 11,482,532 ("'532 Patent"), 11,145,666 ("'666 Patent"), 11,450,604 ("'604 Patent"), 10,672,711 ("'711 Patent"), 11,101,276 ("'276 Patent"), 11,568,941 ("'941 Patent"), 10,879,164 ("'164 Patent"), and 12,010,838 ("'838 Patent") (together, "YMTC II Asserted Patents," "Asserted Patents" or "patents-in-suit")), the prior art located to date, and Defendants' current understanding of Plaintiff's apparent claim interpretations.[1] Defendants continue to pursue discovery and to investigate and analyze the prior art.

Deficiencies in Plaintiff's Infringement Contentions have made it difficult for Defendants to understand Plaintiff's claim construction and infringement positions. Micron has attempted to seek clarification of Plaintiff's claim constriction and infringement position through discovery, however, to date Defendants have not received this information. *See, e.g.*, Plaintiff and Counterclaim Defendants' Responses to First Set of Requests for Production (Nos. 1-81), Request Nos. 10, 12, 16, 32. Accordingly, Defendants' Invalidity Contentions are based on Defendants'

[1] Defendants' understanding of Plaintiff's apparent claim interpretation is based on YMTC's Disclosure of YMTC II Asserted Claims and Infringement Contentions pursuant to Local Patent Rules 3-1 and 3-2 dated October 2, 2024, as to the YMTC II Asserted Patents ("YMTC II Infringement Contentions" or "Infringement Contentions"). Defendants' understanding is further based on YMTC's Consolidated Complaint filed on September 3, 2024, and First Amended Consolidated Complaint filed on October 8, 2024.

present understanding of Plaintiff's apparent positions as to the scope of the claims asserted by Plaintiff (at times, "Asserted Claims"). By explaining how the prior art invalidates the Asserted Claims, Defendants are neither adopting nor acceding in any manner to Plaintiff's claim construction or infringement positions. Furthermore, the statements herein shall not be treated as an admission or suggestion that Defendants agree with Plaintiff regarding either the scope of any of the Asserted Claims or with the claim constructions that Plaintiff appears to advance in its infringement contentions or anywhere else. Nor shall anything in these Invalidity Contentions be treated as an admission that any of Defendants' products or instrumentalities meet any limitations of the claims.

To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in Asserted Claims, Defendants are not proposing any such constructions as the proper constructions of those terms or phrases at this time. For example, certain of these Invalidity Contentions, including the charts attached hereto, may be based on claim constructions that appear to underlie Plaintiff's Infringement Contentions.[2] Defendants, however, do not concede that Plaintiff's apparent constructions are proper, and they reserve the right to contest any such constructions. Moreover, nothing herein admits in any way that any Accused Instrumentality, or any of Defendants' other products, methods, or services, infringes any of the Asserted Claims. Defendants reserve the right to supplement, modify, or amend these Invalidity Contentions as allowed by Patent L.R. 3-6 or as otherwise permitted.

The information that Defendants provide and the documents that Defendants produce are provisional and subject to further revision. Defendants expressly reserve the right to amend the disclosures and document production herein if, for example, Plaintiff provides any information that it failed to provide in its infringement contentions or if Plaintiff attempts to amend its infringement

[2] Plaintiff's Infringement Contentions are inconclusive, vague, and not compliant with the Patent Local Rules. In addition, they appear to be based on an improperly broad interpretation of the Asserted Claims. Thus, certain of these Invalidity Contentions may likewise be based on Plaintiff's overbroad interpretation. Defendants reserves the right to supplement and/or modify these Invalidity Contentions if, for example, Plaintiff modifies its positions regarding the scope of the Asserted Claims (*e.g.*, by amending its Infringement Contentions).

contentions in any way. Further, because Plaintiff's failures have prevented Defendants from completing their search for and analysis of relevant prior art, Defendants reserve the right to revise, amend, and/or supplement the information provided herein, including identifying and relying on additional references, should Defendants' further search and analysis yield additional information or references, consistent with this Court's orders and the Federal Rules of Civil Procedure. Moreover, Defendants reserve the right to revise its ultimate contentions concerning the invalidity of the Asserted Claims, which may change depending upon the Court's construction of the Asserted Claims and/or positions that Plaintiff or its expert witness(es) may take concerning issues of claim construction, infringement, and/or invalidity.

Prior art not included in this disclosure, whether known or not known to Defendants, may become relevant. For example, Defendants are currently unaware of the extent to which Plaintiff will contend that limitations of the Asserted Claims are not disclosed in the prior art identified herein. To the extent that such an issue arises, Defendants reserve the right to identify additional teachings in the same references or other references that disclose or render obvious the allegedly missing limitation(s).

Defendants' accompanying claim charts cite to particular teachings and disclosures of the prior art as applied to the limitations of the Asserted Claims. Although Defendants have complied with Patent L.R. 3-3's directive to identify "specifically where and how in each alleged item of prior art each limitation of each asserted claim is found," Defendants have not necessarily identified each and every disclosure of an element in a reference in an effort to avoid redundancy. Similarly, the lack of a citation for an element should not be deemed an admission that the element is not disclosed or is not inherent in the reference. In an effort to focus the issues, Defendants are identifying exemplary portions of the cited references from which Plaintiff can easily ascertain Defendants' invalidity theories. Moreover, Defendants are not providing the complete universe of knowledge held by a person of ordinary skill in the art ("POSA"). As such, the cited portions of references are only examples, and Defendants reserve the right to rely on uncited portions of the prior art references, other publications, and expert testimony as aids in understanding and interpreting the cited portions, as providing context thereto, and as additional evidence that a claim

limitation is known or disclosed. Defendants further reserve the right to rely on uncited portions of the prior art references, other publications, and testimony to establish bases for combinations of certain cited references that render the Asserted Claims obvious. Where Defendants cite to a particular figure in the accompanying charts, the citation encompasses the description of the figure, as well as any text associated with the figure. Similarly, where Defendants cite to particular text concerning a figure, the citation encompasses that figure as well.

Throughout the attached Exhibits, Defendants provide examples of where references disclose subject matter recited in preambles, without regard to whether the preambles are properly considered to be limitations of the Asserted Claims. Defendants reserve the right to argue that any claim elements of the Asserted Claims (including preambles) do not in fact limit the scope of the Asserted Claims.

The references discussed in the claim charts or elsewhere identified may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or may be relied upon to show the state of the art in the relevant time frame. Defendants' proposed obviousness arguments or obviousness combinations are provided in the alternative to Defendants' anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not by itself anticipatory.

These Invalidity Contentions address only those claims that Plaintiff has asserted in its Infringement Contentions. Defendants reserve the right to supplement these contentions if Plaintiff attempts to assert any claims not addressed in its Infringement Contentions or attempts to modify or revise its Infringement Contentions in any way.

Although these Invalidity Contentions may associate particular prior art patents and/or printed publications with a specific statutory subsection of 35 U.S.C. § 102, it should be understood that Defendants may also rely on these patents and/or printed publications under other subsections of Section 102. For example, where patents or printed publications are cited as evidence of the functionality of prior art public use or sale under § 102(a), it should be understood that such patents or printed publications are also being disclosed for use as prior art under the other provisions of § 102(a).

These contentions cite to the petitions for inter partes review ("IPR") that Micron has filed with the Patent Trial and Appeal Board. Plaintiff is well aware of those IPRs, and Micron fully incorporates those IPRs herein subject to the stipulations that Micron provided with those IPRs. Those IPRs identify, on a claim-by-claim basis, where the prior art in those IPRs discloses each claim element. Thus, those IPRs comply with the local rules and the IPRs are, in effect, claim charts. Further, those IPRs identify obviousness arguments and provide substantial detail regarding motivation to combine and reasonable expectation of success. Each such obviousness and motivation argument is incorporated herein. As the IPRs demonstrate, to the extent that Plaintiff argues that a limitation is not met by the prior art, it would have been obvious to provide that limitation in view of the prior art, as the IPRs detail. Such obviousness arguments are equally applicable to the prior art in these contentions, and these contentions thus incorporate those obviousness arguments here.

These contentions identify certain terms as indefinite, e.g., as a result of Plaintiff's apparent interpretation of those terms for purposes of infringement. Nothing about those contentions prevents the PTAB from ruling that the respective claims are unpatentable, because the PTAB is reviewing patentability outside of the context of Plaintiff's incorrect claim interpretations (which give rise to the indefiniteness) and because the prior art in Micron's IPRs discloses the claim limitations under any reasonable interpretation thereof.

Defendants are unaware of any secondary considerations of nonobviousness, and YMTC has yet to identify any alleged secondary considerations. Defendants will address any such considerations that YMTC properly identifies in response to Defendants' discovery requests or otherwise.

II. ASSERTED PATENTS AND CLAIMS

Plaintiff asserts the following claims from the YMTC II Asserted Patents (collectively, "Asserted Claims"):

YMTC II Asserted Patent	Asserted Claims
'254	1-15, 17-18, and 20
'322	1-20
'291	1-12 and 14-20

YMTC II Asserted Patent	Asserted Claims
’532	1-3, 7-8, 10, 11, 13, 15-18, and 20
’666	17, 19, and 20
’604	1-5, 8-13, and 15-20
’711	1-6 and 8-19
’276	1-5, 7-15, and 17-18
’941	1-14
’164	1-14
’838	1, 3-7, and 12-20

YMTC II Infringement Contentions at 1.

III. INVALIDITY OF THE ’254 PATENT

A. Invalidity Based on the Prior Art

As shown below, the alleged inventions of the ’254 Patent were well-known in the prior art. Those skilled in the art were aware of all of the limitations claimed in the ’254 Patent. Thus, many prior art patents, publications, products, and combinations thereof, disclose, teach, or embody every limitation of the Asserted Claims and thus invalidate those claims. Examples of these disclosures, teachings, and embodiments are identified in the following sections and in the attached claim charts.

1. Identification of Prior Art References (Patent L.R. 3-3(a))

Subject to the reservation of rights above, Defendants identify each item of prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the ’254 Patent. The patents/applications, publications, and systems identified are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations.

Some of the below citations and those in the corresponding invalidity claim charts involve prior art references that have corresponding related, foreign, and/or PCT counterpart publications. In such cases, where either the U.S. patent or related, foreign, and/or PCT counterpart is cited, it is to be understood that the corresponding disclosures from the counterpart patent and publications (which are substantively the same) are implicitly incorporated by reference in the alternative to avoid needless repetition.

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
I-01	U.S. 2019/0198524 ("Fujiki")	December 25, 2017[3]	June 27, 2019
I-02	U.S. 2019/0287894 ("Nakajima")	July 3, 2018	September 19, 2019
I-03	U.S. 2019/0081061 ("Tessariol")	September 14, 2017	March 14, 2019
I-04	U.S. 10,388,666 ("Kai3")	March 8, 2018	August 20, 2019
See IPRs[4]	U.S. 10,658,378 ("Tao")	May 3, 2018	May 19, 2020
See IPRs	U.S. 2017/0179026 ("Toyama")	December 22, 2015	June 22, 2017
See IPRs	U.S. 10,354,980 ("Mushiga")	March 22, 2018	July 16, 2019
See IPRs	U.S. 2019/0229125 ("Zhou")	January 22, 2018	July 25, 2019
See IPRs	WO 2019/042103 ("Dai")	August 28, 2017	March 7, 2019
See IPRs	U.S. 10,679,721 ("Kim")	March 8, 2017	June 9, 2020
See IPRs	U.S. 10,290,643 ("Kai")	January 22, 2018	May 14, 2019
See IPRs	U.S. 9,859,297 ("Park2")	March 10, 2015	January 2, 2018
See IPRs	U.S. 2018/0308559 ("Kim2")	April 25, 2017	October 25, 2018
See IPRs	U.S. 8,945,996 ("Tang")	April 12, 2011	February 3, 2015
See IPRs	U.S. 10,115,632 ("Masamori2")	April 17, 2017	October 30, 2018
See IPRs	U.S. 5,945,717 ("Chevallier")	March 11, 1997	August 31, 1999
See IPRs	U.S. 10,347,487 ("Lee 487")	November 14, 2017	July 9, 2019
See IPRs	U.S. 2019/0081061 ("Tessariol")	September 14, 2017	March 14, 2019
See IPRs	U.S. 9,620,514 ("Kai2")	September 5, 2014	April 11, 2017
See IPRs	U.S. 10,515,799 ("Wang")	May 24, 2018	Dec. 14, 2019
See IPRs	U.S. 9,570,460 ("Kanakamedala")	July 29, 2014	February 14, 2017
See IPRs	U.S. 9,728,546 ("Serov")	September 5, 2014	August 8, 2017

[3] The IPR demonstrates Fujiki is entitled to its foreign priority date.

[4] The IPRs provide the equivalents of charts by identifying relevant pinpoint citations.

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
See IPRs	U.S. 11,075,084 ("Shen")	August 31, 2017	July 27, 2021
See IPRs	U.S. 10,304,852 ("Cui")	February 15, 2018	May 28, 2019
See IPRs	U.S. 9,793,139 ("Sharangpani")	October 29, 2015	October 17, 2017
See IPRs	U.S. 10,714,341 ("Cohen")	December 31, 2015	July 14, 2020

Table I-1: Prior Art Patents and Patent Publications for the '254 Patent

Ex.	Title	Authors	Publisher	Date of Publication
See IPRs	"3D Flash Memories" ("Micheloni 2016")	Micheloni		2016
See IPRs	"NAND Flash Memory Technologies" ("Aritome")	Aritome		2016
See IPRs	"Optical lithography—a historical perspective" ("Ronse")	Ronse	C. R. Physique 7	2006
See IPRs	"Atomic Layer Deposition for Semiconductors" ("Hwang")	Hwang	Springer	2014
See IPRs	"Principles of CMOS VLSI Design" ("Weste")	Weste	Addison-Wesley	1993
See IPRs	"Silicon Processing for the VLSI Era, Volume 1-Process Technology" ("Wolf Vol. 1")	Wolf	Lattice Press	1986
See IPRs	"Silicon Processing for the VLSI Era, Volume 1-Process Integration" ("Wolf Vol. 2")	Wolf	Lattice Press	1990

Table I-2: Prior Art Non-Patent Publications for the '254 Patent

Defendants are still investigating prior uses and sales. Based upon at least Plaintiff's apparent position as to the scope of the Asserted Claims, and as further explained below and in the cited exhibits, it appears that the following systems (and development thereof) qualify as prior art under at least one or more of 35 U.S.C. § 102(a):

Ex.	Description	Entities Involved	Prior Art Date
I-05	120 Series Products	Micron	1/11/2018

Table J-3: Prior Art Systems for the '254 Patent

Micron's 120 series products were publicly available, on sale, or in public use prior to the

effective filing date of the ’254 Patent. MYM0042611-MYM0042676, MYM0042896-MYM0042896, MYM0065110, MYM0065111.

Description	Availability
Travelers	to be made available via inspection
Process information	to be made available via inspection
Schematics	to be made available via inspection
Layouts	to be made available via inspection
Waveforms	MYM0042897-MYM0043247, MYM0069190-MYM0069236
TEM/SEM Imagery	MYM0043255-MYM0043296, MYM0043316-MYM0043339, MYM0043423-MYM0043424, MYM0043248-MYM0043254, MYM0058889-MYM0058891, MYM0069181-MYM0069181
Datasheets	MYM0043425-MYM0043844, MYM0065164-MYM0066151
Trim Spreadsheets	MYM0065112-MYM0065115, MYM0069182-MYM0069189, MYM0069715-MYM0069940

Table J-4: Listing of Prior Art Systems Documentation for the ’254 Patent

2. Anticipation and Obviousness (Patent L.R. 3-3(b) and (c))

The Asserted Claims of the ’254 Patent are invalid because they are anticipated by the prior art and/or because they would have been obvious in view of the prior art.

The prior art identified by Defendants anticipates and/or renders obvious one or more of the Asserted Claims of the '254 Patent under at least AIA §§ 102(a)(1), 102(a)(2), and 103. For each prior art reference, Defendants have provided claim charts attached to these Invalidity Contentions as Exhibits I-1 through I-05. These charts identify where each element of each Asserted Claim can be found in each item of prior art. In addition to the above identified claims charts, Micron hereby incorporates by reference IPR2025-00034 filed with the United States Patent and Trademark Office on October 11, 2024.

Again, to the extent not anticipated, the Asserted Claims of the '254 Patent are invalid as obvious under 35 U.S.C. § 103. Each prior art reference identified in the preceding sections—either alone or in combination with another prior art reference and/or in combination with the knowledge of one skilled in the art—renders the Asserted Claims invalid as obvious. In rendering the Asserted Claims obvious, each prior art reference identified in the preceding sections may be combined with: (1) information known to persons skilled in the art at the time of the alleged invention, (2) any of the other anticipatory or obviousness prior art references, (3) any statements in the intrinsic record of the '254 Patent and related applications, or (4) any of the additional prior art identified below.

3. Motivations to Combine[5]

A person of ordinary skill in the art would have been motivated to combine the preceding references (*see* Section III.A.1) for the following reasons. Teachings, suggestions, motivations and/or reasons to modify any of the references and/or to combine any two or more of the references can come from many sources, including the prior art (by specific reference and when read as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obviousness to try, the nature of the problem faced, and/or knowledge possessed by a person of ordinary skill.

Although a patent claim may be invalidated based on a teaching-suggestion-motivation ("TSM") rationale—*i.e.,* that some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference

[5] The statements in this section about what was known and obvious to a POSA are made with respect to the effective filing date of the '254 Patent.

teachings to arrive at the claimed invention—the Supreme Court identified additional rationales in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007). The following of these rationales apply here:

> (A) the asserted claims combine prior art elements according to known methods to yield predictable results;
>
> (B) the asserted claims involve the simple substitution of one known element for another to obtain predictable results;
>
> (C) the asserted claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;
>
> (D) the asserted claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;
>
> (E) the asserted claims involve combinations of prior art references that would have been "obvious to try"'—a person of ordinary skill in the art could have reached the asserted claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
>
> (F) the asserted claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach); *see also* Department of Commerce, Patent and Trademark Office, Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.,* 72 Fed. Reg. 57,526 (Oct. 10, 2007). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420-21.

Thus, even in the absence of a specific teaching, suggestion, or motivation to combine references, the Asserted Claims here are obvious and therefore invalid. Each of the cited references or devices is in the same field as the '254 Patent, making it obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. One of ordinary skill in the art would have recognized that improvements could be achieved by combining or modifying prior art references that described such improvements. Each of the above prior art references

describes systems, products, or methods that were known to offer such improvements, and, accordingly, one of ordinary skill in the art would have been motivated to combine or modify the references as identified in each of the combinations below.

Furthermore, because each prior art reference concerns three-dimensional NAND memory designs, common industry knowledge supplied a reason to combine any one the above references. It was well understood that different three-dimensional NAND memory structural features could be employed together or interchanged with each other, fitting together like puzzle pieces. Each combination would have produced predictable results and would simply represent a known alternative to one of ordinary skill in the art of NAND memory. This is a further motivation to combine any of the above references.

The below sections further address particular reasons to combine the above references. The below should not be construed as an admission that there is any value to the alleged invention of the ’254 Patent. As discussed previously, these contentions are based in significant part on how Plaintiff is apparently construing the asserted claim in its Infringement Contentions, which is an incorrect and overbroad interpretation of the alleged invention of the ’254 Patent. Accordingly, to the extent the below refers to benefits of certain elements or industry trends towards these elements, this is not an admission that the alleged invention of the ’254 Patent provides any benefits: to the contrary, properly construed and compared to the prior art, the ’254 Patent provides no benefits. Likewise, to the extent the below refers to substituting elements, this is not an admission that the elements subject to the substitution are in any way similar, *e.g.,* perform the same function, in the same way, to achieve the same result.

The various elements of the Asserted Claims were well known in the prior art at the time of the alleged invention, and the combination would have been obvious to one of skill in the art. The combinations simply (a) combine prior art elements according to known methods to yield predictable results; (b) involve the simple substitution of one known element for another to obtain predictable results; (c) involve the use of a known technique to improve similar devices (methods, or products) in the same way; (d) apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) involves combinations of prior art references

that would have been "obvious to try" – a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and/or (f) would have been prompted by known work, based on design incentives or other market forces, because such variations were predictable to one of ordinary skill in the art.

Moreover, the Supreme Court has stated that a motivation to combine may be simply "common sense" and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420. Indeed, the Supreme Court held that it is sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421. Here, all the claim elements are common sense and are easily fit together by one of ordinary skill in the art.

While not necessary, a motivation to combine may also be found in the references themselves. One of skill in the art would have been motivated to combine a reference that refers to, or otherwise explicitly invites combination with, another reference. Where the references cited herein have such an explicit invitation to combine, that invitation would have motivated one of skill in the art to combine any such references.

Micron hereby identifies the following '254 Patent Primary References: Fujiki, Nakajima, and Tessariol.

The below provides several exemplary combinations and motivations for combining an '254 Patent Primary Reference with another reference.

a. Dielectric / Sacrificial Pairs

To the extent any '254 Patent Primary Reference is determined to be missing the claimed "dielectric/sacrificial layer pairs" a POSA would have considered it obvious and been motivated to form dielectric sacrificial pairs.

Sacrificial gates were textbook material, i.e., forming sacrificial gates and replacing them with metal gates later in the fabrication process. Micheloni, 115-16. The advantages were well known, including that it increases access speed. *Id.*

A POSITA would have had a high expectation of success in implementing sacrificial gates for the gate replacement process. Again, it was textbook material. *Id.* In addition, it does not otherwise change the 3D design, other than requiring support structures. However, as Tessariol teaches, TAC and other support structures were well known. Tessariol, [0029]-[0032], [0041]. Thus, to the extent any '254 Patent Primary Reference is determined not to disclose this limitation, it would have been obvious in view of Tessariol and/or Micheloni.

b. Forming channel structures before TACs and slits

To the extent any '254 Patent Primary Reference is determined to be missing the claimed "forming a channel structure extending vertically through the stack" a POSA would have considered it obvious and been motivated to so form channel structures.

For example, to the extent that it is to argued that forming the channels must occur before the TACs and slits, it would be incorrect, because this limitation does not recite when it occurs (compare the final limitation, which does state a relative time when it occurs). Regardless, it would have been obvious. For example, Nakajima forms the channels before the TACs and slits. Nakajima focuses on the manufacture of the TACs, and thus starts the description of the manufacturing process there. Nakajima, 7:5-8. There, Nakajima discloses forming the TACs (C4s), forming the slits, and then replacing the sacrificial gates. *Id.*, 7:5-8:23. Nakajima describes that the channel pillars support the structure during the gate replacement process, and thus it would have been understood, and certainly obvious, that Nakajima discloses forming the channels before the TACs (C4) and slits, because the description assumes that the channels have already been made before the C4 structures. *Id.*, 8:24-33. For these and the reasons discussed below, a POSA would have also found in obvious and been motivated to form dummy channels structures before formed TACs and slits. Thus, to the extent any '254 Patent Primary Reference is determined not to disclose this limitation, it would have been obvious in view of Nakajima and Kai, Kim, and/or Park (see below).

c. Forming dummy channels

To the extent any '254 Patent Primary Reference is determined to be missing the claimed "prior to forming the first opening, forming a dummy channel structure extending vertically through the stack" a POSA would have considered it obvious and been motivated to so form dummy channel structures, e.g., in view of Kai, Kim, and/or Park.

For example, it would have been obvious to implement dummy channel structures in the '254 Patent Primary References. Kai, for example, discloses forming active and dummy channels, which provide structural support. Kai, 9:23-26 (defining "support opening" as "a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed"), 9:45-48 ("support openings 19" extend through stack), 10:20-27 (forming channels in support openings). Kai refers to the dummy channels as "support pillar 20" and active channels as "memory stack structured." *Id.*, 16:28-38; Fig. 15A, 25:58-63 (dummy support channels (20) have no connection to the upper level, whereas the active channel structures (55) include contacts (88)). Park, likewise, discloses active and dummy, supporting channels. Park, 6:19-26, 7:45-51. Kim, too, forms dummy channels and dummy channels through the stack at the same time. Kim2, [0047] ("The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region CTR," "DS may physically support," and listing same materials as channels), [0071] ("The channel holes CH and the dummy holes DH may be formed at the same time."), [0072] (same time), Fig. 13 (DH through stack on edge). It was known that to perform this gate replacement process, "support pillars" were necessary. Tang, 5:64-6:2, 7:19-23.

A POSITA would have been motivated to employ dummy channels through the stack for several reasons. First, it is advantageous to use dummy channels as support structures because they can be made by the same process and at the same time as the active channels. Kai, 10:20-27. Second, dummy channels do not require connections to the upper-level devices, thereby not consuming space above the structures while also serving as support structures. Park, 8:55-65. Third, it was well known to include dummy support members, including ones that travel through the entire stack or partially through the stack. Kai, Fig. 6A (support members 20), 16:28-38. It was well known that adding additional dummy channels "provide[s] additional structural support

during replacement of the [sacrificial gate layers]." Masamori2, 30:14-27; *see also id.*, 15:3-22 (structures 20 are dummy channel structures). Fourth, adding the additional dummy structures would result in reducing the likelihood of defective bits on the edge of the memory cell region, because the addition of the additional rows extends the memory cell pattern for those respective columns into the dummy region. It was well known that when a pattern stops (instead of extending into the dummy region), defects occur on the edge. Chevallier, 8:47-53 and Lee 487, 2:20-43 (both explaining the edge effect). Fifth, adding the additional dummy structures would result in an overall more uniform feature pattern, which reduces processing issues. Ronse, 11 (explaining this processing issue).

Adding dummy structures would have been routine and a POSITA would have had a high expectation of success. First, as the above discusses, 3D memory references already disclose forming channel structures, and the same materials are used for dummy channels. Second, for the reasons above, the additional dummy channel structures would actually reduce processing issues. Third, as the above demonstrates, dummy channels were commonplace.

d. Depositing dielectric layers using atomic layer deposition

To the extent any '254 Patent Primary Reference is determined to be missing the claimed "wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD)" a POSA would have considered it obvious and been motivated to so deposit dielectric layers, e.g., in view of the prior art below.

It was well known to deposit a dielectric liner, including silicon oxide, in a hole or trench through a memory stack via ALD. Toyama, [0226] (backside trench 79), [0313] (moat trenches 579); Kai2, 35:51-61 (forming "dielectric spacer" by first forming "silicon oxide layer" via "ALD"); Tessariol, [0063] (ALD), [0038] (conductive vias 58). A POSITA would have been motivated to employ ALD given that it provides a conformal deposition. ALD became popular in large part due to its ability to deposit material conformally for 3D structures. Hwang, 12 ("better conformality over three-dimensional (3D) structures") 13 ("unprecedented conformality over the 3D structures"). And ALD was highly predictable, as it was textbook material and routine to

implement before the ’254 patent was filed. *Id.*; *see also* Toyama, [0226], [0313]; Tessariol, [0063], [0038].

e. Anisotropic etching of the bottom layer of the holes

To the extent any ’254 Patent Primary Reference is determined to be missing the claimed “the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening” a POSA would have considered it obvious and been motivated to so etch the bottom surface of openings, e.g., in view of the prior art below.

For example, when forming a TAC, it would have been understood to disclose the removal of the bottom portion of the dielectric ([5.B]) via anisotropic etching. For example, Nakajima discloses: “Next, as shown in FIG. 10, a portion of the silicon oxide layer 81 that is located at the bottom of the hole H1 is removed by, for example, RIE using a mask layer not shown in the drawing, so that the silicon nitride layer 41 is exposed.” Nakajima, 7:50-53. First, this Nakajima’s RIE is anisotropic because it is a directional etch (with nearly vertical sidewalls). Wang, 6:63-65 (“For example, channel hole 120 can be formed by anisotropic reactive ion etching (RIE).”); Kanakamedala, 11:55-58 (“The at least one memory film 7, 9, 11 and cover layer 410 may be etched using RIE or another suitable anisotropic wet or dry etching method to form the opening 417.”). That is precisely what Nakajima discloses in removing the bottom portion of the liner. Thus, in forming an insulating liner, it was understood that a typical, advantageous process was anisotropic etching and to remove the bottom oxide portion.

Further, it was well known, and obvious, that to form a material, including a dielectric liner, on only the sidewall of a hole, the typical approach involves a deposition and then an etch—such as an anisotropic etch—to remove the deposition on the bottom portion. Serov, 34:62-35:3 (“The dielectric liners 141 can be formed, for example, by formation of a dielectric material layer including a first dielectric material, and by a subsequent anisotropic etch (such as a reactive ion etch) that removes horizontal portions of the dielectric material layer to form dielectric spacers 141”), 17:41-46 (“Each first semiconductor channel portion 601 can be formed on inner sidewalls of each memory film 50 by deposition of a semiconductor material layer and a subsequent

anisotropic etch of the semiconductor material layer."). Removing the bottom portion has the obvious benefit of enabling a subsequent conductive core to connect to the underlying element.

f. Unintentional Recesses

To the extent any '254 Patent Primary Reference is determined to be missing the claimed "forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening," under YMTC's infringement theory, a POSA would have considered it obvious, e.g., in view of the art below. Typical prior art etches that were both well known and beneficial in that they create holes through the stack, e.g., for contacts, were also known to result in lateral recesses in either the dielectric spacers or sacrificial layers. Shen, 2:59-67. Thus, it would have been obvious to form unintentional recesses in any references disclosing TACs.

g. Rib-Shaped Through Array Contacts

To the extent any '254 Patent Primary Reference is determined to be missing the claimed "forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening," a POSA would have considered it obvious and been motivated to so form channel structures, e.g., in view of the art below.

For example, it was well known that an option for a TAC or other through-memory structures was to have a ribbed shape, that is, forming recesses in one of the stack layers. Cui discloses contacts 183 that travel through the staircase and through the entire array. Cui, Fig. 14A, 25:51-53 (e.g., 183 contact on right of region 200); *see also* Kai, 11:9-34 ("laterally recessed"). Cui depicts an embodiment in which the sidewalls of this contact are straight ("cylindrical via cavity"). Cui, Fig. 15A, 25:63-26:22. And it depicts an alternative embodiment that intentionally creates large recesses in the conductor layers ("ribbed via cavity"). *Id.*, Fig. 16A, 26:23-33.

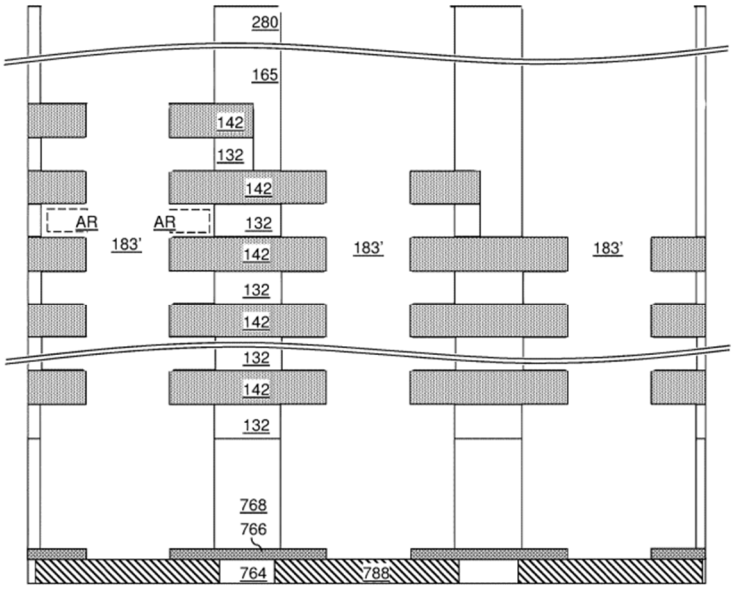


FIG. 16A

Id., Fig. 16A.

In view of the knowledge of a POSITA, it would have been obvious, and a POSITA would have been motivated to, create a ribbed via cavity in, for example, the Primary References TACs. It would have been advantageous because it was known to create "rib regions." Cui, 26:23-34. This creates additional area for the dielectric material. There are only two options for creating such rib regions: in the sacrificial gates or in the conductive layers. Both were known and result in the same benefit. Cui, Fig. 16A, 26:23-33 (recesses in conductive layers); Kai, 11:9-34 (recesses in sacrificial gates). A POSITA would have had a high expectation of success in forming the rib regions because the isotropic and selective etches were well known. *E.g.*, Cui, 26:33-45; Kai, 11:9-34 (recesses in sacrificial gates).

h. Use of isotropic etches

To the extent any '254 Patent Primary Reference is determined to be missing the claimed "wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening" a POSA would have considered it obvious and been motivated to so etch openings, e.g., in view of the art below.

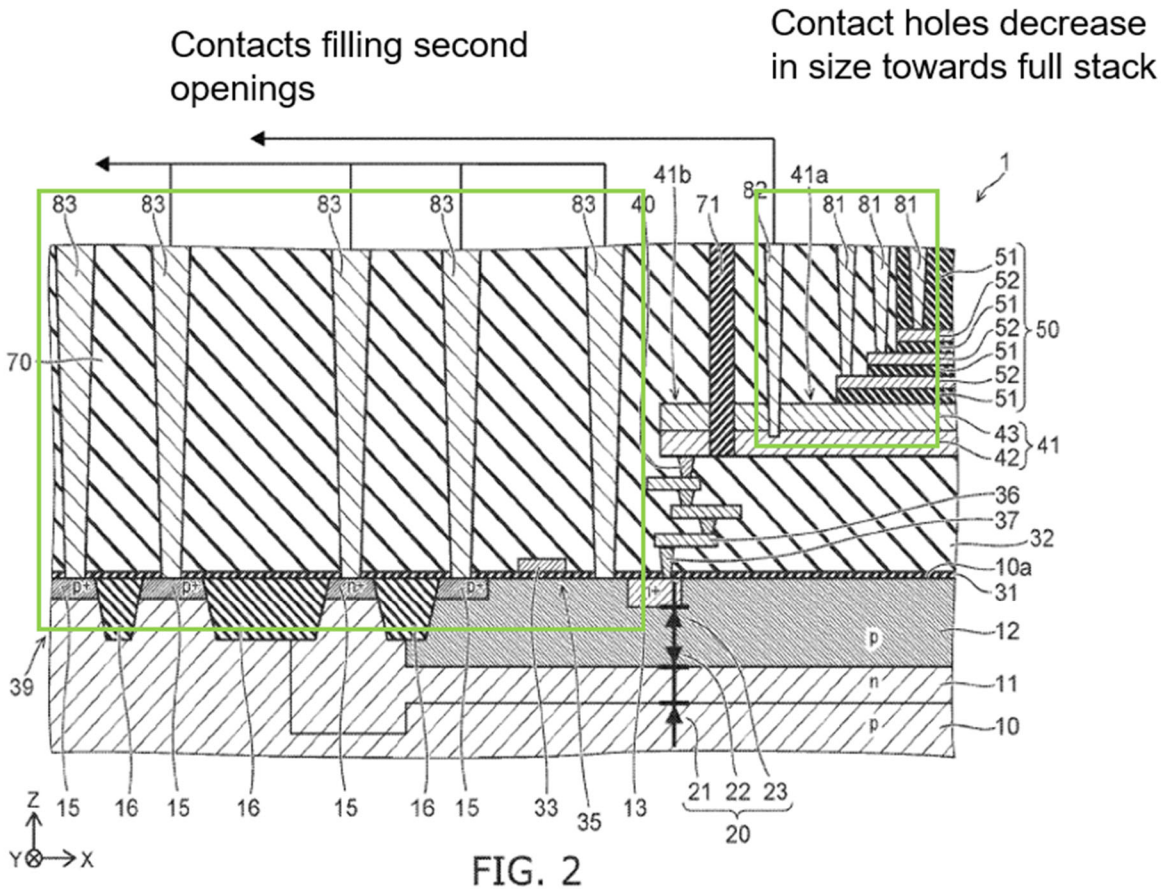
For example, it was well known that an isotropic etch is suitable when attempting to remove a material from an area (here, oxide on the bottom) if there is less material on that area relative to

the other areas in which the etch chemical will contact. *E.g.*, U.S. Pat. 10,714,341, 1:48-62 ("Furthermore, since the sacrificial material is removed using an isotropic etch process, the use of a thick sacrificial material, which is needed to form a thick metal film on the substrate, will require the formation of a large lateral overhang, since the vertical etch rate of the sacrificial material is the same as lateral etch rate of the sacrificial material."). A POSITA would have had a high expectation of success, because isotropic etches were generally well known, including for this very application. *Id.*

i. Dummy Channel Structures of Smaller Diameter Than TACs and Peripheral Contacts

To the extent any '254 Patent Primary Reference is determined to be missing the claimed "wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings" a POSA would have considered it obvious and been motivated to so form channel structures, e.g., in view of the art below.

The lateral dimensions of via structures typically get smaller towards the array, because the array contains millions or billions of channel structures. This is shown below:



Fujiki, Fig. 2. Thus, it would have been obvious that contacts outside of the array may be the largest (though, it was textbook material to form all contacts the same size).

It would have been obvious that channel hole (and dummy channel holes) will have the smallest lateral dimensions relative to contacts. Channel holes are miniscule in size relative to contacts. For example, below is a top-down view showing channel structures in region 100 versus various contacts:

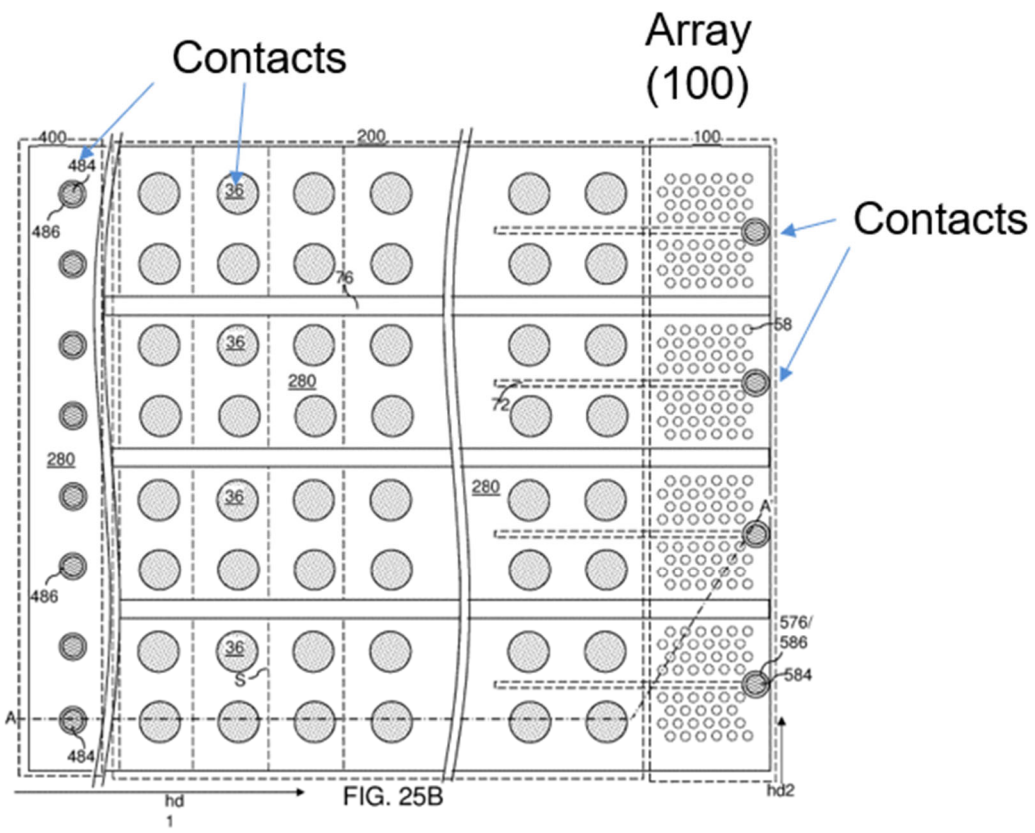


FIG. 25B

Cui, Fig. 25B. A POSITA would have understood the above figure to illustrate relative size differences in the dense array and the less dense peripheral, because of the inclusion of relative more channel structures. Also note the height difference in Figure 2 above. The contacts 83 are longer, and as a natural result of etches that taper (as shown in Figure 2), the lateral width of the top is naturally wider. Further, the third holes are dummy holes. This means an active structure, such as a channel structure, will not fill the dummy hole. As a result, such features do not present process margin issues, and employing smaller feature is not an issue.

j. Fully filling dummy channels with dielectric material

To the extent any '254 Patent Primary Reference is determined to be missing the claimed "depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure" a POSA would have considered it obvious and been motivated to so fill dummy channels, e.g., in view of the art below.

A common support pillar was a solid dielectric, e.g., oxide, pillar. Ex. 1032 (U.S. Pat. 9,793,139), 15:21-36 ("dielectric support pillar 7P"). The benefit of the complete fill is more

support relative to only a partial fill. *Id.* Thus, it would have been obvious to fully fill a dummy channel hole with a dielectric material.

k. Removing parts of the dielectric layer that are deposited on a bottom surface of openings

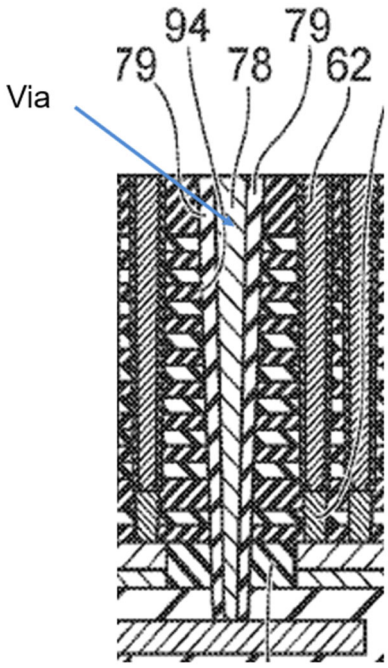
To the extent any '254 Patent Primary Reference is determined to be missing the claimed "removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening" a POSA would have considered it obvious and been motivated to so remove dielectric layers.

It would have been obvious to remove the bottom dielectric layer for each contact, so that the proper interconnection path can be made with good electrical coupling. Moreover, as the Nakajima reference demonstrates, forming a conformal spacer typically results in a dielectric on the bottom surface, requiring its removal to form a functional contact.

l. Vias including conductive layers

To the extent any '254 Patent Primary Reference is determined to be missing the claimed "forming a through array contact (TAC) extending vertically through the stack by depositing a conductor layer over the spacer in the first opening" a POSA would have considered it obvious and been motivated to form vias that include conductive layers.

For example, Fujiki discloses "the through-via 78 is formed on the inner surface of the insulating film 79. The through-via 78 is connected to the interconnect 36." Fujiki, [0053].



Id., Fig. 9 (partial).

It would have been understood, and certainly obvious, that "through-via 78" is a conductor layer. As Nakajimi and Tessariol demonstrate, the conductive fill provides a conductive core, thereby providing a structure that enables electrically coupling upper level devices to underlying devices. For example, Fujiki discloses that "[t]he through-via 78 is insulated from the electrode films 52 and the source electrode film 41 by the insulating film 79." Fujiki, [0042]. In other words, through-via 78 is conductive, because it requires an insulating film to prevent short circuits to the conductive gate layers. By way of another example, Fujiki provides a "control circuit" under the array. Fujiki, [0032]. The through-via connects this circuit to upper-level devices via lower interconnect 36, plug 77, and upper layer interconnect 80. Id., [0042], Fig. 1. Thus, the via must be conductive to accomplish the connection. Indeed, it would be advantageous for it to be conductive, as that would enable the "control circuit" under the array to connect to the upper-level devices, and routine to implement because it simply involves a conductive fill.

m. Slits and TACs extending all the way through the stack

To the extent any '254 Patent Primary Reference is determined to be missing the claimed " forming a through array contact (TAC) extending vertically through the stack" or "after forming

the TAC, forming a slit extending vertically through the stack" a POSA would have considered it obvious and been motivated to form the TAC and slits that extend all of the way through the stack, e.g., in view of the art below.

For example, it would have been obvious that to form slits extend through the entire stack. First, it was well known that slits are often the voids that the gate replacement process uses to etch out the sacrificial gates and provide pathways for the replacement gate material to fill the void areas in the stacked body region (50). Fujiki uses slits 96 for both of these processes. Fujiki, [0055]. That process involves creating slits through the entire stack. Nakajima, 8:12-15, Fig. 11. Second, it was well known that creating the slits may involves an RIE etch. *Id.* That etch has to ensure that the slit extends through the stack to ensure that the slit is usable to replace the bottom gate. The layer underlying the stack acts as a buffer of sorts, that is, it ensures that the etch creates the slit through the stack but does not etch any layer underlying the layer, e.g., silicon, supporting the stack. The slits extend through the entire stack to ensure that the void interfaces each sacrificial layer, thereby enabling the etching of the sacrificial gates and deposition of replacement gates. In other words, an etch that did not extend through the stack would prevent replacement of, for example, the bottom sacrificial gates. Thus, a POSITA would have been motivated and had a high expectation of success given that such etches were textbook material, to perform the etch all the way through the stack to, in effect, etch into a buffer to ensure proper gate replacement and form the slit through the entire stack.

For example, Mushiga discloses forming holes for through-array contacts (588) (as well the insulating spacers and conductive cores) through the stack:

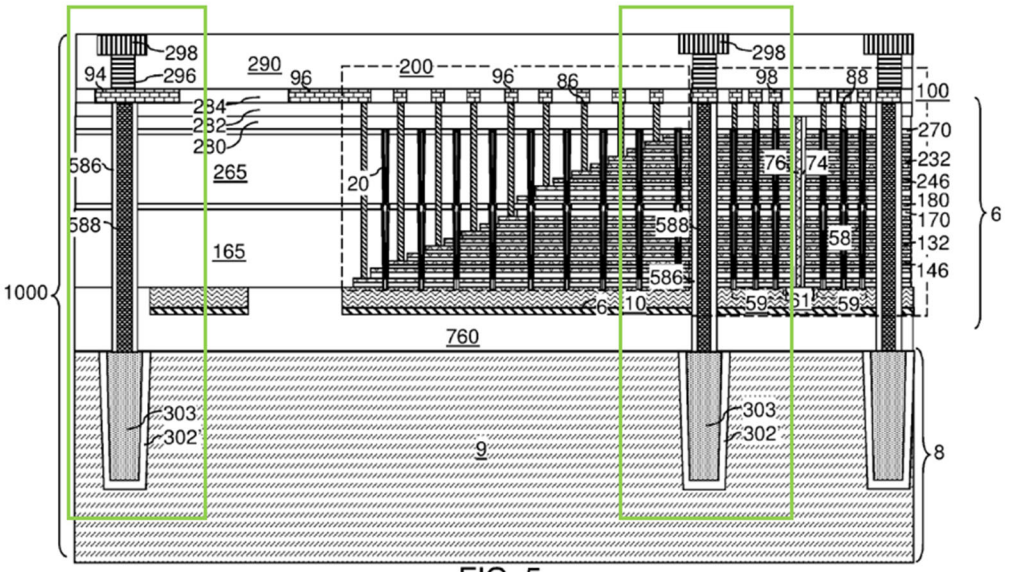


FIG. 5

Mushiga, Fig. 5, 10:31-58.

By way of another example, Masamori2 discloses forming holes for contacts (as well as the conductive fill) and TACs through the stack:

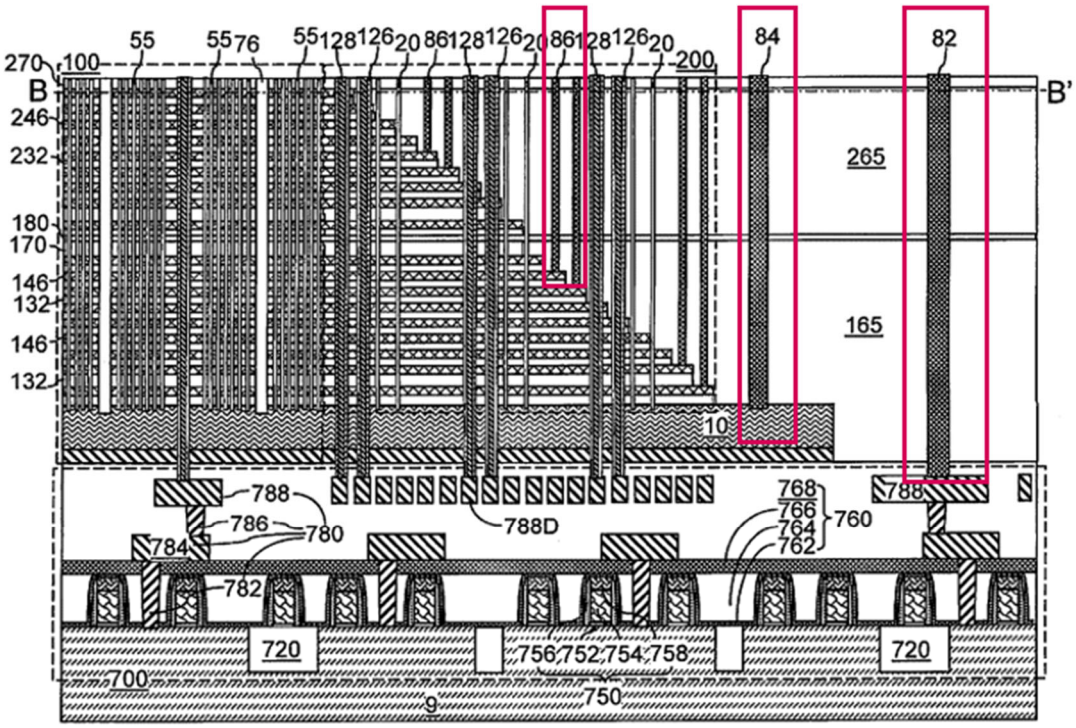


FIG. 13A

Masamori2, Fig. 13A, 24:22-29 ("Alternatively, two or more types of contact via structures (82, 84, 86) may be formed employing a common set of patterning processes and fill processes provided

that the anisotropic etch process therein can control vertical extent of cavities at target height levels for each type of cavities that are simultaneously formed.”).

By way of another example, Kai3 discloses the same:

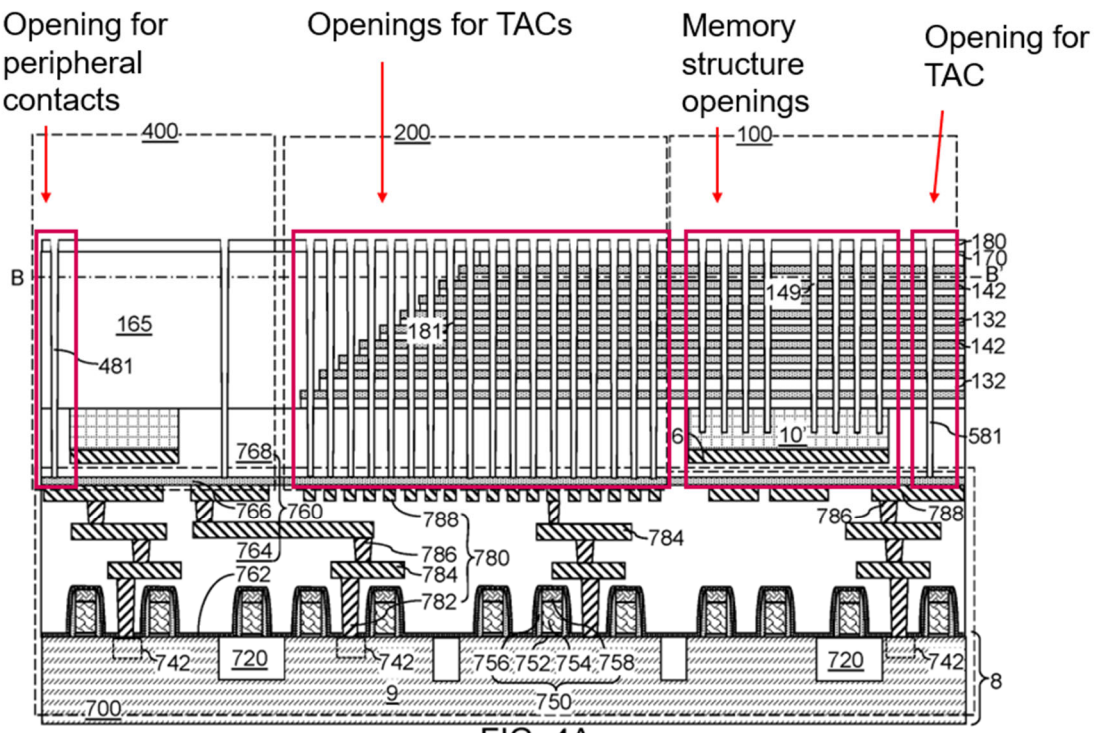


FIG. 4A

Kai3, Fig. 4A, 17:30-44 (“The pattern of openings in the photoresist layer can be transferred through the inter-tier dielectric layer 180 and the first-tier structure (132, 142, 170, 165) and into the in-process source-level material layers 10′and the at least one second dielectric layer 768 by a first anisotropic etch process to form the various first-tier openings (149, 181, 481, 581) concurrently, i.e., during the first anisotropic etch process. The various first-tier openings (149, 181, 481, 581) can include first-tier memory openings 149, first-tier staircase-region openings 181, first-tier array-region openings 581, and first-tier peripheral-region openings 481.”). Notably, the memory structure openings (149) extend into the substrate (as shown above), while the other openings extend down to the metal interconnects. *E.g.*, *id.*, 17:48-58, 18:9-21 (181 and 581 openings extending to interconnect). TACs enable connecting upper-level devices to underlying logic, e.g., under the stack. This beneficially saves space, e.g., moving peripheral logic to under

the array. As the above demonstrates, a POSITA would have had a high expectation of success, because the processes therefor were textbook material, e.g., anisotropic etch, conformal deposition of a spacer, and CVD deposition of the conductive core.

n. Simultaneously depositing the conductor layer in the first opening to form the TAC and in the second opening to form a peripheral contact and TAC s through the array

To the extent any '254 Patent Primary Reference is determined to be missing this limitation, or any limitation relating to forming TACs simultaneously, a POSA would have considered it obvious and been motivated to do so.

Contacts, as the below demonstrates, provide upper-level connections down to substrate-level devices on the peripheral and within the array, thereby enabling the inclusion of peripheral logic and logic under the stack.

For example, Fujiki discloses forming "contacts 81 to 83" outside of the stack. Fujiki, [0043]. These include contacts 82 and 83 that extend through insulating layer 70, either of which is in a "a second opening":

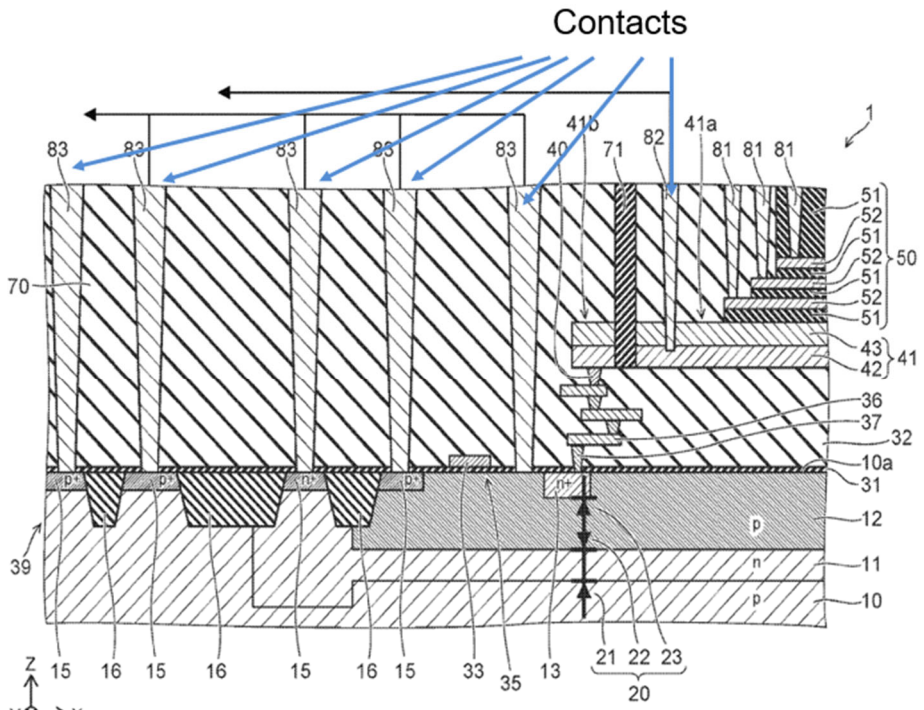


FIG. 2

Id., Fig. 2.

In the manufacturing description of embodiment one, however, Fujiki only describes forming one through-via. Fujiki, [0050]. As explained below, it would have been understood, and certainly obvious, that Fujiki and other prior art would (or could) simply etch all contact holes for Fujiki's TAC and contacts 82 or 83 at once, just as Fujiki does with its channel holes. *Id.*, [0052].

A POSITA would have been highly motivated to do so with a high expectation of success.

First, it would have been known to reduce processing time, because only one etch process would be necessary to process all contact holes. That is why it was known to form openings for different structures at the same. *E.g.*, Tessariol, [0037] ("dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously)"), Fig. 9. This was widely known in the art. Because of this well-known benefit, process technologies, e.g., etch chemistries, that achieve simultaneous etching of different holes—including holes of different sizes—became textbook material. *E.g.*, Wolf Vol. 2, 47.

For example, Mushiga discloses forming holes for through-array contacts (588) (as well the insulating spacers and conductive cores) at the same time:

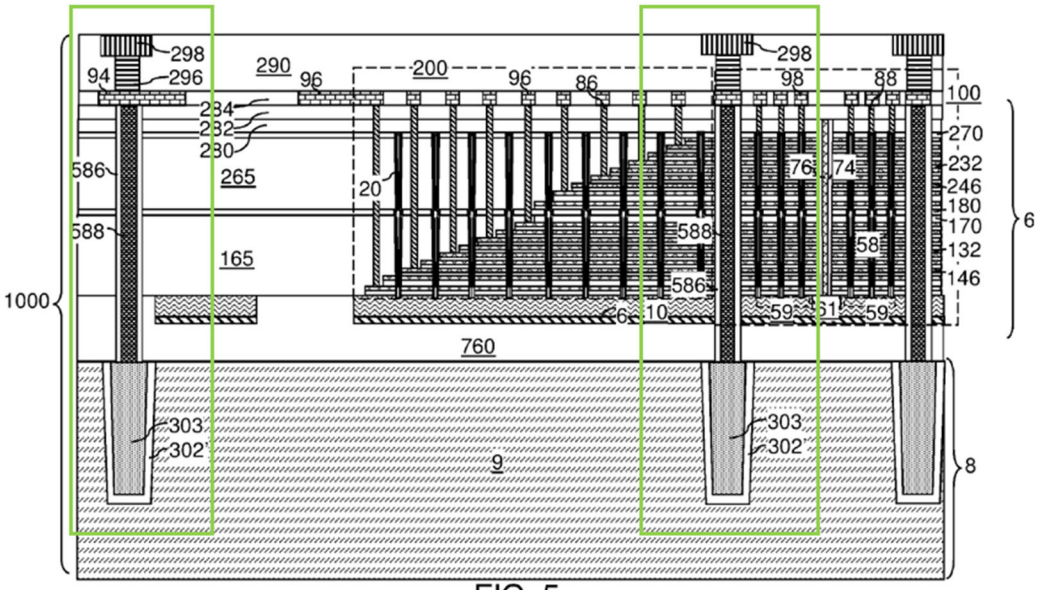


FIG. 5

Mushiga, Fig. 5, 10:31-58.

By way of another example, Masamori2 discloses forming holes for contacts (as well as the conductive fill) at the same time as well as support structures and multiple contacts at the same time:

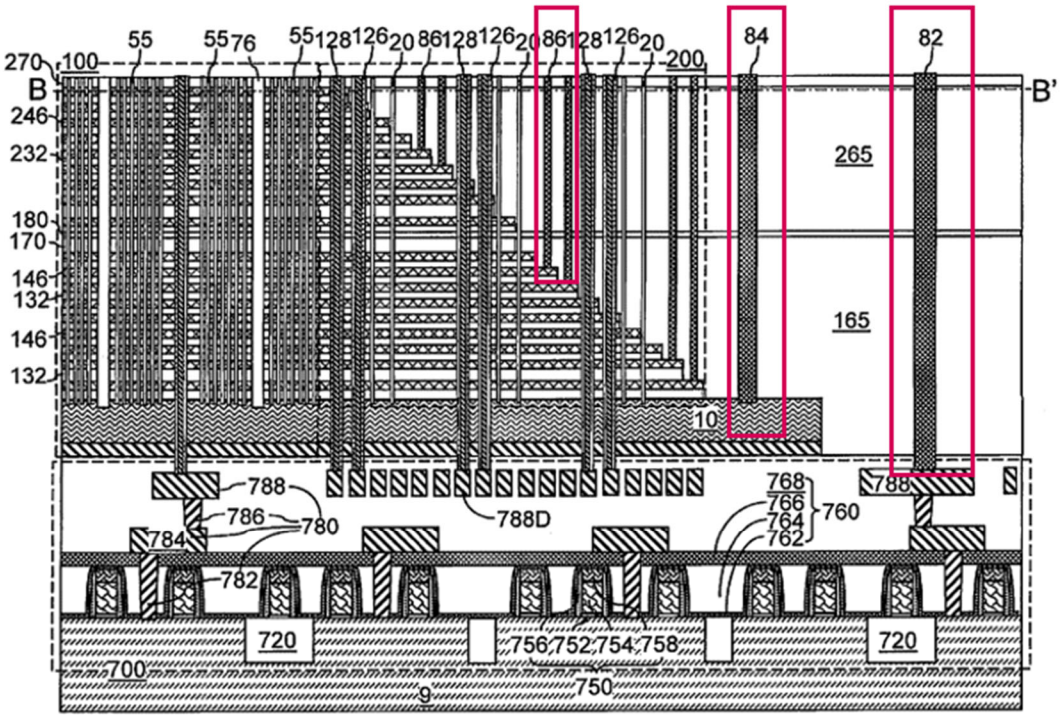


FIG. 13A

Masamori2, Fig. 13A, 24:22-29 ("Alternatively, two or more types of contact via structures (82, 84, 86) may be formed employing a common set of patterning processes and fill processes provided that the anisotropic etch process therein can control vertical extent of cavities at target height levels for each type of cavities that are simultaneously formed."). Notably, the contact holes extend down to conductive gate layer (86), the substrate (84), and a metal interconnect (82). But Masamori2 describes using a timed anisotropic etch to control the target heights. *Id*.

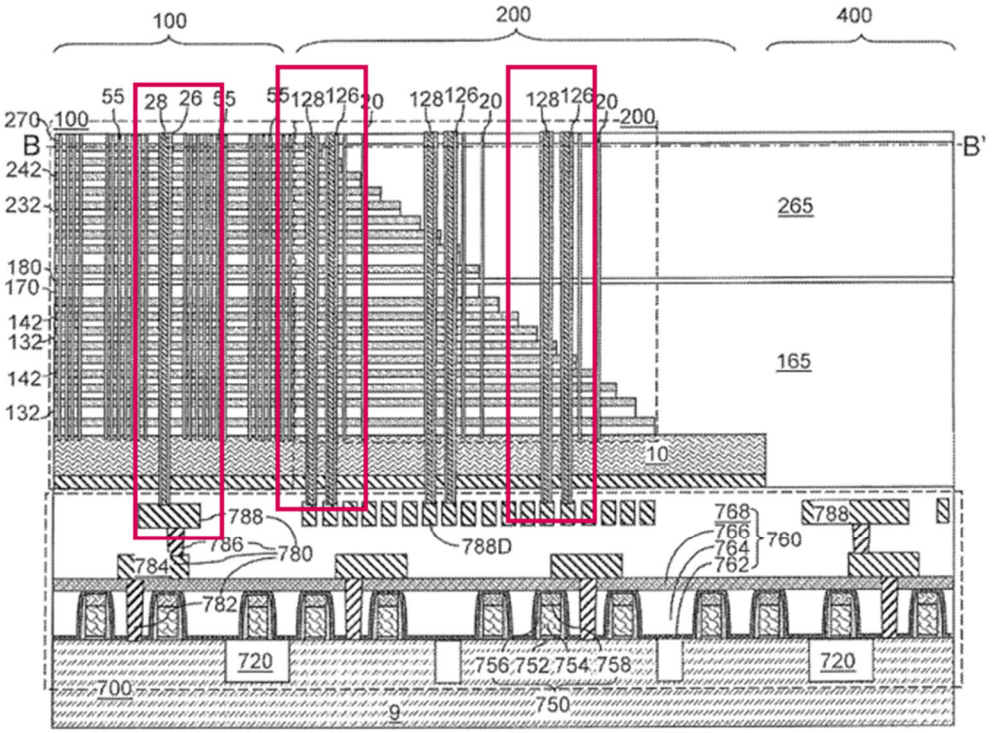


FIG. 8A

Id., Fig. 8A, 17:51-54 ("In one embodiment, the laterally-insulated support structures (126, 128) can be formed concurrently with the laterally-insulated conductive via structures (26, 28) and can have the same structure.").

By way of another example, Kai3 discloses forming openings for various contacts and memory structure openings in a single step:

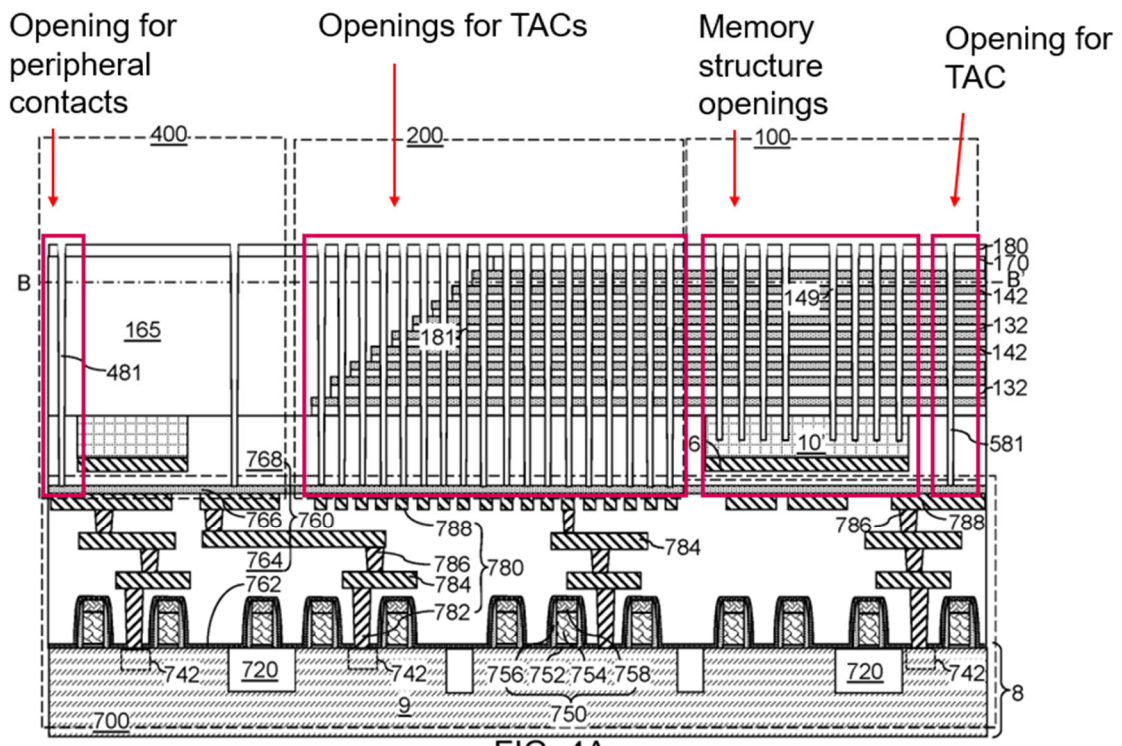


FIG. 4A

Kai3, Fig. 4A, 17:30-44 ("The pattern of openings in the photoresist layer can be transferred through the inter-tier dielectric layer 180 and the first-tier structure (132, 142, 170, 165) and into the in-process source-level material layers 10′and the at least one second dielectric layer 768 by a first anisotropic etch process to form the various first-tier openings (149, 181, 481, 581) concurrently, i.e., during the first anisotropic etch process. The various first-tier openings (149, 181, 481, 581) can include first-tier memory openings 149, first-tier staircase-region openings 181, first-tier array-region openings 581, and first-tier peripheral-region openings 481."). Notably, the memory structure openings (149) extend into the substrate (as shown above), while the other openings extend down to the metal interconnects. *E.g.*, *id.*, 17:48-58, 18:9-21 (181 and 581 openings extending to interconnect). Like Masamori2, Kai3 employs an anisotropic etch. *Id.*, Fig. 4A, 17:30-44.

Indeed, because Fujiki describes one process for forming the through-vias, it would have been understood that Fujiki describes forming multiple contacts simultaneously. Specifically, Fujiki states that the shown components are "fewer than the actual components." Fujiki, [0024].

And it was known when implementing TACs, the typical configuration includes multiple TACs. Mushiga, Fig. 5, 10:31-58; Nakajima, Figs. 1, 2 (multiple TACs, i.e., C4s), 7:26-8:11. It was typical to describe a process for creating a single contact even though that process actually forms multiple contacts simultaneously. Nakajima, Figs. 1, 2 (multiple TACs, i.e., C4s), 7:26-8:11. Thus, Fujiki already discloses the ability to form multiple contacts (including the openings) at the same time.

And it would have been routine and highly predictable to simultaneously etch multiple holes. Etches that simultaneously etch holes, regardless of whether some of the holes extend through all of the stack and other holes extend through only a portion (or none) of the stack, were well known and routine to implement. *E.g.*, Nakajima, 7:37-43 (forming holes for C4 contacts), Fig. 2 (TACs, C4, through in various locations); Tessariol, [0037] ("dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously)"), Fig. 9 (extending through different number of stack layers). And as the above describes, controlling the target depth, even if the target depth interfaces to a different material, was well known. For example, a process forms multiple holes in a mask before the etch that simultaneously creates the holes and other factors, such as time and etch chemistries, control the depth of, e.g., an anisotropic etch. Wolf Vol. 2, 47.

To the extent that it is argued that this filling must occur simultaneously (the claim does not recite such a requirement), Fujiki would have been understood, or at least render obvious, such simultaneous deposition for the following reasons.

As the above analysis demonstrates, it would have been understood, or at least obvious, to etch the contact holes at the same time. For effectively the same reasons, it would have been understood, or at least obvious, to form the conductive layers at the same time (as well as the spacers). Again, this saves considerable processing time.

o. Depositing a dielectric layer on the sidewall and a bottom surface of the first opening

To the extent any '254 Patent Primary Reference is determined to be missing the claimed "depositing a dielectric layer on the sidewall and a bottom surface of the first opening" a POSA would have considered it obvious and been motivated to form dielectric layers as claimed, e.g., in view of the below art.

For example, it was well known, and obvious, that to form a material, including an insulator liner, on only the sidewall of a hole, the typical approach involves deposition of material on all surfaces of the hole and then an etch to remove the deposition on the bottom surface. Serov, 34:62-35:3 ("The dielectric liners 141 can be formed, for example, by formation of a dielectric material layer including a first dielectric material, and by a subsequent anisotropic etch (such as a reactive ion etch) that removes horizontal portions of the dielectric material layer to form dielectric spacers 141"), 17:41-46 ("Each first semiconductor channel portion 601 can be formed on inner sidewalls of each memory film 50 by deposition of a semiconductor material layer and a subsequent anisotropic etch of the semiconductor material layer.").

By way of another example, Nakajima discloses that in forming a spacer: "silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1." Nakajima, 7:44-49.

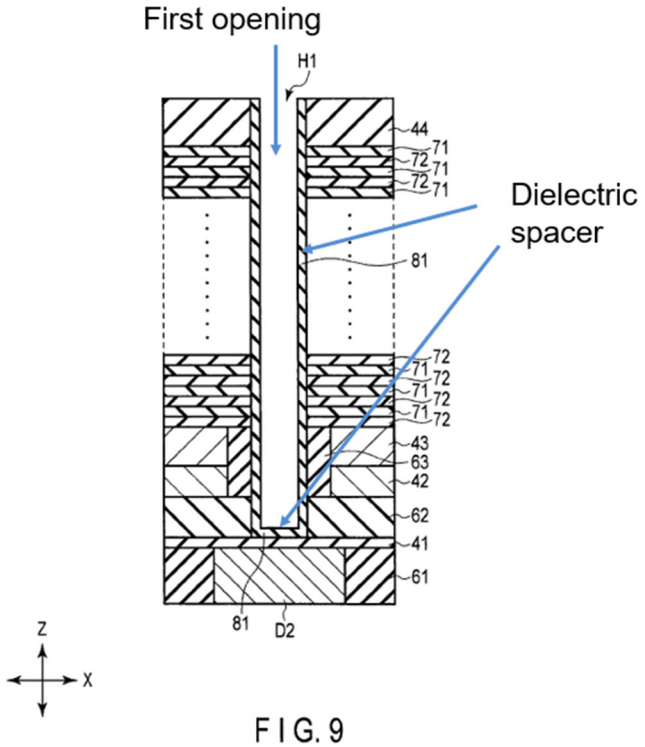


FIG. 9

Id., Fig. 9.

A strong motivation for the process that creates the dielectric portion on the bottom is providing a conformal liner. Nakajima, 7:44-49. The typical conformal process for forming a

conformal spacer involves forming the conformal dielectric layer along the sides and bottom surface. *Id.*, ("silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1"). Otherwise, it would be difficult to form the conformal layers on the sidewall. As dimensions shrink in semiconductor devices, conformal liners are critical, and in fact, led to the popularity of ALD processes. Hwang, 12 ("better conformality over three-dimensional (3D) structures"), 13 ("unprecedented conformality over the 3D structures").

Such techniques, including ALD, were highly predictable, as they were textbook material and routine to implement. Again, the process for forming a spacer that creates the bottom portion was well known and understood, involving basic depositions (e.g., ALD) and etches (e.g., anisotropic etch). *E.g.*, Nakajima, 7:44-61 (deposition and etch to form spacer); Serov, 17:41-46, 34:62-35:3 (same); Toyama, [0226], [0313] (ALD for spacers); Tessariol, [0038], [0063] (recognizing multiple suitable deposition and etch types for spacers).

p. Additional Motivations for Micron's Prior Art Products

The above sections demonstrate that a POSA would have been motivated to combine the '254 Patent Primary References, including Micron's prior art products (B27A), with various prior art references. Note that Micron's bit line exit region provides an area for contacts. As the discussion in Section III.A.3.m demonstrates, implementing those contacts as TAC through the array was readily known. And as Tessariol demonstrates (another Micron patent), Micron already had the TAC technology, and in fact, this Section demonstrates that TACs that extend through various portions of the array were well known. As B27A and Tessariol both demonstrate Micron prior art technology, both are fully compatible.

B. Invalidity Based on Improper Inventorship Under Section 101 (Patent L.R. 3-3(d))

The Asserted Claims of the '254 Patent are invalid under 35 U.S.C. § 101 because the patent improperly omits inventors that contributed to the invention of the subject matter sought to be patented. In this regard, 35 U.S.C. § 101 states that "[w]hoever invents … may obtain a patent … ." On information and belief, employees of Micron contributed to the inventions claimed by the '254 Patent and such Micron employees have been improperly omitted from the list of named inventors on the patent.

The ’254 Patent currently names Hongbin Zhu as an inventor of the claimed subject matter. Hongbin Zhu worked at Micron as an engineer from January 9, 2006, to September 18, 2017. The application which resulted in the ’254 Patent was filed on August 21, 2018, meaning that Hongbin Zhu had been working on 3D NAND technology at Micron shortly before the filing of the application for this patent. On information and belief, Hongbin Zhu worked with other Micron employees at Micron to conceive of the invention claimed in the ’254 Patent and thus these Micron employees have been improperly omitted as named inventors of the patent. Furthermore, YMTC is a latecomer to 3D NAND products and technology, having only been established in 2016, long after Micron had patented, manufactured, and shipped its first 3D NAND products. This all suggests that the subject matter claimed in the patent was conceived and developed at Micron and involved other Micron employees not currently listed as named inventors on the patent.

Micron is currently seeking discovery from YMTC related to inventorship of this patent and individuals who contributed to the conception of the invention claimed in this patent. However, despite Micron’s requests, YMTC to date has refused to provide responsive information or documents.

C. Invalidity Based on Section 112 (Patent L.R. 3-3(d))

1. Indefiniteness

Defendants provide the following grounds for invalidity under 35 U.S.C. § 112. Defendants’ investigation of the Asserted Patents is ongoing, and Defendants reserve the right to amend or supplement these disclosures based on further investigation and in a manner consistent with the Federal Rules of Civil Procedure, the Local Patent Rules for the Northern District of California, and the Docket Control Order, or otherwise in accordance with any order or direction of this Court or agreement of the parties. Further, Plaintiff’s Infringement Contentions fail to provide sufficient detail to fully understand its proposed application of the Asserted Claims, and Defendants reserve the right to assert additional grounds for invalidity under 35 U.S.C. § 112 in response to Plaintiff’s claim interpretations. Defendants also reserve the right to supplement, modify, or otherwise amend these grounds for invalidity under 35 U.S.C. § 112 based on the Court’s claim construction rulings or opinions or the parties’ positions or arguments taken in

connection with the claim construction process. Given the deficiencies in Plaintiff's infringement contentions, Micron reserves the right to identify terms that are indefinite should Plaintiff serve contentions that raise indefinite issues.

2. Written Description and Enablement

The specification of the '254 Patent does not provide adequate written description to support the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims. 35 U.S.C. § 112(a) requires that a patent specification contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharm., Inc.*, 598 F.3d at 1351 (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ.*, 541 F.3d at 1122 (quoting *Vas-Cath Inc.*, 935 F.2d at 1563–64). The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Additionally, the Asserted Patents do not enable the claim scopes contained in Plaintiff's Infringement Contentions. Section 112(a) requires a specification to describe "the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention]." The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This "requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp.*, 344 F.3d at 1244 (citation omitted); *see Wyeth & Cordis Corp.*, 720 F.3d at 1385–86. The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Defendants provide below an identification of terms in Asserted Claims that render the Asserted Claims, at least as apparently construed by Plaintiff in its Infringement Contentions as discussed above, invalid pursuant to 35 U.S.C. § 112 as not enabled or lacking sufficient written

description:

- "after forming the TAC, forming a slit extending vertically through the stack"
- "isotropic etching"
- "fully filling"

IV. INVALIDITY OF THE '322 PATENT

A. Invalidity Based on the Prior Art

As shown below, the alleged inventions of the '322 Patent were well-known in the prior art. Those skilled in the art were aware of all of the limitations claimed in the '322 Patent. Thus, many prior art patents, publications, products, and combinations thereof, disclose, teach, or embody every limitation of the Asserted Claims and thus invalidate those claims. Examples of these disclosures, teachings, and embodiments are identified in the following sections and in the attached claim charts.

1. Identification of Prior Art References (Patent L.R. 3-3(a))

Subject to the reservation of rights above, Defendants identify each item of prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the '322 Patent. The patents/applications, publications, and systems identified are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations.

Some of the below citations and those in the corresponding invalidity claim charts involve prior art references that have corresponding related, foreign, and/or PCT counterpart publications. In such cases, where either the U.S. patent or related, foreign, and/or PCT counterpart is cited, it is to be understood that the corresponding disclosures from the counterpart patent and publications (which are substantively the same) are implicitly incorporated by reference in the alternative to avoid needless repetition.

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
J-01	U.S. 2018/0301374 ("Masamori")	April 18, 2018	October 18, 2018
J-02	U.S. 2019/0287894 ("Nakajima")	July 3, 2018	September 19, 2019
J-03	U.S. 2017/0148805 ("Nishikawa")	January 28, 2016	May 25, 2017
J-04	U.S. 2019/0081061 ("Tessariol")	September 14, 2017	March 14, 2019
J-05	U.S. 2019/0229125 ("Zhou")	Jan. 22, 2018	July 25, 2019
J-06	U.S. 9,853,046 ("Lu")	October 8, 2014	December 26, 2017
J-07	U.S. 10,354,980 ("Mushiga")	March 22, 2018	July 16, 2019

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
J-08	U.S. 8,107,292 ("Maejima")	April 23, 2008	January 31, 2012
J-09	U.S. 10,347,654 ("Iwai")	May 11, 2018	July 9, 2019
§IV.A.3.[6]	U.S. 10,658,378 ("Tao")	May 3, 2018	May 19, 2020
§IV.A.3.	U.S. 10,777,501 ("Nakajima2")	March 16, 2018	September 15, 2020
§IV.A.3.	U.S. 2017/0179026 ("Toyama")	December 22, 2015	June 22, 2017
§IV.A.3.	WO 2019/042103 ("Dai")	August 28, 2017	March 7, 2019
§IV.A.3.	U.S. 10,679,721 ("Kim")	March 8, 2017	June 9, 2020
§IV.A.3.	U.S. 2012/0280304 ("Lee 304")	May 3, 2011	November 8, 2012
§IV.A.3.	U.S. 2017/0125430 ("Nishikawa2")	October 28, 2015	May 4, 2017
§IV.A.3.	U.S. 2015/0348987 ("Lee 987")	June 3, 2014	December 3, 2015
§IV.A.3.	U.S. 10,559,583 ("Park")	July 20, 2016	February 11, 2020
§IV.A.3.	U.S. 5,945,717 ("Chevallier")	March 11, 1997	August 31, 1999
§IV.A.3.	U.S. 10,347,487 ("Lee 487")	November 14, 2017	July 9, 2019
§IV.A.3.	U.S. 10,290,643 ("Kai")	January 22, 2018	May 14, 2019
§IV.A.3.	U.S. 9,859,297 ("Park2")	March 10, 2015	January 2, 2018
§IV.A.3.	U.S. 2018/0308559 ("Kim2")	April 25, 2017	October 25, 2018
§IV.A.3.	U.S. 8,945,996 ("Tang")	April 12, 2011	February 3, 2015
§IV.A.3.	U.S. 10,115,632 ("Masamori2")	April 17, 2017	October 30, 2018
§IV.A.3.	U.S. 9,793,139 ("Sharangpani")	October 29, 2015	October 17, 2017
§IV.A.3.	U.S. 10,304,852 ("Cui")	February 15, 2018	May 28, 2019
§IV.A.3.	U.S. 11,075,084 ("Shen")	August 31, 2017	July 27, 2021
§IV.A.3.	U.S. 10,381,369 ("Kim1")	February 21, 2017	August 13, 2019
§IV.A.3.	U.S. 9,837,431 ("Nishikawa3")	January 28, 2016	December 5, 2017
§IV.A.3.	U.S. 9,935,123 ("Nishikawa123")[7]	Jul. 26, 2016	May 25, 2017

Table J-1: Prior Art Patents and Patent Publications for the '322 Patent

Ex.	Title	Authors	Publisher	Date of Publication
§IV.A.3.	"3D Flash Memories" ("Micheloni 2016")	Micheloni		2016
§IV.A.3.	"NAND Flash Memory Technologies" ("Aritome")	Aritome		2016
§IV.A.3.	"Optical lithography—a historical perspective" ("Ronse")	Ronse	C. R. Physique 7	2006

[6] *See* §IV.A.3. The equivalent of a chart is set forth with pinpoint citations to the reference in the motivation to combine sections. The same is true for all references without an exhibit.

[7] *See also* J-03. Nishikawa and Nishikawa123 are the same inventor, and both disclose the same memory architecture. Nishikawa123 adds the specific disclosure of circular TACs being suitable for the common source line connections. Nishikawa, 22:38-42.

Ex.	Title	Authors	Publisher	Date of Publication
§IV.A.3.	"Silicon Processing for the VLSI Era, Volume 1-Process Technology" ("Wolf Vol. 1")	Wolf	Lattice Press	1986
§IV.A.3.	"Silicon Processing for the VLSI Era, Volume 1-Process Integration" ("Wolf Vol. 2")	Wolf	Lattice Press	1990

Table J-2: Prior Art Non-Patent Publications for the '322 Patent

Defendants are still investigating prior uses and sales. Based upon at least Plaintiff's apparent position as to the scope of the Asserted Claims, and as further explained below and in the cited exhibits, it appears that the following systems (and development thereof) qualify as prior art under at least one or more of 35 U.S.C. § 102(a):

Ex.	Description	Entities Involved	Prior Art Date
J-10	120 Series Products	Micron	1/11/2018

Table J-3: Prior Art Systems for the '322 Patent

Micron's 120 series products were publicly available, on sale, or in public use prior to the effective filing date of the '322 Patent. MYM0042611-MYM0042676, MYM0042896-MYM0042896, MYM0065110, MYM0065111.

Description	Availability
Travelers	to be made available via inspection
Process information	to be made available via inspection
Schematics	to be made available via inspection
Layouts	to be made available via inspection
Waveforms	MYM0042897-MYM0043247, MYM0069190-MYM0069236
TEM/SEM Imagery	MYM0043255-MYM0043296, MYM0043316-MYM0043339, MYM0043423-MYM0043424,

Description	Availability
	MYM0043248-MYM0043254, MYM0058880-MYM0058891, MYM0069181-MYM0069181
Datasheets	MYM0043425-MYM0043844, MYM0065164-MYM0066151
Trim Spreadsheets	MYM0065112-MYM0065115, MYM0069182-MYM0069189, MYM0069715-MYM0069940

Table J-4: Listing of Prior Art Systems Documentation for the ’322 Patent

2. Anticipation and Obviousness (Patent L.R. 3-3(b) and (c))

The Asserted Claims of the ’322 Patent are invalid because they are anticipated by the prior art and/or because they would have been obvious in view of the prior art.

The prior art identified by Defendants anticipates and/or renders obvious one or more of the Asserted Claims of the ’322 Patent under at least AIA §§ 102(a)(1), 102(a)(2), and 103. For each prior art reference, Defendants have provided claim charts attached to these Invalidity Contentions as Exhibits J-1 through J-10. These charts identify where each element of each Asserted Claim can be found in each item of prior art.

Again, to the extent not anticipated, the Asserted Claims of the ’322 Patent are invalid as obvious under 35 U.S.C. § 103. Each prior art reference identified in the preceding sections—either alone or in combination with another prior art reference and/or in combination with the knowledge of one skilled in the art—renders the Asserted Claims invalid as obvious. In rendering the Asserted Claims obvious, each prior art reference identified in the preceding sections may be combined with: (1) information known to persons skilled in the art at the time of the alleged invention, (2) any of

the other anticipatory or obviousness prior art references, (3) any statements in the intrinsic record of the '322 Patent and related applications, or (4) any of the additional prior art identified below.

3. Motivations to Combine[8]

A person of ordinary skill in the art would have been motivated to combine the preceding references (*see* Section IV.A.1) for the following reasons. Teachings, suggestions, motivations and/or reasons to modify any of the references and/or to combine any two or more of the references can come from many sources, including the prior art (by specific reference and when read as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obviousness to try, the nature of the problem faced, and/or knowledge possessed by a person of ordinary skill.

Although a patent claim may be invalidated based on a teaching-suggestion-motivation ("TSM") rationale—*i.e.,* that some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention—the Supreme Court identified additional rationales in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007). The following of these rationales apply here:

(A) the asserted claims combine prior art elements according to known methods to yield predictable results;

(B) the asserted claims involve the simple substitution of one known element for another to obtain predictable results;

(C) the asserted claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;

(D) the asserted claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) the asserted claims involve combinations of prior art references that would have been "obvious to try"'—a person of ordinary skill in the art could have reached the asserted claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

[8] The statements in this section about what was known and obvious to a POSA are made with respect to the effective filing date of the '322 Patent.

(F) the asserted claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach); *see also* Department of Commerce, Patent and Trademark Office, Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.,* 72 Fed. Reg. 57,526 (Oct. 10, 2007). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420-21.

Thus, even in the absence of a specific teaching, suggestion, or motivation to combine references, the Asserted Claims here are obvious and therefore invalid. Each of the cited references or devices is in the same field as the '322 Patent, making it obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. One of ordinary skill in the art would have recognized that improvements could be achieved by combining or modifying prior art references that described such improvements. Each of the above prior art references describes systems, products, or methods that were known to offer such improvements, and, accordingly, one of ordinary skill in the art would have been motivated to combine or modify the references as identified in each of the combinations below.

Furthermore, because each prior art reference concerns three-dimensional NAND memory designs, common industry knowledge supplied a reason to combine any one the above references. It was well understood that different three-dimensional NAND memory structural features could be employed together or interchanged with each other, fitting together like puzzle pieces. Each combination would have produced predictable results and would simply represent a known alternative to one of ordinary skill in the art of NAND memory. This is a further motivation to combine any of the above references.

The below sections further address particular reasons to combine the above references. The

below should not be construed as an admission that there is any value to the alleged invention of the '322 Patent. As discussed previously, these contentions are based in significant part on how Plaintiff is apparently construing the asserted claim in its Infringement Contentions, which is an incorrect and overbroad interpretation of the alleged invention of the '322 Patent. Accordingly, to the extent the below refers to benefits of certain elements or industry trends towards these elements, this is not an admission that the alleged invention of the '322 Patent provides any benefits: to the contrary, properly construed and compared to the prior art, the '322 Patent provides no benefits. Likewise, to the extent the below refers to substituting elements, this is not an admission that the elements subject to the substitution are in any way similar, *e.g.,* perform the same function, in the same way, to achieve the same result.

The various elements of the Asserted Claims were well known in the prior art at the time of the alleged invention, and the combination would have been obvious to one of skill in the art. The combinations simply (a) combine prior art elements according to known methods to yield predictable results; (b) involve the simple substitution of one known element for another to obtain predictable results; (c) involve the use of a known technique to improve similar devices (methods, or products) in the same way; (d) apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) involves combinations of prior art references that would have been "obvious to try" – a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and/or (f) would have been prompted by known work, based on design incentives or other market forces, because such variations were predictable to one of ordinary skill in the art.

Moreover, the Supreme Court has stated that a motivation to combine may be simply "common sense" and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420. Indeed, the Supreme Court held that it is sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified,

predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421. Here, all the claim elements are common sense and are easily fit together by one of ordinary skill in the art.

While not necessary, a motivation to combine may also be found in the references themselves. One of skill in the art would have been motivated to combine a reference that refers to, or otherwise explicitly invites combination with, another reference. Where the references cited herein have such an explicit invitation to combine, that invitation would have motivated one of skill in the art to combine any such references.

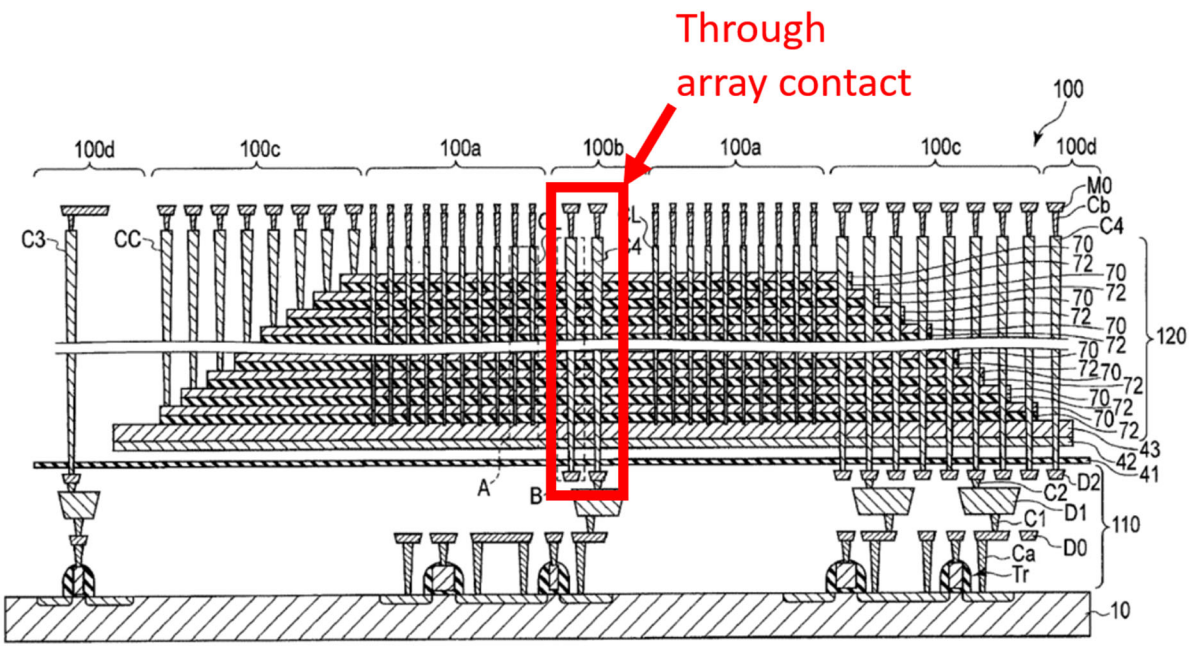
Micron hereby identifies the following '322 Patent Primary References: Masamori, Nakajima, Nishikawa, Tessariol, Zhou, and Micron 120 Series Products.

The below provides several exemplary combinations and motivations for combining an '322 Patent Primary Reference with another reference.

a. Cylindrical Through Array Contacts such as Source Lines and TACs through the stack

To the extent any '322 Patent Primary Reference is determined to be missing the claimed "a through array contact (TAC) comprising a substantially circular section" (or a TAC in general through the full stack) a POSA would have considered it obvious and been motivated to include such a TAC, e.g., in view of the art below.

For example, circular (or cylindrical) TACs were well known. Nakajima discloses circular TACs C4 extending through the middle of the memory stack:



Nakajima, Fig. 2 (annotated), 3:64-67 ("The shape of the contacts CC, C3, and C4 is a rectangular shape in FIG. 1, as viewed in the Z-direction. However, the shape of the contacts CC, C3, and C4 is not limited thereto, but may be a substantially circular shape."). Indeed, it was known that TACs "can have any suitable shape, such as circular, rectangular or elongated trench shape." Nishikawa123, 22:38-42.

Masamori likewise discloses through-array contacts (e.g., laterally-insulated conductive via structures (26, 28)) that have a cylindrical shape and extend through the stack:

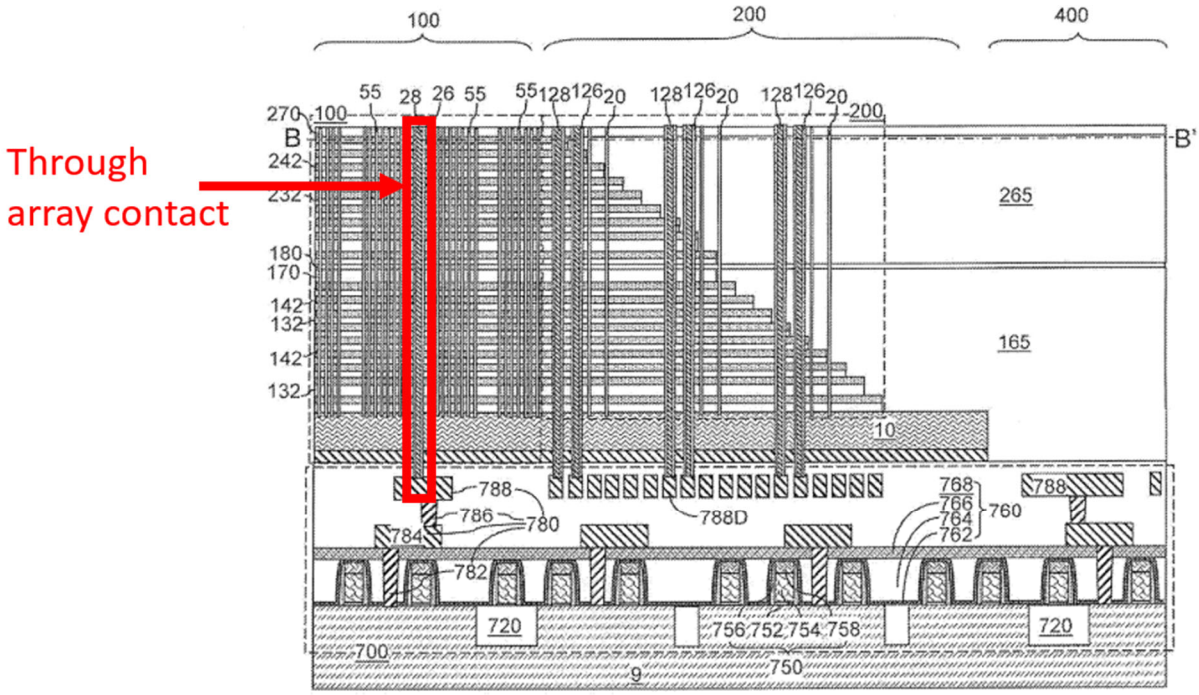


FIG. 8A

Masamori, Fig. 8A (annotated), [0096] ("Referring to FIGS. 8A and 8B, laterally-insulated conductive via structures (26, 28) and laterally-insulated support structures (126, 128) can be formed through each layer in the alternating stacks {(132, 142), (232, 242)}").

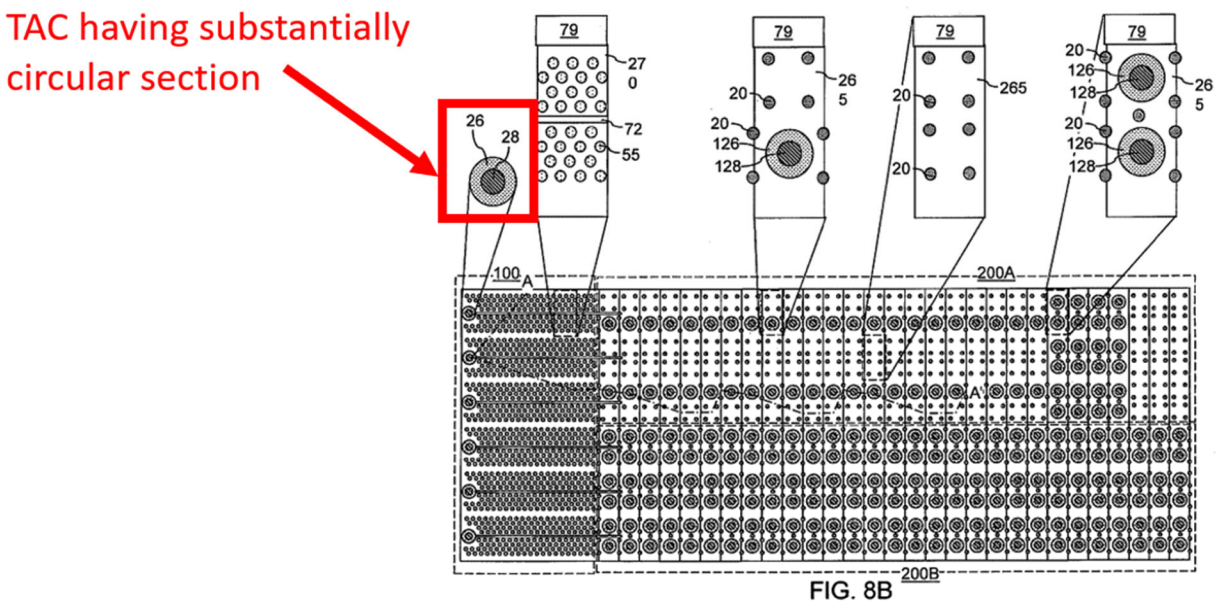
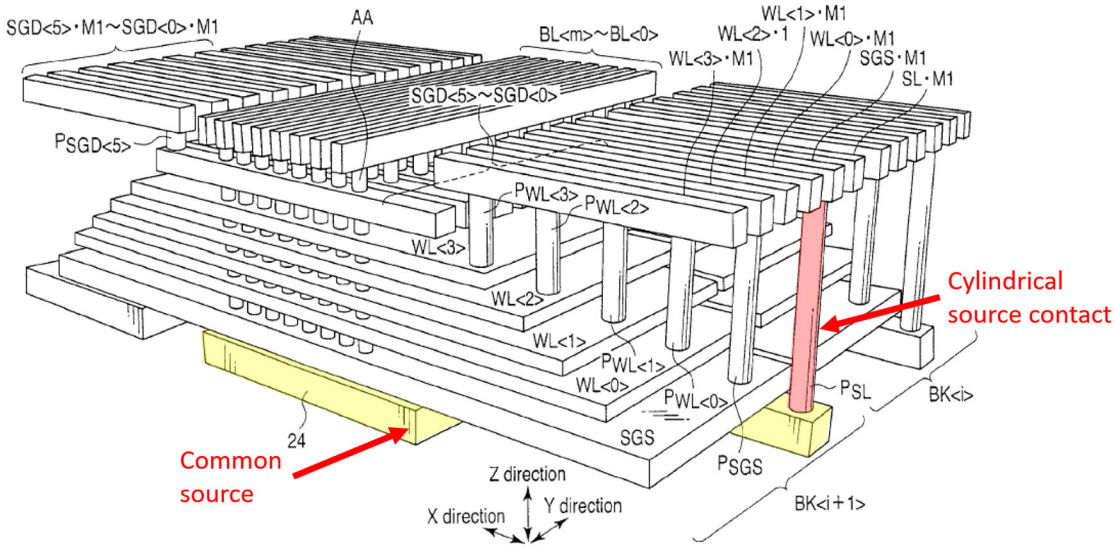


FIG. 8B

Masamori, Fig. 8B (annotated).

Next, implementing source line contacts as cylindrical structures was well known. For example, Maejima discloses a cylindrical source contact extending from above a memory stack down to a common source below the memory stack as illustrated below:



Maejima, Fig. 1 (annotated), 4:59-62 ("A source diffusion layer 24 formed in a semiconductor substrate is shared by, for example, all the blocks. The source diffusion layer 24 is connected to a source line SL·M1 through a contact plug P_{SL}."). Indeed, cylindrical source contacts were textbook material before the filing of the '322 Patent:

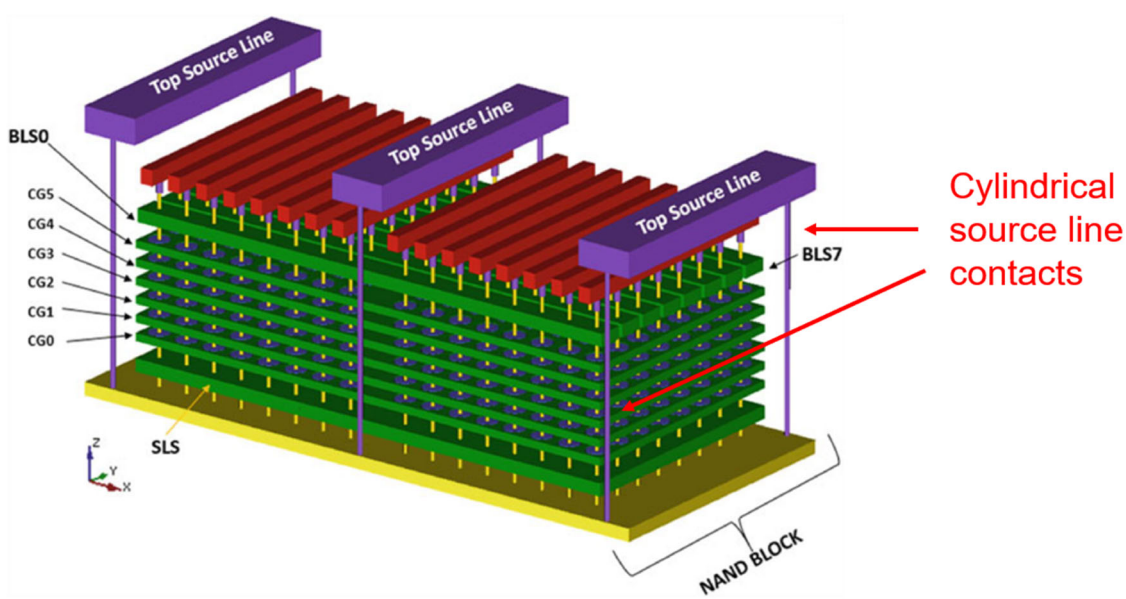


Fig. 5.17 C-FG array with top source line

Micheloni, 155.

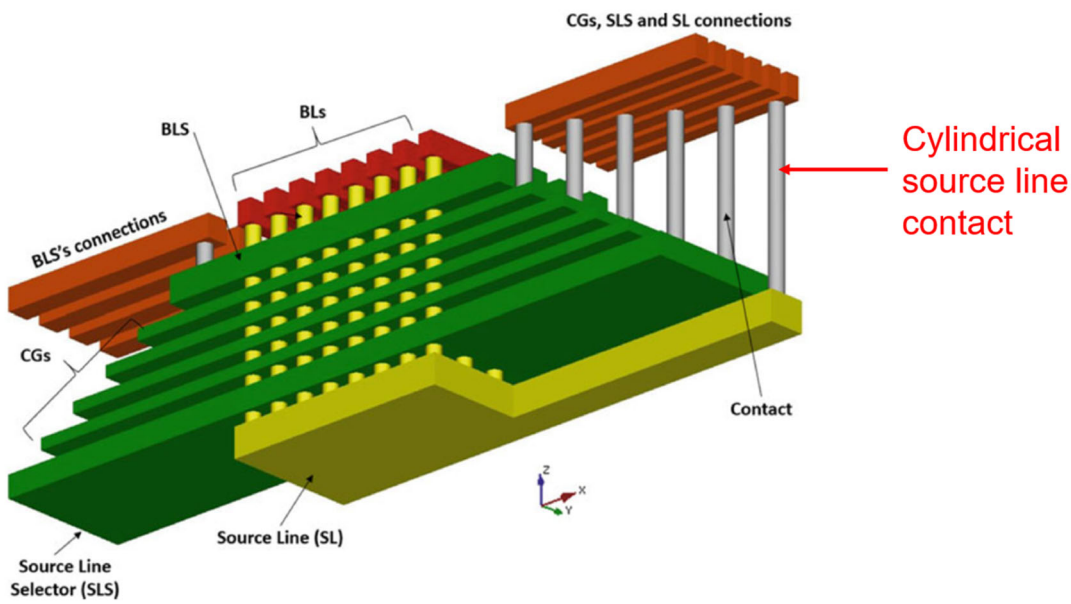


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Id., 110.

Finally, even if were one to implement the gate replacement process in a circular hole for a TAC, a POSITA understood that using circular holes for the TACs and those holes for the gate replacement process was a suitable option. Iwai, for example, teaches using cylindrical voids (79) for the gate replacement process:

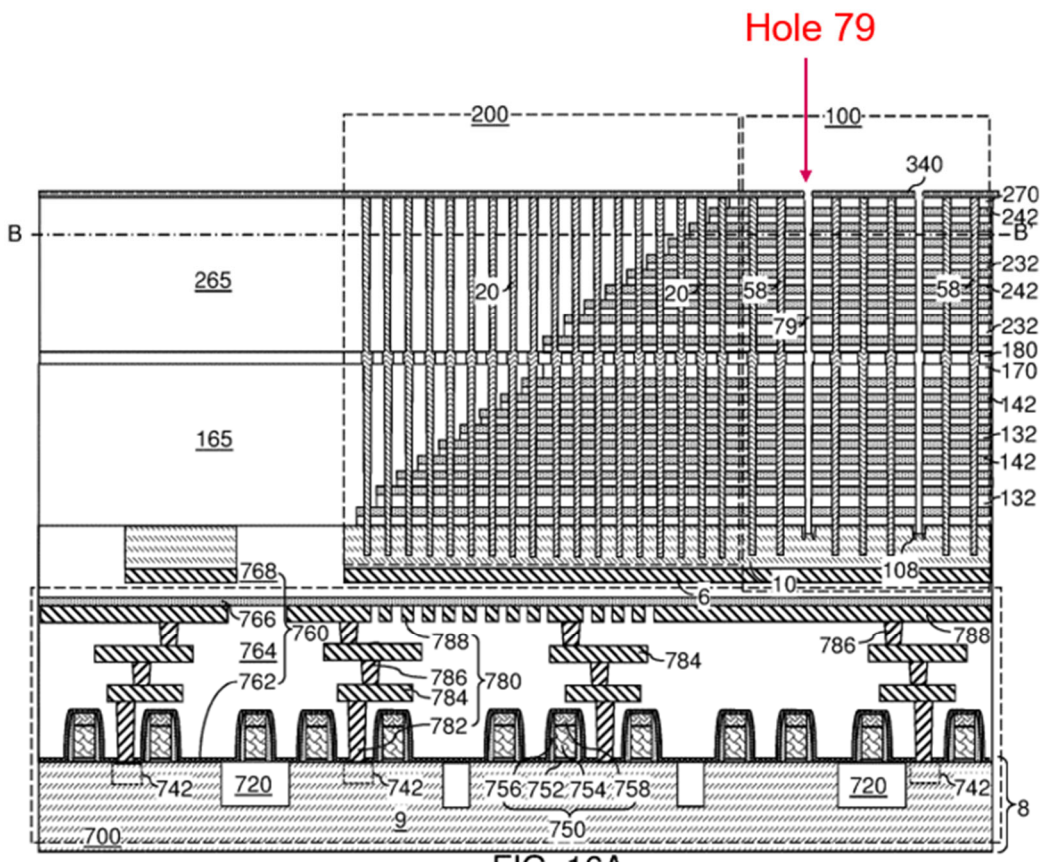


FIG. 16A

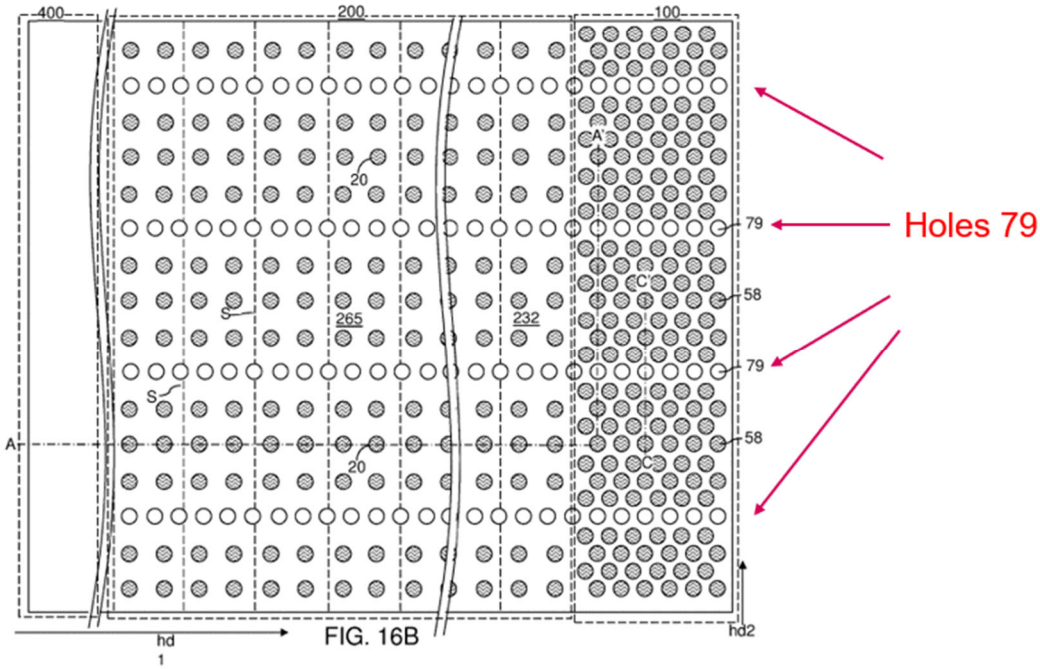


FIG. 16B

Iwai, Figs. 16A, 16B, 28:52-65 (extending through stack), 30:25-58 (using 79 voids for gate replacement process); *see also id.*, Fig. 25B, 33:18-21 ("Thus, each electrically conductive layer

(146L, 246L) can be formed as a continuous material layer including multiple rows of holes, which are the multiple rows of backside openings 79."), 37:47-51 (circular 79 arrangement). Iwai further discloses that the voids 79 may be converted to a trench if there is a desire to segment the array. *Id.*, 33:22-49, 34:18-33 ("In contrast, as shown in FIG. 19C, the backside openings 79 are not significantly expanded and are not merged into continuous trenches at the levels of the insulating layers (132, 232)."). In other words, Iwai expressly recognizes that a trench is not necessary for the gate replacement process.

Accordingly, in addition to the below motivations, replacing the backside contact via with cylindrical TAC was a "known technique" that was at least "a suitable option" for 3D memories. *Retractable Techs.,* 653 F.3d 1296, 1303 (Fed. Cir. 2011).

The trench has a large footprint. Replacing the trench with smaller cylindrical source contact(s), in effect, recovers a large portion of that lost footprint, providing additional room for memory cells. In short, the modification increases the memory capacity. In addition, it was well known to advantageously spread source connection points throughout the array. Micheloni, 111 (showing 3 source connections); Park, 6:8-12, Fig. 11 (showing first and second common source lines spread throughout memory array).

TACs enable connecting upper-level devices to underlying logic, e.g., under the stack. This beneficially saves space, e.g., moving peripheral logic to under the array. As the above demonstrates, a POSITA would have had a high expectation of success, because the processes therefor were textbook material, e.g., anisotropic etch, conformal deposition of a spacer, and CVD deposition of the conductive core. In addition, as illustrated above, cylindrical contacts, including those that extend through the memory stack, were well known. Cylindrical contacts were known to be suitable for, e.g., source connections and the holes therefor were known to be suitable for the gate replacement process. Again, processing techniques to implement these features were routine.

b. Dummy Channel Structures

To the extent any '322 Patent Primary Reference is determined to be missing the claimed "a dummy channel structure filled with a dielectric layer" a POSA would have considered it

obvious and been motivated to include such dummy channel structures, e.g., in view of the art below.

To start, regardless of whether the gate replacement process is used, it was well known to include dummy channel structures in memory stacks for processing reasons. First, adding dummy channel structures would reduce the likelihood of defective bits on the edge of the memory cell region, because the additional rows of dummy channel structures extend the memory cell pattern to include the dummy region on the edges. It was well known that when a pattern stops (instead of extending into the dummy region), defects occur on the edge. Park, 8:47-52 and Lee 487, 2:20-43 (both explaining the edge effect). Second, adding dummy structures would result in an overall more uniform feature pattern, which reduces processing issues. Ronse, 11 (explaining this processing issue). Thus, expanding the channel structure region (that is, in the cell region of the memory stack) to include dummy channels structures on all edges (that extend through the memory stack), thereby resulting in the dummy channel structures surrounding the active region, was a well-known technique to improve yield.

Next, if employing the gate replacement process, it was well known to include dummy channel structures to provide structural support. For example, Masamori discloses that as three-dimensional devices scale to smaller sizes, additional structural support is desired during the sacrificial gate replacement process. Masamori, [0003]. Masamori discloses a dummy channel structure ("semiconductor-containing support structure 20") that extend vertically through the conductor/dielectric layer pairs (second insulating layers 232, second conductive material layers 246 and first insulating layers 132, first conductive material layers 146) in the memory stack (annotated in Fig. 7A below). Although the layers of the semiconductor-containing support structure 20 are described in the context of the memory opening fill structures 55, Masamori discloses that "[t]he memory opening fill structures 55 and the semiconductor-containing support structures 20 can be formed simultaneously employing a same set of processing steps." *Id.*, [0085]. Thus, a POSITA would have understood that the semiconductor-containing support structures 20 have the same layers as memory opening fill structures 55, as shown in Fig. 7A (including the dielectric layers, e.g., tunneling and blocking layers).

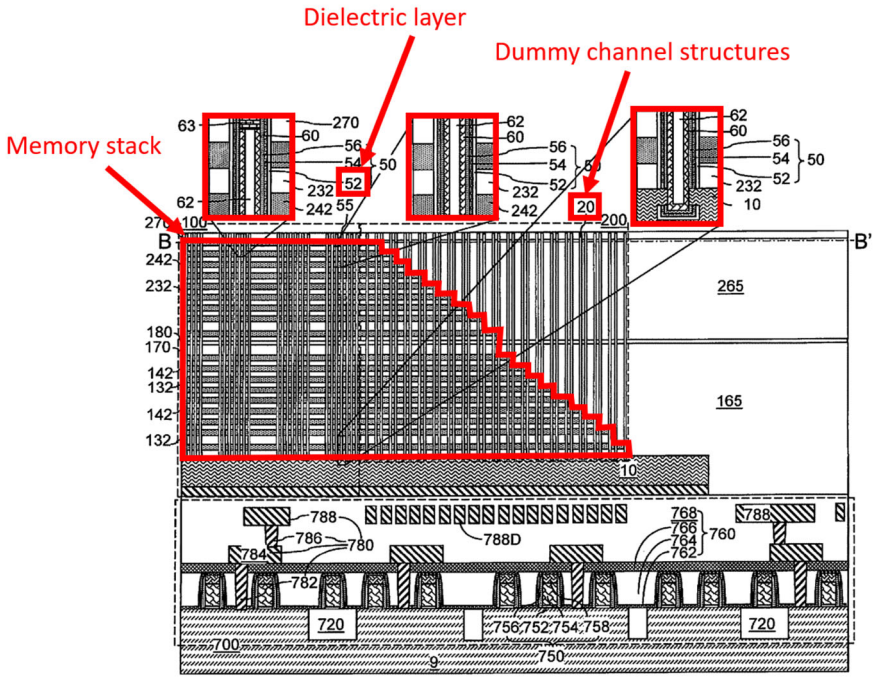


FIG. 7A

Masamori, Fig. 7A (annotated). Masamori discloses that "[t]he blocking dielectric layer 52 includes a blocking dielectric layer material such as silicon oxide, a dielectric metal oxide (such as aluminum oxide), or a combination thereof." Masamori, [0086]. Silicon oxide layers are dielectric layers. As illustrated, the semiconductor-containing support structures 20 extend through the second insulating layers 232, second conductive material layers 246 and first insulating layers 132, first conductive material layers 146.

Kai further confirms the knowledge of a POSITA regarding dummy channel structures. Kai, for example, discloses forming active and dummy channels, which provide structural support. Kai, 9:23-26 (defining "support opening" as "a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed"), 9:45-48 ("support openings 19" extend through stack), 10:20-26 (forming channels in support openings). Kai refers to the dummy channels as "support pillar 20" and active channels as "memory stack structures." *Id.*, 16:28-48, Figs. 6A, 15A, 25:58-63 (dummy support channels (20) have no connection to the upper level, whereas the active channel structures (55) include contacts (88)). Park2, likewise, discloses active and dummy supporting channels. Park2, 6:19-26, 7:45-51. Kim2, too, forms active channels and dummy channels through the stack at the same time. Kim2, [0047]

("The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region CTR," "DS [Dummy Structure] may physically support," and listing same materials as channels), [0071] ("The channel holes CH and the dummy holes DH may be formed at the same time."), [0072] (same time), Fig. 13 (DH through stack on edge). It was known that to perform this gate replacement process, "support pillars" were necessary. Tang, 5:64-6:2, 7:19-22.

Thus, additional motivation to use dummy channels when employing the gate replacement process includes, first, providing additional support during the gate replacement process. *E.g.*, Kai, Fig. 6A (support members 20), 16:28-39. It was well known that adding additional dummy channels "provide[s] additional structural support during replacement of the [sacrificial gate layers]." Masamori2, 30:14-27; *see also id.*, 15:3-22 (structures 20 are dummy channel structures). Second, dummy channels can be made by the same process and at the same time as the active channels. Kai, 10:20-26. Third, dummy channels do not require connections to the upper-level devices, thereby not consuming space above the structures while also serving as support structures. Park2, 8:55-65.

Adding dummy channel structures would have been routine and a POSITA would have had a high expectation of success. First, 3D memories already disclose forming channel structures, and the same materials are used for dummy channels. Second, for the reasons above, the additional dummy channel structures would actually reduce processing issues. Third, demonstrated above, dummy channels were commonplace.

Note that fully filling dummy channel structures with a dielectric material would have been obvious as well. One known beneficial use of dummy structures was as a support pillar. A common support pillar was a solid dielectric, e.g., silicon oxide, pillar. Sharangpani, 15:21-39 ("dielectric support pillar 7P"). The benefit of the complete fill is that it provides more support relative to partial fill. *Id*.

c. Silicon Oxide Spacers

To the extent any '322 Patent Primary Reference is determined to be missing the claimed "wherein each of the dielectric layer in the dummy channel structure, a spacer in the TAC, and a

spacer in the peripheral contact comprises silicon oxide" a POSA would have considered it obvious and been motivated to such silicon oxide spacers, e.g., in view of the below art.

A POSITA would have been motivated with a reasonable expectation of success to employ silicon oxide as the spacers and as the dummy channel material layer as well as the spacer material for other vertical structures for several reasons. First, for example, 3D NAND devices, e.g., Nishikawa3, already disclose using silicon oxide as a dielectric material to form other dielectric layers such as "insulating layers 32" and "blocking dielectric layer 52." Nishikawa3, 7:17-33, 11:52-57. Second, silicon oxide was the typical dielectric material for spacers and channel structures, because of its relative ease of use in semiconductor fabrication. Wolf Vol. 1, 182-183. Third, silicon oxide was known to be an ideal insulator. Finally, a POSITA would have had a reasonable expectation of success. Again, for example, 3D NAND devices, e.g., Nishikawa3, already employ silicon oxide in its process. And the deposition of silicon oxide to form spacers was routine, e.g., including the conformal deposition of silicon oxide spacers. *Id.*; Nakajima, 7:44-49.

d. Array and Peripheral Contacts of the Same Size

To the extent any '322 Patent Primary Reference is determined to be missing the claimed "a diameter of the TAC is at least equal to a diameter of the peripheral contact" or a "peripheral contact" in general, a POSA would have considered it obvious and been motivated to include such contacts, e.g., in view of the below art.

For example, one common, textbook approach was to make contacts the same size. Wolf Vol. 2, 47. As the '254 analysis discusses, peripheral contacts allow for peripheral contacts to peripheral devices, e.g., peripheral logic. And using the same contact size was known and standard specifically in the 3D memory space as well. For example, Mushiga discloses forming, at the same time, through-array contacts (588), having the same size and using the same processing steps:

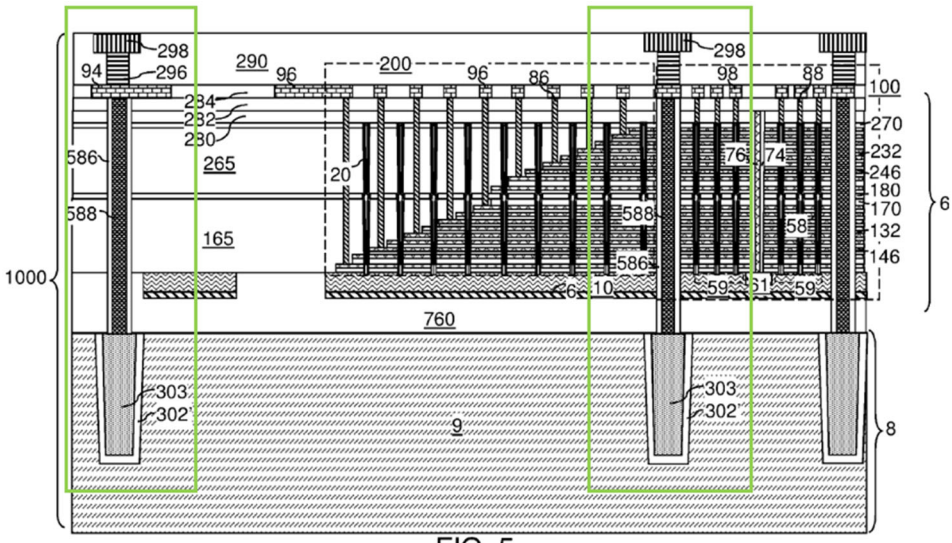


FIG. 5

Mushiga, Fig. 5 (annotated), 10:31-58. As another example Nakajima discloses forming holes H1 through the stack for its TAVs (C4). One C4 structure is outside of the stack (on the right below):

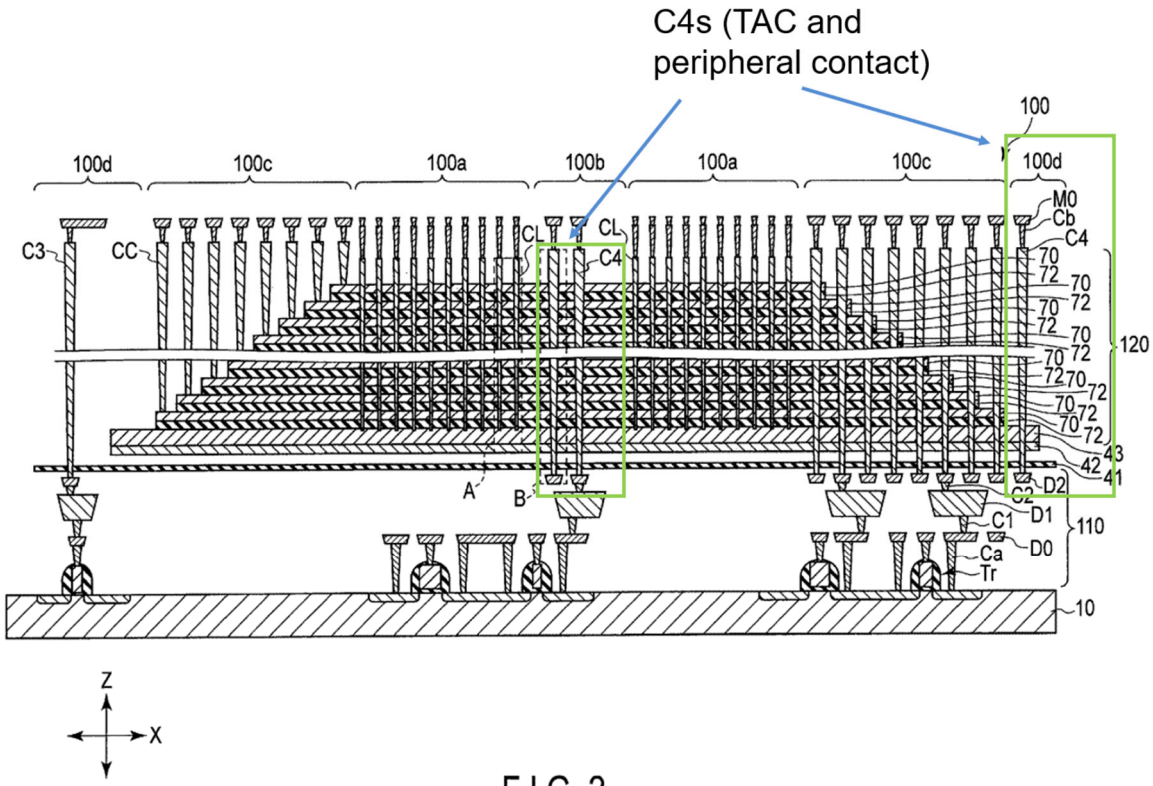


FIG. 2

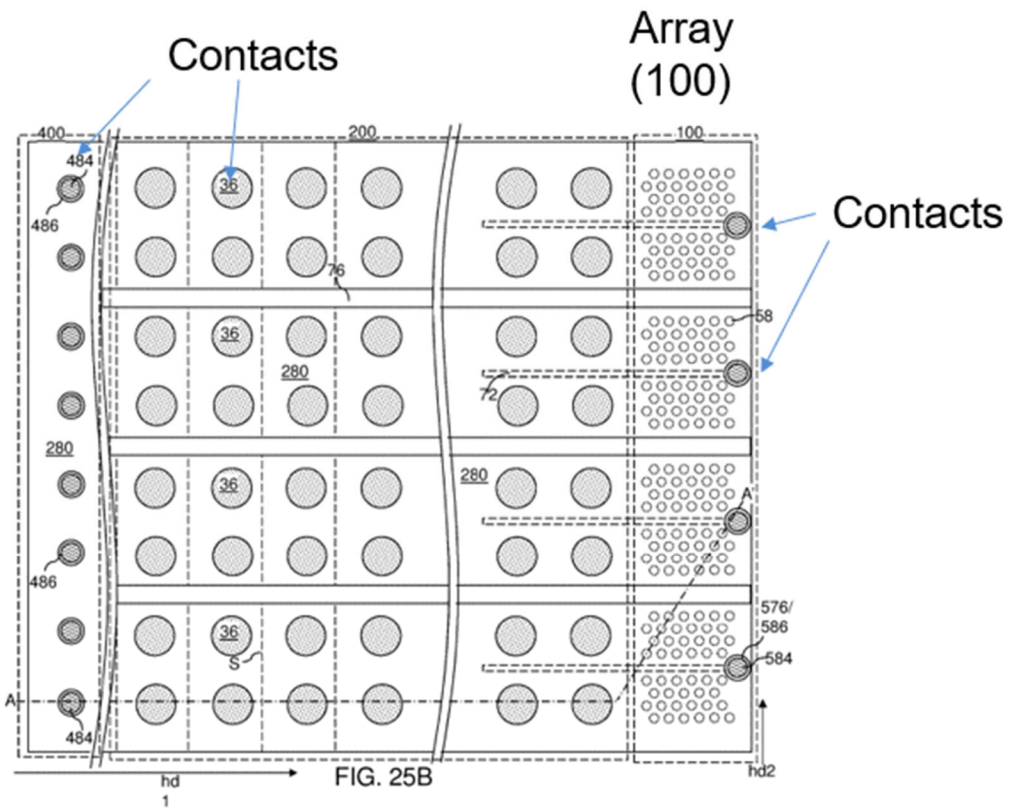
Nakajima, Fig. 2 (annotated). Nakajima only discloses one step for creating the H1 holes. Id., 7:37-43. And Nakajima only discloses one set of steps for forming the C4 contacts. *Id.*, 7:5-8:11.

A POSITA would have been motivated to make the TAC and peripheral contacts the same size to employ a common process (including the hole size in masking steps) when forming the contacts. As can be seen above, this is precisely what Mushiga and Nakajima do for contacts in, and outside, the array. It saves considerable process time to use a common set of process steps to form multiple elements. That is why it was known to form openings for different structures at the same. *E.g.*, Tessariol, [0037] ("dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously)"), Fig. 9. But if the holes sizes are different, then modifications to the etch chemistries are necessary. Wolf Vol. 2, 47. Because of this well-known benefit, process technologies, e.g., etch chemistries, that achieve simultaneous etching of different holes had become textbook material before the '322 Patent was filed. *Id*.

e. Dummy Channel Structures of Smaller Diameter Than TACs and Peripheral Contacts

To the extent any '322 Patent Primary Reference is determined to be missing the claimed "a diameter of the dummy channel structure is smaller than each of a diameter of the TAC and a diameter of the peripheral contact" a POSA would have considered it obvious and been motivated to so form such channel structures, e.g., in view of the below art.

Memory stacks contain millions or billions of channel structures, and these channel structures are smaller than contacts because the entire point of a memory is to have a very dense memory region. Indeed, the fabrication process typically uses special processing to form a dense memory array region. Thus, it was textbook material to make the channel holes as small as possible, typically using memory-hole specific processing steps. Micheloni, 211-215. Dummy channel holes will generally have the same size as active channel holes to maintain a uniform pattern and reduce the edge effect issues (that is, repeating the uniform pattern). Recall the memory and dummy memory holes are made using the same process as well. For example, below is a top-down view showing channel structures in region 100 versus various contacts in regions 200 and 400:



Cui, Fig. 25B (annotated). A POSITA would have understood the above figure to illustrate that features in the dense array are relatively smaller than features in the less dense peripheral region. Thus, it would have been understood, or at least obvious, that the dummy channels have a diameter that is smaller than the diameters of the TACs and peripheral contacts.

f. Unintentional Recesses

To the extent any '322 Patent Primary Reference is determined to be missing the claimed "wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs," under YMTC's infringement theory, it would have been obvious. *See* "unintentional recesses" analysis limitation for '254 patent; *see also* Shen, 2:59-67.

g. Rib-shaped Through Array Contacts

To the extent any '322 Patent Primary Reference is determined to be missing the claimed "wherein a first lateral dimension of the TAC corresponding to each conductive layer of the

conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs" a POSA would have considered it obvious and been motivated to form TACs as claimed, e.g., in view of the below art.

It was well known that an option for a TAC or other through-memory structures was to have a ribbed shape, that is, forming recesses in one of the stack layers. For example, Cui discloses contacts 183 that travel through the staircase and through the entire array. Cui, Fig. 14A, 25:51-53 (e.g., 183 contact on right of region 200); *see also* Ex. 1027, 11:9-34 ("laterally recessed"). Cui depicts an embodiment in which the sidewalls of this contact are straight ("cylindrical via cavity"). Cui, Fig. 15A, 25:63-26:22. And it depicts an alternative embodiment that intentionally creates large recesses in the insulating layers ("ribbed via cavity"). *Id.*, Fig. 16A, 26:23-32.

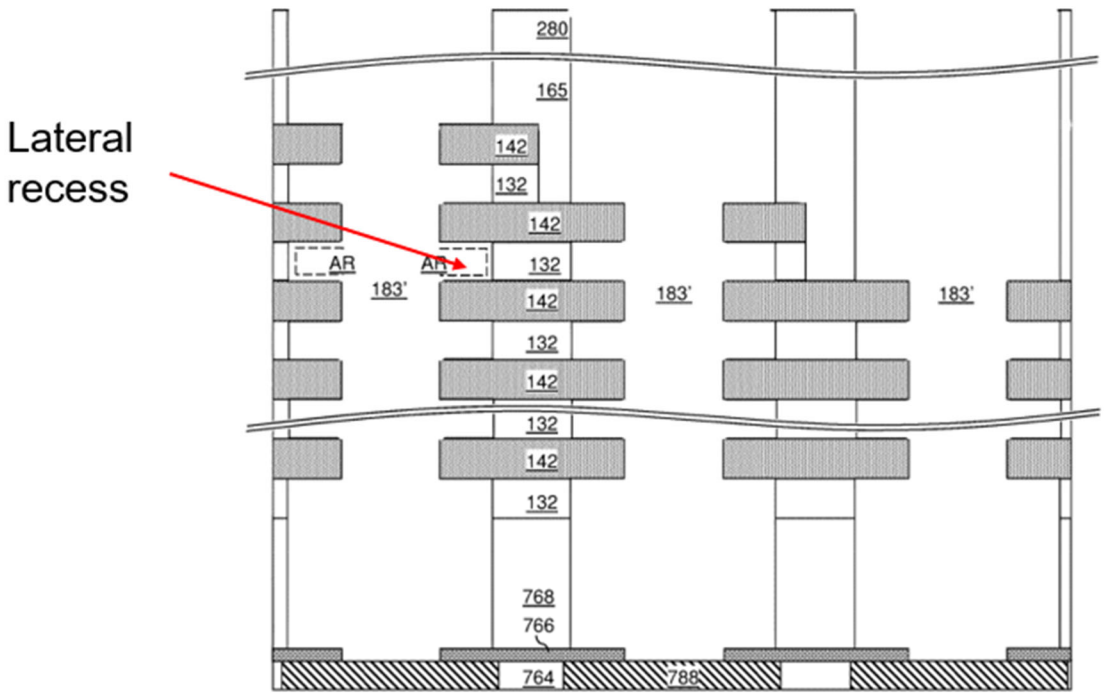


FIG. 16A

Id., Fig. 16A (annotated).

It would have been further obvious, and a POSITA would have been motivated, to create a ribbed via cavity in, for example, Nishikawa3's through-array via holes. First, it was known to create lateral recesses to form "rib regions." *Id.*, 26:23-32. This advantageously creates additional area for the insulating spacer. Second, there are only two options for creating such rib regions: in

the sacrificial (or conductive) gates or in the dielectric layers. Both were known and result in a common benefit. Cui, Fig. 16A, 26:23-32 (recesses in the insulating layers); Kai, 11:9-34 (recesses in sacrificial gates). A POSITA would have had a high expectation of success in forming the rib regions because the isotropic and selective etches were well known. Cui, 26:33-45; Kai, 11:9-34.

h. Same Thickness of Spacer on Through Array Contacts and Peripheral Contacts

To the extent any '322 Patent Primary Reference is determined to be missing the claimed "wherein a thickness of the spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact" a POSA would have considered it obvious and been motivated include such spacers, e.g., in view of the below art.

It would have been obvious for the spacers to have a nominally identical thickness, particularly if the holes are the same size, because the spacer deposition will form spacers of nominally identical thicknesses. Again, forming the contacts at the same time, including the spacer deposition step, saves processing time.

Mushiga conceptually illustrates that this simultaneous formation of spacers in forming through-array contacts (588) results in the same spacer thickness:

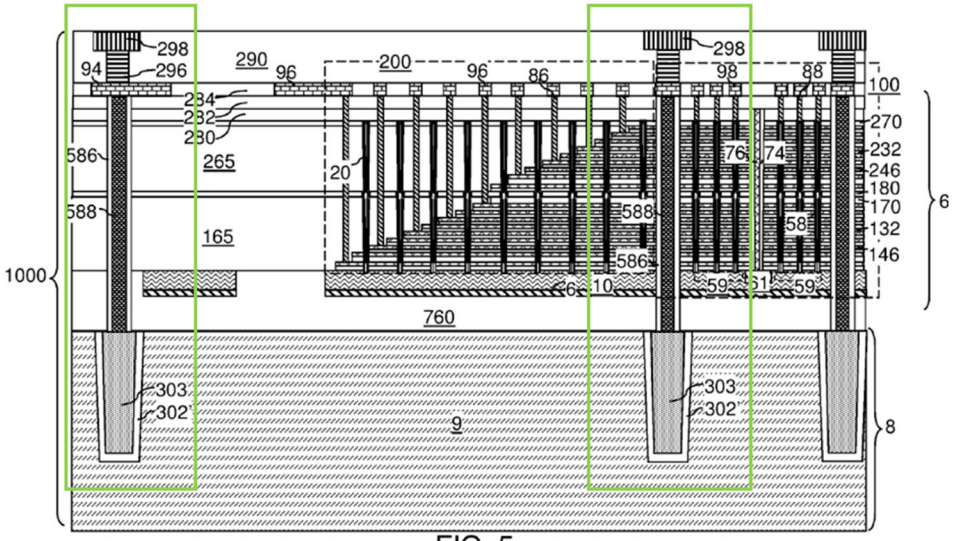
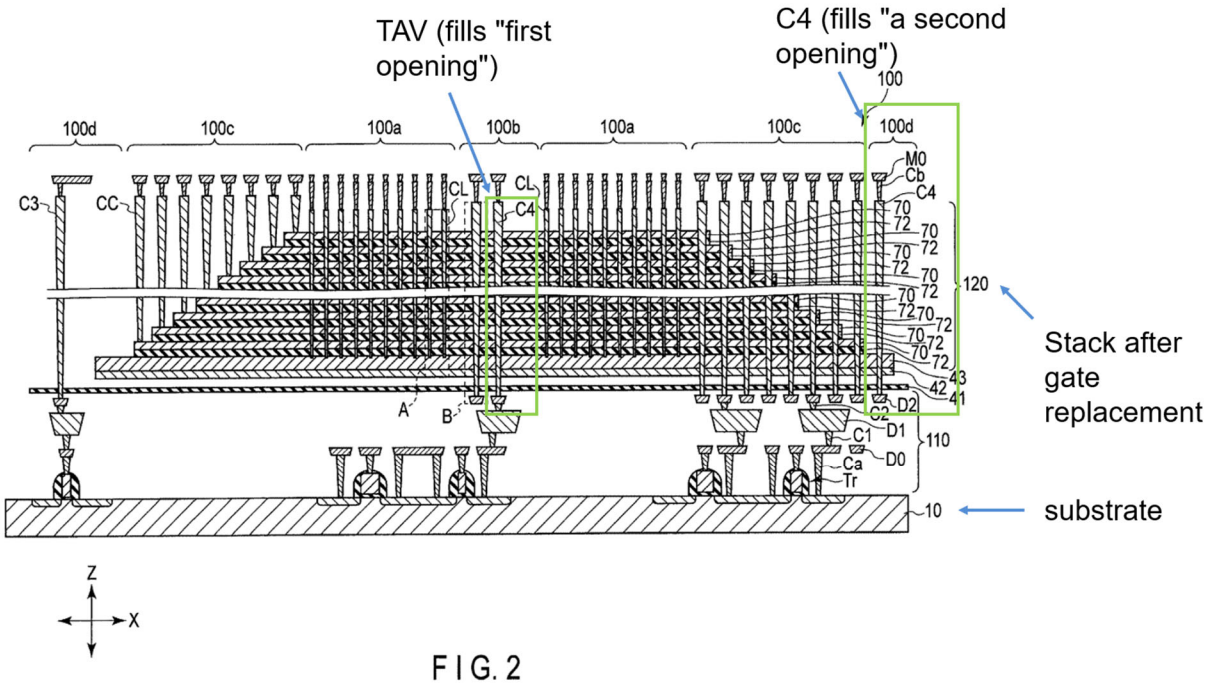


FIG. 5

Mushiga, Fig. 4 (annotated), 10:31-58.

Forming spacers of the same thickness can also be seen in Nakajima, as Nakajima discloses

forming one type of contact (C4) in various parts of the array, and only discloses a single spacer type:



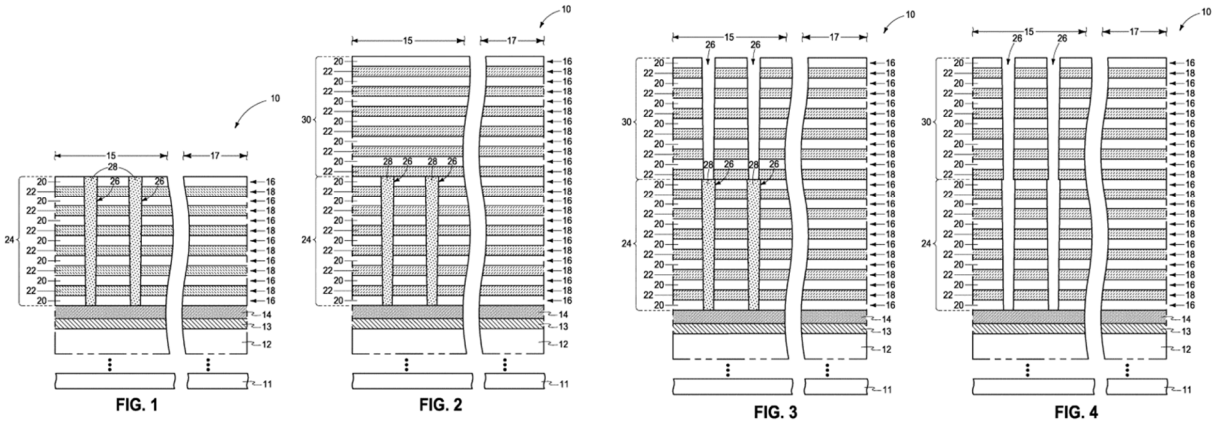
F I G. 2

Nakajima, Fig. 2 (annotated). A POSITA would have had a high expectation of success, because the process merely involves forming the conformal oxide spacer at the same time or with the same process, which was textbook material. *See* §IV.A.3.c.

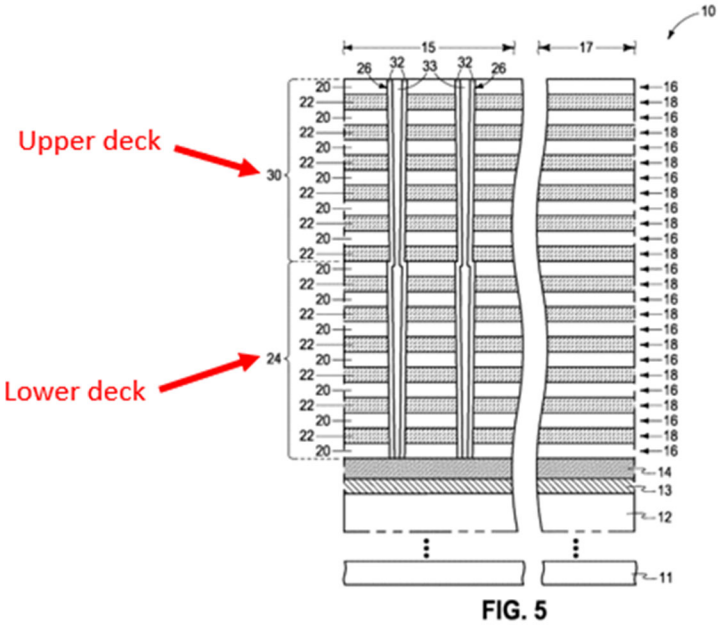
i. Multi-Tier Memory Arrays

To the extent any '322 Patent Primary Reference is determined to be missing the claimed "memory stack" comprising "a lower memory deck on the substrate" and "an upper memory deck above the lower memory deck" a POSA would have considered it obvious and been motivated to include such memory stacks, e.g., in view of the below art.

A multi-deck memory stack refers to forming a first stack and then forming a second stack on top of the first. The driving motivation for multi-deck structures is the difficulty in etching high aspect ratio channel holes. This challenge became a limiting factor to memory density. Micheloni, 211-215. A multi-deck structure, however, enables the formation of high aspect ratio channel holes by forming the first deck, etching a hole through the first deck, forming the second deck, and then etching another hole through the top deck. This is shown below:



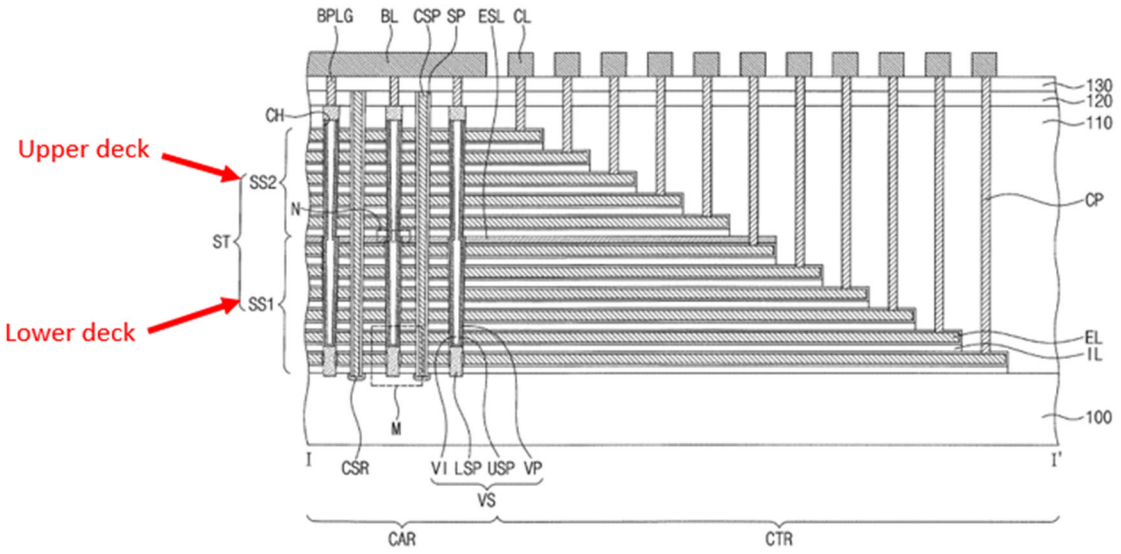
Tessariol, Figs. 1-4. The final channel structure is shown below:



Id., Fig. 5 (annotated). As can be seen above, each hole tapers due to natural etch processes. If there was only a single etch through a single stack with the same number of layers as both decks, the taper would be so large that the hole's diameter on the top would be too large, requiring too much surface area for a single channel. In effect, the taper would be twice as much, and the channel footprint on the surface of the top stack layer would be double in size.

As such, multi-deck 3D memories became the norm. For example, Kim1 discloses a multi-deck 3D NAND stack structure:

FIG. 4A



Kim1, Fig. 4A (annotated). Kim1 discloses that "[a] cell array block BLK may be disposed on the substrate 100. The cell array block BLK may include stack structures ST, each of which includes insulating layers IL and electrodes layers EL which are vertically alternately stacked (sometimes referred to as alternating electrode layers and insulating layers). Each of the stack structures ST may include a lower structure SS1 and an upper structure SS2. The upper structure SS2 may be disposed on the lower structure SS1." *Id.*, 5:60-6:1.

As yet another example, Masamori discloses a multi-deck 3D NAND stack structure:

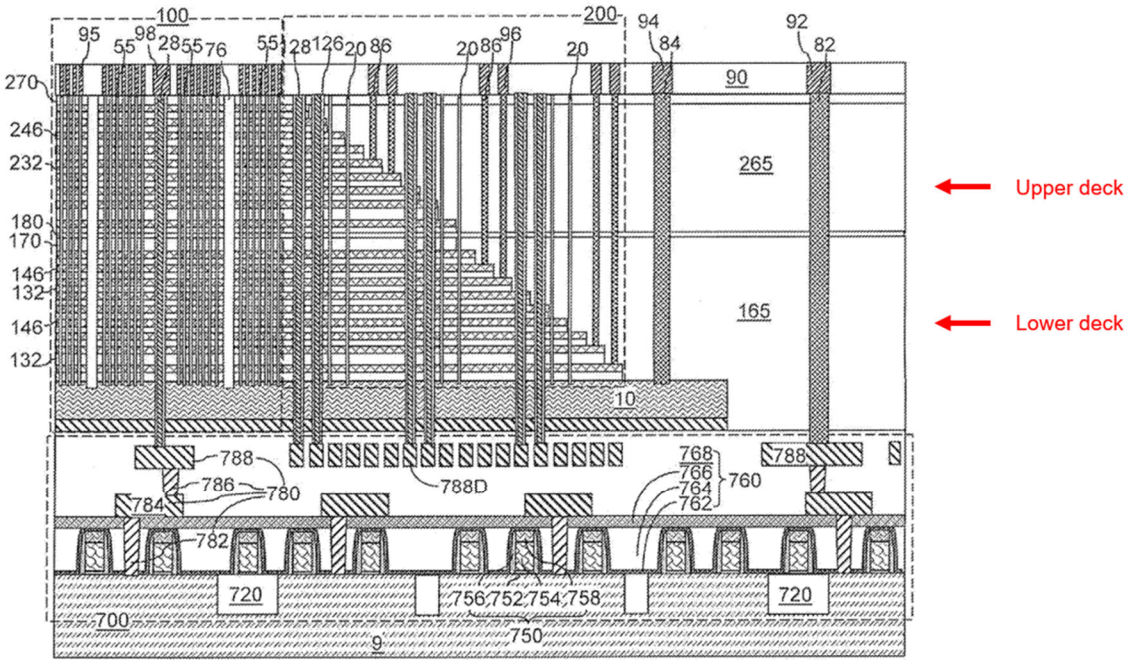


FIG. 14

Masamori, Fig. 14 (annotated). Masamori discloses that "[a] second tier structure can be formed over the first tier structure (132, 142, 170, 131). The second tier structure can include an additional alternating stack of insulating layers and spacer material layers, which can be sacrificial material layers. For example, a second alternating stack (232, 242) of material layers can be subsequently formed on the top surface of the first alternating stack (132, 142)." *Id.*, [0073].

By way of another example, Lu itself recognizes that "[a]s demand for storage capacity increases, the number of memory cell levels in some memory devices may be increased to accommodate the increased storage capacity. In some cases, forming such memory devices using conventional techniques may pose a challenge." *Id.*, 1:13-22. That is, forming the dense array via high-aspect ratios poses a challenge. Thus, Lu discloses techniques to form a first deck, etch the channel sub-hole, form a deck on top of that, and then etch another channel sub-hole. *E.g.*, Lu, Fig. 3A-L.

Thus, a POSITA would have been highly motivated to employ multi-deck teachings to at least reduce the widths of the channel holes in any 3D memory device.

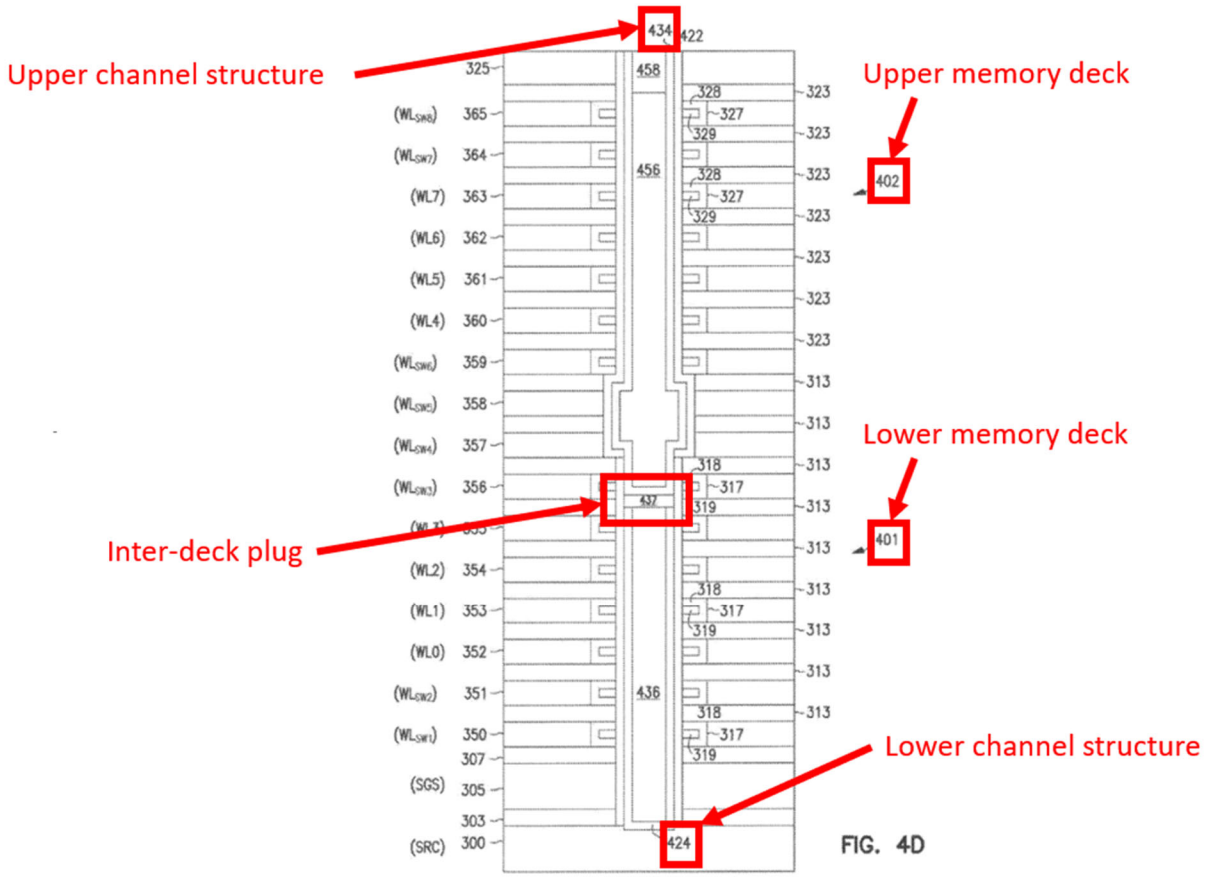
A POSITA would have had a reasonable expectation of success in adapting any of the '322 Patent Primary References to include a multi-deck structure. As the above multi-deck structures illustrate, multi-deck structures were the norm, including in devices that employ TACs. Typically, the process first creates the multi-deck structure and channels, then the TACs and slits. *E.g.*, Tessariol, [0029]-[0033] (forming decks and channels), [0034]-[0037] (forming staircase), [0038]-[0040] (forming TACs and dummy structures), [0041]-[0044] (forming trenches and performing gate replacement process).

j. Multiple Channel Structures Connected by an Inter-Deck Plug

To the extent any '322 Patent Primary Reference is determined to be missing the claimed "channel structure" comprising " a lower channel structure extending vertically through the lower memory deck," " an upper channel structure extending vertically through the upper memory deck," and "an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure," a POSA would have considered it obvious and been motivated to so form channel structures, e.g., in view of the below art. §IV.A.3.j discusses the motivations and obviousness of multi-deck structures.

Notably, the inter-deck plug provides a larger interface between the sub-channels, i.e., the lower and upper deck channel structures. This beneficially ensures electrical coupling between the sub-channel plugs to ensure the sub-channels collectively operate as a single channel structure consistent with teachings of Lu below.

For example, Lu discloses an inter-deck plug ("material 437") disposed vertically between and in contact with the lower channel structure ("channel material 424") and the upper channel structure ("channel material 434"):



Lu, Fig. 4D (annotated).

Lu discloses "with reference to FIG. 4A through FIG. 4D may be used to form a . . . channel with solid conductive plug (e.g., polysilicon plug) between the . . . channel." Lu, 14:25-28. Lu further discloses that "[a] material 437 can be formed adjacent tunneling material 312 . . . . Material 437 can include polysilicon (e.g., conductively doped polysilicon)." *Id.* 14:38-43. As illustrated, conductive polysilicon material 437 is formed between and in contact with the lower channel material 424 and upper channel material 434. A POSITA would have had a high expectation of success, because the deposition is a simple deposition of, e.g., poly, and the larger interface ensures both channel structures connect thereto.

k. Additional Motivations for Micron's Prior Art Products

The above sections demonstrate that a POSA would have been motivated to combine the '322 Patent Primary References, including Micron's prior art products (B27A), with various prior art references. Note that Micron's bit line exit region provides an area for contacts. As the

discussion in Section IV.A.3.a demonstrates, implementing those contacts as TAC through the array was readily known. And as Tessariol demonstrates (another Micron patent), Micron already had the TAC technology, and in fact, this Section demonstrates that TACs that extend through various portions of the array were well known. As B27A and Tessariol both demonstrate Micron prior art technology, both are fully compatible.

B. Invalidity Based on Improper Inventorship Under Section 101 (Patent L.R. 3-3(d))

The Asserted Claims of the '322 Patent are invalid under 35 U.S.C. § 101 because the patent improperly omits inventors that contributed to the invention of the subject matter sought to be patented. In this regard, 35 U.S.C. § 101 states that "[w]hoever invents … may obtain a patent … ." On information and belief, employees of Micron contributed to the inventions claimed by the '322 Patent and such Micron employees have been improperly omitted from the list of named inventors on the patent.

The '322 Patent currently names Hongbin Zhu as an inventor of the claimed subject matter. Hongbin Zhu worked at Micron as an engineer from January 9, 2006, to September 18, 2017. The application which resulted in the '322 Patent was filed on August 21, 2018, meaning that Hongbin Zhu had been working on 3D NAND technology at Micron shortly before the filing of the application for this patent. On information and belief, Hongbin Zhu worked with other Micron employees at Micron to conceive of the invention claimed in the '322 Patent and thus these Micron employees have been improperly omitted as named inventors of the patent. Furthermore, YMTC is a latecomer to 3D NAND products and technology, having only been established in 2016, long after Micron had patented, manufactured, and shipped its first 3D NAND products. This all suggests that the subject matter claimed in the patent was conceived and developed at Micron and involved other Micron employees not currently listed as named inventors on the patent.

Micron is currently seeking discovery from YMTC related to inventorship of this patent and individuals who contributed to the conception of the invention claimed in this patent. However, despite Micron's requests, YMTC to date has refused to provide responsive information or documents.

C. Invalidity Based on Section 112 (Patent L.R. 3-3(d))

1. Indefiniteness

Defendants provide the following grounds for invalidity under 35 U.S.C. § 112. Defendants' investigation of the Asserted Patents is ongoing, and Defendants reserve the right to amend or supplement these disclosures based on further investigation and in a manner consistent with the Federal Rules of Civil Procedure, the Local Patent Rules for the Northern District of California, and the Docket Control Order, or otherwise in accordance with any order or direction of this Court or agreement of the parties. Further, Plaintiff's Infringement Contentions fail to provide sufficient detail to fully understand its proposed application of the Asserted Claims, and Defendants reserve the right to assert additional grounds for invalidity under 35 U.S.C. § 112 in response to Plaintiff's claim interpretations. Defendants also reserve the right to supplement, modify, or otherwise amend these grounds for invalidity under 35 U.S.C. § 112 based on the Court's claim construction rulings or opinions or the parties' positions or arguments taken in connection with the claim construction process.

2. Written Description and Enablement

The specification of the '322 Patent does not provide adequate written description to support the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims. 35 U.S.C. § 112(a) requires that a patent specification contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharm., Inc.*, 598 F.3d at 1351 (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ.*, 541 F.3d at 1122 (quoting *Vas-Cath Inc.*, 935 F.2d at 1563–64). The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Additionally, the Asserted Patents do not enable the claim scopes contained in Plaintiff's Infringement Contentions. Section 112(a) requires a specification to describe "the manner and

process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention]." The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This "requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp.*, 344 F.3d at 1244 (citation omitted); *see Wyeth & Cordis Corp.*, 720 F.3d at 1385–86. The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Defendants provide below an identification of terms in Asserted Claims that render the Asserted Claims, at least as apparently construed by Plaintiff in its Infringement Contentions as discussed above, invalid pursuant to 35 U.S.C. § 112 as not enabled or lacking sufficient written description:

- "buried into the substrate"
- "isotropic etching"
- "fully filling"
- "a slit structure"

V. <u>INVALIDITY OF THE '291 PATENT</u>

A. Invalidity Based on the Prior Art

As shown below, the alleged inventions of the '291 Patent were well-known in the prior art. Those skilled in the art were aware of all of the limitations claimed in the '291 Patent. Thus, many prior art patents, publications, products, and combinations thereof, disclose, teach, or embody every limitation of the Asserted Claims and thus invalidate those claims. Examples of these disclosures, teachings, and embodiments are identified in the following sections and in the attached claim charts.

1. Identification of Prior Art References (Patent L.R. 3-3(a))

Subject to the reservation of rights above, Defendants identify each item of prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the '291 Patent. The patents/applications, publications, and systems identified are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations.

Some of the below citations and those in the corresponding invalidity claim charts involve prior art references that have corresponding related, foreign, and/or PCT counterpart publications. In such cases, where either the U.S. patent or related, foreign, and/or PCT counterpart is cited, it is to be understood that the corresponding disclosures from the counterpart patent and publications (which are substantively the same) are implicitly incorporated by reference in the alternative to avoid needless repetition.

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
K-01	U.S. 2018/0182771A1 ("Costa2")	Feb. 28, 2017	June 28, 2017
K-02	KR 101487746 ("Lee 746")	Feb. 7, 2014	Feb. 4, 2015
K-03	U.S. 9,768,018 ("Seo3")	April 13, 2016	Sept. 19, 2017
K-04	U.S. 9,245,962 ("Yang4")	Jan. 20, 2015	Jan. 26, 2016
K-05	U.S. 9,698,153 ("Liu4")	March 24, 2016	July 4, 2017
K-06	U.S. 9,343,475 ("Jang2")	Jan. 15, 2014	May 17, 2016
K-07	U.S. 2017/0162592A1 ("Nishikawa4")	Dec. 4, 2015	June 8, 2017
K-08	U.S. 2017/0154892A1 ("Oh2")	June 10, 2016	June 1, 2017
K-09	U.S. 2015/0279855A1 ("Lu2")	March 27, 2014	Oct. 1, 2015
§V.A.3.[9]	U.S. 20120126308A1 ("Yong 308")	Nov. 17, 2011	May 24, 2012
§V.A.3.	U.S. 2016/0300846A1 ("Yoshiaka 846")	Mar. 13, 2015	Oct. 1, 2016
§V.A.3.	U.S. 2010/0327339A1 ("Hiroyasu 339")		
§V.A.3.	U.S. 20150155296A1 ("Sung 296")	Dec. 3, 2013	Jun. 4, 2015
§V.A.3.	U.S. 9,837,431 ("Nishikawa3")	January 28, 2016	December 5, 2017
§V.A.3.	U.S. 2017/0179026 ("Toyama")	December 22, 2015	June 22, 2017
§V.A.3.	U.S. 9,595,531 ("Zhu")	July 11, 2014	March 14, 2017
§V.A.3.	KR1018075250 ("KR 250")	July 11, 2011	December 11, 2017
§V.A.3.	U.S. 9,905,575 ("Lee 575")	June 7, 2016	February 27, 2018
§V.A.3.	U.S. 9,536,896 ("Lee 896")	April 27, 2012	January 3, 2017
§V.A.3.	US20170263614A1 ("Tokuhira")	March 11, 2016	September 14, 2017
§V.A.3.	US20100327339A1 ("Tanaka")	June 24, 2019	December 30, 2010
§V.A.3.	US20150270282A1 ("Koshiishi")	March 20, 2014	September 24, 2015
§V.A.3.	US20150155296A1 ("Yoon")	December 3, 2013	June 4, 2015

Table K-1: Prior Art Patents and Patent Publications for the '291 Patent

[9] *See* §V.A.3. The equivalent of a chart is set forth with pinpoint citations to the reference in the motivation to combine sections. The same is true for all references without an exhibit.

Defendants are still investigating prior uses and sales. Based upon at least Plaintiff's apparent position as to the scope of the Asserted Claims, and as further explained below and in the cited exhibits, it appears that the following systems (and development thereof) qualify as prior art under at least one or more of 35 U.S.C. § 102(a):

Ex.	Description	Entities Involved	Prior Art Date
K-10	110 Series Products	Micron	8/10/2016

Table K-2: Prior Art Systems for the '291 Patent

Micron's 110 series products were publicly available, on sale, or in public use prior to the effective filing date of the '291 Patent. MYM0042611-MYM0042676, MYM0042896-MYM0042896, MYM0065110, MYM0065111.

Description	Availability
Travelers	to be made available via inspection
Process information	to be made available via inspection
Schematics	to be made available via inspection
Layouts	to be made available via inspection
Waveforms	MYM0042897-MYM0043247, MYM0069190-MYM0069236
TEM/SEM Imagery	MYM0043255-MYM0043296, MYM0043316-MYM0043339, MYM0043423-MYM0043424, MYM0043248-MYM0043254, MYM0058880-MYM0058891, MYM0069181-MYM0069181
Datasheets	MYM0043425-MYM0043844, MYM0065164-MYM0066151
Trim Spreadsheets	MYM0065112-

Description	Availability
	MYM0065115, MYM0069182-MYM0069189, MYM0069715-MYM0069940

Table K-3: Listing of Prior Art Systems Documentation for the ’291 Patent

2. Anticipation and Obviousness (Patent L.R. 3-3(b) and (c))

The Asserted Claims of the ’291 Patent are invalid because they are anticipated by the prior art and/or because they would have been obvious in view of the prior art.

The prior art identified by Defendants anticipates and/or renders obvious one or more of the Asserted Claims of the ’291 Patent under at least AIA §§ 102(a)(1), 102(a)(2), and 103. For each prior art reference, Defendants have provided claim charts attached to these Invalidity Contentions as Exhibits K-1 through K-10. These charts identify where each element of each Asserted Claim can be found in each item of prior art.

Again, to the extent not anticipated, the Asserted Claims of the ’291 Patent are invalid as obvious under 35 U.S.C. § 103. Each prior art reference identified in the preceding sections—either alone or in combination with another prior art reference and/or in combination with the knowledge of one skilled in the art—renders the Asserted Claims invalid as obvious. In rendering the Asserted Claims obvious, each prior art reference identified in the preceding sections may be combined with: (1) information known to persons skilled in the art at the time of the alleged invention, (2) any of the other anticipatory or obviousness prior art references, (3) any statements in the intrinsic record of the ’291 Patent and related applications, or (4) any of the additional prior art identified below.

3. Motivations to Combine[10]

A person of ordinary skill in the art would have been motivated to combine the preceding references (*see* Section V.A.1) for the following reasons. Teachings, suggestions, motivations and/or reasons to modify any of the references and/or to combine any two or more of the references

[10] The statements in this section about what was known and obvious to a POSA are made with respect to the effective filing date of the ’291 Patent.

can come from many sources, including the prior art (by specific reference and when read as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obviousness to try, the nature of the problem faced, and/or knowledge possessed by a person of ordinary skill.

Although a patent claim may be invalidated based on a teaching-suggestion-motivation ("TSM") rationale—*i.e.,* that some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention—the Supreme Court identified additional rationales in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007). The following of these rationales apply here:

> (A) the asserted claims combine prior art elements according to known methods to yield predictable results;
>
> (B) the asserted claims involve the simple substitution of one known element for another to obtain predictable results;
>
> (C) the asserted claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;
>
> (D) the asserted claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;
>
> (E) the asserted claims involve combinations of prior art references that would have been "obvious to try"'—a person of ordinary skill in the art could have reached the asserted claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
>
> (F) the asserted claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach); *see also* Department of Commerce, Patent and Trademark Office, Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.,* 72 Fed. Reg. 57,526 (Oct. 10, 2007). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity,

not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420-21.

Thus, even in the absence of a specific teaching, suggestion, or motivation to combine references, the Asserted Claims here are obvious and therefore invalid. Each of the cited references or devices is in the same field as the '291 Patent, making it obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. One of ordinary skill in the art would have recognized that improvements could be achieved by combining or modifying prior art references that described such improvements. Each of the above prior art references describes systems, products, or methods that were known to offer such improvements, and, accordingly, one of ordinary skill in the art would have been motivated to combine or modify the references as identified in each of the combinations below.

Furthermore, because each prior art reference concerns three-dimensional memory device designs, common industry knowledge supplied a reason to combine any one the above references. It was well understood that different three-dimensional memory structural features could be employed together or interchanged with each other, fitting together like puzzle pieces. Each combination would have produced predictable results and would simply represent a known alternative to one of ordinary skill in the art of memory devices (whether or not specifically related to three-dimensional memory devices). This is a further motivation to combine any of the above references.

The below sections further address particular reasons to combine the above references. The below should not be construed as an admission that there is any value to the alleged invention of the '291 Patent. As discussed previously, these contentions are based in significant part on how Plaintiff is apparently construing the asserted claim in its Infringement Contentions, which is an incorrect and overbroad interpretation of the alleged invention of the '291 Patent. Accordingly, to the extent the below refers to benefits of certain elements or industry trends towards these elements, this is not an admission that the alleged invention of the '291 Patent provides any benefits: to the contrary, properly construed and compared to the prior art, the '291 Patent provides no benefits. Likewise, to the extent the below refers to substituting elements, this is not an admission that the

elements subject to the substitution are in any way similar, *e.g.,* perform the same function, in the same way, to achieve the same result.

The various elements of the Asserted Claims were well known in the prior art at the time of the alleged invention, and the combination would have been obvious to one of skill in the art. The combinations simply (a) combine prior art elements according to known methods to yield predictable results; (b) involve the simple substitution of one known element for another to obtain predictable results; (c) involve the use of a known technique to improve similar devices (methods, or products) in the same way; (d) apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) involves combinations of prior art references that would have been "obvious to try" – a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and/or (f) would have been prompted by known work, based on design incentives or other market forces, because such variations were predictable to one of ordinary skill in the art.

Moreover, the Supreme Court has stated that a motivation to combine may be simply "common sense" and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420. Indeed, the Supreme Court held that it is sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421. Here, all the claim elements are common sense and are easily fit together by one of ordinary skill in the art.

While not necessary, a motivation to combine may also be found in the references themselves. One of skill in the art would have been motivated to combine a reference that refers to, or otherwise explicitly invites combination with, another reference. Where the references cited herein have such an explicit invitation to combine, that invitation would have motivated one of skill in the art to combine any such references.

Micron hereby identifies the following ’291 Patent Primary References: Costa2, Lee 746, Seo3, and Micron 110 Series Products.

The below provides several exemplary combinations and motivations for combining a ’291 Patent Primary Reference with another reference.

a. Multideck Three Dimensional Structures

The Asserted Claims of the ’291 Patent recite two stacked layers of alternating material (i.e., “oxide/nitride layer pairs,” claims 2, 16) disposed one on the other. Usage of such structures was routine in the prior art and well understood by a POSA by the time of the filing of the ’291 Patent. *See, e.g.*, Costa2, [0002] (“The present disclosure relates generally to the field of three-dimensional memory devices and specifically to multi-tier three-dimensional memory devices containing dummy memory cells for providing inter-tier connection and methods of making the same.”); Lee 746, [0002] (“Electronic products are becoming increasingly smaller while requiring high-capacity data processing. Accordingly, it is necessary to reduce the volume of memory chips used in such electronic products while increasing their density. In this regard, nonvolatile memory devices having a tertiary structure that stack memory cells vertically on a substrate instead of a conventional flat structure are being considered for such a highly integrated memorial chip.”); Seo3, 1:20-25 (“A three-dimensional integrated circuit (3D-IC) memory technique includes various techniques for three-dimensionally arranging memory cells to achieve an increase in memory capacity. The memory capacity may be increased by a fine pattern technique and a multi-level cell (MLC) technique as well as the 3D-IC memory technique.”); Yang4 at 4:39-44 (“As illustrated in FIGS. 4A and 4B, the semiconductor device may include a second stacked structure ST2, a first stacked structure ST1 disposed on the second stacked structure ST2, and a connection pattern 16 disposed between the first stacked structure ST1 and the second stacked structure ST2.”); Liu4, 1:50-54 (“a monolithic three-dimensional memory device is provided, which comprises: a first tier structure located over a top surface of a substrate and comprising a first alternating stack of first insulating layers and first electrically conductive layers; an insulating cap layer overlying the first tier structure; a second tier structure located over the insulating cap layer and comprising a second alternating stack of second insulating layers and second electrically conductive layers”); Jang2,

1:67-2:3 ("Additionally, a second plurality of first insulation layers and first sacrificial layers may be formed alternately and repeatedly on an uppermost one of the second insulation layer and the second sacrificial layer."); Nishikawa4, Abstract ("The resistor may be provided in a peripheral area of a 3D memory device which has a two-tier or other multi-tier stack of memory cells."). The prior art cited in this paragraph, and the prior art for which the corresponding claim charts provide teachings of multideck three-dimensional memory structures will be referred to as "Multideck Structure Art."

To the extent any of the '291 Patent Primary References are argued or shown not to include multideck three-dimensional memory structures in the manner claimed in the '291 Patent, a POSA would have been motivated to combine the reference with any one, or several, of the Multideck Structure Art.

Furthermore, a POSA would have had a reasonable expectation of success in combining the teachings of the Multideck Structure Art with other teachings because these references describe the use of well-known and well understood semiconductor manufacturing techniques applied in the context of three-dimensional multideck memory devices. *E.g.*, Costa2, [0137] ("The first-tier memory openings 149 and the first-tier support openings 119 can be formed concurrently by a patterning process. To form the first-tier openings (149, 119), a lithographic material stack (not shown) including at least a photoresist layer can be formed over the first tier structure (132, 142, 172, 165), and can be lithographically patterned to form openings within the lithographic material stack. The pattern in the lithographic material stack can be transferred through the entirety of the first tier structure (132, 142, 172, 165) by at least one anisotropic etch that employs the patterned lithographic material stack as an etch mask. Portions of the first tier structure (132, 142, 172, 165) underlying the openings in the patterned lithographic material stack are etched to form the first-tier openings (149, 119)."); Lee 746, [0062] ("The number of first through-holes (120a) may be appropriately selected and does not limit the scope of this embodiment. For example, photo lithography techniques may be used to form a photoresist mask (not shown), and the first through holes (120a) may be formed by etching the first insulating layer (110a) and the first conductive layer (115a) with the mask as a protective film."); Seo3, 7:19-20 ("The first preliminary stack

structure 10 is patterned to form a first active hole H1 exposing the substrate 1."); Liu4, 7:14-18 ("The separate etching of memory opening portions in each portion of the stack may be conducted with separate hard masks. Thus, each hard mask used during each etching step may be relatively thin and the hard mask thickness does not limit the total number of memory layers in the stack."); Jang2, 12:26-28 ("The planarization process may be performed by a chemical mechanical polishing (CMP) process and/or an etch back process."). A POSA would have been well acquainted with and well understood the application of such techniques as taught in the Multideck Structure Art in the context of multideck three-dimensional memory device manufacturing.

b. Continuous Vertical Channel

The Asserted Claims of the '291 Patent recite "[forming] a third channel structure … [above/disposed over] the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate," "[forming] a second through hole …, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate," and "[forming] a fifth channel structure … [above/disposed over] the second through hole." '291 Patent, claims 1, 11, 20. These claims all relate to one of the stated challenges the '291 Patent sought to overcome: "[a]s semiconductor technology advances, three-dimensional (3D) memory devices, such as 3D NAND memory devices, keep scaling more oxide/nitride (ON) layers. As such, it becomes difficult to use a single etching process to form the channel holes in the 3D memory devices that have a substantial depth. As the channel hole aspect ratio increases, channel hole etching becomes exponentially slower. Further, the process capability control of the formed channel holes, including bow-free, straight profile, critical dimension (CD) uniformity, minimal twisting, etc., tend to be more challenging. Thus, a single etching method may not be efficient in both cost and process capability." '291 Patent at 1:24-35. In effect, to overcome such difficulties, a multi-deck process is utilized where each tier's channel hole overlaps with the one below to form a single, continuous vertical channel.

Difficulties in manufacturing three-dimensional devices with increasing numbers of oxide/nitride layers were well-known in the art. *E.g.*, Lee 746, [0003] ("as the number of stacks of

memory cells in nonvolatile memory devices having a tertiary structure increase, the aspect ratio increases, making the manufacturing process difficult."); Costa2, [0003] ("Some of the challenges for fabricating a multi-tier memory stack structure include formation of memory openings having high aspect ratios and alleviation of effects of misalignment of tier-level memory openings formed in different tier structures. Thus, methods are desired for providing a reliable connection between vertically neighboring memory stack structures."); Seo3, 1:25-27 ("the fine pattern technique may be expensive and the MLC technique may be limited to the number of bits per cell"); Yang4, 1:33-34 ("However, as the height of the stacked structure increases, difficulties in performing an etch process may increase."); Liu4, Abstract ("Alignment between memory openings through multiple tier structures can be facilitated employing a temporary landing pad."), 7:23-35 ("However, because the different portions of the memory openings are etched during different etching steps using different lithography steps and different hard mask layers, it may be difficult to align the different portions of each memory opening (i.e., lower portion, upper portion and optionally one or more middle portions) to form a continuous memory opening through the entire stack due to photolithography misalignment issues, especially if each memory opening has more than two portions (i.e., the stack is etched three or more times to form a memory opening). The misalignment of the memory opening portions may lead to channel discontinuity which results in an open NAND string."); Jang2, 1:30-32 ("Due to the high aspect ratio of the hole, exposing the top surface of the substrate is not easy, and the channel may not be electrically connected to the substrate."). The prior art cited in this paragraph, and the prior art for which the corresponding claim charts provide teachings of techniques to form a continuous vertical channel in three-dimensional multideck memory devices will be referred to as "Continuous Vertical Channel Art."

To the extent any of the '291 Patent Primary References are argued or shown to not disclose overlapping structures to form a continuous vertical channel, a POSA would have been motivated to combine the reference with any one, or several of, the Continuous Vertical Channel Art references.

For example, a POSA would have been motivated and considered it obvious to use an inter-tier channel structure of a size (in the horizontal direction, for example, aperture) that is at least

equal to, if not greater than, the size of the underlying channel hole to overcome the above-described manufacturing challenges and ensure a continuous vertical channel. *See, e.g.*, Lee 746, [0023] ("The lateral extension portion (135) may have a larger cross-sectional area than the first and second semiconductor pillars (130a, 130b) based on a cross-section parallel to the substrate (105). For example, the lateral extension portion (135) may substantially cover the entire upper surface of the first semiconductor pillar (130a) and may extend laterally."); Costa2, [00164] ("Each first joint-level doped semiconductor portion 173 covers and protects the underlying first vertical semiconductor channel 61 from oxidation during a subsequent oxidation process."), [0265] ("Referring to FIG. 20B, a photoresist layer 147 can be applied over the joint-level doped semiconductor layer 173L and lithographically patterned to cover each of the first memory opening fill structures 57…. Each joint-level doped semiconductor portion 173 covers and protects the underlying first vertical semiconductor channel 61 from oxidation during a subsequent oxidation process. In one embodiment, the bottom surface of each joint-level doped semiconductor portion 173 can contact an entire top surface of an underlying first memory opening fill structure 57."); Yang4, 4:63-5:3 ("The connection pattern 16 may be interposed between the first stacked structure ST1 and the second stacked structure ST2, and connect each of the upper first semiconductor patterns 13 to each of the lower second semiconductor patterns 23. Here, since the connection pattern 16 is formed as a part of a channel layer, the connection pattern 16 may have an island shape so as to connect one of the first semiconductor patterns 13 to one of the second semiconductor patterns 23."), Fig. 4B; Seo3, 11:47-50 ("Referring to FIG. 25, a second preliminary stack structure 20 is formed on the first sub-stack structure ST1. The second preliminary stack structure 20 is patterned to form a second active hole H2 exposing the first active pad 54."), Fig. 25; Liu4, 11:1-6 ("The landing pad 25 may extend horizontally beyond the memory hole 84 diameter or width to be located over and under adjacent control gates 3 inside the dielectric fill material 121[.] Thus, the landing pad 25 may extend into the insulating layer 121 between the first 3 a and the second 3 b control gate electrodes 3. The fill material 121 isolates the landing pad 25 from direct contact with the control gate electrodes 3."), Fig. 2A.

Furthermore, a POSA would have also had a reasonable expectation of success in

combining the teachings of the Continuous Vertical Channel Art with other teachings because it was well understood that failure to correct a misalignment (and construct a continuous vertical channel) would "result in an open NAND string." Liu4, 7:34-35; *see also, e.g.*, Costa2, [0164] (noting doped semiconductor portion 173 must have a larger diameter "than that of the first memory cavity 149' … to account for misalignment of the layers"); Nishikawa4, [0109] ("Step 915 includes forming a widened area at the top of the vertical holes in the first dielectric peripheral area. This provides a larger area for the overlaying vertical holes to make contact, to allow for some misalignment."). Thus, a POSA would have been well acquainted with and well understood how to apply the techniques as taught in the Continuous Vertical Channel Art to other teachings in three-dimensional memory devices.

c. Groove and Planarizing Top Surface Limitations

Claims 6, 7, and 10 relate to forming a groove, forming a material therein, and planarizing the top surface to form an interface between the channel structures or between the top channel structure and a higher-level interconnect. It would have been obvious to implement such grooves and planarization with any of the '291 Patent Primary References for the following reasons, e.g., in view of the below prior art.

To start, the groove, deposition, and planarization to form such an interface was well. For example, Yong 308 discloses forming a channel hole, insulating layer 76, etching a large groove, and forming a large interface between two channel structures. Yong 308, Figs. 7A-7F, [0076]-[0091]. By way of another example, Yoshiaka 846 discloses the same process by for an upper-level interface. Yoshiaka 846, Figs. 5A-B, [0027], [0070]-[0077], [0096]-[0099] (see interface through layers 40, 65, 66). By way of another example, Hiroyasu 339 discloses the same. Hiroyasu 339, Figs. 9A-9D, [0028]-[0030] (see interfaces to channel structures). By way of another example, Sung 296 discloses the same. Sung 296, Fig. 1B, [0027]-[0033] (see interfaces to substrate and above channel). *See also* Tanaka [0027], [0028], [0030], [0064], [0068]-[0070], Figs. 9A-D, 17A-D; Yoon, [0027], [0029]-[0033], [0035]-[0036], [0040]-[0041], Fig. 1B, 1F; Koshiishi, [0048], [0050]-[0052], [0056], Figs. 4A-C, 5A-C (discussing planarization of joint materials); Tokuhira [0011], [0050]-[0056], [0058]-[0059], [0064], Figs. 4D, 6C; Zhu Fig. 2

(conductor 124, insulator 160-A, insulator 160-B); KR 250 Figs. 1-24; Lee 575 2:1-7:64, Figs. 1-4; Liu4, Figs. 26-27, 36:29-37:4. Collectively, this art is "Groove and Planarization Art."

To the extent any of the '291 Patent Primary References are argued or shown to not disclose overlapping structures to form a continuous vertical channel, a POSA would have been motivated to combine the reference with any one, or several of, the Continuous Vertical Channel Art references.

For example, a POSA would have been motivated and considered it obvious to use an inter-tier channel structure of a size (in the horizontal direction, for example, aperture) that is at least equal to, if not

d. Mask Layers

Claim 8 recites forming mask layers before forming the channel holes. It would have been obvious to employ such masks with any of the '291 Patent Primary References for the following reasons. Note that it would have been understood that the '291 Patent Primary References do employ such masks for the following reasons as well, e.g., in view of the below art.

To start, the use of masks was a basic semiconductor technique to form holes selectively, that is, form holes in a given pattern. The mask protects the layers from unintentional etching, that is, the mask defines the pattern of holes to etch and protects the other areas of the layers. *See* Costa2, [0120], [0135] (for first holes), [0165] (photoresist masks), [0171] (mask with anisotropic etch), [0191] (first tier holes), [0192] (second tier holes); Micheloni 2016, 68 (standard lithographic mask steps for NAND); Nishikawa4, [0109] (masking to etch holes), [0118]-[0120] (masking to protect and crate holes). Collectively, this art is "Mask Art."

To the extent any of the '291 Patent Primary References are argued or shown to not to disclose claims 8, a POSITA would have been motivated to combine the reference with any one, or several of, the Mask Art.

For example, a POSITA would have been motivated and considered it obvious to use a mask because it protects the non-target areas. Nishikawa4, [0118]-[0120] (masking to protect and crate holes). In addition, the mask defines the hole pattern to mask, thereby defining, for

example, the pattern of channel holes. *See* Costa2, [0120], [0135] (for first holes), [0191] (first tier holes), [0192] (second tier holes); Nishikawa4, [0109] (masking to etch holes). Of course, as these references demonstrate, it was necessary to remove the mask after etching the holes, thereby leaving a planar surface for further fabrication. *Id.*

A POSITA would have had a high expectation of success. Indeed, it was known to use mask as necessary when etching holes. Costa2, [0120] (may use as necessary). Further, the material therefore, e.g., photoresist, were well known. *Id.*, [0165] (photoresist masks). The masks were known compatible with etches, e.g., anisotropic etches. *Id.*, [0171] (mask with anisotropic etch). As such, masks were inherently part of any NAND fabrication. Micheloni 2016, 68 (standard lithographic mask steps for NAND). And masks increase the likelihood of success of any device by providing a protective function. Nishikawa4, [0118]-[0120] (masking to protect and crate holes).

e. Filling Structure, Interconnected Holes, and Non-Interconnected Holes

Various claims recite "filing structure." *See* Claims 1, 5, 8, 9, 12, and 13. Further, various claims recite whether the holes are interconnected or non-interconnected. *See* Claims 12-13. It would have been obvious to employ such filling structures, and either connect or not the sub-channel holes, with any of the '291 Patent Primary References for the following reasons, e.g., in view of the below prior art.

To start, the use of a filing structure was well known, and simply provide a stable channel structure. The channel, e.g., semiconductor film, is thin layer (as well as the other memory layers). As a result, the core would be a void without a filling structure. The filling structure provide a stable channel structure. Costa2, [0158] (core layer), Lu2, [0030] ("Oxide 252 can help with the performance characteristics of the hollow channel.") (Fig. 2C ("oxide 252"). Further, whether one connects the channel holes is merely a design choice, wherein connecting the holes can enable an etch through the holes. Nishikawa4, Fig. 18. Another design choice is to employ a plug between the holes. Costa2, Figs. 11A-B. Collectively, this art is "Filling Structure and Connection Art."

To the extent any of the ’291 Patent Primary References are argued or shown to not to disclose claims any of the above claims, a POSITA would have been motivated to combine the reference with any one, or several of, the Filling Structure and Connection Art.

For example, a POSITA would have been motivated and considered it obvious to use a filling structure because it provides support and improve the channel structure. Costa2, [0158] (core layer), Lu2, [0030] (“Oxide 252 can help with the performance characteristics of the hollow channel.”). And whether connecting the holes or not, the two sub-channel must electrically couple. As a result, it was obvious to use a plug or directly connect the holes (thereby interconnecting the sub-channel semiconductor films). *Compare* Nishikawa4, Fig. 18 *with* Costa2, Figs. 11A-B. Moreover, a POSITA would have been motivated and considered it obvious to use well-known deposition and processing steps to form the filling structures as claimed by the ’291 Patent (*see* claim 9). For example, Costa teaches that semiconductor channel layers can be deposited in the memory cavity, followed by depositing a dielectric core—certain portions of these layers can then be removed by well-known techniques (such as etching). *See* Costa [0275], Figs. 21C-D.

A POSITA would have had a high expectation of success. A filling structure simply involve deposition of, for example, an oxide. Costa2, [0158] (core layer), Lu2, [0030] (“Oxide 252 can help with the performance characteristics of the hollow channel.”) (Fig. 2C (“oxide 252”). Similarly, connecting the holes or not merely involves an etch and an optional plug. *Compare* Nishikawa4, Fig. 18 *with* Costa2, Figs. 11A-B. And depositing a thin layer of material followed by planarization or etching to remove portions of that material was well-known and commonly used. Costa2, [0275], Figs. 21C-D, [0257]. Such techniques were textbook material.

f. Plurality of Through Array Contact Barriers in a Third Region of the 3D Memory

Claim 20 recites, in effect, peripheral contacts in the peripheral. It would have been obvious to employ a peripheral region with such contacts with any of the ’291 Patent Primary References for the following reasons, e.g., in view of the below art.

To start, the use of a peripheral region was well known. Toyama, Fig. 73A (peripheral region); Nishikawa3, Fig. 1 (peripheral region 200); Nishikawa4, Fig. 10 (peripheral region 1000p). Memories require supporting logic, e.g., a state machine. This supporting logic became known as a peripheral region. In 3D memories, the peripheral region requires peripheral contacts to interconnect higher-level devices with peripheral logic on the substate. *Id.* Collectively, this art is "Peripheral Contacts Art."

To the extent any of the '291 Patent Primary References are argued or shown to not to disclose claim 20, a POSITA would have been motivated to combine the reference with any one, or several of, the Peripheral Contacts Art.

For example, a POSITA would have been motivated and considered it obvious to use a peripheral region, because this provides the region for the peripheral logic. Toyama, Fig. 73A (peripheral region); Nishikawa3, Fig. 1 (peripheral region 200); Nishiakwa4 (peripheral region 1000p). Further, this enables connecting upper-level devices with transistors on the substrate. *Id.*

A POSITA would have had a high expectation of success. Contacts were textbook material for many decades before the filing of the '291 Patent. So, too, were peripheral transistors. The basic steps merely involve masking, etching, and depositing a liner and/or a metal core. *Id.*

g. Forming Active Memory Cells Strings

Claim 1 of the '291 Patent requires the formation of a "first functional layer." This layer, in the context of the '291 Patent, is a portion of an active memory cell string. Claim 4 identifies the specific layers that comprise the first functional layer: a tunneling layer, a storage layer, a barrier layer, and a passivation layer. Such structures are well-known in the art and expected. *See* e.g., Lee 746 [0063]-[0066], Fig. 6A; Lee 896 17:9-3; Jang 14:61-65, Fig. 13. As another example, Costa discloses forming a "first tunneling dielectric layer 156 [that] includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions." Costa, [0151], Fig. 4C. A POSITA would have well understood the tunneling dielectric layer 156 described in Costa to be a tunneling layer.

Costa further discloses "[t]he first charge storage layer 154 can comprise a charge trapping material or a floating gate material." Costa, [0154]. First charge storage layer 154 is described as performing the same functions and comprising the same materials as the claimed first storage layer as described in the '291 Patent. Costa, [0148] ("first charge storage layer 154 can be a continuous layer or patterned discrete portions of a charge trapping material including a dielectric charge trapping material, which can be, for example, silicon nitride [or, a]lteratively … a continuous layer or patterned discrete portions of a conductive material such as doped polysilicon or a metallic material…. In one embodiment, the first charge storage layer 154 includes a silicon nitride layer.")

Costa further discloses, "[t]he first blocking dielectric layer 152 can include a single dielectric material layer or a stack of a plurality of dielectric material layers." Costa, [0145]. According to Costa, "first blocking dielectric layer 152 can a dielectric metal oxide having a dielectric constant greater than 7.9." *Id.*

Costa further discloses a first passivation layer (optional "first outer semiconductor channel layer 611") to protect the first barrier layer ("first blocking dielectric layer 152") from being damaged in a subsequent removal process. According to Costa, "optional first outer semiconductor channel layer 611 includes … semiconductor materials known in the art." Costa, [0152]. After this layer is deposited, a subsequent etching process removes portions of it and the other layers of the first functional layer. Thus, given the optional nature of layer 611, and the subsequent etching process, a POSITA would understand it to have at least the implicit purpose of protecting the underlying layers—including first blocking dielectric layer 152—from follow-on processes.

Costa further discloses after the first tunneling dielectric layer 156, the first charge storage layer 154, the first blocking dielectric layer 152, and the first outer semiconductor channel layer 611 are deposited in first-tier memory opening 149, a subsequent etching process removes the "portions … located above the top surface of the first-tier insulting cap layer 172 [and] the horizontal portions … at the bottom of each first memory cavity 149'…." Costa, [0153], Fig. 4D.

Claim 5 further requires: forming a second channel layer, forming a filling that that covers the second channel layer, removing portions of the second channel layer and the filing layer. Like the structure of claim 4, these structures and process are well-known in the art and expected. See e.g., Lee 746 [0066], [0073], Fig. 6A, 9; Lee 896 17:9-32, Fig. 23; Jang 14:61-65, Fig. 13; Liu 37:1-38:2, Fig. 27.

Thus, at the time of the invention it would have been obvious and a person of skill would have been motivated to form active memory cells strings in the manner claimed in claims 4 and 5, e.g., in view of the above art, as such was well-known and expected and could have been accomplished with a high degree of success.

h. Thickness Limitations

Claim 18 of the '291 Patent recite that "a thickness of the third channel structure is in a range between 30 nm and 70 nm." It would have been obvious to utilize such thicknesses with any of the '291 Patent Primary References for the following reasons.

Such ranges of thicknesses of material layers were common in the art. *See, e.g.*, Costa, [0163] ("The thickness of the first joint-level doped semiconductor layer 173L can be in a range from 20 nm to 100 nm…."), [0133] ("The thicknesses of the first insulating layers 132 and the first sacrificial material layers 142 can be in a range from 20 nm to 50 nm"); Liu4, 37:19-22 ("In one embodiment, the recess depth can be in a range from 10 nm to 300 nm, although lesser and greater recess depths can also be employed."), 8:28-31 (discussing resistance of landing pad with 30 nm thickness). Collectively, this art is "Material Thickness Art."

To the extent any of the '291 Patent Primary References are argued or shown to not to disclose claim 18, a POSITA would have been motivated to combine the reference with any one, or several of, the Material Thickness Art.

For example, a POSITA would have been motivated and considered it obvious to use an inter-tier material layer thickness in the range of 30 nm to 70 nm at least to reduce follow-on processing steps (e.g., excessive planarization or etching) to reduce the inter-tier material's thickness. And maintaining consistent—and minimized—inter-tier material thickness would aid in other processing steps, such as forming peripheral contacts (see above).

A POSITA would have had a high expectation of success. As discussed above, such material thicknesses were well-known and widely used.

B. Invalidity Based on Section 112 (Patent L.R. 3-3(d))

1. Indefiniteness

Defendants provide the following grounds for invalidity under 35 U.S.C. § 112. Defendants' investigation of the Asserted Patents is ongoing, and Defendants reserve the right to amend or supplement these disclosures based on further investigation and in a manner consistent with the Federal Rules of Civil Procedure, the Local Patent Rules for the Northern District of California, and the Docket Control Order, or otherwise in accordance with any order or direction of this Court or agreement of the parties. Further, Plaintiff's Infringement Contentions fail to provide sufficient detail to fully understand its proposed application of the Asserted Claims, and Defendants reserve the right to assert additional grounds for invalidity under 35 U.S.C. § 112 in response to Plaintiff's claim interpretations. Defendants also reserve the right to supplement, modify, or otherwise amend these grounds for invalidity under 35 U.S.C. § 112 based on the Court's claim construction rulings or opinions or the parties' positions or arguments taken in connection with the claim construction process.

2. Written Description and Enablement

The specification of the '291 Patent does not provide adequate written description to support the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims. 35 U.S.C. § 112(a) requires that a patent specification contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharm., Inc.*, 598 F.3d at 1351 (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ.*, 541 F.3d at 1122 (quoting *Vas-Cath Inc.*, 935 F.2d at 1563–64). The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Additionally, the Asserted Patents do not enable the claim scopes contained in Plaintiff's Infringement Contentions. Section 112(a) requires a specification to describe "the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention]." The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This "requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp.*, 344 F.3d at 1244 (citation omitted); *see Wyeth & Cordis Corp.*, 720 F.3d at 1385–86. The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Defendants provide below an identification of terms in Asserted Claims that render the Asserted Claims, at least as apparently construed by Plaintiff in its Infringement Contentions as discussed above, invalid pursuant to 35 U.S.C. § 112 as not enabled or lacking sufficient written description:

- "planarizing the top surfaces of the first insulating connection layer and the third channel layer to form the third channel structure" (Claim 6)
- "planarizing the top surfaces of the first insulating connection layer and the third channel structure" (Claim 7)
- "forming a third channel structure in contact with the second channel structure above the first through hole" (Claim 1)
- "forming a fifth channel structure in contact with the fourth channel structure above the second through hole" (Claim 1)
- "a plurality of through array contact barriers in a third region of the 3D memory device" (claim 20)
- "wherein the first through hole is non-interconnected with the second through hole" (claim 12)
- "wherein the first through hole is interconnected with the second through hole" (claim 13)

VI. INVALIDITY OF THE ’532 PATENT

A. Invalidity Based on the Prior Art

As shown below, the alleged inventions of the ’532 Patent were well-known in the prior art. Those skilled in the art were aware of all of the limitations claimed in the ’532 Patent. Thus, many prior art patents, publications, products, and combinations thereof, disclose, teach, or embody every limitation of the Asserted Claims and thus invalidate those claims. Examples of these disclosures, teachings, and embodiments are identified in the following sections and in the attached claim charts.

1. Identification of Prior Art References (Patent L.R. 3-3(a))

Subject to the reservation of rights above, Defendants identify each item of prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the ’532 Patent. The patents/applications, publications, and systems identified are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations.

Some of the below citations and those in the corresponding invalidity claim charts involve prior art references that have corresponding related, foreign, and/or PCT counterpart publications. In such cases, where either the U.S. patent or related, foreign, and/or PCT counterpart is cited, it is to be understood that the corresponding disclosures from the counterpart patent and publications (which are substantively the same) are implicitly incorporated by reference in the alternative to avoid needless repetition.

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
L-01	U.S. 2018/0182771A1 (“Costa2”)	Feb. 28, 2017	June 28, 2017
L-02	KR 101487746 (“Lee 746”)	Feb. 7, 2014	Feb. 4, 2015
L-03	U.S. 9,768,018 (“Seo3”)	April 13, 2016	Sept. 19, 2017
L-04	U.S. 9,245,962 (“Yang4”)	Jan. 20, 2015	Jan. 26, 2016
L-05	U.S. 9,698,153 (“Liu4”)	March 24, 2016	July 4, 2017
L-06	U.S. 9,343,475 (“Jang2”)	Jan. 15, 2014	May 17, 2016
L-07	U.S. 2017/0162592A1 (“Nishikawa4”)	Dec. 4, 2015	June 8, 2017
L-08	U.S. 2017/0154892A1 (“Oh2”)	June 10, 2016	June 1, 2017
L-09	U.S. 2015/0279855A1 (“Lu2”)	March 27, 2014	Oct. 1, 2015

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
§VI.A.3.[11]	U.S. 20120126308A1 ("Yong 308")	Nov. 17, 2011	May 24, 2012
§VI.A.3.	U.S. 2016/0300846A1 ("Yoshiaka 846")	Mar. 13, 2015	Oct. 1, 2016
§VI.A.3.	U.S. 2010/0327339A1 ("Hiroyasu 339")	Jun. 24, 2009	Dec. 30, 2010
§VI.A.3.	U.S. 20150155296A1 ("Sung 296")	Dec. 3, 2013	Jun. 4, 2015
§VI.A.3.	U.S. 9,595,531 ("Zhu")	July 11, 2014	March 14, 2017
§VI.A.3.	KR1018075250 ("KR 250")	July 11, 2011	December 11, 2017
§VI.A.3.	U.S. 9,905,575 ("Lee 575")	June 7, 2016	February 27, 2018
§VI.A.3.	U.S. 9,536,896 ("Lee 896")	April 27, 2012	January 3, 2017
§VI.A.3.	US20170263614A1 ("Tokuhira")	March 11, 2016	September 14, 2017
§VI.A.3.	US20100327339A1 ("Tanaka")	June 24, 2019	December 30, 2010
§VI.A.3.	US20150270282A1 ("Koshiishi")	March 20, 2014	September 24, 2015
§VI.A.3.	US20150155296A1 ("Yoon")	December 3, 2013	June 4, 2015

Table L-1: Prior Art Patents and Patent Publications for the '532 Patent

Defendants are still investigating prior uses and sales. Based upon at least Plaintiff's apparent position as to the scope of the Asserted Claims, and as further explained below and in the cited exhibits, it appears that the following systems (and development thereof) qualify as prior art under at least one or more of 35 U.S.C. § 102(a):

Ex.	Description	Entities Involved	Prior Art Date
L-10	110 Series Products	Micron	8/10/2016

Table L-2: Prior Art Systems for the '532 Patent

Micron's 110 series products were publicly available, on sale, or in public use prior to the effective filing date of the '532 Patent. MYM0042611-MYM0042676, MYM0042896-MYM0042896, MYM0065110, MYM0065111.

Description	Availability
Travelers	to be made available via inspection
Process information	to be made available via inspection

[11] *See* §VI.A.3. The equivalent of a chart is set forth with pinpoint citations to the reference in the motivation to combine sections. The same is true for all references without an exhibit.

Description	Availability
Schematics	to be made available via inspection
Layouts	to be made available via inspection
Waveforms	MYM0042897-MYM0043247, MYM0069190-MYM0069236
TEM/SEM Imagery	MYM0043255-MYM0043296, MYM0043316-MYM0043339, MYM0043423-MYM0043424, MYM0043248-MYM0043254, MYM0058880-MYM0058891, MYM0069181-MYM0069181
Datasheets	MYM0043425-MYM0043844, MYM0065164-MYM0066151
Trim Spreadsheets	MYM0065112-MYM0065115, MYM0069182-MYM0069189, MYM0069715-MYM0069940

Table L-3: Listing of Prior Art Systems Documentation for the '532 Patent

2. Anticipation and Obviousness (Patent L.R. 3-3(b) and (c))

The Asserted Claims of the '532 Patent are invalid because they are anticipated by the prior art and/or because they would have been obvious in view of the prior art.

The prior art identified by Defendants anticipates and/or renders obvious one or more of the Asserted Claims of the '532 Patent under at least AIA §§ 102(a)(1), 102(a)(2), and 103. For each prior art reference, Defendants have provided claim charts attached to these Invalidity Contentions

as Exhibits L-1 through L-10. These charts identify where each element of each Asserted Claim can be found in each item of prior art.

Again, to the extent not anticipated, the Asserted Claims of the '532 Patent are invalid as obvious under 35 U.S.C. § 103. Each prior art reference identified in the preceding sections—either alone or in combination with another prior art reference and/or in combination with the knowledge of one skilled in the art—renders the Asserted Claims invalid as obvious. In rendering the Asserted Claims obvious, each prior art reference identified in the preceding sections may be combined with: (1) information known to persons skilled in the art at the time of the alleged invention, (2) any of the other anticipatory or obviousness prior art references, (3) any statements in the intrinsic record of the '532 Patent and related applications, or (4) any of the additional prior art identified below.

3. Motivations to Combine[12]

A person of ordinary skill in the art would have been motivated to combine the preceding references (*see* Section VI.A.1) for the following reasons. Teachings, suggestions, motivations and/or reasons to modify any of the references and/or to combine any two or more of the references can come from many sources, including the prior art (by specific reference and when read as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obviousness to try, the nature of the problem faced, and/or knowledge possessed by a person of ordinary skill.

Although a patent claim may be invalidated based on a teaching-suggestion-motivation ("TSM") rationale—*i.e.,* that some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention—the Supreme Court identified additional rationales in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007). The following of these rationales apply here:

(A) the asserted claims combine prior art elements according to known methods to yield predictable results;

[12] The statements in this section about what was known and obvious to a POSA are made with respect to the effective filing date of the '532 Patent.

(B) the asserted claims involve the simple substitution of one known element for another to obtain predictable results;

(C) the asserted claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;

(D) the asserted claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) the asserted claims involve combinations of prior art references that would have been "obvious to try"'—a person of ordinary skill in the art could have reached the asserted claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) the asserted claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach); *see also* Department of Commerce, Patent and Trademark Office, Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.,* 72 Fed. Reg. 57,526 (Oct. 10, 2007). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420-21.

Thus, even in the absence of a specific teaching, suggestion, or motivation to combine references, the Asserted Claims here are obvious and therefore invalid. Each of the cited references or devices is in the same field as the '532 Patent, making it obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. One of ordinary skill in the art would have recognized that improvements could be achieved by combining or modifying prior art references that described such improvements. Each of the above prior art references describes systems, products, or methods that were known to offer such improvements, and, accordingly, one of ordinary skill in the art would have been motivated to combine or modify the references as identified in each of the combinations below.

Furthermore, because each prior art reference concerns three-dimensional memory device designs, common industry knowledge supplied a reason to combine any one the above references. It was well understood that different three-dimensional memory structural features could be employed together or interchanged with each other, fitting together like puzzle pieces. Each combination would have produced predictable results and would simply represent a known alternative to one of ordinary skill in the art of memory devices (whether or not specifically related to three-dimensional memory devices). This is a further motivation to combine any of the above references.

The below sections further address particular reasons to combine the above references. The below should not be construed as an admission that there is any value to the alleged invention of the ’532 Patent. As discussed previously, these contentions are based in significant part on how Plaintiff is apparently construing the asserted claim in its Infringement Contentions, which is an incorrect and overbroad interpretation of the alleged invention of the ’532 Patent. Accordingly, to the extent the below refers to benefits of certain elements or industry trends towards these elements, this is not an admission that the alleged invention of the ’532 Patent provides any benefits: to the contrary, properly construed and compared to the prior art, the ’532 Patent provides no benefits. Likewise, to the extent the below refers to substituting elements, this is not an admission that the elements subject to the substitution are in any way similar, *e.g.,* perform the same function, in the same way, to achieve the same result.

The various elements of the Asserted Claims were well known in the prior art at the time of the alleged invention, and the combination would have been obvious to one of skill in the art. The combinations simply (a) combine prior art elements according to known methods to yield predictable results; (b) involve the simple substitution of one known element for another to obtain predictable results; (c) involve the use of a known technique to improve similar devices (methods, or products) in the same way; (d) apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) involves combinations of prior art references that would have been “obvious to try” – a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a

reasonable expectation of success; and/or (f) would have been prompted by known work, based on design incentives or other market forces, because such variations were predictable to one of ordinary skill in the art.

Moreover, the Supreme Court has stated that a motivation to combine may be simply "common sense" and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420. Indeed, the Supreme Court held that it is sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421. Here, all the claim elements are common sense and are easily fit together by one of ordinary skill in the art.

While not necessary, a motivation to combine may also be found in the references themselves. One of skill in the art would have been motivated to combine a reference that refers to, or otherwise explicitly invites combination with, another reference. Where the references cited herein have such an explicit invitation to combine, that invitation would have motivated one of skill in the art to combine any such references.

Micron hereby identifies the following '532 Patent Primary References: Costa2, Lee 746, Seo3, and Micron 110 Series Products.

The below provides several exemplary combinations and motivations for combining an '532 Patent Primary Reference with another reference.

a. Multideck Three Dimensional Structures

The Asserted Claims of the '532 Patent recite two stacked layers of alternating material (i.e., "oxide/nitride layer pairs," claims 2) disposed one on the other. Usage of such structures was routine in the prior art and well understood by a POSA by the time of the filing of the '532 Patent. *See, e.g.*, Costa2, [0002] ("The present disclosure relates generally to the field of three-dimensional memory devices and specifically to multi-tier three-dimensional memory devices containing dummy memory cells for providing inter-tier connection and methods of making the same."); Lee

746, [0002] ("Electronic products are becoming increasingly smaller while requiring high-capacity data processing. Accordingly, it is necessary to reduce the volume of memory chips used in such electronic products while increasing their density. In this regard, nonvolatile memory devices having a tertiary structure that stack memory cells vertically on a substrate instead of a conventional flat structure are being considered for such a highly integrated memorial chip."); Seo3, 1:20-25 ("A three-dimensional integrated circuit (3D-IC) memory technique includes various techniques for three-dimensionally arranging memory cells to achieve an increase in memory capacity. The memory capacity may be increased by a fine pattern technique and a multi-level cell (MLC) technique as well as the 3D-IC memory technique."); Yang4 at 4:39-44 ("As illustrated in FIGS. 4A and 4B, the semiconductor device may include a second stacked structure ST2, a first stacked structure ST1 disposed on the second stacked structure ST2, and a connection pattern 16 disposed between the first stacked structure ST1 and the second stacked structure ST2."); Liu4, 1:50-54 ("a monolithic three-dimensional memory device is provided, which comprises: a first tier structure located over a top surface of a substrate and comprising a first alternating stack of first insulating layers and first electrically conductive layers; an insulating cap layer overlying the first tier structure; a second tier structure located over the insulating cap layer and comprising a second alternating stack of second insulating layers and second electrically conductive layers"); Jang2, 1:67-2:3 ("Additionally, a second plurality of first insulation layers and first sacrificial layers may be formed alternately and repeatedly on an uppermost one of the second insulation layer and the second sacrificial layer."); Nishikawa4, Abstract ("The resistor may be provided in a peripheral area of a 3D memory device which has a two-tier or other multi-tier stack of memory cells."). The prior art cited in this paragraph, and the prior art for which the corresponding claim charts provide teachings of multideck three-dimensional memory structures will be referred to as "Multideck Structure Art."

To the extent any of the '532 Patent Primary References are argued or shown not to include multideck three-dimensional memory structures in the manner claimed in the '532 Patent, a POSA would have been motivated to combine the reference with any one, or several, of the Multideck Structure Art.

Furthermore, a POSA would have had a reasonable expectation of success in combining the teachings of the Multideck Structure Art with other teachings because these references describe the use of well-known and well understood semiconductor manufacturing techniques applied in the context of three-dimensional multideck memory devices. *E.g.*, Costa2, [0137] ("The first-tier memory openings 149 and the first-tier support openings 119 can be formed concurrently by a patterning process. To form the first-tier openings (149, 119), a lithographic material stack (not shown) including at least a photoresist layer can be formed over the first tier structure (132, 142, 172, 165), and can be lithographically patterned to form openings within the lithographic material stack. The pattern in the lithographic material stack can be transferred through the entirety of the first tier structure (132, 142, 172, 165) by at least one anisotropic etch that employs the patterned lithographic material stack as an etch mask. Portions of the first tier structure (132, 142, 172, 165) underlying the openings in the patterned lithographic material stack are etched to form the first-tier openings (149, 119)."); Lee 746, [0062] ("The number of first through-holes (120a) may be appropriately selected and does not limit the scope of this embodiment. For example, photo lithography techniques may be used to form a photoresist mask (not shown), and the first through holes (120a) may be formed by etching the first insulating layer (110a) and the first conductive layer (115a) with the mask as a protective film."); Seo3, 7:19-20 ("The first preliminary stack structure 10 is patterned to form a first active hole H1 exposing the substrate 1."); Liu4, 7:14-18 ("The separate etching of memory opening portions in each portion of the stack may be conducted with separate hard masks. Thus, each hard mask used during each etching step may be relatively thin and the hard mask thickness does not limit the total number of memory layers in the stack."); Jang2, 12:26-28 ("The planarization process may be performed by a chemical mechanical polishing (CMP) process and/or an etch back process."). A POSA would have been well acquainted with and well understood the application of such techniques as taught in the Multideck Structure Art in the context of multideck three-dimensional memory device manufacturing.

b. Continuous Vertical Channel

The Asserted Claims of the '532 Patent recite "forming a third channel structure above the first through hole…, wherein a projection of the third channel structure on the substrate covers a

projection of the first through hole on the substrate" and "forming a fifth channel structure above the second through hole." '532 Patent, claim 1; *see also* '532 Patent, claims 11, 18 (claiming "a third channel structure … disposed over the first through hole, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole" and "a fifth channel structure … disposed over the second through hole"). These claims all relate to one of the stated challenges the '532 Patent sought to overcome: "[a]s semiconductor technology advances, three-dimensional (3D) memory devices, such as 3D NAND memory devices, keep scaling more oxide/nitride (ON) layers. As such, it becomes difficult to use a single etching process to form the channel holes in the 3D memory devices that have a substantial depth. As the channel hole aspect ratio increases, channel hole etching becomes exponentially slower. Further, the process capability control of the formed channel holes, including bow-free, straight profile, critical dimension (CD) uniformity, minimal twisting, etc., tend to be more challenging. Thus, a single etching method may not be efficient in both cost and process capability." '532 Patent at 1:26-37. In effect, to overcome such difficulties, a multi-deck process is utilized where each tier's channel hole overlaps with the one below to form a single, continuous vertical channel.

Difficulties in manufacturing three-dimensional devices with increasing numbers of oxide/nitride layers were well-known in the art. *E.g.*, Lee 746, [0003] ("as the number of stacks of memory cells in nonvolatile memory devices having a tertiary structure increase, the aspect ratio increases, making the manufacturing process difficult."); Costa2, [0003] ("Some of the challenges for fabricating a multi-tier memory stack structure include formation of memory openings having high aspect ratios and alleviation of effects of misalignment of tier-level memory openings formed in different tier structures. Thus, methods are desired for providing a reliable connection between vertically neighboring memory stack structures."); Seo3, 1:25-27 ("the fine pattern technique may be expensive and the MLC technique may be limited to the number of bits per cell"); Yang4, 1:33-34 ("However, as the height of the stacked structure increases, difficulties in performing an etch process may increase."); Liu4, Abstract ("Alignment between memory openings through multiple tier structures can be facilitated employing a temporary landing pad."), 7:23-35 ("However, because the different portions of the memory openings are etched during different etching steps

using different lithography steps and different hard mask layers, it may be difficult to align the different portions of each memory opening (i.e., lower portion, upper portion and optionally one or more middle portions) to form a continuous memory opening through the entire stack due to photolithography misalignment issues, especially if each memory opening has more than two portions (i.e., the stack is etched three or more times to form a memory opening). The misalignment of the memory opening portions may lead to channel discontinuity which results in an open NAND string."); Jang2, 1:30-32 ("Due to the high aspect ratio of the hole, exposing the top surface of the substrate is not easy, and the channel may not be electrically connected to the substrate."). The prior art cited in this paragraph, and the prior art for which the corresponding claim charts provide teachings of techniques to form a continuous vertical channel in three-dimensional multideck memory devices will be referred to as "Continuous Vertical Channel Art."

To the extent any of the '532 Patent Primary References are argued or shown to not disclose overlapping structures to form a continuous vertical channel, a POSA would have been motivated to combine the reference with any one, or several of, the Continuous Vertical Channel Art references.

For example, a POSA would have been motivated and considered it obvious to use an inter-tier channel structure of a size (in the horizontal direction, for example, aperture) that is at least equal to, if not greater than, the size of the underlying channel hole to overcome the above-described manufacturing challenges and ensure a continuous vertical channel. *See, e.g.*, Lee 746, [0023] ("The lateral extension portion (135) may have a larger cross-sectional area than the first and second semiconductor pillars (130a, 130b) based on a cross-section parallel to the substrate (105). For example, the lateral extension portion (135) may substantially cover the entire upper surface of the first semiconductor pillar (130a) and may extend laterally."); Costa2, [00164] ("Each first joint-level doped semiconductor portion 173 covers and protects the underlying first vertical semiconductor channel 61 from oxidation during a subsequent oxidation process."), [0265] ("Referring to FIG. 20B, a photoresist layer 147 can be applied over the joint-level doped semiconductor layer 173L and lithographically patterned to cover each of the first memory opening fill structures 57…. Each joint-level doped semiconductor portion 173 covers and protects the

underlying first vertical semiconductor channel 61 from oxidation during a subsequent oxidation process. In one embodiment, the bottom surface of each joint-level doped semiconductor portion 173 can contact an entire top surface of an underlying first memory opening fill structure 57."); Yang4, 4:63-5:3 ("The connection pattern 16 may be interposed between the first stacked structure ST1 and the second stacked structure ST2, and connect each of the upper first semiconductor patterns 13 to each of the lower second semiconductor patterns 23. Here, since the connection pattern 16 is formed as a part of a channel layer, the connection pattern 16 may have an island shape so as to connect one of the first semiconductor patterns 13 to one of the second semiconductor patterns 23."), Fig. 4B; Seo3, 11:47-50 ("Referring to FIG. 25, a second preliminary stack structure 20 is formed on the first sub-stack structure ST1. The second preliminary stack structure 20 is patterned to form a second active hole H2 exposing the first active pad 54."), Fig. 25; Liu4, 11:1-6 ("The landing pad 25 may extend horizontally beyond the memory hole 84 diameter or width to be located over and under adjacent control gates 3 inside the dielectric fill material 121[.] Thus, the landing pad 25 may extend into the insulating layer 121 between the first 3 a and the second 3 b control gate electrodes 3. The fill material 121 isolates the landing pad 25 from direct contact with the control gate electrodes 3."), Fig. 2A.

Furthermore, a POSA would have also had a reasonable expectation of success in combining the teachings of the Continuous Vertical Channel Art with other teachings because it was well understood that failure to correct a misalignment (and construct a continuous vertical channel) would "result in an open NAND string." Liu4, 7:34-35; *see also, e.g.*, Costa2, [0164] (noting doped semiconductor portion 173 must have a larger diameter "than that of the first memory cavity 149' … to account for misalignment of the layers"); Nishikawa4, [0109] ("Step 915 includes forming a widened area at the top of the vertical holes in the first dielectric peripheral area. This provides a larger area for the overlaying vertical holes to make contact, to allow for some misalignment."). Thus, a POSA would have been well acquainted with and well understood how to apply the techniques as taught in the Continuous Vertical Channel Art to other teachings in three-dimensional memory devices.

c. Groove and Planarizing Top Surface Limitations

Claims 7-8 and 10 relate to forming a groove, forming a material therein, and planarizing the top surface to form an interface between the channel structures or between the top channel structure and a higher-level interconnect. It would have been obvious to implement such grooves and planarization with any of the '532 Patent Primary References for the following reasons.

To start, the groove, deposition, and planarization to form such an interface was well. For example, Yong 308 discloses forming a channel hole, insulating layer 76, etching a large groove, and forming a large interface between two channel structures. Yong 308, Figs. 7A-7F, [0076]-[0091]. By way of another example, Yoshiaka 846 discloses the same process by for an upper-level interface. Yoshiaka 846, Figs. 5A-B, [0027], [0070]-[0077], [0096]-[0099] (see interface through layers 40, 65, 66). By way of another example, Hiroyasu 339 discloses the same. Hiroyasu 339, Figs. 9A-9D, [0028]-[0030] (see interfaces to channel structures). By way of another example, Sung 296 discloses the same. Sung 296, Fig. 1B, [0027]-[0033] (see interfaces to substrate and above channel). *See also* Tanaka [0027], [0028], [0030], [0064], [0068]-[0070], Figs. 9A-D, 17A-D; Yoon, [0027], [0029]-[0033], [0035]-[0036], [0040]-[0041], Fig. 1B, 1F; Koshiishi, [0048], [0050]-[0052], [0056], Figs. 4A-C, 5A-C (discussing planarization of joint materials); Tokuhira [0011], [0050]-[0056], [0058]-[0059], [0064], Figs. 4D, 6C; Zhu Fig. 2 (conductor 124, insulator 160-A, insulator 160-B); KR 250 Figs. 1-24; Lee 575 2:1-7:64, Figs. 1-4; Liu4, Figs. 26-27, 36:29-37:4. Collectively, this art is "Groove and Planarization Art."

To the extent any of the '532 Patent Primary References are argued or shown to not claims 7-8 and/or 10, a POSA would have been motivated to combine the reference with any one, or several of, the Groove and Planarization Art references.

For example, a POSA would have been motivated and considered it obvious to use a grove to create a large contact portion to underlying channel structure. As the Groove and Planarization Art demonstrate, the channel structure will include a semiconductor layer, but that layer does not fill the entire core of the channel hole. As a result, the necessary area to contact is small. The Groove and Planarization Art beneficially provide a large contact interface by forming a grove, depositing an interface material therein, and then planarizing that material. The planarization is necessary in the context of 3D NAND, because each layer must be flat, otherwise

the entire structure will lose planarity at each level. Planar levers are particularly important for metallization.

A POSITA would have had a high expectation of success. As the Groove and Planarization Art demonstrate, the basic steps include an etch, deposition, and planarization. Such etches, e.g., anisotropic, depositions, e.g., CVD, and planarization, e.g., CMP, were all textbook material well before the filing of the ’532 Patent. The analysis of the ’254 and ’322 patent demonstrate this with citations materials relating to forming TACs, and that support equally applies here.

d. Filling Structure, Interconnected Holes, and Non-Interconnected Holes

Various claims recite “filing structure.” *See* Claims 6, 9, 13, and 14. Further, various claims recite whether the holes are interconnected or non-interconnected. *See* Claims 13, 14. It would have been obvious to employ such filling structures, and either connect or not the sub-channel holes, with any of the ’532 Patent Primary References for the following reasons.

To start, the use of a filing structure was well known, and simply provide a stable channel structure. The channel, e.g., semiconductor film, is thin layer (as well as the other memory layers). As a result, the core would be a void without a filling structure. The filling structure provide a stable channel structure. Costa2, [0158] (core layer), Lu2, [0030] (“Oxide 252 can help with the performance characteristics of the hollow channel.”) (Fig. 2C (“oxide 252”). Further, whether one connects the channel holes is merely a design choice, wherein connecting the holes can enable an etch through the holes. Nishikawa4, Fig. 18. Another design choice is to employ a plug between the holes. Costa2, Figs. 11A-B. Collectively, this art is “Filling Structure and Connection Art.”

To the extent any of the ’532 Patent Primary References are argued or shown to not to disclose claims any of the above claims, a POSITA would have been motivated to combine the reference with any one, or several of, the Filling Structure and Connection Art.

For example, a POSITA would have been motivated and considered it obvious to use a filling structure because it provides support and improve the channel structure. Costa2, [0158] (core layer), Lu2, [0030] (“Oxide 252 can help with the performance characteristics of the hollow

channel."). And whether connecting the holes or not, the two sub-channel must electrically couple. As a result, it was obvious to use a plug or directly connect the holes (thereby interconnecting the sub-channel semiconductor films). *Compare* Nishikawa4, Fig. 18 *with* Costa2, Figs. 11A-B. Moreover, a POSITA would have been motivated and considered it obvious to use well-known deposition and processing steps to form the filling structures as claimed by the '532 Patent (*see* claim 9). For example, Costa teaches that semiconductor channel layers can be deposited in the memory cavity, followed by depositing a dielectric core—certain portions of these layers can then be removed by well-known techniques (such as etching). *See* Costa [0275], Figs. 21C-D.

A POSITA would have had a high expectation of success. A filling structure simply involve deposition of, for example, an oxide. Costa2, [0158] (core layer), Lu2, [0030] ("Oxide 252 can help with the performance characteristics of the hollow channel.") (Fig. 2C ("oxide 252"). Similarly, connecting the holes or not merely involves an etch and an optional plug. *Compare* Nishikawa4, Fig. 18 *with* Costa2, Figs. 11A-B. And depositing a thin layer of material followed by planarization or etching to remove portions of that material was well-known and commonly used. Costa2, [0275], Figs. 21C-D, [0257]. Such techniques were textbook material.

e. Forming Active Memory Cells Strings

Claim 4 of the '532 Patent requires the formation of a "first functional layer." This layer, in the context of the '532 Patent, is a portion of an active memory cell string. Claim 5 identifies the specific layers that comprise the first functional layer: a tunneling layer, a storage layer, a barrier layer, and a passivation layer. Such structures are well-known in the art and expected. *See* e.g., Lee 746 [0063]-[0066], Fig. 6A; Lee 896 17:9-32, Fig. 23; Jang 14:61-65, Fig. 13. As another example, Costa discloses forming a "first tunneling dielectric layer 156 [that] includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions." Costa, [0151], Fig. 4C. A POSITA would have well understood the tunneling dielectric layer 156 described in Costa to be a tunneling layer.

Costa further discloses "[t]he first charge storage layer 154 can comprise a charge trapping material or a floating gate material." Costa, [0154]. First charge storage layer 154 is

described as performing the same functions and comprising the same materials as the claimed first storage layer as described in the '532 Patent. Costa, [0148] ("first charge storage layer 154 can be a continuous layer or patterned discrete portions of a charge trapping material including a dielectric charge trapping material, which can be, for example, silicon nitride [or, a]lteratively … a continuous layer or patterned discrete portions of a conductive material such as doped polysilicon or a metallic material…. In one embodiment, the first charge storage layer 154 includes a silicon nitride layer.")

Costa further discloses, "[t]he first blocking dielectric layer 152 can include a single dielectric material layer or a stack of a plurality of dielectric material layers." Costa, [0145]. According to Costa, "first blocking dielectric layer 152 can a dielectric metal oxide having a dielectric constant greater than 7.9." *Id.*

Costa further discloses a first passivation layer (optional "first outer semiconductor channel layer 611") to protect the first barrier layer ("first blocking dielectric layer 152") from being damaged in a subsequent removal process. According to Costa, "optional first outer semiconductor channel layer 611 includes … semiconductor materials known in the art." Costa, [0152]. After this layer is deposited, a subsequent etching process removes portions of it and the other layers of the first functional layer. Thus, given the optional nature of layer 611, and the subsequent etching process, a POSITA would understand it to have at least the implicit purpose of protecting the underlying layers—including first blocking dielectric layer 152—from follow-on processes.

Costa further discloses after the first tunneling dielectric layer 156, the first charge storage layer 154, the first blocking dielectric layer 152, and the first outer semiconductor channel layer 611 are deposited in first-tier memory opening 149, a subsequent etching process removes the "portions … located above the top surface of the first-tier insulting cap layer 172 [and] the horizontal portions … at the bottom of each first memory cavity 149'…." Costa, [0153], Fig. 4D.

Claim 6 further requires: forming a second channel layer, forming a filling that that covers the second channel layer, removing portions of the second channel layer and the filing layer. Like the structure of claim 4, these structures and process are well-known in the art and expected. *See*

e.g., Lee 746 [0066], [0073], Fig. 6A, 9; Lee 896 17:9-32, Fig. 23; Jang 14:61-65, Fig. 13; Liu 37:1-38:2, Fig. 27.

Thus, at the time of the invention it would have been obvious and a person of skill would have been motivated to form active memory cells strings in the manner claimed in claims 5 and 6 as such was well-known and expected and could have been accomplished with a high degree of success.

f. Thickness Limitations

Claims 16 and 20 of the '532 Patent recite that "a thickness of the third channel structure is in a range between 30 nm and 70 nm." It would have been obvious to utilize such thicknesses with any of the '532 Patent Primary References for the following reasons.

Such ranges of thicknesses of material layers were common in the art. *See, e.g.*, Costa, [0163] ("The thickness of the first joint-level doped semiconductor layer 173L can be in a range from 20 nm to 100 nm…."), [0133] ("The thicknesses of the first insulating layers 132 and the first sacrificial material layers 142 can be in a range from 20 nm to 50 nm"); Liu4, 37:19-22 ("In one embodiment, the recess depth can be in a range from 10 nm to 300 nm, although lesser and greater recess depths can also be employed."), 8:28-31 (discussing resistance of landing pad with 30 nm thickness). Collectively, this art is "Material Thickness Art."

To the extent any of the '532 Patent Primary References are argued or shown to not to disclose claims 16 and 18, a POSITA would have been motivated to combine the reference with any one, or several of, the Material Thickness Art.

For example, a POSITA would have been motivated and considered it obvious to use an inter-tier material layer thickness in the range of 30 nm to 70 nm at least to reduce follow-on processing steps (e.g., excessive planarization or etching) to reduce the inter-tier material's thickness. And maintaining consistent—and minimized—inter-tier material thickness would aid in other processing steps, such as forming peripheral contacts (see above).

A POSITA would have had a high expectation of success. As discussed above, such material thicknesses were well-known and widely used.

B. Invalidity Based on Section 112 (Patent L.R. 3-3(d))

1. Indefiniteness

Defendants provide the following grounds for invalidity under 35 U.S.C. § 112. Defendants' investigation of the Asserted Patents is ongoing, and Defendants reserve the right to amend or supplement these disclosures based on further investigation and in a manner consistent with the Federal Rules of Civil Procedure, the Local Patent Rules for the Northern District of California, and the Docket Control Order, or otherwise in accordance with any order or direction of this Court or agreement of the parties. Further, Plaintiff's Infringement Contentions fail to provide sufficient detail to fully understand its proposed application of the Asserted Claims, and Defendants reserve the right to assert additional grounds for invalidity under 35 U.S.C. § 112 in response to Plaintiff's claim interpretations. Defendants also reserve the right to supplement, modify, or otherwise amend these grounds for invalidity under 35 U.S.C. § 112 based on the Court's claim construction rulings or opinions or the parties' positions or arguments taken in connection with the claim construction process.

2. Written Description and Enablement

The specification of the '532 Patent does not provide adequate written description to support the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims. 35 U.S.C. § 112(a) requires that a patent specification contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharm., Inc.*, 598 F.3d at 1351 (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ.*, 541 F.3d at 1122 (quoting *Vas-Cath Inc.*, 935 F.2d at 1563–64). The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Additionally, the Asserted Patents do not enable the claim scopes contained in Plaintiff's Infringement Contentions. Section 112(a) requires a specification to describe "the manner and

process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention].” The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This “requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation.” *AK Steel Corp.*, 344 F.3d at 1244 (citation omitted); *see Wyeth & Cordis Corp.*, 720 F.3d at 1385–86. The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Defendants provide below an identification of terms in Asserted Claims that render the Asserted Claims, at least as apparently construed by Plaintiff in its Infringement Contentions as discussed above, invalid pursuant to 35 U.S.C. § 112 as not enabled or lacking sufficient written description:

- “forming a first insulating connection layer on the first stacked layer to cover the first through hole” (Claims 7, 8)
- “etching the first insulating connection layer to form a first groove to expose the first through hole” (Claim 7)
- “etching the first insulating connection layer and at least a portion of a top nitride layer of the first stacked layer to form a first groove to expose the first through hole” (Claim 8)
- “planarizing the top surfaces of the first insulating connection layer and the third channel layer to form the third channel structure” (Claim 7)
- “planarizing the top surfaces of the first insulating connection layer and the third channel structure” (Claim 8)
- “forming a third channel structure above the first through hole and in contact with the second channel structure” (Claim 1)
- “forming a fifth channel structure above the second through hole and in contact with the fourth channel structure” (Claim 1)
- “wherein the first through hole is non-interconnected with the second through hole”

(claim 13)

- "wherein the first through hole is interconnected with the second through hole" (claim 14)

VII. INVALIDITY OF THE '666 PATENT

A. Invalidity Based on the Prior Art

As shown below, the alleged inventions of the '666 Patent were well-known in the prior art. Those skilled in the art were aware of all of the limitations claimed in the '666 Patent. Thus, many prior art patents, publications, products, and combinations thereof, disclose, teach, or embody every limitation of the Asserted Claims and thus invalidate those claims. Examples of these disclosures, teachings, and embodiments are identified in the following sections and in the attached claim charts.

1. Identification of Prior Art References (Patent L.R. 3-3(a))

Subject to the reservation of rights above, Defendants identify each item of prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the '666 Patent. The patents/applications, publications, and systems identified are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations.

Some of the below citations and those in the corresponding invalidity claim charts involve prior art references that have corresponding related, foreign, and/or PCT counterpart publications. In such cases, where either the U.S. patent or related, foreign, and/or PCT counterpart is cited, it is to be understood that the corresponding disclosures from the counterpart patent and publications (which are substantively the same) are implicitly incorporated by reference in the alternative to avoid needless repetition.

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
M-1	U.S. 2018/0130701 A1 to Chun et al. ("Chun")	June 30, 2017	May 10, 2018
M-2	U.S. 2018/0053686 A1 to Hyun ("Hyun")	March 23, 2017	February 22, 2018
M-3	U.S. 10,229,929 to Kim et al. ("Kim5")	July 18, 2017	March 12, 2019
M-4	U.S. 2015/0255386 A1 to Lee et al. ("Lee 386")	March 4, 2015	September 10, 2015

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
M-5	U.S. 2014/0191389 A1 to Lee et al. ("Lee 389")	March 18, 2013	July 10, 2014
M-6	U.S. 2018/0261618 A1 to Lee et al. ("Lee 618")	October 2, 2017	March 9, 2017
M-7	U.S. 2018/0026046 A1 to Nam et al. ("Nam2")	December 12, 2016	January 15, 2018
M-8	U.S. 2017/0194255 A1 to Oh ("Oh1")	July 11, 2016	July 6, 2017
M-9	U.S. 2018/0166380 A1 to Park et al. ("Park6")	June 13, 2017	June 14, 2018
M-10	U.S. 9,941,153 to Yang ("Yang5")	December 22, 2016	April 10, 2018
M-11	U.S. 2015/0287710 A1 to Yun et al. ("Yun")	November 17, 2014	October 8, 2015
M-12	U.S. 2017/0271256 A1 to Inatsuka ("Inatsuka")	January 18, 2017	September 21, 2017

Table M-1: Prior Art Patents and Patent Publications for the '666 Patent

2. Anticipation and Obviousness (Patent L.R. 3-3(b) and (c))

The Asserted Claims of the '666 Patent are invalid because they are anticipated by the prior art and/or because they would have been obvious in view of the prior art.

The prior art identified by Defendants anticipates and/or renders obvious one or more of the Asserted Claims of the '666 Patent under at least AIA §§ 102(a)(1), 102(a)(2), and 103. For each prior art reference, Defendants have provided claim charts attached to these Invalidity Contentions as Exhibits M-1 through M-12. These charts identify where each element of each Asserted Claim can be found in each item of prior art. In addition to the above identified claims charts, Micron hereby incorporates by reference IPR2025-00189 filed with the United States Patent and Trademark Office on November 25, 2024.

Again, to the extent not anticipated, the Asserted Claims of the '666 Patent are invalid as obvious under 35 U.S.C. § 103. Each prior art reference identified in the preceding sections—either alone or in combination with another prior art reference and/or in combination with the knowledge of one skilled in the art—renders the Asserted Claims invalid as obvious. In rendering the Asserted Claims obvious, each prior art reference identified in the preceding sections may be combined with:

(1) information known to persons skilled in the art at the time of the alleged invention, (2) any of the other anticipatory or obviousness prior art references, (3) any statements in the intrinsic record of the '666 Patent and related applications, or (4) any of the additional prior art identified below.

3. Motivations to Combine[13]

A person of ordinary skill in the art would have been motivated to combine the preceding references (*see* Section VII.A.1) for the following reasons. Teachings, suggestions, motivations and/or reasons to modify any of the references and/or to combine any two or more of the references can come from many sources, including the prior art (by specific reference and when read as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obviousness to try, the nature of the problem faced, and/or knowledge possessed by a person of ordinary skill.

Although a patent claim may be invalidated based on a teaching-suggestion-motivation ("TSM") rationale—*i.e.,* that some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention—the Supreme Court identified additional rationales in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007). The following of these rationales apply here:

(A) the asserted claims combine prior art elements according to known methods to yield predictable results;

(B) the asserted claims involve the simple substitution of one known element for another to obtain predictable results;

(C) the asserted claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;

(D) the asserted claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) the asserted claims involve combinations of prior art references that would have been "obvious to try"'—a person of ordinary skill in the art could have reached the asserted claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

[13] The statements in this section about what was known and obvious to a POSA are made with respect to the effective filing date of the '666 Patent.

(F) the asserted claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach); *see also* Department of Commerce, Patent and Trademark Office, Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.,* 72 Fed. Reg. 57,526 (Oct. 10, 2007). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420-21.

Thus, even in the absence of a specific teaching, suggestion, or motivation to combine references, the Asserted Claims here are obvious and therefore invalid. Each of the cited references or devices is in the same field as the '666 Patent, making it obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. One of ordinary skill in the art would have recognized that improvements could be achieved by combining or modifying prior art references that described such improvements. Each of the above prior art references describes systems, products, or methods that were known to offer such improvements, and, accordingly, one of ordinary skill in the art would have been motivated to combine or modify the references as identified in each of the combinations below.

Furthermore, because each prior art reference concerns three-dimensional memory designs, and in particular three-dimensional memory designs that employs staircase structures with contact or landing pads, common industry knowledge supplied a reason to combine any one the above references. It was well understood that different three-dimensional memory structural features, including various different staircase and contact / landing pad features, sizes, and shapes, could be employed together or interchanged with each other, fitting together like puzzle pieces. Each combination would have produced predictable results and would simply represent a known alternative to one of ordinary skill in the art of three-dimensional memory. This is a further

motivation to combine any of the above references.

The below sections further address particular reasons to combine the above references. The below should not be construed as an admission that there is any value to the alleged invention of the '666 Patent. As discussed previously, these contentions are based in significant part on how Plaintiff is apparently construing the asserted claim in its Infringement Contentions, which is an incorrect and overbroad interpretation of the alleged invention of the '666 Patent. Accordingly, to the extent the below refers to benefits of certain elements or industry trends towards these elements, this is not an admission that the alleged invention of the '666 Patent provides any benefits: to the contrary, properly construed and compared to the prior art, the '666 Patent provides no benefits. Likewise, to the extent the below refers to substituting elements, this is not an admission that the elements subject to the substitution are in any way similar, *e.g.,* perform the same function, in the same way, to achieve the same result.

The various elements of the Asserted Claims were well known in the prior art at the time of the alleged invention, and the combination would have been obvious to one of skill in the art. The combinations simply (a) combine prior art elements according to known methods to yield predictable results; (b) involve the simple substitution of one known element for another to obtain predictable results; (c) involve the use of a known technique to improve similar devices (methods, or products) in the same way; (d) apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) involves combinations of prior art references that would have been "obvious to try" – a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and/or (f) would have been prompted by known work, based on design incentives or other market forces, because such variations were predictable to one of ordinary skill in the art.

Moreover, the Supreme Court has stated that a motivation to combine may be simply "common sense" and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420. Indeed, the Supreme Court held that it is

sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421. Here, all the claim elements are common sense and are easily fit together by one of ordinary skill in the art.

While not necessary, a motivation to combine may also be found in the references themselves. One of skill in the art would have been motivated to combine a reference that refers to, or otherwise explicitly invites combination with, another reference. Where the references cited herein have such an explicit invitation to combine, that invitation would have motivated one of skill in the art to combine any such references.

Micron hereby identifies the following '666 Patent Primary References: Chun, Hyun, Kim5, Lee 386, Lee 389 , Lee 618, Nam2, Oh1, Park6, Yang5, Yun, and Inatsuka.

The below provides several exemplary combinations and motivations for combining an '666 Patent Primary Reference with another reference.

a. Use of Contact or Landing Pads With "Curved" Side Surfaces

To the extent any '666 Patent Primary Reference is determined to be missing the claimed "second portion of the conductive layer comprises a curved side surface" required by claim 17 of the '666 Patent, a POSA would have considered it obvious and been motivated to form that reference's contact / landing pad such that it includes the type of "curved side surface" the claim requires, e.g., in view of the below art. At the time the '666 patent was filed, the prior art was replete with examples of "curved" contact or landing pads for use with memory devices that included a stepped structure. *See, e.g.,* Kim5, 8:29-34, Fig. 4B (referencing contact pad with "curved surface" or "cylindrical shape"); Lee 386, ¶ [0090] (noting that contact pad may be "cylindrical pillar"); Nam2, ¶¶ [0068], [0072], Fig. 8A (noting that contact pad can have "convex" or "bull nose shape"), Oh1, ¶ [0021], Fig. 31 (noting that pad sidewalls can be sloped), Park6, ¶¶ [0056] (noting that contact pad sides can be rounded), Yang5, 2:12-15 (noting that the pads can have a square, circular, rectangular, or bar shape), Yun, ¶ [0060], Figs. 5A-5F (noting that contact pads can have "rounded" surface). Given that the use of pads with rounded side surfaces was well-

known and routine in the prior art, a POSA would have considered use of such a structure with any of '666 Patent Primary References to constitute a routine, highly obvious design choice.

Further, it was also known that contact pads with curved or rounded sides are less likely to cause a "short circuit between … adjacent conductive layer patterns." *E.g.*, Park6 ¶¶ [0056], [0058]. This also would have motivated use of such a contact or landing pad shape with any of the '666 Patent Primary References. A POSA would have understood that by forming contact or landing pads with curved—as opposed to straight—side surfaces, the distance between the pads and adjacent conductive layers could be increased. This would have in turn reduced the possibility of short circuit resulting from, for example, manufacturing defects.

A POSA would also have had a reasonable expectation of success. Again, contact or landing pads with curved side surfaces were routinely used in three-dimensional memory devices with stepped structures. As this type of contact or landing pad had been shown to be successfully used in other devices, a POSA would have expected use of such a shape to also be successful in when employed in the '666 Patent Primary References.

b. Use of Insulating Layers With Various Physical Extents

To the extent any '666 Patent Primary Reference is determined to be missing the claimed contact or landing pad with a "side surface in contact with a side surface of the insulating layer" required by claim 17 of the '666 Patent, a POSA would have considered this obvious, e.g., in view of the below art. The prior art disclosed a range of different interlayer insulation physical extends. This included, for instance, interlayer insulation layers that extend out and around a stepped device's contact pads. *See, e.g.,* Yang5, Figs. 2, 4A-9B (showing various examples of insulating layers 114 extending out from stack and surrounding contact pads 120); Lee 389, Fig. 7A (showing insulating layers 22 surrounding contact pads on conductive layers 25), Inatsuka, Figs. 3, 14, 17 (showing insulating layers extending to contact structures). All of the '666 Patent Primary References teach memory devices with staircase structures including contact or landing pads on the staircase steps. Moreover, all of the '666 Patent Primary References surround those landing pads with insulation. While certain of the '666 Patent Primary References teach that that insulation is formed in a separate step from the layers insulation forming the staircase structure's alternating

stack of insulating and conductive layers, a POSA would have considered it obvious (and would have been motivated) to form the insulation in the stack and around the contact pad in a single step such that this layer constitutes a single, unified structure. A POSA would have considered this to be nothing more than a routine, obvious design choice. Moreover, given that the insulation surrounding the contact or landing pad was routinely formed from the same material as that in the stack (*see, e.g.,* Exs. M-1 through M-12), a POSA would have recognized that forming the layers of insulation during the same step would have simplified the process employed to manufacture the '666 Patent Primary References' devices. A POSA would also have had every reason to believe that the '666 Patent Primary References could be successfully modified in the manner discussed above. Again, it was known in the prior art that the same layer of insulation present in an alternating stack of conductive and insulating layers could also extend around a device's contact or landing pads. *See, e.g.,* Yang5, Figs. 2, 4A-9B; Lee 389, Fig. 7A; Inatsuka, Figs. 3, 14, 17.

B. Invalidity Based on Section 112 (Patent L.R. 3-3(d))

1. Indefiniteness

Defendants provide the following grounds for invalidity under 35 U.S.C. § 112. Defendants' investigation of the Asserted Patents is ongoing, and Defendants reserve the right to amend or supplement these disclosures based on further investigation and in a manner consistent with the Federal Rules of Civil Procedure, the Local Patent Rules for the Northern District of California, and the Docket Control Order, or otherwise in accordance with any order or direction of this Court or agreement of the parties. Further, Plaintiff's Infringement Contentions fail to provide sufficient detail to fully understand its proposed application of the Asserted Claims, and Defendants reserve the right to assert additional grounds for invalidity under 35 U.S.C. § 112 in response to Plaintiff's claim interpretations. Defendants also reserve the right to supplement, modify, or otherwise amend these grounds for invalidity under 35 U.S.C. § 112 based on the Court's claim construction rulings or opinions or the parties' positions or arguments taken in connection with the claim construction process.

2. Written Description and Enablement

The specification of the '666 Patent does not provide adequate written description to support

the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims. 35 U.S.C. § 112(a) requires that a patent specification contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharm., Inc.*, 598 F.3d at 1351 (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ.*, 541 F.3d at 1122 (quoting *Vas-Cath Inc.*, 935 F.2d at 1563–64). The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Additionally, the Asserted Patents do not enable the claim scopes contained in Plaintiff's Infringement Contentions. Section 112(a) requires a specification to describe "the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention]." The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This "requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp.*, 344 F.3d at 1244 (citation omitted); *see Wyeth & Cordis Corp.*, 720 F.3d at 1385–86. The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Defendants provide below an identification of terms in Asserted Claims that render the Asserted Claims, at least as apparently construed by Plaintiff in its Infringement Contentions as discussed above, invalid pursuant to 35 U.S.C. § 112 as not enabled or lacking sufficient written description:

- "a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer" (Claim 17)
- "wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer" (Claim 17)

VIII. INVALIDITY OF THE '604 PATENT

A. Invalidity Based on the Prior Art

As shown below, the alleged inventions of the '604 Patent were well-known in the prior art. Those skilled in the art were aware of all of the limitations claimed in the '604 Patent. Thus, many prior art patents, publications, products, and combinations thereof, disclose, teach, or embody every limitation of the Asserted Claims and thus invalidate those claims. Examples of these disclosures, teachings, and embodiments are identified in the following sections and in the attached claim charts.

1. Identification of Prior Art References (Patent L.R. 3-3(a))

Subject to the reservation of rights above, Defendants identify each item of prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the '604 Patent. The patents/applications, publications, and systems identified are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations.

Some of the below citations and those in the corresponding invalidity claim charts involve prior art references that have corresponding related, foreign, and/or PCT counterpart publications. In such cases, where either the U.S. patent or related, foreign, and/or PCT counterpart is cited, it is to be understood that the corresponding disclosures from the counterpart patent and publications (which are substantively the same) are implicitly incorporated by reference in the alternative to avoid needless repetition.

Exs.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
N-1 to N-5	U.S. 2017/0256551 ("Lee 551")	Mar. 2, 2016	Sep. 7, 2017
N-6 to N-10	U.S. 2016/0027793 ("Yip2")	Jul. 1, 2013	Jan. 28, 2016
N-1, N-6	U.S. 2019/0006275 ("Kobayashi")	Jun. 28, 2017	Jan. 3, 2019
N-2, N-7	U.S. 2016/0027730 ("Lee 730")	Jul. 28, 2014	Jan. 28, 2016
N-3, N-8	U.S. 2015/0069499 ("Nakaki")	Sep. 10, 2013	Mar. 12, 2015
N-4, N-9	U.S. 9,252,156 ("Shih")	Feb. 7, 2013	Feb. 2, 2016
N-5, N-10	U.S. 10,991,717 ("Baek")	Sep. 28, 2018	Apr. 27, 2021

Exs.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
See IPRs	U.S. 10,515,973 ("Thimmegowda")	Nov. 30, 2017	Dec. 24, 2019
See IPRs	U.S. 2021/0193676 ("Zhang2")	Dec. 24, 2019	Jun. 24, 2021
See IPRs	U.S. 9,029,938 ("Nakaki2")	Sep. 10, 2013	May 12, 2015
See IPRs	U.S. 11,239,248 ("Xu")	Nov. 18, 2019	Feb. 1, 2022
See IPRs	U.S. 11,217,601 ("Luo")	Oct. 29, 2019	Jan. 4, 2022
See IPRs	U.S. 12,087,572 ("van Schravendijk")	Mar. 28, 2019	Sep. 10, 2024
See IPRs	U.S. 2021/0193536 ("Kris")	Dec. 18, 2019	Jun. 24, 2021
See IPRs	U.S. 10,475,737 ("Tang2")	Apr. 12, 2011	Nov. 12, 2019
See IPRs	U.S. 10,381,369 ("Kim1")	Feb. 21, 2017	Aug. 13, 2019
See IPRs	CN108766971 ("Liu1")		Nov. 6, 2018
See IPRs	U.S. 2012/0070944 ("Kim3")	Sep. 17, 2010	Mar. 22, 2012
See IPRs	U.S. 10,026,692 ("Chen4")	Apr. 12, 2016	Jul. 17, 2018

Table N-1: Prior Art Patents and Patent Publications for the '604 Patent

Ex.	Title	Authors	Publisher	Date of Publication
See IPRs	"NAND Flash Memory Technologies" ("Aritome")	Aritome		2016
See IPRs	"3D NAND Flash Based on Planar Cells" ("Silvagni")	Silvagni	Computers	2017
See IPRs	"Inside Solid State Drives (SSDs)" ("Micheloni 2018")	Micheloni et al.		2018
See IPRs	"3D Flash Memories" ("Micheloni 2016")	Micheloni		2016

Table N-2: Prior Art Non-Patent Publications for the '604 Patent

2. Anticipation and Obviousness (Patent L.R. 3-3(b) and (c))

The Asserted Claims of the '604 Patent are invalid because they are anticipated by the prior art and/or because they would have been obvious in view of the prior art.

The prior art identified by Defendants anticipates and/or renders obvious one or more of the Asserted Claims of the '604 Patent under at least AIA §§ 102(a)(1), 102(a)(2), and 103. For each prior art reference, Defendants have provided claim charts attached to these Invalidity Contentions as Exhibits N-1 through N-10. These charts identify where each element of each Asserted Claim can be found in each item of prior art. In addition to the above identified claims charts, Micron hereby incorporates by reference IPR2025-00035 filed with the United States Patent and Trademark Office on October 11, 2024.

Again, to the extent not anticipated, the Asserted Claims of the '604 Patent are invalid as obvious under 35 U.S.C. § 103. Each prior art reference identified in the preceding sections—either alone or in combination with another prior art reference and/or in combination with the knowledge of one skilled in the art—renders the Asserted Claims invalid as obvious. In rendering the Asserted Claims obvious, each prior art reference identified in the preceding sections may be combined with: (1) information known to persons skilled in the art at the time of the alleged invention, (2) any of the other anticipatory or obviousness prior art references, (3) any statements in the intrinsic record of the '604 Patent and related applications, or (4) any of the additional prior art identified below.

3. Motivations to Combine[14]

A person of ordinary skill in the art would have been motivated to combine the preceding references (*see* Section VIII.A.1) for the following reasons. Teachings, suggestions, motivations and/or reasons to modify any of the references and/or to combine any two or more of the references can come from many sources, including the prior art (by specific reference and when read as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obviousness to try, the nature of the problem faced, and/or knowledge possessed by a person of ordinary skill.

Although a patent claim may be invalidated based on a teaching-suggestion-motivation ("TSM") rationale—*i.e.,* that some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference

[14] The statements in this section about what was known and obvious to a POSA are made with respect to the effective filing date of the '604 Patent.

teachings to arrive at the claimed invention—the Supreme Court identified additional rationales in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007). The following of these rationales apply here:

> (A) the asserted claims combine prior art elements according to known methods to yield predictable results;
>
> (B) the asserted claims involve the simple substitution of one known element for another to obtain predictable results;
>
> (C) the asserted claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;
>
> (D) the asserted claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;
>
> (E) the asserted claims involve combinations of prior art references that would have been "obvious to try"'—a person of ordinary skill in the art could have reached the asserted claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
>
> (F) the asserted claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach); *see also* Department of Commerce, Patent and Trademark Office, Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.,* 72 Fed. Reg. 57,526 (Oct. 10, 2007). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420-21.

Thus, even in the absence of a specific teaching, suggestion, or motivation to combine references, the Asserted Claims here are obvious and therefore invalid. Each of the cited references or devices is in the same field as the '604 Patent, making it obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. One of ordinary skill in the art would have recognized that improvements could be achieved by combining or modifying prior art references that described such improvements. Each of the above prior art references

describes systems, products, or methods that were known to offer such improvements, and, accordingly, one of ordinary skill in the art would have been motivated to combine or modify the references as identified in each of the combinations below.

Furthermore, because each prior art reference concerns three-dimensional NAND memory designs, common industry knowledge supplied a reason to combine any one the above references. It was well understood that different three-dimensional NAND memory structural features could be employed together or interchanged with each other, fitting together like puzzle pieces. Each combination would have produced predictable results and would simply represent a known alternative to one of ordinary skill in the art of NAND memory. This is a further motivation to combine any of the above references.

The below sections further address particular reasons to combine the above references. The below should not be construed as an admission that there is any value to the alleged invention of the '604 Patent. As discussed previously, these contentions are based in significant part on how Plaintiff is apparently construing the asserted claim in its Infringement Contentions, which is an incorrect and overbroad interpretation of the alleged invention of the '604 Patent. Accordingly, to the extent the below refers to benefits of certain elements or industry trends towards these elements, this is not an admission that the alleged invention of the '604 Patent provides any benefits: to the contrary, properly construed and compared to the prior art, the '604 Patent provides no benefits. Likewise, to the extent the below refers to substituting elements, this is not an admission that the elements subject to the substitution are in any way similar, *e.g.,* perform the same function, in the same way, to achieve the same result.

The various elements of the Asserted Claims were well known in the prior art at the time of the alleged invention, and the combination would have been obvious to one of skill in the art. The combinations simply (a) combine prior art elements according to known methods to yield predictable results; (b) involve the simple substitution of one known element for another to obtain predictable results; (c) involve the use of a known technique to improve similar devices (methods, or products) in the same way; (d) apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) involves combinations of prior art references

that would have been "obvious to try" – a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and/or (f) would have been prompted by known work, based on design incentives or other market forces, because such variations were predictable to one of ordinary skill in the art.

Moreover, the Supreme Court has stated that a motivation to combine may be simply "common sense" and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420. Indeed, the Supreme Court held that it is sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421. Here, all the claim elements are common sense and are easily fit together by one of ordinary skill in the art.

While not necessary, a motivation to combine may also be found in the references themselves. One of skill in the art would have been motivated to combine a reference that refers to, or otherwise explicitly invites combination with, another reference. Where the references cited herein have such an explicit invitation to combine, that invitation would have motivated one of skill in the art to combine any such references.

Micron hereby identifies the following '604 Patent Primary References: Lee 551, Yip2, and Thimmegowda.

The below provides several exemplary combinations and motivations for combining an '604 Patent Primary Reference with another reference.

A POSA would have been motivated to combine the teachings of any of the bridge/staircase references (*e.g.*, Lee 551, Yip2, etc.) with any of the "finger" references (*e.g.*, Kobayashi, Lee 730, Nakaki, Shih, Baek, etc.) with a reasonable expectation of success.

To begin, it bears noting note that Micron is not bodily incorporating Kobayashi/Lee II/Nakaki/Shih/Baek into Lee 551/Yip2, or vice versa. Rather, Micron is combining the respective

teachings of Lee 551/Yip2's bridge and array architecture that enables a single staircase to bidirectionally drive two arrays and Kobayashi/Lee 730/Nakaki/Shih/Baek stairstep teachings that mitigate punch through. *See, e.g., In re Keller*, 642 F.2d 413, 425 (CCPA 1981) ("The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference .... Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art.").

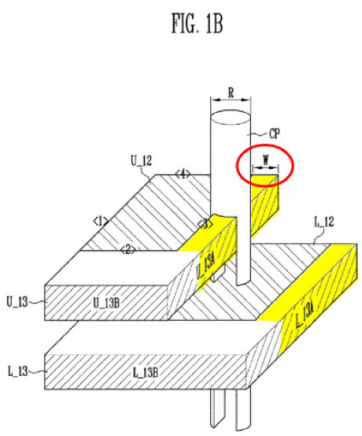
Put another way, Micron's invalidity/obviousness contentions are the same whether one were to frame the combination as Kobayashi/Lee 730/Nakaki/Shih/Baek stairstep finger approach in view of Lee 551/Yip2's bridge and array architecture teachings. A POSA would have been motivated to apply Kobayashi/Lee 730/Nakaki/Shih/Baek's teaching of nonoverlapping conductive fingers to ameliorate the known problems (*e.g.*, short circuits) associated with punch through in Lee 551/Yip2's staircase.

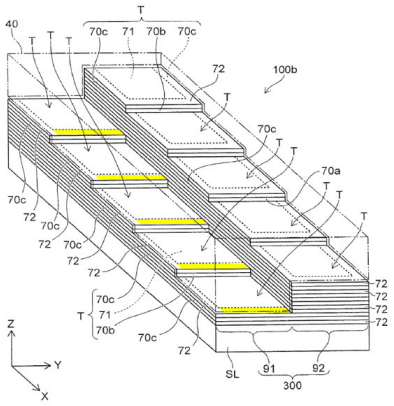
The problem of overetching wordline via holes in 3D NAND staircase structures was well-known in the art. *See, e.g.*, U.S. Pat. 11,239,248, 13:2-11 ("forming electrically conductive contact structures 126 in a conventional microelectronic device may undesirably punch through the one or more of the electrically conductive materials (e.g., the electrically conductive structures 122) of relatively shallower stadia (such as of the first stair step structure 102 a and the second stair step structure 102 b)"); U.S. Pat. 11,217,601, 1:66-2:1 (discussing "undesirable defect[]" of "word line contact punch through"), 9:62-10:6; U.S. Pat. 12,087,572, 3:52-58 ("contact surfaces on wordlines located at higher positions on the staircase may be over-etched relative to wordlines located toward the bottom of the staircase pattern. As a result, the etch may punch through those wordlines to reach another wordline below. When the via is then filled with metal these wordlines will be shorted, causing yield loss."), 7:42-46 ("such a phenomenon is typically undesirable and referred to as 'punchthrough,' or 'breakthrough,' to the layers positioned beneath the intended tungsten wordline 45 contact point or layer."), 7:61-63 ("Challenges in forming 3D NAND structures include punchthrough of tungsten wordlines when etching vias of different depths."); U.S. Pub. 2021/0193536, Fig. 5, [0061] ("a second degree overetched hole … may represent a punch through

scenario."), [0079]-[0080] ("If fourth hole 44 is filled with conductive material—the sixth and fifth conductive layers will be shorted.").

A POSA would naturally look to existing solutions, such as those proposed by Kobayashi/Lee 730/Nakaki/Shih/Baek, to address the punch-through problem (*e.g.*, to improve yield). Lee 730 discloses using non-overlapping conductive fingers to mitigate the effects of punch-through. Lee 730, [0037]-[0038], [0056]. So, too, does Kobayashi. Kobayashi, [0139]-[0145] ("Because the spacer portions 71 [] are insulating bodies, the contact CC is not shorted … even when the contact CC reaches the spacer portions 71 of the other layers lower than the [desired wordline]"). Likewise, Nakaki explains its solution to punch through. *See generally* U.S. Pub. 2015/0069499, [0183]-[0199], [0192] ("The contact parts 141 do not overlap each other in the Z-direction. The contact parts 141 are displaced in the Y-direction parallel to the surface of the substrate 10. The contact parts 141 are spaced in the Y-direction."). Shih also discloses a similar solution to this issue. Shih, Figs.11-13B (showing contact openings filled with conductive material are formed over and connect to inner lower resistance regions, where the inner lower resistance regions are offset from and do not overlap each other in the Z direction), 7:35-8:67. So does Baek. Baek, Figs. 2, 3, 6, and 7 (showing that a given contact plug 202 can connect to a pad pattern 180c and pass through the insulating material disposed on and under the pad pattern 180c because each pad pattern is offset from and do not overlap each other in the first direction), 8:18-42.

Each of Lee 551/Yip2 and Kobayashi/Lee 730/Nakaki/Shih/Baek disclose 3D NAND memory devices that utilize a staircase structure to provide wordline contacts for accessing the memory arrays. While Lee 730 discloses forming multiple sets of staircases (labeled "interconnection structures C1 to C3"), all of which employ the "finger" approach (see Lee 730, Fig. 1), Lee 730's finger approach is readily applicable to the single staircase illustrated in Yip2 Fig. 3 and Lee 551 Fig. 1F. In view of the combined teachings of Lee 551/Yip2 and Kobayashi/Lee 730/Nakaki/Shih/Baek, two implementations of Kobayashi/Lee 730/Nakaki/Shih/Baek finger approach would have been obvious to a POSA. First, it would have been obvious to a POSA to use a "thin" finger narrower (in the x-direction) than the width of a step as Lee 730 Fig. 1B and Kobayashi Fig. 5 expressly disclose. Kobayashi, Fig. 5, [0069] ("first conductive portion 70b").

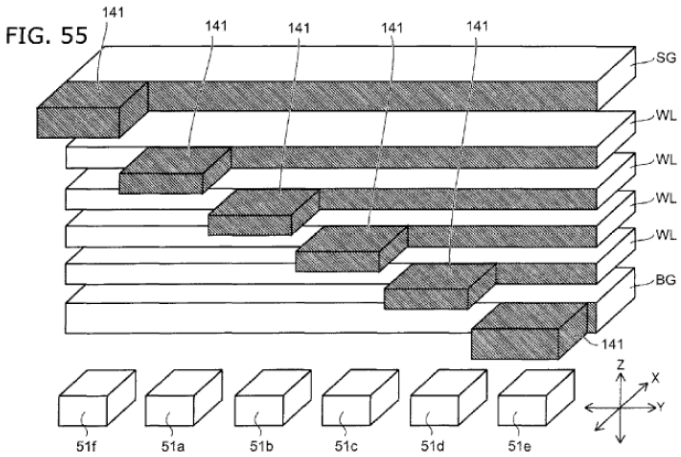




Lee 730 Kobayashi

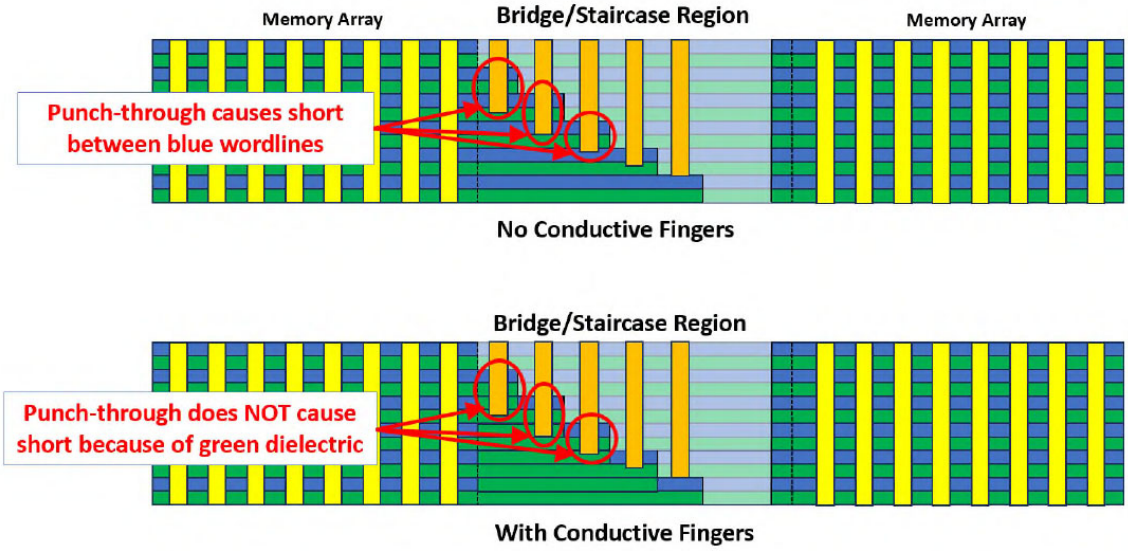
Lee 730, Fig. 1B (showing finger with width "W" less than step width); Kobayashi, Fig. 5 (similar); Shih, Figs. 11, 12, 13 (similar); Baek, Figs. 1, 4, 5, 6 (similar).

Second, it would also have been obvious to a POSA to make the conductive finger cover the full width of the step, especially given that Lee 551/Yip2's landing pad already did so. Further, other 3D NAND references, like Nakaki Fig. 55 below, already disclosed non-overlapping conductive fingers (which solved punch through) that covered the full exposed surface area of each stairstep. Nakaki, 14:64-65 ("the end parts 141 of the aforementioned staircase structure section 140 are provided as contact parts"), 15:10-11 ("The contact parts 141 do not overlap each other in the Z-direction.").



Id., Fig. 55; *see also id.*, Fig. 56. A POSA would have readily understood that a conductive finger covering the full exposed area of a stair step mitigates the deleterious effects of punch through.

This is illustrated, at a conceptual level, by the demonstrative cross-section figures below. The blue layers represent conductive wordlines, the green layers are dielectric, the orange pillars are wordline vias, and the yellow pillars are memory strings.



In the top figure, which does not employ a "finger" approach, the wordline vias "punch through" the intended wordline to an underlying wordline and electrically short the two wordlines together. The lower figure employs conductive fingers that cover the full width of each exposed step. Significantly, adjacent to each step (in the x-direction) is green dielectric material, instead of conductor. Thus, even though the wordline vias "punch through" the intended wordline, they merely extend in the z-direction through additional dielectric and do not create a short to another wordline. Especially given that Lee 551/Yip2's wordline via landing area already covered the full step width and placed the wordline via in the center of the landing pad (*see, e.g.*, Yip2, Fig. 3, Lee 551, Fig. 1F), a POSA would have found it obvious to use a full step-width conductive finger in view of the combined teachings of Lee 551/Yip2 and Kobayashi/Lee 730/Nakaki/Shih/Baek to mitigate punch through.

Additionally, all of Lee 551/Yip2/Kobayashi/Lee 730/Nakaki/Shih/Baek discloses and/or are compatible with the well-known gate-replacement manufacturing process, which provides additional motivation to combine Lee 551/Yip2 with Kobayashi/Lee 730/Nakaki/Shih/Baek. For example, Lee 730 discloses forming its conductive fingers (and the memory device at large) using gate-replacement, which would benefit Lee 551/Yip2's bridge and array architecture. Lee 730,

[0044] (replacing "sacrificial layers"). And Kobayashi discloses forming its conductive fingers (and the memory device at large) using gate-replacement, which would benefit Lee 551/Yip2's bridge and array architecture. Kobayashi, Figs. 7-33B, [0010]-[0012], [0087]-[0145]. For example, Kobayashi discloses using tungtsen wordlines (Kobayashi, [0074], [0135]) or other metals which were known to substantially lower wordline resistance and provide faster memory read/write operations, as described in textbooks published several years before the '604 patent's priority date. *See* Micheloni, "3D Flash Memories" (2016), 131-32. Moreover, employing the bridge and architecture in Lee 551/Yip2 would have provided the advantage of bidirectionally driving two arrays using a single staircase (which saves space), and would be complementary to lower resistance from metal gates (via gate replacement). *See, e.g.*, Lee 551, [0011] ("The structures and methods of the disclosure may permit individual (e.g., single) switching devices (e.g., transistors) of at least one string driver device electrically connected to one or more conductive structures of an individual tier to drive voltages completely across and / or in opposing directions across the tier. The structures and methods of the disclosure may decrease the number of switching devices and interconnections required to effectively operate a memory device, and may increase one or more of memory device performance, scalability, efficiency, and simplicity as compared to many conventional structures and methods"); Baek, 7:63-8:6 ("the gate electrode 180a, the conductive line 180b, the pad pattern 180c, and the connection line 180d may include the same metal material. The gate electrode 180a, the conductive line 180b, the pad pattern 180c, and the connection line 180d may include a barrier pattern and a metal pattern. … The metal pattern may include a metal having low resistance, e.g., tungsten, titanium, tantalum, platinum, cobalt, etc.").

Yip2 also discloses that a bridge between two memory arrays "reduc[es] an area covered by the stair step vertical memory arrays" and results in "the formation of structures including a higher number of memory cells and conductive tiers," which further motivates a POSA to apply Yip2's teachings to the finger references. Yip2, [0006]; *see also id.*, [0048] ("A length LSS (FIG. 5) of the stair step structure may be adjusted as desired to provide sufficient space for forming the access lines 306 such that electrical stress and manufacturing cost is reduced or maintained at a relatively low level, without adding significant width W and/or number of first select gates 308 and

corresponding sub-blocks to the memory array block 350 as a whole, or even while reducing the width W and/or number of first select gates 308 and corresponding sub-blocks of the memory array block 350."); [0033] ("electrical resistance through the access lines 306 may be reduced.").

Kobayashi discloses that its disclosure makes it "possible to reduce the surface area of the terrace portions T. This makes it possible to reduce the surface area of the entire semiconductor device (chip)," providing further motivation to use its finger teachings. Kobayashi, [0133],

A POSA would have had a reasonable expectation of success in combining the teachings of Lee 551/Yip2's bridge and array architecture (to drive two memory arrays with one wordline via) with Kobayashi/Lee 730/Nakaki/Shih/Baek's staircase finger approach (to mitigate punch through). To begin, all of Lee 551/Yip2/Kobayashi/Lee 730/Nakaki/Shih/Baek relate to 3D NAND memory devices with memory arrays whose memory strings are accessed using wordline vias in contact with individual staircase steps.

Thus, the references share a number of key architectural similarities. In particular, combining Kobayashi/Lee 730/Nakaki/Shih/Baek's finger approach with Lee 551/Yip2's bridge would not change the functionality of how wordline vias read/write the memory cells (viz., there would still be an electrically conductive path to the memory arrays). Likewise, applying Yip2/ Lee 551's bidirectional wordline bridge teachings to Kobayashi/Lee 730/Nakaki/Shih/Baek would not have any impact on how the finger approach mitigates punch through. And all five references disclose and/or are entirely compatible with a gate replacement manufacturing process. Indeed, a POSA looking at their references would recognize as much, and would not be able to tell by looking at the conceptual or architectural figures what type of manufacturing process (e.g., gate replacement) was used, and would have understood that no particular manufacturing process was required (e.g., the wordline could be made of doped polysilicon or metal such as tungsten).

Concerning manufacturing, Lee 730 (for example) provides detailed teachings regarding a gate replacement process for forming the fingers, and explains in detail how to manufacture the conductive fingers 13 and adjacent dielectric portions 12. *See* Lee 730, Figs. 4-13B (and accompanying discussion at [0043]-[0062] describing the gate replacement manufacturing process in detail, especially [0044]-[0045], [0048], [0050], and [0053]-[0055]). More generally, gate

replacement techniques were well-known and well within the knowledge and skill of a POSA, and could readily be applied to form the bridge/staircase structure in Lee 551/Yip2. *See also, e.g.*, U.S. Pub. 2017/0256551, Figs. 1A-1F (illustrating formation of 3D NAND bridge using gate-replacement process). Kobayashi, too, provides detailed teachings regarding a gate replacement process for forming the fingers, and explains in how to manufacture the conductive fingers 70b and adjacent "spacer portions 71" formed of sacrificial dielectric material. See Kobayashi, Figs. 7-33B (and accompanying discussion at [0087]-[0144] describing the gate replacement manufacturing process in detail). Shih similarly discloses details a "process flow." Shih, Fig. 14, 9:1-50. Baek also discloses manufacturing details, including related to its replacement process. Baek, 7:63-8:6, 14:55-63. Accordingly, a POSA would have had a reasonable expectation of success in combing the bridge and finger teachings.

To the extent any reference's top stair portion is the oxide layer of the stack and the bottom comprises the conductor and dielectric portions (*see, e.g.*, Kobayashi, Fig. 3, [0029]), it was widely known that when forming a staircase, interchangeable options include having the top or bottom portion the oxide layer, and this grounds applies the obvious variation in which the oxide is on the bottom of the step. *See, e.g.*, U.S. Pub. 2012/0070944), [0090] ("each of top surfaces of the insulating layers . . . constituting the stepwise stacked layer . . . may be partially exposed in the word line contact region WCTR. In other embodiments, each of top surfaces of the sacrificial layers . . ., not the top surfaces of the insulating layers . . ., may be partially exposed"), [0091] (same), [0240] (similar); U.S. Pat. 10,026,692, Figs. 7A, 7B (showing each alternative). Further, it was known how to create the finger with the conductive layer on top, as Lee 730 demonstrates. *See* Lee 730, Fig. 1A-C. Each arrangement is simply a choice among two options, both of which provide the beneficial staircase and finger structure, and the only difference is a minor change in manufacturing the staircase and finger. As Lee 730 and the other mentioned reference demonstrate, it was well within a POSA's knowledge how to form the staircase and finger with the conductor portion on top.

B. Invalidity Based on Section 112 (Patent L.R. 3-3(d))

1. Indefiniteness

Defendants provide the following grounds for invalidity under 35 U.S.C. § 112. Defendants' investigation of the Asserted Patents is ongoing, and Defendants reserve the right to amend or supplement these disclosures based on further investigation and in a manner consistent with the Federal Rules of Civil Procedure, the Local Patent Rules for the Northern District of California, and the Docket Control Order, or otherwise in accordance with any order or direction of this Court or agreement of the parties. Further, Plaintiff's Infringement Contentions fail to provide sufficient detail to fully understand its proposed application of the Asserted Claims, and Defendants reserve the right to assert additional grounds for invalidity under 35 U.S.C. § 112 in response to Plaintiff's claim interpretations. Defendants also reserve the right to supplement, modify, or otherwise amend these grounds for invalidity under 35 U.S.C. § 112 based on the Court's claim construction rulings or opinions or the parties' positions or arguments taken in connection with the claim construction process.

2. Written Description and Enablement

The specification of the '604 Patent does not provide adequate written description to support the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims. 35 U.S.C. § 112(a) requires that a patent specification contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharm., Inc.*, 598 F.3d at 1351 (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ.*, 541 F.3d at 1122 (quoting *Vas-Cath Inc.*, 935 F.2d at 1563–64). The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Additionally, the Asserted Patents do not enable the claim scopes contained in Plaintiff's Infringement Contentions. Section 112(a) requires a specification to describe "the manner and

process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention].” The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This “requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation.” *AK Steel Corp.*, 344 F.3d at 1244 (citation omitted); *see Wyeth & Cordis Corp.*, 720 F.3d at 1385–86. The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Defendants provide below an identification of terms in Asserted Claims that render the Asserted Claims, at least as apparently construed by Plaintiff in its Infringement Contentions as discussed above, invalid pursuant to 35 U.S.C. § 112 as not enabled or lacking sufficient written description:

- “performing a plasma treatment to an exposed portion of the first sacrificial layer of the at least one of the stairs to alter an etch rate” (Claim 18)
- “one or more dielectric pairs” (Claims 1, 3, 11)
- “a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure” (Claim 1)
- “a bridge structure in contact with the first memory array structure and the second memory array structure” (Claim 1)
- “a dielectric portion at a same level and in contact with the conductor portion” (Claims 1, 9)
- “along a second lateral direction perpendicular to the lateral direction” (Claims 1, 9)
- “a dielectric layer under the conductor portion and the dielectric portion” (Claims 2, 10)
- “the conductor portion is above a second dielectric portion that is located between a dielectric layer and the conductor portion” (Claims 6, 14)
- “a dielectric layer is arranged under the conductor portion and the dielectric portion” (Claim 8)

- "a conductor portion on a top surface of the stair and a dielectric portion at a same level and in contact with the conductor portion" (Claim 9)
- "a dielectric layer under the conductor portion and the dielectric portion" (Claims 2, 10)
- "the conductor portion and the dielectric layer are each above one or more dielectric pairs" (Claim 11)
- "the conductor portion is above a second dielectric portion that is located between a dielectric layer and the conductor portion" (Claims 6, 14)
- "forming a plurality of stairs comprising interleaved a plurality of first sacrificial layers and a plurality of first dielectric layers in a plurality of stairs" (Claim 15)
- "the bridge structure comprising interleaved a plurality of second sacrificial layers and a plurality of second dielectric layers" (Claim 15)
- "each first sacrificial layer being in contact with a respective second sacrificial layer of the same level, and each first dielectric layer being in contact with a respective second dielectric layer of the same level" (Claim 15)
- "forming a sacrificial portion in the first sacrificial layer corresponding to at least one of the stairs" (Claim 15)
- "removing, by a first etching process, the second sacrificial layers to form a plurality of lateral recesses" (Claim 15)
- "removing, by a second etching process, the sacrificial portion to form a lateral recess portion" (Claim 15)
- "forming (i) a plurality of conductor layers in the lateral recesses and (ii) a conductor portion in the lateral recess portion and in contact with a respective one of the conductor layers" (Claim 15)
- "forming a protection layer on the first sacrificial layer before the plasma treatment" (Claim 19)
- "retaining a portion of the first sacrificial layers and first dielectric layers under the sacrificial portion" (Claim 20)

IX. INVALIDITY OF THE '711 PATENT

A. Priority Date

The '711 Patent claims priority through application no. PCT/CN2018/101308, filed on August 20, 2018, to Chinese application no. 201710774754.6 (the "CN Application"), filed on August 31, 2017. The CN Application contains a significantly shorter disclosure and does not disclose at least the subject matters of claims 4, 7, 8, 10, 12, 15, 17, 19. Accordingly, these claims of the '711 Patent are entitled to a priority date no earlier than August 20, 2018.

B. Invalidity Based on the Prior Art

As shown below, the alleged inventions of the '711 Patent were well-known in the prior art. Those skilled in the art were aware of all of the limitations claimed in the '711 Patent. Thus, many prior art patents, publications, products, and combinations thereof, disclose, teach, or embody every limitation of the Asserted Claims and thus invalidate those claims. Examples of these disclosures, teachings, and embodiments are identified in the following sections and in the attached claim charts.

1. Identification of Prior Art References (Patent L.R. 3-3(a))

Subject to the reservation of rights above, Defendants identify each item of prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the '711 Patent. The patents/applications, publications, and systems identified are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations.

Some of the below citations and those in the corresponding invalidity claim charts involve prior art references that have corresponding related, foreign, and/or PCT counterpart publications. In such cases, where either the U.S. patent or related, foreign, and/or PCT counterpart is cited, it is to be understood that the corresponding disclosures from the counterpart patent and publications (which are substantively the same) are implicitly incorporated by reference in the alternative to avoid needless repetition.

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
O-1	U.S. 2019/0067306A1 ("Fang")	Aug. 24, 2017	Feb. 28, 2019
O-2	U.S. 2018/0114794A1 ("Jang1")	Oct. 26, 2016	Apr. 26, 2018
O-3	U.S. 2018/0068707A1 ("Shin")	Sep. 6, 2016	Mar. 8, 2018
O-4	U.S. 2017/0294384A1 ("Chen3")	Apr. 12, 2016	Oct. 12, 2017

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
O-5	U.S. 2017/0117222A1 ("Kim4")	Oct. 22, 2015	Apr. 27, 2017
O-6	KR10-2013-0015120 ("Lee 120")	Aug. 2, 2011	Feb. 13, 2013
O-7	U.S. 2018/0330985A1 ("Yu3")	Nov. 23, 2016	Nov. 15, 2018
O-8	U.S. 2017/0062470A1 ("Han")	Aug. 28, 2015	Mar. 2, 2017
See IPR	U.S. 2012/0070944A1 ("Kim3")	Sep. 17, 2010	Mar. 22, 2012
See IPR	KR10-2015-0051841 ("Park5")	Nov. 5, 2013	May 13, 2015
See IPR	U.S. 9,728,547 ("Ohsaki")	May 19, 2016	Aug. 8, 2017
See IPR	U.S. 2013/0313627A1 ("Lee 627")	May 23, 2012	Nov. 28, 2013

Table O-1: Prior Art Patents and Patent Publications for the '711 Patent

Ex.	Title	Authors	Publisher	Date of Publication
See IPR	"NAND Flash Memory Technologies" ("Aritome")	Aritome		2016
See IPR	"3D NAND Flash Based on Planar Cells" ("Silvagni")	Silvagni	Computers	2017
See IPR	"Inside Solid State Drives (SSDs)" ("Micheloni 2018")	Micheloni		2018
See IPR	"ULSI Technology" ("Chang")	Chang		1996
See IPR	*Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy* ("Orlowski")	Orlowski		2010

Table O-2: Prior Art Non-Patent Publications for the '711 Patent

2. Anticipation and Obviousness (Patent L.R. 3-3(b) and (c))

The Asserted Claims of the '711 Patent are invalid because they are anticipated by the prior art and/or because they would have been obvious in view of the prior art.

The prior art identified by Defendants anticipates and/or renders obvious one or more of the Asserted Claims of the '711 Patent under at least AIA §§ 102(a)(1), 102(a)(2), and 103. For each prior art reference, Defendants have provided claim charts attached to these Invalidity Contentions as Exhibits O-1 through O-8. These charts identify where each element of each Asserted Claim can

be found in each item of prior art. In addition to the above identified claims charts, Micron hereby incorporates by reference IPR2025-00117 filed with the United States Patent and Trademark Office on November 12, 2024 ("'711 IPR").

Again, to the extent not anticipated, the Asserted Claims of the '711 Patent are invalid as obvious under 35 U.S.C. § 103. Each prior art reference identified in the preceding sections—either alone or in combination with another prior art reference and/or in combination with the knowledge of one skilled in the art—renders the Asserted Claims invalid as obvious. In rendering the Asserted Claims obvious, each prior art reference identified in the preceding sections may be combined with: (1) information known to persons skilled in the art at the time of the alleged invention, (2) any of the other anticipatory or obviousness prior art references, (3) any statements in the intrinsic record of the '711 Patent and related applications, or (4) any of the additional prior art identified below.

3. Motivations to Combine[15]

A person of ordinary skill in the art would have been motivated to combine the preceding references (*see* Section IX.B.1) for the following reasons. Teachings, suggestions, motivations and/or reasons to modify any of the references and/or to combine any two or more of the references can come from many sources, including the prior art (by specific reference and when read as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obviousness to try, the nature of the problem faced, and/or knowledge possessed by a person of ordinary skill.

Although a patent claim may be invalidated based on a teaching-suggestion-motivation ("TSM") rationale—*i.e.,* that some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention—the Supreme Court identified additional rationales in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007). The following of these rationales apply here:

(A) the asserted claims combine prior art elements according to known methods to yield predictable results;

[15] The statements in this section about what was known and obvious to a POSA are made with respect to the effective filing date of the '711 Patent.

(B) the asserted claims involve the simple substitution of one known element for another to obtain predictable results;

(C) the asserted claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;

(D) the asserted claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) the asserted claims involve combinations of prior art references that would have been "obvious to try"'—a person of ordinary skill in the art could have reached the asserted claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) the asserted claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach); *see also* Department of Commerce, Patent and Trademark Office, Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.,* 72 Fed. Reg. 57,526 (Oct. 10, 2007). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420-21.

Thus, even in the absence of a specific teaching, suggestion, or motivation to combine references, the Asserted Claims here are obvious and therefore invalid. Each of the cited references or devices is in the same field as the '711 Patent, making it obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. One of ordinary skill in the art would have recognized that improvements could be achieved by combining or modifying prior art references that described such improvements. Each of the above prior art references describes systems, products, or methods that were known to offer such improvements, and, accordingly, one of ordinary skill in the art would have been motivated to combine or modify the references as identified in each of the combinations below.

Furthermore, because each prior art reference concerns three-dimensional NAND memory designs, and more specifically word-line contact structures, common industry knowledge supplied a reason to combine any one the above references. It was well understood that different three-dimensional NAND memory structural features, including those of word-line contact structures, could be employed together or interchanged with each other, fitting together like puzzle pieces. Each combination would have produced predictable results and would simply represent a known alternative to one of ordinary skill in the art of NAND memory. This is a further motivation to combine any of the above references.

The below sections further address particular reasons to combine the above references. The below should not be construed as an admission that there is any value to the alleged invention of the '711 Patent. As discussed previously, these contentions are based in significant part on how Plaintiff is apparently construing the asserted claim in its Infringement Contentions, which is an incorrect and overbroad interpretation of the alleged invention of the '711 Patent. Accordingly, to the extent the below refers to benefits of certain elements or industry trends towards these elements, this is not an admission that the alleged invention of the '711 Patent provides any benefits: to the contrary, properly construed and compared to the prior art, the '711 Patent provides no benefits. Likewise, to the extent the below refers to substituting elements, this is not an admission that the elements subject to the substitution are in any way similar, *e.g.,* perform the same function, in the same way, to achieve the same result.

The various elements of the Asserted Claims were well known in the prior art at the time of the alleged invention, and the combination would have been obvious to one of skill in the art. The combinations simply (a) combine prior art elements according to known methods to yield predictable results; (b) involve the simple substitution of one known element for another to obtain predictable results; (c) involve the use of a known technique to improve similar devices (methods, or products) in the same way; (d) apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) involves combinations of prior art references that would have been "obvious to try" – a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a

reasonable expectation of success; and/or (f) would have been prompted by known work, based on design incentives or other market forces, because such variations were predictable to one of ordinary skill in the art.

Moreover, the Supreme Court has stated that a motivation to combine may be simply "common sense" and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420. Indeed, the Supreme Court held that it is sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421. Here, all the claim elements are common sense and are easily fit together by one of ordinary skill in the art.

While not necessary, a motivation to combine may also be found in the references themselves. One of skill in the art would have been motivated to combine a reference that refers to, or otherwise explicitly invites combination with, another reference. Where the references cited herein have such an explicit invitation to combine, that invitation would have motivated one of skill in the art to combine any such references.

Micron hereby identifies the following '711 Patent Primary References: Yu3, Jang1, Shin, Han, Kim3, and Park5.

The below provides several exemplary combinations and motivations for combining an '711 Patent Primary Reference with another reference.

a. A Barrier Layer and an Etch-Stop Layer

Claim 1 recites "a barrier layer disposed over a portion of the gate stack of the each step" and "an etch-stop layer disposed on the barrier layer." Independent claim 13 recites "an etch-stop layer disposed on a portion of the gate stack of the each step." Certain '711 Patent Primary References, *e.g.*, Jang1, Shin, and Han (collectively, the "Gate-Stack Prior Art"), disclose a gate stack but do not disclose an etch-stop layer or a barrier layer. On the other hand, certain other '711 Patent references, *e.g.*, Park5, Chen3, Kim4, Lee 120, Fang, Kim3, and Yu3 (collectively, the

"Etch-Stop Prior Art"), disclose an etch-stop layer and most disclose a barrier layer as well.[16] A POSA would have been motivated to combine the gate-stack disclosure from the Gate-Stack Prior Art with the etch-stop layer and/or the barrier from the Etch-Stop Prior Art and would have had a reasonable expectation of success for doing so.

A staircase structure for word-line contacts in 3D memory devices was conventional and routine by the time of the '711 Patent, as almost all '711 Patent references demonstrate. It was also well known that these word-line contacts require etching vertical holes from a top planar surface of the structure to each of the step in the staircase, *i.e.*, holes of various depths must be etched. *See, e.g.*, Fang ¶ [0004]. This in turn requires etching deep holes as well as shallow holes. *Id.* But etching deep holes increases the likelihood of over-etching shallow holes, a defect called "punch through." *Id.*; *see also* Kim4 ¶ [0070]. On the flip side, under-etching to prevent punch through may result in insufficiently etched holes at the low-level steps of the staircase, where the contact holes must have greater depth, leading to open circuits. Kim4 ¶¶ [0070], [0124]-[0125]. "Adjustments to etch chemistries used in the etch process [could] not sufficiently address[] this problem." Fang ¶ [0004]. Using multiple masks could address the problem, but at the expense of "additional processing acts, complexity, and cost to the overall process." *Id.*; *see also* Kim4 ¶ [0125] (similar). Therefore, a technique of using one or more etch-stop layers to reduce the likelihood of punch-through had been developed. *See, e.g.*, Fang ¶ [0008], Chen3 ¶¶ [0037]-[0039], Kim4 ¶¶ [0032], [0054]-[0058], [0148]-[0151].

An etch-stop layer also provides a benefit of preventing or reducing gaps that may form between dielectric layers when sacrificial layers are removed from the stack of the staircase structure. Yu3 ¶ [0081]. This would reduce the manufacturing defect rate and would have further motivated a POSA to apply an etch-stop layer to the word-line contact structure.

In view of the problem of over- or under-etching contact holes of various depths and shorting between gate electrode layers due to gaps created when sacrificial layers are removed, and

[16] A barrier layer of the '711 Patent is simply another etch-stop layer. Related explanation from the IPR Petition against the '711 Patent is hereby incorporated by reference.

further in view of prior ineffective (adjusting etch chemistries) or costly (using multiple masks) solutions, a POSA would have been motivated to use one or more etch-stop layers to address this problem.

A POSA would have had a reasonable expectation of success for several reasons. First, the use of etch-stop layers was already well known in the art and routinely used to fabricate similar word-line contact structures. Second, the techniques of forming etch-stop layers were also conventional. They typically involve nothing more than depositing additional conformal films to form these layers. These layers were formed by conventional deposition processes that were already used to form the staircase stack. For example, Kim4 uses atomic layer deposition (ALD) in forming both the staircase stack and the etch-stop layers. Kim4 ¶¶ [0074], [0081]. Fang discloses that ALD, chemical vapor deposition (CVD), physical vapor deposition (PVD), or a diffusion process may be used to form an etch-stop layer. Fang ¶ [0020]. These were all well-understood and widely used processes within the knowledge and skills of a POSA. Moreover, the fact that one of multiple processes may be used to form etch-stop layers increases the likelihood of success (and, where an existing process may be used, reducing the manufacturing cost of forming the additional etch-stop layer(s)). To the extent a POSA may desire additional information, Yu3 discloses in detail one exemplary ALD and/or CVD apparatus and process. *See generally* Yu3. The additional information further renders the combination obvious and enhances a POSA's reasonable expectation of success.

The number of etch-stop layers (*e.g.*, one etch-stop layer with or without an additional barrier layer) was simply a design choice. For example, Park discloses embodiments with one or two etch-stop layers. Park5 ¶¶ [0042], [0049]. So does Chen3. Chen3, Figs. 4A-4B (one layer), 7A-7B (two layers). Fang uses one etch-stop layer while Kim4 uses two. Fang, Fig. 6; Kim4, Fig. 2. Either choice would have been obvious and was well known. Additionally, Chen3 teaches that using two etch-stop layers, for example a silicon oxide layer and a silicon nitride layer, can provide a larger tunneling length to reduce the likelihood of electron tunneling between the conductive layers through the etch-stop layers. Chen3 ¶¶ [0051]-[0053]. This would have motivated a POSA to add an etch-stop layer (*i.e.*, the barrier layer of the '711 Patent) to a design that has a single layer.

A POSA would have had a reasonable expectation of success because, again, these layers were well known and routine and formed using widely used conventional processes.

b. A Gate Stack Disposed over a Dielectric Layer

The Asserted Claims recite "a gate stack disposed over a dielectric layer." Certain Etch-Stop Prior Art, *e.g.*, Fang and Kim4, shows a reverse layer ordering at each step, *i.e.*, a gate stack on the bottom of each step. Nonetheless, a POSA would have found it obvious that the layer ordering may be flipped to gate stack on top.

Both orders were conventional by the time of the '711 Patent. For example, Kim3 illustrates its staircase structure with a dielectric-layer-on-top configuration. But Kim3 also discloses that the staircase structure may be configured to have gate stack on top at each step. Kim3 ¶¶ [0090]-[0091], [0240]. As another example, Park5 also illustrates its staircase structure with a dielectric-layer-on-top configuration and discloses a gate-stack-on-top configuration. Park5 ¶¶ [0042], [0102]. Yu3 teaches that the layers may be formed in either order. Yu3 ¶¶ [0034]-[0035]. As a final example, Chen3 illustrates both configurations side by side. Chen3, Figs. 7A-7B. At a minimum, these disclosures presenting both orders demonstrate a known technique (a reverse order in which gate stack is on top) that is at least a suitable option for the Etch-Stop Prior Art that discloses only a dielectric-layer-on-top configuration. Knowledge of a suitable option itself provides a motivation to modify. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023). Furthermore, since there are only two orders, it would have been obvious to try either order.

As demonstrated by Kim3, Park5, Yu3, and Chen3, a POSA would have known that either order was routine, highly predictable, and would have had a reasonable expectation of success for implementing a gate-stack-on-top embodiment. A POSA would have further known that the deposition and etching processes used to form staircase structures would work for either order. This further contributes to a reasonable expectation of success.

c. A High-K Dielectric Layer Around a Conductive Gate Layer

The Asserted Claims recite "the gate stack comprising a high-k dielectric layer and a conductive layer."

Yu3 discloses forming "a barrier layer and/or a tungsten nucleation layer … prior to depositing bulk tungsten," which is the conductive layer. Yu3 ¶ [0041]. A POSA would have understood the "barrier layer" to constitute a gate insulating layer that are deposited on the perimeter of the channel. A POSA would have known that such a gate insulating layer commonly comprises a high-k dielectric material. Furthermore, a POSA would have understood Yu3's process of replacing sacrificial layers with gate stacks to be consistent with the process disclosed by individual Gate-Stack Prior Art, *i.e.*, (1) removing sacrificial layers to form gaps in the stack connected to a substrate opening through which the sacrificial layers are removed; and (2) depositing materials to the gaps through the substrate opening. A POSA would have further known that depositing a gate insulating layer before depositing the conductive gate layers to be a viable and common approach from the Gate-Stack Prior Art. Therefore, a POSA would have been motivated by Yu3's express teaching to adopt this approach, thereby forming a gate insulating layer on the perimeter of the channel as well as the perimeter of the gaps (*i.e.*, a high-k dielectric layer around the conductive gate layer).

A POSA would have had a reasonable expectation of success because Yu3's express disclosure confirms the viability of the added layer around the conductive gate layer, and because this approach was well known in the art.

d. Thickness Range and Uniformity of Etch-Stop Layer

Claims 10 and 17 recites a thickness range for the etch-stop layer. Although most Etch-Stop Prior Art references do not disclose the thickness of the etch-stop layer, a POSA would have found the claimed range obvious.

As an initial matter, as the Examiner took official notice during the prosecution of the '711 Patent, the claimed etch-stop layer thickness "[wa]s notoriously well known in the art." '711 Patent File History, Oct. 24, 2019 Office Action at 7. The claimed range—spanning three orders of magnitude—"lacks criticality." *Id.* This is clear from the laundry list of permissible thicknesses in the specification that the Examiner cited. It is further evidenced by the claims of the '711 Patent, where the same range is claimed in claims 10 and 17 for devices with or without a barrier layer (which, again, is another etch-stop layer). Where, as here, the "[d]ifferences between the prior art

and the claimed invention[, if any, is merely] dimensional," not resulting in "differences in performance," the claim is not valid. *Gardner v. TEC Sys., Inc.*, 725 F.2d 1338, 1345-46 (Fed. Cir. 1984).

If more is required (it is not), Fang and Yu3 both disclose a thickness range for an etch-stop layer. Fang's etch-stop layer may have a thickness ranging from about 50 Å to about 1000 Å, or about 5 nm to 100 nm. Fang ¶ [0021]. Yu3's etch-stop layer may have a thickness between about 1 nm to about 250 or 350 nm. Yu3 ¶¶ [0005], [0050]. Both overlaps with the claimed range.

To the extent Fang's or Yu3's disclosed thickness range may be adjusted based on the staircase structure of a particular Etch-Stop Prior Art, such adjustment would have been well within the knowledge and skill of a POSA.

A POSA would have been motivated to apply Fang's or Yu3's disclosure of the etch-stop-layer thickness on a device disclosed in Etch-Stop Prior Art and would have had a reasonable expectation of success to do so.

A POSA would have known that the thickness of an etch-stop layer is at least a necessary (but routine) design parameter and may be important to its purpose of preventing punch-through to underlying layers or shorting between conductive layers in the stack. Thus, for an Etch-Stop Prior Art reference that does not disclose a thickness, a POSA would have been motivated to adapt the etch-stop layer of in view of Fang's or Yu3's thickness range.

A POSA would have understood that the thickness of the etch-stop layer is flexible because other parameters such as the type of etchants or the relative etching rates of the etch-stop and neighboring layers may be adjusted. Accordingly, a POSA would have found the ranges disclosed in Fang and Yu3 to be consistent with expectation. Further, Fang and Yu3 and other Etch-Stop Prior Art disclose analogous semiconductor structures with a conformal etch-stop layer. The respective etch-stop layers comprise similar materials and may be formed using conventional techniques such as CVD or ALD. Fang ¶ [0020]; Yu3 ¶ [0049]. Their disclosures indicate a common and conventional etch-stop layer, which would have lowered any technical barrier for a POSA to adapt a device to the thickness disclosed in Fang or Yu3 and increased the POSA's expectation of success. Further, a POSA would have had a reasonable expectation of success in

applying Fang's or Yu3's etch-stop-layer thickness to another Etch-Stop Prior Art because Fang's and Yu3's ranges were reasonable.

To the extent the thickness of Fang's or Yu3's etch-stop layer would need to be reduced to account for two etch-stop layers in an Etch-Stop Prior Art reference, *e.g.*, to maintain a total etch resistance, a POSA would have found it obvious that the thickness would still overlap with the claimed range. For example, a POSA would have found it unnecessary to reduce the maximum range of Fang's or Yu3's disclosure to below 10 nm (the reduction required to avoid any overlap with the claimed range) to account for one extra etch-stop layer.

C. Invalidity Based on Section 112 (Patent L.R. 3-3(d))

1. Indefiniteness

Defendants provide the following grounds for invalidity under 35 U.S.C. § 112. Defendants' investigation of the Asserted Patents is ongoing, and Defendants reserve the right to amend or supplement these disclosures based on further investigation and in a manner consistent with the Federal Rules of Civil Procedure, the Local Patent Rules for the Northern District of California, and the Docket Control Order, or otherwise in accordance with any order or direction of this Court or agreement of the parties. Further, Plaintiff's Infringement Contentions fail to provide sufficient detail to fully understand its proposed application of the Asserted Claims, and Defendants reserve the right to assert additional grounds for invalidity under 35 U.S.C. § 112 in response to Plaintiff's claim interpretations. Defendants also reserve the right to supplement, modify, or otherwise amend these grounds for invalidity under 35 U.S.C. § 112 based on the Court's claim construction rulings or opinions or the parties' positions or arguments taken in connection with the claim construction process.

2. Written Description and Enablement

The specification of the '711 Patent does not provide adequate written description to support the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims. 35 U.S.C. § 112(a) requires that a patent specification contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that [the inventor]

invented what is claimed." *Ariad Pharm., Inc.*, 598 F.3d at 1351 (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ.*, 541 F.3d at 1122 (quoting *Vas-Cath Inc.*, 935 F.2d at 1563–64). The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Additionally, the Asserted Patents do not enable the claim scopes contained in Plaintiff's Infringement Contentions. Section 112(a) requires a specification to describe "the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention]." The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This "requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp.*, 344 F.3d at 1244 (citation omitted); *see Wyeth & Cordis Corp.*, 720 F.3d at 1385–86. The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Defendants provide below an identification of terms in Asserted Claims that render the Asserted Claims, at least as apparently construed by Plaintiff in its Infringement Contentions as discussed above, invalid pursuant to 35 U.S.C. § 112 as not enabled or lacking sufficient written description:

- "a staircase structure comprising a plurality of steps"
- "a barrier layer"
- "a high-k dielectric layer"

X. <u>INVALIDITY OF THE '276 PATENT</u>

A. Priority Date

The '276 Patent claims priority through application no. PCT/CN2018/101308, filed on August 20, 2018, to Chinese application no. 201710774754.6 (the "CN Application"), filed on August 31, 2017. The CN Application contains a significantly shorter disclosure and does not

disclose at least the subject matters of claims 1, 3-8, 11, 12, 16, and 18. Accordingly, all claims of the ’276 Patent are entitled to a priority date no earlier than August 20, 2018.

B. Invalidity Based on the Prior Art

As shown below, the alleged inventions of the ’276 Patent were well-known in the prior art. Those skilled in the art were aware of all of the limitations claimed in the ’276 Patent. Thus, many prior art patents, publications, products, and combinations thereof, disclose, teach, or embody every limitation of the Asserted Claims and thus invalidate those claims. Examples of these disclosures, teachings, and embodiments are identified in the following sections and in the attached claim charts.

1. Identification of Prior Art References (Patent L.R. 3-3(a))

Subject to the reservation of rights above, Defendants identify each item of prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the ’276 Patent. The patents/applications, publications, and systems identified are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations.

Some of the below citations and those in the corresponding invalidity claim charts involve prior art references that have corresponding related, foreign, and/or PCT counterpart publications. In such cases, where either the U.S. patent or related, foreign, and/or PCT counterpart is cited, it is to be understood that the corresponding disclosures from the counterpart patent and publications (which are substantively the same) are implicitly incorporated by reference in the alternative to avoid needless repetition.

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
P-1	U.S. 2019/0067306A1 (“Fang”)	Aug. 24, 2017	Feb. 28, 2019
P-2	U.S. 2018/0114794A1 (“Jang1”)	Oct. 26, 2016	Apr. 26, 2018
P-3	U.S. 2018/0068707A1 (“Shin”)	Sep. 6, 2016	Mar. 8, 2018
P-4	U.S. 2017/0294384A1 (“Chen3”)	Apr. 12, 2016	Oct. 12, 2017
P-5	U.S. 2017/0117222A1 (“Kim4”)	Oct. 22, 2015	Apr. 27, 2017
P-6	KR10-2013-0015120 (“Lee 120”)	Aug. 2, 2011	Feb. 13, 2013
P-7	U.S. 2018/0330985A1 (“Yu3”)	Nov. 23, 2016	Nov. 15, 2018
P-8	U.S. 2017/0062470A1 (“Han”)	Aug. 28, 2015	Mar. 2, 2017
P-9	U.S. 2012/0070944A1 (“Kim3”)	Sep. 17, 2010	Mar. 22, 2012
P-10	KR10-2015-0051841 (“Park5”)	Nov. 5, 2013	May 13, 2015

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
See ’711 IPR	U.S. 9,728,547 (“Ohsaki”)	May 19, 2016	Aug. 8, 2017
See ’711 IPR	U.S. 2013/0313627A1 (“Lee 627”)	May 23, 2012	Nov. 28, 2013

Table P-1: Prior Art Patents and Patent Publications for the ’276 Patent

Ex.	Title	Authors	Publisher	Date of Publication
See ’711 IPR	“NAND Flash Memory Technologies” (“Aritome”)	Aritome		2016
See ’711 IPR	“3D NAND Flash Based on Planar Cells” (“Silvagni”)	Silvagni	Computers	2017
See ’711 IPR	“Inside Solid State Drives (SSDs)” (“Micheloni 2018”)	Micheloni		2018
See ’711 IPR	“ULSI Technology” (“Chang”)	Chang		1996
See ’711 IPR	*Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy* (“Orlowski”)	Orlowski		2010

Table P-2: Prior Art Non-Patent Publications for the ’276 Patent

2. Anticipation and Obviousness (Patent L.R. 3-3(b) and (c))

The Asserted Claims of the ’276 Patent are invalid because they are anticipated by the prior art and/or because they would have been obvious in view of the prior art.

The prior art identified by Defendants anticipates and/or renders obvious one or more of the Asserted Claims of the ’276 Patent under at least AIA §§ 102(a)(1), 102(a)(2), and 103. For each prior art reference, Defendants have provided claim charts attached to these Invalidity Contentions as Exhibits P-1 through P-10. These charts identify where each element of each Asserted Claim can be found in each item of prior art.

Again, to the extent not anticipated, the Asserted Claims of the '276 Patent are invalid as obvious under 35 U.S.C. § 103. Each prior art reference identified in the preceding sections—either alone or in combination with another prior art reference and/or in combination with the knowledge of one skilled in the art—renders the Asserted Claims invalid as obvious. In rendering the Asserted Claims obvious, each prior art reference identified in the preceding sections may be combined with: (1) information known to persons skilled in the art at the time of the alleged invention, (2) any of the other anticipatory or obviousness prior art references, (3) any statements in the intrinsic record of the '276 Patent and related applications, or (4) any of the additional prior art identified below.

3. Motivations to Combine[17]

A person of ordinary skill in the art would have been motivated to combine the preceding references (*see* Section X.B.1) for the following reasons. Teachings, suggestions, motivations and/or reasons to modify any of the references and/or to combine any two or more of the references can come from many sources, including the prior art (by specific reference and when read as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obviousness to try, the nature of the problem faced, and/or knowledge possessed by a person of ordinary skill.

Although a patent claim may be invalidated based on a teaching-suggestion-motivation ("TSM") rationale—*i.e.,* that some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention—the Supreme Court identified additional rationales in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007). The following of these rationales apply here:

(A) the asserted claims combine prior art elements according to known methods to yield predictable results;

(B) the asserted claims involve the simple substitution of one known element for another to obtain predictable results;

[17] The statements in this section about what was known and obvious to a POSA are made with respect to the effective filing date of the '276 Patent.

(C) the asserted claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;

(D) the asserted claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) the asserted claims involve combinations of prior art references that would have been "obvious to try"'—a person of ordinary skill in the art could have reached the asserted claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) the asserted claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach); *see also* Department of Commerce, Patent and Trademark Office, Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.,* 72 Fed. Reg. 57,526 (Oct. 10, 2007). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420-21.

Thus, even in the absence of a specific teaching, suggestion, or motivation to combine references, the Asserted Claims here are obvious and therefore invalid. Each of the cited references or devices is in the same field as the '276 Patent, making it obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. One of ordinary skill in the art would have recognized that improvements could be achieved by combining or modifying prior art references that described such improvements. Each of the above prior art references describes systems, products, or methods that were known to offer such improvements, and, accordingly, one of ordinary skill in the art would have been motivated to combine or modify the references as identified in each of the combinations below.

Furthermore, because each prior art reference concerns three-dimensional NAND memory designs, and more specifically word-line contact structures, common industry knowledge supplied

a reason to combine any one the above references. It was well understood that different three-dimensional NAND memory structural features, including those of word-line contact structures, could be employed together or interchanged with each other, fitting together like puzzle pieces. Each combination would have produced predictable results and would simply represent a known alternative to one of ordinary skill in the art of NAND memory. This is a further motivation to combine any of the above references.

The below sections further address particular reasons to combine the above references. The below should not be construed as an admission that there is any value to the alleged invention of the ’276 Patent. As discussed previously, these contentions are based in significant part on how Plaintiff is apparently construing the asserted claim in its Infringement Contentions, which is an incorrect and overbroad interpretation of the alleged invention of the ’276 Patent. Accordingly, to the extent the below refers to benefits of certain elements or industry trends towards these elements, this is not an admission that the alleged invention of the ’276 Patent provides any benefits: to the contrary, properly construed and compared to the prior art, the ’276 Patent provides no benefits. Likewise, to the extent the below refers to substituting elements, this is not an admission that the elements subject to the substitution are in any way similar, *e.g.,* perform the same function, in the same way, to achieve the same result.

The various elements of the Asserted Claims were well known in the prior art at the time of the alleged invention, and the combination would have been obvious to one of skill in the art. The combinations simply (a) combine prior art elements according to known methods to yield predictable results; (b) involve the simple substitution of one known element for another to obtain predictable results; (c) involve the use of a known technique to improve similar devices (methods, or products) in the same way; (d) apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) involves combinations of prior art references that would have been “obvious to try” – a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and/or (f) would have been prompted by known work, based on

design incentives or other market forces, because such variations were predictable to one of ordinary skill in the art.

Moreover, the Supreme Court has stated that a motivation to combine may be simply "common sense" and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420. Indeed, the Supreme Court held that it is sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421. Here, all the claim elements are common sense and are easily fit together by one of ordinary skill in the art.

While not necessary, a motivation to combine may also be found in the references themselves. One of skill in the art would have been motivated to combine a reference that refers to, or otherwise explicitly invites combination with, another reference. Where the references cited herein have such an explicit invitation to combine, that invitation would have motivated one of skill in the art to combine any such references.

Micron hereby identifies the following '276 Patent Primary References: Park5, Jang1, Shin, Kim3, Han, and Yu3.

The below provides several exemplary combinations and motivations for combining an '276 Patent Primary Reference with another reference.

a. Forming an Etch-Stop Layer and Optionally a Barrier Layer

The Asserted Claims recite "disposing an etch-stop layer on each step of the plurality of steps." Claims 17 and 18 further recite "prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps." Certain '276 Patent Primary References, *e.g.*, Jang1, Shin, and Han (collectively, the "Gate-Stack Prior Art"), disclose a gate stack (another claim limitation) but do not disclose an etch-stop layer or a barrier layer. On the other hand, certain other '276 Patent references, *e.g.*, Park5, Chen3, Kim4, Lee 120, Fang, Kim3, and Yu3 (collectively, the "Etch-Stop Prior Art"), disclose an etch-stop layer and most disclose a barrier

layer as well.[18] A POSA would have been motivated to combine the gate-stack disclosure from the Gate-Stack Prior Art with the etch-stop layer and/or the barrier from the Etch-Stop Prior Art and would have had a reasonable expectation of success for doing so.

A staircase structure for word-line contacts in 3D memory devices was conventional and routine by the time of the '276 Patent, as almost all'276 Patent references demonstrate. It was also well known that these word-line contacts require etching vertical holes from a top planar surface of the structure to each of the step in the staircase, *i.e.*, holes of various depths must be etched. *See, e.g.*, Fang ¶ [0004]. This in turn requires etching deep holes as well as shallow holes. *Id.* But etching deep holes increases the likelihood of over-etching shallow holes, a defect called "punch through." *Id.*; *see also* Kim4 ¶ [0070]. On the flip side, under-etching to prevent punch through may result in insufficiently etched holes at the low-level steps of the staircase, where the contact holes must have greater depth, leading to open circuits. Kim4 ¶¶ [0070], [0124]-[0125]. "Adjustments to etch chemistries used in the etch process [could] not sufficiently address[] this problem." Fang ¶ [0004]. Using multiple masks could address the problem, but at the expense of "additional processing acts, complexity, and cost to the overall process." *Id.*; *see also* Kim4 ¶ [0125] (similar). Therefore, a technique of using one or more etch-stop layers to reduce the likelihood of punch-through had been developed. *See, e.g.*, Fang ¶ [0008], Chen3 ¶¶ [0037]-[0039], Kim4 ¶¶ [0032], [0054]-[0058], [0148]-[0151].

An etch-stop layer also provides a benefit of preventing or reducing gaps that may form between dielectric layers when sacrificial layers are removed from the stack of the staircase structure. Yu3 ¶ [0081]. This would reduce the manufacturing defect rate and would have further motivated a POSA to apply an etch-stop layer to the word-line contact structure.

In view of the problem of over- or under-etching contact holes of various depths and shorting between gate electrode layers due to gaps created when sacrificial layers are removed, and further in view of prior ineffective (adjusting etch chemistries) or costly (using multiple masks)

[18] A barrier layer of the '276 Patent is simply another etch-stop layer. Related explanation from the IPR Petition against the '711 Patent (the '711 IPR) is hereby incorporated by reference.

solutions, a POSA would have been motivated to use one or more etch-stop layers to address this problem.

A POSA would have had a reasonable expectation of success for several reasons. First, the use of etch-stop layers was already well known in the art and routinely used to fabricate similar word-line contact structures. Second, the techniques of forming etch-stop layers were also conventional. They typically involve nothing more than depositing additional conformal films to form these layers. These layers were formed by conventional deposition processes that were already used to form the staircase stack. For example, Kim4 uses atomic layer deposition (ALD) in forming both the staircase stack and the etch-stop layers. Kim4 ¶¶ [0074], [0081]. Fang discloses that ALD, chemical vapor deposition (CVD), physical vapor deposition (PVD), or a diffusion process may be used to form an etch-stop layer. Fang ¶ [0020]. These were all well-understood and widely used processes within the knowledge and skills of a POSA. Moreover, the fact that one of multiple processes may be used to form etch-stop layers increases the likelihood of success (and, where an existing process may be used, reducing the manufacturing cost of forming the additional etch-stop layer(s)). To the extent a POSA may desire additional information, Yu3 discloses in detail one exemplary ALD and/or CVD apparatus and process. *See generally* Yu3. The additional information further renders the combination obvious and enhances a POSA's reasonable expectation of success.

The number of etch-stop layers (*e.g.*, one etch-stop layer with or without an additional barrier layer) was simply a design choice. For example, Park5 discloses embodiments with one or two etch-stop layers. Park5 ¶¶ [0042], [0049]. So does Chen3. Chen3, Figs. 4A-4B (one layer), 7A-7B (two layers). Fang uses one etch-stop layer while Kim4 uses two. Fang, Fig. 6; Kim4, Fig. 2. Either choice would have been obvious and was well known. Additionally, Chen3 teaches that using two etch-stop layers, for example a silicon oxide layer and a high-k dielectric layer, can provide a larger tunneling length to reduce the likelihood of electron tunneling between the conductive layers through the etch-stop layers. Chen3 ¶¶ [0051]-[0053]. This would have motivated a POSA to add an etch-stop layer (*i.e.*, the barrier layer of the '276 Patent) to a design that has a single layer. A POSA would have had a reasonable expectation of success because,

again, these layers were well known and routine and formed using widely used conventional processes.

b. Forming a High-K Dielectric Layer Around a Conductive Gate Layer

The Asserted Claims recite "the gate stack comprising a conductive layer and a first high-k dielectric layer" when the gate stack is formed to replace a sacrificial layer.

Yu3 discloses forming "a barrier layer and/or a tungsten nucleation layer … prior to depositing bulk tungsten," which is the conductive layer. Yu3 ¶ [0041]. A POSA would have understood the "barrier layer" to constitute a gate insulating layer that are deposited on the perimeter of the channel. A POSA would have known that such a gate insulating layer commonly comprises a high-k dielectric material. Furthermore, a POSA would have understood Yu3's process of replacing sacrificial layers with gate stacks to be consistent with the process disclosed by individual Gate-Stack Prior Art, *i.e.*, (1) removing sacrificial layers to form gaps in the stack connected to a substrate opening through which the sacrificial layers are removed; and (2) depositing materials to the gaps through the substrate opening. A POSA would have further known that depositing a gate insulating layer before depositing the conductive gate layers to be a viable and common approach from the Gate-Stack Prior Art. Therefore, a POSA would have been motivated by Yu3's express teaching to adopt this approach, thereby forming a gate insulating layer on the perimeter of the channel as well as the perimeter of the gaps.

A POSA would have had a reasonable expectation of success because Yu3's express disclosure confirms the viability of the added layer around the conductive gate layer, and because this approach was well known in the art.

c. A Sacrificial Layer/Gate Stack over a Dielectric Layer

The Asserted Claims recite "the forming of each step … comprises disposing a sacrificial layer over a dielectric layer" and "replacing the sacrificial layer of each step with a gate stack." Accordingly, the sacrificial layer of each step is disposed above the corresponding dielectric layer during the claimed manufacturing method, and the gate stack of each step is disposed above the corresponding dielectric layer in the semiconductor structure by the end of the claimed method.

Certain Etch-Stop Prior Art, *e.g.*, Fang and Kim4, shows a reverse layer ordering at each step, *i.e.*, sacrificial layer/gate stack on the bottom of each step. Nonetheless, a POSA would have found it obvious that the layer ordering may be flipped to gate stack on top.

Both orders were conventional by the time of the '276 Patent. For example, Kim3 illustrates its staircase structure with a dielectric-layer-on-top configuration. But Kim3 also discloses that the staircase structure may be configured to have sacrificial layer on top at each step. Kim3 ¶¶ [0090]-[0091], [0240]. As another example, Park5 also illustrates its staircase structure with a dielectric-layer-on-top configuration and discloses a sacrificial-layer-on-top configuration. Park5 ¶¶ [0042], [0102]. Yu3 teaches that the layers may be formed in either order. Yu3 ¶¶ [0034]-[0035]. As a final example, Chen3 illustrates both configurations side by side. Chen3, Figs. 7A-7B. At a minimum, these disclosures presenting both orders demonstrate a known technique (a reverse order in which sacrificial layer/gate stack is on top) that is at least a suitable option for the Etch-Stop Prior Art that discloses only a dielectric-layer-on-top configuration. Knowledge of a suitable option itself provides a motivation to modify. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023). Furthermore, since there are only two orders, it would have been obvious to try either order.

As demonstrated by Kim3, Park5, Yu3, and Chen3, a POSA would have known that either order was routine, highly predictable, and would have had a reasonable expectation of success for implementing a gate-stack-on-top embodiment. A POSA would have further known that the deposition and etching processes used to form staircase structures would work for either order. This further contributes to a reasonable expectation of success.

d. A Second High-k Dielectric Layer

Claim 1 recites that "the etch-stop layer comprises a second high-k dielectric layer." To the extent any Etch-Stop Prior Art does not disclose using a high-k dielectric for the etch-stop layer, such usage would have been obvious and within a POSA's knowledge.

For example, Fang discloses a high-k dielectric etch-stop layer. Fang ¶ [0022]. So does Chen3. Chen3 ¶¶ [0023], [0041]. Park5 discloses that the etch-stop layer may comprise the same material as the gate insulating layer, which in turn may comprise aluminum oxide, a high-k

dielectric. Park5 ¶¶ [0061]-[0063], [0092], [0105], [0124]. Kim3 discloses that the etch-stop layer may comprise silicon nitride, which it identifies as a high-k dielectric material. Kim3 ¶¶ [0186], [0064]. Although Micron does not agree with Kim3 that silicon nitride is a high-k dielectric, YMTC's apparent interpretation evidenced by its infringement contentions agrees with Kim3's disclosure. Additionally, Yu3 discloses an etch-stop layer comprising silicon carbide. Yu3 ¶¶ [0006], [0047], [0053]. Silicon carbide is a high-k dielectric, at least under YMTC's apparent interpretation.

A POSA would have known that a high-k dielectric material was a suitable choice for etch-stop layers because the availability of different etchants allows greater flexibility in the choices of materials to use as an etch stop. Knowledge of a suitable option itself provides a motivation to modify. *Intel*, 61 F.4th at 1380. Furthermore, a POSA would have known that a high-k dielectric etch-stop layer could be formed via a conventional deposition process such as CVD, ALD, or PVD. The flexibility in material and the conventional process together would have provided a POSA a reasonable expectation of success in using a high-k dielectric material for an etch-stop layer. Additionally, several Etch-Stop Prior Art references, Park5, Kim4, and Kim3 were all derived from the work at Samsung Electronics Co. Ltd. This would have rendered it obvious that disclosure in one could be applied to another. For example, it would have been obvious to apply Park5's teaching that the etch-stop layer and a gate-insulating layer may comprise the same material to Kim3, which discloses a high-k dielectric gate insulating layer. Kim3 ¶¶ [0151]-[0152].

e. Disposing an Etch-Stop Layer and Forming Openings Therein

Claim 1 recites "disposing an etch-stop layer on each step of the plurality of steps," "forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer," and "etching the exposed portions of the etch-stop layer in the plurality of openings." Claim 1 therefore requires forming a plurality of openings on and through the same etch-stop layer that was deposited on the steps.

Park5 and Kim4 disclose first disposing an etch-stop sacrificial layer, which is subsequently replaced *in situ* with a final etch-stop layer. Park5 ¶¶ [0103]-[0105]; Kim4 ¶¶ [0079]-[0081], [0099]. Other Etch-Stop Prior Art, however, disclose directly disposing an etch-stop layer without

replacing it with a different material. *See, e.g.*, Fang, ¶ [0020]; Kim3 ¶¶ [0173]-[0174], [0185], Yu3 ¶ [0079], [0083]-[0084].

As a specific example, Fang discloses disposing carbon-doped silicon nitride to form an etch-stop layer and disposing silicon nitride to form sacrificial layers. Fang ¶¶ [0020], [0025]. Fang further teaches that, when a phosphorus-based etch chemistry is used, the carbon-doped silicon-nitride etch-stop layer may be preserved when silicon-nitride sacrificial layers are removed. *Id.* ¶ [0025]. Park5's sacrificial layers and final etch-stop layer both comprise silicon nitride. Park5 ¶¶ [0061]-[0063], [0074], [0092], [0105], [0124]. In view of Fang's teaching, by disposing silicon-nitride sacrificial layers and disposing carbon-doped silicon-nitride etch-stop layer in the first instance in Park5's fabrication (*i.e.*, omitting the step of depositing a sacrificial etch-stop layer), the etch-stop layer may be preserved instead of being removed at the same time as the sacrificial layers.

A POSA would have known this approach to be a suitable alternative to Park5's two-step approach because either replacing or not replacing an etch-stop layer, even one of multiple etch-stop layers, was a viable approach. Park5 discloses removing and replacing both of two etch-stop layers. Park5 ¶ [0104]. Kim4 discloses removing and replacing only one (a "preliminary second etch-stop layer") of two etch-stop layers. Kim4 ¶¶ [0101]-[0102], Figs. 16-20. Kim3 discloses not removing and replacing either of its two etch-stop layers. *See* Kim3 ¶¶ [0185]-[0187], [0211]-[0213]. Each of these alternatives represents a known technique that is at least a suitable option for Park5.

Moreover, POSA would have been motivated to adopt Fang's one-step approach to replace Park5's two-step process to simplify manufacturing process and reduce manufacturing cost. A POSA would have had a reasonable expectation of success because directly depositing a final etch-stop layer was a common and routine approach, as demonstrated by the other Etch-Stop Prior Art. Furthermore, Fang discloses analogous alternatives with respect to gate formation. Specifically, Fang discloses both a "replacement gate process," wherein gate stacks are formed through removing and replacing sacrificial layers, and a "floating gate process, where conductive materials are present," *i.e.*, disposed directly during the staircase formation. Fang ¶¶ [0025], [0032], Figs.

1, 7. These alternatives already used to manufacture word-line staircase structures would have further provided a POSA a reasonable expectation of success of using a similar alternative on a different layer, the etch-stop layer, of the structure.

f. Relative Etching Rates

Claims 2, 4, and 5 recite relative etching rates between the etch-stop layer and another layer. To the extent that any Etch-Stop Prior Art, *e.g.*, Chen3, does not explicitly disclose these relative etching rates, a POSA would have understood them to be inherent or obvious for the functioning of an etch-stop layer.

A POSA would have known that the very idea of an etch-stop layer is to slow down etching when etching reaches the layer. This function protects the underlying layers from over-etching. In the context of word-line staircase structures, the etch-stop layer prevents over-etching shallower holes while deeper holes are being etched. To slow down the etching, the etch-stop layer needs to have a lower etching rate than that of the layer above (the insulating layer). Furthermore, for etching to continue by penetrating the etch-stop layer to eventually form contact holes reaching the gate electrode (another necessary condition for the proper functioning of the device), the etch-stop layer needs to have a higher etching rate than that of the layer below so that etching can penetrate the etch-stop layer without penetrating the lower layer. Otherwise the punch-through defect the etch-stop layer is intended to reduce may still occur.

More generally, a layer ("layer 2") functions as an etch-stop layer when its etching rate is lower than that of the layer immediately above ("layer 1"). This is known as selective etching, based on the relative etch selectivity of materials in the layers. It implies that layers 1 and 2 cannot be the same material if layer 2 is to function as an etch-stop layer because the same material will have the same etching rate. Etch selectivity depends on the etchant: layer 1 may have a higher etching rate than layer 2 when one etchant is used, but a lower etching rate when a different etchant is used. These conventional processes were known as "selective etching" and "reverse selective etching." Using different etchants allows greater flexibility in the choices of materials to use as an etch stop, allowing the etch-stop layer to have the necessary etching rate relative to its neighboring layers.

Accordingly, a POSA would have known that the claimed relative etching rates to be inherent in the disclosure of the Etch-Stop Prior Art, whether it is explicitly disclosed. Further, a POSA would have a reasonable expectation of success in selecting etch-stop material and etchants from a flexible array of choices to achieve the required relative etching rates.

Additionally, claim 4 is obvious in view of a POSA's knowledge. In claim limitation [1.F], portions of the etch-stop layer in the openings are etched to expose a portion of the conductive layer of each step. One common approach to this is to extend the etching time to penetrate both the etch-stop layer and the first high-k dielectric layer until the openings reach the conductive layers. *See* Fang ¶ [0029] (disclosing the same regarding etching the etch-stop layer). But since punch-through of gate electrode layers must be prevented, it would have been prudent and obvious to slow down the etching once it reaches the conductive layer. This means that the etch-stop layer has a higher etching rate than an etching rate of the conductive layer of each step. Moreover, because the first high-k dielectric layer is typically very thin, even when that layer is configured to slow down etching to protect the underlying conductive layer, it would have still been desirable to have a conductive layer with low etching rate relative to that of the etch-stop layer for additional protection. Finally, there are only three possible relationships of one etching rate relative to another: higher, equal, or lower. It would have made no sense for the conductive layer to have a higher etching rate than that of the etch-stop layer since the conductive layer should be preserved. Since the two layers have different materials, they do not have equal etching rates. Thus, the only remaining possibility is the relationship recited in claim 4.

Similarly, claim 5 is obvious in view of a POSA's knowledge. Since punch-through of gate electrode layers must be prevented, it would have been desirable to further protect the gate electrode layer in addition to relying on the layer's low etching rate. Accordingly, the first high-k dielectric layer may be advantageously used as an etch stop to protect the conductive layer below. That means that the etch-stop layer has a higher etching rate than an etching rate of the first high-k dielectric layer. Further, only the claimed relative etching rates have a sensible relationship. The two layers do not have equal etching rate since they comprise different materials. And it would not have made sense for the etch-stop layer to have a lower etching rate than that of the first high-k

dielectric layer because the etch-stop layer is thicker and because it is desirable for the first high-k dielectric layer to serve as an etch stop to protect the gate conductive layer when the etch-stop layer is etched.

g. Thickness Range of Etch-Stop Layer

Claim 7 recites a thickness range for the etch-stop layer. Although most Etch-Stop Prior Art references do not disclose the thickness of the etch-stop layer, a POSA would have found the claimed range obvious.

As an initial matter, as the Examiner took official notice during the prosecution of the parent '711 Patent, the claimed etch-stop layer thickness "[wa]s notoriously well known in the art." '711 Patent File History, Oct. 24, 2019 Office Action at 7. Although the '276 Patent claims a smaller range than the '711 Patent, both ranges—spanning two to three orders of magnitude—"lacks criticality." *Id.* This is clear from the laundry list of permissible thicknesses in the specification that the Examiner cited. It is further evidenced by the claims of the parent '711 Patent, where the same range is claimed in claims 10 and 17 for devices with or without a barrier layer (which, again, is another etch-stop layer). Similarly, during the prosecution of the '276 Patent, the Examiner noted that the specification provides a range of 3 orders of magnitude, indicating that the thickness is not critical. '276 Patent File History, Mar. 25, 2021 Office Action at 4-5. Further, no evidence showed that the claimed thickness operates any differently from the prior art. *Id.* at 5. Where, as here, the "[d]ifferences between the prior art and the claimed invention[, if any, is merely] dimensional," not resulting in "differences in performance," the claim is not valid. *Gardner v. TEC Sys., Inc.*, 725 F.2d 1338, 1345-46 (Fed. Cir. 1984).

If more is required (it is not), Fang and Yu3 both disclose a thickness range for an etch-stop layer. Fang's etch-stop layer may have a thickness ranging from about 50 Å to about 1000 Å, or about 5 nm to 100 nm. Fang ¶ [0021]. Yu3's etch-stop layer may have a thickness between about 1 nm to about 250 or 350 nm. Yu3 ¶¶ [0005], [0050]. Both overlaps with the claimed range.

To the extent Fang's or Yu3's disclosed thickness range may be adjusted based on the staircase structure of a particular Etch-Stop Prior Art, such adjustment would have been well within the knowledge and skill of a POSA.

A POSA would have been motivated to apply Fang's or Yu3's disclosure of the etch-stop-layer thickness on a device disclosed in Etch-Stop Prior Art and would have had a reasonable expectation of success to do so.

A POSA would have known that the thickness of an etch-stop layer is at least a necessary (but routine) design parameter and may be important to its purpose of preventing punch-through to underlying layers or shorting between conductive layers in the stack. Thus, for an Etch-Stop Prior Art reference that does not disclose a thickness, a POSA would have been motivated to adapt the etch-stop layer of in view of Fang's or Yu3's thickness range.

A POSA would have understood that the thickness of the etch-stop layer is flexible because other parameters such as the type of etchants or the relative etching rates of the etch-stop and neighboring layers may be adjusted. Accordingly, a POSA would have found the ranges disclosed in Fang and Yu3 to be consistent with expectation. Further, Fang and Yu3 and other Etch-Stop Prior Art disclose analogous semiconductor structures with a conformal etch-stop layer. The respective etch-stop layers comprise similar materials and may be formed using conventional techniques such as CVD or ALD. Fang ¶ [0020]; Yu3 ¶ [0049]. Their disclosures indicate a common and conventional etch-stop layer, which would have lowered any technical barrier for a POSA to adapt a device to the thickness disclosed in Fang or Yu3 and increased the POSA's expectation of success. Further, a POSA would have had a reasonable expectation of success in applying Fang's or Yu3's etch-stop-layer thickness to another Etch-Stop Prior Art because Fang's and Yu3's ranges were reasonable.

h. Repetitive Etch-Trim Process

Claim 12 recites "forming the staircase structure further comprises performing a repetitive etch-trim process on the sacrificial layers and the dielectric layers." To the extent that any Gate-Stack Prior Art does not expressly disclose using such a process to form the staircase structure, a POSA would have known it to be the typical if not an universal process used to form staircase structures.

Indeed, even the Gate-Stack Prior Art that does not explicitly disclose a repetitive etch-trim process contains disclosure that a POSA would have understood to be at least consistent with, if

not indicative of, the use of such a process. For example, Jang1 discloses "forming a mask pattern … on the thin-layer structure 110, and sequentially etching the insulating layers 114a and 114b, the sacrificial layers 112, and the buffer insulating layer 105 by using the mask pattern as an etch mask." Jang1 ¶ [0079]. Since "areas of the gate electrodes EL on the contact region CTR may sequentially decrease as vertical heights of the gate electrodes EL sequentially increase," a POSA would have understood Jang1's sequential etching process to involve a repetitive etch-trim process. *Id.* ¶ [0114]. At the very least, a POSA would have known that such a process was suitable to form staircase structures. *See, e.g.*, Kim3 ¶¶ [0087], [0182]; Park5 ¶ [0080]; Shin ¶ [0084]. Further, a POSA would have had a reasonable expectation of success because such a process was common, routine, and consistent with the existing disclosure of the Gate-Stack Prior Art, *e.g.*, Jang1.

C. Invalidity Based on Section 112 (Patent L.R. 3-3(d))

1. Indefiniteness

Defendants provide the following grounds for invalidity under 35 U.S.C. § 112. Defendants' investigation of the Asserted Patents is ongoing, and Defendants reserve the right to amend or supplement these disclosures based on further investigation and in a manner consistent with the Federal Rules of Civil Procedure, the Local Patent Rules for the Northern District of California, and the Docket Control Order, or otherwise in accordance with any order or direction of this Court or agreement of the parties. Further, Plaintiff's Infringement Contentions fail to provide sufficient detail to fully understand its proposed application of the Asserted Claims, and Defendants reserve the right to assert additional grounds for invalidity under 35 U.S.C. § 112 in response to Plaintiff's claim interpretations. Defendants also reserve the right to supplement, modify, or otherwise amend these grounds for invalidity under 35 U.S.C. § 112 based on the Court's claim construction rulings or opinions or the parties' positions or arguments taken in connection with the claim construction process.

2. Written Description and Enablement

The specification of the '276 Patent does not provide adequate written description to support the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims. 35 U.S.C. § 112(a) requires that a patent specification

contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharm., Inc.*, 598 F.3d at 1351 (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ.*, 541 F.3d at 1122 (quoting *Vas-Cath Inc.*, 935 F.2d at 1563–64). The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Additionally, the Asserted Patents do not enable the claim scopes contained in Plaintiff's Infringement Contentions. Section 112(a) requires a specification to describe "the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention]." The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This "requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp.*, 344 F.3d at 1244 (citation omitted); *see Wyeth & Cordis Corp.*, 720 F.3d at 1385–86. The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Defendants provide below an identification of terms in Asserted Claims that render the Asserted Claims, at least as apparently construed by Plaintiff in its Infringement Contentions as discussed above, invalid pursuant to 35 U.S.C. § 112 as not enabled or lacking sufficient written description:

- "forming a staircase structure having a plurality of steps"
- "disposing an etch-stop layer on each step of the plurality of steps"
- "high-k dielectric layer"
- "wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step" (Claim 4)

XI. INVALIDITY OF THE '941 PATENT

A. Invalidity Based on the Prior Art

As shown below, the alleged inventions of the '941 Patent were well-known in the prior art. Those skilled in the art were aware of all of the limitations claimed in the '941 Patent. Thus, many prior art patents, publications, products, and combinations thereof, disclose, teach, or embody every limitation of the Asserted Claims and thus invalidate those claims. Examples of these disclosures, teachings, and embodiments are identified in the following sections and in the attached claim charts.

1. Identification of Prior Art References (Patent L.R. 3-3(a))

Subject to the reservation of rights above, Defendants identify each item of prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the '941 Patent. The patents/applications, publications, and systems identified are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations.

Some of the below citations and those in the corresponding invalidity claim charts involve prior art references that have corresponding related, foreign, and/or PCT counterpart publications. In such cases, where either the U.S. patent or related, foreign, and/or PCT counterpart is cited, it is to be understood that the corresponding disclosures from the counterpart patent and publications (which are substantively the same) are implicitly incorporated by reference in the alternative to avoid needless repetition.

Exs.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
Q-1	U.S. 2008/0279008 ("Dong I")	May 7, 2007	Nov. 13, 2008
Q-2	U.S. 2008/0159003 ("Dong II")	Dec. 29, 2006	Jul. 3, 2008
Q-3	U.S. 2019/0102104 ("Righetti")	Sep. 29, 2017	Apr. 4, 2019
Q-3	U.S. 2012/0003800 ("Lee 800")	Jul. 2, 2010	Jan. 5, 2012
Q-4, Q-5	U.S. 2018/0190498 ("Lee 498")	Jan. 5, 2017	Jul. 5, 2018
Q-4	U.S. 2018/0012667 ("Costa")	Jul. 7, 2016	Jan. 11, 2018
Q-5	U.S. 2006/0250850 ("Lee 850")	May 6, 2005	Nov. 9, 2006
Q-1, Q-2	U.S. 6,859,397 ("Lutze")	Mar. 5, 2003	Feb. 22, 2005
Q-1, Q-2	U.S. 2012/0163096 ("Futatsuyama")	Dec. 28, 2010	Jun. 28, 2012
Q-3	U.S. 2019/0214405 ("Shirai")	Sep. 21, 2016	Jul. 11, 2019
Q-3	U.S. 10,438,671 ("Chen5")	Jun. 22, 2018	Oct. 8, 2019

Table Q-1: Prior Art Patents and Patent Publications for the '941 Patent

Ex.	Title	Authors	Publisher	Date of Publication
§XI.A.3.[19]	"NAND Flash Memory Technologies" ("Aritome")	Aritome		2016

Table Q-2: Prior Art Non-Patent Publications for the '941 Patent

Defendants are still investigating prior uses and sales. Based upon at least Plaintiff's apparent position as to the scope of the Asserted Claims, and as further explained below and in the cited exhibits, it appears that the following systems (and development thereof) qualify as prior art under at least one or more of 35 U.S.C. § 102(a):

Ex.	Description	Entities Involved	Prior Art Date
Q-6	120 Series Products	Micron	1/11/2018

Table Q-3: Prior Art Systems for the '941 Patent

Micron's 120 series products were publicly available, on sale, or in public use prior to the effective filing date of the '941 Patent. MYM0042611-MYM0042676, MYM0042896-MYM0042896, MYM0065110, MYM0065111. B27A PR20 was released April 18, 2018. *See* MYM0069818, MYM0069871.

Description	Availability
Travelers	to be made available via inspection
Process information	to be made available via inspection
Schematics	to be made available via inspection
Layouts	to be made available via inspection
Waveforms	MYM0042897-MYM0043247, MYM0069190-MYM0069236
TEM/SEM Imagery	MYM0043255-MYM0043296,

[19] *See* §XI.A.3. The equivalent of a chart is set forth with pinpoint citations to the reference in the motivation to combine sections.

Description	Availability
	MYM0043316-MYM0043339, MYM0043423-MYM0043424, MYM0043248-MYM0043254, MYM0058880-MYM0058891, MYM0069181-MYM0069181
Datasheets	MYM0043425-MYM0043844, MYM0065164-MYM0066151
Trim Spreadsheets	MYM0065112-MYM0065115, MYM0069182-MYM0069189, MYM0069715-MYM0069940

Table Q-4: Listing of Prior Art Systems Documentation for the '941 Patent

2. Anticipation and Obviousness (Patent L.R. 3-3(b) and (c))

The Asserted Claims of the '941 Patent are invalid because they are anticipated by the prior art and/or because they would have been obvious in view of the prior art.

The prior art identified by Defendants anticipates and/or renders obvious one or more of the Asserted Claims of the '941 Patent under at least AIA §§ 102(a)(1), 102(a)(2), and 103. For each prior art reference, Defendants have provided claim charts attached to these Invalidity Contentions as Exhibits Q-1 through Q-6. These charts identify where each element of each Asserted Claim can be found in each item of prior art.

Again, to the extent not anticipated, the Asserted Claims of the '941 Patent are invalid as obvious under 35 U.S.C. § 103. Each prior art reference identified in the preceding sections—either alone or in combination with another prior art reference and/or in combination with the knowledge of one skilled in the art—renders the Asserted Claims invalid as obvious. In rendering the Asserted Claims obvious, each prior art reference identified in the preceding sections may be combined with:

(1) information known to persons skilled in the art at the time of the alleged invention, (2) any of the other anticipatory or obviousness prior art references, (3) any statements in the intrinsic record of the '941 Patent and related applications, or (4) any of the additional prior art identified below.

3. Motivations to Combine[20]

A person of ordinary skill in the art would have been motivated to combine the preceding references (*see* Section XI.A.1) for the following reasons. Teachings, suggestions, motivations and/or reasons to modify any of the references and/or to combine any two or more of the references can come from many sources, including the prior art (by specific reference and when read as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obviousness to try, the nature of the problem faced, and/or knowledge possessed by a person of ordinary skill.

Although a patent claim may be invalidated based on a teaching-suggestion-motivation ("TSM") rationale—*i.e.,* that some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention—the Supreme Court identified additional rationales in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007). The following of these rationales apply here:

(A) the asserted claims combine prior art elements according to known methods to yield predictable results;

(B) the asserted claims involve the simple substitution of one known element for another to obtain predictable results;

(C) the asserted claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;

(D) the asserted claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) the asserted claims involve combinations of prior art references that would have been "obvious to try"'—a person of ordinary skill in the art could have reached the asserted claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

[20] The statements in this section about what was known and obvious to a POSA are made with respect to the effective filing date of the '941 Patent.

(F) the asserted claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach); *see also* Department of Commerce, Patent and Trademark Office, Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.,* 72 Fed. Reg. 57,526 (Oct. 10, 2007). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420-21.

Thus, even in the absence of a specific teaching, suggestion, or motivation to combine references, the Asserted Claims here are obvious and therefore invalid. Each of the cited references or devices is in the same field as the '941 Patent, making it obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. One of ordinary skill in the art would have recognized that improvements could be achieved by combining or modifying prior art references that described such improvements. Each of the above prior art references describes systems, products, or methods that were known to offer such improvements, and, accordingly, one of ordinary skill in the art would have been motivated to combine or modify the references as identified in each of the combinations below.

Furthermore, because each prior art reference concerns three-dimensional NAND memory designs or general methods of operation relevant to both two- and three-dimensional NAND, common industry knowledge supplied a reason to combine any one the above references. It was well understood that different three-dimensional NAND memory structural features and two- or three-dimensional NAND memory methods of operations could be employed together or interchanged with each other, fitting together like puzzle pieces. Each combination would have produced predictable results and would simply represent a known alternative to one of ordinary skill in the art of NAND memory. This is a further motivation to combine any of the above

references.

The below sections further address particular reasons to combine the above references. The below should not be construed as an admission that there is any value to the alleged invention of the '941 Patent. As discussed previously, these contentions are based in significant part on how Plaintiff is apparently construing the asserted claim in its Infringement Contentions, which is an incorrect and overbroad interpretation of the alleged invention of the '941 Patent. Accordingly, to the extent the below refers to benefits of certain elements or industry trends towards these elements, this is not an admission that the alleged invention of the '941 Patent provides any benefits: to the contrary, properly construed and compared to the prior art, the '941 Patent provides no benefits. Likewise, to the extent the below refers to substituting elements, this is not an admission that the elements subject to the substitution are in any way similar, *e.g.,* perform the same function, in the same way, to achieve the same result.

The various elements of the Asserted Claims were well known in the prior art at the time of the alleged invention, and the combination would have been obvious to one of skill in the art. The combinations simply (a) combine prior art elements according to known methods to yield predictable results; (b) involve the simple substitution of one known element for another to obtain predictable results; (c) involve the use of a known technique to improve similar devices (methods, or products) in the same way; (d) apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) involves combinations of prior art references that would have been "obvious to try" – a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and/or (f) would have been prompted by known work, based on design incentives or other market forces, because such variations were predictable to one of ordinary skill in the art.

Moreover, the Supreme Court has stated that a motivation to combine may be simply "common sense" and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420. Indeed, the Supreme Court held that it is

sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421. Here, all the claim elements are common sense and are easily fit together by one of ordinary skill in the art.

While not necessary, a motivation to combine may also be found in the references themselves. One of skill in the art would have been motivated to combine a reference that refers to, or otherwise explicitly invites combination with, another reference. Where the references cited herein have such an explicit invitation to combine, that invitation would have motivated one of skill in the art to combine any such references.

Micron hereby identifies the following '941 Patent Primary References: Dong I, Dong II, and Micron 120 Series Products.

The below provides several exemplary combinations and motivations for combining an '941 Patent Primary Reference with another reference.

a. Two Deck Teachings

Asserted Claims of the '941 Patent recite a "dummy word line[s]" and a "joint oxide layer" as part of a "two-deck structure." *See* '941 Patent claims 4, 10, and 14. The usage of such a two-deck structure was routine in the prior art and well known and understood by a POSA by the time of the filing of the '941 Patent. *See, e.g.*, Righetti, [0002], [0017]-[0032], [0048], Fig. 1; Lee 800, Abstract, [0005]-[0010], [0100]-[0106], [0134]-[0139], [0173]-[0178], [0222]-[0227], [0243]-[0258], Figs. 15-17, 27-28, 41, 54, 57-58, 60; Shirai, [0003], [0014], [0030]-[0042], Figs. 2, 5A-15; Chen5, 4:10-57, Figs. 6, 16A-16G. The prior art cited in this paragraph, and the prior art for which the corresponding claim charts provide teachings of the two deck teachings will be referred to as "Two Deck Art."

To the extent any of the '941 Patent Primary References are argued or shown to not disclose the two-deck structure as claimed in the '941 Patent, a POSA would have been motivated to combine the reference with any one, or several of, the Two Deck Art references.

For example, a POSA would have been motivated and considered it obvious to include a two-deck structure because it would have improved the yield and profitability of the memory devices. There was and still is a relentless demand for increased memory capacity at lower cost per bit, which may be achieved by longer 3D NAND memory strings. Aritome, "NAND Flash Memory Technologies" (2016) ("Aritome"), 292-295. However, it was well known that as memory chips becomes denser and require an increasing number of layers, it becomes increasingly difficult to etch straight holes. *See, e.g.*, Shirai, [0003] (when "manufacturing [3D NAND memory devices], holes are formed in a stacked body including multiple conductive layers. As the number of stacked layers in the stacked body increases, it becomes difficult to collectively form the holes."), [0042]. By using multiple decks stacked on each other the memory chips may include more memory cells per string without hurting product yield by increasing manufacturing difficulty. This would increase memory density and reduce cost, increasing profit. *See, e.g.*, Lee 800, [0002]-[0004] (desirable to be able to reliably fabricate memory with increasingly lower cost per bit), [0089]-[0093], Figs. 7-10 (showing and discussing how a lower deck layer may be etched first and then an upper deck layer may be added and then later etched, reducing the depth needed to etch through the two decks stacked together); Shirai, Figs. 2, 7A-15, [0042], [0003] ("A method has been proposed in which holes can be easily formed even in a stacked body having a large number of stacked layers by repeating formation of the holes and formation of the stacked body (stacked portion).").

Furthermore, a POSA would have also had a reasonable expectation of success in combining the teachings of the Two Deck Art with other teachings because the fabrication of multiple decks simply requires repeating the same fabrication steps for one deck, which was clearly known and understood by the POSA to fabricate memory chips such as those disclosed in the '194 Patent Primary References. *See, e.g.*, Lee 800, [0087]-[0144], Figs. 4-19 (describing and showing the steps of fabricating a two deck memory structure which largely consists of fabricating one deck then repeating similar steps for a second deck layered on top); Righetti, [0029]-[0030] (discussing that decks may simply be formed on top of one another to make a structure with "any number of decks" by using a "[s]imilar process … repeated for additional decks"); Shirai, Figs. 5A-15, [0005], [0042], [0074], [0003] ("A method has been proposed in which holes can be easily formed even in

a stacked body having a large number of stacked layers by repeating formation of the holes and formation of the stacked body (stacked portion)."); Chen5, Figs. 6 and 16, 4:10-32 ("The memory hole is etched separately in each tier so that a low aspect ratio can be achieved."), 14:64-15:25.

b. Pass Voltage Under the Program Cell Increase as the Cell Being Programmed Moves up the Stack ("Increasing Pass Voltage Teachings")

Asserted Claims of the '941 Patent recite increasing "the first voltage" as the "xth word line" moves up the stack from the "first portion," to the "second portion," and to the "third portion." *See* '941 Patent claims 8, 9. Increasing the voltage applied to lines under the program cell line existed in the prior art and was well known and understood by a POSA by the time of the filing of the '941 Patent. *See, e.g.*, Lee 498, [0007]-[0010], [0151]-[0163], Figs. 14-16, 18-20; Costa, [0029]-[0035], [0105]-[0116], [0138]-[0148], Figs. 8-9B, 12A-12H. The prior art cited in this paragraph, and the prior art for which the corresponding claim charts provide teachings of the two deck teachings will be referred to as "Increasing Pass Voltage Art."

To the extent any of the '941 Patent Primary References are argued or shown to not disclose increasing the first voltage as claimed in the '941 Patent, a POSA would have been motivated to combine the reference with any one, or several of, the Increasing Pass Voltage Art references.

For example, a POSA would have been motivated and considered it obvious to increase the pass voltage applied to lines under the program cell line in the manner claimed by the '941 Patent because it would have "improve[d] the reliability of a program operation of the memory device" by suppressing "variation in the threshold voltages of programmed memory cells … and a program disturb phenomenon may be reduced. Lee 498, [0007], [0163], [0185]. Because of this "the reliability of the program operation of the memory device may be improved." *Id.*, [0163]. Furthermore, a POSA would have understood that "channel resistance increases as each memory cell is programmed, leading to the highest resistance and lowest channel conductance when programming the later programmed memory cells of the group." Costa, [0029]. This can cause issues including that the "increased channel resistance when programming the later programmed memory cells may cause them to be programmed to higher levels than intended" and introduces "potential read errors." *Id.*, [0029], [0101]. But the issue can be "compensate[d]" for by increasing

"pass voltage applied to [a] subset of memory cells … as programming progresses." Costa, [0030]; *see also id.*, [0104].

Furthermore, a POSA would have also had a reasonable expectation of success in combining the teachings of the Increasing Pass Voltage Art with other teachings because integration of these teachings would have required no structural modification to the '941 Patent Primary References and instead are simply a trivial modification to the operation of the memory chips to change the voltage levels applied to some of the word lines. Specifically, the Increasing Pass Voltage Art states that they relate to the operation of memory devices, rather than the structure or construction of the devices. Lee 498, [0002]-[0010]; Costa, [0028]-[0035]. Furthermore, the Increasing Pass Voltage Art shows that its method of operation may be applied to both memory "hav[ing] a two-dimensional (2D) structure" and memory constructed using a "three-dimensional (3D) structure," confirming that the teachings would be applicable to the memory devices disclosed in the '941 Patent Primary References. Lee 498, [0006], [0044], [0114]. The Increasing Pass Voltage Art explicitly states that a POSA would have recognized that these methods of operation are "not limited to a single specific memory structure, but covers many relevant memory structures." Costa, [0050]. Thus, a POSA would have understood that these teachings from the Increasing Pass Voltage Art may be applied to the '941 Patent Primary References just as readily as they were applied to the exemplary memory of the Increasing Pass Voltage Art.

c. V4 Pass Voltage Applies to Multiple Wordlines and is Greater Than V5, and V5 is Greater than V6 ("V4-V6 Pass Voltage Teachings")

Asserted Claims of the '941 Patent recite a "fourth voltage" applied to multiple wordlines, and in some claims the fifth voltage is lower than the fourth voltage. *See* '941 Patent claims 1, 6, 7, 11. As an obvious extension of this (i.e., the application of a lower voltage to word lines further down the stack as compared to the voltage applied to lines further up the stack), Asserted Claims of the '941 Patent recite a "six[th] voltage" applied is lower than a "fifth voltage." *See* '941 Patent claims 2, 12. The usage of a voltage applied to multiple lines where that voltage is higher than a voltage applied to word lines further down the structure existed in the prior art and was well known and understood by a POSA by the time of the filing of the '941 Patent. *See, e.g.*, Lee 498, [0151]-

[0163], Figs. 18, 20; Lee 850, [0041]-[0062], Figs. 4-10. The prior art cited in this paragraph, and the prior art for which the corresponding claim charts provide teachings of the two deck teachings will be referred to as "V4-V6 Pass Voltage Art."

To the extent any of the '941 Patent Primary References are argued or shown to not disclose the fourth voltage as claimed in the '941 Patent, a POSA would have been motivated to combine the reference with any one, or several of, the V4-V6 Pass Voltage Art references.

For example, a POSA would have been motivated and considered it obvious to include a fourth voltage applied to multiple lines, including the situation where the fourth voltage is greater than a fifth voltage further down the structure, and extended this to including a sixth voltage further down the stack which is even lower voltage than the fifth voltage, because it would have "improve[d] the reliability of a program operation of the memory device" by suppressing "variation in the threshold voltages of programmed memory cells … and a program disturb phenomenon may be reduced. Lee 498, [0007], [0163], [0185]. Because of this "the reliability of the program operation of the memory device may be improved." Lee 498, [0163]; *see also* Lee 850, [0033], [0063]-[0064].

Furthermore, a POSA would have also had a reasonable expectation of success in combining the teachings of the V4-V6 Pass Voltage Art with other teachings because integration of these teachings would have required no structural modification to the '941 Patent Primary References and instead are simply a trivial modification to the operation of the memory chips to change the voltage levels applied to some of the word lines. Specifically, the V4-V6 Pass Voltage Art states that they relate to the operation of memory devices, rather than the structure or construction of the devices. Lee 498, [0002]-[0010]; Lee 850, Abstract, [0002], [0018]-[0020]. Furthermore, the V4-V6 Pass Voltage Art shows that its method of operation may be applied to both memory "hav[ing] a two-dimensional (2D) structure" and memory constructed using a "three-dimensional (3D) structure," confirming that the teachings would be applicable to the memory devices disclosed in the '941 Patent Primary References. Lee 498, [0006], [0044], [0114]; *see also* Lee 850, [0060]. Thus, a POSA would have understood that these teachings from the V4-V6 Pass

Voltage Art may be applied to the '941 Patent Primary References just as readily as they were applied to the exemplary memory of the V4-V6 Pass Voltage Art.

B. Invalidity Based on Section 112 (Patent L.R. 3-3(d))

1. Indefiniteness

Defendants provide the following grounds for invalidity under 35 U.S.C. § 112. Defendants' investigation of the Asserted Patents is ongoing, and Defendants reserve the right to amend or supplement these disclosures based on further investigation and in a manner consistent with the Federal Rules of Civil Procedure, the Local Patent Rules for the Northern District of California, and the Docket Control Order, or otherwise in accordance with any order or direction of this Court or agreement of the parties. Further, Plaintiff's Infringement Contentions fail to provide sufficient detail to fully understand its proposed application of the Asserted Claims, and Defendants reserve the right to assert additional grounds for invalidity under 35 U.S.C. § 112 in response to Plaintiff's claim interpretations. Defendants also reserve the right to supplement, modify, or otherwise amend these grounds for invalidity under 35 U.S.C. § 112 based on the Court's claim construction rulings or opinions or the parties' positions or arguments taken in connection with the claim construction process.

2. Written Description and Enablement

The specification of the '941 Patent does not provide adequate written description to support the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims. 35 U.S.C. § 112(a) requires that a patent specification contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharm., Inc.*, 598 F.3d at 1351 (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ.*, 541 F.3d at 1122 (quoting *Vas-Cath Inc.*, 935 F.2d at 1563–64). The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Additionally, the Asserted Patents do not enable the claim scopes contained in Plaintiff's Infringement Contentions. Section 112(a) requires a specification to describe "the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention]." The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This "requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp.*, 344 F.3d at 1244 (citation omitted); *see Wyeth & Cordis Corp.*, 720 F.3d at 1385–86. The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Defendants provide below an identification of terms in Asserted Claims that render the Asserted Claims, at least as apparently construed by Plaintiff in its Infringement Contentions as discussed above, invalid pursuant to 35 U.S.C. § 112 as not enabled or lacking sufficient written description:

- "[first/second/third] portion" (Claims 1-5, 7-14)
- "[first/second/third/fourth/fifth/six/sixth] voltage" (Claims 1-3, 5-9, 11-13)
- "bottom to top" / "below" (Claims 1-2, 4-5, 7, 10-12, 14)
- "(m+1)th word line to an nth word line" / "a (k+1)th word line to an mth word line" / "an (x+2)th word line to the nth word line" / "an (x+1)th word line" / "an (x−1)th word line" / "the (m+1)th word line to an (x−2)th word line" / "an xth word line is used to perform a program operation" / "$0 \leqslant k < m$, $(m+2) < x < (n-1)$" / "$1 < k < m$ and $3 \leqslant x$" / "first word line to an (x−2)th word line" (Claims 1, 5, 11)
- "the controller is further configured to apply a six voltage to the first word line to the kth word line when the xth word line is used to perform the program operation, $0 \leqslant k$, and the sixth voltage is lower than the fifth voltage." (Claim 2)
- "applying a six voltage to the first word line to the kth word line" (Claim 12)
- "the sixth voltage is lower than the fifth voltage" (Claims 2 and 12)

XII. INVALIDITY OF THE '164 PATENT

A. Invalidity Based on the Prior Art

As shown below, the alleged inventions of the '164 Patent were well-known in the prior art. Those skilled in the art were aware of all of the limitations claimed in the '164 Patent. Thus, many prior art patents, publications, products, and combinations thereof, disclose, teach, or embody every limitation of the Asserted Claims and thus invalidate those claims. Examples of these disclosures, teachings, and embodiments are identified in the following sections and in the attached claim charts.

1. Identification of Prior Art References (Patent L.R. 3-3(a))

Subject to the reservation of rights above, Defendants identify each item of prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the '164 Patent. The patents/applications, publications, and systems identified are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations.

Some of the below citations and those in the corresponding invalidity claim charts involve prior art references that have corresponding related, foreign, and/or PCT counterpart publications. In such cases, where either the U.S. patent or related, foreign, and/or PCT counterpart is cited, it is to be understood that the corresponding disclosures from the counterpart patent and publications (which are substantively the same) are implicitly incorporated by reference in the alternative to avoid needless repetition.

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
R-1	JP2006-093598 ("Yoshinaga")	Sep. 27, 2004	Apr. 6, 2006
R-3	U.S. 5,821,804 ("Nikutta")	Apr. 6, 1995	Oct. 13, 1998
R-4	U.S. 9,070,700 ("Haralabidis")	Nov. 4, 2011	Jun. 30, 2015
R-5	U.S. 2007/0215994 ("Beauchamp")	Jul. 31, 2002	Sep. 20, 2007
R-6	U.S. 2004/0140860 ("Miller")	Feb. 25, 1999	Jul. 22, 2004
R-7	U.S. 7,880,310 ("Mathew")	Sep. 28, 2007	Feb. 1, 2011
R-8	U.S. 6,097,098 ("Ball")	Feb. 14, 1997	Aug. 1, 2000
R-9	U.S. 9,947,651 ("Toba")	Dec. 19, 2008	Apr. 17, 2018
R-10	JP2008-311589 ("Kinugasa")	Jun. 18, 2007	Dec. 25, 2008
R-11	U.S. 8,194,373 ("Padden")	Jul. 30, 2007	Jun. 5, 2012
See IPR	U.S. 6,144,542 ("Ker")	Dec. 15, 1998	Nov. 7, 2000

Table R-1: Prior Art Patents and Patent Publications for the '164 Patent

Ex.	Title	Authors	Publisher	Date of Publication
R-2	IC Mask Design: Essential Layout Techniques ("Saint")	Christopher Saint & Judy Saint	McGraw-Hill Professional Engineering	2002

Table R-2: Prior Art Non-Patent Publications for the '164 Patent

Defendants are still investigating prior uses and sales. Based upon at least Plaintiff's apparent position as to the scope of the Asserted Claims, and as further explained below and in the cited exhibits, it appears that the following systems (and development thereof) qualify as prior art under at least one or more of 35 U.S.C. § 102(a):

Ex.	Description	Entities Involved	Prior Art Date
R-12	Z11M	Micron	2017
R-13	Z1AM	Micron	2017
R-13	Z2BM	Micron	2017

Table R-3: Prior Art Systems for the '164 Patent

Micron's Z11M, Z1AM, and Z2BM products were publicly available, on sale, or in public use prior to the effective filing date of the '164 Patent. *See* Prior Art sales spreadsheets and invoices.

Description	Availability
Schematics	to be made available via inspection, YMTC-MSC_0001-YMTC-MSC_0010
Layouts	to be made available via inspection
Design Review	MYM0069941-MYM0069958

Table R-4: Listing of Prior Art Systems Documentation for the '164 Patent

2. Anticipation and Obviousness (Patent L.R. 3-3(b) and (c))

The Asserted Claims of the '164 Patent are invalid because they are anticipated by the prior art and/or because they would have been obvious in view of the prior art.

The prior art identified by Defendants anticipates and/or renders obvious one or more of the Asserted Claims of the '164 Patent under at least AIA §§ 102(a)(1), 102(a)(2), and 103. For each prior art reference, Defendants have provided claim charts attached to these Invalidity Contentions as Exhibits R-1 through R-13. These charts identify where each element of each Asserted Claim can be found in each item of prior art. In addition to the above identified claims charts, Micron hereby incorporates by reference IPR2025-00118 filed with the United States Patent and Trademark Office on November 14, 2024.

Again, to the extent not anticipated, the Asserted Claims of the '164 Patent are invalid as obvious under 35 U.S.C. § 103. Each prior art reference identified in the preceding sections—either alone or in combination with another prior art reference and/or in combination with the knowledge of one skilled in the art—renders the Asserted Claims invalid as obvious. In rendering the Asserted Claims obvious, each prior art reference identified in the preceding sections may be combined with: (1) information known to persons skilled in the art at the time of the alleged invention, (2) any of the other anticipatory or obviousness prior art references, (3) any statements in the intrinsic record of the '164 Patent and related applications, or (4) any of the additional prior art identified below.

3. Motivations to Combine[21]

A person of ordinary skill in the art would have been motivated to combine the preceding references (*see* Section XII.A.1) for the following reasons. Teachings, suggestions, motivations and/or reasons to modify any of the references and/or to combine any two or more of the references can come from many sources, including the prior art (by specific reference and when read as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obviousness to try, the nature of the problem faced, and/or knowledge possessed by a person of ordinary skill.

Although a patent claim may be invalidated based on a teaching-suggestion-motivation ("TSM") rationale—*i.e.,* that some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference

[21] The statements in this section about what was known and obvious to a POSA are made with respect to the effective filing date of the '164 Patent.

teachings to arrive at the claimed invention—the Supreme Court identified additional rationales in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007). The following of these rationales apply here:

> (A) the asserted claims combine prior art elements according to known methods to yield predictable results;
>
> (B) the asserted claims involve the simple substitution of one known element for another to obtain predictable results;
>
> (C) the asserted claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;
>
> (D) the asserted claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;
>
> (E) the asserted claims involve combinations of prior art references that would have been "obvious to try"'—a person of ordinary skill in the art could have reached the asserted claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
>
> (F) the asserted claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach); *see also* Department of Commerce, Patent and Trademark Office, Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.,* 72 Fed. Reg. 57,526 (Oct. 10, 2007). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420-21.

Thus, even in the absence of a specific teaching, suggestion, or motivation to combine references, the Asserted Claims here are obvious and therefore invalid. Each of the cited references or devices is in the same field as the '164 Patent, making it obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. One of ordinary skill in the art would have recognized that improvements could be achieved by combining or modifying prior art references that described such improvements. Each of the above prior art references

describes systems, products, or methods that were known to offer such improvements, and, accordingly, one of ordinary skill in the art would have been motivated to combine or modify the references as identified in each of the combinations below.

Furthermore, because each prior art reference concerns integrated circuit designs involving the use of ESD circuitry, common industry knowledge supplied a reason to combine any one the above references. It was well understood that different integrated circuit and ESD structural features could be employed together or interchanged with each other, fitting together like puzzle pieces. Each combination would have produced predictable results and would simply represent a known alternative to one of ordinary skill in the art of integrated circuit design. This is a further motivation to combine any of the above references.

The below sections further address particular reasons to combine the above references. The below should not be construed as an admission that there is any value to the alleged invention of the '164 Patent. As discussed previously, these contentions are based in significant part on how Plaintiff is apparently construing the asserted claim in its Infringement Contentions, which is an incorrect and overbroad interpretation of the alleged invention of the '164 Patent. Accordingly, to the extent the below refers to benefits of certain elements or industry trends towards these elements, this is not an admission that the alleged invention of the '164 Patent provides any benefits: to the contrary, properly construed and compared to the prior art, the '164 Patent provides no benefits. Likewise, to the extent the below refers to substituting elements, this is not an admission that the elements subject to the substitution are in any way similar, *e.g.,* perform the same function, in the same way, to achieve the same result.

The various elements of the Asserted Claims were well known in the prior art at the time of the alleged invention, and the combination would have been obvious to one of skill in the art. The combinations simply (a) combine prior art elements according to known methods to yield predictable results; (b) involve the simple substitution of one known element for another to obtain predictable results; (c) involve the use of a known technique to improve similar devices (methods, or products) in the same way; (d) apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) involves combinations of prior art references

that would have been "obvious to try" – a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and/or (f) would have been prompted by known work, based on design incentives or other market forces, because such variations were predictable to one of ordinary skill in the art.

Moreover, the Supreme Court has stated that a motivation to combine may be simply "common sense" and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420. Indeed, the Supreme Court held that it is sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421. Here, all the claim elements are common sense and are easily fit together by one of ordinary skill in the art.

While not necessary, a motivation to combine may also be found in the references themselves. One of skill in the art would have been motivated to combine a reference that refers to, or otherwise explicitly invites combination with, another reference. Where the references cited herein have such an explicit invitation to combine, that invitation would have motivated one of skill in the art to combine any such references.

Micron hereby identifies the following '164 Patent Primary References: Yoshinaga, Saint, Nikutta, Micron Z11M Product, Micron Z1AM Product, and Micron Z2BM Product.

The below provides several exemplary combinations and motivations for combining an '164 Patent Primary Reference with another reference.

a. Bonding Wires

Asserted Claims of the '164 Patent recite "bonding wires" bonded between pads or pad groups and other pads or pad groups or between pads or pad groups and a common ESD bus. Usage of bonding wires was routine in the prior art and well understood by a POSA by the time of the filing of the '164 patent, whether the bonding wires are being used to bond pads or bond pad groups

to other pads or pad groups, pads to package pins or package pads, or pads to other interconnects or which may act as a common bus. *See, e.g.*, Haralabidis, 1:50-2:4, 2:31-41, Figs. 1, 3-5 (discussing the use of wire bonds); Beauchamp, Abstract, [0007], [0027]-[0030], [0034]-[0036], Figs. 1-8 (showing and discussing using a single bond wire bonded between one or more die bond pads); Miller, Abstract, Figs. 1, 4, 7, 10, 13-15 (showing and discussing contact pads connected to each other or other elements using bond wires); Mathew, 6:67-7:7 (discussing using wire bonding by bonding to conductive elements such as conductive pillars); Ball, 2:17-40, Figs. 6, 6A, 6B (discussing interconnecting bond pads on a single integrated circuit die and showing bond wires connecting pads); Saint, 162, 202-211, 337, Figs. 7-7, CS1-97 (discussing and showing usage of bond wires to connect to bond pads on a chip and discussing how common was the use of bond wires); Toba, Fig. 1, 4:55-59 (discussing usage of bonding wires to couple pads of an integrated circuit); Kinugasa, ¶¶8-10, 28-31, Figs. 1, 2 (discussing and showing how pads of integrated circuits may be connected using wires). The prior art cited in this paragraph, and the prior art for which the corresponding claim charts provide teachings of bonding wires will be referred to as "Bonding Wire Art."

To the extent any of the '164 Patent Primary References are argued or shown to not disclose bonding wires bonded between pads or pad groups, or between pads or pad groups and a common ESD bus, a POSA would have been motivated to combine the reference with any one, or several of, the Bonding Wire Art references.

For example, a POSA would have been motivated and considered it obvious to use bonding wires to form connections between IC pads or pad groups, or between pads or pad groups and a common ESD bus. Yoshinaga and Nikutta both include pads which are shown in respective figures to be connected to reference potential lines (Yoshinaga, Figs. 1-4) and supply potential lines (Nikutta, Figs. 4-5). A POSA would have recognized that although these connections are shown neither Yoshinaga or Nikutta shows how the connections are made. A POSA would have been encouraged to form the connections using bonding wires because it was known that bonding wires was an extremely common method of forming connections involving pads as well as providing a way to "fuse[] the wire to the bond pad" resulting in "firmly attach[ed]" connections. Saint, 204. A

POSA would have been further motivated to use bond wires because they were known to "create[] a low resistance connection" Beauchamp, [0027].

Furthermore, a POSA would have also had a reasonable expectation of success in combining the teachings of the Bonding Wire Art with other teachings because wire bonding was the "most common method of attaching a chip to a package." Saint, 207. Thus, a POSA would have been well acquainted and well understood how to apply bonding wires when making connections involving pads or pad groups. Also, the same techniques for connecting one end of a wire bond to a pad would apply to the other end, so a POSA would have had a high expectation of success in forming connections between pads or pad groups, or pads or pad groups and an ESD bus. *See* Miller, Figs. 7, 10, 13, Abstract; Mathew, 6:67-7:7; Beauchamp, [0007], [0027]-[0030], [0034]-[0036], Figs. 4-6 (discussing connecting two bond pads); Ball, 6:57-7:19, Figs. 4-6B; Toba, 4:55-59; Kinugasa, ¶¶8-10, 28-31, Figs. 1, 2.

b. Saved Area

Asserted Claims of the '164 Patent recite "at least one saved area." Inclusion of one or more saved areas in integrated circuits was common in the prior art and a concept well understood by a POSA by the time of the filing of the '164 patent. *See, e.g.*, Yoshinaga, Fig. 6 (showing space between pads, power supply lines, and reference potential lines); Saint, 162, 213, 220-221, Figs. 7-7, 9-21, 9-28 (discussing and showing how chip space can be more efficiently used if "wasted" space between IC pads near the edges of the chip is also used for circuitry); Nikutta, Fig. 5 (showing space between pads, local potential bars which may include circuitry). The prior art cited in this paragraph, and the prior art for which the corresponding claim charts providing teachings of saved area will be referred to as "Saved Area Art."

To the extent any of the '164 Patent Primary References are argued or shown to not disclose saved area, a POSA would have been motivated to combine the reference with any one, or several of, the Saved Area Art references.

For example, a POSA would have been motivated and considered it obvious to include saved area. '164 Patent Primary References teach that it is desirable to "keep[] the chip size as small as possible." Yoshinaga, [0084], [0086]. The references disclosing saved area indicate that

the inclusion of saved area can act to shrink the size of the chip, and allows for better utilization of the chip space by using what would otherwise be "wasted space around the edges between the pads." Saint, 220-221. Thus, a POSA would have recognized that it would be advantageous to apply the saved area teachings from the Saved Area Art in order to reduce the size of the chip and make most efficient use if the space available on the chip.

Furthermore, a POSA would have also had a reasonable expectation of success in combining the teachings of the Saved Area Art with other teachings. First, the '164 Patent Primary References disclose space between bond pads and ESD buses which is either shown to be unused or explicitly shown to include circuitry. Yoshinaga, Fig. 6; Nikutta, Fig. 5; Saint, 221, Fig. 9-28. The Saved Area Art teaches placing circuitry in the saved spaces. Saint, 221, Fig. 9-28; Nikutta, Fig. 5. Each of the Saved Area Art references deal with the floorplanning and placement of components on integrated circuits and a POSA would have known that the teachings from these references may be applied successfully to the integrated circuits of the '164 Patent Primary References. Saint, 156-175, 221, Fig. 9-21; Nikutta, Fig. 5; Yoshinaga, Fig. 6.

c. Common ESD Bus

Asserted Claims of the '164 Patent recite a "common ESD bus" which may be "adjacent to the plurality of pad groups," connected to the "plurality of pad groups," comprise a "plurality of discontinuous ESD bus groups," be "outside the plurality of chip edges or inside the plurality of chip edges," and/or "parallel to the plurality of ESD buses." Use of common ESD buses was routine in the prior art and well understood by a POSA by the time of the filing of the '164 patent. *See, e.g.*, Haralabidis, 1:59-2:4, 2:31-41, 3:9-33, 3:65-5:41, Figs. 1, 3, 5 (discussing and showing a common ground rail and connection thereto in various formats including in segments); Saint, 160-163, 202-212, 221, 337, 344, Figs. 7-6, 7-7, 9-19, 9-20, 9-28, CS1-97, CS1-99 (discussing and showing ground or reference voltage buses and about ESD Ground Wiring including a continuous ring around active circuitry and wire bonding to bond pads); Nikutta, Figs. 4-5 (showing local potential bars and supply potential bars as a part of integrated semiconductor circuit and layout); Padden, 1:35-2:2, 4:3-45, Fig. 1-3 (showing and describing the usage of a common voltage supply bus and a common ground bus). The prior art cited in this paragraph, and the prior art for which the

corresponding claim charts provide teachings of common ESD buses will be referred to as "Common ESD Bus Art."

To the extent any of the '164 Patent Primary References are argued or shown to not disclose common ESD buses in the manners claimed in the '164 Patent, a POSA would have been motivated to combine the reference with any one, or several of, the Common ESD Bus Art references.

For example, a POSA would have been motivated and considered it obvious to include a common ESD bus for several reasons. First, a POSA would have understood that a common ground rail would help "ensure a solid return path for ESD protection" (Haralabidis, 2:55-61), which explained as beneficial and depicted as a goal of at least one '164 Patent Primary Reference (Yoshinaga, [0007]-[0008]). Furthermore, Yoshinaga teaches connecting reference potential lines for different circuits, but does not teach the specifics of how to do this. Yoshinaga, Figs. 1-4, [0005], [0009], [0061]. However, the Common ESD Bus Art discloses a common bus which is a way that this connection may be achieved. A POSA would have been further encouraged to apply the teachings of a common ESD bus to the '164 Patent Primary References because doing so would reduce die size and increase profits given that using common ground rails can reduce die sizes by locating the common ground rail off chip. Haralabidis, Figs. 3, 5. Furthermore, usage of common ESD rails "enables the IC to be constructed with fewer components and connections, thus minimizing the physical size thereof, and reducing the electrical connection complexity." Padden, 2:59-3:3.

Furthermore, a POSA would have also had a reasonable expectation of success in combining the teachings of the Common ESD Bus Art with other teachings because the usage of common lines is "conventional" (Haralabidis, 3:9-64, Figs. 3, 4) and a known method that was featured in texts from well before the filing of the '164 Patent (Saint, 160-163, 202-212, 221, 337, 344, Figs. 7-6, 7-7, 9-19, 9-20, 9-28, CS1-97, CS1-99). Furthermore, as Padden describes, such common ESD buses may be "utilised in any chip having a plurality of blocks, and thus utilised in any number of different applications." Padden, 6:24-27. Thus, a POSA would have been well acquainted and well understood how to apply a common ESD bus to an integrated circuit design

such as those disclosed by the '164 Primary Patent References, so a POSA would have had a high expectation of success in applying the teachings from the Common ESD Bus Art.

d. Additional Motivations for Micron's Prior Art Products

The above sections demonstrate that a POSA would have been motivated to combine the '164 Patent Primary References, including Micron's prior art products, with various prior art references, including those in the Micron IPRs. Micron's prior art products employ bond pads, bond wiring, and a package ground plane, demonstrating it is suitable for combination with the above art.

B. Invalidity Based on Section 112 (Patent L.R. 3-3(d))

1. Indefiniteness

Defendants provide the following grounds for invalidity under 35 U.S.C. § 112. Defendants' investigation of the Asserted Patents is ongoing, and Defendants reserve the right to amend or supplement these disclosures based on further investigation and in a manner consistent with the Federal Rules of Civil Procedure, the Local Patent Rules for the Northern District of California, and the Docket Control Order, or otherwise in accordance with any order or direction of this Court or agreement of the parties. Further, Plaintiff's Infringement Contentions fail to provide sufficient detail to fully understand its proposed application of the Asserted Claims, and Defendants reserve the right to assert additional grounds for invalidity under 35 U.S.C. § 112 in response to Plaintiff's claim interpretations. Defendants also reserve the right to supplement, modify, or otherwise amend these grounds for invalidity under 35 U.S.C. § 112 based on the Court's claim construction rulings or opinions or the parties' positions or arguments taken in connection with the claim construction process.

2. Written Description and Enablement

The specification of the '164 Patent does not provide adequate written description to support the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims. 35 U.S.C. § 112(a) requires that a patent specification contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that [the inventor]

invented what is claimed." *Ariad Pharm., Inc.*, 598 F.3d at 1351 (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ.*, 541 F.3d at 1122 (quoting *Vas-Cath Inc.*, 935 F.2d at 1563–64). The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Additionally, the Asserted Patents do not enable the claim scopes contained in Plaintiff's Infringement Contentions. Section 112(a) requires a specification to describe "the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention]." The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This "requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp.*, 344 F.3d at 1244 (citation omitted); *see Wyeth & Cordis Corp.*, 720 F.3d at 1385–86. The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Defendants provide below an identification of terms in Asserted Claims that render the Asserted Claims, at least as apparently construed by Plaintiff in its Infringement Contentions as discussed above, invalid pursuant to 35 U.S.C. § 112 as not enabled or lacking sufficient written description:

- "integrated circuit structure" (Claims 1-14)
- "circuit area" (Claims 1, 6, 8, 12)
- "adjacent" (Claims 1, 6, 8, 12)
- "parallel to the plurality of ESD buses" (Claims 5, 11, 13)
- "outside the plurality of chip edges or inside the plurality of chip edges" (Claims 4, 10)
- "a plurality discontinuous ESD bus groups" (Claim 3)
- "a connecting pad, and the plurality of bonding wires are configured to connect the

connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups" (Claim 7)

- "a plurality of discontinuous boundaries of the circuit area" (Claims 8, 12)

XIII. INVALIDITY OF THE '838 PATENT

A. Invalidity Based on the Prior Art

As shown below, the alleged inventions of the '838 Patent were well-known in the prior art. Those skilled in the art were aware of all of the limitations claimed in the '838 Patent. Thus, many prior art patents, publications, products, and combinations thereof, disclose, teach, or embody every limitation of the Asserted Claims and thus invalidate those claims. Examples of these disclosures, teachings, and embodiments are identified in the following sections and in the attached claim charts.

1. Identification of Prior Art References (Patent L.R. 3-3(a))

Subject to the reservation of rights above, Defendants identify each item of prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the '838 Patent. The patents/applications, publications, and systems identified are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations.

Some of the below citations and those in the corresponding invalidity claim charts involve prior art references that have corresponding related, foreign, and/or PCT counterpart publications. In such cases, where either the U.S. patent or related, foreign, and/or PCT counterpart is cited, it is to be understood that the corresponding disclosures from the counterpart patent and publications (which are substantively the same) are implicitly incorporated by reference in the alternative to avoid needless repetition.

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
S-1	U.S. 2018/0130701 A1 to Chun et al. ("Chun")	June 30, 2017	May 10, 2018
S-2	U.S. 2018/0053686 A1 to Hyun ("Hyun")	March 23, 2017	February 22, 2018
S-3	U.S. 10,229,929 to Kim et al. ("Kim5")	July 18, 2017	March 12, 2019
S-4	U.S. 2015/0255386 A1 to Lee et al. ("Lee 386")	March 4, 2015	September 10, 2015

Ex.	Patent No./Patent Pub. No.	Priority Date	Date of Issue/Publication
S-5	U.S. 2014/0191389 A1 to Lee et al. ("Lee 389")	March 18, 2013	July 10, 2014
S-6	U.S. 2018/0261618 A1 to Lee et al. ("Lee 618")	October 2, 2017	March 9, 2017
S-7	U.S. 2018/0026046 A1 to Nam et al. ("Nam2")	December 12, 2016	January 15, 2018
S-8	U.S. 2017/0194255 A1 to Oh ("Oh1")	July 11, 2016	July 6, 2017
S-9	U.S. 2018/0166380 A1 to Park et al. ("Park6")	June 13, 2017	June 14, 2018
S-10	U.S. 9,941,153 to Yang ("Yang5")	December 22, 2016	April 10, 2018
S-11	U.S. 2015/0287710 A1 to Yun et al. ("Yun")	November 17, 2014	October 8, 2015
S-12	U.S. 2017/0271256 A1 to Inatsuka ("Inatsuka")	January 18, 2017	September 21, 2017
S-13	U.S. 9,520,402 to Haller et al. ("Haller")	August 25, 2015	December 13, 2016

Table S-1: Prior Art Patents and Patent Publications for the '838 Patent

2. Anticipation and Obviousness (Patent L.R. 3-3(b) and (c))

The Asserted Claims of the '838 Patent are invalid because they are anticipated by the prior art and/or because they would have been obvious in view of the prior art.

The prior art identified by Defendants anticipates and/or renders obvious one or more of the Asserted Claims of the '838 Patent under at least AIA §§ 102(a)(1), 102(a)(2), and 103. For each prior art reference, Defendants have provided claim charts attached to these Invalidity Contentions as Exhibits S-1 through S-13. These charts identify where each element of each Asserted Claim can be found in each item of prior art. In addition to the above identified claims charts.

Again, to the extent not anticipated, the Asserted Claims of the '838 Patent are invalid as obvious under 35 U.S.C. § 103. Each prior art reference identified in the preceding sections—either alone or in combination with another prior art reference and/or in combination with the knowledge of one skilled in the art—renders the Asserted Claims invalid as obvious. In rendering the Asserted Claims obvious, each prior art reference identified in the preceding sections may be combined with: (1) information known to persons skilled in the art at the time of the alleged invention, (2) any of

the other anticipatory or obviousness prior art references, (3) any statements in the intrinsic record of the '838 Patent and related applications, or (4) any of the additional prior art identified below.

3. Motivations to Combine[22]

A person of ordinary skill in the art would have been motivated to combine the preceding references (*see* Section XIII.A.1) for the following reasons. Teachings, suggestions, motivations and/or reasons to modify any of the references and/or to combine any two or more of the references can come from many sources, including the prior art (by specific reference and when read as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obviousness to try, the nature of the problem faced, and/or knowledge possessed by a person of ordinary skill.

Although a patent claim may be invalidated based on a teaching-suggestion-motivation ("TSM") rationale—*i.e.,* that some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention—the Supreme Court identified additional rationales in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007). The following of these rationales apply here:

(A) the asserted claims combine prior art elements according to known methods to yield predictable results;

(B) the asserted claims involve the simple substitution of one known element for another to obtain predictable results;

(C) the asserted claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;

(D) the asserted claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) the asserted claims involve combinations of prior art references that would have been "obvious to try"'—a person of ordinary skill in the art could have reached the asserted claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

[22] The statements in this section about what was known and obvious to a POSA are made with respect to the effective filing date of the '838 Patent.

(F) the asserted claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach); *see also* Department of Commerce, Patent and Trademark Office, Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.,* 72 Fed. Reg. 57,526 (Oct. 10, 2007). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420-21.

Thus, even in the absence of a specific teaching, suggestion, or motivation to combine references, the Asserted Claims here are obvious and therefore invalid. Each of the cited references or devices is in the same field as the '838 Patent, making it obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. One of ordinary skill in the art would have recognized that improvements could be achieved by combining or modifying prior art references that described such improvements. Each of the above prior art references describes systems, products, or methods that were known to offer such improvements, and, accordingly, one of ordinary skill in the art would have been motivated to combine or modify the references as identified in each of the combinations below.

Furthermore, because each prior art reference concerns three-dimensional memory designs, and in particular three-dimensional memory designs that employs staircase structures with contact or landing pads, common industry knowledge supplied a reason to combine any one the above references. It was well understood that different three-dimensional memory structural features, including various different staircase and contact / landing pad features, sizes, and shapes, could be employed together or interchanged with each other, fitting together like puzzle pieces. Each combination would have produced predictable results and would simply represent a known alternative to one of ordinary skill in the art of three-dimensional memory. This is a further

motivation to combine any of the above references.

The below sections further address particular reasons to combine the above references. The below should not be construed as an admission that there is any value to the alleged invention of the '838 Patent. As discussed previously, these contentions are based in significant part on how Plaintiff is apparently construing the asserted claim in its Infringement Contentions, which is an incorrect and overbroad interpretation of the alleged invention of the '838 Patent. Accordingly, to the extent the below refers to benefits of certain elements or industry trends towards these elements, this is not an admission that the alleged invention of the '838 Patent provides any benefits: to the contrary, properly construed and compared to the prior art, the '838 Patent provides no benefits. Likewise, to the extent the below refers to substituting elements, this is not an admission that the elements subject to the substitution are in any way similar, *e.g.,* perform the same function, in the same way, to achieve the same result.

The various elements of the Asserted Claims were well known in the prior art at the time of the alleged invention, and the combination would have been obvious to one of skill in the art. The combinations simply (a) combine prior art elements according to known methods to yield predictable results; (b) involve the simple substitution of one known element for another to obtain predictable results; (c) involve the use of a known technique to improve similar devices (methods, or products) in the same way; (d) apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) involves combinations of prior art references that would have been "obvious to try" – a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and/or (f) would have been prompted by known work, based on design incentives or other market forces, because such variations were predictable to one of ordinary skill in the art.

Moreover, the Supreme Court has stated that a motivation to combine may be simply "common sense" and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR,* 550 U.S. at 420. Indeed, the Supreme Court held that it is

sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421. Here, all the claim elements are common sense and are easily fit together by one of ordinary skill in the art.

While not necessary, a motivation to combine may also be found in the references themselves. One of skill in the art would have been motivated to combine a reference that refers to, or otherwise explicitly invites combination with, another reference. Where the references cited herein have such an explicit invitation to combine, that invitation would have motivated one of skill in the art to combine any such references.

Micron hereby identifies the following '838 Patent Primary References: Chun, Hyun, Kim5, Lee 386, Lee 389 , Lee 618, Nam2, Oh1, Park6, Yang5, Yun, and Inatsuka.

The below provides several exemplary combinations and motivations for combining an '838 Patent Primary Reference with another reference.

a. Use of Contact or Landing Pads That Are "Laterally Displaced"

To the extent any '838 Patent Primary Reference is determined to be missing the claimed "landing pad" with a "second side surface" that is "laterally displaced form a side surface of the second portion of the second material layer" required by claims 1 and 12 of the '838 Patent, a POSA would have considered it obvious and been motivated to form that reference's contact / landing pad such that it includes the type of "laterally displaced" surface that the claims requires. At the time the '838 patent was filed, the prior art was replete with examples of "laterally displaced" contact or landing pads for use with memory devices that included a stepped structure. *See, e.g.,* Chun, [0195]; Figs. 25-30; Hyun, [0050], 5E; Kim5, 7:54-8:10, Fig. 4B; Lee 389, [0048]-[0050], Fig. 8B; Nam2, [0073], Fig. 10; Oh1, [0021], Fig. 3I; Yang5, 5:42-58, Fig. 2; Yun, [0060], Figs. 5A, 5C, 5D (all providing examples of landing pads that either extend beyond the side of an underlying conductive layer, or are set back from the side of the underlying conductive layer). Given that the use of pads with rounded side surfaces was well-known and routine in the prior art, a POSA would have considered use of such a structure with any of '838 Patent Primary References to constitute a

routine, highly obvious design choice. A POSA would have been motivated to employ such a design to, among other things, either increase the size of the contact pad to ensure better electrical connection with other circuitry or avoid manufacturing problems or defects by situating the pads—and the structure with which the pads interconnect—away from other conductive material in the memory device.

A POSA would also have had a reasonable expectation of success. Again, contact or landing pads situated such that they are offset from the side of the underlying conductive layer were routinely used in three-dimensional memory devices with stepped structures. As this type of contact or landing pad had been shown to be successfully used in other devices, a POSA would have expected use of such a shape to also be successful in when employed in the '838 Patent Primary References.

b. Use of Insulating Layers With Various Physical Extents

To the extent any '838 Patent Primary Reference is determined to be missing the claimed contact or landing pad with a "first side surface … in contact with the first material layer" required by claims 1 and 12 of the '838 Patent, a POSA would have considered this obvious. The prior art disclosed a range of different interlayer insulation physical extends. This included, for instance, interlayer insulation layers that extend out and around a stepped device's contact pads. *See, e.g.,* Yang5, Figs. 2, 4A-9B (showing various examples of insulating layers 114 extending out from stack and surrounding contact pads 120); Lee 389, Fig. 7A (showing insulating layers 22 surrounding contact pads on conductive layers 25), Inatsuka, Figs. 3, 14, 17 (showing insulating layers extending to contact structures). All of the '838 Patent Primary References teach memory devices with staircase structures including contact or landing pads on the staircase steps. Moreover, all of the '838 Patent Primary References surround those landing pads with insulation. While certain of the '838 Patent Primary References teach that that insulation is formed in a separate step from the layers insulation forming the staircase structure's alternating stack of insulating and conductive layers, a POSA would have considered it obvious (and would have been motivated) to form the insulation in the stack and around the contact pad in a single step such that this layer constitutes a single, unified structure. A POSA would have considered this to be nothing more than

a routine, obvious design choice. Moreover, given that the insulation surrounding the contact or landing pad was routinely formed from the same material as that in the stack (*see, e.g.,* Exs. S-1 through S-12), a POSA would have recognized that forming the layers of insulation during the same step would have simplified the process employed to manufacture the '838 Patent Primary References' devices. A POSA would also have had every reason to believe that the '838 Patent Primary References could be successfully modified in the manner discussed above. Again, it was known in the prior art that the same layer of insulation present in an alternating stack of conductive and insulating layers could also extend around a device's contact or landing pads. *See, e.g.,* Yang5, Figs. 2, 4A-9B; Lee 389, Fig. 7A; Inatsuka, Figs. 3, 14, 17.

c. Use of the Distances Required by Claims 3 and 18

To the extent any '838 Patent Primary Reference is determined to not itself teach " a lateral distance between the second side surface and the side surface of the second portion of the second material layer is between 10 nm and 300 nm" as required by claims 3 and 18, a POSA would have considered it obvious and been motivated to employ a distance within this range when forming the reference's contact/landing pads. A POSA would have considered the specific relative sizing of a memory device's insulating layers, conductive layers, and contact pads to be nothing more than a routine, obvious design choice. Further, the prior art shows that the layers—and contact pads—were sized and situated with thicknesses and offsets falling within the claimed range. See, e.g., Yang5, 5:54-58, 6:23-28, 7:23-63, 10:7-39, Figs. 2, 4A-B, 5A-B (providing example layer thicknesses and contact pad sizes), Haller, 4:17-5:39; Figs. 2-8 (discussing example offset sizes). A POSA would have recognized that the claimed range is nothing more than the standard sizing and offset routinely used in the prior art.

A POSA would also have had a reasonable expectation of success. Given that the claimed range was standard, a POSA would have had every reason to believe that it could be successfully employed when implementing the memory devices of the '838 Patent Primary References.

d. Use of the Materials Required by Claims 5 and 16

To the extent any '838 Patent Primary Reference is determined to not itself teach one of the specific types of conductive materials listed by claims 5 and 16, a POSA would have considered it

obvious and been motivated to employ such a material. A POSA would have considered the specific type of conductive material used to form the electrode layers and contact pads of the ''838 Patent Primary Reference to be routine, obvious design choice. Numerous example materials identified as acceptable for use—including materials falling within the claim scope—are identified by the prior art. *See, e.g.*, Inatsuka, [0177]; Kim5, 6:31-35, 14:12-17; Lee 386, [0095], [0100]; Lee 618, [0115]; Nam2, [0094], [0107]; Yang5, 8:39-64. A POSA would have been motivated to use any of these known, acceptable materials and would have expected to succeed when doing so.

e. Use of Contact or Landing Pads With "Curved" Side Surfaces

To the extent any '838 Patent Primary Reference is determined to be missing the claimed "second portion of the conductive layer comprises a curved side surface" required by claim 13 of the '838 Patent, a POSA would have considered it obvious and been motivated to form that reference's contact / landing pad such that it includes the type of "curved side surface" the claim requires. At the time the '838 patent was filed, the prior art was replete with examples of "curved" contact or landing pads for use with memory devices that included a stepped structure. *See, e.g.,* Kim5, 8:29-34, Fig. 4B (referencing contact pad with "curved surface" or "cylindrical shape"); Lee 386, ¶ [0090] (noting that contact pad may be "cylindrical pillar"); Nam2, ¶¶ [0068], [0072], Fig. 8A (noting that contact pad can have "convex" or "bull nose shape"), Oh1, ¶ [0021], Fig. 31 (noting that pad sidewalls can be sloped), Park6, ¶¶ [0056] (noting that contact pad sides can be rounded), Yang5, 2:12-15 (noting that the pads can have a square, circular, rectangular, or bar shape), Yun, ¶ [0060], Figs. 5A-5F (noting that contact pads can have "rounded" surface). Given that the use of pads with rounded side surfaces was well-known and routine in the prior art, a POSA would have considered use of such a structure with any of '838 Patent Primary References to constitute a routine, highly obvious design choice.

Further, it was also known that contact pads with curved or rounded sides are less likely to cause a "short circuit between … adjacent conductive layer patterns." *E.g.*, Park6 ¶¶ [0056], [0058]. This also would have motivated use of such a contact or landing pad shape with any of the '838 Patent Primary References. A POSA would have understood that by forming contact or landing pads with curved—as opposed to straight—side surfaces, the distance between the pads

and adjacent conductive layers could be increased. This would have in turn reduced the possibility of short circuit resulting from, for example, manufacturing defects.

A POSA would also have had a reasonable expectation of success. Again, contact or landing pads with curved side surfaces were routinely used in three-dimensional memory devices with stepped structures. As this type of contact or landing pad had been shown to be successfully used in other devices, a POSA would have expected use of such a shape to also be successful in when employed in the '838 Patent Primary References.

f. Use of the Different Distances Required by Claim 14

To the extent any '838 Patent Primary Reference is determined to not itself teach use of the different "lateral distances" required by claim 14, this would have been obvious in view of the teachings of Kim5. Kim5 teaches that landing pads can be made differently sized (and thus differently offset) depending on the level of the staircase on which the pads are situated. *See* Kim5, 11:57-12:7; Fig. 9. A POSA would have understood that including differently sized landing pads on different staircase levels facilitates better electrical connection with other circuitry and reduces the potential for manufacturing defects. This would have provided a strong motivation to employ differently sized contact pads with the '838 Patent Primary References. A POSA would also have had a reasonable expectation of success. In particular, a POSA would have recognized that resizing landing pads is a simple, straightforward, and routine exercise of design optimization.

B. Invalidity Based on Section 112 (Patent L.R. 3-3(d))

1. Indefiniteness

Defendants provide the following grounds for invalidity under 35 U.S.C. § 112. Defendants' investigation of the Asserted Patents is ongoing, and Defendants reserve the right to amend or supplement these disclosures based on further investigation and in a manner consistent with the Federal Rules of Civil Procedure, the Local Patent Rules for the Northern District of California, and the Docket Control Order, or otherwise in accordance with any order or direction of this Court or agreement of the parties. Further, Plaintiff's Infringement Contentions fail to provide sufficient detail to fully understand its proposed application of the Asserted Claims, and Defendants reserve the right to assert additional grounds for invalidity under 35 U.S.C. § 112 in

response to Plaintiff's claim interpretations. Defendants also reserve the right to supplement, modify, or otherwise amend these grounds for invalidity under 35 U.S.C. § 112 based on the Court's claim construction rulings or opinions or the parties' positions or arguments taken in connection with the claim construction process.

2. Written Description and Enablement

The specification of the '838 Patent does not provide adequate written description to support the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims. 35 U.S.C. § 112(a) requires that a patent specification contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharm., Inc.*, 598 F.3d at 1351 (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ.*, 541 F.3d at 1122 (quoting *Vas-Cath Inc.*, 935 F.2d at 1563–64). The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Additionally, the Asserted Patents do not enable the claim scopes contained in Plaintiff's Infringement Contentions. Section 112(a) requires a specification to describe "the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention]." The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This "requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp.*, 344 F.3d at 1244 (citation omitted); *see Wyeth & Cordis Corp.*, 720 F.3d at 1385–86. The Asserted Patents do not meet that requirement for the list of terms below, which Defendants reserve the right to amend.

Defendants provide below an identification of terms in Asserted Claims that render the Asserted Claims, at least as apparently construed by Plaintiff in its Infringement Contentions as

discussed above, invalid pursuant to 35 U.S.C. § 112 as not enabled or lacking sufficient written description:

- "a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer" (Claims 1, 12)
- "wherein the first side surface is in contact with the first material layer" (Claims 1, 12)
- "the second side surface is laterally displaced from a side surface of the second portion of the second material layer" (Claims 1, 12)
- "wherein the first side surface comprises a curved side surface" (Claim 13)

XV. DOCUMENT PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS (Patent L.R. 3-4)

A. Patent L.R. 3-4(a)—Source code, specifications, schematics, flow charts, artwork, formulas, or other documentation sufficient to show the operation of any aspects or elements of an Accused Instrumentality identified by the patent claimant in its Patent L.R. 3-1(c) chart

Technical documentation is either being produced or is to be made available via inspection. The produced prior art documents are located at: MYM0043255-MYM0043296, MYM0043297-MYM0043339, MYM0043340-MYM0043352, MYM0042897-MYM0043247; MYM0043849-MYM0050565; MYM0050566-MYM0058876; MYM0058892-MYM0060608; MYM0060609-MYM0065109; MYM0065112-MYM0065115, MYM0069237-MYM0069714, MYM0089971-MYM0090837.

As for layouts, schematics, and process information, Micron has made available its Cadence environment available for inspection at the Silicon Valley office of Orrick, Herrington & Sutcliffe LLP.

B. Patent L.R. 3-4(b)—A copy or sample of the prior art identified pursuant to Patent L.R. 3-3(a) which does not appear in the file history of the patent(s) at issue. To the extent any such item is not in English, an English translation of the portion(s) relied upon shall be produced

The prior art referenced herein is either being produced or is to be made available via inspection. The produced prior art documents are located at: MYM0069181-MYM0069181, MYM0042897-MYM0043247, MYM0069190-MYM0069236, MYM0043255-MYM0043296, MYM0043316-MYM0043339, MYM0043423-MYM0043424, MYM0043248-MYM0043254, MYM0058880-MYM0058891, MYM0043425-MYM0043844, MYM0065164-MYM0066151, MYM0065112-MYM0065115, MYM0069182-MYM0069189, MYM0069715-MYM0069940, YMTC-MSC_0001-YMTC-MSC_0010, MYM0069941-MYM0069958, MYM0069959-MYM0089924.

As for layouts, schematics, and process information, Micron has made available its Cadence environment available for inspection at the Silicon Valley office of Orrick, Herrington & Sutcliffe LLP.

C. Patent L.R. 3-4(c)—All agreements that may be related to the accused instrumentality or may be comparable to a license that would result from a hypothetical reasonable royalty negotiation

Micron has produced license documents at: MYM0043353-MYM0043422, MYM0089925-MYM0089970.

D. Patent L.R. 3-4(d)—Documents sufficient to show the sales, revenue, cost, and profits for accused instrumentalities identified pursuant to Patent L.R. 3-1(b) for any period of alleged infringement

Micron has or is producing spreadsheets in compliance with Patent L.R. 3-4(d) at: MYM0058877-MYM0055878 (as to units sold) and MYM0058879 (as to revenue, cost, and profits), MYM0090838-MYM0090840.

E. Patent L.R. 3-4(e)—All agreements that may be used to support the party denying infringement's damages case

Micron reserves the right to rely on agreements produced pursuant to Patent L.R. 3-4(c).

Micron's search for additional documentation, and/or corroborating evidence is ongoing. Accordingly, Micron reserves the right to continue to supplement its production as it identifies additional and/or corroborating evidence during the course of discovery.

Dated: November 25, 2024

ORRICK, HERRINGTON & SUTCLIFFE LLP

By: */s/ Jared Bobrow*
Jared Bobrow
Attorneys for Defendant and Counterclaim Plaintiff Micron Technology, Inc. and Defendant Micron Consumer Products Group, LLC

CERTIFICATE OF SERVICE

I am employed in San Mateo County, in the State of California. I am over the age of 18 years old and not a party to this action. My business address is Orrick, Herrington & Sutcliffe LLP, 1000 Marsh Road, Menlo Park, California, 94025-1015. On November 25, 2024, I served the **DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND DOCUMENT PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS RE YMTC II ASSERTED PATENTS (PATENT LOCAL RULES 3-3 AND 3-4)** on all interested parties to this action in the manner described as follows:

☐ **(VIA U.S. MAIL)** On November 25, 2024, by placing a true copy of the document(s) listed above in an envelope, with postage thereon fully prepaid, addressed as set forth below and then sealing the envelope and depositing it in the U.S. mail at Menlo Park, California.

☒ **(VIA EMAIL)** On November 25, 2024, via electronic mail in Adobe PDF format the document(s) listed above to the electronic address(es) set forth below.

☐ **(VIA OVERNIGHT-FED EX)** I caused the within document(s) to be delivered by overnight courier to the address(es) set forth below.

Allen S. Cross (DCB No. 252687)
allen.cross@ropesgray.com
James R. Batchelder (Bar No. 136347)
james.batchelder@ropesgray.com
Andrew T. Radsch (Bar No. 303665)
andrew.radsch@ropesgray.com
James F. Mack (Bar No. 322056)
james.mack@ropesgray.com
Nancy N. Attalla (Bar No. 341070)
nancy.attalla@ropesgray.com
Rachael S. Bacha (NYB No. 4817938)
rachael.bacha@ropesgray.com
Hyun-Joong Kim (Pro Hac Vice)
daniel.kim@ropesgray.com
Alexander Middleton (Pro Hac Vice)
alexander.middleton@ropesgray.com
Nicole S. L. Pobre (Pro Hac Vice)
nicole.pobre@ropesgray.com
Stepan Starchenko (Bar No. 318606)
stepan.starchenko@ropesgray.com
ymtc-micron-ropes-service@ropesgray.com
ROPES & GRAY LLP

Kevin C. Wheeler (Bar No. 261177)
kevin.wheeler@lw.com
Clement Naples (Pro Hac Vice)
clement.naples@lw.com

Brenda L. Danek (Pro Hac Vice)
brenda.danek@lw.com
Thomas W. Yeh (Bar No. 287118)
thomas.yeh@lw.com
Brett M. Sandford (Bar No. 302072)
brett.sandford@lw.com
Benjamin Behrendt (Pro Hac Vice)
benjamin.behrendt@lw.com
Brent Thomas Watson (Bar No. 301274)
thomas.watson@lw.com
Elliott Greb (Bar No. 347483)
elliott.greb@lw.com
Richard Lowry (Pro Hac Vice)
richard.lowry@lw.com
ymtcmicron.lwteam@lw.com
LATHAM & WATKINS LLP

Counsel for Plaintiff, Yangtze Memory Technologies Company, Ltd.

I declare under penalty of perjury under the laws of the State of California and the United States that the foregoing is true and correct.

Executed on November 25, 2024, at Menlo Park, California.

/s/ Matthew Bonini
Matthew Bonini