

2006 International Electron Devices Meeting TECHNICAL DIGEST

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IEEE Catalog Number: 06CH37807C

ISBN: 1-4244-0439-8

Library of Congress Number: 81-642284

Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node

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Abstract

For the first time, the 3 dimensionally stacked NAND Flash memory, is developed by implementing S^3 (Single-crystal Si layer Stacking) technology, which was used to develop S^3 SRAM previously. The NAND cell arrays are formed on the ILD as well as on the bulk to double the memory density without increasing the chip size. The feasibility of the technology was proven by the successful operation of 32 bit NAND Flash memory cell strings with 63nm dimension and TANOS structures. The novel NAND cell operational scheme, so called SBT (Source-Body Tied) scheme, is presented to maximize the advantages of 3 dimensionally stacked NAND cell structures.

Introduction

Recently, the great demands for higher density and lower bit cost in NAND Flash memories are growing because they are key devices for the mass data storage applications in various portable electronic products, such as portable audio and video players, cellular phones, USB memories and newly introduced solid state disks for PC. In order to keep trends of reducing the bit cost and increasing the bit density, the linear shrink of the patterns have been aggressively driven by developing MLC (Multi Level Cell) technology and early adopting the advanced lithographic tools .[1] However, the linear scaling down of the NAND Flash memories are approaching to the physical, electrical and reliability limitations, especially as the technology node is advancing to near 30nm dimension .

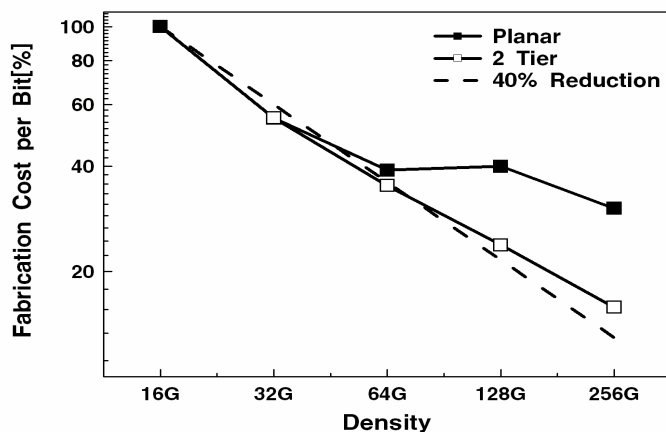


Fig. 1 Predictions of fabrication cost of NAND flash memory as the bit density increases for the planar cell and the stacked cell.

First, it has to use EUV lithography for the patterning, which is expected to be available after year 2009, according to ITRS

roadmap. Even if the tool is prepared, a cost of the tool will be much more expensive and its throughput will not be comparable to those of the ArF lithography. From the standpoint of the bit cost, it means that even if the dimensions is shrunk and the density is increased, the bit cost down trends will not be kept up with the historical trends any more as shown in Fig1. The economic needs of the further shrink for the higher density will diminish and the bit growth rate in the data storage applications will slow down.

Secondly, from the electrical and reliability perspective, the further shrink below 30nm dimension, will cause the serious problems, such as electrical isolations between the word-lines and the cell nodes , the short channel effect, the cell current reduction and tolerable charge losses of the stored charges for data retention, which is less than 10, and etc. as shown in Fig.2 even in newly being developed SONOS-like structures. Furthermore, these problems are resulted from the fundamental physical limits, which are difficult to be overcome with the conventional modifications generally used in the past nodes.

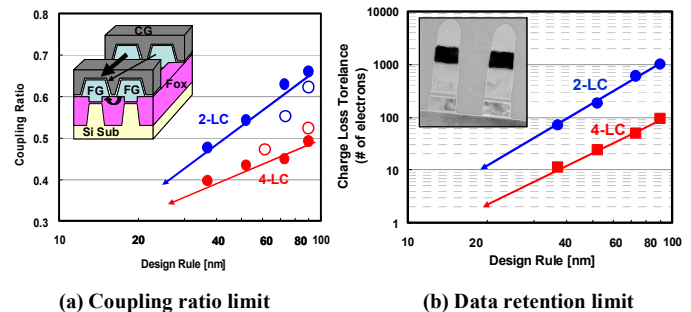


Fig.2 Limitations of NAND flash memory with the shrinkage of D/R

Therefore, one of the best ways to circumvent these barriers caused by simple conventional linear shrink technology is to stack three dimensionally the cell arrays with minimizing the additional processes for stacking. As one of easy solutions to increase the density, chips or packages have been simply stacked with bonding or packing technology. However, the simple stacking process of the chips or packages cannot reduce the bit cost or the fabrication cost because they stack the already completely integrated chips. However, in our S^3 (Single-crystal Si layer Stacking) technology, the Si active layers are stacked with minimum processes and are interconnected simultaneously with the bottom cell arrays and the peripheral circuits.[2] Also, it can improve the electrical characteristics by reducing the capacitive and resistive loading without reducing the cell current.

Process Integration

In the doubly stacked NAND Flash cell strings of Fig.3, the cell strings of the upper layers are stacked over the bottom layer ones already formed on the bulk Si Substrate. The cell strings have TANOS (TaN-AL₂O₃-Nitride-Oxide-Silicon) structures.[3]. In order to achieve same electrical characteristics of the cell strings in both layers, perfect SOI –like single crystal Si layers are formed on the ILD layers with S³ technology. The bit line contacts and the common source lines are patterned simultaneously on the both layers of the cell string by etching layers vertically through the upper level Si layers to the bottom active layer as shown in Fig.4. The bit line holes are filled sequentially with the N-doped poly-Si and W. Therefore, both of the cell strings are connected through a single contact hole to the same bit line. The x-decoders of the upper and lower cell arrays are laid out separately at the other ends of the arrays as shown in Fig.5. Only three additional photo layers are used to double the density of NAND cell by stacking cell arrays on the ILD. The key processes are summarized in Table 1.

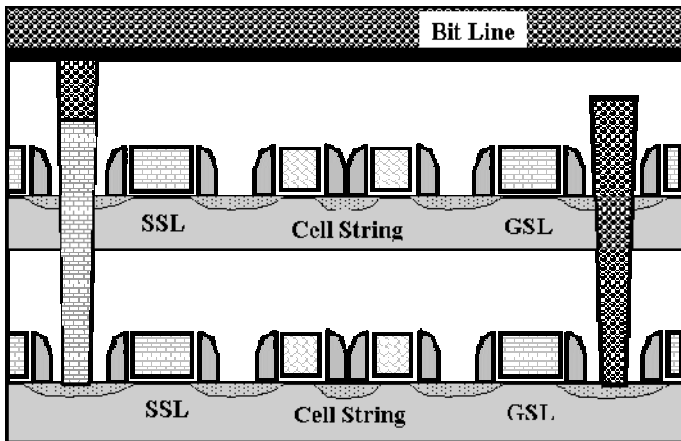


Fig. 3 Vertical structure of the 3D stacked cell string. Bit-line and common source line (CSL) are formed through 2nd active layer. Well bias is simultaneously applied by CSL. (Source-body tied)

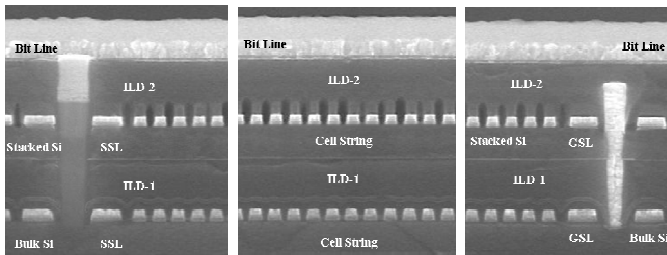


Fig. 4 Vertical SEM photographs of the fabricated 3D stacked NAND cell string. The 2nd active layer is SOI like perfect single crystal.

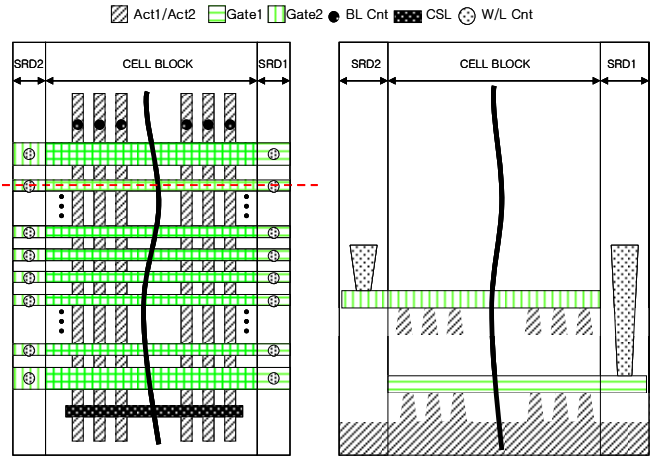


Fig. 5 Top view layout and vertical structure of word-lines and x-decoders for the doubly stacked NAND flash memory cell array.

Table I Summary of key process flow sequence for the 3D Stacked NAND flash memory.

- Well & Vth Adjust Implantation
- Active (Dual Trench Isolation)
- 1st Gate Stack Structure ; (Tunnel Ox/Trap SiN/Blocking Ox/TaN/WN+W)
- Gate-1 Poly Patterning
- Halo/LDD Implant, 1st Spacer, S/D Implant and RTA
- 1st ILD/ILD CMP
- **Formation of Single Crystal Active Si for 2nd Cell String**
- 2nd Gate Stack Structure ; (Tunnel Ox/Trap SiN/Blocking Ox/TaN/WN+W)
- Gate-2 Poly Patterning
- Halo/LDD Implant, 1st Spacer, S/D Implant and RTA
- 2nd ILD/ILD CMP
- **Cell Penetration Contact (for Source-Body Tied) Formation**
- Other Contacts and Metal (Bit Line)

Electrical Characteristics

Basically, the upper and lower cell strings were designed to have the same electrical characteristics. The characteristics of program and erase operations are shown in Fig.6 and Fig.7. The cell current characteristics of the upper cell strings under the worst cell bias condition are comparable with ones of the lower as shown in Fig.8. The reliability of the cell strings were measured. Fig.9 and Fig.10 show the characteristics of the endurance and the read disturbance in the stacked NAND cell strings, respectively. The differences between both cell strings are negligible. It was shown that the novel stacked NAND cell could satisfy the requirements of the NAND Flash memory product.

SBT (Source-Body Tied) Operational Scheme

In stacking NAND cell arrays, thin stacked Si layers are desirable for simplicity in integration of the processes. However, when a thin body is used, the body of the cell strings is disconnected with the other cell strings by trench isolations and is floated electrically. The cell strings with the floated body have a disadvantage in the erase operation as shown in Fig.11. In conventional body bias scheme, a block or whole cells of the string can be erased simultaneously because the body is biased negatively and all word-lines are grounded. However, in the

floating thin body scheme, only one cell of the string can be erased at one time because the word-lines of other cells are biased at V_{pass} to connect the channel of the selected cell. The erase time of the product will be increased by 32 times. Therefore, in order to solve the erase problem in SOI type thin body structures, the novel operational scheme is suggested. The common source of the cell string is tied with the body of the string electrically. This scheme can erase the cell strings in an exactly same way as the conventional body bias scheme does.

But, in program operations, inhibited WL0 cell can be interfered by the leakage current through the SSL to the ground due to coupling of the grounded SSL gate as shown in Fig.12. The channel potential of the WL0 cell will not follow the program voltage of the WL0 gate. It can be improved by applying negative bias, such as -1.2V at the SSL gate as shown in Fig.13. The interference characteristics of the WL0 cell for various bias conditions are shown in Fig.14.

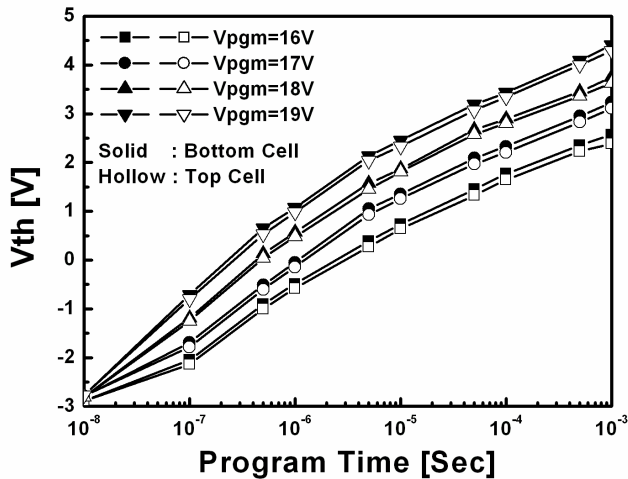


Fig. 6 Comparisons of the program speed characteristics between the top cell and the bottom cell of the stacked NAND cell strings

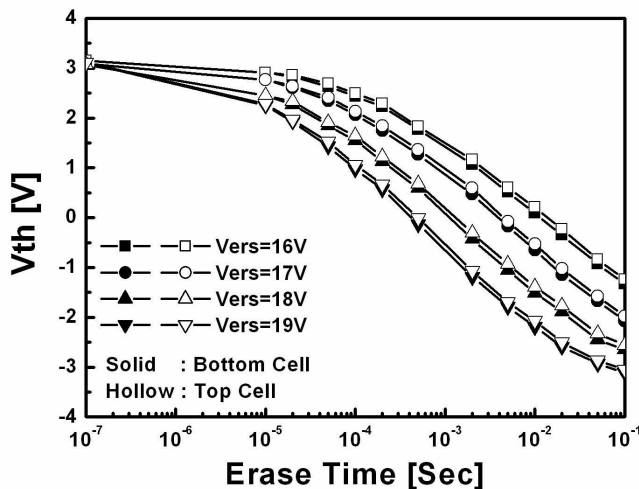


Fig. 7 Comparisons of the erase speed characteristics between the top cell and the bottom cell of the stacked NAND cell strings.

Conclusions

For the first time, the 3 dimensionally stacked NAND Flash memory cell arrays are formed on the ILD as well as on the bulk to double the memory density without increasing the chip size by implementing S^3 technology. The feasibility of the technology was proven by the successful operations of 32 bit NAND Flash memory cell strings with 63nm dimension, TANOS structures, and the novel SBT (Source-Body Tied) operational scheme.

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- [2] Soon-Moon Jung et al, IEDM Tech. Dig., pp 265-268, 2004
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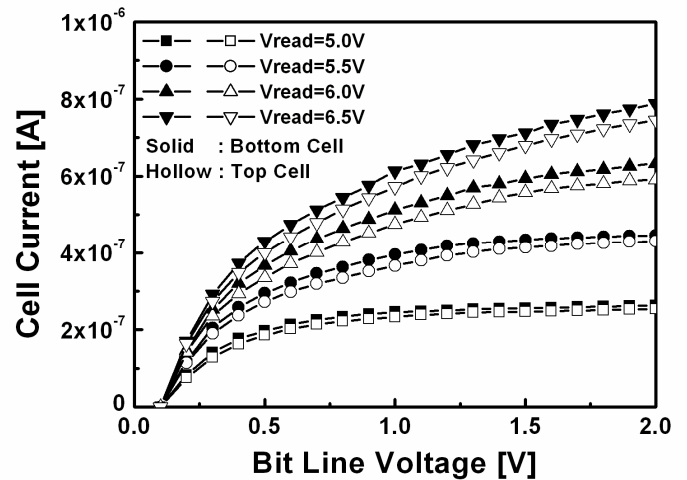


Fig. 8 The characteristics of cell current between the top cell strings and the bottom cell strings under the worst bias condition.

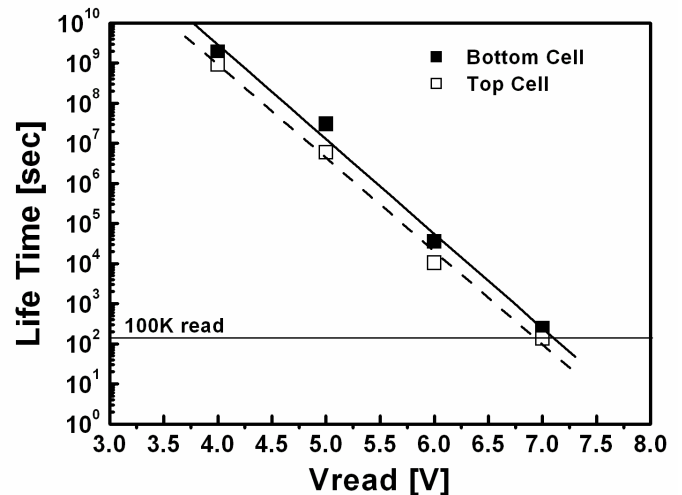


Fig. 9 Comparison of read disturbance characteristics between top cell and bottom cell.

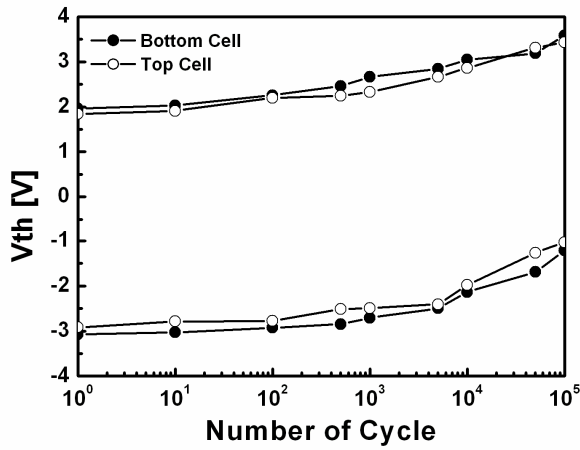


Fig. 10 Endurance characteristics of the top cell and the bottom cell of the stacked NAND cell strings

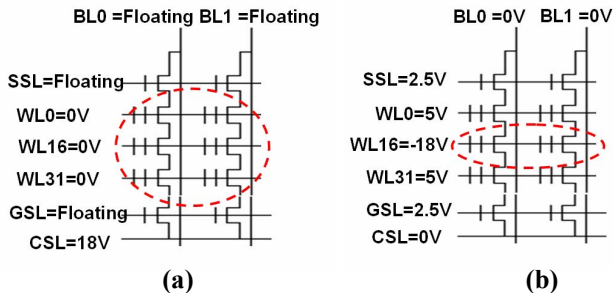


Fig. 11 Comparisons of the erase operation (a) Erase by page *without* well bias. (b) Erase by block *with* well bias.

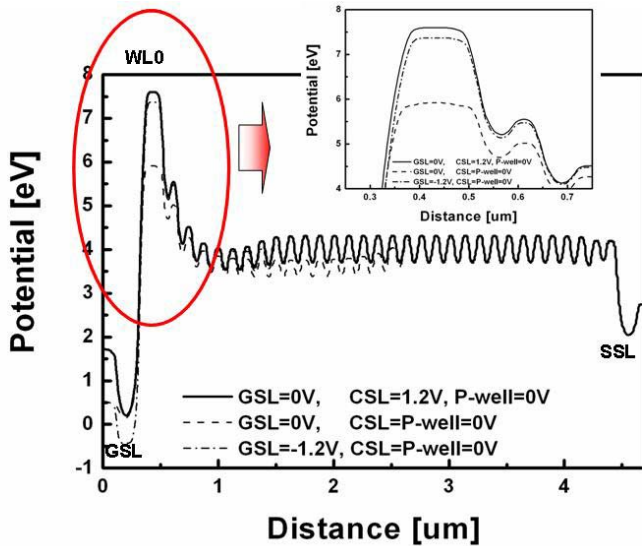


Fig. 12 Potentials of the inhibited cells at the various bias conditions during the program operation. WL0 is Vp_{gm} and other word lines are V_{pass}. At the condition of dotted-line, the channel potential of inhibited cell is lowered and it resulted in poor boosting.

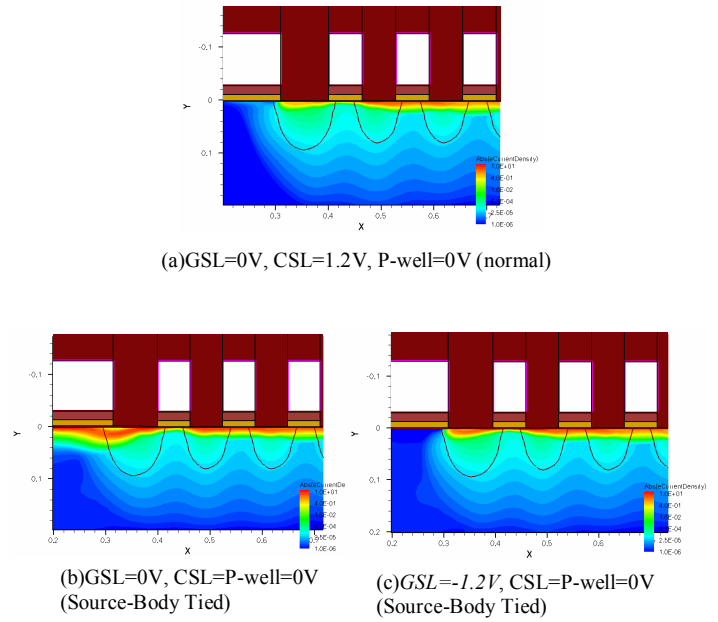


Fig. 13 Current density comparisons of inhibited cells; WL0=V_{p_{gm}}, Other WLs=V_{pass}. At the (b) condition, some leakage current is observed at GSL Tr. , It results in lowered channel potential of the adjacent cell Tr. (inhibited WL0 cell) as shown in Fig. 12.

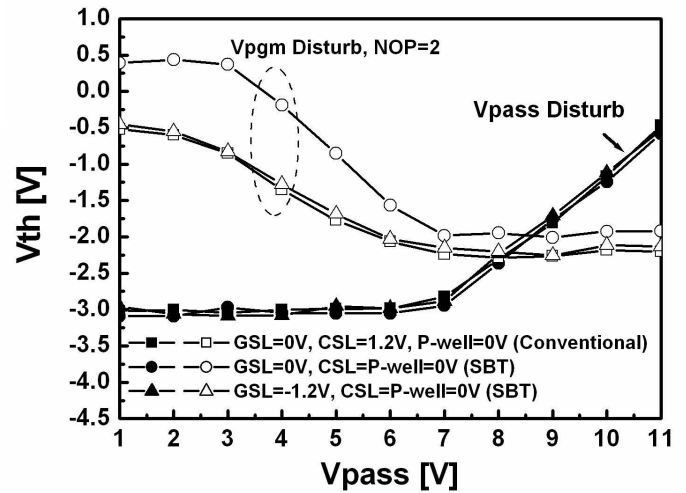


Fig. 14 Comparisons of the interference characteristics the cell strings at the bias conditions of the source-body tied scheme and the conventional well bias condition .