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8 *Micron Technology, Inc., and Defendant Micron*
Consumer Products Group, LLC

9
10 UNITED STATES DISTRICT COURT
11 NORTHERN DISTRICT OF CALIFORNIA
12 SAN FRANCISCO DIVISION

13 YANGTZE MEMORY TECHNOLOGIES
14 COMPANY, LTD.,

15 Plaintiff,

16 v.

17 MICRON TECHNOLOGY, INC., et al.,

18 Defendants.

Case No. 3:23-cv-05792-RFL

**DECLARATION OF E. FRED
SCHUBERT, PH.D. IN SUPPORT OF
DEFENDANTS' PROPOSED CLAIM
CONSTRUCTIONS (PATENT LOCAL
RULE 4-3)**

Honorable Rita F. Lin

19
20 MICRON TECHNOLOGY, INC.,

21 Counterclaim Plaintiff,

22 v.

23 YANGTZE MEMORY TECHNOLOGIES
24 COMPANY, LTD., and YANGTZE
25 MEMORY TECHNOLOGIES, INC.,

26 Counterclaim Defendants.
27
28

1 I, E. Fred Schubert, Ph.D., hereby declare:

2 **I. INTRODUCTION**

3 1. I make this declaration in support of certain proposed claim constructions of
4 Defendant and Counterclaim Plaintiff Micron Technology, Inc.'s, and Defendant Micron
5 Consumer Products Group LLC's (collectively "Micron") based on my personal knowledge, my
6 experience, and my investigation into this case, including my review of the materials cited
7 herein. If called upon as a witness, I could competently testify to the truth of each statement herein.

8 2. I have been retained by counsel for Micron in the above-captioned action to provide
9 opinions regarding the construction of certain terms in the asserted claims of U.S. Patent Nos.
10 11,501,822 ("the '822 patent"), 10,872,903 ("the '903 patent"), and 11,568,941 ("the '941 patent").

11 3. My opinions provided herein are based on my years of education, research, and
12 experience, as well as my investigation and study of relevant materials and materials that I was
13 asked to consider (identified below). Further, I may also consider additional documents and
14 information in forming further opinions, including documents that may not yet have been provided
15 to me.

16 4. My analysis of the materials produced in this matter is ongoing, and I will continue
17 to review any new material as it is provided. This declaration represents only those opinions that I
18 have formed to date. I reserve the right to revise, supplement, or amend my opinions below based
19 on new information and on my continuing analysis of the materials already provided.

20 **II. COMPENSATION**

21 5. I am being compensated for my services in this matter at my rate of \$525.00 per
22 hour. I am also being reimbursed for reasonable out-of-pocket expenses incurred as a result of my
23 work in this matter. My compensation is not contingent upon the opinions I render or the outcome
24 of this litigation.

1 4[d] wherein the memory has a two-deck structure.

2 5[pre] A program method of a memory, the memory comprising a first
3 portion and a second portion, the first portion comprising a first wordline to a
4 kth wordline from bottom to top, the second portion formed above the first
5 portion and comprising a (k+1)th wordline to an mth wordline from bottom to
6 top, the program method comprising:

7 5[a] applying a first voltage to the to the first wordline to an (x-2)th wordline
8 when an xth wordline is used to perform a program operation;

9 5[b] applying a second voltage to an (x-1)th wordline; and

10 5[c] applying a third voltage to an (x+1)th wordline;

11 5[d] wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.

12 10[pre] The program method of claim 5, wherein the memory further
13 comprises:

14 10[a] a lower dummy wordline formed above the first portion;

15 10[b] an upper dummy wordline formed below the second portion;

16 10[c] a joint oxide layer formed between the lower dummy wordline and the
17 upper dummy wordline;

18 10[d] wherein the memory has a two-deck structure.

19 **E. DISPUTED TERMS**

20 134. I have been asked to provide my opinions regarding the parties' proposed
21 constructions for one claim term of the '941 patent. That term is set forth below.

22 **i. "from bottom to top" (Claims 1, 5)**

Micron's Proposed Construction	YMTC's Proposed Construction
Plain and ordinary meaning	Plain and ordinary meaning, <i>i.e.</i> , from lowest to highest

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24
25
26 135. Both Micron and YMTC propose that this term be given its plain and ordinary
27 meaning, but YMTC proposes that the plain and ordinary meaning is "from lowest to highest." As
28 I discuss below, YMTC's proposed plain and ordinary meaning does not provide meaningful

1 as the bottom/top of a memory string does make sense. YMTC's apparent focus on physical
2 positional relationships (bottom, top, lowest, and highest) is in conflict with the positional
3 relationships of, for example, 2-D NAND technology where YMTC's bottom and top are at the
4 same physical level (at the surface of the substrate). I further note that the '294 patent states "[t]he
5 bottom (or source end) of each NAND string is in contact with the well region, and the top end (or
6 drain end) of each NAND string is connected to a respective bit line," confirming this typical usage.
7 *Id.*, 12:53-56. Moreover, in the '294 patent, "[t]he memory structure can be 2D or 3D." *Id.*, 6:14.

8 156. I understand that YMTC cites to the Merriam Webster Dictionary (2016) (YMTC-
9 MICRON-PA_0010352) in support of its proposed construction. However, the definition it
10 provides is not in the context of NAND memory and does not reflect the plain and ordinary meaning
11 as would be understood by a POSITA as I discuss in this section. That is, this dictionary defines
12 "top" as "the highest part, point, or level of something" and "the upper end, edge, or surface." *Id.*,
13 YMTC-MICRON-PA_0010356. It defines "bottom" as, *e.g.*, "the lowest part or place." *Id.*,
14 YMTC-MICRON-PA_0010355. While it may sometimes be the case that the "top" wordline is
15 physically near the "highest part, point, or level" of a NAND chip along a z-axis (*i.e.*, if that is
16 where the drain is located), that is not in any way definitional of "bottom to top" as used in the '941
17 context of a NAND memory string or wordline. The same is true for YMTC's general purpose
18 dictionary definition of "bottom." It may sometimes be the case that the "bottom" wordline is near
19 the physical bottom of a chip along a z-axis (*i.e.*, if that is where the source is located), but that is
20 merely coincidental, not definitional. And YMTC's dictionary definition makes no sense in the
21 context of planar 2-D NAND or various 3-D NAND architectures (like the U-shaped memory
22 string) already discussed. Thus, to the extent YMTC's construction is using "lowest" and "highest"
23 to define the physical positional coordinates (such as along a z-axis) of the wordlines in a NAND
24 memory, YMTC is incorrect because that is not how a POSITA would have understood the term in
25 the NAND memory context.

26 157. The various textbooks and the exemplary YMTC patent publication discussed above
27 convey a consistent understanding. That is, when one talks about the "bottom" of a NAND memory
28 string (or the wordlines) without any further contextualization or redefinition of that term "bottom",

1 a POSITA would have understood that to be the *source* side in the context of both 2D and 3D
2 NAND memories. Likewise, without any further contextualization or redefinition, a POSITA
3 would have understood the term “top” to mean the *drain* side in the context of both 2D and 3D
4 NAND memories. Therefore, the plain and ordinary meaning of “from bottom to top” as
5 understood by a POSITA would have been “from the source to the drain side.”

6 Executed on the 31st day of January, 2025, in Troy, New York.

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8 I declare under penalty of perjury that the foregoing is true and correct.

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11 E. Fred Schubert, Ph.D.
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