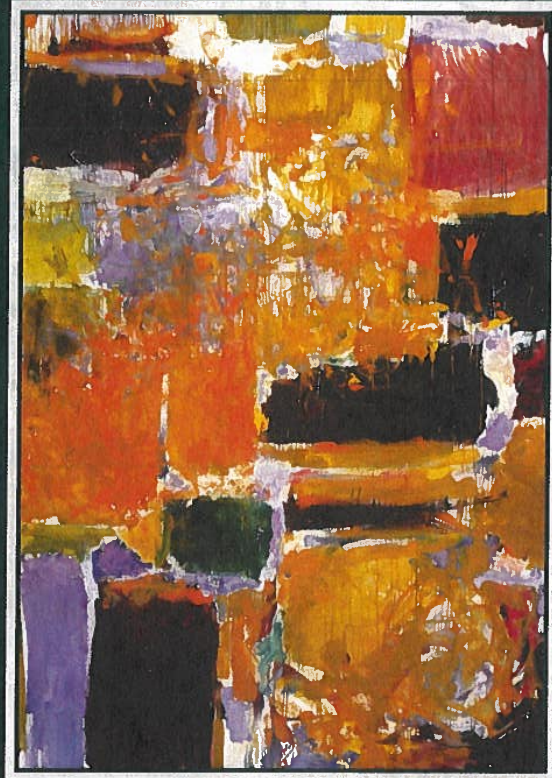


DIGITAL INTEGRATED CIRCUITS

A DESIGN PERSPECTIVE

SECOND EDITION



JAN M. RABAEY
ANANTHA CHANDRAKASAN
BORIVOJE NIKOLIĆ

PRENTICE HALL ELECTRONICS AND VLSI SERIES
CHARLES G. SODINI, SERIES EDITOR

YMTC
Exhibit 2019
Micron v. YMTC
IPR2025-00190

Ex. 2019-001

**DIGITAL
INTEGRATED
CIRCUITS**

A DESIGN PERSPECTIVE

Prentice Hall Electronics and VLSI Series

Charles S. Sodini, Series Editor

LEE, SHUR, FIELDLY, YTTERDAL *Semiconductor Devices Modeling for VLSI*

LEUNG *VLSI for Wireless Communications*

PLUMMER, DEAL, GRIFFIN *Silicon VLSI Technology: Fundamentals, Practice, and Modeling*

RABAEY, CHANDRAKASAN, NIKOLIĆ *Digital Integrated Circuits: A Design Perspective, Second Edition*

DIGITAL INTEGRATED CIRCUITS

**A DESIGN PERSPECTIVE
SECOND EDITION**

Modeling
ve, Second Edition

**JAN M. RABAEY
ANANTHA CHANDRAKASAN
BORIVOJE NIKOLIĆ**

PRENTICE HALL ELECTRONICS AND VLSI SERIES
CHARLES G. SODINI, SERIES EDITOR



Pearson Education, Inc.
Upper Saddle River, New Jersey 07458

Library of Congress Cataloging-in-Publication Data on file.

Vice President and Editorial Director, ECS: *Marcia J. Horton*
Publisher: *Tom Robbins*
Editorial Assistant: *Eric Van Ostenbridge*
Vice President and Director of Production and Manufacturing, ESM: *David W. Riccardi*
Executive Managing Editor: *Vince O'Brien*
Managing Editor: *David A. George*
Production Editor: *Daniel Sandin*
Director of Creative Services: *Paul Belfanti*
Creative Director: *Carole Anson*
Art and Cover Director: *Jayne Conte*
Art Editor: *Greg Dulles*
Manufacturing Manager: *Trudy Piscioti*
Manufacturing Buyer: *Lisa McDowell*
Marketing Manager: *Holly Stark*

About the Cover: Detail of "Wet Orange," by Joan Mitchell (American, 1925–1992). Oil on canvas, 112 × 245 in. (284.5 × 622.3 cm). Carnegie Museum of Art, Pittsburgh, PA. Gift of Kaufmann's Department Store and the National Endowment for the Arts, 74.11. Photograph by Peter Harholdt, 1995.



© 2003, 1996 by Pearson Education, Inc.
Pearson Education, Inc.
Upper Saddle River, NJ 07458

The author and publisher of this book have used their best efforts in preparing this book. These efforts include the development, research, and testing of the theories and programs to determine their effectiveness. The author and publisher shall not be liable in any event for incidental and consequential damages in connection with, or arising out of, the furnishing, performance, or use of these programs.

All rights reserved. No part of this book may be reproduced, in any form or by any means, without permission in writing from the publisher.

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

ISBN 0-13-597444-5

Pearson Education Ltd., *London*
Pearson Education Australia Pty, Ltd., *Sydney*
Pearson Education Singapore, Pte. Ltd.
Pearson Education North Asia Ltd., *Hong Kong*
Pearson Education Canada Inc., *Toronto*
Pearson Educación de Mexico, S.A. de C.V.
Pearson Education—Japan, *Tokyo*
Pearson Education Malaysia, Pte. Ltd.
Pearson Education Inc., *Upper Saddle River, New Jersey*

canvas, 112 x 245 in.
tment Store and the

orts include the devel-
author and publisher
rising out of, the fur-

*To Kathelijn, Karthiyayani, Krithivasan,
and our Parents*

*"Qu'est-ce que l'homme dans la nature?
Un néant a l'égard de l'infini,
un tout al l'égard du néant,
un milieu entre rien et tout."*

*"What is man in nature?
Nothing in relation to the infinite,
everything in relation to nothing,
a mean between nothing and everything."*

Blaise Pascal, *Pensées*, n. 4, 1670.

and noise. For brevity, we limited the listing to the parameters of direct interest to this text. For a complete description of the device models and the usage of SPICE, we refer the reader to the numerous textbooks on the subject. (See, for example, [Banhzaf92], [Thorpe92], and [Vladimirescu93].)

3.3 The MOS(FET) Transistor

The metal–oxide–semiconductor field-effect transistor (MOSFET, or MOS, for short) is certainly the workhorse of contemporary digital design. Its major asset, from a digital perspective, is that it performs very well as a switch, and it introduces very few parasitic effects. Other important advantages are its integration density, combined with a relatively “simple” manufacturing process, which make it possible to produce large and complex circuits in an economical way.

Following the approach we took for the diode, we restrict ourselves in this section to a general overview of the transistor and its parameters. After a generic overview of the device, we present an analytical description of the transistor from both a static (steady-state) and a dynamic (transient) viewpoint. We conclude the discussion with an enumeration of some second-order effects and the introduction of the SPICE MOS transistor models.

3.3.1 A First Glance at the Device

The MOSFET is a four-terminal device. The voltage applied to the *gate* terminal determines if and how much current flows between the *source* and the *drain* ports. The *body* represents the fourth terminal of the transistor. Its function is secondary because it only serves to modulate the device characteristics and parameters.

At the most superficial level, the transistor can be thought of as a switch. When voltage is applied to the gate that is larger than a given value (the *threshold voltage* V_T), a conducting channel is formed between drain and source. In the presence of a voltage difference between the latter two, electrical current flows between them. The conductivity of the channel is modulated by the gate voltage—the larger the voltage difference between gate and source, the smaller the resistance of the conducting channel and the larger the current. When the gate voltage is lower than the threshold, no such channel exists, and the switch is considered open.

Two types of MOSFET devices can be identified. The NMOS transistor consists of n^+ drain and source regions embedded in a p -type substrate. The current is carried by electrons moving through an n -type channel between source and drain. This is in contrast to the pn -junction diode, where current is carried by both holes and electrons. MOS devices can also be made by using an n -type substrate and p^+ drain and source regions. In such a transistor, current is carried by holes moving through a p -type channel. The device is called a p -channel MOS, or PMOS transistor. In a complementary MOS technology (CMOS), both devices are present. The cross section of a contemporary dual-well CMOS process was presented in Chapter 2, and is reproduced here for convenience. (See Figure 3-11.)

ance C_D , which
depletion-region)
in this chapter,
near capacitance

(3.13)

3-1. Besides the
lt value used by
complete—other
n-level injection,

ult Value

0 E-14

1

0

0

0

0.5

1

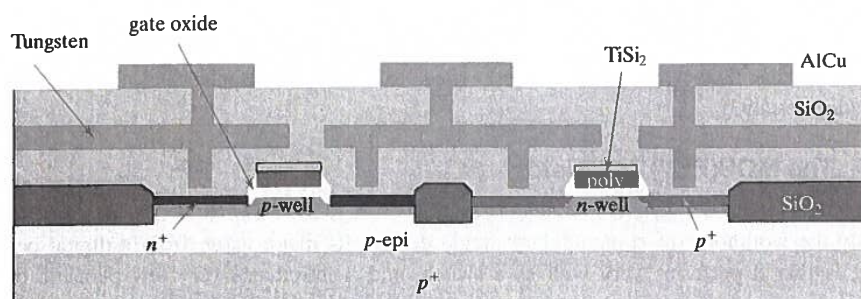


Figure 3-11 Cross section of contemporary dual-well CMOS process.

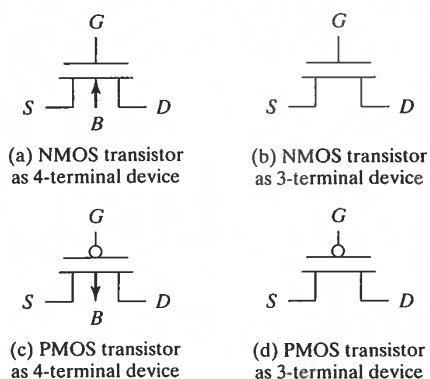


Figure 3-12 Circuit symbols for MOS transistors.

Circuit symbols for the various MOS transistors are shown in Figure 3-12. As mentioned earlier, the transistor is a four-port device, with gate, source, drain, and body terminals (Figure 3-12a and c). Since the body is generally connected to a dc supply that is identical for all devices of the same type (GND for NMOS, V_{dd} for PMOS), most often it is not shown on the schematics (Figure 3-12b and d). **If the fourth terminal is not shown, it is assumed that the body is connected to the appropriate supply.**

3.3.2 The MOS Transistor under Static Conditions

In the derivation of the static model of the MOS transistor, we concentrate on the NMOS device. All of these arguments are valid for PMOS devices as well, and they are discussed at the end of the section.

The Threshold Voltage

Consider first the case in which $V_{GS} = 0$, and drain, source, and bulk are connected to ground. The drain and source are connected by back-to-back pn -junctions (substrate–source and

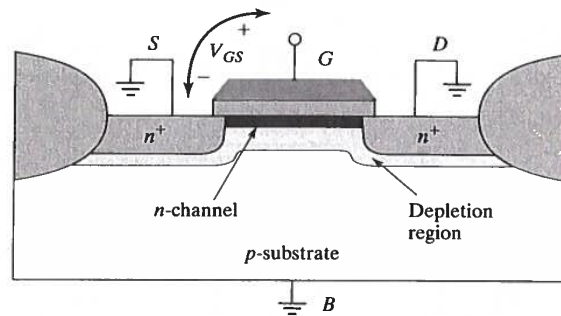


Figure 3-13 NMOS transistor for positive V_{GS} , showing depletion region and induced channel.

substrate–drain). Under the mentioned conditions, both junctions have a 0 V bias and can be considered off, which results in an extremely high resistance between drain and source.

Assume now that a positive voltage is applied to the gate (with respect to the source), as shown in Figure 3-13. The gate and substrate form the plates of a capacitor with the gate oxide as the dielectric. The positive gate voltage causes positive and negative charge to accumulate on the gate electrode and the substrate side, respectively. The latter manifests itself initially by repelling mobile holes. Hence, a depletion region is formed below the gate. This depletion region is similar to the one occurring in a pn -junction diode. Consequently, similar expressions hold for the width and the space charge per unit area. Compare the following expressions with Eq. (3.4) and Eq. (3.5):

$$W_d = \sqrt{\frac{2\epsilon_{si}\phi}{qN_A}} \quad (3.14)$$

and

$$Q_d = \sqrt{2qN_A\epsilon_{si}\phi} \quad (3.15)$$

In these equations, N_A is the substrate doping and ϕ is the voltage across the depletion layer (this is, the potential at the oxide–silicon boundary).

As the gate voltage increases, the potential at the silicon surface reaches a critical value at some point, and the semiconductor surface inverts to n -type material. This point marks the onset of a phenomenon known as *strong inversion*, which occurs at a voltage equal to twice the *Fermi Potential* (Eq. (3.16)) ($\phi_F \approx -0.3$ V for typical p -type silicon substrates):

$$\phi_F = \phi_T \ln\left(\frac{N_A}{n_i}\right) \quad (3.16)$$

Further increases in the gate voltage produce no further changes in the depletion layer width, but result in additional electrons in the thin inversion layer directly under the oxide. These are drawn into the inversion layer from the heavily doped $n+$ source region. Hence, a continuous