

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: April 28, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00190
U.S. Patent No. 11,568,941

PATENT OWNER'S PRELIMINARY RESPONSE

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2001	Defendants' Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)
2002	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2003	Order Granting Stipulation to Extend Certain Deadlines Pursuant to Patent L.R. 4-2 and the Scheduling Order (ECF No. 141) Pursuant to Civil Local Rule 6-1(b), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 8, 2025), ECF No. 194
2004	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 14, 2025), ECF No. 243
2005	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending <i>Inter Partes</i> Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2006	Declaration of Dr. Sunil P. Khatri, Ph.D In Support Of Patent Owner's Preliminary Response ("Khatri")
2007	<i>Curriculum Vitae</i> of Dr. Sunil P. Khatri

Ex.	Description
2008	Soon-Moon Jung et al., <i>Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node</i> , 2006 International Electron Devices Meeting Technical Digest (“Jung”)
2009	Erh-Kun Lai et al., <i>A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory</i> , 2006 International Electron Devices Meeting Technical Digest (“Lai 2006”)
2010	Declaration of E. Fred Schubert, Ph.D. in Support of Defendants’ Proposed claim Constructions (Patent Local Rule 4-3), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv- 05792-RFL (N.D. Cal. Jan. 31, 2025) (“Schubert Decl.”) (excerpts)
2011	U.S. Patent Application Publication No. 2016/0071595 A1 (“Dong III”)
2012	U.S. Patent Application Publication No. 2019/0006021 A1 (“Ghai”)
2013	Excerpts from <i>The Merriam-Webster Dictionary</i> (2016), (“2016 Merriam-Webster Dictionary”)
2014	Excerpts from <i>The American Heritage Dictionary of the English Language</i> (5th ed. 2018) (“2018 American Heritage Dictionary”)
2015	U.S. Patent Application Publication No. 2016/0343414 A1 (“Lee V”)
2016	U.S. Patent Application Publication No. 2016/0099060 A1 (“Yoo”)
2017	Rino Micheloni et al., <i>Inside NAND Flash Memories</i> (2010) (excerpts)
2018	Order Granting Motion to Consolidate, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Aug. 21, 2024), ECF No. 106
2019	Jan M. Rabaey et al., <i>Digital Integrated Circuits: A Design Perspective</i> (2003) (excerpts)

I. Introduction

As explained in this Preliminary Response to the Petition for *inter partes* review of Patent Owner Yangtze Memory Technology Company, Ltd.'s ("YMTC's") U.S. Patent No. 11,568,941 ("941 Patent"), Petitioner fails to show a reasonable likelihood of prevailing as to any claim. All Petitioner's grounds fail for a basic reason—horizontal is the opposite of vertical. Each independent claim requires a memory having vertical structures of word lines arranged "from bottom to top." Petitioner relies exclusively on Dong for this claim element, but Dong only discloses word lines arranged horizontally. Petitioner identifies no teaching or suggestion to reorient Dong's word lines vertically and does not even contend that it would have been obvious to do so. Because Dong's horizontal word line arrangement is the opposite of the claimed vertical word line arrangement, Petitioner fails to show a reasonable likelihood of prevailing as to any claim. The Board should deny institution.

The '941 Patent describes a novel **vertically** arranged three-dimensional memory. Each challenged independent claim recites word lines in a first portion arranged "**from bottom to top**," word lines in a second portion arranged "**from bottom to top**," with the second portion "formed **below**" or "**above** the first portion." Ex. 1001 at 6:55-7:2 (claim 1 ("formed below")), 7:23-34 (claim 5 ("formed above")), 8:15-31 (claim 11 ("formed below")). This vertical structure of word lines

is shown in Figure 8 below, with “a second portion 720 [colored orange] ... formed *below* the first portion 710 [colored blue].” *Id.* at 4:29-36.

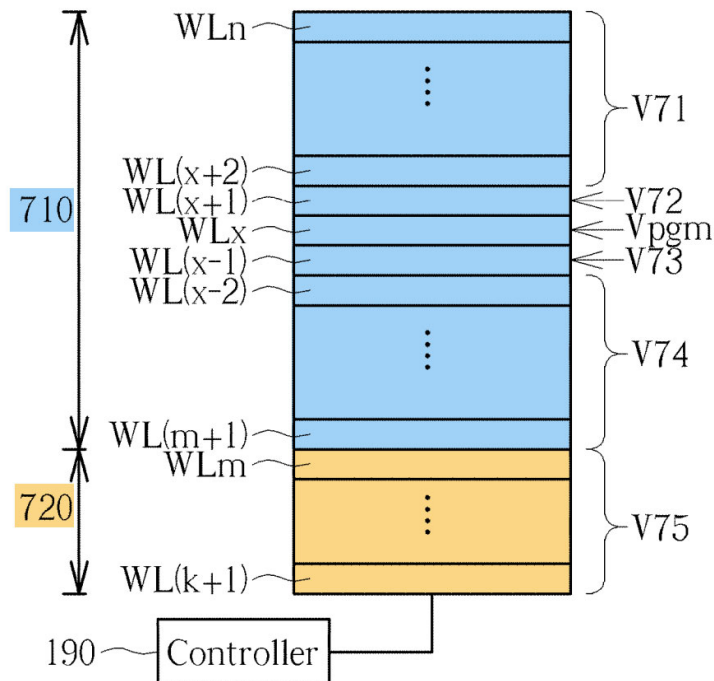


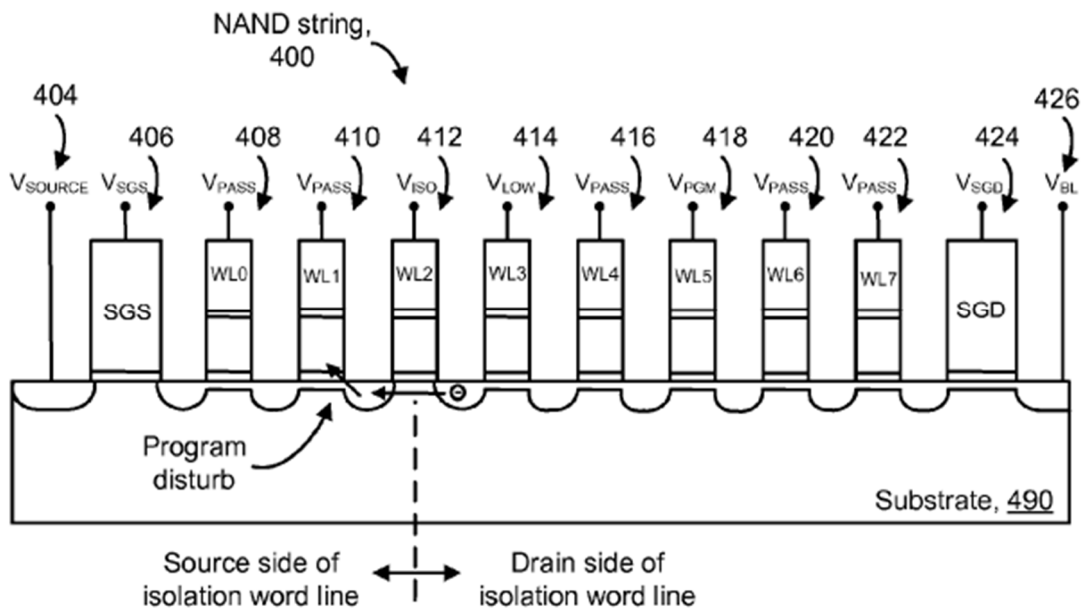
FIG. 8

Id. at Fig. 8.¹ The first portion 710 (blue) includes word line WL_(m+1) to word line WL_n arranged “from bottom to top.” *Id.* at 4:32-34. The second portion 720 (orange) similarly includes word line WL_(k+1) to word line WL_m arranged “from bottom to top.” *Id.* at 4:34-36.

The Petition presents four grounds of purported invalidity, all based on Dong (Ex. 1005). All fail because Dong does not teach or suggest a vertical arrangement

¹ Annotations are added to Figures unless stated otherwise.

of word lines “from bottom to top.” Instead, as shown below in Figure 4, Dong discloses a two-dimensional NAND memory with word lines (WL0 to WL7) arranged horizontally, from left to right.



Ex. 1005 at Fig. 4.

Petitioner resorts to distorting the challenged claims and Dong in three ways to try to read Dong’s horizontal structure onto the claimed vertical structure. **First**, Petitioner argues that the plain meaning of “from bottom to top” is from “source end” to “drain end,” to warp the claims to cover a horizontal arrangement of word lines. But the plain meaning of “bottom” is not “source” and the plain meaning of “top” is not “drain.” The ’941 Patent, which never once depicts or discusses a “source” or “drain,” uses the phrase “from bottom to top” according to its ordinary meaning: from the lowest to highest in a vertical direction. Petitioner’s rewrite of

the claim language is contrary to the intrinsic evidence, the extrinsic evidence, and basic principles of the English language.

Second, Petitioner points to Dong's voltage charts, which for ease of labeling list the word lines and applied voltages in two vertical columns. But these voltage charts do not show the physical structure of Dong's memory. Every memory shown or described in Dong is physically arranged horizontally—not vertically.

Third, Petitioner relies on Dong's statement that, "[i]n some embodiments, the array of storage elements can be three dimensional." But this statement does not teach or suggest arranging word lines vertically. To be sure, there can be three-dimensional arrangements of Dong's memory, but they do not have word lines arranged vertically as recited. Indeed, a person of ordinary skill would not have interpreted Dong's passing mention of a "three dimensional" "array of storage elements" to refer to vertically arranged word lines as taught in the '941 Patent because such structures did not even exist at the time of Dong's filing in May 2007.

Because the claims require a vertical arrangement of word lines but Dong only teaches or suggests a horizontal arrangement of word lines—and Petitioner does not even contend it would have been obvious to modify Dong to create a vertical arrangement—Petitioner fails to show a reasonable likelihood of success for any challenged claim. As a result, the Board should deny institution.

II. Background

A. Technical Background

The NAND flash memory landscape developed significantly from 2000 to today. Khatri (Ex. 2006) ¶36. 3D NAND memory devices are “memory arrays” with memory cells stacked one on top of the other. Memory cells can be written or read by applying a voltage to corresponding conductors that run across the memory array, called “word lines.”² *Id.*

1. Two-Dimensional (2D) or Planar NAND

In 2D or Planar NAND, word lines are arranged horizontally between a source and a drain. Khatri ¶37. That is, the word lines, source terminals, and drain terminals are all physically located on the same horizontal plane above the substrate. *Id.* Figure 2.3 below from Petitioner's Exhibit 1009 shows (a) a top view and (b) a cross-sectional view of an exemplary 2D NAND flash memory.

² For consistency, Patent Owner uses “word line” as in the '941 Patent instead of “wordline” as in other references.

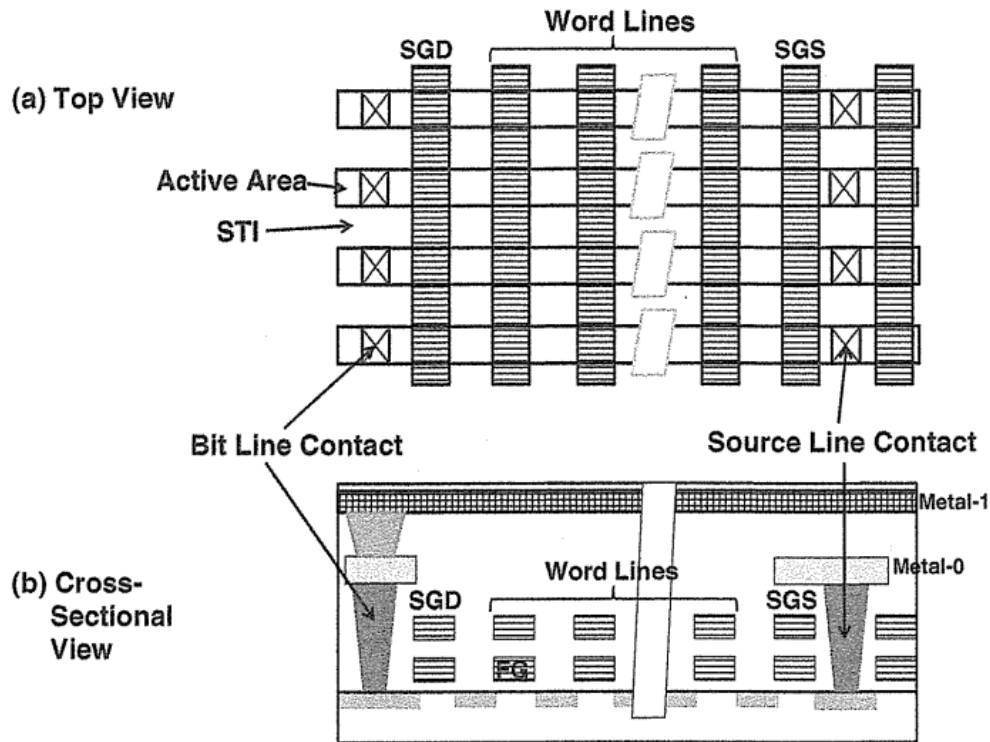


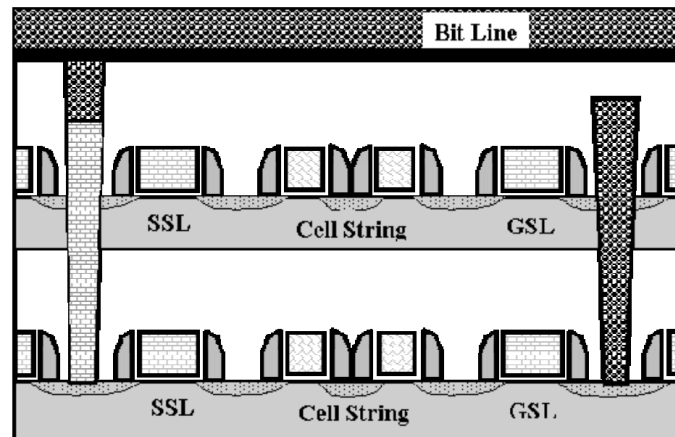
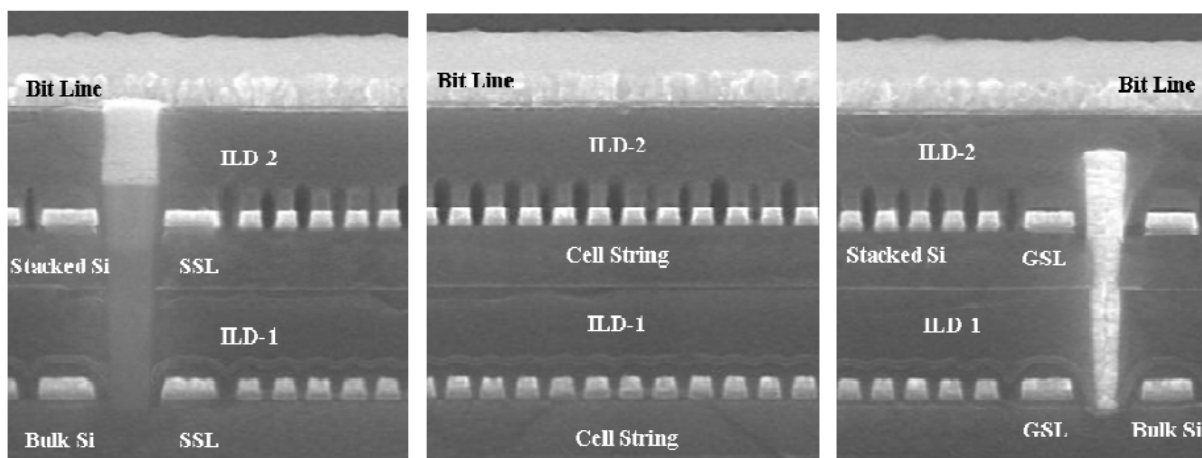
FIGURE 2.3 (a) Top schematic view and (b) cross-sectional view of NAND flash memory cells.

Ex. 1009 pt. 1 at 40; Khatri ¶37. This memory array includes 32 word lines arranged between two select transistors, the source-side transistor (“SGS” or Select Gate Source) and the drain-side transistor (“SGD” or Select Gate Drain)—each arranged on the same horizontal plane above the substrate. Ex. 1009 pt. 1 at 38, 40; Khatri ¶37. However, the scaling of 2D NAND flash memory faced many limitations, including inadvertent programming of memory cells near the cell being programmed, thus resulting in “major scaling limitations.” Ex. 1009 pt. 1 at 150; Khatri ¶37.

2. Three-Dimensional (3D) NAND At The Time Of Dong's Filing Date Included Stacked 2D NAND

To further scale NAND flash memory, some initial 3D NAND designs were available the time of Dong's filing date, May 7, 2007. *See* Dong 1005 at 1. For example, Stacked NAND and Multi Thin-Film Transistor ("Multi TFT") designs "stacked" horizontally arranged NAND memories on top of each other, creating a three-dimensional memory array which did not have vertically arranged word lines. Khatri ¶38.

Stacked NAND, shown below in Figure 7.2, uses that same structure as the traditional 2D NAND, with the source side select transistor ("GSL" or ground select line, near the source), drain side select transistor ("SSL" or string select line, near the drain), and word lines ("Cell String") arranged horizontally. Khatri ¶¶38-39. Rather than only have one level, however, Stacked NAND uses several 2D horizontally arranged NAND layers stacked on top of one another, with each layer of NAND strings arranged in a 2D horizontal manner. Khatri ¶¶38-39.



Ex. 2008 (Jung) at 3, Figs. 3, 4 (showing diagram and physical representations of Stacked NAND). As seen above, the word lines within each layer are still arranged horizontally on a substrate between the source and drain, not vertically. *Id.* at 3 (“In the doubly stacked NAND Flash cell strings of Fig. 3, the cell strings of the upper layers are stacked over the bottom layer ones already formed on the bulk Si Substrate.”); Khatri ¶40.

Multi TFT 3D NAND is similar to the Stacked NAND design, but uses a special type of transistor in the NAND cells (a TFT transistor). Khatri ¶41. For

example, the below Multi TFT 3D NAND shows two two-dimensional NAND layers (“bottom” and “top” layers) with word lines (“channel[s]”) arranged horizontally on a substrate.

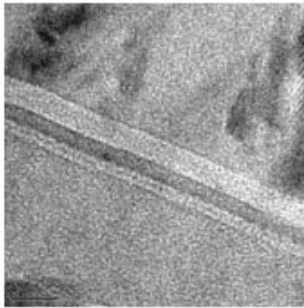


Fig. 1 TEM of the O1/N1/O2/N2/O3 structure for TFT BE-SONOS.

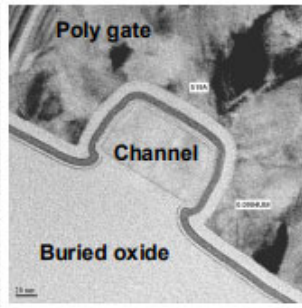


Fig. 2 Tri-gate structure of the TFT device.

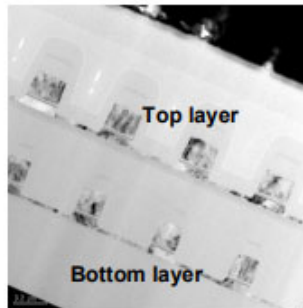


Fig. 3 Channel-length direction of double-layer TFT NAND devices.

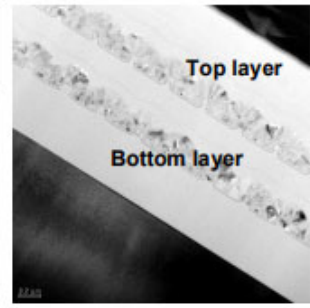


Fig. 4 Channel-width direction of double-layer TFT NAND devices.

Ex. 2009 (Lai 2006) at 4; Khatri ¶41. In other words, like the Stacked NAND design, the word lines in the Multi TFT design are still arranged horizontally, not vertically. Khatri ¶41. Even so, “[t]he program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed.” Ex. 1009 pt. 2 at 354; Khatri ¶42.

B. The '941 Patent (Ex. 1001)

The '941 Patent, filed on September 10, 2021 and claiming priority to a PCT application filed on February 10, 2020, discloses and claims “a solution for reducing program disturbance and pass voltage disturbance when operating a three-dimensional memory.” Ex. 1001 at 1:39-41, 1:19-22; Khatri ¶43. In particular, as “the number of layers is increased” for three-dimensional NAND, pass voltage disturbance occurs and program disturbance “become[s] more significant,” resulting

in “a higher failure rate of programming.” Ex. 1001 at 1:34-38; Khatri ¶43. These issues were especially problematic in three-dimensional NAND memory with a plurality of layers wherein memory cells or word lines are in close proximity. Ex. 1001 at 1:30-41; Khatri ¶43. By applying specific voltages to specific word lines of the 3D NAND memory, the '941 Patent provides a solution to reduce program disturbance and pass voltage disturbance. Ex. 1001 at 6:39-41; Khatri ¶43. The '941 Patent describes this solution in the specification, including with reference to the Figure 8 embodiment.

Figure 8, for example, illustrates a 3D memory including a “first portion 710” (blue) including word lines “WL(m+1)” to “WLn” arranged “from bottom to top.” Ex. 1001 at 4:29-34; Khatri ¶44. The 3D memory also has a “second portion 720” (orange), which is “formed below the first portion 710,” and includes word lines “WL(k+1)” to “WLm” arranged “from bottom to top.” Ex. 1001 at 4:34-36; *see also id.* at 6:55-60 (claim 1), 7:23-28 (claim 5), 8:15-20 (claim 11); Khatri ¶44.

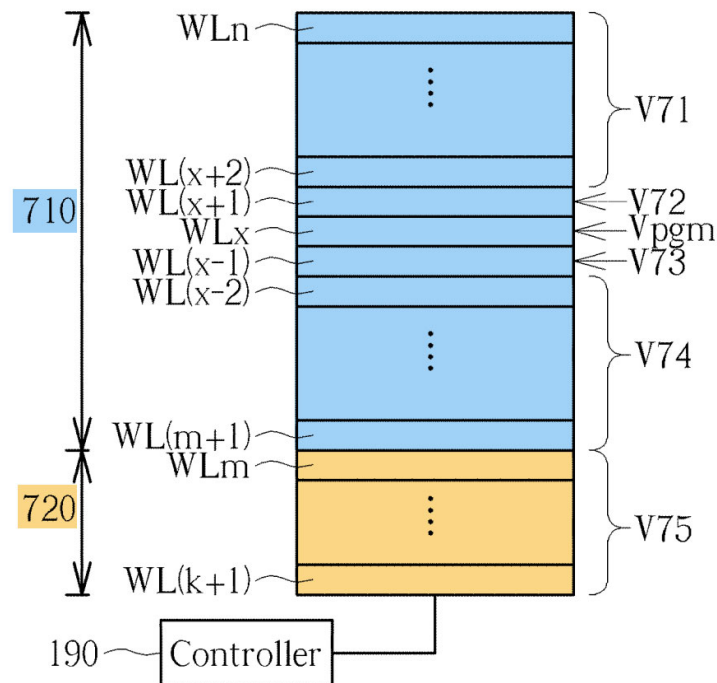


FIG. 8

Ex. 1001 at Fig. 8. A POSITA would also understand, in light of the intrinsic evidence, that the three-dimensional memory of the '941 Patent has a substrate located below and perpendicular to the vertical arrangement of word lines, i.e., a “three-dimensional stack NAND flash memory.” Ex. 1001 at 1:26-29; Khatri ¶44.

Controller 190 applies voltages $V71$, $V72$, $Vpgm$, $V73$, $V74$, and $V75$ to specific word lines of a three-dimensional memory to reduce the effect of program and pass voltage disturbances. Ex. 1001 at 1:30-41, 4:51-61, 6:39-43, Fig. 8. When the x th word line (i.e., “ WLx ”) is programmed, the controller 190 applies a program voltage “ Vpm ” to WLx . *Id.* at 3:9-11. At the same time, the controller 190 applies a first voltage $V71$ to word lines “ $WL(x+2)$ ” to “ WLn ,” a second voltage $V72$ to word line “ $WL(x+1)$,” a third voltage $V73$ to word line “ $WL(x-1)$,” a fourth voltage

V74 to word lines “WL(m+1)” to “WL(x-2),” and a fifth voltage V75 to word lines “WL(k+1)” to “WLm”). *Id.* at 4:37-42, 4:51-59. The '941 Patent also discloses having the fifth voltage V75 be lower than the fourth voltage V74. *Id.* at 4:60-61; Khatri ¶44.

C. Prosecution History

For brevity, YMTC does not address the prosecution history in this Preliminary Response. YMTC's decision not to address the prosecution history here should not be understood as agreement or acquiescence with the statements made by Petitioner regarding the prosecution history. *See* Pet. 22; Khatri ¶45.

D. Person of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art in the field of the '941 Patent “would have had a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) NAND memory devices (including issues relating to the operation, *e.g.*, programming, of said devices), or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may substitute for professional experience).” Pet. 22. Petitioner also claims that a person having ordinary skill in the art (“POSITA”) “would have been aware of and generally knowledgeable about NAND memory's structure and fabrication, its component parts, how it operates, and how it is controlled.” *Id.* at 22-23; Khatri ¶¶32-35.

YMTC takes no position on the level of ordinary skill in the art in this Preliminary Response only, as Petitioner has failed to establish a reasonable likelihood of prevailing under any reasonable definition for a POSITA. Khatri ¶¶32-35.

E. Challenged Claims

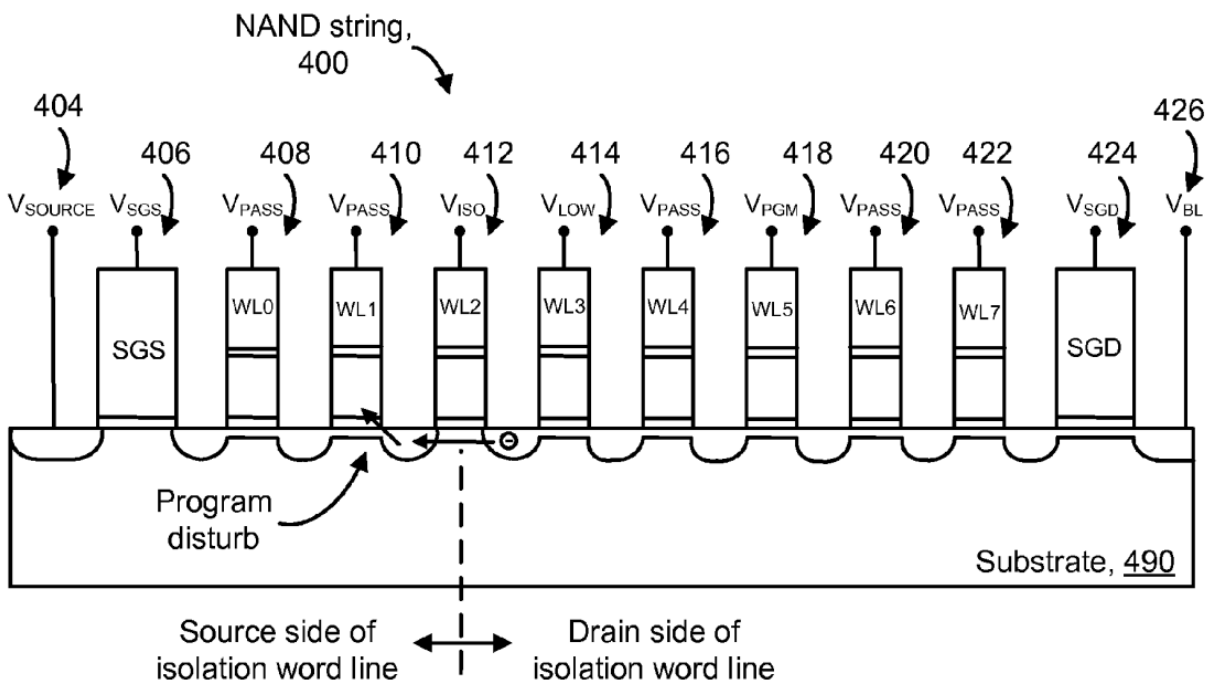
Petitioner presents four grounds to challenge the patentability of claims 1, 3-11, and 13-14 of the '941 Patent. Pet. 7. Each ground relies on Dong (Ex. 1005) as the primary reference. *Id.* In particular, Petitioner alleges that Dong alone anticipates and renders obvious all independent claims (claims 1, 5, and 11) and several dependent claims (claims 3, 6, 7, and 13). *Id.* Petitioner also relies on Dong combined with secondary reference Costa (Ex. 1012) to allege that claims 8-9 are obvious, and on Dong combined with secondary reference Shirai (Ex. 1018) to allege that dependent claims 4, 10, and 14 are obvious. *Id.*; Khatri ¶46.

Since Petitioner exclusively relies on Dong in its challenges to the independent claims, if the Board finds that Dong fails to disclose or suggest at least one limitation present in each independent claim based on Petitioner's arguments, then the Board should deny institution.

F. Dong (Ex. 1005)

Dong discloses a purported solution to address program disturb in two-dimensional NAND memory strings. Ex. 1005 at ¶¶11, 45, Fig. 4. For example,

Figure 4 of Dong illustrates a cross-section of a two-dimensional NAND memory string 400 with storage elements (408, 410, 412, 414, 416, 418, 420, and 422), their corresponding word lines (WL0, WL1, WL2, WL3, WL4, WL5, WL6 and WL7), source-side select gate control line SGS (406), and drain-side select gate control line SGD (424) at the same physical level in a horizontal arrangement above a substrate (490). *Id.* ¶45; Khatri ¶47. As shown below, the word lines (WL0 to WL7) are arranged horizontally, with no word line at the “bottom” or “top” compared to any other word line.



Ex. 1005 at Fig. 4, ¶¶45, 48, 49; Khatri ¶47. The programming voltage V_{PGM} is applied to the fifth word line (418, “WL5”) when it is selected for programming.

Ex. 1005 at ¶¶45-46. As seen above, other voltages V_{PASS} , V_{ISO} , and V_{LOW} are

applied to neighboring word lines of the NAND cell that are not selected for programming. *Id.* ¶46; Khatri ¶47.

G. Claim Construction

In Petitioner's claim construction section, Petitioner alleges "the '941 Patent's claims do not require further construction and should receive their plain and ordinary meaning." Pet. 22. However, when analyzing the '941 Patent claims, Petitioner and its expert rewrite the claimed phrase "from bottom to top" to "from source to drain." Pet. 34-35; Ex. 1004 ¶¶112-113, 120. Petitioner states that "[t]he '941 Patent does not define the phrase *bottom to top*, but it was (and is) common in NAND flash memory devices to refer to the source end of a memory string as the 'bottom,' and the drain end as the 'top.' ... That common usage will be applied here." Pet. 35 (citing Ex. 1004 ¶¶112-113, 120). In the parallel district court litigation, Petitioner's expert Dr. Schubert applied the rewrite in his sworn declaration, stating, "the plain and ordinary meaning of 'from bottom to top' as understood by a POSITA would have been 'from the source to the drain side.'" Ex. 2010 (Schubert Decl.) at 60; Khatri ¶¶48-54.

The Board should reject Petitioner's attempt to rewrite the claim language "from bottom to top" to from "source end" to "drain end." The plain meaning of "bottom" is not "source" and the plain meaning of "top" is not "drain." Khatri ¶55. The plain meaning of "bottom" and "top" is well understood—bottom means lowest

point and top means highest point above the substrate. *See* Ex. 1001 at 1:26-41, 6:39-47; Khatri ¶55. Petitioner's interpretation is contrary to the claims' plain language and the intrinsic record. Khatri ¶55.

The term "from bottom to top" has no special meaning in the semiconductor manufacturing context or in the context of the '941 Patent. Khatri ¶56. Nothing in the '941 Patent or its file history provides any special definition for the phrase "from bottom to top" or disclaims its ordinary meaning. Khatri ¶56. The '941 Patent claims, which recite word lines arranged "from bottom to top," use that phrase in its plain and ordinary sense, simply referring to word lines vertically arranged from lowest (bottom) to highest (top), as the intrinsic evidence confirms. Khatri ¶¶56-58.

To be clear, YMTC does not believe any terms require construction for the Board to deny institution.³ That is, the Board need only apply the plain and ordinary meaning of "from bottom to top," which is not from "source end" to "drain end." Nevertheless, Patent Owner explains why, if the Board were to construe this term, its construction would be—consistent with its plain meaning—from lowest to highest.

³ YMTC reserves the right to advocate for claim constructions if the Board institutes review.

1. The Intrinsic Evidence Shows “From Bottom To Top” Means From Lowest To Highest

The '941 Patent claims refer to word lines in a vertical arrangement by reciting word lines arranged “from bottom to top”:

- “an (m+1)th word line to an nth word line *from bottom to top*” (claims 1, 7, and 11);
- “a first word line to a kth word line *from bottom to top*” (claims 2, 5, and 12); and
- “a (k+1)th word line to an mth word line *from bottom to top*” (claim 11).⁴

The claims confirm this vertical word line arrangement, reciting portions, which consist of word lines, formed “above” or “below” each other (claims 1-3, 5, 7, 11-13) and “dummy word line[s]” formed “above” and “below” other portions (claims 4, 10, 14). Khatri ¶¶59-60.

The specification confirms that the '941 Patent is directed to a three-dimensional NAND memory with word lines arranged vertically, one on top of another. Like the claims, the specification also describes word lines vertically arranged “from bottom to top.” *See, e.g.,* Ex. 1001 at 4:29-36; *see also id.* at Abstract; Khatri ¶¶61-63. For example, Figure 8 below illustrates a three-

⁴ Emphasis added unless stated otherwise.

dimensional memory with a first portion 710 (blue) and a second portion 720 (orange), each including word lines arranged vertically from bottom to top (i.e., from lowest to highest) above the substrate (not shown).

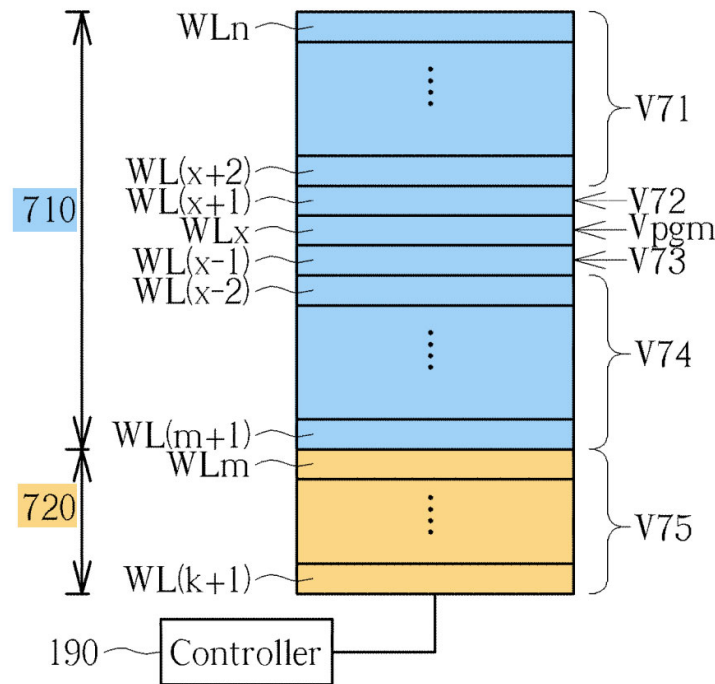


FIG. 8

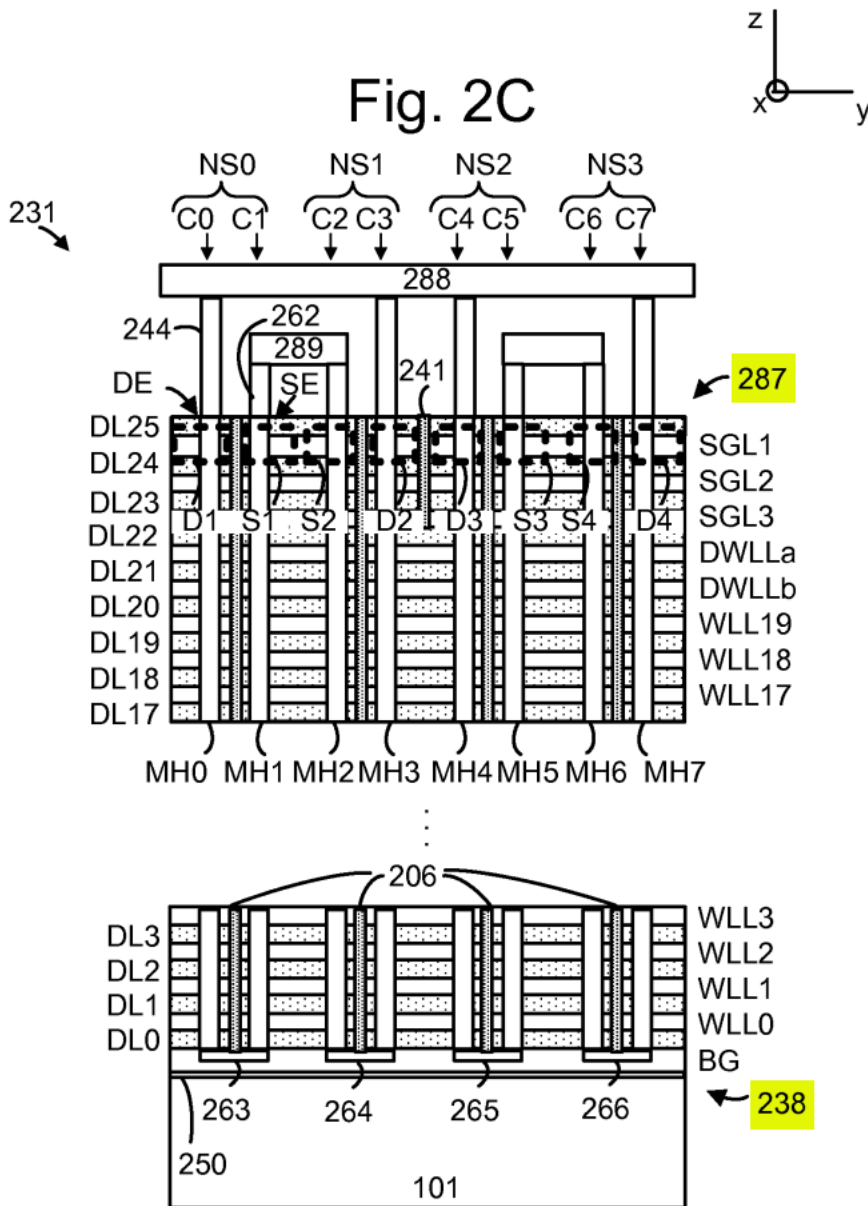
Ex. 1001 at Fig. 8; *see id.* at 1:26-41, 6:39-47; Khatri ¶62. The first portion 710 includes “an (m+1)th word line $WL(m+1)$ to an nth word WLn line **from bottom to top.**” Ex. 1001 at 4:32-34; *see also id.* at Abstract. Consistent with the plain and ordinary meaning of the term “bottom,” the (m+1)th word line is shown as the vertically lowest word line in first portion 710. *Id.* at 4:29-32, Fig. 8; Khatri ¶62. Similarly, and consistent with the plain and ordinary meaning of the term “top,” the WLn word line is shown as the vertically highest word line in first portion 710. Ex. 1001 at 4:29-32, Fig. 8; Khatri ¶62. Second portion 720, described as “formed **below**

the first portion 710,” is vertically lower than the first portion. Ex. 1001 at 4:34-36, Fig. 8; Khatri ¶62. And the “second portion 720” is shown having “a (k+1)th word line WL(k+1) to an mth word line WLm *from bottom to top*”—i.e., vertically from lowest to highest in that portion. Ex. 1001 at 4:34-36, Fig. 8; Khatri ¶62.

Notably, all other figures of the '941 Patent also illustrate word lines arranged vertically, as in Figure 8, reinforcing that the plain and ordinary meaning of “bottom” and “top” applies. Ex. 1001 at Figs. 1-7 and 9-11; Khatri ¶63; *see Seabed Geosolutions (US) Inc. v. Magseis FF LLC*, 8 F.4th 1285, 1287-88 (Fed. Cir. 2021) (determining the plain and ordinary meaning of “fixed” is “attached or fastened” consistent with the specification); *Wis. Alumni Rsch. Found. v. Apple Inc.*, 905 F.3d 1341, 1350-52 (Fed. Cir. 2018) (interpreting a term based on consistent characterization in the specification). The specification further describes this vertical arrangement by referring to “portions” that are “above” or “below” each other, where each “portion” consists of “word lines.” Ex. 1001 at Abstract, 2:65-3:3 (first and second portions), 4:30-36 (same), 1:46-50 (same), 1:56-60 (same), 2:4-6 (same), 2:14-18 (same); *id.* at 3:46-48 (third portion), 5:7-9 (same), 5:32-34 (same); *id.* at 5:4-19 (describing that programming occurs in a word line in a portion “above the lowermost portion”); Khatri ¶64.

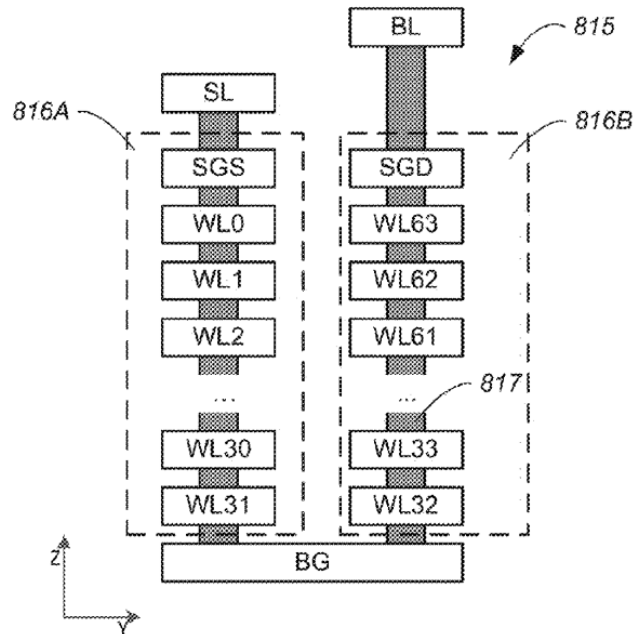
The references cited on the face of the '941 Patent reaffirm that a POSITA would interpret word lines arranged “from bottom to top” to mean from lowest to

highest above the substrate, and not from source to drain. *See Powell v. Home Depot U.S.A., Inc.*, 663 F.3d 1221, 1230-31 (Fed. Cir. 2011) (“prior art cited in a patent or cited in the prosecution history of the patent constitutes intrinsic evidence”); Khatri ¶65. For example, U.S. Patent Publication No. 2016/0071595 (Ex. 2011, “Dong III”)—by the same inventor as Petitioner’s Dong reference (Ex. 1005)—describes a 3D NAND memory stack with “a top 287 and a bottom 238,” referring to the respective highest and lowest portions of the memory stack (i.e., below bit line 288 and vias 244, 262, and above substrate 101).



Ex. 2011 ¶¶75, 77, Fig. 2C; Khatri ¶65.

Similarly, U.S. Patent Publication No. 2019/0006021 (Ex. 2012), also cited on the '941 Patent, discloses a NAND string in a U-shape, “with external elements (source line ‘SL’ and bit line ‘BL’) located at the top of the structure,” and “[a]t the bottom of NAND string 815 is a controllable gate (back gate ‘BG’).”

**FIG. 8**

Ex. 2012 ¶84, Fig. 8; Khatri ¶66. This also shows that Petitioner's claim that "bottom to top" means effectively "source to drain" Pet. 35, is wrong because the word "bottom" is explicitly used to refer *not* to the "source," but to the vertically lowest element, the "back gate." Similarly, the word "top" is used to refer *not* to the drain, but to the two elements (source line and bit line) shown vertically highest. Khatri ¶66. Because the intrinsic evidence establishes that "from bottom to top" in the context of the '941 Patent has its plain and ordinary meaning of from vertically lowest to vertically highest, the Board need not consider any extrinsic evidence. See *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (when "an analysis of the intrinsic evidence alone will resolve any ambiguity in a disputed claim term[,] ... it is improper to rely on extrinsic evidence"); *Phillips v. AWH Corp.*,

415 F.3d 1303, 1318, 1320-22 (Fed. Cir. 2005) (recognizing extrinsic evidence “as less reliable than the patent and its prosecution history in determining how to read claim terms,” and cautioning against “plac[ing] too much reliance on extrinsic sources” which “focus[] the inquiry on the abstract meaning of words rather than on the meaning of claim terms within the context of the patent”); Khatri ¶¶67.

To the extent the Board considers the extrinsic evidence, however, even Petitioner's own cited references show that “from bottom to top” means from lowest to highest. Petitioner's Exhibit 1009 uses the terms “top” and “bottom” to describe the vertically highest and vertically lowest physical components of 3D NAND memory—not where the source or drain are. *See, e.g.*, Ex. 1009 pt. 2 at 327 (“the charge trap nitride layer is physically connected from top to bottom [control gates] in 3D SONOS/TANOS NAND flash”); Khatri ¶¶68-69. This extrinsic evidence in the semiconductor field aligns with the ordinary meaning in the Merriam-Webster Dictionary, which defines “bottom” as “the lowest part or place” and “top” as “the highest part, point or level of something.” Ex. 2013 (2016 Merriam-Webster Dictionary) at 83, 752; *see also* Ex. 2014 (2018 American Heritage Dictionary) (defining “bottom” as “the deepest or lowest part” and “top” as “the uppermost part, point, surface or end”); Khatri ¶¶70.

2. Petitioner's Proposed Construction Improperly Relies Solely on Extrinsic Evidence

Petitioner does not even try to argue that the intrinsic evidence supports its incorrect interpretation that “from bottom to top” means “from source to drain”—it does not support such a construction. Petitioner's sole mention of the '941 Patent is to allege that it “does not define the phrase bottom to top.” Pet. 35; Ex. 1004 ¶120. But a patent need not (and preferably does not) define plain and ordinary English words. Petitioner also ignores the '941 Patent's consistent usage of the phrase “bottom to top” to refer to the vertically lowest and highest word lines respectively, consistent with the plain and ordinary meaning of this phrase. *Supra* at Section II.G.1; Khatri ¶71.

No intrinsic evidence supports Petitioner's construction that “from bottom to top” means “from source to drain.” Khatri ¶72. Indeed, the figures of the '941 Patent do not even show the source or drain of the inventive memory. The claims do not recite a “source” or a “drain.” *See* Ex. 1001 at 6:55-8:54. And the specification never once refers to or depicts the “source” or “drain” ends of a memory string, much less use those never-described elements to define the “bottom” and “top.” *Nystrom v. TREX Co.*, 424 F.3d 1136, 1144-46 (Fed. Cir. 2005) (construing a term at odds with the intrinsic record “violates the principles articulated in *Phillips*”); *In re Smith Int'l, Inc.*, 871 F.3d 1375, 1383 (Fed. Cir. 2017) (correct claim construction must “correspond[] with ... how the inventor describes

his invention in the specification, *i.e.*, an interpretation that is ‘consistent with the specification’” (citation omitted)). Petitioner’s construction thus ***relies solely on extrinsic evidence***, which is legally improper. *See Seabed Geosolutions*, 8 F.4th at 1287 (vacating and remanding PTAB decision that construed a claim term “based entirely on extrinsic evidence”).

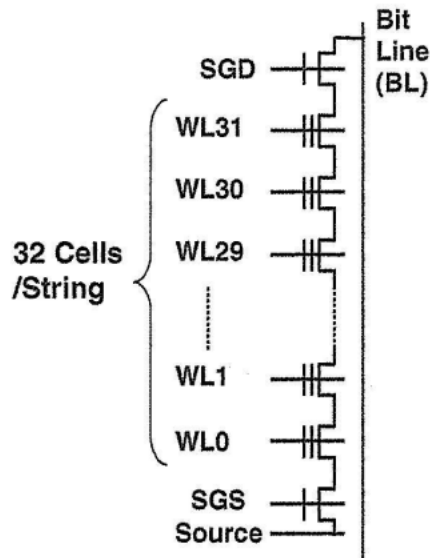
Petitioner’s approach to rewriting the claim is wrong as a matter of law. When the specification does not define a term and there is no prosecution history disclaimer (as here), the correct construction should “not depart from the natural reading of a phrase.” *Columbia Ins. Co. v. Simpson Strong-Tie Co.*, Nos. 2021-2145, 2021-2157, 2023 WL 2733427, at *7 (Fed. Cir. Mar. 31, 2023). Yet that is exactly what Petitioner proposes here, arguing that the lack of explicit definition in the patent justifies rewriting the claim, contrary to its plain language, to have an entirely different meaning.

Even if the Board were to look to on extrinsic evidence, the extrinsic evidence does not consistently teach that “bottom” means closest to the source and “top” means closest to the drain. Petitioner asserts that “it was (and is) common in NAND flash memory devices to refer to the source end of a memory string as the ‘bottom,’ and the drain end as the ‘top.’” Pet. 35 (citing Ex. 1004 ¶¶112-113, 120). In support, Petitioner relies on its expert’s interpretation of circuit diagrams (not physical memories) for 2D NAND flash memories, which he says show “the source end of

the NAND string at the bottom, and the drain end of the NAND string at the top.”

Ex. 1004 ¶113; Pet. 35. But none of the examples cited by Petitioner's expert actually use the word “bottom” to refer to the word line closest to the source or the word “top” to refer to the word line closest to the drain. Khatri ¶73.

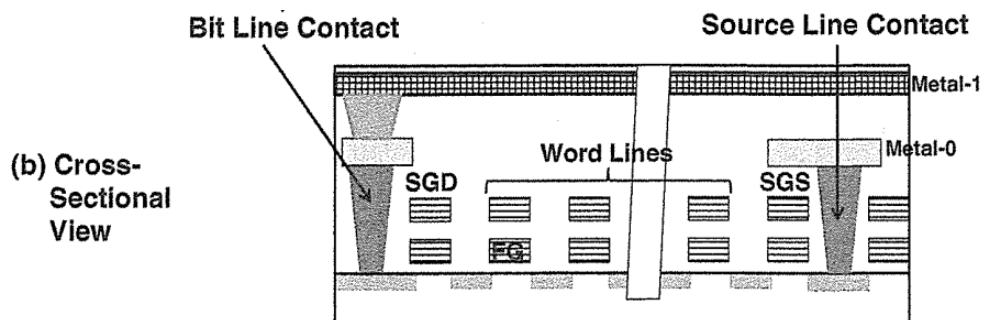
For example, Petitioner's expert refers to the following circuit diagram from Exhibit 1009:



Ex. 1009 pt. 1 at 39 (Fig. 2.2); Ex. 1004 ¶113. This figure shows a circuit diagram for a 2D NAND flash memory consisting of several word lines (“WL0” to “WL31”) and select transistors “SGD” and “SGS” to isolate the NAND string. Ex. 1009 pt. 1 at 39 (Fig. 2.2); Khatri ¶74. SGD is connected at the drain end (the bit line end) of the NAND string, while SGS is connected at the source end of the NAND string. See Ex. 1004 ¶113; Khatri ¶74. But the diagram above is not a representation of the physical layout of the memory, as a POSITA would readily understand, at least

because it uses circuit symbols for flash and NMOS transistors. Khatri ¶74; *see, e.g.*, Ex. 2017 at 7, Fig. 2.1 (illustrating a physical representation of a floating gate memory cell next to its circuit symbol seen in circuit diagrams); Ex. 2019 at 8-9, Figs. 3-13 (physical representation of an NMOS transistor), 3-12(b) (circuit symbol for an NMOS transistor). Notably, no substrate is identified because it is a circuit diagram. Khatri ¶74.

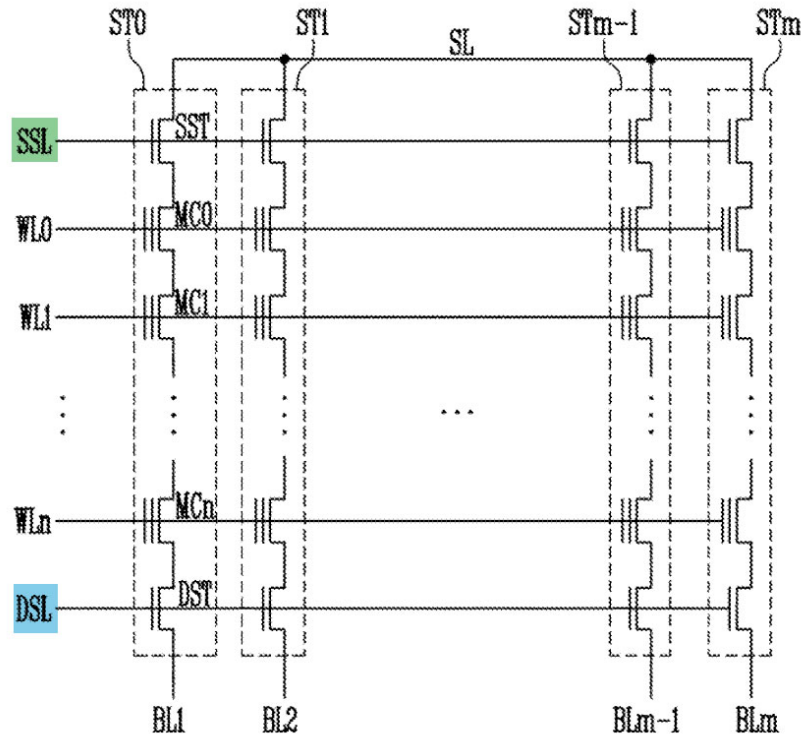
Diagrams like the above are merely symbolic depictions of the circuit and its connectivity, and do not reflect the actual, physical arrangement of word lines on the memory. Khatri ¶75. Petitioner's expert confirms that the circuit diagrams he relies on, including the one above, "are discussing two-dimensional NAND flash memories." Ex. 1004 ¶113. While the circuit diagram shown above is oriented vertically, two-dimensional NAND flash memories have word lines physically arranged in a horizontal plane above the substrate, i.e., from left to right, as seen in the below figure:



Ex. 1009 pt. 1 at 38-40, Fig. 2.3 (cropped); Khatri ¶75. In this physical planar structure, word lines are not physically arranged "from bottom to top" because they

are not arranged in a vertical direction at all. Khatri ¶75. Moreover, despite Petitioner's argument that it is common convention to do so (Pet. 35), none of Petitioner's cited circuit diagrams use the word "bottom" to refer to the source, or "top" to refer to the drain. Khatri ¶75.

Even if Petitioner were correct that its few cited references placed the source end of a memory string at the bottom, many other references show different arrangements, disproving Petitioner's suggestion that it was common convention for "bottom to top" to effectively mean "source to drain." *See* Pet. 35 (citing Ex. 1004 ¶¶112-113, 120); Khatri ¶76. For example, U.S. Patent Publication No. 2016/0343414 (Ex. 2015, "Lee V"), cited on the '941 Patent, provides a circuit diagram of a memory string with the source ("SSL" or "source select line," in green) at the top and the drain ("DSL" or "drain select line," in blue) at the bottom:



Ex. 2015 at Fig. 2, ¶¶15, 44-46; Khatri ¶¶76-77. To the extent that Petitioner’s cited diagram from Figure 2.2 of Ex. 1009 is (incorrectly) viewed as showing the memory’s physical structure, the above diagram from Ex. 2015 shows the opposite arrangement—source at the top and drain at the bottom. Khatri ¶¶76-77.

Furthermore, in two-dimensional memory arrays (such as those discussed above) the word lines are physically arranged horizontally from left to right; neither the source nor the drain is at the “bottom” or “top” because they are at the same physical height above the substrate. Khatri ¶78. For example, the Aritome reference cited by Petitioner illustrates a physical diagram of a two-dimensional NAND flash memory array with the source (near the “SGS” or the source select gate, in green)

and the drain (near the “SGD” or drain select gate, in blue) at the same physical level as the word lines above the substrate:

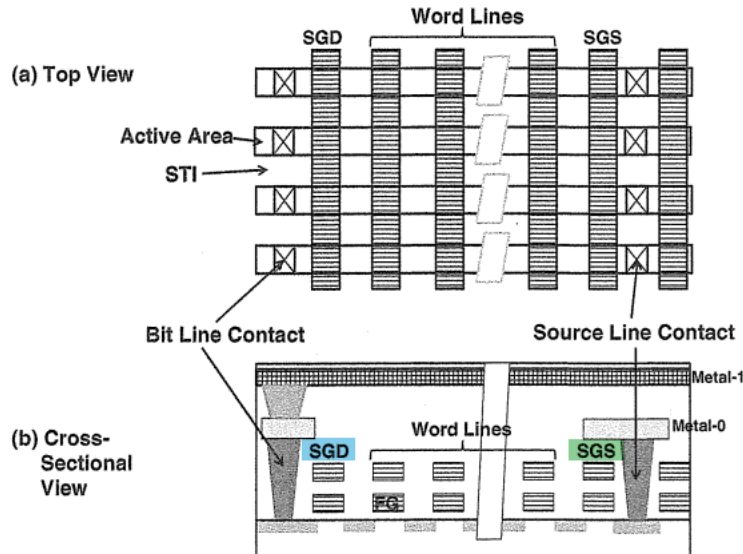


FIGURE 2.3 (a) Top schematic view and (b) cross-sectional view of NAND flash memory cells.

Ex. 1009 at 39-40; Khatri ¶78.

If Petitioner’s construction were adopted, it would lead to the absurd conclusion that, as Petitioner’s expert in the district court litigation admitted, the “bottom and top are at the same physical level.” Ex. 2010 (Schubert Decl.) at 59; Khatri ¶79. In other words, Petitioner’s construction would effectively rewrite “from bottom to top” in the claims to “from source to drain,” rendering both “bottom” and “top” meaningless (e.g., Petitioner effectively proposes that “from bottom to top” in the two-dimensional memory array from Ex. 1009 above means “from right to left”). See *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 810 (Fed. Cir.

2021) (“It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.”).

Petitioner’s rewrite makes no sense because, even in a three-dimensional NAND memory structure, the “source” is not necessarily at the “bottom” and the “drain” is not necessarily at the “top.” Khatri ¶80. Indeed, both the “source” and the “drain” can be at the “top.” *Id.* For example, U.S. Patent Publication No. 2019/0006021 (Ex. 2012, “Ghai”), cited by the ’941 Patent, depicts the physical structure of a U-shaped three-dimensional NAND memory where both the source (near the source select line “SGS,” green) and the drain (near the drain select line “SGD,” blue) are at the top, as shown in Figure 8 below.

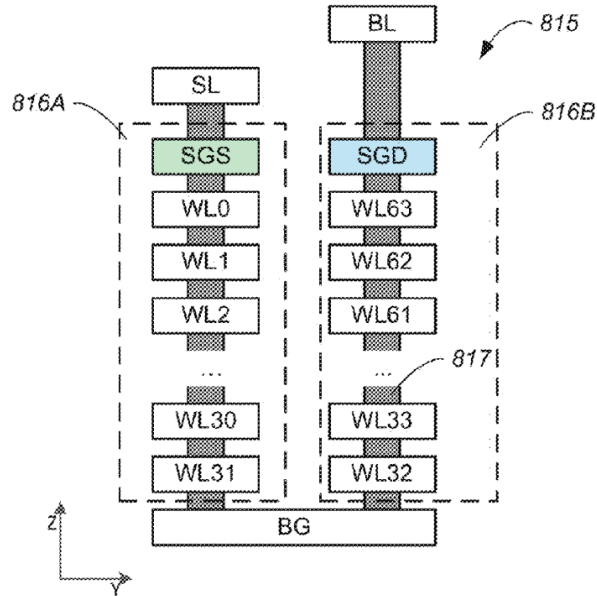
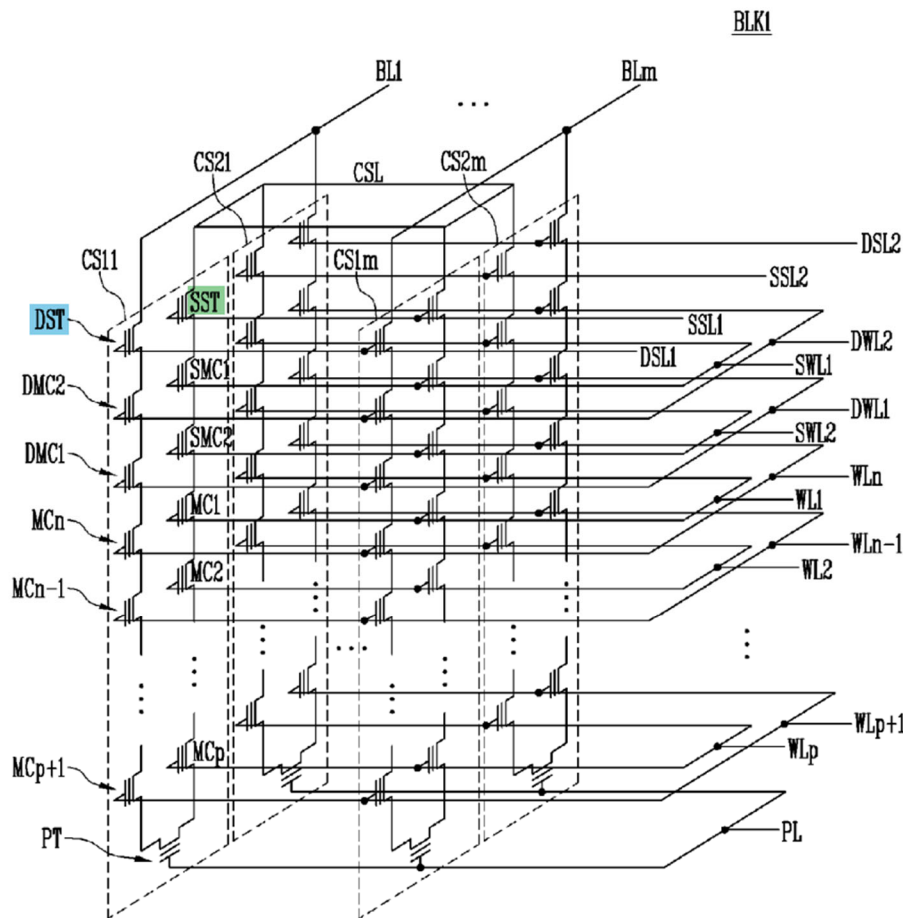


FIG. 8

Ex. 2012 (Ghai) at Fig. 8 (“SGS” stands for “source select line”; “SGD” stands for “drain select line”); *see also id.* ¶¶16-17, 80, 84-87, Fig. 9; Khatri ¶80. If incorrectly

one assumes (as Petitioner does) that circuit diagrams show physical structure, then U.S. Patent Publication No. 2016/0099060 (“Yoo”), also cited on the face of the ’941 Patent, shows a U-shaped memory string with both the source (near the “SST” or “source select transistor,” in green) and the drain (near the “DST” or “drain select transistor,” in blue) at the top:



Ex. 2016 (Yoo) at Fig. 3, ¶¶50-65; Khatri ¶81; *see also* Ex. 1008 (cited on the face of the ’941 Patent) at Fig. 13, ¶¶115-129 (reference cited on the face of the ’941 Patent describing a circuit diagram of a U-shaped three-dimensional NAND memory with the source and drain select transistors (SST and DST respectively) at the top).

In light of the above examples, Petitioner cannot reasonably argue that “it was (and is) common in NAND flash memory devices to refer to the source end of a memory string as the ‘bottom,’ and the drain end as the ‘top.’”⁵ *See* Pet. 35; Khatri ¶81.

In sum, Petitioner's proposed construction of “from bottom to top” drastically deviates from the plain English meaning of the term and the intrinsic evidence, and is not even supported by extrinsic evidence. Khatri ¶83. Indeed, Petitioner's expert admits that his interpretation makes it irrelevant “whether the physical device is in a horizontal or vertical direction.” Ex. 1004 ¶113. Petitioner's proposed rewrite is simply an improper attempt to map the claimed vertical arrangement of word lines to Dong's horizontal arrangement of word lines in hindsight.

III. Dong Does Not Disclose Word Lines Arranged “From Bottom To Top”

Under the plain and ordinary meaning of “from bottom to top”—i.e., from lowest to highest—all Petitioner's grounds fail because they exclusively rely on

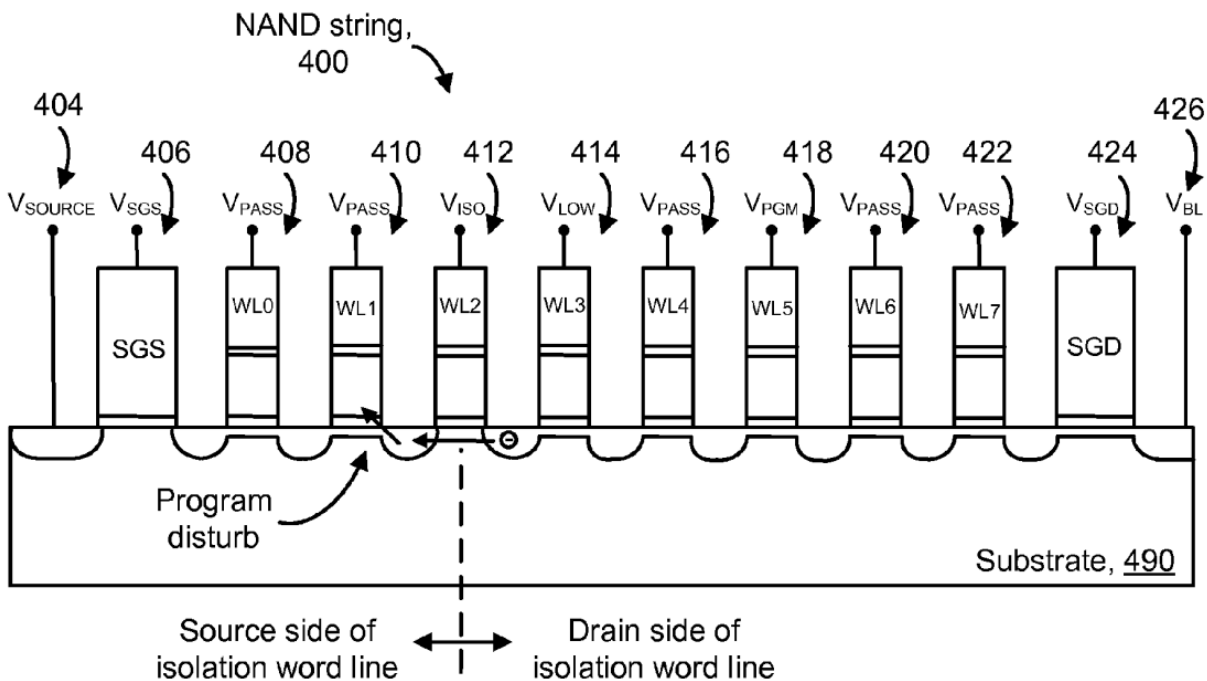
⁵ In support of its claim construction position, Petitioner also cites paragraph 112 of its expert's declaration, which states that “it was well-known to POSITA's [sic] that programming typically proceeded one cell at a time, either from source to drain or from drain to source depending on the architecture of the system.” Pet. 35 (citing Ex. 1004 ¶112). This is irrelevant to the meaning of “from bottom to top.” Khatri ¶82.

Dong for the elements of the challenged independent claims. Pet. 2, 7, 35. Dong does not anticipate or render obvious the independent claims of the '941 Patent because it does not disclose or suggest the claimed word lines vertically arranged “from bottom to top,” i.e., from lowest to highest. Instead, Dong teaches word lines arranged horizontally, i.e., from left to right, above the substrate. Petitioner argues that “to the extent *bottom to top* is interpreted to require vertical strings in a 3D NAND memory, Dong discloses its ‘array of storage elements can be three dimensional’ and shows Fig. 5a in a vertical orientation which satisfies the claim.” Pet. 35. But as explained below, the teaching that an “array of storage elements can be three dimensional” is not a teaching or suggestion to have word lines arranged vertically, and Figures 5a and 5g do not show the physical structure of the word lines. Khatri ¶¶84-95.

A. Dong's Word Lines Are Arranged In A Horizontal Plane Above the Substrate, Not “From Bottom To Top”

Dong teaches that its memory is 2D or Planar NAND, having word lines arranged horizontally—not from “bottom to top,” as claimed in the '941 Patent. Khatri ¶85. Petitioner points to Dong's disclosure of a “memory die 1298” which “*includes a two-dimensional array of storage elements 1100.*” Pet. 34 (citing Ex. 1005 at ¶95, Fig. 12), 51 (addressing preamble of claim 1 by citing back to claim 5), 68 (addressing preamble of claim 11 by citing back to claim 1). Figure 4 (copied below) illustrates a “cross-sectional view” of a two-dimensional “NAND string”

with storage elements (408, 410, 412, 414, 416, 418, 420, and 422), their corresponding word lines (WL0, WL1, WL2, WL3, WL4, WL5, WL6 and WL7), source-side select gate control line SGS (406), and drain-side select gate control line SGD (424) at the same physical level above a substrate (490). Ex. 1005 at ¶¶19, 45, 48, 49; Khatri ¶85.

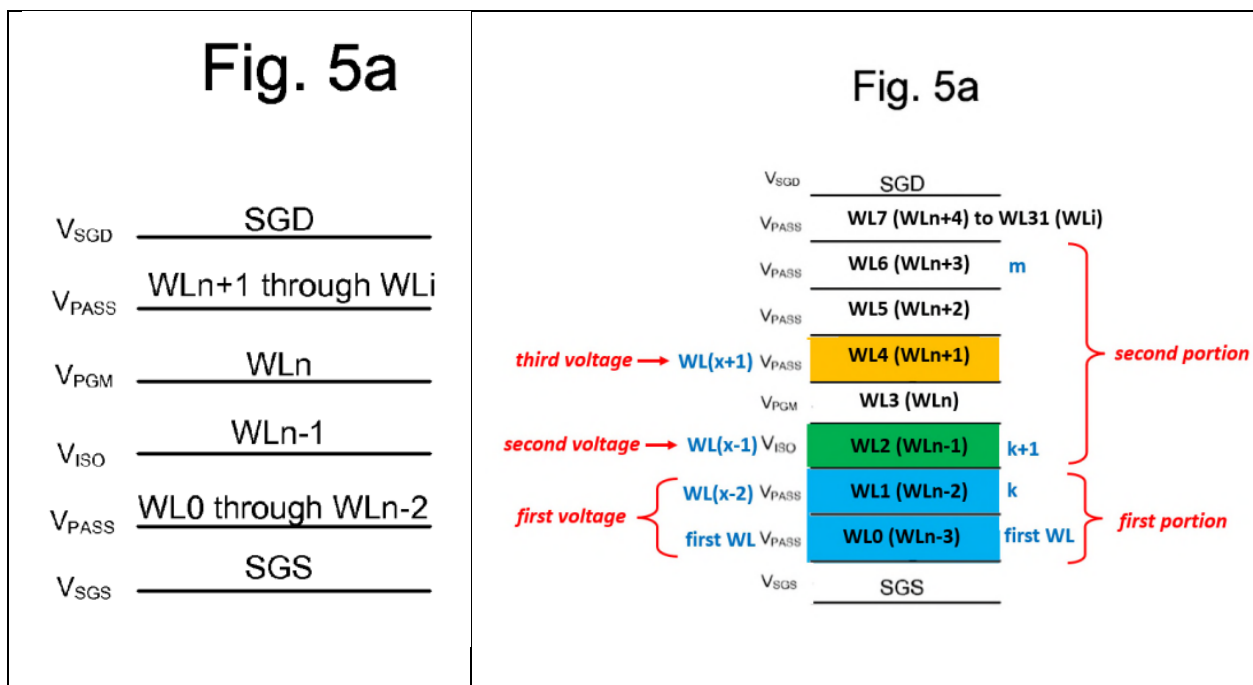


Ex. 1005 at Fig. 4. As shown in Figure 4 above, the word lines (WL0 to WL7) are arranged horizontally, from left to right. *Id.* at Fig. 4; Khatri ¶85.

Although Figure 4 shows the memory's physical structure, Petitioner relies on Dong's voltage charts in Figures 5a and 5g, which do not show physical structure, for the "bottom to top" claim limitations. *See* Pet. 29-38 (claim 5), 52-53 (claim 1), 68 (claim 11). These charts simply represent which voltages are applied to which

word lines. As Dong explains, “FIGS. 5a-h depict different examples of self-boosting modes,” showing voltages applied differently to the word lines. Ex. 1005 at ¶20. They are presented vertically, as most lists are, for ease of reading. But they do not represent—and cannot alter—the actual physical arrangement of the word lines in the memory, which is horizontal as shown in Dong’s Figure 4, as would be expected from two-dimensional NAND memory arrays. Khatri ¶86.

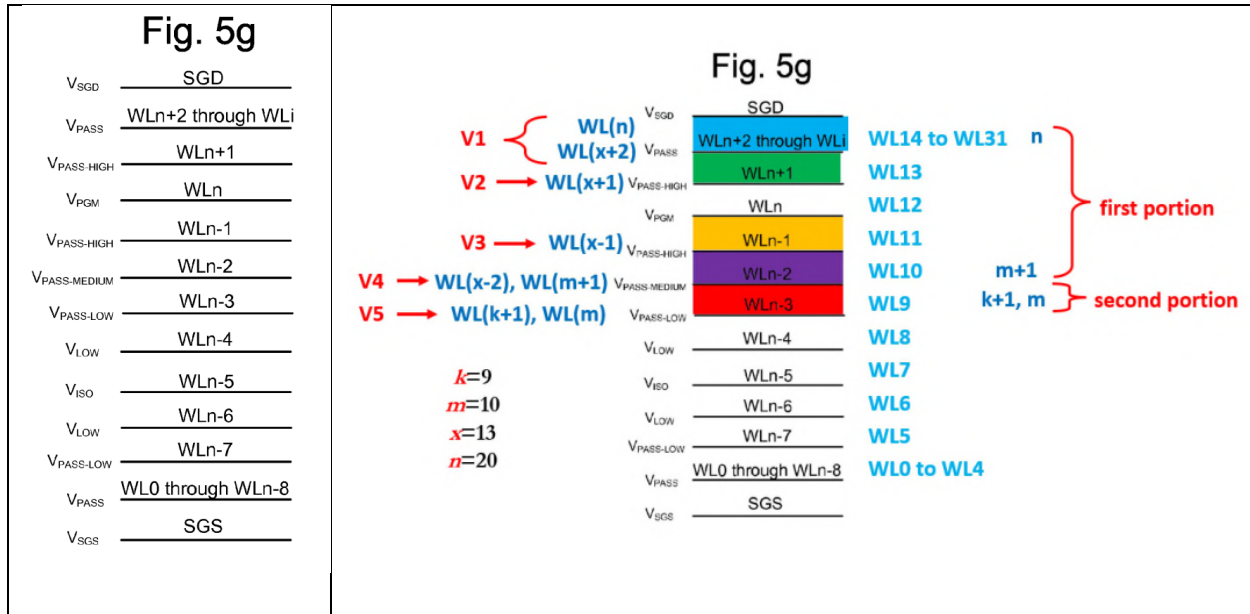
For independent claim 5, for example, Petitioner annotates Dong’s voltage chart in Figure 5a as shown below:



Original Figure 5a

Petitioner's Annotated Figure 5a

Pet. 33 (claim 5); *see id.* at 31 (Petitioner’s sole obviousness position for claim 5 to utilize a 32-cell memory string in Figure 5a); Khatri ¶87. For independent claims 1 and 11, Petitioner similarly annotates Dong’s voltage chart in Figure 5g:



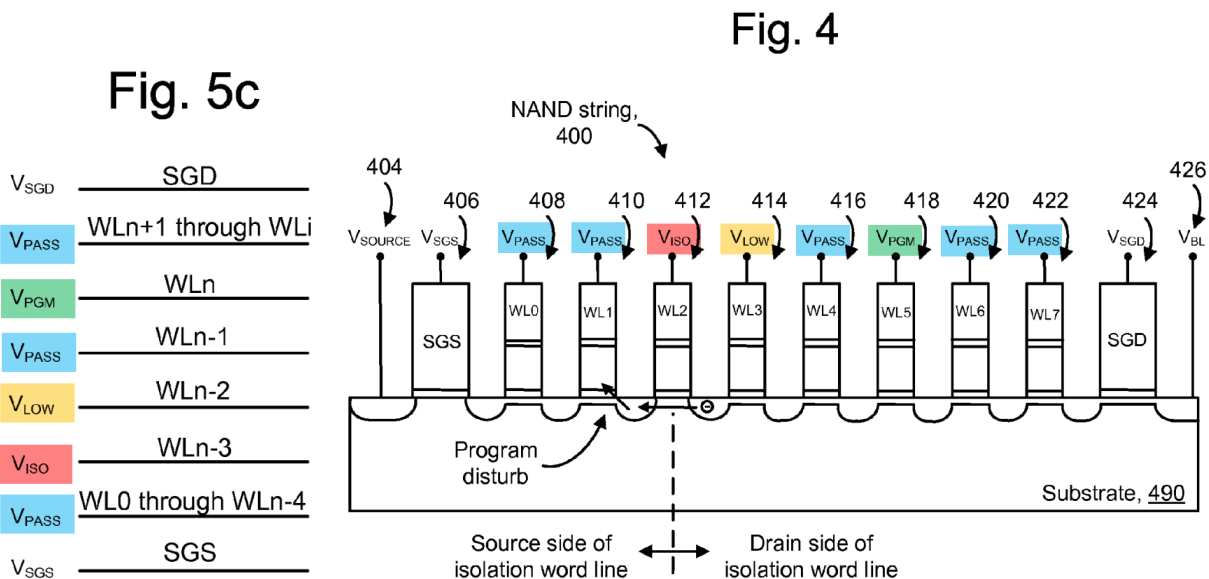
Original Figure 5g

Petitioner's Annotated Figure 5g

Pet. 51 (claim 1); *see id.* at 31 (Petitioner's sole obviousness position for claim 5 regarding Figure 5a to utilize a 32-cell memory string); *id.* at 50 (Petitioner referring back to Petitioner's sole obviousness position for claim 5 at Pet. 31 to allege Dong's Fig. 5g with a 32-cell memory string reads on claim 1); *id.* at 68 (Petitioner addressing claim 11 by referring back to claim 1); Khatri ¶88.

But Figures 5a and 5g, like all of Dong's voltage charts, merely list in two vertical columns which voltages are applied to which word lines. Like flow charts or box diagrams, these voltage charts do not represent the physical arrangement of any word lines in a memory, let alone word lines arranged "from bottom to top" as the independent claims of the '941 Patent require. *See, e.g.,* Ex. 1005 at ¶¶20, 47, 87; Khatri ¶89. Notably, Figures 5a and 5g do not identify a substrate. Instead, the

physical arrangement of the memory is shown in Figure 4, which depicts a two-dimensional memory array with word lines arranged in a horizontal plane above the substrate. Ex. 1005 at ¶¶45, 65; Khatri ¶89. As shown below, the voltages applied to word lines in the voltage chart of Figure 5c correspond to the labeled voltage inputs in the physical memory structure shown Figure 4:



Ex. 1005 at Figs. 4, 5c, ¶¶45 (In Figure 4, “a revised erased self-boosting (REASB) mode, such as depicted in Fig. 5c, is used.”), 54 (“FIG. 5c depicts another ... self-boosting mode. ... This boosting mode is also discussed in connection with FIG. 4.”); Khatri ¶¶90-91.

As highlighted in green above, V_{PGM} is applied to WL5 (418) in Figure 4, just as V_{PGM} is applied to WLn in Figure 5c (in other words, n=5 in Figure 5c). Ex. 1005 at ¶¶45-46, 54, Figs. 4, 5c; Khatri ¶92. As another example, as highlighted in blue

above, V_{PASS} is applied to WL4 (416) in Figure 4, just as V_{PASS} is applied to $WLn-1$ in Figure 5c. Ex. 1005 at ¶¶45-46, 54, Figs. 4, 5c; Khatri ¶92.

Importantly, word lines WL4 (416) and WL5 (418), as well as all of the other word lines, are physically arranged next to each other horizontally in the memory array, as shown in the “cross-sectional view” of the “NAND string” in Figure 4. Ex. 1005 at ¶19; Khatri ¶93. The word lines are not arranged “from bottom to top.” The column structure in Figure 5c is only a diagrammatic representation of voltages applied to the word lines in a particular mode—not a representation of how the word lines are arranged in the physical memory, which is instead shown in Figure 4. Ex. 1005 at ¶45, Figs. 4, 5c; Khatri ¶93.

The same is true of Dong's Figures 5a and 5g relied on in the Petition. *See* Pet. 29-44 (relying on Fig. 5a for claim 5), 50-66 (relying on Fig. 5g for claim 1), 68-70 (referring back to Fig. 5g for claim 11). Figures 5a and 5g are charts that indicate which voltages are applied to the word lines that are physically arranged horizontally, as shown in Figure 4. Khatri ¶94. Like Figure 5c, Dong describes Figures 5a and 5g in the context of Figure 4's two-dimensional NAND string. Ex. 1005 at ¶47 (“FIGS. 5a-h depict different examples of self-boosting modes.”), ¶59 (“FIG. 5g depicts another revised erased area self-boosting mode.”); Khatri ¶94. Dong relies on elements of Figure 4, like “substrate 490” and “word line 412,” to describe the operation of the “revised erased area self-boosting mode” (“REASB”)

described in Figure 5g, confirming that the Figure 5 diagrams correspond to the physical arrangement of Figure 4. Ex. 1005 at ¶¶59, 65 (“With the EASB or REASB boosting modes, ... a channel area of the substrate 490 on a source-side of the isolation word line 412 is isolated from a channel area of the substrate on a drain-side of the isolation word line 412.”); *see also id.* ¶67 (recognizing a “hot carrier injection” program disturb occurring with “EASB and REASB” is depicted in Figure 4 “where the arrows depict electrons moving across the channel under the isolation storage element 412 and into the floating gate of storage element 410”); *compare id.* ¶65 (describing that, for EASB or REASB modes, “ V_{ISO} is applied to one or more source-side neighbors of the selected word line”), *with id.* ¶49 (stating, “[a] low isolation voltage V_{ISO} , in a typical range of 0-4V, is applied to the word line which is adjacent to the selected word line on the source side, in the example of FIG. 5a”), Figs. 5a, 6 (showing the source-side neighbor of the selected word line receiving V_{ISO}); Khatri ¶94.

Thus, a POSITA would understand that the voltage charts of Figures 5a and 5g refer to the word lines that are physically arranged in a horizontal plane above a substrate, as shown in Figure 4. Khatri ¶95. No other conclusion is reasonable, because Figure 4’s “cross-sectional view of a NAND string” is the *only* depiction in Dong of how its word lines are physically arranged. Ex. 1005 at ¶45; Khatri ¶95. Dong’s voltage charts cannot meet the Petitioner’s burden to demonstrate the

existence of word lines physically arranged “from bottom to top” as claimed. *See, e.g., NanoCollect Biomedical, Inc. v. Cytonome/ST, LLC*, IPR2020-00546, Paper 15 at 27-31 (PTAB Aug. 31, 2020) (denying institution in part because a prior art reference generic disclosure of control ports “does not disclose specific structure” of a buffer as recited).

B. Dong's Passing Reference To “Three-Dimensional” Storage Does Not Disclose Or Suggest Vertically Arranged Word Lines As Recited

Besides Dong's voltage charts, Petitioner points only to a single sentence referencing three-dimensional storage—“In some embodiments, the array of storage elements can be three dimensional”—and simply assumes, without explanation, that this refers to vertically arranged word lines. Ex. 1005 at ¶95; *see* Pet. 35. But this is not a reference to word lines arranged vertically and perpendicular to a substrate, and Petitioner does not even argue that it would have been obvious to use vertically arranged word lines. Khatri ¶¶96-102. This sentence in Dong does not refer to any particular arrangement of word lines, and does not disclose the claimed invention, which requires “[a] memory” with a “first portion” having word lines vertically arranged “from bottom to top,” a “second portion formed below the first portion” having word lines vertically arranged “from bottom to top,” and applying specific voltages to particular word lines. *See, e.g.,* Ex. 1001 at 6:55-7:2 (claim 1); Khatri ¶96.

Petitioner's anticipation argument (Ground 1) fails because Dong's single mention of "three-dimensional" fails to disclose "all elements of [the] claimed invention *arranged as in the claim.*" *Therasense, Inc. v. Becton, Dickinson & Co.*, 593 F.3d 1325, 1332 (Fed. Cir. 2010). As described above, Dong's voltage charts like Figure 5a do not disclose the physical arrangement of its word lines, and the cross-sectional view in Figure 4 expressly shows that they are arranged horizontally. Khatri ¶¶97. The reference to "three-dimensional" storage is insufficient to disclose the specific three-dimensional memory as claimed with word lines arranged vertically "from bottom to top," and therefore insufficient for anticipation. *NetMoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008) ("[U]nless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations *arranged or combined in the same way as recited in the claim*, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate."); Khatri ¶¶97. Petitioner does not explain, for example, why a reference to "three-dimensional" storage would have taught arranging word lines bottom to top, rather than horizontally.⁶ That Petitioner does

⁶ In addition, Dong's single reference to a "three-dimensional" array of storage elements does not provide enough information for a POSITA to make and use a three-dimensional memory as claimed with word lines arranged vertically "from

not try to do so is unsurprising. As explained in the following section, a reference to “three dimensional” storage would not have taught arranging word lines vertically as recited. Khatri ¶97.

Petitioner's obviousness argument based on Dong (Ground 2) fails for the same reason. Importantly, Petitioner ***does not argue*** that it would have been obvious to turn Dong's horizontally arranged word lines into vertically arranged word lines. *See Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312) (Petitioner bears “the burden from the onset to show with particularity why the patent it challenges is unpatentable.”). Petitioner proposes no such modification of Dong, provides no reason to modify Dong to have vertical word lines, and offers no basis to support that a POSITA would have had a reasonable expectation of success in doing so. Khatri ¶¶99-100. Petitioner's obvious argument

bottom to top.” *See Forest Laboratories, Inc. v. Ivax Pharms., Inc.*, 501 F.3d 1263, 1268, (Fed. Cir. 2007) (“A reference that is not enabling is not anticipating.”); *Impax Laboratories, Inc. v. Aventis Pharms., Inc.*, 545 F.3d 1312, 1314 (Fed. Cir. 2008) (“In order to anticipate a claimed invention, a prior art reference must enable one of ordinary skill in the art to make the invention without undue experimentation. ... [T]he prior art must enable the claimed invention.”); Khatri ¶98; *see also* Section III.C *infra* (regarding knowledge of a POSITA at the time of Dong's filing).

has nothing to do with the claim requirement that word lines are arranged “from bottom to top.” Pet. 31.

Petitioner only relies on obviousness to argue that “it would have been obvious to a POSITA to utilize a 32-cell memory string”—an entirely different limitation not relevant to this paper. Pet. 31. Thus, with respect to the claim limitation “from bottom to top,” Petitioner’s Ground 1 and Ground 2 are identical and fail for the same reason—there is no teaching of word lines arranged from “bottom to top” in Dong. Khatri ¶¶100-101.

Petitioner cannot incorporate an argument not made in the Petition by citing its expert’s declaration. *See 3M Co. v. Evergreen Adhesives, Inc.*, 860 F. App’x 724, 726 (Fed. Cir. 2021) (affirming PTAB’s decision that 3M failed to meet its burden because “3M’s filings never sufficiently made the relevant ‘contention’ or argument at all, and instead supported 3M’s position entirely by reference to [its expert’s] declarations and testimony”); 37 C.F.R. § 42.6(a)(3) (“Arguments must not be incorporated by reference from one document into another document.”). And Petitioner simply did not make any argument in its Petition that arranging word lines vertically would have been obvious in view of Dong. Instead, Petitioner chose to rely on Dong alone, focusing on Dong’s sole mention of “three dimensional” and “Fig. 5a in a vertical orientation” to disclose the “bottom to top” limitation. Pet. 35;

id. at 7 (“Ground 2: Dong renders obvious claims 1, 3, 5-7, 11, and 13 under §103.”); Khatri ¶¶100-101.

Regardless, even considering the argument in Petitioner’s expert declaration—not made in the Petition—does not help Petitioner. *Compare* Pet. 35, with Ex. 1004 ¶120. Petitioner’s expert states in a bare, conclusory manner that “given the similarities between 2D and 3D NAND discussed in the Technology Background section, even a 2D memory string would at a minimum render obvious the **bottom to top** requirement, even if narrowly construed.” Ex. 1004 ¶120; Khatri ¶102. Petitioner’s expert offers no explanation to support this *ipse dixit* testimony. Petitioner’s expert’s conclusory assertions cannot meet its burden as a matter of law. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (An assertion of obviousness “cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”); *see, e.g., Apple Inc. v. Voip-Pal.com, Inc.*, 976 F.3d 1316, 1325 (Fed. Cir. 2020) (affirming the PTAB’s decision, recognizing the Board maintained “the proper evidentiary standard” by rejecting expert testimony that provided “only ‘conclusory and insufficient’ reasons”); *Securus Techs., Inc. v. Glob. Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. 2017) (affirming the Board in its finding that conclusory expert testimony was not enough for Petitioner to “meet its burden of presenting a sufficient rationale to support an obviousness conclusion”).

Moreover, while Petitioner did not make the argument in Petitioner's expert declaration and it is not in the Petition, a POSITA would not be motivated to apply Dong's program disturb methods for 2D NAND cells to vertical 3D NAND cells at least because vertical 3D NAND cells have vertically stacked cells that exhibit more complex disturb mechanisms that can lead to increased errors during programming. Ex. 1009 pt. 2 at 354 (recognizing "[t]he program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed"), 356 ("The program disturb conditions and characteristics of 3D cells are greatly changed from that of 2D cells."), 362 ("Program disturb phenomena and mechanisms of a 3D NAND cell are much different from that of a 2D NAND cell."); Khatri ¶102. For example, vertical 3D NAND cells have new program disturb mechanisms not present in 2D NAND because vertical 3D NAND cells have "N strings in one block [that] are connected to the same bit line through different select transistors of DSL_1 to DSL_N," whereas "[i]n the case of a 2D NAND cell, one string in the block is connected to one bit line." Ex. 1009 pt. 2 at 362-63; Khatri ¶102.

In a precedential opinion, the Board denied institution where (as here) an expert offered only conclusory testimony, even where (unlike here) the Petition included the relevant argument. *See, e.g., Xerox Corp. v. Bytemark*, IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential) (PTAB denying institution

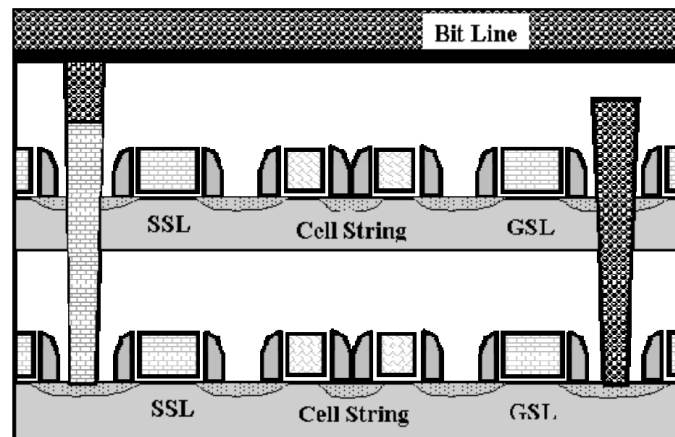
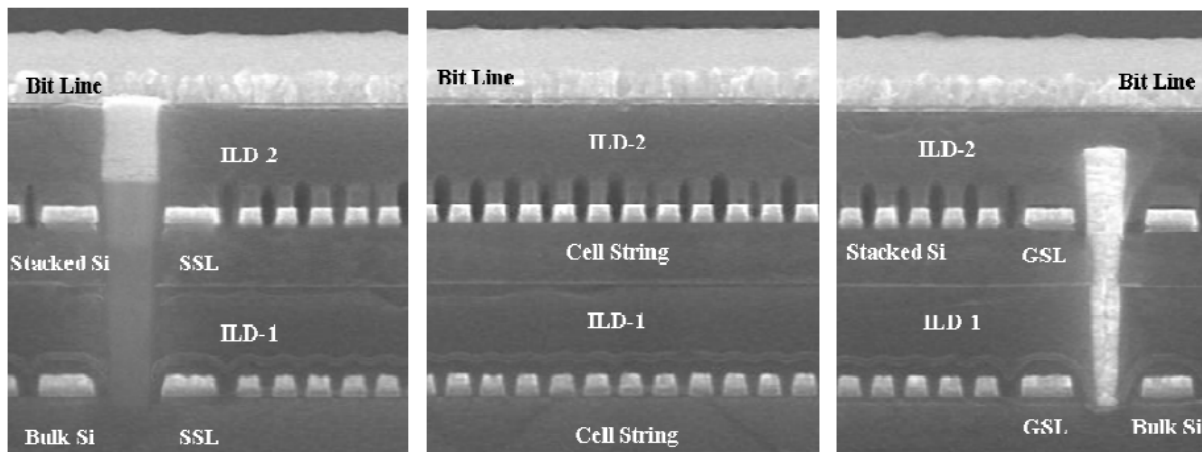
recognizing that “the cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight”). Accordingly, even if Petitioner’s expert’s argument absent from the Petition were considered, it fails to support a reasonable likelihood of showing any claim unpatentable because the argument is no more than a conclusory assertion, unsupported by any articulated reasoning.

C. Dong’s “Three-Dimensional” Disclosure In May 2007 Does Not Refer To 3D NAND Designs With Word Lines Arranged Vertically As Recited

As described above, Petitioner’s reliance on Dong’s single mention of “three-dimensional” memories to assume that Dong discloses the claimed vertical word lines arranged “from bottom to top” is legally erroneous, and institution should be denied for that reason alone. Petitioner’s argument also is factually wrong.

Dong’s disclosure of “three-dimensional” memory arrays refers to 3D memory arrays known as of Dong’s May 7, 2007 filing date. *See Lynk Labs, Inc. v. Samsung Elecs. Co.*, 125 F.4th 1120, 1126-27 (Fed. Cir. 2025) (“[A] published patent application—this *specific* type of ‘printed publication’—is deemed prior art as of its filing date.”). At that time, a POSITA would be aware of three-dimensional storage designs like Stacked NAND and Multi TFT 3D NAND that did not have vertically arranged word lines. Khatri ¶¶103-105. Those three-dimensional memory arrays had several layers of horizontal 2D NAND arrays stacked one on top of the

other, with the source side select transistor (“GSL” or ground select line, near the source), drain side select transistor (“SSL” or string select line, near the drain), and word lines (“Cell String”) arranged horizontally (as in Dong), as shown below.



Ex. 2008 (Jung) at 3, Figs. 3, 4; Ex. 2009 (Lai 2006) at 4; Khatri ¶104. As shown above, the word lines are arranged horizontally in each layer—not vertically—and there are multiple layers of horizontally arranged word lines. Khatri ¶104. These three-dimensional memory arrays do not have word lines arranged vertically “from bottom to top” as recited in each independent claim of the ’941 Patent.

Thus, at the time of Dong's May 7, 2007 filing, "three-dimensional" memory would not have been understood by a POSITA to disclose a memory structure with word lines arranged vertically "from bottom to top," as recited in the independent claims of the '941 Patent. Khatri ¶105. This may explain why Petitioner did not try to explain Dong's reference to "three-dimensional" storage. Explaining it would not have helped Petitioner because it refers to "three-dimensional" arrays of that time with word lines arranged horizontally. Petitioner has failed to meet its burden to establish a reasonable likelihood of showing any challenged claim is unpatentable.

IV. Conclusion

For the reasons set forth above, the Board should deny the Petition for *Inter Partes* Review.

Respectfully submitted,

Dated: April 28, 2025

By: / Inge A. Osman /

Inge A. Osman (Reg. No. 74,480)
inge.osman@lw.com
Latham & Watkins LLP
555 Eleventh Street, NW, Ste. 1000
Washington, D.C. 20004-1304
Telephone: 202.637.2200
Fax: 202.637.2201

*Counsel for Patent Owner
Yangtze Memory Technologies
Company, Ltd.*

CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Preliminary Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(1) because the Patent Owner's Preliminary Response contains 8,977 words using Microsoft Word's counting feature, excluding the cover page, signature block, and the parts of the Patent Owner's Preliminary Response exempted by 37 C.F.R. § 42.24(b)(1).

By: / Inge A. Osman /

Inge A. Osman (Reg. No. 74,480)
inge.osman@lw.com
Latham & Watkins LLP
555 Eleventh Street, NW, Ste. 1000
Washington, D.C. 20004-1304
Telephone: 202.637.2200
Fax: 202.637.2201

*Counsel for Patent Owner
Yangtze Memory Technologies
Company, Ltd.*

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 28th day of April, 2025, a true and correct copy of the foregoing **Patent Owner's Preliminary Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

Jeremy Jason Lang
Travis Jensen
Jared Bobrow
Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road
Menlo Park, CA 94025-1015
T: 650-614-7400
F: 650-614-7401
jlang@orrick.com
tjensen@orrick.com
jbobrow@orrick.com
PTABDocketJL2@orrick.com
T61PTABDocket@orrick.com
PTABDocketJ3B3@orrick.com
micron-ymtc_ohs@orrick.com

By: / Inge A. Osman /

Inge A. Osman (Reg. No. 74,480)
inge.osman@lw.com
Latham & Watkins LLP
555 Eleventh Street, NW, Ste. 1000
Washington, D.C. 20004-1304
Telephone: 202.637.2200
Fax: 202.637.2201

*Counsel for Patent Owner
Yangtze Memory Technologies
Company, Ltd.*