

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No. IPR2025-00190
U.S. Patent No. 11,568,941

**PETITIONER'S OPPOSITION TO PATENT OWNER'S BRIEF ON
DISCRETIONARY DENIAL**

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1010	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1012	U.S. Patent Publication No. 2018/0012667 (“Costa”)
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1022	Yeh et al., “Z-Interference and Z-Disturbance in Vertical Gate- Type 3-D NAND,” <i>IEEE Transactions on Electron Devices</i> , Vol. 63, No. 3, March 2016, pp. 1047-1053
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1061	Yoko Kubota et al., <i>U.S. Chip Equipment Suppliers Suspend Business Activities at Yangtze Memory</i> , WALL STREET JOURNAL CHINA (Oct. 13, 2022) (https://cn.wsj.com/articles/美国供应商暂停在中国长江存储科技的业务活动-11665617406) (“WSJ China Article”)
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1066	U.S. Department of Defense, <i>DOD Releases List of People’s Republic of China (PRC) Military Companies in Accordance with Section 1260H of the National Defense Authorization Act for Fiscal Year 2021</i> (Jan. 31, 2024) (https://www.defense.gov/News/Releases/Release/article/3661985/dod-releases-list-of-peoples-republic-of-china-prc-military-companies-in-accord/)

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I. INTRODUCTION

Petitioner Micron submits this opposition to Patent Owner YMTC's Brief on Discretionary Denial (Paper 10, "DD Brief"). This IPR—along with all the other still-pending IPRs/PGR Micron filed against YMTC's patents—should proceed to a merits decision.

The public has a strong interest in reviewing the patents that YMTC has asserted. Micron—the target of YMTC's infringement allegations—is a U.S.-based semiconductor memory innovator and manufacturer. Indeed, it is the only such U.S. manufacturer. YMTC is a Chinese-state owned entity that operates to further the Chinese government's goal of expanding its global influence in the semiconductor field. IPR here is not only appropriate, but necessary to ensure that an entity operating at the behest of a foreign state is not asserting invalid patents to improperly suppress, undermine, and capture an important part of the U.S. economy.

YMTC argues that the mere fact that it chose to assert 19 patents against Micron in district court somehow warrants denial of IPR. The Board, however, routinely handles more than a thousand post grant filings a year. Micron's filings represent only a very small percentage of this. Moreover, this is a problem of YMTC's own making. If it did not want its patents subject to post-grant proceedings, it should have been more circumscribed when selecting which patents to assert in the first place. Instead, YMTC chose to assert 19 patents. YMTC's complaint that

Micron cannot invoke the AIA to defend itself against this type of onslaught rings hollow. Asserting numerous patents does not (and cannot) operate as a get-out-of-the-PTAB free card. Holding otherwise will incentivize other patent holders to flood district courts with excessive numbers of patent infringement allegations.

The *Fintiv* factors also heavily favor institution. The district court stayed the parallel district court action at least until the completion of all Micron IPRs/PGR. Thus, no trial (or any other district court work) will take place until well after the IPRs/PGR conclude. Moreover, Micron's IPRs/PGR will undeniably simplify the complex issues before the district court. The number of asserted YMTC patents is likely to be substantially reduced. And the Board's findings—regardless of whether they favor Micron or YMTC—will inform the district court's later analysis. Among other things, the IPR/PGR proceedings will prevent YMTC from making the type of ambiguous, overbroad, and tenuous allegations that currently permeate its complaint and infringement contentions. Indeed, the likelihood of issue simplification motivated the district court to stay the case in the first place.

Additionally, the mere fact that Petitioner submitted an expert declaration does not merit denial of IPR. Certain of the Petition's grounds—including Grounds 1 and 2 (anticipation and obviousness over Dong)—are readily understood without expert testimony due to their clarity and simplicity. The testimony accompanying the Petition simply serves to confirm that the Petition properly interpreted the prior

art. Petitioner’s expert testimony is no different from the testimony accompanying almost every filed IPR/PGR: it discusses a POSITA’s background knowledge and explains the prior art’s teachings from that perspective.

Finally, Patent Owner’s argument that the petition is “weak” (DD Brief, 23) is baseless. Patent Owner makes a single merits argument—that the prior art does not disclose 3D NAND—which fails under scrutiny. Even if the claims required 3D NAND (they do not), the Petition cites Dong’s express disclosure of “three-dimensional” NAND. §II.D.6. And, in any event, Petitioner argued obviousness with Patent Owner fails to address. *Id.*

For the reasons explained in this paper—and in the Petition itself—the Director should refer the petition to the merits panel for an institution decision.

II. ARGUMENT

No good reason exists for the Director to exercise its discretion to deny institution. In fact, the Director has every reason to reject YMTC’s arguments and institute this proceeding.

A. Compelling Economic and National Security Interests Favor Institution

As explained in recent guidance, the Director considers “[c]ompelling economic, public health, or nationality security interests” when deciding whether to exercise its institution discretion. *See* March 26, 2025 Interim Processes for PTAB

Workload Management (“March 26, 2025 Processes”). This case presents just such issues.

1. *Factual Background*

a. Micron Is a Pioneer in NAND Flash Memory

The ’941 patent—like most of the other YMTC patents¹ that Micron challenges—relates generally to NAND flash memory. See Ex. 1001, 1:24-29. NAND flash memory is a crucial component in the semiconductor ecosystem. It is a type of memory that does not lose data when it loses power. Conventional NAND stores data in memory cells laid out in an array of rows and columns. Historically, NAND arrays were laid out two-dimensionally in a single level. But, as demand for data storage grew, the semiconductor industry developed multi-level NAND devices, in which multiple levels of NAND memory cells are stacked vertically on top of each other. This is 3D NAND. By stacking levels vertically, 3D NAND dramatically increases memory storage capacity compared to conventional NAND. Connection with the stacked levels is typically accomplished using a staircase structure.

Micron—headquartered in Boise, Idaho—began its pioneering work in developing 3D NAND products more than fifteen years ago. Micron invested

¹ The ’164 patent relates to ESD circuitry generally. IPR2025-00118.

billions of dollars and years of effort towards researching, developing, and manufacturing 3D NAND technology. As part of this effort, Micron filed for (and later obtained) thousands of U.S. patents on this technology starting at least by 2010. This culminated in Micron launching its first 3D NAND product on March 26, 2015. *See* Ex. 1028 at 1-2.

Since 2015, Micron has continued to innovate its 3D NAND technology by developing memory products with more and more capacity and capabilities. Micron has received numerous awards and widespread recognition for its innovation (*see, e.g.*, Ex. 1029 at 1), and is a leading innovator—both in the U.S. and globally—of semiconductor memory devices, with over 57,000 patents (*see* Ex. 1030 at 2). In fact, Micron remains the only U.S.-based manufacturer of semiconductor memory devices.

YMTC did not file the earliest application identified on the face of '941 patent until 2020. *See* Ex. 1001, Cover.

b. The Chinese Government's Control of Its Semiconductor Industry

YMTC's role in the global semiconductor industry (and the strategic, state-backed initiative of which it is part) contrasts sharply with that of Micron. For more than a decade, the Chinese government has invested heavily in the semiconductor industry within its borders and set policies for Chinese semiconductor companies. In June 2014, China's State Council announced its "National Integrated Circuit

Industry Development Outline” with the “goal of establishing a world-leading semiconductor industry in all areas of the integrated circuit supply chain.” *See* Ex. 1032 at 1; Ex. 1033 at 19-20. It sought to remove “bottleneck[s] of industrial development,” establish “a national integrated circuit industry development leading group ... for the overall coordination of the integrated circuit industry,” and create “a financing platform and policy environment.” Ex. 1032 at 1-2; Ex. 1033 at 19-23.

The Chinese government then created the “National Integrated Circuit Industry Investment Fund” (or “Big Fund”) and raised 138.7 billion yuan from multiple government and state-owned enterprises,² including China’s Ministry of Finance. Ex. 1034 at 5; *see id.* at 3-7. The Big Fund aimed to “***support[] the integrated circuit manufacturing field,***” “implement mergers,” and “***standardize***

² According to China’s State Council, the term “state-owned enterprise” includes “state-owned enterprises, state-owned companies and state-owned capital holding companies that the State Council and local people’s governments respectively perform the duties of investors on behalf of the state, including enterprises supervised by central and local state-owned assets supervision and administration agencies and other departments at the same level and enterprises formed by their investment at each level.” Ex. 1036.

corporate governance.”³ Ex. 1032 at 2.

In May 2015, China’s State Council launched its “Made in China 2025” initiative. *See* Ex. 1038. The initiative set an ambitious ten-year roadmap for China to become a global leader in high-tech industries and officially solidified the semiconductor industry as one of the Chinese government’s targets. Ex. 1038 at 1-13 (*e.g.*, “[W]e must seize the current rare strategic opportunities, actively respond to challenges, strengthen overall planning, highlight innovation-driven, formulate special policies, give full play to institutional advantages, mobilize the whole society to work hard, rely more on Chinese equipment and Chinese brands, ... and complete the strategic task of transforming Chinese manufacturing from big to strong.”), 30.

The “Made in China 2025” initiative also outlined a comprehensive set of strategic goals, emphasizing the government’s central role in control and financing.⁴ *Id.* at 8-9 (*e.g.*, “Market-led, **government-guided**. Comprehensively deepen reform, give full play to the decisive role of the market in resource allocation, strengthen the dominant position of enterprises, and stimulate the vitality and creativity of

³ All emphases added unless otherwise noted.

⁴ *See also* Ex. 1070 at 4-5 (“Strengthen services and guidance for the construction of major integrated circuit projects [and] orderly guide and regulate the development of the integrated circuit industry”), 8-9.

enterprises. *Actively transform government functions, strengthen strategic research and planning guidance*, improve relevant support policies, and create a good environment for enterprise development.”), 37, 39, 41-44 (e.g., “*Deepen the reform of state-owned enterprises [and] improve the corporate governance structure....*”).

The Chinese government has aggressively sought foreign (including U.S.) patent protection in support of its goal to increase its control over the global semiconductor market. Indeed, the U.S. Congressional Research Service (CRS) explained:

China’s policies feature *a substantial and central role for the government in directing and financing Chinese businesses to obtain foreign IP* related to semiconductors. The Chinese government uses production targets; subsidies; tax preferences; trade and investment barriers (including pressure to engage in joint ventures); and discriminatory antitrust, IP, procurement, and standards practices. The policies seek to leverage China’s central role in global consumer electronics manufacturing and potential as a semiconductor production hub to incentivize and pressure foreign companies to localize production, share technology, and partner with the Chinese government and affiliated entities.

Ex. 1039 at 6; *see also id.* at 7-11.

c. YMTC Is China’s State-Owned NAND Memory

Company

In pursuit of its “Made in China 2025” initiative, the Chinese government tasked Tsinghua Unigroup, a state-controlled company, with leading the country’s memory chip development. *See* Ex. 1041 at 2; Ex. 1044 at 7. On July 26, 2016, Tsinghua Unigroup—jointly with the Big Fund and municipal governments—founded YMTC to develop NAND memory. Ex. 1043 at 1. This joint venture initially invested more than \$24 billion (USD) in YMTC. *See* Ex. 1044 at 7. Since then, the Chinese government has continued to invest heavily in YMTC. In 2023, for example, the Chinese government invested another \$7 billion (USD) through various investment vehicles, such as the second phase of its Big Fund. Ex. 1045 at 1; Ex. 1047 at 1-2.

The Chinese government not only invests heavily in YMTC, but it also owns and controls YMTC. YMTC is wholly owned by one parent corporation: Yangtze Memory Technologies Holding Co., Ltd. (“YMTC Holding”). *See* Ex. 1048 at 2. And YMTC Holding is owned by the following state-owned enterprises (as of March 12, 2025):

Shareholder	Ownership
Hubei Changsheng Development Co., Ltd. (湖北长晟发展有限责任公司), a state-owned enterprise	~29%
Wuhan Xinfei Technology Investment Co., Ltd. (武汉芯飞科技投资有限公司), a state-owned enterprise	~27%

Shareholder	Ownership
National IC Industry Investment Fund Co., Ltd. (国家集成电路产业投资基金股份有限公司), a state-owned enterprise	~13%
National IC Industry Investment Fund Phase II Co., Ltd. (国家集成电路产业投资基金二期股份有限公司), a state-owned enterprise	~12%
Hubei Science & Technology Investment Group Co., Ltd. (湖北省科技投资集团有限公司), a state-owned enterprise	~10%
Hubei Guoxin Industry Investment Fund Partnership (L.P.) (湖北国芯产业投资基金合伙企业 (有限合伙)), a state-owned enterprise	~6%
Yangtze Industrial Investment Group Co., Ltd. (长江产业投资集团有限公司), a state-owned enterprise	~3%
Total	100%

See Ex. 1050 at 9-10; Ex.1054 at 1 (“Yangtze Memory is a state-controlled enterprise ... [where] all seven shareholders of Yangtze Memory Technologies Holdings Co., Ltd. are state-owned assets.”); Ex. 1047 at 1-2 (“Hubei Changsheng Development Co., Ltd. is held by Hubei Integrated Circuit Industry Investment Fund, Wuhan Optics Valley Finance and Yangtze River Industrial Investment Group”—with the actual “controller behind the scenes [being the governmental] Administration of Wuhan East Lake High-tech Development Zone.... [The] actual controller of Yangtze River Industrial Investment Group is the Hubei Provincial State-owned

Assets Supervision and Administration Commission.... [The] actual controller of Hubei Guoxin Industry Investment Fund Partnership (Limited Partnership) is the Wuhan State-owned Assets Supervision and Administration Commission, and the actual controller of Hubei Science [&] Technology Investment Group Co., Ltd. is the [governmental] Administration of Wuhan East Lake High-tech Development Zone.”). All shareholders (listed above) are state-owned enterprises and, therefore, YMTC Holding and YMTC are state owned. See Ex. 1050 at 9-10; Ex. 1054 at 1; Ex. 1047 at 1-2.

This ownership structure and the Chinese government’s significant investment (*i.e.*, tens of billions of U.S. dollars) clearly show that YMTC serves the Chinese government’s semiconductor strategy and operates under the direction and control of the Chinese government. Indeed, China’s State Council has described YMTC as a “state-owned enterprise.” Ex. 1052 at 2. And Chinese media outlets and Chinese universities identify YMTC as a “state-owned enterprise” or “state-controlled enterprise.” Ex. 1054 at 1 (“***Yangtze Memory [Technologies, Inc.] is a state-controlled enterprise***”); see also, *e.g.*, Ex. 1056 at 1 (“***Nature of [YMTC]: State-owned enterprise***”); Ex. 1058 at 1 (same); Ex. 1060 at 1 (same); Ex. 1062 at 1-2 (“***China’s state-owned enterprise Yangtze Memory Technologies Co. Ltd.... Yangtze Memory is controlled by the Hubei Provincial Government and the China National Integrated Circuit Industry Investment Fund.***”).

d. Bipartisan U.S. Policymakers Agree That the Chinese Government Controls YMTC

U.S. policymakers consistently highlight the Chinese government’s ownership and control over YMTC. In July 2021, U.S. Senator Bill Hagerty and U.S. Representative Michael McCaul urged the U.S. Commerce Secretary to add YMTC to the Department of Commerce’s Entity List⁵ because it “has clear ties to the Party-state and military and plays a significant role in CCP plans to control the supply chain for a strategic dual-use sector.” Ex. 1063 at 1-2. They explained that:

YMTC is the PRC’s state-owned national champion for memory chips

— a type of semiconductor with defense, artificial intelligence, and aerospace applications. YMTC was created as a joint-venture by the National Integrated Circuit (IC) Industry Investment Fund, Tsinghua Unigroup (a state investment firm that is one of the IC Fund’s shareholders), the Hubei IC Industry Fund (a regional branch of the national IC Fund), and the Hubei Science and Technology Investment Group (an investment vehicle of the Wuhan Municipal Government

⁵ The “Entity List” identifies persons—including corporate entities—reasonably believed to be involved, or pose a significant risk of being or becoming involved, in activities contrary to the national security or foreign policy interests of the United States. See <https://www.bis.gov/licensing/guidance-on-end-user-and-end-use-controls-and-us-person-controls#End-usercontrols>

that provides capital investment, infrastructure and services for the PRC's strategic industries, including semiconductors).

Id.; see also Ex. 1064 at 2 (“The White House has described YMTC as a Chinese ‘national champion.’”).

In April 2022, Mr. Stephen Ezell, Vice President of Global Innovation Policy at the Information Technology and Innovation Foundation, testified before the U.S.-China Economic and Security Review Commission (which is a bipartisan legislative commission created by the U.S. Congress) on “U.S.-China Innovation, Technology, and Intellectual Property Concern.” Ex. 1044 at 1, 3. In his testimony, he explained:

[YMTC] is a Chinese state-controlled joint venture stood up from whole cloth by the National IC Industry Investment Fund, the state university-controlled fabless semiconductor firm Tsinghua Unigroup, and the Hubei Science and Technology Investment Group, supported by \$24 billion in initial government funding allocated for its initial Wuhan factory alone. In effect, YMTC is China's state-owned national champion for memory chips.

Id. at 7. Similarly, in September 2022, U.S. Senator Mark Warner stated it “has been clear for some time now that YMTC is ... a key part of the Chinese Communist party's goal of shifting control of global microelectronics to the PRC.” Ex. 1064 at 2. Similarly, in December 2022, U.S. Senator Charles E. Schumer called YMTC a “CCP-backed technology compan[y].” Ex. 1065 at 1.

Next, pursuant to Section 1260H of the William M. (Mac) Thornberry National Defense Authorization Act, the Secretary of Defense must identify entities that the Secretary “determines” to be a “Chinese military company” “based on the most recent information available.” H.R. 6395, 116th Cong. §1260H(a), (d) (2021). A ‘Chinese military company’ refers to any entity that is “directly or indirectly owned, controlled, or beneficially owned by, or in an official or unofficial capacity acting as an agent of or on behalf of, the People’s Liberation Army or any other organization subordinate to the Central Military Commission of the Chinese Communist Party”—*i.e.*, an entity that is owned and/or controlled by the Chinese government. *Id.* §1260H(d). On January 31, 2024, the Department of Defense identified YMTC as a “Chinese military compan[y].” Ex. 1066 at 1; Ex. 1067 at 1, 3; *see also* 90 Fed. Reg. 1105 (Jan. 7, 2025) (same).

2. *YMTC’s State-Owned Status Weighs in Favor of Institution*

The USPTO’s regulations governing IPR/PGR proceedings—including those controlling IPR/PGR institution—are intended to account for “the effect ... on the economy” and “the integrity of the patent system....” 35 U.S.C. §316(b). Consistent with this, as the former USPTO Director explained to Congress in 2023, “the USPTO is committed to an all-of-Government approach to leveraging IP rights to catalyze U.S. economic competitiveness and national security.” Ex. 1068 at 9. She further testified, “[t]he USPTO is working globally to strengthen the innovation, creativity,

and entrepreneurship ecosystem, to hold competitors to their agreements, to curb abuses and unfair practices, and to directly assist stakeholders facing IP issues abroad.” *Id.*

Proceeding to a merits decision in this IPR will further these goals. Accepting YMTC’s arguments, however, will frustrate them. Micron is the sole U.S.-based semiconductor memory manufacturer. Micron is currently the target of an expansive district court patent infringement action brought by YMTC involving 19 patents. YMTC is a Chinese-state owned and controlled company. As explained above, China has publicly explained that it intends to, among other things, leverage foreign intellectual property rights to increase its control over the global semiconductor market. Engaging in a full, comprehensive, and substantive review of YMTC’s patents will ensure that China is not improperly using U.S. patents—through its proxy YMTC—to target, impose costs on, and potentially extract monetary concessions on invalid patents from U.S.-based companies like Micron. This in turn furthers U.S. economic interests by ensuring continued, fair competition in the semiconductor field. Relatedly, it will ensure that the U.S. patent system operates to further U.S. economic and national security interests, as opposed to those of a foreign state and its proxy YMTC. This all weighs heavily in favor of institution.

B. The Large Number of Patents Asserted by YMTC Does Not Weigh Against Institution

None of YMTC's other arguments even remotely suggests any other course of action, and a merits decision is appropriate here.

YMTC begins its brief by discussing the supposedly "substantial burden" imposed on both it and the Board by Micron's "barrage" of IPR and PGR petitions. DD Brief, 1. According to YMTC, these petitions are meant to provide Micron with a "tactical advantage in district court" and somehow operate only to "harass[]" and "punish[]" YMTC. *Id.* Further, YMTC complains that instituting would unnecessarily consume the Board's "finite resources." *Id.*

As an initial matter, the Board handles over a thousand IPRs and PGRs every year. Micron's filings represent only a very, very small percentage of this total. This falls well short of imposing anything that could even remotely be characterized as a "substantial burden" on the Board.

Next, in complaining that it will be burdened by Micron's filings, YMTC has it backwards. Micron filed the number of IPRs/PGRs it did only because YMTC chose to assert an excessive number of patents (19 in total) and claims (more than 200) in district court. Thus, it was YMTC—not Micron—that improperly sought a "tactical advantage." By arguing for discretionary denial due to the large number of Micron IPRs/PGR, YMTC is attempting to prevent meaningful review of its many (and non-meritorious) patent allegations simply by asserting a large number of

patents. Micron, unsurprisingly, sought to defend itself against YMTC’s “barrage” both in district court and in the USPTO. The district court also refused to become bogged down by YMTC’s excessive assertions and instead stayed the case pending resolution of Micron’s IPR/PGR filings. *See* Ex. 1073 at 2 (noting that a stay will “simplify the issues” by reducing the number of “infringement, validity, and claim construction issues”). If YMTC did not want to defend multiple patents in IPR/PGR, it should have exercised more care when selecting which patents to assert in the first place. This would have both allowed for more expeditious district court proceedings and reduced the number of IPR petitions Micron filed. Once again, YMTC made its bed and must lie in it.

Nor does the fact that Micron occasionally filed multiple petitions against certain YMTC patents have any bearing on whether institution is appropriate here. **YMTC’s** actions—like the total number of filed IPRs/PGRs—required that Micron file multiple petitions against certain YMTC patents. Rather than asserting only a single claim (or small number of claims) per patent, YMTC chose to assert **many** claims. Indeed, even as the district court action progressed from the pleadings stage into early fact discovery, YMTC continued to expand the total number of asserted claims. *See, e.g.,* Ex. 1025 at 2 (asserting more than 150 claims across 11 patents); Ex. 1074 at 2 (asserting more than 50 claims across 8 patents). It was YMTC’s expansion that necessitated additional IPR/PGR filings.

Declining to address Micron’s petitions on the grounds that YMTC asserted numerous patents would serve little purpose besides improperly rewarding YMTC for its chosen litigation tactic. Even more perniciously, however, were the Board to agree with YMTC, the Board would incentivize other patent owners to behave similarly. Rather than limiting and focusing their district court assertions, patent owners will be motivated to assert even more patents in district court in the hopes of similarly avoiding Board review. The Director should discourage this type of gamesmanship and forum shopping—which has the potential to further burden district courts with reams of unnecessary allegations. The most straightforward way to do so is to strongly and unambiguously reject YMTC’s argument here: the volume of IPRs filed does not (and cannot) have any bearing on whether institution is appropriate, particularly when that volume was patent owner’s own creation.

C. The District Court Has Deferred to the PTAB

YMTC next argues that this IPR is “unlikely to result in a commensurate simplification of the issues before the District Court.” DD Brief, 11. Relatedly, it posits that the district court—and not the Board—is better situated to manage the scope of the parties’ dispute. *See id.* at 14-15.

The district court arrived at the opposite conclusion when it stayed the co-pending district court case. In particular, the district court explained that “staying the case pending IPR will simplify the issues.” Ex. 1073 at 2. Among other things,

the district court noted that Micron’s IPRs/PGR will likely entirely eliminate patents from the case, resulting in simplification of the “infringement, validity, and claim construction issues” confronting the court. *Id.* at 2. Moreover, the district court noted that many of YMTC’s patents embrace “overlapping subject matter.” *Id.* So each Board decision has the potential to resolve issues spanning across multiple patents. *See id.*

While the district court did issue a series of orders requiring YMTC to reduce the number of asserted claims as YMTC notes in its brief (*see* DD Brief, 10-11), this fact alone does not merit a discretionary denial of IPR/PGR. Micron’s IPRs/PGR cover a larger number of claims than will ultimately be at issue in district court because YMTC itself chose to assert these claims in the first instance in its district court infringement contentions. Moreover, most of the independent claims addressed by Micron’s IPRs/PGR—which will likely be the focus of any disputes between the parties if the Board institutes this and Micron’s other proceedings—currently remain at issue in district court. YMTC’s argument is also self-contradictory. If Micron had waited to file until after the district court had narrowed the number of asserted claims, YMTC presumably would have argued that Micron’s petitions should be discretionarily denied because they were filed too late. Given this, YMTC cannot now argue that filing early (and addressing the claims at issue at the time when doing so) somehow also merits a discretionary denial. Agreeing with

YMTC would be nonsensical: both early and late IPR/PGR filings would be deemed unworthy of review on the merits.

D. The *Fintiv* Factors Weigh Strongly In Favor of Institution

The Director also continues to evaluate “the discretionary considerations enumerated in existing Board precedent” including *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper No. 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”). March 26, 2025 Processes at 2. These considerations make it abundantly clear that Micron’s IPR petition should be reviewed on the merits. In particular: the district court has stayed the parallel district court case, no trial is currently scheduled, no substantive district court work has occurred, the stay ensures that there will be little overlap, and the petition is substantively strong.

1. *The District Court Litigation Is Stayed*

The district court has stayed the case pending IPR/PGR. *See* Ex. 1073. By issuing a stay, the district court indicated that it prefers the Board to address unpatentability of YMTC’s patents in the first instance. This weighs strongly in favor of institution. *See Fintiv* at 12.

Patent Owner argues that if the Director declines to institute, it “intends to seek to lift the District Court stay and resume the litigation.” DD Brief, 16. No basis exists for doing so any time soon. The district court ordered that the case be stayed until “the completion of all IPR proceedings.” Ex. 1073 at 1, 3. The PTAB has

already instituted several Micron IPRs. *See, e.g.*, IPR2024-00788, -00789, -00790, -00791, -00792, -00794, -00795, -00909, -00911, and IPR2025-00034. The most recent of these will not reach final decision until May 2026. *See* IPR2025-00034, Paper 19. Other IPRs remain in the pre-institution phase, with institution decisions not due for several months. *See, e.g.*, IPR2025-00117, -00118, -00119, -00189, -00191, -00190, -00228, -00244, -00294, and -00245. Given this, IPR/PGR involving YMTC's patents will be ongoing for quite some time. The district court's stay will remain in place throughout this process. Any suggestion by YMTC to the contrary is pure speculation. This factor weighs heavily in favor of institution.

2. *No Trial Is Scheduled*

Next, because the district court case is stayed, no trial date is currently scheduled. As a result, if IPR is instituted, proceedings before the Board will be completed long before any potential district court trial. YMTC references the district court's previously scheduled June 2026 filing date. *See* DD Brief, 16. But the district court vacated that date, and it no longer applies. *See generally* Ex. 1073. And as the case is currently stayed, once the stay is eventually lifted, it will take more than a year (if not years) of further work before the parties will be ready for trial. This also weighs strongly in favor of institution.

3. *Little Substantive Progress Has Been Made*

According to YMTC, "[t]he parties extensively invested in the district court

litigation prior to the court staying the case.” DD Brief, 17. The district court reached the opposite conclusion. As explained in its stay order, “the litigation is in an early stage.” Ex. 1073 at 1. “Fact discovery” remained open and “the parties had not yet taken a single deposition.” *Id.* “Claim construction briefs [had] not yet been filed....” *Id.* So, while the parties had engaged in some fact discovery, almost all substantive work—including depositions, claim construction briefing, expert discovery, and dispositive motion briefing—remained to be done. None of this work will occur until after the district court’s stay is lifted. This also weighs in favor of institution. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative).

While YMTC makes much of the fact that it was “forced to defend against” various discovery motions (*e.g.*, DD Brief, 17-18), this was also a problem of its own making. YMTC aggressively pursued overbroad, extraordinarily burdensome, and irrelevant discovery from Micron. At the same time, it largely refused to provide any meaningful productions of its own. This lopsided approach predictably led to discovery briefing. Moreover, the parties’ briefing focused on the scope of discovery. The fact that back-and-forth briefing regarding discovery scope was still ongoing at the time of the stay (*see, e.g.*, Ex. 1073 at 2-3 (referencing still pending motions)) further evinces the parties’ lack of meaningful progress and the amount of work that remains in district court. Rather than finishing the discovery process, the

parties were still in the process of debating what fact discovery would entail.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv* at 11. Here, Petitioner proceeded with diligence, filing only months after being served with the complaint. *See* Ex. 1026. This, just like the early stage of the district court action, also weighs in favor of institution.

4. *The Stay Minimizes Any Issue Overlap*

YMTC argues that “[t]here is substantial overlap” between this proceeding and the district court action. DD Brief, 19. This, however, entirely ignores that the impact of the district court’s stay. The district court action will not resume until all of Micron’s IPRs conclude. Because of this, in the event the Board institutes and renders a final written decision, estoppel will prevent Micron from asserting the petition’s grounds (or grounds it reasonably could have included in the petition) in district court if YMTC prevails (if Micron wins, there will be no valid patent on which to proceed). There will be no overlap at all. Moreover, even if the district court were to lift the stay for some reason (it will not be), Micron stipulated in the Petition that it will not advance the Petition’s grounds in district court. *See* Petition at 10. This all weighs in favor of institution. *See Sand Revolution*, 11-12.

5. *Party Overlap*

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as parallel proceedings often result in party overlap.

6. *Other Circumstances (Merits of the Petition)*

In various places throughout its DD Brief, Patent Owner argues the merits of the Petition, including in the Introduction (DD Brief, 3), in connection with the *Fintiv* factors (*id.* at 11), and as a standalone argument in §III.E (*id.* at 23-25). In each instance, Patent Owner raise the same baseless arguments, which it summarizes in the Introduction as follows:

Each independent claim requires a memory having vertical structures of word lines arranged “from bottom to top.” Petitioner relies exclusively on Dong (Ex.1005) for this claim element, but Dong only discloses word lines arranged horizontally. Petitioner identifies no teaching or suggestion to reorient Dong’s word lines vertically and does not even contend that it would have been obvious to do so, instead relying on its expert’s testimony to fill this missing disclosure in the prior art.

DD Brief, 3. Patent Owner’s DD Brief elaborates on this in §III.E (“Petitioner’s Weak Unpatentability Challenge Favors Discretionary Denial”).⁶ Patent Owner is

⁶ Patent Owner cross-references its merits POPR at least twice, where Patent Owner elaborates on the same misguided argument. See DD Brief, 3 (“As

incorrect for three separate reasons: (1) Dong discloses vertical 3D memory strings; (2) the claims do not require a vertical memory string; and (3) Petitioner does argue obviousness.

Before turning to the substantive analysis, Patent Owner's assertion is belied by its actions in defending the validity of the Chinese counterpart to the '941 patent (CN202080000267.4/CN111344792). In particular, in the Chinese invalidation proceeding, Patent Owner recently amended independent claim 6 (corresponding to '941 patent claim 1) by adding a dependent claim limitation requiring a "third portion." *See* Ex. 1077. As provided for in the Chinese counterpart to the MPEP (*i.e.*, CNIPA's Guidelines for Patent Examination), this action constitutes an admission by the patentee that the claim should be invalidated.⁷ By extension, Patent Owner conceded that counterpart claim 1 in the

described in the Patent Owner Preliminary Response, each of Petitioner's grounds fail for a basic reason ..."), 11 ("[A]s discussed in detail in the Patent Owner Preliminary Response, the Petition's challenge fails on the merits, ...").

⁷ *See* CNIPAGuidelines for Patent Examination, Section 2.2, Chapter 3, Part IV ("In invalidation proceedings, if the patentee voluntarily narrows the scope of patent protection in response to the invalidation request filed by the petitioner, and the corresponding amended claims have been accepted by the panel, it shall be

'941 patent should also be invalidated.

e. Dong Discloses Vertical 3D Memory Strings

Patent Owner argues that Dong “does not disclose the specific three-dimensional memory as claimed with word lines arranged vertically ‘from bottom to top.’” DD Brief, 24. But Dong expressly discloses that “the array of storage elements can be three dimensional.” Ex. 1005, [0095]. And a POSITA reading Dong in 2020 (the effective filing date of the '941 patent) would readily envisage a 3D memory with vertical memory strings.

Notwithstanding Dong’s express disclosure of “three dimensional” NAND, Patent Owner contends “it does not disclose the specific three-dimensional memory as claimed with word lines arranged vertically ‘from bottom to top.’” DD Brief, 24. The POPR makes clear that Patent Owner’s argument is premised on interpreting Dong in 2007 (*i.e.*, Dong’s filing date) instead of through a POSITA’s

deemed that the patentee acknowledges that the claims broader than this scope have, from the outset, failed to comply with the relevant provisions of the Patent Law and its Implementing Regulations, and also acknowledges the petitioner’s request for invalidation of those claims. As a result, the petitioner is relieved of the burden of proof for the assertion that those claims should be declared invalid.”).

lens at the Challenged Patent’s priority date in 2020.⁸ POPR, §§II.A.2, III.C (“Dong’s disclosure of ‘three-dimensional’ memory arrays refers to 3D memory arrays known as of Dong’s May 7, 2007 filing date.”). This contradicts black letter law that invalidity (including the scope and content of the prior art and a POSITA’s knowledge) is evaluated as of the priority date of the patent being challenged (*i.e.*, the question here is not what Dong would have disclosed to a POSITA in 2007, but what Dong would have disclosed to a POSITA in 2020, including in view of the knowledge of a POSITA).⁹ *Sage Prods., LLC v. Stewart*, Nos. 2023-1603, 2023-1604, 2025 U.S. App. LEXIS 8816, at *17 n.5 (Fed. Cir.

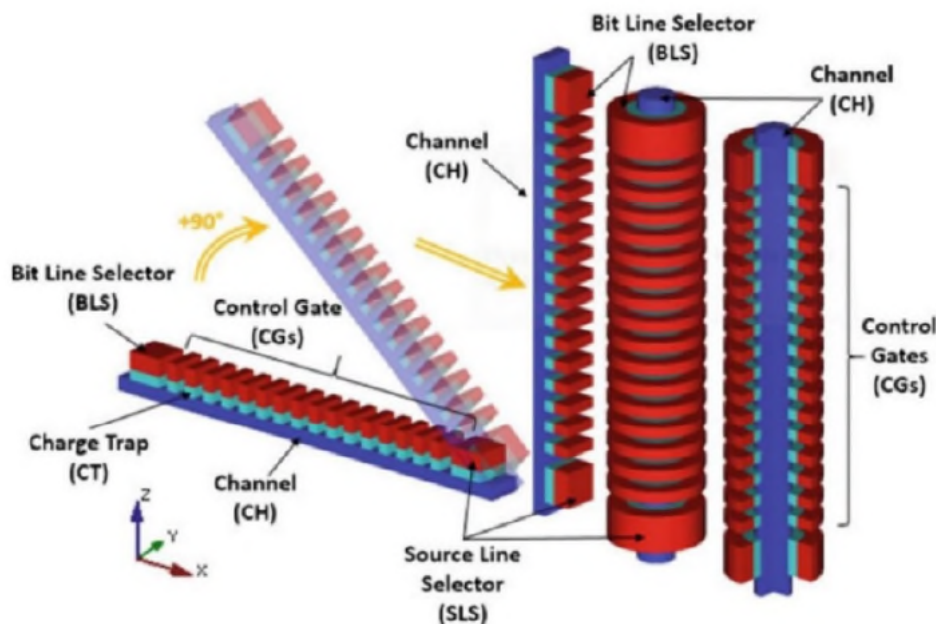
⁸ In this case, the earliest priority date is undisputedly February 10, 2020. Ex. 1001, 1 (priority claim to PCT/CN2020/074580, filed February 10, 2020).

⁹ Petitioner maintains that, in 2007, a POSITA would have understood Dong’s disclosure of 3D NAND to include vertical memory strings. *See, e.g.*, Ex. 1009 at 28-29 (“In 2007, three-dimensional (3D) NAND flash device technology of BiCS (bit cost scalable) was proposed [58] in order to scale down the NAND flash memory cell ... The vertical [] channel is fabricated by through-holes in stacked multilayer word lines”); Ex. 1075 (2007 article discussing vertical 3D NAND architecture). But since that analysis evaluates the prior art at the wrong point in time, Petitioner does not pursue that line of argument here.

Apr. 15, 2025) (“An anticipation analysis is undertaken from the perspective of the person of ordinary skill in the art and, therefore, must take account of the knowledge of such a person. ... [E]ven if a piece of prior art does not expressly disclose a limitation, it anticipates if a person of ordinary skill in the art would understand the prior art to disclose the limitation and could combine the prior art description with his own knowledge to make the claimed invention. ... Such a person would have carried that knowledge with her when examining each of the challenged claims.”) (internal citation omitted). Moreover, Patent Owner’s own expert admits that “the level of ordinary skill in the relevant art” is assessed “at the time of the invention.” Ex. 2006, ¶32. Thus, Patent Owner’s argument is premised on legal error.

Indeed, Patent Owner does not even argue that a POSITA in 2020 would have thought that the scope of 3D NAND did not encompass vertical NAND strings. *See* POPR, §§II.A.2, III.C. Nor could it, given that vertical NAND strings are (and were at all relevant times) the most common 3D NAND architecture. *See* Pet., §V (“Technology Background” discussing transition from 2D NAND to 3D NAND). Indeed, as the Petition explained, textbooks published well before the 2020 priority dates explained, “3D NAND structure[s] could be conceived by starting from the 2D NAND string building block and turning the 2D NAND string upside, resulting in a 3D structure with a vertical channel.” Pet, 12-13 (quotes

omitting) (citing Ex. 1010 at 122, Ex. 1011 at 3)).



Pet., 13 (excerpting Ex. 1010 at 122).

And neither Patent Owner nor its expert disputes Petitioner’s assertion that a POSITA in 2020 “would have been aware of and generally knowledgeable about NAND memory’s structure and fabrication, its component parts, how it operates, and how it is controlled.” POPR, 12; Ex. 2006, ¶¶34-35.

In view of the well-developed state of 3D NAND memory in 2020, a POSITA would “at once envisage” the ’941 patent’s claimed “bottom to top” arrangement upon reading Dong’s disclosure of “three dimensional” NAND. Pet., 35; *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (“However, a reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of

skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.”); *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022) (“the assessment of a claim’s patentability is inextricably tied to a skilled artisan’s knowledge and skill level”).

This not only distinguishes *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008), cited in the DD Brief, 24, but also disposes of Patent Owner’s argument that Petitioner needed to argue obviousness for the “bottom to top” element. DD Brief, 24. Regardless, as discussed *infra* §II.D.6.c, Petitioner did argue obviousness. *E.g.*, Pet., 31; Liu, ¶120 (“given the similarities between 2D and 3D NAND discussed in the Technology Background section, even a 2D memory string would at a minimum render obvious the bottom to top requirement.”).

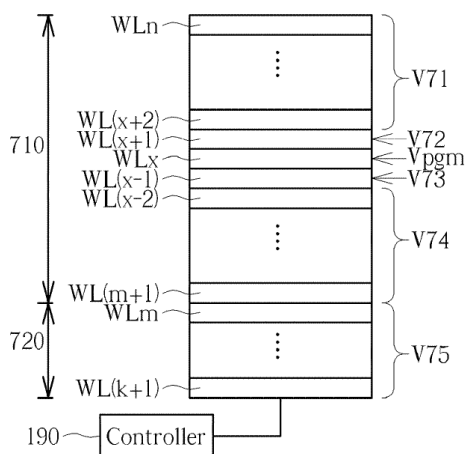
In various locations throughout its DD Brief, Patent Owner asserts that Dong “discloses word lines arranged horizontally.” DD Brief, 23. In support, Patent Owner’s merits POPR cites extensively to Dong Figure 4 and reproduces it several times (see POPR, 3, 14, 35). Tellingly, Figure 4 is not among the figures relied

upon in the Petition.¹⁰ To be sure, Dong Figure 4 illustrates a 2D NAND string, but that in no way restricts the scope of Dong’s additional disclosure of “three dimensional” NAND (Dong, [0095]). In other words, Patent Owner improperly attempts to restrict the applicability of Dong’s disclosure of “three dimensional” NAND to somehow exclude Figure 5 which, in contrast to Figure 4, shows a memory stack oriented vertically in the same manner as the ’941 patent.¹¹

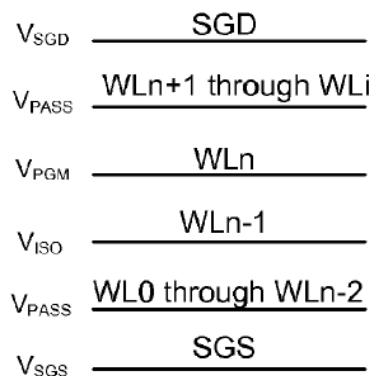
¹⁰ If anything, Figure 4—which illustrates programming voltage in a horizontal layout—rebutts Patent Owner’s assertion that Dong Figure 5 illustrates the programming voltages vertically only for “ease of reading.” POPR, 36.

¹¹ Petitioner expressly identifies Dong Figure 12 as disclosing the “memory” recited in the preamble. Pet., 34 (mapping “memory” as including Dong’s “memory array 1100” in Figure 12). Dong’s “three dimensional” memory disclosure is in the specific context of Figure 12’s “memory array 1100” on which Petitioner relies. Ex. 1005, [0095]. Thus, even if Patent Owner were correct (it is not) that Dong Figures 5a and 5g are merely “voltage diagrams” and thus do not necessarily disclose a 3D architecture with vertical NAND strings (DD Brief, 23-24), Dong Figure 12 (illustrating “a block diagram of a non-volatile memory system”) provides such disclosure. Dong, [0095].

Patent Owner also faults Petitioner for pointing to various vertically-oriented diagrams in Dong (*e.g.*, Fig. 5a). DD Brief, 23-24. Patent Owner characterizes these as “voltage diagrams” which “do not show the physical structure of Dong’s memory,” and thus do not “disclose vertical word lines as recited in the independent claims of ’941 Patent.” *Id.* But these are precisely the types of diagrams found in the ’941 patent, which Patent Owner contends disclose a vertical “bottom to top” arrangement. *E.g.*, POPR, 19 (stating that all ’941 figures “illustrate word lines arranged vertically, as in Figure 8”). The side-by-side figures below compare a representative image from the ’941 patent (on the left) and Dong (on the right).



'941 patent, Fig. 8



Dong, Fig. 5a

Rather than labelling the voltages with names as Dong does, the ’941 patent uses a numbering scheme where V71 refers to a “first voltage,” V72 refers to a “second voltage,” V73 refers to a “third voltage,” and so on. Ex. 1001, 4:37-61.

Given that Figures 1-11 in the '941 patent follow a similar scheme, under Patent Owner's reasoning, they would all qualify as "voltage diagrams" subject to the same criticism Patent Owner levels against Dong. Moreover, taking '941 patent Figure 8 as an example, it shows a "Controller" connected to a single wordline (WL(k+1)). If Figure 8 were intended to illustrate the physical structure of a memory string, it would not work because the controller would need to access and control *all* wordlines. Thus, Patent Owner's reliance on the '941 patent figures to support its interpretation of "bottom to top" employs a double standard.

f. The Claims Do Not Require Vertical Memory Strings

Patent Owner's arguments are premised on an incorrect claim construction that ignores the knowledge and perspective of a POSITA. The claims themselves do not recite "three dimensional memory," "3D memory," or "vertical" memory strings. *See* Ex. 1001. As the Petition explains, a POSITA would have understood the terms "top" and "bottom" of a NAND memory string to refer to the drain and source ends of the memory string, respectively, as was well-known in the art.¹²

¹² Patent Owner insinuates that Petitioner relies exclusively on its expert for this interpretation. DD Brief, 22. Both the Petition and Dr. Liu's declaration discuss numerous references using the source and drain nomenclature. *See, e.g.*, Ex. 1009 (Aritome) at 297 ("The bottom of memory string is connected to the common

Pet., 35. This is true regardless of the orientation of the memory device. For example, neither infringement nor invalidity should turn on whether a 3D memory happens to be turned on its side (such that it resembles a 2D NAND memory), is flipped upside down, or is otherwise oriented in a different direction. Nor should it turn on the orientation of a 2D NAND device. The POSITA's understanding of bottom-to-top as source to drain avoids this arbitrariness.

Patent Owner's contention that "the plain meaning of 'bottom' is not 'source' and the plain meaning of 'top' is not 'drain'" (DD Brief, 25) violates the

source diffusion formed on the silicon substrate."), 38 (discussion of connecting "SGD" to the string's drain side and SGS to string's source side), 39 (figure showing 32-cell NAND string with SGS at the bottom and SGD at the top); Ex. 1010 (Michelsoni) at 122 (showing relationship between structure of 2D NAND string and 3D NAND string by turning the 2D NAND string so it "stands up"); Ex.1011 (Silvagni) at 3 (shows relationship between 2D and 3D NAND as standing the string on its end with current flowing from the bottom of the 3D NAND string), 4 ("It can be noted that the NAND string is vertical, and the string current flows in the vertical direction and is collected by a drain contacting the top of the cell stack. The source current must be provided by source diffusion at the bottom."); Ex. 1008 (Lee II), Figs. 3, 6-9, 11-12, 14-16, 18-20.

bedrock principle that claims are understood from the perspective of a POSITA. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (“We have made clear, moreover, that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.”). The only purpose the “bottom to top” language in the claim serves is to determine the application of the recited voltages relative to other memory cells in the memory string. It does not mandate any particular structure (nor does the ’941 specification impose such a requirement). Notably, none of the ’941 claims even recites 3D memory and are not limited to 3D memory structures. To hold otherwise, as Patent Owner posits, would impermissibly read a preferred embodiment into the claims.

Patent Owner’s merits POPR attempts to spin certain of Dr. Schubert’s statements (Petitioner’s expert in the parallel district court proceeding) by cherry-picking excerpts out of context and submitting containing only 5-pages of his 60-page declaration (see Ex. 2010).¹³ For completeness/fairness, and consistent with

¹³ Submitting the entirety of Dr. Schubert’s declaration would have required Patent Owner to contend with the numerous 2D NAND references which used the “bottom” and “top” nomenclature to refer to the source and drain. Ex. 1076, ¶¶139, 142-146 (discussing various 2D NAND references).

F.R.E. 106, Petitioner submits the entirety of Dr. Schubert’s declaration. Ex. 1076. Dr. Schubert discusses the evolution and relationship between 2D and 3D NAND, and explaining in detail why a POSITA would understand bottom-to-top as source to drain. *Id.*, §§VII.A, X.E.

Patent Owner asserts that “[i]f Petitioner’s construction were adopted, it would lead to the absurd conclusion that, as Petitioner’s expert in the district court litigation admitted, the ‘bottom and top are at the same physical level.’ Ex. 2010 (Schubert Decl.) at 59,” and would “render[] both ‘bottom’ and ‘top’ meaningless.” POPR, 30. But read in context, Dr. Schubert merely explains how the source/drain construction has applicability across a variety of memory architectures (including both 2D and 3D NAND implementations). Ex. 1076, ¶¶134-157 (the “Schubert Dec.”). In addition to the textbooks already discussed, Dr. Schubert explains how the following references support his interpretation:

- U.S. Pat. 7,672,165 (“Pham”) (discussed at Schubert Dec., ¶144): “NAND arrays are well known in the art and are widely utilized in various consumer devices” Col. 1:38-2:9. The “top and bottom of the string connect to the bit line and a common source line respectively.” *Id.* 1:59-63; *see also id.*, Fig. 2A.
- U.S. Pat. 9,230,658 (“Han”) (discussed at Schubert Dec., ¶¶145-146): “data is written on a memory block in a bottom-up fashion, starting from memory cells on or near the lowermost (or bottom) wordline. Then data is sequentially written page-by-page on memory cells on

wordlines above the lowermost wordline until memory cells on the uppermost (or top) wordline are filled up.” Col. 3:25-33. In other words, Han describes the term “top” and “bottom” in relation to NAND string wordlines, where wordlines near the “bottom” are those closer to the source and wordlines near the “top” are those closer to the drain.

- U.S. Pat. 9,530,492 (discussed at Schubert Dec., ¶154): showing a 3D NAND architecture with both memory string ends at the same z-axis level due to “U-shaped” architecture. Fig. 1D.
- U.S. Pat. 9,613,704 (“Lee 704”) (applicable to both 2D and 3D NAND, discussed at Schubert Dec., ¶148): “each String comprising M cells connected in series and capped by a top string-select transistor and a bottom String-select transistor, the top string-select transistor connecting its drain to one corresponding [bit line], the bottom string-select transistor connecting its source to a common source line.” Col. 121:41-46.
- U.S. Pat. Pub. 2021/0158880 (a YMTC patent application with some of the same inventors listed on the ’941 patent) (discussed at Schubert Dec., ¶150): referring to a “top select gate SG_T (on the drain side) and a bottom select gate SG_B (on the source side).” [0018]; *see also* [0020]-[0021].

By contrast, Patent Owner’s construction (taken from a non-technical Merriam-Webster’s online dictionary) disregards numerous memory architectures and renders the meaning of bottom and top arbitrary. *E.g.*, Schubert Dec., ¶¶136, 156. The Director should disregard Patent Owner’s misleading and out-of-context

arguments regarding Dr. Schubert’s declaration. Assessing all of the evidence, Petitioner’s construction—which reflects a POSITA’s knowledge and understanding of NAND memory development and operation at the time of the ’941 patent’s priority—clearly prevails over Patent Owner’s narrow, non-technical approach that excludes numerous memory architectures.

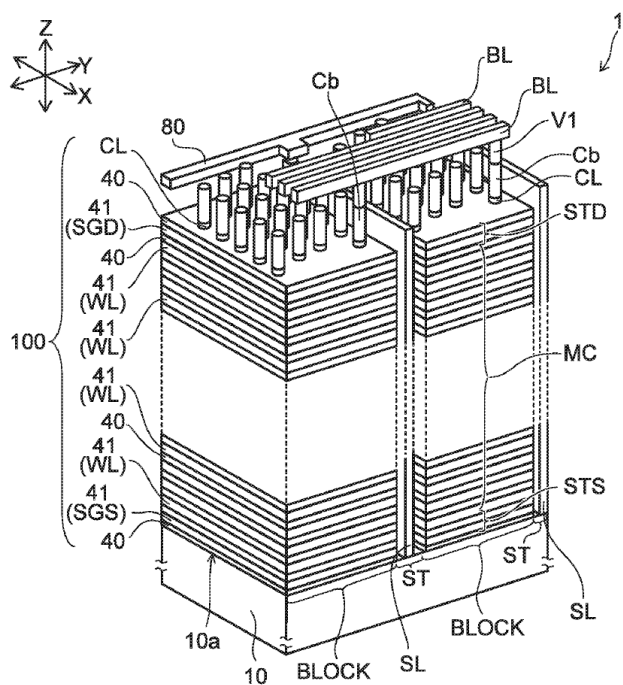
g. Petitioner Did Argue Obviousness

In various places, Patent Owner asserts that Petitioner “does not even contend that it would have been obvious to” use vertical 3D NAND memory strings. DD Brief, 3; *see also id.*, 24; POPR, 41-44. For all the reasons explained above, it was not necessary for Petitioner to argue obviousness at all, but Petitioner did so anyway. For example, Ground 2 is “Dong renders obvious claims 1, 3, 5-7, 11, and 13 under §103.” Pet., 7. Patent Owner even acknowledges Dr. Liu’s testimony that “given the similarities between 2D and 3D NAND discussed in the Technology Background section, even a 2D memory string would at a minimum render obvious the **bottom to top** requirement, even if narrowly construed.” POPR, 45 (quoting Ex. 1004, ¶120). This passage is also cited in the Petition for the exact **bottom to top** claim language. Pet., 35.

Nevertheless, Patent Owner makes the baseless assertion that the argument is only made “in Petitioner’s expert declaration,” but is “not made in the Petition.” POPR, 45. Patent Owner’s assertion is further belied by the Petition’s holistic

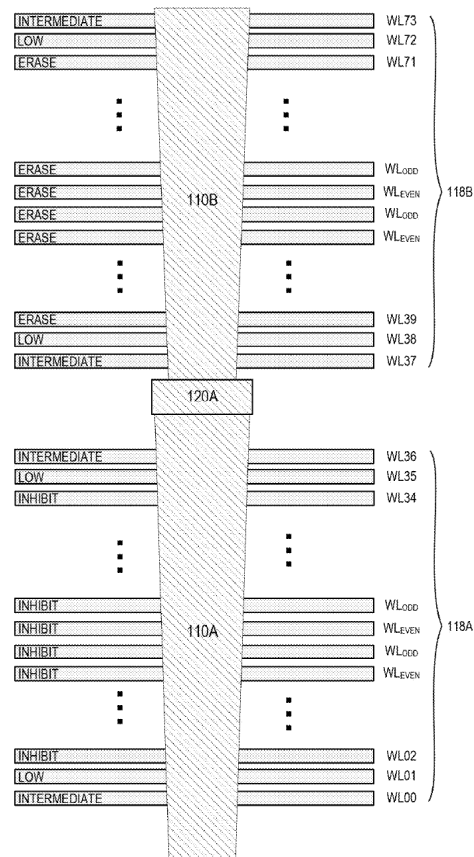
discussion of how “Dong anticipates and/or renders obvious claim 5.” Pet., 29-33. In particular, the Petition explains that “32-cell (and larger) memory strings were well-known to POSITAs by the Priority Date and would have been obvious to use,” and proceeds to explain why. *Id.*, 31. The explanation cites various references, including several vertical 3D NAND string references. *Id.*, For example, the Petition cites Shirai, [0019], which discusses the 3D NAND figure below and states that “Any number of electrode layers 41 may be stacked.” *Id.*

FIG. 1



Shirai, Fig. 1. As another example, the Petition cites to Righetti, Fig. 6 (reproduced below), which also plainly shows 3D NAND.

FIG. 6



Righetti, Fig. 6. Petitioner ignores all of this disclosure and blatantly misrepresents that Petitioner did not argue obviousness.

Patent Owner also alleges that Petitioner “provides no reason to modify Dong to have vertical word lines.” DD Brief, 24; POPR, 43. Again, Patent Owner misrepresents the record. For example, Petitioner offers extensive discussion that the desire for greater memory density motivated the transition from 2D NAND architectures to 3D NAND architectures. Pet., 12 (“[T]o further scale down the memory cell size, ‘three-dimensional (3D) NAND flash cells’ were developed.”); Liu, ¶110 (“More generally, as discussed in the Technology Background, there has

been a constant demand for increased memory density that has led to increasing number of memory cells in a memory string.”). Given the ubiquity of 3D NAND in 2020 as reflected in no fewer than three textbooks on the subject (Ex. 1009, Ex. 1010, and Ex. 1011), Patent Owner’s bare assertion that there exists “no basis to support that a POSITA would have had a reasonable expectation of success” does not even get off the starting block (POPR, 43).

E. Expert Testimony Accompanying the Petition

YMTC’s DD Brief also argues that the Petition’s “extensive reliance on expert testimony indicates that its assertions are better resolved in district court.” DD Brief, 22. Once again, the district court disagreed: it deferred to the Board and stayed the district court case. *See* Ex. 1073. In doing so, the district court signaled its belief that it is more appropriate for the **Board** to assess Micron’s arguments first.

Petitioner recognizes that, after it filed its IPR, the Board recently issued guidance stating that the “extent of the petition’s reliance on expert testimony” may play a role in the Board’s institution decision. March 26, 2025 Processes at 2. Here, the IPR does not use expert testimony in a way that favors denial. Patent Owner faults Petitioner for citing its expert declaration throughout the Petition. DD Brief, 22. But Patent Owner does not even challenge that the overwhelming majority of the expert’s analysis and opinions are correct on the merits and merely corroborative of the prior art itself.

Patent Owner’s only substantive quibble is with Petitioner’s expert opinion regarding the “bottom to top” limitation. *Id.*, 22-23. But Petitioner has already discussed at length how the Petition and prior art address and satisfy that limitation, under two separate interpretations. *See* II.D.6.

Petitioner also notes that, contrary to YMTC’s arguments, binding Federal Circuit precedent appears to require (or at least strongly favor) a thorough expert declaration like that accompanying the Petition. For instance, the Federal Circuit has explained that it is “reasonable for the Board to accept” one party’s “expert testimony over” the other party’s “bare attorney argument.” *Wasica Finance GmbH v. Continental Auto. Sys.*, 853 F.3d 1272, 1284 (Fed. Cir. 2017). In view of this, if Micron had not submitted comprehensive expert testimony with its Petitions, YMTC may have submitted its own expert testimony and then argued that this testimony—even if tenuous and poorly supported by the prior art—trumps whatever the Petition says. Next, the Federal Circuit has explained that a “[p]etitioner may not submit new evidence or argument in reply that it could have presented earlier.” *See VidStream LLC v. Twitter, Inc.*, 981 F.3d 1060, 1064 (Fed. Cir. 2020). Thus, if Micron did not address all claim limitations with expert testimony when it filed the Petition, it is unclear whether it would be able to do so as the IPR proceeds. It follows that without Micron’s own expert testimony, the Board may be deprived of relevant information to assess the technical accuracy of Patent Owner’s response

arguments. The Board's decision in this matter should be premised on facts and the prior art. Allowing both parties to submit expert testimony (and then subjecting that testimony to cross examination and discussion in briefing as provided for in the Board's rules) will ensure that the focus remains—as it must—on these facts and the prior art of record.

III. CONCLUSION

Petitioner respectfully requests the Director to instruct the merits panel to evaluate the merits of the Petition and issue an institution decision.

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: May 28, 2025

/Jeremy Jason Lang/

Jeremy Jason Lang
Lead Counsel for Petitioner
Reg. No. 73,064
1000 Marsh Road
Menlo Park, CA 94025-1015
T: (650) 614-7400
F: (650) 614-7401
Email: PTABDocketJJL2@orrick.com

*Attorney for Petitioner Micron
Technology, Inc.*

CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITIONER’S OPPOSITION TO PATENT OWNER’S BRIEF ON DISCRETIONARY DENIAL complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system’s word count, the paper—excluding the caption, table of contents, table of exhibits, certificate of word count, and certificate of service—contains 9,150 words.

Dated: May 28, 2025

/Jeremy Jason Lang/

Jeremy Jason Lang
Lead Counsel for Petitioner
Reg. No. 73,064
1000 Marsh Road
Menlo Park, CA 94025-1015
T: (650) 614-7400
F: (650) 614-7401
Email: PTABDocketJJL2@orrick.com

*Attorney for Petitioner Micron
Technology, Inc.*

CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing paper was caused to be served on May 28, 2025 via electronic mail, upon the following attorneys of record for the Patent Owner:

Inge A. Osman (inge.osman@lw.com)
Kevin Wheeler (kevin.wheeler@lw.com)
Brenda L. Danek (brenda.danek@lw.com)
Steven W. Peters (steven.peters@lw.com)
Amit Makker (amit.makker@lw.com)

/Karen Johnson/

Karen Johnson