Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory

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Abstract

We propose Bit-Cost Scalable (BiCS) technology which realizes a multi-stacked memory array with a few constant critical lithography steps regardless of number of stacked layer to keep a continuous reduction of bit cost. In this technology, whole stack of electrode plate is punched through and plugged by another electrode material. SONOS type flash technology is successfully applied to achieve BiCS flash memory. Its cell array concept, fabrication process and characteristics of key features are presented.

Introduction

It is strongly demanded to keep a trend of increasing bit density and reducing bit cost of flash memories. To achieve that, aggressive scaling of the device dimension and multi-level-cell have been developed. However, bit cost will turn to rise up near future, as shown in figure 1, because process cost will increase more rapidly than shrink rate.

One solution to avoid such situation is three dimensionally stacked array structures as reported in previous papers [1] [2], in which planar NAND structures are simply stacked. But there are two severe issues on those structures. One is that several critical lithography steps to make minimum feature size are necessary for each stacked layer. The other is that the area of driver transistors for control gates is multiplied by the number of layers. Dotted line in the figure 2 illustrates the estimated bit cost of three dimensionally stacked NAND, calculated by a simple formula inset in figure 2. It is important to note that the cost does not decrease or even increases due to a yield loss and an area penalty if the number of stacked layers is more than three.

In this paper, a novel SONOS flash memory using a newly devised Bit-Cost Scalable (BiCS) technology which realizes a multi-stacked array with a few constant number of critical lithography process steps, without area penalty and with continuous reduction of bit cost as shown as solid line in figure 2 is proposed.

Concept

Figures 3(a), 3(b) and figure 4 show schematic Birds-eye view, top down view of BiCS flash memory array and the equivalent circuit, respectively. String of the cells is on the plugs located vertically in the holes punched through whole stack of the gate plates. Each plate acts as control gate except the lowest plate which takes a role of the lower select gate. Cell size of BiCS memory is $6F^2/n$, where n is the number of control gate plates. Bit density can be increased by adding more gate plates, while the number of the critical lithography steps remains constant because whole stack of control gates is punched with only one lithography step. A single cell is accessed by control gate on the string which is selected by a bit line and an row select line. The bottom of memory plug is connected to source diffusion formed on the silicon substrate. For the erase operation of BiCS Flash memory, hole current which is generated by GIDL near the lower select gate is used. Edges of control gate are processed to be stair-like structure for via holes which are connected to driver transistors. They are shared by several rows of strings, so that the area for driver transistors does not increase even if more control gates are stacked. Table I summarizes the comparison of BiCS Flash and simply stacked 3D NAND.

Fabrication

Figure 5 shows the fabrication sequence. Lower select gate transistor, memory string and upper select gate transistor are fabricated individually. Gate material is P+ poly-Si. Holes for transistor channel or memory plug are punched through and LPCVD TEOS film or ONO films are deposited. The bottom of dielectric films are removed by RIE and plugged by amorphous Si. Arsenic is implanted and activated for drain and also source of upper device. Figure 6 shows schematic cross sections of vertical FET and SONOS memory cell on poly-Si gate. It should be pointed out that ONO films are deposited in the opposite order of the conventional SONOS device, i.e. from LPCVD TEOS film as top block oxide (5nm), LPCVD SiN film (11nm) and LPCVD TEOS film as tunnel oxide (2.5nm). Edges of control gate are processed into stair-like structure by repeating of RIE and resist sliming as shown in figure 8. For minimizing disturb, whole stack of control gate and lower select line are etched to have a slit which separates a block of memory plugs from each other. Only upper select gate is cut into line pattern to work as row address selector. Via hole and BL are processed on the array and peripheral circuit simultaneously.

Result and Discussion

Figures 7(a) and 7(b) show the cross sectional SEM images of the successfully fabricated 90nm BiCS flash cell array and the stair-like structure at the edge of control gates. Figure 7(c) is a top down photograph of n x 512k bit BiCS Flash macro.

Id-Vg characteristics of select gate FET (L=150nm, Φ=90nm) is shown in figure 9. Subthreshold slope is 250 mV/dec. In the case that Ioff is 30 pA, on-current is 2.4 μA. Figure 10 shows Id-Vg characteristics of the vertical SONOS FET after program and erase. Figure 11 shows the program/erase characteristics of SONOS FET. Endurance to 1E5 cycles is shown in figure 12. Vth shift is less than 0.5V after 1E4 cycle. Data retention measured on SONOS FET at initial and after 1000 cycles of endurance are shown in figure 13. 2.5V of Vth window is remains after 10years.

Conclusion

We have proposed BiCS flash memory as one of the most cost-effective memories to increase bit density. We have confirmed that this technology is a promising candidate for the Ultra High Density Memory.

Reference

[1]Soon -Moon Jung et al, IEDM Tech. Dig., pp 37-40, 2006.
[2]Erh-Kun Lai et al, IEDM Tech. Dig., pp 41-44, 2006.

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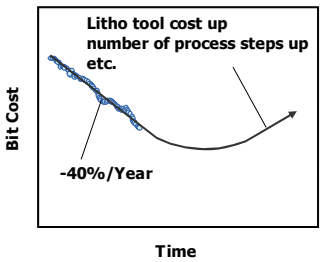
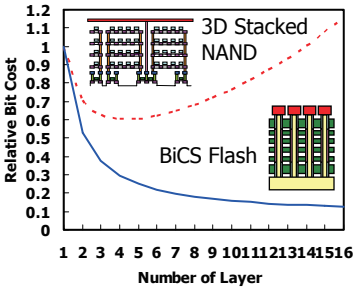


Fig. 1 Bit cost trend of flash memory.

TABLE I
Comparison of three dimensional flash memories.

	Pros	Cons
3D Stacked NAND	Expansion of Current Technology	Higher Cost (Large number of Lithography Steps)
BiCS Flash	Lower Cost (Small number of Lithography Steps)	New Technology - LPCVD tunnel oxide - Vertical FET - Multi Gate Stack RIE



$$\frac{1}{n}(C_f + nC_v)\left(\frac{1+A}{1-Y}\right)^{n-1}$$

n : Number of stacked layers.
C_f : Cost for common part.
C_v : Cost per single layer.
A : Area penalty rate per single layer.
Y : Yield loss per single layer.

Fig. 2 Bit Cost scalability of three dimensional flash memory.

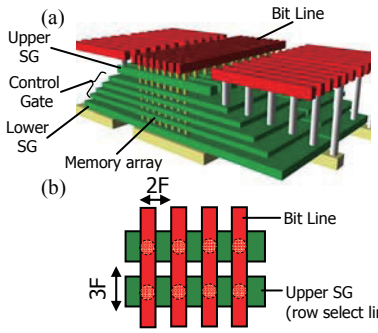


Fig. 3 (a) Birds-eye view of BiCS flash memory, (b) Top down view of BiCS flash memory array.

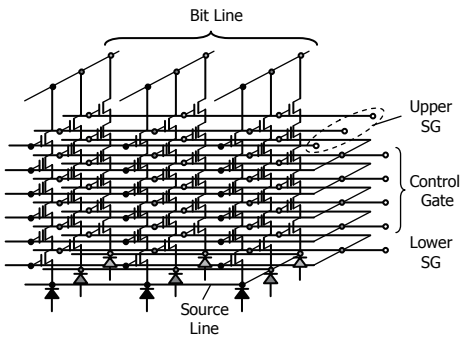


Fig. 4 Equivalent circuit of BiCS flash memory.

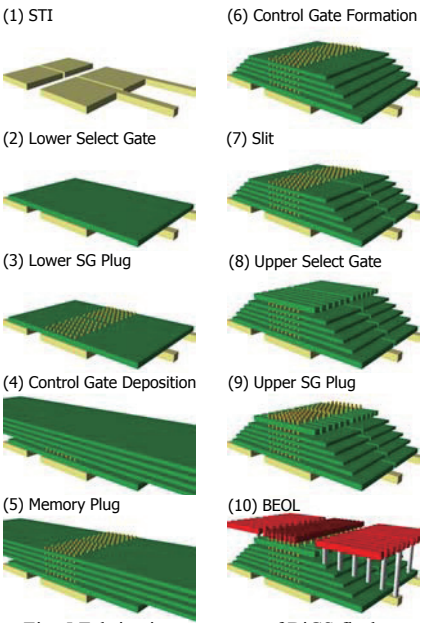


Fig. 5 Fabrication sequence of BiCS flash memory.

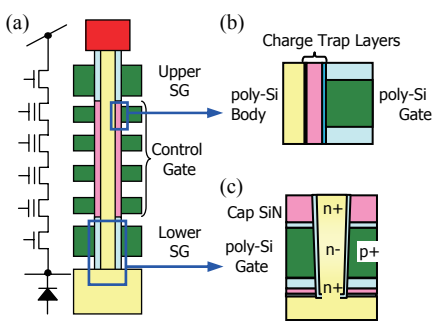


Fig. 6 (a) Cross section of BiCS flash memory string, (b) Cross section of vertical SONOS cell, (c) Cross sections of vertical FET.

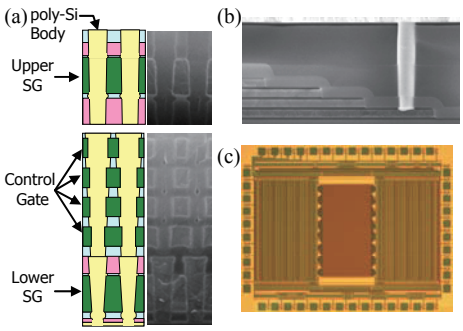


Fig. 7 (a) Cross sectional SEM of BiCS flash memory string, (b) Cross sectional SEM of edge of control gates, (c) n x 512 kbit macro image.

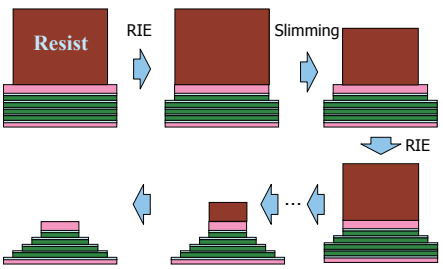


Fig. 8 Fabrication Sequence of edge of control gates into stair-like structure.

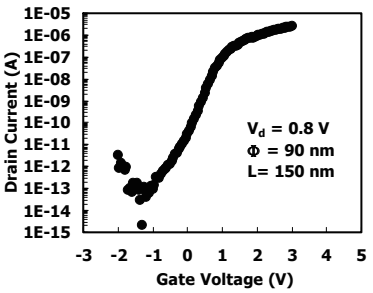


Fig. 9 Id-Vg characteristics of vertical transistor.

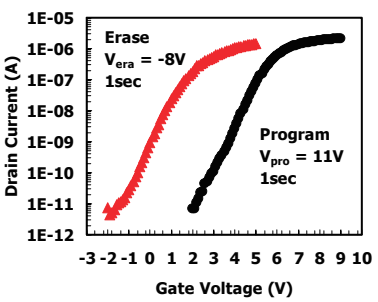


Fig. 10 Id-Vg characteristics for Program/Erase of vertical SONOS.

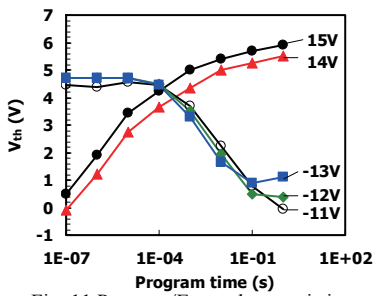


Fig. 11 Program/Erase characteristics.

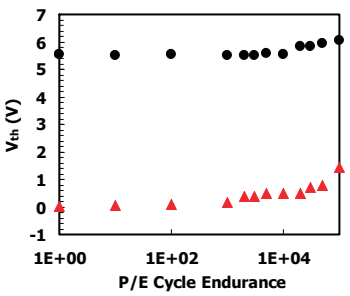


Fig. 12 Endurance of vertical SONOS.

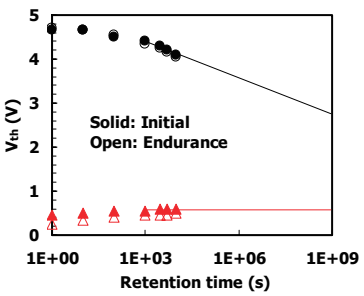


Fig. 13 Data retention of vertical SONOS.

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