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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Plaintiff,

v.

MICRON TECHNOLOGY, INC., et al.,

Defendants.

MICRON TECHNOLOGY, INC.,

Counterclaim Plaintiff,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD., and YANGTZE MEMORY TECHNOLOGIES, INC.,

Counterclaim Defendants.

Case No. 3:23-cv-05792-RFL

DECLARATION OF E. FRED SCHUBERT, PH.D. IN SUPPORT OF DEFENDANTS' PROPOSED CLAIM CONSTRUCTIONS (PATENT LOCAL RULE 4-3)

Honorable Rita F. Lin

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I, E. Fred Schubert, Ph.D., hereby declare:

I. INTRODUCTION

1. I make this declaration in support of certain proposed claim constructions of Defendant and Counterclaim Plaintiff Micron Technology, Inc.'s, and Defendant Micron Consumer Products Group LLC's (collectively "Micron") based on my personal knowledge, my experience, and my investigation into this case, including my review of the materials cited herein. If called upon as a witness, I could competently testify to the truth of each statement herein.

2. I have been retained by counsel for Micron in the above-captioned action to provide opinions regarding the construction of certain terms in the asserted claims of U.S. Patent Nos. 11,501,822 ("the '822 patent"), 10,872,903 ("the '903 patent"), and 11,568,941 ("the '941 patent").

3. My opinions provided herein are based on my years of education, research, and experience, as well as my investigation and study of relevant materials and materials that I was asked to consider (identified below). Further, I may also consider additional documents and information in forming further opinions, including documents that may not yet have been provided to me.

4. My analysis of the materials produced in this matter is ongoing, and I will continue to review any new material as it is provided. This declaration represents only those opinions that I have formed to date. I reserve the right to revise, supplement, or amend my opinions below based on new information and on my continuing analysis of the materials already provided.

II. COMPENSATION

5. I am being compensated for my services in this matter at my rate of $525.00 per hour. I am also being reimbursed for reasonable out-of-pocket expenses incurred as a result of my work in this matter. My compensation is not contingent upon the opinions I render or the outcome of this litigation.

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III. SUMMARY OF QUALIFICATIONS

6. I have summarized in this section my educational background, career history, publications, and other relevant qualifications. My *Curriculum Vitae*, which includes my qualifications, my publications within the last ten years, and my previous testimony at trial or by deposition, is attached as Exhibit A.

7. I am currently an active tenured full professor in the Department of Electrical, Computer, and Systems Engineering at Rensselaer Polytechnic Institute ("RPI") located in Troy NY. RPI is a private research university and the first technological university in the English-speaking world.

8. In 1978, I received a BS degree, and in 1981 an MS degree, both in electrical engineering and from the University of Stuttgart (Germany). From 1981 to 1985, I worked as a Member of the Scientific Staff at the Max Planck Institute for Solid State Research on field-effect transistors made of III-V semiconductors, for which I was awarded a Ph.D. degree in electrical engineering from the University of Stuttgart.

9. In 1985, following my education, I joined industry, AT&T Bell Laboratories, initially as a post-doctoral fellow and two years later as a member of technical staff and principal investigator. I worked for AT&T Bell Laboratories, in Holmdel, NJ, and Murray Hill, NJ, for a period of ten years, until 1995.

10. After my tenure in industry, I joined academia, initially Boston University (1995 to 2002) and subsequently RPI (2002 to present). At RPI, I have held various leadership positions, including head of the Future Chips Constellation, and Director of the Smart Lighting Engineering Research Center that was funded by the US National Science Foundation with forty million dollars over ten years.

11. I have been working in the field of silicon (Si) integrated circuit (IC) technology for more than 25 years. During my career in industry and academia, my work and research activities have included various aspects of Si IC technology.

12. For example, I conducted pioneering research in the doping of semiconductors. Generally, semiconductors such as Si are doped with dopants to provide them with the appropriate

type of electrical conductivity (n-type or p-type, that is, negative (electron) or positive (hole) type) as well as an appropriate magnitude of the electrical conductivity (frequently expressed by the concentration of dopants, *e.g.* 10^{18} dopants per cm^3). My research resulted in the shallowest junctions and the most well-defined doping profiles attainable in silicon. The very well-defined doping profiles are known under the technical term "delta doping" profiles because the doping profiles resemble the well-known delta function.

13. Another example of my research in Si ICs is my pioneering work in the field of materials with a very low dielectric constant. These materials are also known as low-k materials which have a dielectric constant lower than that of silica (SiO_2). Silica has a dielectric constant of 3.9. Historically, silica has been the standard and most commonly used dielectric material in Si IC technology. I developed highly porous SiO_2 by using the oblique angle deposition technique. The technique allowed my research group to demonstrate silica films with a porosity exceeding 90% and an associated dielectric constant lower than 1.5. I developed the theoretical underpinnings of the oblique angle deposition technique, specifically the dependence of the porosity on the oblique angle used during deposition. Parasitic capacitances can be formed across interlayer dielectric films. To keep the parasitic capacitances small, the dielectric constant of interlayer dielectric films should be as low as possible. Accordingly, low-k materials allow for a reduction of parasitic capacitances.

14. Yet another example of my work relates to CVD (Chemical Vapor Deposition) and ALD (Atomic Layer Deposition) equipment and associated fabrication processes. The dielectric material of gate insulating films (*i.e.*, the gate oxide of a field-effect transistor) as well as capacitor insulating films (*i.e.*, a capacitor for storing information) is commonly based on a high-k material (such as HfO_2 or ZrO_2). Nevertheless, a very thin SiO_2 layer is typically included in the insulating high-k films. I developed ALD processes that limit the thickness of the SiO_2 film to the desired value of essentially one atomic layer. I considered the diffusion of nonmetal atoms (such as oxygen atoms) as well as metal atoms (such as zirconium or copper atoms) when developing very thin dielectric layers for gate electrodes and storage capacitors.

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15. I am the author of the book "Physical Foundations of Solid-State Devices" (Google Books, Mountain View, 2015, ISBN-13: 978-0-9863826-2-8). The book presents and analyzes many fundamental concepts governing Si IC technology such as electrical contacts, Si inversion layers, and quantum tunneling. Tunneling phenomena can be a fundamental limitation to the development of Si IC technology. Fowler-Nordheim tunneling, a tunneling mechanism relevant in 3D NAND devices, is discussed in detail in my book. In my research, I have conducted analyses of tunneling currents, both desirable and undesirable, in metal oxides and metalloid oxides, relevant to the programming, reading, and erasing of 3D NAND memory cell transistors. My analyses included one-dimensional structures, as well as cylindrical structures (relevant for string-type geometries).

16. Throughout my career and to the present day, I have worked extensively and in a hands-on manner in Si fabrication facilities, also known as fabs. The fabs I worked in includes IBM's Boeblingen fab facility (Germany), AT&T's Holmdel and Murray Hill facilities (the latter one was also known as "blue zoo"), Boston University's silicon fabrication laboratory, and RPI's Micro and Nano Fabrication Clean Room facility.

17. My hands-on work includes a wide range of fabrication methods and associated tools such as material growth (epitaxy), material deposition (physical vapor, chemical vapor, and atomic layer deposition), material removal (wet chemical etching, gas-phase chemical etching, and physical ion beam etching), and material patterning (photolithography, 193 nm lithography, and electron beam lithography).

18. At my home institution, RPI, I regularly teach in the fields of Si microelectronics theory, Si IC fabrication technology, and Si integrated circuits. My teachings include advanced topics such as 3D integrated circuit devices, particularly 3D NAND devices, using floating gate and charge trapping technologies. I keep current with the state of technology in integrated circuits (including 3D NAND technology) through my regular reviews of technical journal articles, overview articles, and books. I have served regularly as technical reviewer for multiple technical journals. My research has included floating gate and charge trapping technologies, particularly the fundamental theoretical limits of retention times in 3D NAND devices.

19. I have consulted with industry and have served as a technical expert on various aspects of Si IC technology such as Si doping, 193 nm photolithography, shallow trench isolation, high-k dielectric gate insulating films, DRAM memory technologies, atomic layer deposition (ALD), and ALD equipment.

20. Several of my former Ph.D. students have joined the Si IC industry as engineers. Companies my former students chose to work for include Global Foundries (Malta NY), IBM (Fishkill NY), Intel (San Jose, CA) and Micron Technology (Boise ID).

21. I have received several awards for my technical contributions. They include: Senior Member IEEE (1993); Literature Prize of Verein Deutscher Elektrotechniker for my book "Doping in III-V Semiconductors" (1994); Fellow SPIE (1999); Alexander von Humboldt Senior Research Award (1999); Fellow IEEE (1999); Fellow OSA (2000); Boston University Provost Innovation Award (2000); Discover Magazine Award for Technological Innovation (2000); R&D 100 Award for RCLED (2001); Fellow APS (2001); RPI Trustees Award for Faculty Achievement (2002 and 2008); honorary membership in Eta Kappa Nu (2004); 25 Most Innovative Micro- and Nano-Products of the Year Award of R&D Magazine (2007); and Scientific American 50 Award (2007).

22. Further details about my education, experience, publications, prior testimony, and other qualifications are summarized in my *Curriculum Vitae* attached hereto as Exhibit A. As shown in that Exhibit, I have served as an independent technical expert consultant or expert witness in numerous patent litigations. I have been deposed and testified in patent litigations, including at a Markman hearing.

IV. MATERIALS CONSIDERED

23. In preparing this declaration, I reviewed and considered the materials cited by the parties in their respective Patent Local Rule 4-2 disclosures and Micron's amendments thereto as to terms for patents I discuss below and any other materials referenced in the body of this declaration, along with the '822, '903, and '941 patents and corresponding file histories.

24. I may use these documents and information, or other information obtained during the course of this proceeding, as well as representative charts, graphs, schematics and diagrams,

animations, and models based on those documents and information, to support and to explain my conclusions and opinions.

25. My conclusions and opinions are based in part on a review and analysis of the above-mentioned documents and materials. I have also drawn on my education, experience, and knowledge in reaching my conclusions and forming my opinions.

V. UNDERSTANDING OF THE LAW

26. I am not an attorney and will not offer opinions on the law. I have been advised of various legal principles that may be applicable to the issues discussed in this declaration, including claim construction. I have used that information in forming my opinions and arriving at my conclusions. My understanding of the relevant legal principles is set forth below.

27. I understand that claim construction is a legal question for the Court to decide. I understand that when a court construes a claim, claim terms are to be given the meaning they would have to one of ordinary skill in the art as of the effective filing date of the patent or the time of the invention, depending on the effective filing date of the patent. I further understand that claim terms are to be construed in light of the claim language, the patent specification, and the file history (collectively the intrinsic evidence). I understand that absent lexicography or disclaimer in the intrinsic evidence, claim terms should be assigned their plain and ordinary meaning as understood by one skilled in the art. As such, I understand that claims should not be construed to read out, or render nonsensical, express limitations of the claims. I understand that it is improper to read limitations from exemplary embodiments of the specification into the claims. And, I understand that claim terms should be interpreted in the context they are presented in the claim. However, I further understand claim terms should also be interpreted in light of the specification and prosecution history.

28. I understand that the applicant may act as a lexicographer in a variety of ways. For example, I understand that the intrinsic evidence may expressly define terms in the specification and that the claims should be interpreted consistently with those express definitions when the claims use those defined terms. I further understand that when the intrinsic evidence describes a particular feature as the invention, a claim may be required to be interpreted consistently with the patent's

definition of the invention. Similarly, I understand that when the intrinsic evidence consistently and repeatedly uses a term in a particular way, the claims of the patent may be construed to require an interpretation in accordance with the consistent and repeated use in the intrinsic evidence.

29. I also understand that extrinsic evidence, such as contemporaneous technical dictionaries, textbooks, expert testimony and the like may also be considered in claim construction to provide the understanding of one of ordinary skill in the art but typically is given less weight than the intrinsic evidence. I understand that extrinsic evidence cannot be used to vary or contradict the meaning of the claims that is unambiguous in light of the intrinsic evidence. I also understand that, to be informative of the meaning of a claim term, extrinsic evidence must reflect unbiased, contemporaneous reflection of the common understanding of the technical terms in question as to be considered a reliable source of information on the meaning attributed to those terms by those skilled in the art.

VI. LEVEL OF SKILL IN THE ART

30. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a person of ordinary skill in the art (a "POSITA") may have for combining references.

31. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art is also a person of ordinary creativity.

32. As to the '822, '903, and '941 patents, a person of ordinary skill in the art at the time of the alleged inventions would have had a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, developing, or teaching) NAND flash memory devices (including issues relating to the operation, *e.g.*, programming, of said devices), or an equivalent level of skill, knowledge, and

experience (*e.g.*, an advanced degree may replace some of the professional experience or additional professional experience may account for a different academic background).

33. In my opinion, this POSITA would have been aware of and generally knowledgeable about NAND memory's structure, its component parts, how it operates, and how it is controlled.

34. In view of my educational background (*e.g.* a Ph.D. in electrical engineering) and decades of experience working with semiconductor electronics and integrated circuits, as discussed in Section III, I was a person of more than the ordinary level of skill in the art as of the filing of the '822, '903, and '941 patents. My opinions herein, however, were formed considering the perspective of an ordinarily skilled artisan.

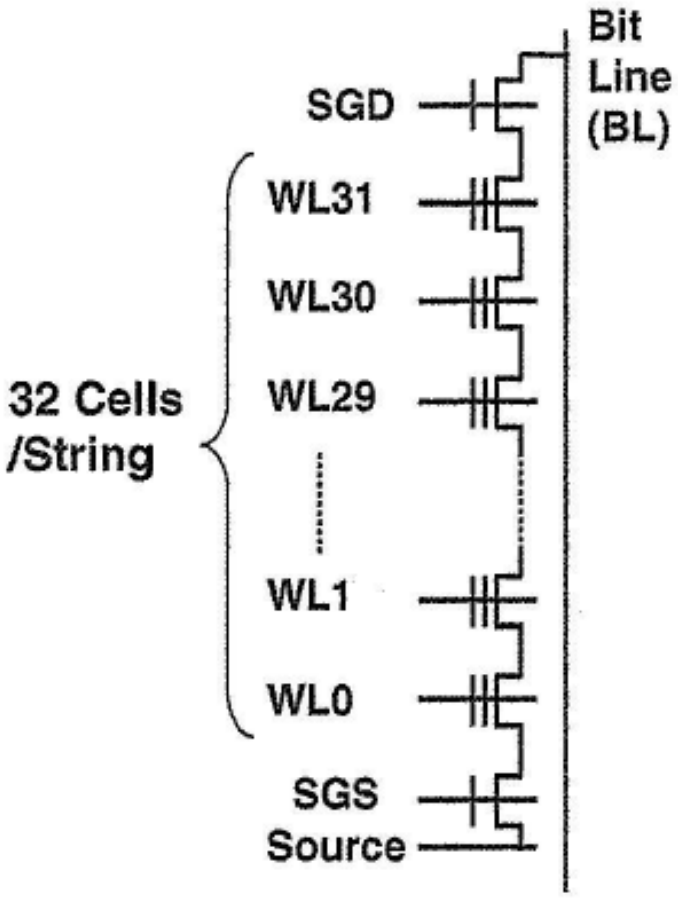
VII. TECHNOLOGICAL BACKGROUND

35. In this section I provide the background essential to understanding the relevant technology, as a POSITA at the time of the alleged invention would have understood the technology.

A. Structure of NAND Flash Devices

36. "Flash memory" is a type of digital memory that is "non-volatile" (that is, it retains the stored data even if the power source is removed). MYM0038844 (U.S. Patent No. 9,589,978 to Yip ("Yip")), 1:26-28.

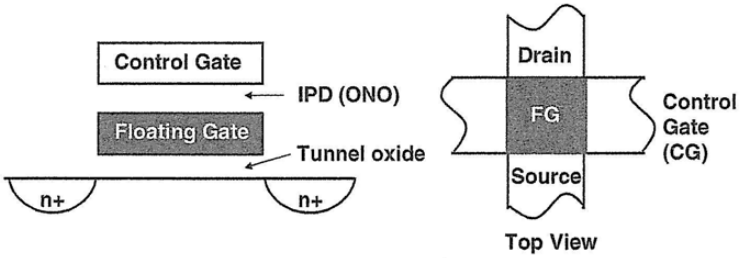
37. Flash memory is comprised of many flash memory "cells" (such as NAND cells) arranged in a "string" like arrangement where many cells are connected in series. MYM0027804 (Aritome, "NAND Flash Memory Technologies" (2016) ("Aritome")), MYM0027841. The flash memory device stores each bit of binary information into each of these cells. *Id.*, MYM0027841-42. The cells are surrounded by select transistors (SGD and SGS), one on the top (usually the drain side) and one of the bottom (usually the source side). A string of cells is shown in the illustration below:



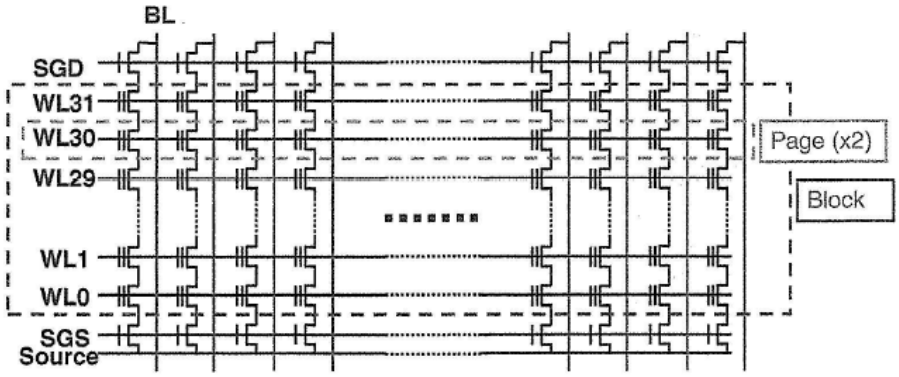
Id., MYM0027842.

38. Prior to the advent of 3D NAND devices, NAND devices were created as a two-dimensional array of cells on a substrate surface. *Id.*, MYM0027841.

39. Memory cells are located at the "intersection[s]" of the lines. *Id*. An example of this is shown below, with an example memory cell again shown in the top figure, and a two-dimensional array of such cells shown in the figure below:



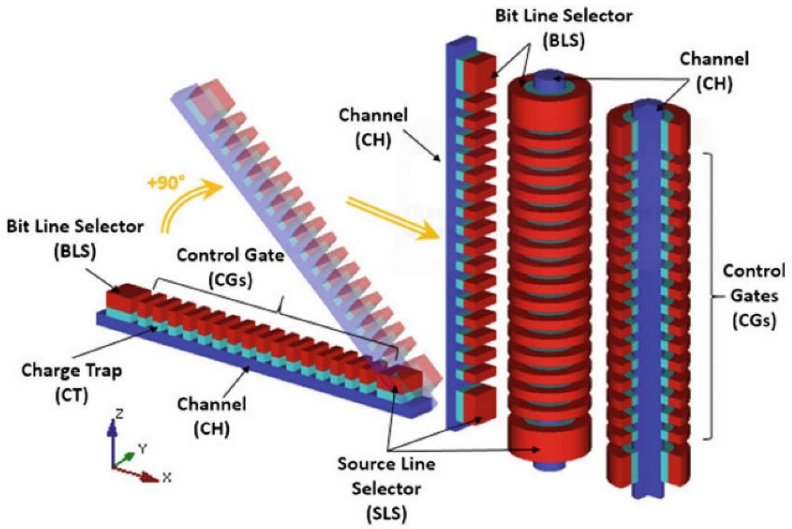
Id., MYM0027842.



Id., MYM0027843.

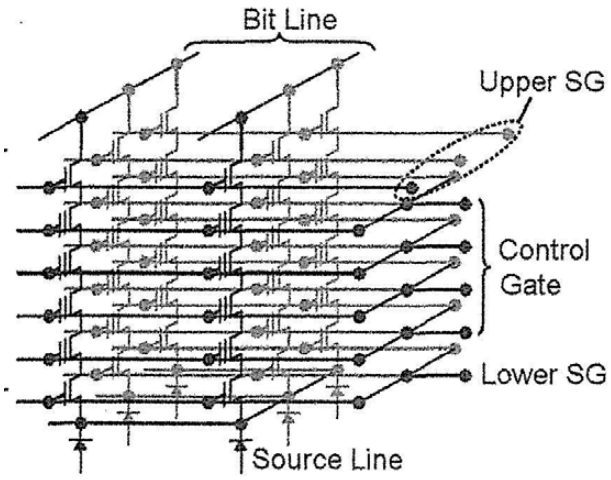
40. As the illustrated two-dimensional array above shows, multiple memory cells are connected in series and sandwiched between the "SDS" and "SGD" select transistors (on the source and drain side respectively), to constitute a NAND string of memory cells. Given that the select transistors, along with a respective data sensing circuitry for each NAND string are a fixed overhead cost, it is advantageous to place as many transistors as possible in a string to increase the capacity and density of the memory, and to amortize this overhead cost across as many memory cells as possible. In this manner, bit density per a given area can be maximized while the bit cost per memory cell is minimized. *See generally* Aritome, §§7.1-7.2.

41. This changed when "three-dimensional (3D) NAND flash cells" were developed. *Id.*, MYM0028095. "In order to further scale down the memory cell size of NAND flash memory," the art developed so-called "three-dimensional (3D) NAND flash cells" starting in about 2006. *Id*. In 3D NAND, rather than arranging memory cells in a two-dimensional array, 3D NAND arranges cells in a three-dimensional array that is built up in layers. A POSITA would have known that "[c]onceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." MYM0035101 (Silvagni, 3D NAND Flash Based on Planar Cells) at 103. The following image provides a demonstrative example of the relationship between the structure of a 2D NAND string and a 3D NAND string:



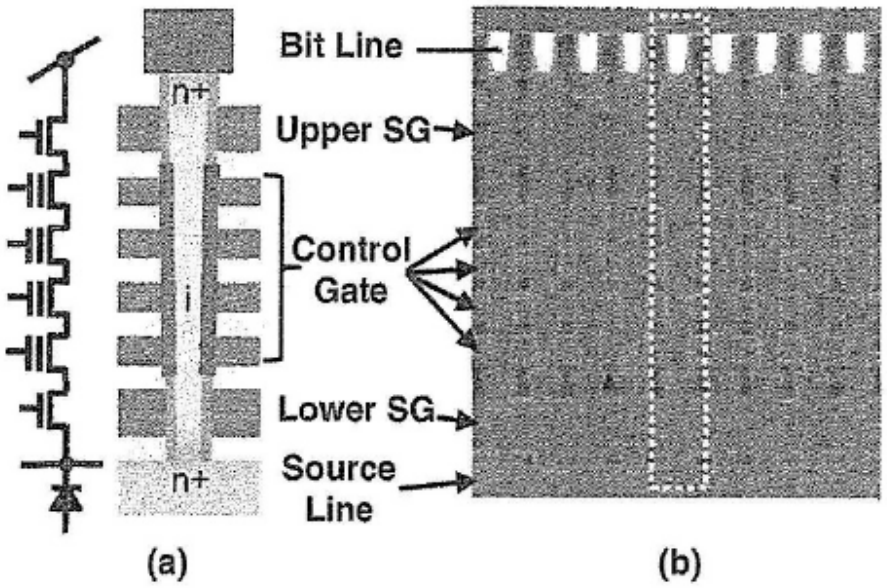
MYM0034141 (Micheloni et al., "Inside Solid State Drives (SSDs)" (2nd Ed. 2018) ("Micheloni Inside SSDs")) at 262.

42. Memory cells (which themselves comprise transistors) are formed vertically by stacking several alternating layers of metal and dielectric (for example, oxide such as SiO_2) around a cylindrical pillar. Aritome, MYM0028097-98. Each of the metal layers acts as the control gate (gate terminal) of a transistor. *Id.* Below is a figure illustrating how multiple such vertical pillars (channels or strings) are then repeated to form a three-dimensional array:

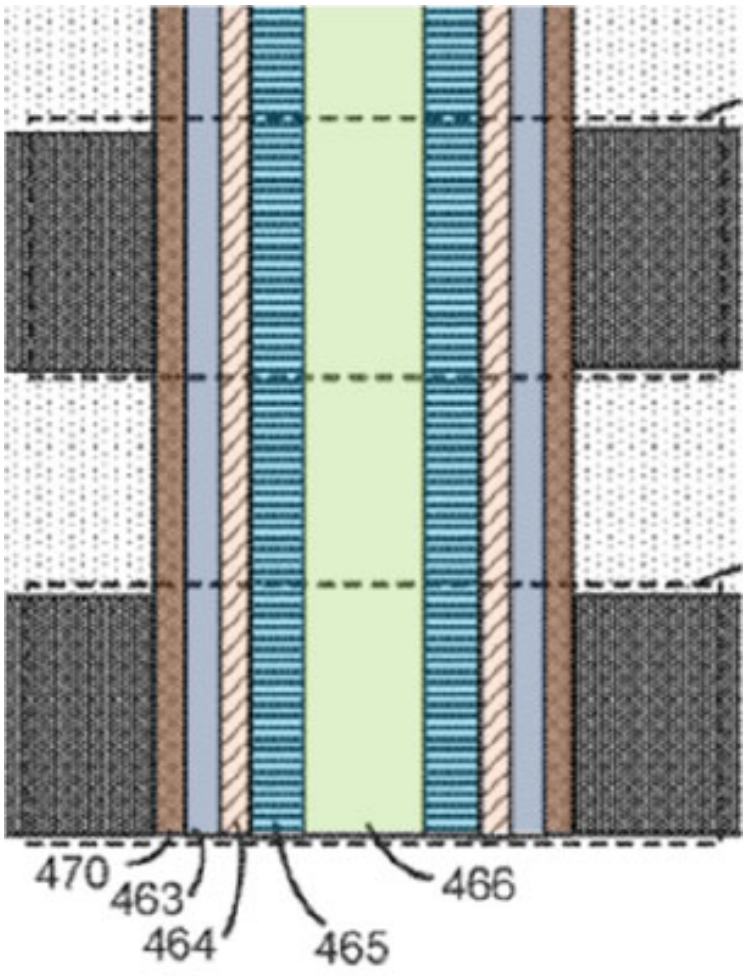


Id., MYM0028099. Selection of a specific vertical memory cell is done by using a wordline and a bit line, along with the select gates. *Id.*, MYM0028098-100.

43. As a further example, the figure reproduced below shows a 3D NAND vertical memory cell string with a charge-trapping layer:

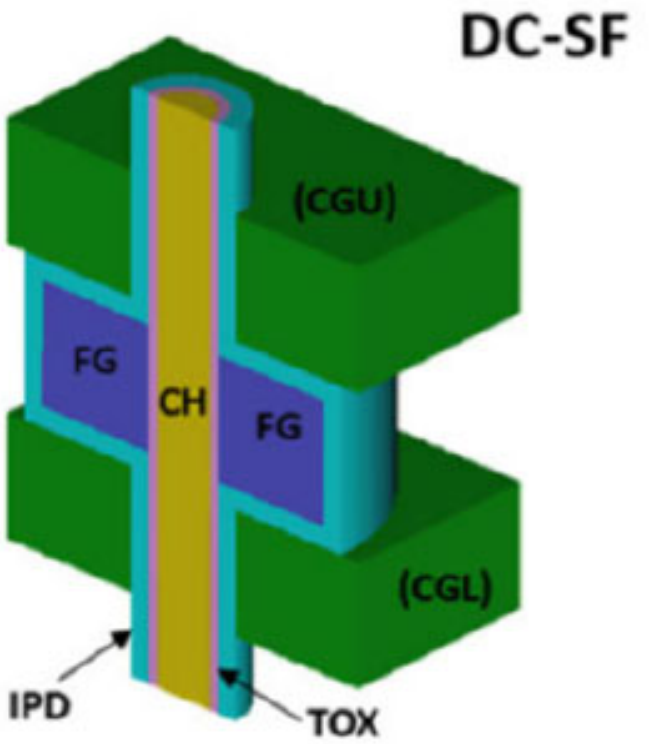


Id., MYM0028099. Here the sidewall, referred to as an ONO sidewall of the memory-string pillar, can comprise an oxide blocking layer (e.g., 470) ("O" in "ONO"), a nitride charge-trapping or storage layer (e.g., 463) ("N" in "ONO"), and an oxide tunneling layer (e.g., 464) ("O" in "ONO"), all shown in the figure reproduced and annotated below to show these various layers:



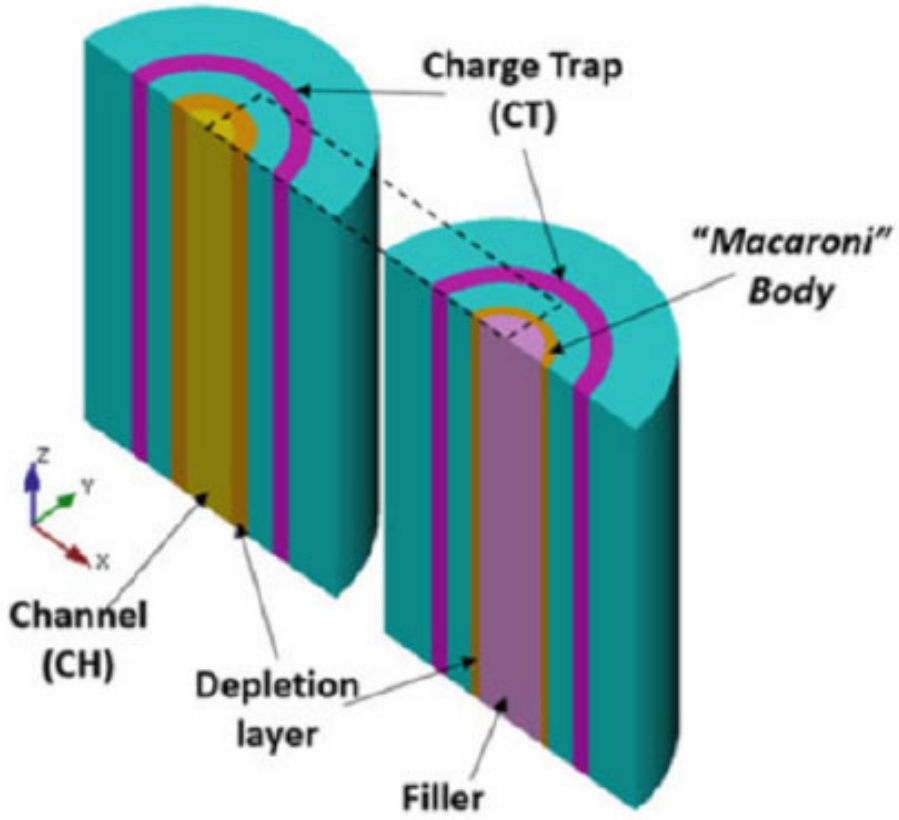
MYM0037822 (U.S. Pat. App. No. 2020/0168276), Fig. 4E (excerpted and annotated); *see also id.* [0083]; MYM0038909 (U.S. Patent No. 9,620,233 ("the '233 patent")), 13:19-26.

44. There are two common types of 3D Flash memory cells: conductive floating gate memory cells and charge-trap memory cells. In the conductive floating gate memory cell variant, the floating gates are conductive (or semi-conductive). Because of this the vertical memory string is made with multiple, separated floating gates as shown in the figure below:



MYM0033167 (Micheloni, 3D Flash Memories (2016) ("Micheloni 3D Flash")) at 311.

45. On the other hand, charge-trap technology uses a non-conductive data storage portion (such as silicon nitride). Because of this, the charge-trap layer is not separated and simply extends through the entire vertical string as depicted in the figure below:



Id., MYM0033272.

46. "Production of 3D NAND flash memory … started in August 2013." Aritome, MYM0028196. Given that the origins of 3D NAND came from 2D NAND, there are many similarities between 2D and 3D NAND flash memory devices, including basic principles of operation, memory storage techniques, the techniques and algorithms used to read, erase, and program memory cells and memory cell strings. In this context, the term "program" refers to writing/storing/saving data to a memory cell.

47. Memory cells are frequently organized into "blocks," "pages," or other groupings that are used for reading, writing, and erasing operations. "[R]ead and program operations are performed per page" while "the erase operation is performed per block." Aritome, MYM0027842.

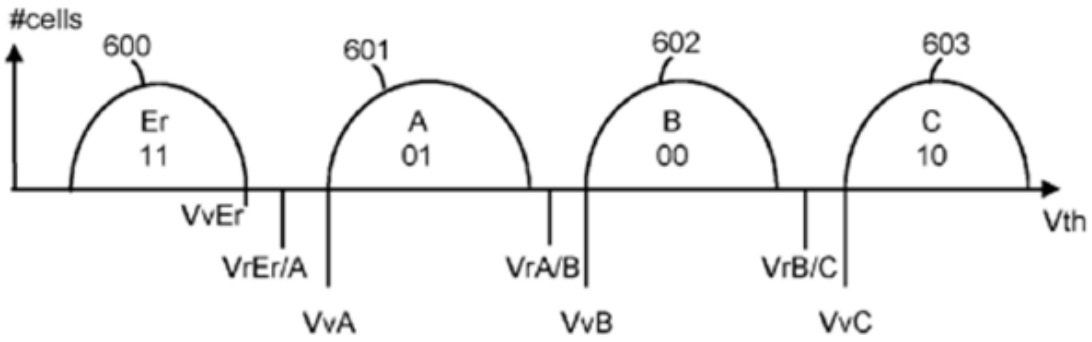
48. As the illustrations for the 3-D NAND flash array reproduced above showed, the strings of memory cells are placed in the vertical direction. In contrast, the wordlines (which function as the memory cell control gates), are horizontal conductive planes which intersect

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numerous memory strings at the same cell location in each string. Thus, any voltage that is applied on a given wordline will be applied as the control gate voltage to all the memory cells intersecting that plane.

B. Operation of 3D NAND Devices

49. When data is stored in a 3D NAND device, bits are "written" (stored) to the memory cells by a programming process. For example, if a memory cell is designed to store two bits, a memory cell may be "programmed" to store the data state of binary 00, 01, 10, or 11. This is achieved by storing some amount of charge in the cells' charge-storage material using a programming operation where a charged state represents one binary state and an uncharged state represents the other binary state. There is a "threshold voltage" (Vth) at which point the cell transistor turns on, and this threshold voltage level increases "in proportion to the amount of stored charge." *See*'233 patent, 13:43-49. A two-bit-per-cell NAND memory device may have a distribution of Vth-to-data-state as shown in the figure below:



Id., Fig. 6; *see also* Aritome, MYM0028145-147 (Fig. 7.77). Cells which are *unprogrammed* have the erased state "Er" and a low value of Vth. *See* '233 patent, 14:11-12.

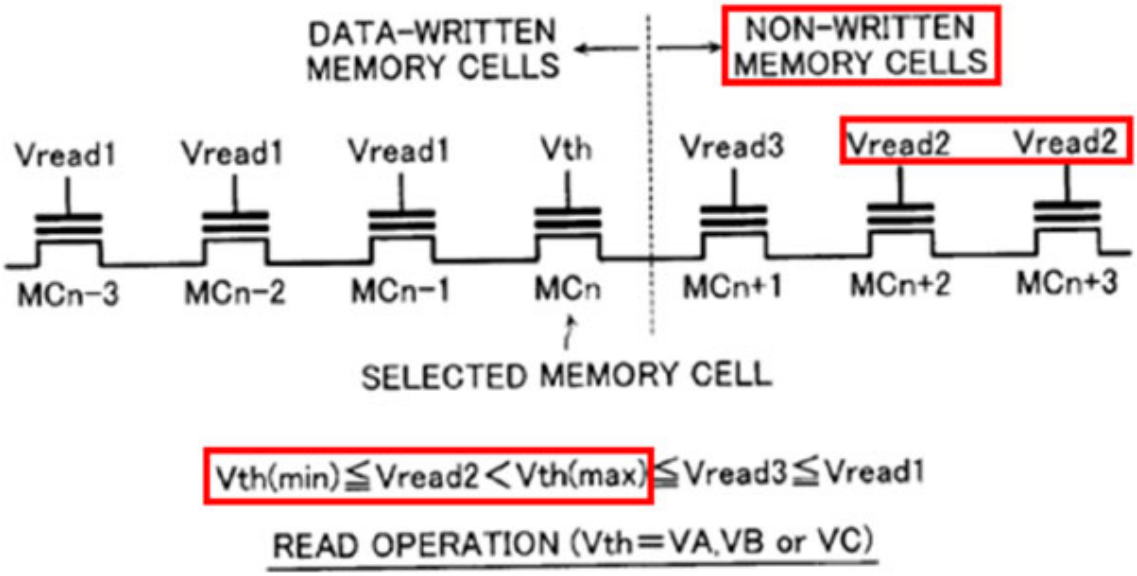
50. To read the memory cells during read operations, the threshold voltage of the selected cell to be read is measured and its data state is determined from that measurement. *Id.*, 3:10-11, 9:66-10:15, 14:34-37. All cell transistors on a selected memory string—except the selected cell to be read—can be supplied with a control gate voltage (also referred to as a pass voltage) that is higher than the highest Vth of all possible data states to make the transistors conductive. *Id.*, 3:21-27, 3:33-37. A read voltage that is between two data states is applied to the

control gate of the selected cell. *Id.*, 3:22-29, 14:31-34. If that read voltage is *higher* than the Vth of the selected cell, the cell transistor turns on and the memory string conducts current. Otherwise, the string does not conduct current. Sensing whether current is conducted allows the threshold voltage of the selected cell to be measured and then the data state can be determined. *Id.*, 3:10-11, 9:66-10:15, 14:34-37.

51. During a typical programming operation, the memory cells are programmed according to a wordline programming order as the operation is performed from one end of the string to the other end. NAND memory programming typically involves iteratively repeating two related, but distinct, operations: a programming operation and a read operation where the read operation is also known as a *verify* operation. For 3D NAND flash devices, the programming option is generally done via a process known as "incremental step pulse programming" or "ISPP." The ISPP process involves applying a voltage pulse to a control gate of the selected wordline to inject electrons into a charge-storing part of the transistor and, at the same time, applying a pass voltage to unselected wordlines. *See, e.g.*, MYM0038613 (U.S. Patent No. 9,361,993 ("the '993 patent"), 11:47-49. After this, a read (verify) operation may be performed to verify that the memory cell has been correctly programmed (i.e., determine whether the programming pulse was sufficient). *See, e.g.*, MYM0035540 (U.S. Patent No. 10,276,251), 10:43-47; '993 patent, 11:50-52; '233 patent, 3:21-29. The ISPP process will stop if the verify operation confirms that the memory cell was programmed to a proper threshold voltage. *See* '993 patent, 11:27-32. If the verify operation fails to confirm this, the ISPP process will continue until a proper threshold voltage is reached. Memory cells on a memory string are typically programmed from one end to the other (for instance, from the source side to drain side, or vice versa). *See, e.g.*, Aritome, MYM0027848 (Fig. 2.12); MYM0037760 (U.S. Pat. Pub. No. 2019/0348122) [0110]-[0112].

52. Storing data in and reading data from NAND flash is subject to various influences that reduce its reliability including, but not limited to, data-retention degradation and read disturb. *See* Aritome, MYM0027831. For example, read disturb can occur when read operations repeatedly apply high pass voltages on unselected wordlines, which induces an unexpected boosting effect in unselected cells in a NAND string called hot-carrier injection or "HCI." *Id.*, MYM0028057. "To

limit read disturb on unselected wordlines during sensing, the value of [pass voltage] may generally be set as low as possible to ensure that the memory cells are conductive and appropriately act as pass gates." *See* MYM0037191 (U.S. Pat. Pub. No. 2018/0012667) [0096]. Because of this, a lower pass voltage may be applied to unprogrammed cells since they have low threshold voltages. *See*, MYM0036348 (U.S. Pat. Pub. No. 2013/0077404) [0052]-[0062].



Id., Fig. 6 (annotated).

53. In addition to data storage and reading reliability issues, 3D NAND designs also account for reliability issues encountered during programming.

54. As discussed above, typical 3D NAND is formed from an array of memory cells arranged in rows and columns. This arrangement of memory cells results in each cell being in close physical proximity to other cells in multiple directions. This close proximity, coupled with the application of various different voltages to adjacent cells during programming, results in a well-known "phenomenon" referred to as "[p]rogram disturb." Aritome, MYM0027855.

55. "Program disturb" involves "the threshold voltage … of unselected cells" undesirably "increas[ing] during program operation." Aritome, MYM0027855-56. This threshold voltage increase can in turn cause cells not identified for programming modification to enter a different/unintended programmed state. *Id.*

56. When the ’822 patent was filed, it was known that voltages applied during programming (for example, voltages applied to wordlines above and below the memory cell to be programmed) can be selected such that the potential for program disturb is minimized. Aritome, MYM0027855-56.

VIII. THE ’822 PATENT

A. The ’822 Patent’s Effective Filing Date

57. For purposes of this declaration, I have been instructed to use October 22, 2019, as the effective filing date of the ’822 patent. With respect to the ’822 patent, my opinions in this declaration were formed from the perspective of a person of ordinary skill in the art as of October 22, 2019, including both the knowledge of a person or ordinary skill in the art at that time as well as how a person of ordinary skill in the art would have understood the ’822 patent.

B. Overview of the ’822 Patent

58. The ’822 patent relates to a “control method” for a “three-dimensional (3D) NAND flash memory” device. ’822 patent, 1:15-29.

59. Per the patent, typical “3D NAND memory architecture stacks memory cells vertically in multiple layers, achieving a higher density….” ’822 patent, 1:29-32.

60. “As more layers are added, the bit density increases, thus increasing … storage capacity.” ’822 patent, 1:32-33.

61. However, while storage capacity increases the patent explains that “[w]ith the layer increases, … program disturb becomes worse.” *Id.*, 1:34-35.

62. According to the patent, the prior art attempted to address this “program disturb” by applying “[a] pre-pulse signal … to an unselected bit line….” ’822 patent, 1:34-37. But when additional layers are employed to increase memory density, a longer memory string channel results which in turn “reduce[s]” “[t]he effect” of such a “bit line pre-charge.” *Id.*, 1:39-41.

63. “A traditional method for improving the bit line pre-charge effect” for these longer channels “is to extend the bit line pre-pulse time.” ’822 patent, 1:41-44. This, however, results in slower programming. *Id.* Another “traditional method” entails “increas[ing] the voltage level of

the bit line pre-pulse." '822 patent, 1:44-48. This "increase[s] the risk of the breakdown" of the "bit line transistor." *Id.*

64. Rather than employing what it identifies as "traditional methods," the '822 patent "appl[ies] wordline pre-pulse signals with different voltage levels" for purposes of "reducing programming disturb." '822 patent, 1:17-19. Per the patent, the further a wordline is "away from the selected wordline, the larger voltage level of the" applied "wordline pre-pulse signal[.]" *Id.*, 4:39-43.

65. The '822 patent alleges that using these types of "wordline pre-pulse signals" "enhance[s]" "the channel potential gradient" in the unselected NAND strings, which in turn "enhance[es] the pre-charge effect" and "reduc[es] programming disturb." '822 patent, 4:54-59.

66. Figures 3 and 4—which are annotated below to show the patent's different groupings and applied pre-pulse signals—provide an example of this.

67. Figure 3 shows a single unselected "memory string." '822 patent, 5:7-11.

68. Connection of the "memory string" to an "unselected bit line BL" is controlled by a "top select gate line TSG" (green). '822 patent, 5:11-15.

69. "[W]ordlines WL0 to WLn" pass through the memory string. '822 patent, 5:14-16.

70. "WL0" (yellow) is currently "the selected wordline" (*i.e.*, the wordline connected to the memory cell to be programmed). '822 patent, 5:18-20.

71. The other wordlines that are not selected are divided into a "first group" (blue "Bottom WL"), "second group" (orange "Middle WL"), and "third group" (purple "Top WL"). '822 patent, 5:19-34.

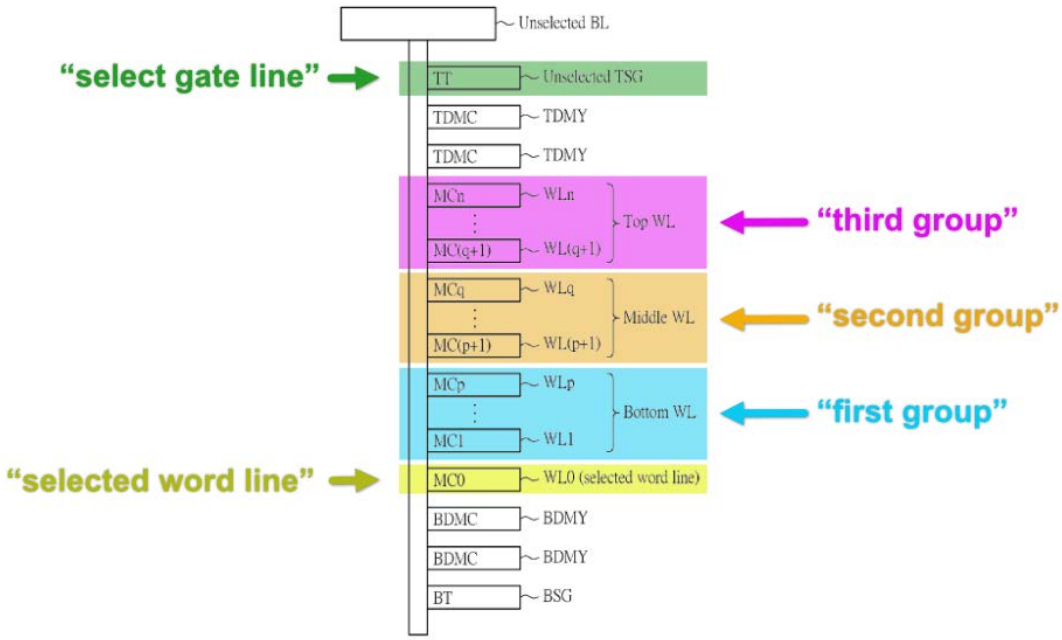


FIG. 3

'822 patent, Fig. 3.

72. Figure 4 is a "signal timing diagram of" Figure 3's "memory string[.]" '822 patent, 5:35-38.

73. As shown in this figure, three different "wordline pre-pulse signals"— with maximum voltages labeled VP_BOTTOMWL (blue), VP_MIDDLEWL (orange), and VP_TOPWL (purple) in the figure—are applied to the three groups of wordlines. '822 patent, 5:50-55.

74. As shown in the figure, each of these "pre-pulse signals" is applied in the form of a pulse. The voltage increases from 0V to another value for a period of time, and then returns back to 0V. The maximum voltage level of these pulse signals increases with distance from the "selected wordline." The applied signal is a "pre-pulse" because it is applied (*i.e.*, it starts and then stops) in advance of a later programming step shown to the right of the figure. During this later programming step, the selected wordline is supplied with a programming voltage pulse (Vpgm) while the unselected wordlines are supplied with a pass voltage (Vpass):

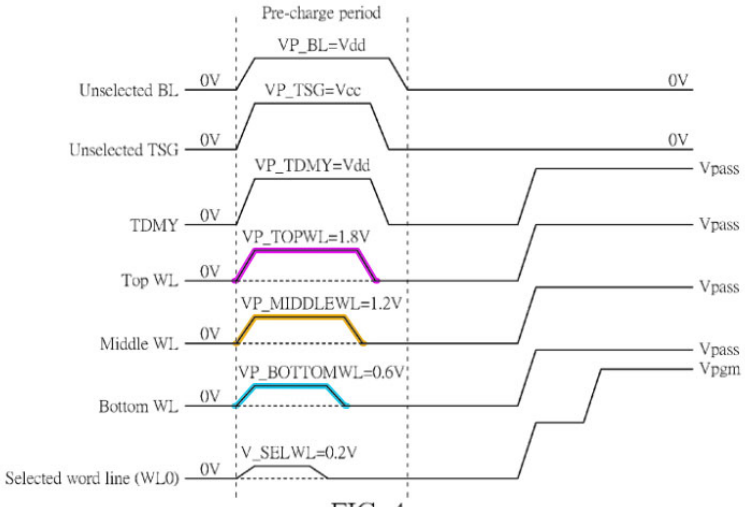


FIG. 4

'822 patent, Fig. 4.

C. <u>The Prosecution History of the '822 Patent</u>

75. I have reviewed the '822 patent's prosecution history. During prosecution, the claims were rejected only on double patenting grounds. No other prior art was discussed by the Examiner. *See* '822 Patent File History, 12/30/2021 Office Action.

76. I have also reviewed the prosecution history of the '822 patent's parent application: U.S. App. 16/709,944. *See* U.S. Pat. App. 16/709,944 File History ("'944 Application FH").

77. During prosecution of this application, the claims were rejected over U.S. Patent No. 10,283,202 ("Chen") and U.S. Pub. 2011/0194351 ("Kim"). *See id.*, 1/15/2021 Office Action. The Examiner noted that Chen taught two different wordline pre-pulse voltages (0 or 2V). *Id.*

78. In response, Applicant amended the pending claims to require (1) "first," "second," and "third" "pre-pulse signal" voltages, (2) "first," "second," and "third" groups of wordlines arranged in order between the "selected wordline and the select gate line," and (3) increasing "pre-pulse signal" "voltage levels" from the "first" to the "third" group. *Id.*, 3/4/2021 Applicant Response and Amendment. This then led to allowance of the pending claims in the parent application. *See id.*, 4/5/2021 Notice of Allowance.

D. The Relevant Claims of the ’822 Patent

79. I understand that claims 1 and 2 of the ’822 patent are asserted in this case. Out of that group of asserted claims, claim 1 is the only independent claim.

80. Independent claim 1 recites:

1[pre] A memory device, comprising:

1[a] a plurality of memory strings;

1[b] a bit line connected to a first memory string of the plurality of memory strings;

1[c] a select gate line connected to the first memory string of the plurality of memory strings;

1[d] a selected wordline of a plurality of wordlines, wherein the plurality of wordlines is connected to the first memory string; and;

1[e] a control circuit configured to

1[e(1)] apply a first wordline pre-pulse signal of a plurality of wordline pre-pulse signals to a first group of the plurality of wordlines during a pre-charge period;

1[e(2)] apply a second wordline pre-pulse signal of the plurality of wordline pre-pulse signals to a second group of the plurality of wordlines during the pre-charge period; and

1[e.(3)] apply a third wordline pre-pulse signal of the plurality of wordlines pre-pulse signals to a third group of the plurality of wordlines during the pre-charge period,

1[e(4)] wherein a voltage level of the second wordline pre-pulse signal is greater than that of the first wordline pre-pulse signal, and a voltage level of the third wordline pre-pulse signal is greater than that of the second wordline pre-pulse signal.

E. DISPUTED TERMS

81. I have been asked to provide my opinions regarding the parties’ proposed constructions for one claim term of the ’822 patent. That term is set forth below.

i. “wordline pre-pulse signal” (Claim 1)

Micron’s Proposed Construction	YMTC’s Proposed Construction
“a signal that increases in value and then decreases in value (or vice versa) before a programming step”	“pulse signal to prepare wordlines for a programming step”

82. Independent claims 1 and 11 reference and require a "first," "second," and "third" "wordline pre-pulse signal." In my opinion, a POSITA would have understood this "wordline pre-pulse signal" to be "a signal that increases in value and then decreases in value (or vice versa) before a programming step." In other words, a "pulse signal" has both a defined beginning and defined end, both of which occur before the subsequent programming step. This is consistent with the plain and ordinary meaning of the claim term, the context provided by surrounding claim language, the figures of the '822 patent, and discussion of the terms in the '822 patent's specification.

83. To begin, this claim term requires a signal in the form of a "pulse." The term "pulse" had a well-understood meaning in the art at the time the '822 patent was filed. In particular, a POSITA would have understood this to refer to a signal that increases and then decreases in value (or alternatively, decreases and then increases in value).

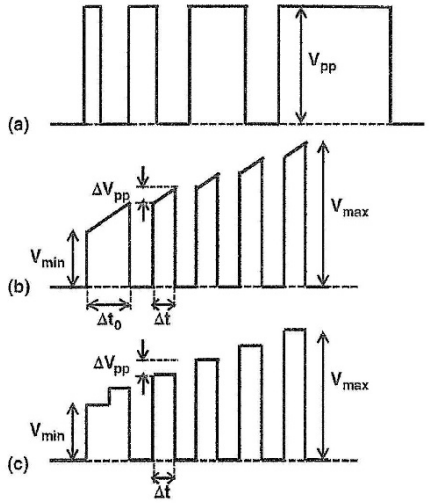
84. Multiple dictionaries—including both standard and technical dictionaries—define the term "pulse" in this way:

- "quick change in the current or voltage produced in a circuit used to operate an electrical switch or relay or which can be detected by a logic circuit" (Newton's Telecom Dictionary (26th ed. 2011) (MYM0068599) at 601);
- "[a] wave that departs from a first nominal state, attains a second nominal state, and ultimately returns to the first nominal state" or "[a] variation in the value of a magnitude which is short in relation to the time schedule of interest, the final value being the same as the initial value" (IEEE Standard Dictionary of Electrical and Electronics Terms (1996) (MYM0069160) at 162-63);
- "[f]or a quantity which is normally constant, a well-defined variation which increases from a steady value to a maximum, then back to or near the original value, all in a comparatively short time" (Wiley Electrical and Electronics Engineers Dictionary (2004) (MYM0069175) at 177); and

- "a transient amplification or intensification of a characteristic of a system, esp. of a wave characteristic, followed by a return to equilibrium or a steady state" (Webster's II New College Dictionary (2001) (MYM0068603) at 605).

85. As can be seen, in all cases the term "pulse" refers to a signal that starts at one value, increases or decreases to another value, and then returns back to its original value.

86. An example of one such "pulse" is provided below. This figure depicts "conventional" NAND "program pulse waveforms" employed when programming NAND memory cells. As shown, each "pulse" entails an increase in voltage from an initial state (*i.e.*, the pulse has a beginning), followed by a return back to that original state after a period of time (*i.e.*, the pulse has an end):



Aritome, MYM0027920-21.

87. The '822 patent's dependent claims serve to further confirm that the claimed "pulse" requires a signal that increases and then decreases (or decreases and then increases) such that the signal has a defined beginning and end.

88. In particular, claim 10—which depends on claim 1—specifies that the "pre-pulse signal[s]" of claim 1 have various different "pulse duration[s]":

> wherein a pulse duration of the second wordline pre-pulse signal is greater than that of the first wordline pre-pulse signal, and a pulse duration of the third wordline pre-pulse signal is greater than that of the second wordline pre-pulse signal.

89. While claim 1 does not use the word "duration," the claims nonetheless presume that all pulses have such a "duration." If this were not the case, the limitation added by claim 10 would not make sense in context: pulse durations cannot differ from pulse-to-pulse as claim 10 requires if the pulses did not have durations in the first place. And a pulse has a "duration"—which can differ from pulse-to-pulse as claim 10 requires—because it has a defined start and end. A signal without a defined start (or a defined end) is not a pulse and has undefined duration that cannot vary from signal-to-signal. Instead, a pulse requires both a defined start and a defined end to have a pulse duration. In other words, a pulse has a pulse duration associated with it. Without the pulse having rising and falling edges (or falling and rising edges), the pulse duration becomes meaningless.

90. Consistent with this usage of the term in the '822 patent's claims, it was generally known in the art at the time the '822 patent was filed that pulses have determinable widths or durations. *See, e.g.,* Comprehensive Dictionary of Electrical Engineering (2d ed. 2005) (MYM0068593) at 595 ("Pulse width" is "width of the temporal region over which a pulse has significant amplitude; sometimes represented more specifically as, for example, full width at half maximum"); New Penguin Dictionary of Computing (2001) (MYM0068596) at 598 ("pulse width" at is the "the duration of the higher voltage portions of a SQUARE WAVE signal (that is, the tops of the waves), which may be varied in length to carry information (see MODULATE).") Because a pulse has a determinable width and duration, a POSITA would understand that it must also have a defined beginning and end.

91. The '822 patent specification uses "pulse" in a way that is entirely consistent with the above construction and plain and ordinary meaning of the term.

92. For example, the specification explains that the patent's "pre-pulse signal[s]" have both a "rising edge" and an "ending," "end point," or "falling edge." '822 patent, 6:30-7:18.

93. Likewise, the specification notes that the "wordline pre-pulse signals" have a "pulse duration" "[d]uring the pre-charge period." *Id.*, 7:21-35. Again, a "pulse" can only have a "duration" if it also has both a defined beginning and a defined end.

Micron Ex. 1076, p. 27
Micron v. YMTC
IPR2025-00190

94. Next, according to the ’822 patent, Figs. 4 and 5 are “signal timing diagram[s]” showing, among other things, the patent’s “pre-pulse signal.” *Id.*, 5:35-64, 6:9-10. Figure 4 is reproduced below:

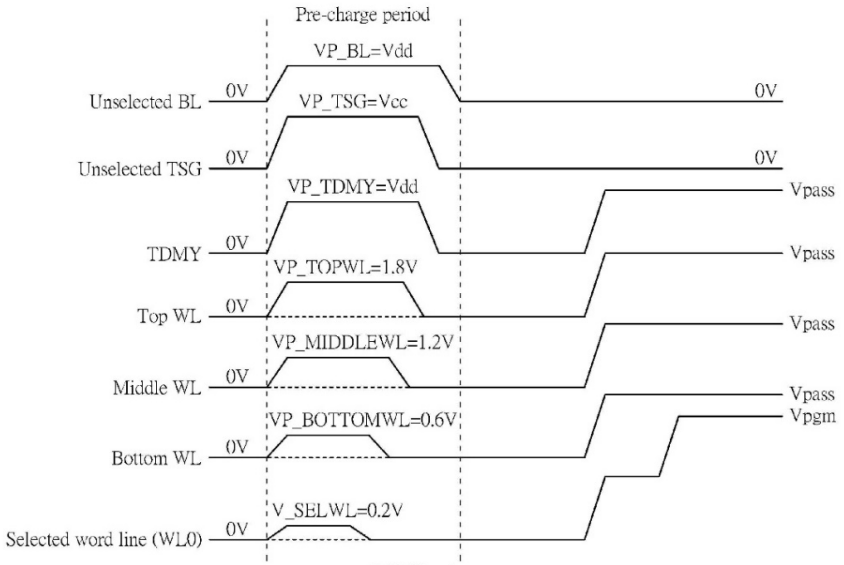


FIG. 4

Id., Fig. 4.

95. The figure shows “pulse[s]” applied to, among other lines, a “Top WL,” “Middle WL,” and “Bottom WL.” In all cases, the pulses applied to these lines increase in value (have a defined beginning) and then decrease in value (have a defined end).

96. For example, the “Top WL” begins at 0V. Then, a pulse signal is applied increasing the line’s voltage to VP_TOPWL=1.8V. This pulse signal then ends, allowing the line’s voltage to return back to 0V before a subsequent programming step.

97. The pulse signals applied to the “Middle WL” and “Bottom WL” are similar: the line’s voltage starts at 0V, a pulse signal is applied increasing voltage (to either VP_MIDDLEWL=1.2V or VP_BOTTOMWL=0.6V). This pulse signal then ends allowing the line’s voltage to return back to 0V before the actual programming. Figure 5 is similar, except it employs negative as opposed to positive voltages. *See id.*, Fig. 5. To summarize, all pictorial disclosures in the ’822 patent of the pulse signals show a defined beginning and end.

98. While the '822 patent does reference a wordline pre-pulse signal "voltage level" (*e.g.*, '822 patent, 1:54-55, 2:7-8) this does not re-define the term in a way that departs from its plain and ordinary meaning. This "voltage level" is simply the voltage to which the pre-pulse signal increases (or decreases) for a fixed period of time in advance of programming before returning back to its original value. *See, e.g., id.*, Figs. 4-5, 6:30-7:18.

99. I also understand that YMTC itself characterized the claimed "pulse signal" as having a defined beginning and end. In particular, in its preliminary response in IPR2024-00795, it explained that the claimed "pre-pulse signal [that] prepares the wordline before the programming step" is "in the form of a pulse" with a "duration," and "does not include a flat voltage." *See* MYM0080152 (Preliminary Response), pp. 17-19. In other words, a "pulse" has a "duration" (i.e., it starts and ends) and is not simply a "flat voltage." Unlike a "pulse," a flat voltage would not have a distinguishable start and end and would not increase and then decrease in voltage as a pulse does. Further, I understand that YMTC took a similar position in its patent owner response. There, it represented that construing "pulse" to mean a "signal that must increase in value and then decrease in value (or vice versa)" is "supported by the intrinsic record." MYM0092479 (IPR2024-00795, Paper 12), p. 13. YMTC then proceeded to discuss the same claim language, specification passages, and dictionary definitions I cite above. *See id.*, pp. 13-16. More particularly, according to YMTC, the '822 patent's claims "confirm that" a pulse must have "a beginning and an end." *Id.*, p. 14. Moreover, YMTC states that "[t]he specification further confirms that a 'pulse' must increase in value and then decrease in value (or vice-versa)." *Id.* And, YMTC further agreed that "dictionary definitions" would have led a POSITA to the same conclusion regarding the meaning of the term "pulse": the term references a signal that "[i]ncreas[es] in value and then decreas[es] in value (or vice-versa)…." *Id.*, p. 16. YMTC also repeatedly distinguished the claimed "wordline pre-pulse signal" from a "flat voltage signal" that does not increase/decrease and then return to its original value in advance of programming. *See, e.g., id.*, pp. 16, 24, 31, 39, 40, 42, 43, 44. According to YMTC, the claimed "pre-pulse signal" requires more than "pre-bias voltages … applied as a single, flat, value followed immediately by programming voltages." *Id.*, p. 31. I agree. To be a "pulse," the voltage applied to a wordline must increase/decrease from an original value

for some duration, and then return to that original value. YMTC's IPR expert also took this same claim construction position—repeating the statements YMTC made in its patent owner response—further confirming that a POSITA would understand the term "pulse" to have the meaning discussed above. *See* MYM0092358 (IPR2024-00795, Ex. 2011), ¶¶ 47-54.

100. Next, claims 1 and 11 refer not just to a "pulse signal" but a "***pre***-pulse signal." Because it uses "pre-," a POSITA would understand that the claimed "pulse signal" must be applied in advance of some other, subsequent step. This is what "pre-" means. Because the '822 patent is directed to a method specifically intended to be performed during programming (and not some other step such as reading or erasing), a POSITA would understand that the "pre-pulse signals" are applied in advance of programming.

101. The specification further elaborates on what it means by a "pre-pulse signal." In particular, according to the patent, "wordline pre-pulse signals" are applied "[d]uring a pre-charge period (before programming)." '822 patent, 3:43-59.

102. This is also shown in Figure 4. Here, each of the "pre-pulse signal[s]" is applied in a "pre-charge period" that occurs prior to a later programming step when a program voltage Vpgm is applied. *See id.*, Fig. 4.

103. YMTC appears to agree that the claimed "pre-pulse signal" must be applied in advance of programming: its construction specifies that the "signal[] … prepare wordlines for a programming step."

104. Nonetheless, YMTC's proposed construction does not reflect the plain and ordinary meaning of "pre-pulse signal."

105. First, it simply re-uses the word "pulse" rather than articulating the term's plain and ordinary meaning. As I have explained, a "pulse" must have both a defined beginning and end. It is not apparent from YMTC's construction that it is interpreting the term "pulse" in this way. Moreover, by simply reusing the words of the claim in its construction, YMTC has not clarified the claim term's meaning.

106. Second, YMTC's construction appears to graft a requirement onto the claims that the signal "prepare wordlines for programming." Neither the claims nor the specification uses the

word "prepare." Thus, rather than clarifying the meaning of the claims, YMTC's construction makes them more ambiguous. Further, in my opinion, the claim term "wordline pre-pulse signal" simply specifies the nature of the signal applied (a "pulse") and its general timing (it is "pre" or before other subsequent steps). This limitation does not, however, impose any requirements on the purpose of the signal. That comes later in the claim, which specifies that the signals be applied "during a pre-charge period."

IX. THE '903 PATENT

A. The '903 Patent's Effective Filing Date

107. For purposes of this declaration, I have been instructed to use June 28, 2010, as the effective filing date of the '903 patent. With respect to the '903 patent, my opinions in this declaration were formed from the perspective of a person of ordinary skill in the art as of June 28, 2010, including both the knowledge of a person or ordinary skill in the art at that time as well as how a person of ordinary skill in the art would have understood the '903 patent.

B. Overview of the '903 Patent

108. The '903 patent is titled "Three Dimensional Memory and Method of Forming the Same." '903 patent, Cover. Three-dimensional memories work in relevant parts as follows. Memory cell strings are formed vertically within a volume of material and control gates are formed horizontally in that volume to form an intersecting three-dimensional matrix of memory cells and control gates as illustrated below:

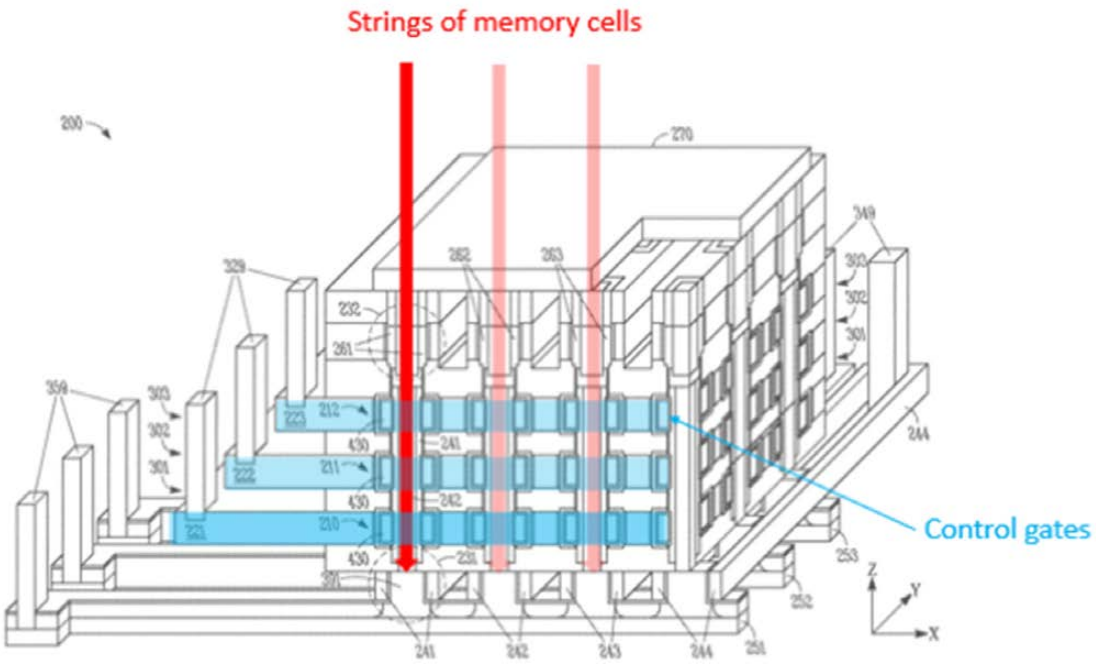


FIG. 3

'903 patent, Fig. 3 (annotated), 1:65-3:25; *see also*, ¶ 42, above, (illustrating a possible electrical circuit equivalent of Fig. 3). Three-dimensional flash memories save information as an amount of charge, and these charges are stored in the memory cells of the memory cell strings. *See* '903 patent, 5:4-19. To store charge in a particular memory cell, a high positive voltage is applied to a control gate which pulls electrons into the memory cell (specifically into its floating gate or charge trap) from a channel of electrons that flows vertically through the memory along the string of memory cells. *See id.* Thus, it is necessary to form the memory cells surrounded by the control gates such that there is a physical proximity that allows a high positive voltage applied to the control gate to pull electrons from the electron channel into the memory cell (specifically into its floating gate or charge trap). *See id.*, 5:4-19, 8:51-59.

109. Figure 3 of the '903 patent depicts one embodiment of the three-dimensional memory structure in which the control gates may have horizontally and vertically extending cavities in which the individual memory cells are located:

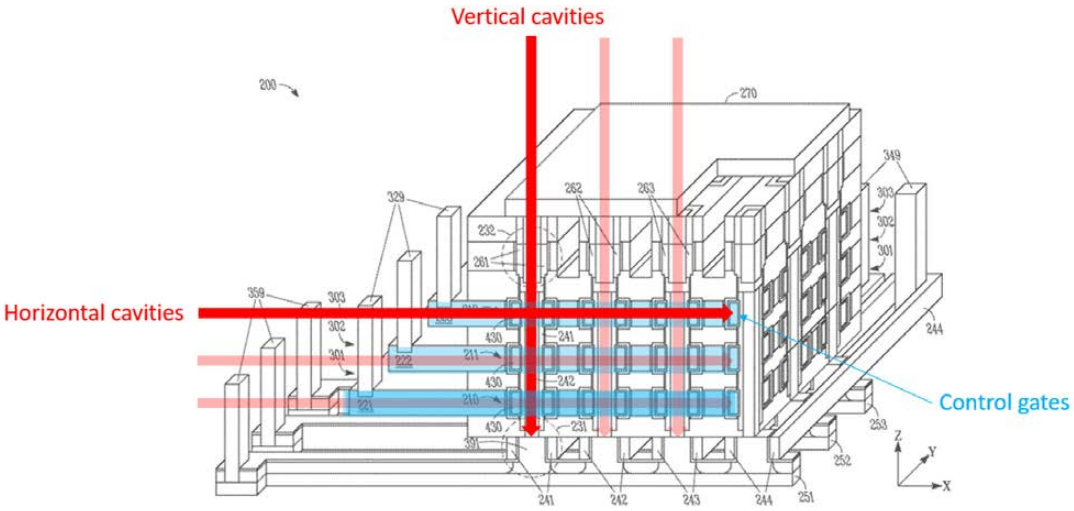


FIG. 3

Id., Fig. 3 (annotated). Figure 11 of the '903 patent illustrates the formation of vertical cavities (or holes) of the same diameter through each layer of material used to form control gate layers (1002, 1004, 1006) and insulating layers (1003, 1005, 1007):

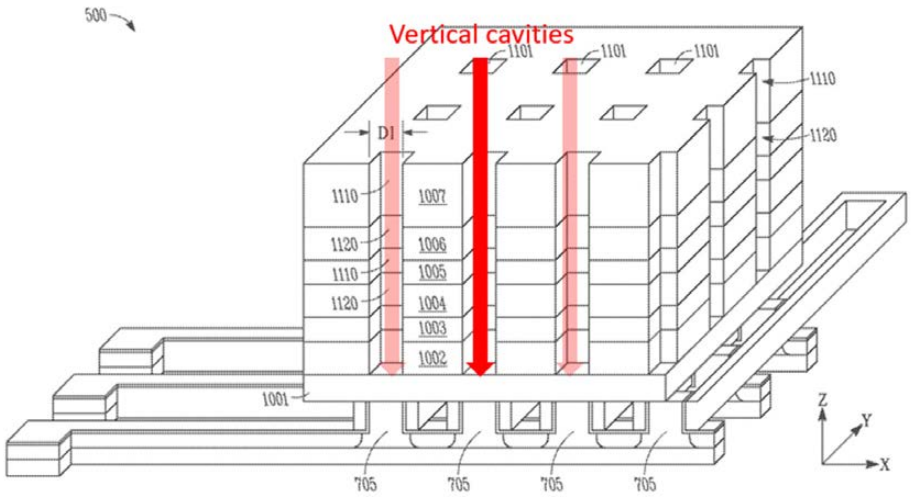


FIG. 11

Id., Fig. 11 (annotated). The specification of the '903 patent states that "forming holes [] results in forming cavities[]." '903 patent, 7:27-46. In the embodiment of Fig. 11, the specification describes that holes are formed through each of the layers 1002 to 1007 to form cavities therein. *Id.* The specification further describes that when forming a hole in the layers of material, the hole formed

in each layer is its own cavity: "Each cavity 1110 and each cavity 1120 may have substantially the same diameter, D1. Diameter D1 can also be considered the diameter of each hole 1101 at the location of each cavity 1110 and each cavity 1120." *Id.*, 7:42-46; *see also id.*, 12:52-64.

110. The specification separately provides that in an optional embodiment, the diameter of some of the vertical cavities can be expanded to form horizontal cavities:

> Forming cavities 1220 can include enlarging the size of cavities 1120 (FIG. 11) while keeping the size of cavities 1110 substantially unchanged (e.g., remaining substantially at diameter D1). For example, enlarging the size of cavities 1120 (FIG. 11) can include selectively removing (e.g., selective wet or dry etching) a portion of each of materials 1002, 1004, and 1006 at each cavity 1120 (FIG. 11) such that the diameter of each cavity 1220 increases to substantially diameter D2, while the diameter D1 at each cavity 1110 remains substantially unchanged.

Id., 7:49-59.

111. Figure 28 illustrates control gates 1221, 1222, 1223, formed from materials 1002, 1004, 1006, discussed in the context of Fig. 11, in which enlarged cavities were formed between alternating layers of materials according to the optional embodiment discussed above:

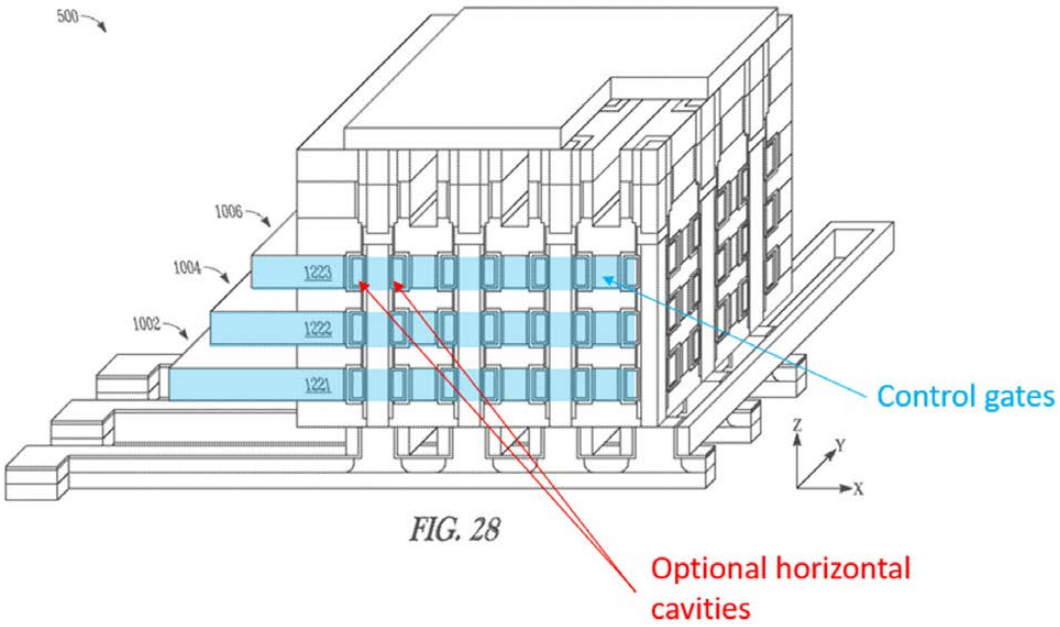


FIG. 28

Id., Fig. 28 (annotated). *See also id.*, 10:19-35.

C. The Prosecution History of the ’903 Patent

112. I have reviewed the prosecution history of the ’903 patent. During prosecution the ’903 patent was allowed after a double patenting rejection. ’903 Patent File History, 3/19/2020 Office Action; 8/19/2020 Notice of Allowance. Applicant cancelled all original claims and added the claims as issued. *Id.*, 6/19/2020 Applicant Response and Amendment.

D. The Asserted Claims of the ’903 Patent

1[pre] An apparatus comprising:

1[a] conductive pillars extending outward from a substrate;

1[b] memory cell strings, each of the memory cell strings is formed over a respective conductive pillar of the conductive pillars;

1[c] a first control gate formed in a first device level, the memory cell strings including a memory cell string, the memory cell string including a first memory cell having a memory element formed in a cavity of the first control gate;

1[d] a second control gate formed in a second device level, the memory cell string including a second memory cell having a memory element formed in a cavity of the second control gate; and

1[e] a conductive channel extending between the first memory cell and the second memory cell and electrically coupled to a conductive pillar of the conductive pillars.

2[a] The apparatus of claim 1, further comprising: a first conductive region located on a first side of the conductive pillar and separated from the conductive pillar by a first dielectric material; and

2[b] a second conductive region located on a second side opposite from the first side of the conductive pillar and separated from the conductive pillar by a second dielectric material.

3 The apparatus of claim 2, wherein the first conductive region is coupled to the second conductive region.

5 The apparatus of claim 2, wherein each of the first and second conductive regions comprises metal.

7 The apparatus of claim 1, further comprising a data line coupled to the conductive channel, wherein the first and second memory cells are located between the data line and the substrate.

8 The apparatus of claim 1, wherein the memory element comprises polysilicon.

9 The apparatus of claim 1, wherein the memory element comprises a dielectric material.

17[pre] An apparatus comprising:

17[a] a first conductive pillar and a second conductive pillar extending outward from a substrate;

17[b] a third conductive pillar and a fourth conductive pillars extending outward from the substrate;

17[c] a region including a conductive material, the region coupled to the first, second, third, and fourth conductive pillars, the region located between substrate and the first, second, third, and fourth conductive pillars;

17[d] a first memory cell string formed over the first conductive pillar;

17[e] a second memory cell string formed over the second conductive pillar;

17[f] a third memory cell string formed over the third conductive pillar;

17[g] a fourth memory cell string formed over the fourth conductive pillar;

17[h] a first data line coupled to the first and second memory cell strings, the first and second memory cell strings located between the first data line and the substrate;

17[i] a second data line coupled to the third and fourth memory cell strings, the third and fourth memory cell strings located between the second data line and the substrate;

17[j] a first control gate formed in a first device level;

17[k] a second control gate formed in a second device level, wherein,

17[l] the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate;

17[m] the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate;

17[n] the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate; and

17[o] the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.

18 The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells comprises polysilicon.

19 The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells comprises a silicon nitride.

20[a] The apparatus of claim 17, further comprising: a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells;

20[b] a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells;

20[c] a third conductive channel coupled to the third conductive pillar and extending between the fifth and sixth memory cells; and

20[d] a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells.

E. DISPUTED TERMS

113. I have been asked to provide my opinions regarding the parties' proposed constructions for two claim terms of the '903 patent. Those terms are set forth below.

i. "a cavity of the [first/second] control gate" (Claim 1)

Micron's Proposed Construction	YMTC's Proposed Construction
Plain and ordinary meaning	"a hole with a larger diameter than holes in the layers immediately above and below the [first/second] control gate"

114. Claim 1 of the '903 patent recites "a cavity of the first control gate" and "a cavity of the second control gate." A POSITA would understand these phrases to have a plain and ordinary meaning, that is, a hole in a control gate. This is so because "hole" is the plain meaning of "cavity." The American Heritage Dictionary (2009) (MYM0067565-567) (defining cavity as "[a] hollow; a hole"); Merriam-Webster's Collegiate Dictionary (2006) (MYM0067568-570) (defining cavity as "an unfilled space within a mass; *esp* : a hollowed-out space"); Webster's Third New International Dictionary (2002) (MYM0067571-573) (defining cavity as "a space hollowed out").

115. The specification of the '903 patent uses the term cavity consistently with its plain meaning. For example, the specification explains that "forming holes [] results in forming cavities[]." '903 patent, 7:27-46. Indeed, whenever the specification refers to a cavity, it is referring to a hole. *Id.*, 4:53-56 (calling horizontally extending holes 420 cavities); 7:28-46 (referring to vertically extending holes 1110 and 1120 as cavities); 7:64-8:3, 8:27-50 (each referring to hole structures as cavities).

116. YMTC's proposed construction, "a hole with a larger diameter than holes in the layers immediately above and below the [first/second] control gate," attempts to import an optional embodiment into the claims. For example, the specification recites:

> Forming cavities 1220 ***can include*** enlarging the size of cavities 1120 (FIG. 11) while keeping the size of cavities 1110 substantially unchanged (e.g., remaining substantially at diameter D1). For example, enlarging the size of cavities 1120 (FIG. 11) ***can include*** selectively removing (e.g., selective wet or dry etching) a portion of each of materials 1002, 1004, and 1006 at each cavity 1120 (FIG. 11) such that the diameter of each cavity 1220 increases to substantially diameter D2, while the diameter D1 at each cavity 1110 remains substantially unchanged.

Id., 7:49-59 (emphases added). A POSITA would understand this permissive language to allow but not require the creation of holes with different diameters, including enlarged holes in control gate layers. *See* Section IX.B., above. Indeed, had Micron intended to limit the claims to cavities of control gates to cavities that are enlarged relative to layers above and below it would have done so explicitly as it did in related application no. 16/125,242 which claimed: "enlarging a size of each of the initial cavities to form enlarged cavities." MYM0092558 (7/18/2019 Amendment (Claims) in U.S. Pat. App. 16/125,242) at 4153.

117. Accordingly, "a cavity of the first control gate" and "a cavity of the second control gate" should be assigned their plain and ordinary meaning which is "a hole in the first control gate" and "a hole in the second control gate," respectively.

ii. <u>"a [first/second/third/fourth] cavity of the [first/second] control gate" (Claim 17)</u>

Micron's Proposed Construction	YMTC's Proposed Construction
Plain and ordinary meaning	"a [first/second/third/ fourth] hole with a larger diameter than holes in the layers immediately above and below [first/second] the control gate"

118. YMTC's proposed construction of "a [first/second/third/ fourth] hole with a larger diameter than holes in the layers immediately above and below [first/second] the control gate" merely attempts to import the same embodiment of the specification discussed in Section IX.E.i., above, into the context of claim 17. *See also* Section IX.B., above. Nothing about the language of claim 17 indicates to a POSITA that "cavity" should have a different meaning than it does in claim 1.

119. Accordingly, "[a] first cavity of the first control gate", "a first cavity of the second control gate", "a second cavity of the first control gate", "a second cavity of the second control

gate", "a third cavity of the first control gate", "a third cavity of the second control gate", "a fourth cavity of the first control gate", and "a fourth cavity of the second control gate[]" should be assigned their plain and ordinary meaning, which is: "[a] first hole in the first control gate", "a first hole in the second control gate", "a second hole in the first control gate", "a second hole in the second control gate", "a third hole in the first control gate", "a third hole in the second control gate", "a fourth hole in the first control gate", and "a fourth hole in the second control gate[]", respectively.

X. THE '941 PATENT

A. The '941 Patent's Effective Filing Date

120. I understand that the application leading to the '941 patent was filed on September 10, 2021. I further understand that the patent is a division of application No. 16/827,734, filed on March 24, 2020, (which was issued as U.S. Patent No. 11,195,590 ("the '590 patent")) and claims priority to an earlier-filed PCT publication No. PCT/CN2020/074580, filed on February 10, 2020.

121. For purposes of this declaration, I have been instructed to use February 10, 2020, as the priority date of the '941 patent. My opinions in this declaration were formed from the perspective of a POSITA as of February 10, 2020, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the '941 patent.

B. Overview of the '941 Patent[1]

122. The '941 patent is titled "Memory Including a Plurality of Portions and Used for Reducing Program Disturbance and Program Method Thereof." '941 patent, Cover. The U.S. application that resulted in the '941 patent was filed on September 10, 2021, and was based on a PCT application filed February 20, 2020. *Id*.

123. The specification of the '941 patent discusses "[p]rogram disturbance" and "pass voltage disturbance" problems that "lead to a higher failure rate of programming a memory." *Id*.,1:34-38. It is worth noting that pass voltages are applied to the cell memory string during both the programming pulse cycle and the verification pulse cycle of the programming operation.

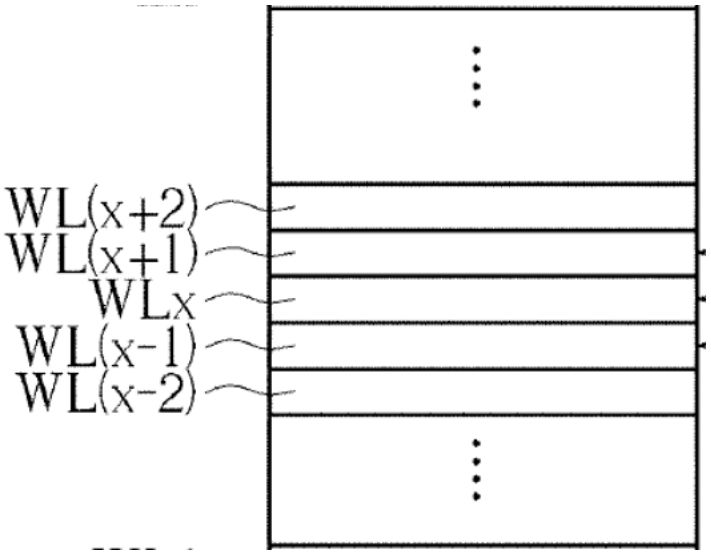
[1] I have reviewed Dr. David Kuan-Yu Liu's declaration in support of Micron's Petition for *Inter Partes* Review of the '941 Patent submitted as Exhibit 1004 to Micron's petition in Case No. IPR2025-00190. Finding his summary accurate to my own review of the '941 patent I am adopting his summary of the '941 patent.

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124. To supposedly try and address these challenges, the '941 specification proposes applying various voltages to particular wordlines when programming the cells in the memory string. *See generally* '941 patent. I note that the '941 specification fails to disclose any actual voltage levels to be applied to the wordlines as part of its alleged solution. *Id*. Even relative voltage levels are only given in rare instances. *See, e.g., id.*, 1:66-67 ("The fifth voltage is lower than the fourth voltage."). There are no voltages identified (even relative voltages) in the specification for the memory cells that are directly adjacent to the cell being programmed. Consistent with this lack of disclosure, the '941 specification mentions that "experiments" and "simulations" were performed, without disclosing what the experiments and simulations were or any results therefrom. *Id*., 6:39-43. More generally, the '941 specification gives no explanation at all of how its programming method(s) allegedly reduce program disturbances and pass voltage disturbances. *See generally* '941 patent.

125. It is helpful to understand how the '941 patent identifies wordlines before discussing the topic of programming voltages. In the '941 patent, the memory cell being programmed is identified by the index "x," and "WLx" refers to the wordline for that cell. *Id*., Abstract, 3:9-11. Other wordlines are identified relative to the location of the memory cell "x." As an example, WL(x+1) and WL(x-1) refer to the wordlines immediately above and below WLx, respectively. *See id*., Figs. 1-5, and 7-11. This pattern continues for other wordlines such as WL(x+2) and WL(x-2), as an excerpt of Figure 1 below shows.

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'941 patent, Fig. 1 (excerpted).

126. The '941 patent uses a different numbering approach to identify what it calls "portions" of a memory string (along with the corresponding wordlines for any cells that are part of that "portion"). The '941 patent identifies a "portion" as a contiguous group of memory cells (and their corresponding wordlines). *See id.*, Figs. 1-11. To show what "portion" a wordline belongs to, the '941 patent uses the variables "k" and "m" (and in some embodiments "n"). *Id*. As with the variable "x," an increment of "+1" identifies the wordline immediately above "k," "m," etc., and a decrement of "-1" to denote the wordline immediately below. *See id.*, Figs. 1-11. As an example, in the excerpted version of Figure 1 below, the "first portion 110" "include[s] a first wordline WL1 to a kth wordline" and "second portion 120" includes "wordline WL(k+1) to an mth wordline WLm." *Id*., 2:63-3:3.

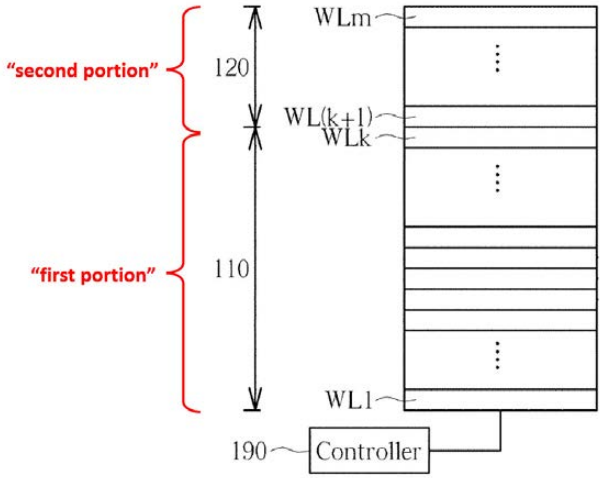


FIG. 1

Id., Fig. 1 (excerpted and annotated).

127. The '941 patent applies both of these numbering schemes to a single memory stack to identify in which "portion" a cell is being programmed. Comparing Figures 1 and 2 below demonstrates this where the wordline of the cell being programmed (WLx) is in the first portion 110 in Figure 1, but in Figure 2 the wordline used for programming "WLx is located in the second portion 120." *Id.*, 3:26-28.

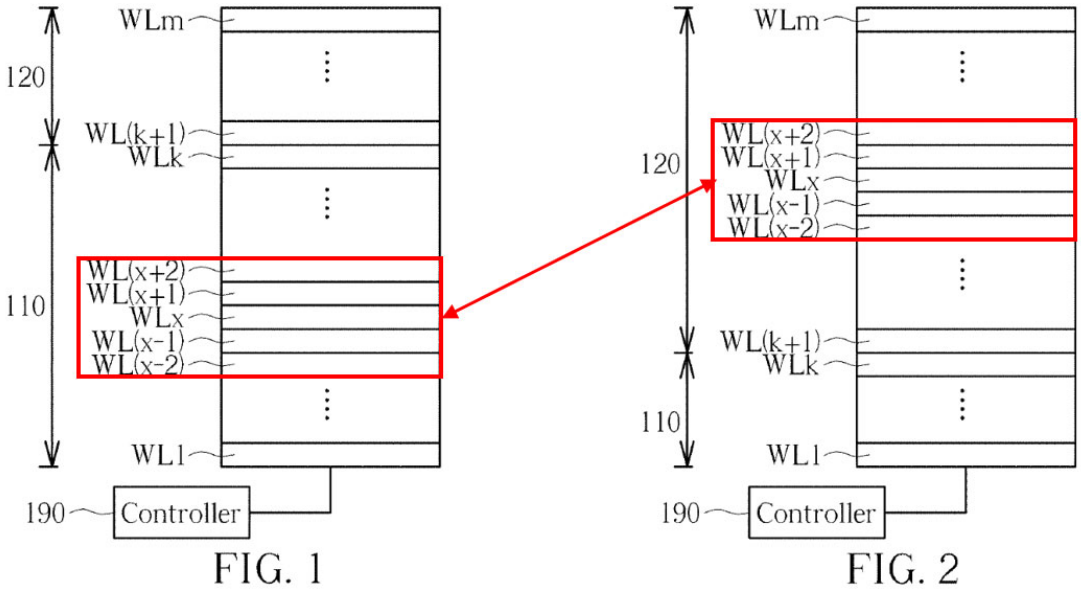


FIG. 1 FIG. 2

Id., Figs. 1 and 2 (excerpted and annotated).

128. Turning now to the programming pulses applied during the program operation, the '941 patent says the voltage "Vpgm" is applied to the wordline for the cell being programmed. *Id.*, 3:9-11 ("When an xth wordline WLx is used to performed a program operation, the controller 190 may apply a program voltage Vpgm to the xth wordline WLx"); Figs. 1-5 and 7-11. The other wordline voltages are all generically referred to as "first voltage V1," "second voltage V2," "third voltage V3," etc. *See, e.g., id.*, 3:11-16. As noted above, the '941 patent fails to disclose any actual values (or even ranges) for these generic voltages. Further, the '941 patent is silent regarding the relationships (*e.g.*, whether the values can be the same, overlap, are mutually exclusive, etc.) between V1, V2, V3, etc. with only very limited exceptions. It is worth reiterating that these are frequently the voltages of the wordlines for the cells that are directly adjacent to the cell being programmed.

129. In some embodiments, a named voltage is applied to a singular wordline, and in other embodiments, the named voltage is applied to multiple wordlines. *See id.*, Fig. 1-5 and 7-11. Figure 1 below is an example where the "first voltage V1" is applied from WL1 to WL(x-2), "second voltage V2" is applied to WL(x-1), Vpgm is applied to WLx, V3 is applied to WL(x+1), and V4 is applied from WL(x+2) to WLm. *Id.*, 3:11-21. Figure 2 is the same, except that WLx is in the second portion 120. *See id.*, 3:28-30, Fig. 2.

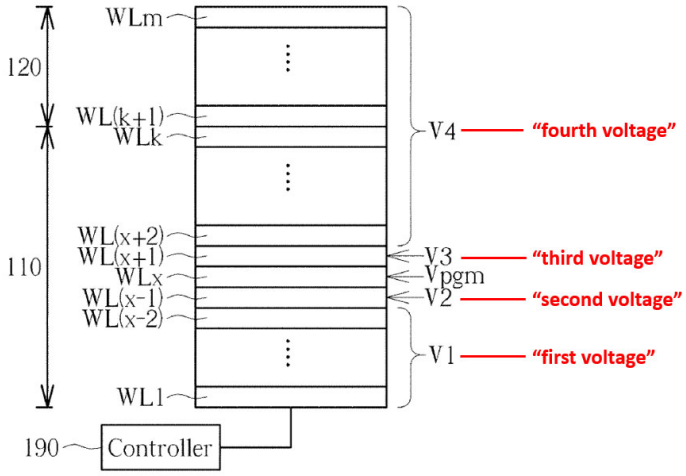


FIG. 1

Id., Figure 1 (annotated).

130. I flag one other example here (Figure 8) to show that the voltage label assignments V1, V2, V3, etc. in the '941 patent are rather arbitrary as they differ significantly from the assignments in Figures 1 and 2. In Figures 7-11, the prefix "7" is appended to the front of the generic voltage names, calling them V71 (first voltage), V72 (second voltage), V73 (third voltage), etc. *Id.*, 4:37-61. Unlike Figure 1, the second voltage in Figure 8 is located ***above*** the cell being programmed and the third voltage is ***below*** the cell being programmed. *Id.*, 4:37-61, Fig. 8.

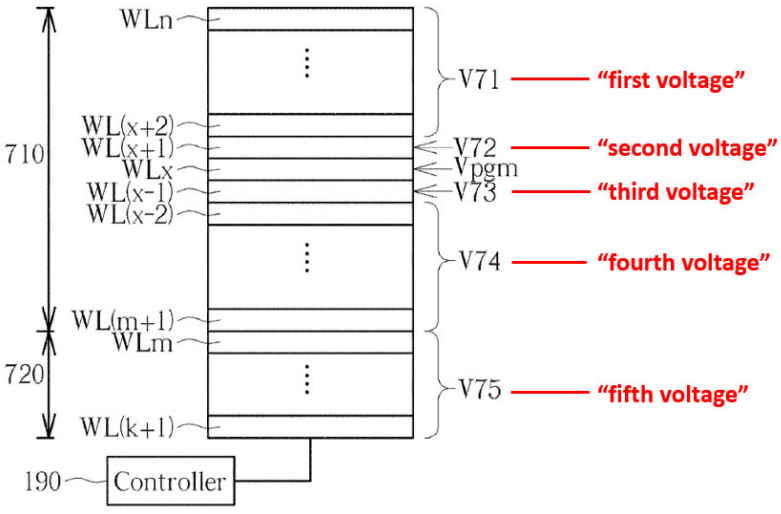


FIG. 8

Id., Fig. 8 (annotated). As I discussed above, only in rare instances are relative voltage levels specified, but Figure 8 is one such example that requires the fifth voltage to be less than the fourth voltage. *Id.*, 4:60-61.

131. The last concept I will discuss is associated with the '941 patent's "first voltage." The '941 patent states that "the first voltage V1 may have a first level if the xth wordline WLx is in the first portion 110 and a second level if the xth wordline WLx is in the second portion 120, where the first level may be lower than the second level. For example, the first voltage V1 in FIG. 1 may have a lower value than the first voltage V1 in FIG. 2." *Id.*, 3:35-41. In other words, as programming advances up a memory string (*e.g.*, from the source end to the drain end), the pass voltage that is applied to the previously programmed cells may increase.

C. The Prosecution History of the ’941 Patent

132. I also reviewed the prosecution history for the ’941 patent. The ’941 patent is a divisional of U.S. Patent No. 11,195,590. ’941 patent, Cover. The file history is rather short, as the claims in the patent were the result of a first-action allowance. *See* ’941 Patent File History, 10/4/2022 Notice of Allowance. I noted that the Examiner’s reasons for allowance in the ’941 patent just recited most of the claim language for each independent claim without identifying any specific point of novelty. *Id.*

D. The Relevant Claims of the ’941 Patent

133. I understand that claims 4 and 10 of the ’941 patent are asserted in this case. Because claim 4 depends on claim 1 and claim 10 depends on claim 5, I also include those claims below as “relevant” claims but understand that they have not been asserted.

1[pre] A memory comprising:

1[a] a first portion comprising an (m+1)th wordline to an nth wordline from bottom to top; and

1[b] a second portion formed below the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top; and

1[c] a controller configured to apply a first voltage to an (x+2)th wordline to the nth wordline, a second voltage to an (x+1)th wordline, a third voltage to an (x−1)th wordline, a fourth voltage to the (m+1)th wordline to an (x−2)th wordline, and a fifth voltage to the (k+1)th wordline to the mth wordline when an xth wordline is used to perform a program operation;

1[d] wherein x, k and m are integers, $0 \leqslant k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

4[pre] The memory of claim 1, further comprising:

4[a] an upper dummy wordline formed below the first portion;

4[b] a lower dummy wordline formed above the second portion; and

4[c] a joint oxide layer formed between the upper dummy wordline and the lower dummy wordline;

4[d] wherein the memory has a two-deck structure.

5[pre] A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first wordline to a kth wordline from bottom to top, the second portion formed above the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top, the program method comprising:

5[a] applying a first voltage to the to the first wordline to an (x−2)th wordline when an xth wordline is used to perform a program operation;

5[b] applying a second voltage to an (x−1)th wordline; and

5[c] applying a third voltage to an (x+1)th wordline;

5[d] wherein x, k and m are positive integers, $1<k<m$ and $3 \leqslant x$.

10[pre] The program method of claim 5, wherein the memory further comprises:

10[a] a lower dummy wordline formed above the first portion;

10[b] an upper dummy wordline formed below the second portion;

10[c] a joint oxide layer formed between the lower dummy wordline and the upper dummy wordline;

10[d] wherein the memory has a two-deck structure.

E. DISPUTED TERMS

134. I have been asked to provide my opinions regarding the parties' proposed constructions for one claim term of the '941 patent. That term is set forth below.

i. "from bottom to top" (Claims 1, 5)

Micron's Proposed Construction	YMTC's Proposed Construction
Plain and ordinary meaning	Plain and ordinary meaning, *i.e.*, from lowest to highest

135. Both Micron and YMTC propose that this term be given its plain and ordinary meaning, but YMTC proposes that the plain and ordinary meaning is "from lowest to highest." As I discuss below, YMTC's proposed plain and ordinary meaning does not provide meaningful

guidance in the application of the claim terms because it is ambiguous, and it is not how a POSITA would have understood the term.

136. It is not clear what YMTC means by "lowest" or "highest." For example, it's possible that YMTC is referring to spatial locations (*i.e.*, the lowest may be the lowest point on a vertical or z-axis), but it is also possible that YMTC is referring to the ordinal location (*i.e.*, in a span of elements (*e.g.*, wordlines) 1 through 10, 1 would be the "lowest" and 10 would be the "highest"). Even with respect to a spatial location such as the z-axis, YMTC's proposed construction is ambiguous because if it were adopted it would not provide clear guidance as to what wordline is meant by "bottom" ("lowest") or "top" ("highest"). Specifically, YMTC's construction would depend on the orientation of a memory chip (*e.g.*, it could be rotated or flipped, resulting in multiple different "bottom" or "top" reference points). Instead of this, a POSITA would have understood "from bottom to top" to have the meaning I discuss below, which clearly indicates what wordline is the "bottom" and what wordline is the "top" in the context of the claims.

137. As an initial matter, the claims 1 and 5 of the '941 patent (where the phrase "bottom to top" first appears) are not limited to 3D NAND. Specifically, the claims simply recite "[a] memory" (claims 1) and "[a] program method of a memory" (claims 5). They do not recite 2D or 3D memory, and would not be limited to a particular memory architecture. Indeed, the specification only mentions such details in the "Description of the Prior Art" in which it referenced the development of "three-dimensional stack NAND" which was developed to "increase the capacity of [] memory." '941 patent, 1:24-41. And the Field of Invention states: "The disclosure is related to a memory and a program method, and more particularly, a memory including a plurality of portions and used for reducing program disturbance and a program method thereof." And the Title is: "MEMORY INCLUDING A PLURALITY OF PORTIONS AND USED FOR REDUCING PROGRAM DISTURBANCE AND PROGRAM METHOD THEREOF." Thus, a POSITA would not have understood that the patentee was limiting the claim scope to 3D memory.

138. Because of this, I address how this term would have been understood in both the 2D and 3D memory context. As described below, the plain and ordinary meaning of "from bottom to top" is readily apparent in both contexts.

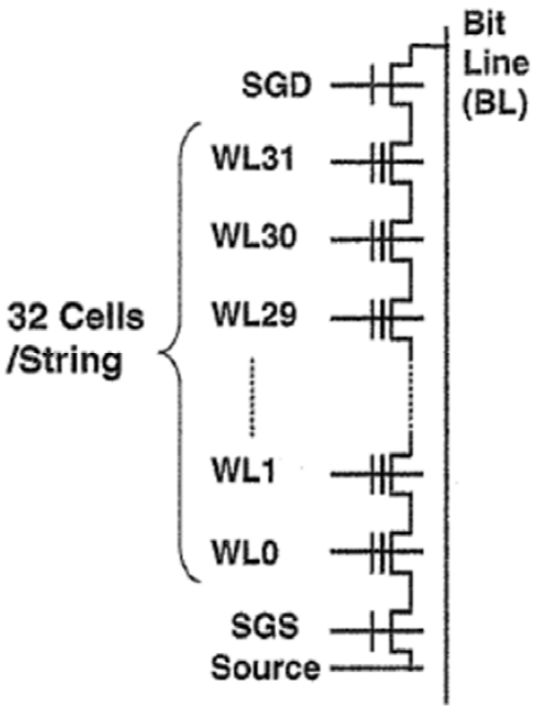
139. As described below, it would have been readily apparent to a POSITA what the "bottom" and "top" sides of a NAND memory string refer to. Going back many years, for both 2-D and 3-D NAND memory, the "source" and "drain" ends of a memory string were commonly referred to in the art as the "bottom" and "top," respectively. This is true regardless of the orientation of the memory chip and applies equally to both 2-D and 3-D memory. Indeed, even in terms of memory arrays generally a POSITA would have known that the terms "top" and "bottom" were used to indicate the position of wordlines. *See, e.g.*, MYM0094308 (U.S. Patent No. 6,961,805 to Lakhani), 1:50-54.

140. Thus, it is my opinion that a POSITA would have understood the plain and ordinary meaning of "from bottom to top" to mean from the source side (the bottom in the '941 patent's illustrations) to the drain side (the top in the '941 patent's illustrations). I should explain that when I say "source side" I mean to say that "bottom" refers to the side that is *closest* to the source side, not that "bottom" has to be *at* the source side. Similarly, "top" refers to the side that is *closest* to the drain, not that the "top" has to be *at* the drain. This understanding is consistent with the wealth of extrinsic evidence, including other YMTC patent applications (discussed below) involving the same inventors listed as named inventors of the '941 patent.

141. After examining the intrinsic evidence (including the '941 patent's claims, specification, and file history), it is clear that the '941 patent does not contain helpful information in defining the "bottom" or "top" from a structural perspective. That is, the '941 patent itself does not provide disclosures that help the reader understand where in a NAND memory device (whether 2D or 3D) is the "bottom" or "top" as recited in the claims. Nor does the '941 patent provide any information which suggests a definition of the term different from how a POSITA would have understood how it is used in the context of the claims, and in the industry generally. For example, I note that there is no figure in the '941 patent showing a complete structural diagram of a NAND memory device, nor is there a discussion of other structural elements of a NAND memory device which otherwise might have helped the reader understand to what in the NAND memory device "bottom" and "top" may refer. *See generally* '941 patent; '941 Patent File History. Rather, the figures are all illustrative of the wordlines in a memory for purposes of explaining the grouping of

the wordlines and the relative voltages applied to those wordlines. '941 patent, Figs. 1-11. Thus, it is useful to examine the types of literature and other resources which will show what a POSITA would have understood "bottom" and "top" to mean in the context of the claims (*i.e.*, in relation to the wordlines and memory strings in a NAND memory device). Indeed, the fact that the '941 patent's first portion can be below and above the second portion (compare Fig. 1 with Fig. 7) demonstrates that there is no unique positional relationship between the portions.

142. In the 2-D context, a POSITA would have understood that the "bottom" typically refers to the wordline closest to the *source* side of the string while the "top" typically refers to the wordline closest to the *drain* side of the string. This is supported by the wealth of NAND literature, some of which I discussed in Section VII. For example, the Aritome textbook referred to in that section shows a string of cells with wordlines where the bottom of the string (where the bottom wordline is "WL0") is nearest to the source and the top of the string (where the top wordline is "WL31") is at the drain:



Aritome, MYM0027842; *see also id.*, MYM0027843. The acronyms SGS and SGD were well-known to POSITAs and refer to Select Gate Source (SGS) and Select Gate Drain (SGD). Naturally, the "bottom" wordline nearest the source is WL0 and the "top" wordline nearest the drain is WL31.

143. Other textbooks discussing 2D NAND strings depict the same arrangement. Below is another NAND string where the "bottom" wordline nearest the source is WL<0> and the "top" wordline nearest the drain is WL<63>. In the image below "DSL" refers to Drain Selection Line and "SSL" refers to Source Selection Line. *See* MYM0033558 ("Micheloni Inside NAND") at 3588, 3985, 4110.

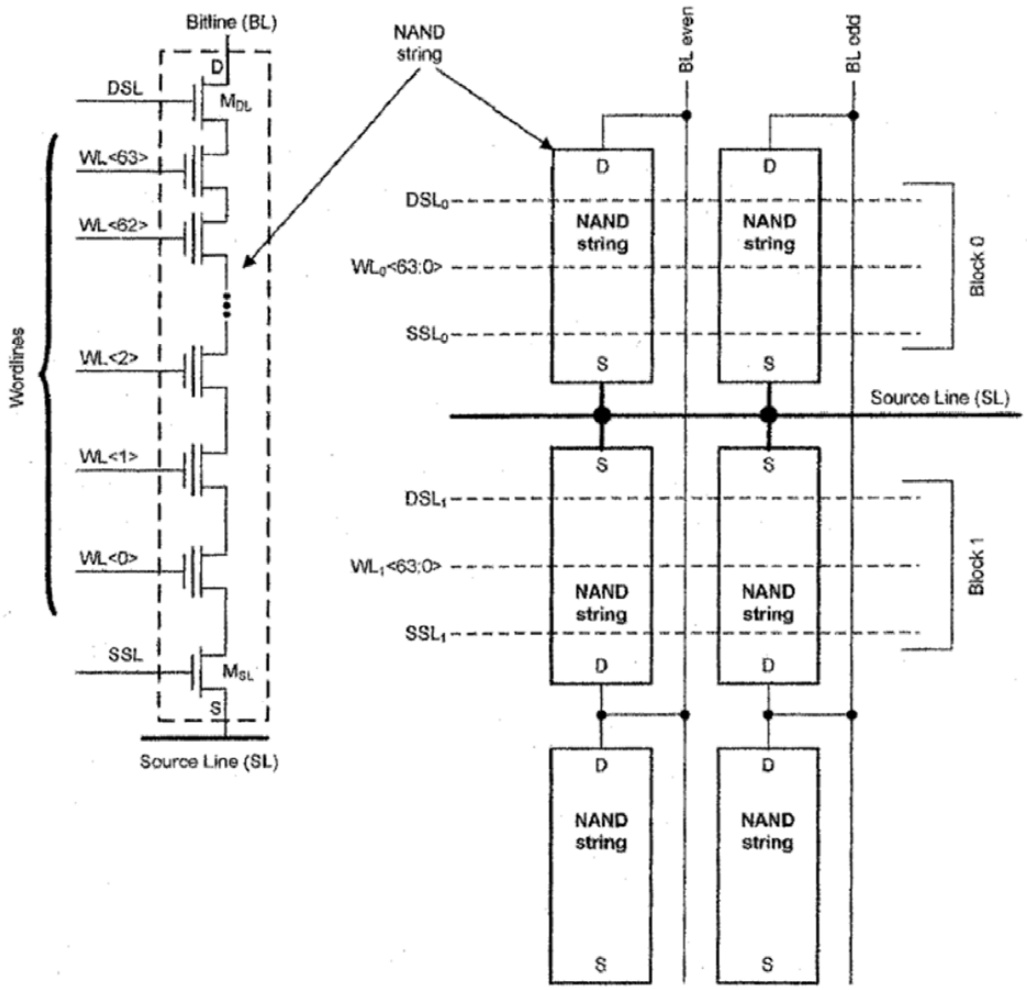


Fig. 2.2. NAND string (left) and NAND array (right)

Id., MYM0033588.

144. Consistent with the textbooks cited above, patents filed by developers of NAND memory show that the "bottom" of a 2D NAND string refers to the "source" side of the string and the "top" refers to the other, or "drain," side of the string. For example, U.S. Patent No. 7,672,165 to Pham et al. ("Pham") is a patent directed to "[a] NAND flash memory device" and depicts 2D

NAND strings. MYM0094334, Abstract, Fig. 2A, 3A. Pham states that "NAND arrays are well known in the art and are widely utilized in various consumer devices." *Id.*, 1:38-2:9.

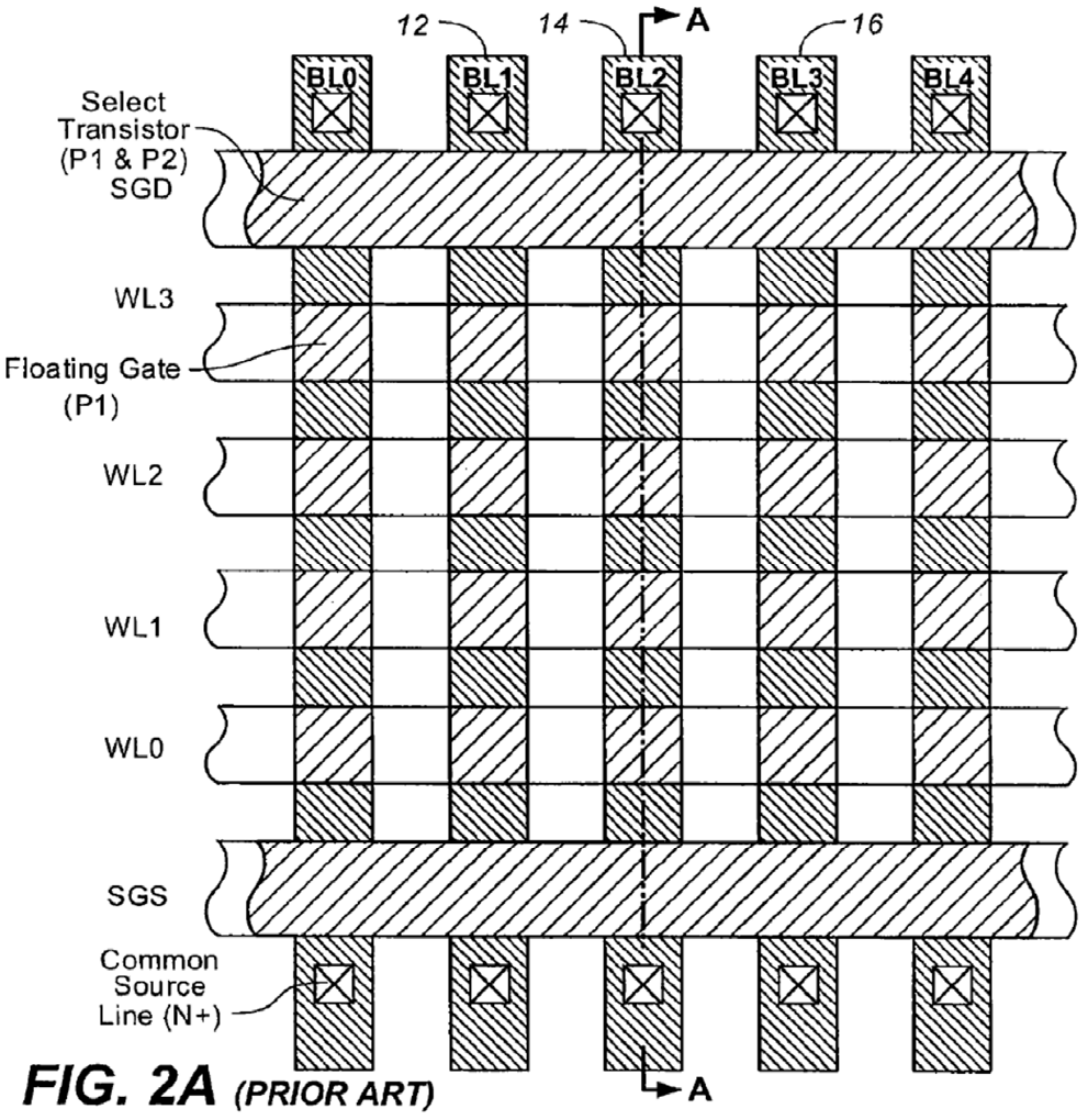


FIG. 2A ***(PRIOR ART)***

Id., Fig. 2A. Pham states that "top and bottom of the string connect to the bit line and a common source line respectively." *Id.*, 1:59-63 (emphasis added). Furthermore, Figure 2A again uses the common acronyms "SGS" and "SGD" which a POSITA would have understood refers to Select Gate **Source** (SG**S**) and Select Gate **Drain** (SG**D**).

145. Similarly, U.S. Patent No. 9,230,658 to Han ("Han") uses the term "top" and "bottom" in relation to NAND string wordlines, where wordlines near the "bottom" are those closer to the source and wordlines near the "top" are those closer to the drain. Han states that "data is

written on a memory block in a bottom-up fashion, starting from memory cells on or near the lowermost (or bottom) wordline. Then data is sequentially written page-by-page on memory cells on wordlines above the lowermost wordline until memory cells on the uppermost (or top) wordline are filled up." MYM0094350, 3:25-33.

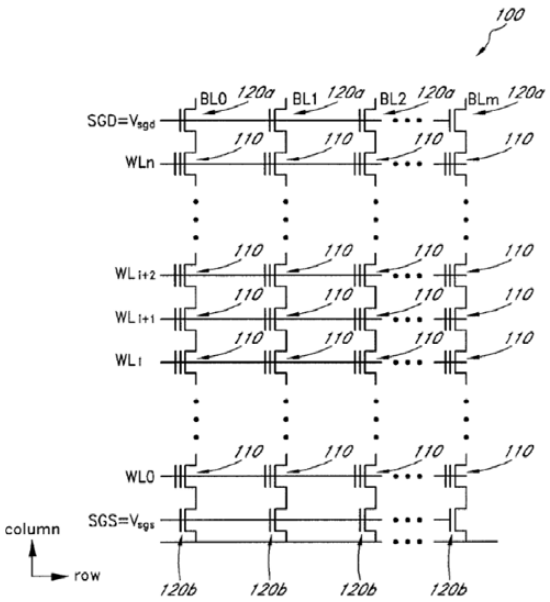


FIG. 2A
(PRIOR ART)

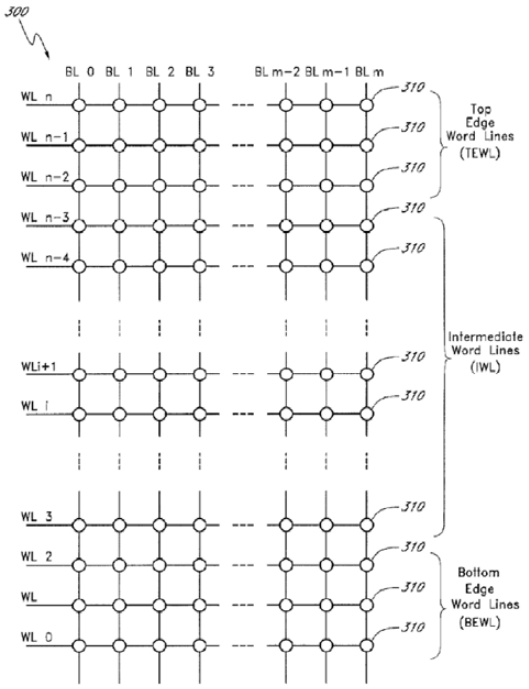


FIG.3

Id., Figs. 2A, 3. Viewing Figures 2A and 3 side by side reveals that what Han refers to as the "bottom" (at WL0) is the side of the string closest to SGS, which a POSITA would have understood to be the Select Gate **Source**. What Han refers to as the "top" (at WLn) is the side of the string closest to SGD, which a POSITA would have understood to be the Select Gate **Drain**.

146. Thus, in the 2D memory context, a POSITA would have understood that the meaning of "from bottom to top" to mean from the source side to the drain side.

147. In the 3D memory context, this same plain and ordinary meaning applies. For example, literature such as Micheloni 3D Flash likewise uses the same "bottom" and "top" terminology with reference to the source and drain ends, respectively:

Fig. 5.30 Bird's-eye view and side views of the DC-SF NAND Flash string

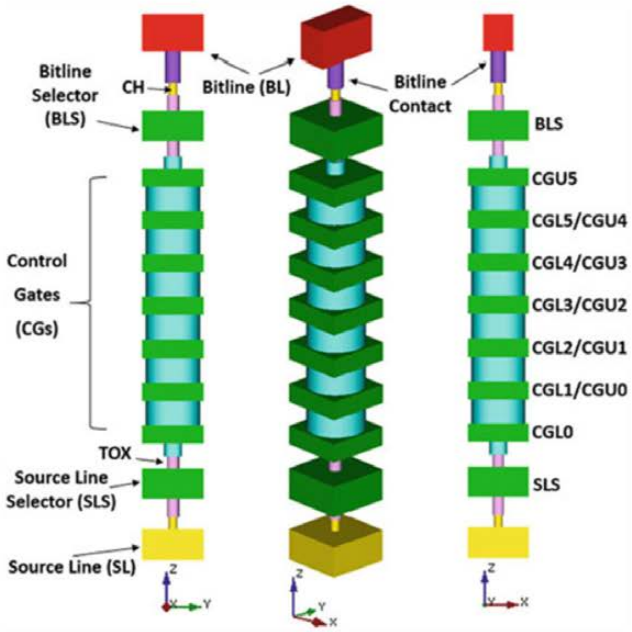
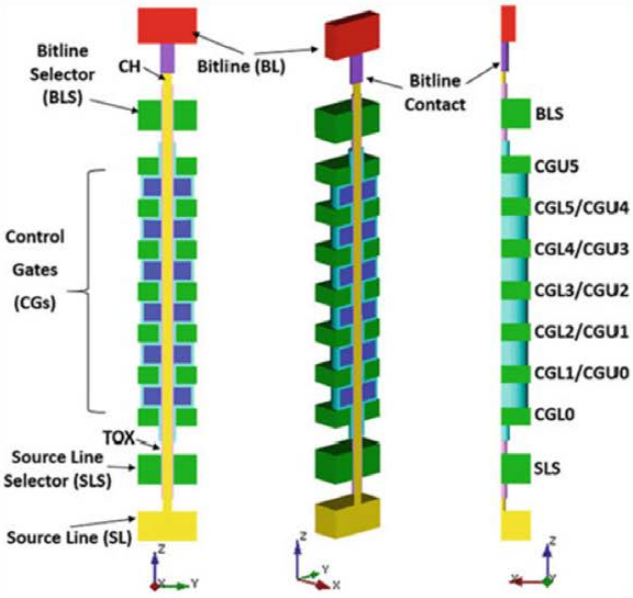


Fig. 5.31 Cross sections of Fig. 5.30

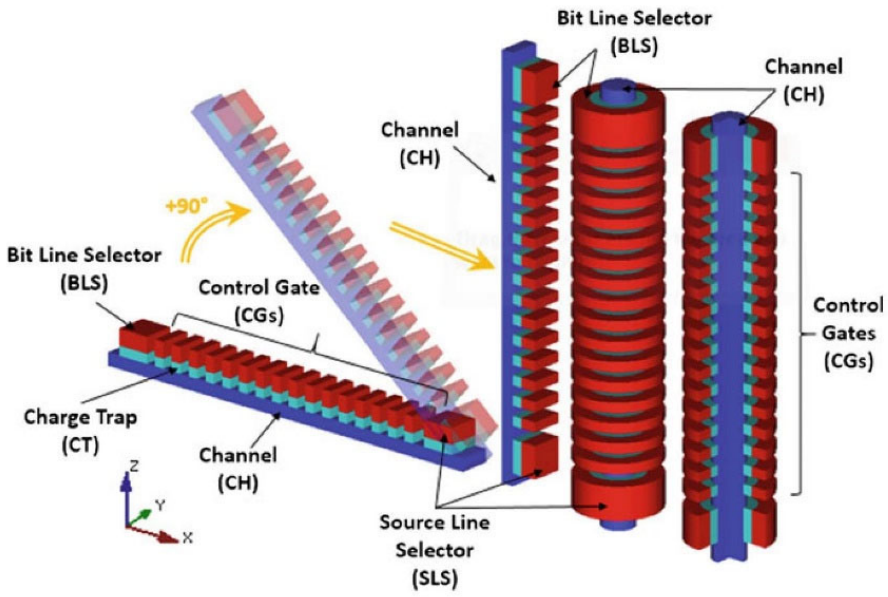


Micheloni 3D Flash, MYM0033330. Figures 5.30 and 5.31 both show a NAND memory string where the bottom of the string is closest to the Source. *See also id.*, MYM0033326, 33331, 33334.

148. Numerous other references confirm the same common usage for both 2-D and 3-D memory. For example, U.S. Patent No. 9,613,704 ("the '704 patent") is titled "2D/3D NAND memory array with bit-line hierarchical structure for multi-page concurrent SLC/MLC program and program-verify," and expressly applies to both 2D and 3D NAND memory. MYM0094365,

6:65-7:2 ("the terms of '2D' or '3D' NAND flash means any part or whole of either NMOS or PMOS NAND cell device, component, die or chip made of any varied kinds of two-dimension or three-dimension manufacturing process"). The '704 patent explains that "each conventional NAND String is made of M NAND cells that are connected in series." *Id.*, 1:40-41. The '704 patent states that "each String comprising M cells connected in series and capped by a top String-select transistor and a bottom String-select transistor, the top String-select transistor connecting its drain to one corresponding [bit line], the bottom String-select transistor connecting its source to a common source line." *Id.*, 121:41-46. Even though the '704 patent provided more flexibility regarding the order in which memory cells could be programmed and erased, it did not change the "conventional" terminology of programming from "bottom of a NAND String to top of NAND String," which it consistently describes as source-to-drain. *Id.*, 10:23-26.

149. Other extrinsic evidence supports the common and consistent usage of the bottom (source) and top (drain) terminology across both 2-D and 3-D memory. In fact, much of the terminology for 3-D NAND derives directly from 2-D NAND, including the term "memory string" with its concomitant source/drain ends. As explained in Section VII, one way of conceptualizing the move from 2D NAND to 3D NAND is tilting a 2-D memory string on its end to orient the string vertically rather than horizontally. This is shown again with reference to a figure from the Micheloni Inside SSDs textbook, where the source line selector is at the bottom of the NAND memory string.



MYM0034141 ("Micheloni Inside SSDs") at 262.

150. Furthermore, the POSITA's understanding of bottom/top as source/drain ends is supported by other patent applications filed by YMTC with some of the same named inventors as those listed as named inventors of the '941 patent. For example, U.S. Patent Application No. 2021/0158880 lists XiangNan Zhao and Yali Song as inventors. MYM0091776 ("the '880 patent publication"). These two individuals are two of the three named inventors listed on the cover of the '941 patent. '941 patent, Cover Page. The '880 patent publication is "related to a method of programming and verifying a memory device and related memory device." The '880 patent publication, [0002].

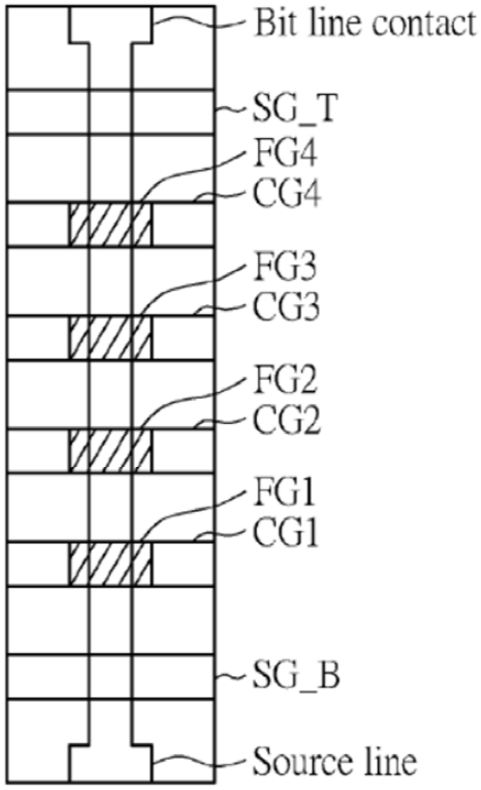


FIG. 1

'880 patent publication, Fig. 1. In conjunction with the above "diagram illustrating a NAND string" the '880 patent publication states that there is a "top select gate SG_T (on the drain side) and a bottom select gate SG_B (on the source side)." *Id.*, [0018]; *see also id.*, [0020]-[0021]. This confirms that a POSITA would have understood that in the context of a NAND memory string in general (e.g., whether a 2D or 3D memory structure), the "top" refers to the drain side and the "bottom" refers to the source side.

151. The extrinsic evidence textbooks consistently identify the source side of the NAND memory string as being the bottom. For example, Micheloni 3D Flash states "[t]he bottom of the memory string is connected to the common source diffusion, which is formed on the silicon substrate." Micheloni 3D Flash, MYM0033268-269.

152. Aritome states that "[t]he bottom of memory string is connected to the common source diffusion formed on the silicon substrate." Aritome, MYM0028100. Aritome provides a depiction of the structure showing this:

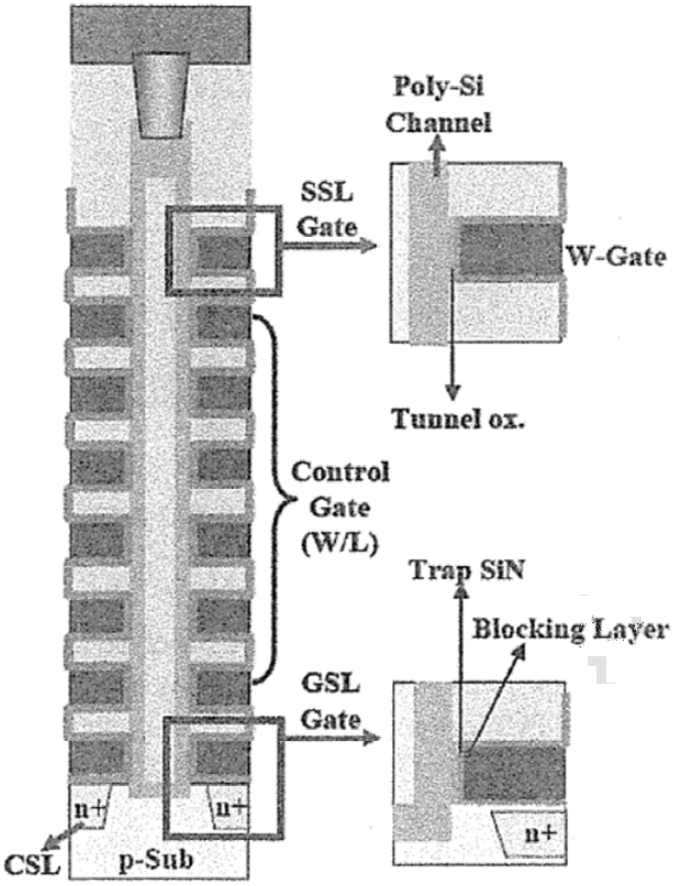


FIGURE 7.27 Schematic structures of TCAT flash cell string. Details of selection transistors are shown.

Id., MYM0028112. This figure shows that the "bottom of memory string is connected to the common source line (CSL) diffusion." *Id.*

153. Next, the text Vertical 3D Memory Technologies by Betty Prince states—in a section on Vertical NAND Flash—"The bottom of [a NAND string pillar] is connected to the common source diffusion." MYM0091817 ("Prince") at 949, 957; *see also id.*, MYM0091972-73.

154. Another problem with YMTC's proposed construction is that it is non-sensical in the context of 3-D NAND memory that employs a "U-shaped" memory string architecture as shown, for example, in Fig. 1D of U.S. Patent No. 9,530,492 ("the '492 patent") (MYM0038652-

728), reproduced below. '492 patent, 12:46-48 ("[Fig. 1D is] a cross-sectional view of a memory unit device configuration of a conventional U-shape vertical-channel 3D memory String that comprises eight 3D NAND cells."). YMTC's notion of "lowest to highest" does not make sense here because there are multiple cells in the same memory string at the same vertical z-axis dimension. But the '492 patent does disclose a "drain-string-select transistor 81 and one source-string-select transistor 82 respectively coupled at two ends," which provide the requisite reference points. *Id*., 20:8-11.

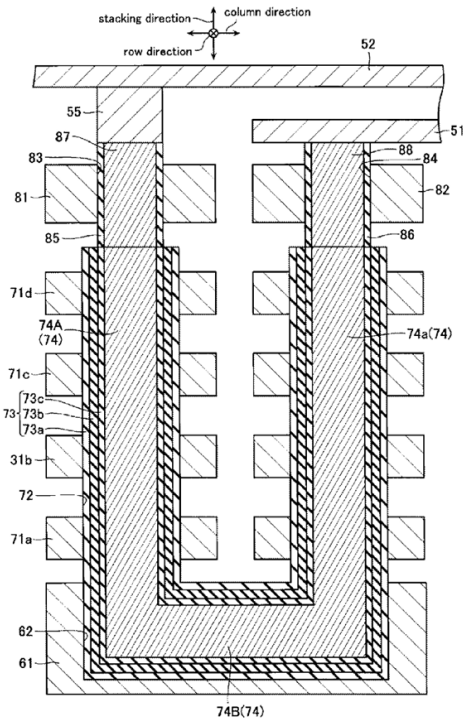


FIG.1D (Prior Art)

155. Yet another problem with YMTC's proposed construction is that it ignores various types of 3D NAND memory, such as are described in U.S. Patent No. 10,235,294 ("the '294 patent") (MYM0094237-272), which discloses that "a 3D memory structure may be vertically arranged as a stack of multiple 2D memory device levels" ('294 patent, 8:62-64) and that "in a 3D NAND memory array, the memory elements may be coupled together to form a NAND string within a single horizontal (e.g., x-y) memory device level" (*id*., 9:7-10). Again, in this circumstance, YMTC's proposal makes no sense, but a POSITA's understanding of source/drain

as the bottom/top of a memory string does make sense. YMTC's apparent focus on physical positional relationships (bottom, top, lowest, and highest) is in conflict with the positional relationships of, for example, 2-D NAND technology where YMTC's bottom and top are at the same physical level (at the surface of the substrate). I further note that the '294 patent states "[t]he bottom (or source end) of each NAND string is in contact with the well region, and the top end (or drain end) of each NAND string is connected to a respective bit line," confirming this typical usage. *Id*., 12:53-56. Moreover, in the '294 patent, "[t]he memory structure can be 2D or 3D." *Id*., 6:14.

156. I understand that YMTC cites to the Merriam Webster Dictionary (2016) (YMTC-MICRON-PA_0010352) in support of its proposed construction. However, the definition it provides is not in the context of NAND memory and does not reflect the plain and ordinary meaning as would be understood by a POSITA as I discuss in this section. That is, this dictionary defines "top" as "the highest part, point, or level of something" and "the upper end, edge, or surface." *Id.*, YMTC-MICRON-PA_0010356. It defines "bottom" as, *e.g.*, "the lowest part or place." *Id.*, YMTC-MICRON-PA_0010355. While it may sometimes be the case that the "top" wordline is physically near the "highest part, point, or level" of a NAND chip along a z-axis (*i.e.*, if that is where the drain is located), that is not in any way definitional of "bottom to top" as used in the '941 context of a NAND memory string or wordline. The same is true for YMTC's general purpose dictionary definition of "bottom." It may sometimes be the case that the "bottom" wordline is near the physical bottom of a chip along a z-axis (*i.e.*, if that is where the source is located), but that is merely coincidental, not definitional. And YMTC's dictionary definition makes no sense in the context of planar 2-D NAND or various 3-D NAND architectures (like the U-shaped memory string) already discussed. Thus, to the extent YMTC's construction is using "lowest" and "highest" to define the physical positional coordinates (such as along a z-axis) of the wordlines in a NAND memory, YMTC is incorrect because that is not how a POSITA would have understood the term in the NAND memory context.

157. The various textbooks and the exemplary YMTC patent publication discussed above convey a consistent understanding. That is, when one talks about the "bottom" of a NAND memory string (or the wordlines) without any further contextualization or redefinition of that term "bottom",

a POSITA would have understood that to be the *source* side in the context of both 2D and 3D NAND memories. Likewise, without any further contextualization or redefinition, a POSITA would have understood the term "top" to mean the *drain* side in the context of both 2D and 3D NAND memories. Therefore, the plain and ordinary meaning of "from bottom to top" as understood by a POSITA would have been "from the source to the drain side."

Executed on the 31st day of January, 2025, in Troy, New York.

I declare under penalty of perjury that the foregoing is true and correct.



E. Fred Schubert, Ph.D.

CERTIFICATE OF SERVICE

I am employed in the County of San Mateo, State of California. I am over the age of 18 years old and not a party to this action. My business address is Orrick, Herrington & Sutcliffe LLP, 1000 Marsh Road, Menlo Park, California 94025-1015. On January 31, 2025, I served the **DECLARATION OF E. FRED SCHUBERT, PH.D. IN SUPPORT OF DEFENDANT'S PATENT RULE 4-3 DISCLOSURE** on all interested parties to this action in the manner described as follows:

☐ **(VIA U.S. MAIL)** On January 31, 2025, by placing a true copy of the document(s) listed above in an envelope, with postage thereon fully prepaid, addressed as set forth below and then sealing the envelope and depositing it in the U.S. mail at Menlo Park, California.

☒ **(VIA EMAIL)** On January 31, 2025, via electronic mail in Adobe PDF format the document(s) listed above to the electronic address(es) set forth below.

☐ **(VIA OVERNIGHT-FED EX)** I caused the within document(s) to be delivered by overnight courier to the address(es) set forth below.

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Counsel for Plaintiff and Counterclaim Defendants, Yangtze Memory Technologies Company, Ltd. and Yangtze Memory Technologies Company, Inc.

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I declare under penalty of perjury under the laws of the State of California and the United States that the foregoing is true and correct.

Executed on January 31, 2025, at Menlo Park, California.

/s/ Matthew Bonini
Matthew Bonini

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EXHIBIT A

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Citizenship

Born in Stuttgart, Germany (1956)
Naturalized United States Citizen (1995)

Education

University of Stuttgart	Electrical Engineering	Vordiplom	(U. S. equivalent BSEE)	1978
University of Stuttgart	Electrical Engineering	Diplom Ingenieur (Honors)	(U. S. equivalent MSEE)	1981
Oregon State University	Electrical Engineering	Exchange Student		1977–1978
University of Stuttgart	Electrical Engineering	Doktor Ingenieur (Honors)	(U. S. equivalent Ph.D.)	1986

Current appointment

2002 – present: Professor, Department of Electrical, Computer, and Systems Engineering; Rensselaer Polytechnic Institute, Troy NY

Previous appointments

2002 – 2015: Head and Founder of the Future Chips Constellation; Rensselaer Polytechnic Institute
2002 – 2015: Wellfleet Senior Constellation Professor, Future Chips (Chaired Professor); Rensselaer Polytechnic Institute
2002 – 2012: Professor Department of Physics, Applied Physics, and Astronomy; Rensselaer Polytechnic Institute
2008 – 2009: Director, Founding Director, and Principal Investigator, NSF Engineering Center for Smart Lighting, Rensselaer Polytechnic Institute
2002 – 2003: Adjunct Professor, Boston University
1995 – 2002: Professor, Boston University, Department of Electrical and Computer Engineering; Director of the Semiconductor Devices Research Laboratory; Affiliated Faculty of the Photonics Center.
1988 – 1995: Member of Technical Staff; Principal Investigator; and Member of Management at AT&T Bell Laboratories in Murray Hill, New Jersey
1985 – 1987: Post-Doctoral Member of Technical Staff at AT&T Bell Laboratories in Holmdel, New Jersey.
1981 – 1985: Scientific Member of Staff in the Department of Solid-State Chemistry at the Max Planck Institute for Solid-State Research in Stuttgart, Germany. Ph.D. Dissertation title: "Modern Schottky gate field-effect transistors based on III–V semiconductors"

Fields of Technical Expertise, Hands-on Experience, and Teaching

- Expertise, hands-on experience, and teaching in semiconductor opto-electronics including the following devices: LED, semiconductor laser, vertical cavity surface-emitting laser (VCSEL), solar cell, photo-detector, LED displays, micro-LED displays, LCD displays, and OLED displays. The activities include the design, fabrication, processing, and packaging of the devices, and the use of the devices in circuits and systems. (1981 to present)
- Expertise, hands-on experience, and teaching in semiconductor electronics including the following devices: MESFET, HFET, MOSFET, CMOS-FET, LDD MOSFET, LD MOS FET, FinFET, GAA FET, Vertical MOSFET (high-power MOSFET), thyristor, GTO thyristor, and IGBT. The activities include the design, fabrication, processing, and packaging of the devices, and the use of the devices in discrete and integrated circuits. (1979 to present)
- Expertise, hands-on experience, and teaching in thin-film deposition of metal, semiconductor, and insulator films by PVD (physical vapor deposition) and CVD (chemical vapor deposition) including PECVD (plasma enhanced CVD), MOCVD (metal-organic CVD), ALE (atomic layer epitaxy), ALD (atomic layer deposition), and bulk crystal growth (AlN, GaN, and sapphire). Epitaxial growth of silicon, III-V arsenide, phosphide and nitride epitaxial layers on GaAs, sapphire, Si, and GaN substrates by epitaxy including molecular beam epitaxy (MBE),

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metal-organic chemical vapor deposition (MOCVD), and vapor-phase epitaxy (VPE). High-k materials, low-k-materials, phosphors, resins, polymers, encapsulants, alloy semiconductors and their deposition technologies such as epitaxy, CVD, and PVD. Doping of semiconductors by various means including delta doping and atomic monolayer doping. (1981 to present)

- Expertise, hands-on experience, and teaching in the design, operation, and usage of semiconductor devices in lighting systems, communication systems, and power-supply systems and in the analysis and development of LED power supplies using Boost and Buck Converters. (1993 to present)

Technical Research Activities

- Design, development and fabrication of a Si pressure sensor based on the piezo-resistivity of Si using a bridge configuration of four thin-film Si resistors (1979 – 1980)
- Design of a electro-optic Mach-Zehnder Interference Modulator based on Lithium niobate ($LiNbO_3$) operating at a wavelength of 1300 nm (1980 – 1981)
- First study of hot electron effects in selectively doped $Al_xGa_{1-x}As/GaAs$ heterostructures (1983)
- Demonstration and elimination of parallel conduction in $Al_xGa_{1-x}As/GaAs$ heterostructures (1984)
- First analysis of semiconductors doped with simultaneously shallow and deep donors (1984).
- Development and use of thyristor circuits (including GTO thyristor circuits) for the control of a lamp heating system (1984 – 1985)
- Proposal and demonstration of the δ-doped field-effect transistor. Short-channel effects in sub-micron field-effect transistors can be reduced to their theoretical minimum by using δ-doped structures (1985)
- Development of the theory of alloy broadening in luminescence spectra of alloy semiconductors such as $Al_xGa_{1-x}As$. The current understanding of the low-temperature spectral linewidths of ternary and quaternary alloy semiconductors is based on this theoretical model. The publication analyzing the phenomenon of alloy broadening has been referenced far in excess of 100 times (1984)
- First demonstration of a light-emitting diode with a doping superlattice active region (1985)
- Application of δ-doping to selectively doped heterostructures; Demonstration of high-electron-mobility transistors (HEMTs) with highest free electron concentrations; Analysis of structures by SEM, TEM, and SIMS (1986).
- Demonstration of delta-doped non-alloyed ohmic contacts with very low contact resistance and subsequent demonstration of self-aligned field-effect transistor with delta-doped non-alloyed ohmic contacts (1986)
- Demonstration of the spatial localization of dopants within 20 Å for a number of doping elements in delta-doped semiconductors including GaAs and Si for MESFET and lightly-doped drain (LDD) MOSFET applications and the analysis of delta-doped structures by SIMS (secondary ion mass spectrometry) (with colleague Henry S. Luftman, 1983-1995)
- Significant improvement of the optical properties of doping superlattices by employment of delta doping. Improvement is demonstrated by the first observation of quantized interband transitions in the absorption (1988) and in the emission spectra (1989)
- First demonstration of tunable doping superlattice laser (1989)
- First quantitative analysis of the capacitance-voltage (CV) profiling technique in semiconductors with quantum-confined carriers. Demonstration that resolution of CV profiles in quantum-confined semiconductors is not limited to the Debye screening length (1990)
- Invention and demonstration a new concept by which heterojunction band discontinuities occurring between two different semiconductors are eliminated. The *elimination of heterojunction barriers* is based on parabolic compositional grading of doped heterojunctions. This concept is widely used in the fabrication of vertical cavity surface emitting lasers and other heterojunction devices (1991)
- Invention and first demonstration of resonant cavity light-emitting diode (RCLED) which uses photon quantization in microcavities to enhance the spontaneous emission properties (1992)
- Demonstration of giant enhancement of luminescence intensity in Er-doped Si-SiO_2 microcavities (1992)
- First demonstration of a resonant-cavity detector which is useful for wavelength-selective detection (1993)
- Demonstration of resonant-cavity light-emitting diode (RCLED) with very high brightness. The experimental brightness of the RCLED is five times higher than that of conventional LEDs. Based on calculations, the brightness of RCLEDs is expected to exceed that of conventional LEDs by more than a factor of ten (1994)
- Demonstration of delta doping in silicon for the fabrication of shallow junctions in scaled-down Si lightly-doped drain (LDD) MOSFETs for integrated circuits (Si ICs) (with colleague Dr. H. J. Gossmann, 1990 – 1995)
- Invention of a new concept, *superlattice doping*, for enhanced p-type doping of GaN. All acceptors in GaN are deep, resulting in a low electrical acceptor activation of only 5 %. The new concept of superlattice doping is expected to increase the electrical activation of acceptors by more than a factor of ten (with post-doctoral associate Dr. W. Grieshaber, 1995)

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- Investigation of yellow luminescence in GaN and the use of microcavity effects in Ag / GaN / sapphire structures to determine the refractive index of GaN (with post-doctoral associate Dr. W. Grieshaber, 1996)
- Demonstration of the first GaN / GaInN double heterostructure laser. The laser has cleaved facets and was optically pumped. Laser action was demonstrated by (*i*) a threshold in the light-versus-current characteristic, (*ii*) spectral narrowing below *kT* above threshold, (*iii*) a TE / TM polarization ratio greater than one hundred above threshold, and (*iv*) increased slope efficiency with increasing back-side facet reflectivity (with graduate student D. A. Stocker, 1997)
- Co-inventor of photonic-crystal light-emitting diode, PC-LED, jointly with group of Prof. John D. Joannopoulos at MIT (publication by Shanhui Fan *et al.* appeared in *Physical Review Letters* in 1997; US patent 5,955,749 was issued in 1999)
- First demonstration of crystallographic etching of GaN (with graduate student D. A. Stocker, 1998). The discovery, crystallographic etching, can be implemented by wet chemical etching, including photo-enhanced electrochemical (PEC) wet etching. The discovery is widely used in the LED industry to strongly enhance light extraction from LED chips and is found in LED light bulbs.
- Experimental demonstration of a ten-fold enhancement of p-type doping activation in $Al_xGa_{1-x}N$/GaN doped superlattices as compared to bulk GaN and $Al_xGa_{1-x}N$ (with graduate students D. A. Stocker and I. D. Goepfert, 1999)
- Invention and demonstration of the photon-recycling semiconductor light-emitting diode (PRS-LED) which emits *white* light and many other colors with very high luminous performance of > 300 lm/W (with graduate students X. Guo and J. W. Graff, 1999). Invention of the monolithically integrated GaInN/GaN PRS-LED (with graduate students X. Guo and J. W. Graff, 2000)
- Invention and demonstration of polarization-enhanced ohmic contacts in p-type and n-type GaN (with graduate students Y.-L. Li and J. W. Graff 2000)
- Invention and demonstration of AlGaInP light-emitting diode with omni-directional reflector (ODR) for high light extraction efficiency (with post-doctoral associate Th. Gessmann and graduate student J. W. Graff, 2001)
- Developed novel model for high diodes ideality factors ($n >> 2.0$) in UV LEDs based on multiple rectifying elements (with graduate student J. M. Shah and Prof. Th. Gessmann, 2003)
- Developed new class of materials, low-refractive index materials, or low-*n* materials, with an unprecedented low refractive index of $n < 1.10$; use of these materials as low-*k* materials for inter-metal-layer dielectrics in Si lightly-doped drain (LDD) MOSFETs in conjunction with ALD-deposited high-*k* gate dielectric MOSFETs for integrated circuits (Si ICs) (with Dr. Jong Kyu Kim, "JQ" Xi, Professors Joel Plawsky, Bill Gill, starting in 2003)
- Developed theory for temperature coefficient of forward voltage in light-emitting diodes, particularly UV light-emitting diodes (with graduate student Yangang "Andrew" Xi, Dr. Jong Kyu Kim, and collaborators at Sandia National Laboratories, 2004, 2005)
- Invented highly efficient "remote phosphor configurations" in white light-emitting diodes (with Jong Kyu Kim, Hong Luo, and collaborators at SAIT-Samsung) (2004, 2005)
- Discovered whispering gallery modes in white LEDs with remote phosphors (with graduate student Hong Luo, Jong Kyu Kim, Yangang "Andrew" Xi, and collaborators at SAIT-Samsung, 2005)
- Developed graded-index antireflection coatings that, unlike conventional anti-reflection coatings, have broadband omni-directional characteristics; the graded-index antireflection coatings use novel low-*n* materials (with Jingqun "JQ" Xi, Jong Kyu Kim, 2007)
- Developed efficiency-droop reducing GaInN / GaInN and GaInN / AlGaInN LED active regions grown by MOCVD and ALE that were demonstrated to reduce the efficiency droop by as much as 40% (with Jong Kyu Kim, Martin F. Schubert, Di Zhu, Jiuru Xu, Mary Crawford, and Dan Koleske, starting in 2007)
- Developed analytic model for efficiency droop based on drift-induced reduction of the carrier-injection efficiency (with Guan Bo Lin, Jaehee Cho, and others, 2012)

Honors and awards

- Google Scholar profile, including the Hirsch-index (h-index) can be found at < http://scholar.google.com > under profile "E. Fred Schubert"
- Elected to *Senior Member* of the *IEEE* "in recognition of professional standing" (1993)
- Recipient of the Literature Prize of the *Verein Deutscher Elektrotechniker* (*VDE*) for "Doping in III–V semiconductors" (Cambridge University Press, Cambridge, 1993). Citation: "The book concerns all aspects of doping in III–V semiconductors. Fundamental, practical, and technological issues of doping are addressed. The book covers the basic theory of shallow donors, shallow acceptors, deep levels, and their influence on the free carrier concentration. It also discusses doping during growth, epitaxy, diffusion, and ion implantation. In the field of semiconductor devices, the book emphasizes applications requiring highly controlled doping distributions. It is an excellent monograph equally suited for study, research, and industry" (1994)

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- Elected as a member of the *Bohemian Physical Society* (Cornell University, Ithaca, NY). Citation: "For seminal contributions to the control of spontaneous emission by use of wavelength-size optical cavities, specifically the first demonstration in a glass host using rare earth implanted Si/SiO_2 resonant microcavities" (1994)
- Listed in "Who's Who In Science And Engineering" and "Who's Who in America" published by *Marquis Who's Who*, publishers of the original *Who's Who in America*. (*Marquis Who's Who*, New Providence, NJ) ISBN 0-8379-5755-9 (1996 – present)
- Elected Fellow *of the SPIE* "For pioneering research in semiconductor doping and sustained contributions to the development of high-efficiency light-emitting diodes and lasers". According to the Society's bylaws, a Fellow "shall be distinguished through his achievements and shall have made outstanding contributions in the field of optics, or optoelectronics, or in a related scientific, technical, or engineering field" (1999)
- Recipient of the *Alexander von Humboldt Senior Research Award* of the Alexander von Humboldt Foundation, a Bonn-based non-profit organization promoting the exchange of scientific knowledge between German and highly qualified foreign scholars. According to the Alexander von Humboldt Foundation, academic qualification is the only selection criterion for the award. The award resulted in two extended visits with the Microoptics Laboratory of Professor Jürgen Jahns at the University of Hagen, Germany (1999)
- Elected to *Fellow of the IEEE* "for contributions to semiconductor doping and resonant-cavity devices". According to the IEEE definition "the grade of Fellow is one of unusual professional distinction conferred by the Board of Directors only upon a person of extraordinary qualifications and experience" (1999)
- Listed in the "Dictionary of International Biography, 29th Edition" published by the *International Biography Center*, Cambridge, United Kingdom (2000)
- Recipient of the 2000 *Discover Magazine Award for Technological Innovation* presented by the *Christopher Columbus Foundation* in the category "Energy". The prize was awarded "for the invention and demonstration of the photon recycling semiconductor light-emitting diode", an all-semiconductor LED capable of emitting white light with very high efficiency, see < www.discover.com/awards > (2000)
- Recipient of the *RD100 Award* of the R&D Magazine that honors the "100 most technologically significant products of the year" (with Klaus Streubel of Osram-Sylvania Corp. and Rickard Marcks von Wurtemberg of Mitel Corp.). The prize was awarded for the "*Resonant-cavity light-emitting diode*" that uses enhanced spontaneous emission occurring in resonant cavities. The device is used in plastic optical fiber communication links, in telescopes for rifles, and many other applications (2000).
- Elected to *Fellow of the OSA* "for the invention and demonstration of the resonant-cavity LED and the photon-recycling semiconductor LED". OSA Fellows are elected by the OSA Board of Directors (2001)
- Recipient of the Boston University Provost Innovation Fund Award (Provost Dennis D. Berkey) valued at $ 25,000 for research and development of promising technologies (2001)
- Elected to *Fellow of the APS* "for pioneering contributions to the doping of semiconductors including delta doping, doping of compositionally graded structures resulting in the elimination of band discontinuities, and superlattice doping to enhance acceptor activation" (2001)
- Honored with RPI Medal as Senior Constellation Chair during Investiture Ceremony (2002)
- Received "2002 Rensselaer Polytechnic Institute Trustee Faculty Achievement Award" (2002)
- Inducted as Wellfleet Senior Constellation Professor, Future Chips, Rensselaer Polytechnic Institute, November 21 (November 2003)
- Distinguished Lecturer of the IEEE Electron Devices Society (2003–2006)
- Elected member in Eta Kappa Nu (2004)
- "Best Oral Presentation Award" was won by Ph. D. student Hong Luo (who was the presenter), J. K. Kim, Y. A. Xi, J. M. Shah, Th. Gessmann and E. F. Schubert "Improvement of extraction efficiency of GaInN light-emitting diodes by employment diffuse omni-directional reflectors" *Connecticut Microelectronics & Optoelectronics Consortium (CMOC)*, 14th annual symposium, New Haven CT, March 17 (March 2005).
- "Best Student Poster Award" of the *International Semiconductor Device Research Symposium (ISDRS)* was won by Ph. D. student J.Q. Xi (presenter), Jong Kyu Kim, Dexian Ye, Jasbir S. Juneja, T.-M. Lu, Shawn-Yu Lin, and E. Fred Schubert "Optical Thin Films with Very Low Refractive Index and Their Application in Photonic Devices", *International Semiconductor Device Research Symposium (ISDRS)*, Dec. 7 – 9, Bethesda, MD (December 2005)
- "MRS Silver Award" of the Materials Research Society was won by Ph. D. student Yangang Andrew Xi (who was the presenter), K. X. Chen, F. Mont, J. K. Kim, C. Wetzel, E. F. Schubert, W. Liu, X. Li, J. A. Smart "Extremely high quality AlN grown on (0001) sapphire by using metal-organic vapor-phase epitaxy" *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 – December 1 (2006) Boston MA (December 2006)
- "25 Most Innovative Micro- and Nano-Products of 2007 Award" in July 2007 issue of *R&D Magazine* and *Micro/Nano Newsletter*. This recognition was given for the "Non-Reflective Coating" product that was published in *Nature Photonics* in 2007; full citation: Xi, J.-Q., Martin F. Schubert, J. K. Kim, E. F. Schubert,

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Minfeng Chen, Shawn-Yu Lin, Wayne Liu, and Joe A. Smart "Optical thin-film materials with low refractive index for broadband elimination of Fresnel reflection" *Nature Photonics* **1**, 176, March 2007 (July 2007)

- "Scientific American 50 Award" of 2007, as published in the January 2008 issue of *Scientific American*. According to the *Scientific American Magazine*, this award "celebrates visionaries from the worlds of research, industry and politics whose recent accomplishments point toward a brighter technological future for everyone" (January 2008)
- "Editors' Choice" of *Science Magazine*, *Science*, Volume **319**, page 1163, February 29 (February 2008). This distinction was awarded for the publication: Jong Kyu Kim et al., "Light-extraction enhancement of GaInN light-emitting diodes by graded-refractive-index indium tin oxide anti-reflection contact" that appeared in *Advanced Materials* **20**, 801, 2008 (February / March 2008)
- Received "2008 Rensselaer Polytechnic Institute Trustee Faculty Achievement Award" (2008)
- "Best Oral Presentation Award" won by David J. Poxson (who was the presenter), Frank W. Mont, Jong Kyu Kim, and E. Fred Schubert "Multilayer nano-structured anti-reflection coating with broad-band omni-directional characteristics" *Connecticut Microelectronics and Optoelectronics Conference* (*CMOC*), University of Connecticut, Storrs, Connecticut, April 9 (April 2008)
- "Best Oral Presentation Award" for presentation: David Meyaard, Sameer Chhajed, Jaehee Cho, E. Fred Schubert, Jong Kyu Kim, Daniel D. Koleske, and Mary H. Crawford "Temperature-dependent light-output characteristics of GaInN light-emitting diodes with different dislocation densities" *Connecticut Microelectronics and Optoelectronics Consortium* (CMOC) Symposium, New Haven CT, March 2 (March 2011)
- Identified as top 1% of patentees in the field of optoelectronics by study conducted by Professor Erica Fuchs of Carnegie Mellon University under a study supported by the US National Science Foundation (July 2011)
- Received "2012 Rensselaer Polytechnic Institute Trustee Faculty Achievement Award" (November 2012)
- My "LinkedIn" profile was one of the top 10% most viewed "LinkedIn" profiles during 2012 (January 2013)
- My graduate student, Mr. Ming Ma, received the $ 30,000.00 Lemelson-Rensselaer Student Prize for the invention entitled "Graded-refractive-index (GRIN) structures for brighter and smarter light-emitting diodes"; The Prize is awarded annually by the Lemelson Foundation (March 2013)
- Received the IEEE Life Fellow Award (2022)

Service to the technical community

- Current or former member of the *American Physical Society* (Member of the *Division of Materials Physics*, Member of the *Division of Condensed Matter Physics*), *Institute of Electrical and Electronics Engineers*, *Materials Research Society*, *Optical Society of America*, *Society for Optical Engineering* (*SPIE*), and the *Verein Deutscher Elektrotechniker*
- Co-author of hundreds of research articles, co-inventor of more than 30 United States patents, and numerous foreign patents (1981 – present)
- Gave many invited talks at scientific conferences organized by the *American Physical Society*, *Institute of Electrical and Electronic Engineers*, *Materials Research Society*, *SPIE* (*The International Society for Optical Engineering*), *Electrochemical Society*, *American Vacuum Society*, *Engineering Foundation*, and other professional societies (1985 – present).
- Co-editor (with A. M. Glass) of a Special Issue of the *Journal of Optical and Quantum Electronics* (Vol. **22**, 1990) on "Charge-transport assisted optical non-linearities in semiconductors" (1990)
- Symposium chair of the *American Vacuum Society Greater New York and New Jersey Chapter* on "Epitaxially grown semiconductors with atomic level control" (1991).
- Moderator of MRS Internet discussion on "Doping and Dopants in GaN" (MRS Internet Journal, 1995 – 1997)
- Member of review panels of the National Science Foundation (1995 – present)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (1997)
- Technical work has been featured in popular journals, magazines and newspapers including the New Scientist, Discover Magazine, Wall Street Journal, Boston Globe, Focus, and on National Public Radio (1996 – present)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (1998)
- Program Committee Member: IEEE IEDM, International Electron Devices Meeting (1999 and 2000)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (1999)
- Program Committee Member: ISBLLED, International Symposium on Blue Laser and Light-Emitting Diodes, Berlin, Germany, March 5 – 10 (2000)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (2000)

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- Conference Chair and Co-Organizer of the TMS- and ONR-sponsored conference on "Doping, Dopants, and Low Field Carrier Dynamics in Wide Gap Semiconductors", Copper Mountain, Colorado, April 2 - 6 (2000)
- Chair, IEEE LEOS, Central New England Chapter. During my tenure as Chair, the Central New England Chapter won the IEEE LEOS Chapter award for the highest membership growth (1999 – 2000)
- Expert Witness involving semiconductor materials, devices, and packaging including elemental and compound semiconductors such as Si, SiGe, SiC, as well as III–V arsenides, phosphides and nitrides (1998 – present)
- Member of the Board of Governors, IEEE Laser and Electro-Optics Society (LEOS) (1999 – 2000)
- Member of the Optoelectronics Industry Development Association (OIDA) Roadmap Panel on Solid-State Lighting, Albuquerque NM Oct. 26 – 28 (2000)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (2001)
- Panel Member of National Research Council meeting on "Solid-State Lighting:" held at NAS and NAE, Washington DC, March 26 (2001)
- Program Committee Member of SPIE Photonics West conference on "Laser and LED Applications" chaired by Dr. Kurt Linden, San Jose CA Jan (2002)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (2002)
- Program Committee Member: ISBLLED, International Symposium on Blue Laser and Light-Emitting Diodes, Cordoba, Spain, March 11–15 (2002)
- Program Committee Member for subcommittee on "Semiconductor lasers and LEDs" for OSA Conference on Lasers and Electro-Optics and Quantum Electronics and Laser Science Conference (CLEO / QELS) (2002 – 2003) Baltimore MD June 1–6 (2003)
- Reviewer for the National Research Council of report entitled "Partnerships for Solid-State Lighting: Report of a Workshop" authored by the Board on Science, Technology, and Economic Policy. This report is forwarded to the US Congress for the initiation of a national Solid-State Lighting Initiative. (2002)
- Program Committee Member "Lester Eastman conference on high performance devices" University of Delaware, Newark, Delaware, August 6 – 8 (2002)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose CA (2003)
- OIDA Next Generation Lighting (NGL) Consortium. Member of "Light-Emitting Diode" Committee (2003)
- Program Committee Member, International Semiconductor Device Research Symposium (ISDRS) Washington DC, Dec. 8 – 12 (2003)
- Program Committee Member of "Display and Solid-State Lighting Devices" conference for OSA/IEEE Conference on Lasers and Electro-Optics (CLEO) (2003 – 2004)
- Elected Member of the IEEE Electron Device Society Administration Committee (IEEE AdCom) (2003 – 2008)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose CA (2004)
- Program Committee Member "Fourth International Conference on Solid-State Lighting" August 2 – 6 Denver, CO (2004)
- Program Committee Member for the "Blue 2004: Advanced LEDs and Lasers Conference" Hsinchu, Taiwan, May 10 – 12 (2004)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose CA (2005)
- Program Committee Member "International Semiconductor Device Research Symposium" December 7 – 9 Washington, DC (2005)
- Chair of "Display and Solid-State Lighting Devices" conference of OSA/IEEE Conference on Lasers and Electro-Optics (CLEO) (2005)
- Best Oral Presentation Award (Presenter: Hong Luo) at *Connecticut Microelectronics & Optoelectronics Consortium* (CMOC), 14th annual symposium, New Haven CT, March 17 (March 2005)
- Conference Chair of MRS Spring meeting "Symposium DD: Solid-State Lighting Materials and Devices" San Francisco, April 17 – 21 (April 2006)
- Member on the International Advisory Committee of *First International Conference on Display LEDs* (ICDL 2007), Seoul, Korea, January 31 to February 2 (2007)
- Member, Program Committee of *SPIE Photonics West* conference "Light-Emitting Diodes: Research, Manufacturing, and Applications XI" San Jose, CA, January 20 – 25 (2007)
- Program Chair of *SPIE Photonics West* conference "Semiconductor Lasers and LEDs" San Jose, CA, January 20 – 25 (2007)
- Member, Executive Organizing Committee *SPIE Photonics West* conference "LASE 2007" San Jose, CA, January

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20 – 25 (2007)

- Opto Track Chair of *SPIE Photonics West* conference "Semiconductor Lasers and LEDs" San Jose, CA, January 21 – 24 (January 2008)
- Member, Program Committee, Light-emitting diodes: Research, Manufacturing, and Applications, SPIE Photonics West 2008, San Jose, California, January 19 – 24 (January 2008)
- Program Committee Member of the 7th International Symposium on Semiconductor Light Emitting Devices (ISSLED-2008) held in Phoenix, Arizona (USA), April 27 – May 2 (April 2008)
- Member, Program Committee, China SSL 2008, Shenzhen Convention & Exhibition Center, China, July 24 – 26 (July 2008)
- Member, Program Committee, International Workshop on Nitride Semiconductors, IWN 2008, Montreux, Switzerland, October 6 – 10 (October 2008)
- Opto Track Chair of *SPIE Photonics West* conference "Semiconductor Lasers and LEDs" San Jose, CA, January 25 – 29 (January 2009)
- Guest Editor of Special Issue on *Solid-State Lighting* published in the *IEEE Journal of Selected Topic in Quantum Electronics*, July / August edition (August 2009)
- Honorable Conference Chair, 6th China International Forum on Solid-State Lighting (China SSL), Shenzhen Convention & Exhibition Center, China, October 14 – 16 (October 2009)
- Program Committee Member, International Conference on Nitride Semiconductors (ICNS), Jeju, South Korea, October 18 – 23 (October 2009)
- Program Committee Member, The Second International Conference on White LEDs and Solid-State Lighting, Taipei, Taiwan, December 13 – 16 (December 2009)
- Editor, *Compound Semiconductors and Energy Applications and Environmental Sustainability*, Materials Research Society (MRS) Symposium Proceedings Volume 1167 (MRS, Warrendale PA, 2009)
- Conference Chair, OPTO, *SPIE Photonics West 2010*, San Francisco, California, January 23 – 27 (January 2010)
- Guest Editor of Special Issue on *Light-Emitting Diodes* published in the *IEEE Transactions on Electron Devices* (January 2010)
- Program Committee Member, *8th International Symposium on Semiconductor Light Emitting Devices* (ISSLED), Beijing, China, May 16 – 21 (May 2010)
- International Advisory Committee Member of the 16th *Microoptics Conference* (MOC'10) held in Hsinchu, Taiwan, sponsored and endorsed by OSA and IEEE/Photonics Society and organized by National Chiao Tung University, Oct. 31 to Nov. 3 (October 2010)
- Member of Academic Committee of *China Solid-State Lighting Conference* (CHINA SSL 2010) Shenzhen, China, October 14 – 16 (October 2010)
- Conference Co-Chair, OPTO, *SPIE Photonics West 2011*, San Francisco, California, January 22 – 27 (January 2011)
- Executive Organizing Committee OPTO, *SPIE Photonics West 2011*, San Francisco, California, January 22 – 27 (January 2011)
- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid-State Lighting XV *SPIE Photonics West 2011*, San Francisco, California, January 22 – 27 (January 2011)
- Member of CLEO Subcommittee 15, entitled "LEDs, Photovoltaics and Energy-Efficient ("Green") Photonics" for the 2011 Conference on Lasers and Electro-Optics (CLEO), Baltimore, Maryland May 1 – 6 (May 2011)
- Member of the Academic Committee of the 8th China International Forum on Solid-State Lighting (CHINA-SSL-2011) Guangzhou November 8 – 10 (November 2011)
- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid-State Lighting XV *SPIE Photonics West 2012*, San Francisco, California, January 21 – 26 (January 2012)
- Member of CLEO Subcommittee 15, entitled "LEDs, Photovoltaics and Energy-Efficient ("Green") Photonics" for the 2012 Conference on Lasers and Electro-Optics (CLEO), San Jose, California, May 6 – 11 (May 2012)
- Member of Academic Committee of the 9th China International Forum on Solid-State Lighting (CHINA SSL 2012), Guangzhou, China, November 5 – 7, 2012 (November 2012)
- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid-State Lighting XVI *SPIE Photonics West 2013*, San Francisco, California, 2 – 7 February 2013 (February 2013)
- Member of CLEO Subcommittee in the topic area: "Science & Innovation 15: LEDS, Photovoltaics and Energy-Efficient ("Green") Photonics" for the CLEO 2013 conference, April 28 – May 3, 2013 in Baltimore, Maryland (May 2013)
- Member, International Advisory Committee of the International Conference on Advanced Electromaterials (ICAE 2013) held on Jeju Island, Korea, from November 12 – 15, 2013 (November 2013)

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- Program Committee Member, *Solid-State and Organic Lighting* (*SOLED*), OSA Topical Meeting, 3 – 7 November 2013, Marriott Tucson Star Pass, Tucson, Arizona, USA (November 2013)
- Co-Chair, OPTIC International Conference, Chung Li, Taiwan, National Central University, December 5 – 7, 2013 (December 2013)
- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid-State Lighting XVII" *SPIE Photonics West* 2013, San Francisco, California, 1 – 8 February (2014)
- Publication Committee Member, *5th International Conference on White LEDs and Solid-State Lighting* (White LEDs), Jeju Island, Korea, May 25 – 28, 2014 (May 2014)
- Sub-Committee Chair of Track 6: Displays, Solid-State Lighting, Photovoltaics, and Energy-Efficient Photonics of *Asia Communications and Photonics Conference 2014* (ACP 2014). ACP is the largest and the most influential conference in Asia and Pacific Rim for communications and photonics technologies. ACP 2014, Shanghai International Convention Center, Shanghai, China, November 11 – 14 (2014)
- International Consultant of technical seminar of the 11th China International Forum on Solid-State Lighting (SSL-China 2014) Guangzhou, China, November 6 – 8 (2014)
- Member of the International Advisory Committee of the 11th International Symposium on Semiconductor Light Emitting Devices (ISSLED 2017) held in Banff, Canada on October 8 – 13 (2017)
- Assisting the US Judicial Government Branch (various US District Courts), the USPTO (US Patent and Trademark Office) and the ITC (International Trade Commission) by serving as an independent Technical Expert Witness (1997 to present)

Books

- ***Doping in III-V semiconductors*** (author) Hardback and paperback, 628 pages (Cambridge University Press, Cambridge, UK, 1993). The following excerpt is from a book review by D. L. Miller, *University of Pennsylvania*, University Park PA, which appeared in *Physics Today*, Oct. 1994, p. 71: "[...] Fred Schubert has written a book that very nicely fills two roles: It serves as a reference volume for those of us who use III-V materials, and it provides enlightening explanations of interesting and important problems in semiconductor physics. [...] Schubert, who is employed by AT&T Bell Laboratories, brings his extensive research involvement with III-V materials physics straight to this book. His lucid explanations of some of the important physics of doped semiconductors is a major strength. For example, the chapter on deep centers provides the clearest treatment of the DX center I can remember reading, and it uses the large lattice distortion model and configurational coordinates introduced for the DX center to describe the EL2 deep level. This book can also serve as an excellent reference volume, because it briefly describes epitaxial growth techniques and the doping methods used with them, catalogs dopant-related phenomena, describes characterization techniques and provides 45 pages of citations to published articles and books. [...] I will use it to help my graduate students in the physics of semiconductors. [...] It will certainly be available on my bookshelf, in part to remind me what the Burstein-Moss shift is and in part for the literally hundreds of references that it provides on nearly every topic related to III-V semiconductor doping. Because of its clarity in treating some interesting phenomena of modern semiconductor physics, you too might want to get a copy of this book, even if you believe that Ga and As are just poor alternatives for doping silicon"
- ***Delta doping in semiconductors*** (editor) Hardback and paperback, 616 pages (Cambridge University Press, Cambridge, U. K., 1996)
- ***Light-emitting diodes*** (author) Hardback and paperback, 328 pages (Cambridge University Press, Cambridge, UK, 2003). The following excerpt is from a book review by David Bour, *Agilent Laboratories*, Palo Alto CA, which appeared in *Physics Today*, Nov. 2004, p. 66: "[...] In "*Light-emitting diodes*", E. Fred Schubert provides an excellent review of the physics and technology of semiconductor LEDs. [...] Interesting anecdotes like [the first demonstration of electroluminescence], clearly written by someone with a broad perspective and expertise, appear throughout the book, making it enjoyable to read. [...] Schubert provides an excellent description of the undesirable [non-radiative] recombination pathway. [...] Schubert has made pioneering contributions to those devices, and this variety of LEDs may become more widely used in the future. [...] Overall, "*Light-emitting diodes*" is an excellent examination of the physics and technology of semiconductor LEDs. The narration is simple and direct, and the book is well referenced for those seeking a deeper understanding of the topic. Written for the graduate level, the text will appeal to a broad audience; and for specialists who make semiconductor LEDs and laser diodes, it will serve as a useful connection to the scientific literature."
- ***Light-emitting diodes, second edition*** (author) Hardback, 422 pages (Cambridge University Press, Cambridge, UK, 2006)
- ***Physical Foundations of Solid-State Devices*** (author) eBook, 275 pages, ISBN-13: 978-0-9863826-2-8 (Google Books, Mountain View CA, 2015)

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- ***Light-emitting diodes, 3rd edition*** (author) eBook, 672 pages with hundreds of colored illustrations, ISBN: 978-0-9 863826-6-6 (Google Books, Mountain View CA, 2018) "The 1st edition of the book "Light-Emitting Diodes" was published in 2003. The 2nd edition was published in 2006. The current 3rd edition of the book is a substantial expansion of the second edition and has 37 chapters. The book includes a thorough discussion of white light-emitting diodes (LEDs), phosphor materials used in white LEDs, packaging technology, and the various efficiencies and efficacies encountered in the context of LEDs. The background of light, color science, and human vision is provided as well. The fully colored illustrations of the 3rd edition are undoubtedly beneficial given the prominent role of light and color in the field of LEDs. The book is a comprehensive discussion of the LED, particularly its semiconductor physics, electrical, optical, material science, thermal, mechanical, and chemical foundations. The 3rd edition is published in electronic format in order to make the book affordable and easily accessible to a wide readership."

Courses and laboratories developed at Boston University

- Developed first laboratory for "Physics of semiconductor devices" (SC-471) Fall (1998)
- Developed course "Quantum mechanics applied to semiconductor devices" (SC-574) Fall (1999)
- Developed course "Semiconductor light emitters" (SC-760) Fall (2000)
- Developed distance-learning course and NTU course on "Light-emitting diodes – Device physics and applications" Fall (2000)

Courses taught at Boston University

- Undergraduate Course "Physics of semiconductor devices" (SC-471)
- Graduate course "Fiber optic communication systems" (SC-563)
- Graduate course "Quantum mechanics applied to semiconductor devices" (SC-574)
- Graduate course "Introduction to solid-state physics of devices" (SC-577)
- Graduate course "Quantum electronics" (SC-700)
- Graduate course "Integrated optoelectronics" (SC-770)
- Graduate course "Compound semiconductor devices" (SC-771)
- Graduate course "Light-emitting diodes" (SC-760)
- Graduate course "Research seminar" (SC-860, SC-892)
- Other courses "Research", "Guided Study", "Master Thesis", and "Dissertation" (SC-900)

Courses taught at Rensselaer Polytechnic Institute

- Graduate Course "Semiconductor devices and models II" (ECSE-6290)
- Undergraduate course "Microelectronics technology" (ECSE-2210)
- Undergraduate course "Fields and Waves 1" (ECSE-2100)
- Graduate course "Quantum mechanics applied to semiconductor devices" (ECSE-6968)
- Graduate course "Physical foundations of solid-state devices" (SC-6960)
- Graduate course "Light-emitting diodes and solid-state lighting" (SC-6961)
- Undergraduate course "Introduction to Electronics" (ECSE-2050)
- Other courses "Research", "Guided Study", "Master Thesis", and "Dissertation"

Teaching evaluations and students' comments

1997 – Students made the following comments: "Clear … organized … excellent explanations … I've never had a professor like him – I wish all were like him … very clear and concise presentations … strong response to students' questions and concerns … Professor provided excellent notes … laid out lectures in a clear and precise manner which worked out wonderfully … well organized and confident … responsive to students' concerns … excellent for students going into the semiconductor industry … excellent hand-outs and course materials … well prepared … clear lectures … I was strongly encouraged … materials are very interesting … hand-outs were excellent … material is very important … the presentation of materials was very clear … hand-outs were excellent support to the class … efforts made by Prof. Schubert in keeping everyone at the same pace was remarkable …"

1998 – Students made the following comments: "Professor was always well prepared … excellent content … very relevant for the field of solid-state devices … excellent preparation for the class … handouts were very good … very well-organized teacher … excellent knowledge of material … provided a complete background of all material … easy to talk to … excellent overall teaching skills … really enjoyed coming to class … his choice of topics and homework helped me a lot … enthusiastic in teaching and helpful during the office hours … one of the best professors I have had at BU … course gave a very good overview of the different solid-state physics principles … the course was very well organized … relevant examples and homework were given … good explanations were

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given ... presented clearly ... presentation was clear ... communicated effectively ... very knowledgeable ... good demonstrations in class ... gives clear descriptions ... asks questions of class ... grades homework fairly ... good at answering questions ... no weak points ... excellent instructor and scientist ... inspiring professor ... thorough ... the instructor is very precise and well prepared ... his knowledge of the material is exact ... very responsive to feedback ... encourages student questions, class participation and discussion ... the instructor cared about whether students understood material ... the instructor used applications immediately after showing theory ... handouts were excellent ... guest lecture and lab tour excellent idea ... excellent class notes ... presented topics neatly ... well prepared ... review of ongoing research topics was great ... Professor Schubert is undoubtedly an expert in his area ..."

1999 – Students made the following comments: "He enjoyed teaching the material and was very clear ... the presentation of the material in class was excellent ... he helped me to understand a lot about semiconductors ... Prof. Schubert always tried to make sure that we would all have a clear understanding of the material ... manuscripts were very helpful ... encouraged lots of class participation and was always readily available for help ... presentation was excellent ... the instructor was always willing to help me ... very helpful ... Clearly, Prof. Schubert is *more* than just extremely knowledgeable about this material ... very thorough and exact communication of points ... excellent course packet written by the instructor ... he was very well prepared for class ... He is extremely fair and encourages participation ... he is also very accessible ... excellent instructor ... very approachable and easy to ask questions of ... handouts were very effective and helpful ... Prof. Schubert is very prepared and concepts are well explained ... materials will be very useful for my future ... very open to questions"

2000 – Students made the following comments: "He did a lot of experiments which really helped ... the material is very interesting and cutting edge ... clear presentations ... good in-class demonstrations ... very clear lectures ... the material really does challenge you ... takes the time to answer your questions ... very interesting material ... relevant to today's world of communication ... the field trip was fun ... in-class demonstrations really added to class ... good understanding of course material ... excellent details, willing to help, good explanations ... in-depth details on quantum mechanics ... the instructor was extremely accessible to students ... he encouraged participation in class ... he gave intuitive arguments and explained concepts in a very physical way ... I very much enjoyed Professor Schubert and would like to take more classes with him ... material was very beautiful ... I *very much* enjoyed the papers that were discussed ... everything is well organized ... hand-out material is very complete and clear ... lectures are clear ... the professor prepared an excellent manuscript ... explained things very clearly ... he has strong enthusiasm to solve students' questions ... it's a very important course ... Professor follows the course notes exactly, so one can concentrate on material without having to focus on details ... clearly presented material ... the course is great preparation for future courses in solid-state physics ... I greatly admire Professor Schubert ..."

2001 – Students made the following comments: "He has a thorough understanding of the subject ... I like the fact that he shows us examples in class demonstrations ... the manuscript was good ... instructor provides good notes ... materials are presented clearly ... in this course you learn a lot ... very illustrative and in depth ... very interesting course ... Professor presented the material well ... Professor seemed to have a strong grasp on what he was teaching ... the basics were presented correctly ... smooth transition into more complex materials ... presented basics well ... Professor's strong points are knowledge, organization and class materials ... clear conception ... very important and useful class ... Professor knew what was going on ... manuscript and his notes were very helpful ... responded to suggestions ... notes were comprehensive ... just fine ... manuscript was good ... knows the material very well ... notes handed out are good ... expert knowledge of material ... developed lectures logically and straightforward ... lecture notes were prepared for us - very nice touch ... Professor has deep knowledge of the materials ... Professor is always prepared for lectures ... he emphasizes principles and the concepts ... good preparation ... good stuff and clear presentation ... good research and industry experience ... excellent handout notes and materials ... excellent teaching skills ... inspires the interest of students ... great knowledge of material ... well organized course notes ... Professor Schubert gave very clear instructions ... listening to his presentation is a true enjoyment of an excellent art of lecture style ... the manuscript has the quality of an excellent book ... the manuscript was an excellent reference source book ... the instructor was very clear and well organized and encouraged participation ... text [written by Schubert] was extremely good ... expert knowledge of materials ... class demonstrations were very beneficial ... can clearly relate complex ideas – very good ... has a high amount of patience ... excellent understanding of material ... very enthusiastic in teaching ... always available for discussion ... very knowledgeable ... I don't see any weak points ... he explains the theory very clearly ..."

2002 – Students made the following comments: "Always prepared ... presented difficult material in a manner that was easy to understand ... presented everything neatly ... very helpful and organized ... presents subjects in a very easy and friendly format ... very well qualified ... great experience ... very detailed notes ... well organized ... very useful ... very good diagrams and explanations ... he knows the material extremely well ... notes given to us

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are extremely helpful … professor was very knowledgeable … was able to answer any of our questions … very informative course … very knowledgeable and a great teacher … the instructor is enthusiastic to teach students … the instructor can explain the theory very clearly …"

2003 – Students made the following comments: "Great overall knowledge … good organization skills … demonstrations were very interesting and useful … effective instructor … handouts were extremely useful and organized … good course for completely understanding many points of fiber optics …"

2004 – SPIE short course: "Encouraged questions and handled them well … excellent short course … I really appreciated and enjoyed this course … good course – covered very broad matters … the instructor was very knowledgeable on the topic … excellent! …"; RPI Semiconductor devices and models II (ECSE 6290): Overall excellence of teacher: 4.8 out of 5.0. Student comments: "course was very well prepared … [course] was very organized … this is an excellent course … I learned a lot from this course … the course was very good … thanks Prof. Schubert for a wonderful course … it's been a great course … thank you …" RPI Microelectronics Technology (ECSE 2210): Overall excellence of teacher: 4.7 (average 4.2). Overall excellence of course: 4.3 (average 3.9). Student comments: "Understandable presentation … great job [of] Prof. Schubert … very nicely done class … very helpful throughout the entire course … provided timely explanations to complicated material … very informative … course was fun and interesting … very interesting lecturer … very down to earth and easy to ask for help … [instructor] did a good job in presenting [material] … good course … fun course … excellent instructor … he is a great guy and very knowledgeable … I would definitely take a class from him again" **Book review** by Neal Oldham (San Jose, CA, USA) on "Doping in III–V semiconductors" (E. F. Schubert, Cambridge University Press, Cambridge UK, 1993) on amazon.com (May 17, 2002): "[This is the] best book I've encountered in the semiconductor field. This is, no question, the best book that I've encountered in the entire field of semiconductor physics. It is expertly organized and indexed, easy to follow, complete in its treatment of electrical and materials-science aspects of III-V semiconductor production and measurement, well-written ... worth every penny if you even have the most remote interest in the subject." **Book review** by Debdeep Jena (Santa Barbara, CA, United States) on "Doping in III–V semiconductors" (E. F. Schubert, Cambridge University Press, Cambridge UK, 1993) on amazon.com (July 6, 2001): "Very useful text for semiconductor crystal growers. Doping is a big, big issue in semiconductors; this text does appreciable justice in its treatment of the issue. In addition, Schubert treats heterostructure physics appreciably well (in fact better than many textbooks on semiconductor physics!). Perusal of this book has proved very rewarding for me, and I expect it will do the same wonder for you too."

2005 – SPIE Photonics West short course student comments: "Very good instructor! … very knowledgeable … clear on complex subjects … good job fielding questions … (numerical score 4.3 out of 5.0). Educational materials on the web: … I have greatly enjoyed your LED slideshow. CLEO short course: … very good and well-organized course!" ECSE 6968: "Class presentations were very helpful in learning … very useful in learning *the details* of fundamental concepts … the course is very good … the course is excellent for engineers … your […] treatment brought about a much better understanding … examples were great and helpful … [discussion of] history and photons […] helped increase interest … After your course now, I can actually approach a quantum mechanics text book without fear … overall, I just wanted to say – *thank you* … excellent course … the instructor made it interesting and taught very effectively … the manuscript provided was also very well written … class was excellently structured … will benefit my studies in the future … especially liked the term paper requirement … Prof. Schubert is an excellent instructor, who is well prepared …" (excellence of instructor: 4.8 out of 5.0). SPIE Photonics North short course: "Very good and clear in presentation …" (numerical score 4.4 out of 5.0). ECSE 6960 mid-course and final feedback by students: "Professor has provided all course materials … I really appreciate it … well presented … technical support was great … my learning experience has been good … responses to my homework questions have been very timely … I have enjoyed the course and found it interesting and useful … homework assignments have been extremely beneficial … the set of notes is very comprehensive … good class structure …" (numerical scores of students' course and instructor evaluation: 5.0 out of 5.0). Comment on web educational materials: "Notes look very thorough and clear …"

2006 – SPIE Photonics West short course student feedback: "Excellent, knowledgeable … excellent presentation …" (numerical score 3.91 out of 5.0). ECSE 6961 (Light-emitting diodes and solid-state lighting): "excellent … Informative, comprehensive and interesting … the best part of this course, in terms of my learning experience, has been the course materials … just an outstanding class … so much is newly discovered and so much is current on-going research and commercially relevant … Dr. Schubert is obviously a leading researcher and did a great job of conveying his experience and understanding to the class … a highly technical topic that still makes a good general conversational topic … I liked the course material … I liked the fact that Prof. Schubert lectured directly from the textbook … I liked the structure of the course … I learned a lot about lasers and LEDs and other optical devices … it is a basic and fundamental class … the instructor gives ideas, concepts, and samples very clearly … very good course … students interested in LEDs and solid-state lighting are strongly recommended to take it … liked the overall coverage … the teaching pace was good … he covered a lot of material that is

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important for the subject, but it was clearly always related to the topic … the manuscript that he let us use was excellent in my opinion … the most important thing I liked about the course was the course material and the structure of the course … right amount of homework and the two exams and the term paper presentation … it was great to learn this course from someone who is a world leader in this field … well-organized material … liked the course format … organization was good … allowed me to know exactly what we were covering so I could look through the material prior to the lecture … course content was good, starting with LED basics and covering materials through modern technologies, and then a look at solid-state lighting and sort of an intro to communication devices … good fundamentals in LEDs … GREAT Professor … awesome course … informative course … ability to view course materials online was helpful … very fruitful course … covering a lot of materials … very good and very important for graduate students to take this one … for people in industry it's also useful … for the instructor, this course is thought through very clearly … the text book is also very good … great course … excellent instructor … cute instructor … course is very good … I benefited a lot from it …" (numerical scores: 4.7 out of 5.0). ECSE 2210 (Microelectronics Technology) student comments "Excellent teaching method … I like that the Professor asks random questions at the end of class – it helped me understand the subject better … I thought Prof. Schubert was fabulous … his organization of the class encouraged learning … I highly recommend this class to everyone … a devoted and involved teacher … displayed more enthusiasm in teaching than other Professors I had … he also seemed to have a philosophy about teaching that was beyond helping students get good grades … he emphasized real-world applications of material and had general advice about working in the real world after leaving academia … helpful … although he was harder in grading and exams, Prof. Schubert challenged us more and made the course more interesting … the many class activities provide lots of practice of materials just learned … provided good back-up information … made sure students understand concepts …thank you for asking students questions during class to reinforce concepts … thank you for allowing open book exams …" (numerical scores: excellence of teacher 4.4 out of 5.0; excellence of course 4.3 out of 5.0; overall average of ratings 4.4 out of 5.0)

2007 – Book review by Steven J. Wojtczuk (Lexington, MA, USA) on "Light-Emitting Diodes" (E.F. Schubert, Cambridge University Press, Cambridge UK, 2003) on amazon.com (March 14, 2006): "Schubert (RPI) has written an excellent book on LEDs that manages to explain and derive simple quantitative models for many phenomena of current interest … many monographs are a compendium of results in the field with hundreds of references … in contrast, Schubert, while giving copious references, is the sole author, leading to a coherent presentation well suited to learning … there are plentiful and good figures and drawings, as well as many exercises and solutions integrated into the text …" SPIE photonics West Short Course: "Excellent talk …" ECSE 2210 (Microelectronics Technology) "Thank you … great course … excellent instructor … interesting course … appreciated that you did not lecture completely from the slides and that you probed the class to ensure that we were understanding the key points … course is fine … good professor … Professor Schubert is one of the best lecturers I had … the pace at which he moves the topic, the way he explains things, and the manner in which he asks students questions all came together to help me learn much more form his lectures than I could on my own … instructors are absolutely very intelligent … Professor Schubert was a good professor … I actually learned things when Professor Schubert taught …" ECSE 6968 (Physical Foundations of Solid-State Devices) "The instructor explained every concept in a very simple and effective manner … I really enjoyed taking this course …" (numerical scores: 4.5 out of 5.0)

2008 – SPIE Photonics West short course feedback: "Very good … clear … very nice … answered questions readily …" (numerical score 4.3 out of 5.0) … ECSE 6961 (Light-emitting diodes and solid-state lighting) feedback: "It was great for me to have the opportunities to take two consecutive classes, *Physical Foundation* and *LEDs*, from you … both these classes have taught me a lot … they were very well organized … thank you for all the help … I have really enjoyed your classes … relevant material … very good professor …" (numerical scores: 4.3 out of 5.0) … Internet educational materials feedback: "I recently came across your course notes while trying to get a basic understanding about semiconductors and I wanted to thank you. Your notes for course "ECSE-2210 Microelectronics Technology" are the most useful and informative thing I have found on semiconductors on the Internet. I'm a chemist by trade and this is a great introduction for me …" 2007 Chautauqua Short Course and High School Teacher Summer Course, held at RPI June 26 and July 12, 2007 (numerical average of scores: 9 out of 10) … ECSE 6968 (Physical Foundations of Solid-State Devices) feedback: "Prof. Schubert is one of the best professors I've ever had … his ability to explain difficult and complex materials in a clear and concise manner is unmatched … the presentations, although time consuming, I felt were a great idea … thanks for your efforts professor! … I have really enjoyed taking this course …" By email: "Thank you professor … it has been a pleasure taking this course with you …" (numerical scores: 4.4 out of 5.0)

2009 – SPIE Photonics West short course feedback by students: "One of the best short courses I have taken … it was very nice to hear about the history of LEDs … very interesting but also very theoretical …" (numerical score 4.1 out of 5.0). ECSE 2210 (Microelectronics Technology) "Great course … instructors were excellent … encourages students to stay up to date with the subject matter … Thanks for this well-organized class … [the instructor] tries

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to get students to come out with the best grade possible … this was a good class …" ECSE 6968 (Physical Foundations of Solid-State Devices) feedback by students: "It is really an excellent course … clear hand script … great professor! …" (numerical scores: 4.7 out of 5.0)

2010 – SPIE Photonics West short course feedback by students: "Good to get the latest data and charts … very good … very broad course and well organized … it was great …" (numerical score 4.04 out of 5.0) … ECSE 6961 (Light-emitting diodes and solid-state lighting) feedback by students: "A good course … this was a wonderful course … it has given me a lot of understanding … the course has inspired me to take up LED research … useful … straight forward … very good advisor … good course …" (numerical scores: 4.3 out of 5.0) … ECSE 6220 (Physical Foundations of Solid-State Devices) feedback by students: "Overall excellent course … Professor Schubert is a good teacher … he can explain every discipline very clearly and relate them to practical applications … I like his teaching style very much … overall, it was a nice course … material explained in a clear organized manner …" (numerical scores: 4.7 out of 5.0)

2011 – SPIE Photonics West short course feedback: "Very nice overview … instructor was excellent! … very good instructor … I would recommend lengthening to 6 hours … excellent presentation, materials and text … thanks … very clear and easy to follow … to be recommended … excellent presentation … good compromise for a person with a busy schedule …" (numerical score 4.45 out of 5.0); … ECSE 2210 (Microelectronics Technology) "This was a great course … I enjoyed Professor Schubert's views … I was successful … this course was taught very well … this subject I now find quite interesting and am no longer intimidated by it … I liked the material of this course … thank you …" (numerical scores: 3.3 out of 5.0); Feedback on book *Light-Emitting Diodes*: "I am a graduate student from National Chiao Tung University, Taiwan … your wonderful book *Light-Emitting Diodes*, both first- and second-edition, gave me a lot of information and help … I would like to ask when can the third of the masterpiece be published? I wish I can get it as soon as possible and study more about the lighting devices; Feedback on Internet pages: I found your website and information […] quite enlightening and provides a great start … I simply wish to quickly express my thanks and gratitude." Feedback on book *Physical Foundations of Solid-State Devices*: "Dear Prof. Schubert, I have read your book Physical Foundations of Solid-State Devices and I must say it is amazing the explanations are really good and I am most thankful that you have decided to put the book online thank you." Itamar Jade Balla, The Israel Institute Of Technology. Feedback on book *Light-Emitting Diodes* by Trung Nguyen (San Jose, California): "It is a good book about Light Emitting Diodes (LEDs). It provides very good info and it is a good reference for engineers who work in the LED field"; … ECSE 6220 (Physical Foundations of Solid-State Devices) feedback: "Amazing course … great instructor … very good course … The text and lectures were very useful and informative … I definitely learned a lot from taking this course … I liked the course materials! …" (numerical scores: 4.6 out of 5.0)

2012 – Feedback on Internet-based materials: "I'm Cheng Liu [Wuhan National Laboratory for Optoelectronics, China], currently a graduate student major in Physical Electronics … I deeply admire your profound knowledge on this field and your unselfish sharing of it …"; … SPIE Photonics West short course feedback: "Dr. Schubert was very clear and very patient with people who had questions … the materials were comprehensive …"; Feedback on Internet-based materials: "Supremely-rich course contents posted on your website. Thank you very much for showing such awesome materials for the world to see …" (Prof. Natee Tangtrakarn, Thailand) … ECSE 6962 (Light-Emitting Diodes and Solid-State Lighting) feedback: "… very interesting course … Professor Schubert did a great job explaining the material … his textbook is very clear and understandable … nice course … I learned a lot of new things by taking it …" (numerical scores: 4.7 out of 5.0)

2013 – ***SPIE Photonics West short course*** feedback (SC-052, Light-Emitting Diodes): "Great instructor with admirable combination of knowledge in academic and commercial knowledge … I appreciated the depth of his knowledge and experience … the length of the course was good … Overall this was an excellent course … Thank you … course is very easy and I understand it easily … Excellent course! … Instructor was fantastic -- clear, explicit, took questions as we went and answered well … One of the best SPIE courses I've taken (and I've taken lots)! … Great course -- thanks! … I was happy that the slides were updated with 2012 data". ***RPI course numerical scores (ECSE-6962, Light-Emitting Diodes and Solid-State Lighting)***: Numerical score of students' evaluations: 4.67 out of 5.0; Verbatim comments: "The course is pretty good … needs no improvement … I can appreciate the more wide-angle approach from the course … These areas are very important and previously I had no knowledge of them … It was a pleasure attending your class …" ***RPI course numerical scores (ECSE-6968, Physical Foundations of Solid-State Devices)***; Verbatim comments: "It has been an awesome experience of learning for me in this course ... Thank you for everything ... Thank you for the great semester ... Have a good break ... Thank you for the great semester ... Have a good break ... Professor, thank you for an engaging and interesting class this semester ... I enjoyed the subject of my paper and learned quite a bit particularly about GaN, which I had not had a chance to really do any research into before ... Very good and interactive class ... I liked the style of the class ... I thought the topics covered were very interesting ... I think I got much more out of the class this way than if we would have followed the manuscript chapter by chapter …" Numerical score of students' evaluations: 4.83 out of 5.0

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2014 – *SPIE Photonics West short course* verbatim feedback (SC-052, Light-Emitting Diodes): "Very knowledgeable instructor ... the course was packed with information ... handouts are excellent ... Excellent presentation and contents ... the color rendering section which was interesting and fun ..." Numerical score of students' evaluations: 4.36 out of 5.0; ***RPI Course ECSE-2210 Microelectronics Technology***; Verbatim comments: "Instructor is clearly very knowledgeable about the topics ... Very clear and comprehensive ... This is the best class ever ... I'm quite enjoying this course ... I don't really have any recommendations on things to change ... The homework and lectures being sent out at the beginning was very helpful ... Both the TA and the professor were able to explain things very well ... I think he is a good lecturer ... I think the homework each was very, very good at teaching me the material, and the exam was fairly graded and easy to understand ... I definitely like the professor and I would have him again ... A good class ... I enjoyed Prof. Schubert's style of teaching ... I would still recommend Prof. Schubert as a professor ... Microelectronics is a good class ... Prof. Schubert keeps it interesting though ... he's a great professor ... The two TAs are also great ..." Numerical score of students' evaluations of instructor: 4.25 out of 5.0. ***RPI Course ECSE-6220 Physical Foundations of Solid-State Devices***; Verbatim comments: "The book and lectures seem to be entirely in sync with one another ... it really enforces the material covered in the book ... the material is covered thoroughly and improves students' understanding of quantum physics ... The class was interesting with excellent learning materials ... I loved how the course was so well organized ... The lectures were very well put together ..." Numerical score of students' evaluations of instructor: 4.75 out of 5.0.

2015 – *SPIE Photonics West Short Course SC-052 titled Light Emitting Diodes*, Verbatim comments: "I was very satisfied with this short course" Numerical score of students' evaluations: 4.53 out of 5.0; ***RPI Course ECSE-6960 Light-Emitting Diodes***; Verbatim comments: "the class has been excellent! ... I've learned a good amount about LEDs ... Also I'd like to thank you for a great semester and say that you've peaked my interest in the LED field! ... I would like to add that the course was an excellent experience for me and that I really enjoyed learning about LED technology! ... Thank you very much for teaching such a wonderful class ... It was a great learning course" Numerical score of students' evaluations: 5.0 out of 5.0. ***RPI Course ECSE-2100 Fields and Waves 1***; Verbatim comments: "This class is going perfectly and I love the way it's run ... The material is great and understandable ... the pace is perfect ... I like the pacing of the course and the fact that we spend time really developing an understanding of the theory and concepts that we will be using ... I like the Professor ... The lectures are great ... I really enjoy this professor and he is very understanding of the students' levels of learning and focused on that ... Professor Schubert is clear and easy to understand ... Overall a very good professor ... very knowledgeable and helpful ... I thought the professor was very knowledgeable and was an excellent instructor ..." Numerical score of students' evaluations of instructor: 4.17 out of 5.0.

2016 – *SPIE Photonics West Short Course SC-052 titled Light Emitting Diodes*, Verbatim comments: "This has been my favorite course (over 3 years) ... Well-structured presentation, and well given ... I was surprised by how much I didn't know. I learned a lot ... Explained difficult concepts in a clear and simple manner ... Able to go "off script" to clarify during questions." Numerical score of students' evaluations: 4.56 out of 5.0; ***RPI Course ECSE-2100 Fields and Waves 1***; Verbatim comments: "This is cool material ... This class was one of the most well put together I have ever taken in terms of lecture pace, lecture clarity, TA support, and quality of teaching and communication ... The lectures never felt too long or too short, the pace was good, I never felt lost or without an option to turn for help ... The homework was neither too long nor too short, and was well balanced with conceptual and quantitative questions ... Prof. Schubert's lecture style was very clear, concise, and to the point, with many useful examples in real life scenarios which made the material more interesting ... Very well done ... Great class ... I liked the pace of the class ... it helps with understanding the material a lot ... The labs [...] were fun and very educational ... Overall, I learned a lot from this course ... The speed of the class is perfect ... I really got a chance to learn ... This professor is very good ... Also, [in] the lab section I was able to really break down what I learned in class ... Schubert has the neatest handwriting of any professor I've ever had in my 3 years here ... His diagrams are extremely neat and he is easy to understand verbally too ... Lots of conceptual knowledge covered ... Overall [...] it was an enjoyable class ..." Numerical score of students' evaluations: 5.0 out of 5.0. ***RPI Course ECSE-2210 Microelectronics Technology***; Verbatim comments: "So far, this has been one of my favorite courses at RPI ... I'm a huge fan of Prof. Schubert's ability to clearly describe concepts both conceptually and mathematically ... Class activities [...] were really helpful! ... Otherwise the class is great! ... Prof Schubert knows his stuff ... Best professor I have had ... This course was well taught ... Professor Schubert's explanations were very clear and understandable ... he took time to address student questions with in-depth answers ... I feel as though I gained a lot from this course, especially with regards to explanations of why certain things in ECSE-2050 (Intro to Electronics) occur the way they do like where the diode property comes from and how material properties of electronic components give rise to the very real circuit characteristics we see in ECSE-2050 labs ... In this sense, Microelectronics Tech is a very good companion class to Intro to Electronics, and I highly recommend future students take them at the same time ... this was a quite good class ... Best MET instructor ... I was so actively engaged during the lectures that it was kind of scary ... The lecture notes and lectures were mostly great ... The material covered in it was succinct and interesting,

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yet still covered the knowledge needed to tackle engineering problems in semiconductors …" Numerical score of students' evaluations: 4.64 out of 5.0.

2017 – *RPI Course ECSE-2100 Fields and Waves 1*; Verbatim comments: "I thoroughly enjoy this class … Schubert is awesome! … Enjoyed the class … He is a good teacher … Most teachers talk really fast making it hard to follow … Schubert talks slow and explains things really well … Professor Schubert is an excellent professor, and has been one of my favorites at RPI so far … He made a difficult topic approachable, interesting and understandable … I hope I have him as a professor in the future … Thank you … I enjoyed this class, especially the labs … Lectures were good too … great class! … The professor does a great job of engaging the students by asking questions and making students ask questions to make them think about the labs … This course is overall excellent in that the professor does know the pace of class and gives feedback appropriately …"; Numerical score of students' evaluations: 4.63 out of 5.0. ***SPIE Photonics West Short Course SC-052 titled Light Emitting Diodes***, Verbatim comments: "the course covered a wide variety of concepts …" Numerical score of students' evaluations: 4.03 out of 5.0.

2018 – *RPI Course ECSE-2100 Fields and Waves 1*; Verbatim comments: "Professor Schubert is great and very entertaining to listen to in the lab and in lecture … Really appreciate how Prof. Schubert structures lectures … Schubert is great! … The professor is excellent at relaying concepts … This course is very interesting and it goes at a good pace … One of the better professors here at RPI … He cares about his students and helps them to learn the most through lectures and labs … Fantastic course that goes into great detail into not only knowing the material but also understanding the material … [the course] has been clarified and allowed for a greater learning process." Numerical score of students' evaluations of instructor: 4.17 out of 5.0. ***RPI Course ECSE-6220 Physical Foundations of Solid-State Devices***; Verbatim comments: "Perfect professor, no complaints." Numerical score of students' evaluations (median): 5.0 out of 5.0.

2019 – *RPI Course ECSE-2100 Fields and Waves 1*; Verbatim comments by students: "Schubert is excellent in relating information in a practical manner especially in the lab … Overall, both the professor and TAs prioritize if students understand material over semantics in reports and homework, which is really helping me in the course, and feedback given is incredibly helpful in both … Schubert is a mystery. He speaks very slowly and clearly, but you somehow learn everything at a very fast rate … Class […] being just the right amount focused and adequately paced … Overall great class … Labs were educational and we were allowed to have fun with it … Otherwise great lectures, notes were available and understandable … this was one of my favorite classes … Very well run by Schubert … lectures were informative and easy … labs were fun … The TA's were allowed to have personalities and interact with the students … 10/10 would take again … Schubert was okay … The best parts about the course for me were everything was online and I could copy the notes at my leisure with my busy schedule … I also liked that exams were open book and we had a lot of opportunities for practice … I have nothing but good things to say about both TAs and Professor Schubert – this has been my favorite class this semester … Though challenging, I have found the course material very interesting and all teachers have been excellent … Course was good … I like Professor Schubert's class notes online. They're super well written and helpful." Numerical score of students' evaluations of instructor: 4.63 out of 5.0 (average) and 5.0 out of 5.0 (median).

2019 – *RPI Course ECSE-6280 Light Emitting Diodes*; Verbatim comments by students: "This was a great course … I learned a lot during the semester … Great class … Really enjoyed Professor Schubert's expertise on the subject … Gives both in-depth technical knowledge as well as high level background to better understand the driving factors of the LED industry … Would highly recommend it to anyone in ECSE." Numerical score of students' evaluations: 4.83 out of 5.0 (average) 5.0 out of 5.0 (median).

2020 – *RPI Course ECSE-2100 Fields and Waves 1*; Verbatim comments by students: "I really enjoyed this class … the cool labs with good help and good lectures made me really enjoy this class and help the information stick in my head better … The labs provided a great use to show theory in practice and how certain concepts are applied to real-life applications … The laboratory session was also a great time to ask questions and have in-depth talks about the material … I would have already commended this professor for class organization and material availability prior to online courses (course material easily available, organized well, and easy to understand; interactive lectures; interactive labs better than most other ECSE courses), Prof. Schubert handled the change to online coursework best of all of my professors and maintained the quality of lecture almost perfectly … The 'live' online classes were interactive and courteous by students and the professor, organized, and just as in-depth as before, even including miniature homemade demonstrations and experiments … The course was taught very fundamentally which allowed me to think and learn more … Thank you, Professor Schubert … I really missed your live lectures and labs! … Professor Schubert made the best of the situation of online learning … Great class … I learn a lot from this class … I enjoy lab sessions and try never to miss any class … Prof. Schubert is really good!" Numerical score of students' evaluations: 4.75 out of 5.0 (average) 5.0 out of 5.0 (median).

2020 – *RPI Course ECSE-2050 Introduction to Electronics*; Verbatim comments by students: "I really enjoyed how easy it was to follow along with the lecture … I really enjoyed the content of this course, and I feel that the

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applications of this content in the lab were extremely effective to help students understand the content ... the concepts in general were extremely interesting … I liked how the lecture sessions for this class provided much more room for discussion and examples than nearly any other ECSE course I have taken at RPI so far … Schubert was very aware of the students ability to fully comprehend the topic ... He was very patient with the students that needed extra explaining … I learned a lot about the course material … I liked the one-on-one attention we received in the in-person lab … I enjoyed the in person laboratory sessions, they were a good place to get all my questions answered … I really like the lecture notes and the detailed diagrams / graphs that help explain the concepts … Professor Schubert does a great job of breaking down the material, he always tries to engage the students in every lecture … Very clear notes, responded quickly, answered any confusing questions really well, and very nice and accommodating towards the current COVID situation everyone is going through … He had very organized notes that helped especially with the difficulties of online learning … I loved the explanation of diodes, it's never been so clear to me before! … Examples were excellent … The course was great! … I learned a lot and this course stimulated my interest … Very engaging … stimulates participation … Professor Schubert was a refreshing exception … the professor was very knowledgeable in the subject area … explanations were clear and easy to understand … I really like the format of this class compared to my other classes … I really enjoyed the format … Very detailed lecture, very helpful with students, made very complex material easy to understand … Prof is really understanding and cares about his students ... He is really willing to work with us which I found is really rare at RPI ... He is easily one of the best professors I have had … He cares most about whether we are learning and understanding, rather than following his desired schedule perfectly ... Cannot say anything bad about Prof Schubert … Class is great" Overall instructor rating: 4 out of 5. Overall course rating: 4 out of 5.

2021 – ***RPI Course ECSE-2050 Introduction to Electronics***; Verbatim comments by students: "Class has been going smoothly … Professor Schubert includes real world-examples of devices in his lectures, showing the importance of our course materials … He is always very considerate of students, trying to adapt to what would help people most … He engages students in lectures." Overall instructor rating: 4.8 out of 5.0. Overall course rating: 4.6 out of 5.0.

2021 – ***RPI Course ECSE-2050 Introduction to Electronics***; Verbatim comments by students: "Professor is always able to conceptually answer our questions, and run through circuit analysis with us if the results we're measuring don't match up … I tried taking this class once before, and I failed it. This time around, I feel like I know everything about everything. I had never imagined just what a difference teaching style could make in my ability to learn information, but this class is so much more welcoming to me this time around. It was with a different professor the first time. I much prefer Professor Schubert and the way he conveys information so effortlessly. He also seems like he's passionate about teaching the information and his handwritten notes are astonishingly detailed … Great professor! I appreciate Professor Schubert taking the time to clarify different topics and always checking in with the students. He seems to genuinely care about our education. He is strict about deadlines, more so than other professors at least, but I think he has earned that … Professor Schubert is very friendly to his students … He was very helpful and one of the few professors who actually stays and talks to students all throughout the lab period. It was very helpful because often I would think that I fully understood a concept and then he would ask a question that would either stump me or reinforce information. Additionally he kept lectures short and to-the-point, which I appreciate." Overall instructor rating: 4.3 out of 5.0. Overall course rating: 4.3 out of 5.0.

2022 – ***RPI Course ECSE-2050 Introduction to Electronics***; Verbatim comments by students: "Great professor! … Handwriting is amazing … His notes are flawless and easy to understand … This course covers much more than most other EE courses I've taken, and yet I feel as though this has been the easiest EE course due to his teaching abilities … Professor Schubert is a very knowledgeable professor … It's clear that he wants his students to learn …" Overall instructor rating: 4.3 out of 5.0. Overall course rating: 4.4 out of 5.0.

2022 – ***RPI Course ECSE-2210 Microelectronics Technology***; Verbatim comments by students: "I think Schubert does a great job of teaching … He makes the pn junctions as interesting as he can … I also love the chalk-board! So great, every professor should be forced to use it, because you can follow the work so smoothly (not like powerpoints) … I would not change the class … I also like how Prof. Schubert asks for feedback from everyone after class … Course was at a great pace and the level of difficulty … Professor Fred Schubert is one of my most favorite professors at RPI … I am sad to see in the course schedule for Spring 2023 that he is not teaching any 4000 level ECSE courses … I think that the department and students are missing out by not having someone as knowledgeable as him teaching more conceptually hard topics because Professor Schubert does that exceptionally … Best ever lecture experience, clear structure of lecture notes, comprehensive homework that helps to improve students' understandings, and always eager to solve students' questions … Thanks for another great course Professor!"

2024 – ***RPI Course ECSE-2050 Introduction to Electronics***; Verbatim comments by students: "... It's great to learn how a component works and learn "Iconic Circuits" that use those components … I really appreciated the

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Homeworks, they were well thought out and helped me understand the content ... I liked the open notes exams, they allowed me to use the notes I took in class and demonstrate how I can apply the concepts we learned in class to a different problem ... I appreciated [Professor Schubert] talking to everyone in [the] lab one-on-one ... I also liked that he showed interest in all the students and answered our questions promptly and thoroughly ... Very nice and understanding professor, one of the best in the ECSE department ... Professor Schubert seems to know what he is talking about ... Professor Schubert is very nice and during labs walks around and asks students questions making sure we understand the concepts ... He also introduced some applications not taught in the previous versions of the course and even added a lecture on class-D amplifiers to attempt to keep the course up with modern technology ... The last few lectures left a good impression though and were extremely engaging ..."

2024 – ***RPI Course ECSE-2210 Microelectronics Technology***; Verbatim comments by students: "... Professor Schubert is very passionate about his subject and that passion rubs off on his students ... The professor was truly excellent and I enjoyed attending his lectures twice a week ... He was very good at teaching. ..."

Post-doctoral & visiting personnel for which I served as Major Research Advisor

Dr. Li-Wei Tu	Post-Doctoral Fellow	1988–1990
Dr. Neil Hunt	Post-Doctoral Fellow	1991–1993
Dr. Matthias Passlack	Post-Doctoral Fellow	1993–1995
Dr. Wolf Grieshaber	Post-Doctoral Fellow	1995–1997
Dr. Thomas Gessmann	Post-Doctoral Fellow	2000–2002
Dr. Jong Kyu Kim	Post-Doctoral Fellow	2003–2005
Dr. Min Ho Kim, SEMCo	Visiting Engineer	2007–2008
Prof. Ji-Myon Lee, Sunchon Univ.	Visiting Professor	2007–2008
Dr. Jaehee Cho	Post-Doctoral Fellow	2008–2009
Dr. Yongjo Park, Samsung LED	Visiting Vice President	2010–2012
Dr. Yangang Andrew Xi	Visiting Scientist	2013–2014
Dr. Guan-Bo Lin	Post-Doctoral Fellow	2014–2015

Graduate students for which I served as Major Research Advisor

Dr. Dean A. Stocker	Ph.D. Dissertation	Ph. D. completed in 1999
Xiaoyun (Jane) Guo	Master Thesis	M.S.E.E. completed in 1999
John W. Graff	Master Thesis	M.S.E.E. completed in 1999
Dr. Ian D. Goepfert	Ph.D. Dissertation	Ph. D. completed in 2000
Yun-Li Li	Master Thesis	M.S.E.E. completed in 2000
Dr. Xiaoyun (Jane) Guo	Ph.D. Dissertation	Ph. D. completed in 2001
Dr. John W. Graff	Ph.D. Dissertation	Ph. D. completed in 2002
Dr. Erik L. Waldron	Ph.D. Dissertation	Ph. D. completed in 2002
Jay M. Shah	Master Thesis	M.S.E.E. completed in 2002
Dr. Yun-Li Li	Ph.D. Dissertation	Ph. D. completed in 2003
Jingqun ("JQ") Xi	Master Thesis	M.S. completed in 2003
Yangang Andrew Xi	Master Thesis	M.S. completed in 2003
Ronald Jackson	Master Thesis	M.S. completed in 2004
Sameer Chhajed	Master Thesis	M.S. completed in 2004
Hong Luo	Master Thesis	M.S. completed in 2005
Xiaolu Li	Master Thesis	M.S. completed in 2005
Kaixuan Chen	Master Thesis	M.S. completed in 2005
Dr. Jay M. Shah	Ph.D. Dissertation	Ph. D. completed in 2006
Frank Mont	Master Thesis	M.S.E.E. completed in 2006
Dr. Hong Luo	Ph.D. Dissertation	Ph. D. completed in 2006
Dr. Jingqun ("JQ") Xi	Ph.D. Dissertation	Ph. D. completed in 2006
Dr. Yangang Andrew Xi	Ph.D. Dissertation	Ph. D. completed in 2006
Won Seok Lee	Master Thesis	M.S. completed in 2007
Qi Dai	Master Thesis	M.S. completed in 2007
Di Zhu	Master Thesis	M.S. completed in 2007

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Jiuru Xu	Master Thesis	M.S. completed in 2007
Ahmed Noemaun	Master Thesis	M.S. completed in 2007
Roya Mirhosseini	Master Thesis	M.S. completed in 2008
David Poxson	Master Thesis	M.S. completed in 2008
Qifeng Shan	Master Thesis	M.S. completed in 2009
Ming Ma	Master Thesis	M.S. completed in 2010
Xing Yan	Master Thesis	M.S. completed in 2010
Dr. Roya Mirhosseini	Ph.D. Dissertation	Ph. D. completed in 2010
Dr. Sameer Chhajed	Ph.D. Dissertation	Ph. D. completed in 2010
Dr. Jiuru Xu	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Frank Mont	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Wonseok Lee	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Di Zhu	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Qi Dai	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Ahmed Noemaun	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. David Poxson	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Qifeng Shan	Ph.D. Dissertation	Ph. D. completed in 2012
Dr. Ann Mao	Ph.D. Dissertation	Ph. D. completed in 2013
Dr. Xing Yan	Ph.D. Dissertation	Ph. D. completed in 2013
Dr. Ming Ma	Ph.D. Dissertation	Ph. D. completed in 2013
Dr. David Meyaard	Ph.D. Dissertation	Ph. D. completed in 2013
Dr. Guan-Bo Lin	Ph.D. Dissertation	Ph. D. completed in 2013

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Expert Witness Consulting Service

1997 ***Case***: Hewlett-Packard Company versus CEO of United Epitaxy Company (Taiwan)
Nature: Trade secret misappropriation
Venue: U.S. District Court.
Law firm: Morrison & Foerster LLP, Washington DC.
Role: I served as technical expert witness on behalf of United Epitaxy (Defendant). I wrote one or more expert reports.

1998 ***Case***: Hewlett-Packard Company versus United Epitaxy Company (Taiwan)
Nature: Patent infringement.
Venue: U.S. District Court for the Northern District of California.
Law firm: Quinn Emanuel Urquhart Oliver and Hedges LLP
Role: I served as technical expert witness on behalf of United Epitaxy (Defendant). I wrote one or more expert reports.

2006 ***Case***: Kerr Company versus 3M and Dentsply International Company.
Nature: Patent infringement.
Venue: U.S. District Court for the Western District of Wisconsin.
Law Firm: Woodcock Washburn LLP, Philadelphia, Pennsylvania.
Role: I served as technical expert witness on behalf of Dentsply (Defendant). I wrote one or more expert reports.

2006 ***Case***: Nichia Corporation (Japan) versus Seoul Semiconductor Company (Korea).
Nature: Design patent infringement.
Venue: U.S. District Court for Northern District of California, San Francisco Division.
Law firm: Foley & Lardner LLP Washington DC.
Role: I served as technical expert witness on behalf of Nichia (Plaintiff). I wrote one or more expert reports; I was deposed.

2008 ***Case***: Seoul Semiconductor (SSC) Company LTD (Korea) versus Nichia Corporation (Japan).
Nature: Patent infringement.
Venue: U.S. District Court for the Eastern District of Texas, Beaumont Division.
Law firm: Morrison & Foerster LLP, Palo Alto, California.
Role: I served as technical expert witness on behalf of Nichia (Defendant). I wrote one or more expert reports; I testified in District Court during the claim construction / Markman hearing.

2008 ***Case***: Professor Gertrude Rothschild versus Toshiba Company (Japan).
Nature: Patent infringement.
Venue: U.S. International Trade Commission (ITC), Washington DC.
Law firm: DLA Piper LLP, San Francisco California.
Role: I served as technical expert witness on behalf of Toshiba (Defendant). I wrote one or more expert reports; I was deposed.

2008 ***Case***: Honeywell Company versus Cree Company and Lumileds Company.
Nature: Patent infringement and Reexamination of patent.
Venue: U.S. District Court for the Eastern District of Texas, Marshall Division. Reexamination before the USPTO's Patent Trial and Appeal Board.
Law firms: Paul Hastings LLP, Washington DC and Ingrassia, Fisher & Lorenz PC, Washington DC.
Role: I served as technical expert witness on behalf of Honeywell (Plaintiff). I wrote one or more expert reports. I testified at the USPTO during a re-examination hearing.

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2010 ***Case***: Landmark Screens Company versus MLB Company and Kohler.
Nature: Mishandling of a patent application.
Venue: U.S. District Court for the Northern District of California, San Jose Division.
Law firm: Keker & Van Nest LLP, San Francisco, California.
Role: I served as technical expert witness on behalf of MLB and Kohler (Defendant). Negligence in conjunction with a patent application; I wrote one or more expert reports.

2011 ***Case***: Koninklijke Philips Electronics N.V. versus Seoul Semiconductor (SSC) Company LTD.
Nature: Patent infringement.
Venue: U.S. District Court for the Central District of California Southern Division
Law firm: Latham & Watkins LLP, Washington DC.
Role: I served as technical expert witness on behalf of SSC (Defendant). I wrote one or more expert reports.

2011 ***Case***: Jeou-Nan Tseng versus Home Depot USA Inc. and Guangde LEDup Enterprise Inc.
Nature: Patent infringement.
Venue: U.S. District Court for the Western District of Washington at Seattle.
Law firm: DLA Piper, Philadelphia, Pennsylvania.
Role: I served as technical expert witness on behalf of Home Depot (Defendant). I wrote one or more expert reports.

2011 ***Case***: Lightpanels Ltd. Company versus Fuzhou F&V Photographic Company.
Nature: Patent infringement.
Venue: U.S. International Trade Commission (ITC), Washington DC.
Law firm: Locke Lord LLP, New York, New York.
Role: I served as technical expert witness on behalf of Fuzhou F&V and Nanguang Photographic (Defendant). I wrote one or more expert reports; I was deposed.

2012 ***Case***: Osram Company versus LG Company.
Nature: Patent infringement.
Venue: U.S. International Trade Commission (ITC), Washington DC.
Law firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington DC.
Role: I served as technical expert witness on behalf of LG (Defendant). I wrote one or more expert reports; I was deposed; I testified at the ITC Hearing.

2012 ***Case***: Osram Company versus LG Company and Samsung Company.
Nature: Patent infringement.
Venue: U.S. International Trade Commission (ITC), Washington DC.
Law firm: Covington & Burling LLP, Washington DC.
Role: I served as technical expert witness on behalf of LG and Samsung (Defendant). I wrote one or more expert reports; I was deposed; I testified at the ITC Hearing.

2013 ***Case***: Chao Tai Electron Co. LTD. versus LEDup Enterprise Inc. and others.
Nature: Patent infringement.
Venue: U.S. District Court for the Central District of California.
Law firm: Hunton & Williams LLP, Washington DC.
Role: I served as technical expert witness on behalf of LEDup Enterprise Inc. and others (Defendants). I wrote one or more expert reports.

2013 ***Case***: Nichia Corporation versus Everlight Company and Emcore Company.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.

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Law firm: Foley & Lardner LLP, Washington DC.
Role: I served as technical expert witness on behalf of Nichia Corporation (Petitioner). I wrote one or more expert reports; I was deposed.

2014 ***Case***: Everlight Electronics Co. LTD. versus Nichia Corporation.
Nature: Patent infringement.
Venue: U.S. District Court for the Eastern District of Michigan, Southern Division.
Law firm: Foley & Lardner LLP, Washington DC.
Role: I served as technical expert witness on behalf of Nichia Corporation (Defendant). I wrote one or more expert reports; I was deposed; I testified at Phase 1 of trial (jury trial) and I testified at Phase 2 of trial (bench trial).

2014 ***Case***: LEDup Company versus Nicolas Holiday Company.
Nature: Patent infringement.
Venue: U.S. District Court for the Central District of California.
Law firm: Pendleton, Wilson, Hennessey, and Crow PC, Denver, Colorado.
Role: I served as technical expert witness on behalf of LEDup (Plaintiff). I wrote one or more expert reports.

2014 ***Case***: Nichia Corporation versus Everlight Electronics Co. LTD.
Nature: Patent infringement.
Venue: U.S. District Court for the Eastern District of Texas, Marshall Division.
Case number: 02:13-cv-702-JRG (E.D. Texas).
Law firm: Rothwell, Figg, Ernst & Manbeck PC, Washington DC.
Role: I served as technical expert witness on behalf of Nichia (Plaintiff). I wrote one or more expert reports; I was deposed; I testified at trial (bench trial).

2015 ***Case***: Cree Company versus Unity Opto, Unity Microelectronics, and Feit Electric Company
Nature: Patent infringement.
Venue: U.S. International Trade Commission (ITC), Washington DC.
Law firm: Alston & Bird LLP, Silicon Valley, East Palo Alto, California.
Role: I served as expert witness on behalf of Unity Opto Technology *et al.* (Defendants). I wrote one or more expert reports; I was deposed; I testified at trial (ITC Hearing).

2015 ***Case***: Honeywell International Inc. versus Cree Inc.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.
Law firm: Arnold & Porter LLP, San Francisco, California.
Role: I served as expert witness on behalf of Honeywell International Inc. (Plaintiff). I wrote one or more expert reports.

2015 ***Case***: Honeywell International Inc. versus Cree Inc.
Nature: Patent infringement.
Venue: U.S. District Court for the District of New Jersey.
Law firm: Arnold & Porter LLP, San Francisco, California.
Role: I served as expert witness on behalf of Honeywell International Inc. (Plaintiff).

2015 ***Case***: Cree Inc. versus Kingbright Electronic Co. LTD and SunLED Corporation.
Nature: Patent infringement.
Venue: U.S. District Court for the Western District of Wisconsin.
Law firm: Hansen Reynolds Dickinson Crueger LLC, Milwaukee, Wisconsin.
Role: I served as technical expert witness on behalf of Kingbright and SunLED (Defendants). I wrote one or more expert reports; I was deposed.

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2016 ***Case***: Acuity Brands Lighting Inc. versus Lynk Labs Inc.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.
Law firm: Haynes Boone LLP, Chicago, Illinois.
Role: I served as technical expert witness on behalf of Lynk Labs (Plaintiff). I wrote one or more expert reports.

2016 ***Case***: Godo Kaisha IP Bridge 1 Company versus Broadcom Company and others.
Nature: Patent infringement.
Venue: U.S. District Court for the Eastern District of Texas, Marshall Division.
Law firm: Ropes and Gray LLP, New York City, New York.
Role: I served as technical expert witness on behalf of IP Bridge 1 (Plaintiff). I wrote one or more expert reports; I was deposed.

2016 ***Case***: TSMC Company versus Godo Kaisha IP Bridge 1 Company.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.
Law firm: Greenblum & Bernstein, P.L.C., Reston, Virginia.
Role: I served as technical expert witness on behalf of IP Bridge (Patent Owner). I wrote one or more expert reports; I was deposed.

2017 ***Case***: Harvard University versus Micron Technology Company.
Nature: Patent infringement.
Venue: U.S. District Court for MA, Boston; U.S. District Court for Delaware, Wilmington.
Law firm: Weil Gotshal & Manges LLP, Redwood Shores, California.
Role: I served as technical expert witness on behalf of Micron Technology Company (Defendant). I wrote one or more expert reports; I was deposed.

2017 ***Case***: Seoul Viosys Company versus P3 Company.
Nature: Patent infringement.
Venue: U.S. District Court, Southern District of New York, New York City.
Law firm: Holland & Knight LLP, New York City, New York.
Role: I served as technical expert witness on behalf of Seoul Viosys (Plaintiff). I wrote one or more expert reports.

2017 ***Case***: Nitride Semiconductor Company versus Rayvio Company.
Nature: Patent infringement.
Venue: US District Court for the Northern District of California.
Law firm: Dentons LLP, Palo Alto, California.
Role: I served as technical expert witness on behalf of Rayvio (Defendant).

2018 ***Case***: CRX Tech LLC versus Samsung Electronics Co. LTD.
Nature: Patent infringement.
Venue: U.S. District Court for the Eastern District of Texas, Marshall Division.
Law firm: Arnold & Porter LLP, Los Angeles, California.
Role: I served as technical expert witness on behalf of Samsung (Defendant).

2018 ***Case***: Macom Technology Solutions Holdings Inc. versus Infineon Technologies AG.
Nature: Patent infringement.
Venue: U.S. District Court Central District of California Western Division, Los Angeles.
Law firm: Perkins Coie LLP, Denver, Colorado.

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Role: I served as technical expert witness on behalf of Macom (Plaintiff). I wrote one or more expert reports; I was deposed.

2018 ***Case***: Vizio Inc. versus Nichia Corporation.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.
Case number: Case No. IPR-2017-01608 and IPR-2017-01623 (PTAB).
Law firm: Rothwell, Figg, Ernst & Manbeck, P.C., Washington DC.
Role: I served as technical expert witness on behalf of Nichia Corporation (Patent Owner). I wrote one or more expert declarations.

2018 ***Case***: Lowe's Companies Inc. versus Nichia Corporation.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.
Case number: Case No. IPR2017-02014 (PTAB).
Law firm: Rothwell, Figg, Ernst & Manbeck, P.C., Washington DC.
Role: I served as technical expert witness on behalf of Nichia Corporation (Patent Owner). I wrote one or more expert declarations.

2018 ***Case***: Ultravision Technologies LLC versus Prismaflex USA Inc.
Nature: Patent infringement.
Venue: US International Trade Commission (ITC), Washington DC.
Case number: Investigation No. 337-TA-1114 (ITC)
Law firm: Womble Bond Dickinson LLP, Winston-Salem, NC
Role: I served as technical expert witness on behalf of Prismaflex USA (Defendant). I wrote one or more expert reports. I was deposed.

2019 ***Case***: Carl Zeiss AG versus Nikon USA Inc.
Nature: Patent infringement.
Venue: US International Trade Commission (ITC), Washington DC.
Case number: Investigation No. 337-TA-1129 (US ITC)
Law firm: Morrison & Foerster LLP, Los Angeles CA.
Role: I served as technical expert witness on behalf of Nikon USA (Defendant). I wrote one or more expert reports. I was deposed.

2019 ***Case***: ASM IP Holding B.V. versus Hitachi Kokusai Electric Inc.
Nature: Arbitration related to IP licensing dispute.
Venue: ICDR (International Center for Dispute Resolution), Palo Alto CA.
Case number: Case No. ICDR 01-17-0005-1963 (Palo Alto CA)
Law firm: Quinn Emanuel Urquhart & Sullivan LLP, San Francisco CA.
Role: I served as technical expert witness on behalf of ASM IP Holding B.V. (Complainant). I authored multiple witness statements. I testified at the Arbitration Hearing.

2019 ***Case***: Power Integrations Inc. versus C. W. Park.
Nature: Breach of employment contract.
Venue: US District Court, Northern District of California, San Jose Division.
Case number: 5:16-cv-02366-BLF (Northern District of California)
Law firm: Miclean Gleason LLP, San Mateo CA.
Role: I served as technical expert witness on behalf of Power Integrations Inc. (Complainant). I performed analyses relating to switched-mode power supplies (SMPS) including flyback transformers. The matter ended in settlement.

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2019 ***Case***: Omni MedSci Inc. versus Apple Inc.
Nature: Patent infringement.
Venue: US District Court, Eastern District of Texas, Marshall Division.
Case number: Civil Action No. 2:18-cv-134-RWS (E.D. Texas)
Law firm: Sidley Austin LLP, Washington DC.
Role: I served as technical expert witness on behalf of Apple Inc. (Defendant). I performed a non-infringement analysis relating to the heart rate monitor of the Apple Watch, authored an expert report, and testified at a deposition.

2019 ***Case***: Fluxwerx Illumination Inc., versus OKT Lighting USA LLC
Nature: Design patent infringement.
Venue: US District Court, Southern District of Texas, Houston Division.
Case number: Civil Action No. 4:19-CV-01113 (S.D. Texas)
Law firm: Burns & Levinson LLP, Boston MA.
Role: I served as technical expert witness on behalf of Fluxwerx Illumination, Inc. (Plaintiff). I performed an infringement analysis.

2020 ***Case***: Lighting Science Group Corporation versus Nichia Corporation and others
Nature: Patent infringement.
Venue: US ITC, Office for Unfair Import Investigations, Washington DC
Case number: Investigation No. 337-TA-1168
Law firm: Shearman & Sterling LLP, New York, NY.
Role: I served as technical expert witness on behalf of Nichia Corporation. I performed a non-infringement analysis, authored an expert report, was deposed, and testified at the ITC hearing as key technical witness on behalf of Nichia and Respondents (6 hours live testimony).

2020 ***Case***: Regents of the University of California versus Amazon, Walmart, Ikea, Target, and others
Nature: Patent infringement.
Venue: US ITC, Office for Unfair Import Investigations, Washington DC
Case number: Investigation No. 337-TA-1172
Law firm: Nixon Peabody LLP, Los Angeles CA.
Role: I served as technical expert witness on behalf of the Regents of the University of California. I performed an infringement analysis, authored an expert report, and was deposed.

2020 ***Case***: Samsung Electronics Company versus Acorn Technologies Company.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case numbers: IPR-2020-01183 ('261), IPR-2020-01182 ('423), IPR-2020-01204 ('336), IPR-2020-01264 ('336), IPR-2020-01205 ('167), IPR-2020-01241 ('167), IPR-2020-01206 ('691), IPR-2020-01279 ('691), IPR-2020-01207 ('395), and IPR-2020-01282 ('395)
Law firm: Desmarais LLP, New York NY.
Role: I served as technical expert witness on behalf of Samsung Electronics Company. I authored several expert declarations and was deposed multiple times.

2020 ***Case***: Satco Company versus The Regents of the University of California.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case number: IPR-2020-00579, IPR-2020-00695, IPR-2020-00780, and IPR-2020-00813.
Law firm: Nixon Peabody LLP, Los Angeles CA.
Role: I served as technical expert witness on behalf of The Regents of the University of California. I authored several expert declarations and was deposed.

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2020 ***Case***: Godo Kaisha IP Bridge 1 Company versus Micron Technology Company.
Nature: Patent infringement.
Venue: US District Court for the Western District of Texas, Waco Division.
Case number: C.A. No. 6:20-cv-178-ADA.
Law firm: Orrick Herrington & Sutcliffe LLP, Menlo Park CA.
Role: I served as technical expert witness on behalf of Micron Technology Company. I authored multiple expert reports and was deposed.

2020 ***Case***: Nichia Company versus Healthe Company and Lighting Science Group Company.
Nature: Patent infringement.
Venue: US District Court for the Middle District of Florida, Orlando Division.
Case number: 6:19-cv-1332-RBD-EJK and 6:19-cv-1333-RBD-EJK.
Law firm: Rothwell, Figg, Ernst & Manbeck, PC, Washington DC.
Role: I served as technical expert witness on behalf of Nichia Company. I authored one or more expert reports.

2020 ***Case***: Semiconductor Energy Laboratory (SEL) Co., Ltd. versus BOE Technology Group Co., Ltd.
Nature: Patent infringement.
Venue: US District Court for the Northern District of California.
Case number: 3:20-cv-04297-EMC, N.D. Cal.
Law firm: Fish and Richardson, P.C., Redwood City CA.
Role: I served as technical expert witness on behalf of SEL.

2021 ***Case***: The University of California versus General Electric, Ikea, Home Depot and others
Nature: Patent infringement.
Venue: US ITC, Office for Unfair Import Investigations, Washington DC
Case number: Investigation No. 337-TA-1220
Law firm: Nixon Peabody LLP, Los Angeles CA.
Role: I served as technical expert witness on behalf of the University of California. I performed multiple analyses, authored several expert reports, was deposed multiple times, and testified at trial.

2021 ***Case***: Tianma Microelectronics Co., Ltd. versus Japan Display Inc. (JDI)
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA
Case numbers: IPR-2021-01029, IPR-2021-01057 and IPR-2021-01058
Law firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington DC.
Role: I served as technical expert witness on behalf of Tianma. I performed multiple analyses and authored several declarations.

2021 ***Case***: Japan Display Inc. (JDI) versus Tianma Microelectronics Co., Ltd.
Nature: Patent infringement.
Venue: US District Court for the Eastern District of Texas, Marshall Division.
Case numbers: Civil Action No. 2:20-cv-00283-JRG; 2:20-cv-00284-JRG; and 2:20-cv-00285-JRG
Law firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington DC.
Role: I served as technical expert witness on behalf of Tianma. I performed multiple analyses, authored several expert reports, and was deposed multiple times.

2022 ***Case***: Satco Products Inc. versus The Regents of the University of California.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case number: IPR-2021-00662.
Law firm: Nixon Peabody LLP, Los Angeles CA.

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Role: I served as technical expert witness on behalf of The Regents of the University of California, authored one expert declaration, and was deposed.

2022 ***Case***: Samsung Electronics Co. Ltd. versus Bishop Display Tech LLC.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case numbers: IPR-2022-00500 and IPR-2022-00502.
Law firm: Baker Botts LLP, New York City NY.
Role: I served as technical expert witness on behalf of Samsung Electronics and have authored two expert declarations.

2022 ***Case***: Semiconductor Energy Laboratory (SEL) Co. Ltd. versus TCL China Star Optoelectronics Technology Co., Ltd.
Nature: Patent infringement.
Venue: US District Court for the Central District of California, Southern Division.
Case number: 8:21–cv–00554–JAK–ADS.
Law firm: Fish and Richardson, P.C., Redwood City CA.
Role: I served as technical expert witness on behalf of SEL, authored two expert reports, and was deposed.

2022 ***Case***: Nvidia Corporation versus Ocean Semiconductors LLC.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case number: IPR2022-01288.
Law firm: Sheppard Mullin LLP, Menlo Park CA.
Role: I served as technical expert witness on behalf of Nvidia and authored one expert declaration.

2022 ***Case***: Nicor, Inc. versus SourceBlue LLC and InfiniLux Corporation.
Nature: Patent infringement.
Venue: US District Court for the Central District of California.
Case number: 2:21-cv-05876-AB(PDx) (C.D. Cal.).
Law firm: Loza & Loza IP LLP, Upland CA.
Role: I served as technical expert witness on behalf of Nicor, Inc., authored three expert reports, and was deposed.

2023 ***Case***: Dr. Shimon Maimon versus Lockheed Martin Corporation.
Nature: Dispute relating to a License Agreement.
Venue: JAMS ADR (Alternative Dispute Resolution).
Case number: JAMS Ref. No. 1460005932.
Law firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington DC.
Role: I served as technical expert witness on behalf of Lockheed Martin Corporation, authored three expert reports, was deposed, and testified at the Hearing.

2023 ***Case***: Samsung Electronics Co. Ltd. versus Daedalus Prime LLC.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case number: IPR2023-00536 and IPR2023-00653.
Law firm: Fish & Richardson PC, Minneapolis MN.
Role: I served as technical expert witness on behalf of Samsung Electronics and authored two expert declarations.

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2023 ***Case***: Seoul Semiconductor Co. Ltd., et al. versus GE Healthcare Inc.
Nature: Patent infringement.
Venue: United States District Court for the District of Delaware.
Case number: Civil Action No. 1:22-cv-01455.
Law firm: Shearman & Sterling LLP, New York, NY.
Role: I served as technical expert witness on behalf of GE Healthcare.

2023 ***Case***: Efficient Power Conversion Corp. versus Innoscience (Zhuhai) Technology Company.
Nature: Patent infringement.
Venue: US International Trade Commission (ITC), Washington DC.
Case number: Investigation No. 337-TA-1366.
Law firm: Blank Rome LLP, Washington DC
Role: I served as technical expert witness on behalf of EPC, authored multiple expert reports, was deposed, and testified at the ITC Hearing.

2023 ***Case***: Innoscience (Zhuhai) Technology Company versus Efficient Power Conversion Corp.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case number: IPR2023-01381, IPR2023-01382, IPR2023-01383, and IPR2023-01384.
Law firm: Blank Rome LLP, Washington DC.
Role: I served as technical expert witness on behalf of Efficient Power Conversion Corp. and authored multiple expert declarations.

2023 ***Case***: Xu Peicheng (Hong Kong) Optoelectronic Technol. Co. versus SemiSilicon Technol. Corp.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case number: IPR2024-00156 and IPR2024-00157 (US Patent 8,124,988 and US 8,884,546)
Law firm: Rimon Law PC, McLean VA.
Role: I served as technical expert witness on behalf of Xu Peicheng and authored two expert declarations.

2024 ***Case***: Seasonal Specialties, LLC versus LEDUP Manufacturing Group LTD.
Nature: Patent infringement.
Venue: US District Court, Central District of California, Western Division.
Case number: 2:23-cv-06318-SB-AS.
Law firm: Fairfield & Woods PC, Denver CO.
Role: I served as technical expert witness on behalf of LEDUP Manufacturing Group and composed multiple Invalidity Claim Charts.

2024 ***Case***: Wuxi Autowell Technology Co. Ltd. versus Teamtechnik Maschinen und Anlagen GmbH.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case number: US patent numbers 8,247,681 and 8,253,009.
Law firm: Novick, Kim & Lee, PLLC, (NKL Law), Fairfax VA.
Role: I served as technical expert witness on behalf of Wuxi Autowell Technology and composed one expert declaration.

2024 ***Case***: Greenthread LLC versus Omnivision Technologies, Inc., and Texas Instruments, Inc.
Nature: Patent infringement.
Venue: US District Court, Eastern District of Texas, Marshall Division.
Case numbers: 2:23-cv-00212-JRG and 2:23-cv-00157-JRG.
Law firms: Benesch Friedlander Coplan & Aronoff LLP and Caldwell Cassady & Curry PC.
Role: I served as technical expert witness on behalf of Omnivision Technologies and Texas

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Instruments, composed one expert declaration, and was deposed.

2024 ***Case***: Lian Li Industrial Co. Ltd. and CHEN, Chien-Hao versus Thermaltake Technology Co. Ltd.
Nature: Patent infringement.
Venue: US District Court, Central District of California.
Case numbers: 2:23-cv-07470.
Law firm: The Gikkas Law Firm, PC, Palo Alto CA
Role: I served as technical expert witness on behalf of Thermaltake Technology, composed one expert declaration, and was deposed.

2024 ***Case***: Pictive Displays International Ltd. versus Samsung Electronics Co. Ltd.
Nature: Patent infringement.
Venue: US District Court, Eastern District of Texas, Marshall Division.
Case numbers: 2:23-cv-00495-JRG.
Law firm: Quinn Eammanual Urquhart & Sullivan LLP, Seattle WA.
Role: I served as technical expert witness on behalf of Samsung Electronics Co., composed one expert declaration, and was deposed.

2024 ***Case***: Feit Electric Company versus Savant Technologies and additional parties
Nature: Patent infringement.
Venue: US District Court, Northern District of Ohio and additional venues.
Case numbers: 1:24-cv-473.
Law firm: Benesch, Friedlander, Coplan & Aronoff LLP, Chicago ILL.
Role: I served as technical expert witness on behalf of Feit Electric Company, composed one or more expert declarations, and was deposed.

2024 ***Case***: Savant Technologies LLC and LEDvance LLC versus Feit Electric Company.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case number: US patent number 8,604,678. IPR2024-01357.
Law firm: Novick, Kim & Lee, PLLC, (NKL Law), Fairfax VA.
Role: I served as technical expert witness on behalf of Feit Electric Company and composed one expert declaration.

2024 ***Case***: Longitude Licensing Limited and 138 East LCD Advancements Ltd. versus BOE Technology Group Co., Ltd.
Nature: Patent infringement.
Venue: US District Court, Eastern District of Texas, Marshall Division.
Case numbers: 2:23-cv-515-JRG-RSP.
Law firm: Robins Kaplan LLP Law Firm, Minneapolis MN.
Role: I served as technical expert witness on behalf of Longitude Licensing Limited and 138 East LCD Advancements Ltd. and composed one or more expert declarations.

2024 ***Case***: BOE Technology Group Co., Ltd. versus 138 East LCD Advancements Ltd.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case number: IPR2024-00973, IPR2024-00977, and IPR2024-00977.
Law firm: Robins Kaplan LLP Law Firm, Minneapolis MN.
Role: I served as technical expert witness on behalf of 138 East LCD Advancements Ltd. and composed multiple expert declarations.

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United States Patents

1. A. Fischer, Y. Horikoshi, K. Ploog, and E. F. Schubert "Semiconductor devices with at least one monoatomic layer of doping atoms" European Patent No. 0183 146 A2; US Patent No. 4,882,609; issued on November 15 (1985)
2. J. E. Cunningham, E. F. Schubert, and W. T. Tsang "Delta doped ohmic metal to semiconductor contacts" US Patent No. 4,772,934; issued on September 20 (1988)
3. J. E. Cunningham, E. F. Schubert, and W. T. Tsang "Field-effect transistor having a delta-doped ohmic contact" US Patent No. 4,780,748; issued on October 25 (1988)
4. J. E. Cunningham, E. F. Schubert, and W. T. Tsang "Method for fabricating a field-effect transistor with a self-aligned gate" US Patent No. 4,784,967; issued on November 15 (1988)
5. E. Fred Schubert "Optical communications modulator device" US Patent No. 4,929,064; filed on July 21 (1988) issued on May 29 (1990)
6. J. E. Cunningham, A. M. Glass, and E. F. Schubert "Devices having asymmetric delta-doping" US Patent No. 4,974,044; issued on November 27 (1990)
7. J. E. Cunningham, A. M. Glass, and E. F. Schubert "Devices having asymmetric delta-doping" US Patent No. 5,031,012; issued on July 9 (1991)
8. J. E. Cunningham, T. D. Harris, E. F. Schubert, and J. P. van der Ziel "Optical system including wavelength tunable semiconductor laser" US Patent No. 4,980,892; issued on December 25 (1990)
9. R. F. Kopf, J. M. Kuo, H. S. Luftman, and E. F. Schubert "Doping procedures for semiconductor devices" US Patent No. 5,024,967; issued on June 18 (1991)
10. D. G. Deppe, R. D. Dupuis, and E. F. Schubert "Vertical cavity semiconductor lasers" US Patent No. 5,018,157; issued on May 21 (1991)
11. D. G. Deppe, L. C. Feldman, R. F. Kopf, E. F. Schubert, L.-W. Tu, and G. J. Zydzik "Vertical cavity surface emitting lasers with electrically conducting mirrors" US Patent No. 5,068,868; issued on November 26 (1991)
12. D. G. Deppe, E. F. Schubert, L.-W. Tu, and G. D. Zydzik "Optical devices with electron-beam evaporated multilayer mirror" US Patent No. 5,206,871; issued on April 27 (1993)
13. R. F. Kopf, E. F. Schubert, H. O'Brian, L.-W. Tu, Y. H. Wang, and G. J. Zydzik "Vertical cavity surface emitting lasers with transparent electrodes" US Patent No. 5,115,441; issued on May 19 (1992)
14. E. F. Schubert, L.-W. Tu, and G. J. Zydzik "Elimination of heterojunction band discontinuities" US Patent No. 5,170,407; issued on December 8 (1992)
15. S. W. Downey, A. B. Emerson, R. F. Kopf, and E. F. Schubert "Devices having repetitive layers" US Patent No. 5,226,055; issued on July 6 (1993)
16. A. Y. Cho, E. F. Schubert, L.-W. Tu, and G. J. Zydzik "Resonant cavity light emitting diode" US Patent No. 5,226,053; issued on July 6 (1993)
17. L. C. Feldman, N. E. J. Hunt, D. C. Jacobson, J. M. Poate, E. F. Schubert, A. M. Vredenberg, Y. H. Wong, and G. J. Zydzik "Erbium-doped optical devices" US Patent No. 5,249,195; issued on September 28 (1993)

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18. R. F. Kopf and E. F. Schubert "PN junction devices with group IV element-doped group III-V compound semiconductors" US Patent No. 5,268,582; issued on December 7 (1993)

19. N. E. J. Hunt and E. F. Schubert "Single mirror light-emitting diodes with enhanced intensity" US Patent No. 5,362,977; issued on November 8 (1994)

20. N. E. J. Hunt, E. F. Schubert, and G. J. Zydzik "Photodetector with a resonant cavity" US Patent No. 5,315,128; issued on May 24 (1994)

21. A. M. Glass, N. E. J. Hunt, J. M. Poate, E. F. Schubert, and G. J. Zydzik "Absorption resonant rare-earth-doped microcavities" US Patent No. 5,363,398; issued on November 8 (1994)

22. N. E. J. Hunt, M. Passlack, E. F. Schubert, and G. J. Zydzik "Electron beam deposition of gallium oxide thin films using a single high purity crystal source" US Patent No. 5,451,548; issued on September 19 (1995)

23. N. K. Dutta, R. J. Fischer, N. E. J. Hunt, M. Passlack, E. F. Schubert, and G. J. Zydzik "Gallium oxide coatings for optoelectronic devices using electron beam evaporation of a high purity single crystal $Gd_3Ga_5O_{12}$ source" US Patent No. 5,550,089; issued on August 27 (1996)

24. U. K. Chakrabarti, J. de Jong, E. F. Schubert, J. Wynn, and G. J. Zydzik "Mechanical fixture and procedure for in-vacuum coating of semiconductor laser facets" US Patent No. 5,719,077; issued on February 17 (1998)

25. E. F. Schubert "Enhanced p-type doping of wide-gap semiconductors" US Patent No. 5,932,899; issued on August 3 (1999)

26. J. D. Joannopoulos, S. Fan, P. R. Villeneuve, and E. F. Schubert "Light emitting device utilizing a periodic dielectric structure" US Patent No. 5,955,749; issued on September 21 (1999)

27. E. F. Schubert and D. A. Stocker "Crystallographic wet chemical etching on GaN" US Patent No. 6,294,475; issued on September 25 (2001)

28. E. F. Schubert "Light-emitting diode with omni-directional reflector" US Patent No. 6,784,462; issued on August 31 (2004)

29. Jaehee Cho, Hong Luo, Jong Kyu Kim, Yong Jo Park, Cheolsoo Sone, and E. Fred Schubert "Light emitting device having protection element and method of manufacturing the light emitting device" US Patent No. 7,411,221 B2; issued on August 12 (2008)

30. Jaehee Cho, Frank Wilhelm Mont, Cheolsoo Sone, Jong-kyu Kim, June-o Song, E. Fred Schubert "Optical thin film, semiconductor light emitting device having the same and methods of fabricating the same" US Patent No. 7,483,212; issued on January 27 (2009)

31. Jaehee Cho, Martin F. Schubert, E. Fred Schubert, Jong Kyu Kim, Cheolsoo Sone "Light emitting diodes and display apparatuses using the same" US Patent No. 7,560,746; issued on July 14 (2009)

32. Martin F. Schubert, Sameer Chhajed, Jong Kyu Kim, E. Fred Schubert, and Jaehee Cho "Reflector shapes for light-emitting diode-polarized light sources" US Patent No. 7,766,495; filed on June 24 (2008); issued on August 3 (2010)

33. Martin F. Schubert, Ahmed Noemaun, Sameer Chhajed, Jong Kyu Kim, E. F. Schubert, Cheolsoo Sone "Encapsulant shapes for light emitting devices lacking rotational symmetry designed to enhance extraction of light with a particular linear polarization" US Patent No. 7,819,557; filed on June 24 (2008); issued on October 6 (2010)

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34. Jaehee Cho, Jong-Kyu Kim, Cheolsoo Sone, and E. F. Schubert "LED device having diffuse reflective surface" US Patent No. 7,816,855; filed on December 28 (2005); issued on October 19 (2010)

35. Jaehee Cho, E. Fred Schubert, and Xing Yan "Liquid crystal display with refractive index matched electrodes" US Patent No. 8,164,727; filed on April 28, 2010; issued on April 24 (2012)

36. Mary H. Crawford, Daniel Koleske, Jaehee Cho, Di Zhu, Ahmed Noemaun, Martin F. Schubert, and E. Fred Schubert "High efficiency III-Nitride light-emitting diodes" US Patent No. 8,451,877; filed on March 17, 2011; issued on May 28 (2013)

37. Min-ho Kim, Martin F. Schubert, Jong Kyu Kim, E. Fred Schubert, Yongjo Park, Cheolsoo Sone, and Sukho Yoon "Nitride semiconductor light-emitting device" US Patent No. 8,502,266; filed on September 8 (2010); issued on August 6 (2013)

38. David J. Poxson, Frank W. Mont, E. Fred Schubert, and Richard W. Siegel "Tunable nanoporous film on polymer substrates, and method for their manufacture" US Patent No. 9,732,427; filed on April 23 (2013); issued on August 15 (2017)

39. Sameer Chhajed, Jong Kyu Kim, Shawn-Yu Lin, Mei-Ling Kuo, Frank W Mont, David J Poxson, E Fred Schubert, Martin F Schubert "Ultra-low reflectance broadband omni-directional anti-reflection coating" US Patent No. 11,088,291; filed on July 22 (2016); issued on August 10 (2021)

Patent Licensing: Several patents listed above have been licensed to companies, including the Luminus Devices Company, Samsung Company, Epistar Company, Cree Company, Osram Company, and Lumileds Company.

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Journal Publications

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1. H. Künzel, H. Jung, E. F. Schubert, and K. Ploog "Influence of growth conditions and of alloy composition on electrical and optical properties of MBE AlGaAs" *Journal Physique Colloque C5*, **C5/175**, 42 (1982)

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2. E. F. Schubert, K. Ploog, H. Dämbkes, and K. Heime "Selectively doped n-AlGaAs/ GaAs heterostructures with high-mobility two-dimensional electron gas for field-effect transistors. Part I: Effect of parallel conductance" *Applied Physics* **A33**, 63 (1984)
3. E. F. Schubert, K. Ploog, H Dämbkes., and K. Heime "Selectively doped n-AlGaAs/ GaAs heterostructures with high-mobility two-dimensional electron gas for field-effect transistors. Part II: Hot electron effects" *Applied Physics* **A33**, 183 (1984)
4. E. F. Schubert and K. Ploog "Transient photoconductivity in selectively doped n-type AlGaAs/GaAs heterostructures" *Physical Review* **B29**, 4562 (1984)
5. E. F. Schubert, E. O. Göbel, Y. Horikoshi, K. Ploog, and H. J. Queisser "Alloy broadening in photoluminescence spectra of AlGaAs" *Physical Review* **B30**, 813 (1984)
6. E. F. Schubert and K. Ploog "Shallow and deep donors in direct-gap n-AlGaAs:Si grown by molecular-beam epitaxy" *Physical Review* **B30**, 7021 (1984)

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7. E. F. Schubert, J. Knecht, and K. Ploog "Transient and persistent photoconductivity in n-AlGaAs and selectively doped n-AlGaAs/GaAs heterostructures" *Journal of Physics C: Solid-State Physics* **18**, L215 (1985)
8. E. F. Schubert, A. Fischer, and K. Ploog "GaAs sawtooth superlattice light-emitting diode operating monochromatically at $\lambda > 0.9$ μm" *Electronics Letters* **21**, 411 (1985)
9. E. F. Schubert, A. Fischer, Y. Horikoshi, and K. Ploog "GaAs sawtooth superlattice laser emitting at wavelengths $\lambda > 0.9$ μm" *Applied Physics Letters* **47**, 219 (1985)
10. E. F. Schubert, A. Fischer, and K. Ploog "Electron-impurity tunneling in selectively doped n-type AlGaAs/GaAs heterostructures" *Physical Review* **B31**, 7937 (1985)
11. E. F. Schubert, Y. Horikoshi, and K. Ploog "Radiative electron-hole recombination in a new sawtooth semiconductor superlattice grown by molecular-beam epitaxy" *Physical Review* **B32**, 1085 (1985)
12. E. F. Schubert and K. Ploog "The delta-doped field-effect transistor" *Japanese Journal Applied Physics Letters* **24**, L608 (1985)
13. K. Ploog, A. Fischer, E. F. Schubert "Preparation and properties of a new GaAs sawtooth doping superlattice" *Proceedings of the Second International Conference (Yamada Conference) on Modulated Semiconductor Structures*; September 9-13 (1985), Kyoto, Japan
14. E. F. Schubert and K. Ploog "Electron subband structure in selectively doped n-AlGaAs/ GaAs heterostructures" *IEEE Transactions on Electron Devices*, **ED-32**, 1868 (1985)
15. E. F. Schubert and K. Ploog "Optical properties of a new sawtooth superlattice grown by molecular beam epitaxy" *Journal de Physique* (Paris), **46**, 147 (1985)

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16. E. F. Schubert, A. Fischer, and K. Ploog "The delta-doped field-effect transistor" *IEEE Transactions on Electron Devices,* **ED-33**, 625 (1986)
17. E. F. Schubert and K. Ploog "Interpretation of capacitance-voltage profiles from delta-doped GaAs grown by molecular-beam epitaxy" *Japanese Journal of Applied Physics* **25**, 966 (1986)
18. E. F. Schubert and W. T. Tsang "Photoluminescence line shape of excitons in alloy semiconductors" *Physical Review B, Rapid Communications*, **B34**, 2991 (1986)
19. E. F. Schubert, J. E. Cunningham, W. T. Tsang, and T. H. Chiu "Delta-doped ohmic contacts to n-GaAs" *Applied Physics Letters* **49**, 292 (1986) and *Applied Physics Letters* **49**, 984 (1986)
20. K. Ploog, A. Fischer, and E. F. Schubert "Preparation and properties of a new GaAs sawtooth doping superlattice" *Surface Science* **174**, 120 (1986)
21. B. I. Miller, E. F. Schubert, U. Koren, A. Ourmazd, A. H. Dayem, and R. J. Capik "High quality narrow GaInAs/InP quantum wells grown by atmospheric organometallic vapor phase epitaxy" *Applied Physics Letters* **49**, 1384 (1986)
22. E. F. Schubert, Cunningham J. E., and Tsang W. T. "Self-aligned enhancement and depletion-mode GaAs field-effect transistors employing the delta-doping technique" *Applied Physics Letters* **49**, 1729 (1986)

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24. W. T. Tsang and E. F. Schubert "Extremely high quality GaInAs/InP quantum wells grown by chemical beam epitaxy" *Applied Physics Letters* **49**, 220 (1986)
25. W. T. Tsang, A. H. Dayem, T. H. Chiu, J. E. Cunningham, E. F. Schubert, J. A. Ditzenberger, J. Shah, J. L. Zyskind, and N. Tabatabaie "Chemical beam epitaxial growth of extremely high quality GaInAs on InP" *Applied Physics Letters* **49**, 170 (1986)
26. E. F. Schubert, A. Fischer, and K. Ploog "Photoconductivity in selectively n- and p-doped AlGaAs/GaAs heterostructures" *Solid-State Electronics 29*, 173 (1986)

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27. E. F. Schubert, J. E. Cunningham, and W. T. Tsang "'Type A' sawtooth doping superlattice: realization of the Esaki-Tsu type superlattice" *Physical Review B Rapid Communications* **B36**, 1348 (1987)
28. E. F. Schubert, J. E. Cunningham, and W. T. Tsang "Electron-mobility enhancement and electron-concentration enhancement in delta-doped n-GaAs at T = 300 K" *Solid-State Communications* **63**, 591 (1987)
29. W. T. Tsang, E. F. Schubert, T. H. Chiu, J. E. Cunningham, E. G. Burkhardt, J. A. Ditzenberger, and E. Agyekum "Growth of high-quality GaInAsP by chemical beam epitaxy" *Applied Physics Letters* **51**, 761 (1987)
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31. W. T. Tsang, E. F. Schubert, T. H. Chiu, J. E. Cunningham, and J. A. Ditzenberger "Chemical beam epitaxial growth of very high quality GaInAs and GaInAs/InP quantum well heterostructures" *GaAs and Related Compounds* (1987) Ed. by W. T. Lindley.
32. J. E. Cunningham, W. T. Tsang, T. H. Chiu, and E. F. Schubert "Molecular beam epitaxial growth of high purity AlGaAs" *Applied Physics Letters* **50**, 769 (1987)
33. Y. Horikoshi, A. Fischer, E. F. Schubert, and K. Ploog "High-mobility two-dimensional electron gas from delta-doped asymmetric AlGaAs/GaAs/AlGaAs quantum wells" *Japanese Journal Applied Physics* **26**, 263 (1987)
34. T. H. Chiu, E. Agyekum, J. A. Ditzenberger, A. Robertson, E. F. Schubert, W. T. Tsang, and C. W. Tu "Growth and characterization of (001) GaAs epilayers by chemical beam epitaxy" *Journal of Electronic Materials* **16**, A21 (1987)
35. E. F. Schubert, J. E. Cunningham, and W. T. Tsang "Perpendicular electronic transport in doping superlattices" *Applied Physics Letters* **51**, 817 (1987)
36. E. F. Schubert, J. E. Cunningham, W. T. Tsang, and G. L. Timp "Selectively delta-doped AlGaAs/GaAs heterostructures with two-dimensional electron-gas concentrations $n_{2DEG} \geq 1.5 \times 10^{12}$ cm^{-2} for field-effect transistors" *Applied Physics Letters* **51**, 1170 (1987)
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39. E. F. Schubert, J. Stark, T. H. Chiu, and B. Tell "Diffusion of atomic silicon in gallium arsenide" *Applied Physics Letters* **53**, 293 (1988)
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