Amended Claims of ZL 202080000267.4 (CN111344792B)

CN Claims in Chinese	CN Claims in English
1.一种存储器，包括： 包括从底部到顶部的第一字线到第 k 字线的第一部分；以及 形成于所述第一部分以上、并且包括从底部到顶部的第(k+1)字线到第 m 字线的第二部分； 以及 控制器，其被配置为：在使用第 x 字线执行编程操作时，向所述第一字线到第(x-2)字线施加第一电压，向第(x-1)字线施加第二电压，向第(x+1)字线施加第三电压，并且向其余的字线施加第四电压； 其中，x、k 和 m 是正整数，1<k<m 并且 3≤x； 如果所述第 x 字线处于所述第一部分中，则所述第一电压具有第一电平； 如果所述第 x 字线处于所述第二部分中，则所述第一电压具有第二电平；并且其中，所述第一电平低于所述第二电平。	1. A memory, comprising: a first portion comprising a first word line to a kth word line from bottom to top; and a second portion formed above the first portion and comprising a (k+1)th word line to an mth word line from bottom to top; and a controller configured to apply a first voltage to the first word line to an (x-2)th word line, a second voltage to an (x-1)th word line, a third voltage to an (x+1)th word line, and a fourth voltage to remaining word lines when an xth word line is used to perform a program operation; wherein x, k and m are positive integers, 1 < k < m and 3 ⩽ x; the first voltage has a first level if the xth word line is in the first portion; the first voltage has a second level if the xth word line is in the second portion; and wherein the first level is lower than the second level.
2.根据权利要求 1 所述的存储器，其中，	2. The memory of claim 1, wherein the controller is further configured to apply a fourth voltage to an (x+2)th word line to the mth word line when the xth word line is used to perform the program operation, and x < (m-1).

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所述控制器还被配置为：在使用所述第 x 字线执行所述编程操作并且 x<(m-1)时，向第(x+2)字线到所述第 m 字线施加所述第四电压。	
3.根据权利要求 1 所述的存储器，还包括形成于所述第二部分以上、并且包括从底部到顶部的第(m+1)字线到第 n 字线的第三部分，其中， 所述控制器还被配置为：在使用所述第 x 字线执行所述编程操作、m<n 并且 x<(n-1)时，向第(x+2)字线到所述第 n 字线施加所述第四电压。	3. The memory of claim 1, further comprising a third portion formed above the second portion and comprising an (m+1)th word line to an nth word line from bottom to top, wherein: the controller is further configured to apply a fourth voltage to the (x+2)th word line to the nth word line when the xth word line is used to perform the program operation, m < n, and x < (n-1).
4.根据权利要求 3 所述的存储器，其中： 如果所述第 x 字线处于所述第三部分中，则所述第一电压具有第三电平；并且 所述第二电平低于所述第三电平。	4. The memory of claim 3, wherein: the first voltage has a third level if the xth word line is in the third portion; and the second level is lower than the third level.
5.根据权利要求 1 所述的存储器，还包括： 形成于所述第一部分以上的下伪字线； 形成于所述第二部分以下的上伪字线； 形成于所述下伪字线和所述上伪字线之间的接头氧化物层； 其中，所述存储器具有两个堆栈的结构。	5. The memory of claim 1, further comprising: a lower dummy word line formed above the first portion; an upper dummy word line formed below the second portion; a joint oxide layer formed between the lower dummy word line and the upper dummy word line; wherein the memory has a two-deck structure.
6.一种存储器，包括：	6. A memory comprising: a first portion comprising an (m+1)th word line to an nth word line from bottom to top; and

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包括从底部到顶部的第(m+1)字线到第 n 字线的第一部分；以及 形成于所述第一部分以下、并且包括从底部到顶部的第(k+1)字线到第 m 字线的第二部分；以及 控制器，其被配置为：在使用第 x 字线执行编程操作时，向第(x+2)字线到所述第 n 字线施加第一电压，向第(x+1)字线施加第二电压，向第(x-1)字线施加第三电压，向所述第(m+1)字线到第(x-2)字线施加第四电压，并且向所述第(k+1)字线到所述第 m 字线施加第五电压； 其中，x、k 和 m 是整数，0≤k<m，(m+2)<x<(n-1) 并且所述第五电压低于所述第四电压， 还包括形成于所述第一部分以上并且包括多个字线的第三部分，其中，所述控制器还被配置为：在使用所述第 x 字线执行所述编程操作时，向所述多个字线施加所述第一电压。	a second portion formed below the first portion and comprising a (k+1)th word line to an mth word line from bottom to top; and a controller configured to apply a first voltage to an (x+2)th word line to the nth word line, a second voltage to an (x+1)th word line, a third voltage to an (x-1)th word line, a fourth voltage to the (m+1)th word line to an (x-2)th word line, and a fifth voltage to the (k+1)th word line to the mth word line when an xth word line is used to perform a program operation; wherein x, k and m are integers, 0 ≤ k < m, (m+2) < x < (n-1), and the fifth voltage is lower than the fourth voltage, further comprising a third portion formed above the first portion and comprising a plurality of word lines, wherein the controller is further configured to apply the first voltage to the plurality of word lines when the xth word line is used to perform the program operation.
7.一种存储器，包括： 包括从底部到顶部的第(m+1)字线到第 n 字线的第一部分；以及 形成于所述第一部分以下、并且包括从底部到顶部的第(k+1)字线到第 m 字线的第二部分；以及	7. A memory comprising: a first portion comprising an (m+1)th word line to an nth word line from bottom to top; and a second portion formed below the first portion and comprising a (k+1)th word line to an mth word line from bottom to top; and a controller configured to apply a first voltage to an (x+2)th word line to the nth word line, a second voltage to an (x+1)th word line, a third voltage to an (x-1)th word line, a fourth voltage to the (m+1)th word line to an (x-2)th word line, and a

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控制器，其被配置为：在使用第 x 字线执行编程操作时，向第(x+2)字线到所述第 n 字线施加第一电压，向第(x+1)字线施加第二电压，向第(x-1)字线施加第三电压，向所述第(m+1)字线到第(x-2)字线施加第四电压，并且向所述第(k+1)字线到所述第 m 字线施加第五电压； 其中，x、k 和 m 是整数，0≤k<m，(m+2)<x<(n-1) 并且所述第五电压低于所述第四电压~~根据权利要求 6 所述的存储器~~， 还包括形成于所述第二部分以下、并且包括从底部到顶部的第一字线到第 k 字线的第三部分，其中，所述控制器还被配置为：在使用所述第 x 字线执行所述编程操作、0<k 时，向所述第一字线到所述第 k 字线施加第六电压，并且所述第六电压低于所述第五电压。	fifth voltage to the (k+1)th word line to the mth word line when an xth word line is used to perform a program operation; wherein x, k and m are integers, 0 ≤ k < m, (m+2) < x < (n-1), and the fifth voltage is lower than the fourth voltage~~The memory of claim 6~~, ~~-~~further comprising a third portion formed below the second portion and comprising a first word line to a kth word line from bottom to top, wherein: the controller is further configured to apply a sixth voltage to the first word line to the kth word line when the xth word line is used to perform the program operation and 0 < k, and the sixth voltage is lower than the fifth voltage.
~~8.根据权利要求 6 所述的存储器，还包括形成于所述第一部分以上并且包括多个字线的第三部分，其中，~~ ~~所述控制器还被配置为：在使用所述第 x 字线执行所述编程操作时，向所述多个字线施加所述第一电压。~~	~~8. The memory of claim 6, further comprising a third portion formed above the first portion and comprising a plurality of word lines, wherein:~~ ~~the controller is further configured to apply the first voltage to the plurality of word lines when the xth word line is used to perform the program operation.~~

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~~98~~. 一种存储器，包括： 包括从底部到顶部的第(m+1)字线到第 n 字线的第一部分；以及 形成于所述第一部分以下、并且包括从底部到顶部的第(k+1)字线到第 m 字线的第二部分；以及 控制器，其被配置为：在使用第 x 字线执行编程操作时，向第(x+2)字线到所述第 n 字线施加第一电压，向第(x+1)字线施加第二电压，向第(x-1)字线施加第三电压，向所述第(m+1)字线到第(x-2)字线施加第四电压，并且向所述第(k+1)字线到所述第 m 字线施加第五电压； 其中，x、k 和 m 是整数，0≤k<m，(m+2)<x<(n-1) 并且所述第五电压低于所述第四电压~~根据权利要求 6 所述的存储器~~， 还包括： 形成于所述第一部分以下的上伪字线； 形成于所述第二部分以上的下伪字线；以及 形成于所述上伪字线和所述下伪字线之间的接头氧化物层； 其中，所述存储器具有两个堆栈的结构。	~~98~~. A memory comprising: a first portion comprising an (m+1)th word line to an nth word line from bottom to top; and a second portion formed below the first portion and comprising a (k+1)th word line to an mth word line from bottom to top; and a controller configured to apply a first voltage to an (x+2)th word line to the nth word line, a second voltage to an (x+1)th word line, a third voltage to an (x-1)th word line, a fourth voltage to the (m+1)th word line to an (x-2)th word line, and a fifth voltage to the (k+1)th word line to the mth word line when an xth word line is used to perform a program operation; wherein x, k and m are integers, 0 ≤ k < m, (m+2) < x < (n-1), and the fifth voltage is lower than the fourth voltage~~The memory of claim 6~~, further comprising: an upper dummy word line formed below the first portion; a lower dummy word line formed above the second portion; and a joint oxide layer formed between the upper dummy word line and the lower dummy word line; wherein the memory has a two-deck structure.

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~~109~~.一种存储器的编程方法，所述存储器包括第一部分和第二部分，所述第一部分包括从底部到顶部的第一字线到第 k 字线，所述第二部分形成于所述第一部分以上、并且包括从底部到顶部的第(k+1)字线到第 m 字线，所述编程方法包括： 在使用第 x 字线执行编程操作时，向所述第一字线到第(x-2)字线施加第一电压； 向第(x-1)字线施加第二电压； 向第(x+1)字线施加第三电压；以及 向其余的字线施加第四电压； 其中，x、k 和 m 是正整数，1<k<m 并且 3≤x； 如果所述第 x 字线处于所述第一部分中，则所述第一电压具有第一电平；如果所述第 x 字线处于所述第二部分中，则所述第一电压具有第二电平；并且所述第一电平低于所述第二电平。	~~109~~. A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first word line to a kth word line from bottom to top, the second portion formed above the first portion and comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising: applying a first voltage to the to the first word line to an (x-2)th word line when an xth word line is used to perform a program operation; applying a second voltage to an (x-1)th word line; applying a third voltage to an (x+1)th word line; and applying a fourth voltage to remaining word lines; wherein x, k and m are positive integers, 1 < k < m and 3 ⩽ x; the first voltage has a first level if the xth word line is in the first portion; the first voltage has a second level if the xth word line is in the second portion; and the first level is lower than the second level.
~~11~~10.根据权利要求 ~~10~~9 所述的编程方法，还包括： 向第(x+2)字线到所述第 m 字线施加所述第四电压；并且 其中，x<(m-1)。	~~11~~10. The program method of claim ~~10~~9, further comprising: applying a fourth voltage to an (x+2)th word line to the mth word line; and wherein x < (m-1).
~~12~~11.根据权利要求 ~~10~~9 所述的编程方法，其中，所述存储器还包括形成于所述第二部分以上的第三部	~~12~~11. The program method of claim ~~10~~9, wherein the memory further comprises a third portion formed above the second portion, the third portion comprises an

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分，所述第三部分包括从底部到顶部的第(m+1)字线到第 n 字线，并且所述编程方法还包括： 向第(x+2)字线到所述第 n 字线施加所述第四电压； 其中，m<n，并且 x<(n-1)。	(m+1)th word line to an nth word line from bottom to top, and the program method further comprises: applying a fourth voltage to the (x+2)th word line to the nth word line; wherein m < n, and x < (n-1).
~~13~~12.根据权利要求 ~~12~~11 所述的编程方法，其中： 如果所述第 x 字线处于所述第三部分中，则所述第一电压具有第三电平；并且 所述第二电平低于所述第三电平。	~~13~~12. The program method of claim ~~12~~11, wherein: the first voltage has a third level if the xth word line is in the third portion; and the second level is lower than the third level.
~~14~~13.根据权利要求 ~~10~~9 所述的编程方法，其中，所述存储器还包括： 形成于所述第一部分以上的下伪字线； 形成于所述第二部分以下的上伪字线； 形成于所述下伪字线和所述上伪字线之间的接头氧化物层； 其中，所述存储器具有两个堆栈的结构。	~~14~~13. The program method of claim ~~10~~9, wherein the memory further comprises: a lower dummy word line formed above the first portion; an upper dummy word line formed below the second portion; a joint oxide layer formed between the lower dummy word line and the upper dummy word line; wherein the memory has a two-deck structure.
~~15~~14.一种存储器的编程方法，所述存储器包括第一部分和形成于所述第一部分以下的第二部分，所述第一部分包括从底部到顶部的第(m+1)字线到第 n 字线，所述第二部分包括从底部到顶部的第(k+1)字线到第 m 字线，所述编程方法包括：	~~15~~14. A program method of a memory, the memory comprising a first portion and a second portion formed below the first portion, the first portion comprising an (m+1)th word line to an nth word line from bottom to top, the second portion comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising: applying a first voltage to an (x+2)th word line to the nth word line when an xth word line is used to perform a program operation; applying a second voltage to an (x+1)th word line; applying a third voltage to an (x-1)th word line;

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在使用第 x 字线执行编程操作时，向第(x+2)字线到所述第 n 字线施加第一电压； 向第(x+1)字线施加第二电压； 向第(x-1)字线施加第三电压； 向所述第(m+1)字线到第(x-2)字线施加第四电压；以及 向所述第(k+1)字线到所述第 m 字线施加第五电压； 其中，x、k 和 m 是整数，0≤k<m，(m+2)<x<(n-1) 并且所述第五电压低于所述第四电压。	applying a fourth voltage to the (m+1)th word line to an (x-2)th word line; and applying a fifth voltage to the (k+1)th word line to the mth word line; wherein x, k and m are integers, 0 ≤ k < m, (m+2) < x < (n-1), and the fifth voltage is lower than the fourth voltage.
~~16~~15.根据权利要求 ~~15~~14 所述的编程方法，其中，所述存储器还包括形成于所述第二部分以下的第三部分，所述第三部分包括从底部到顶部的第一字线到第 k 字线，并且所述编程方法还包括： 向所述第一字线到所述第 k 字线施加第六电压； 其中，0<k，并且所述第六电压低于所述第五电压。	~~16~~15. The program method of claim ~~15~~14, wherein the memory further comprises a third portion formed below the second portion, the third portion comprises a first word line to a kth word line from bottom to top, and the program method further comprises: applying a sixth voltage to the first word line to the kth word line; wherein 0 < k, and the sixth voltage is lower than the fifth voltage.
~~17~~16.根据权利要求 ~~15~~14 所述的编程方法，其中，所述存储器还包括形成于所述第一部分以上的第三部分，所述第三部分包括多个字线，并且所述编程方法还包括： 向所述第三部分的所述多个字线施加所述第一电压。	~~17~~16. The program method of claim ~~15~~14, wherein the memory further comprises a third portion formed above the first portion, the third portion comprises a plurality of word lines, and the program method further comprises: applying the first voltage to the plurality of word lines of the third portion.

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~~18~~17.根据权利要求 ~~15~~14 所述的编程方法，其中，所述存储器还包括： 形成于所述第一部分以下的上伪字线； 形成于所述第二部分以上的下伪字线；以及 形成于所述上伪字线和所述下伪字线之间的接头氧化物层； 其中，所述存储器具有两个堆栈的结构。	~~18~~17. The program method of claim ~~15~~14, wherein the memory further comprises: an upper dummy word line formed below the first portion; a lower dummy word line formed above the second portion; and a joint oxide layer formed between the upper dummy word line and the lower dummy word line; wherein the memory has a two-deck structure.

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