

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES CO., LTD.,
Patent Owner.

IPR2025-00190
Patent 11,568,941 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and MICHAEL
T. CYGAN, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Petitioner, Micron Technology, Inc., filed a petition for *inter partes* review of claims 1–3, 5–11, 13, and 14 of U.S. Patent No. 11,568,941 B2 (Ex. 1001, “the ’941 patent”). Paper 1 (“Pet.” or “Petition”). Patent Owner, Yangtze Memory Technologies Co., Ltd., filed a preliminary response. Paper 11 (“Prelim. Resp.”). Per the bifurcation process, Patent Owner filed a Brief on Discretionary Denial (Paper 10) to which Petitioner filed an Opposition (Paper 18). The Director denied Patent Owner’s request for discretionary denial. Paper 21.

Under the authority delegated to us by the Director under 37 C.F.R. § 42.4(a), we may only institute an *inter partes* review when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); *see also* 37 C.F.R. § 42.108(c). Based upon our review of the present record, Petitioner has sufficiently shown a reasonable likelihood it will prevail with respect to at least one of the challenged claims. Accordingly, we institute an *inter partes* review as to all challenged claims.

II. BACKGROUND

A. *Related Matters*

The parties identify *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group*, No. 3:24-cv-04223 (N.D. Cal.), which was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, No. 3:23-cv-05792-RFL (N.D. Cal.) as

related matters. Pet. 5; Paper 6, 1 (Petitioner’s Updated Mandatory Notice); Paper 4 (Patent Owner’s Mandatory Notice), 1.

Petitioner also identifies twenty-three IPR proceedings that challenge patents that Patent Owner asserted in the District Court Litigation. Pet. 5–6.

B. Real Parties in Interest

Petitioner identifies itself (Micron Technology, Inc.) “and its subsidiaries, including Micron Consumer Products Group LLC” as real parties in interest. Pet. 4.

Patent Owner identifies itself (Yangtze Memory Technologies Co., Ltd.) as the real party in interest. Paper 4 (Patent Owner’s Mandatory Notices), 1.

C. The ’941 Patent (Ex. 1001)

The ’941 patent, titled “Memory Including a Plurality of Portions and Used for Reducing Program Disturbance and Program Method Thereof,” states that it provides a solution for reducing program disturbance and pass voltage disturbance when opening a three-dimensional (3D) memory. *See* Ex. 1001, codes (54), (57), 1:39–41. The patent explains that by “using a memory sectioned to have a plurality of portions and applying voltages to the word lines of the memory according to the portions, program disturbance and pass voltage disturbance may be reduced.” *Id.* at 6:39–43.

Figure 1 of the '941 patent is reproduced below.

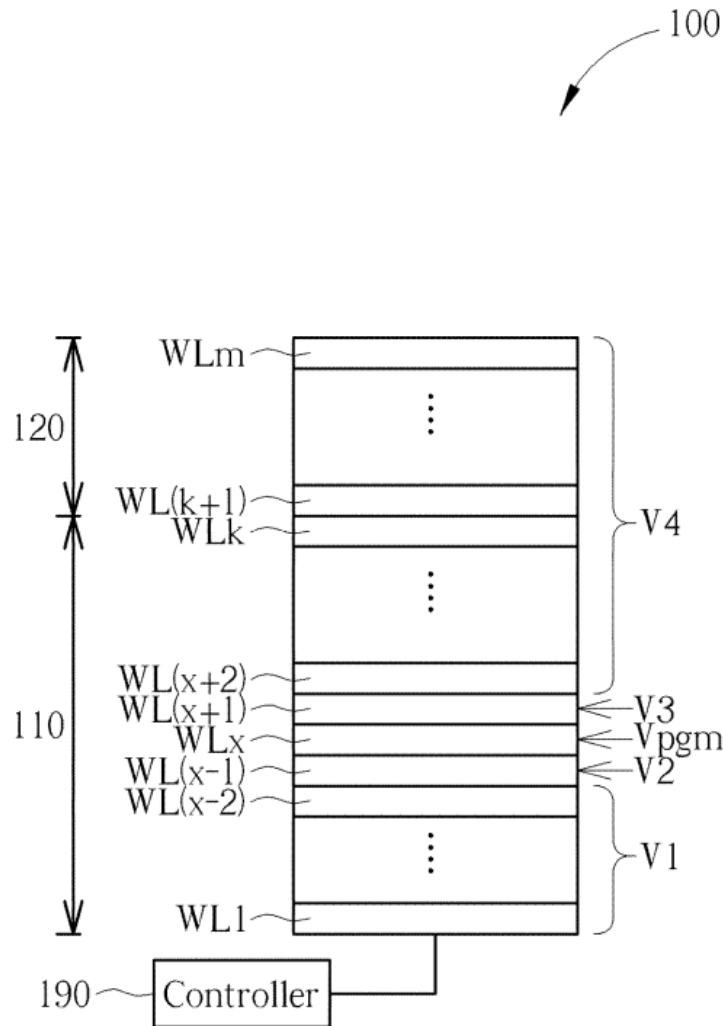


FIG. 1

Figure 1 illustrates memory 100 having first portion 110, second portion 120, and controller 190. *Id.* at 2:64–65. First portion 110 includes first word line (WL1) to kth word line (WLk) from bottom to top; second portion 120, formed above first portion 110, includes a (k+1)th word line WL(k+1) to an mth word line WLn from bottom to top. *Id.* at 2:63–3:3.

The '941 patent states that Figure 1 shows that when an xth wordline WLx is used to perform a program operation, controller 190 applies a program voltage Vpgm to the xth word line WLx. *Id.* at 3:9–11. Controller

190 can also apply voltages to other word lines, such as a first voltage V1 to first word line WL1 to an (x-2)th word line WL(x-2), a second voltage V2 to an (x-1)th word line WL(x-1), and a third voltage V3 to an (x+1)th word line WL(x+1), when k is greater than 1 and less than m and x is less than or equal to 3. *Id.* at 3:11–17. Additionally, controller 190 can apply a fourth voltage V4 to an (x+2)th word line WL(x+2) to the mth word line WLM when the xth word line WLx is used to perform the program operation and $x < m-1$. *Id.* at 3:18–21.

The '941 patent also discloses additional embodiments in which different voltages are applied to different word lines. *See, e.g., id.* at 1:45–2:27, 3:26–4:61.

D. The Challenged Claims

Petitioner challenges claims 1–3, 5–11, 13, and 14 of the '941 patent. Pet. 7. Claims 1, 5, and 11 are independent. Claims 1 and 5, with Petitioner's bracketed material added, are reproduced below.

[1.PRE] A memory comprising:

[1.A] a first portion comprising an (m+1)th wordline to an nth wordline from bottom to top; and

[1.B] a second portion formed below the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top; and

[1.C] a controller configured to apply

[1.D] a first voltage to an (x+2)th wordline to the nth wordline,

[1.E] a second voltage to an (x+1)th wordline,

[1.F] a third voltage to an (x-1)th wordline,

[1.G] a fourth voltage to the (m+1)th wordline to an (x-2)th wordline, and

[1.H] a fifth voltage to the (k+1)th wordline to the mth wordline when an xth wordline is used to perform a program operation;

[1.I] wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

Ex. 1001, 6:55–7:2; Pet. viii.

[5.PRE] A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first wordline to a kth wordline from bottom to top, the second portion formed above the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top, the program method comprising:

[5.A] applying a first voltage to the to the [sic] first wordline to an (x–2)th wordline when an xth wordline is used to perform a program operation;

[5.B] applying a second voltage to an (x–1)th wordline; and

[5.C] applying a third voltage to an (x+1)th wordline;

[5.D] wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.

Ex. 1001, 7:23–34; Pet. ix.

E. Asserted Grounds of Unpatentability

Petitioner contends claims 1–3, 5–11, 13, and 14 are unpatentable on the following grounds.

Claims Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1–3, 5–7, 11, 13	102(a)(1)	Dong ²

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102, 103. The earliest claimed priority date for the ’941 patent is after the effective date of the applicable AIA amendment. See Ex. 1001, (60). Thus, we refer to the AIA version of 35 U.S.C. §§ 102, 103.

² Dong, US Pub. 2008/0279008 (filed May 7, 2008, published Nov. 13, 2008) (Ex. 1005, “Dong”).

Claims Challenged	35 U.S.C. § ¹	Reference(s)/Basis
	102(a)(2)	
1–3, 5–7, 11, 13	103(a)	Dong
8, 9	103(a)	Dong, Costa ³
4, 10, 14	103(a)	Dong, Shirai ⁴

Pet. 7.

In support of its unpatentability arguments, Petitioner relies on the declaration of David Kuan-Yi Liu, Ph.D. (Ex. 1004). Patent Owner relies on the declaration of Sunil P. Khatri, Ph.D. (Ex. 2006).

F. Overview of Asserted Art

1. Dong (Ex. 1005)

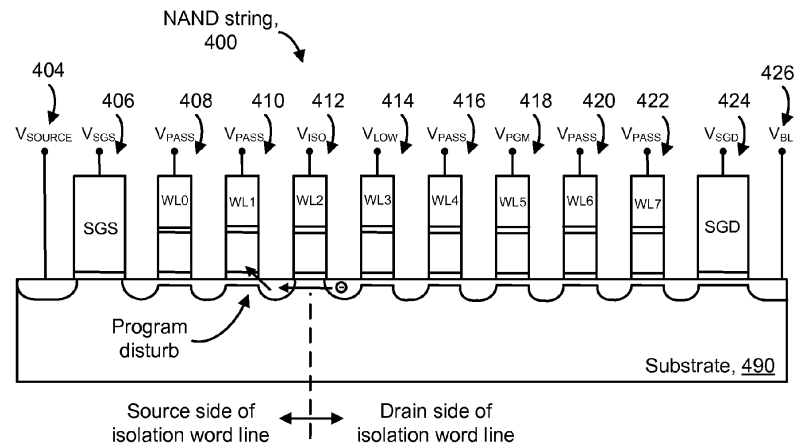
Dong, titled “Non-volatile Storage with Boosting Using Channel Isolation Switching,” is directed to non-volatile storage “in which program disturb is reduced by preventing source side boosting in selected NAND strings.” Ex. 1006, codes (12), (43), (54), (57). Dong states that “program disturb” occurs when the threshold voltage of an unselected non-volatile storage element is shifted due to the programming of other non-volatile storage elements. *Id.* ¶ 11.

Dong Figure 4, reproduced below, depicts a cross-sectional view of a 2D NAND string showing a program disturb mechanism. *Id.* ¶ 19.

³ Costa, US 2018/0012667 A1 (filed July 7, 2016, published Jan. 11, 2018) (Ex. 1012, “Costa”).

⁴ Shirai, US 2019/024405 A1 (filed Mar. 13, 2019, published July 11, 2019) (Ex. 1018, “Shirai”).

Fig. 4

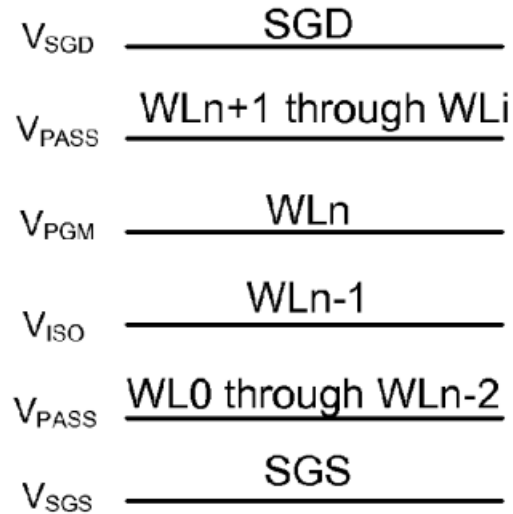


Dong Figure 4 depicts a cross-sectional view of a NAND string showing a program disturb mechanism. *Id.* ¶¶ 19, 45.

The 2D NAND string includes a source side select gate 406, a drain side select gate 424, eight storage elements (408, 410, 412, 414, 416, 418, 420, 422) formed on substrate 490, source supply line 404, and bit line 426. *Id.* ¶ 45.

Dong Figures 5a (reproduced below) through 5h depict different examples of self-boosting modes. *Id.* ¶¶ 20, 47.

Fig. 5a



Dong Figure 5a above depicts an example of a self-boasting mode.
Id. ¶ 49.

In the self-boasting mode example shown in Figure 5a, various voltages (V_{PASS} , V_{PGM} , V_{ISO} , V_{SGS} , V_{SGD}) are applied to the word lines (W_{L0} – W_{Li}) and gate control lines (SGS, SGD). *Id.* ¶ 49. More particularly, the voltage V_{SGS} is applied to the source-side selected gate control line SGS; a pass voltage V_{PASS} is applied to each of the unselected word lines, W_{L0} through W_{Ln-2} and W_{Ln+1} through W_{Li} ; a program voltage V_{PGM} is applied to the selected word line W_{Ln} ; isolation voltage V_{ISO} is applied to W_{Ln-1} , the word line which is adjacent to the selected word line on the source side; and V_{SGD} is applied via the drain-side select gate control line SGD. *Id.* ¶ 49. These voltages are used during the drain side boosting, which occurs after source side boosting. *Id.* ¶ 47.

2. *Costa (Ex. 1012)*

Costa is a US Patent Publication titled “Word Line Dependent Pass Voltages in Non-Volatile Memory” that is directed to reducing errors when sensing in non-volatile memory. Ex. 1012, codes (12), (43), (54), ¶ 28. Costa teaches that programming memory tends to raise the channel resistance of a group of memory cells that are programmed from one end to the other. *Id.* ¶ 29. Costa states that varying the pass voltage applied to a subset of memory cells during sensing can compensate for the increased channel resistance. *Id.* ¶ 30. In one embodiment during reading, the pass voltage applied when reading the earlier programmed memory cells is higher relative to the pass voltage applied when reading the later programmed memory cells. The higher pass voltage can directly compensate for an apparent increase in threshold voltage due to the increased channel resistance from programming the later programmed memory cells. *Id.* ¶ 31.

3. *Shirai (Ex. 1018)*

Shirai, published July 11, 2019, is a US Patent Publication titled “Semiconductor Device and Method of Manufacturing the Same.” Ex. 1007, codes (10), (54). In manufacturing the device, holes are formed in a stacked body having multiple conductive layers. *Id.* ¶ 3. The method involves repeating formation of the holes and formation of the stacked body. *Id.*

III. ANALYSIS

A. *Grounds of the Petition*

For the reasons below, we determine that Petitioner has satisfied the threshold for institution as to at least one claim. Accordingly, we institute *inter partes* review on all claims and all grounds raised in the Petition. *See SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60

(2018) (holding that a decision to institute under 35 U.S.C. § 314 may not institute on fewer than all claims challenged in the petition); *AC Technologies S.A. v. Amazon.com*, 912 F.3d 1358, 1364 (Fed. Cir. 2019) (stating “if the Board institutes an [*inter partes* review], it must similarly address all grounds of unpatentability raised by the petitioner”).

1. Legal Standards

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

Anticipation under 35 U.S.C. § 102 “requires that every element and limitation of the claim was previously described in a single prior art reference, either expressly or inherently, so as to place a person of ordinary skill in possession of the invention.” *Sanofi-Synthelabo v. Apotex, Inc.*, 550 F.3d 1075, 1082 (Fed. Cir. 2008); *see also* *Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) (“[T]he dispositive question regarding anticipation [i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference’s] teaching that every claim element was disclosed in that single reference.”). Anticipation also requires that a reference discloses “all of the limitations arranged or

combined in the same way as recited in the claim.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008).

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the [relevant time frame] to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence⁵, objective evidence of obviousness or nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2016) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)).

B. Level of Ordinary Skill in the Art

In determining whether a claimed invention would have been obvious, we consider the level of ordinary skill at the time of filing. 35 U.S.C. § 103; *see also Graham*, 383 U.S. at 17 (discussing pre-AIA obviousness).

⁵ The present record does not contain evidence of secondary considerations. *See* Pet. 85; Prelim. Resp.

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had a had a bachelor’s degree in electrical engineering or a similar discipline, along with 2–3 years of professional experience working with (e.g., researching, designing, or teaching) NAND memory devices (including issues relating to the operation, e.g., programming, of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). Pet. 22 (citing Ex. 1004 ¶¶ 40–42). Petitioner also asserts that a POSITA would have been aware of and generally knowledgeable about NAND memory’s structure and fabrication, its component parts, how it operates, and how it is controlled. *Id.* at 22–23 (citing Ex. 1004 ¶ 41). Patent Owner does not take a position on the level of ordinary skill in the art at this stage of the proceeding. Prelim. Resp. 12–13; *see also* Ex. 2006 ¶ 35 (applying Petitioner’s definition of a POSITA to the opinions set forth in the declaration but reserving the right to opine to an alternative level of a POSITA).

For purposes of this Decision, we adopt Petitioner’s definition of a POSITA as it appears consistent with the level of ordinary skill in the art that is reflected by the prior art of record.

C. Claim Construction

We construe the ’941 patent claims using the same claim construction standard that would be used to construe a claim in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–

14 (Fed. Cir. 2005) (en banc). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

1. Preamble

The preamble of claim 5 recites:

A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first wordline to a k th wordline from bottom to top, the second portion formed above the first portion and comprising a $(k+1)$ th wordline to an m th wordline from bottom to top, the program method comprising:

Ex. 1001, 7:23–28.

The preamble of claim 11 recites:

A program method of a memory, the memory comprising a first portion and a second portion formed below the first portion, the first portion comprising an $(m+1)$ th wordline to an n th wordline from bottom to top, the second portion comprising a $(k+1)$ th wordline to an m th wordline from bottom to top, the program method comprising:

Ex. 1001, 8:15–20.

Petitioner presents its unpatentability arguments as if the preambles of claims 5 and 11 are limiting without expressly stating that they are so. *See, e.g.*, Pet. 34 (stating to “the extent the preamble [of claim 5] is limiting”), 68 (stating “[i]f the preamble of claim 11 is limiting”); Ex. 1004 ¶¶ 116, 194 (stating the analysis treats the preamble of claims 5 and 11 as if it were a limitation). At this stage of the proceeding, Patent Owner does not address whether or not the preamble is limiting. *See generally* Prelim. Resp.

Because the preambles of independent claims 5 and 11 provide antecedent basis for the word line limitations recited in the body of their respective claim, we treat the preambles of claims 5 and 11 as limiting. *See Deere & Co. v. Bush Hog, LLC*, 703 F.3d 1349, 1358 (Fed. Cir. 2012) (stating “a preamble phrase that provides antecedent basis for a claim limitation generally limits the scope of the claim”). The parties are invited to address whether the preamble is limiting if they so choose, to the extent permitted by our rules.

2. “*from bottom to top*”

Each of the independent claims recite a memory comprising a first and a second portion having various word lines “from bottom to top.” Ex. 1001, 6:55–60, 7:23–38, 8:15–20. Claims 1 and 11 state the second memory portion is “formed below” the first portion; claim 5 states the second memory portion is “formed above” the first portion. *Id.*

Petitioner asserts that the claims should be construed according their plain and ordinary meaning and that no further construction is required. Pet. 22. However, in its unpatentability arguments, Petitioner asserts that while the ’941 patent does not define the phrase “bottom to top,” it is common usage to refer to the “source end” of a memory string of a NAND flash memory device as the “bottom” and the “drain end” as the “top.” Pet. 35 (citing Ex. 1004 ¶¶ 112–113, 120). Petitioner thus asserts that the claim term “bottom to top” as understood by a person of ordinary skill in the art means from source side to drain side. *See id.* at 34–35. To support this contention, Petitioner’s declarant Dr. Liu points to figures in a text book discussing two-dimensional NAND flash memories showing the source end

on the bottom and the drain end on the top, and states that this “convention applies irrespective of whether the physical device is in a horizontal or vertical direction.” Ex. 1004 ¶ 113 (citing Ex. 1009, Figures 2.1, 2.2, 2.4); *see also id.* (stating that it is common, when discussing NAND flash memory, to refer to the source end of a memory string as the “bottom” and the drain end as the “top”).

Patent Owner disagrees and states that the “plain meaning of ‘bottom’ and ‘top’ is well understood—bottom means lowest point and top means highest point above the substrate.” Prelim. Resp. 15–16 (citing Ex. 1001, 1:26–41, 6:39–47; Ex. 2006 ¶ 55). Patent Owner asserts that the claims of the ’941 patent use the terms “top” and “bottom” consistent with the plain and ordinary meaning and that the term “from bottom to top” has no special meaning in the semiconductor manufacturing context or the context of the ’941 patent. Prelim. Resp. 16–19 (citing Ex. 1001, code (57), 1:26–41, 4:29–36, 6:39–47, Figs. 1–11; Ex. 2006 ¶¶ 55–63). Patent Owner further states that the figures of the ’941 patent illustrate word lines arranged vertically, which reinforces that the plain and ordinary meaning of bottom and top applies. *Id.* at 19; *see also id.* (stating references cited on face of the patent use the terms top and bottom to refer to the highest and lowest portion of a memory stack, respectively).

At this stage of the proceeding, we disagree with Petitioner’s contention that plain and ordinary meaning of the claim term “from bottom to top” as understood by a person of ordinary skill in the art means from source end to drain end.

The independent claims state that the second memory portion is *formed* either *above* or *below* the first memory portion. The forming of a

one memory portion above or below another portion establishes a relative top and bottom. For example, claim 5 is directed to a “program method of memory” that requires a second portion *formed above* the first portion. A second memory portion that is formed *above* a first memory portion would be on *top* of the first portion. Given that the claims themselves identify relative vertical locations of the memory portions (i.e., second memory portion is above the first portion), it follows that claim terms referring to the top and bottom of word lines within the memory portions also refer to relative vertical locations of the word lines within the memory portions. Thus, we understand the plain and ordinary meaning of claim language referring to first and second memory portions that comprise word lines “from bottom to top” to mean that the word lines of the memory portions are arranged vertically from the bottom end of the memory portion toward the top of the memory portion (i.e., from bottom to top).

Our understanding that the term “from bottom to top” refers to the vertical arrangement of word lines in the memory portions from bottom to top and not from source end to drain end is supported by the ’941 patent Specification, which does not refer to source or drain side of the word lines. *See generally* Ex. 1001. Rather, the ’941 patent illustrates and describes figures of memory devices having word lines arranged vertically from bottom to top. For example, Figures 1–11 each depict “a memory” having vertically arranged word lines. *See id.* at 2:37–55, Figs. 1–11. The Specification describes embodiments with first, second, and/or third memory portions as including various word lines “from bottom to top” and that the memory portions are formed above or below each other, thus supporting that the claim term “from bottom to top” is used according to its plain and

ordinary meaning of from bottom to top and not from source side to drain side. *See, e.g., id.* at 1:45–50, 1:55–60, 2:1–7, 2:14–18, 2:64–3:3, 3:46–48.

Additionally, the Specification describes the location of certain word lines relative to the “lowermost” or “uppermost” portion of a memory portion. *See, e.g.,* Ex. 1001, 5:10–12 (stating word line WLx of Figure 9 “is located in the lowermost portion 920”), 5:15–19 (stating wordline WLx of Figure 10 “is located in the portion 910 above the lowermost portion 920”), *see also id.* at 5:38–50 (describing the operation of the same memory in different conditions and identifying the word lines as located in “lowermost” or “uppermost” portion of the memory portions). The Specification’s identification of the location of the word lines in relation to the “lowermost” or “uppermost” memory portions shows that the Specification identifies the location of the word line in relation to its vertical location, not to its location relative to the source or drain.

Finally, Petitioner does not point to any persuasive intrinsic evidence to support its contention that “from bottom to top” means “from the source side to the drain side.” *See* Pet. 34–35 (citing Ex. 1004 ¶¶ 112–113, 120). Petitioner’s declarant Dr. Liu testifies that a POSITA would be familiar with the convention that a memory array would have the source end of the NAND string at the bottom and the drain end at the top. Ex. 1004 ¶ 113. To support this position, Dr. Liu points to figures of 2D NAND flash memories that depict the source end of the NAND string at the bottom of the string and the drain end string at the top. *See* Ex. 1004 ¶¶ 49, 112–113, 120 (citing, *inter alia*, Ex. 1009, 39–40, Figs. 2.1, 2.2, 2.4). Petitioner fails to persuasively explain, however, how figures that depict the architecture of 2D NAND strings with the source end on the bottom means that the term “from bottom

to top” means from source end to drain end. *See also* Ex. 1009, 39–40, Figs. 2.1, 2.2, 2.4 (not using the terms “bottom” or “top” to refer to source end or drain end).

Moreover, Patent Owner’s declarant Dr. Khatri provides contrary testimony that a POSITA looking at the textbook identified by Petitioner (Ex. 1009) would understand that the reference uses the terms “top” and “bottom” when describing the vertically highest or lowest physical components of the 3D NAND memory. Ex. 2006 ¶¶ 68–69 (citing Ex. 1009, 327 (stating “the charge trap nitride layer is physically connected from top to bottom [control gates] in” a 3D flash memory)). Patent Owner also provides evidence of a patent publication (Ex. 2012), cited on the face of the ’941 patent, depicting a “U” shaped memory array that *does not* have the source end on the bottom or the drain end on the top of the array. *See, e.g.*, Prelim. Resp. 21 (citing Ex. 2012 as showing the source line on the top of the structure and the bottom of the NAND string is a “controllable gate” and not a “source”). This evidence belies Petitioner’s contention that “from bottom to top” means from source end to drain end.

Thus, Petitioner’s argument and evidence that a skilled artisan would understand “from bottom to top” to mean “from source side to drain side” is not persuasive. Based on the present record, we construe the claim language referring to first and second memory portions that comprise word lines “from bottom to top” to mean that word lines of the memory portions are arranged vertically from bottom (lowest) to top (highest). The parties, however, are invited to address the proper constructions of these terms during trial if they so choose, to the extent allowed by our rules.

D. Asserted Unpatentability of Claims 1, 3, 5–7, 11 and 13 over Dong

Petitioner contends that independent claims 1, 5 and 11 and dependent claims 3, 6, 7, and 13 are either anticipated by or would have been obvious over Dong. Pet. 28–70. Petitioner maps Dong Figure 5a to the “Group One” claims (i.e., independent claim 5 and dependent claims 6 and 7) and maps Dong Figure 5g to the “Group Two” claims (independent claims 1 and 11 and dependent claims 3 and 13). *Id.* at 28. Patent Owner opposes, contending Dong does not disclose word lines arranged “from bottom to top” or a first portion formed either above or below second portion as required by all challenged claims. Prelim Resp. 33–49.

For the reasons set forth below, we determine Petitioner shows a reasonable likelihood that at least one claim would have been obvious over Dong. Thus, we institute review on all challenged claims on all asserted grounds. *See SAS Institute Inc.*, 138 S. Ct. at 1359–60; *AC Technologies*, 912 F.3d at 1364.

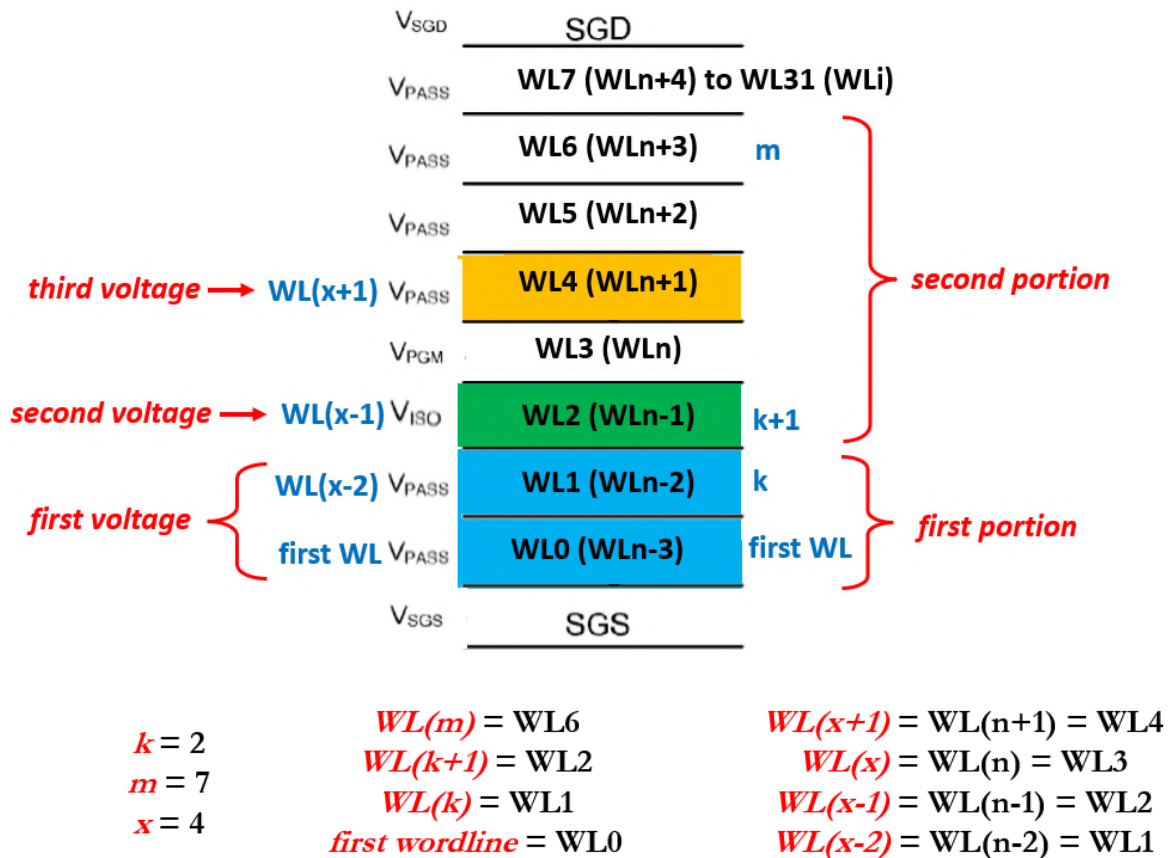
1. Claim 5

Independent claim 5 is directed to a method of programming memory involving applying first, second, and third voltages to various word lines. Ex. 1001, 7:23–34. The preamble states that memory has a “first portion” and a “*second portion formed above the first portion*,” each portion having word lines. *Id.* at 7:23–28 (emphasis added). In particular, the first portion has a “first wordline to a kth wordline from *bottom to top*” and the second portion has as a “(k+1)th wordline to an mth wordline from *bottom to top*.” *Id.* at 7:23–34 (emphases added).

The claimed method requires applying a first voltage to the first word line to an $(x-2)$ th word line when an x th word line is used to perform a program operation (claim element 5.A), applying a second voltage to an $(x-1)$ th word line (claim element 5.B), and applying a third voltage to an $(x+1)$ th word line (claim element 5.C), wherein x , k , and m are positive integers, k is greater than 1 and less than m , and x is greater than or equal to 3 (claim element 5.D). *Id.* at 7:29–34.

Petitioner asserts Dong's method of programming NAND flash memory strings, as depicted in Figure 5a, discloses or teaches the subject matter of claim 5. Pet. 23, 28–44. Petitioner provides a color annotated, modified version of Dong Figure 5a (top) and a chart (bottom), reproduced below, to show how Petitioner maps the word lines, portions, and voltages of Dong Figure 5a to claim 5 in a 32-cell memory string having 32 word lines (i.e., word lines W0 through WL31). Pet. 32–33 (citing Ex. 1004 ¶ 115; Ex. 1005, Fig. 5a).

Fig. 5a



Petitioner’s modified Dong Figure 5a above depicts an example of self-boosting mode in which various voltages (V_{PASS} , V_{PGM} , V_{ISO} , V_{SGS} , V_{SGD}) are applied to the wordlines (WL0–WL32) and gate control lines (SGS, SGD) of a 32-cell memory. Pet. 33; Ex. 1005 ¶ 49.

Petitioner maps the voltages recited in claim 5 to Dong Figure 5a⁶, by mapping the claimed “first voltage” to Dong’s voltage V_{PASS} , the claimed

⁶⁶ Unlike Figure 8 of the ’941 patent, which depicts “memory 700”, we do not understand Dong Figures 5a–5h to depict the physical structure of a memory cell, but rather to depict a self-boosting mode. Ex. 1001, 4:29–30

“second voltage” to Dong’s voltage VISO, and the claimed “third voltage” to Dong’s voltage VPASS applied to word line WL4. *See* Pet. 32–33.

With regard to word lines recited in claim 5, Petitioner uses a 32-cell NAND string (having 32 word lines) as an example and assigns labels WL0 through WL31 to the word lines depicted in Figure 5a, where, for example, WL3 corresponds to WLn, WL0 corresponds to WLn-3, WL7 corresponds to WLn+4, and WL31 corresponds to WLi. Pet. 31–32. Petitioner also maps Dong’s word lines WL0–WL1 to the claimed “first portion” and word lines WL2–WL6 to the claimed “second portion,” and asserts that word lines WL2 to WL6 are in Dong’s “second portion” of memory that is “formed above” the first portion. Pet. 36–38 (citing Ex. 1004 ¶ 127; Ex. 1005, Fig. 5a). Petitioner further asserts that Dong’s first portion includes a first wordline (WL0) to a kth wordline (WL1) from bottom to top and that Dong’s second portion includes a (k+1)th wordline (WL2) to an mth wordline (WL6) from bottom to top. Pet. 37–38 (citing Ex. 1005 ¶ 48, Fig. 5a; Ex. 1006 ¶¶ 104–105, 107, 120, 124–127, 120).

Finally, Petitioner asserts that Dong’s method meets the remaining limitations of claim 5 because when Dong’s word line WL3 is used for programing (a) a first voltage (VPASS) is applied to WL0 to WL1 (the first word line to an (x-2)th word line) as required by claim element 5.A; (b) a second voltage (VISO) is applied to WL2, the (x-1)th word line as required by claim element 5.B; and (c) a third voltage (Vpass) is applied to WL4, the

(stating Figure 8 illustrates “memory 700”); Ex. 1005 ¶ 20 (stating “FIGS. 5a-h depict different examples of self-boosting modes”); Ex. 2006 ¶¶ 86–95 (stating the voltage charts in Dong’s Figures 5a and 5g do not show physical structure). The parties are invited to address this issue if they so choose.

(x+1)th word line required by claim element 5.C, (d) wherein $k=2$, $m=7$, $x=4$ thus meeting the limitations of claim element 5.D. Pet. 38–44.

At this stage of the proceeding, Patent Owner does not dispute Petitioner’s mapping of the particular voltages and word lines of Dong to the asserted corresponding voltages and word lines recited in claim 5. *See generally* Prelim. Resp. Rather, as noted above, Patent Owner disputes Petitioner’s construction of “*from bottom to top*” as meaning that the word lines are arranged from source end to drain end. *Id.* at 15–33. Patent Owner asserts that Dong only discloses word lines arranged horizontally, i.e., in a horizontal plane, above the substrate and, thus, does not teach or suggest a memory having a second portion formed over a first portion or word lines arranged from bottom to top as recited in the claims. *Id.* at 33–41.

Based on the current record, we determine Petitioner sufficiently shows that Dong teaches or suggests all of the limitations of claim 5. First, we agree with Petitioner’s undisputed mapping of Dong’s word lines and voltages to the corresponding word lines and voltages of claim 5. We also determine that Petitioner has sufficiently shown that Dong teaches or suggests the limitations requiring word lines arranged vertically from bottom to top and a second memory portion formed above a first memory portion.

Because we did not adopt Petitioner’s proposed construction of “from bottom to top” as meaning from source end to drain end, we disagree that Dong’s method applied to a 2D memory, which has word lines arranged horizontally from source to drain end, teaches these limitations. Pet. 34–35 (citing Ex. 1004 ¶¶ 112–113, 120). However, we are persuaded at this stage of the proceeding by Petitioner’s alternative argument that even if “from bottom to top” is construed to require vertical strings in a 3D NAND

memory, that Dong still satisfies this limitation by teaching that its array of storage elements can be 3D and by showing Figure 5a in a vertical orientation. *See e.g.*, Pet. 35 (citing Ex. 1005 ¶ 95, Fig. 5a; Ex. 1004 ¶ 120).

We understand the Petition to assert that a POSITA would have understood that Dong's method could be applied to a 3D NAND memory device having vertically oriented word lines. *Id.* The Petition asserts that Dong teaches methods to decrease program disturb of memory arrays, that Dong expressly states that its methods can apply to 3D memory arrays, and that Figure 5a, when applied to a 3D memory array, shows vertical word lines in first and second memory portions arranged "from bottom to top" as recited in the claims. *See, e.g.*, Pet. 14–15, 34–38 (citing Ex. 1005 ¶ 95, Fig. 5a; Ex. 1004 ¶¶ 120, 127); *see also* Ex. 1004 ¶¶ 104–105, 124–127.

Petitioner explains that NAND devices were originally formed as 2D memory arrays but that 3D NAND flash cells were developed to scale down memory cell size. Pet. 11–13 (citing Ex. 1009, 58, 40, 292). The Petitioner further asserts that conceptually modern 3D NAND structure can be viewed as turning the 2D NAND string on its side resulting in a 3D structure with a vertical channel. Pet. 12–14 (citing Ex. 1009, 296; Ex. 1010, 122; Ex. 1011, 3); Ex. 1004 ¶¶ 52–54. Petitioner further argues that similar techniques and algorithms are used to program 2D and 3D NAND flash memory devices. Pet. 12–14 (citing Ex. 1001, 3; Ex. 1010, 122; Ex. 1009, 44–46, 52–53, 296; Ex. 1004 ¶¶ 49–56); *see also* Ex. 1004 ¶ 61 (stating that many techniques for mitigating program disturb originally developed for 2D NAND apply equally to 3D NAND devices because of "many of the same fundamental principles of device physics are at play in both 2D and 3D NAND").

Patent Owner argues that Dong's passing reference to 3D storage does not disclose or suggest vertically arranged word lines. Prelim. Resp. 41–49 (citing Ex. 2006 ¶¶ 96–102). Patent Owner asserts that (1) Petitioner does not explain why 3D storage would have word lines arranged vertically from bottom to top rather than horizontally, (2) Petitioner does not argue that that it would have been obvious to turn Dong's horizontally arranged word lines into vertically arranged word lines, and (3) Petitioner has not shown a POSITA would have had a reasonable expectation in modifying Dong to have vertical word lines. *Id.*

We are not persuaded by Patent Owner's arguments at this stage of the proceeding because they fail to address Petitioner's contentions about 3D NAND memory, including that 3D NAND flash devices have strings of memory cells placed in the vertical direction (Ex. 1004 ¶ 56 (citing Ex. 1009, 296)) and the similarities between 2D and 3D NAND flash memory devices, including the techniques and algorithms used to program the cells of such devices. *See e.g.*, Pet. 14.

We are also not persuaded by Patent Owner's argument that because Dong was filed in May 2007, a POSITA would not understand Dong's 3D memory arrays to have vertically arranged word lines or that POSITA would not apply Dong's program disturb methods to vertical 3D NAND cells due differences between 2D and 3D NAND cells, including cell structure, array architecture, and program disturb conditions. Prelim. Resp. 46–49 (citing, *inter alia*, Ex. 1009 pt. 2, 354, 356, 362–363; Ex. 2006 ¶ 102); Ex. 2006 ¶ 42. An obviousness determined is assessed based on the knowledge of a

POSITA at the time the challenged patent's effective filing date.⁷ *See* 35 U.S.C. § 103 (stating the test for obviousness asks whether “the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains”). Whether a POSITA would have understood as of this date that Dong's methods could be applied to 3D NAND memory arrays having word lines arranged vertically from bottom to top is an issue best resolved on a full record.

Thus, for the foregoing reasons, Petitioner has shown a reasonable likelihood that it will prevail in showing that claim 5 would have been obvious over Dong.

2. *Independent claims 1 and 11*

Petitioner asserts that Dong anticipates or renders obvious claims 1 and 11 and presents argument and evidence mapping Dong Figure 5g to these claims. *See* Pet. 50–66 (addressing claim 1), 68–70 (addressing claim 11). Petitioner states that the “same preliminary comments about Dong Fig. 5a (provided in §X.A for claim 5) apply here.” Pet. 50 (discussing claim 1); *see also* Pet. 52 (stating the same discussion regarding the preamble of claim 5 (§ X.A.1) applies to claim 1 regarding the meaning of bottom to top); *id.* at 68 (discussing claim 11). At this stage of the proceeding, we understand Petitioner's reference to § X.A.1 to mean that Dong's statement that its

⁷ To the extent the parties dispute that knowledge of a POSITA should be assessed as of February 10, 2020, the earliest claimed priority date of the '941 patent, the parties are invited to address this issue at trial.

“array of storage elements can be three dimensional” also applies to Figure 5g.

Other than the arguments discussed above, Patent Owner does not present any additional arguments directed to independent claims 1 and 11. We have reviewed Petitioner’s arguments and evidence for claims 1 and 11 and are persuaded that Petitioner has shown a reasonable likelihood that it will prevail in showing that these claims are unpatentable over Dong.

E. Asserted Unpatentability of Dependent Claims 4, 8–10, and 14

Petitioner asserts dependent claims 8 and 9 (which depend indirectly from claim 5), would have been obvious over Dong in combination with Costa and that claim 4 (which depends from claim 1), claim 10 (which depends from claim 5), and 14 (which depends from claim 11), would have been obvious over Dong in combination with Shirai. Pet. 70–84. Other than the arguments discussed above, Patent Owner does not dispute Petitioner’s contentions regarding these claims at this stage of the proceeding. Because we determine Petitioner has sufficiently shown a reasonable likelihood that it will prevail in showing at least one claim would have been unpatentable, we institute *inter partes* review of all challenged claims on all grounds, including the asserted unpatentability of claims 8 and 9 over Dong and Costa and of claims 4, 10, and 14 over Dong and Shirai.

IV. CONCLUSION

For the foregoing reasons, we determine that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing at least one of the challenged claims of the ’941 patent is unpatentable. Because Petitioner has satisfied the threshold for institution as to at least one

claim, we institute *inter partes* review on all claims and all grounds raised in the Petition.

At this preliminary stage, we have not made a final determination with respect to the patentability of the challenged claims or any underlying factual and legal issues, including claim construction.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of all challenged claims of the '941 patent on all asserted grounds is instituted; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this Decision.

IPR2025-00190
Patent 11,568,941 B2

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