UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00792
U.S. Patent No. 11,468,957
Issue Date: October 11, 2022

Title: ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION

DECLARATION OF DAVID KUAN-YU LIU, PH.D.

YMTC
Exhibit 2022
Micron v. YMTC
IPR2025-00190
Ex. 2022-001

Micron Ex. 1003, p. 1
Micron v. YMTC
IPR2024-00792

TABLE OF CONTENTS

I. INTRODUCTION 4

II. BACKGROUND AND EXPERT QUALIFICATIONS 4

III. ASSIGNMENT AND MATERIALS CONSIDERED 7

IV. UNDERSTANDING OF THE LAW 9

V. LEVEL OF SKILL IN THE ART 13

VI. TECHNOLOGY BACKGROUND 14

A. NAND Flash Structure 14

B. 3D NAND Flash Operation 18

VII. THE '957 PATENT 21

A. Effective Filing Date 21

B. Overview 22

C. Prosecution History 25

D. Claims 25

VIII. CLAIM CONSTRUCTION 29

IX. UNPATENTABILITY ANALYSIS 32

A. Overview of the Prior Art 32

1. Hongtao 32

2. Yu 36

3. Suzuki 37

4. Costa 40

5. Seo 42

B. *Ground 1*: Claims 1-6 Are Obvious Over Hongtao in View of Yu 44

1. Claim 1 44
2. Claim 2 59
3. Claim 3 62
4. Claim 4 66
5. Claim 5 81
6. Claim 6 90

C. Secondary Considerations of Non-Obviousness 171

I David Kuan-Yu Liu, Ph.D., declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. ("Micron") as an independent expert consultant in this proceeding before the United States Patent and Trademark Office ("PTO"). I am not an employee of Micron or of any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in the claims of U.S. Patent No. 11,468,957, which I refer to herein as the '957 Patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of $550 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My curriculum vitae ("CV") is included as Ex. 1004 and provides an accurate description of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

6. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

7. I worked on a novel Conductivity Modulated Power MOSFET for my Ph.D. thesis. The novel device uses a trench injector to facilitate an optimal tradeoff between the breakdown voltage and ON-Resistance of a Power MOSFET (Vertical DMOS) through the use of a minority carrier injector.

8. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration, device modeling, high-voltage CMOS process integration, and investigating a novel source-side injection mechanism for flash EPROM channel hot-electron programming. A source-side injection mechanism is one particular form of a hot carrier injection (HCI) mechanism.

9. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing flash cell and periphery devices in AMD's CMOS-based 0.5 μm and 0.35 μm flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology to accommodate x-decoder transistors and high voltage transistors for negative gate

erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

10. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices. This included various different types of memory, including NAND flash memory and embedded flash memory.

11. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

12. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75 nm CMOS technology node, a half node version between 90 nm and 65 nm).

13. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing embedded non-volatile memory process technology for power management product applications.

14. Since 2007, I have served as a technical consultant where I have provided expert advice regarding flash memory technology, CMOS process

technology, and semiconductor device physics. As part of this, I have considered, assessed, and assisted with the design of various different memory devices, including NAND flash and monolithic 3D memory structures.

III. ASSIGNMENT AND MATERIALS CONSIDERED

15. I have been asked to provide analysis and explain the subject matter of the ’957 patent, including the state of the art when the application underlying the ’957 patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the ’957 patent including how that art relates to the challenged claims of the ’957 patent and to provide my opinions regarding whether that art invalidates the claimed subject matter.

16. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the claims of the ’957 patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any applicable rule.

17. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the ’957 patent.

18. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of

scientific and engineering principles, and my experience. I have also reviewed and considered the '957 Patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials.

Exhibit	Description
1005	Chinese Patent Publ. No. 109065091 A to Hongtao Liu et al. (certified translation and original) ("Hongtao")
1006	U.S. Patent Publ. No. 2019/0198117 A1 to Yu et al. ("Yu")
1007	U.S. Patent Publ. No. 2021/0082505 A1 to Suzuki ("Suzuki")
1008	U.S. Patent Publ. No. 2018/0012667 A1 to Costa ("Costa")
1009	U.S. Patent Publ. No. 2021/0027848 A1 to Seo ("Seo")
1013	U.S. Patent No. 9,589,978 B1 to Yip
1014	Aritome, "NAND Flash Memory Technologies" (2016)
1015	Silvagni, "3D NAND Flash Based on Planar Cells," Computers 2017
1016	U.S. Patent Publ. No. 2020/0168276 A1 to Yang
1017	U.S. Patent No. 9,620,233 B1 to Dong et al.
1018	Micheloni, "3D Flash Memories" (2016)
1019	U.S Patent No. 9,361,993 B1 to Chen et al.
1020	U.S Patent No. 10,276,251 B1 to Lobana et al.
1021	U.S. Patent Publ. No. 2019/0348122 A1 to Ko et al.
1022	U.S. Patent Publ. No. 2013/0077404 A1 to Nawata et al.
1023	U.S Patent No. 10,121,529 B2 to Lee

Exhibit	Description
1024	U.S. Patent Publ. No. 2016/0293271 A1 to Won et al.
1025	U.S. Patent No. 11,600,342 to Chen et al.

IV. UNDERSTANDING OF THE LAW

19. I am not an attorney, but have been instructed in and applied the law as described in this section.

20. I understand that the first step in comparing an asserted claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the claims of the alleged invention in Section V below.

21. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

22. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show

simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

23. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

24. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

25. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

26. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

27. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

28. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

29. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

30. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

31. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

32. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a "nexus," between any such secondary indicia and the claimed invention.

33. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

34. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

35. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

36. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a POSITA is also a person of ordinary creativity.

37. In my opinion, a POSITA in the field of the '957 patent would have had a master's degree in electrical engineering or a similar discipline, along with 4-5 years of professional experience working with (e.g., researching, designing, or developing) NAND flash memory devices (including issues relating to the operation, e.g., reading of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

38. In my opinion, this POSITA would have been aware of and generally knowledgeable about NAND memory's structure, its component parts, how it operates, and how it is controlled.

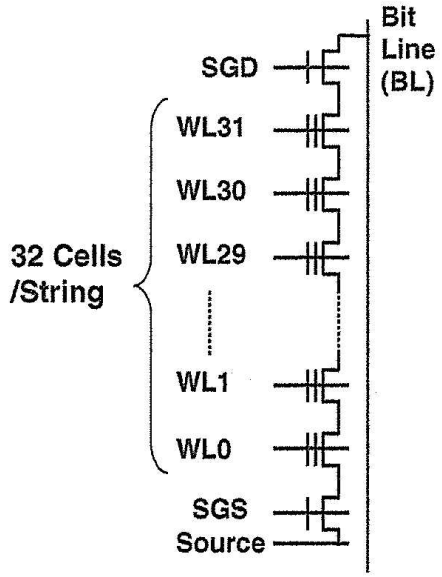
39. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile NAND flash memory—I was a person of more than the ordinary level of skill in the art as of December 15, 2020, which I have been asked to assume is the effective filing date of the '957 patent. In forming my opinions, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of an ordinarily skilled artisan.

VI. TECHNOLOGY BACKGROUND

40. This section provides technology background to the '957 patent.

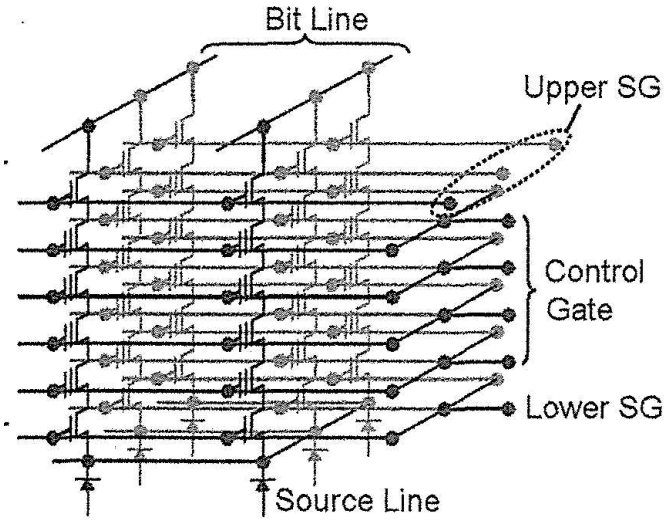
A. NAND Flash Structure

41. "Flash memory" is a form of "non-volatile memory." Ex. 1013, 1:24-26. Flash memory cells, e.g., NAND cells, are arranged in "strings" with multiple cells "connected in series." Ex. 1014, 38. The cells are surrounded by "select transistors (SGD, SGS)," one on the top (usually, drain side) and one on the bottom (usually, source side). *Id.*, 38-39. One such string is shown below.



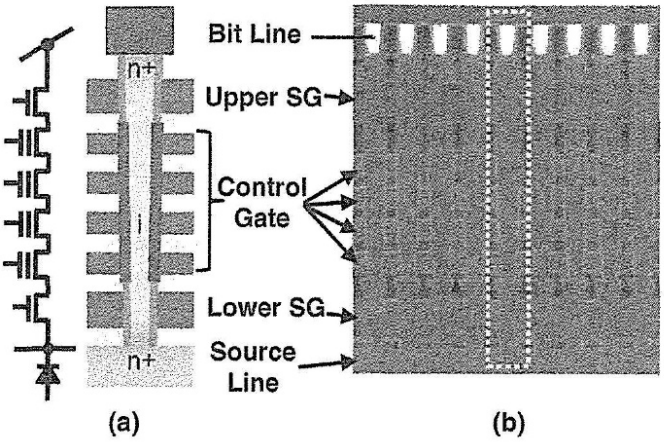
Id., 39.

42. Early NAND devices were formed as two-dimensional arrays of cells on a substrate surface. Ex. 1014, 38. But "three-dimensional (3D) NAND flash cells" were developed. *Id.*, 292. "Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1015, 3. Memory cells (comprising transistors) are formed vertically by stacking alternating layers of metal and dielectric (e.g., oxide such as SiO_2) around a cylindrical pillar. Ex. 1014, 294-95. Each metal layer acts as the control gate (gate terminal) of a transistor. *Id.*, 295. Multiple such vertical pillars/channels are then repeated in a three-dimensional array:

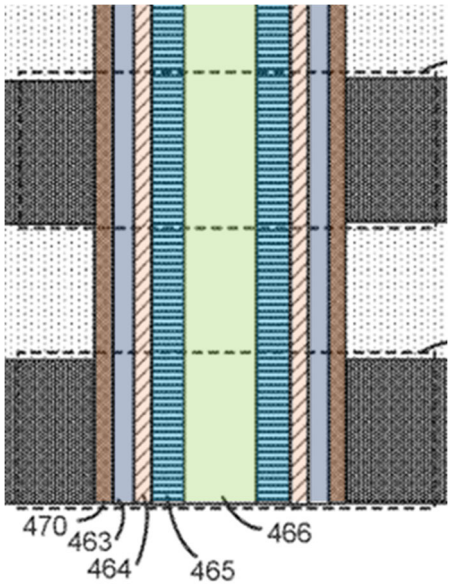


Id., 296. A particular vertical memory cell is selected using a word line and bit line, along with the select gates. *Id.*, 295-97.

43. An example 3D NAND vertical memory cell string with a charge-trapping layer is shown below:

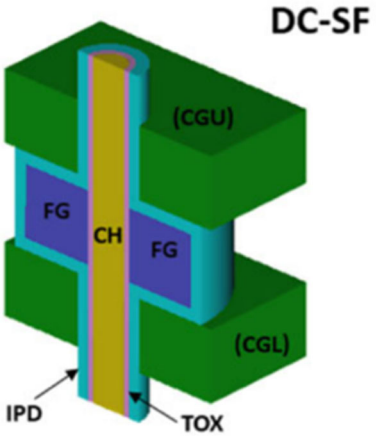


Ex. 1014, 296. The ONO sidewall of a memory-string pillar can comprise an oxide blocking layer (e.g., 470 below), a nitride charge-trapping or storage layer (463), and an oxide tunneling layer (464). Ex. 1016, [0083], Ex. 1017, 13:19-26.

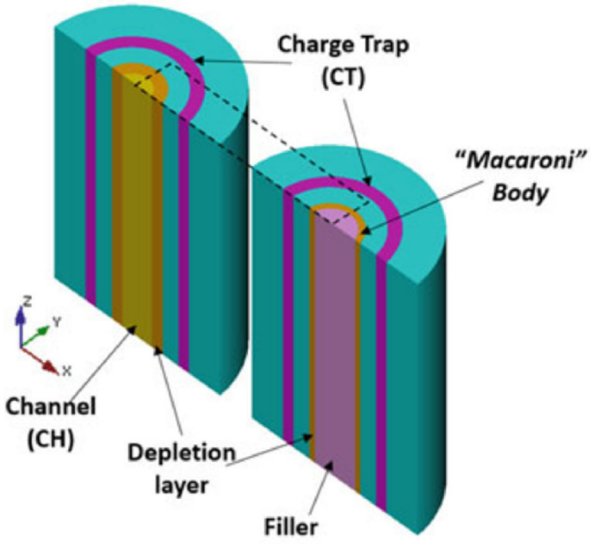


Ex. 1016, FIG. 4E (partial) (annotated).

44. The two most common types of 3D Flash memory cells are conductive floating gate memory cells and charge-trap memory cells. Because floating gates are conductive, the vertical memory string is made with separated floating gates:



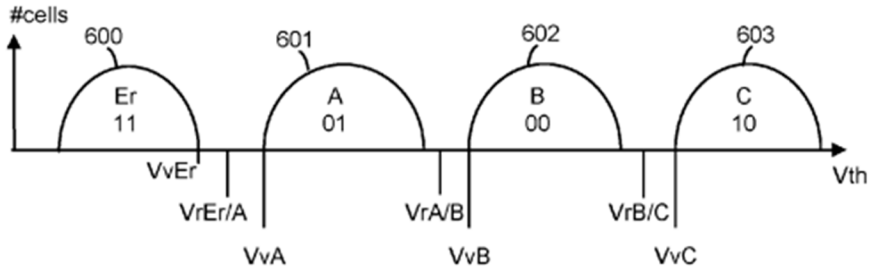
Ex. 1018, 145. Charge-trap technology, however, employs a non-conductive data storage portion, e.g., silicon nitride, and thus the charge-trap layer is not separated and merely extends through the entire vertical string:



Id., 106.

B. 3D NAND Flash Operation

45. A memory cell is programmed to store a data state (e.g., binary 00, 01, 10, or 11 for a cell designed to hold two bits) by storing some amount of charge in its charge-storage material using a programming operation. The threshold voltage (Vth) at which the cell transistor turns on increases "in proportion to the amount of stored charge." Ex. 1017, 13:43-49. A two-bit-per-cell NAND memory may have a Vth-versus-data-state distribution illustrated below:



Id., Fig. 6; *see also* Ex. 1014, 342-44 (Fig. 7.77 showing same). Unprogrammed cells have the erased Er state and a low Vth. Ex. 1017, 14:11-12.

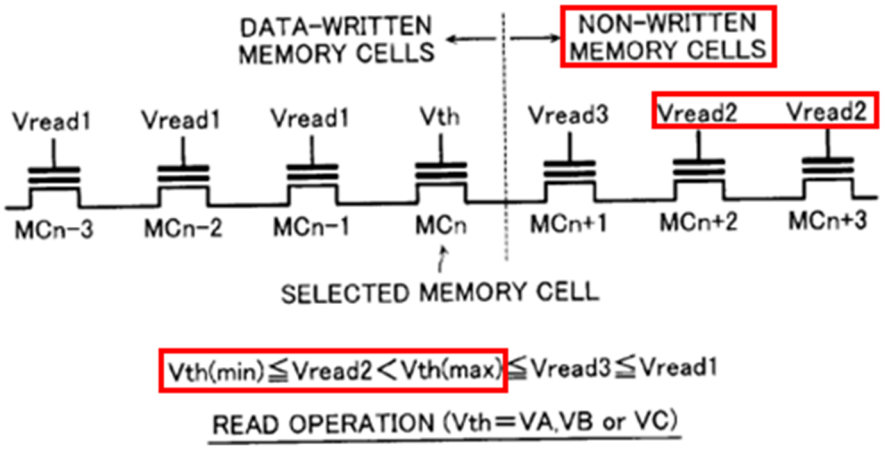
46. During read operations, all cell transistors on a selected memory string—except the selected cell to be read—can be given a control gate voltage, also known as a pass voltage, that is higher than the highest Vth of all possible data states to render the transistors conductive. Ex. 1017, 3:21-27, 3:33-37. A read voltage between two data states is applied to the control gate of the selected cell. *Id.*, 3:22-29, 14:31-34. If the read voltage is higher than the Vth of the selected cell, the cell transistor turns on and the memory string conducts current. Otherwise, the string does not conduct current. This process allows the threshold voltage of the selected cell to be measured and its data state to be determined. *Id.*, 3:10-11, 9:66-10:15, 14:34-37.

47. NAND device programming involves a cycle of two steps: a programming operation and a read (also known as verify) operation. For 3D NAND flash devices, the programming operation is typically done via incremental step pulse programming ("ISPP"). The ISPP process involves applying a voltage pulse

to a control gate of the selected word line—while simultaneously applying a pass voltage to unselected word lines—to inject electrons into a charge-storing part of the transistor. *See e.g.*, Ex. 1019, 11:47-49. Then, a read (verify) operation may be performed after the programming operation to verify correct programming of the memory cell, i.e., to determine whether the programming pulse was sufficient. Ex. 1020, 10:43-47; Ex. 1019, 11:50-52; Ex. 1017, 10:47-49. This verify operation can be identical to the read operation described above (using a verify voltage). Ex. 1021, [0103]; Ex. 1020, 16:16-21; Ex. 1019, 17:10-14; Ex. 1017, 3:21-29. ISPP will stop if the verify operation confirms that the memory cell has been programmed to a correct threshold voltage. Ex. 1019, 11:27-32. Otherwise, the ISPP process will continue until a proper threshold voltage has been reached. Cells on a memory string are typically programmed from one end to the other, i.e., from source side to drain side, or vice versa. Ex. 1014, 45 (Fig. 2.12); Ex. 1021, [0110]-[0112].

48. Data storage using NAND flash is subject to various influences, such as data-retention degradation and read disturb, that reduce its reliability. Ex. 1014, 28. Read disturb can occur when read operations repeatedly apply high pass voltages on unselected word lines, which induces a boosting effect called hot-carrier injection ("HCI"). *Id.*, 254. "To limit read disturb on unselected word lines during sensing, the value of [pass voltage] may generally be set as low as possible to ensure that the memory cells are conductive and appropriately act as pass gates." Ex. 1008, [0096].

Accordingly, a lower pass voltage may be applied to unprogrammed cells since they have low threshold voltages. Ex. 1022, [0055]-[0062].



Id., Fig. 6.

VII. THE '957 PATENT

A. Effective Filing Date

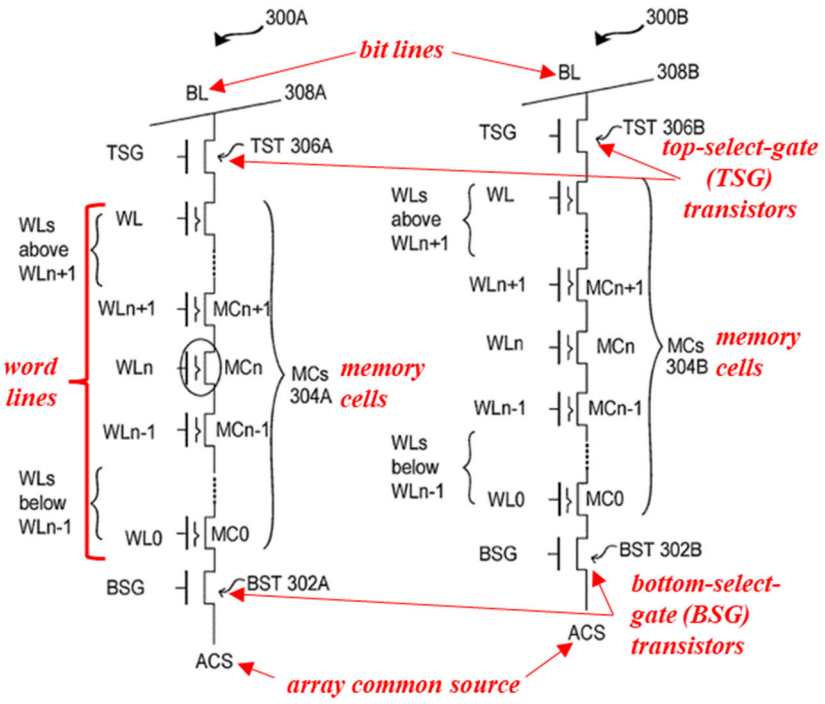
49. I understand that the application leading to the '957 patent was filed on March 4, 2021. Based on my review of the '957 patent, I note that it also references a PCT application on its face, which was filed December 15, 2020. For purposes of this declaration, I have been instructed to assume that December 15, 2020 is the effective filing date of the '957 patent.

50. My opinions in this declaration were formed from the perspective of a POSITA as of December 15, 2020, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the '957 patent and the prior art.

B. Overview

51. The '957 patent's alleged objective is to reduce HCI-induced read disturb on 3D NAND flash devices by including a pre-verify stage (a stage before the verify operation). Ex. 1001, 1:44-49, 17:7-17. I discuss HCI in §IX.A.1. The claims, however, do not recite reducing HCI and, instead, refer to the application of various voltages that I describe below.

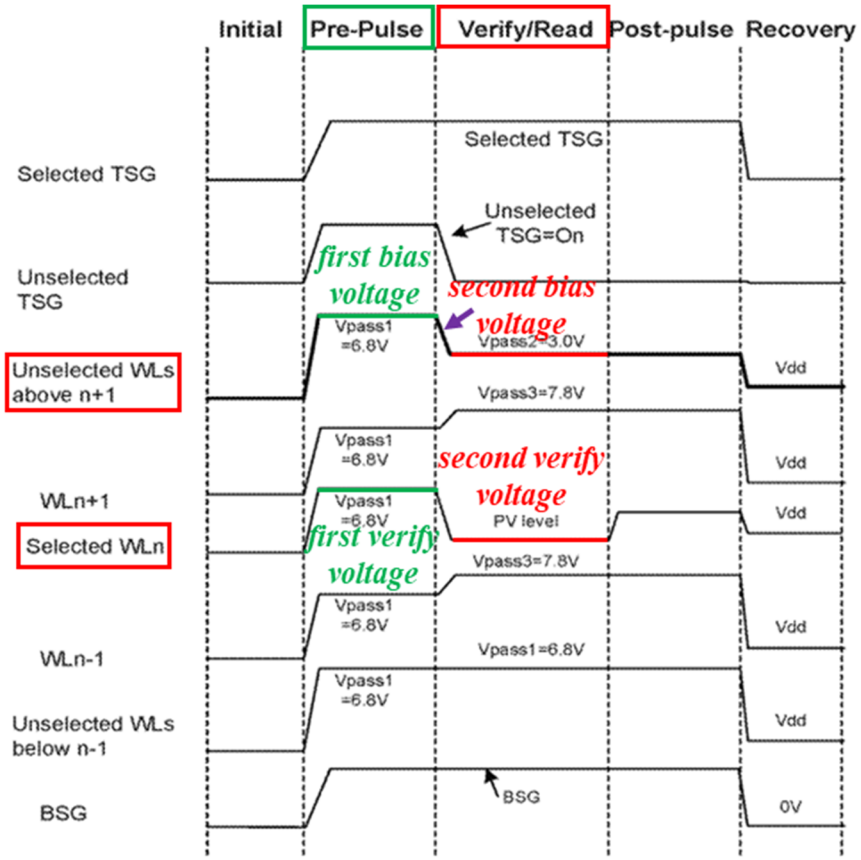
52. First, the '957 patent is in the context of a conventional NAND memory array configuration with NAND strings that include top and bottom select gates:



Ex. 1001, Fig. 3, *id.* 9:3-30. I discuss this conventional structure in §VI.A.

53. The '957 patent teaches applying verify and bias voltages to a selected cell and to an unprogrammed cell, respectively, during a pre-verify (or pre-pulse)

stage and a verify (or read) stage, wherein the bias voltage on the unprogrammed cell in the verify stage is lower than the voltage in the pre-verify stage, as indicated by a purple arrow below. Ex. 1001, Abstract, 6:50-7:12, 12:63-13:4, 14:19-30, 15:18-30. Note that while the claim refers to applying voltages to the selected and unselected memory cell, that voltage is actually applied to the respective word lines, which connect to the respective memory cells.



Id., Fig. 6; *see also id.*, Figs. 7-9 (same).

54. In this embodiment, the first and second bias voltages and the first verify voltage are set sufficiently high to turn on the corresponding cells. Ex. 1001,

11:12-15. As I discuss in the claim mapping section, however, the '957 patent describes verify and bias voltages that are 0 volts. The second verify voltage is set to "program verify (PV) level" for determining whether the threshold voltage of the selected cell is above or below the PV level. *Id.*, 11:35-39; *supra* §VI.B.

55. The verify stage is the sensing stage. And the second verify voltage is the read verify or read voltage. The sensing determines whether the selected memory cell's threshold voltage is above or below the second verify voltage. Note that even though the '957 patent refers to the "first verify voltage," this is not a voltage that verifies anything. In other words, the pre-verify stage does not function to verify any data state of the selected memory cell. Instead, the pre-verify stage assists in preparing for the actual verify (or sensing) stage.

56. I also note that claims 1 and 4-6 repeatedly recite "apply[ing]" a voltage "on a gate terminal" of a memory cell or a top-select-gate ("TSG") or bottom-select-gate ("BSG") transistor. Ex. 1001, 17:41-56, 18:13-30, 18:35-45, 18:48-58. Like its reference to applying a voltage to a memory cell, the respective voltage is applied through a conductor coupled to the corresponding cell or transistor, i.e., a word line coupled to a corresponding memory cell (which in 3D memories, is actually a conductive gate layer). The voltage applied to the gate terminal controls the cell or transistor, e.g., to turn it on or off.

C. Prosecution History

57. As noted above, I have reviewed the '957 patent's prosecution history.

58. The '957 patent was filed on March 4, 2021, as U.S. application 17/191,768. Ex. 1001, Cover. The application was subject to a restriction/election requirement. Ex. 1002, 212-217. In response, Applicant elected pending claims 15-20, which issued as claims 1-6 without rejection. *Id.*, 220-221.

D. Claims

59. For reference, claims 1-6 of the '957 patent are reproduced below:

> **1**. An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising:
>
> processing circuitry configured to:
>
> apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;

apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and

apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.

2. The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string.

3. The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string.

4. The apparatus of claim 1, wherein the processing circuitry is further configured to:

in the pre-verify stage,

apply a first gate voltage on a gate terminal of the TSG transistor of the second memory cell string,

apply a first pass voltage on a gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and

apply a first read voltage on a gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string; and

in the verify stage,

apply a second gate voltage on the gate terminal of the TSG transistor of the second memory cell string,

apply a second pass voltage on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and

apply a second read voltage on the gate terminal of the second adjacent memory cell of the selected memory cell of the first memory cell string, wherein

at least one of the second pass voltage and the second read voltage is larger than the second gate voltage.

5. The apparatus of claim 2, wherein the processing circuitry is further configured to:

apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

6. The apparatus of claim 3, wherein the processing circuitry is further configured to:

apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

apply a positive voltage on gate terminals of any memory cells that are positioned between the first adjacent memory cell of the selected memory cell and

the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

VIII. CLAIM CONSTRUCTION

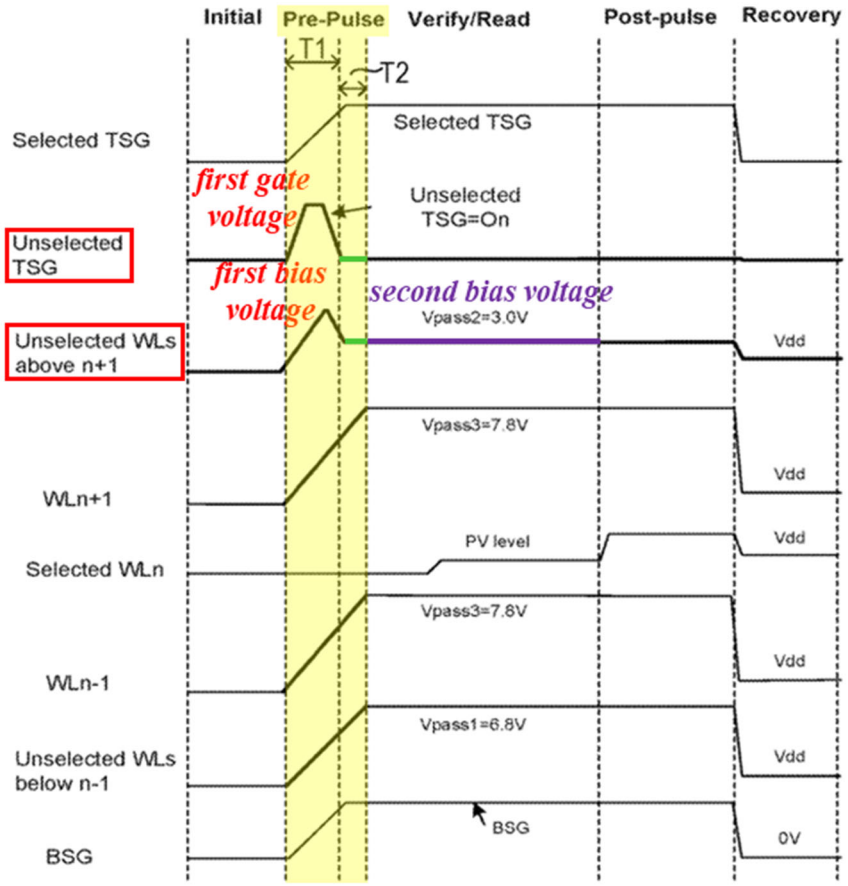
60. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

61. I have been informed that the words of a claim are generally given the ordinary and customary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification, and the file history (collectively, the "intrinsic evidence" or "intrinsic record").

62. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the "extrinsic evidence" or the "extrinsic record"), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

63. Relevant to my analysis is how the '957 patent uses the claim language of "apply[ing]" voltages "in" a "pre-verify" and/or "verify stage." Here, I discuss how the '957 patent uses these terms.

64. The '957 patent uses that language to mean that at some point during a given stage, a voltage is applied. The voltage does not need to be applied during the entire period. This is consistent with the plain and ordinary meaning of this claim language. This is evident from claims 1 and 4. For example, the claimed first bias voltage and the claimed first gate voltage are not applied throughout the pre-pulse (pre-verify) stage. Instead, as shown below, these voltages are clearly not applied during the entire pre-verify stage, because the voltages start to ramp down before the end of the pre-verify stage ("pre-pulse"):



Ex. 1001, Fig. 7, 13:11-25, 17:33-42.

65. Moreover, as shown above, claim 1's limitation that "the second bias voltage is smaller than the first bias voltage" does not require the second bias voltage during the verify stage to be smaller than the first bias voltage for the entire duration of the pre-verify stage. As can be seen, the first bias voltage is 0 volts at the start of the pre-verify period.

IX. UNPATENTABILITY ANALYSIS

66. For the reasons I explain in greater detail below, it is my opinion that claims 1-6 of the '957 patent are unpatentable as obvious over the prior art discussed in this declaration.

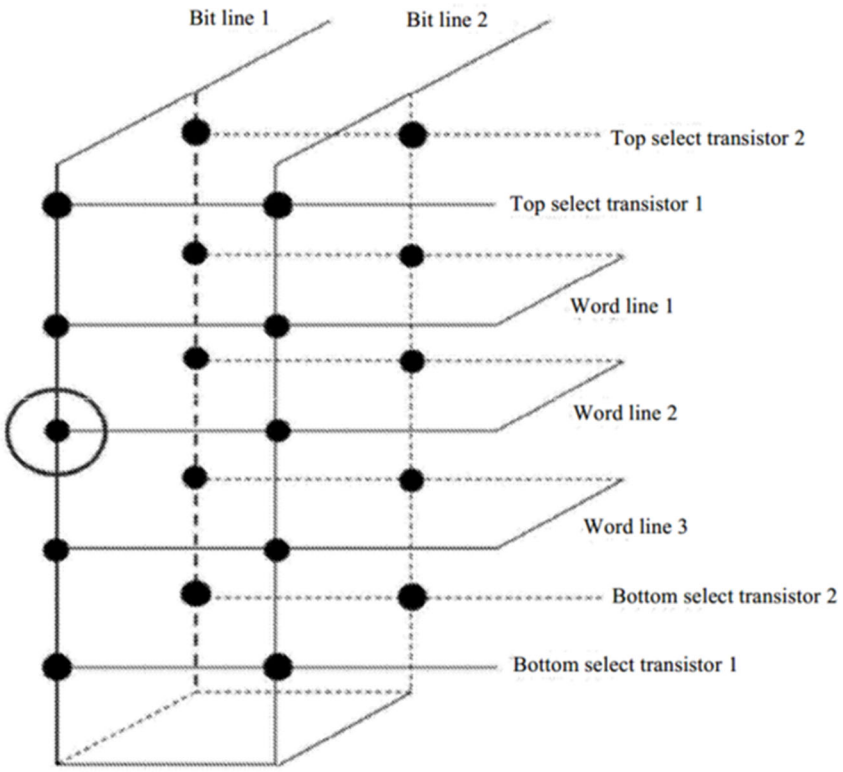
A. Overview of the Prior Art

67. The following paragraphs provide an overview of the main prior art references I discuss throughout this declaration.

1. Hongtao

68. Chinese Patent Publ. No. 109065091A ("Hongtao") was filed on August 1, 2018, and was published on December 21, 2018. Ex. 1005, Cover. I understand that this Patent is assigned to the Patent Owner. I did not observe Hongtao being disclosed during the prosecution of the '957 patent. I understand that Hongtao is prior art to the '957 patent under 35 U.S.C. §102(a)(1) (AIA).

69. Hongtao is directed to read operations of nonvolatile 3D NAND flash memory. Ex. 1005, Abstract, [0001]. Hongtao depicts at a very high-level a conventional 3D NAND array. The illustration below shows memory strings with top and bottom selects gates. I should note that the below illustrations is clearly just for explanatory purposes, because memory strings at the time included dozens, if not more, of memory cells.

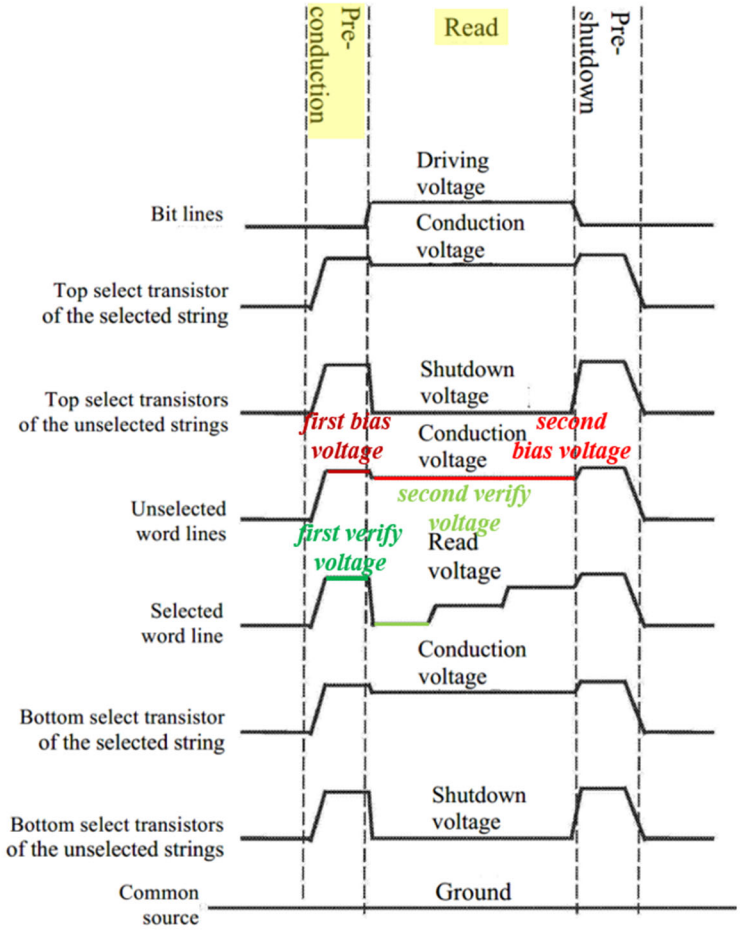


Id., Fig. 1.

70. Hongtao is directed to reducing HCI induced by high pass voltages in read operations. Ex. 1005, [0003]-[0004], [0020], [0023]; *supra* §VI.B. I discuss HCI in Section §IX.A.1.

71. Hongtao's approach involves two time periods (or two "stages," as Hongtao calls them). These stages are a "pre-conduction phase" and a "read phase." The pre-conduction phase is basically a step that prepares for the sensing operation. And the read phase is the actual sensing phase in which the selected memory cell is read or verified.

72. To reduce HCI, the channels of unselected strings and the selected string are kept "pre-conditioned" at 0V during the pre-conduction phase. This locking of the channel of the unselected string at 0V will remain in effect even during the sensing phase when the channel of the unselected string is disconnected from the bit line. Ex. 1005, [0022]-[0024]. As shown below, Hongtao's waveform matches the '957 patent claims:



Id., Fig. 2.

73. As can be seen above, Hongtao applies a conduction voltage on unselected word lines that is lower than the pre-conduction voltage. Hongtao explains why: "the greater the conduction voltage, the greater the read disturbance to the memory cell." Ex. 1005, [0026]. It was known that high pass voltages during the sensing phase can cause read disturbance problems.

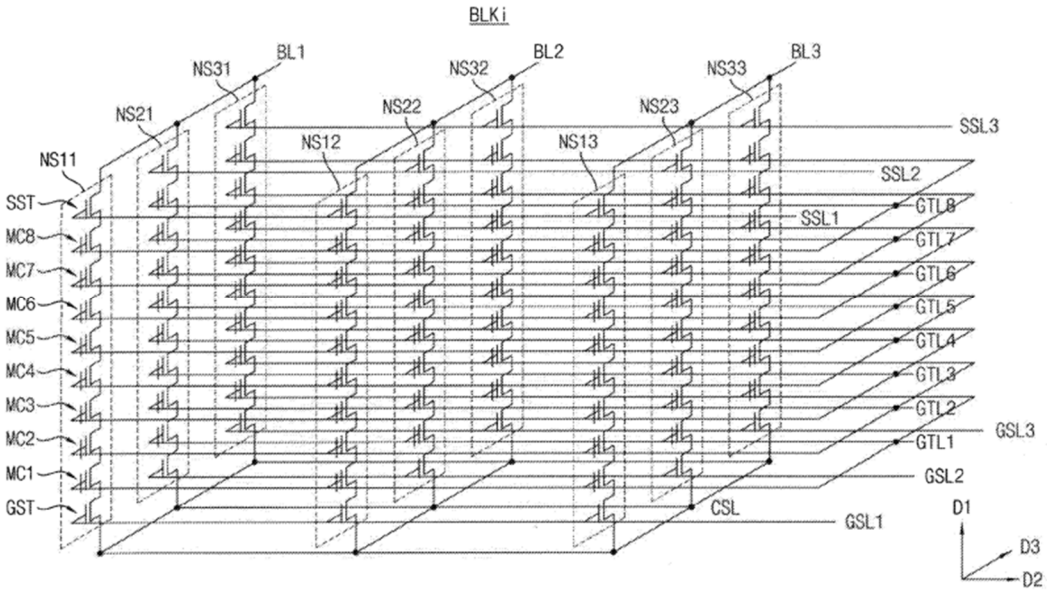
74. Read disturb can be caused by two different physical mechanisms: one due to a high vertical electrical field, perpendicular to the channel, across a given memory cell that causes unintentional F-N injection; and one due to a high electric field parallel with the channel of a given memory cell that causes hot carrier injection (HCI). The F-N type of disturb tends to occur on the selected string when the channel is biased at 0V or at a low bit line voltage. The HCI disturb tends to occur on an unselected memory string whose channel is disconnected from the bit line voltage. In this situation, read disturb can occur when read operations repeatedly apply high pass voltages on unselected word lines, which induce a boosting effect of the channel potential, leading to hot-carrier injection ("HCI").

75. In summary, Hongtao attempts to reduce the HCI induced read disturb on the unselected strings by locking the channel voltage during the pre-conduction period, while also being cognizant of the "conduction voltage" on the unselected word lines not causing read disturb on the selected string due to the voltage difference of (conduction voltage – driving voltage) perpendicular to the channel.

2. Yu

76. U.S. Patent Publ. No. 2019/0198117A1 ("Yu") was filed on September 25, 2018, and was published on June 27, 2019. Ex. 1006, Cover. Yu claims priority to a Korean application KR10-2017-0178312 filed on December 22, 2017. I understand that Yu is prior art to the '957 patent under 35 U.S.C. §§102(a)(1)-(2) (AIA).

77. Yu relates to programming 3D NAND memory devices. Ex. 1006, Abstract, [0004]. Yu's devices have a conventional structure. Again, as can be seen below, Yu employs the basic memory string architecture in which the strings include bottom and top select gates.



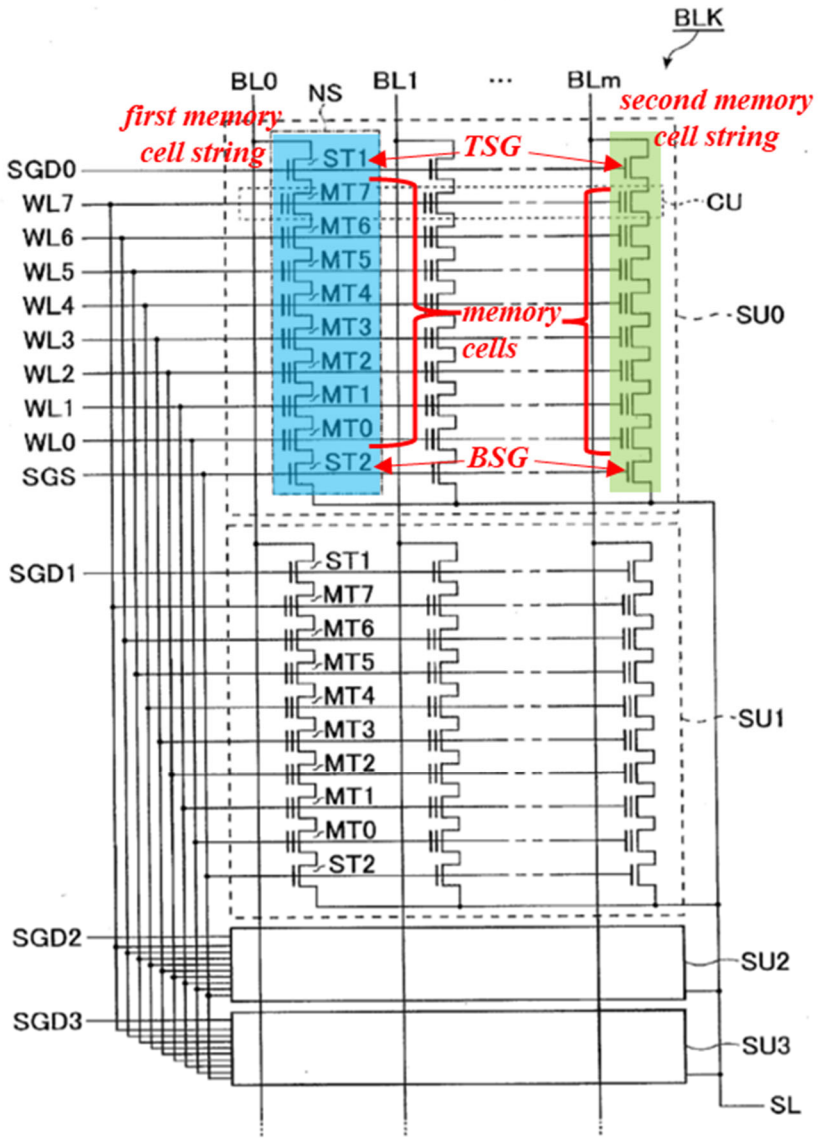
Id., Fig. 6.

78. Yu discloses that programming may proceed from the source end to the drain end of a string, or vice versa. Ex. 1006, [0115], [0130]. Typically, the source end is on the bottom. There are typically source regions in the substrate, and thus the bottom side is the source side. The top is the drain end. I discuss in more detail programming in a sequential order (from bottom to top, or from top to bottom) in Sections IX.B.1.[1.A.ii], IX.B.3, and IX.B.7. I note that sequential programming was conventional and had well known benefits.

3. Suzuki

79. U.S. Patent Publ. No. 2021/0082505A1 ("Suzuki") was filed on July 13, 2020, and was published on March 18, 2021. Ex. 1007, Cover. Suzuki claims priority to a Japanese application 2019-168394 filed on September 17, 2019. I understand that Suzuki is prior art to the '957 patent at least under 35 U.S.C. §102(a)(2) (AIA).

80. Suzuki discloses a 3D NAND flash memory of a conventional structure. Ex. 1007, [0003]. Again, the memory strings include top (or drain) and bottom (or source) select gates.

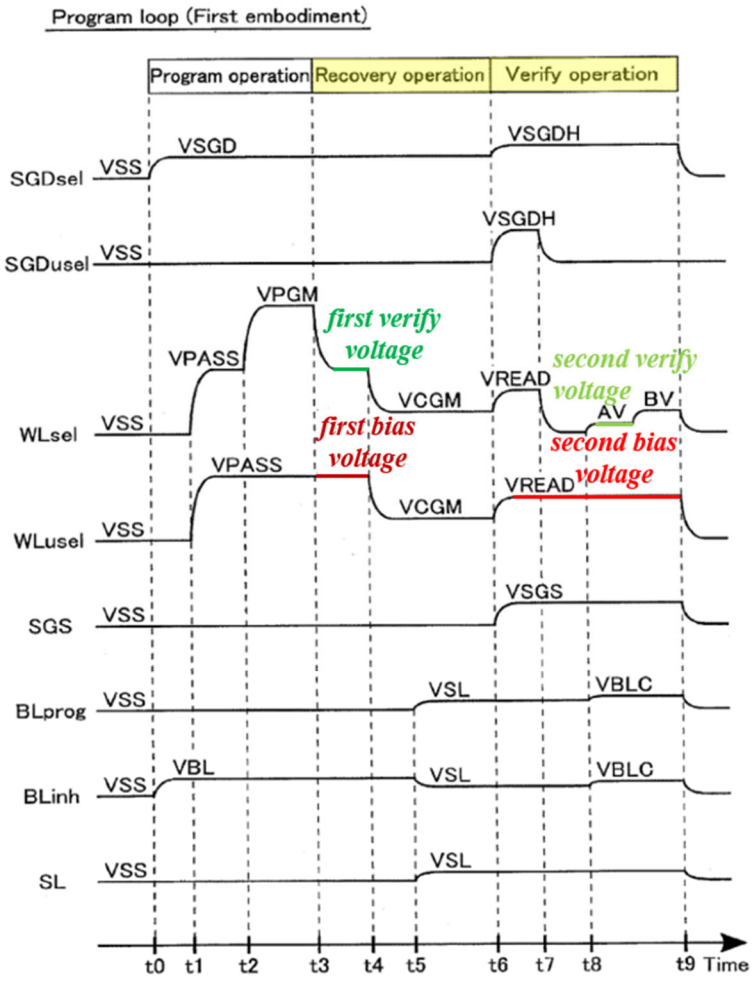


Id., Fig. 2, [0047]-[0050]; *see also id.*, Fig. 7.

81. Suzuki further discloses the basic programming sequence that I discuss in §IX.B.1.[1.A.ii] and §IX.B.3. Specifically, Suzuki discloses sequentially: a program operation, a recovery operation, and a verify operation. Ex. 1007, Abstract. The program operation is a pulse that creates charge in the storage region and the

verify operation determines whether the pulse was sufficient to properly program the cell.

82. Suzuki recognizes that read-back errors result from post-verify threshold-voltage drift caused by carrier de-trapping. Ex. 1007, [0148]-[0152]. Suzuki reduces such errors by applying control voltages to facilitate de-trapping in the recovery operation. *Id.*, [0153]. In short, this will expedite the de-trapping, so when the verification occurs, there will not be post-verify threshold voltage drift. Suzuki discloses the claimed '957 waveforms:

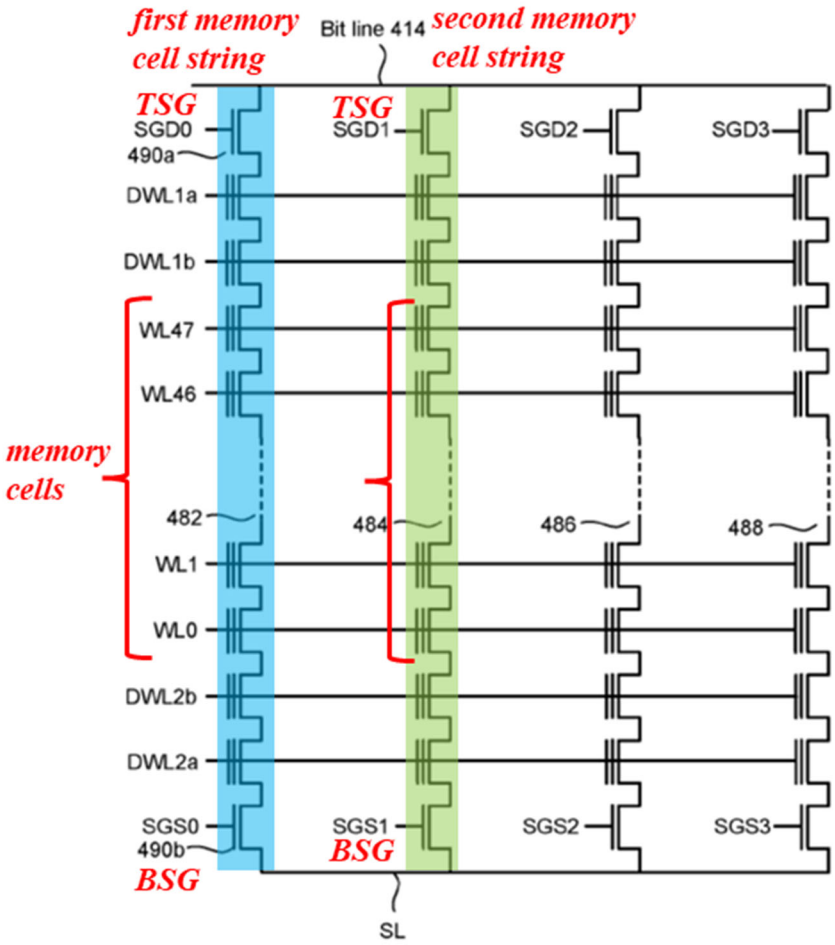


Id., Fig. 11.

4. Costa

83. U.S. Patent Publ. No. 2018/0012667A1 ("Costa") was filed on July 7, 2016, and was published on January 11, 2018. Ex. 1008, Cover. I understand that Costa is prior art to the '957 patent under 35 U.S.C. §§102(a)(1)-(2) (AIA).

84. Costa discloses a NAND flash memory device of a conventional structure. Again, the memory strings include a top (or drain) select gate and a bottom (or source) select gate:



Ex. 1008, Fig. 4F, [0077].

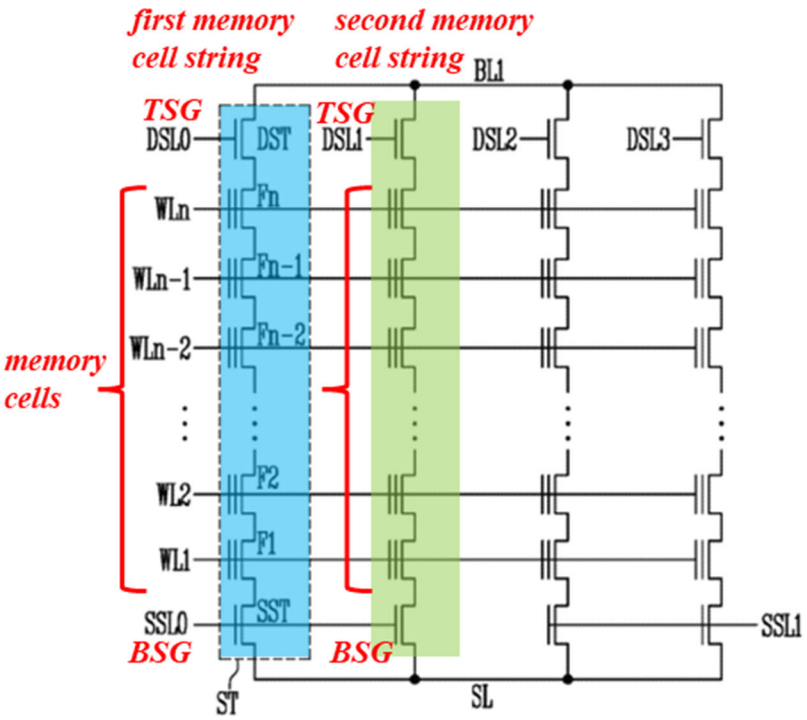
85. Costa discloses that channel resistance increases as more memory cells are programmed. Ex. 1008, Abstract. Channel resistance of the memory string can be considered as the sum of the channel resistance of each memory cell in the string when the string is conducting, with the channel resistance of each memory cell

increasing as that memory cell is programmed to a higher Vt. To reduce the adverse impact, Costa teaches a technique that uses a low read pass voltage on unprogrammed cells. *See, e.g.*, *id.*, cl. 5.

5. Seo

86. U.S. Patent Publ. No. 2021/0027848A1 ("Seo") was filed on October 18, 2019, and was published on January 28, 2021. Ex. 1009, Cover. I understand that Seo is prior art to the '957 patent under 35 U.S.C. §§102(a)(1)-(2) (AIA).

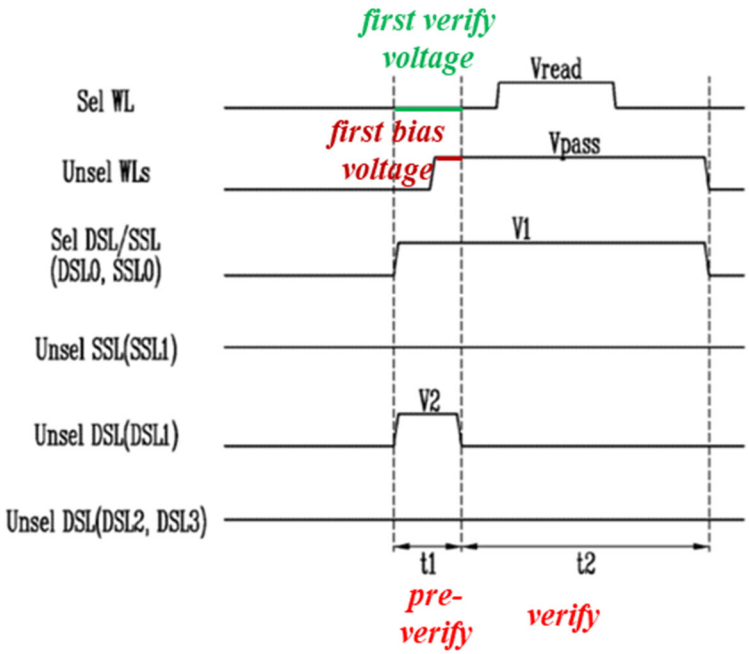
87. Seo relates to 3D NAND flash memory with a conventional structure. Ex. 1009, Abstract, [0004]-[0007]. Again, the memory strings include a top (or drain) select gate and a bottom (or source) select gate:



Id., Fig. 4; *see also id.*, [0053]-[0059].

88. Seo is focused on reducing HCI occurring on unselected memory strings during read operations. Ex. 1009, [0008]. I discuss HCI in §IX.A.1.

89. Seo reduces HCI by applying voltages in a time period t1 before the read operation that match the claimed '957 voltages. Ex. 1009, [0088]-[0089]. A POSITA would recognize that, just like Hongtao and the '957 patent, Seo is locking the channel voltage of the unselected memory string during the pre-verify period, with the exception that the channel voltage of the memory cells above the selected WL are pre-conditioned to the bit line voltage, while the channel voltage of the memory cells below the selected WL are pre-conditioned to 0V, due to the fact that the selected WL is biased at 0V.



Id., Fig. 8.

B. *Ground 1*: Claims 1-6 Are Obvious Over Hongtao in View of Yu

90. In my opinion, a POSITA would have considered Hongtao and Yu to be within the scope of the prior art and highly relevant to the patentability of the '957 patent's claims.

91. In my opinion, Hongtao in view of Yu and the knowledge of a POSITA renders claims 1-6 obvious.

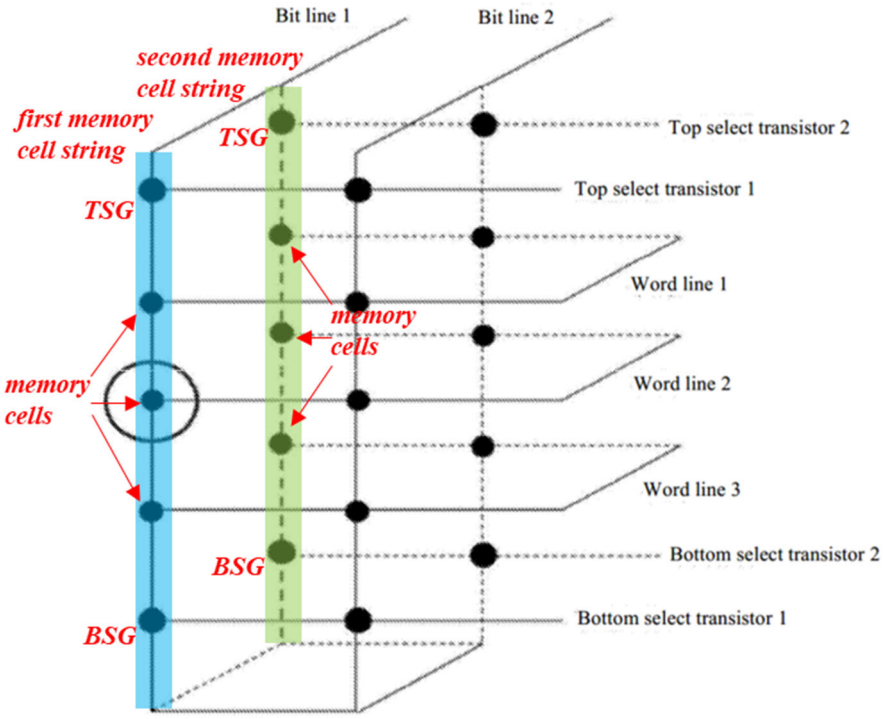
1. Claim 1

[1.PRE] "An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising:"

92. In my opinion, to the extent the preamble is limiting, Hongtao discloses, or at least renders obvious, the preamble.

93. Hongtao discloses "a reading method of 3D NAND flash memory." Ex. 1005, Abstract. This NAND flash is *an apparatus for reading a memory device*. This NAND flash, while shown at a very high-level, is conventional in nature. It includes multiple memory strings such as *a first memory cell string* (highlighted blue) *and a second memory cell string* (green):[1]

[1] For clarity, I use red italics in the claim-mapping sections to indicate claim language.



Id., Fig. 1, [0006], [0017], [0018].

94. As with a conventional 3D NAND memory, it includes a "top select transistor" (typically the drain side) (*a top-select-gate (TSG) transistor*) and "bottom select transistor" (typically source side) (*a bottom-select-gate (BSG) transistor*), with *memory cells* that are *connected in series*. Ex. 1005, [0018]. In practice, these 3D NAND memory strings are a pillars made with continuous layers.

95. I note that this illustration is clearly for explanatory purposes. 3D NAND devices at the time had dozens of memory cells.

[1.A] "processing circuitry configured to:"

96. Hongtao discloses, or at least renders obvious, *processing circuitry*.

97. *Processing circuitry* is simply the circuitry that applies the claimed voltages. Ex. 1001, 4:25-36, 16:55-60.

98. As I discuss in detail in this Ground, Hongtao discloses applying various voltages as the claims require. *Infra* §§IX.B.2.[2].[1.A.i]-IX.B.1.[1.A.iv]. Hongtao discloses, and would have been understood to disclose, *processing circuitry* to apply these voltages. In the other grounds, I discuss this circuitry. §§IX.B.3.[3].[1.A], IX.D.1.[1A]. Yu, as an additional example, also discloses such conventional circuitry required to operate memory cell arrays. Ex. 1006, Fig. 3, [0045]-[0059]. For example, there must be circuitry to generate the voltages, such as charge-pumps, and there are decoders that identify the appropriate rows to apply the voltages. By Hongtao disclosing different voltages, selected word lines, and unselected word lines, Hongtao would have been understood to disclose such *processing circuitry*.

99. It would have at least been obvious that Hongtao discloses *processing circuitry*, in view of a POSITA's knowledge or in view of Yu, for the reasons above. Such circuitry was conventional and routine to implement. §§IX.B.3.[3].[1.A], IX.D.1.[1A]. Practically speaking, this basic circuitry is the only way that such

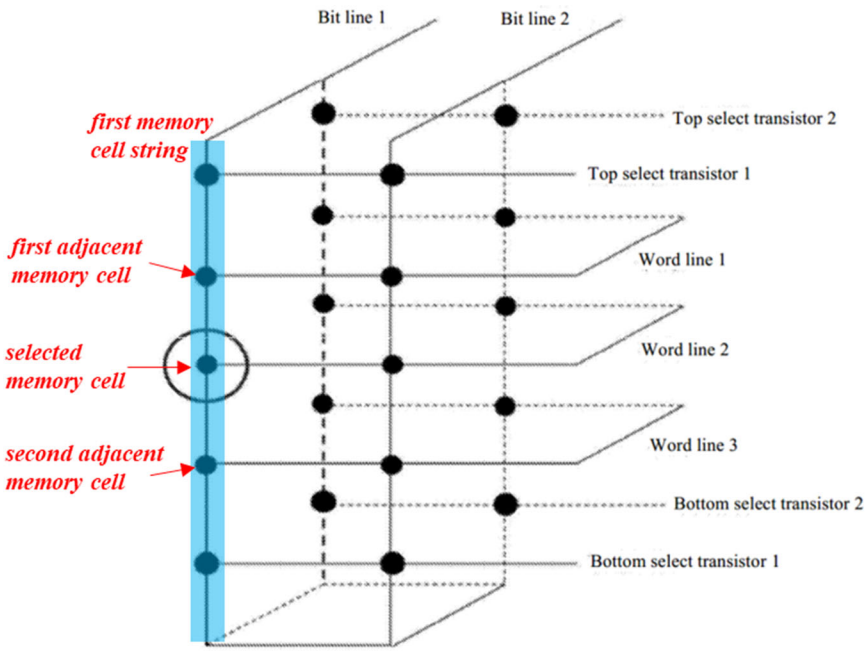
semiconductor devices can deliver these voltages to the various word lines and other elements of the device.

[1.A.i] "apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;"

100. Hongtao in view of Yu renders this limitation obvious.

101. I note here for clarity that A.i and A.iii both relate to the *selected memory cell* that is *programmed*.

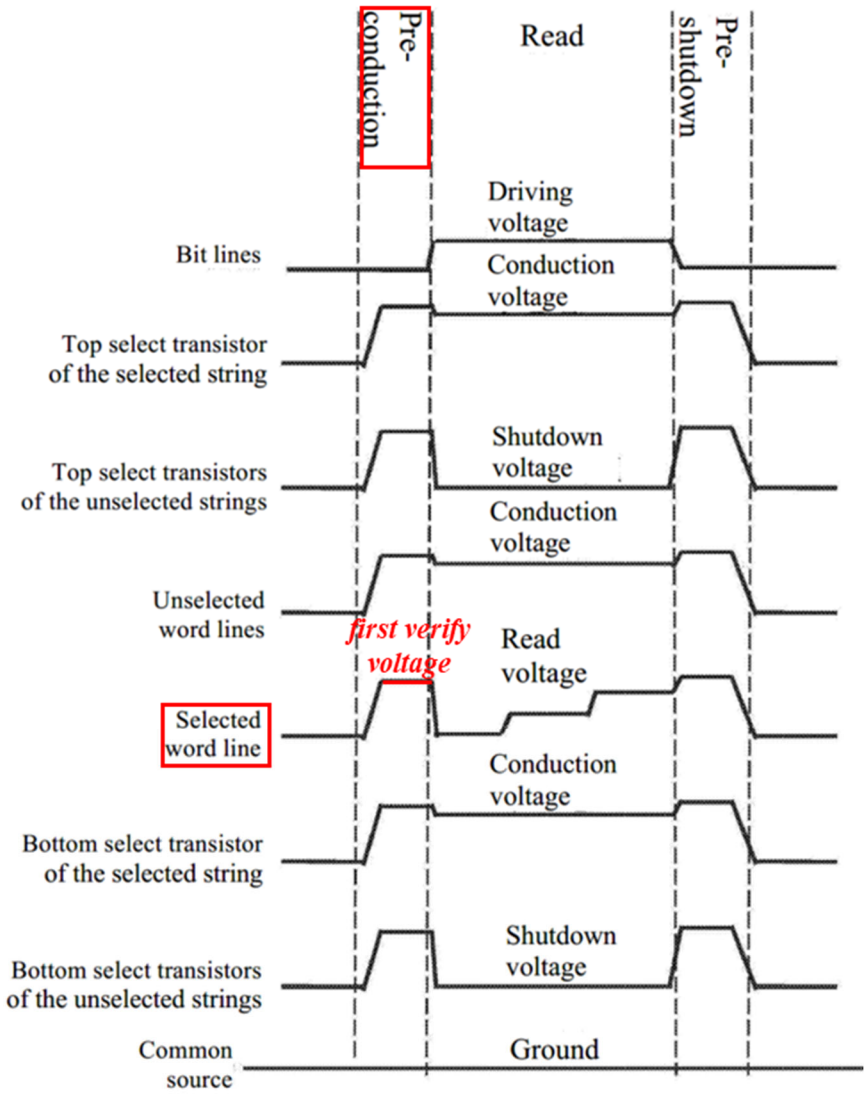
102. Hongtao discloses "read[ing] … the *selected memory cell* circled in Figure 1." Ex. 1005, [0019]. The *selected memory cell*, e.g., coupled to word line 2, is positioned between adjacent memory cells. Note that it is selected using word line 2 and bit line 1, as was conventional. §VI.A.



Ex. 1005, Fig. 1.

103. I discuss the program-read (verify) loop in §IX.B.7. Again, the read (verify) occurs after the program to verify whether the program operation was successful. Thus, when using Hongtao's read operation to verify program operations, the same selected cell is programmed and then verified. In other words, when the *selected memory cell* is being verified, it is *programmed*. As I discuss in §IX.B.7., it would have been obvious to employ Hongtao's read for program verification. *See* §IX.B.7. In fact, a POSITA would have understood from reading Hongtao alone that its read is applicable to a verify, because that is a basic application of a read operation. §VI.B.

104. Hongtao discloses that the selected cell to be read is connected to the selected word line. Ex. 1005, [0022]; *see also* §VI.B (word line-memory cell coupling). Hongtao further discloses applying "a pre-conduction voltage … to the selected word line" in a "pre-conduction phase." Ex. 1005, [0008], [0023].



Id., Fig. 2.

105. The pre-conduction phase precedes the read/verify phase. Ex. 1005, claim 1, [0022]. Like the "pre-verify" stage of the '957 patent, this stage assists in preparing for the read (sensing) stage. And like the first verify voltage of embodiments of the '957 patent, the pre-conduction voltage turns on the channel. Ex. 1001, 11:12-15; Ex. 1005, [0023]. Thus, this "pre-conduction voltage"

constitutes *a first verify voltage on … a selected memory cell, appl[ied] in a pre-verify* (pre-conduction) *stage*.

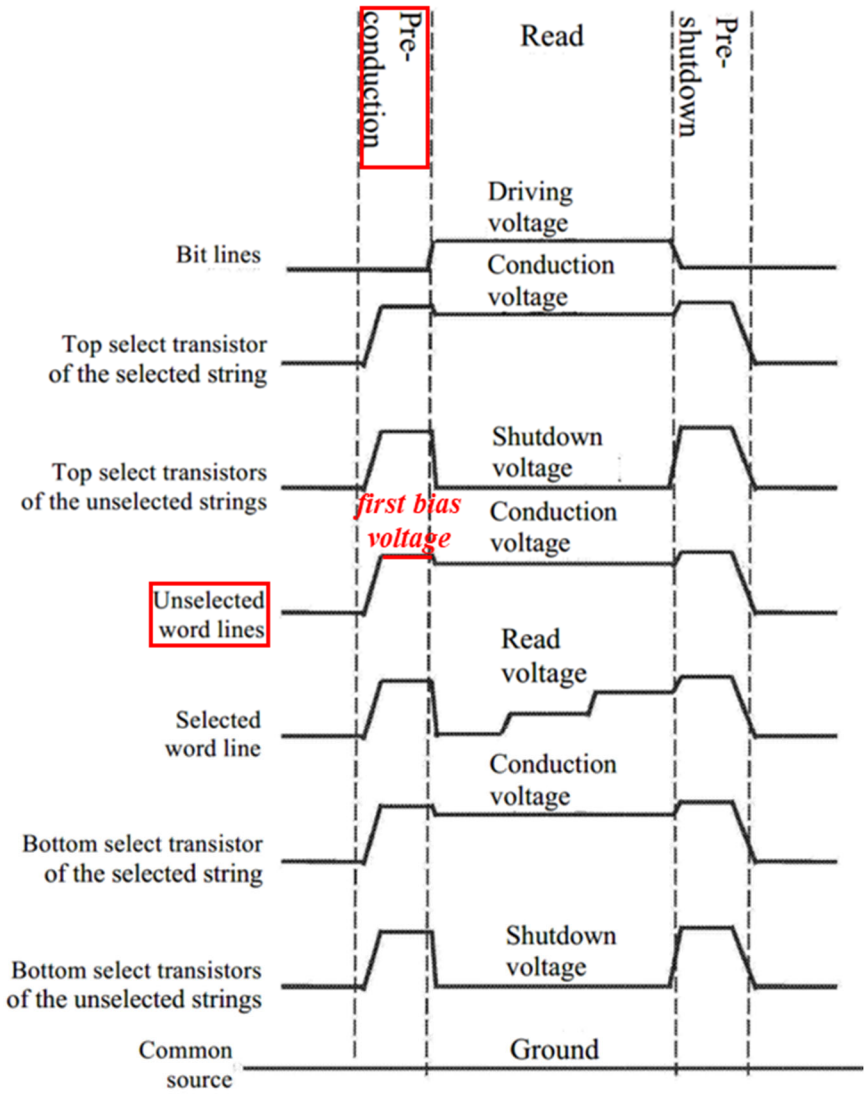
106. Relatedly, a POSITA would have understood that the '957 patent's use of the term a "verify voltage" in the pre-verify stage is a misnomer, because verification (reading) does not occur in that stage. Rather, verification occurs in the verify stage. The voltages applied during the pre-verify stage are intended, according to the patent, to pre-condition the memory device before actual verification (reading) operation to mitigate HCI. Ex. 1001, 6:50-65, 11:58-12:9.

[1.A.ii] "apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;"

107. Hongtao in view of Yu renders this limitation obvious.

108. I note here for clarity that A.ii and A.iv both relate to the *not programed memory cell*. This corresponds to a different word line that does not couple to the *selected memory cell*. But the claim requires that this different word line couple to a memory cell that is specifically *not programmed*.

109. Hongtao discloses applying "a pre-conduction voltage … to … unselected word line[s]" "in the pre-conduction stage." Ex. 1005, [0023], *see also id.*, [0008]. Here, "unselected word line[s]" means that these are not the selected word line, i.e., the cells to which these word lines couple are not the target of the access operation.

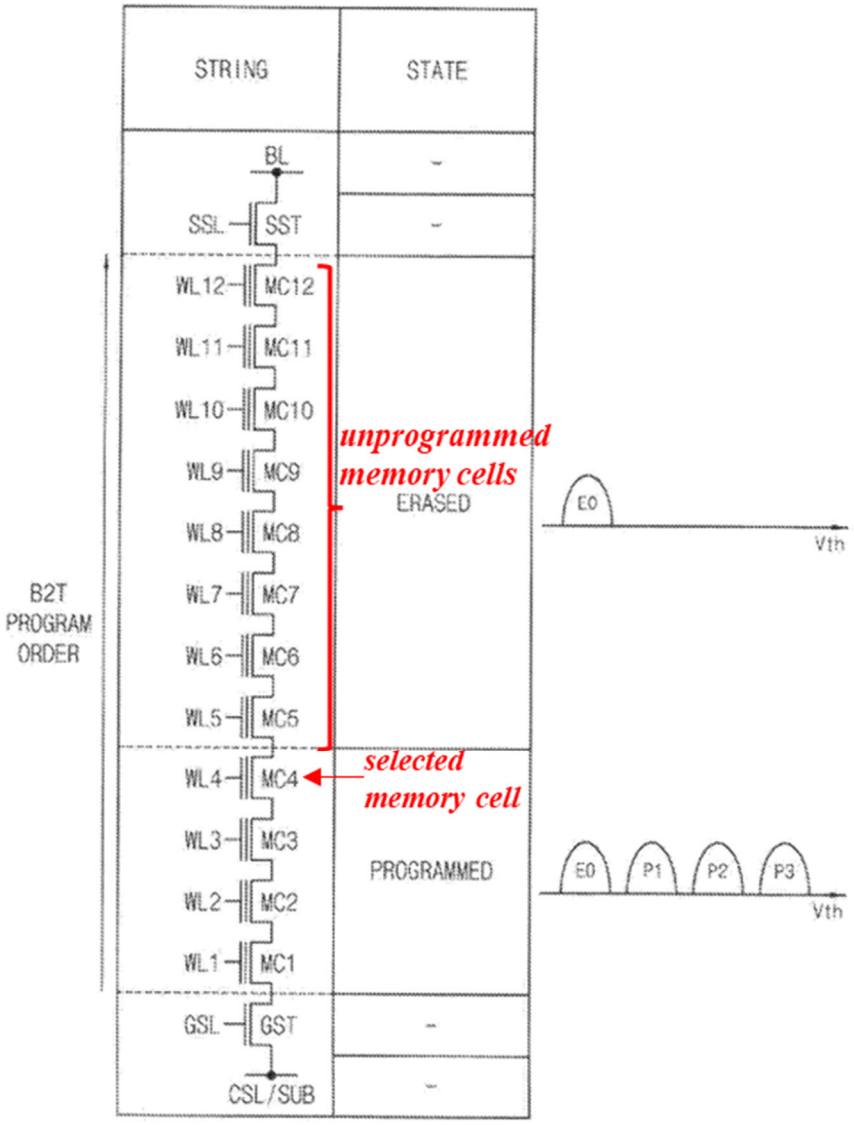


Id., Fig. 2.

110. The unselected word lines, e.g., word lines 1 and 3, are coupled to unselected cells in the selected memory string, i.e., the same memory string in which the selected memory cell belongs. Ex. 1005, [0019]. Thus, Hongtao discloses *apply[ing], in the pre-verify stage* (the pre-conduction stage), *a first bias voltage* (a pre-conduction voltage) *on … at least one memory cell* (e.g., at word line 1) *of the first memory cell string* (the selected string).

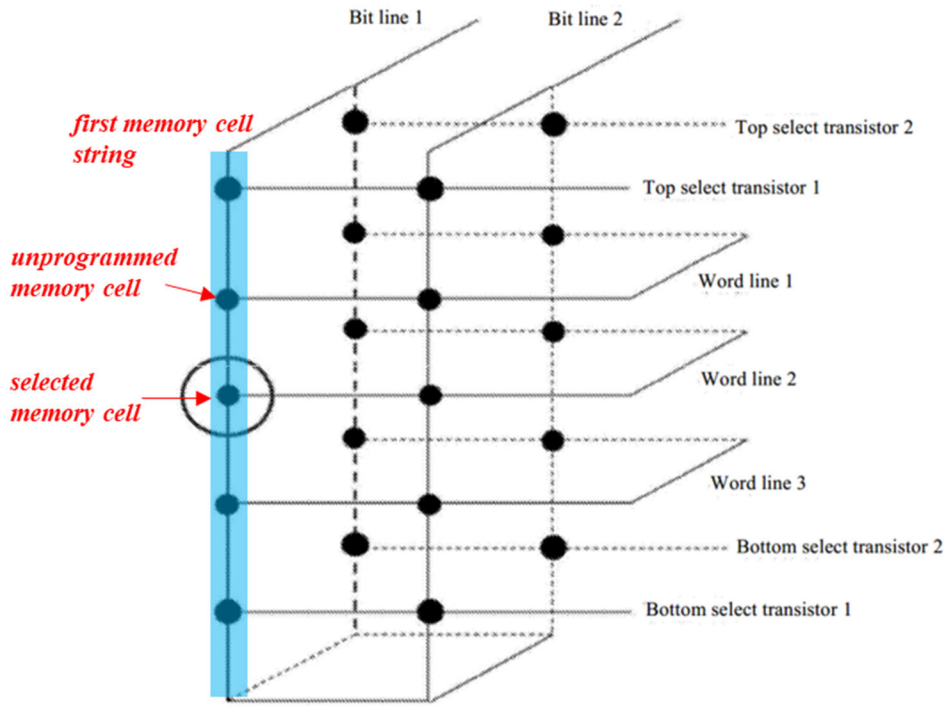
111. Now I will address the requirement of the memory cell not being programmed (which means that it is erased and has not yet been programmed). It would have been obvious that memory cells above or below the selected memory cells would not be programmed. I demonstrate this with respect to Yu. Yu discloses "the program operation may be performed in an upward direction from a lowest word line … from bottom to top (B2T program order)." Ex. 1006, [0115]. Yu also discloses program operation from highest word line to lowest, i.e., T2B. *Id.*, [0130] This simply means that the programming sequence involves starting on the top (drain side) or on the bottom (source side). And the programming occurs sequentially to the other end of the string. That is, after completing the programming of one cell and the cell properly verifies, the next sequential cell is programmed.

112. For example, taking the case of B2T, when memory cell MC4 below undergoes programming verification, cells MC1 through MC4 have been programmed, and cells MC5 through MC12 are unprogrammed and "in an erased state." Ex. 1006, [0115]. In Flash devices, typically an entire block is erased, which includes the entire memory string. Thus, the unprogrammed cells are erased.



Id., Fig. 11.

113. The B2T program order can be illustrated in Hongtao's embodiment as follows:

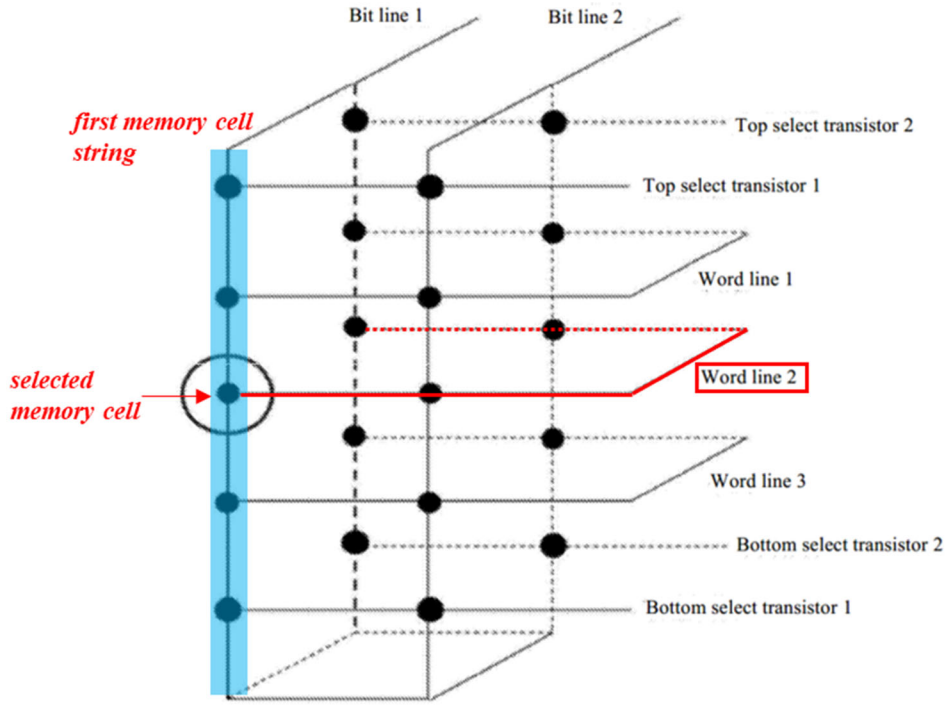


Ex. 1005, Fig. 1. The pre-conduction voltage is applied to unselected memory cells, including the unprogrammed memory cell illustrated above (the cells under the selected memory cell are programmed). That is, all of the cells above the cell being programmed receive the pre-conduction voltage. I discuss the advantages of B2T and T2B in §IX.B.7.

[1.A.iii] "apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and"

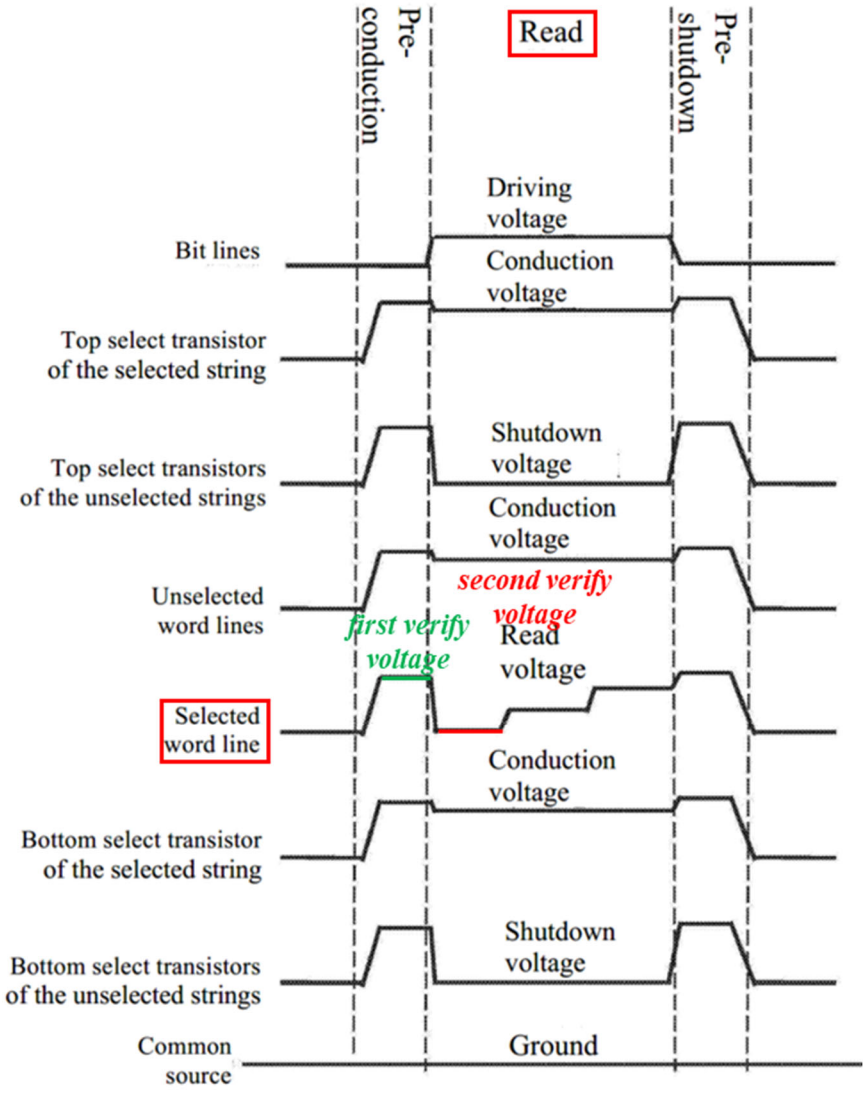
114. Hongtao discloses this limitation.

115. The limitation refers to the memory cell coupled to, e.g., word line 2 (the selected memory cell). *See* §IX.B.1.[1.A.i].



Ex. 1005, Fig. 1.

116. Hongtao discloses "apply[ing] a read voltage to the word line 2 … to read the information in the selected memory cell" in a read phase. Ex. 1005, [0019]. Note that Hongtao discloses multiple read voltages as shown during that phase. This is because Hongtao is employing multi-level cells in which multiple reads are necessary to distinguish between multiple data states.



Id., Fig. 2. The read voltage(s) can determine the data state of the selected memory cell and thus are the same as *the second verify voltage*. Ex. 1001, 11:35-39; *supra* §VI.B. This phase is the read (sensing) stage in which the threshold voltage of the *selected memory cell* is determined. Technically, the threshold voltage is distinguished between various threshold distributions, with those distributions corresponding to data states. §VI.B. Thus, the read phase constitutes a verify stage.

Again, as I describe in §IX.B.7, it would have been obvious to employ Hongtao's read operation to verify.

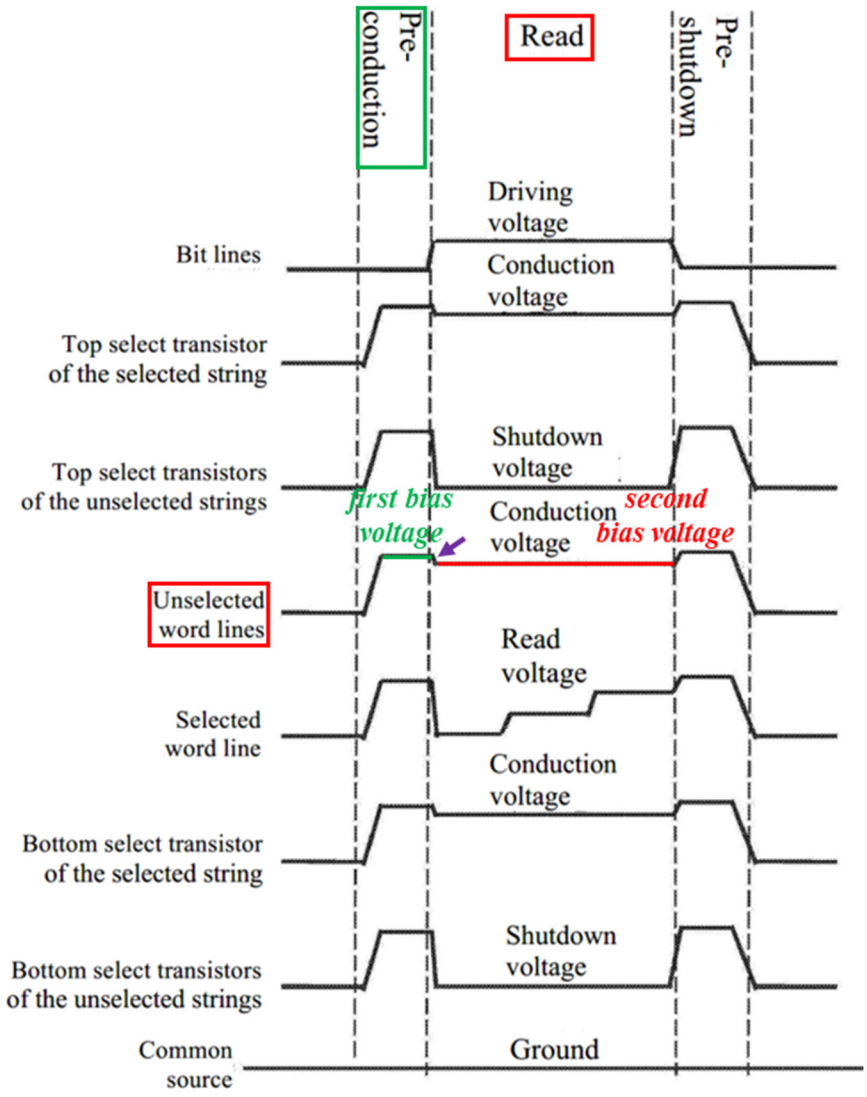
117. Accordingly, Hongtao discloses *apply[ing], in a verify stage* (read phase)*, a second verify voltage* (read voltage) *on … the selected memory cell* (e.g., at word line 2) *of the first memory cell string* (the selected string).

[1.A.iv] "apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage."

118. Hongtao discloses this limitation.

119. This limitation refers to the same memory cell in claim [1.A.ii] during the subsequent verify stage (the unselected, unprogrammed memory cell). *See* §IX.B.1.[1.A.ii].

120. Hongtao further discloses applying *a second bias voltage* (a conduction voltage) on the same cell through the same unselected word lines *in the verify stage* (the read phase):



Ex. 1005, Fig. 2; *see also id.*, [0019], [0025]. As indicated by the purple arrow, the voltage applied to the unselected word lines ramps down from the pre-conduction voltage to reach the conduction voltage. Thus, *the second bias voltage is smaller than the first bias voltage*. I note Hongtao explains why the unselected word lines voltage is dropped. Specifically, Hongtao discloses that "the greater the conduction voltage, the greater the read disturbance to the memory cell." *Id.*, [0026]; *see also id.*, [0024]-[0025]. Accordingly, the conduction voltage is reduced during the read

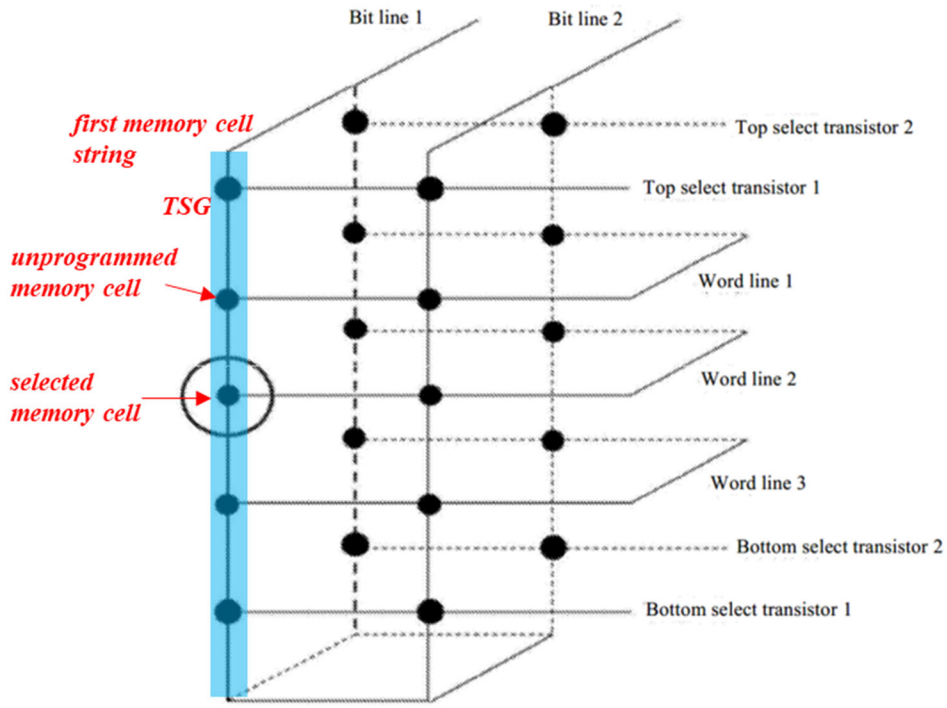
phase to reduce read disturbance. I note that Hongtao discloses this read disturbance is a function of the (conduction voltage – *channel* voltage), with the channel voltage being the driving voltage for the selected string and 0V for the unselected string. Lowering the conduction voltage on the unselected word lines alleviates the read disturbance on the unselected memory cell for both the selected string and the unselected string during the longer period of the read phase. Of course, this voltage cannot be dropped to zero, because it has to turn on the transistor. And that is why it drops only slightly.

2. Claim 2

[2] "The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string."

121. Hongtao in view of Yu renders this limitation obvious.

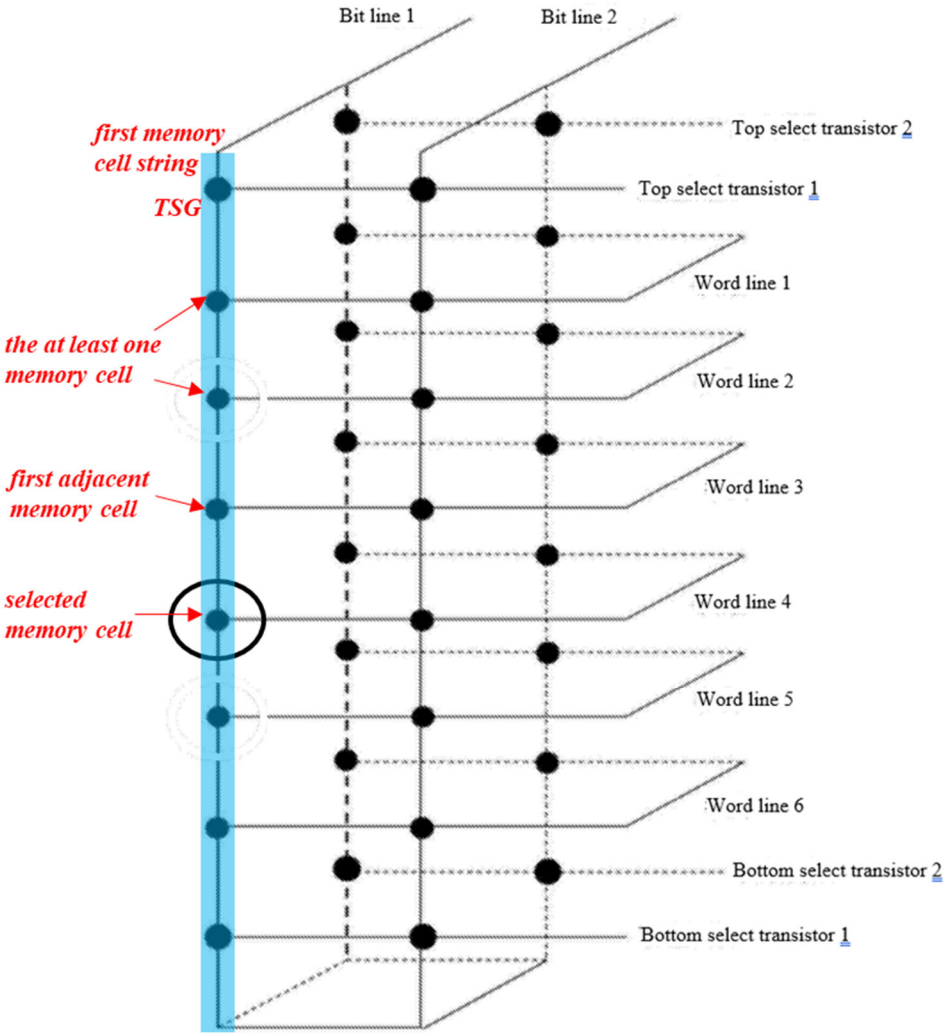
122. Claim 2 refers to the *not programmed* memory cell of claim [1.A.ii] and [1.A.iv] (i.e., unselected and unprogrammed memory cell). For claim 1, that memory cell can be a cell positioned above the selected cell (i.e., can be the first adjacent memory cell). *Supra* §§IX.B.1.[1.A.ii], IX.B.1.[1.A.iv].



Ex. 1005, Fig. 1. Again, this figure is merely an illustration for explanatory purposes. 3D NANDs at the time had dozens of memory cells in a memory string. In fact, Hongtao would have been understood to apply to memory strings with many more memory cells, because a string with merely 3 memory cells would have been understood to be for purely explanatory purposes.

123. At a minimum, it would have been obvious to apply Hongtao's teachings to memory strings with many more memory cells than in the above picture. Hongtao does not describe any limitations on how many memory cells its strings may include, and again, 3D memory string at the time typically included dozens of memory cells. Hongtao describes the memory strings as including "a plurality of memory cells." Ex. 1005, Abstract. Well before 2020, it was textbook material that

3D Flash devices' memory strings typically include "32, 64, 128, or even 150" memory cells. Ex. 1018, 80. As can be seen, for illustration purposes, patents typically do not illustrate so many memory cells. §§IX.A.2-IX.A.5. It was well understood how to implement 3D NAND with dozens of memory cells in each string well before 2020. *Id.* Thus, below I extend Hongtao's illustrative figure to account for some of the understood, and at least obvious, additional memory cell. As can be seen, with more than three memory cells per string, and with the selected cell as the one coupled to word line 4 as an example, there is *at least one memory cell* (e.g., at word line 1 or 2) *... that receives the first bias voltage and the second bias voltage [that] is positioned between the first adjacent memory cell* (at word line 3) *... and the TSG transistor ...*:



Ex. 1005, Fig. 1 (expanded).

3. Claim 3

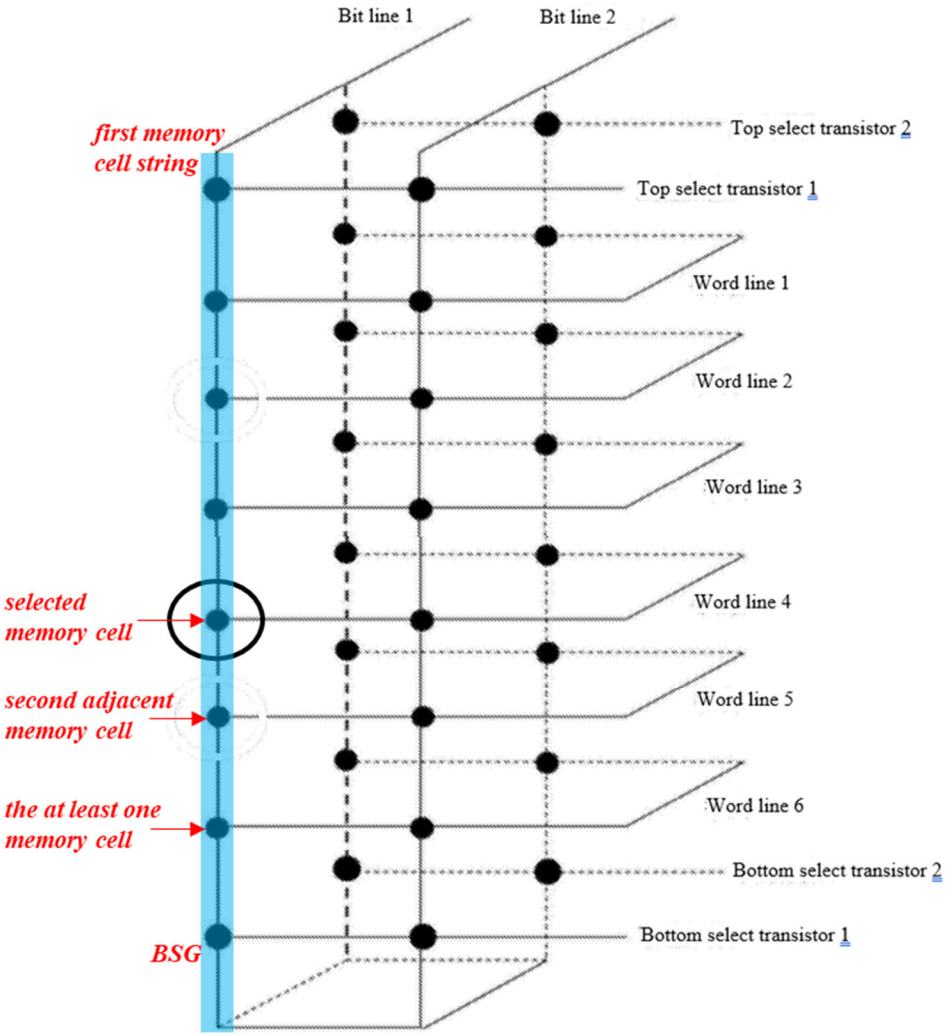
[3] "The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string."

124. Hongtao in view of Yu renders this limitation obvious.

125. Claim 3 is the mirror image of claim 2. Here, effectively opposite of claim 2, claim 3 requires that the unprogrammed memory cell receiving the bias

voltages be positioned *below* the selected cell, between the second adjacent memory cell and the BSG transistor. Again, it would have been obvious to employ sequential programming, either B2T or T2B. §IX.B.7. When employing T2B, this limitation is met.

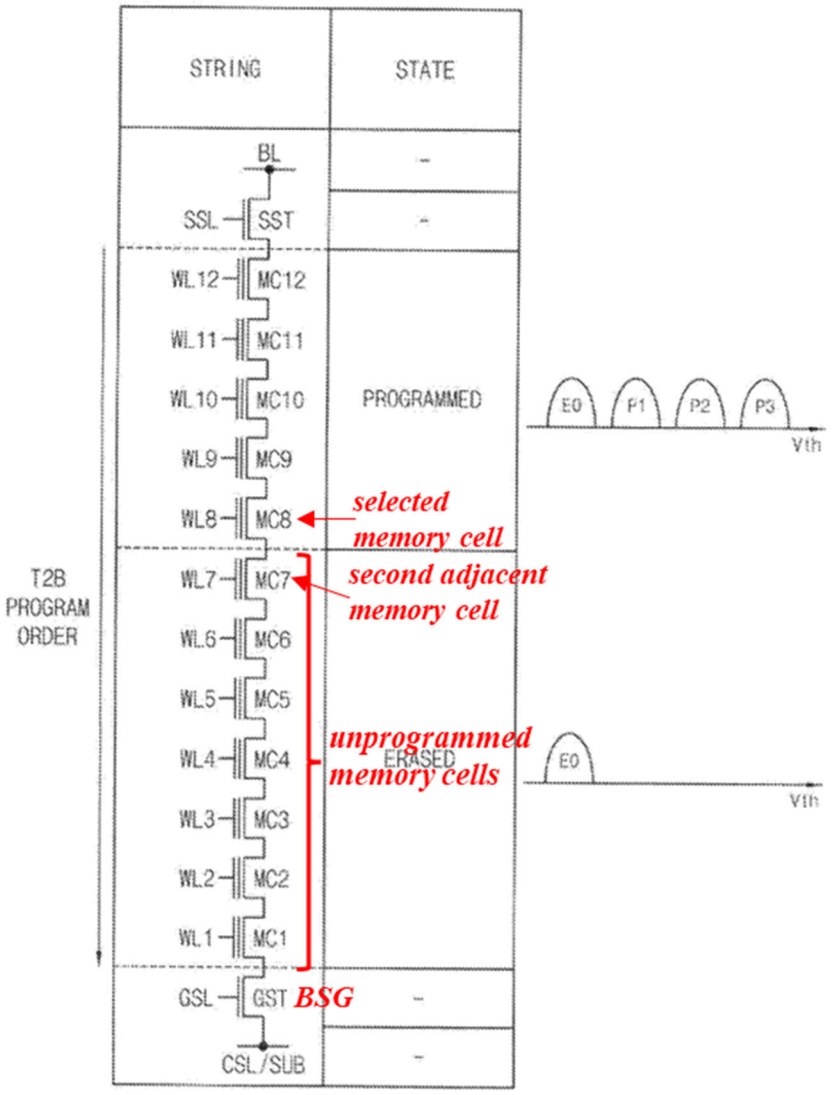
126. Hongtao discloses that all unselected cells receive the bias voltages. *See* §§IX.B.1.[1.A.ii], IX.B.1.[1.A.iv]. As I explain above, Hongtao's figure is merely illustrative for explanatory purposes. Thus, I again use the longer version of Figure 1 below. *Supra* §IX.B.2.[2]. Accordingly, if the memory cell coupled to word line 4 is the selected cell and the cell coupled to word line 5 is the second adjacent memory cell, then another cell below, e.g., one coupled to word line 6, can constitute *the at least one memory cell … that receives the … bias voltage[s]*:



Ex. 1005, Fig. 1 (expanded).

127. It would have been obvious that the memory cell coupled to word line 6 would not be programmed in view of Yu. Specifically, Yu teaches that "the program operation may be performed in a downward direction from an uppermost word line … from top to bottom (T2B program order)." Ex. 1006, [0130]. This is just the opposite direction as B2T. With T2B, for example, when memory cell MC8 below is being verified, cells MC12 through MC8 have been programmed, and cells

MC7 through MC1 are unprogrammed and "in an erased state." *Id.* Note that in Flash devices, typically an entire block is erased, which includes the entire memory string. Thus, the unprogrammed cells are erased.



Id., Fig. 14.

128. Unprogrammed cells MC6 through MC1 are positioned between the second adjacent memory cell MC7 and the ground selection transistor GST, Yu's

BSG. Yu teaches that, using a T2B program order, Hongtao's memory cell at word line 6 is unprogrammed.

129. Note that Claim [1.A.ii] requires an unprogrammed memory cell to receive the bias voltages—without imposing any location requirement on this cell. Thus, either the B2T or the T2B program order satisfies that limitation, and the B2T program order is used there merely to explain that limitation. Because claim 3 depends from claim 1, this mapping assumes that T2B is used for claim 1.

4. Claim 4

[4.PRE] "The apparatus of claim 1, wherein the processing circuitry is further configured to:"

130. Hongtao discloses or at least renders obvious a *processing circuitry further configured to* perform the limitations of claim 4. *Supra* §IX.B.1.[1.A].

[4.A] "in the pre-verify stage,"

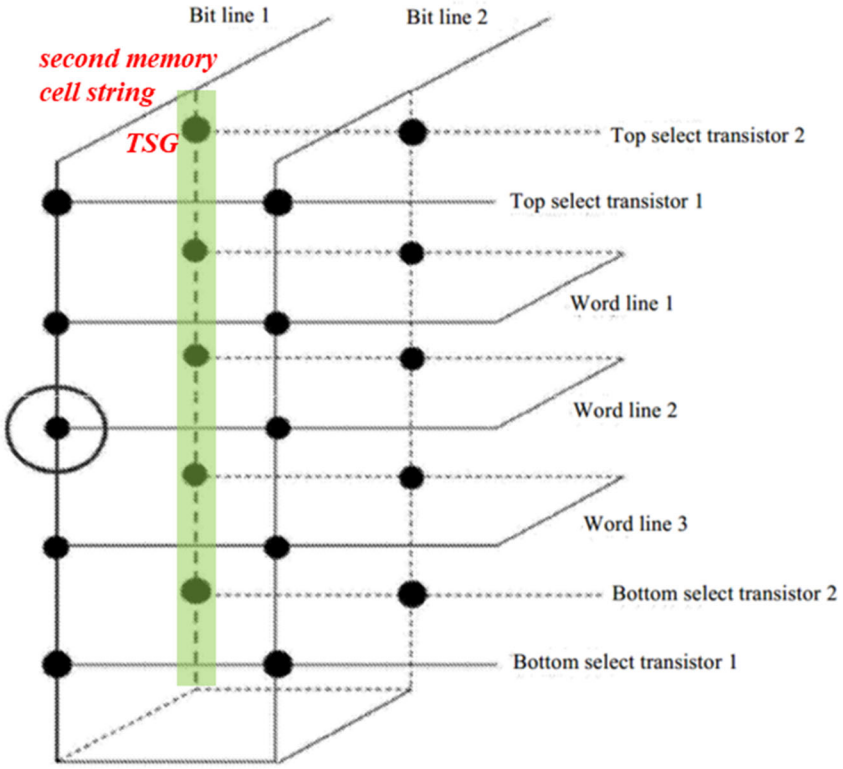
131. The pre-verify stage corresponds to Hongtao's "pre-conduction phase." *Supra* §§IX.B.1.[1.A.i]-IX.B.1.[1.A.ii].

[4.A.i] "apply a first gate voltage on a gate terminal of the TSG transistor of the second memory cell string,"

132. Hongtao discloses this limitation.

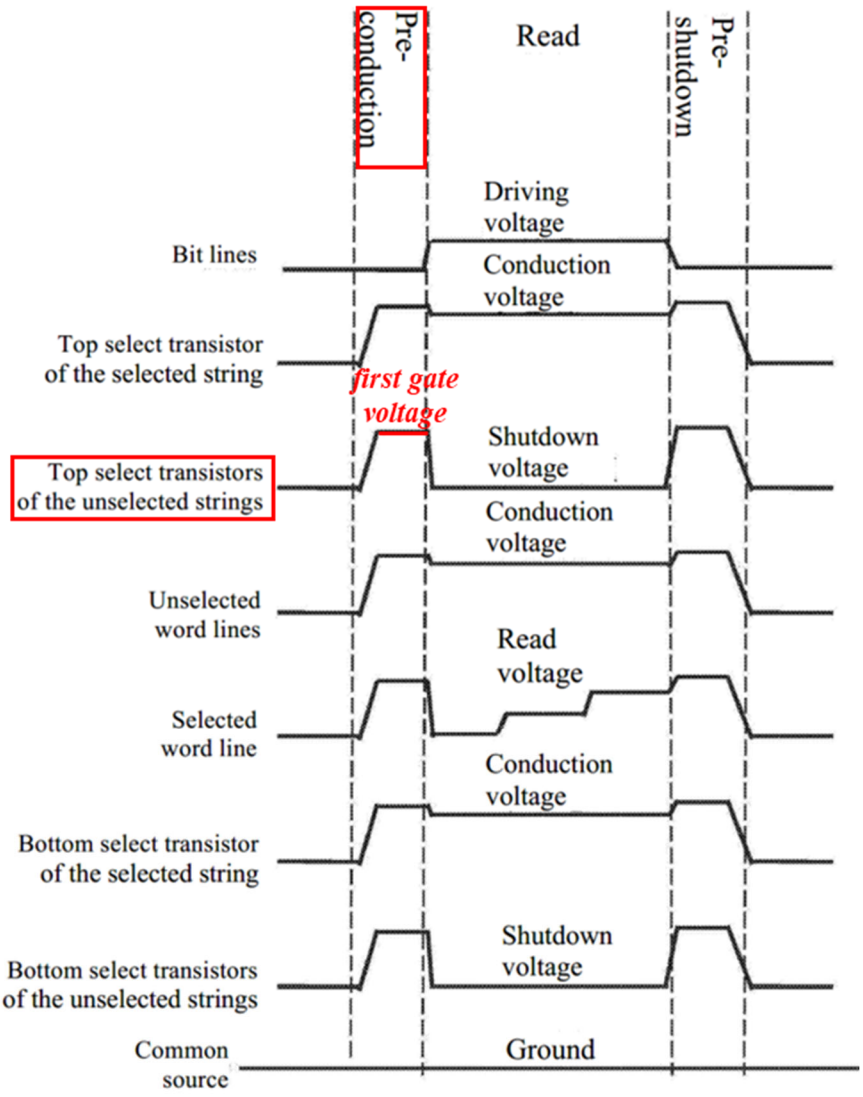
133. *The second memory cell string* is an unselected memory string since the selected memory cell belongs the first memory cell string. Ex. 1001, 17:42-43 (claim [1.A.i]). In other words, claim 1 operates on the first memory string, which

includes the selected memory cell. Thus, in this context, the second memory string is not selected. Hongtao discloses a top select transistor (*TSG transistor*) of an unselected memory string (*the second memory string*):



Ex. 1005, Fig. 1; *see also supra* §IX.B.1.[1.PRE] (claim [1.PRE] showing the same figure).

134. Hongtao further discloses *apply[ing] a gate voltage* on this transistor *in the pre-verify stage* (pre-conduction phase):

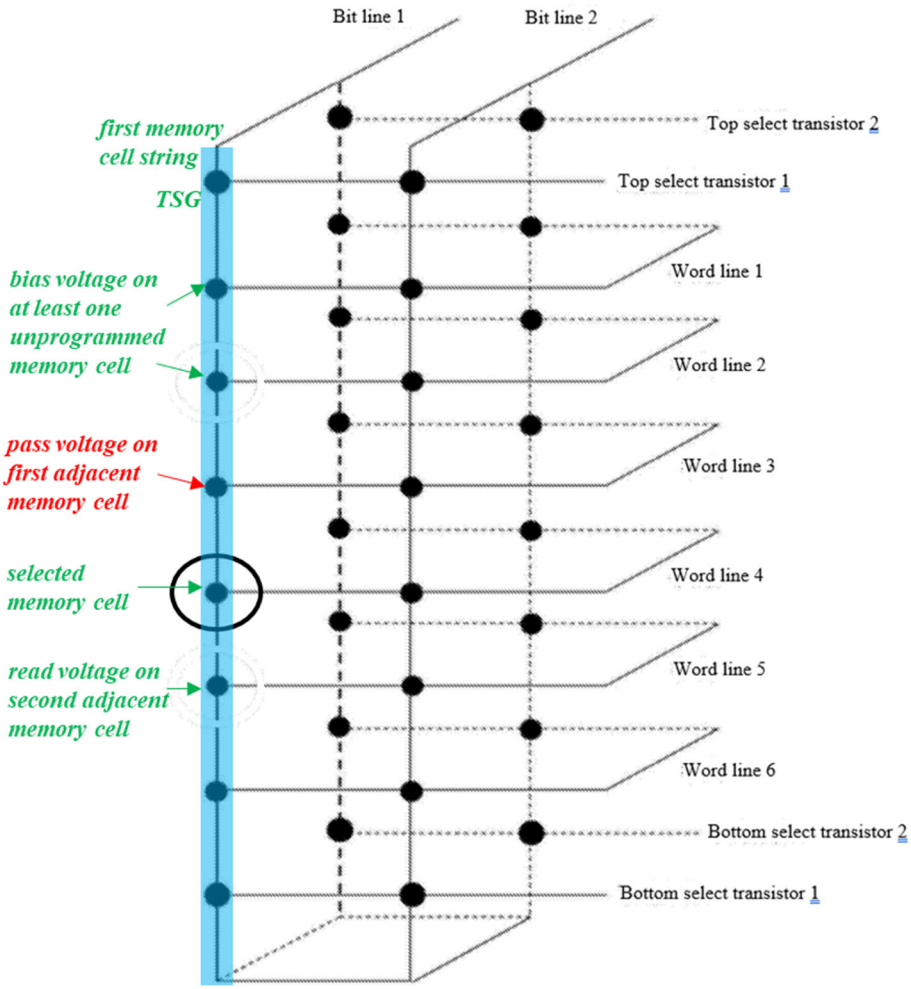


Ex. 1005, Fig. 2. I note that this voltage turns on the unselected memory string. *Id.*, Abstract, [0006]. In other words, this voltage is sufficient to render that transistor conductive.

[4.A.ii] "apply a first pass voltage on a gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and"

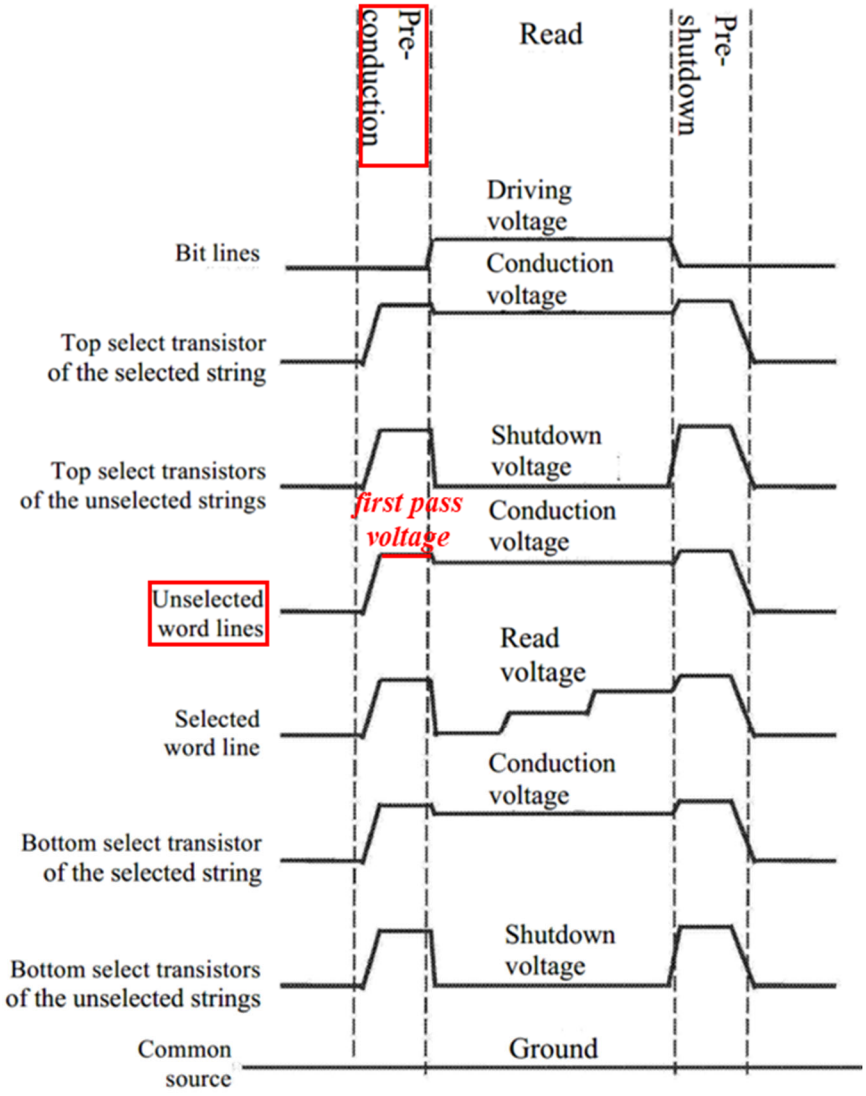
135. Hongtao in view of Yu renders this limitation obvious.

136. For example, *the first adjacent memory cell* may be located as illustrated below:



Ex. 1005, Fig. 1 (expanded). *See* §IX.B.2.[2] (for obvious extension of Hongtao's memory string). Note that while I did not refer to this expanded Figure 1 in claim 1, it satisfies claim 1, because it simply expands the memory string.

137. The *first pass voltage* is the voltage on unselected word lines:



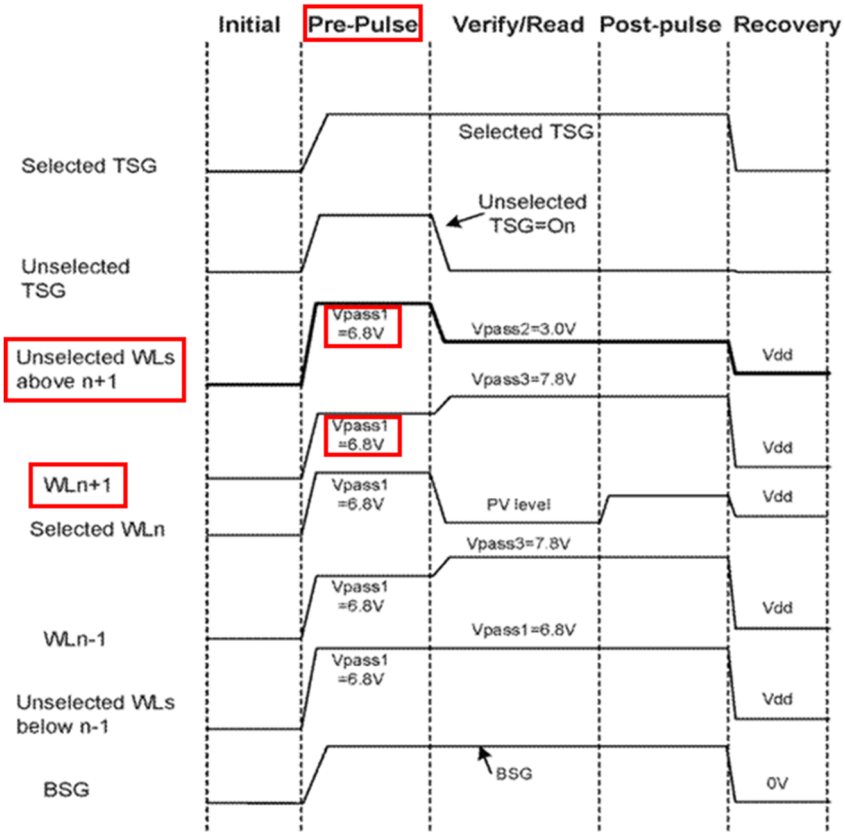
Ex. 1005, Fig. 2.

138. To the extent that Patent Owner argues the first pass voltage and the first bias voltage must have different values or be distinct voltages, I disagree, because it would be inconsistent with the '957 patent.

139. First, as a general point, when the '957 patent requires two voltage terms to have different values, it expressly states this requirement. For example,

claim 1 requires "the second bias voltage [to be] smaller than the first bias voltage." Ex. 1001, 17:55-56 (claim [1.A.iv]). As another example, claim 4 requires that "at least one of the second pass voltage and the second read voltage is larger than the second gate voltage." *Id.*, 18:31-32 (claim [4.C]). Here, there is no language that distinguishes *first bias voltage* and the *first pass voltage*.

140. More specifically, the '957 patent uses the same voltage—6.8V—for both the *first bias voltage* (applied on "Unselected WLs above n+1") and the *first pass voltage* (applied on "WLn+1"):



Ex. 1001, Fig. 6; *id.*, Fig. 8 (same); *see also id.*, 11:3-5 (describing the same in Figure 4).

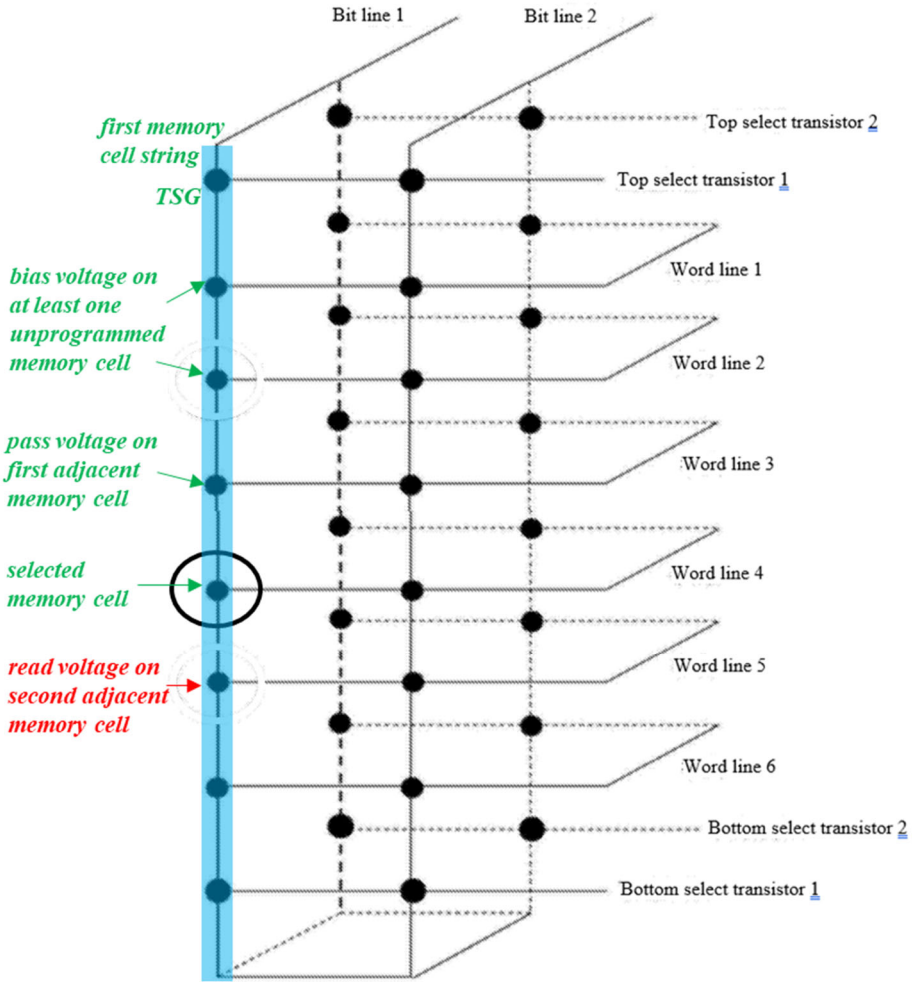
141. Moreover, as the figure also shows, both the first bias voltage and the first pass voltage are "Vpass1." *See also* Ex. 1001, Fig. 8 (same).

142. The '957 patent also equates bias voltages with pass voltages three different times. Ex. 1001, 9:35, 11:4, 11:26-27. Although the latter two references are to Figure 4, the waveforms during the pre-pulse stage in Figures 4, 6, and 8 are identical. Either bias voltages or pass voltages can be applied to unselected memory cells. *Id.*, 9:34-38. Moreover, "[a] bias voltage (*or* pass voltage) … can be applied on the WLn+1," the first adjacent memory cell. *Id.*, 11:4-5, 11:26-28 (emphasis added). Accordingly, bias voltages and pass voltages need not be distinct voltages.

[4.A.iii] "apply a first read voltage on a gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string; and"

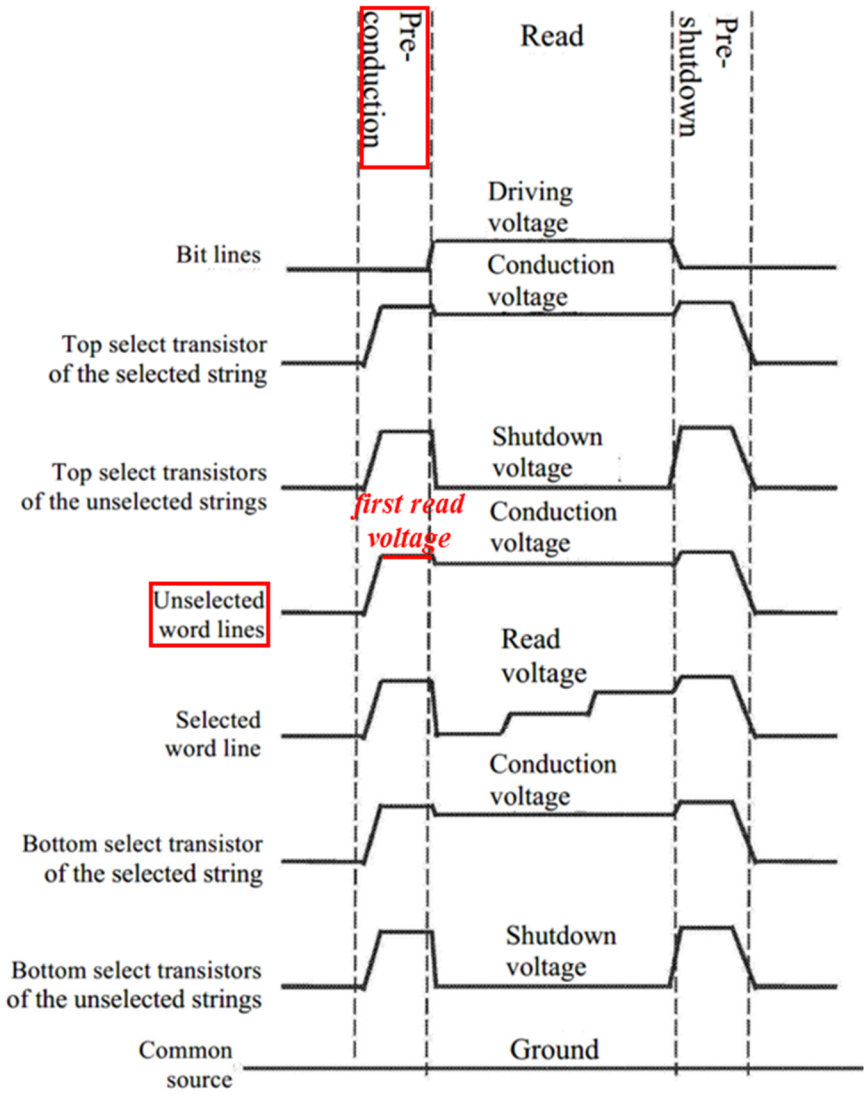
143. Hongtao discloses this limitation.

144. For example, *the second adjacent memory cell* may be located as indicated (in red) below:



Ex. 1005, Fig. 1 (expanded). *See* §IX.B.2.[2] (for obvious extension of Hongtao's memory string).

145. And the *first read voltage* is the voltage on unselected word lines:

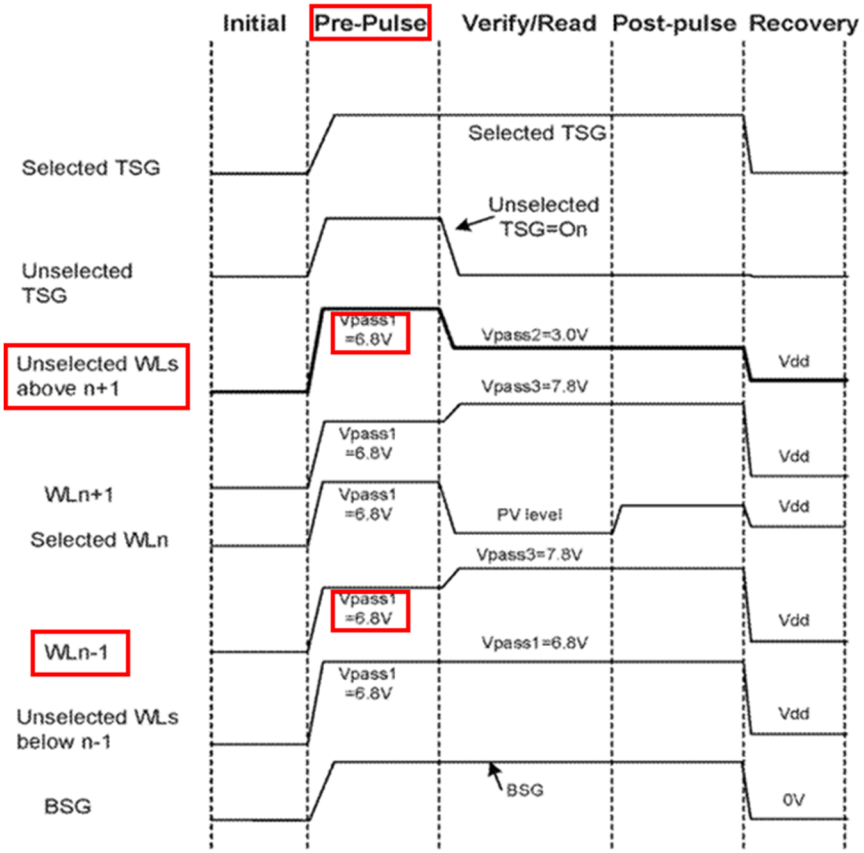


Ex. 1005, Fig. 2.

146. To the extent that Patent Owner argues the *first read voltage* and the *first bias voltage* must have different values or be distinct voltages, I disagree.

147. As I explain above, the '957 patent distinguishes different claimed voltages expressly when defining them to have different values, and no such language exits here. *Supra* §IX.B.4.[4.A.ii].

148. Further, embodiments of the '957 patent uses the same voltage—6.8V—for both the *first bias voltage* (applied on "Unselected WLs above n+1") and *the first read voltage* (applied on "WLn-1"):



Ex. 1001, Fig. 6; *id.*, Fig. 8 (same).

149. Moreover, as the figure also shows, both the first bias voltage and the first read voltage are "Vpass1." *See also* Ex. 1001, Fig. 8 (same). Notably, the '957 patent twice equates bias voltages with read voltages in the context of WLn-1, *the*

second adjacent memory cell. *Id.*, 11:7-8, 11:29-30.[2] The voltage applied on WLn-1 can be either "[a] bias voltage (or read voltage)." *Id.*

[4.B] "in the verify stage,"

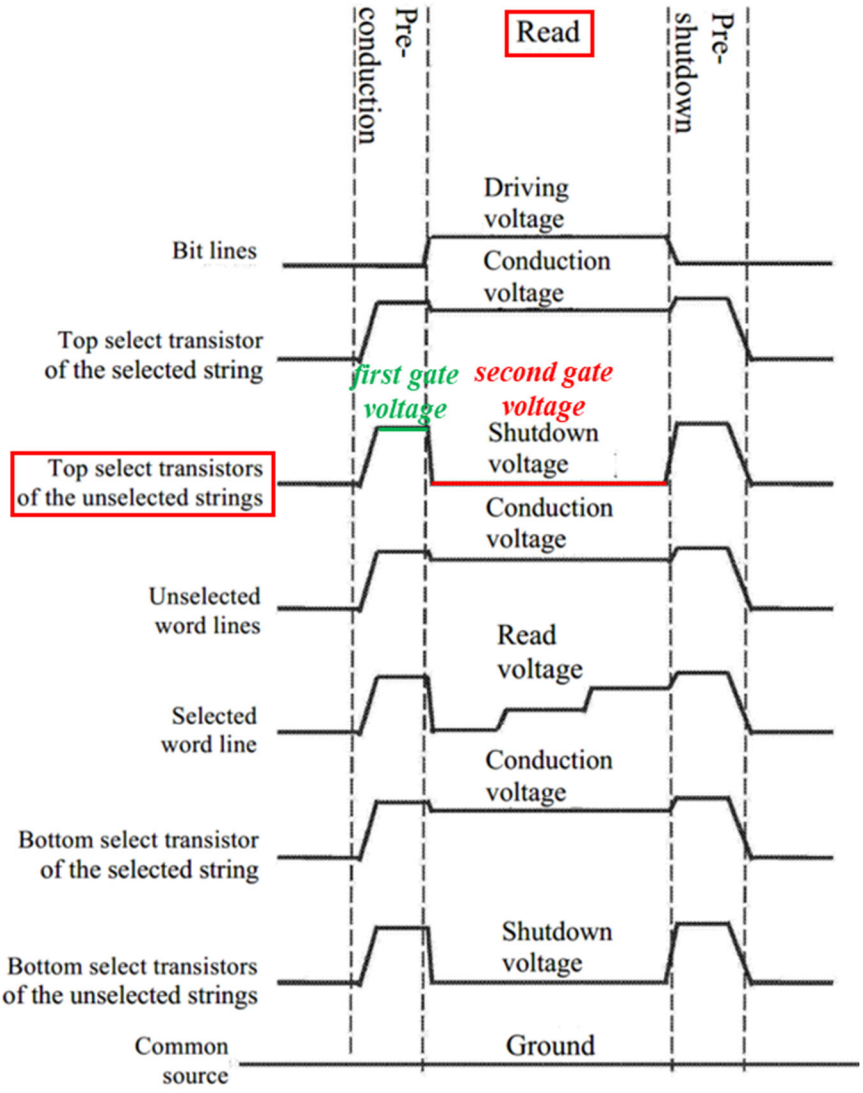
150. The verify stage corresponds to Hongtao's "read phase." *Supra* §§IX.B.1.[1.A.iii]-IX.B.1.[1.A.iv].

[4.B.i] "apply a second gate voltage on the gate terminal of the TSG transistor of the second memory cell string,"

151. Hongtao discloses this limitation.

152. This limitation refers to the same transistor in claim [4.A.i] during the subsequent verify stage. *Supra* §IX.B.4.[4.A.i]. The *second gate voltage* is shown below:

[2] Although these references are to Figure 4, the waveforms during the pre-pulse stage in Figures 4, 6, and 8 are identical.

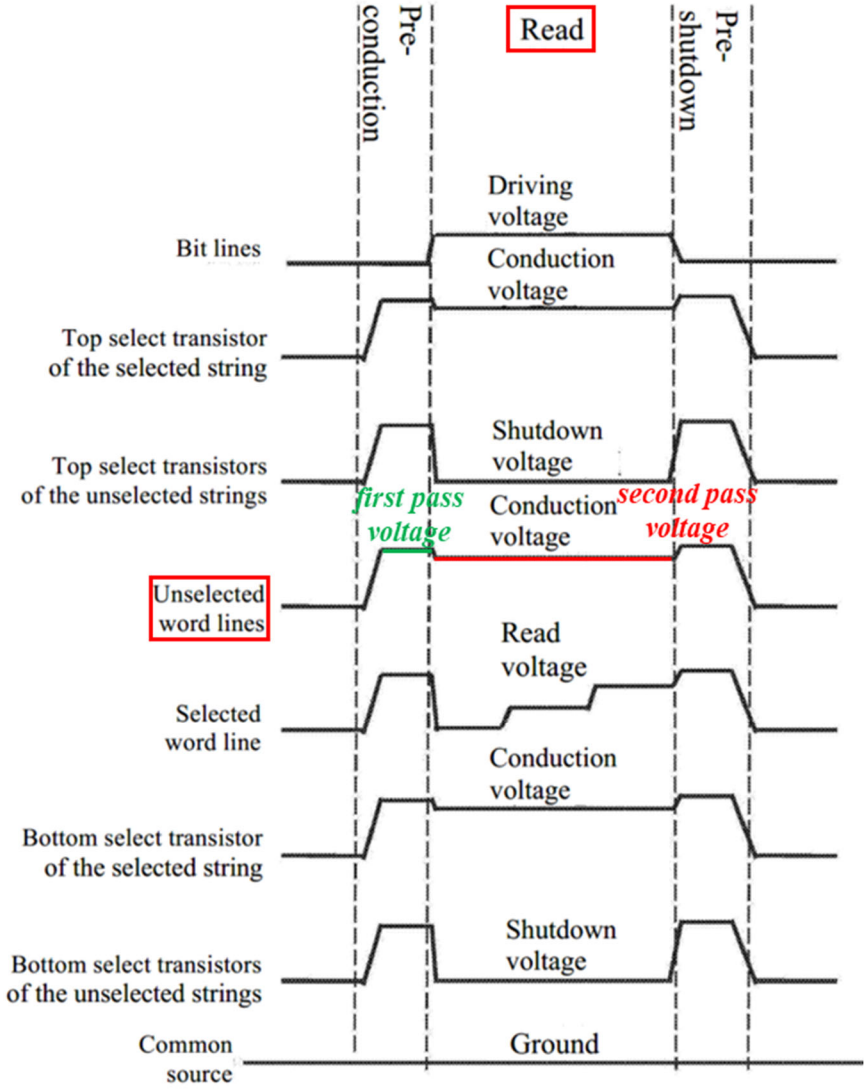


Ex. 1005, Fig. 2. This "[s]hutdown voltage" or "disconnection voltage" turns off the TSG of the unselected memory string. *Id.*, [0008], [0012], [0019], [0024].

[4.B.ii] "apply a second pass voltage on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and"

153. Hongtao in view of Yu renders this limitation obvious.

154. This limitation refers to the same transistor in claim [4.A.ii] during the subsequent verify stage. *Supra* §IX.B.4.[4.A.ii]. The *second pass voltage* is shown below:

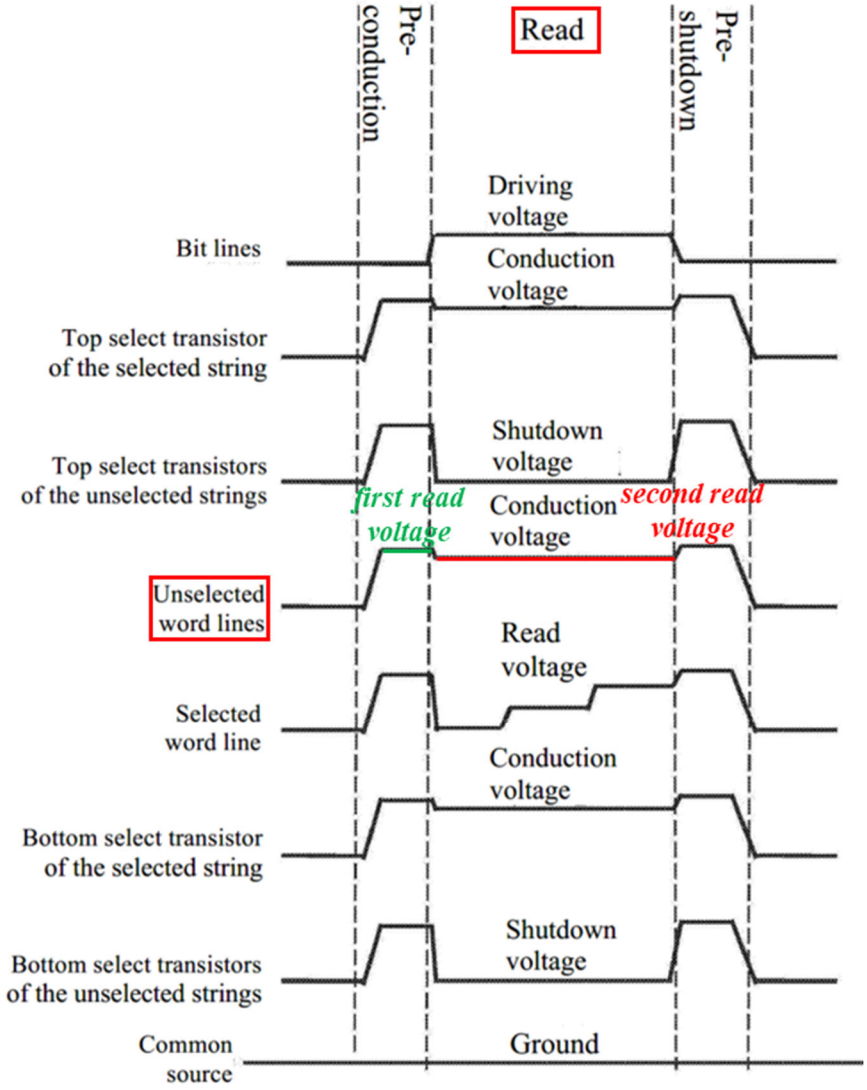


Ex. 1005, Fig. 2. This voltage slightly drops from the *first pass voltage*.

[4.B.iii] "apply a second read voltage on the gate terminal of the second adjacent memory cell of the selected memory cell of the first memory cell string, wherein"

155. Hongtao in view of Yu renders this limitation obvious.

156. This limitation refers to the same transistor in claim [4.A.iii] during the subsequent verify stage. *Supra* §IX.B.4.[4.A.iii]. The *second read voltage* is shown below:

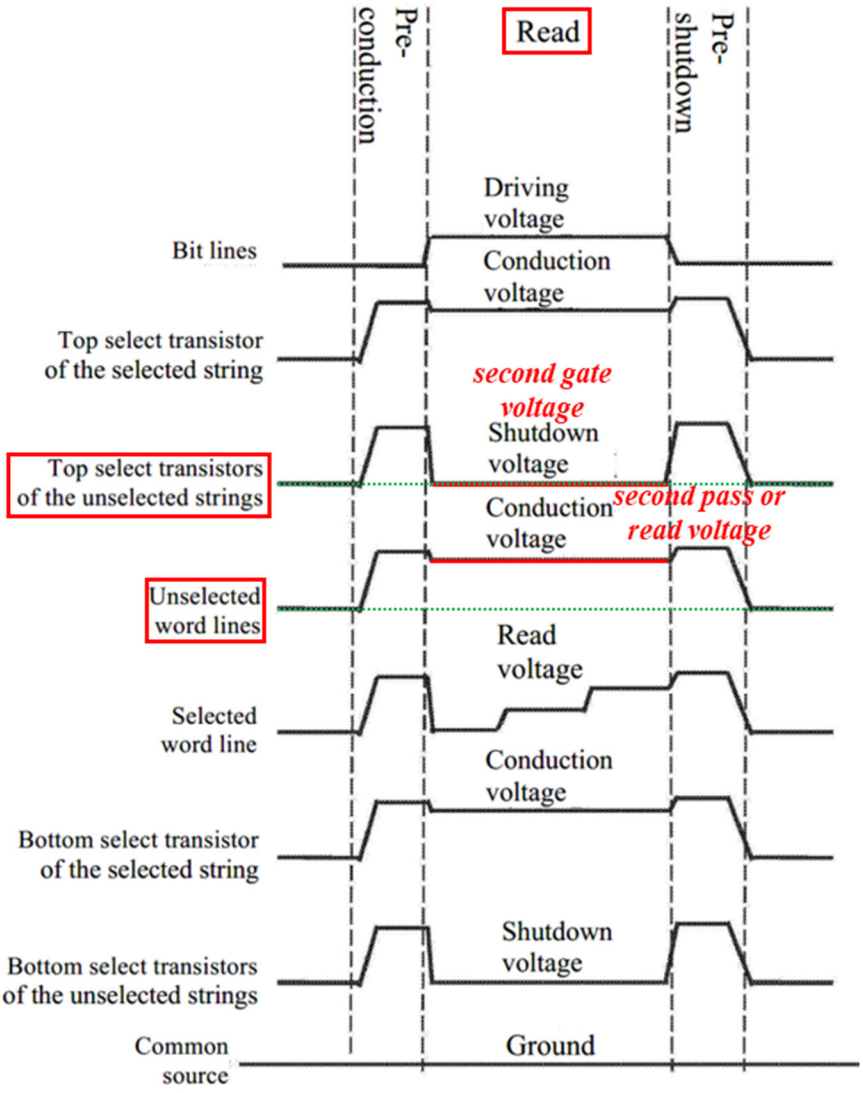


Ex. 1005, Fig. 2.

[4.C] "at least one of the second pass voltage and the second read voltage is larger than the second gate voltage."

157. Hongtao in view of Yu renders this limitation obvious.

158. Both the second pass voltage and the second read voltage are Hongtao's conduction voltage. *Supra* §§IX.B.4.[4.B.ii]-9. The second gate voltage is Hongtao's shutdown voltage or disconnection voltage. *Supra* §IX.B.4.[4.B.i]. The conduction voltage turns on a memory cell while the shutdown voltage turns off the TSG. *See, e.g.*, Ex. 1005, [0008]. Thus, *the second pass voltage and the second read voltage [are] larger than the second gate voltage*:



Id., Fig. 2.

5. Claim 5

[5.PRE] The apparatus of claim 2, wherein the processing circuitry is further configured to:

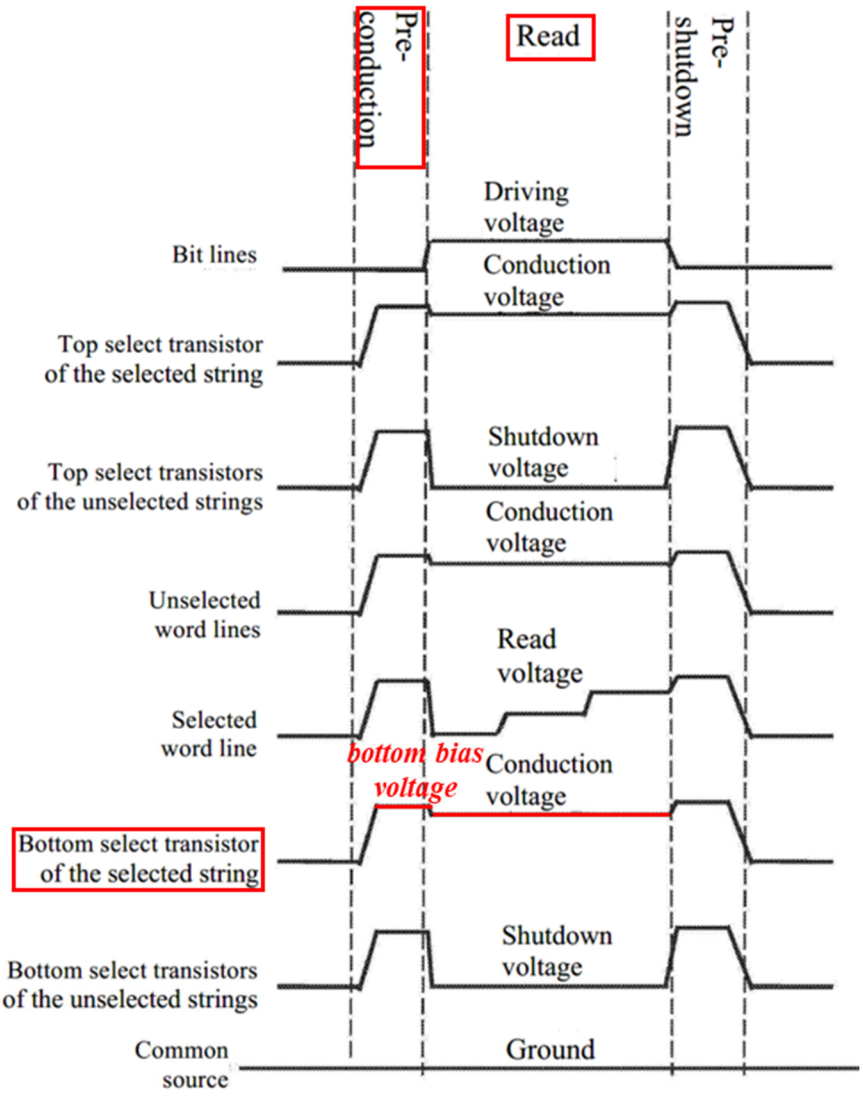
159. Hongtao discloses or at least renders obvious *processing circuitry further configure to* perform the limitations of claim 5. *Supra* §IX.B.1.[1.A].

[5.A] "apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;"

160. Hongtao in view of Yu renders this limitation obvious.

161. I note that it is clear that the claim is using *bottom* to refer to the BSG voltage, because subsequently the claims use *top* to refer to the voltage on the TSG.

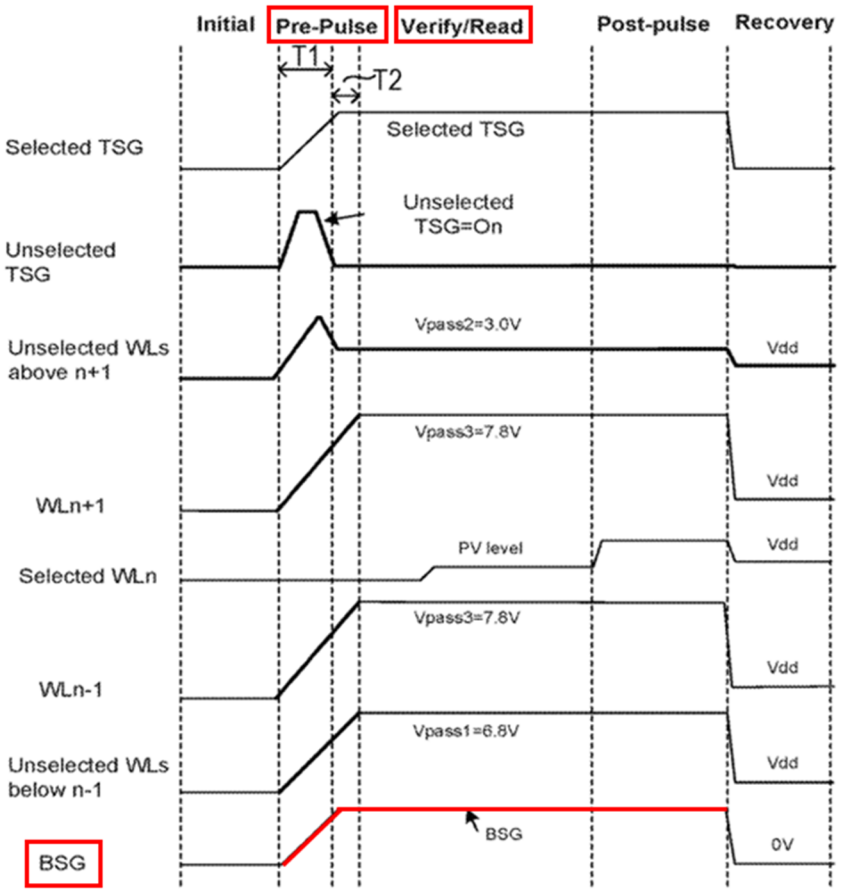
162. Hongtao discloses *apply[ing] a bottom bias voltage* (a pre-conduction voltage and conduction voltage) *on … the BSG transistor of the first memory cell string* (the selected string) *in the pre-verify stage* (the pre-conduction phase) *and the verify stage* (the read phase):



Ex. 1005, Fig. 2; *see also id.*, [0023], [0025]. The conduction voltage is high enough to "turn on" the bottom select (BSG) transistor. *Id.*, [0019].

163. To the extent that Patent Owner argues "a bottom bias voltage" must have only one voltage level, I disagree, because it would be inconsistent with the '957 patent.

164. The '957 patent discloses that a bottom bias voltage may "be increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage." Ex. 1001, 2:56-59, 4:4-7.

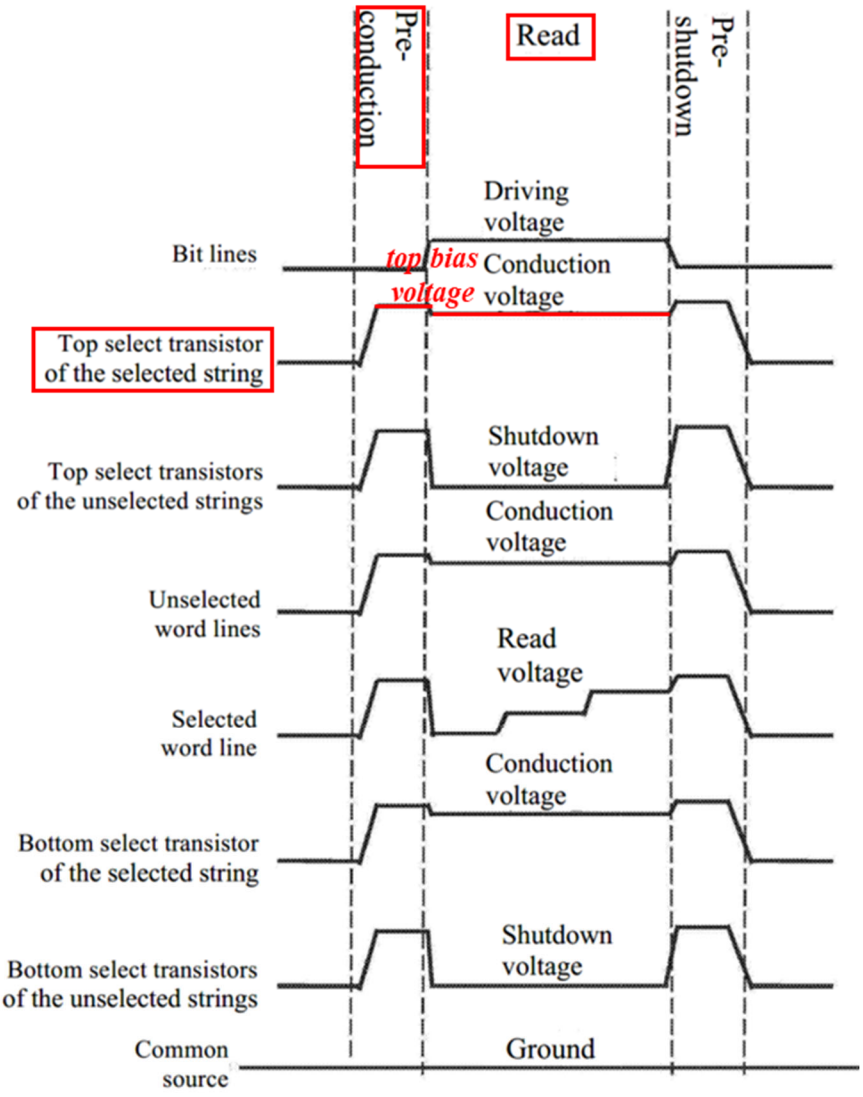


Id., Fig. 7, 13:43-47; *see also id.*, Fig. 9 (same). Thus, the '957 patent does not use "bias" to refer to a constant voltage.

[5.B] "apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and"

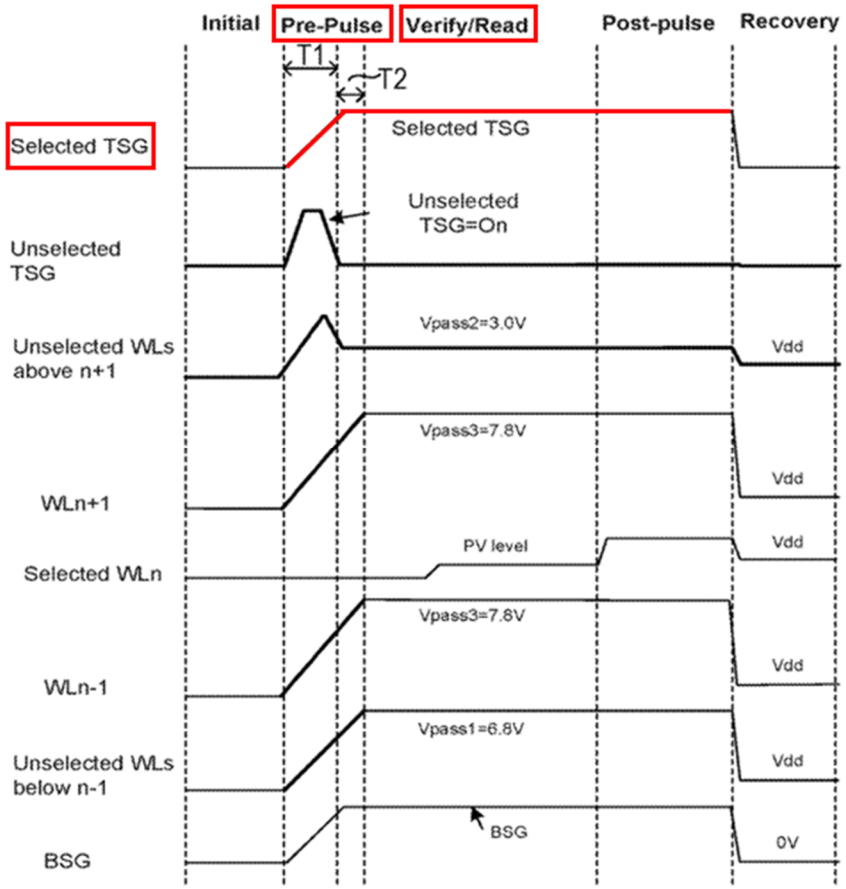
165. Hongtao in view of Yu renders this limitation obvious.

166. Hongtao discloses *apply[ing] a top bias voltage* (a pre-conduction voltage and conduction voltage) *on … the TSG transistor of the first memory cell string* (the selected string) *in the pre-verify stage* (the pre-conduction phase) *and the verify stage* (the read phase):



Ex. 1005, Fig. 2; *see also id.*, Abstract, [0023], [0025]. The pre-conduction and conduction voltages are high enough to turn on the top select (TSG) transistor. *Id.*, [0006], [0019].

167. Like the bottom bias voltage, a top bias voltage also need not have only one voltage level for the same reasons. *Supra* §IX.B.5.[5.A]; Ex. 1001, 2:59-61, 4:7-9:

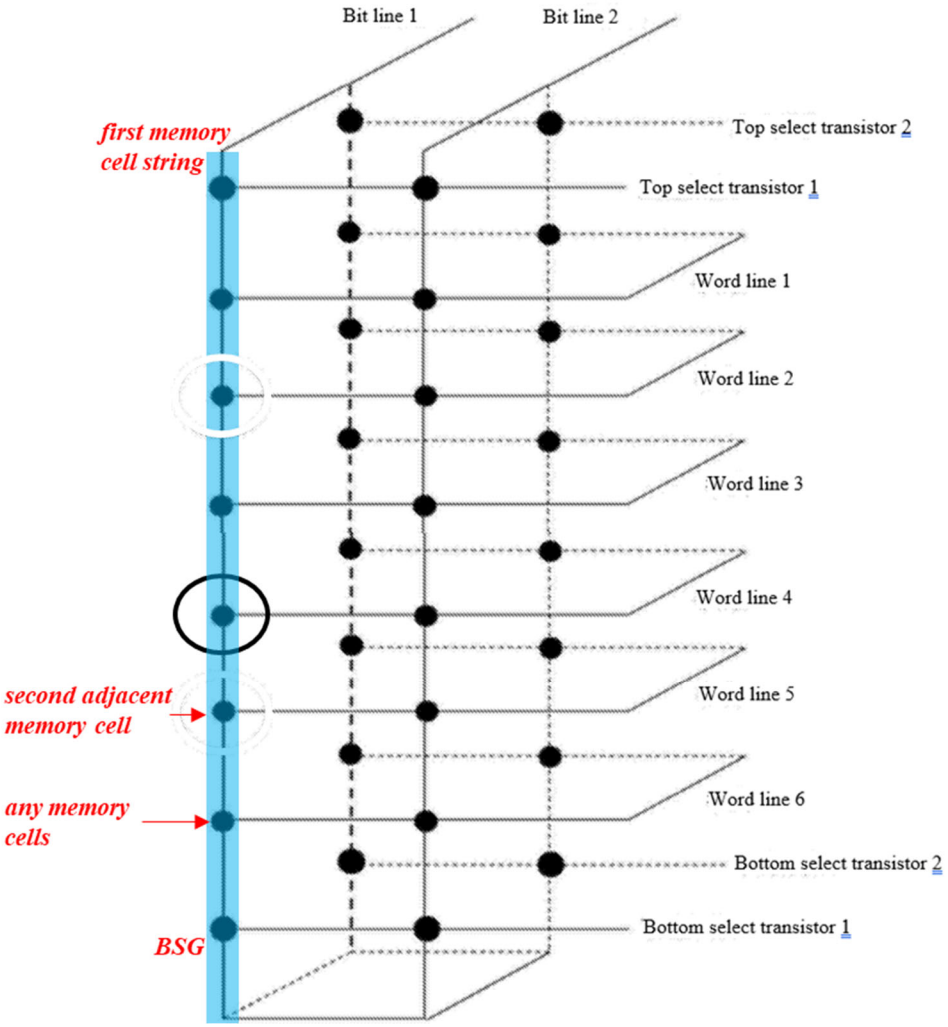


Id., Fig. 7, 13:49-53; *see also id.*, Fig. 9 (same).

[5.C] "apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage."

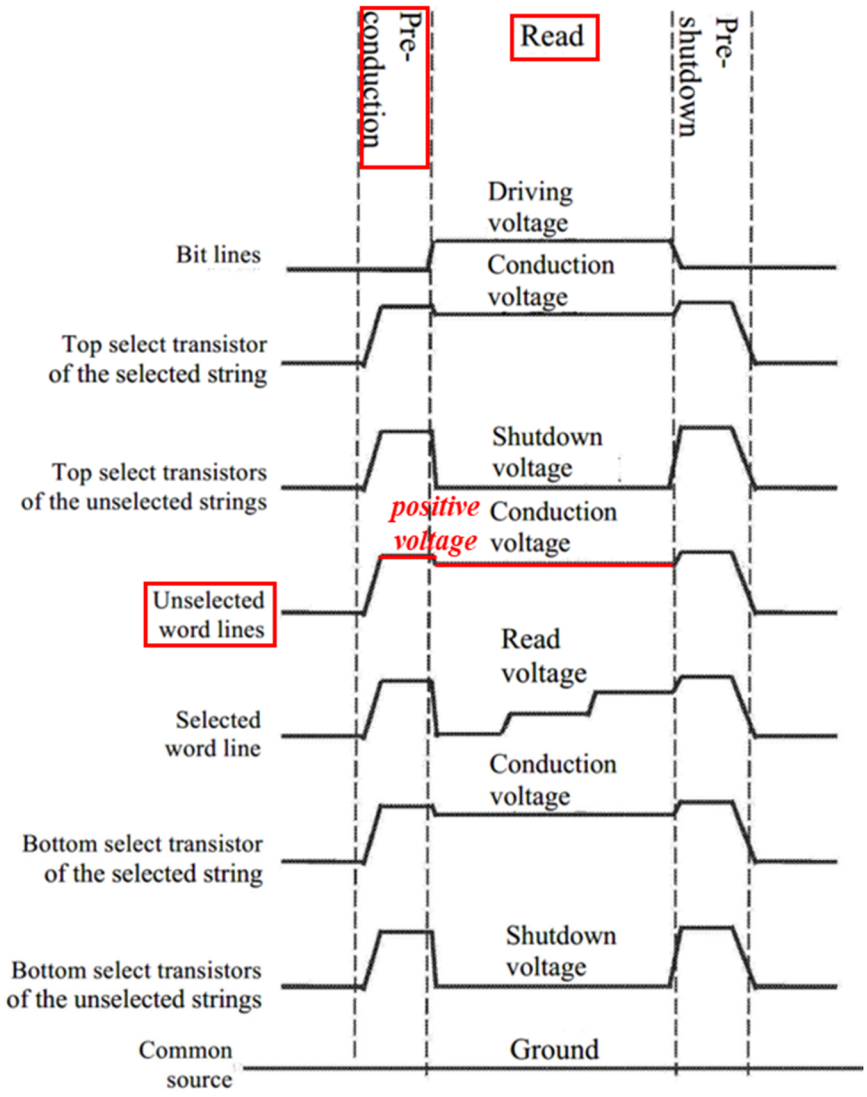
168. Hongtao in view of Yu renders this limitation obvious.

169. The *any memory cells* may be *positioned* as shown:



Ex. 1005, Fig. 1 (expanded). *See* §IX.B.2.[2] (for obvious extension of Hongtao's memory string).

170. Hongtao discloses *apply[ing] a positive voltage* (a pre-conduction voltage and conduction voltage) *on … any memory cells that are positioned* (at word line 6) *between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string* (the selected string) *in the pre-verify stage* (the pre-conduction phase) *and the verify stage* (the read phase):

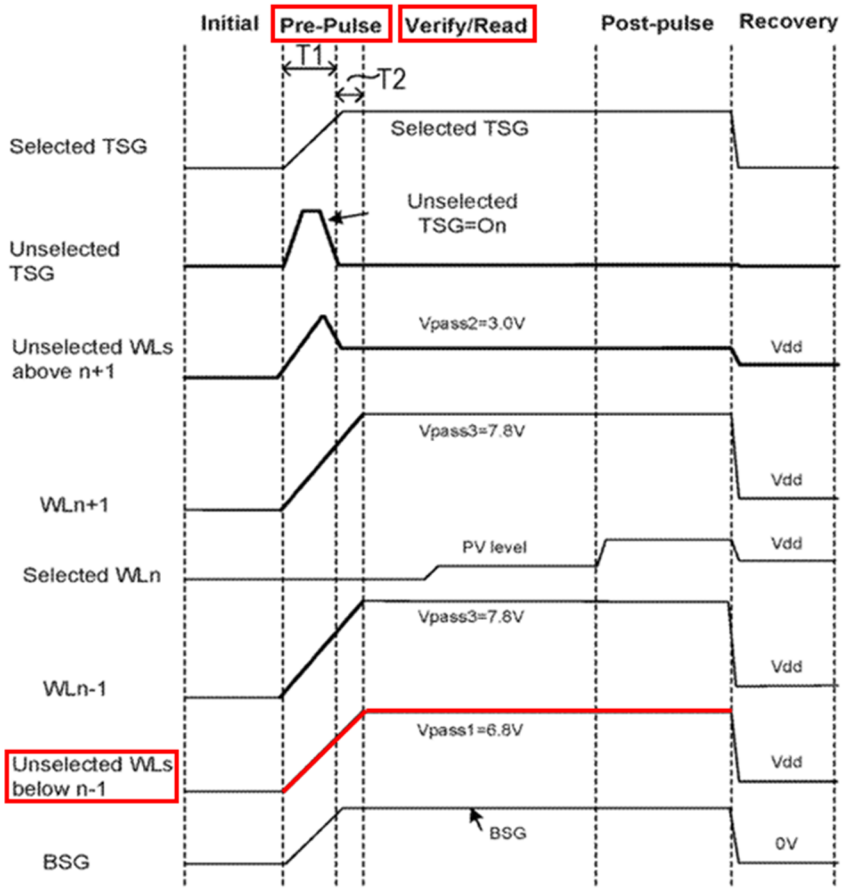


Ex. 1005, Fig. 2.

171. To the extent that Patent Owner argues "a positive voltage" must have only one voltage level or that it must be a voltage distinct from the bias voltages, I disagree, because it would be inconsistent with the '957 patent.

172. The '957 patent discloses that a positive voltage may "be increased from the initial voltage in the pre-verify stage." Ex. 1001, 2:62-63, 4:10-11. Indeed, the '957 patent refers to different levels of voltages as "*the* positive voltage." *Id.*,

13:54-58 ("*The positive voltage* applied on the WLs (<n−1) *can be increased from the initial voltage in the pre-verify stage* to a target value (e.g., 6.8 volts) in the pre-pulse stage, where the target value is equal *to the positive voltage applied in the verify/read stage*.") (emphases added) (describing Figure 7):



Id., Fig. 7. Thus, the '957 patent is not using *a positive voltage* to refer to a constant voltage.

173. Also, a *positive voltage* and a *bias voltage* need not be distinct voltages. Again, the claim includes no language distinguishing these voltages as different values. And the '957 patent twice equates bias voltages with positive voltages. Ex.

1001, 11:7-8, 11:39. In fact, the patent refers to the (positive) voltage applied to word lines between the second adjacent memory cell and the BSG transistor ("WLs (<n-1)") as a "bias voltage." *Id.* 11:7-10, 11:39-41.

6. Claim 6

[6.PRE] "The apparatus of claim 3, wherein the processing circuitry is further configured to:"

174. Hongtao discloses or at least renders obvious *processing circuitry further configured to* perform the limitations of claim 6. *Supra* §IX.B.1.[1.A].

[6.A] "apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;"

175. This limitation is identical to claim [5.A]. Hongtao in view of Yu renders this limitation obvious for the same reasons. *Supra* §IX.B.5.[5.A].

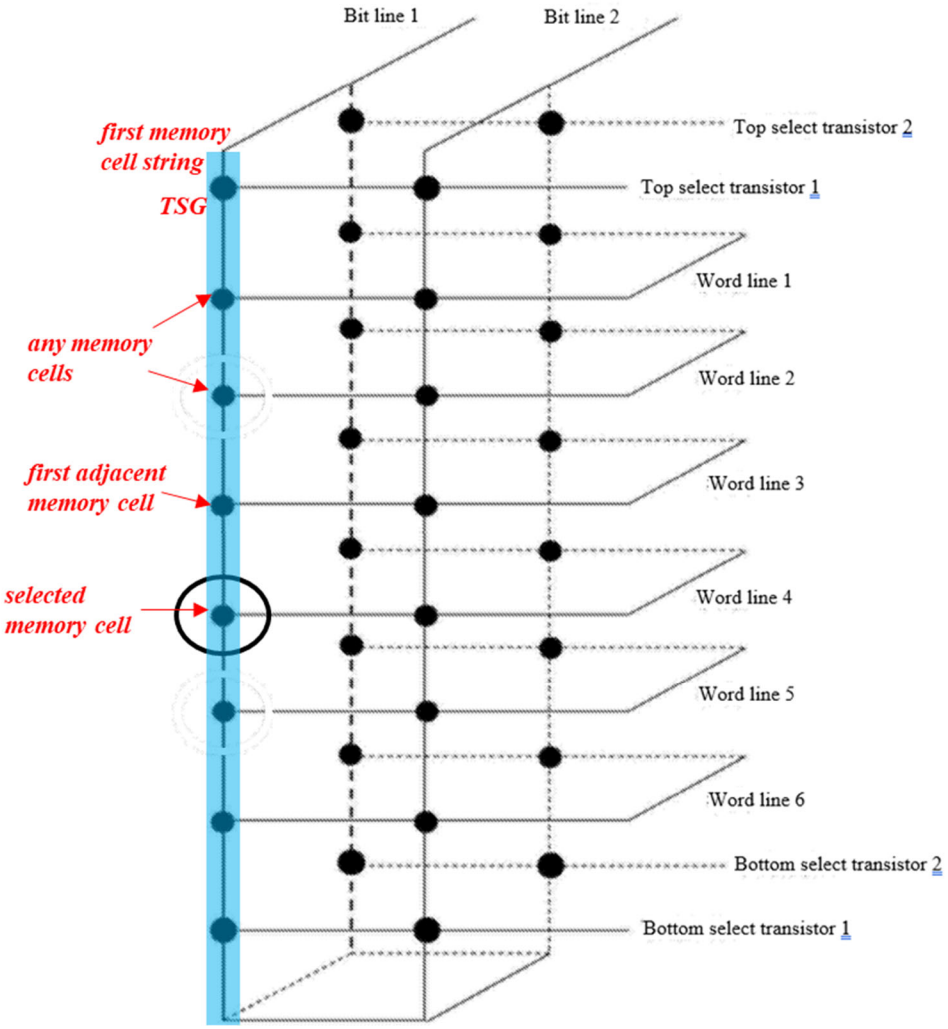
[6.B] "apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and"

176. This limitation is identical to claim [5.B]. Hongtao in view of Yu renders this limitation obvious for the same reasons. *Supra* §IX.B.5.[5.B].

[6.C] "apply a positive voltage on gate terminals of any memory cells that are positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage."

177. Hongtao discloses or at least renders obvious this limitation.

178. Just as claim 3 is the mirror image of claim 2, this limitation is the mirror image of claim [5.C]. The *any memory cells* may be *positioned* as shown:



Ex. 1005, Fig. 1 (expanded). *See* §IX.B.2.[2] (for obvious extension of Hongtao's memory string).

179. Because Hongtao's positive voltage is applied on all unselected word lines, including those above and below the selected memory cell, Hongtao discloses or at least renders obvious this limitation for the same reasons explained with respect to claim [5.C]. *Supra* §IX.B.5.[5.C].

7. Motivation to Combine

Programming Order

180. A POSITA would have been motivated, with a reasonable expectation of success, to apply Yu's teaching on programming order to Hongtao's memory device for several reasons.

181. First, while Hongtao discloses read operations, it is silent on program operations. It goes without saying that a memory that is read was programmed. Given that Hongtao does not discuss programming, a POSITA would have been motivated to consider other references, such as Yu, that do discuss programming. Further, both Hongtao and Yu disclose 3D NAND devices with vertical memory strings. Thus, Yu's programming teachings, particularly the sequential order of programming the strings, is particularly instructive to Hongtao's memory. Ex. 1005, Abstract, Fig. 1; Ex. 1006, [0004], Fig. 6.

182. Second, both Hongtao and Yu relate to reducing disturbance during memory operations. Ex. 1005, [0026], [0034]-[0035]; Ex. 1006, [0005]-[0006], [0010]. Thus, a POSITA considering Hongtao with that specific concern would look to programming references, such as Yu, that also have that concern. Put another way, a POSITA would look to further improve disturbance issues by considering references that complement Hongtao's teachings. This is evident from Hongtao's goal: to "improve the accuracy of … data." Ex. 1005, [0004].

183. Third, a sequential program order simplifies controller decoding operation since the address of the next page (word line) to be programmed in the sequence would not need to be fetched again from the controller once the programming operation commences; and allows the programming operation to take advantage of the knowledge of the state of the neighboring cells to reduce disturb and/or compensate for parasitic effects.

184. Specifically, sequential programming enables identifying whether the rows above or below the selected row are programmed or erased. In practice and in simple terms, a pointer (that has a variable row address) would indicate the next row to program. With a B2T approach, for example, all rows below this pointer (row address) are programmed and all rows above are erased. Such information can be taken into account during access operations to mitigate various issues that can inadvertently alter the data state of memory cells. In other words, this knowledge can assist in preventing errors in access operations. *E.g.*, Ex. 1023, 8:18-53. Thus, sequential programming enables easily applying these mitigation techniques.

185. Fifth, again, it goes without saying that programming is a necessary operation to implement on Hongtao's device. Yu's sequential program order was a conventional approach. Examples include Ex. 1014, 45 (Fig. 2.12); Ex. 1021, [0110]-[0112]. Again, all that is necessary is an incrementing pointer that progresses up or down the strings.

186. A POSITA would have had a reasonable expectation of success in applying Yu's well-known technique to Hongtao. First, per above, both Hongtao and Yu are in the context of 3D NAND devices. More specifically, Yu's approach applies to memory strings, just as Hongtao discloses. Thus, B2T and T2B directly apply to Hongtao's vertical memory strings. Second, the sequential program order was conventional, textbook material, and such implementation merely involves using a pointer (that points to a row via a row address) to identify the next-to-program row. Ex. 1014, 45 (Fig. 2.12); Ex. 1021, [0110]-[0112]. After each program, the pointer increments to the next row to program. In fact, such an approach, as I describe above, simplifies decoder operation.

Using Read to Verify

187. A POSITA would have been motivated, with a reasonable expectation of success, to employ Hongtao's read operations in a program-verification loop in view of Yu and the knowledge of a POSITA for several reasons. I refer to the knowledge of a POSITA here to emphasize that in my opinion, it was readily apparent that Hongtao's read operation would be understood in view of the knowledge of a POSITA to be applicable to a verification operation because that was a basic use of a read operation.

188. Yu discloses: "Each program loop may include a program operation and a program verification operation." Ex. 1006, [0049]. This refers to the basic

programming process of a programming pulse and then the read (verification) to determine whether the programming pulse was sufficient for the memory cell to reach the correct data state. If not, the cycle repeats. §VI.B. A POSITA reading this would have understood that Hongtao's read operation was suitable for the "verification operation."

189. First, it was well known that read operations and verify operations are virtually identical. I describe this in §VI.B. A POSITA understood that "the read operation may include the verification read operation for verifying the success of the program operation or the normal read operation for determining the data stored in the memory cells." Ex. 1021, [0103]. By "normal read operation," this refers to a read that does not immediately follow a program operation and that does not verify the program operation. Imagine taking a picture. When this occurs, the data is programmed into the memory and the read operation will verify that the program was successful. Of course, as I describe in §VI.B, this may involve several program/verify cycles. Later on, when viewing that picture, "normal read operations" retrieve the data to display the picture. Thus, a read operation for both verifying and normal reads are the fundamental uses of the read algorithm in Flash memories.

190. Second, the details of this read algorithm are important to reduce issues relating to the various disturb mechanisms that I discuss throughout this declaration.

In short, a read operation can inadvertently alter the data state of the target and other memory cells. In simple terms, this means a read operation can actually corrupt the data in the memory. These concerns are no less important when verifying a program operation, because the read operation to verify programming can cause the exact same problems. Thus, Hongtao's read operation that mitigates these issues would have been equally applicable to mitigate these issues for either a normal read or for a read that verifies a programming operation.

191. Third, as I discuss above, the read operation is very important to mitigate the various disturb issues. As a result, a read operation is not something that designers simply select and implement. Rather, there is significant testing to arrive at the ideal read operation that balances the various disturb issues with performance. Once arriving at a suitable read operation that strikes the right balance, a POSITA would have been highly motivated to employ that same operation, rather than creating an entirely different operation. I describe below the slight tweak to the read voltage for verification. This only slightly changes the voltage on the selected word line during the sensing stage.

192. A POSITA would have had a reasonable expectation of success in employing Hongtao's read operation for verification. First, it was already known that a read operation applies both to normal reads and verifications. Ex. 1021, [0103].

193. Second, how to use a read operation for both purposes was well understood. In a normal read operation, the read voltage (the voltage applied on the selected word line during sensing) is typically set between threshold voltage ranges for adjacent data states (for multi-level cells). In a verify operation, instead of a read voltage, a verify voltage is used. *See* Ex. 1024, [0181]. Setting different voltage levels for read and verify operations was a routine practice. *See* Ex. 1019, 25:2-8; Ex. 1005, [0054]-[0055]. There is just a slight difference in these voltages, because, for example, the verify voltage may be set to the low end of the threshold distribution and the read voltage is between data states (for multi-level cells). *Id.* The voltages on other memory elements are kept the same, because those voltages relate to mitigating issues relating to inadvertently altering data states.

194. As I discuss earlier, read disturb can be caused by two different physical mechanisms: one due to a high vertical electrical field, perpendicular to the channel, across a given memory cell that causes unintentional F-N injection; and one due to a high electric field parallel with the channel of a given memory cell that causes hot carrier injection (HCI). The F-N type of disturb tends to occur on the selected string when the channel is biased at 0V or at a low bit line voltage. The HCI disturb tends to occur on an unselected memory string whose channel is disconnected from the bit line voltage. In this situation, read disturb can occur when read operations repeatedly apply high pass voltages on unselected word lines, which induces a boosting effect

of the channel potential, leading to hot-carrier injection ("HCI"). By judiciously setting the voltages on the other memory elements, Hongtao attempts to reduce the HCI induced read disturb on the unselected strings by locking the channel voltage during a pre-conduction period, while also being cognizant of the "conduction voltage" on the unselected word lines not causing read disturb on the selected string due to the voltage difference of (conduction voltage – driving voltage) perpendicular to the channel. All of this is to say that a POSITA would have understood that Hongtao carefully balances these issues, and thus had an expectation that Hongtao's read operation would be suitable for verification.

195. Third, Hongtao already discloses circuitry to generate different read voltage levels, e.g., VrEr/A, VrA/B, VrB/C in Ex. 1017, Fig. 6. Thus, generating additional levels for verify operations (e.g., VvA, VvB, and VvC) simply uses this same type of circuitry. Ex. 1017, Fig. 6.

196. Finally, I should note that Hongtao does not specifically address the issue of fast-charge loss, which is only an issue in charge-trap memories. The claims of the '957 patent are not limited to charge-trap memories. Nonetheless, even if one were to consider charge-trap memories, another patent assigned to the Patent Owner, U.S. Patent No. 11,600,342 (Ex. 1025), describes one way to address fast-charge loss in view of the timing of the verification operation. Namely, in the pre-verify stage, an electric field may be created to remove the fast charges before verification.

However, there were other known ways to deal with this issue, including adjusting the verification voltages given the expected fast-charge loss. Suzuki, [0150].[3]

C. *Ground 2*: Claims 1-6 Are Anticipated by Suzuki

197. In my opinion, a POSITA would have considered Suzuki to be within the scope of the prior art and highly relevant to the patentability of the '957 patent's claims.

198. In my opinion, Suzuki anticipates claims 1-6 obvious.

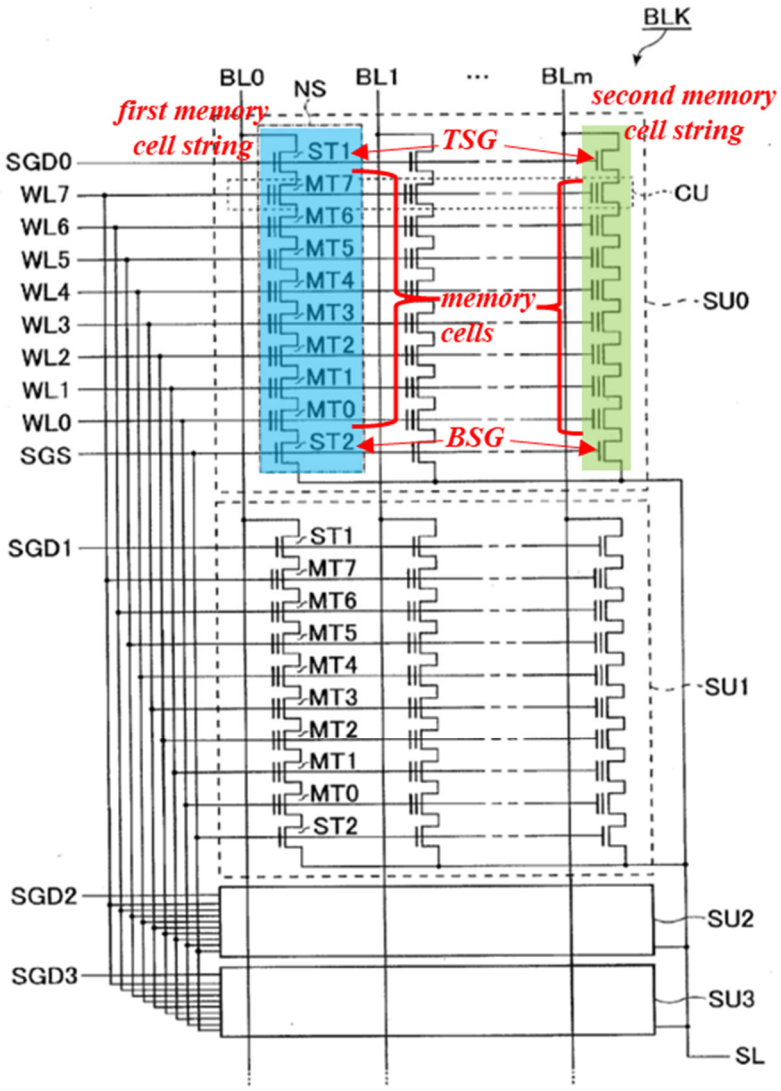
1. Claim 1

[1.PRE] "An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising:"

199. To the extent the preamble is limiting, Suzuki discloses it.

[3] Hongtao discloses or at least renders obvious processing circuitry, with or without Yu. §IX.B.1.[1.A]. To the extent Yu is used to render processing circuitry obvious, a POSITA would have found it obvious to combine Yu's processing circuitry with Hongtao's memory device with a reasonable expectation of success because Yu's circuitry was conventional, routine, and well understood, and processing circuitry such as Yu's was a necessary component in memory devices like Hongtao's.

200. Suzuki discloses a semiconductor device comprising drain select transistors (*TSG transistor*) (again, the drain is usually on the top), source select transistors (*BSG transistors*) (again, the source is usually on the bottom), and *memory cells*. Ex. 1007, Abstract. Suzuki expressly discloses that its device is for the program-verify loop, and thus is *an apparatus for reading a memory device*. *Id.* Below are *a first memory cell string* (highlighted blue) *and a second memory cell string* (green):

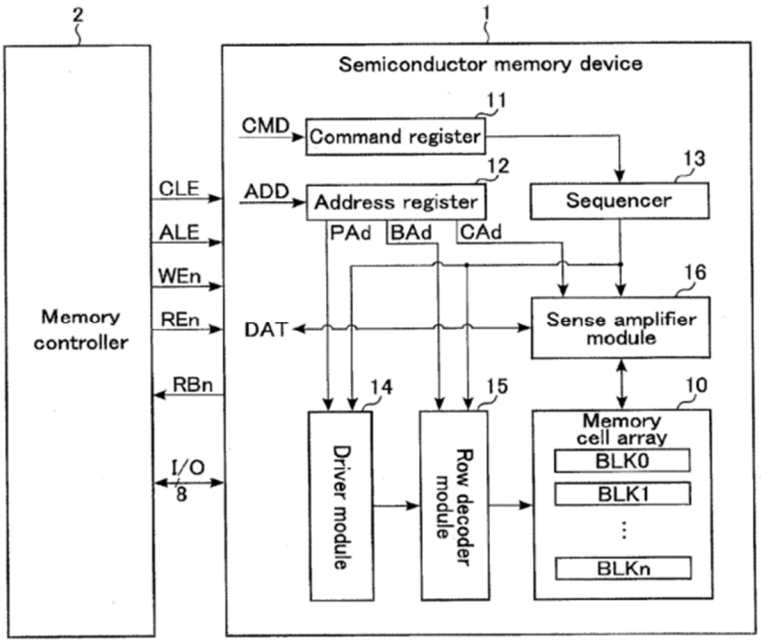


Id., Fig. 2; *see also id.*, [0049] (*connected in series*); [0047]-[0050]; [0048], [0232] (each memory string comprising a drain select transistor ST1 and a source select transistor ST2).

[1.A] "processing circuitry configured to:"

201. Suzuki's controller in conjunction with components including a driver module and a row decoder ("*processing circuitry*") apply various voltages in the

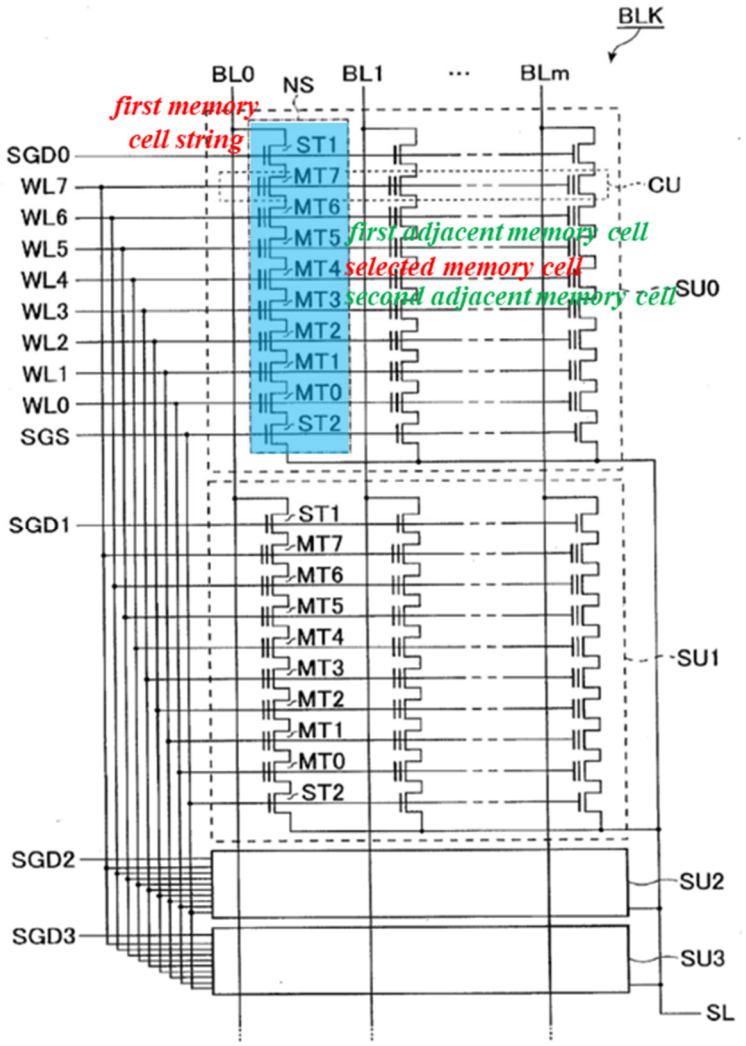
verify and pre-verify operations. Ex. 1007, [0038]-[0040], [0117]. The row decoder will determine the appropriate row to access.



Id., Fig. 1; *see also id.*, [0034], Fig. 3.

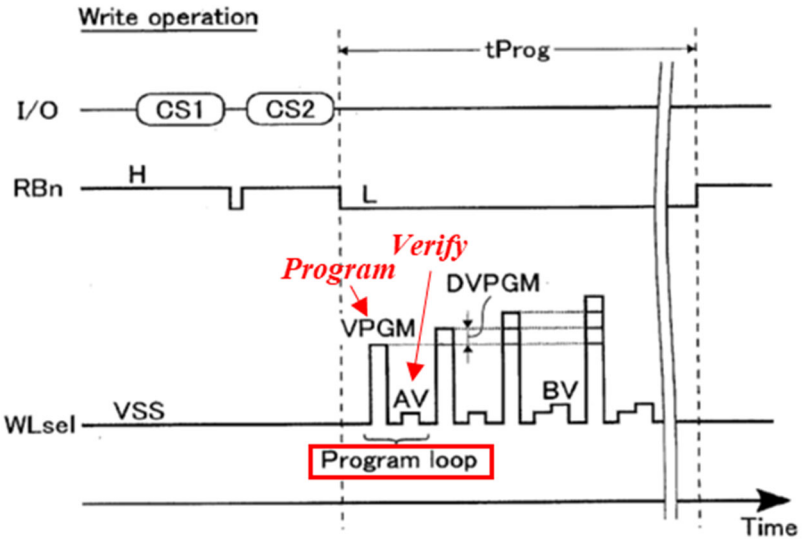
[1.A.i] "apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;"

202. Suzuki discloses operations to verify a "memory cell transistor MT." Ex. 1007, [0125]. For purposes of illustration, I am using MT4 as *a selected memory cell of the first memory cell string*:



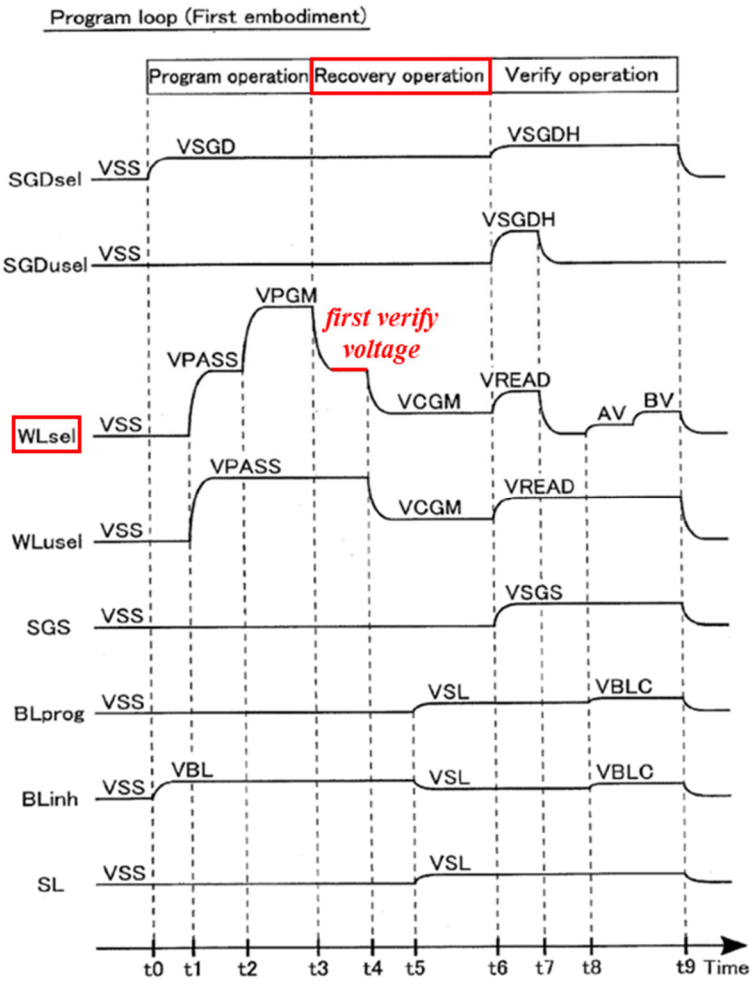
Id., Fig. 2. As shown, MT4 *[is] arranged between a first adjacent memory cell* (MT5) *and a second adjacent memory cell* (MT3).

203. Suzuki discloses a program loop comprising a program operation followed by a verify operation. Ex. 1007, Abstract, [0124]-[0125]. Again, this cycle may repeat several times to successfully program the memory cell. The sequence is illustrated below:



Id., Fig. 10, [0122]. Accordingly, at the time the *selected memory cell* undergoes verification, it is *programmed*. Note that the first pulse programs the cells. Ultimately, a verification occurs on the final pulse that fully programs the cell if multiple pulses are necessary.

204. As explained above, the gate terminal of a memory cell is coupled to a word line. *Supra* §VI.A. Suzuki refers to "a selected word line … as WLsel." Ex. 1007, [0117]. Suzuki further discloses applying voltage VPASS to WLsel at time t3 in a recovery operation before the verify operation, i.e., *in a pre-verify stage*. *Id.*, [0137]. These word lines in 3D memories are typically conductive gate layers through which the memory strings vertically extend.



Id., Fig. 11. This VPASS constitutes *a first verify voltage on ... [the] selected memory cell*. VPASS is a term of art, and it means a voltage that turns on a transistor. Pass refers to creating a conductive path in which the current passes.

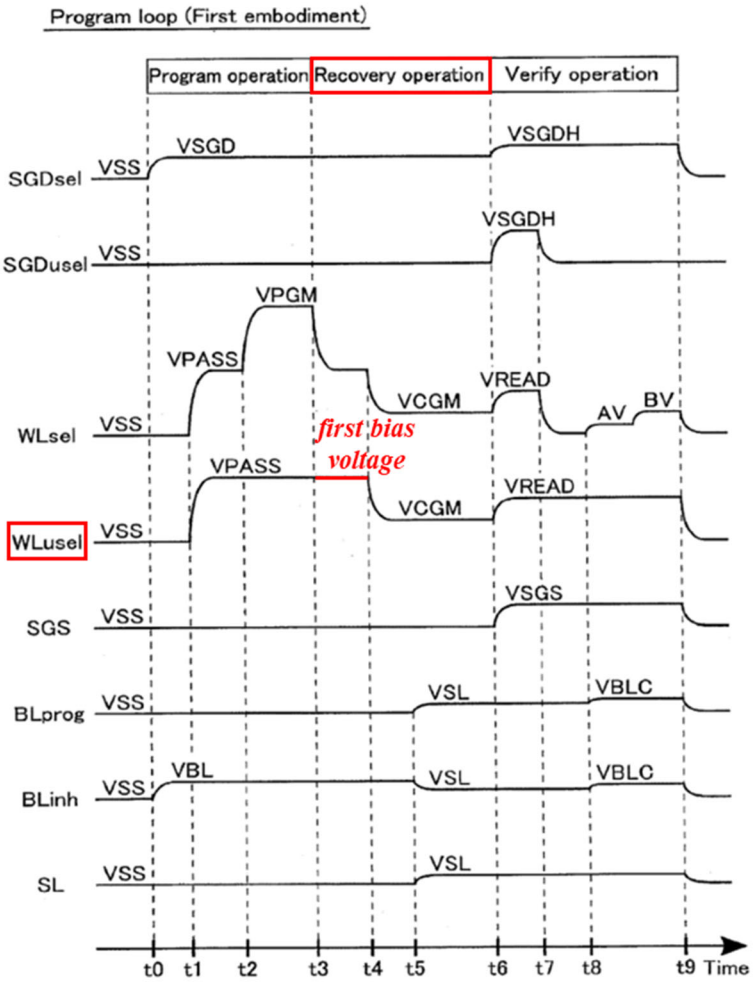
205. Note that Suzuki's recovery operation is a *pre-verify stage*. First, in reviewing the claims of the '957 patent, I have found no language to suggest that the *pre-verify stage* is a stage other than one that comes before the verification, because the claim simply uses ("pre-") to indicate that it comes before the verify stage. That said, the '957 patent makes clear that *pre-verify stage* comes before, and is separate

from, the *verify stage*. Ex. 1001, Figs. 4-9. The specification describes what occurs in the pre-verify stage, but does not describe exactly when it occurs, except that it comes before the *verify stage*. *E.g.*, *id.*, Abstract. The specification, however, does suggest that the "pre-verify scheme" assists with the "verify/read [of] programmed memory cells." *Id.*, 7:13-18. I have found no definitional language or statements on what *pre-verify* is not in the specification.

206. In view of the '957 patent, Suzuki's "recovery period" is a *pre-verify stage*. First, it is separate from, and comes before, the verify step. Ex. 1007, Fig. 11. Suzuki discloses that "a period from time t0 to time t3 corresponds to a program operation, a period from time t3 to time t6 corresponds to a recovery operation, and a period from time t6 to time t9 corresponds to a verify operation." *Id.*, [0131]. At t3, the programming operation is complete, because VPGM terminates. *Id.*, [0137]. VPGM is a very high voltage that causes charge to accumulate in the storage layer of the memory cells. The recovery operation functions to recover from the program operation and prepare for what follows, namely, a verify operation. *Id.*, [0131]. That is, this step is after the program is complete and prepares for the next part of the loop—verification.

[1.A.ii] "apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;"

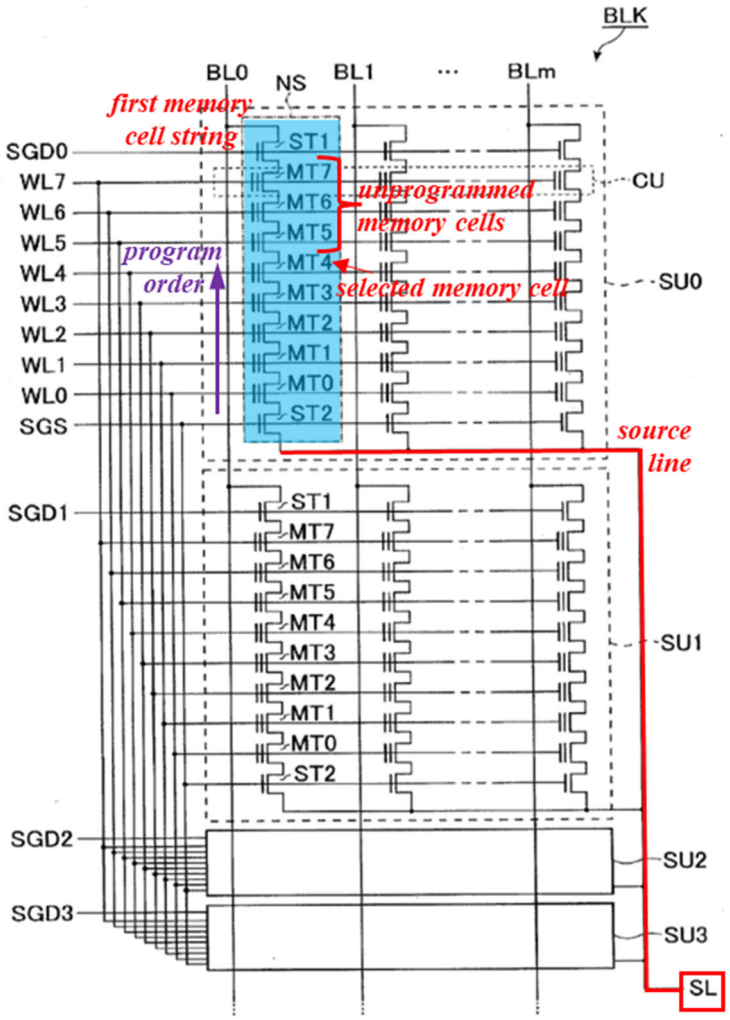
207. Suzuki refers to "non-selected word line[s]" as WLusel. Ex. 1007, [0117]. *[I]n the pre-verify stage*, voltage VPASS is applied to WLusel:



Id., Fig. 11; *see also id.*, [0134]. The unselected word lines are coupled to, e.g., unselected memory cells MT5 through MT7 in the illustrated scenario. *Supra* §IX.C.1.[1.A.i]. Thus, Suzuki discloses applying *a first bias voltage* (VPASS) *on …*

at least one memory cell (e.g., MT6 or MT7) *of the first memory cell string* (the selected string)

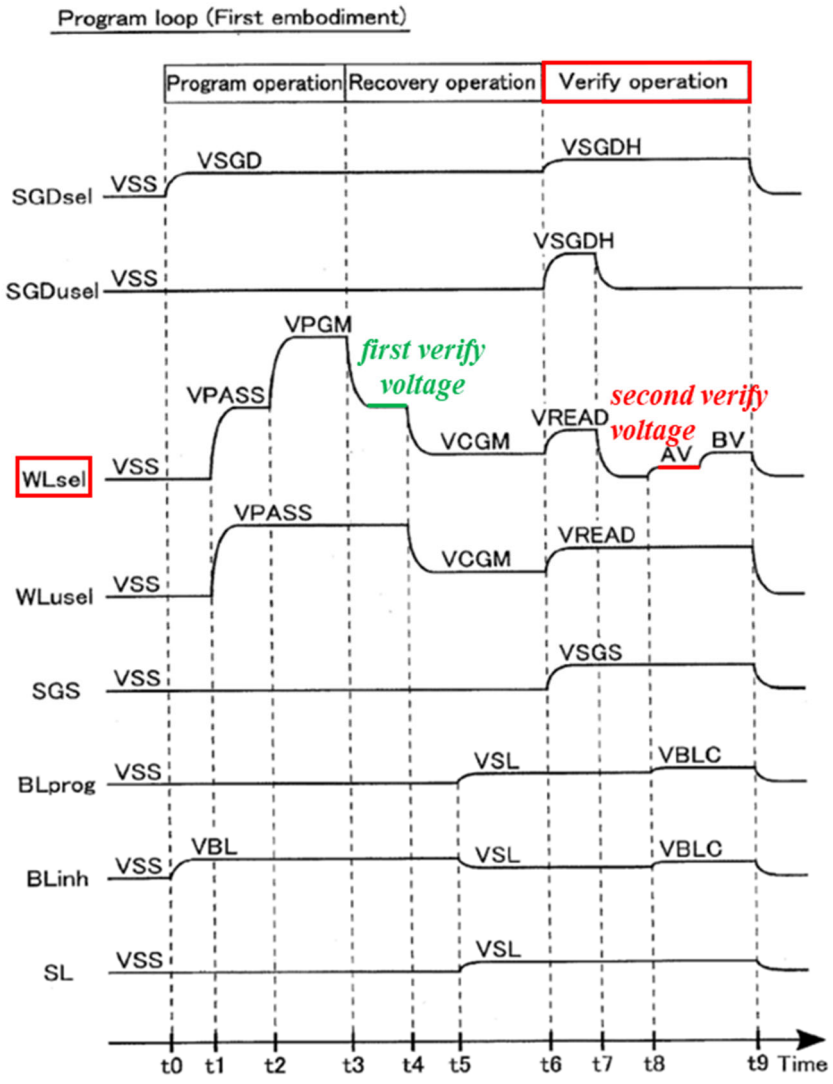
208. Suzuki discloses that this *at least one memory cell* (e.g., MT6 or MT7) *... is not programmed*. In Suzuki's embodiment, memory cell MT0 is at the end of the source line side. And the program operation may proceed "from cell units CU on the source line SL side in sequence." Ex. 1007, [0116].



Id., Fig. 2. Thus, when MT4 is selected for programming verification, MT6 and MT7 are not programmed. *Id.*, [0140].

[1.A.iii] "apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and"

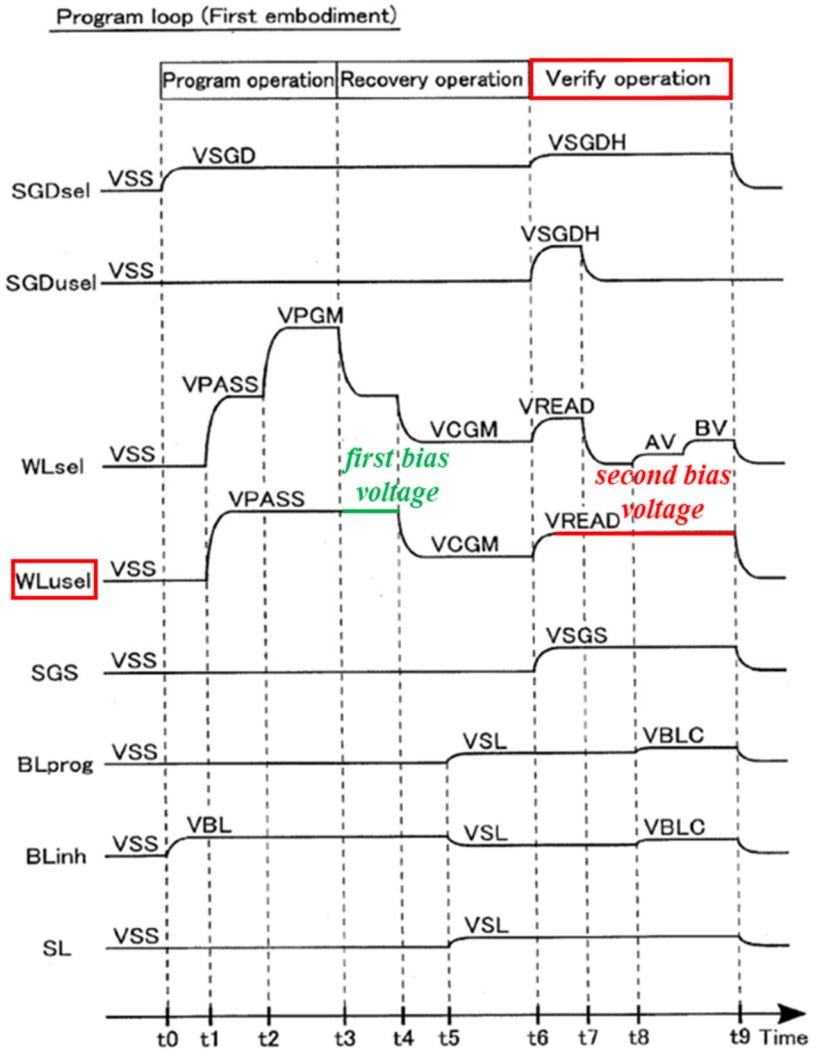
209. Suzuki discloses *apply[ing], in a verify stage* (verify operation), *a second verify voltage* (verify voltage AV) *on … the selected memory cell* (e.g., MT4) *of the first memory cell string*.



Ex. 1007, Fig. 11, [0144].

[1.A.iv] "apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage."

210. Suzuki discloses applying *a second bias voltage* (VREAD) through the same unselected word lines to *the at least one memory cell in the verify stage*:

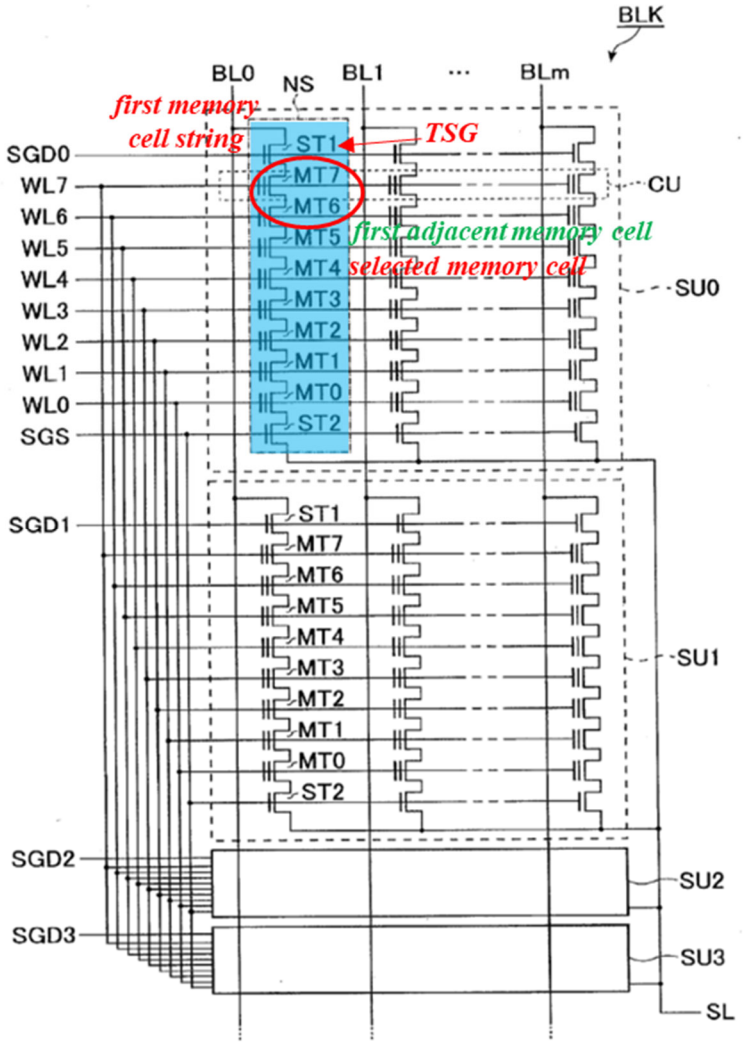


Ex. 1007, Fig. 11; *see also id.*, [0142]. VREAD may be 8V. *Id.* VPASS may be 10V. *Id.*, [0134]. Thus, *the second bias voltage* (VREAD) *is smaller than the first bias voltage* (VPASS).

2. Claim 2

[2] "The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string."

211. Claim 2 refers to the *not programmed memory cell* of claim [1.A.ii] and [1.A.iv]. That memory cell can be MT6 or MT7. *See* §§IX.C.1.[1.A.ii], X.A.6. Either MT6 or MT7 satisfies this limitation:



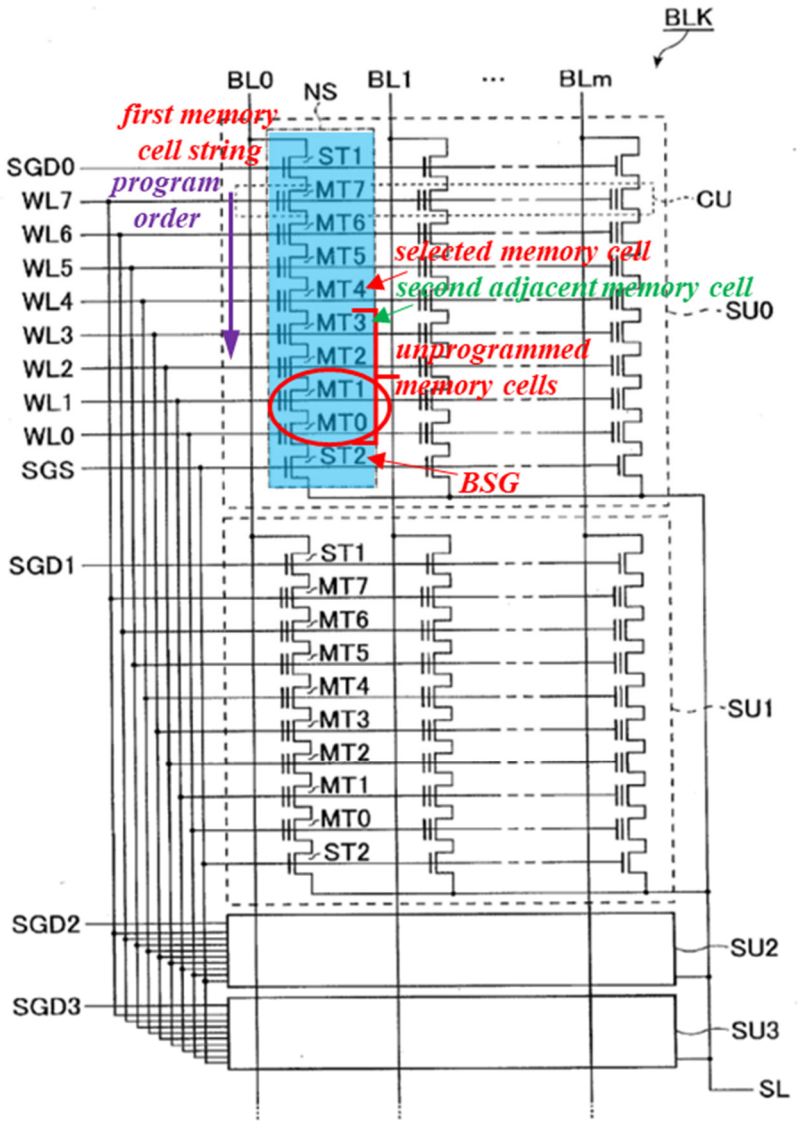
Ex. 1007, Fig. 2; *see also id.*, [0232] (drain select transistor ST1 is the *TSG*).

3. Claim 3

[3] "The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string."

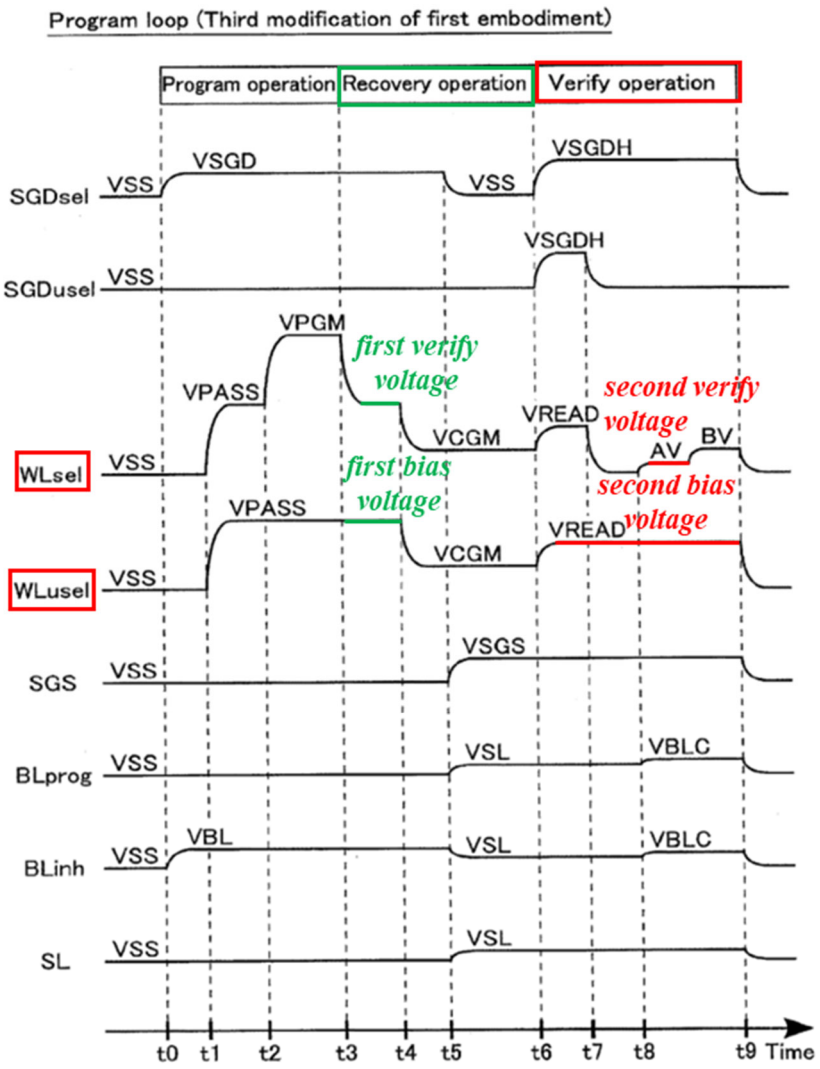
212. As explained in Ground 1, claim 3 requires an unprogrammed memory cell positioned *below* the second adjacent memory cell. *Supra* §IX.C.

213. Claims 1 and 2 above have been described using an embodiment wherein the drain side contains the last cell (e.g., MT6 and MT7) to be programmed. Suzuki further discloses, however, that programming can proceed from the drain side to the source side. Ex. 1007, [0170]. This can be illustrated as follows:



Id., Fig. 2. In this embodiment, the *selected memory cell* may still be MT4, and the *at least one memory cell* may be, e.g., MT0 or MT1 and is unprogrammed, because of the drain-to-source directional programming.

214. This embodiment satisfies claim 3 as shown:



Ex. 1007, Fig. 16; *see also id.*, [0171]-[0174] (describing modifications from Figure 11 to Figure 16 that are irrelevant to claim 3.

4. Claim 4

[4.PRE] "The apparatus of claim 1, wherein the processing circuitry is further configured to:"

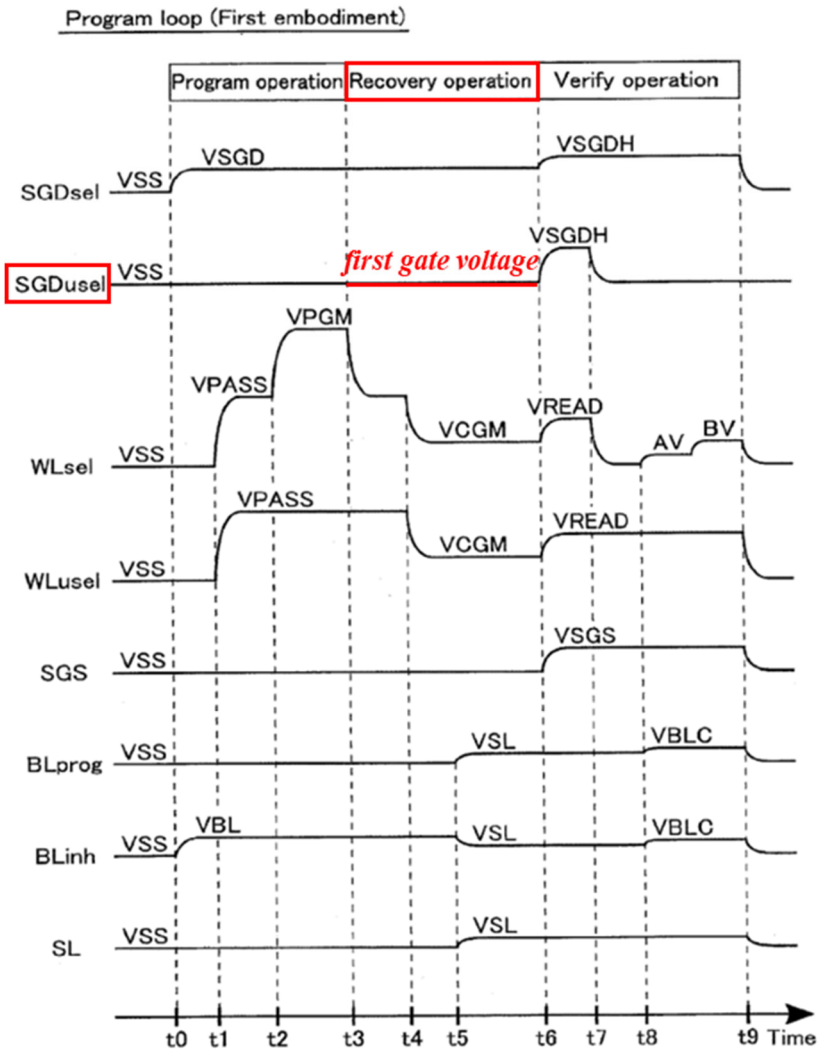
215. Suzuki discloses *processing circuitry further configured to* perform the limitations of claim 4. *See* §IX.C.1.[1.A].

[4.A] "in the pre-verify stage,"

216. The pre-verify stage corresponds to Suzuki's "recovery operation." *Supra* §§IX.C.1.[1.A.i]-[1.A.ii].

[4.A.i] "apply a first gate voltage on a gate terminal of the TSG transistor of the second memory cell string,"

217. *The second memory cell string* is an unselected memory string since the selected memory cell is the first memory cell string. Ex. 1001, 17:42-43 (limitation [1.A.i]). Further, based on the specific context of the '957 patent, a ground or zero voltage can be "applied." *Id.*, 10:57-61, 11:19-23, 11:35-39. Suzuki refers to the line coupled to *TSG transistor of the [unselected,] second memory cell string* as SGDusel. Ex. 1007, [0117]. Suzuki discloses *apply[ing] a first gate voltage* to this *TSG transistor*:

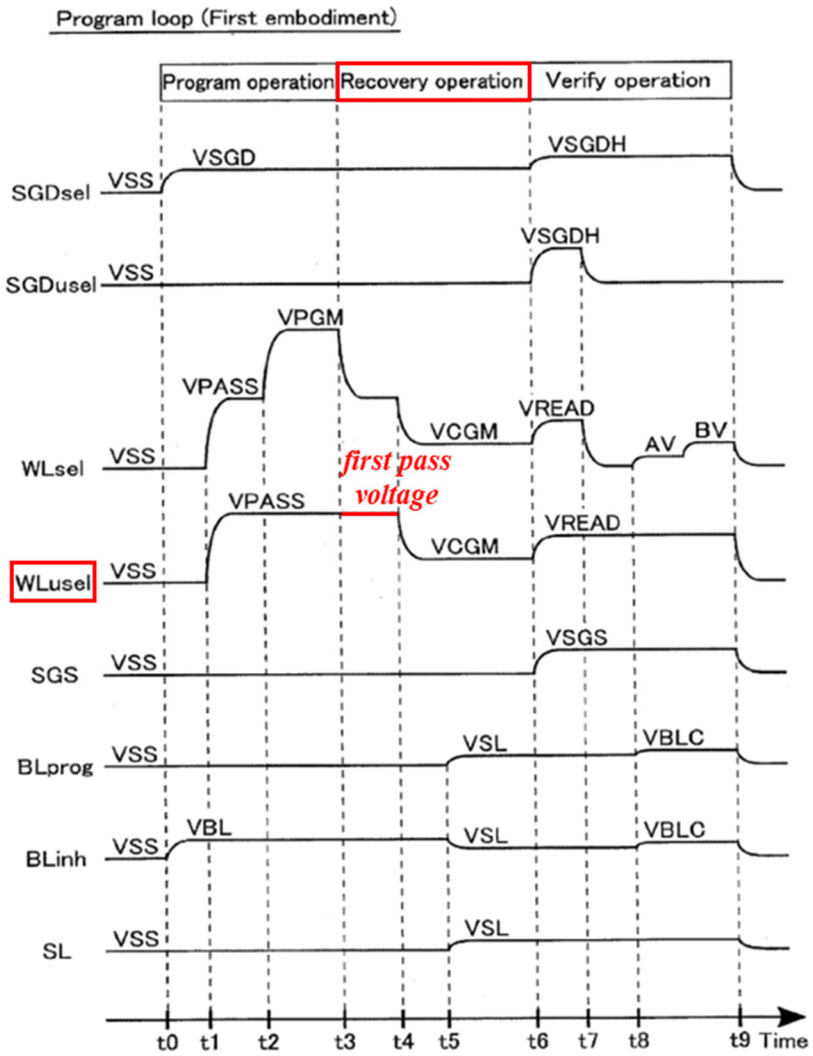


Id., Fig. 11; *see also id.*, [0130].

[4.A.ii] "apply a first pass voltage on a gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and"

218. Suzuki discloses applying voltage VPASS to WLusel. *Supra* §IX.C.1.[1.A.ii]. WLusel includes WL5, coupled to *the first adjacent memory cell of the selected memory cell*. *Id.* As explained in Ground 1, the '957 patent does not require the first bias voltage of claim 1 and the first pass voltage of claim 4 to have

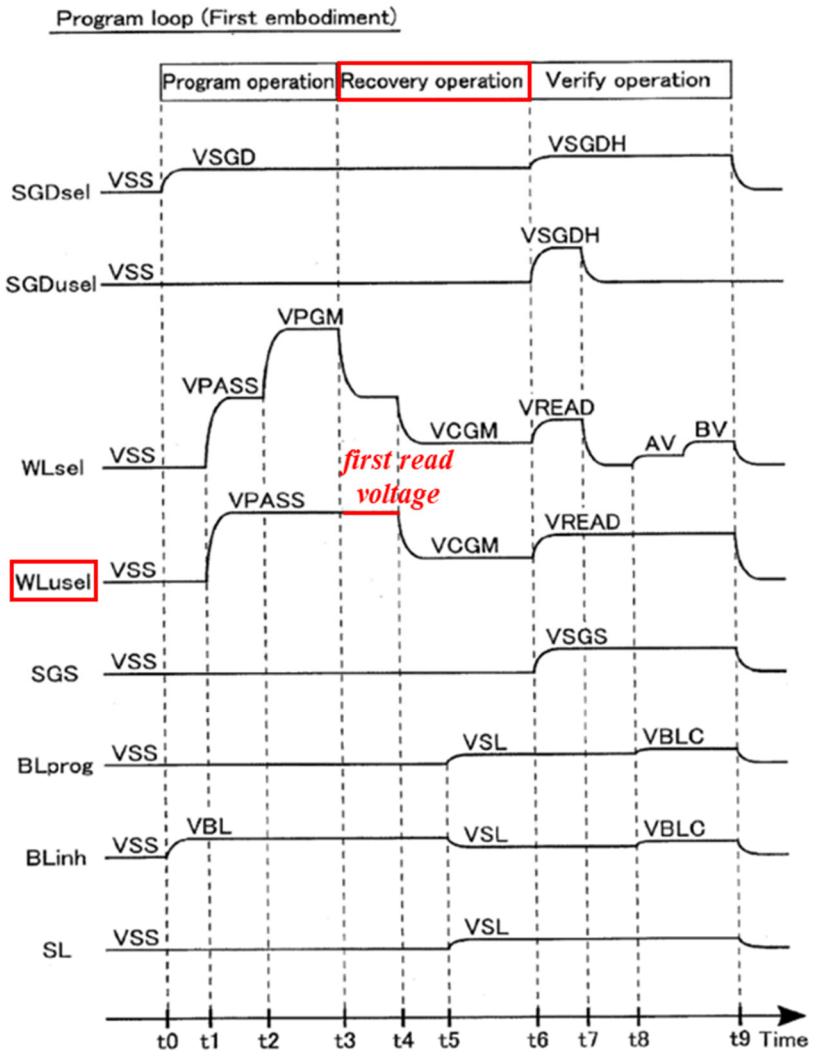
different values, or even that they be distinct voltages. *See* §IX.B.4.[4.A.ii]. Thus, VPASS may constitute *a first pass voltage*.



Ex. 1007, Fig. 11.

[4.A.iii] "apply a first read voltage on a gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string; and"

219. Suzuki discloses applying the VPASS voltage to unselected word lines in the *pre-verify stage* (recovery operation).



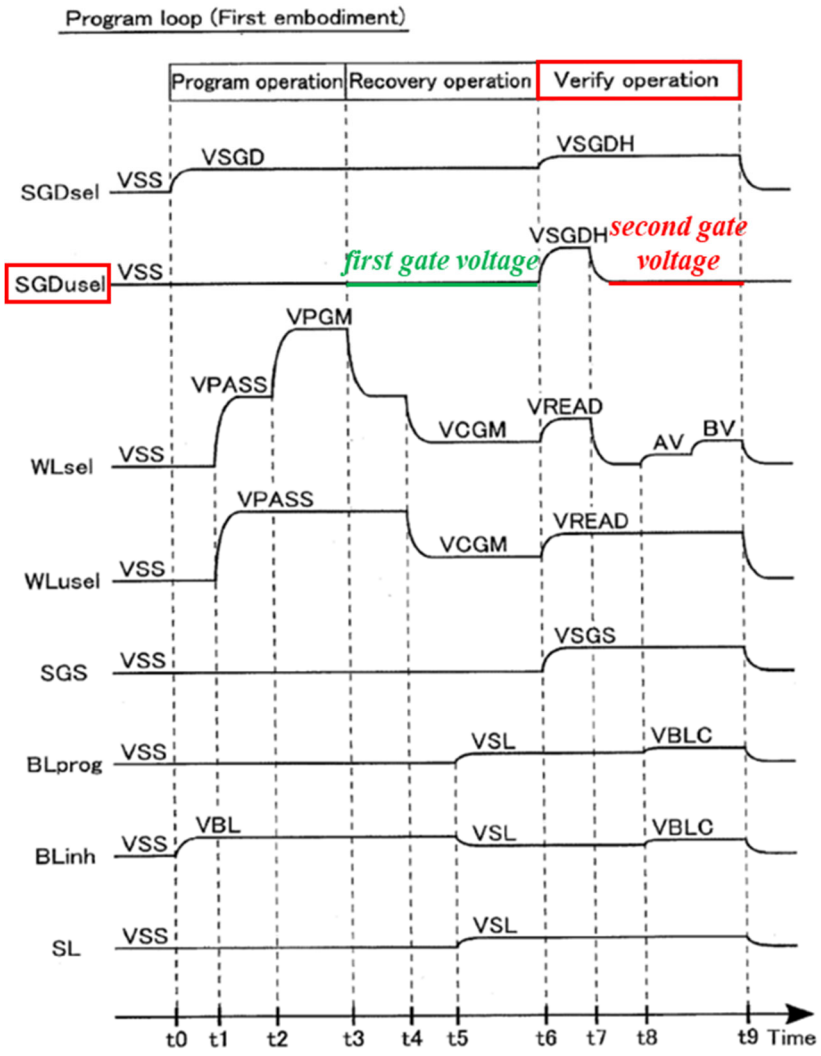
Ex. 1007, Fig. 11. As explained in Ground 1, the '957 patent does not require the first bias voltage of claim 1 and the first read voltage of claim 4 to have different values, or even that they be distinct voltages. *Supra* §IX.B.4.[4.A.iii]. Thus, this voltage constitutes the *first read voltage on … the second adjacent memory cell* (e.g., MT3) *… in the first memory cell string*.

[4.B] "in the verify stage,"

220. The verify stage corresponds to Suzuki's "verify operation." *Supra* §§IX.C.1.[1.A.iii]-[1.A.iv].

[4.B.i] "apply a second gate voltage on the gate terminal of the TSG transistor of the second memory cell string,"

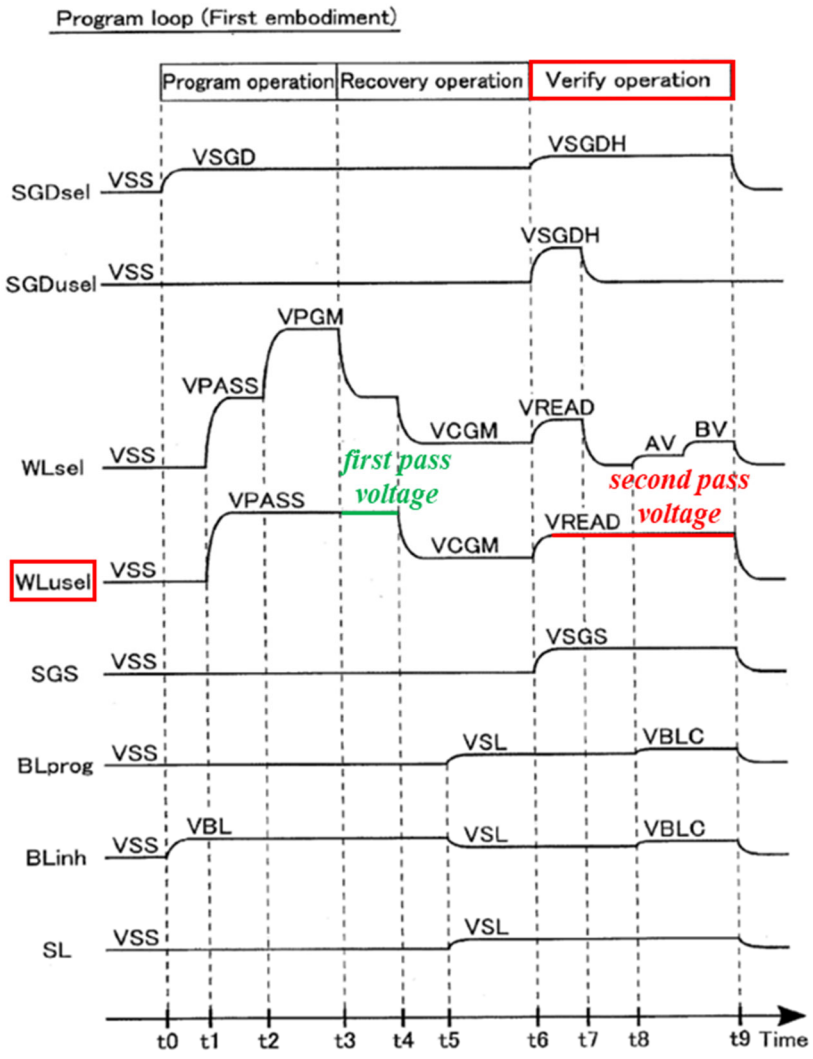
221. This limitation refers to the same transistor in claim [4.A.i] during the subsequent verify stage. *Supra* §IX.C.4.[4.A.i]. The *second gate voltage* is shown below:



Ex. 1007, Fig. 11. This VSS voltage turns off the source select transistor. *Id.*, [0143].

[4.B.ii] "apply a second pass voltage on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and"

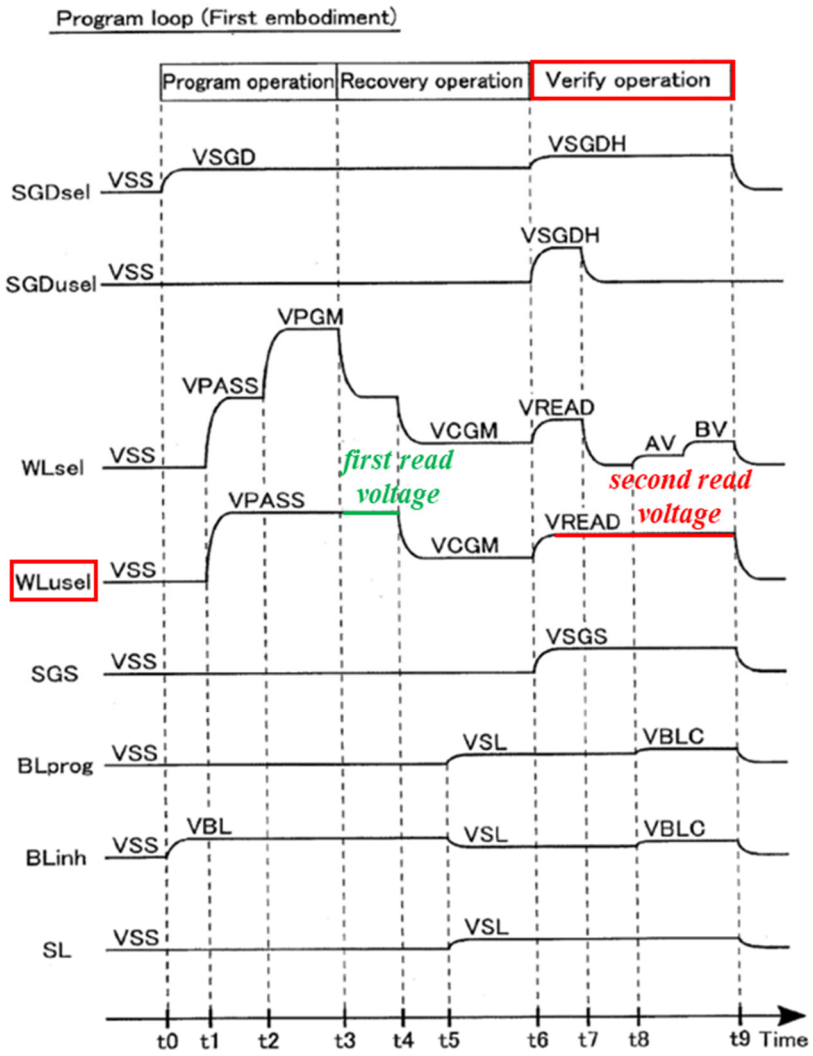
222. This limitation refers to the same transistor in claim [4.A.ii] during the subsequent verify stage. *Supra* §IX.C.4.[4.A.ii]. The *second pass voltage* is shown below:



Ex. 1007, Fig. 11; *id.*, [0142]. Vread is, for example, 8 volts and turns on those transistors and is a pass voltage. *Id.*

[4.B.iii] "apply a second read voltage on the gate terminal of the second adjacent memory cell of the selected memory cell of the first memory cell string, wherein"

223. This limitation refers to the same transistor in claim [4.A.iii] during the subsequent verify stage. *Supra* §IX.C.4.[4.A.iii]. The *second read voltage* is shown below:



Ex. 1007, Fig. 11; *id.*, [0142].

[4.C] "at least one of the second pass voltage and the second read voltage is larger than the second gate voltage."

224. Both the second pass voltage and the second read voltage are Suzuki's VREAD. *Supra* §§IX.C.4.[4.B.ii]-9. The second gate voltage is VSS. *Supra* §IX.C.4.[4.B.i]. VREAD may be 8V. Ex. 1007, [0142]. VSS may be 0V. *Id.*, [0130]. Thus, *the second pass voltage and the second read voltage [are] larger than the second gate voltage*.

225. An alternative second gate voltage for claim [4.B.i] and [4.C] is VSGDH, which is applied on SGDusel in the verify operation and may be 6V, which also is lower than VREAD's 8V. Ex. 1007, Fig. 11, [0142].

5. Claim 5

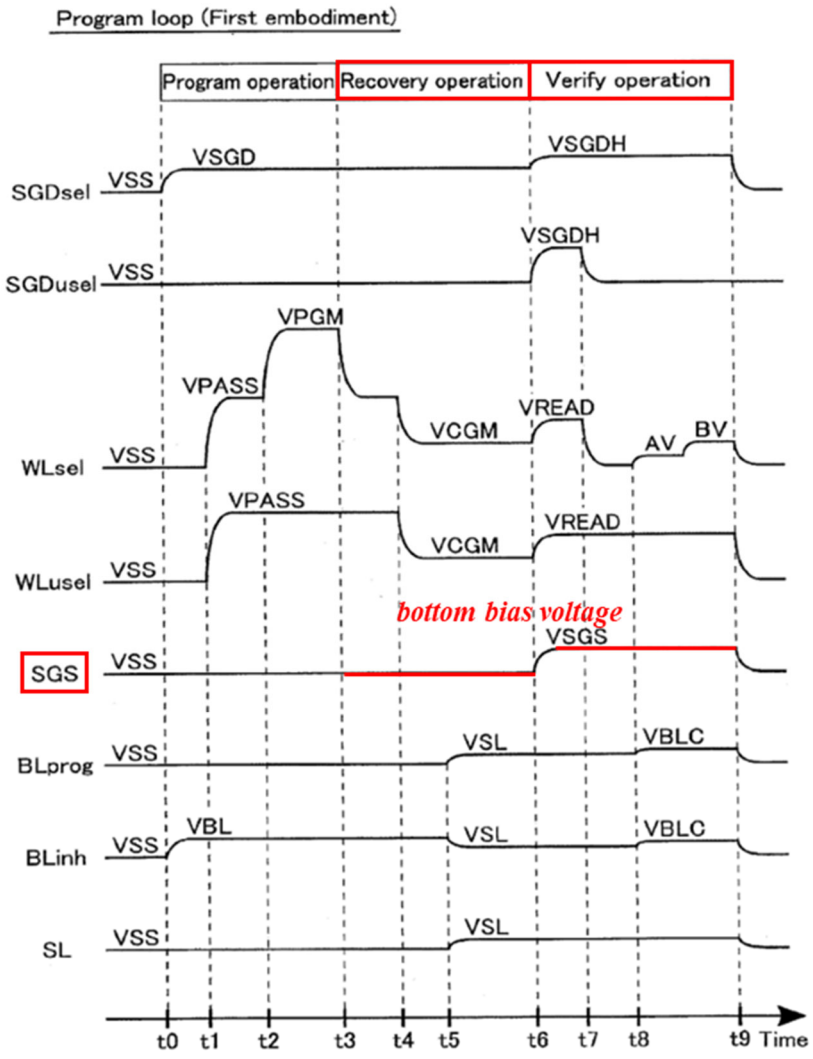
[5.PRE] "The apparatus of claim 2, wherein the processing circuitry is further configured to:"

226. Suzuki discloses *processing circuitry further configured to* perform the limitations of claim 5. *Supra* §IX.C.1.[1.A].

[5.A] "apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;"

227. As explained in Ground 1, "a bottom bias voltage" need not have only one voltage level. *Supra* §IX.B.5.[5.A].

228. Suzuki discloses *apply[ing] a bottom bias voltage* (VSS and VSGS) *on … the BSG transistor of the first memory cell string in the pre-verify stage* (the recovery operation) *and the verify stage* (the verify operation):



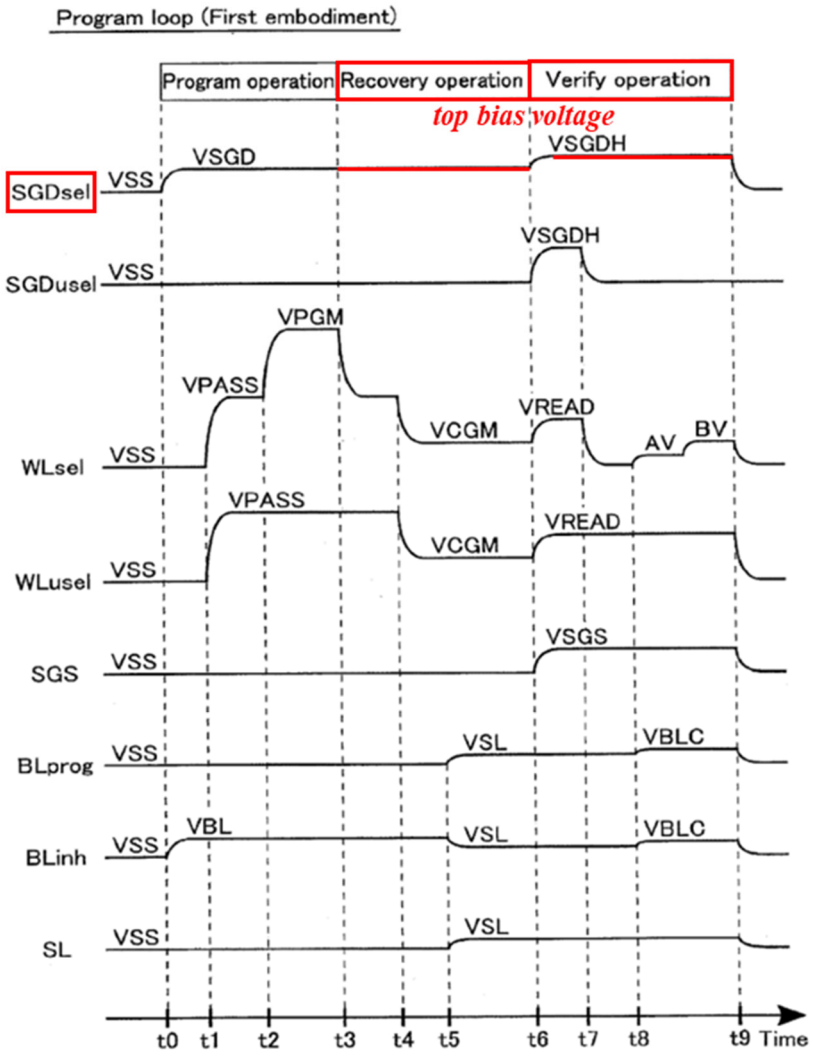
Ex. 1007, Fig. 11, [0142]. VSGS is high enough to turn on the BSG transistor ST2.

Id.

[5.B] "apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and"

229. As explained in Ground 1, "a top bias voltage" also need not have only one voltage level. *Supra* §IX.B.5.[5.B].

230. Suzuki discloses *apply[ing] a top bias voltage* (VSGD and VSGDH) *on … the TSG transistor of the first memory cell string* (the selected string) *in the pre-verify stage* (the recovery operation) *and the verify stage* (the verify operation):

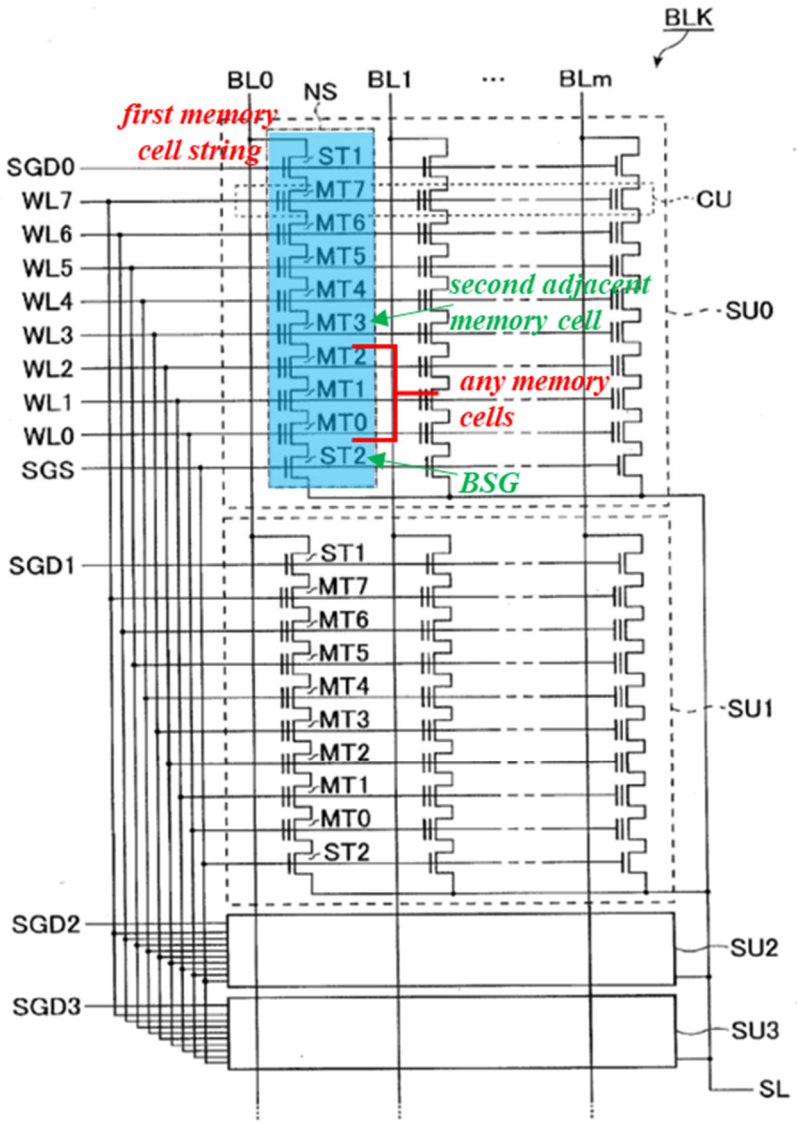


Ex. 1007, Fig. 11, [0133], [0142]. VSGD and VSGDH are high enough to turn on the top select (TSG) transistor. *Id.*, [0133], [0142].

[5.C] "apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage."

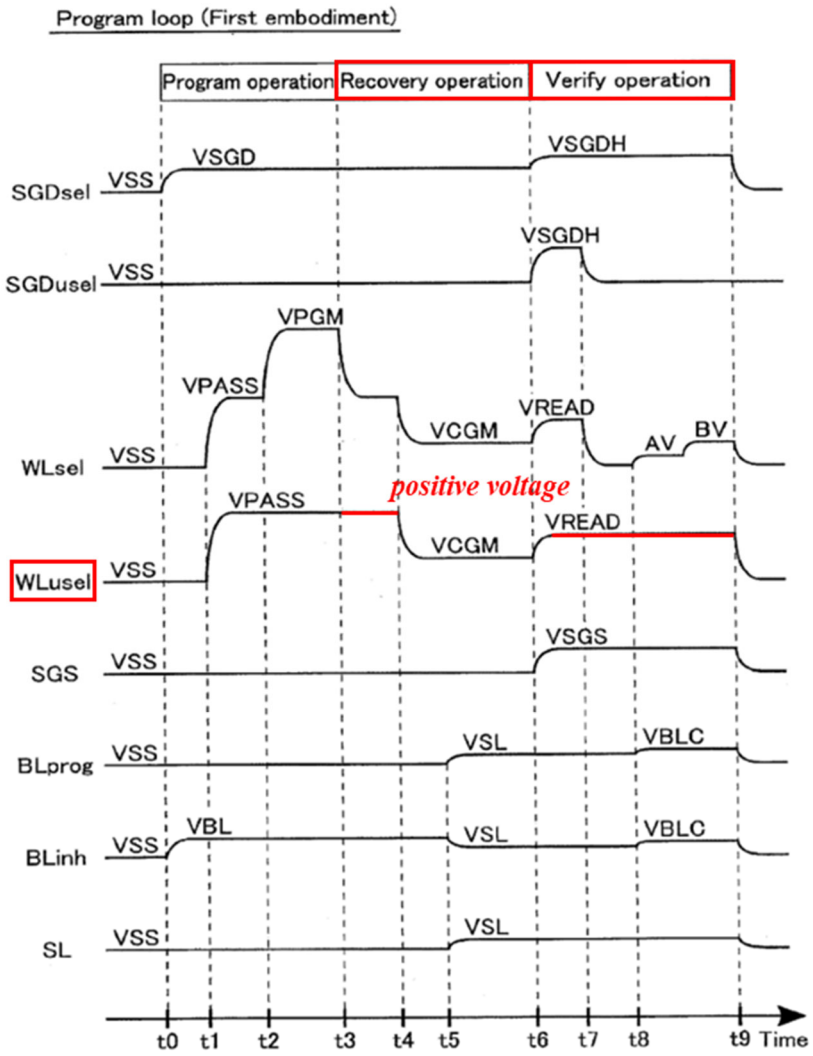
231. As explained in Ground 1, "a positive voltage" also need not have only one voltage level. *See* §IX.B.5.[5.C]. Relatedly, a *positive voltage* and a *bias voltage* need not be distinct voltages. *Id.*

232. The second adjacent memory cell, e.g., MT3, is the cell immediately below the selected cell, e.g., MT4. *Supra* §IX.C.1.[1.A.i]. Thus, any unselected memory cell below MT3 and above the bottom select transistor ST2, e.g., MT2 through MT0, can be used to satisfy this limitation:



Ex. 1007, Fig. 2.

233. Accordingly, Suzuki discloses *apply[ing] a positive voltage* (VPASS and VREAD) *on … any memory cells that are positioned* (as depicted) *between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string* (the selected string) *in the pre-verify stage* (the recovery operation) *and the verify stage* (the verify operation):



Ex. 1007, Fig. 11.

6. Claim 6

[6.PRE] "The apparatus of claim 3, wherein the processing circuitry is further configured to:"

234. Suzuki discloses *processing circuitry further configured to* perform the limitations of claim 6. *Supra* §IX.C.1.[1.A].

[6.A] "apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;"

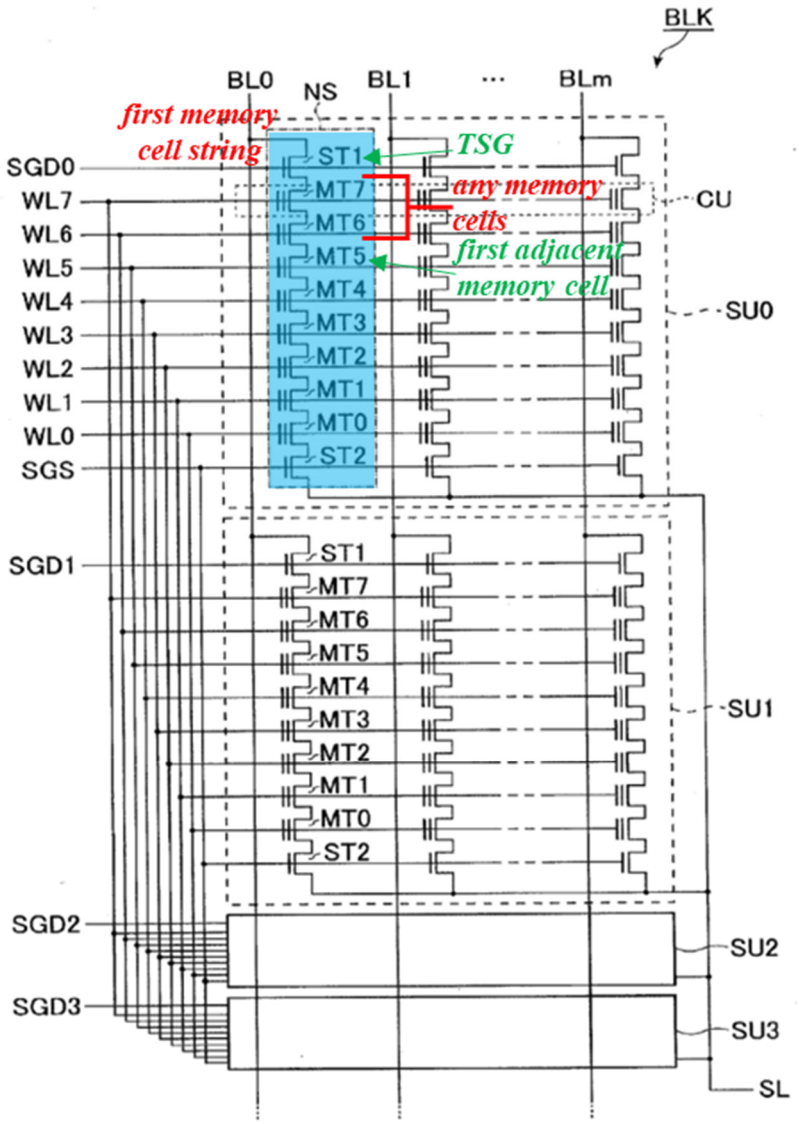
235. This limitation is identical to claim [5.A]. Suzuki discloses it for the same reasons. *Supra* §IX.C.5.[5.A].

[6.B] "apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and"

236. This limitation is identical to claim [5.B]. Suzuki discloses it for the same reasons. *Supra* §IX.C.5.[5.B].

[6.C] "apply a positive voltage on gate terminals of any memory cells that are positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage."

237. As explained in Ground 1, just as claim 3 is the mirror image of claim 2, this limitation is the mirror image of claim [5.C]. *Supra* §IX.B.6.[6.C]. The *any memory cells* may be *positioned* as shown:



Ex. 1007, Fig. 2.

238. Because Suzuki's positive voltage is applied on all unselected word lines, including those above and below the selected cell, Suzuki discloses *apply[ing] a positive voltage … in the pre-verify stage and the verify stage* for the same reasons explained with respect to claim [5.C]. *Supra* §IX.C.5.[5.C].

D. *Ground 3*: Claims 1-6 Are Obvious Over Costa in View of Seo

239. In my opinion, Costa and Seo are within the scope of the prior art and are highly relevant to the patentability of the '957 patent's claims.

240. In my opinion, Costa in view of Seo and the knowledge of a POSITA renders claims 1-6 obvious.

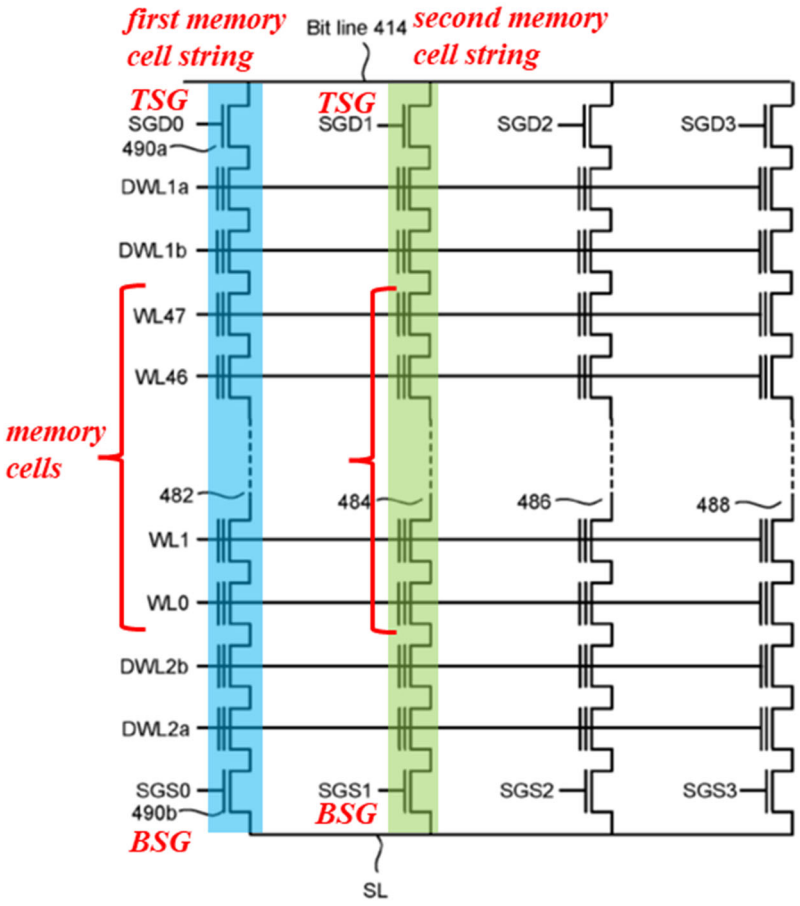
1. Claim 1

[1.PRE] "An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising:"

241. To the extent the preamble is limiting, Costa discloses it.

242. Costa discloses "[s]ensing in non-volatile memory." Ex. 1008, Abstract. "Sensing may be performed during reading [or] program verification…." *Id.*, [0093]; *see also id.*, Fig. 14, [0160]-[0168].

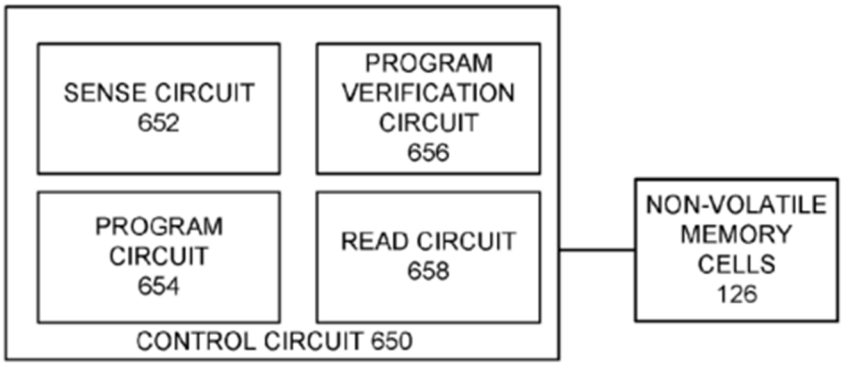
243. Costa's non-volatile memory, *an apparatus for reading a memory device* based on the disclosure above regarding sensing, includes a plurality of memory strings including *a first memory cell string and a second memory cell string* (both highlighted):



Ex. 1008, Fig. 4F. As shown above, each of the memory strings includes *a bottom-select-gate (BSG) transistor* (source select gate SGS0 or SGS1, at the bottom)*, memory cells* (at word lines WL0 to WL47)*, and a top-select-gate (TSG) transistor* (drain select gate SGD0 or SGD1, at the top) *that are connected in series*; *see also id.*, [0029] (memory cell strings), [0069] (source end at bottom of the stack), [0073] (SGD being the top layer), [0075] (memory cells connected in series), [0077] (select gates), [0161] (verification).

[1.A] "processing circuitry configured to:"

244. Costa's sense circuit and program verification circuit constitutes *processing circuitry* that can be configured to perform the claims of the '957 patent.



Ex. 1008, Fig. 15, [0169]-[0172], [0175]. These components, for example, "can be used to apply to and/or generate a variable read pass voltage for a subset of unselected word lines of a group based on the word line selected for sensing." *Id.*, [0169]. And the sense circuit "is configured to perform a sense process as part of reading or verifying for the memory cells." *Id.*, [0170]

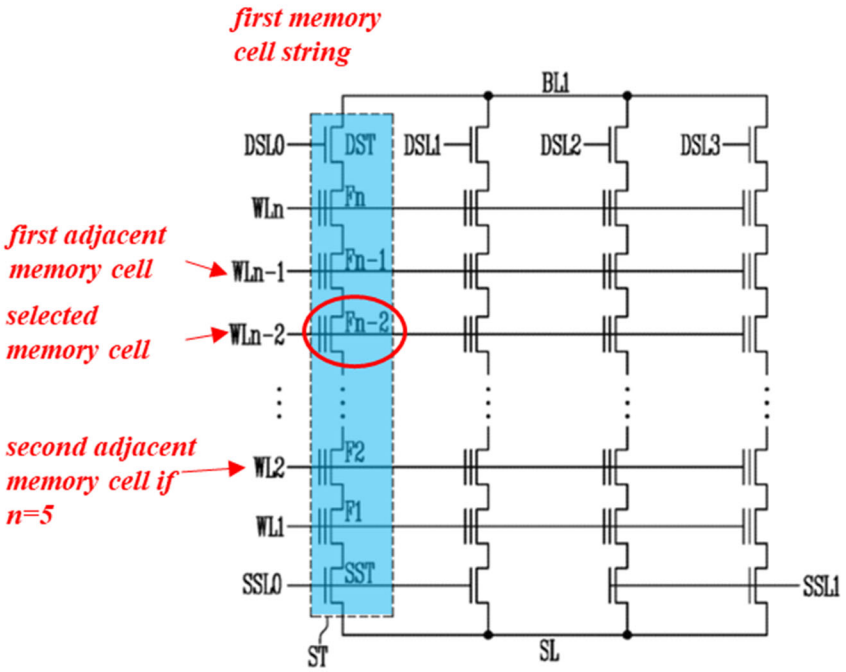
[1.A.i] "apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;"

245. Costa in view of Seo renders this limitation obvious.

246. I note here for clarity that 1.A.i and 1.A.iii both relate to the *selected memory cell* that is *programmed*.

247. Seo's method involves selecting a memory cell for reading by selecting a memory page and a memory string. Ex. 1009, Fig. 7 (step S620), [0073]. The cell

at the intersection of the page and the string is selected. For example, a memory cell coupled to DSL0 and WLn-2 may be selected. *Id.*, [0074] (selecting the cell at DSL0 and WL3, using an exemplary string length n=5):



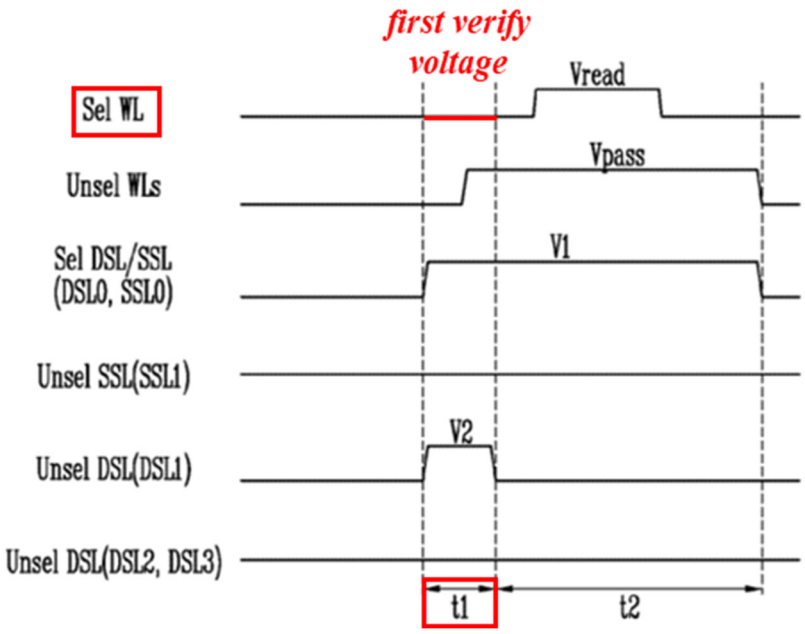
Id., Fig. 4. As shown, the *selected memory cell* (at WLn-2) belongs to *the first memory cell string* (comprising DSL0) and *[is] arranged between a first adjacent memory cell* (at WLn-1) *and a second adjacent memory cell* (at WLn-3, or WL2 if n=5).

248. Costa discloses using its read operations to verify programming. *See* §VI.B; Ex. 1008, Fig. 8, [0093]-[0094] ("Sensing may be performed during reading [or] program verification…."). Moreover, the same selected cell is programmed and then verified. *Supra* §VI.B; Ex. 1008, Fig. 6; *see also id.*, [0086]-[0087]; §IX.B.7

(program-read (verify) loop). Again, the read (verify) occurs after the program operation to verify whether the program operation was successful. *See* Ex. 1008, [0086] ("For example, if none of the memory cells being programmed according to FIG. [7] have reached Vv2, there is no reason to verify at Vv7."). Accordingly, when the *selected memory cell* is being verified, it is *programmed*.

249. Seo discloses *apply[ing], in a pre-verify stage* (a first time period t1 preceding a read/verify period t2)*, a first verify voltage* (a low voltage[4]) *on ... a selected memory cell*:

[4] In the context of the '957 patent, even applying zero volts is applying a voltage, which is *bias voltage* or *verify voltage*. Ex. 1001, 10:57-61 ("an initial voltage, such as zero volt, can be applied on the selected TSG layer, the unselected TSG layer, the WLs (>n+1), the WLn+1, the WLn, the WLs (<n−1), and the BSG layer."), 11:19-23 ("The bias voltage (or gate voltage) applied on the unselected TSG layer of the unselected memory cell string can be reduced to a lower voltage, such as zero volt to turn off the TSG transistor (e.g., 306B) of the unselected memory cell string."), 11:35-39 ("the bias voltage (or verify voltage) applied on the selected word line layer WLn can be reduced to a programming verify (PV) level. In some embodiments, the PV level can be in a range from zero volt to one volt.").



Ex. 1009, Fig. 8; *see also id.*, [0090] (stating that Vread is applied to Sel WL "[s]ubsequently," during period t2).

250. Using Figure 12H as an illustrated embodiment of Costa's memory device, this *first verify voltage* would be applied to the *selected memory cell* coupled to WL28, with *a first and a second adjacent memory cell* at WL29 and WL27, respectively:

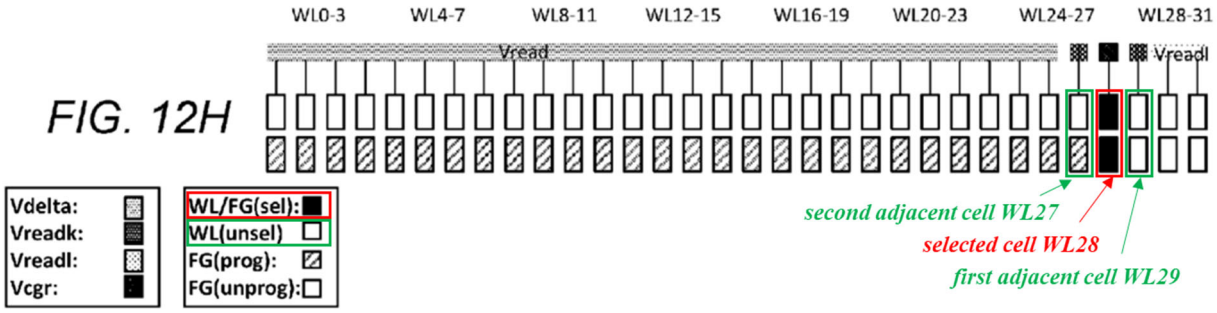


FIG. 12H

Ex. 1008, Fig. 12H, [0138]-[0139] (describing generally Figures 12A-12H, which depict the same memory string but with the selected memory cell at different

locations); *id.*, [0140]-[0143] (identifying drain side toward WL31 and source side toward WL0).

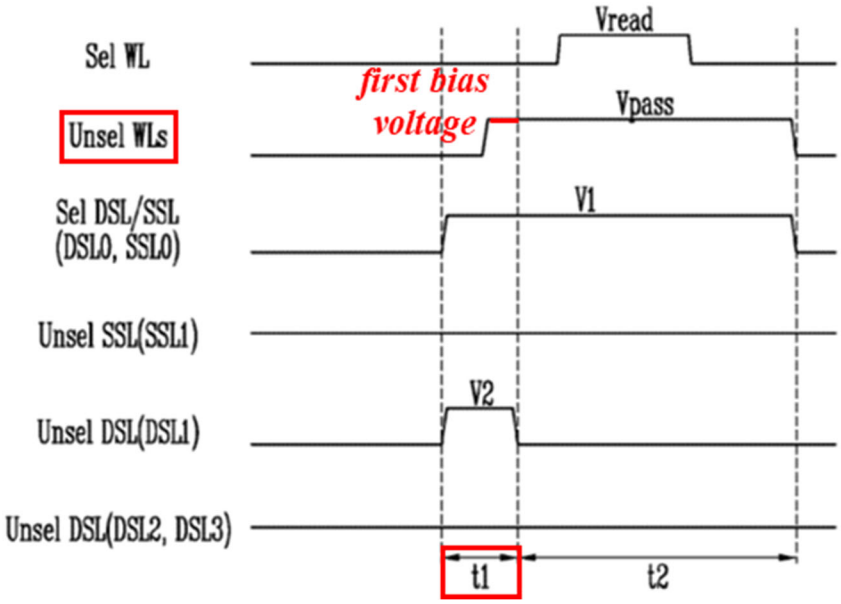
251. I note that Costa Figure 10 and associated descriptions disclose the same concept in a tabular form. Ex. 1008, Fig. 10, [0117]-[0134]. In both Figure 10 and Figures 12A-12H, a memory string is divided into seven zones. *Id.*, [0119], [0147]. Figure 12H corresponds to the rightmost Zone 7 column of Figure 10 because WL28 is located in Zone 7. *Id.*, [0147]. A comparison of that column against Figure 12 confirms that the same voltages are applied to the respective word lines in both. The table in Figure 10 additionally shows the voltages on the bit line, the source line, and on SGD and SGS of the selected memory string. A POSITA would have understood that those voltages are applicable to the embodiments of Figures 12A-12H.

[1.A.ii] "apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;"

252. Costa in view of Seo renders this limitation obvious.

253. I note here again for clarity that 1.A.ii and 1.A.iv both relate to the *not programmed memory cell*. This corresponds to a different word line that does not couple to the *selected memory cell*. But the claim requires that this different word line couple to a memory cell that is specifically *not programmed*.

254. Seo discloses applying a "pass voltage Vpass … to unselected word lines" during a first time period t1. Ex. 1009, [0088]-[0089].

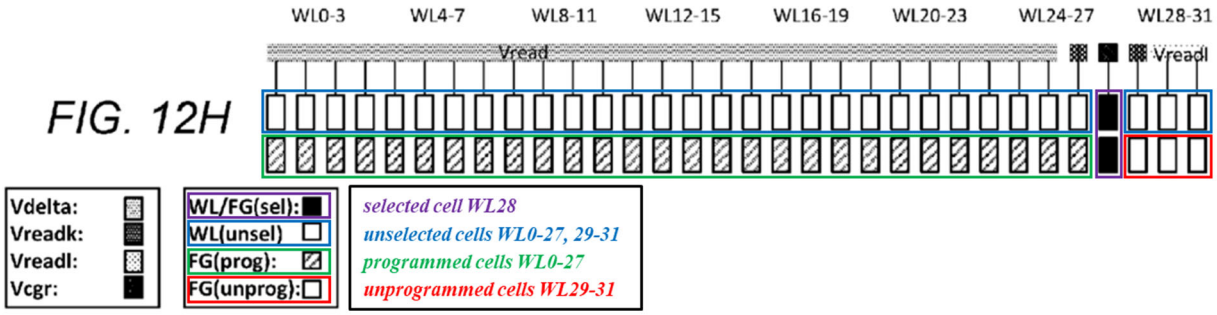


Id., Fig. 8. As shown, Vpass is applied sometime during the first time period t1. *See id.*, [0089] ("[s]ubsequently, the pass voltage Vpass may be applied …."). But as explained in the claim construction section above, the plain and ordinary meaning of the claim in light of the '957 patent specification does not require the voltage to be applied for the entire duration of the relevant stage. Thus, Seo discloses *apply[ing], in the pre-verify stage* (the first time period t1)*, a first bias voltage* (Vpass) *on … at least one memory cell* (via the Unsel WLs) *of the first memory cell string* (the string where the selected memory cell is located).

255. Costa discloses that this *at least one memory cell … is not programmed*. Costa teaches that memory cell strings are typically "programmed in a program order

tha[t] begins at one end … and ends at the other end ….” Ex. 1008, [0029]; *see also id.*, [0100] (stating that programming of memory cell strings “generally occurs in a programming order that begins at one end of each NAND string and proceeds to the other end”). Accordingly, unprogrammed cells are typically positioned between the selected word line and a select line. *Id.*, [0033]. For example, unprogrammed cells are located between the selected memory cell and SGD when programming proceeds from the source end to the drain end. Accordingly, in the following illustration, the unprogrammed cells are at WL29-31, above (toward SGD on the drain side of) the selected cell at WL28:

FIG. 12H



Id., Fig. 12H, [0147]; *see also id.*, [0109] (an analogous embodiment on a longer, 128-cell memory string). Here, as indicated by the legend, the blank rectangles in the top row indicate unselected word lines, and the blank rectangles in the bottom row indicate unprogrammed cells. *Id.*, [0139].

256. Seo’s first bias voltage Vpass is applied on all unselected word lines during the pre-verify stage. *See* Ex. 1009, Fig. 8. Applying that voltage on Costa’s

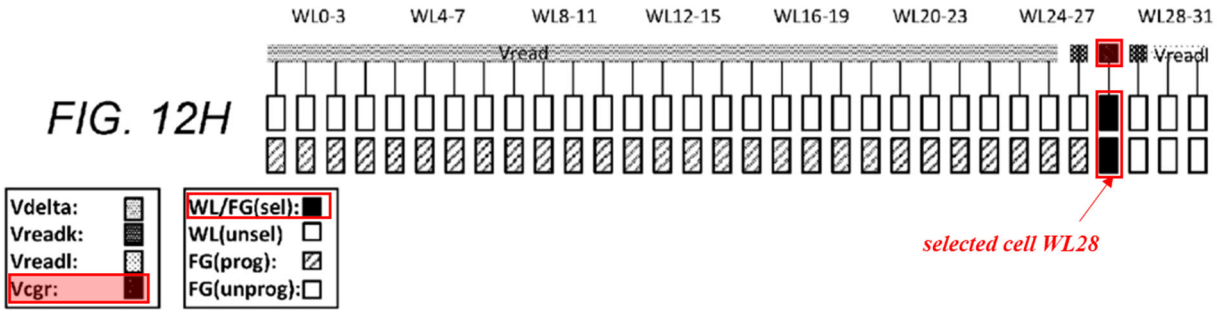
memory device, Vpass is applied on unprogrammed memory cells, including those at WL29-31 in this illustrated scenario.

[1.A.iii] "apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and"

257. Costa discloses this limitation.

258. This limitation refers to the same memory cell in claim [1.A.i], e.g., at WL28 of Costa's exemplary memory string. *See* §IX.D.1.[1.A.i].

FIG. 12H



Ex. 1008, Fig. 12H. "WL28 … is selected for verification and receives Vcgr." *Id.*, [0147]. "The waveform of Vcgr … may be considered a read pulse or a read reference voltage which is used during a sense operation." *Id.*, [0098]. Vcgr is an "example of a reference signal" and can take on one of various verify target levels for verify operations. *Id.*, [0094]. "For example, Vcgr may be set to … Vv1, Vv2, Vv3, etc. to sense at various verify levels for target states during programming." *Id.*, [0098]. Vcgr is applied to the selected word line during the sensing phase of operation. *Id.*, [0166] (step 712 of the Figure 14 flowchart, which describes a sensing process).

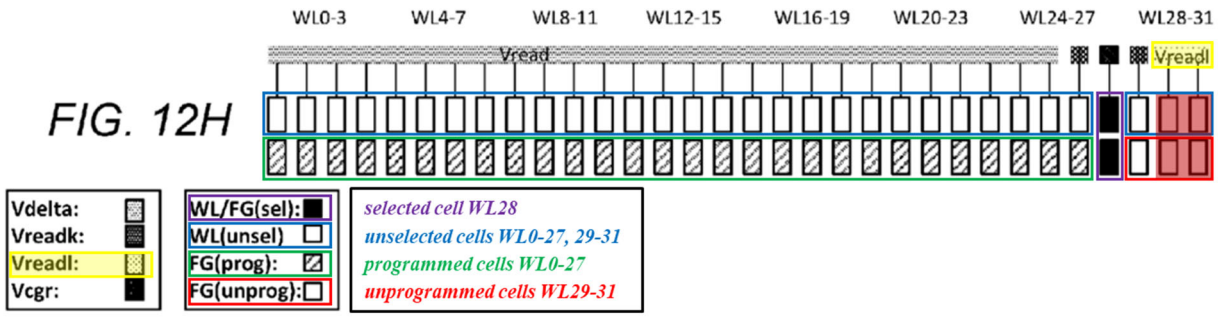
259. Accordingly, Costa discloses *apply[ing], in a verify stage* (sensing phase)*, a second verify voltage* (Vcgr) *on … the selected memory cell* (at WL28) *of the first memory cell string* (the string where the selected memory cell is located).

[1.A.iv] "apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage."

260. Costa in view of Seo renders this limitation obvious.

261. This limitation refers to the same memory cell in claim [1.A.ii] during the subsequent verify stage (the unselected, unprogrammed memory cell). *Supra* §IX.D.1.[1.A.ii]. Specifically, that memory cell can be WL30 or WL31 (within the range of WL29 to WL31). Costa further discloses applying *a second bias voltage* (VreadL) on these unselected word lines *in the verify stage* (sensing phase):

FIG. 12H



Ex. 1008, Fig. 12H, [0147] ("unselected word lines WL30-WL31 receive the low read pass voltage Vreadl"). "VreadL is a lowest read pass voltage used in one example. For example, VreadL may be several millivolts less (e.g., 5.2V) than the standard read pass voltage Vread." *Id.*, [0122]. "VreadL may be used [on WL30 and WL31] because the word lines on the drain side have not undergone

programming, and thus the corresponding memory cells should be in the erased state" and have a low threshold voltage. *Id.* Thus, a low read pass voltage VreadL can still ensure that these unprogrammed cells are turned on.

262. A POSITA would have found it obvious that Seo's *first bias voltage* is not any lower than the standard read pass voltage because the same voltage level is applied to all unselected memory cells, including those already programmed. Ex. 1009, Fig. 8. Thus, to ensure that all memory cells to which the *first bias voltage* is applied are turned on by the voltage, the voltage level must be high enough to turn on memory cells programmed to a data state with the highest threshold voltage (plus some margin). And as I explain below in the section on motivation to combine, Seo turns on all unselected memory cells in the pre-verify stage to pre-condition the channel voltage of these cells, which reduces HCI effects. By applying a single high Vpass voltage level on all unselected gates, Seo's method minimizes the voltage gradient through the channels of memory strings because all unselected cells are subject to the same gate voltage. And as I further explain in that section, Costa seeks to reduce channel resistance issues without introducing read disturb from an unnecessarily high read pass voltage on the unselected cells. This includes applying a low read pass voltage (VreadL) during the verify stage to unprogrammed cells. Thus, a POSITA would not have a reason to lower Seo's standard read pass voltage during pre-verify, or at least would have found it obvious that Seo's standard read

pass voltage should be used in the combination during pre-verify. Accordingly, *the second bias voltage* (VreadL) *is smaller than the first bias voltage* (standard pass voltage Vpass).

2. Claim 2

[2] "The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string."

263. Costa in view of Seo renders this limitation obvious.

264. Claim 2 refers to the *not programmed* memory cell of claim [1.A.ii] and [1.A.iv] (i.e., unselected and unprogrammed memory cell). That memory cell can be a cell positioned above the selected cell (i.e., can be the first adjacent memory cell). *Supra* §§IX.D.1.[1.A.ii], XI.A.6. More specifically, claim 2 requires the cell be positioned above the first adjacent memory cell. That memory cell can be a cell (at WL30 or WL31) *positioned between the first adjacent memory cell* (at WL29) *... and the TSG transistor* (SGD0) *of the first memory cell string* (the string where the selected memory cell is located). *Supra* §§IX.D.1.[1.A.i], X.A.4, X.A.6.

3. Claim 3

[3] "The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string."

265. Costa in view of Seo renders this limitation obvious.

266. As I explained above in Ground 1, whereas claim 2 requires an unprogrammed memory cell positioned *above* the first adjacent memory cell (which is immediately *above* the selected cell), claim 3 requires an unprogrammed memory cell positioned *below* the second adjacent memory cell (which is immediately *below* the selected cell). *Supra* §IX.C. Costa discloses that programming may proceed from the source end to the drain end, or vice versa. Ex. 1008, [0100] ("begin[ning] at one end of each NAND string and proceed[ing] to the other end," e.g., either from the source end to the drain end or in the reverse direction); *id.*, [0165] (same). I have described claims 1 and 2 above using an illustration wherein the drain side (e.g., WL29 through WL31) are the last cells to be programmed. When the programming order proceeds from the drain end to the source end, an unprogrammed memory cell *positioned between the second adjacent memory cell and the BSG transistor* exists. For example, if the selected cell just programmed is at WL28, cells at WL0 through WL27 are unprogrammed. In this scenario, the first bias voltage (Seo's Vpass) is applied to any of the cells at WL0 through WL27 because it is applied to all unselected cells. *Supra* §IX.D.1.[1.A.ii]. Costa explains that the lower read pass voltage VreadL is used on cells that "have not undergone programming … while still ensuring that these memory cells operate as pass gates" because they are in the erased state and have low threshold voltages. Ex. 1008, [0122]. Thus, the second

bias voltage (Costa's VreadL) is also applied on any of these cells because it is an unprogrammed, nonadjacent cell.

4. Claim 4

[4.PRE] "The apparatus of claim 1, wherein the processing circuitry is further configured to:"

267. Costa discloses *processing circuitry further configured to* perform the limitations of claim 4 as explained with respect to claim [1.A]. *Supra* §IX.D.1.[1.A].

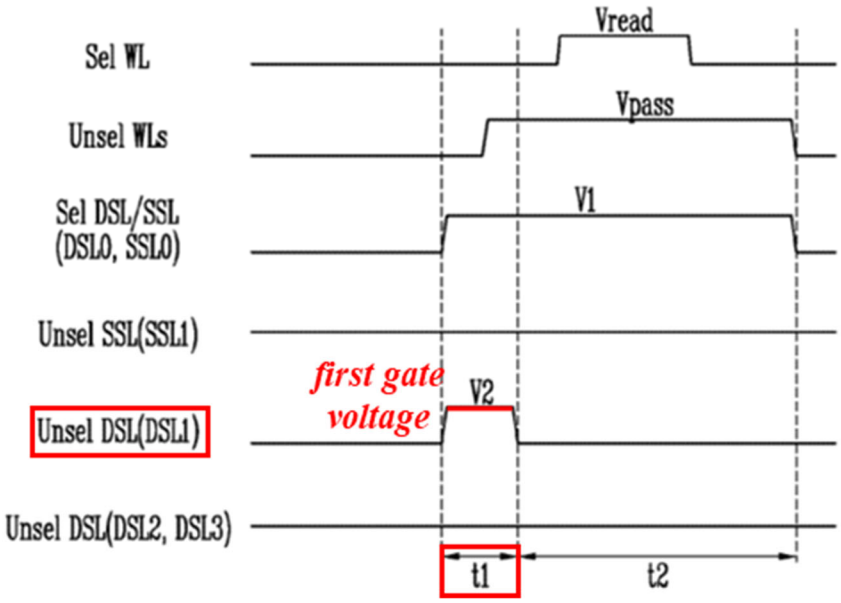
[4.A] "in the pre-verify stage,"

268. The pre-verify stage corresponds to Seo's first time period t1. *Supra* §§IX.D.1.[1.A.i]-[1.A.iv].

[4.A.i] "apply a first gate voltage on a gate terminal of the TSG transistor of the second memory cell string,"

269. Costa in view of Seo renders this limitation obvious.

270. *The second memory cell string* is an unselected memory string since the selected memory cell belongs to the first memory cell string. Ex. 1001, 17:42-43 (claim [1.A.i]). In other words, claim 1 operates on the first memory string, which includes the selected memory cell. Thus, in this context, the second memory string is not selected. Seo discloses *apply[ing] a first gate voltage* (V2) *on … the TSG transistor of the second memory cell string* (Unsel DSL):



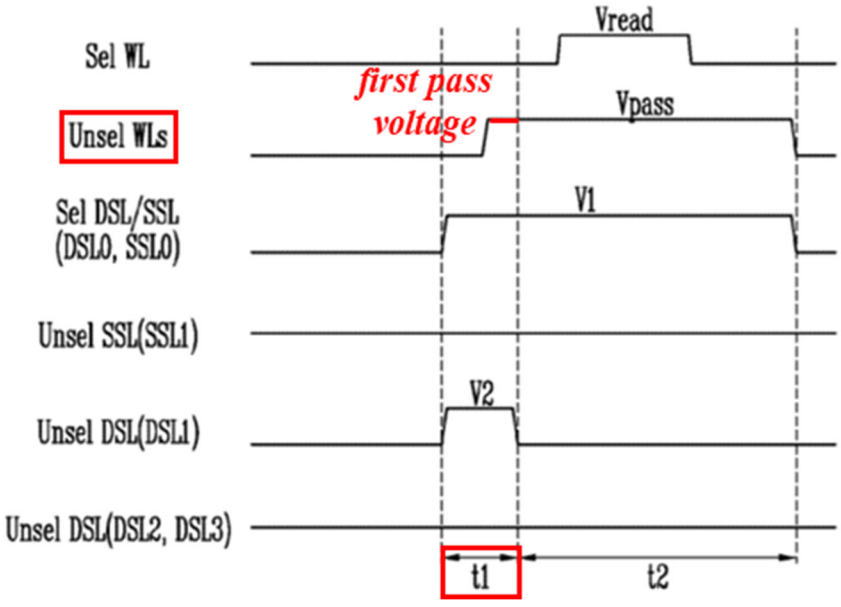
Ex. 1009, Fig. 8; *id.*, [0088] ("a second voltage V2 may be applied to the second drain select line DSL1 corresponding to the unselected memory string which shares the first source select line SSL0 with the selected memory string during a first time period t1"). Voltage V2 turns on the drain select transistor. *Id.* ("the second voltage V2 may have the same potential level as the first voltage V1. Accordingly, the source select transistor SST and the drain select transistor DST included in the unselected memory string which shares the first source select line SSL0 with the selected memory string may be turned on."). This voltage can be applied to Costa's unselected drain select line SGD1 because it serves the same function as Seo's drain select line DSL1.

[4.A.ii] "apply a first pass voltage on a gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and"

271. Costa in view of Seo renders this limitation obvious.

272. As I explained in Ground 1, the '957 patent does not require the first bias voltage of claim 1 and the first pass voltage of claim 4 to have different values, or even that they be distinct voltages. *Supra* §IX.B.4.[4.A.ii].

273. The first bias voltage may be applied to at least one unprogrammed memory cell, e.g., at WL30 or WL31 of Costa's memory device. *Supra* §IX.D.1.[1.A.ii]. The *first pass voltage* (Vpass) may be applied to *the first adjacent memory cell* (e.g., WL29) *in the pre-verify stage* (the first time period t1):



Ex. 1009, Fig. 8. Vpass is applied to all unselected word lines, including WL29. Although Vpass is also applied as the first bias voltage of claim 1, the '957 patent

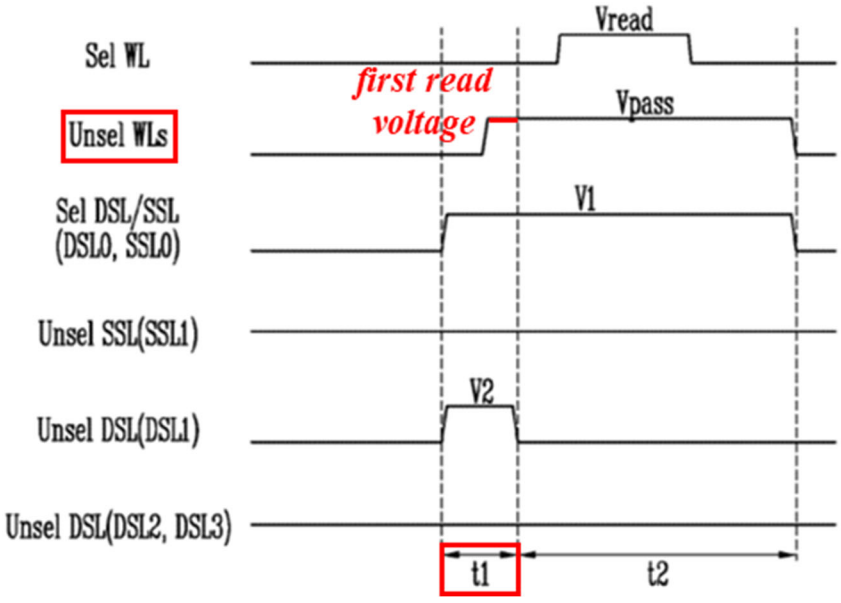
does not require the first pass voltage and the first bias voltage to be distinct or have different values.

[4.A.iii] "apply a first read voltage on a gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string; and"

274. Costa in view of Seo renders this limitation obvious.

275. As I explained in Ground 1, the '957 patent does not require the first bias voltage of claim 1 and the first read voltage of claim 4 to have different values, or even that they be distinct voltages. *Supra* §IX.B.4.[4.A.iii].

276. As I also explained above, Seo discloses applying the same Vpass voltage to unselected word lines in its *pre-verify stage* (the first time period t1). *Supra* §IX.D.4.[4.A.ii]. Applied to Costa's Figure 12H embodiment, this Vpass voltage also constitutes the *first read voltage* (Vpass) *on ... the second adjacent memory cell* (at WL27) *... in the first memory cell string* (the string where the selected memory cell is located).



Ex. 1009, Fig. 8. Although Vpass is also applied as the first bias voltage of claim 1, the '957 patent does not require the first read voltage and the first bias voltage to be distinct or have different values.

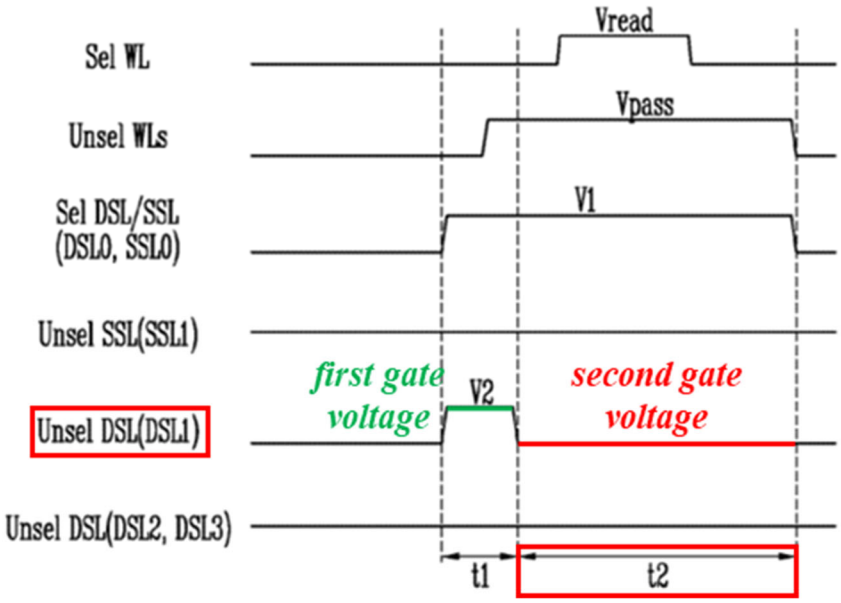
[4.B] "in the verify stage,"

277. The verify stage corresponds to Seo's second time period t2 and Costa's verify operation. *Supra* §§IX.D.1.[1.A.iii]-[1.A.iv].

[4.B.i] "apply a second gate voltage on the gate terminal of the TSG transistor of the second memory cell string,"

278. Costa in view of Seo renders this limitation obvious.

279. This limitation refers to the same transistor in claim [4.A.i] but during the subsequent verify stage. *Supra* §IX.D.4.[4.A.i]. The *second gate voltage appl[ied] on … the TSG transistor of the second memory cell string* is shown below:



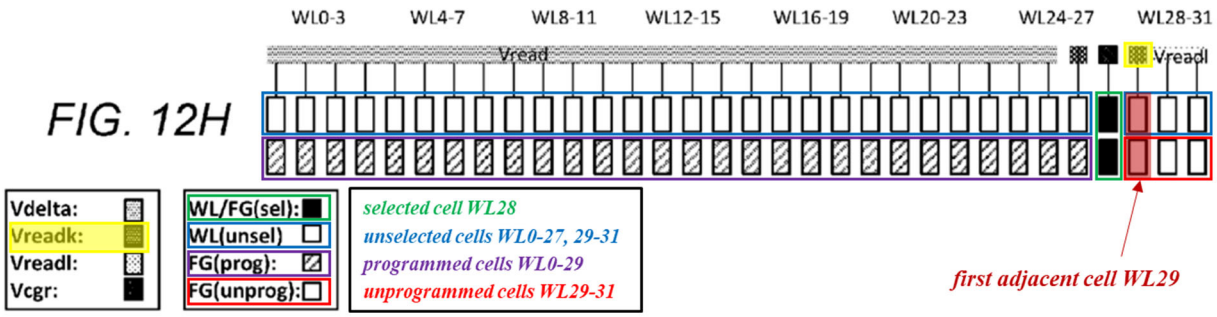
Ex. 1009, Fig. 8. Unlike the first gate voltage V2, which turns on the drain select transistor DST, this voltage turns off the drain select transistor DST. *See id.*, [0088] (disclosing that V2 turns on DST). Even without Seo's disclosure, a POSITA would have recognized that the drain select transistor of an unselected memory string such as *the second memory cell string* must be turned off during the verify stage. During the verify stage, the current through the selected memory string is sensed to determine the state of the selected cell. *Supra* §VI.B. This current is sensed through the bit line. Thus, all other memory strings coupled to the same bit line must be isolated from the bit line by turning off their drain select transistors, otherwise the unselected strings may change the current level on the bit line and make the determination unreliable. Seo's disclosure merely confirms this necessary operating condition that would have been well known to a POSITA. *See also* Ex. 1008, Fig.

4F (showing all memory strings coupled to the same bit line); Ex. 1009, Fig. 4 (same).

[4.B.ii] "apply a second pass voltage on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and"

280. Costa discloses this limitation.

281. This limitation refers to the same transistor in claim [4.A.ii] during the subsequent verify stage. In the combination, that transistor can be, for example, at WL29 in Costa's exemplary embodiment. *Supra* §IX.D.4.[4.A.ii]. Costa discloses *apply[ing] a second pass voltage* (Vreadk) *on … the first adjacent memory cell* (at WL29) *… in the first memory cell string*:



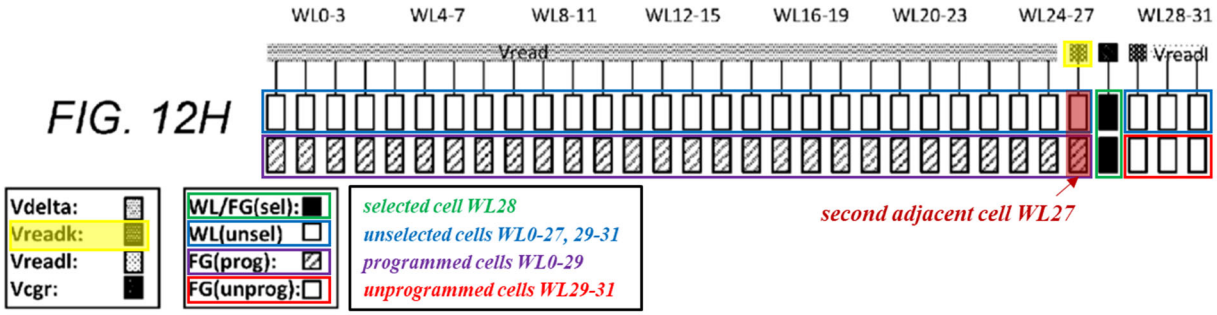
Ex. 1008, Fig. 12H, [0147] ("The adjacent unselected word lines WL27 and WL29 receive Vreadk"), [0165] ("Steps 708 and 710 may also include determining other drain and source side pass voltages, such as a larger read pass voltage Vreadk that is applied to word lines adjacent to the selected word line."). "Vreadk is a highest read pass voltage." *Id.*, [0121]. "The higher read pass voltage Vreadk may be used to guarantee that the channel regions around the selected word line WLn remain

conductive during sensing. Because the selected word line is biased with the low level Vcgr for verification, the higher level of Vreadk can compensate for any reduced channel conductance of the memory cell at WLn+1 due to the lower voltage at word line WLn." *Id.* The high voltage "can compensate for any reduced channel conductance under memory cells at WLn+1 and WLn−1 due to the lower voltage at word line WLn." *Id.*, [0123].

[4.B.iii] "apply a second read voltage on the gate terminal of the second adjacent memory cell of the selected memory cell of the first memory cell string, wherein"

282. Costa discloses this limitation.

283. This limitation refers to the same transistor as in claim [4.A.iii] during the subsequent verify stage. In the combination, that transistor can be, for example, at WL27 in Costa's exemplary embodiment. *Supra* §IX.D.4.[4.A.iii]. Costa discloses *apply[ing] a second read voltage* (Vreadk) *on … the second adjacent memory cell* (at WL27) *… of the first memory cell string*:



Ex. 1008, Fig. 12H, [0147], [0165], [0121].

[4.C] "at least one of the second pass voltage and the second read voltage is larger than the second gate voltage."

284. Costa discloses this limitation.

285. As I explained above, both the second pass voltage and the second read voltage are Costa's Vreadk. *Supra* §§IX.D.4.[4.B.ii]-[4.B.iii]. "Vreadk is a highest read pass voltage … [and] may be [hundreds of] millivolts higher … than a standard read pass voltage Vread." Ex. 1008, [0121]. Read pass voltages are sufficiently high such that the memory cells to which they apply are turned on and conduct current. *Id.*, [0096] ("During a read or verify process, the unselected memory cells and dummy word lines are provided with one or more read pass voltages at their control gates so that these memory cells will operate as pass gates (e.g., conducting current regardless of whether they are programmed or erased)."). The second gate voltage is Seo's voltage to turn off the DST. *Supra* §IX.D.4.[4.B.i]. This voltage may be the ground voltage Vss. Ex. 1009, [0075]. A read pass voltage that turns on memory cells regardless of their data state is higher than a voltage, e.g., Vss, that is low enough to turn off the drain select transistor because the former is higher than the highest threshold voltage and the latter is lower than the threshold voltage of a transistor that is not subject to programming. Thus, *the second pass voltage and the second read voltage* (Vreadk) *[are] larger than the second gate voltage* (e.g., Vss).

5. Claim 5

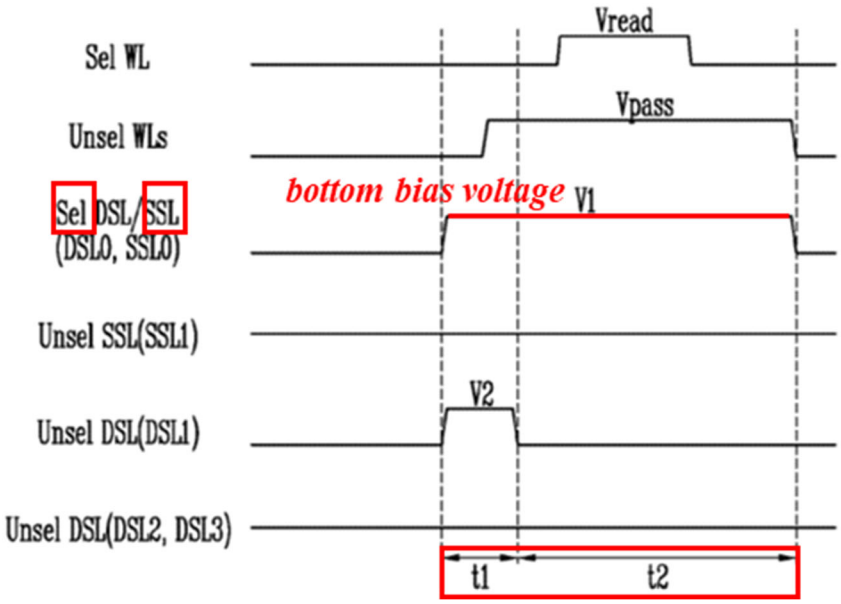
[5.PRE] "The apparatus of claim 2, wherein the processing circuitry is further configured to:"

286. Costa discloses *processing circuitry further configured to* perform the limitations of claim 5 for the same reason discussed with respect to claim 4. *See* §IX.D.4.[4.PRE].

[5.A] "apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;"

287. Costa in view of Seo renders this limitation obvious.

288. Seo discloses *apply[ing] a bottom bias voltage* (V1) *on … the BSG transistor of the first memory cell string* (Sel SSL, e.g., SSL0) *in the pre-verify stage* (the first time period t1) *and the verify stage* (the second time period t2):



Ex. 1009, Fig. 8, [0088] ("a first voltage V1 may be applied to the first drain select line DSL0 and the first source select line SSL0 corresponding to a selected memory

string ST."). "[V]oltage V1 may be a voltage to turn on … the source select transistor SST." *Id.*, [0088].

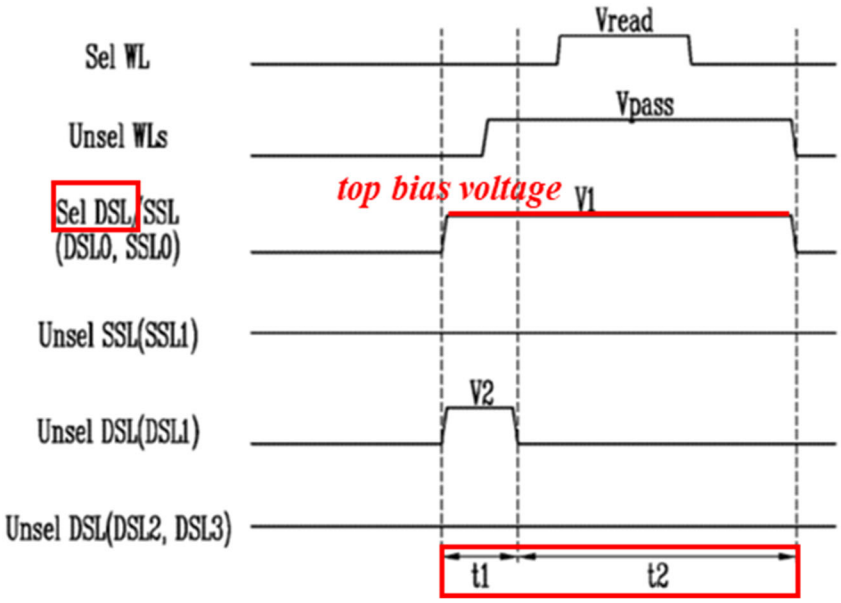
289. Costa discloses that, during *the verify stage* (the sensing phase), "[t]he source select line … [is] set to VSG [*the bottom bias voltage*] to turn on source select gate [*the BSG transistor*] …." Ex. 1008, [0097].

290. Seo's V1 and Costa's VSG have the same function and need to be high enough to turn on the source select transistor. The two may have the same voltage level or may have similar voltage levels. In any event, Costa's VSG may be used in both stages in the combination.

[5.B] "apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and"

291. Costa in view of Seo renders this limitation obvious.

292. Seo discloses *apply[ing] a top bias voltage* (V1) *on … the TSG transistor of the first memory cell string* (Sel DSL, e.g., DSL0) *in the pre-verify stage* (the first time period t1) *and the verify stage* (the second time period t2):



Ex. 1009, Fig. 8, [0088] ("a first voltage V1 may be applied to the first drain select line DSL0 and the first source select line SSL0 corresponding to a selected memory string ST."). "[V]oltage V1 may be a voltage to turn on the drain select transistor DST…." *Id.*, [0088].

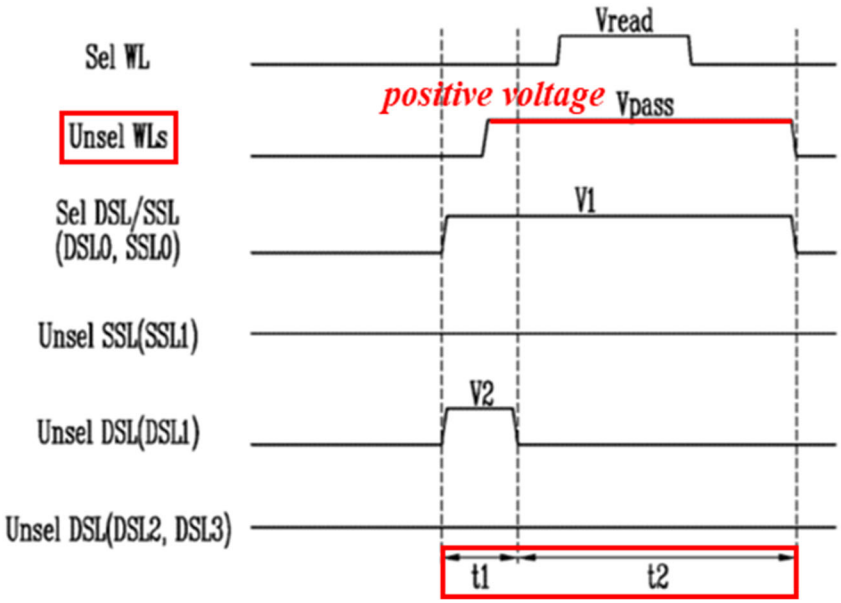
293. Costa discloses that, during *the verify stage* (the sensing phase), the "drain select line … [is] set to VSG [*the top bias voltage*] to turn on … drain select gate [*the TSG transistor*] …." Ex. 1008, [0097].

294. Seo's V1 and Costa's VSG have the same function and need to be high enough to turn on the drain select transistor. The two may have the same voltage level or may have similar voltage levels. In any event, Costa's VSG may be used in both stages in the combination.

[5.C] "apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage."

295. Costa in view of Seo renders this limitation obvious.

296. Seo discloses *apply[ing] a positive voltage* (Vpass) *on ... any* unselected *memory cells*—including those *that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor—of the first memory cell string in the pre-verify stage* (the first time period t1) *and the verify stage* (the second time period t2):



Ex. 1009, Fig. 8, [0088]. Vpass is a voltage that turns on the unselected memory cells regardless of the data states or threshold voltages of the cells. *Supra* §VI.B.

297. Costa also discloses *apply[ing] a positive voltage* (standard read pass voltage Vread, (Ex. 1008, [0121]-[0128])) *on ... any memory cells* (WL0-WL26)

that are positioned between the second adjacent memory cell (WL27) *... and the BSG transistor of the first memory cell string in ... the verify stage* (the sensing phase):

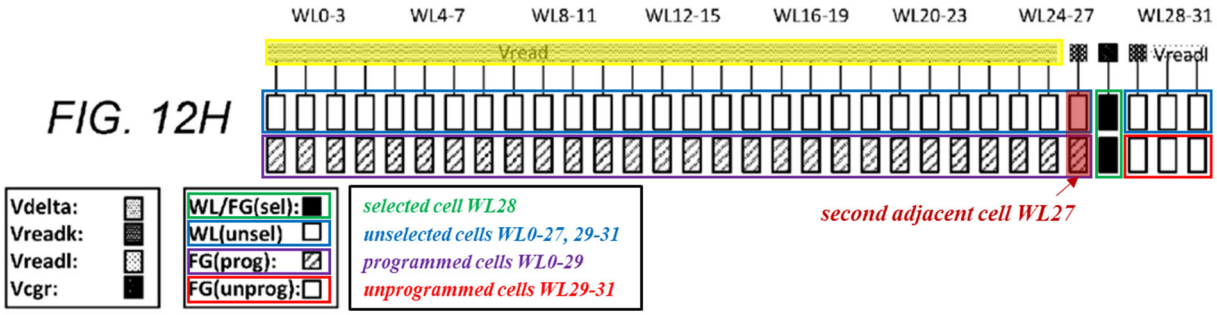


FIG. 12H

Ex. 1008, Fig. 12H, [0147] ("A subset of the unselected source side word lines including word lines WL0-WLWL26 receive the variable read pass voltage. For a selected word line in Zone 7, the variable read pass voltage for word lines WL0-WL26 is Vread.").

298. Because both Seo and Costa apply a nominal read pass voltage on the memory cells recited by this limitation, Costa's nominal read pass voltage may be used in both stages in the combination. More specifically, this nominal read pass voltage is high enough so that these memory cells will operate as pass gates regardless of the data state to which the cells are programmed.

6. Claim 6

[6.PRE] "The apparatus of claim 3, wherein the processing circuitry is further configured to:"

299. Costa discloses *processing circuitry further configured to* perform the limitations of claim 6 for the same reason discussed with respect to claim 4. *See* §IX.D.4.[4.PRE].

[6.A] "apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;"

300. This limitation is identical to claim [5.A]. Costa in view of Seo renders it obvious for the same reasons. *Supra* §IX.D.5.[5.A].

[6.B] "apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and"

301. This limitation is identical to claim [5.B]. Costa in view of Seo renders it obvious for the same reasons. *Supra* §IX.D.5.[5.B].

[6.C] "apply a positive voltage on gate terminals of any memory cells that are positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage."

302. Costa discloses or at least renders obvious this limitation. Specifically, as explained below, when programming proceeds from the drain end to the source end, a standard read pass voltage Vread (*a positive voltage*) is applied to memory cells *between the first adjacent memory cell of the selected memory cell and the TSG transistor*.

303. As I explained in Ground 1, just as claim 3 is the mirror image of claim 2, this limitation is the mirror image of the claim [5.C] limitation. *Supra* §IX.B.6.[6.C]. Specifically, claim 2 recites memory cells *above* (on the *drain* side of) the selected cell, while claim [5.C], which depends from claim 2, recites the remaining unselected memory cells, *i.e.*, those *below* (on the *source* side of) the selected cell. As I explained above, claims 2 and [5.C] are satisfied through a source-to-drain programming order. *Supra* §§IX.D.2.[2], X.E.4. Similarly, but in a mirror image, claim 3 recites memory cells *below* (on the *source* side of) the selected cell, while claim [6.C] recites the remaining unselected memory cells, *i.e.*, those *above* (on the *drain* side of) the selected cell. As I also explained above, Costa discloses source-to-drain as well as drain-to-source programming orders. *Supra* §IX.D.3.[3] (citing Ex. 1008, [0100], [0165]). Thus, Costa discloses, or at least renders obvious, this limitation by a drain-to-source programming order but otherwise for the same reason as it discloses claim [5.C]. More specifically, Costa explains that the increase in channel resistance changes direction with the programming order. Ex. 1008, [0101]. Thus, a POSITA would have understood the voltages applied to various word lines as illustrated in Figure 12H would be reversed in a mirror image to accomplish the same objective of addressing increasing channel resistance. *See id.*, [0115], [0119] (illustrating embodiments using a source-to-drain programming order).

7. Motivation to Combine

304. A POSITA would have been motivated to apply Seo's HCI-reduction technique to Costa's verify operation to precondition the channels of unselected strings during the pre-verify phase, and would have had a reasonable expectation of success, for several reasons.

305. Before I address Seo's HCI-reduction technique, I note that I address that Seo discloses a second gate voltage to turn off the TSG of an unselected memory string during the verify stage in limitation [4.B.i]. *Supra* §IX.D.4.[4.B.i]. As I explain there, even without Seo's disclosure, a POSITA would have recognized that to be a necessary, and certainly obvious, operating condition. *Id.* Thus, the second gate voltage would be obvious in Costa, and Seo's disclosure further supports this knowledge of a POSITA. Thus, here I focus on Seo's HCI-reduction technique.

306. Regarding the HCI techniques, initially, note that both Costa and Seo address issues in the field of 3D NAND flash memory. Ex. 1008, [0041]; Ex. 1009, [0004]-[0006]. Moreover, both references address reliability issues, including disturb issues, specifically related to read/verify operations. Ex. 1008, Abstract ("the effects of an increased channel resistance that occurs as more memory cells are programmed"); *id.*, [0122] ("the lower level of VreadL may cause less read disturb"); Ex. 1009, [0088]-[0089] ("a disturb phenomenon caused by Hot Carrier Injection (HCI)"). A POSITA considering the reliability issues in Costa would have

been motivated to consider references like Seo that also addresses a reliability issue, especially because read disturb is a concern of both. Furthermore, Costa is itself an addition to existing techniques that maintain a consistent and narrow distribution of threshold voltages. Ex. 1008, [0005], [0030]. Thus, a POSITA with knowledge of Costa would have been motivated to investigate other techniques in the same way that Costa was motivated to investigate additional techniques beyond what came before.

307. Costa and Seo focus on two different phenomena that impact the reliability of memory devices. Costa's techniques reduce the adverse impact on threshold voltages of cells in the selected string from increasing channel resistance as programming progresses through the string. Ex. 1008, Abstract, [0029], [0101]-[0104]. To do this while minimizing potential degradation due to read disturb, Costa seeks to reduce the voltage on unselected gate lines as much as possible based on the extent to which a memory string has been programmed. *See, e.g.*, *id.*, Figs. 10-11, [0122]. More specifically, because a potentially low Vcgr voltage is applied to the selected word line (e.g., at WL28), a low read pass voltage VreadL is applied to unprogrammed cells (e.g., at WL30 and WL31) beyond the adjacent cell (e.g., at WL29) to prevent a high voltage gradient across the adjacent cell. Ex. 1008, [0147] (applications of Vcgr and VreadL), [0120], Fig. 7E (showing Vcgr levels including low values). This also minimizes read disturb due to unintentionally programming

by a high read pass voltage on the unprogrammed cell. *Id.*, [0122]. As I explained with respect to claim [4.B.ii], "[t]he higher read pass voltage Vreadk may be used [at the adjacent cells] to guarantee that the channel regions around the selected word line WLn remain conductive during sensing" and thus needs to be high to "compensate for any reduced channel conductance under memory cells at WLn+1 and WLn−1 due to the lower voltage at word line WLn." Ex. 1008, [0123], *supra* §IX.D.4.[4.B.ii]. On the other hand, Seo's pre-verify stage reduces HCI-induced read disturb on unselected memory strings. Ex. 1009, [0008], [0089], [0127]; Ex. 1014, 254. Without the pre-verify stage, unselected memory strings would be subject to a high read pass voltage on all unselected word lines while isolated from the bit lines during the verify stage, a condition that would likely create read disturb due to HCI. To do this, Seo applies the same pass voltage on all unselected word lines in the pre-verify stage. *See* §IX.D.1.[1.A.ii]. The same pass voltage is applied to all unselected word lines such that all unselected cells are subject to the same gate voltage, to minimize voltage gradient across the channel, which in turn minimizes HCI that may occur from a high voltage gradient. Likewise, during the verify stage, Costa also applies the same pass voltage to all unselected word lines on either the drain side or source side beyond the adjacent memory cells. *See, e.g.*, Ex. 1008, Figs. 10, 12H. Importantly, Seo recognizes that this pre-verify stage is shorter than the verify stage. Ex. 1009, [0075]. This further enables a reduction in HCI (because

the pass voltage is applied only briefly, keeping its effect low) while guarding against adverse effects that are caused by long periods of high voltages on the unselected gate lines. This is also the reason that Costa uses a lower level of VreadL—to avoid unintentional programming by the read pass voltage on the unselected gate lines. A POSITA would have recognized that both Costa's and Seo's issues should be addressed to improve the reliability of flash devices. Thus, a POSITA would have considered Costa's techniques with other techniques, such as Seo's technique, for a more comprehensive improvement of memory reliability.

308. A POSITA also would have understood that in Seo's bias scheme, during the pre-conditioning of the channel voltage on the unselected string and the selected string in period t1, Seo is passing the bit line voltage (VBL) to the drain side of the selected transistor, with the word line of the selected transistor being set at 0V. However, that bit line voltage has an impact on the threshold voltage of adjacent transistors. Consider, for example, the transistor (memory cell) above the selected memory cell. As that transistor starts to turn on, the bit line voltage will cause the voltage on the source of that transistor to build. Here, the source of that transistor is not ground, because again, the selected word line is off. Threshold voltage is defined by the voltage on the gate relative to the source. In other words, as the source voltage increases on a transistor, the gate voltage must increase to turn on the transistor. Thus, a Vpass voltage on unselected memory cells on the drain

side of the selected memory cell needs to be high enough to account and compensate for this effect. Because of this, Seo simply applies a full Vpass voltage to the drain and the source side unselected memory cells to compensate for this effect.

309. Although the above discussion of Seo is more germane to a source-to-drain programming scheme, a POSITA would recognize that Seo would use the same full Vpass voltage on all unselected memory cells in a drain-to-source programming scheme. The reason is that Seo includes embodiments where the unselected strings are not conductive during the pre-verify period because, like Costa, Seo's device comprises memory strings on separate source select gates. In such a case, having the same voltage on the unselected word lines on both the drain and source sides of the selected memory cell would reduce the voltage gradient across the channel of the selected memory cell, and thus reduces HCI disturb on the selected memory cell. *See* Ex. 1019, Figs. 9A-9D. This assumes that Seo's Vpass voltage during pre-verify is not to too high to cause HCI injection from the selected memory cell to the adjacent unselected cell, which a POSITA would have found obvious because it is consistent with Seo's objective of reducing HCI. *See id.*, 5:3-21.

310. A POSITA would have understood that the second gate voltage on the TSG transistor of unselected memory strings to be necessary in Costa. *Supra* §IX.D.4.[4.B.i]. But to the extent that Seo is used to render that voltage obvious, a

POSITA would have recognized a need to set proper voltages during the verify stage on unselected memory strings (including TSG and BSG gate voltages), and a lack of disclosure of such voltages in Costa. A POSITA also would have recognized the need to isolate unselected memory strings from the bit line coupled to the selected string. A POSITA would have further recognized Seo to disclose a reasonable configuration to ensure such isolation. Thus, a POSITA would have been motivated to apply Seo's second gate voltage in a combination with Costa.

311. A POSITA would have had a reasonable expectation of success in combining Costa's and Seo's voltage schemes in both pre-verify and verify stages because they are mutually compatible extensions. For example, Seo's pre-verify voltages, which is used for HCI reduction, may be prepended to Costa's verify voltages because the pre-verify voltages are intended for pre-conditioning of channel voltages before a verify stage like Costa's, and the two sets of voltages are compatible as I explained with respect to the claims. *Supra* §§IX.D.1-IX.D.6. And as each of Costa and Seo deals with solving read issues but through nonoverlapping time periods, a POSITA would have expected their techniques to be conflict-free.

312. To view the combination from another perspective, Costa's position-dependent pass voltages on unselected cells simply extend a single Vpass voltage, which Seo already deploys, into multiple levels. In fact, Seo's application of a single Vpass voltage on all unselected lines is discussed in Costa as a basic bias condition:

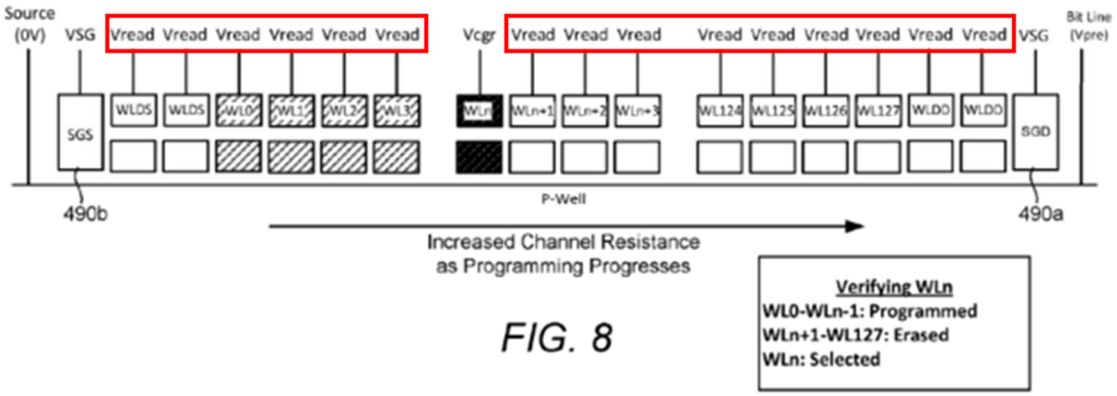
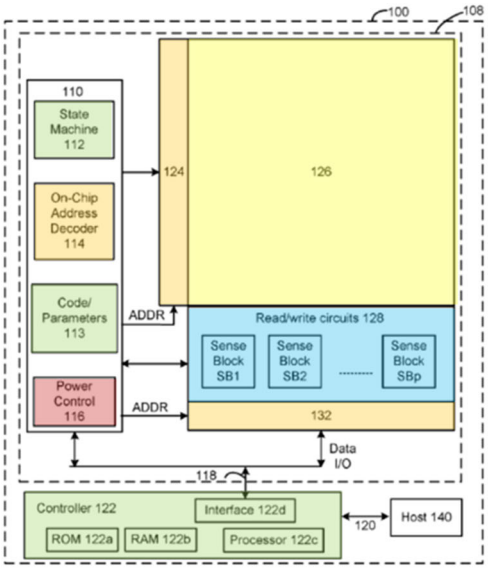


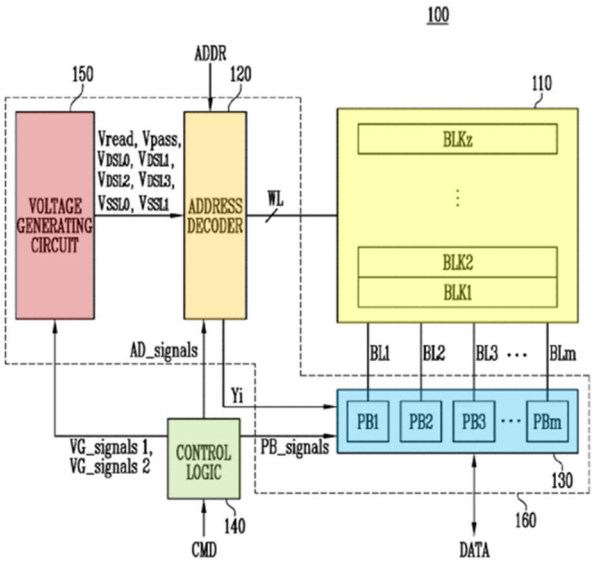
FIG. 8

Ex. 1008, Fig. 8 (showing pass voltage Vread on all unselected cells); *id.*, [0094]. Thus, Costa's techniques improve upon Seo's basic configuration, which Costa describes at length. *Id.*, [0096]-[0104].

313. Moreover, a POSITA also would have had a reasonable expectation of success combining the teachings of Costa and Seo because they disclose similar control circuitry, memory arrays, and read-operation processes.

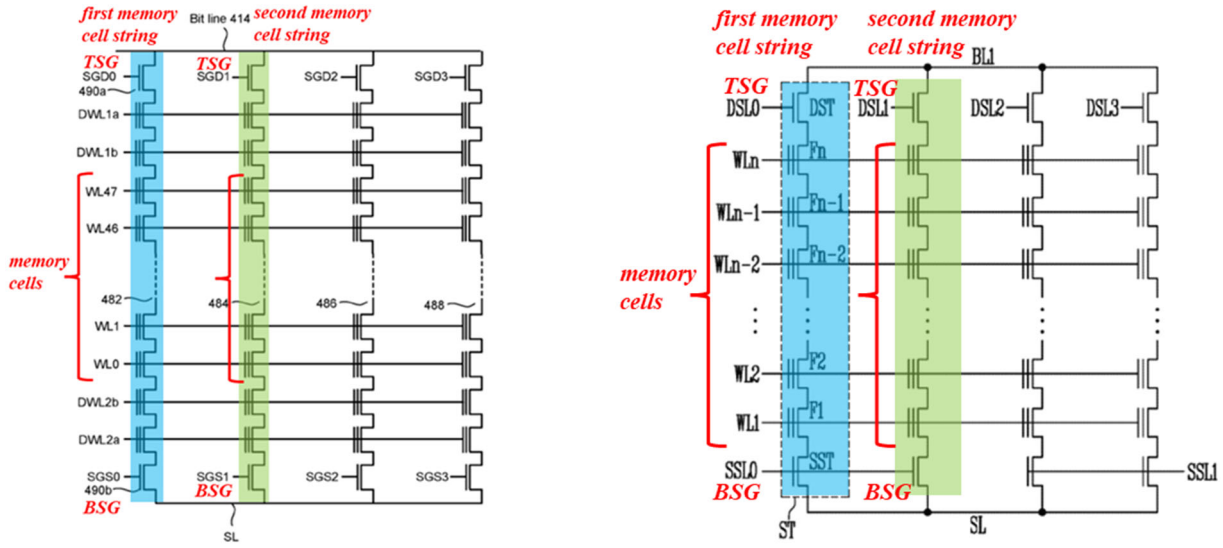
314. For example, both use memory devices comprising address decoding components (highlighted orange below), control voltage generators (red), controllers (green), read/write circuits (blue), and of course memory arrays (yellow):





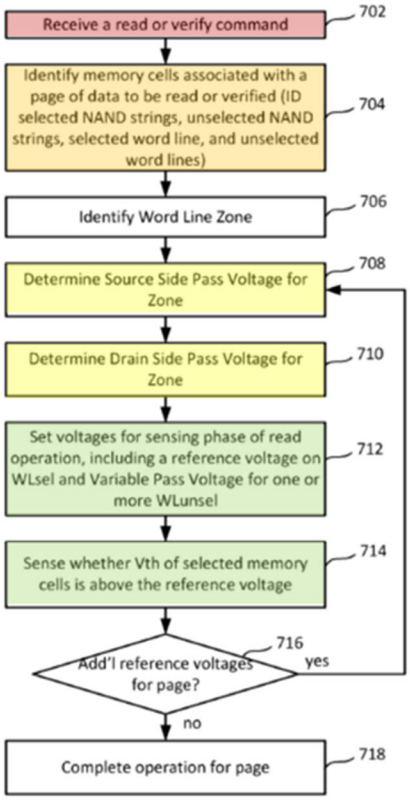
Ex. 1008, Fig. 2; *see also id.*, [0038]; Ex. 1009, Fig. 1. As a specific example, both Costa and Seo disclose a voltage-generating circuit and associated circuitry that generate and output control voltages to the memory cell array. Ex. 1008, [0038]-[0043]; Ex. 1009, [0040], [0049], [0065]-[0067], [0077]-[0085].

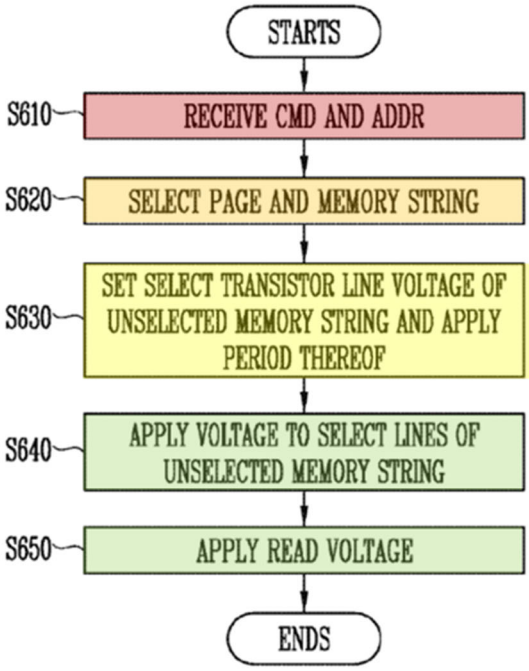
315. The structures of Costa's and Seo's memory cells are also virtually identical. Both have a conventional structure that was well known to a POSITA:



Ex. 1008, Fig. 4F, [0029], [0075], [0077], [0161]; Ex. 1009, Fig. 4, [0053]-[0059], Abstract.

316. Costa and Seo also have similar operating flows. For example, both devices receive a command (highlighted red below), identify and select the memory cell to be verified (orange), determine and set the appropriate voltages (yellow), apply the voltages and sense the results (green):





Ex. 1008, Fig. 14; Ex. 1009, Fig. 7. In light of these similarities, a POSITA would have had a reasonable expectation of success in applying Seo's voltage scheme to Costa's embodiment.

317. As I note for Ground 1, the claims are not limited to charge-trap memories, but even if they were, Seo's pre-verify operation creates an electrical field that mitigates the fast-charge loss for charge-trap memories (this electric field removes the fast-charge loss before the verification). *See* ¶ 196.

E. Secondary Considerations of Non-Obviousness

318. Based on my review of the '957 patent's prosecution history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's claims.

319. I am not separately aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like. Instead, as discussed above, it is my opinion that the subject matter embraced by the '957 patent's claims was known in and obvious over the prior art. Moreover, it is also my opinion the teachings of the prior art would have been expected to successfully function as or be usable with working 3D NAND memory devices.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: April 29, 2024

Location: Fremont, California

Signature: 

DR. DAVID KUAN-YU LIU