

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00792
U.S. Patent No. 11,468,957
Issue Date: October 11, 2022

Title: ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION

REPLY DECLARATION OF DAVID KUAN-YU LIU, PH.D.

YMTC
Exhibit 2023
Micron v. YMTC
IPR2025-00190
Ex. 2023-001

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I David Kuan-Yu Liu, Ph.D., declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron” or “Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office. I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to reply to certain of the opinions set forth in a January 31, 2025 declaration and associated April 17, 2025 deposition testimony of Steven Przybylski, Ph.D. submitted by Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) in this *inter partes* review proceeding relating to U.S. Patent No. 11,468,957, which I refer to herein as the ’957 patent.

3. I am being compensated at my current standard consulting rate, plus reimbursement for any reasonable expenses. My compensation is based solely on the amount of time that I devote to activities related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

4. The prior declaration I submitted in connection with this proceeding, which I understand has been designated as Exhibit 1003, sets forth among other topics my educational background and professional experience (Ex. 1003, ¶¶ 5-14

and associated Exhibit 1004), my understanding of the law (*id.* ¶¶ 19-34), an overview of pertinent technical background (*id.* ¶¶ 40-48), an overview of the '957 patent and its prosecution history (*id.* ¶¶ 49-59), the knowledge and characteristics of a person having ordinary skill in the art (*id.* ¶¶ 35-39), and certain claim construction opinions (*id.* ¶¶ 60-65).

5. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, my work with those of ordinary skill at the time of the alleged invention, and my general experience in the field of art.

6. I have also reviewed and considered the materials listed in my prior declaration (*id.* ¶ 18), the Board's Institution Decision (Paper 13), Patent Owner's Response (Paper 17), Dr. Przybylski's Declaration (Ex. 2003), and the following materials to the extent relevant to my opinions:

Exhibit	Description
1028	Declaration of Steven Przybylski, Ph.D. in Support of Patent Owner's Response in IPR2024-00795 in Connection with U.S. Patent No. 11,501,822
1029	Patent Owner's Preliminary Response in IPR2025-00117 in Connection with U.S. Patent No. 10,672,711 (Paper 9)
1030	U.S. Patent No. 10,861,537 to Lien et al.
1031	Transcript of April 17, 2025 Deposition of Dr. Steven Przybylski
2001	Micron 4-2 Claim Construction Disclosure

Exhibit	Description
2002	YMTC 4-2 Claim Construction Disclosure
2004	U.S. 2024/0295960 (“Li”)
2005	U.S. 2023/0343398 (“Dong”)
2006	Transcript of December 17, 2024 Deposition of Dr. Liu for IPR2024-00795 in Connection with U.S. Patent No. 11,501,822
2007	U.S. 10,726,920 (“Yang”)

7. The paragraphs below respond to certain of the arguments and assertions made by Patent Owner and Dr. Przybylski in this proceeding. In these paragraphs, I address only a fraction of the opinions and assertions Dr. Przybylski set forth in his declaration. The fact that I do not respond to any particular opinion expressed by Dr. Przybylski should not be considered to indicate agreement with that opinion.

II. CLAIM CONSTRUCTION

A. “Apply a [Top/Bottom] Bias Voltage ... in the Pre-Verify Stage and the Verify Stage”

8. In my original declaration, I explained that the plain meaning of these limitations does not require one voltage level in both the pre-verify stage and the verify stage. Ex. 1003 ¶¶ 163-64, 167. This plain meaning is supported by the claims and the specification of the ’957 patent. Furthermore, Patent Owner’s claim construction is at odds with its argument regarding applying voltages on the gate terminals (“on the gate terminal” argument). As I explain below, the requirement of

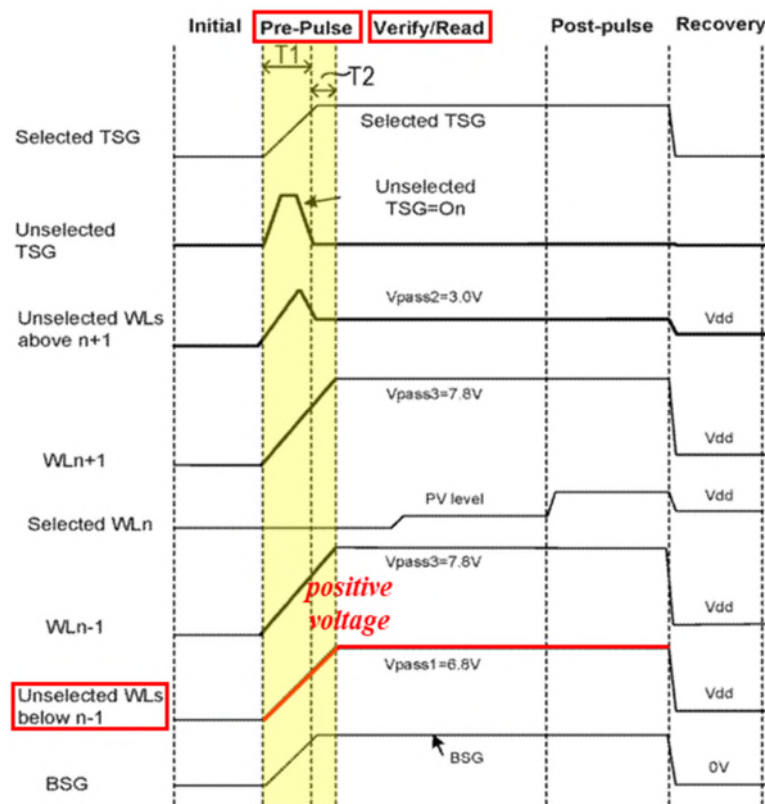
Patent Owner's construction is not feasible given Patent Owner's (incorrect) "on the gate terminal" argument.

9. Allowing more than one voltage level for the top/bottom bias voltage limitations is supported by the plain disclosure of the patent. The patent states "**the bottom bias voltage** can be increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage." Ex. 1001, 2:56-69 (emphasis added) (cited in Ex. 1003 ¶ 164). This means **the bottom bias voltage** may take on any voltage value from the initial voltage to the target voltage; it is not limited to a single voltage level. *See also id.* 4:4-7, 13:43-47 (same). The same is true of the top bias voltage. *Id.*, 2:59-61, 4:7-9, 13:49-53 (cited in Ex. 1003 ¶ 167). Dr. Przybylski's annotated figures omit the rising edges of the top and bottom bias voltages. *See* Ex. 2003 ¶¶ 50, 53. The omission is not consistent with the disclosure of the '957 patent.

10. The identical structure of the positive voltage limitation and its embodiments cannot be limited to a single voltage level in both stages. Claims 5 and 6 also recite a positive voltage limitation that has an identical structure to the top and bottom bias voltage limitations: "apply a positive voltage ... in the pre-verify stage and the verify stage." I explained that this limitation also does not require only one voltage level across the two stages. Ex. 1003 ¶¶ 171-72. Specifically, I explained that **the** positive voltage can have different voltage levels in the pre-verify

stage before reaching a target level applied in the verify stage. *Id.* (citing Ex. 1001, 2:62-63, 4:10-11, 13:54-58).

11. More specifically, and as I illustrated in my original declaration (§ 172), Figure 7 (and 9) embodiment of the '957 patent simply does not have a single positive voltage level in the pre-verify stage. For example, as shown in Figure 7 below, the positive voltage is ramping up for the entire duration of the pre-verify stage and does not reach its verify stage target level (6.8 V) until the beginning of the verify stage:

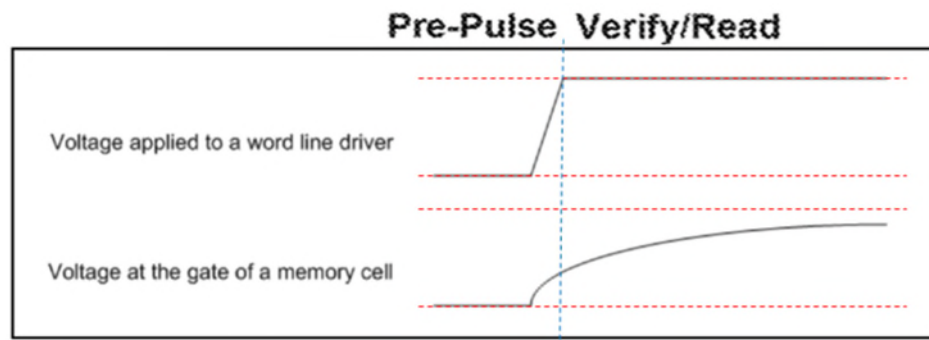


Ex. 1001, Fig. 7 (annotated); see also *id.*, 13:54-58.

12. Dr. Przybylski relies on Figure 7 as an embodiment of claim 5. Ex. 2003 ¶ 113. He specifically cites Figures 5-9 to support his claim construction. *Id.* ¶ 50. Thus, I understand that the positive voltage limitation of claim 5 (and 6) should be construed to encompass Figure 7. Patent Owner did not dispute my opinion of the positive voltage limitation. Therefore, the positive voltage limitation and its embodiments require a construction that allows more than one voltage level. I understand that under patent law parallel or analogous claim elements should be construed consistently. Thus, the same construction applies to the top/bottom bias voltage limitations. And, at the very least, Patent Owner is taking inconsistent positions with respect to the top/bottom bias voltage limitations and the positive voltage limitation.

13. Moreover, under Dr. Przybylski's incorrect "gate terminal" voltage argument, the positive voltage may not reach the target level, if it does at all, until long after the start of the verify stage due to the alleged RC time-constant delay. To illustrate using Dr. Przybylski's figure, if the straight-line waveform represents the positive voltage of Figure 7, and the positive voltage flattens out at the beginning of the Verify/Read period as it does in Figure 7, the alleged curved "Voltage at the gate" does not reach the target value (shown via dotted red lines above the waveforms) even at the start of the verify/read period (as it does in Figure 7). And it becomes all the more obvious that Figure 7 cannot satisfy a claim construction

requiring a single voltage level in both stages at least for the positive voltage limitation, and perhaps even the claim limitations of top/bottom bias voltages. Thus, with Dr. Przybylski's "gate terminal" argument, a positive voltage is never applied in the pre-verify stage and may not be applied in the verify stage either:



Ex. 2003 ¶ 94 (annotated). Dr. Przybylski's testimony effectively confirms this to be the case. He testified about this figure above that "the voltage at the memory cell," i.e., the gate voltage, "will be significantly delayed relative to the transition in the target voltage indicated in the top line." Ex. 1031, 199:6-12, 204:3-18.

14. Furthermore, the same problem exists with the first pass and first read voltages of claim 4, which respectively correspond to the voltages on $WLn+1$ and $WLn-1$ in Figure 7. Those voltages, like the positive voltage, do not reach their target value until the beginning of the verify stage. See Ex. 1001, Fig. 7. But claim 4 requires applying a first pass voltage and a first read voltage on the gate terminals of the adjacent memory cells during the pre-verify stage. While I disagree with Dr. Przybylski's opinion on "gate terminal" voltages, that argument cannot be reconciled with his claim construction argument.

III. GROUND 1

A. Voltage Applied on a Word-Line Layer Is Applied “on a Gate Terminal”

15. It is my opinion that applying voltages on word line layers is applying voltages on the corresponding gate terminals.¹ Hongtao expressly discloses this. Further, the '957 patent and prior art references simply do not distinguish the two but instead use the two interchangeably or even synonymously. Such usages are consistent with the operation of memory devices. Dr. Przybylski's arguments are based on an erroneous view of the '957 patent including the development of voltages and the shape of waveforms. His arguments are also based on a mistaken understanding of the dominant source of RC delays in 3D NAND flash.

1. Hongtao Discloses Applying Voltages on Gate Terminals

16. Dr. Przybylski does not dispute that Hongtao shows distinct voltages in the two stages. See Ex. 2003 ¶ 112 (characterizing similar waveforms in top and bottom select transistors as “***distinct*** target voltages”) (emphasis in original).

17. Dr. Przybylski disputes that Hongtao shows voltages applied on the gate terminals of memory cells. But the distinction of gate voltages and word line voltages has no basis in fact, as I explain further in subsequent sections.

¹ Accordingly, except where the context distinguishes the two, references to word line voltages in my declarations also refer to gate terminal voltages.

18. Additionally or alternatively, Hongtao discloses that “[t]he gates of the unselected memory cells on the selected string are applied with a conduction voltage through the unselected word lines.” Ex. 1005, [0025]; *see also id.*, [0034] (similar for top and bottom select transistors). This statement clearly says the conduction voltage (shown in Figure 2) is applied to the gates of memory cells. Dr. Przybylski’s rebuttal to this statement is the same flawed argument that distinguishes gate and word line voltages. Ex. 2003, ¶¶ 93-100. Further, Hongtao also implicitly teaches that the conduction voltage is applied at the gate of the memory cell. For example, it states that “this conduction voltage will generate a potential via channel coupling in all memory cells connected to word line....” Ex. 1005, [0020]. This implies that the conduction voltage is applied on the gate because channel coupling and read interference are caused by the voltage at the gate, not by a voltage away from the gate. For example, a reference cited on the face of the ’957 patent illustrates this channel coupling between word line (i.e., gate) and channel of memory cells. Ex. 1030, Fig. 10A. A POSITA would have understood Hongtao with that background knowledge. In this regard, I agree with Dr. Przybylski that gate voltages exert electric fields to control memory cell operations (though his opinion of a gate with zero width, even if conceptually, is wrong). Ex. 1031, 56:22-57:10, 63:5-64:21. Similarly, the statement regarding read interference also implies that the conduction voltage is applied on the gate because gate voltage creates read disturbance. Ex.

1005, [0024] (“The memory cells in the unselected rows with a conduction voltage applied to the unselected strings are subject to read interference caused by ‘conduction voltage - 0V,’ while the memory cells in the selected rows of the unselected strings are subject to read interference caused by ‘read voltage - 0V,’ the read voltage is close to the conduction voltage.”). Even if the distinction of gate voltages and word line voltages were real (it is not), Hongtao discloses applying voltages on the gate terminals.

19. Relatedly, because Hongtao’s Figure 2 shows gate voltage waveforms that reach a peak level, flatten out, and remain at that level for a significant amount of time before decreasing to the level at conduction voltage, a POSITA would have understood that these voltages reach the intended target levels, i.e., the high level during the pre-conduction phase and conduction voltage level during the read phase.

20. Dr. Przybylski argues that Hongtao’s paragraph [0026] does not support my opinion. Ex. 2003 ¶¶ 101-03. I disagree. Paragraph [0026] starts with the general principle affecting read interference: “[r]ead interference is positively related to the voltage causing read interference. The greater the voltage, the stronger the read interference. Therefore, the greater the conduction voltage, the greater the read disturbance to the memory cell.” Ex. 1005, [0026]. It then identifies “conduction voltage - driving voltage” as the voltage causing read interference in the Figure 2 embodiment. As such, it identifies a need to “further reduce the read

interference.” *Id.* These disclosures would have rendered obvious that one way to reduce read interference is to reduce conduction voltage, thereby reducing “conduction voltage - driving voltage,” the voltage positively related to read interference. And that is what Figure 2 shows. In fact, the effect of lowering the conduction voltage on unselected word lines will also serve to reduce disturb on the unselected memory cells in the unselected string, the same mechanism that Dr. Przybylski uses to wrongly argue not changing the bias voltages between Hongtao’s pre-conduction and read periods. Ex. 2003 ¶ 99. That Hongtao proceeds to introduce another method to “*further* reduce the read interference” does not negate what it discloses in Figure 2. Ex. 1005, [0026] (emphasis added).

2. PO’s Manufactured Word-Line-Voltage Dispute Fails

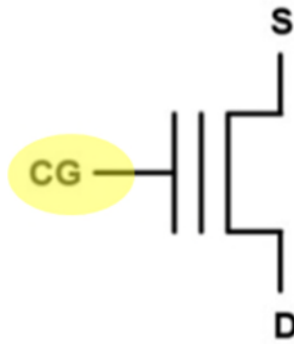
21. Dr. Przybylski’s “on the gate terminal” arguments suffer from many deficiencies. At the core, the focus of the 3D NAND flash field is on operations of such devices, which to a large part are accomplished through gate or word-line voltages, and on the impact such voltages may have on device reliability, such as read/program disturb or hot carrier injection (“HCI”). In that context, literature in the field treats word lines as gate terminal and word line voltages as gate voltages. Such treatment is correct because a word line layer has an equal voltage potential due to its negligible resistance, especially compared with other components in the voltage path. Based on misunderstanding or mischaracterization of the ’957 patent

and the characteristics of 3D NAND flash, Dr. Przybylski creates a distinction that simply does not exist in the patent or the references.

a. The '957 Patent and Prior Art Use Gate Terminals and Word Lines Interchangeably

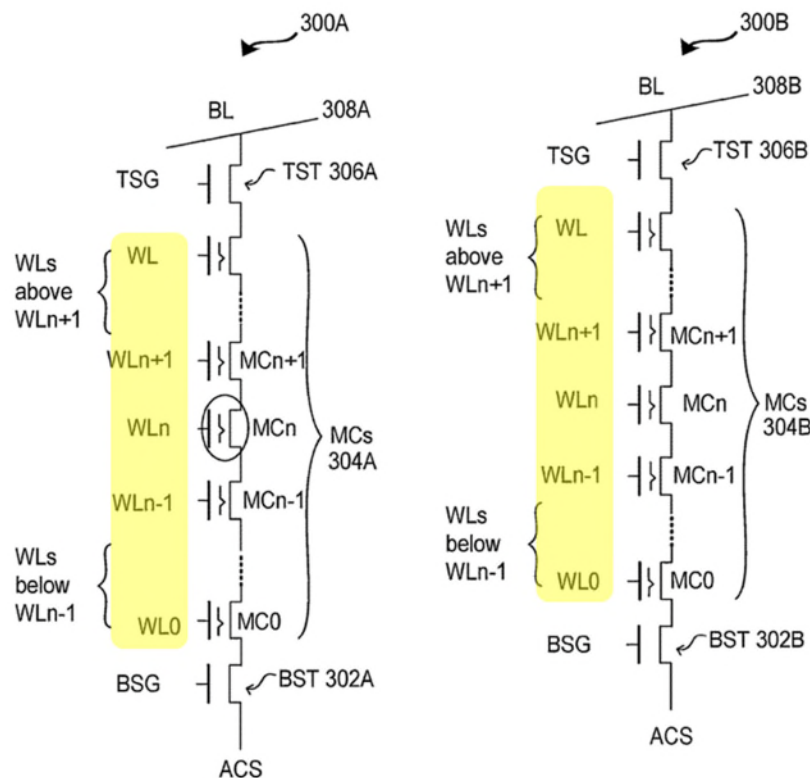
22. Patent Owner actually agrees with my position. It states in another IPR between Petitioner and Patent Owner that “the wordlines serve as the gates of the transistors comprising the memory stack.” Ex. 1029, 11. That is a clear statement of the equivalence between word lines and gates: the word lines functions as gates and thus control the operations of the memory cells. And since the word lines function as gates, word line voltages are gate voltages.

23. As an initial matter, “gate” and “gate terminal” are synonymous in the '957 patent. Ex. 1001, 9:35-36, 9:42. This is consistent with the common parlance in the field. Relatedly, the gate is sometimes referred to as control gate or “CG,” as shown in the well-known symbol of a field effect transistor that forms a memory cell:



Ex. 1018, 81 (annotated). Dr. Przybylski agrees that such usages are common in the field. Ex. 1031, 57:11-19.

24. Turning to the '957 patent, it refers to memory cells as WLs. Ex. 1001, 12:24-27 (“the selected memory cell (WL_n) and the upper adjacent memory cell (WL_{n+1})....”). This disclosure closely associates word lines with the memory cells. More specifically, the patent equates “gate layers” with “word line layers.” *Id.*, 8:4. It further labels the gate terminals of the memory cell transistors as “WL”:



Id., Fig. 3 (annotated). Figure 3 sets the context through which a POSITA would understand the patent disclosure, including the waveform figures 4-9. Specifically, WL is CG or control gate of the memory cells. Thus, the waveforms in Figures 4-9 labeled with “WL” are gate voltages. *See also id.*, 8:54-56 (“**gate voltages can be applied on gates** of the memory cells through the word line contacts 22 that are **coupled to the word line layers** 12 a-12 p.”) (emphases added).

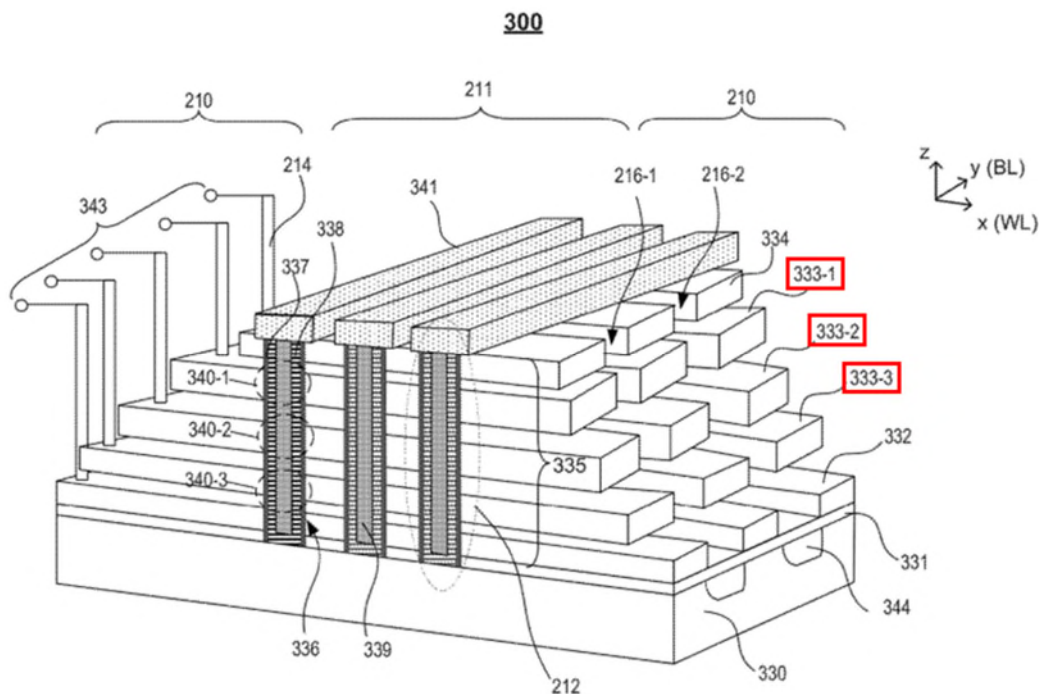
25. Relatedly, except unselected TSG gate voltage in Figure 7, all voltage references in the descriptions of claimed embodiments Figure 6-9 are word line voltages. *See generally* Ex. 1001, 12:27-15:30 (descriptions of Figures 6-9); *id.*, 13:33-42 (unselected TSG gate voltage of Figure 7). A POSITA would understand

these figures to be embodiments of the claims because gate voltages are word line voltages. *Id.*, 8:54-56. Otherwise, there would exist a gap between the descriptions of the embodiments and the claimed inventions. This gap is particularly problematic because of the serious operational issues associated with Dr. Przybylski's alleged distinction between gate and word line voltages. *See infra* § III.A.2.c.

26. Because the '957 patent equates gate voltages and word line voltages, its descriptions of the operation of memory cells based on word line voltages make sense, since in a strict or narrow sense (not used in the '957 patent) memory cell operation depends on the gate voltage. Ex. 1031, 56:22-57:10, 64:1-21 (PO's expert stating the effect of gate voltage on memory-cell operations). By "strict or narrow sense," I am referring to the fact that memory cell transistors, apart from its relationship to the memory block structure, have gate terminals but not word lines. *See* Ex. 1018, 81 (the well-known transistor symbol). For example, the patent discloses that "[t]he verify/read operation can be configured to verify whether memory cells are programmed successfully **by applying appropriate bias voltages on the word line layers** of the memory cells, the TSG layer of the TSG transistor, and the BSG layer of the BSG transistor." Ex. 1001, 9:62-67 (emphasis added). A POSITA would understand bias voltages on the word line layers effectuate verify/read operations because word line layers voltages are gate terminal voltages. Thus, "applying appropriate ... voltages on the word line layers" is applying the

same appropriate voltages on the gate terminals. As another example, the description of Figure 4 repeatedly states voltages “can be applied on” the word lines, the TSG layer, or the BSG layer. *Id.*, 10:57-11:12. The result of these voltages applied on word lines is “to form conducting channels in the selected memory cell string and the unselected memory cell string respectively.” *Id.*, 11:12-15. This result follows from the description of applying word line voltages because the voltages on the word lines are the voltages on the gate to turn on the memory cells to form a conducting channel. As yet another example, comparison of word line voltage with threshold voltage only makes sense if the word line voltage is the gate voltage because the threshold voltage of a transistor is the minimum **gate**-to-source voltage required to turn on the transistor. *See id.*, 11:44-48 (“As mentioned above, the bias voltage (or verify voltage) applied on the selected word line layer WL_n can be equal to the threshold voltage of the selected memory cell when the selected memory cell is not programmed.”); Ex. 1031, 87:1-19 (Dr. Przybylski testifying that threshold voltage is the difference between gate and source voltages).

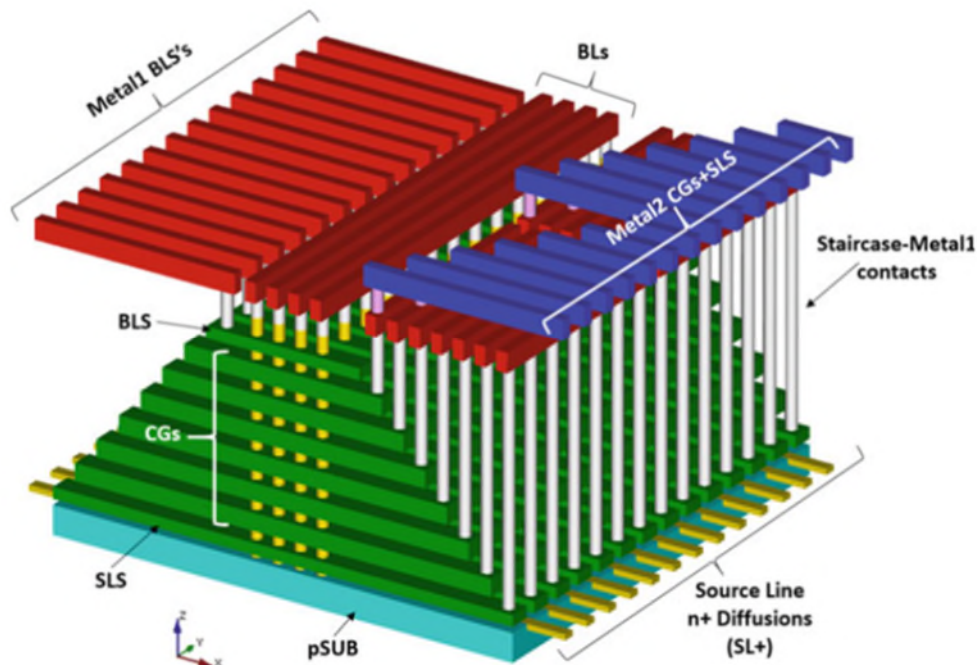
27. Another patent of Patent Owner, U.S. Patent No. 11,600,342, states that “control gates 333 [are] also referred to as ‘word lines (WLs).’” Ex. 1025, 6:41-42:



Id., Fig. 3 (annotated). As shown in the figure, control gates 333 are the word line layers of the NAND flash staircase structure. And it is reasonable that the inventors of that patent and the '957 patent, all Patent Owner's employees, would have the same understanding of such terms of art.

28. The disclosures of the '957 patent reflects the common usage of the prior art, which also supports my opinion.

29. **First**, prior art also refers to gates as word lines. For example, as shown below, the textbook authored by Micheloni labels word line layers as CGs or control gates.



Ex. 1018, 131. Another textbook cites a 1994 reference that equates “Control Gate” with “Word Line”):

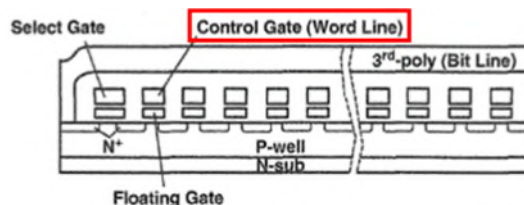


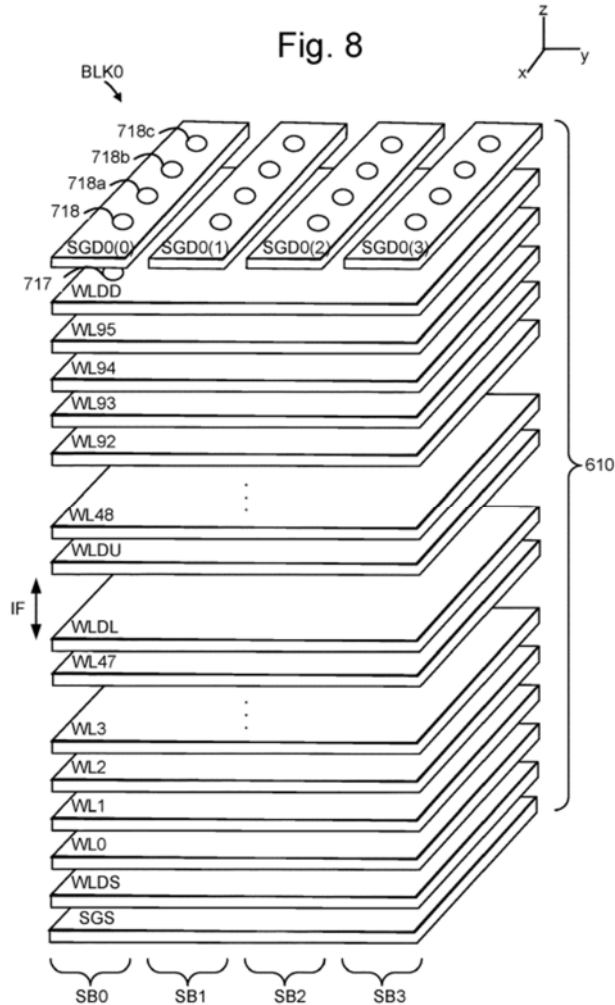
FIGURE 3.4 Cross-sectional view of a 0.4-μm-rule NAND-structure cell. Copyright 1994, The Japan Society of Applied Physics.

Ex. 1014, 62; *see also id.*, 205 (“CGs (word lines: WLs)”).

30. These figures also show PO’s expert testimony that the gate has zero width in the direction of the word line layer to be wrong. Ex. 1031, 70:6-71:2. Since these figures denote the entire word line layers as the control gate, the size of the word line layers is the size of the control gate. Apart from that, Dr. Przybylski’s explanation of gate terminal having zero width is incorrect. He explained that it is

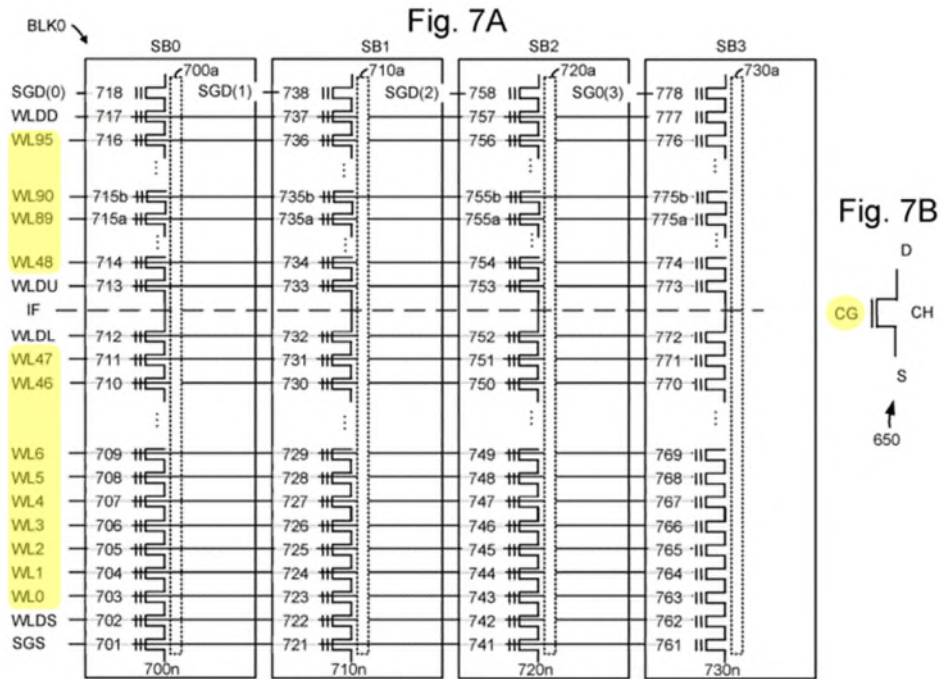
the voltage at the boundary of the word line layer and the gate dielectric that exerts an electric field that controls memory cell operations. But even a voltage at a point further away on the word line can exert an electric field. It does not make sense to separate the boundary of the word line layer from its adjacent material, conceptually or otherwise. In any event, this explanation is irrelevant because, as shown herein, the 3D NAND field simply does not distinguish word line and gate terminal.

31. Patent literature already cited in this proceeding also equates gates with word lines. See Ex. 1022, [0045] (“any one of the voltages VA, VB, and VC ... is applied to the control gate electrode (the word line WLn) of a selected memory cell MCn in the memory string MS.”). A patent cited by the Examiner during the prosecution of the ’957 patent discloses that “the memory cells can be arranged with a common ***control gate line (e.g., word line) which acts a [sic] control gate,***” and that “[t]he control gate layers ... include the layers ... WL0-WL47, ..., WL48-WL95....” Ex. 1030, 3:1-3, 19:14-18. These WLn control gate layers are the word-line layers:

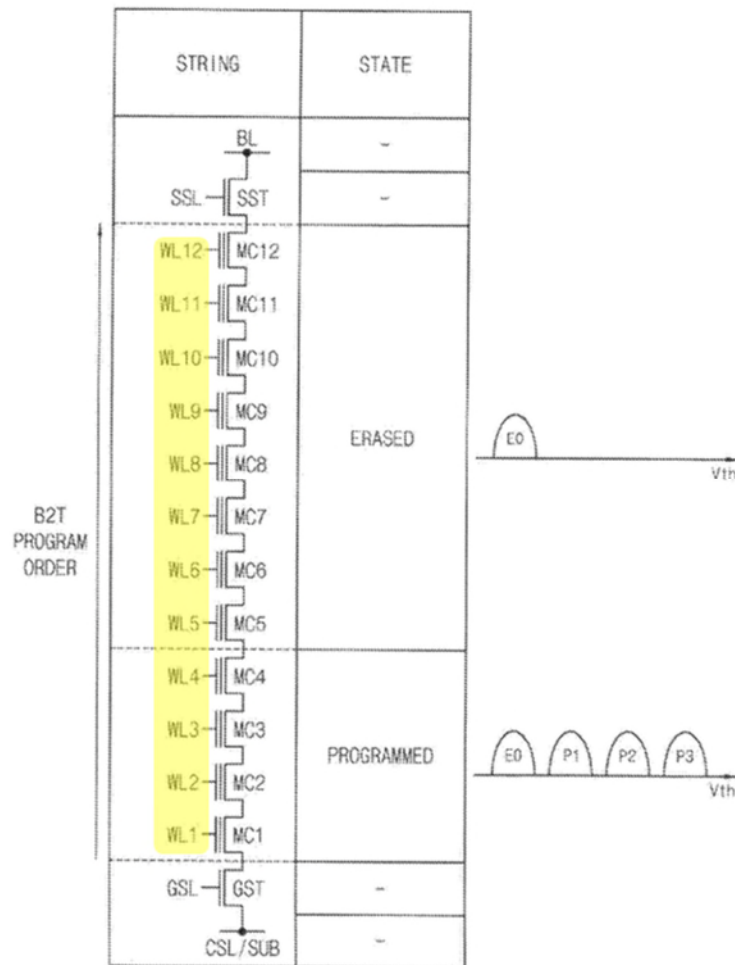


Id., Fig. 8; see also *id.*, 12:41-46 (“If the pass transistors are on, a voltage from the row decoder is provided to the respective **control gate lines or word lines**....”).

32. Further, like the '957 patent, prior art labels gate terminals of the memory cell transistors as “WL”:



Ex. 1030, Figs. 7A-7B (showing the well-known transistor symbol with gate labeled CG side by side with a memory block with the corresponding gates labeled WL).



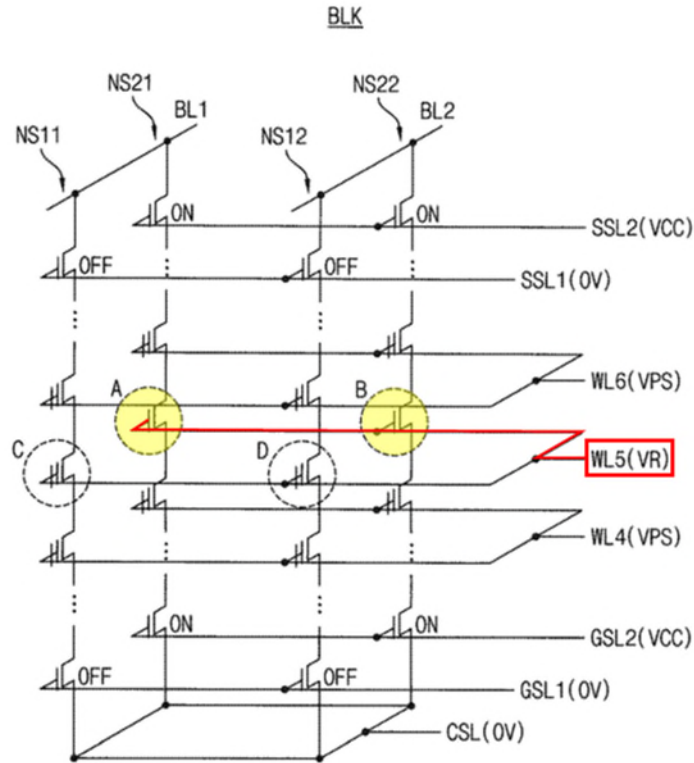
Ex. 1006, Fig. 11 (annotated), *see also id.*, Figs. 14, 20-25 (same).

33. **Second**, a POSITA would have understood “word line” voltages in the literature as “gate terminal” voltages. Otherwise, these disclosures would not provide sufficient information to determine the on/off state of memory cell transistors. Indeed, the same reference cited by the ’957 patent expressly says so: “Vcg is the control gate voltage of the memory cell (the word line voltage).” Ex. 1030, 20:37-38; *id.*, 3:38-42 (“A verify test can involve **applying a control gate voltage** of an assigned data state **to the selected word line** while sensing circuitry

determines whether cells connected to the word line are in a conductive or non-conductive state.”)

34. Costa also supports this conclusion. Costa’s Figure 10 shows “WL” voltages, which Costa describes as “a signal applied to the control gates of a plurality of memory cells connected to a common word line.” Ex. 1008, [0085]. Additionally, Costa explains that “[t]he increased channel resistance may require a larger **gate voltage** for a selected memory cell to turn on” and shows word line voltages. *Id.*, [0103], Figs. 12A-12H; *see also id.*, [0126]-[0127] (similar). A POSITA would have understood this disclosure to mean that the word line voltages shown in the figures are applied to control gates because gate voltage affects memory cell operation and channel resistance.

35. As a final example, the figure below shows read voltage VR applied on a word line WL5:



Ex. 1021, Fig. 13 (annotated). In the corresponding description, the reference discloses that “the selection read voltage VR is applied to **gates** of the selected memory cells A and B.” *Id.*, [0102]. In other words, the voltage applied on a word line shared by two different memory strings (NS21 and NS22) **is** applied to the gates of memory cells of those two memory strings.

36. This disclosure provides a fitting summary of what a POSITA would have known: a voltage applied on word lines “is applied to gates....” *Id.*

37. Additionally, because transistor operations are determined in part by the gate voltage, a POSITA would have understood references that discuss applying a word line voltage to effect memory cell operations to be equating word line

voltages with gate voltages. As Dr. Przybylski defines in his declaration of another IPR proceeding between Petitioner and Patent Owner, the threshold voltage of a memory cell is “the voltage that, when ***applied to the gate terminal*** of the memory cell, will cause the transistor to turn on and begin conducting current between the source and drain.” Ex. 1028 ¶ 30. As explained, gate voltage relative to threshold voltage controls memory cell operations.

38. Many such examples exist in the literature, even just among references already cited in this proceeding. *See, e.g.*, Ex. 1008, [0096] (“During a read or verify process, the unselected memory cells and dummy word lines are provided with one or more read pass voltages at their control gates so that these memory cells will operate as pass gates (e.g., conducting current regardless of whether they are programmed or erased).”); Ex. 1007, [0144], [0232]-[0233] (disclosing applying a voltage to a word line to cause the transistor to turn on or off, and that on/off state is based on the gate voltage); Ex. 1006, [0117], [0121] (disclosing voltages applied on a word line acting on the memory cell); Ex. 1008, [0108] (“The pass voltage applied to the dummy word lines and word lines WL0-2 WL4-WL127 cause the corresponding memory cells to operate as pass gates”); *see also id.*, [0121] (similar); Ex. 1020, 16:16-34 (describing applying voltages on a selected word line for threshold voltage determination). Indeed, it was textbook material to describe applying a voltage to a word line to turn on a memory cell transistor. *See, e.g.*, Ex.

1014, 42 (“ V_{passR} (~6 V) is applied to an unselected word line to be as a pass transistor.”).

39. The application of gate voltages is applicable to programming operations as well. Gate voltage is applied to cause changes in threshold voltage during programming. Yet it is common to describe applying a word line voltage to change the threshold voltage in a programming operation. See Ex. 1007, [0124] (“When program voltage VPGM is applied to the word line WLsel, the threshold voltage of the memory cell transistor MT that is coupled to the word line WLsel and coupled to the program target bit line BL increases.”).

40. **Third**, Dr. Przybylski takes the position that, based on the curved lines, Suzuki shows “actual bias voltages applied on gate terminals.” Ex. 2003 ¶ 127. But he completely ignores that Suzuki itself describes the voltages as word line voltages. Ex. 1007, [0138] (“When VCGM is **applied to the word lines** WLsel and WLusel, the channel voltage of the NAND string NS, which is in the floating state, drops due to the **coupling between the channel and the control gate.**”) (emphases added); see also *id.* [0134] (similar). Applying voltages to the word lines produces coupling between the memory string channel and the control gate because the word line voltage is the control gate voltage.

b. Patent Owner Distorts the Import of Curved Waveforms

41. Before explaining how the '957 patent supports my opinion, it is helpful to explain how various figures of the '957 patent relate to the alleged invention and to other figures.

42. The '957 patent alleges that its voltage levels in the pre-verify versus the verify stage help prevent HCI and ESUM loss. Ex. 1001, 7:13–32. In other words, the alleged invention mitigates the effect of a short pre-pulse time because HCI and ESUM loss also do not occur in the conventional schemes when pre-pulse time is sufficiently long. *See id.*, 12:63–13:4. Specifically, the patent alleges that the lower second bias voltage mitigates the HCI and ESUM loss effects even when the pre-pulse period is short. *Id.*, 12:63-13:42 (description of Figure 7).

43. A lower second bias voltage mitigates the impact of a possible HCI on the selected memory cell, due to a potentially large gradient across the channel toward its upper adjacent cell (in the bottom-to-top programming order of Figure 7), if the first bias voltage is not fully developed on the word line layer before the end of the pre-verify stage. Normally, when there is sufficient time for the first bias voltage to be developed before the unselected top select gate (TSG) is shut off, the voltage on the channel of the upper memory cells are all set to 0V through coupling with a bit line voltage, and the subsequent shutting off the unselected TSG would not further increase the channel voltage due to coupling since the word line voltages

(on both selected and unselected memory cells) would not change afterward. They have already ramped up to the final voltages and simply stay at those respective levels. On these memory cells, there is no further boosting of the channel voltage due to word line coupling. *Id.*, 11:58-12:1. However, if the first bias voltage has not been fully developed on the word line layer before the unselected TSG is shut off, the channel of the unselected strings loses its contact with the bit lines, and if the first bias voltage is still ramping up to V_{pass} (6.8V), the channel of these upper memory cells would be boosted due to the coupling with this ramping gate voltage, and creating a channel voltage gradient relative to the selected memory cell. *Id.*, 12:1-27. Having a lower second bias serves to limit the amount of boosting due to the continuation of first bias voltage ramping. *Compare id.*, Fig. 5 (showing voltage on unselected WLs above $n+1$ continues to ramp up after the unselected TSG starts to shut down) *with id.*, Fig. 7 (showing voltage on unselected WLs above $n+1$ ramps down to V_{pass2} after the unselected TSG starts to shut down). As a side note, the theoretically ideal solution is clamping the first (and the second) bias voltage at whatever voltage it has developed (or ramped) right when the unselected TSG is shut off. Such an ideal case would ensure that the channel of the upper memory cells on the unselected string would not be boosted through coupling since the voltage on their word lines remains constant. But that is not possible to do because, for

example, the voltage generating circuits do not have sufficient information to determine the voltage level at which to clamp the bias voltages.

44. Figure 7, like Figure 5, involves a short pre-pulse period. And Figure 7 is allegedly an inventive improvement over Figure 5. Ex. 1001, 13:8-11. In contrast to Figure 5, in Figure 7 “ESUM loss can be prevented.” *Id.*, 14:19-30. On the other hand, Figure 6, like Figure 4, does not involve a short pre-pulse period. Figures 8 and 9 are respective counterparts to Figures 6 and 7 in which the programming order is reversed such that the unprogrammed memory cells are located below the selected memory cell in Figures 8 and 9 rather than above the selected memory cell in Figures 6 and 7. Because the claims cover embodiments shown in Figures 6 to 9, the length of the pre-verify stage (and whether the gate voltage fully develops) does not define the alleged invention. *Id.*, 12:63-13:4, 14:19-30, 15:18-30 (disclosing that embodiments shown in these figures can prevent ESUM loss). The flow chart of Figure 10 uses language virtually identical to claim limitations [1.A.i]-[1.A.iv] to disclose a method. Figure 10, however, does not disclose an apparatus nor any of the requirements of dependent claims.

45. In deposition, Dr. Przybylski was not able to opine whether any of Figures 4 through 10 embodies any claims of the '957 patent. Ex. 1031, 117:18-124:20. That seems rather strange. He readily opined that Hongtao's Figure 2, like Figure 4 of the '957 patent, shows piecewise linear waveforms and thus does not

disclose gate voltages. *Id.*, 165:12-166:4. In fact, he testified that the piecewise linear waveforms of Hongtao's Figure 2 provide "more than sufficient reason" to conclude they do not show gate voltages. *Id.*, 168:13-169:7. He also opined that Figures 4, 6, and 7 show piecewise linear waveforms. *Id.*, 225:22-226:15. In light of his testimony, one would reasonably think that he could readily conclude that at least none of Figures 4, 6, and 7 is a claimed embodiment. After all, reaching that conclusion based on his opinion involves such a simple logical step that even a layperson can readily make that conclusion. Yet he was unable or perhaps unwilling to opine that the figures of the '957 patent do not show gate voltages based on his theory. *Id.*, 117:18-124:20.

46. Figure 5 of the '957 patent is consistent with the explanation above. It illustrates a scenario in which the voltage on the word line layer (i.e., on the gate terminal) is not sufficiently developed to 6.8V before the end of the pre-pulse period. This is because the delay from the voltage generating circuits to the word line layer does not allow the voltage on the word line layer to rise to the target voltage output by the voltage generating circuits with a short pre-pulse period. Figure 5 illustrates HCI and ESUM loss in the conventional schemes when the pre-pulse period is short, i.e., less than 1 ns. See Ex. 1001, 11:58-60, 12:10-18. In contrast, the claimed embodiments Figures 6 through 9, whether having a short (Figures 7 and 9) or long (Figures 6 and 8) pre-pulse period, allegedly can reduce HCI and ESUM loss. *Id.*,

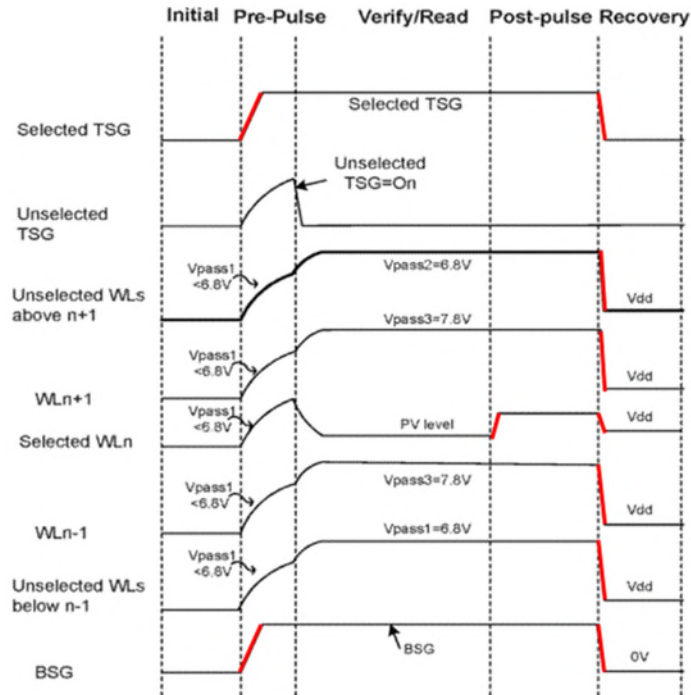
13:13-25, 14:19-30, 15:18-30. Thus, a POSITA would understand that the curves of Figure 5 illustrate their corresponding insufficient voltage development. *Id.*, 6:66–7:12; 11:57–12:27.

47. Consistent with my explanation above, when the '957 patent talks about a voltage being “developed,” it consistently refers to the word line voltage. *Id.*, 7:2-7, 12:15-21, 13:13-20. These disclosures do not mention gate or gate terminal at all. *See also id.*, 6:50-53, 6:66-7:2, 11:60-65, 12:1-6, 14:19-21, 15:18-21. Moreover, disclosures of voltages not fully developed appear in the context conventional schemes having a short pre-pulse duration such as Figure 5. *Id.*, 6:66-7:12, 12:15-18 (“The verify/reading operation can have a pre-pulse stage with a short pre-pulse time. ***The short pre-pulse time may be insufficient for the bias voltages applied on the WLs ($>n+1$), $WLn+1$, WLn , $WLn-1$, and WLs ($<n-1$) to be developed fully in the pre-pulse stage.***”). This confirms that the curves of Figure 5 illustrate such under-developed voltages. Furthermore, such disclosures are consistent with my explanation below that the output voltages from the voltage generating circuits need time to be developed on the word line layer. Specifically, a pre-pulse duration less than 1 ns may be insufficient for the bias voltage from the voltage generating circuits to be developed on the word lines because of the delay from the voltage generating circuits to the word line layers. The main resistive contribution of this delay is the resistance of the row decode circuit. *See infra* § III.A.2.c.

48. Figures 4 and 5 illustrate conventional schemes, which the '957 patent refer to as “related example[s].” Ex. 1001, 5:50–55, 6:37, 9:57-59, 12:10-13. In these conventional schemes, when pre-pulse time is sufficiently long (as illustrated in Figure 4), HCI and ESUM loss may be prevented. *Id.*, 6:50–65, 11:58–12:1. But when pre-pulse time is not sufficiently long (as illustrated in Figure 5), HCI and ESUM loss may occur. *Id.*, 6:66–7:12, 12:10–27 (stating that what Figure 5 depicts “result[s] in the ESUM loss”).

49. Dr. Przybylski’s argument that “straight lines and sudden changes [in a waveform diagram] signifying target voltages” rather than gate voltages creates interpretative problems of the '957 patent that he failed to address. Ex. 2003 ¶ 96. To begin, only Figure 5 shows some curved lines on the rising edge of waveforms in the pre-pulse period. If gate voltages are signified by curved lines, a POSITA would have expected the falling edge of these same waveforms also be shown with curved lines, not straight lines and sudden changes. Ex. 1031, 214:19-215:4 (Dr. Przybylski agreeing that RC delays apply to both rising and falling voltages). Similarly, the straight-line rising edge of the voltage on Selected WLn at the end of Verify/Read period is inconsistent with their argument. And the rising edges of Selected TSG and BSG shown with straight lines and sudden changes are also inconsistent with, e.g., the rising edge of Unselected TSG shown with a curved line.

Id., 76:17-77:5 (Dr. Przybylski agreeing that TSG and BSG layers are word line layers).



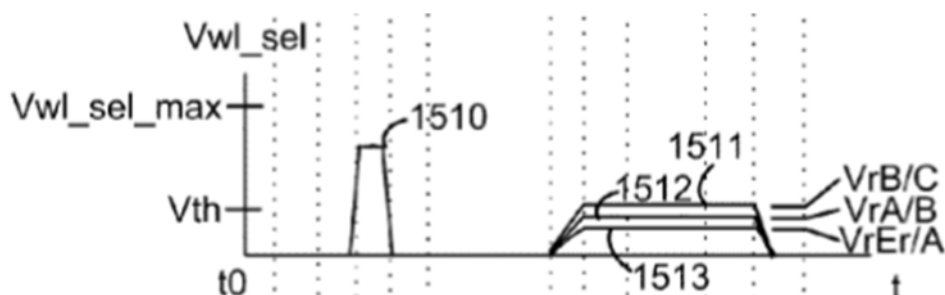
Ex. 1001, Fig. 5. Under his theory, it is also puzzling that none of the claimed embodiments Figures 6-9 show curved waveforms to indicate gate voltages. Instead, all of Figures 6-9 (and Figures 4-5) label their waveforms, whether curved or straight, as WL waveforms. These inconsistencies disappear with the correct understanding that the curved waveforms of Figure 5 illustrate voltages that do not fully develop between the voltage-generating circuit and the word line layers in the short pre-pulse period in the conventional scheme. Specifically, they are voltages that have different voltage levels in the short pre-pulse period and the verify/read

period. In contrast, the voltages on BSG and Selected TSG do not change between pre-pulse and verify/read periods.

50. In my opinion, the internal inconsistencies of Figure 5 make it an unreliable source for interpreting the '957 patent and its claims. An RC delay in the form Dr. Przybylski alleges should apply to both rising and falling edges of waveforms. Thus, for example, Suzuki shows curved lines on both rising and falling edges. Ex. 1007, Fig. 11. Further, the straight-line rising edge of Selected TSG and BSG waveforms in Figure 5 are inconsistent with those of the word lines and Unselected TSG. The word line, TSG, and BSG layers are made from the same material, and all of the voltages are applied via row decoders. See Ex. 1001, 8:2-8 (disclosing that word line layers include BSG and TSG layers); Ex. 1031, 76:17-77:5 (Dr. Przybylski agreeing that TSG and BSG layers are word line layers). Therefore, if there is an RC delay in the form Dr. Przybylski argues, all of these layers should experience the same type of delays and be shown with the same type of lines, whether curved or straight. Further, Figure 5 is a related example, not a claimed embodiment. Ex. 1001, 5:53-55, 12:10-13, 17:7-17 (recognizing Figure 5 as a related example over which the alleged invention offers advantages). Construing the claims based on an embodiment with ESUM loss problem that the patent purports to solve is relying on the wrong foundation. See Ex. 2003 ¶¶ 35-36

(citing Figure 5 as key support to the “on the gate terminal” argument). And the problem created by Dr. Przybylski’s arguments shows that his arguments are wrong.

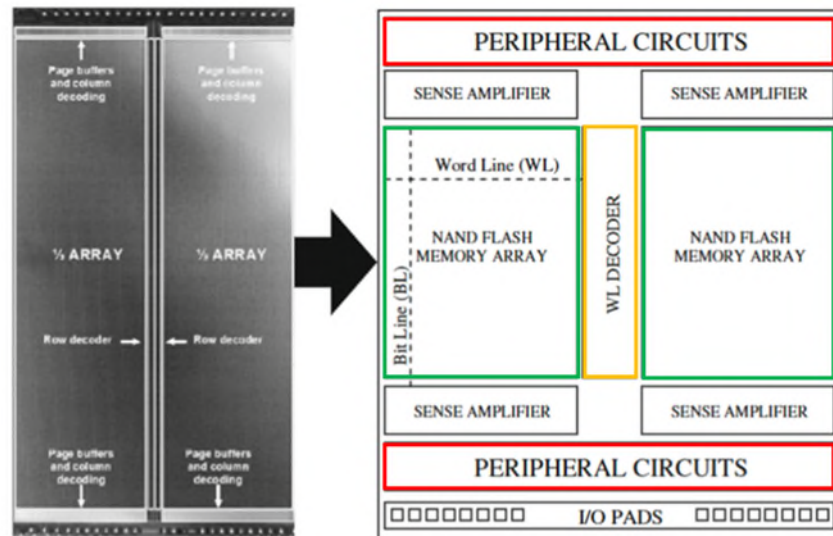
51. Moreover, Dr. Przybylski’s argument based on curved waveforms is also inconsistent with prior art. For example, the figure below shows waveforms with straight lines and sudden changes:



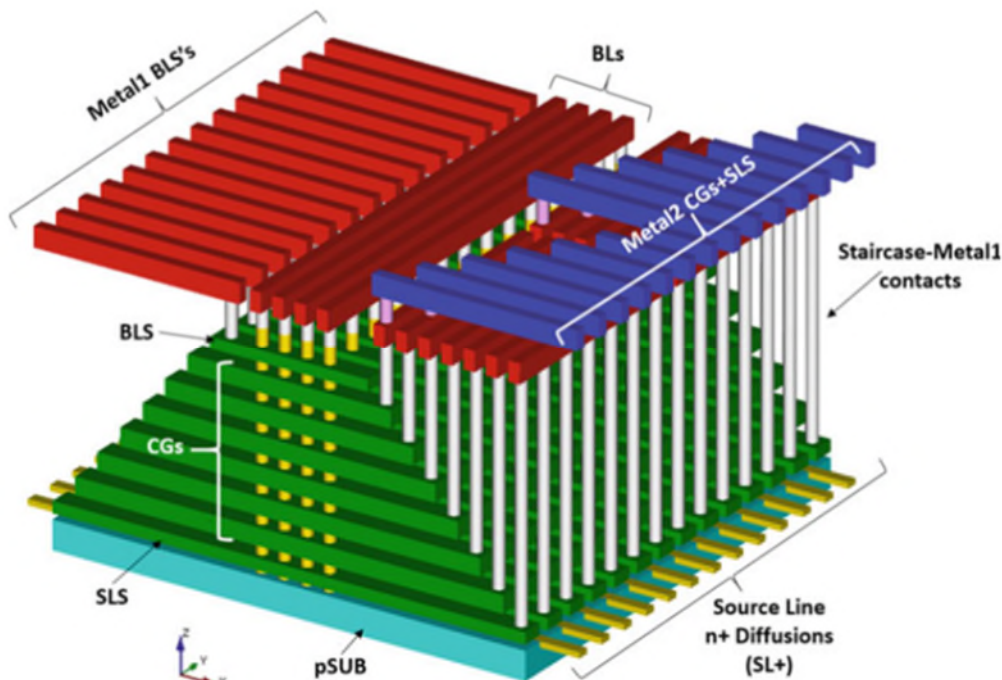
Ex. 1019, Fig. 15B. These waveforms under his theory would not be gate voltages. But the reference states “Vwl_sel can be provided at one of three **control gate** read levels.” *Id.*, 25:2-3 (emphasis added). As an example of the reversed scenario, Dr. Przybylski argues that Suzuki’s curved waveforms indicate gate terminal voltages. Ex. 2003 ¶¶ 127, 138. But Suzuki itself discloses “a voltage VPASS is applied to each of the word lines WLsel and WLusel.” Ex. 1007, [0134]. As yet another example, the ’957 patent-cited reference that I have mentioned expressly discloses an RC delay between the peripheral circuits and the word lines shows a curved waveform and describes it as “a voltage **applied to a word line** during a sensing operation.” Ex. 1030, Fig. 10A, 19:60-61.

c. Patent Owner Errs on the Dominant Source of RC Delays and Creates an Unworkably Complicated Device

52. The applied voltages are generated by voltage generating circuits. These circuits are located in a peripheral circuit section, located apart from the memory arrays:

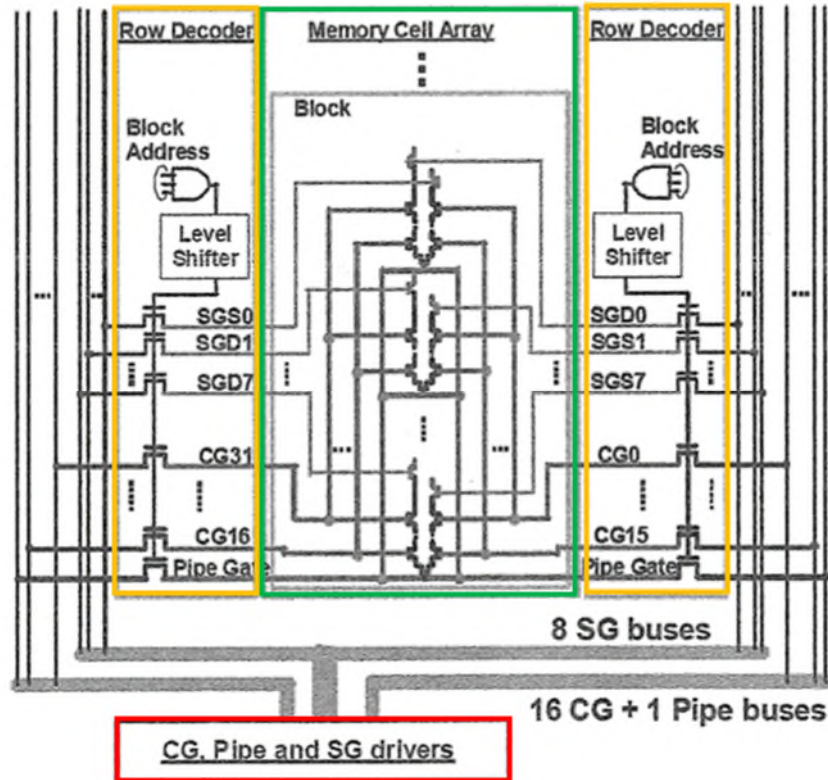


Ex. 1018, 83 (annotated). The voltage output from the voltage generating circuits propagates through word line decoders to NAND flash memory arrays via conducting lines, such as (illustrated in an exemplary memory array structure below) Metal2 lines, Staircase-Metal1 contacts (i.e., word line contacts), to the word line layers (labeled CGs or control gates):

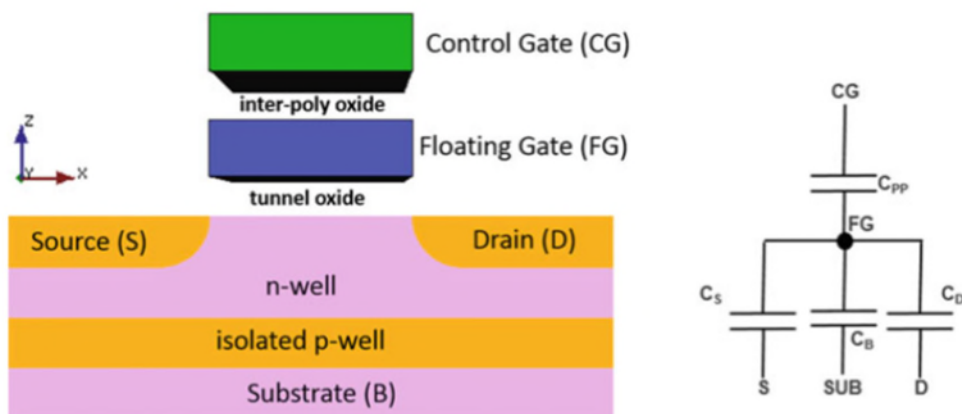


Id., 131.

53. The outputs of the voltage generating circuits do not appear instantaneously on the word line layer due to a RC delay. Ex. 1031, 108:17-22. The resistive component of the delay is dominated by the resistance of components outside the memory arrays including the word line decoder. The word line decoder comprises transistors with a significant resistance across the source and drain (i.e., across the current path) even in the ON state, typically a couple thousand ohms. An exemplary word line coder showing its internal transistors is shown below:



Ex. 1014, 307 (annotated with the same color/functional block pairing as in the flash circuit block diagram above). In contrast, the word line layers comprise conducting materials and their resistance is negligible compared with the resistance through the decoder. The capacitive component of the RC delay is the capacitance between the word line layer/gate terminal of a memory cell and the memory string channel, i.e., with the word line layer (the gate layer) as one plate of the capacitor, and the channel as the other plate. An exemplary model of this capacitance is shown below:



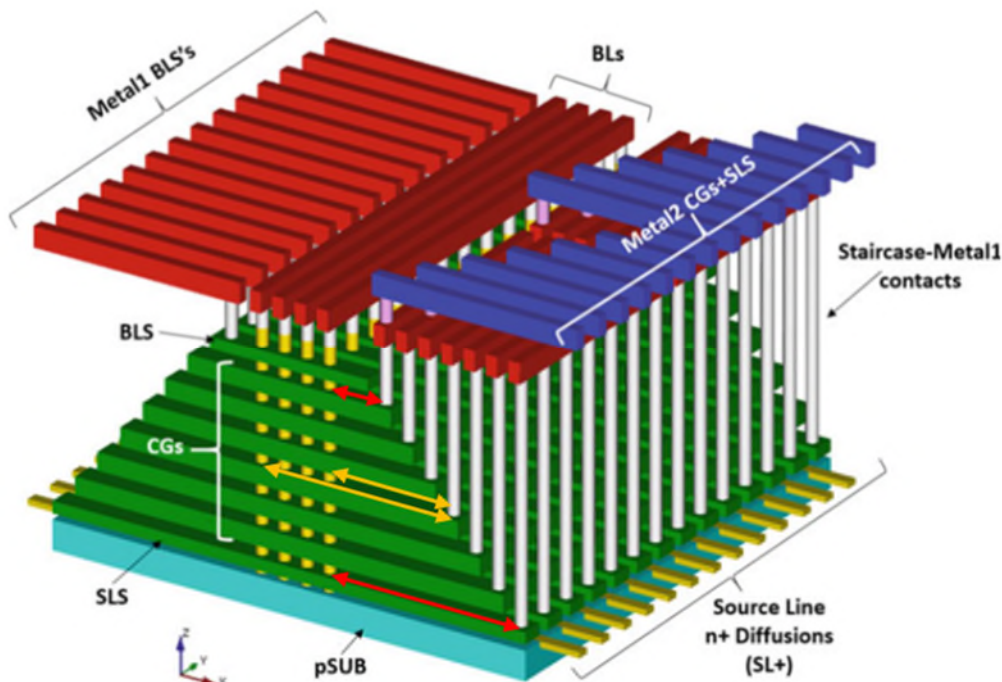
Ex. 1018, 81.

54. Under this correct understanding, the word line layer and the gate terminal are the same. They are the same conductor. And the voltage on a word line layer is developed across the entire layer essentially at the same time, that is, its timing and voltage level are the same across a word line layer. This is due to the insignificant resistance of the word line layers (typically formed of metal such as tungsten) relative to that of the word line decoder.

55. In this context, the word line layer voltages can be said to be developed from the output voltages of the voltage generating circuits. In other words, differences in timing or voltage level can exist between the outputs of voltage generating circuits and the corresponding word line layer voltages if not given sufficient time. The current supplied by the voltage generating circuits encounters resistance in the word line decoder to charge the capacitance between the word line or gate layer and the channel. This results in an RC delay between the output of

voltage generating circuits and the word line layer and is what I testified in the deposition of the IPR proceeding of U.S. Patent No. 11,501,822. See Ex. 2003 ¶ 95 (citing Ex. 2006 (Liu822 Tr.) stating “signal *takes time to go from the voltage generation circuit and be reinserted to the word line*, there would be a parasitic component that causes slight delay in charging the word line.”) (emphasis added in Ex. 2003). A patent cited by the Examiner during the prosecution of the ’957 patent confirms this: “there is an appreciable distance between the word line and the detector, resulting in RC delays.” Ex. 1030, 33:27-30.

56. Any significant RC delay across the word line layer as Dr. Przybylski alleges would create serious operational issues for flash devices that neither the ’957 patent nor prior art discusses. Specifically, memory strings at different locations of a word line plate would have different voltage/timing characteristics, as would different word lines of the same memory string. To illustrate, consider the physical layout of a 3D NAND flash:



Ex. 1018, 131 (red arrows added to illustrate delay paths from word line contacts to gate terminals of the same memory string, and orange arrows added to illustrate delay paths from one word line contact to gate terminals of two different memory strings).

57. As shown above, the word line layers of a channel have different dimensions. Because the cells of a memory string operate synchronously from top to bottom, for example, to turn on at the same time during a program or read/verify operation, if there is a significant RC delay from a vertical word line contact to the gate terminal as Dr. Przybylski alleges, memory cells on the same word line from one end of a memory string to the other end would have different voltage/timing characteristics. Similarly, memory strings are placed at different locations of the

word line plates and thus different strings would experience different RC delays under Dr. Przybylski's incorrect theory. Such different voltage/timing characteristics would create complications not discussed by the '957 patent or the prior art. For example, if the word line voltage is different from the gate voltage, then the NAND array will experience a complication in that the operational characteristics of the memory cells, such as programming, programming disturb, and threshold voltages, would all depend on the locations of their gate terminals and the respective, corresponding word line contacts. This dependency would create additional errors that the '957 patent or the prior art does not discuss or contemplate. Dr. Przybylski's deposition testimony confirms this. He testified that the RC time constant is "different for each memory cell on the word line" because "[e]ach memory cell is in a different physical location." Ex. 1031, 172:13-173:10, 209:19-210:22. He also testified that "RC delay is a complicated aggregation of distributed volt resistances and capacitances and a non-zero source resistance for the driver and a host of other factors," including "the actual physical layout of a specific 3D NAND Flash design." *Id.* 204:19-205:8, 164:19-165:11. He further testified that there are multiple RC time constants associated with each word line layer. *Id.*, 209:19-210:17. He testified that the RC time constants would depend on "[e]very physical aspect of the integrated circuit and the layers therein," "determined by a myriad of factors," resulting in "no simple algebraic representation of the waveform." *Id.*, 207:18-

208:17, 169:12-170:14. If his opinions were true, figuring out the RC delays experienced by each memory cell would be incredibly complicated, and the simple (in comparison) waveforms of the '957 patent and prior art references would be woefully inadequate to show how to apply voltages to a memory array to operate it.

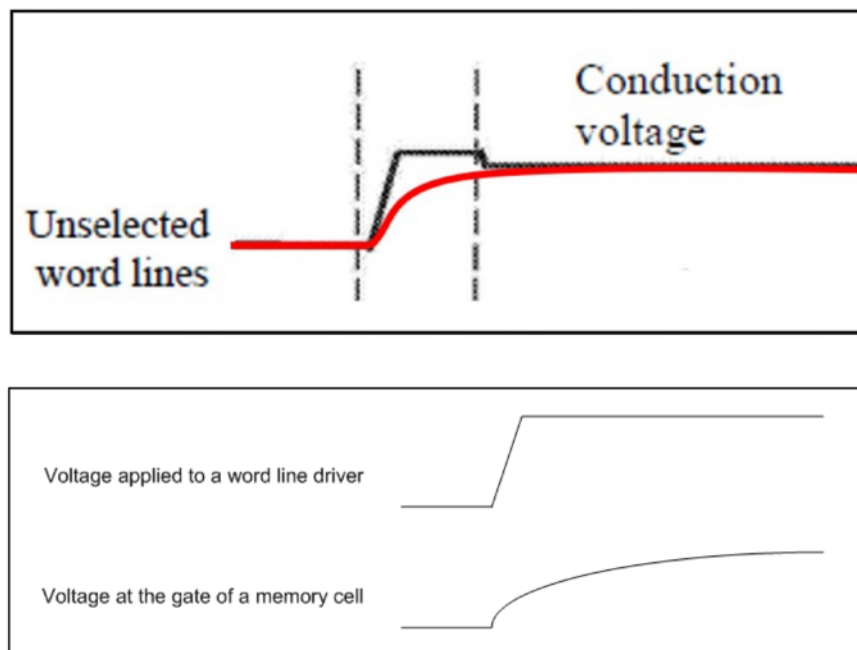
58. Instead, the focus of the literature is on what happens at the memory cells when voltages are applied to the word line layers. This focus is understandable because it is the behavior of the memory cells that is relevant to the operation of the memory device. Further, this focus is justified because voltages applied to the word line layers are voltages applied to the corresponding gate terminals, and it is the gate voltage that controls the operation of a memory cell transistor. For the same reason, waveforms illustrated in literature assume that the desired word line/gate voltage would timely reach the target value. This is why most figures in the '957 patent and in the prior art do not show curved waveforms, as I will show in more detail below.

59. In fact, the teaching of '957 patent only works if each of the word line layer is assumed to be at equipotential across the plate, without a RC delay, during the pre-verify stage. If there is a significant RC delay across a word line layer, as alleged by Dr. Przybylski (there is not), then it is possible that an unselected string close to the word line contact would develop the applied voltage much quicker than another string that is farther away from the word line contact. In such a case, decreasing the unselected word line voltage during the verify stage would create

rather than reduce channel potential gradient at certain memory strings. This is because the control gates of memory cells that are closer to the word line contacts and thus have gate voltages that are developed more quickly would have been pre-conditioned to 0V during the pre-verify stage, and the reduction in the bias voltage (applying 3.0V V_{pass2} instead of 6.8V V_{pass1} during verify stage, as shown in Figures 6 and 8) would couple the channel down to -3.8V ($V_{pass2} - V_{pass1}$). The goal of reducing the gradient of the channel potential (Ex. 1001, 14:19-30) would not be achieved since there will be a potential difference going from $WLn+1$ to $WL>n+1$ due to the channel potential going from a positive value to a negative value. In such a case, the only viable solution is to have a lengthy pre-verify period, thus nullifying the need of the teaching of '957 patent.

60. Dr. Przybylski argues that Hongtao's elevated pre-conduction voltage "appears to be a technique to reduce the time spent in the pre-conduction phase." Ex. 2003 ¶ 98. Preliminarily, this argument has no basis in Hongtao. *See id.* ¶¶ 97-99 (containing no citation to Hongtao). Furthermore, He opines that the RC time constant "depends on many factors," Indeed "a myriad [of] factors." *Id.* ¶ 94; Ex. 1031, 208:8-17. Yet he identifies not a single factor through which he generated the curved waveform overlaid on top of Hongtao's waveform, but the waveform conveniently has a curvature to allow it to reach the target level right around the start of the verify stage, and seemingly rather different from the curvature of the other

waveform he generated also without identifying any factor affecting the RC time constant:



Ex. 2003 ¶¶ 98, 94. Moreover, Dr. Przybylski does not explain how an RC time constant and an elevated pre-conduction voltage level might be determined or controlled to achieve the desired curvature for shortening the pre-conduction phase while simultaneously reaching the target conduction voltage at the start of the verify stage. Neither does Hongtao, because Hongtao does not disclose or suggest the alleged technique. And without such teaching, it is more likely to overshoot or undershoot the target conduction voltage level. A POSITA would not have found it reasonable for Hongtao to employ such a technique without teaching the means to achieve it.

61. Indeed, Dr. Przybylski's alleged technique is simply impractical. If an RC delay exists across a word line layer as he argues, then different word line layers of the staircase structure would experience different RC delays due to each layer's different dimension. Ex. 1031, 209:19-210:13 (his testimony that each memory cell would have a different RC delay). His alleged technique would require determining a right combination of an elevated pre-conduction voltage level and an RC time constant for each layer. That would be a monumental task, to say the least. Further, he testified that "there may be differences ... not evident within these figures of Hongtao." *Id.*, 211:1-4. In other words, what Hongtao discloses is not enough to determine RC delays. I understand that deficiency would create legal issues for patent publications such as Hongtao.

62. Further, because Dr. Przybylski takes a demonstrably wrong position, his arguments lead to inconsistencies and involve mischaracterizations.

63. First, his position cannot be reconciled with his claim construction of the top/bottom bias voltage limitations because his RC delay argument would result in different voltage levels in the pre-verify and verify stages. *See supra* § II.A. Additionally, he cites Figure 7 to support his claim construction argument. The construed terms recite "apply[ing] a ... voltage on a gate terminal." Ex. 2003 ¶ 53. But Figure 7 shows waveforms with "steep slew rates ..., straight lines, and sudden changes," which according to his argument are not gate voltages. *Id.* ¶ 96; Ex. 1031,

222:18-223:19. Dr. Przybylski also argues for his claim construction of gate terminal voltages by referring to TSG/BSG voltage level “administered to the [TSG/BSG] layer.” Ex. 2003 ¶ 50. But the ’957 patent does not support distinguishing the word line layers, TSG layers, and BSG layers in terms of their RC delay characteristics. See Ex. 1001, 8:2-8; Ex. 1031, 76:17-77:5.

64. Second, Dr. Przybylski’s arguments repeatedly mischaracterizes the ’957 patent. One, to support its “gate terminal” argument, he repeatedly relied on passages that don’t even contain the word “gate.” See, e.g., Ex. 2003 ¶¶ 90, 155, 162 (citing Ex. 1001, 11:68 [sic]-12:9 and 12:10-27). Similarly, he cites a passage that does not mention “gate terminal” to argue for “selectively applying different voltages to the gate terminals of the selected memory cell and other not-programmed memory cells during each stage.” *Id.* ¶ 32 (citing Ex. 1001, 7:13-32). Two, he cites portions that say nothing about voltages “develop[ing]” on the gate to allege otherwise. *Id.* ¶ 37 (citing Ex. 1001, 1:58-2:8, 6:37-49). Three, he cites portions that are not part of Figure 6 description to characterize Figure 6. *Id.* (citing Ex. 1001, 6:37-49 (describing “a related example” in which “the pass voltage [is] sustained further through the verify/read scheme at unselected WLs....”). Four, he cites passages disclosing “applied on word lines” (or similar) to argue that the “voltages applied ‘on a gate terminal.’” *Id.* ¶¶ 33, 37, 155 (citing Ex. 1001, 6:37-49). Dr.

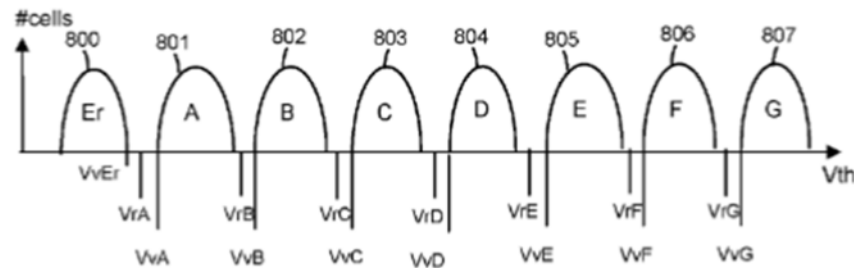
Przybylski's loose interpretation/application of the '957 patent is contradicted by what the patent actually discloses as I explain herein.

65. Third, Dr. Przybylski's arguments mischaracterizes Aritome. Aritome discloses guideline for minimizing RC delay of word lines, which Dr. Przybylski ignores but which a POSITA would have known to follow. See Ex. 1014, 369. Additionally, Aritome discloses that the estimated RC delay of 3D cells is around twice as large as that of 2D cells. *Id.* at 370 (1/4 resistance and 8 times capacitance). Aritome further discloses means to reduce RC delay, e.g., low-k dielectric or air gaps between word lines, to below the 2x factor. *Id.* at 370. Thus, Dr. Przybylski's selective excerpt of Aritome of "greatly increased" "WL capacitance" ignores the full disclosure and appears to be designed to at least create a distorted perception of the RC delay of 3D memory versus 2D memory. See Ex. 2003 ¶¶ 28, 58, 94. Moreover, Aritome does not at all refer to "gate" or "gate terminal" in its discussion. Ex. 1014, 369-72. Instead, Aritome shows curved "[s]imulated waveform of a word-line (WL) signal in a 3D V-NAND array." *Id.* at 372. For these reasons, Aritome does not support Dr. Przybylski's RC delay or curved waveform arguments.

B. Read Operations At Least Render Obvious Verify Operations

66. The read and verify operations are "virtually identical" operations. Ex. 1003 ¶ 189. Specifically, a verify operation is a read operation executed after a program operation. *Id.* ¶ 192. All that is required is to slightly adjust the read

voltage to generate the verify voltage. *Id.* ¶ 193. For example, in the figure below, V_{rA} - V_{rG} denote the read voltage levels, and V_{vA} - V_{vG} denote the corresponding verify levels:



Ex. 1017, Fig. 8A; 15:15-21. Each read voltage level is slightly lower than the corresponding verify voltage level to provide margin for down-shifting of voltage distribution curves that occurs after the memory is programmed and verified. The verify operation applies a tighter voltage distribution. Verification failure results in re-programming to bring the threshold voltage of the selected memory cell to within the tighter distribution. But as I opined before, “[s]etting different voltage levels for read and verify operations was a routine practice.” Ex. 1003 ¶ 193.

67. My opinion is supported by the ’957 patent and the prior art.

68. The ’957 patent claims “[a]n apparatus for **reading** a memory device....” Ex. 1001, claim 1. The same wording appears in the patent specification. The summary consistently describes, as an “aspect of the disclosure, a method [or an apparatus] for reading a memory device.” *Id.*, Abstract, 1:50-51, 2:64-65, 4:12-13. These aspects of the disclosure, like claim 1, involve pre-verify and verify

stages. *Id.*, Abstract, 1:50-2:8, 2:64-3:23, 4:12-36. Furthermore, Figure 10, which contains language virtually verbatim to that in claim limitations [1.A.i]-[1.A.iv] (apart from immaterial verb tenses and a conjunction), is introduced as “a flow chart diagram of a method 1000 for **reading** a memory device including a first memory cell string and a second memory cell string.” *Id.*, 15:31-33 (emphasis added). Moreover, the same sentence equating gate terminal with gate also equates read with verify. *Id.*, 9:41-44 (“In addition, a **read (or verify)** voltage can be applied on the **gate terminal (or gate)** of the selected memory cell MCn through a WL layer (e.g., WLn) that is coupled to the selected memory cell MCn.”). A POSITA would have no doubt that this sentence equates gate terminal with gate because the two are the same in common parlance. Therefore, a POSITA would understand the ’957 patent to be equating read and verify in that same sentence. These passages also reflect the fact that the inventors considered reading and verifying to be interchangeable in the context of the patent. Dr. Przybylski himself used the term “read verify operations” when answering a question about how read operations works. Ex. 1031, 81:2-82:4. That is consistent with how a POSITA would have considered read and verify operations, that is, a verify operation is a read operation.

69. A POSITA’s knowledge as reflected in the prior art also supports my conclusion. My original declaration cited prior art to demonstrate that using a read operation to perform verification would at least have been obvious. Ex. 1003,

¶¶ 187-95. I offer additional explanation below in response to Dr. Przybylski's arguments.

70. Both read and verify operations may be described as a sensing operation with the only difference being the reference voltage. Ex. 1017, Fig. 13, 20:40-22:57 (describing using the same flow chart a sensing operation that may be either a verify or a read operation); *see also* Ex. 1008, [0096], Fig. 14 (applying the same process to either read or verify operation in step 702).

71. Moreover, because of the operations are analogous, the words are used interchangeably. For example, Costa refers to "Vread" for verify operations. Ex. 1008, Figs. 10, 11, 16A-16B.

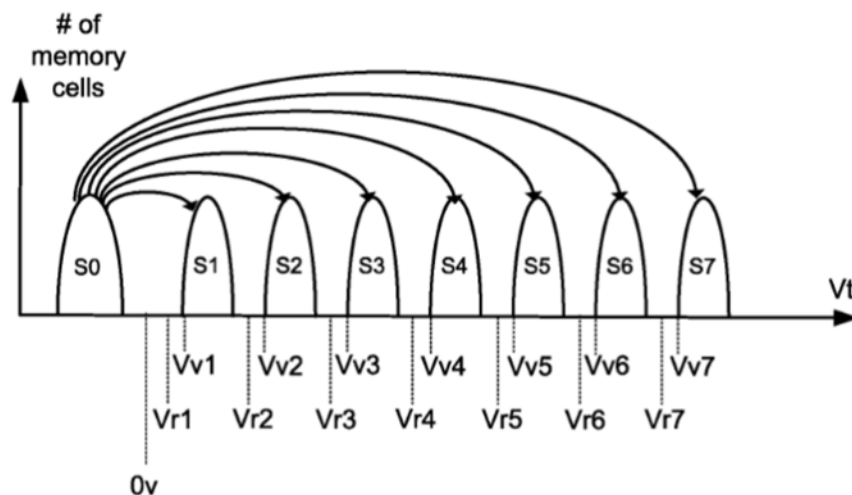
72. I describe above that it was routine to set different voltage levels for read and verify operations. Consistent with that, Yu uses the same voltage generator to generate voltages for read and for verify operations. Ex. 1006, [0054]-[0055]. Dr. Przybylski agrees that the same voltage generators are used to generate voltages to control both operations. Ex. 1031, 101:13-22, 102:18-104:4. Further, Costa teaches adjusting voltages for verify operations alone. Ex. 1008, Figs. 5, 7B-7E. It would have been obvious and well within a POSITA's knowledge to adjust verify voltages to read voltage levels, or vice versa.

73. Dr. Przybylski argues that Hongtao's read operations does not render obvious the verify operation of the '957 patent. I disagree. The same argument that

the two are virtually identical operations or that one is at least obvious based on the other also rebuts his alleged lack of motivation to combine Hongtao and Yu for a verify operation. He also argues that read and verify operations are different because a lower read pass voltage “can be used” on unprogrammed memory cells when performing verify operations because such cells have known locations. Ex. 2003 ¶ 82. I disagree. As his “can” language indicates, there is no technical requirement that verify operations use a read pass voltage on unprogrammed memory cells lower than the read pass voltage on programmed cells. For example, as Suzuki’s Figure 11 shows, its verify operation uses a single read pass voltage on all unselected memory cells WL_{usel}. Ex. 1007, Fig. 11. Further, the ’957 patent does not impose such a requirement either. All that the claims require is that the second bias voltage is lower than the first bias voltage (both voltages applied on unprogrammed memory cells). Relatedly and for completeness, claim 4 requires that the second gate voltage applied on unselected TSG during the verify stage be smaller than either second pass voltage or the second read voltage applied on a memory cell adjacent to the selected cell during the same stage. But none of the claims specify any relative magnitude between unprogrammed versus programmed memory cells during either pre-verify or verify stage.

74. Dr. Przybylski’s citations do not show otherwise. One reference actually supports my opinion that a verification operation is a type of read operation.

Ex. 1021, [0103] (cited in Ex. 2003 ¶ 81) (“the read operation may include the verification read operation for verifying the success of the program operation or the normal read operation for determining the data stored in the memory cells.”). This disclosure clearly discloses that a verify operation is one type of read operation. Another reference confirms that the two differ merely in the read/verify voltage levels. Ex. 1020, 16:16-23 (cited in Ex. 2003 ¶ 81). This is shown below:



Id., Fig. 12. This figure is similar to Figure 8A of Ex. 1017 I used above to explain that the two operations are virtually identical. The remaining references Dr. Przybylski cited confirm that both read and verify are sensing operations. Ex. 1017, 3:21-22; Ex. 1019, 24:63-25:8.

C. Hongtao’s Two Phases Correspond to the Pre-Verify and Verify Stages

75. Dr. Przybylski argues that Hongtao’s pre-conduction and read phases do not necessarily correspond to pre-verify and verify stages of the ’957 patent,

respectively. Ex. 2003 ¶ 84. I disagree. Other than repeating his “read is not verify” arguments and misapplying the Board’s statement regarding Ground 3, Dr. Przybylski provided no substantive explanation to support his argument. *Id.*

76. As I explained in my original declaration, Hongtao’s pre-conduction phase prepares for the sensing operation occurring in the read phase by pre-conditioning the channels to reduce HCI. Ex. 1003 ¶¶ 71-72, 75. I further explained that Hongtao’s pre-conduction voltage serves the same function as the first verify voltage of the ’957 patent. *Id.* ¶ 105. Dr. Przybylski did not rebut any of my arguments.

D. Hongtao At Least Renders Obvious Claims 5 and 6

77. Dr. Przybylski argument against claims 5 and 6 relies on his wrong claim construction. Under a correct claim construction, Hongtao in view of Yu renders obvious claim 5 and 6 as explained in my original declaration. *See supra* § II.A.

78. Dr. Przybylski alleges an inconsistency in identification of the “first adjacent memory cell” and the “not programmed memory cell” in the Petition. Ex. 2003 ¶ 56. That is a straw man argument. Claim 2 requires the “not programmed cell,” which “receives the first bias voltage and the second bias voltage [be] positioned between the first adjacent memory cell ... and the TSG.” Claim 1 permits the two to be the same memory cell. Accordingly, I correctly identified the first

adjacent memory cell as an unprogrammed cell for claim 1 (Ex. 1003 ¶ 102) and identifies different cells for the two for claim 2 (*Id.* ¶ 123).

IV. GROUND 2

A. Suzuki Discloses a First Bias Voltage in a Pre-Verify Stage

79. Dr. Przybylski disputes that Suzuki discloses a first bias voltage in a pre-verify stage. He argues that Suzuki's pre-verify stage does not start at time t3, after the programming operation is completed. I disagree.

80.

81. Suzuki discloses three sequential operations: program, recovery, and verify. Ex. 1007, [0146]. The program operation injects charges into the charge storage layer to change the threshold voltage of the cell being programmed. *Id.*, [0135]. The verify operation senses the charged stored in the storage layer. *Id.*, [0144]. The recovery operation occurs between program and verify. It is clear that the program operation is completed when WLsel starts to decrease from VPGM at time t3. As the Board recognized, the recovery operation combines an end operation of the program operation and the ready operation of the verify operation. ID, 20. That corresponds to the pre-verify stage of the '957 patent.

82. Specifically, for the program operation from t0 to t3, the ramping up of WLsel voltage from low VSS to intermediate VPASS and finally to high VPGM is part of the programming operation to facilitate a disturb free operation, because "an

increase in threshold voltage of the memory cell transistor MP within other NAND strings NS is suppressed because the difference in voltage between the channel and the control gate has been reduced by the self-boost.” Ex. 1007, [0134]-[0135]. Similarly, during the recovery operation (pre-verify stage) that takes place after the program operation, the ramping down of WLsel voltage from high VPGM to intermediate VPASS during t3 to t4 (followed by a further decrease to low VCGM) is part of the recovery operation to facilitate a disturb free recovery of the channel of the memory strings since it results in that “electrons remaining inside the channel of the NAND string NS coupled to the bit line BLprog are pulled out to the bit lines BL.” *Id.*, [0140]. In other words, t1 to t2 is part of the program operation to ensure the program operation can be achieved with minimal disturb, and t3 to t4 is part of the recovery operation to ensure the recovery operation can be achieved with minimal disturb. Both periods are a critical part of their respective operations. Therefore, t3 to t4 belongs to the recovery operation (i.e., pre-verify stage) that prepares for the verify operation (i.e., verify stage).

B. Suzuki Discloses Claims 5 and 6

83. Dr. Przybylski’s argument is basically the same as that in Ground 1. Ex. 2003 ¶ 139. Thus, Suzuki discloses claims 5 and 6 under the correct claim construction. *See supra* § III.D.

V. GROUND 3

84. Preliminarily, Dr. Przybylski's arguments against the two references individually are just straw-man arguments. *See, e.g.*, Ex. 2003 ¶¶ 156-57. I opined that Costa and Seo together rendered the claims of the '957 patent obvious, not that either reference discloses all claim elements.

A. Costa and Seo Render Obvious Applying Voltages on Gate Terminals

85. Dr. Przybylski's argument against claim 1 is the same as in Ground 1, that voltages on word lines are not voltages on gate terminals. Ex. 2003 ¶ 153. This is a fabricated argument. *See supra* § III.A.

B. A POSITA Would Have Had Motivation and Reasonable Expectation of Success to Combine Costa and Seo

1. Combining Costa's Verify Operation and Seo's Read Operation Would Have Been Obvious

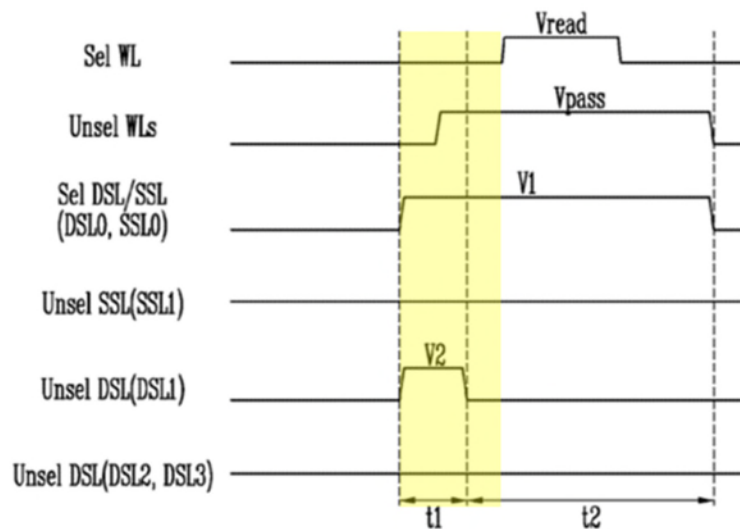
86. Dr. Przybylski's first argument against motivation to combine appears to be that Costa discloses verify operations while Seo discloses read operation. Ex. 2003 ¶¶ 148-50. This is a nonissue because read and verify operations are virtually identical and one is obvious in view of the other. *See supra* § III.B.

2. Seo's Time Periods Correspond to the Two Stages, and Costa's Sensing Phase Corresponds to the Verify Stage

87. With the correct understanding that read and verify operations are virtually identical, it would have been obvious that Seo's two time periods correspond to pre-verify and verify stages of the '957 patent because a POSITA

would have recognized that verification takes place during period t2 when Vread is applied to Sel WL and Vpass is applied to Unsel WLs, and voltages applied in period t1 conditions the channel to reduce HCI before the read operation. Ex. 1003 ¶ 89.

88. As a side note, because it is undisputed that the claims do not require “applying the[] voltages throughout the given stage” (Ex. 2003 ¶ 46), period t1 may be expanded up to the width shown below and still satisfy the requirements for the pre-verify stage of the ’957 patent:



Ex. 1009, Fig. 8. In other words, the verify stage may begin when or before the voltage on the selected word line is raised to Vread, the level that allows current sensing for the verify operation to be performed. *Id.*, [0084]. The pre-verify stage ends when the verify stage begins.

89. Relatedly, Costa’s “sensing phase” corresponds to time period t2 of Seo and the verify phase of the ’957 patent. Costa’s sensing phase is set up such that all

memory cells except the selected cell is turned on via a pass voltage, and the channel is turned on or off depending on the reference voltage V_{cgr} applied to the selected cell relative to its threshold voltage. Ex. 1008, Abstract (“During sensing, a selected memory cell receives a reference voltage while the remaining memory cells receive a read or verify pass voltage.”); *see also id.*, Fig. 12H, [0098]-[0099], [0147] (“In FIG. 12H, WL28 in Zone 7 is selected for verification and receives V_{cgr} .”); *id.*, [0138] (“FIGS. 12A-12H are cross-sectional views of an example of a NAND string depicting the bias conditions for the NAND string *during program verification.*”) (emphasis added); *id.*, [0023] (“FIGS. 12A-12H are cross-sectional views of an example of a NAND string depicting bias conditions for verifying programming....”). It is plain that Costa’s verify operation only has, and corresponds to, the verify stage.

3. Lowering Seo’s Vpass During the Verify Stage Would Have Been Obvious Based on Costa

90. I opined that it would have been obvious to lower Seo’s voltage applied on the unselected word lines during the verify stage. Ex. 1003 ¶ 308. I will further explain that opinion below.

91. To begin, both Costa’s V_{read} and Seo’s V_{pass} serve the same function of turning on the corresponding unselected memory cells. “[Costa’s] V_{read} is a voltage that is higher than any threshold voltage to which a memory cell may be programmed. This may ensure that unselected memory cells and other elements of

the string are conductive during sensing. Vread acts as an overdrive voltage because it causes the unselected storage elements to turn on and act as pass gates.” Ex. 1008, [0096]. Seo’s Vpass is applied on unselected word lines “during the read operation.” Ex. 1009, [0049]. A POSITA would have understood Vpass to be a voltage needed to turn on the unselected cells during read operation because this was conventional for read/verify operations. And Seo confirms it by teaching that the local boosting phenomenon that may occur when the unselected cells are turned on by Vpass is minimized “because the source select transistor SST and the drain select transistor DST are turned on,” thereby reducing any channel potential gradient that may occur in the conductive channel. *Id.*, [0089]. Therefore, in the verify stage of the combination, Costa’s Vread corresponds to Seo’s Vpass. A POSITA would have at least found it obvious to use the same voltage level for both because of this correspondence.

92. Seo does not address the lower threshold voltage of unprogrammed cells but applies a single Vpass level on all unselected memory cells. Thus, as was well known and disclosed by Costa, Vpass must have a value high enough “to ensure that [all] memory cells[, including unselected programmed cells,] are conductive and appropriately act as pass gates.” Ex. 1008, [0096]. Seo’s Vpass is equivalent to Costa’s “standard read pass voltage Vread” because Vread is also a voltage level that would turn on all unselected cells. *Id.*, [0121].

93. Costa teaches that Vread should “generally be set as low as possible” “[t]o limit read disturb on unselected word lines during sensing.” *Id.*, [0096]. A POSITA would have understood that this teaching applies to Seo’s Vpass in the combination because their correspondence. Further, a POSITA would have recognized that limiting read disturb is generally desirable for flash devices and thus would have found it obvious to set the pass voltage during the verify stage as low as possible based on Costa’s teaching. Costa identifies VreadL applied to unselected word lines as “a lower read pass voltage” that is, for example, “several millivolts less (e.g., 5.2V) than the standard read pass voltage Vread.” *Id.*, [0121]-[0122]. So VreadL is a second bias voltage smaller than Vread or, equivalently, a POSITA would have found it obvious to reduce Seo’s Vpass during the verify stage.

94. As I opined in my original declaration, a POSITA would have found it obvious to lower Seo’s Vpass only during the verify stage. Ex. 1003 ¶ 308. Seo applies a low voltage to the selected memory cell during the pre-verify stage, thus turning the memory cell off. Ex. 1009, Fig. 8. Thus, there is not a conductive channel across the selected memory cell, and the source terminals of the cells above the selected cell are floating and their voltages increase. Because the threshold voltage is compared against the gate voltage relative to the source voltage, keeping the gate voltage high when the source voltage increases ensures the memory cell transistors would remain above the threshold voltage and turn on as intended,

whether the memory cell is programmed or unprogrammed. Ex. 1003 ¶ 107; Ex. 1031, 87:1-15 (Dr. Przybylski agreeing that threshold voltage is defined by (gate voltage - source voltage)). This does not significantly increase HCI because the pre-verify period is short. On the other hand, lowering the gate voltage level to below V_{pass} has the risk that the gate voltage relative to the floating source terminal may not be higher than the threshold voltage needed to turn on the unselected memory cells. That would compromise Seo's goal to reduce HCI-induced read disturb on unselected memory strings.

95. Dr. Przybylski alleges without any support or explanation that the combination "contradicts ... the basic principles behind how NAND memory strings operate." Ex. 2003, ¶ 153. I can think of no basic NAND memory operational principles that the combination contradicts. Neither does he provide a substantive explanation based on basic NAND memory operational principles why Costa's teaching "would be equally applicable in both time period t1 and time period t2." *Id.* ¶ 159. I did so in my original declaration and above.

96. In any event, there are only two realistic options for the V_{read} level during the pre-verify stage, either keeping it at the standard level or lowering it to the same level as Costa teaches for the verify stage. For example, a POSITA would have found it obvious to not increase the V_{read} level based on Costa's teaching and

a POSITA's knowledge that higher gate voltages usually cause more undesirable effects such as disturbs. These two options would have been obvious.

97. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: April 25, 2025

Location: Fremont, California

Signature: 
DR. DAVID KUAN-YU LIU